Protection and Fault Location Schemes Suited to Large-Scale Multi-Vendor High Voltage Direct Current Grids

PhD Thesis

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This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

Signed: Vasileios Psaras
Date: 9/11/2021

Abstract

Recent developments in voltage source converter (VSC) technology have led to an increased interest in high voltage direct current (HVDC) transmission to support the integration of massive amounts of renewable energy sources (RES) and especially, offshore wind energy. VSC-based HVDC grids are considered to be the natural evolution of existing point-to-point links and are expected to be one of the key enabling technologies towards expediting the integration and better utilisation of offshore energy, dealing with the variable nature of RES, and driving efficient energy balance over wide areas and across countries. Despite the technological advancements and the valuable knowledge gained from the operation of the already built multi-terminal systems, there are several outstanding issues that need to be resolved in order to facilitate the deployment of large-scale meshed HVDC grids. HVDC protection is of utmost importance to ensure the necessary reliability and security of HVDC grids, yet very challenging due to the fast nature of development of DC faults and the abrupt changes they cause in currents and voltages that may damage the system components. This situation is further exacerbated in highly meshed networks, where the effects of a DC fault on a single component (e.g. DC cable) can quickly propagate across the entire HVDC grid.

To mitigate the effect of DC faults in large-scale meshed HVDC grids, fast and fully selective approaches using dedicated DC circuit breaker and protection relays are required. As the speed of DC fault isolation is one order of magnitude faster than typical AC protection (i.e. less than 10 ms), there is a need for the development of innovative approaches to system protection, including the design and implementation of more advanced protection algorithms. Moreover, in a multi-vendor environment (in which different or the same type of equipment is supplied by various manufacturers), the impact of the grid elements on the DC fault signature may differ considerably from case to case, thus increasing the complexity of designing reliable protection algorithms for HVDC grids. Consequently, there is a need for a more fundamental approach to the design and development of protection algorithms that will enable their general applicability. Furthermore, following successful fault clearance, the next step is to pinpoint promptly the exact location of the fault along the transmission medium in

an effort to expedite inspection and repair time, reduce power outage time and elevate the total availability of the HVDC grid. Successful fault location becomes increasingly challenging in HVDC grids due to the short time windows between fault inception and fault clearance that limit the available fault data records that may be utilised for the execution of fault location methods.

This thesis works towards the development of protection and fault location solutions, designed specifically for application in large-scale multi-vendor HVDC grids. First, a methodology is developed for the design of travelling wave based non-unit protection algorithms that can be easily configured for any grid topology and parameters. Second, using this methodology, a non-unit protection algorithm based on wavelet transform is developed that ensures fast, discriminative and enhanced protection performance. Besides offline simulations, the efficacy of the wavelet transform based algorithm is also demonstrated by means of real-time simulation, thereby removing key technical barriers that have impeded the use of wavelet transform in practical protection applications. Third, in an effort to reinforce the technical and economic feasibility of future HVDC grids, a thorough fault management strategy is presented for systems that employ efficient modular multilevel converters with partial fault tolerant capability. Finally, a fault location scheme is developed for accurately estimating the fault location in HVDC grids that are characterised by short post-fault data windows due to the utilisation of fast acting protection systems.

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List of Abbreviations

AC	Alternate Current
ACCB	Alternate Current Circuit Breaker
AMR	Anisotropic Magneto-Resistance
CGC	Central Grid Controller
CH-MMC	Customised Hybrid Modular Multi-level Converter
CNN	Convolutional Neural Network
CSoTW	Cosine Similarity of Travelling Waves
CLI	Current Limiting Inductor
CT	Current Transformer
CWT	Continuous Wavelet Transform
DC	Direct Current
DCCB	Direct Current Circuit Breaker
DSP	Digital Signal Processor
DRTS	Digital Real Time Simulator
DWT	Discrete Wavelet Transform
EEMD	Ensemble Empirical Mode Decomposition
EMD	Empirical Mode Decomposition
EML	Extreme Machine Learning
FB-SM	Full-Bridge Sub-Module
FB-MMC	Full-Bridge Modular Multi-level Converter
FB	Full-Bridge
FDA	Frequency Domain Analysis

FIR	Finite Impulse Response
FMS	Fault Management Strategy
FPGA	Field-Programmable Gate Array
FT	Fourier Transform
GA	Genetic Algorithm
GMR	Giant Magneto-Resistance
GPS	Global Positioning System
GTO	Gate Turn-Off Thyristor
H-MMC	Hybrid Modular Multi-level Converter
HB-SM	Half-Bridge Sub-Module
HB	Half-Bridge
HB-MMC	Half-Bridge Modular Multi-level Converter
HHT	Hilbert-Huang Transform
HIL	Hardware In-the-Loop
HPF	High-Pass Filter
HVAC	High Voltage Alternate Current
HVDC	High Voltage Direct Current
IDWT	Inverse Discrete Wavelet Transform
IED	Intelligent Electronic Device
IGBT	Insulated Gated Bipolar Transistor
LCC	Line Commutated Converter
LCS	Load Commutation Switch
LPF	Low-Pass Filter
MC-MMC	Mixed-Cell Modular Multi-level Converter
MC	Mixed-Cell
MM	Mathematical Morphology
MMC	Modular Multi-level Converter
MOA	Metal Oxide Arresters

MR	Magnetoresistors
NLM	Nearest-Level Modulation
NPC	Neutral-Point Clamped
OC	Over-Current
OHL	Overhead Line
OP	Operational Amplifier
OWP	Offshore Wind Plant
PCC	Point of Common Coupling
PI	Proportional Integral
PLL	Phase-Locked Loop
PTG	Pole-to-Ground
PTP	Pole-to-Pole
PWM	Pulse Width Modulation
QMF	Quadrature Mirror Filter
RCD	Residual Current Device
RMSE	Root Mean Square Error
ROCOV	Rate of Change of Voltage
ROTV	Rate of Transient Voltage
RT-BSWT	Real-Time Boundary Stationary Wavelet Transform
SA	Surge Arresters
SM	Sub-Module
SNR	Signal-to-Noise Ratio
SPWM	Sinusoidal Pulse Width Modulation
SRIV	Simplified Refined Instrument Variable
SVM	Support Vector Machine
SWT	Stationary Wavelet Transform
TMR	Tunnelling Magneto-Resistance
TW	Travelling Wave

TWD	Travelling Wave Differential
UFD	Ultra-Fast Disconnector
UV	Under-Voltage
VSC	Voltage Source Converter
WMM	Wavelet Modulus Maxima
WT	Wavelet Transform
XLPE	Cross-Linked Polyethylene

Chapter 1

Introduction

1.1 Research Context

The global electric power grids are experiencing a significant transition phase driven by the increasing electricity demands and the requirements for more efficient energy use and higher security of power supply. In addition, in an effort to address the climate crisis, several governments across the world have committed themselves to de-carbonising the electric power system and increasing renewable energy penetration. This trend has been supported by a plethora of laws, policies and directives, of which the primary aim is to reduce greenhouse gas emissions arising from electricity generation [1–3]. Recently, the European Union has set a 55% gas reduction target by 2030 by revising its renewable energy and energy efficiency targets with the ultimate aim of achieving climate carbon neutrality by 2050 [3]. Considering the resource availability of renewable energy sources for large power generation, harnessing the massive potential of wind energy is seen as a key enabler for achieving such ambitious goals [4]. Nevertheless, by increasing the share of renewable energy generation in the total energy mix, bridging the gap between electricity demand and supply is becoming more challenging, leading to an ever-greater need for growth of interconnection capacity between different regions and countries. Moreover, the spatio-temporal variability of wind energy highlights the necessity for more efficient, safer, high-power and long-distance transmission over harsher environments. Especially modern wind farms tend to be installed further and further offshore and consequently, longer undersea electrical connections are necessary.

High Voltage Direct Current (HVDC) transmission system technology has proven to be a viable economic solution for the integration of remote wind farms and the interconnection of AC systems [5]. High Voltage Alternate Current (HVAC) transmission is associated with higher electrical losses and capital costs as transmission distance increases and therefore, there is a critical distance beyond which the alternative option of

HVDC becomes more efficient and economical [6]. This is especially true for submarine power transmission, where HVAC becomes impractical due to the requirement for compensation systems at various points across the cables to cope with the reactive power demands. Moreover, when compared to HVAC transmission, HVDC transmission introduces several advantages such as the capability for bulk power transmission over longer distances, interconnection of asynchronous AC networks, reduced right-of-way, greater stability benefits, and power flow controllability [6, 7]. The difficulties in realising multi-terminal connections and the limited flexibility of the widely used for several decades Line Commutated Converter (LCC) technology have been addressed by the advent of Voltage Source Converters (VSC), which are capable of providing black-start capability, independent active and reactive power controllability, voltage support and connection to weaker AC networks [8, 9].

To date, the vast majority of HVDC projects are point-to-point connections comprising of two converter terminals. HVDC grids are conceived to be the natural evolution of point-to-point links by deploying more than two station terminals (potentially by using existing links), ultimately leading to highly meshed HVDC systems. HVDC grids can further improve the cost-effectiveness of HVDC technology, smooth energy variations of renewable energy sources, expedite the integration and better utilisation of offshore energy, and drive energy balance over wide areas and across countries [5, 10]. Moreover, VSC-based HVDC grids offer a plethora of additional attractive features such as enhanced controllability, flexibility and redundancy, improved reliability and security, lower investment costs, etc [6].

Various concepts for setting up highly meshed HVDC grids have been proposed to interconnect AC systems internationally or even inter-continentally [11–17]. This interest is also reflected in several European projects such as the TWENTIES [18], MEDOW [19], Best Paths [20], and PROMOTioN [21] projects which are focused around removing techno-economic and regulatory barriers blocking the implementation of HVDC grids in Europe. Currently, a few multi-terminal pilot projects have been developed in China such as the Nan'ao three-terminal system [22], the Zhoushan five-terminal system [23], and the Zhangbei four-terminal system [24] which is the only meshed HVDC grid currently in operation. Multi-terminal systems are also under development in Europe including the Moray Firth offshore HVDC hub in Scotland [25], and the system that will be formed by the EuroAsia and EuroAfrica interconnectors [26, 27] in the Mediterranean sea. It is therefore evident that the HVDC grid concept is gradually becoming a reality and that such grids are expected to play a key role in future power networks.

Despite the technological advancements and the valuable knowledge gained from the operation of the existing multi-terminal systems, there are several outstanding issues

that need to be resolved in order to facilitate the deployment of large-scale meshed HVDC grids. These issues concern aspects related to control, protection, operation, regulation, financing, planning and modelling of HVDC grids [6]. The work conducted in this thesis focuses around the challenges arising from DC faults, especially in terms of HVDC grid protection and fault location.

1.2 Motivation of the Work

Effective protection systems and DC fault management are considered to be of utmost importance towards the practical realisation of VSC-based HVDC grids [28]. This is due to the fact that DC faults can place HVDC grids and their components under severe stresses for which they are not designed to withstand. For instance, pole-to-pole faults result in the collapse of DC voltages and in high over-currents that may damage the sensitive components of the system, such as the power electronics devices of the VSCs which cannot tolerate high fault currents. Therefore, protection systems are necessary in order to isolate the faulted component promptly, guarantee safety of the HVDC grid components, and minimise the severe consequences of DC faults.

The main challenges of DC fault management arise from the short available time windows for fault clearance due to the fact that DC faults develop very rapidly. When a DC fault occurs in a cable or an overhead line of a HVDC system, abrupt changes in currents and voltages are provoked, leading to the generation of electromagnetic waves at the fault point. These electromagnetic waves, which are also termed travelling waves, propagate at high-speed along the medium to both directions until they reach a discontinuity point such as a converter, a DC busbar, an inductor etc [29]. For instance at a converter terminal, part of the incident wave is reflected back to the fault location and part of it is transmitted to other feeders connected at the same terminal. This process is repeated at each discontinuity point and consequently, the impact of DC fault is quickly evident across the entire HVDC grid. This highlights the necessity for the development of novel approaches to system protection as the speed of DC fault isolation is required to be one order of magnitude faster than typical AC protection [30].

Rapid DC fault isolation in large-scale meshed HVDC grids is expected to be realised through the use of DC Circuit Breakers (DCCBs) in conjunction with protection relays at each end of all transmission mediums of the grid. Based on this fully selective approach, when a protection relay identifies a DC fault on the medium that it is designated to protect, it sends a trip signal to its associated DCCB. Furthermore, only the DCCBs of the faulted medium are required to be opened in an effort to permit the operation of the remaining healthy part of the grid. To enable such high-speed and selective fault isolation, careful design of fast, robust and discriminative protection

algorithms is required. To meet the demanding time-scales, protection algorithms are preferred to be based exclusively on local voltage and current measurements at the relaying point, thus eliminating the need for telecommunication between different relays [31]. These aims have led to a significant research activity in developing non-unit protection algorithms based on travelling wave principles. Typically, these algorithms are designed and validated based on offline electromagnetic transient simulation studies performed on a single test network. This practice questions the universal applicability of the developed algorithms to any HVDC network. Moreover, due to the absence of a common framework for the design of non-unit protection methods, their functional interoperability in terms of operation performance and compliance with speed, selectivity, reliability and other requirements, as well as their effective coordination with other protection equipment (DCCBs, other local or remote relays etc.) cannot be guaranteed.

An additional desirable feature of non-unit protection is that the underlying protection algorithms need to be suitable for multi-vendor applications and ensure extensibility and adaptability when grid parameters or conditions change. Currently, HVDC schemes are usually built by a single manufacturer providing all equipment along with complete control and protection systems [32]. However, the implementation of future large-scale HVDC grids will necessitate the involvement of multiple vendors as is the case in contemporary AC systems [30], especially if the grid is developed organically over the years in a step-by-step manner. Therefore, HVDC grids will integrate equipment such as power converters, DC breakers, series inductors, cables etc. of different technologies from different vendors. In a multi-vendor environment, the impact of the grid elements on the DC fault signature may differ considerably depending on the technologies used and consequently, the complexity of designing generally applicable protection methods is increased. Therefore, one of the primary objectives of this thesis is to establish a methodology for designing generalised travelling wave based non-unit protection algorithms, and to demonstrate a practical non-unit protection solution that is suitable in a multi-vendor environment, thereby ensuring applicability for a wide range of HVDC grid equipment.

For faster fault current interruption, fully selective approaches typically rely on advanced DC circuit breaker topologies based on power electronic devices, which are characterised by a large capital cost and footprint. The latter is a significant drawback especially in offshore HVDC grids where the DCCBs are installed at offshore platforms, the cost of which can rise significantly for increasing weight and volume of the DCCBs [33]. The use of efficient HVDC converters with partial fault tolerant capability is considered an attractive option for future HVDC grids, in which expensive fast acting power electronics based DCCBs can be replaced with slower but inexpensive and less bulky mechanical DCCBs. In such cases, due to the increase of active grid components

that participate in the fault handling process, the development of a comprehensive fault management strategy that coordinates the actions of protection equipment, converters and other devices is essential. This thesis aims to explore this avenue in an effort to reinforce the technical and economic feasibility of future HVDC grids.

An additional important task in HVDC grids is the determination of the DC fault position along the faulted cable or line. Especially in cable-based systems, DC faults are typically permanent leading to the prolonged disconnection of the faulted cable until the section containing the fault is found and repaired. This may pose significant limitations on the operation of large-scale HVDC grids, in which the disconnection of a single unit can affect to a great extent the power exchange between the system nodes. Therefore, timely and accurate fault location is of crucial importance in order to accelerate system restoration and inspection time, and diminish the repair and operational costs and power outage duration. In the literature, most of the existing fault location techniques for HVDC systems assume that there is a long time window of post-fault measurements available. This assumption is not valid in the case of HVDC grids with high-speed protection systems, which are characterised by short post-fault data windows. In addition, there is currently a lack of consideration of the complexities that are introduced in multi-vendor HVDC grids. Consequently, an additional objective of this thesis is to develop a fault location solution specifically tailored for HVDC grids that addresses the above challenges.

For the execution of protection and fault location applications, measuring instruments are required to be placed on HVDC installations in order to capture the DC fault transients. The proper function and performance of such DC fault detection and location techniques is greatly dependent on the quality of measurements fed to the protection and fault location devices by the corresponding measuring schemes. In the current literature, much of the reported work is developed on a theoretical basis, while practical aspects of the proposed methods including sampling frequency requirements are neglected. Therefore, the capabilities of existing voltage and currents measuring technologies in terms of bandwidth are appraised in this thesis in an effort to develop practical guidelines for protection and location applications in HVDC grids.

1.3 Contributions to Knowledge

The core contributions of this work to knowledge are the following:

- Identification and review of the available voltage and current measuring instruments from the perspective of enabling protection and fault location applications in HVDC grids. This task in conjunction with a review of the existing protec-

tion and location methods has offered meaningful insights for selecting measuring equipment according to the desirable characteristics and requirements of state-of-the-art HVDC protection and location functions.

- Design and application of a methodology that utilises frequency domain analysis of travelling wave phenomena for facilitating systematic and flexible investigation of HVDC grid non-unit protection while avoiding the need for extensive and complex time domain simulations. The methodology has assisted towards the development of specific design guidelines for travelling wave based non-unit protection algorithms.

- Design and implementation of a wavelet-based scheme for fast, robust and discriminative HVDC grid protection. An analytical approach is developed for the efficient and flexible configuration, optimised protection performance, and general applicability of the scheme. The performance of the protection solution has been demonstrated through both offline simulations in PSCAD/EMTDC and in real-time hardware-in-the-loop configuration using a Digital Real Time Simulator (DRTS) and a low-cost hardware prototype executing an algorithm based on stationary wavelet transform, the first implementation of its kind.

- Development of a thorough realistic fault management strategy for HVDC grids that incorporate efficient modular multilevel converters. The strategy supervises and coordinates the actions of protection relays, DC circuit breakers, converters and additional grid controllers. Extensive electromagnetic transient simulations using PSCAD/EMTDC have demonstrated that the strategy enables continuous operation during pole-to-ground faults, and fault-tolerant operation with minimum power flow interruption during pole-to-pole DC faults.

- Development of an advanced single-ended fault location method that is suitable for locating DC faults in HVDC grids that are characterised by short post-fault data windows due to the use of high-speed DC breakers and other fast acting protective actions. Offline simulations have validated the enhanced accuracy of the method over a wide range of DC fault scenarios, and its ability in successfully identifying the faulted segment in heterogeneous transmission line media.

1.4 Thesis Overview

A brief overview of the chapters in this thesis is provided below:

Chapter 2 begins with presenting the fundamentals of HVDC grids and proceeds

with describing their main equipment. Converter technologies, DC circuit breakers, HVDC grid configurations, grounding practices, transmission lines, and DC current and voltage measuring devices are presented in detail. Special attention is given to modelling aspects of HVDC grid components towards realising realistic and high-fidelity but also efficient full-scale modelling of HVDC grids for the conduction of DC fault transient simulation studies.

Chapter 3 describes the main challenges, requirements and design aspects associated with HVDC grid protection and fault location systems. Moreover, the chapter provides a literature review of protection and fault location algorithms for HVDC grids. A case study is included to perform an analysis of transient phenomena that occur as a result of DC faults. The contributions of this chapter include an investigation of existing HVDC measuring instruments for enabling HVDC protection and fault location. This chapter effectively lays the foundation for the design and development of protection and fault location techniques proposed in this thesis, and provides the necessary background knowledge to aid the reader to understand the remainder of the thesis.

Chapter 4 develops a methodology focused on frequency domain analysis of DC faults for performing a systematic investigation of HVDC grid non-unit protection using travelling wave theory principles. After analysing the impact of each grid and fault parameter on DC voltage signatures, specific guidelines are proposed for the design of robust and flexibly configurable voltage-based non-unit protection algorithms.

Chapter 5 presents an advanced wavelet transform-based non-unit protection solution for HVDC grids using the guidelines and recommendations of the previous chapter for enhanced protection performance. The chapter includes a brief description of wavelet transform theory and considers practical facets in terms of computational requirements and protection-related goals to reinforce the technical feasibility of the method. Offline simulation results verifying the performance of the proposed protection solution are presented and further corroborated by dynamic validation using a digital real-time simulator combined with a low-cost relay prototyping platform.

Chapter 6 introduces a fault management strategy for continuous operation of HVDC grids using an efficient converter topology that demonstrates partial fault tolerant capability. The current limiting modes of the converter are explored, and the objectives, functions and implementation procedure of the strategy are described in detail. Rigorous parametric studies for different types of faults, sizes of current limiting inductors, converter parameters, and DC circuit breaker operation times reveal the underlying features, which render the proposed strategy an attractive option for the technical and economical feasibility of future HVDC grids.

Chapter 7 presents the working principle and assesses the performance of a novel single-ended fault location solution that combines travelling wave principles formulated

in the frequency domain with a genetic algorithm driven routine. The method addresses contemporary challenges arising from the utilisation of fast protection systems for DC fault management in HVDC grids, and is applicable to heterogeneous transmission line media (or hybrid media). The accuracy of the method in identifying the fault position is confirmed for different types of faults, fault parameters, transmission line media, signal-to-noise ratios, while the sampling frequency requirements are discussed.

Chapter 8 concludes the thesis by summarising the key outcomes and the principal contributions of the presented research, and recommends several potential directions for future research.

1.5 List of Publications

The following publications have resulted from the work reported in this thesis:

List of Journal Papers

- **V. Psaras**, D. Tzelepis, D. Vozikis, G. Adam and G. Burt, "Non-unit Protection for HVDC Grids: An Analytical Approach for Wavelet Transform-based Schemes," in IEEE Transactions on Power Delivery, early access, Sep. 18 2020, doi: 10.1109/TPWRD.2020.3024818.

- **V. Psaras**, D. Vozikis, G. Adam and G. Burt, "DC Fault Management Strategy for Continuous Operation of HVDC Grids based on Customized Hybrid MMC," in IEEE Journal of Emerging and Selected Topics in Power Electronics, early access, Dec. 30 2020, doi: 10.1109/JESTPE.2020.3048085.

- **V. Psaras**, D. Tzelepis and G. Burt, "A Genetic Algorithm Driven Fault Location Method for HVDC Grids based on Reconstructed Frequency Domain Voltage Profiles," submitted to ELSEVIER International Journal of Electrical Power and Energy Systems, May 2021.

- D. Tzelepis, **V. Psaras** et al., "Voltage and Current Measuring Technologies for High Voltage Direct Current Supergrids: A Technology Review Identifying the Options for Protection, Fault Location and Automation Applications," in IEEE Access, vol. 8, pp. 203398-203428, 2020, doi: 10.1109/ACCESS.2020.3035905.

- D. Vozikis, **V. Psaras**, F. Alsokhiry, G. Adam and Y. Al-turki, "Customized Converter for Cost-Effective and DC-Fault Resilient HVDC Grids," in International Journal of Electrical Power & Energy Systems, vol. 131, 107308, Oct. 2021, doi: 10.1016/j.ijepes.2021.107038.

List of Conference Papers

- **V. Psaras**, D. Vozikis, G. Adam and G. Burt, "Real Time Evaluation of Wavelet Transform for Fast and Efficient HVDC Grid Non-Unit Protection," 2020 IEEE Power & Energy Society General Meeting (PESGM), Montreal, QC, 2020, pp. 1-5, doi: 10.1109/PESGM41954.2020.9281507.

- **V. Psaras**, G. Adam and G. Burt, "Frequency Domain Analysis of HVDC Grid Non-unit Protection," 15th International Conference on Developments in Power System Protection (DPSP 2020), Liverpool, UK, 2020, pp. 1-6, doi: 10.1049/cp.2020.0024.

- **V. Psaras**, A. Emhemed, G. Adam and G. Burt, "Investigation of the Impact of Interoperability of Voltage Source Converters on HVDC Grid Fault Behaviour," 15th IET International Conference on AC and DC Power Transmission (ACDC 2019), Coventry, UK, 2019, pp. 1-6, doi: 10.1049/cp.2019.0031.

- **V. Psaras**, A. Emhemed, G. Adam and G. Burt, "Review and Evaluation of the State of the Art of DC Fault Detection for HVDC Grids," 2018 53rd International Universities Power Engineering Conference (UPEC), Glasgow, 2018, pp. 1-6, doi: 10.1109/UPEC.2018.8541961.

In addition, the learnings of the thesis have contributed to the following journals:

- A. Makkieh, **V. Psaras**, R. Peña-Alzola, D. Tzelepis, A. Emhemed and G. Burt, "Fault Location in DC Microgrids based on a Multiple Capacitive Earthing Scheme," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 9, no. 3, pp. 2550-2559, June 2021, doi: 10.1109/JESTPE.2020.2995946.

- D. Wang, **V. Psaras**, A. A. S. Emhemed and G. M. Burt, "A Novel Fault Let-through Energy based Fault Location for LVDC Distribution Networks," in IEEE Transactions on Power Delivery, vol. 36, no. 2, pp. 966-974, April 2021, doi: 10.1109/TPWRD.2020.2998409.

Chapter 2

HVDC Grid Technologies and Modelling

2.1 HVDC Basics

HVDC transmission is a well-proven and economic technology that offers a plethora of functionalities and solutions to the problems of modern power systems. Some of the major technical and commercial/economic advantages that render HVDC transmission highly competitive are the following [6, 9, 34–38]:

- Capability for long-distance bulk power transmission
- Flexible and efficient integration of renewable energy sources (particularly offshore wind energy)
- Interconnection of AC networks operating at different frequencies
- Fast power flow control capability
- Enhanced controllability through the independent control of active and reactive power (for VSCs)
- Connection to weak AC systems (for VSCs)
- High potential for enhanced grid support services such as frequency support, voltage support and system stability improvement, power oscillations damping blackstart capability etc.
- No need for periodic reactive power compensation and consequently, there is no technical limit to the transmission medium length

- Lower long distance losses
- Reduced right-of-way of DC circuits compared to AC circuits and more compact towers
- Lower investment costs than HVAC for long transmission (after a break-even point)
- Improved market efficiency (e.g.through market integration of separate regions and reduction price spikes)
- Transmission constraints mitigation
- Less visual impact along the transmission route

HVDC grids consist of a variety of equipment that collectively facilitate the robust and safe energy conversion and transmission. The typical structure and the equipment used in HVDC grids are illustrated in Figure 2.1. At the heart of the HVDC grids are the converters, which are responsible for converting the AC voltages and currents to their DC counterparts and for transmitting active and reactive power from the HVDC grid to the interconnected AC networks (or vice versa). Typically, each converter station is terminated with a DC bus at which one or more DC transmission media are connected. The main duty of the DC transmission media, which can be either cables or overhead lines, is to accommodate the DC power flows across the entire HVDC grid. Depending on the adopted HVDC grid protection philosophy, DC circuit breakers can be installed at several locations of the HVDC grid. Current limiting inductors are typically utilised in series with the DCCBs in order to slowdown the rise of DC fault currents and ensure that the DCCB maximum current breaking capacity is not exceeded. In addition, monitoring of the DC quantities (voltages, currents etc.) is essential for the proper operation of the HVDC grid as well as for control and protection applications. DC measurement is realised using voltage and current sensors, which determine the rate at which the information is available to the corresponding equipment.

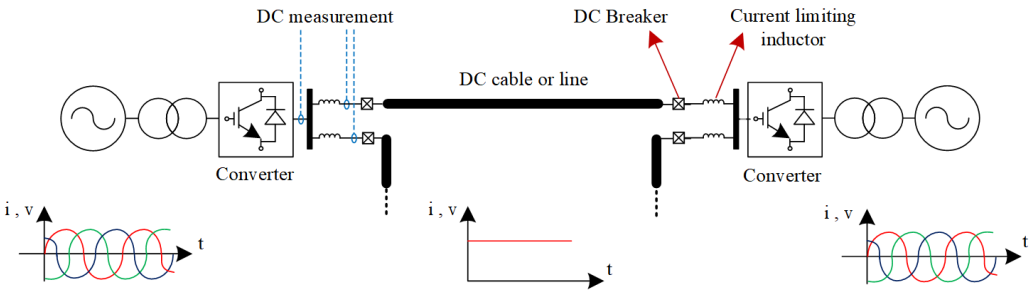


Figure 2.1: Typical structure and equipment of HVDC grids.

The rest of this chapter reviews the main components of HVDC grids which are shown in Figure 2.1, and presents the main control and modelling aspects that need to be considered in order to perform comprehensive and efficient full-scale HVDC grid modelling. The control and modelling aspects are presented from the perspective of HVDC grid protection in order to ensure that the HVDC grid models that will be developed later in the thesis are suitable for high-fidelity DC fault transient simulation studies for the development of novel HVDC protection and location schemes.

2.2 VSC Technology

Line commutated converter technology has been widely used in HVDC bulk power transmission for more than 50 years [6]. This technology relies on the use of line commutated switching devices, mainly thyristors, which turn off at current zeros and depend on the pre-existing AC voltage to commutate the current from the outgoing device to the incoming device [39]. LCC is also known as Current Source Converter (CSC), because it can be seen by the grid as a constant current source. It is a very robust technology and offers high reliability and resiliency to DC faults [36].

Nevertheless, LCC HVDC technology suffers from several well-known drawbacks, which have resulted in its very limited utilisation in modern HVDC transmission [40]. One of the most important limitations is that the converter requires large amounts of reactive power to retain unity power factor, due to the inherent delay between current and voltage waveforms. Moreover, the requirement for reactive power consumption hinders the use of LCCs in weak AC neworks. Another major drawback of LCC technology is the generation of significant low-order harmonic distortions and consequently, there is a need for large and costly AC and DC filters. In addition, LCC necessitates the use of sizeable DC link inductors to achieve continuous DC current. In the context of HVDC grids, the most important drawback of LCC technology is that DC voltage polarity needs to be reversed in order to perform power reversal, which complicates the coordination between converters in a HVDC system with multiple terminals.

The above limiting factors have led to the gradual replacement of LCCs with a new emerging technology based on VSCs, which offers new capabilities and facilitates the deployment of HVDC systems over a wider range of applications. VSCs are based on semiconductor devices that can turn on and off without the need for live AC voltages. In addition to the full controllability of these devices (mainly via external driver circuits), VSC-based systems offer the capability of independent control of active and reactive power. The latter feature is very important, since it significantly mitigates the need for massive and costly reactive power compensation that was required in LCC-based HVDC systems [39]. Moreover, VSC HVDC presents the additional advantages of reduced

operating costs, black start capability, fast power reversal, smaller converter station size, voltage waveforms with low harmonic distortions and hence, smaller station footprint due to the greatly reduced size of AC and DC filters [6, 36]. The aforementioned advantages render the VSC technology a well-suited option for HVDC grids, in which the power direction can be easily changed without the need for reversing the voltage polarity. The rest of this section aims to introduce the main VSC topologies and present important control, operation and converter modelling aspects.

2.2.1 Classic Two-level VSC

The first VSC HVDC schemes that were developed, were based on the classic two-level VSC concept (Figure 2.2). As depicted in the figure, a two-level converter composes of six arms, that employ Insulated Gate Bipolar Transistors (IGBTs), with each pair of arms constituting a phase leg. It is worth mentioning that in high voltage transmission, one single IGBT cannot handle the full magnitude of the voltage. To enable operation at high voltage, a large number of IGBTs must be connected in series to ensure even voltage sharing between individual IGBTs during turn-on and turn-off [41]. Large physical volume and relatively high conversion losses are the main limitations of this converter. The integrated converter control is responsible for turning on all the series devices simultaneously and making them behave as a single coordinated valve. For this purpose, Pulse Width Modulation (PWM) is usually adopted to control the gate signals of the IGBTs for reduced filtering requirements and better dynamic performance. According to this method, the width of the resulting pulse is produced based on the comparison between a usually sinusoidal (SPWM) reference waveform and a triangular carrier waveform.

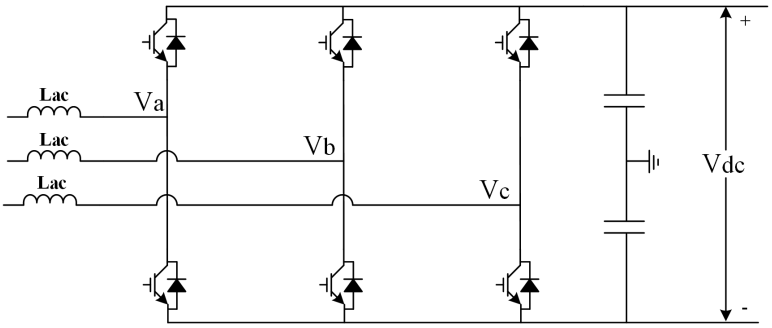


Figure 2.2: Classic two-level converter.

2.2.2 Neutral Clamped Converter

The conventional PWM control of the classic two-level converter can be adjusted and used in multilevel converters such as the Neutral-Point Clamped (NPC) converter [42]. Figure 2.3 illustrates the firstly introduced NPC multilevel topology, which is the well-established three-level NPC converter that has been widely used in AC motor drive applications such as pumps, fans, mills and conveyors [43]. The converter is named after the fact that the midpoint of the switches in each phase is connected to the neutral point of the topology using clamping diodes. The topology can generate a voltage waveform with three different output levels at +Vdc/2, 0, and - Vdc/2 depending on the operation mode (switching states). The converter is based on a modification of the classic two-level converter with the addition of two extra power semiconductors per phase. Each device has to withstand half the voltage compared to the devices in the classic two-level topology (for the same DC-link voltage) and consequently, if the same power devices are used, the input voltage can be doubled. NPC converter demonstrates better harmonic performance, but the circuit relies on the simultaneous operation of two devices to generate each voltage level, which compromises the overall converter efficiency [35].

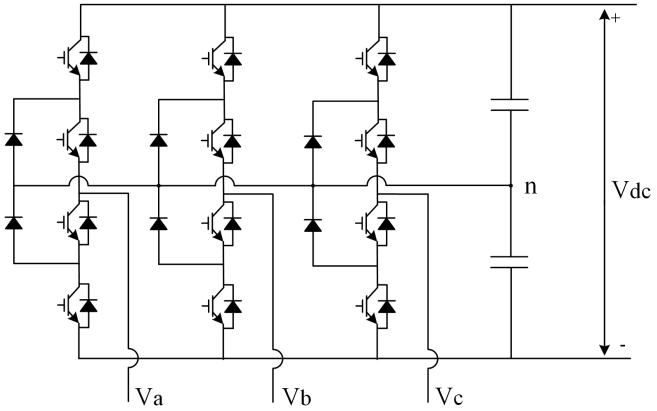


Figure 2.3: A typical three-level neutral-point clamped converter.

The same philosophy can be extended for NPC converters with more output voltage levels, but the associated operation and construction complexity increases substantially, since there is a quadratic relationship between the voltage levels and the required number of clamping diodes [35]. Moreover, critical failure propagation might be presented when the number of levels increases. Another drawback of this topology is that the number of capacitors is not minimised while also, under certain operating conditions the capacitors may experience voltage unbalances that might cause a voltage potential between the neutral point and ground, leading to distorted voltages.

2.2.3 Modular Multi-Level Converter

Some of the limitations of two-level and NPC converters were addressed with the advent of the relatively new and promising concept of Modular Multi-level Converters (MMC). This converter topology was firstly introduced in the Trans Bay cable connection by Siemens [44]. The fundamental difference between MMC and classic VSC is that the latter offers two or three potential voltage levels per phase, while the former can theoretically achieve an arbitrary number of voltage levels (or steps) and hence, the AC voltage can be better approximated [7]. The fundamental component of the MMC is the sub-module (SM) or cell, which consists of semiconductor switches that can be arranged in various topologies, such as half-bridge (HB), full-bridge (FB), mixed-cell (MC) etc. [45]. The sub-modules are connected in series and the same number of sub-modules is connected to each phase, thus forming three identical legs. Moreover, each phase leg can be further divided to an upper and a lower arm that contain the same number of sub-modules. This kind of configuration, along with the most typical sub-module topologies are shown in Figure 2.4.

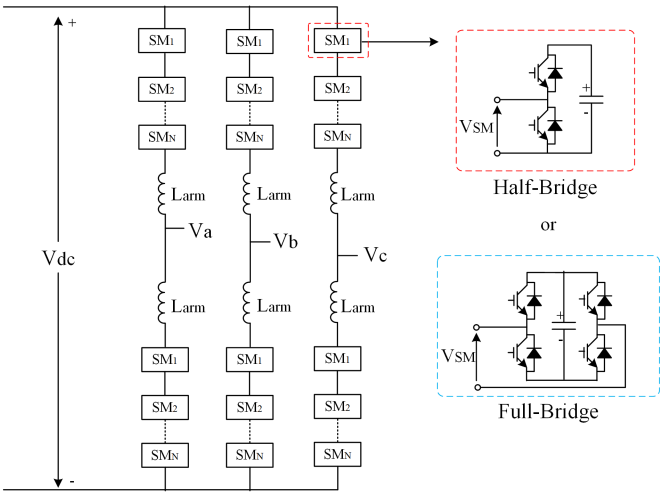


Figure 2.4: Three phase modular multilevel converter with HB or FB sub-modules.

One of the main differences between the MMC and two-level and NPC converters, is the absence of a central DC-link capacitance. Instead, each MMC arm incorporates distributed capacitors in each SM, and the voltage rating of each capacitor is limited to a fraction of the nominal DC voltage (V_{dc}). Therefore, MMCs can generate AC voltages by connecting or disconnecting the distributed capacitors, which results in multiple potential voltage levels. Consequently, as the number of SMs per arm increases, higher-fidelity near-sinusoidal AC voltages can be generated leading to substantially reduced harmonic content. In addition, the MMC can provide several attractive features such as, high modularity, better voltage output performance, lower switching frequency and

improved efficiency and reliability [45]. For all these reasons, MMC technology has evolved into the preferred option for recent and future HVDC systems. It is worth noting that all multi-terminal VSC-MTDC systems mentioned in Section 1.1 are based on the Half-Bridge MMC (HB-MMC).

2.2.4 VSC Control

The most widely used control strategy for VSCs is the current vector control that is realised using park transformations of the AC system voltages and currents at the Point of Common Coupling (PCC) [46]. In this way, the AC variables are projected on the synchronous direct-quadrature (d-q) rotating frame that is synchronised with the AC voltage. A Phase-Locked Loop (PLL) is utilised in order to synchronise the rotating frame with the AC grid voltage by tracking its phase. Moreover, it generates the angle reference θ and velocity ω based on the three-phase voltages at the PCC that are used as inputs for the mathematical transformations of the control variables. The resulting d-q components of the AC variables appear as DC quantities that allow the application of linear control concepts. Independent control of the active and reactive power is possible since the PLL locks the system voltage along one of the axes of the frame.

The general architecture of current vector control in grid-following mode (synchronised with the AC grid) for two-level converters is shown in Figure 2.5. The overall control structure is based on cascaded Proportional Integral (PI) controllers that are classified into outer and inner controllers. The outer controllers are responsible for generating the references for the inner current controllers. For a two-level converter, these PI controllers form the upper-level control of a VSC, while the modulation technique (e.g. PWM) constitutes the lower-level control. A PI controller is applied at each component of the d-q frame to generate the i_d^* and i_q^* reference currents, which are associated with active power loop and reactive power loop respectively. In detail, the d outer controller can directly control either the active power or the DC voltage, while the q outer controller can directly control either the reactive power or the AC voltage. The dynamics of the outer controllers are typically one order of magnitude slower than the inner current controllers [47].

Inner current controllers are based on fast PI controllers which aim to track the reference currents produced by the outer controllers. The terms $\omega L i_d$ and $\omega L i_q$ are added to the q and d components respectively to decouple the two controllers. The inner controllers generate the reference voltages U_d^* and U_q^*, that are fed to the lower-level control that is responsible for developing the firing pulses of the IGBTs. In the case of a two-level converter, PWM is commonly used at the lower-level control to produce the IGBT switching pulses.

Current vector control is also employed in the upper-level control MMC topologies, including the HB-MMC. However, the upper-level control of the HB-MMC is more complex (Figure 2.6). Depending on the control objectives of the converter, a negative sequence current controller might be incorporated in the upper-level control along with the positive sequence current controllers. The architecture of both controllers is identical and is based on the current vector operation principles described before. If maintaining balanced three-phase currents is required, the reference currents of the negative-sequence controller are set to zero [48].

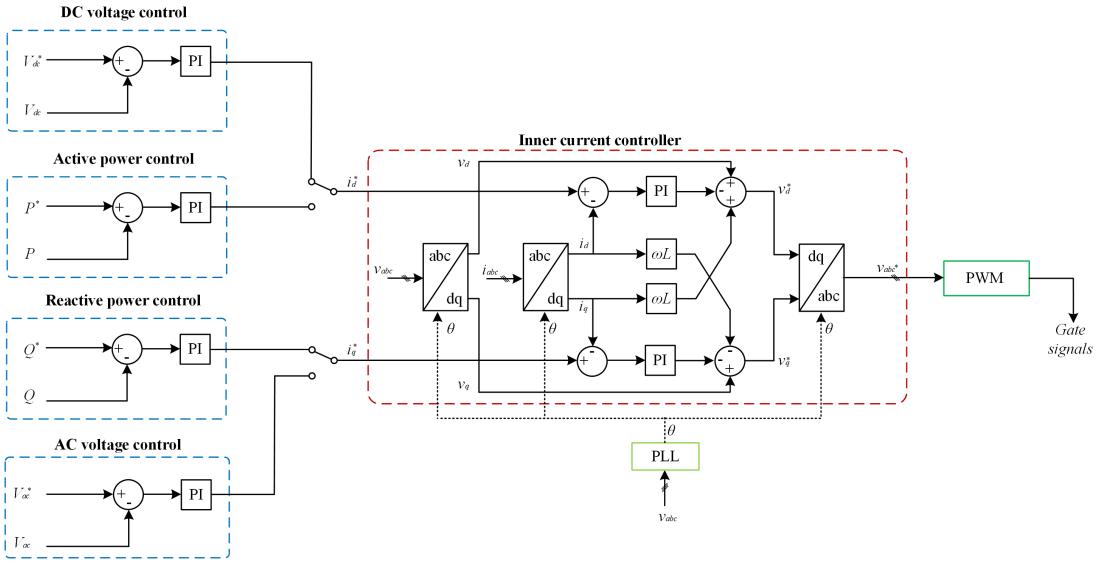


Figure 2.5: Current vector control for two-level converter (grid-following mode).

Horizontal and vertical capacitor voltage balancing controllers are also incorporated at this level [49]. The former ensures equal voltage distribution across phase legs, while the latter is responsible for ensuring that the sum of the upper arm capacitor voltages are equal to the sum of the lower arm capacitor voltages. These controllers also improve the dynamic response of the MMC as changes in DC voltage or active power orders do not result in significant changes in the energy level of the SM capacitors [48]. In addition, the circulating current suppression controller is used to suppress the second order harmonic in the currents of the arms of the MMC.

In the most inner control level of the MMC, capacitor voltage balancing and modulation are the main operations that are performed. Capacitor voltage balancing ensures that the distributed cell capacitor voltages remain balanced and equal to their nominal value. Towards this aim, a voltage balancing algorithm is employed which sorts the SM capacitor voltages in an ascending order, and depending on the current direction, the cells with the higher voltage levels (lower voltage levels) are prioritised to be inserted (bypassed) when the current is positive (negative). This process ensures equal voltage

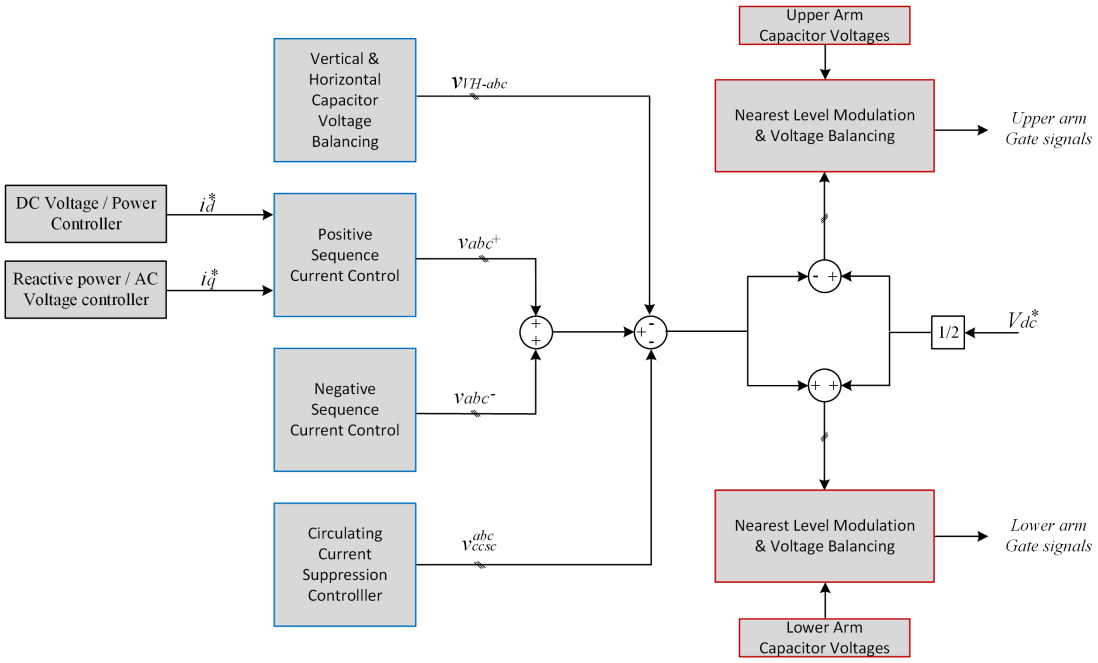


Figure 2.6: Upper and lower level control of HB-MMC.

sharing across the cells in each converter arm. The modulation process determines the number of SMs that are bypassed or inserted in the conduction path at each time instant. Nearest-Level Modulation (NLM) is the simplest modulation technique that remains effective for large numbers of levels of the MMC [50].

2.2.5 Converter Modelling

Efficient and accurate representation of HVDC converters is of paramount importance for the conduction of electromagnetic transient simulations and the investigation of transient phenomena during DC faults. Detailed modelling of two-level and NPC converters is relatively straightforward, since each series of IGBTs in each converter arm can be represented by a single power electronic element (in a similar structure as the circuit of Figure 2.2) [51]. Nevertheless, full scale modelling of MMC topologies is a significantly more complicated and demanding task, computationally and memory-wise. Such challenges are introduced by the large number of switching elements and distributed capacitors in each arm of the MMC that affect the converter's operation and result in a large number of electrical nodes and matrices that need to be computed in each simulation time step. This effect is further exacerbated in large-scale MMC-based HVDC grids, where the computational effort and time required even for the simulation of a small time-scale event is prohibitive.

Several modelling techniques with varying degree of accuracy have been developed

in an effort to overcome the above issues [52–59]. It is worth noting that the level of detail of the selected model is dictated by the requirements, the objectives and the required depth of analysis of the intended study. The MMC model that is selected and used in the studies of this research is the average MMC model that is illustrated in Figure 2.7. The aim of the model is to reduce drastically the number of nodes and achieve a trade-off between computational efficiency and level of detail of converter dynamics without compromising the accuracy for DC fault transient studies.

Figure 2.7 shows the averaged model for the HB-MMC for a single leg (phase) of the converter, in which controlled voltage and current sources replace the SMs in each arm. In the following analysis, N_{SM} is the number of SMs per arm, V_{SM_j} is the capacitor voltage of the j^{th} sub-module (with $j \in [0, N_{SM}]$), and symbols U and L refer to the upper and lower converter arm, respectively. Since the analysis is valid on a per phase basis, the phase notation (A,B and C) is omitted. The switching voltages across the upper arm and lower arm of the MMC, V_{armU} and V_{armL}, can be represented by their average voltages, which are given by [48, 60]:

$$\begin{cases} V_{armU} = \sum_{j=1}^{N_{SM}} V_{SMU_j} \approx \frac{1}{2} V_{carmU}[1 - msin(\omega t + \delta)] \approx V_{carmU} m_U \\ V_{armL} = \sum_{j=1}^{N_{SM}} V_{SML_j} \approx \frac{1}{2} V_{carmL}[1 + msin(\omega t + \delta)] \approx V_{carmL} m_L \end{cases} \tag{2.1}$$

where m is the AC modulation index, and V_{carm} is the total blocking voltage of the HB-SM capacitors in each arm, which is given by $V_{carm} = \sum_{j=1}^{N_{SM}} V_{SM_j} \geq V_{DC}$.

In the average model, the inter-sub-module dynamics of the converter are neglected and the SM capacitor voltages in eah arm are considered to be balanced and oscillating together. Therefore, assuming C_{SM} is the cell capacitance, the upper and lower arm equivalent capacitances are $C_{armU} = C_{SM}/N_U$ and $C_{armL} = C_{SM}/N_L$, respectively, where N_U and N_L is the number of SM capacitors that are inserted in the power path from the upper and lower converter arm. N_U and N_L are approximated by:

$$\begin{cases} N_U \approx \frac{1}{2} N_{SM}[1 - msin(\omega t + \delta)] \approx N_{SM} m_U \\ N_L \approx \frac{1}{2} N_{SM}[1 + msin(\omega t + \delta)] \approx N_{SM} m_L \end{cases} \tag{2.2}$$

Based on (2.2), the dynamics of the upper and lower SM capacitors are given by:

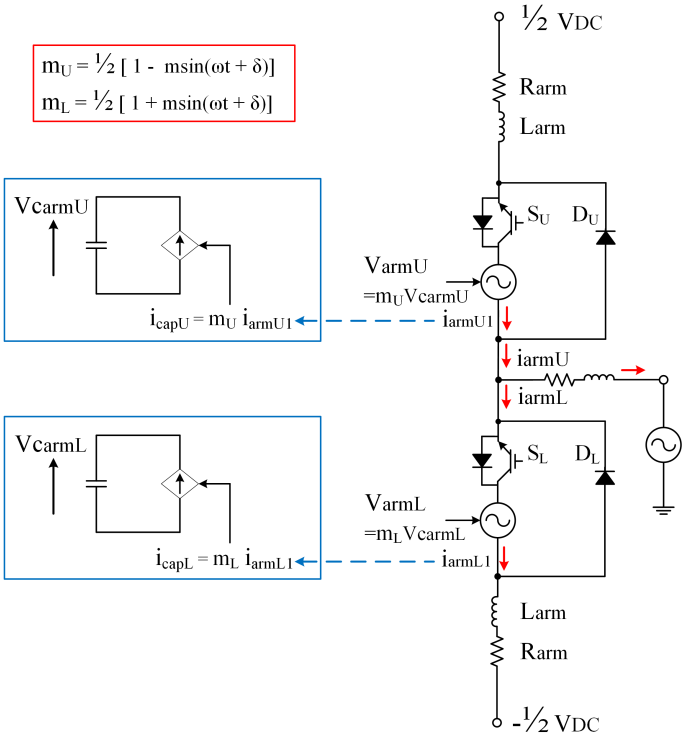


Figure 2.7: Illustration of one phase of the HB-MMC average model.

$$\begin{aligned}
&\frac{C_{SM}}{N_U}\cdot\frac{d}{dt}V_{carmU} \approx i_{armU}\\
&\frac{C_{SM}}{N_{SM}}\cdot\frac{d}{dt}V_{carmU} \approx \frac{1}{2}[1-msin(\omega t+\delta)]i_{armU}\\
&C_{arm}\cdot\frac{d}{dt}V_{carmU} \approx m_U i_{armU}
\end{aligned} \tag{2.3}$$

$$\begin{aligned}
&\frac{C_{SM}}{N_L}\cdot\frac{d}{dt}V_{carmL} \approx i_{armL}\\
&\frac{C_{SM}}{N_{SM}}\cdot\frac{d}{dt}V_{carmL} \approx \frac{1}{2}[1+msin(\omega t+\delta)]i_{armL}\\
&C_{arm}\cdot\frac{d}{dt}V_{carmL} \approx m_L i_{armL}
\end{aligned} \tag{2.4}$$

where C_{arm} is the equivalent capacitance for each arm. From (2.3) and (2.4), the upper and lower equivalent arm capacitor currents are approximated by:

$$\begin{cases}
i_{capU} \approx C_{arm}\cdot\frac{d}{dt}V_{carmU} \approx m_U i_{armU}\\
i_{capL} \approx C_{arm}\cdot\frac{d}{dt}V_{carmL} \approx m_L i_{armL}
\end{cases} \tag{2.5}$$

Equations (2.1) to (2.5) describe the operation of the converter under steady-state conditions, during which the IGBT elements S_U and S_L (shown in Figure 2.7) are in the on-state. Since V_{armU} and V_{armL} are always positive, the diodes D_U and D_L are reverse biased. Nevertheless, the additional IGBTs and diodes are included to represent the converter's behaviour in the blocking state by providing the necessary conduction path. In detail, taking the upper arm as an example, when the HB-MMC is blocked, the IGBT S_U is turned off and m_U is set to 1 to quench the arm current. In this case, if the arm current is positive (with the direction shown in Figure 2.7), it will flow through the anti-parallel diode of S_U, and the arm voltage will be the combined voltages of the SM capacitors. On the other hand, if the arm current is negative, it will flow through D_U that bypasses the SM capacitor and consequently, the arm voltage will be zero. With the additional elements, all states of the HB-MMC can be simulated, including the blocking state of the converter that is invoked during DC faults.

The model is not capable of reproducing the inter-cell dynamics and therefore, it is not suitable for detailed power electronic studies (component sizing, switching characteristics etc.). Nevertheless, the MMC average modelling technique has been validated and benchmarked against more detailed models (Thevenin equivalent and switching function model) using EMT-type software [60] and a real-time simulation platform [61], where it has been demonstrated that it can produce practically identical response with much greater simulation efficiency over a wide range of studies, including DC fault transient studies.

2.3 HVDC Grids Layout

VSC-based HVDC grids utilising any of the converter topologies presented in the previous section can have different layout in terms of system configuration and grounding options. HVDC grid configuration refers to the way the VSC stations are configured and interconnected with each other, and has a direct influence on protection requirements. Furthermore, the type of grounding system and the number of grounding points also influence the system's behaviour during DC faults. Therefore, the remainder of this section presents in detail the most common HVDC grid configurations and grounding practices, and their corresponding impact on DC fault behaviour.

2.3.1 HVDC Grid Configurations

The three basic configurations of HVDC grids that incorporate VSCs are the asymmetrical monopolar, the symmetrical monopolar and the bipolar configuration. Each one of these, presents its own advantages and disadvantages. This section aims to describe

these topologies and the earthing practices that can be applied.

Asymmetrical Monopolar Configuration

The simplest architecture for HVDC networks is the asymmetrical configuration shown in Figure 2.8, in which a single converter is used at each terminal. One pole requires a fully insulated high voltage conductor rated at the nominal system voltage and the other one is grounded, lightly insulated (it only needs to withstand the voltage drop across the line) but rated for nominal current. Due to the use of a single fully rated DC conductor, the asymmetrical monopole is the least expensive option. This topology can either have earth return or metallic return with low insulation requirements. The earth return is preferable since it significantly reduces the cost by eliminating the need for installation of an additional cable or line. However, due to considerable environmental concerns, in most cases a metallic return is also installed to avoid a continuous current flow through the earth or sea (in case of sub-sea systems) but at the expense of higher costs and transmission losses [34]. A loss of a converter or a DC line can lead to the complete disruption of power transfer between the terminals.

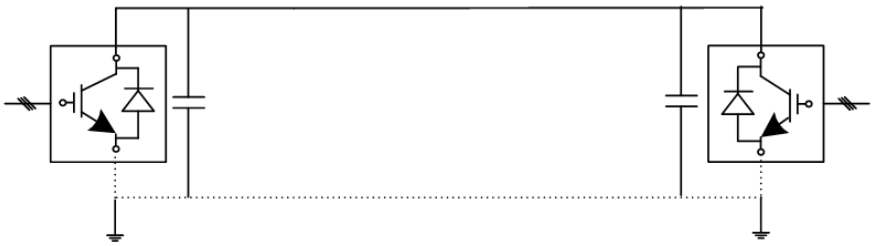


Figure 2.8: Asymmetrical monopolar configuration.

Symmetrical Monopolar Configuration

Symmetrical monopolar configuration (shown in Figure 2.9) is the most widely used option, especially for point-to-point HVDC transmission links. The two poles of the system operate at an equal voltage magnitude but with opposite polarity. The steady state voltage for each conductor is the half of the full converter voltage.

Figure 2.9: Symmetrical monopolar configuration.

Pole-to-ground faults expose converters to limited and short duration of over-current and healthy DC cables to excessive high voltage levels and therefore, both conductors need to be appropriately insulated. On this basis, this topology is significantly more expensive than the asymmetrical monopolar configuration. Similar to the previous topology, the loss of the transmission medium can lead to the disruption of the entire power transfer across the associated link.

Bipolar Configuration

The bipolar configuration can be considered as two asymmetrical monopoles connected to each other while sharing the same return (Figure 2.10). Two converters of equal voltage rating are utilised at each terminal, one is connected between the positive pole and ground and the other between ground and the negative pole. In normal operation, there is no current flowing through the return and the poles are operating at the same voltage level as the converters but with opposite polarity. In analogy to asymmetrical monopolar configuration, the system can have either earth return or metallic return, which operates at zero current during balanced and symmetrical operation. This configuration presents the higher transmission capacity and provides the highest level of reliability, flexibility and redundancy because of the independent operation of each pole [62]. In case of pole-to-pole DC faults, the converters and DC links connected to the faulted pole experience high fault currents. Nevertheless, the system can retain operation at 50% of the transmission capacity, if the faulted pole is isolated. On the downside, this configuration involves the highest costs. The use of bipolar configuration for HVDC grids is considered more practical, especially when overhead lines are to be adopted, in order to allow for higher pole-to-ground DC voltages (500 kV or more) and increase power handling capacity beyond that of the symmetrical monopolar systems.

Figure 2.10: Bipolar configuration.

2.3.2 Grounding Practices

The selected grounding scheme for HVDC grids is of critical importance because it influences to a great degree the system operation and protection requirements. HVDC grids can be grounded either through low or high impedance. During pole-to-ground faults, low impedance grounding results in lower voltage disturbances at the healthy pole but high over-currents, while high impedance grounding results in low over-currents and high voltages at the healthy pole. Common grounding options include a) direct, b) resistive, c) inductive, and d) capacitive grounding, as wells as e) absence of grounding [6]. These grounding options can be realised at the converter stations as shown in Figure 2.11 for the case of asymmetrical or symmetrical monopoles [62].

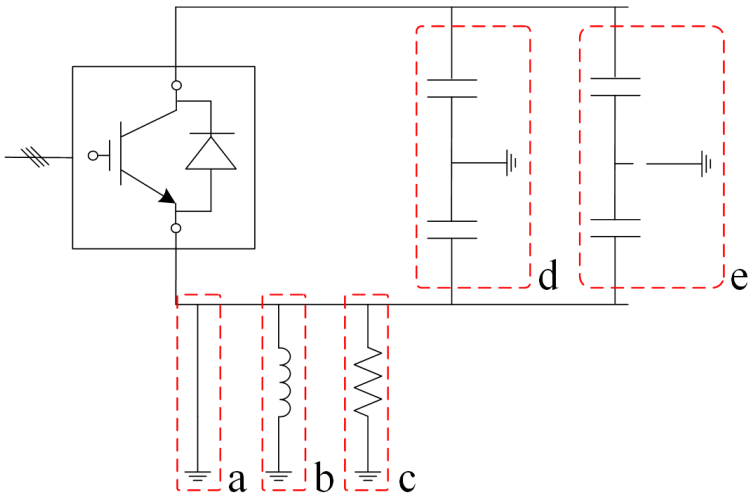


Figure 2.11: Grounding options.

Low impedance grounding can be formed through solid or low-resistive grounding. Inductive and capacitive grounding are frequency dependent. At low frequencies, inductive grounding forms a low impedance path while capacitive grounding forms a high impedance path. For high frequencies, inductive and capacitive grounding form a high impedance and a low impedance path, respectively [63].

Asymmetric monopoles typically use solid grounding (low impedance grounding) in order to mitigate the voltage rise on the metallic return conductor and retain its voltage near zero. In this way, when a pole-to-ground fault occurs, the voltage at the healthy pole does not exceed the nominal value but the fault current demonstrates a steep increase and might reach extreme values. Alternatively, a low-ohmic resistance or an inductance could be used to ground the system. The inductor does not affect the steady-state fault current but limits the current rise during the initial stage of the fault. To avoid earth currents in normal operation, only one converter can be grounded.

A symmetric monopolar system can be solidly grounded at the mid-point of DC capacitors at each converter as shown in Figure 2.9. Regardless of the grounding option used, the system is effectively high impedance grounded [6]. Assuming a pole-to-ground DC fault on the positive pole, a short circuit path is created through ground, the upper capacitor and the faulted pole, resulting in short duration high current (associated with the upper capacitor discharge) and doubling of the DC voltage across the lower capacitor, which is connected between ground and the healthy pole. In this way, the pole-to-pole DC voltage remains intact and the healthy pole is exposed to over-voltage causing a significant risk of insulation failure.

Bipolar HVDC grids can be either high or low impedance grounded. If the system is required to support monopolar operation in case of a faulted pole, it should be either directly grounded at all terminals, or if high impedance grounding is employed, a metallic return should be used and grounded at one terminal [62]. With direct grounding, when a pole-to-ground fault occurs, the postfault voltage of the healthy pole is limited at the nominal converter voltage. On the contrary, when high impedance grounding is used, the voltage of the metallic return can increase up to the nominal converter voltage and consequently, the healthy pole voltage can rise up to two times the rated voltage. It can be concluded that in terms of protection requirements and grounding performance, a bipolar grid can behave either as an asymmetric or a symmetric monopolar grid depending on whether low or high impedance grounding is employed.

2.4 HVDC Grid Control

HVDC grid control strategies can significantly affect the behaviour of HVDC grids during transient events such as fault condition and post-fault recovery. Hence, a basic understanding of such control strategies is required when developing HVDC grid models for DC fault transient simulation studies. Due to the increased controllability of VSCs and especially MMCs, there is a growing interest in HVDC grids providing ancillary services to the AC networks such as power oscillations damping, frequency support etc. To fulfil these objectives, the HVDC grid is controlled based on a hierarchical structure [64]. The levels of the hierarchical structure, from the slowest to the fastest control level, are organised as power dispatch control, secondary control, primary control and current control [65]. The characteristics and the aims of each level are outlined below.
Power dispatch control: This level focuses on the long-term operation of the HVDC grid, where the power injections of each terminal are determined based on technical aspects and economics. Optimal power flow techniques can be employed at this level to minimise the total system operational losses and costs.
Secondary control: This level acts as a link between tertiary (power dispatch) and

primary control. It is responsible for accomplishing the power exchanges among terminals based on the power references set by the tertiary control. If necessary, this level may adjust the power setpoints as corrective actions following contingencies.

Primary control: Primary control refers to the controller that is responsible for adjusting the DC voltage. Its aim is to regulate the DC voltage within certain limits based solely on local measurements.

Current control: Current control is the lowest level of the structure and it is responsible for current regulation at each VSC station as described in Subsection 2.2.4.

Power dispatch control level is not considered in this thesis since its associated timescales (minutes to hours) exceed those of DC fault management (up to few hundreds milliseconds). The rest of this section focuses on the primary control level that is implemented through the individual converter control strategies, and the secondary control that is based on the coordination of these strategies towards achieving power sharing among the grid terminals.

2.4.1 Basic Converter Control Strategies

The primary control of the HVDC grid hierarchical control structure can be implemented by the converter control strategies shown in Figure 2.12. The converter control strategy is part of the outer loop of the current control that is typically employed by VSC topologies. As a result, converter control strategies operate in a decentralised manner, since their implementation is made at each individual terminal station and relies only on local voltage and current measurements. The global behaviour of the grid is dependent on the proper coordination of the controllers implemented at this control level. The different configurations of these controllers are subsequently explained.

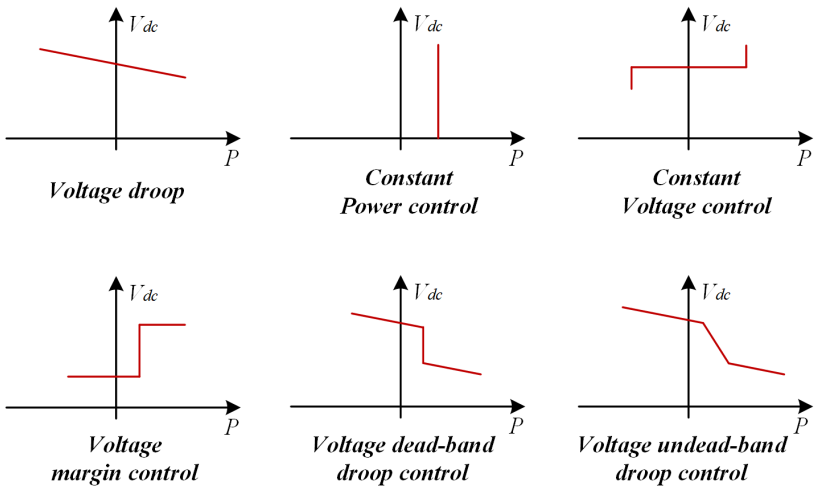


Figure 2.12: Basic converter control strategies.

Voltage droop control: Voltage droop control originates from frequency-power droop control that is used in AC systems. A voltage droop controller commands the converter to inject power in or out of the DC grid based on a proportional function of the DC voltage error. Therefore, voltage droop control represents a linear relationship between power and voltage, as shown in Figure 2.12. As the slope of the relationship increases, the control becomes less sensitive to voltage variations. The slope is determined by the droop value, which highly impacts system operation.

Constant power control: This control scheme ensures that the converter maintains a constant power injection regardless of the DC voltage at the local bus. VSCs operating in this mode usually correspond to converters integrating power sources, such as wind power plants. This case can be considered as a limiting case of voltage droop control, in which its associated droop value approaches infinity [66].

Constant voltage control: In this case, the converter controls the local DC voltage to a specific operating set-point. Converters operating with constant voltage control (also referred to as slack buses) are responsible for guaranteeing the grid power balance by accommodating the injected power flows while maintaining a constant DC voltage. Constant voltage control can be considered as a limiting case for voltage droop, in which the droop constant approaches zero [66].

Voltage margin control: This scheme is a combination of constant power and constant voltage control. The converter operates on a constant power basis as long as the voltage remains within the normal operation range. Outside this range, the converter switches to constant voltage control by regulating the power accordingly.

Voltage dead-band control: Another approach to DC voltage control is the voltage dead-band control, which is a combination of voltage droop and constant power control. Within a specified voltage range, the controller maintains the power constant. If a high voltage deviation occurs, the controller switches to voltage droop control. This control scheme allows the converters to make small power adjustments.

Voltage undead-band control: This control scheme is based on different droop constants that are used in different regions of the voltage-power characteristic. In this way, the control can distinguish between normal and disturbed operation and react in a different way in each case by adjusting the droop constant.

2.4.2 Power Sharing Control Schemes for HVDC Grids

Coordination of the individual converter control strategies on a system level is an important task for ensuring effective power sharing between the grid terminals. Similar to the frequency in AC systems, DC voltage in HVDC grids provides an indication of the power imbalance with the main difference being that the DC voltage is not a

global variable and it is largely influenced by the total DC grid power balance and the energy flows between terminals. Hence, DC voltages differ from terminal to terminal and consequently, a strategy is required for power sharing control schemes (through DC voltage management) in such a way that the desirable power flows are achieved, and the system operates smoothly.

Traditionally, in point-to-point links, the existing practice entails operation of one terminal in constant power control, and operation of the other in voltage control [47]. Similarly, in HVDC grids different terminals can employ different control strategies, and a mixture of the strategies presented in the previous subsection can be utilised to form either centralised or decentralised power sharing schemes. The main schemes that have been designed for DC voltage control in HVDC grids are the a) leader-follower control, b) hierarchical voltage margin control and c) distributed droop control.

Leader-follower Control

In analogy to the common practice followed for point-to-point links, the leader-follower control concept has been proposed for HVDC grid control. In this scheme, only one station is responsible for DC voltage regulation, while the rest converters employ constant power controllers. This scheme is also known as centralised voltage control, since only one converter is responsible for accounting for all grid disturbances. The implementation of such control is relatively simple and offers a well-defined operating point, but its reliability is limited because the successful operation of the entire HVDC grid is dependent on the proper control of the leader-station. In addition, large grid disturbances may lead to the capabilities of the leader converter being exceeded leading to loss of grid control. As a result, controlling all DC network voltages from a single terminal is not desirable and hence, a distributed approach to DC grid control or at least a backup control scheme in case of severe disturbances is required.

Hierarchical Voltage Margin Control

In the hierarchical voltage margin control strategy, the task for controlling the voltage profile can be shifted among several converter stations. This strategy remains a centralised approach to DC grid control, but backup control mode is included. The backup control is provided by another converter station that takes over the task of DC voltage regulation in cases of outage or failure of the master-converter or in case the master-converter reaches its capabilities limits (e.g. maximum power limit). If this backup station malfunctions or reaches its respective limits, an additional converter can offer further backup control and take over as the new master-station. In a similar manner, backup control can be provided by all stations of the HVDC grid. The coordination

between the converters can be achieved either via means of communication or with the use of distinct operating voltage setpoints for each converter. This hierarchical control scheme between terminals is utilised in Zhoushan MTDC system [23]. A drawback of this method is that the shifting of master converter may cause significant oscillations in the DC voltage [46].

Distributed Droop Control

Distributed droop control is implemented by applying voltage droop control to more than one terminal of the HVDC grid. The voltage droop-controlled stations share the responsibility of regulating the DC voltage while the other stations are set to maintain constant power. The droop value used in droop-controlled station determines the amount of contribution and the responsibility each converter has on sharing the power imbalances. The droop-controlled converters can be based on any of the voltage droop control schemes that were presented in Subsection 2.4.1. Distributed droop control offers high reliability and has evolved into the most promising HVDC grid control scheme. Moreover, with this type of control, converters with lower power rating can effectively manage large power imbalances or variations [65]. In [22], it is mentioned that control of the Nan'ao multi-terminal system is based on distributed droop control, in which two converter stations are responsible for manipulating the DC voltage.

2.5 HVDC Circuit Breakers

Secure operation of HVDC grids relies largely on the capability to quickly interrupt DC fault currents. Similar to AC systems, DC circuit breakers can be used to isolate DC network faults and at the same time facilitate the continued operation of the healthy part of the network. For this reason, high-voltage DCCBs are considered one of the key enabling technologies towards the realisation of HVDC grids. Consequently, significant research has been performed in an effort to develop efficient fast operating breakers that can protect DC networks [67–71], while also several manufacturers have invested substantially in developing commercial products [24, 72–74]. In contrast to fault currents in AC systems, DC fault currents do not experience zero crossings, thus making the development of additional dedicated mechanisms a necessity towards achieving similar attributes and performance achieved with AC CBs. Generally, successful interruption of a DC current from a DCCB requires the following [75, 76]:

a) Production of an artificial current zero crossing for local interruption.

b) Insertion of a counter voltage, which is typically larger than the nominal voltage

in order to drive the fault current to zero. This can be done either by introducing a counteracting voltage, or by injecting a reverse current.

c) Dissipation of the energy stored in line inductances and DC reactors during the fault.

d) Establishment of sufficient dielectric strength of the medium between the breaker's contacts in order to withstand the transient recovery voltage.

Various concepts of DC breakers that achieve these objectives have been proposed. All of these topologies involve a main branch or load path, an auxiliary branch or commutation path and an absorption path. During normal operation, the current flows through the load path and when a DC fault occurs, the current is diverted to the commutation path that is responsible for creating the current zero crossing. Finally, the absorption path is used to dissipate the stored energy. The selection of the suitable DCCB technology depends on a plethora of characteristics and requirements such as, the breaker operation speed, DCCB current capacity, cost, losses, size, expected level of energy absorption etc. The most common HVDC breakers can be classified into: a) mechanical breakers (passive or active resonance breaker), b) solid-state breakers and c) hybrid breakers.

2.5.1 Mechanical Circuit Breakers

Mechanical resonant DC breakers have been developed based on conventional AC gas circuit breakers. The commutation path is formed by an additional resonant LC circuit that is placed in parallel to the main load path. Resonant DCCBs can use active or passive resonant circuits (Figure 2.13 a) and b) respectively) to force the DC fault current to zero and allow the breaker to open without the risk of an electric arc. The additional branch in the passive configuration gives rise to an oscillating current that is superimposed to the fault current flowing through the main path. The oscillating current results in a current zero crossing in the load path that can be exploited for current interruption by the CB.

The active resonant breaker uses a pre-charged capacitor to inject a negative current into the load path and is generally faster than the passive equivalent one. In both configurations, Metal Oxide Arresters (MOA) or else, Surge Arresters (SA), are placed in the absorption path. The current is commutated to the absorption path when the threshold voltage of the SAs is exceeded (1.2-1.5 Vdc) and subsequently, the CB voltage rises rapidly. The fault current starts to drop when the voltage across the breaker is larger than the system voltage. A fast acting switch or residual current device (RCD) might be included in front of the main hybrid breaker to eliminate the residual

current flowing through the arrester banks. Recent advancements in mechanical DCCBs have led to implementations with an opening time of 7-10 ms and an interrupting capability of 16 kA [77, 78]. Furthermore, 160 kV active injection mechanical DCCBs have been installed in Nan'ao multiterminal HVDC system, which achieve fault current interruption in less than 5 ms with interrupting capability of 9.2 kA [79].

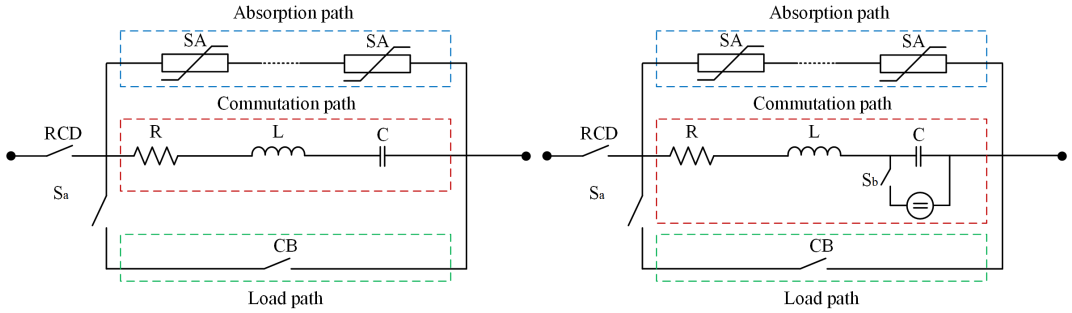


Figure 2.13: a) Passive and b) Active Mechanical DC breakers.

2.5.2 Solid-state Circuit Breakers

The relatively high interruption time of mechanical DCCBs can be significantly reduced if solid state DCCBs are utilised. A typical solid-state DCCB is shown in Figure 2.14 which is based on quick power semiconductor devices such as IGBTs or Gate Turn-Off thyristors (GTOs). This breaker technology relies on the placement of power electronic switches in the main breaker unit which is also part of the main conduction path, hence resulting in high costs and constant on-state losses [75]. The power electronic devices can switch off rapidly and upon their deactivation the fault current is commutated first to the parallel snubber circuits, which are responsible for equal voltage sharing between the IGBTs/GTOs during current breaking. Finally, similar to the mechanical breakers, the current is commutated to the SAs in the absorption path to be extinguished.

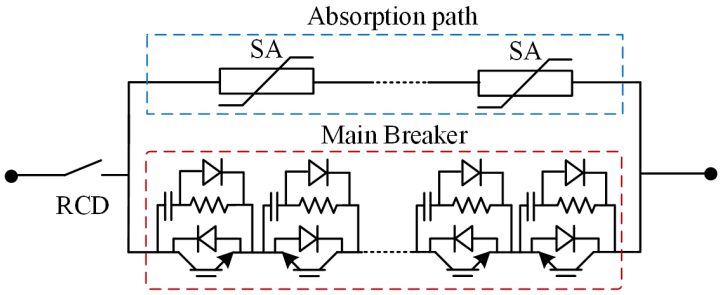


Figure 2.14: Solid-state DC breaker.

Due to their increased losses, solid-state DC breakers have not been used in HVDC applications even though the decrease in fault current interruption time is substantial, i.e. less than 1 ms [75]. Potential future developments in solid state device technology such as, reduction of on-state device forward voltage, may lead to their integration in HVDC grids.

2.5.3 Hybrid Circuit Breakers

Towards the aim of reducing the on-state losses of solid-state breakers, certain proposals were made to use fast-acting mechanical switches in the main branch, thus creating a hybrid topology. A typical hybrid DC breaker (Figure 2.15) consists of the load path, the commutation path and the absorption path, with the latter two forming the main current interruption unit [80].

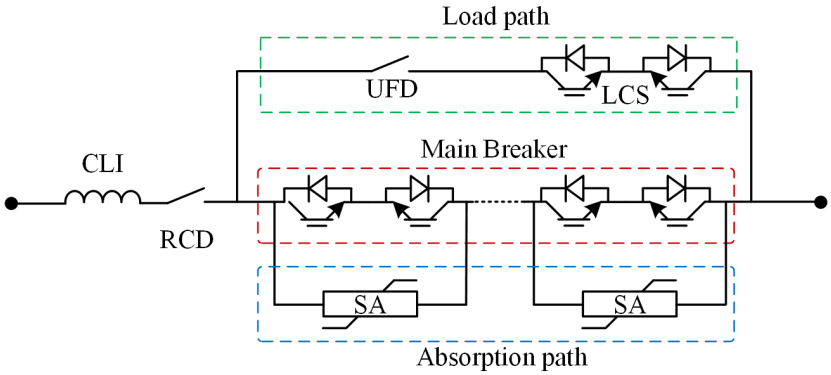


Figure 2.15: Typical hybrid HVDC breaker.

The main load path through which the DC current flows under steady state condition consists of a mechanical Ultra-Fast Disconnector (UFD) in series with a low voltage semiconductor switch referred to as Load Commutation Switch (LCS). The main breaker unit or auxiliary branch is designed to carry the fault current for a limited period, and it consists of several power electronic switches. When the fault is detected, the low voltage switch in the main load path is turned off while the power electronics components of the main breaker are switched on and consequently the fault current is commutated to the main breaker path, allowing the mechanical disconnector to open at almost zero current. Nevertheless, the breaker needs to dissipate the inductive energy that drives the fault current and hence, the absorption branch is employed to provide a back-emf of greater magnitude than the rated system voltage that drives quickly the DC current to zero using SA banks [80]. As in most DCCBs, a current limiting inductor (CLI) is placed in series with the hybrid breaker to limit the magnitude of the fault currents.

This breaker configuration combines the low steady-state losses of mechanical DCCBs with the short current interruption times of solid-state breakers. Nevertheless, the hybrid DCCB topology cannot interrupt the fault current as fast as the solid-state breaker, since after commutation of the fault current to the main breaker unit, the DCCB cannot interrupt the fault current until the UFD has established sufficient dielectric strength to withstand the transient recovery voltage. Recent developments in HVDC breakers have led to interruption times of 2-3 ms and current breaking capabilities of 15-25 kA [72, 74]. Finally, a 500 kV hybrid DCCB prototype has been developed and installed in Zhangbei HVDC grid in China that demonstrates a breaker operation speed of 2.6 ms and 26 kA maximum breaking capacity [24].

2.5.4 DC Circuit Breaker Modelling

For DC fault studies in HVDC grids, if monitoring of the internal DCCB components is not a requirement, a simplified DCCB model can be used. The basic functionality of a DC circuit breaker is to introduce a counter-voltage that drives the fault current to zero and to dissipate the energy that is stored in the DC system during DC faults. In addition, each DCCB technology has its own breaker operation speed.

A simplified DCCB model that achieves the above functionalities is shown in Figure 2.16 [81]. This model comprises of a switch in parallel with a surge arrester that is responsible for providing the counter-voltage and absorbing the energy in the DC grid. The switch is simulated to open after a certain time delay has elapsed from the generation of a trip command, which can be issued either by a protection relay or by the breaker itself (e.g. self-protection in case of over-current). The time delay can be flexibly adjusted to mimic the operation of hybrid DCCBs (2-3 ms), mechanical DCCBs (7-10ms) or any other DCCB technology. It is worth noting that most EMT-type software, like PSCAD/EMTDC, offer the capability to model several other parameters related to circuit breakers, such as the on-state losses, maximum current breaking capacity, residual current for current interruption etc.

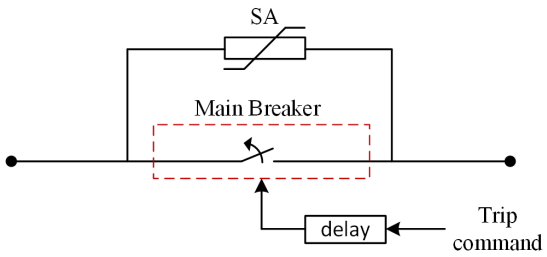


Figure 2.16: Simplified model for HV DCCBs.

2.6 Transmission Line Models

DC overhead lines and cables can both be used for HVDC power transmission, however, due to the fact that HVDC technology is widely used for the integration of offshore wind energy, DC cables have been installed in the vast majority of existing VSC-based HVDC systems. The most notable exceptions are the Zhangbei HVDC grid [24] and the ULTRANET project [82], which incorporate overhead lines.

The two main types that are commonly used for HVDC cable transmission are the mass-impregnated and the extruded cables [6]. The latter are typically polymeric cables with cross-linked polyethylene (XLPE) as the main insulating material. XPLE cables are particularly well-suited for VSC-HVDC transmission, in which power can be transferred bidirectionally without changing the voltage polarity, while in addition they offer several advantages such as, simpler construction, lower cost and higher power rating per mass when compared to mass-impregnated cables [83].

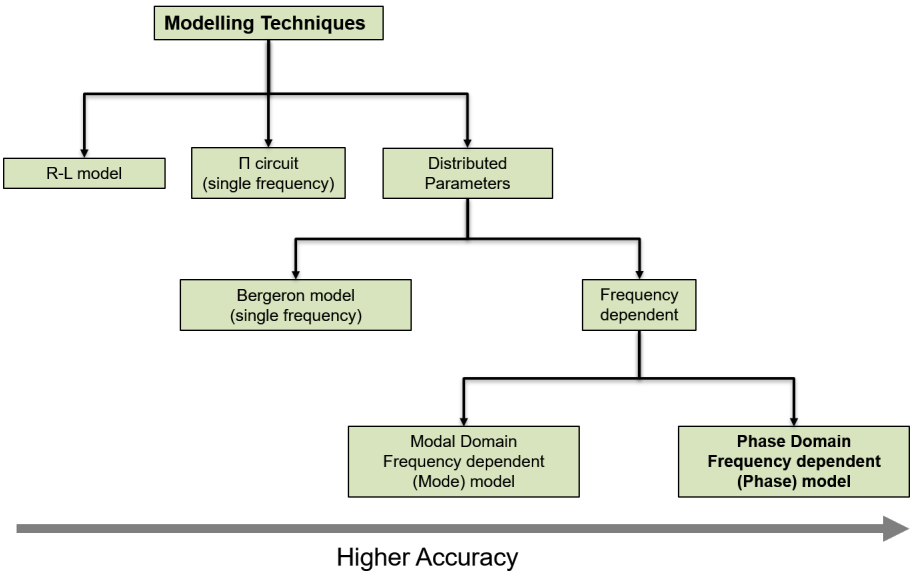


Figure 2.17: Transmission line models.

Accurate representation of the transmission lines is of paramount importance for the conduction of transient simulation analysis. Depending on the power system study and the required degree of accuracy, several transmission line models can be employed for conducting such studies. The available models are summarised in Figure 2.17. The simplest transmission line representation is the R-L model, in which the capacitance is neglected or considered to be of minimal significance with respect to the nature of the simulation study. Lumped resistance and inductance are placed in series to simulate the total impedance of the line. This model is appropriate mainly for load

flow studies, while it has also been widely used for transient studies in LVDC systems where the cable capacitance is negligible, and the length of the feeder is limited to a few kilometres. Alternatively, a Π model can be used in which the capacitance of the transmission medium is also taken into account and is split into two equal components lumped at both ends of the medium. Π-sections provide a simplified means of representing transmission systems for steady-state studies. This model can be suitable for the investigation of interactions between a power system and control systems [84].

2.6.1 Distributed Parameter Models

For HVDC systems, especially those that include undersea cables, the capacitance plays a pivotal role in the transmission medium behaviour especially under fault conditions and therefore, models that incorporate such elements are required. Moreover, for the investigation of transient phenomena in HVDC systems, such as DC faults, transmission line models that operate on the travelling wave principles are desirable. Travelling waves that are generated at the point a disturbance occurs, propagate in both directions of the medium (e.g. assuming a DC fault at some point across a DC cable) with a finite propagation velocity that depends on the medium geometry. Hence, not all points of the transmission system experience the effect of the disturbance at the same time. This is the reason why distributed parameter representation is generally preferred against circuits with lumped components due to the increased lengths associated with HVDC transmission lines and cables.

One such model can be developed by cascading several Π sections in series to simulate the distributed behaviour of the medium. This type of model is only appropriate for very short line segments, where travelling wave-based models cannot be used due to time step constraints.

Another distributed parameter model is the Bergeron model (Figure 2.18), which can be considered as equivalent to the cascaded Π sections model with infinite sections with the exception that the line losses are approximated by lumped resistances. In particular, the 'lossless' distributed parameter line is split into two segments, both of which are terminated by a R/4 resistance at each end. The Bergeron model is generally preferred against the Π model for the representation of transmission systems with over 15 km in length [84]. However, in its basic configuration, the Bergeron model can represent transmission system parameters at a single frequency and therefore, it is only appropriate for studies where frequencies other than the fundamental are of little concern. Models that assume constant parameters (single frequency) cannot adequately simulate the response of a transmission line over the wide range of frequencies that are present in the signals during transient conditions (including DC faults).

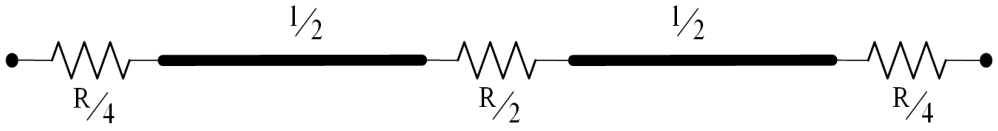


Figure 2.18: Bergeron model.

2.6.2 Frequency Dependent Models

One of the most important aspects that needs to be taken into account in the modelling of DC cables and overhead lines is the frequency behaviour of the system parameters. The resistive and inductive components of the medium are heavily dependent on frequency and have different values depending on system conditions (steady state, fault conditions etc.). Frequency dependent models are thus required to adequately simulate the response of a transmission medium over a wide frequency range. This can be achieved by solving the equivalent system equations at various frequency points.

Frequency dependent transmission line models can be further divided into Modal Domain and Phase Domain frequency dependent models. The former utilises a constant frequency-independent modal transformation matrix to decouple multi-conductor systems into separate modes through modal decomposition techniques [85, 86]. In this way, each mode can be treated as a single conductor. This model provides accurate results for geometrically balanced transmission systems but is deemed unreliable for systems with unbalanced line geometry. Moreover, in cable systems, the frequency dependency of the modal transformation matrices cannot be neglected.

The drawbacks of the modal domain model are addressed by the phase domain frequency dependent model. Despite the increased computational burden, distributed parameter frequency dependent phase model can be used to model any type of transmission medium with satisfactory accuracy [87, 88]. The phase domain model operates on the basic principle that the frequency dependence of the medium can be sufficiently described by two matrix transfer functions: i) the propagation function H and ii) the characteristic admittance Y_c. The frequency dependency of functions H and Y_c can be approximated by calculating their values at various points in the phase domain to derive a set of frequency domain response points. The sets are in turn approximated by low-order rational functions using weighted vector fitting techniques. The frequency domain model can then be used to create a time domain model with high accuracy.

Owing to the high fidelity offered by the phase domain frequency dependent model in representing any line or cable geometry, this approach is selected for modelling the DC transmission mediums for the purposes of the transient simulation analyses conducted in this thesis. In addition, the mathematical formulation of this model is

utilised for the design of the HVDC protection and fault location solutions presented in later chapters. Therefore, the process for deriving the functions H and Y_c is described in detail in the following subsection.

2.6.3 Mathematical Formulation

Any transmission medium can be described as a multi-conductor system with n conductors of length l, as shown in Figure 2.19, which also illustrates the voltages at both ends of the lines.

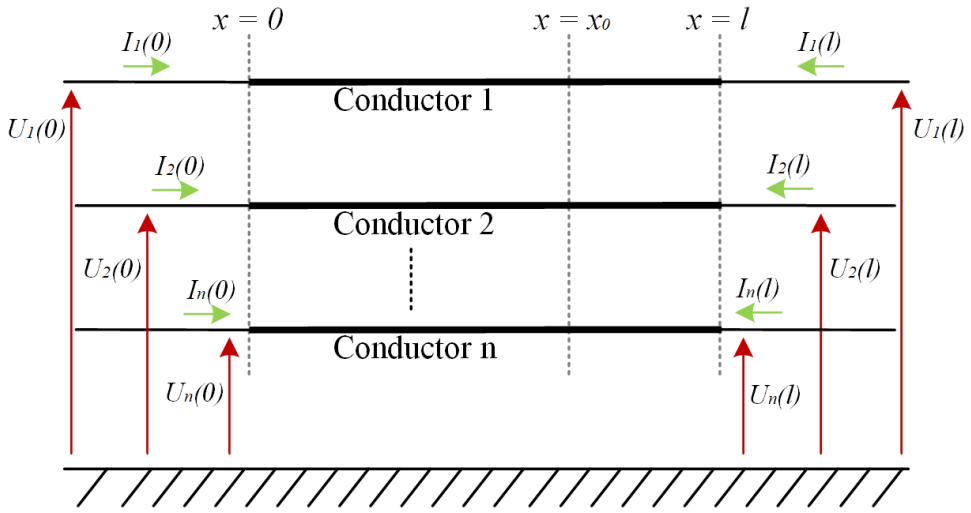


Figure 2.19: Multi-conductor transmission system.

To facilitate the analysis in this section, a small dx section of a single conductor at an arbitrary location x_0 is used (shown in Figure 2.20) in which Rdx, Ldx, Cdx and Gdx represent the per-unit length resistance, inductance, capacitance and admittance of the conductor.

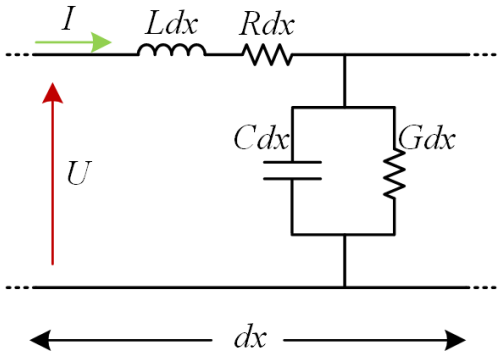


Figure 2.20: Transmission line section.

Assuming U as the voltage across the section dx, and I as the current flowing through section dx, the line equations in the frequency domain can be expressed as [89]:

$$\frac{dU}{dx} = -(R + j\omega L)I = -Z_s I \tag{2.6}$$

$$\frac{dI}{dx} = -(G + j\omega C)I = -Y_s I \tag{2.7}$$

where Y_s is the per-unit-length shunt admittance matrix and Z_s is the per-unit length series impedance, which are dependent on the line or cable geometry. These are nxn matrices in which the diagonal elements correspond to each conductor and the off-diagonal elements represent the coupling between different conductors. Moreover, U and I are column vectors with a dimension of nx1 that represent the voltage and current at each conductor at the arbitrary location x, respectively. Combining the above equations, the voltage and current propagation equations can be obtained:

$$\frac{d^2U}{dx} = (Z_s Y_s)U \tag{2.8}$$

$$\frac{d^2I}{dx} = (Y_s Z_s)I \tag{2.9}$$

The solution of equations (2.8) and (2.9) lead to:

$$V_x = e^{-\gamma x} I^+ + e^{+\gamma x} I^- \tag{2.10}$$

$$I_x = e^{-\gamma x} V^+ + e^{+\gamma x} V^- \tag{2.11}$$

where I^+ and V^+ are the forward current and voltage travelling waves, I^- and $V^-$are the backward current and voltage travelling waves, and $\gamma = \sqrt{Z_s Y_s}$ is the propagation constant that represents the attenuation travelling waves experience while travelling through the transmission system. The relation between voltage and current waves is given by:

$$V_x = Z_c(e^{-\gamma x} I^+ - e^{+\gamma x} I^-) = Y_c^{-1}(e^{-\gamma x} I^+ - e^{+\gamma x} I^-) \tag{2.12}$$

in which Y_c is the characteristic admittance, Z_c is the characteristic impedance, and H is the propagation function, which are calculated based on Z_s and Y_s as [90]:

$$
\begin{aligned}
Y_c &= \sqrt{(Z_s Y_s)^{-1}} Y_s \\
Z_c &= \sqrt{\frac{Z_s}{Y_s}} \\
H &= e^{-\sqrt{Y_s Z_s} l}
\end{aligned}
\tag{2.13}
$$

Transients Line Model

For the analysis of electromagnetic transients in transmission lines in time domain simulations, the equivalent circuit of Figure 2.21 can be used, in which a single conductor is considered [85, 91]. Assuming that the travelling time of the waves is greater than the simulation time step $\Delta\tau$, the model makes use of the decoupling effect between the sending and the receiving end of the transmission line.

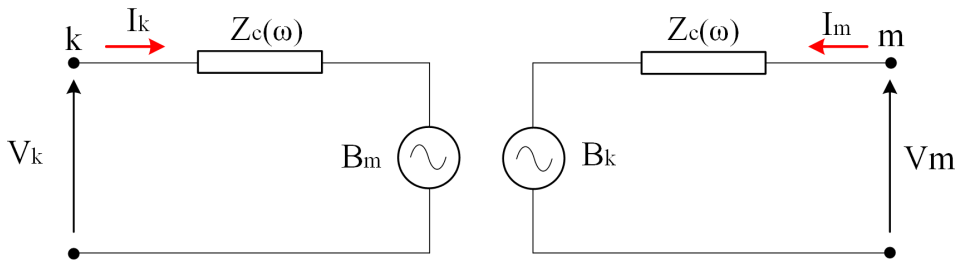


Figure 2.21: Frequency domain transients line model.

Based on the travelling wave principles, the forward waves (waves that have the same direction as currents I_k and I_m) at each line end can be expressed as:

$$F_k = V_k + Z_c I_k \tag{2.14}$$

$$F_m = V_m + Z_c I_m \tag{2.15}$$

The voltage sources B_m and B_k can be related to the forward travelling waves as follows:

$$B_m = H(V_m + Z_c I_m) \tag{2.16}$$

$$B_k = H(V_k + Z_c I_k) \tag{2.17}$$

The above equations can be interpreted as follows: taking as an example equation (2.16), the source B_m transmits a current and voltage at node k (given by equation (2.17)), onto node m but influenced by the propagation function H.

In the frequency domain, the voltage/current relationship at both ends of the line are related to each other through the following formulas:

$$I_k = Y_c V_k - H(Y_c V_m + I_m) \tag{2.18}$$

$$I_m = Y_c V_m - H(Y_c V_k + I_k) \tag{2.19}$$

The meaning of these equations is that the waves which enter the transmission line at one of its ends, appear at the other end influenced by the propagation function H. Generally, the propagation function consists of both real and imaginary parts, which describe the attenuation and the delay travelling waves experience while propagating across the transmission medium. Migration of these equations to the time domain yields:

$$i_k = y_c * v_k - h * u_m \tag{2.20}$$

$$i_m = y_c * v_m - h * u_k \tag{2.21}$$

where the symbol $(*)$ denotes the mathematical operation of convolution. In theory, numeric convolution using the time-domain counterparts of the characteristic admittance and the propagation functions is feasible, but the solution is computationally inefficient and time consuming. The modelling of the transmission line becomes more efficient and easier when the solution is modulated in the phase domain. The propagation function H is first fitted in the modal domain and followingly, the results are used for fitting in the phase domain. On the other hand, the elements of the characteristic admittance Y_c are a smooth function of frequency and can be directly fitted in the phase domain [87]. The approximation of the two functions with low order rational functions in the phase domain facilitates the migration to the time domain through means of recursive implementation of convolutions [92].

Vector Fitting

The method that is used for the low-order rational fitting is called vector fitting [92,93]. The objective of this technique is to obtain a function of the form:

$$f(s) = d + sh + \sum_{n=1}^{N} \frac{c_n}{s - p_n} \tag{2.22}$$

in which p_n are the poles and c_n are the residues of the function, while d and h are constant numbers. This non-linear problem can be solved in a least square sense. Assuming an initial reasonable set of poles $\widetilde{p_n}$, an auxiliary underdetermined function $\sigma(s)$ is assumed and expressed as [84, 89]:

$$\sigma(s) = \sum_{n=1}^{N} \frac{\widetilde{c_n}}{s - \widetilde{p_n}} + 1 \tag{2.23}$$

Moreover, the function $F(s)$, which serves as an approximation to $f(s)$ is given by:

$$\begin{aligned} F(s) = \sigma(s) \cdot f(s) = d + sh + \sum_{n=1}^{N} \frac{c_n}{s - \widetilde{p_n}} \\ \implies \left(d + sh + \sum_{n=1}^{N} \frac{c_n}{s - \widetilde{p_n}} \right) = \left(\sum_{n=1}^{N} \frac{\widetilde{c_n}}{s - \widetilde{p_n}} + 1 \right) \cdot f(s) \end{aligned} \tag{2.24}$$

or equivalently:

$$d + sh + \sum_{n=1}^{N} \frac{c_n}{s - \widetilde{p_n}} - \sum_{n=1}^{N} \frac{\widetilde{c_n}}{s - \widetilde{p_n}} f(s) = f(s) \tag{2.25}$$

Selecting M frequency points over the frequency spectrum of interest (typically from DC to 1 MHz), M equations of the form given in (2.24) can be written in the form of $A \cdot x = B$. For the k^{th} element ($s_k = j\omega_k$ with $K \leq M$), A, x and B matrices are defined as:

$$\begin{aligned} A_k = \left[\frac{1}{s_k - \widetilde{p_1}}, ..., \frac{1}{s_k - \widetilde{p_n}}, 1, s_k, \frac{-f(s_k)}{s_k - \widetilde{p_1}}, ..., \frac{-f(s_k)}{s_k - \widetilde{p_n}} \right] \\ x = [c_1, c_2, ..., c_n, d, h, \widetilde{c_1}, \widetilde{c_2}, ..., \widetilde{c_n}] \\ B_k = f(s_k) \end{aligned} \tag{2.26}$$

where B is a vector with M elements which correspond to the response of the propagation function in the phase domain at the corresponding frequency points. M also corresponds to the number of rows of matrices A and B, which are Mx($2N$+2) matrices. Provided that the number of frequency points is higher than $2N$+2, then we have an overdetermined system with more equations than unknowns. Therefore, this system can be solved as a least squares problem.

Moreover, equation (2.24) can also be written as:

$$(\sigma f)_{fit}(s) = \sigma_{fit}(s) \cdot f(s) \tag{2.27}$$

Solving in terms of f(s) we get:

$$\begin{aligned} f(s) &= \frac{(\sigma f)_{fit}(s)}{\sigma_{fit}(s)} \\ \implies f(s) &= \frac{\prod_{n=1}^{N}(s-c_n)}{\prod_{n=1}^{N}(s-\widetilde{c_n})} \end{aligned} \tag{2.28}$$

Hence, the poles of $f(s)$ are the zeroes of $\sigma(s)$ and the initial estimates of poles cancel out. Therefore, the poles of $f(s)$ are determined more efficiently by instead solving the zeros of $\sigma(s)$. The same procedure can be used to solve for the residues c_n of f(s). If a zero of $\sigma(s)$ has a positive real part, it is reversed to a negative value [84].

Propagation Function Fitting

For a multi-conductor system, the propagation function matrix contains several propagation modes that are characterised by different modal propagation delays. Therefore, the frequency dependent phase domain model uses a multiple-delay approach. In doing so, the decoupled modes of the propagation function are obtained in order to derive the corresponding modal delays. Then, a solution is obtained in the modal domain and the results are used for fitting the propagation function in the phase domain. This procedure can be performed analytically in the following three steps [88, 94].

Step 1

The modes of the propagation function $H(s) = e^{-\sqrt{YsZsl}}$ are calculated with the use of a frequency dependent transformation matrix T that is derived using the Newton-Raphson approach as described in [95]. Then, the time delays for each mode are extracted. Modes with very similar time delays are replaced by a single mode that represents the average of the grouped time delays to effectively reduce the total number of modes and increase the speed of the curve fitting technique for $H(s)$.

The new time delays of the grouped modes are then used to 'back-wind' each respective delay group. The back-wound modal propagation function is then fitted as follows [84, 96]:

$$e^{-s\tau}H_i^m = \sum_{n=1}^{N}\frac{c_n}{s-p_n} \tag{2.29}$$

where τ is the calculated modal delay and H_i^m is the propagation function in the modal domain.

Alternatively, a real constant modal transformation matrix evaluated at a high frequency (e.g. 1 MHz) can be used without significantly impacting the accuracy of the method [94]. In particular, based on the per unit series impedance and shunt

admittance of the cable, the following nearly diagonal matrix is calculated:

$$\overline{\Lambda} = T_{\infty}^{-1} Y_s Z_s T_{\infty} \tag{2.30}$$

in which T_{∞} is an approximation of the modal transformation matrix.

Step 2

Next, the off-diagonal elements of matrix $\overline{\Lambda}$, are discarded to obtain matrix $\hat{\Lambda}$. For each diagonal element of this matrix, a delay time is extracted and used for the fitting in the modal domain of the corresponding diagonal element i in $H_i^m(s) = e^{-\sqrt{\hat{\Lambda}}l}$.

Step 3

The calculated poles from step 2 are used as starting poles for fitting $H(s)$ in the phase domain, while the calculated residues are discarded. In this case $H(s)$ is expressed in a similar manner as equation (2.22). The final propagation function is given by:

$$H(s) = \sum_{m=1}^{q_m} \left(\sum_{n=1}^{N} \frac{\bar{\bar{c}}_n}{s - p_n} \right) e^{-s\tau_m} \tag{2.31}$$

where q_m is the number of group delays, N is the order of the transfer function and τ_m is the modal time delay of group m. The residues $\bar{\bar{c}}_n$ of the propagation function are calculated for each group delay by solving the least squares problem as explained in the previous section.

Characteristic Admittance Fitting

The elements of the characteristic admittance matrix Y_c are generally smooth functions of frequency and therefore, the application of vector fitting directly in the phase domain is possible by approximating each element by M^{th} order rational functions [87]. In particular, all matrix elements share the same set of poles but different residues. This can be mathematically expressed for each element (i, j) of the matrix as:

$$Y_{c(i,j)}(s) = d_{(i,j)} + \sum_{n=1}^{M} \frac{c_{n(i,j)}}{s - p_n} \tag{2.32}$$

2.7 DC Voltage and Current Measurement

Reliability and accuracy of DC voltage and current measurement are significant requirements for HVDC control and protection purposes. Therefore, voltage and current sensors are essential in modern HVDC switchgear and their primary aim is to provide

to protection relays low amplitude signals, which should be accurate representations of the original measurements. Figure 2.22 illustrates the schematic block diagram of a typical measuring instrument. The high voltage setup comprises of a primary sensor and its associated primary converter, which sends the current or voltage measurements by means of a transmitting system to the secondary converter. The sampled values are converted by the secondary transformer into either low energy analogue, high-energy analogue or digital signal for further processing within the protective relays [97, 98]. For digital interfaces, the output of the measuring instrument is sent to a merging unit that is responsible for reformatting the signals in a form that can be used by the protection relays. The rest of this section describes the main voltage and current measuring instruments that are typically employed in HVDC applications.

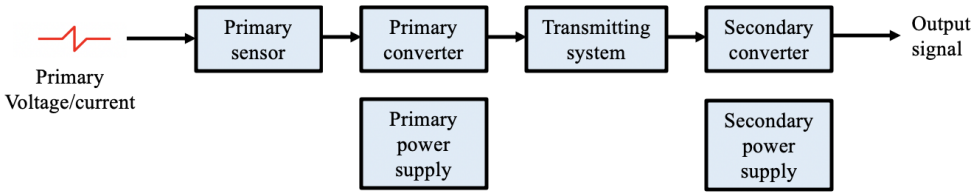


Figure 2.22: Schematic block diagram of measuring instruments [99].

2.7.1 Voltage Measuring Technologies

Resistive-Capacitive Voltage Divider

In VSC-based HVDC systems, measurement of voltage is usually obtained using a resistive-capacitive voltage divider [6], as shown in Figure 2.23. The resistors connected in parallel to the capacitors are designed to guarantee an extremely low resistance variation through time, electrical stress and temperature [100]. Single- or double-shielded coaxial cables are used to transmit pulses from one end to another, preserving the information in the signal. To prevent any possible reflection phenomena (occurring mainly during fast transients), the coaxial cable is usually terminated with an external burden impedance. Resistive-capacitive voltage dividers output an accurate voltage representation over a wide frequency band (typically from DC up to 500 kHz) [100,101].

Considering the design depicted in Figure 2.23, the voltage V_2 obtained at the low-voltage side of the RC divider can be given by:

$$\frac{V_2}{V_{dc}} = \frac{R_2}{R_2 + R_1 \frac{1+R_2 j\omega C_2}{1+R_1 j\omega C_1}} = \frac{C_1}{C_1 + C_2 \frac{1+1/R_2 j\omega C_2}{1+1/R_1 j\omega C_1}} \tag{2.33}$$

Expression in (2.33) is valid considering that the following design criterion is met:

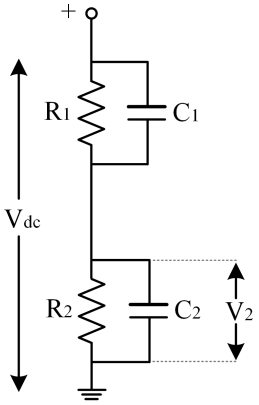


Figure 2.23: Resistive-capacitive voltage divider.

$$R_1 \cdot C_1 = R_2 \cdot C_2 \tag{2.34}$$

The features of RC dividers which make them a very compelling option for measurement of voltage are listed below [100, 101]:

- Excellent transient characteristics
- Conform to microprocessor-based secondary technology
- Ferroresonance-free (for saturable cores)
- Short-circuit proof design
- Disconnection during commissioning tests on site not necessary, e.g. in case of DC-tests (cable tests)
- Significant size and weight reduction

Optical Voltage Sensors

An optical electric sensing technology which is suited for high voltage measurements in DC applications based on Pockels effects is presented in [98, 102–105]. Such optical voltage sensors are used in applications where a wide frequency range is required and overcome some shortcomings of the conventional voltage sensors while using simpler structure and presenting better accuracy. Specifically, an optical sensing system based on the combination of the longitudinal Pockels effect and the optical technology is reported in [102]. The sensing scheme is used for measuring high-voltage levels up to 400 kV in a wide frequency range between DC to 30 MHz. In addition, [103] presents an improved optical HVDC measuring system using a Pockels crystal in a longitudinal

modulation arrangement and two-wavelength laser systems in order to expand the measurable voltage. The developed system is used for directly measuring high voltages up to 450 kV in the DC to GHz frequency range.

However, the use of the aforementioned sensing technology for DC voltage measurements includes some uncertainties which are influenced by many factors such as the light source, the current-to-voltage converter and the unwanted cross electric field [102]. Furthermore, some technical challenges which have to be addressed include:

- The moving electric charges in the crystal causes drift of the output intensity of the light sources
- The modulated signal of the DC voltage is difficult to be distinguished from the light intensity

2.7.2 Current Measuring Technologies

The main current measuring technologies that are currently available and appropriate for HVDC applications are depicted in Figure 2.24. This subsection describes in detail the various current sensing techniques while special emphasis is paid on their suitability with respect to the current measurement range, accuracy and bandwidth.

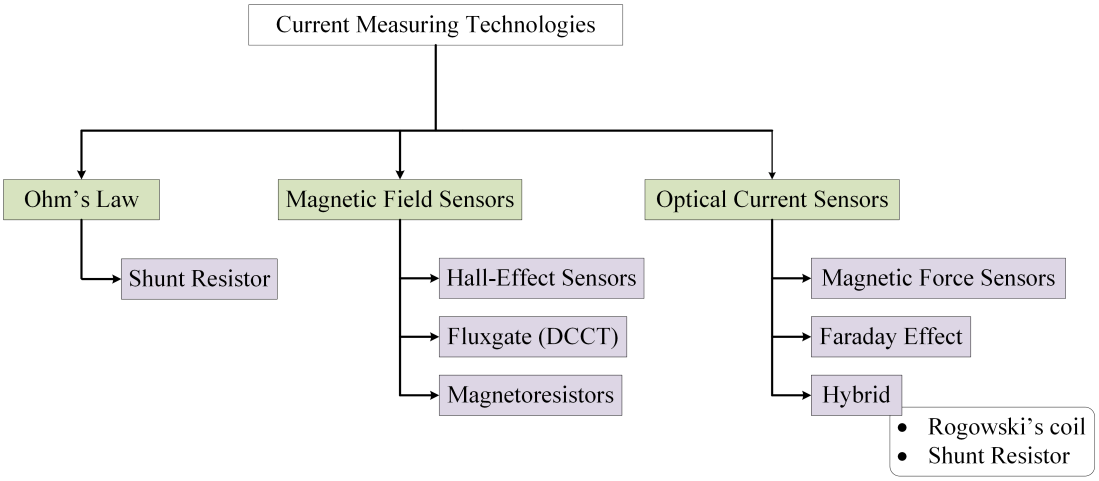


Figure 2.24: Classification of current measuring technologies.

Ohms Law - Shunt Resistor

The well-known Ohm's law states that the current that flows through a resistor is analogous to the voltage drop across this resistor. A simple means of current measurement is the use of a shunt resistor with low ohmic value that is directly connected into the main current conduction path. The voltage that is measured at the pins of the resistor

represents a proportional measure of the current that flows in the circuit. Because of the direct integration into the main circuit, shunt resistor can generate substantial power losses and reduced efficiency, especially in high current applications (losses are proportional to the square of the measured current).

This sensing technology is relatively simple, reliable and is applicable for both AC and DC technologies with a measurement bandwidth up to several MHz [106]. A number of factors can affect accuracy performance, such as temperature effects, mechanical forces and thermoelectric voltages. From the several available implementations, the squirrel cage shunt that consists of parallel manganese and copper bars is suitable for high current applications due to its low thermoelectric voltage and temperature coefficient [107]. Moreover, the impedance of the shunt can increase as frequency increases due to the proximity and skin effect. [108,109]. The frequency dependent characteristic of the shunt can be mitigated by suitable selection of the radius of the conductors and the distance between the conductors [110]. However, the lack of galvanic isolation is the main disadvantage of shunt resistors.

Magnetic Field Sensors

Conventional AC current sensors based on Faraday's law of induction, such as current transformer (CT) and Rogowski coil, are not capable of sensing static magnetic fields. On the contrary, magnetic field sensors can recognise and respond to static magnetic fields. Moreover, CT and Rogowski coil perform remarkably well in the high frequency regions, while magnetic field sensors perform better for lower frequencies. Therefore, it makes sense to combine conventional current sensors with magnetic field sensors in order to build a sensor with an extended bandwidth from DC to several MHz. The effect of this is illustrated in Figure 2.25.

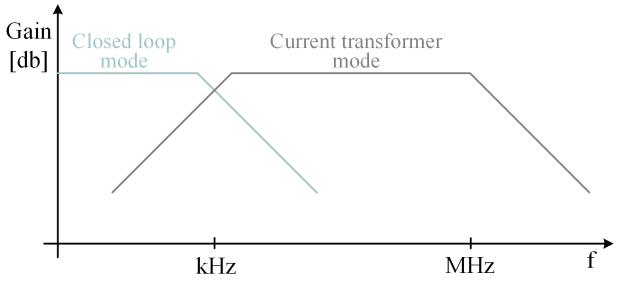


Figure 2.25: Typical illustration of bandwidth for closed-loop and CT mode.

There are three main categories of magnetic field sensors: a) hall-effect sensors, b) sensors based on the fluxgate principle and c) magnetoresistors. All three of them can be used in an open loop or in a closed loop sensing configuration. In the open loop

technology, the field sensor can be placed in the vicinity of the main current carrying conductor or alternatively, a magnetic core is used to concentrate the magnetic field generated from the enclosed conductor onto the magnetic field sensor that is situated in the airgap of the core material. The former is susceptible to the skin effect and external magnetic fields, while in the latter configuration the sensitivity is substantially improved due to the high magnetic permeability of the core material, and the skin effect is eliminated. Additional limiting factors for both topologies are the relatively low bandwidth of the sensors and the significant thermal drift of the sensing element [111]. Nevertheless, the open loop configuration provides a simple and cost-effective solution.

In the closed loop configuration, the output voltage of the magnetic field sensor is used as a feedback control signal to drive a compensating current in a secondary winding that is wound in the magnetic core to counter the magnetic flux that is generated by the primary current. This results in a zero-flux transducer. With the use of a secondary winding, the transducer operates as a current transformer in the high frequency region, resulting in extended bandwidth [112]. The closed loop sensing configuration reduces significantly or eliminates the thermal drift and dramatically improves the performance of the sensor [113]. Complexity and extra cost are the limitations of this technology.
Hall-effect sensor is the most widely used magnetic field sensor. It is based on the hall effect that is illustrated in Figure 2.26.

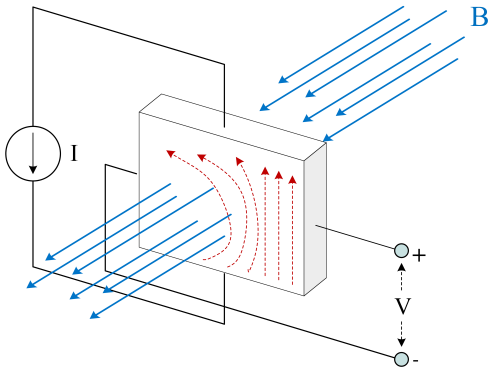


Figure 2.26: Illustration of Hall effect through a conductive material.

The effect describes that when a current flows through a conductive material in the presence of a magnetic flux density that cuts through the surface of the conductor, then a voltage is induced that is perpendicular to both the magnetic field and the current. The effect can be described mathematically as:

$$V = \frac{IB}{nqd} \tag{2.35}$$

where q is the charge of each electron, n is the charge carrier density, and d is the

thickness of the conductive material. Although the hall effect is very small in metallic conductors, the effect is enhanced when semi-conductors are used [114].

Hall-effect sensors can be used in both open-loop and close-loop configuration. Closed loop transducers, also called Hall effect compensated, or zero flux transformers are commonly used for the measurement of DC current in HVDC applications [6, 101]. A typical structure of the transformer can be seen in Figure 2.27 [115], which consists of a magnetic core, a Hall sensor, an operational amplifier (OP) and a compensating winding.

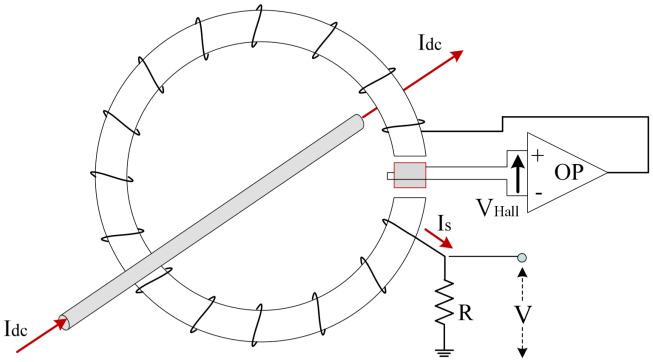


Figure 2.27: Zero flux DC current transformer.

When primary current I_{dc} flows through the magnetic core, it generates a magnetic field B that induces a voltage V_{Hall} at the sensor output, which is almost proportional to the magnetic field, which in turn is proportional to the current to be measured. The primary current I_{dc} is compensated with current I_s fed to the compensating winding which results in zero flux ($B = 0$) in the magnetic core. If now the primary current contains a DC component, the current proportional to this is fed to the positive input of the OP. The resulting compensation current I_s is a true-to-scale, galvanically-separated copy of the primary current [116]. Depending on the type of construction of the DC transformers, bandwidths of up to 500 kHz at currents of maximum 5 kA, and up to 10 kHz at currents of maximum 25 kA can be attained [113, 117]. An alternative configuration based on the combination of hall-effect sensor with a Rogowski coil that achieves a bandwidth of 75 MHz has been reported in [118].

Fluxgate sensors refer to the sensor family that employs the fluxgate working principle, which is essentially based on the detection of the inductance change in the sensing element [113]. In its simplest form, a fluxgate transducer can be built in a similar manner with a hall-effect based current transducer (Figure 2.28), where the hall-effect sensor is replaced with a fluxgate element. The sensing element comprises a coil that is wound around a thin magnetic core. The underlying principle of this sensor depends on the detection of a change in the inductance of the coil.

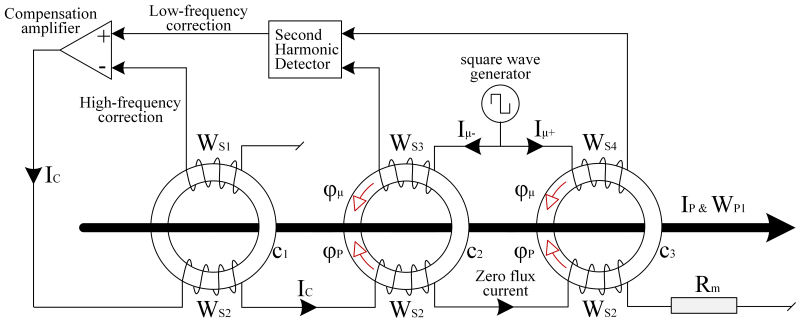


Figure 2.28: Closed-loop fluxgate transducer.

The non-linear relationship between the magnetic flux density B and the field H for a magnetic material is utilised by the fluxgate technology. The value of the inductance of the sensing element is dependent on the magnetic permeability of the core. When the flux density is high the inductance increases, while when the flux density is low the inductance decreases.

The fluxgate element is designed in such a way that its saturation level varies with respect to the applied external field B_{ext}, produced by the primary current I_P, which provokes a change in the magnetic permeability of the core and hence, the inductance. Moreover, a current that is injected into the coil of the fluxgate element produces an additional magnetic field H_0 that also affects the inductance of the element. The frequency of the injected current can be increased to improve the accuracy of the sensor [111]. The two magnetic fields may add or counter each other. Thus, the fluxgate transducer is developed in a way that near zero total flux corresponds to low inductance, and high flux leads to core saturation and high inductance.

Various fluxgate transducers have been designed that use either open loop or closed loop configuration [119, 120]. In the closed loop configuration, the variation of the inductance of the fluxgate element is measured and processed by adequately designed electronics to manipulate the injected current with the aim to operate the core under zero flux condition [121]. Subsequently, the measured current can be simply calculated based on the turns ratio. Figure 2.28 presents a closed-loop fluxgate transducer that has been manufactured by LEM [113]. In this configuration three magnetic cores are used with separate secondary windings, a common primary winding (current carrying conductor) and a common compensation winding.

The closed-loop configuration is achieved with the injection of current I_c that flows in compensation windings. The transducer operates as a fluxgate sensor for low frequencies with W_{S3} and W_{S4} serving as the fluxgate elements, and as a current transformer in the high frequency region (W_{S1} and W_{S2}). The transducer achieves very high accuracy and extended bandwidth from DC to 100 kHz.

Magnetoresistors (MR) make use of the magneto-resistance effect, which describes the tendency of some materials, to vary the value of their resistance under the influence of an external field. MR sensors are developed based on metal alloys and present better sensitivity, measurement accuracy and higher bandwidth as opposed to hall-effect based sensors [122]. This effect has been successfully used for the construction of read heads in magnetic recording but in the recent past, they have been examined for DC current measurement applications [114, 123–125]. Based on the magneto-resistance effect, several kinds of magnetic field sensors have been designed and three of the most appropriate ones for DC current measurement are subsequently described.

- Anisotropic Magneto-Resistance (AMR) Sensors: Within the family of MR sensors, AMR sensors is the most mature technology. The term anisotropic derives from the sensor's dependence on the angle between magnetisation direction and the measured electrical current. The angle between these two affects the resistance of the ferromagnetic material and depends on the magnitude of the field. The resistance is at its maximum when the primary current flows in parallel with the magnetisation and at its minimum when the current is perpendicular to the magnetisation. AMR sensors are usually used in a Wheatstone bridge configuration and demonstrate a high frequency response up to 1 MHz, that is usually limited by the integrated necessary amplification stages to several hundreds of kHz [111, 126].

- Giant Magneto-Resistance (GMR) Sensors: GMR is another method that can also detect static magnetic fields. GMR effect is manifested in structures which consist of thin magnetic layers that are separated by thin non-magnetic layers. Similar to the AMR effect, under the influence of an external magnetic field, the structure's resistance reduces significantly. GMR sensors can also be utilised in a Wheatstone bridge configuration and they are more sensitive than the AMR sensors [127]. The drawbacks of GMR technology include the relatively higher cost and lower bandwidth compared to AMR technology [128].

- Tunneling Magneto-Resistance (TMR) sensors: TMR sensors is another promising sensor technology that exhibits significantly higher sensitivity than current GMR and AMR sensors. A TMR sensor includes insulating layers rather than metallic layers that are employed by GMR sensors [128]. The sensor technology is at its early stages of development with limited applications. For high current applications, a prototype that is based on the combination of a TMR sensor with a Rogowski coil, has been proposed in [129].

Optical Current Sensors

Optical current sensors for high voltage applications have received increased interest in the last decades, mainly because of their small size and weight, low power consumption and their capability to measure both AC and DC currents. Optical sensors use optical fibre as the sensing element and hence, they provide inherent isolation and immunity against electromagnetic interference, features that are of vital importance in high voltage applications. [130]. Current sensors based on optical sensing commonly rely on the Faraday effect (or magneto-optic effect) or the magnetorestrictive effect (magnetic force sensors).

Faraday effect describes that when light passes through a transparent medium under the effect of a magnetic field, its travelling speed changes slightly causing a change in the state of light's polarisation. As such, light waves accumulate an optical phase difference in proportion to the field's strength. This optical phase difference β can be expressed by:

$$\beta = V \int \vec{H} \cdot \vec{ds} \tag{2.36}$$

where V is the Verdet constant that is dependent on the medium that is used for light transmission. The detection of a change in the state of polarisation of light can be realised via the polarimetric and the interferometric detection schemes.

Polarimetric detection scheme: A typical scheme based on Faraday effect is the fibre polarimeter, depicted in Figure 2.29. A laser with a polariser generates a linearly polarised light wave that is fed into N turns of a fibre coil that encloses the main current carrying conductor and acts as the sensing material [130].

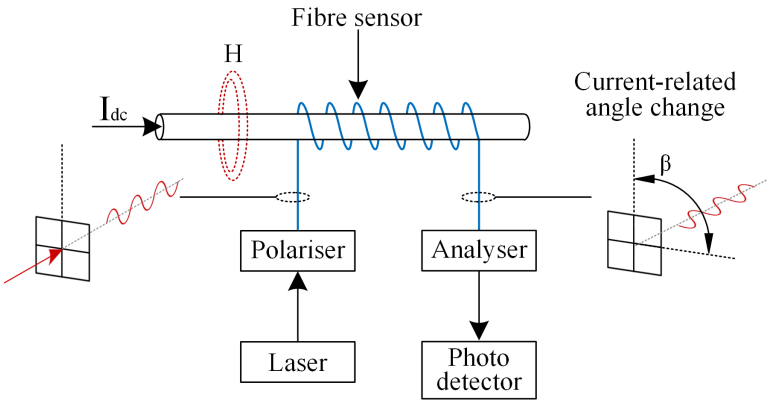


Figure 2.29: Optical fibre current sensor as per the Faraday effect.

The use of the fibre coil has the desirable effect of immunity to all other external magnetic fields apart from the magnetic field caused by the current inside the coil. The

magnetic field H, is the result of current I_{dc} flowing in parallel with the fibre sensor. As per the Faraday effect, field H causes a rotation of the polarisation plane by an angle β, that is expressed as:

$$\beta = VNI_c \tag{2.37}$$

Angle β represents a measure of the magnetic field inside the Faraday medium (fibre). The combination of the analyser and the photo-detector converts and modulates the polarised light into an electrical signal, which in turns corresponds to the current to be measured. With respect to the light intensity I_0 of the source, the output light intensity is given by:

$$I_d = \frac{I_o}{2}(1 + sin2\beta) \tag{2.38}$$

Polarimetric devices experience severe linear birefringence effect that can distort the rotation of polarisation, thus reducing the accuracy and sensitivity of the sensor [130]. Interferometric detection schemes were developed to overcome this issue.

Interferometric detection scheme: In interferometric detection schemes, the linear polarisation of light is analysed into two orthogonal circular polarised light waves; a left-hand circular-polarised light wave and a right-hand circular-polarised light wave. When the light waves pass through the fibre coil, the magnetic field that is created by the current to be measured slows the one component and accelerates the other as a result of the Faraday effect. The shift between the two circular polarised light waves can be used as the detection signal.

A typical example of interferometric arrangement that exploits this effect is the Sagnac interferometer [131]. In this interferometer, the light from the source is initially polarised linearly and is split into two equal light beams with opposite circular polarisation with the use of quarter wave retarders. The two-counter propagating light waves enter the fibre coil (Sagnac loop). After the two waves cross the Sagnac loop with different velocities, they are converted back to linear light waves that now have a phase shift that is given by

$$\phi_s = VN \int \vec{H} \cdot \vec{ds} = 2VNI_c \tag{2.39}$$

A phase modulator that generates a high frequency carrier is used to detect the optical signal. Demodulation of the detected signal then retrieves the phase information. Open loop Sagnac interferometer has been used for HVDC applications [132]. The interferometer can also be used in a closed loop configuration, where a control signal is fed back to the modulator to counter the current induced phase shift. In this case,

the control signal is a direct measure of the phase shift and an image of the primary current [133].

In Figure 2.30 [134], a reflective fibre optic current sensor scheme is depicted which is an enhanced version of the Sagnac interferometer [131]. The presented scheme consists of an electronic device (light source, detector and signal processor), a retarder and a mirror. A simple loop of optical fibre is wounded around the conductor which carries the current to be measured.

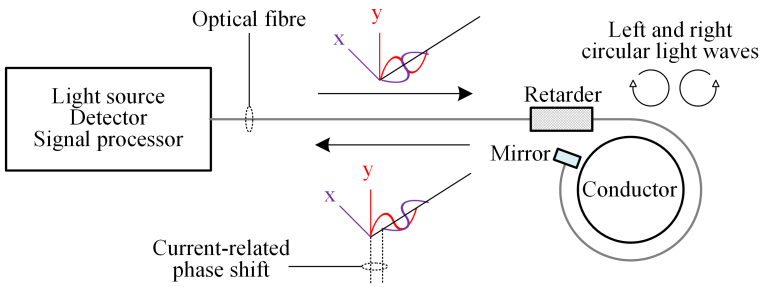


Figure 2.30: Reflective optical fibre current sensor.

As in Sagnac interferometer, the light source generates a light wave which is decomposed in right and left circularly polarised light waves which travel along the coil of the sensing fibre. The waves are then reflected by the mirror and their polarisation direction is swapped. When a DC current is flowing though the conductor, a current-related phase shift is present to the reflected wave. In this case, the total phase shift is doubled compared to the previous interferometer:

$$\phi_s = 4VNI_c \tag{2.40}$$

In a similar manner with Sagnac interferometers, the phase shift Φ_s is detected and analysed by the detector and signal processor. In this configuration, temperature sensitivities and mechanical disturbances that are present in the Sagnac interferometer are significantly mitigated.

The aforementioned fibre-optic current sensor is commercially available by ABB [135], and can measure uni- or bidirectional DC currents of up to 500 kA with an accuracy of $\pm 0.1\%$ of the measured value. Similar performance has been achieved for optical current sensors developed by NxtPhase (now Alstom) [136], and GE [137, 138].

Current interrogation techniques limit the available bandwidth of existing optical current sensors, mainly because of the requirements of the applications that they have been designed to be used. Typically, the output of optical current sensors is digital and is transformed to other forms via a merging unit [97]. The sampling rate of the merging unit limits the available bandwidth of the optical current sensor [139]. However, the

technology offers a high potential for a wide frequency range from DC to several MHz. In [140], a methodology for the optical sensors to have several output interfaces has been proposed. The proposed system can use an output interface suitable for demanding high-bandwidth applications, such as fault transients in HVDC systems, that works separately from an output interface that is designed to be in line with existing national and international standards that typically require low bandwidth.

Hybrid Optical Current Sensors

Hybrid optical current sensors combine standard current transducers such as Rogowski coil or shunt resistor, with optical fibre sensors. The conventional current transducer serves as the sensing element of hybrid devices, while the optical fibre system is used as the interrogation and transmitting element. The major advantage of hybrid sensors is that the fibre optic system provides galvanic isolation between the sensor head that measures the current in the main circuit at a high voltage level and the control system where these measurements are used. In this way, safe operation is ensured, insulation costs are significantly reduced, and the sensor is shielded from electromagnetic interference. The configuration of a hybrid optical sensor that is used for HVDC applications is shown in Figure 2.31 [107].

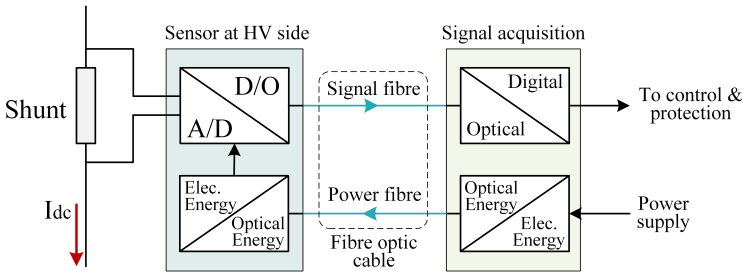


Figure 2.31: Layout of hybrid optical sensor scheme [107].

This sensor uses a direct shunt to measure the DC current that is located at high voltage together with an analogue/digital voltage processing unit that converts analogue measurements to optical signals. Then an optical fibre data link is used for the transmission of the optical signals to the control/protection system that is located at ground level. This system contains a power supply and an optical processing unit that is used for the interrogation of the sensing element. In critical applications, such as protection purposes, redundant equipment can be used to enhance the reliability of the sensor. An additional Rogowski coil can be used in conjunction with the shunt resistor, where the latter is used for measurement of currents close to DC and the former is used to increase the overall bandwidth of the device [98].

2.8 Summary

In this chapter, a comprehensive literature review of the most important equipment of HVDC grids has been performed. The review included the main converter technologies, HVDC grid configurations and ground practices, transmission lines, and important converter and HVDC grid control and modelling aspects. Furthermore, important material related to HVDC grid protection have been presented, such as DC circuit breakers and the available current and voltage measurement techniques for HVDC applications.

The review of the state-of-the-art HVDC grid technologies has contributed towards selecting the most suitable network components and their corresponding modelling approach for realistic representation and efficient full-scale modelling of HVDC grids. In detail, the MMC architecture has been adopted due to the numerous advantages it presents over other VSC topologies. Furthermore, the MMC is already installed in all VSC-based multi-terminal systems and it is expected to be the dominant option in future HVDC grids. With respect to HVDC grid architecture, the symmetric monopolar and bipolar configuration have been identified as the main options, and the former is used in the remainder of the thesis. With respect to DCCB technologies, the hybrid and mechanical DCCBs have been put forward. The decision was based on the fact that these configurations both present themselves as the main candidates for utilisation in future HVDC grids, while also several manufacturers have developed and installed prototypes in existing projects.

Special emphasis was given on the modelling aspects of VSC-HVDC converters, DC transmission lines and cables, and DC circuit breakers. For the modelling of the HB-MMC, an efficient averaged model, which has been validated against fully detailed models, has been presented. The adopted model simplifies the representation of the converter to reduce computational burden, while maintaining accurate converter response over a wide range of scenarios, including steady-state, transient and fault conditions. A representative DCCB model has been presented, which includes all the required functionalities that need to be considered for the conduction of DC fault transient studies. The phase-domain frequency-dependent model has been chosen for the accurate representation of transmission lines. Such a requirement stems from the need to capture transient phenomena over a wide range of frequencies from DC to several tens or hundreds of kHz. The transmission line modelling analysis forms the basis for the design principles of the proposed protection and location solutions in Chapter 5 and 7

Finally, a detailed analysis of the state-of-the-art of current and voltage measuring devices has been performed with the aim to identify their capabilities and the limitations that present technologies pose on the design of DC protection and fault location

systems, especially in terms of sampling frequency requirements. The findings have assisted towards the development of practical guidelines in the next chapters.

Chapter 3

HVDC Grid Protection and Fault Location

3.1 Introduction

One of the most significant challenges towards practical realisation of HVDC networks is the development of DC fault protection solutions. This challenge is driven by the fact that DC faults can propagate very quickly over the network, and owing to the high rate of rise of the fault currents and the under-voltages during DC faults, DC protection and control systems are characterised by more stringent requirements in terms of speed, selectivity, sensitivity and reliability [141]. For HVDC point-to-point connections, the current practice is to open the AC breakers at both ends of the link [34]. Application of the same method to HVDC networks, would lead to the shut-down of the entire network for relatively long time. This would furthermore pose a serious threat to the operation of the AC network, in terms of system frequency, rotor angle stability etc., and might compromise the total system security [142]. In detail, the main protection issues resulting from DC faults are the following:

- Contrary to AC currents, DC fault currents present no natural zero crossings. Therefore, DC breakers should be designed in such a way to drive the current down to zero and then extinguish the resulting over-voltage. Due to this issue, DC breakers are much more complex and costly than AC breakers.

- In HVDC grids the line impedances are significantly lower than in HVAC systems. In HVAC transmission systems, inductance constitutes a considerable part of line impedance with an X/R ratio of 20-25 [143]. In DC systems the inductive part of the links is much smaller than the resistive one. This results in much higher fault currents and greater under-voltages due to reduced total impedance across

the line. Lower line impedance also poses significant challenges to fault location schemes, since traditional AC protection solutions such as distance protection cannot be directly applied.

- Power electronics are characterised by a limited over-current capability that introduces a constraint on the time available for fault current interruption. IGBTs and other power electronics-based components that are used in VSC converters can operate at a limited range of currents and voltages. Typically, the maximum current that can be safely turned off is approximately twice the nominal current, while diodes on the other hand, can withstand higher over-currents [39]. Thus, it is of vital importance for the DC protection systems to act fast enough and protect the semiconductor devices.

- In case the converter terminal voltage falls below a critical limit as a result of the DC fault, the controllability of the converter can be lost. This would lead to undesirable tripping of the power converters and their start-up process would take a significant period of time. The loss of a critical converter station, or in extreme cases, a potential cascading converter tripping effect will cause the outage of the entire HVDC grid and may compromise the stability of the AC networks [143].

- When a DC short-circuit fault occurs in a HVDC grid, distributed cell capacitors of the commonly used HB-MMCs tend to contribute currents to the DC fault prior converter tripping, while further current stresses are induced on the converter semiconductor devices by the additional distributed capacitors of the DC lines [144]. The combined effect results in substantial fault current values, especially if the fault is not interrupted rapidly.

HVDC protection systems typically comprise of DCCBs, dis-connectors, protective relays, current and voltage measuring devices, active or passive fault current limiting devices (e.g. current limiting inductors) and AC-side equipment (e.g AC CBs). In addition, fault tolerant converters can be part of the protection sequence and contribute towards a safe and timely fault clearance. All these devices are collectively responsible for recognising and isolating DC faults, thereby ensuring the security of the HVDC grid, and minimising the effects of DC faults on the HVDC grid operation. Moreover, the HVDC grid protection system should minimise the stresses to critical equipment and ensure human safety [142].

Although the requirements of DC protection are similar with those of AC protection, their fulfilment is more difficult due to more stringent constraints. The critical clearing time in each system is governed by different factors. In AC systems, the avoidance of loss of synchronism of synchronous generators is the main factor that influences

the critical fault clearing time. In DC systems however, time constraints are imposed by the vulnerable grid components, such as the power electronics, and the current breaking capability of DC breakers. Moreover, the impact of power flow disruption from the DC side of the HVDC grid to the surrounded AC networks might generate additional constraints on HVDC protection. In analogy to AC protection systems, HVDC protection should fulfil the following requirements [34, 145]:

- **Selectivity**: the protection system must isolate only the faulted part of the HVDC system. Protection zones should be defined, and the protection system must operate only if the fault lies within its own zone.
- **Sensitivity**: the system should detect any fault that may occur.
- **Robustness**: the performance of the protection system should not be compromised even under degraded conditions. The system must be capable of discriminating between different types of faults and other events such as set-point changes, converter blocking actions, breaker tripping etc.
- **Reliability**: the protection scheme must act for any DC fault that may occur (dependability) and remain idle under non-fault conditions (security). Moreover, backup protection should be in place and be activated in case of primary protection failure.
- **Speed**: timely fault clearing is very critical for HVDC systems. Therefore, the protection system should operate fast enough to minimise system disturbance, avoid converter blocking and other harmful consequences.
- **Stability**: following DC fault clearance, the HVDC grid should remain stable and reach a new acceptable state within a reasonable time period.

Following successful fault clearance, the fault position should be identified to direct inspection, repair and re-commissioning of the faulted component. Towards this aim, fault location techniques that enable accurate fault location estimation are required in order to accelerate inspection time and system restoration and diminish the operational costs and power outage duration. Therefore, HVDC fault location is another essential function that should be run following HVDC protection. Successful fault location becomes increasingly challenging in HVDC grids due to the short time windows between fault inception and fault clearance that limit the available fault data records for execution of fault location methods.

3.2 DC Faults in HVDC Grids

3.2.1 DC Fault Types

The most common faults in HVDC grids are pole-to-pole (PTP) and pole-to-ground faults (PTG), with the latter being the most likely to occur. DC faults are mainly caused by aging or degradation of the insulation material [146]. In the case of overhead lines, the insulation material is the air that surrounds them, and degradation might be caused by arcing with vegetation, lightning strike or pollution, and the resulting fault is usually non-permanent [147]. On the contrary, DC cables include insulation material such as insulated paper or XLPE and their failure is usually permanent [144]. Both DC fault types are more likely to occur in overhead line based HVDC systems.

Pole-to-pole faults occur as a result of direct contact between the negative and positive conductors of a DC feeder [148]. Such faults are not common and if the poles are sufficiently separated there is a very low probability of occurrence. PTP faults lead to very high fault currents and low DC voltages at both poles and have the most severe influence on the grid. Pole-to-ground faults are the most common fault and are considerably less severe than PTP faults. Such faults occur due to insulation breakage of the DC line when the current-carrying conductor touches the ground either directly or through another path. In high-impedance grounded systems, PTG faults result in high over-currents during the fault transient stage, while the steady state fault currents are very limited. Nevertheless, persistent over-voltage is caused on the healthy pole, which must be mitigated quickly to avoid failure of the DC feeder, by isolating the faulty DC pole and activating pole rebalancing measures.

3.2.2 Fault Behaviour of VSCs

This section presents the fault behaviour of the two-level converter and the HB-MMC, which are the most widely used VSC topologies in HVDC applications. Although a PTP DC fault presents a low probability of occurrence, it is the most severe fault that may occur on the DC side of a HVDC system and therefore, the converters' response during this fault type is presented.

Two-level Converter

The central DC link capacitance of two-level converters, which is mainly used to maintain a constant smooth DC voltage, gives rise to a significant discharge current during DC faults. The two-level converter is defenceless against such faults because when the converter is blocked to avoid over-current in the IGBTs, it operates as an uncontrolled rectifier. The fault response of the two-level converter to a pole-to-pole fault is

characterised by three stages (Figure 3.1) [149].

- **Stage A: DC capacitor discharge.** In this stage, the DC-link capacitor causes large transient discharge current that increases rapidly and can reach very high peaks within a very short time. Consequently, the system experiences a severe collapse of the DC voltage
- **Stage B: Diode freewheeling.** Following the DC voltage collapse, the fault current commutates to the anti-parallel diodes. During this stage, each converter leg carries one third of the total DC fault current. This is the most hazardous phase for the diodes.
- **Stage C: Grid current feeding.** In this stage, the blocked converter behaves as an uncontrolled rectifier, injecting a steady-state fault current. An R-L-C circuit is formed that presents a forced response in the form of an AC current source.

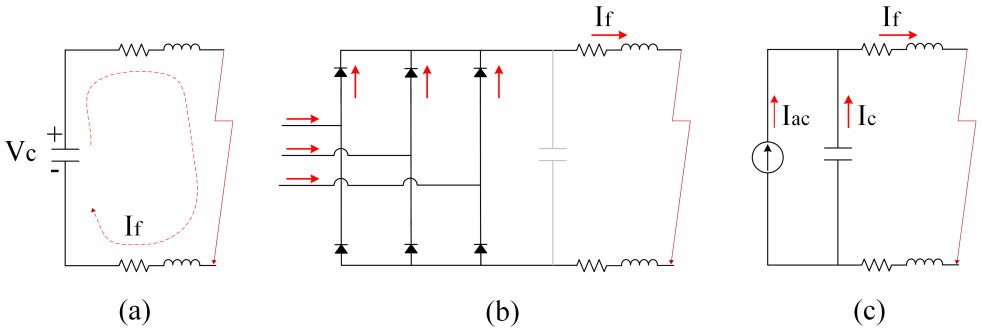


Figure 3.1: The three stages during a pole-to-pole DC fault in a two-level converter.

Half-Bridge MMC

In the HB-MMC, the DC link capacitance is distributed among the converter sub-modules. During a PTP DC fault, the SM capacitors can be quickly bypassed and therefore, the discharge of the capacitors is avoided. Owing to the limited discharge of the SM capacitors during a DC fault, the grid restoration time can be greatly reduced. Similarly, three simplified stages can be distinguished:

- **Stage A: SM capacitors discharge.** This stage takes place after the fault is seen by the converter until the time the converter is blocked, by simultaneous turn-off of the IGBTs in all arms of the MMC. During this period, which can extend from tens of microseconds to milliseconds, the inserted SM capacitors will discharge into the fault. Given that a sorting algorithm for the SMs is integrated

in the control system of the converter, all SM capacitances are equally discharged to some extent (assuming the converter retains controllability).

- **Stage B: Arm current decay.** This stage initiates once the converter is blocked and all SM capacitors are bypassed. The current flows into the fault through the anti-parallel diodes of the blocked IGBTs, leaving all three AC phases exposed to reduced impedance and consequently, the AC current in-feed from the AC grid will rise, while the transient DC current component decays. Initially, the AC current flows through all converter arms. The majority of the current flows within the paths shown in Figure 3.2(b). The arm and line inductance play a significant role in this stage [150].

- **Stage C: Grid current feeding.** This stage starts when the current flowing through three of the converter arms has decayed to zero. At this stage, the total DC fault current is contributed from the AC grid. The AC fault current can flow either through three or four arms as shown in Figure 3.2(c). The fault current reaches a steady-state value determined by the strength of the AC grid, the converter transformer impedance, the arm reactors, the inductive line termination (if present) and the distance to the fault.

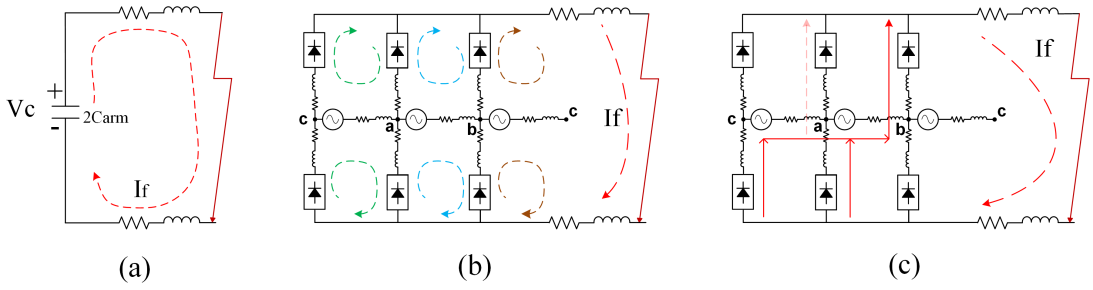


Figure 3.2: The three stages during a pole-to-pole DC fault in a HB-MMC.

Fault Blocking Converters

An alternative method for addressing HVDC grid vulnerability to DC faults is to use converters with fault current blocking capabilities, such as the Full-Bridge MMC (FB-MMC) [151–153]. Unlike the HB-SMs, Full-Bridge Sub-modules (FB-SMs) used in the FB-MMC can recreate any DC voltage the DC fault may present at its DC terminal if the bipolar capability of the FB-SM is fully exploited; thus, providing greater controllability during DC faults that enables the converter to control the fault current at zero. The DC fault blocking capability feature can be exploited to improve the HVDC grid fault response and extend the fault clearing times to a range in line with AC systems.

In this way, DCCBs with lower ratings or fast dis-connectors can be used to isolate the faulted line. On this basis, converters with fault blocking capability represent an attractive option, especially, for overhead lines based HVDC grids, in which DC faults are expected to be more frequent.

3.2.3 Fault Clearing Strategies

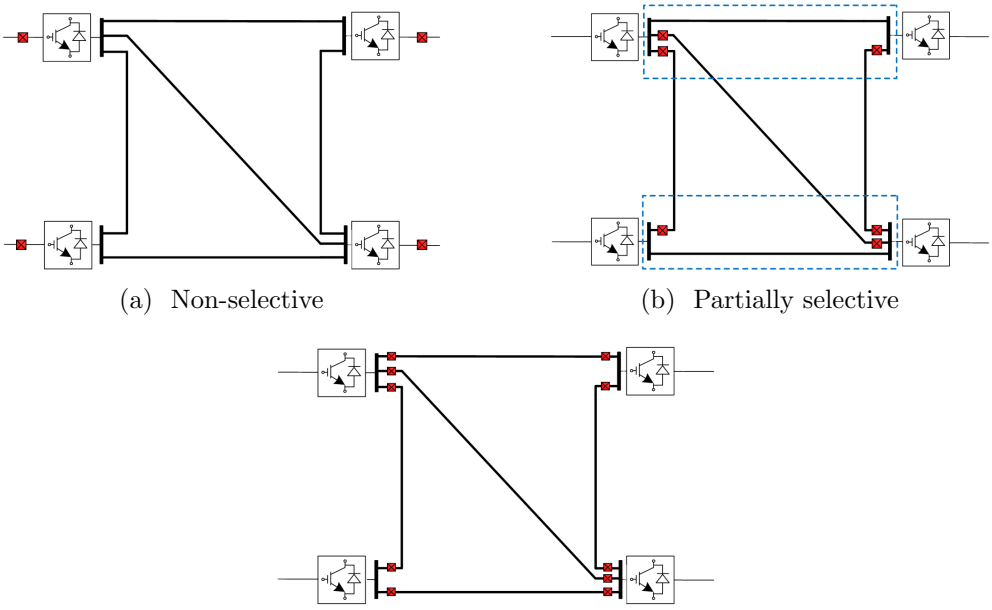
Several protection strategies are available for clearing DC faults in HVDC grids [6]. These are typically classified into a) non-selective, b) partially selective, and c) fully selective strategies. The main differences between the strategies is the definition of protection zones, the number and locations of the employed DCCBs and the type of converter technologies. The selection of the appropriate strategy is the result of a techno-economic analysis and is mainly dictated by the AC system characteristics, the impact of the HVDC grid on the interconnected AC systems (in terms of DC network capacity), protection system costs, and the maximum acceptable fault clearing time.

Non-selective Strategy

In a non-selective strategy, the whole HVDC grid is treated as a single protection zone, as illustrated in Figure 3.3(a). When a DC fault is detected, the AC breakers from the AC-side of all converters are tripped to isolate the HVDC grid and eliminate the AC grid fault current contributions. Subsequently, when DC fault currents drop to zero, fast dis-connectors are used to selectively isolate the faulty DC line/cable. Following successful fault clearance, the AC breakers are re-closed to allow for the re-energisation of the remaining healthy HVDC network. The cost of DC protection in non-selective strategies is minimised due to the reduced count of DCCBs.

The use of ACCBs for fault clearance in HVDC grids is an economic and simple approach, which has been discussed in [154, 155]. Nevertheless, these approaches lead to de-energisation of the DC grid and the post-fault recovery process may take several hundreds of milliseconds or seconds, which is not suitable for critical power corridors. Therefore, this strategy is considered appropriate for small-scale HVDC networks that have low impact on the operation of the interconnected AC grids. Nevertheless, the use of AC breakers for fault clearance can be used for backup protection.

Alternatively, non-selective approaches can be implemented with the use of fault tolerant converters, such as the FB-MMC or the hybrid MMC. Due to the capability of these converters for extended voltage range control, the DC voltage at all terminals can be quickly controlled to zero. In this way, the fault clearing process can be significantly expedited when compared to strategies that are based on AC breakers only. On the downside, the cost of these topologies is higher than that of the HB-MMC due to the



(a) Non-selective (b) Partially selective

(c) Fully selective

Figure 3.3: Fault clearing strategies in HVDC grids.

increased number of semiconductor devices per SM.

Partially Selective Strategy

Partially-selective approaches have been also proposed, in which the HVDC grid is divided into smaller protection zones (Figure 3.3(b)), which comprise of multiple transmission mediums and converters. When a fault happens inside a predefined zone, the whole zone is disconnected using DC breakers at strategic locations, or other devices such as DC-DC converters, while the remaining zones continue their normal operation [152, 156]. Afterwards, the faulted medium within the faulted zone is identified and isolated.

Partially selective strategies achieve a trade-off between DC protection cost and the impact caused on the AC grids by splitting the grid into smaller zones and avoiding the de-energisation of the entire DC network. The approach is effective for small-to-average scale HVDC grids, and it can divide a large complex HVDC grid into smaller manageable sub-grids. However, its adoption is more challenging in highly meshed networks or in large-scale HVDC grids with increased power transmission, in which minimum grid disturbance is required under all circumstances.

Fully Selective Strategy

Fully selective strategies resemble the approach followed in AC systems, in which each transmission line forms an individual protection zone. As illustrated in Figure 3.3(c), DCCBs (typically in series with line inductors) are located at all transmission media ends. In the event of a DC fault, only the DCCBs attached to the faulted medium are commanded to trip, while the remaining DCCBs remain idle. To enable such operation, fully-selective protection algorithms are required. In fully-selective strategies, the cost of DC protection rises significantly due to the increased count of DCCBs, and the total cost is influenced by the choice of DCCB technology.

When a fully selective strategy is adopted in a HVDC grid, the minimum disruption to its operation is ensured. The converters adjacent to the faulted medium may block or remain connected depending on the severity of the DC fault and the operation time and characteristics of the employed DCCBs. An approach for DCCB sizing has been proposed in [157], for three fault-ride through scenarios: a) all converters are prohibited from blocking, b) only the converters adjacent to the faulted medium are allowed to temporarily block and c) all converters can be temporarily blocked.

3.2.4 DC Fault Clearing Sequence

The sequence of events during the fault clearing process under a fully selective protection strategy is illustrated in Figure 3.4, in which positive pole current measurements are obtained at one end of a DC cable for a PTP DC fault that occurs in the middle of the medium. The moment the fault occurs, travelling waves start to travel from the fault location along the cable to both directions. At time t_f, the waves reach the measuring point and the fault current starts to rise. The protective relay at the measuring point initially detects a DC fault event at time t_{det} and subsequently, the fault is determined to be within the relay's protection zone at time t_{dscr}. At this moment, the relay issues a trip command to the relevant DCCB, which is characterised by a certain breaker operation time depending on the DCCB technology. At time t_{int}, the main breaker contacts are separated, and the fault current is commutated to the energy absorption branch (surge arresters). Finally, at time t_{fclr} the fault current has been extinguished.

From the above analysis and as shown from equation (3.1), the fault clearing process can be divided into two main stages. The first stage is determined by the actions of the protective relay, i.e. DC fault detection and discrimination. The second stage represents the actions of the DCCB and comprises of the breaker operation time and the fault current interruption time.

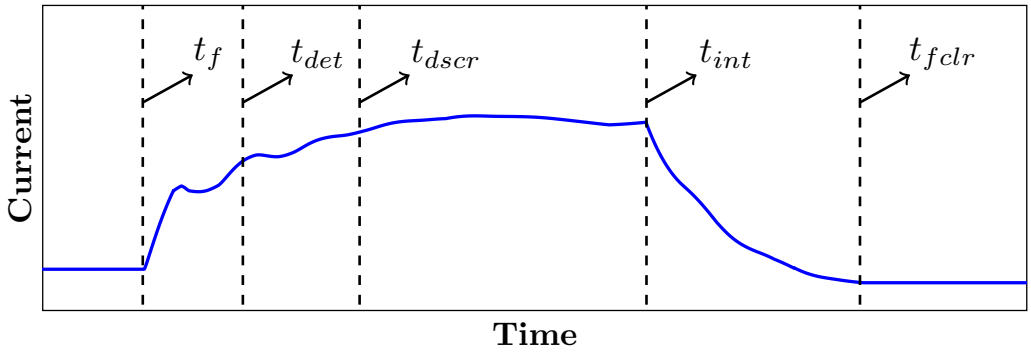


Figure 3.4: Indicative sequence of events during the DC fault clearing process.

$$(t_{fclr} - t_f) = \underbrace{(t_{dscr} - t_f)}_{\text{relay actions}} + \underbrace{(t_{fclr} - t_{dscr})}_{\text{DCCB actions}} \tag{3.1}$$

Typically, fault current interruption and breaker operation times are determined by the selected breaker technology and its corresponding acting speed and rest characteristics. Moreover, fault current interruption depends on the moment the breaker is opened, the amount of energy stored in inductive elements of the DC system, and the value the DC current has attained at this instant and consequently, the duration of this stage can vary significantly.

Since protective switchgear (DCCBs) are selected from the initial protection design stages for a given HVDC grid, the only degree of flexibility in total protection operation speed is provided by the speed of the protective relay's actions. On this basis, selective and high-speed protection algorithms are critical for ensuring that the trip signals are sent to the relevant DCCBs as quickly as possible. It is worth noting, that in certain hybrid DCCB topologies, the proactive mode can be invoked, in which the fault current is transferred to the commutation branch upon fault detection [41]. Afterwards, if the fault is deemed to be within the protection zone, the DCCB proceeds to fault current interruption, otherwise, the current is re-diverted back to the main branch. In this way, the time delay between fault detection and fault discrimination is eliminated, and the total fault clearing process is expedited.

3.3 Design and Implementation of HVDC Protection

3.3.1 HVDC Protection Design

Reliable and cost-effective HVDC protection systems are of vital importance for the realisation of the HVDC grid concept. HVDC protection design is the result of a complex techno-economic analysis that depends on a plethora of factors. Drawing from

the trends observed in the technical literature, a high-level summary of the HVDC protection design process is presented in Figure 3.5. It is worth mentioning that protection design is closely connected with the design stage of the HVDC grid, in which a number of decisions taken may directly affect the selection of protection equipment. Aspects of the project design stage that influence HVDC protection design include the decisions made on the system configuration, number and locations of converter terminals, power ratings of converters, nominal DC voltage, types of connections between terminals (meshed, highly meshed etc.), system grounding, and the selected equipment such as types of transmission media and HVDC converters.

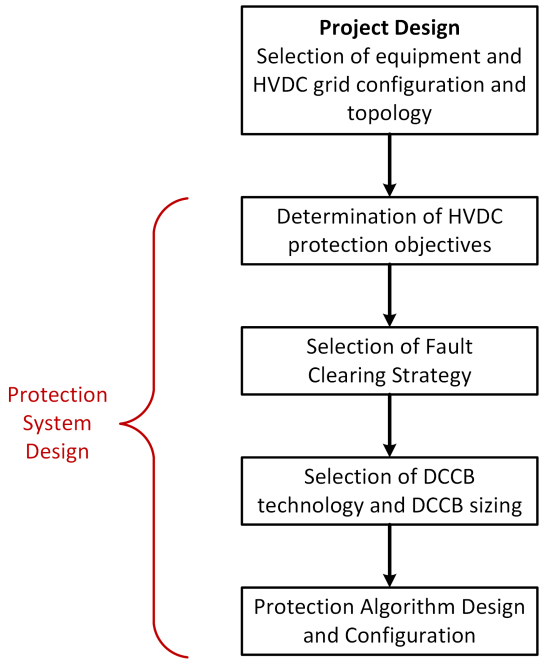


Figure 3.5: High-level protection design steps.

Determination of HVDC Protection Objectives

Using the selected equipment and design characteristics of the HVDC grid itself as an input, the first step is to define the objectives and functional requirements of HVDC protection. This stage aims to perform a risk assessment by considering the probability of occurrence of DC faults and their potential impact on the DC-side and AC-side of the HVDC grid [28]. The principal priority of HVDC protection is to avoid damage of the most critical components (e.g. converters) and ensure continuity and security of HVDC grid operation. Furthermore, the protection objectives should be shaped around both AC-side and DC-side operational constraints.

The most stringent constraints on HVDC protection arise from the DC-side of the

grid, such as the converter and transmission line over-current limits. To satisfy these constraints, the current limits of the grid components and the expected fault current development under worst-case scenarios are identified to determine the maximum fault current that needs to be interrupted by HVDC protection systems and the maximum time-scales for DC fault clearing. The required behaviour and DC fault ride through performance of the HVDC grid are also determined in this stage. The HVDC grid fault-ride through strategy mainly refers to the desired behaviour of grid converters during DC faults. Based on the specified requirements on the continuity of grid operation, HVDC protection can be designed to i) avoid disconnection of any grid converter, ii) permit disconnection of converters that are only in the vicinity of the fault or iii) permit disconnection of all grid converters. Moreover, the cost associated with ensuring the expected fault ride through performance should be taken into account, and in any case outweighed by the obtained benefits.

Besides the constraints imposed by the DC-side network equipment, AC-side constraints should also be taken into account, as well as the disturbance caused to the AC networks as a result of DC faults. The loss of power in-feed towards the interconnected AC systems should be maintained within the acceptable limits designated by the corresponding grid codes and standards with the aim to ensure system stability and avoid loss-of-synchronism of the AC generators. For instance in the UK, according to the National Electricity Transmission System Security and Quality of Supply Standard (NETS SQSS), in order to avoid unacceptable frequency conditions (i.e. frequency deviations below 49.5Hz for more than 60 seconds), the maximum infeed loss is limited to 1.8 GW [158]. Therefore, HVDC grid protection should prevent the disconnection of converters and lines that result in such high loss of power in-feed to the AC grid.

Selection of Fault Clearing Strategy

The selection of the fault clearing strategy is determined by the required fault clearing time, which should be matched with the time scales imposed by the HVDC protection objectives of the previous step. The capacity of the HVDC grid, the potential impact of DC faults on the surrounding AC networks, and the expected frequency of DC faults are the key determining factors behind the strategy selection. For instance, in Overhead Lines (OHL)-based systems in which the probability of fault occurrence is much higher, a considerable investment in DC protection is more likely when compared to cable-based systems. The grid converter technologies in the project design stage directly influence the choice of fault clearing strategy. For example, selection of fault-blocking converters in the project design stage implies the use of a non-selective fault clearing strategy in conjunction with high-speed switches or DCCBs with reduced requirements.

An additional factor that needs to be considered when selecting protection strategy is its extensibility. Investing on a fully selective protection strategy (e.g. using hybrid DCCBs at all cables) in a small-scale HVDC grid with minimal impact on the connected AC grids is not beneficial if no further grid expansion is planned or expected in the future. In such a case, a non-selective strategy can be initially selected and if the capacity of the HVDC grid is further increased, the protection philosophy can be modified into a partially or fully-selective strategy (or a combination thereof).

Selection of DCCB Technology and DCCB Sizing

The selection of the fault clearing strategy defines the requirements with regards to the number and locations of DCCBs. Moreover, depending on the protection objectives set out in previous steps, the appropriate DCCB technology should be selected that satisfies the constraints in maximum fault clearance time and maximum breaking current. It is possible that several implementations and technologies may be applicable.

The placement of sizeable current limiting series inductors in series with DC breakers is one of the practical measures that have been adopted to slowdown the rate of rise of current, thus allowing the breakers to act before the maximum current breaking capability is exceeded. Consequently, the size of the inductor can be adjusted to achieve a certain current breaking capacity for the selected DCCB. An approach for DCCB sizing in terms of breaker operation speed and inductor size for various fault-ride through scenarios has been proposed in [157]. In addition, the DCCB absorption branch should be sized according to the energy that is expected to be absorbed during fault current interruption.

In the event of primary protection failure, backup protection measures should be in place to guarantee safety of HVDC grid components. Backup protection can be provided by adjacent DCCBs (e.g. in case of fully selective strategies), or with the use of AC-side breakers or other measures (e.g. in case of non-selective strategies). If the protection objectives must be satisfied in full even for the rare event of primary protection failure, then the DCCB sizing should be refined to account for the increased fault current levels, e.g. through the insertion of a larger current limiting inductor.

Protection Algorithm Design and Configuration

The last step of HVDC protection design is the selection, design and configuration of appropriate protection algorithms that lead to the correct decision in terms of identifying the faulted component, and the components that should be disconnected to isolate DC faults. Protection algorithms work in conjunction with DCCBs to realise the implementation of the fault clearing strategy and meet its required time-scales.

A combination of DC fault detection and discrimination criteria can be employed to identify the faulted line, while more than one protection algorithm can be executed in parallel to provide an additional degree of reliability.

Factors that need to be considered when designing a protection algorithm are the instrumentation requirements (e.g. sampling frequency, measurement locations, measurement equipment etc.), the underlying detection and discrimination functions, the use of a communication channel depending on whether only local or both local and remote measurements are needed, and the protection settings (e.g. protection threshold). Particular attention should be paid to the design of the protection threshold based on which internal faults are discriminated from external faults. Protection threshold determination should guarantee both dependability and security with sufficient margins.

3.3.2 Implementation of HVDC Grid Protection

Implementation of HVDC grid protection can be realised using an architecture illustrated for a decentralised protection design in Figure 3.6. The figure illustrates the protection system for a fully selective protection strategy, which entails the maximum use of protection equipment, while in non-selective and partially selective strategies fewer protection devices may be present. In this implementation, protective relays, which are also referred to as Intelligent Electronic Devices (IEDs), are installed next to DCCBs at each line/cable end of the HVDC grid. Alternatively, a centralised approach can be adopted, in which a master IED gathers all the functions of the distributed relays of the decentralised design case, and is responsible for the overall protection of the DC bus and the connected grid components. However, the decentralised design is considered a more viable option for HVDC grid protection as it eliminates vendor-dependence, improves reliability, and facilitates the integration of multi-vendor equipment [159].

In the decentralised design, each IED is responsible for the protection of an individual line or cable. Towards this aim, DC fault detection and discrimination logics are embedded and executed within the protective relays. The DC fault can be detected based exclusively on local measured quantities or alternatively, communicated measurements from the remote end of the line may also be required, in which case a reliable communication channel should be available. For the correct operation of the protection relays, accurate and reliable voltage and/or current measurements are required. The measurement sampling frequency can have a critical effect on DC fault detection and discrimination speed depending on the detection function that is employed. The choice of measuring technologies for HVDC protection depends on the selected protection algorithm and its requirements in terms of bandwidth, acceptable measurement error etc. More details on this matter will be presented in Section 3.6.

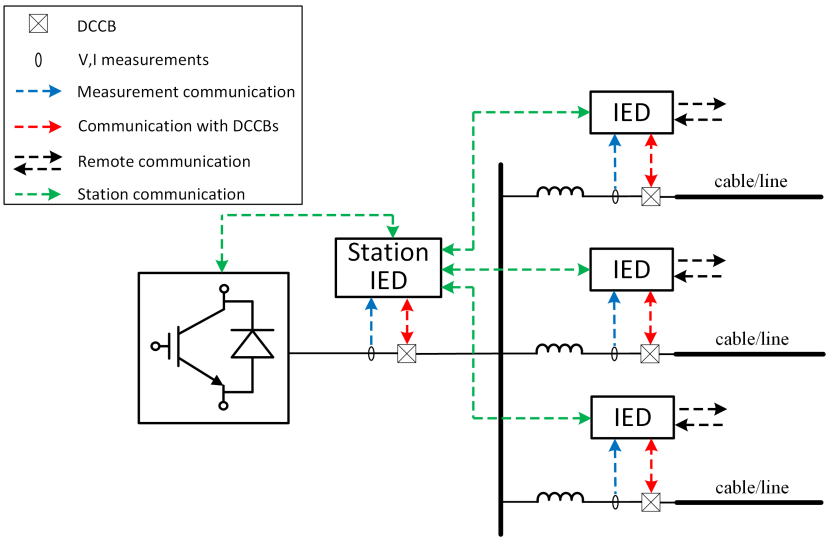


Figure 3.6: Implementation of fully selective HVDC protection strategy.

As shown in Figure 3.6, each protective relay also exchanges signals with its neighbouring DCCB to support a variety of functions. Breaker opening for fault current interruption is the most basic DCCB function that is supported by the IED by issuing a trip signal if a fault that lies within its protection zone is identified by the underlying protection logic. Additional DCCB functions can also be supported by the IEDs such as, proactive DCCB operation and fault current limiting mode (for certain hybrid DCCB designs), breaker status monitoring, fast re-closing, breaker failure detection and others [159].

Communication between protective relays and a station IED will also be required in future HVDC grids to coordinate the actions of the main protective relays with control and protection actions at a station level under fault conditions (e.g. converter protection, blocking) and under post-fault conditions in order to ensure smooth system restoration (e.g. pole rebalancing, converter re-energisation etc.) [32,160]. This kind of interface between dedicated protective relays and the station IED can also be used to support further protection related aspects, such as backup protection in case of a failure of one or more DCCBs or IEDs. As an additional backup measure, a converter-side DCCB may be installed, the actions of which are controlled by the main station IED.

3.3.3 Interoperability of HVDC Protection

To date, most HVDC projects have been developed as turn-key solutions by a single manufacturer. However, as HVDC grids gain more attention, their scale is expected to become increasingly larger and hence their implementation will necessitate the involvement of multiple vendors as is the case in large-scale AC systems. Therefore,

a multi-vendor approach is required for future DC grids in which power converters, cables, protection and switchgear and other equipment will be supplied from multiple vendors. Such an approach will prevent vendor lock-in by ensuring impartial access to a global market, which in turn will encourage competition, innovation and cost reduction and will expedite the deployment of HVDC grids.

One of the main challenges of multi-vendor HVDC grids is to achieve interoperability of the various grid components with the ultimate aim to operate the grid reliably and securely under all network conditions. For instance, different converter control and protection systems should not compromise the overall functionality of the grid, which must remain statically and dynamically stable regardless of the control and protection logic that is adopted at each station [143]. This is a main challenge that needs to be tackled in order to enhance the applicability, the maturity, the modularity, and flexibility of HVDC grids.

In an effort to facilitate the multi-vendor approach and the development of best practices, several international standardisation bodies and independent groups have highlighted the necessity for the standardisation of HVDC systems. CIGRE working groups [34], the European HVDC study group [161] and CENELEC [162] have worked on standards and technical guidelines for HVDC grids and although these have resulted in significant progress, there is still lack of a consensus and standardisation regarding requirements about the voltage level, the control and protection principles etc. The determination of such technical requirements will pave the way for the development of specifications of the equipment that HVDC grids will contain.

Interoperability of HVDC protection is no exemption to the required multi-vendor solution. Traditionally, converter manufacturers provide a combined control and protection system, which is not accessible to potential HVDC end-users (e.g. transmission system operators) due to sensitivity issues regarding intellectual property; however, this practice hinders the deployment of multi-vendor HVDC grids. Successful operation of multi-vendor HVDC protection requires beforehand the determination of protection philosophies (fault clearing strategy, targets and requirements) and the designation of functional specifications for the various protection system components, including the protective relays or IEDs. Successful interoperability between different IEDs or between IEDs and other equipment is of paramount importance in HVDC grid protection. In detail, the interoperability aspects related to protection relays that need to be considered in a multi-vendor environment are the following [163]:

- Operation performance and compliance with speed, selectivity, and reliability requirements
- Interface and coordination with acting equipment such as DCCBs and converters

- Interface and coordination with local or remote protection relays
- Interface and coordination with other devices for post-fault restoration (e.g. with pole-rebalancing devices)
- Interface with measuring devices for data acquisition
- Communication interface standards and protocols (data size and format, communication channel, speed, bandwidth etc.)

Moreover, the underlying protection algorithms (unit or non-unit) need to be suitable for multi-vendor applications and ensure extensibility and adaptability when conditions change (e.g. grid expansion). Due to the requirement for fast protection operation, an ongoing research and development activity is focused on HVDC protection relays (or IEDS) that utilise DC fault detection and discrimination functions based on fast DC fault transients (e.g. using travelling wave theory). Nevertheless, there is currently no suitable well-defined framework for the design of these solutions and their interoperability with other protection equipment is not guaranteed.

3.4 Review of HVDC Protection Algorithms

In current literature, the proposed HVDC protection algorithms can be classified into unit protection and non-unit protection methods [41]. Unit protection methods, (also known as double-ended protection methods) have well-defined protection zones and rely on a communication link/channel in order to obtain signal measurements from both ends of the protected feeder and execute the protection logic. In non-unit protection methods, the algorithm is executed based exclusively on local measurements. Nevertheless, one of the main challenges of non-unit protection lies in the determination of artificial protection boundaries. Non-unit protection has generally received wider attention due to its significantly higher speed than unit protection. The rest of this section presents the main principles of unit and non-unit protection and the state-of-the-art of fully selective protection algorithms for HVDC applications.

3.4.1 Non-unit Protection

Non-unit protection techniques typically rely on the placement of series inductors at each end of the transmission medium to define protection boundaries as shown in Figure 3.7 that illustrates an example HVDC grid section, in which each DC feeder is terminated with DC inductors. The protection zone of relay R is the full length of the DC feeder between the two inductors. Figure 3.7 also illustrates several potential

DC faults that may occur on the HVDC grid section. With respect to relay R, faults F_1, F_2, F_3, F_4 are forward faults and F_5, F_6 are backward faults. A well-designed non-unit protection algorithm should be able to discriminate internal faults (i.e. faults $F1$ and F_2) from external faults (i.e. faults F_3, F_4, F_5 and F_6) based only on local measurements. In doing so, the non-unit protection algorithm should be able to i) **detect** any DC fault, ii) use a **directional** criterion (if necessary) to recognise forward DC faults, and iii) **discriminate** between internal and external faults. [141, 164–167].

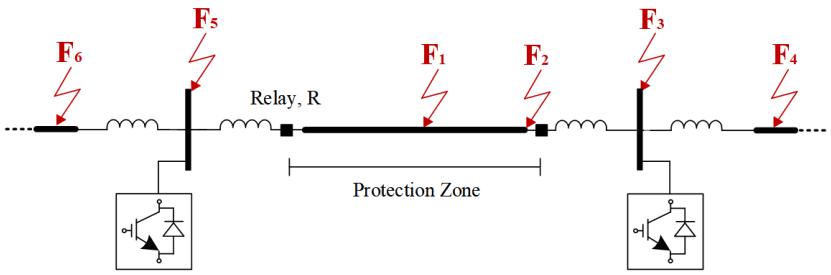


Figure 3.7: Protection zone of a protective relay and potential faults.

On this basis, most of the non-unit protection methods proposed in the open literature use a fault detection function (or start-up element) to identify the occurrence of a DC fault and activate the protection logic. Afterwards, a fault discrimination function is employed to identify faults that lie within the relay's protection zone. Depending on the non-unit protection algorithm principles, DC fault detection and discrimination may be performed by the same function. In case the fault discrimination function can only discriminate between forward internal and external DC faults, an additional directional element is required to ensure that the relay does not operate for backward external faults. This is a common limitation of DC fault discrimination methods, which is caused by the fact that remote internal DC faults (i.e. Fault F_2) can have less impact on DC current and voltage traces than close backward external faults (i.e. Fault F_5).

Basic DC Protection Methods

Over-current (OC) protection has been widely used in AC systems as a non-unit protection method based on local current measurements. In a similar manner, over-current protection can be employed for DC grids by setting a threshold on line currents for detecting DC faults. The polarity of the current serves as an indication of the direction of the DC fault (forward or backward). Nevertheless, selectivity cannot be achieved through this method, since both forward internal and external faults result in high fault currents. The over-current criterion is mostly used as backup protection or in combination with other methods to form a complete protection scheme [41].

Under-voltage (UV) relays can be used as a means of fault detection owing to the fact that DC faults cause a significant drop in DC voltage and hence, a DC fault can be detected if the measured voltage drops below a critical threshold [147]. Under-voltage protection cannot distinguish between forward and backward faults. Hence, this method can also be used as a backup protection or as one of the fault detection criteria of a complete protection scheme. It is worth noting that typical converter internal protection makes use of an over-current threshold on converter arm currents, and an under-voltage threshold on converter terminal voltage.

Current derivative or di/dt method uses the initial rate of rise of fault current to determine whether a fault has occurred on the protected line. The principle is the same as in over-current protection, but the magnitude of the di/dt is used instead for increased detection speed. Nevertheless, the method is susceptible to noise and might suffer from the collection of incorrect data samples [168]. An additional limitation is that di/dt for remote internal faults with large fault resistance may be lower than di/dt for external faults [41]. di/dt is commonly used as a direction criterion in HVDC protection schemes, in which a forward DC fault is identified for positive values of di/dt (assuming positive current direction when the current enters the transmission medium).

Voltage derivative or simply dv/dt has been widely used in LCC-based HVDC point-to-point transmission [169], in which a fixed threshold on the derivative of the voltage is applied for DC fault detection. The reach of dv/dt increases for higher values of current limiting inductance. Due to the rapid collapse of DC voltage during DC faults, DC fault detection is significantly accelerated when dv/dt is used.

Several protection schemes have been designed based on one or more of the aforementioned methods [170–172]. Nevertheless, due to the limitations of these techniques, alternative algorithms based on travelling wave principles have been developed for faster HVDC grid protection.

Travelling Wave based Non-unit Protection Algorithms

According to travelling wave theory, voltage and current travelling waves are generated at the DC fault point and start to propagate rapidly along the faulted medium to both directions from the fault location. Travelling waves contain a significant amount of information over a wide frequency spectrum and especially, in the high frequency region. As travelling waves weaken due to the attenuation caused by the line components and the successive reflections that occur at discontinuity points, the most important information is contained within the first voltage and current travelling waves that are initiated by the fault. Travelling-wave based methods attempt to capture that information to rapidly detect the fault and act against it. This attempt is assisted by the

deliberate inclusion of current limiting series inductors.

Series inductors do not only serve as current limiters that restrain the rate of rise of the fault current (di/dt), but they also behave as a natural boundary filter by damping a range of frequencies of the incident waves, thus influencing the transient voltage and current signatures. This important feature has been exploited to assist DC fault detection and discrimination based on the first incident travelling wave generated by the DC fault [141, 164–167]. These schemes make use of the inductive termination to define protection zones, and they are based on the concept that inductive termination provides a high impedance path for the high frequency components, thereby enabling the discrimination between undistorted travelling waves generated by an internal DC fault and travelling waves that have been generated by external faults and have been distorted by the inductive termination. In detail, the algorithms operate on the principle that even in the case of an extreme internal fault, i.e. a highly resistive fault at the end of the protection zone (fault F_2 in Figure 3.7), the voltage wave reaches the relay location without passing through any inductor and therefore, its frequency spectrum remains largely unaffected. On the contrary, for an external fault behind the series inductor (fault F_3 in Figure 3.7), the high frequencies of the incident voltage wave are filtered out due to reflection by the series inductor.

Based on the above traits, several TW voltage-based non-unit methods have been developed. In [164], voltage measurements from the line side of the inductor are utilised to obtain the voltage derivative and quickly detect and discriminate DC faults. Similarly in [141], faults are detected using an under-voltage criterion, and voltage derivative is then utilised to discriminate between forward internal and external faults. Current derivative is also employed to exclude backward DC faults. The authors in [167], use voltage measurements from both sides of the inductive termination to calculate the ratio of transient voltages (ROTV) and to establish a discriminative protection method. Similarly, the basic fault discrimination criterion in [165, 173] is based on voltage measurement across the inductor. Finally in [166], the ratio of the rates of change of voltages before and after the termination is used to implement the protection scheme. As with most non-unit protection methods, the performance of these methods is affected by the fault distance and resistance, line length, and the size of series inductance.

Travelling wave-based techniques have been further refined and improved through means of signal processing. Such methods are still based on line-side voltage and current measurements but employ advanced signal processing and mathematical tools in an effort to detect abrupt, local changes in a signal such as voltage travelling waves induced by DC faults. In the literature, signal processing methods that have been utilised for non-unit protection purposes include Fourier Transform (FT) [174, 175], Mathematical Morphology (MM) [176–178], Hilbert-Huang Transformation (HHT) [179],

S-Transform [180] and Wavelet Transform (WT) [181–191]. WT in particular, is a powerful signal processing tool that has received significant attention for fault detection and discrimination applications. In contrast to other signal processing techniques, wavelet analysis does not work on a time-frequency basis, but rather on a time-scale basis that allows for targeted analysis in specific frequency bands of the analysed signal, which can be conveniently selected for enhanced protection performance.

Table 3.1: Taxonomy of non-unit protection methods according to measuring requirements and protection functions.

Method	**Measurements**		**Sampling**	**Protection Functions**		
	Voltage	**Current**	**Frequency**	**Direction**	**Detection**	**Discrimination**
[174]	×	✓	2 MHz	sign of $TW(i)$	sign of $TW(i)$	FT
[181]	✓	✓	1 MHz	–	WT	WT
[182]	✓	×	500 kHz	–	UV	WT
[192]	✓	✓	200 kHz	–	UV	FPT
[193]	✓	✓	200 kHz	–	UV, $fit(i)$	UV, $fit(i)$
[194]	✓	✓	200 kHz	Δi	UV, $fit(i)$	UV, $fit(i)$
[195]	✓	✓	200 kHz	–	dv/dt, $fit(i)$	dv/dt, $fit(i)$
[176]	✓	✓	110 kHz	SE	SE	MM
[196]	✓	✓	100 kHz	di/dt	WT	WT
[141]	✓	✓	100 kHz	di/dt	UV	dv/dt
[183]	×	✓	96 kHz	–	WT	WT
[184]	✓	✓	96 kHz	–	$cov(i)$	WT
[179]	✓	✓	50 kHz	di/dt	UV, dv/dt	HHT
[197]	×	✓	50 kHz	$d\bar{I}$	$d\bar{I}$, OC	$d\bar{I}$
[167]	✓	×	50 kHz	–	dv/dt	$ROTV$
[175]	×	✓	50 kHz	–	FT	FT
[185]	✓	✓	25 kHz	Δi	UV	WT
[166]	✓	×	25 kHz	dv/dt	dv/dt	dv/dt
[177]	✓	×	20 kHz	UV	MM	MM
[186]	✓	×	20 kHz	–	dv/dt	WT
[198]	✓	✓	20 kHz	di/dt	dv/dt	$d(i/v)/dt$
[178]	✓	✓	20 kHz	MM	∇v	MM, dv/dt
[170]	×	✓	20 kHz	di/dt	di/dt	di/dt
[199]	✓	✓	10 kHz	di/dt	UV	CRP, du/dt
[187]	✓	✓	10 kHz	WT	UV	WT
[200]	×	✓	10 kHz	–	MAD	MAD
[180]	✓	✓	10 kHz	–	$S\text{-}Transform$	S-$Transform$
[188]	✓	×	10 kHz	–	WT	WT
[171]	×	✓	10 kHz	di/dt	di/dt	di/dt
[201]	×	✓	10 kHz	Δi	Δi	$TAVC$
[189]	✓	✓	10 kHz	di/dt, dv/dt	WT	WT
[190]	×	✓	2 kHz	di/dt	OC	WT, MLT
[164]	✓	×	–	–	dv/dt	dv/dt
[165]	✓	×	–	–	dv/dt	dv/dt
[172]	✓	✓	–	di/dt	dv/dt, di/dt	dv/dt
[191]	✓	✓	–	–	WT, dv/dt, UV	WT, dv/dt, UV
[173]	✓	×	–	–	UV	Δv
[202]	✓	✓	–	di/dt	UV	dv/dt
[203]	✓	×	–	–	dv/dt	$\int V_{Ldc}$
[204]	×	✓	–	–	$CLRP$	$CLRP$

Table 3.2: Protection functions of Table 3.1.

Function	Explanation
∇u	Voltage gradient
$d\bar{I}$	Current deviation from moving average
$\int V_{Ldc}$	Integral of voltage
$CLRP$	Current Limiting Reactor Power
$cov(i)$	Current covariance
CRP	Current Reduction Phenomenon
$fit(i)$	Current fitting approximation
MAD	Median Absolute Value
MLT	Machine Learning Techniques
SE	Surge Energy
$TAVC$	Transient Average Value of Current
$TW(i)$	Current travelling wave

Table 3.1 summarises the protection functions of non-unit protection algorithms reported in the literature for the protection of HVDC grids, while the protection functions reported in Table 3.1 are explained in Table 3.2. It is evident that the majority of the algorithms utilises a combination of criteria to detect and discriminate DC faults. A significant number of the protection algorithms also utilise a direction criterion to distinguish between forward and backward faults, with di/dt being the most widely used directional element. Moreover, there is an equal number of methods that have either separate or shared detection and discrimination functions. In algorithms with separate detection and discrimination functions, UV is typically employed for fault detection. Table 3.1 also reveals that dv/dt and WT are the most commonly used discrimination functions, whilst more than half of the solutions make use of WT or other signal processing techniques.

Table 3.1 also reports the measurement requirements of non-unit protection methods and the corresponding sampling frequency in each case. Most schemes use both voltage and current measurements for the execution of the algorithms, while it is evident that the required sampling frequency can vary from a few kHz to a few MHz.

3.4.2 Unit Protection

Current Differential

Unit protection methods based on the current differential scheme that has been traditionally used as the main protection in AC systems, have also been proposed for HVDC unit protection [147, 205, 206]. Each line relay measures the local current and communicates the measured value to the other end of the line. The result of the comparison between current measurements from both ends is called differential current (or Δi),

and when it exceeds a specified fixed threshold a DC fault is detected.

Current differential is a highly robust method and offers very good selectivity and directionality. Nevertheless, the use of signals from both terminals implies the necessity for a communication link. Communication adds a degree of reliability requirements, and introduces time delays and synchronisation challenges. Therefore, each relay has to compensate for the time delay caused by the communication link in order to retrieve the value of the current at the time point of interest. As communication time delays increase for increasing medium length, the use of current differential protection in HVDC grids with long transmission media can be impracticable. Nevertheless, current differential is a well-suited choice for DC grids with shorter lines (less than 200 km), while also it can be used for busbar protection, where the difference between outcoming and incoming currents is measured and if above the threshold, a busbar fault is detected [147].

Directional Protection

Directional protection is another unit protection method that has been used for DC protection [207]. In this case, each relay communicates only the direction of the current to the other end when a fault is detected. If the relays of the protected line identify a fault in their respective forward direction, a trip command is generated, and the line is isolated. Owing to the simplicity of the transmitted information (e.g. sign of the current), the method is more robust than the current differential method [34]. However, this kind of protection suffers from the same limitations caused by the time delay of the communication scheme and the transmission issues.

Travelling Wave Differential

Travelling Wave Differential (TWD) techniques have been proposed in the technical literature in an effort to improve fault detection speed, robustness against external disturbances and to reduce communication delays. The main principle of TWD methods is based on the fact that in the event of external disturbances (e.g. faults outside the protected medium), travelling waves that enter one end of the transmission medium should be identical with those that appear at the other end. If this condition is not satisfied, then an internal DC fault is detected. In travelling wave differential methods the required communication is in the same direction with wave propagation, resulting in smaller communication delays than conventional unit protection methods.

A phase-domain travelling wave differential protection is presented in [208], in which transmission line models have been developed for the application of the protection scheme using only information contained in the first travelling wave. In addition, a sensitivity analysis of the cable parameters has been realised in [209] to investigate

the impact of potential sources of error on the protection scheme. The unit protection method introduced in [210] uses current and voltage measurements (with 20 kHz sampling frequency) of both ends of a transmission line to calculate the differential voltage travelling wave in the time domain by means of convolution. A method to compensate for unsynchronised data measurements from the two sides of the line is provided. Moreover, a comprehensive analysis of all time delay sources is realised to obtain a total time delay estimation formula.

Other Travelling Wave based Methods

In an effort to overcome the practical challenges related to the application of conventional current differential and directional protection, a few other methods combining travelling wave principles with signal processing tools can be found in the technical literature. In [211], DC currents from both line ends are utilised to distinguish between internal and external faults by applying the WT theory on current travelling waves. The method presented in [212] uses the energy of WT coefficients derived from line current measurements. Moreover, a change in current direction ($dir(i)$) from at least one of the medium ends needs to be identified in order to detect an internal fault. The authors in [213] perform a comparison of the polarities of the voltage across the DC reactors on both ends of an overhead line to discriminate DC faults. In [214], a communication-based scheme is proposed based on cosine similarity measure of travelling waves (CSoTW). The proposed scheme utilises voltage and current measurements at both transmission line ends, which are analysed to derive the cosine similarity of backward and forward travelling waves.

Table 3.3: Taxonomy of unit protection methods according to measuring requirements and detection functions.

Method	**Measurements**		**Sampling**	**Detection**
	Voltage	**Current**	**Frequency**	**Function**
[147]	×	✓	1 MHz	Δi,
[211]	×	✓	100 kHz	WT
[206]	×	✓	100 kHz	Δi
[212]	×	✓	50 kHz	$dir(i)$, WT
[213]	✓	×	50 kHz	$\int v$
[214]	✓	✓	10 kHz	$CSoTW$
[210]	✓	✓	10 kHz	TWD
[208]	✓	✓	–	TWD
[205]	×	✓	–	Δi

Table 3.3 summarises the protection functions of unit protection algorithms reported in the literature for the protection of HVDC grids. In contrast to non-unit protection algorithms, unit protection methods mostly utilise a single detection function as they

demonstrate natural selectivity and directionality. In addition, the measurement requirements of the methods are also reported in Table 3.3, in which similar trends as with non-unit protection can be noticed.

3.4.3 Challenges and Discussion

Unit-protection methods offer inherent selectivity as the protection zones are well defined. However, these methods rely on a communication link in order to obtain signal measurements from the other end of the line. Considering that the fault current rise can be in the range of several kA per ms [146], the performance of unit protection is greatly compromised in HVDC grids integrating lines of several hundreds of kilometres, due to the prolonged communication delays that impede their utilisation for primary protection schemes. Consequently, unit protection methods are typically preferred for backup protection.

Due to the requirement for very fast DC fault detection and isolation, non-unit protection methods are generally preferred against unit protection methods, since they rely exclusively on local measurements. The current trend in non-unit protection focuses around the development of travelling-wave based methods that attempt to capture the information contained within the first incident travelling waves and use that information for detecting and discriminating DC faults. These methods do not achieve naturally selective protection, which makes it challenging to discriminate between internal and external faults. For this reason, series inductors are used to define protection boundaries. Nevertheless, non-unit protection algorithms suffer from sensitivity issues and limited protection reach depending on the length of the lines, the DC reactor size and the fault characteristics, such as fault distance and resistance.

An additional important limitation that was identified through the review for most existing non-unit protection methods is that they have been designed based on extensive off-line simulations using detailed models in EMT-type software, in which only a specific HVDC system is considered and hence, their applicability in other HVDC networks is not guaranteed. The above limitations highlight the need for a generalised methodology that can investigate the practical limitations of non-unit protection and the factors that affect and can be adjusted to extend the reach of the algorithm. Such an approach is introduced in Chapter 4 with the aim to set-up a framework for the design of generalised travelling wave based non-unit protection algorithms that can be flexibly configured for any grid topology and parameters.

The review revealed that voltage derivative and wavelet transform are the most widely used protection functions. A research gap has been identified in the case of wavelet transform as a means of DC fault detection and discrimination. In all the

wavelet-based protection schemes reported in Table 3.1, the design relies exclusively on extensive off-line simulations to determine protection thresholds and other important aspects of the technique. In order to render WT generally applicable for HVDC protection purposes, analytical guidelines and methodologies for selecting the above parameters are needed.

3.5 Review of HVDC Fault Location Methods

Following successful fault clearance in HVDC grids, the next step is to determine the accurate location of the fault along the feeder. As mentioned in the 'IEEE Guide for Establishing Basic Requirements for High-Voltage Direct-Current Transmission Protection and Control Equipment' [215], the additional important equipment stated below should be employed to complement the actions of HVDC protection systems:

- DC line fault locator.
- Transient fault recorder.
- Station synchronisation equipment.
- DC measuring equipment.
- Electrode line monitoring equipment.
- Harmonic monitoring equipment.
- Converter valve cooling control and protection equipment.

Therefore, HVDC fault location is considered an essential task that should be executed promptly after operation of the main HVDC protection system. In detail, the exact determination of the fault position is of vital importance because it will enable acceleration of power system restoration, reduction of operating costs due to non-optimised power flows within the HVDC grid and consequently, it minimises the power outage time and enhances the reliability of the HVDC grid.

Existing fault location methods for HVDC systems that have been proposed in the technical literature can be classified into travelling wave based, reflectometry, model-based, frequency domain and learning-based methods.

3.5.1 Travelling-Wave based Fault Location Methods

Fault location techniques based on travelling waves have been widely used both in AC and DC networks. TW-based fault location can be further divided into single-ended and double-ended. Single-ended TW algorithms calculate the fault location by

determining the time between the arrival of two consecutive travelling waves [216–218]. Consequently, high precision in estimating the travelling wave arrival time is required to guarantee high fidelity fault location. Because of this requirement, very high sampling frequencies in the order of 1-2 MHz are typically used. Double-ended (or two-ended) fault location utilises time-stamped measurements at both ends of the transmission medium and relies on estimating the arrival time of only the first incident travelling wave [219, 220]. Generally, two-ended methods are considered more reliable, since the first reflection has the least distorted signature. Nevertheless, the selection between two-ended and single-ended TW-based methods is typically a result of a trade-off between complexity, cost, and accuracy in fault location estimation. Fault location schemes that have been developed on both principles, typically utilise various mathematical tools to reveal specific features in current and/or voltage signatures.

The authors in [220] propose a double-ended TW-based fault location method using time-stamped measurements (sampled at 2 MHz) of DC voltage and capacitor currents to locate DC faults in HVDC networks with non-homogeneous transmission media. Initially, the faulty segment is identified by solving a set of equations for calculating the fault distance for each segment. The method is accurate and robust against noise, nevertheless, only fault resistances up to 100 Ω were investigated. Moreover, the requirements for synchronised measurements and high sampling frequency could be considered technical barriers for practical applications. In [219], a fault location method is proposed for star-connected MTDC networks using continuous wavelet transform on DC line current signals. Nevertheless, time-synchronised measurements and a high sampling frequency of 2 MHz are required. Moreover, highly-resistive DC faults have not been investigated thoroughly.

In [217], modal voltages and currents are used to implement a single-ended travelling-wave based fault location for HVDC cable bundles. The method depends on estimating the difference in arrival times of fault transients due to their difference in the modal velocities. The method requires voltage and current measurements sampled at 1 MHz, and it has been tested with fault resistances up to 100 Ω.

All **travelling wave-based fault location methods** make use of high sampling rates in order to accurately estimate the fault location. This requirement is commonly considered as the main weakness of TW-based techniques. Additional challenges include the requirement for synchronised measurements (for double-ended methods), accurate estimation of wave arrival time, attenuation of TWs due to fault resistance, as well as the fact that the wave propagation speed of the examined transmission medium should be known. Nevertheless, the theoretical value of propagation speed can be either deduced by the transmission medium geometry or it can be estimated through faults at known fault locations, information which can be obtained during the commissioning

of the fault locator system. In addition, for double-ended methods and due to the high speed of fault travelling waves, the effect of synchronisation mismatch can lead to increased estimation errors of the fault distance. Lastly, cost may be a significant concern in TW-based fault location methods, because of the additional components that are typically required such as the Global Positioning System (GPS) and transducers that are used to capture the travelling waves.

3.5.2 Model-based Fault Location Methods

In an effort to tackle the practical challenges associated with the application of TW-based schemes, model-based fault location methods have been developed. The existing model-based fault location methods are a variation of time domain methods, in which the main concept is to establish a relationship between fault location and the transmission line model based on voltage and/or current measurements from both ends of the faulted line.

In [221], voltage and current measurements from both line ends (time-synchronised measurements) are used to calculate the 1-mode voltage distribution across the Bergeron line model and then the fault distance is estimated. The required sampling rate is 100 kHz and the method has been found to be effective for locating DC fault in long transmission lines with fault resistances up to 500 Ω. The authors in [222], combine TW principles together with the Bergeron line model to construct a time-domain DC fault location method. In addition, the need for synchronised measurements is eliminated by setting as the zero-time reference the sampling point at which the surge arrival is detected at each line end. The method can successfully locate DC faults even with a high fault resistance of 500 Ω; nevertheless, a high sampling frequency (1 MHz) is required. A fault location method for HVDC grids based on a simplified R-L line model for representing transmission lines with reduced computational burden is proposed in [223]. A first-order filter is utilised to eliminate the high frequency components of voltage and current measurements at each line end and hence, distributed line capacitance is ignored. The method has been tested for highly resistive faults (500 Ω) and the estimation errors are less than 1% in all DC fault cases.

Model-based fault location methods form an attractive alternative for reducing the complexity while maintaining to some extent high accuracy. Nevertheless, significant assumptions are usually made which are not necessarily applicable to all transmission line geometries. Moreover, these methods typically rely on extended fault data windows (typically more than 10 ms) in order to estimate reliably the fault location. Consequently, their applicability in HVDC grids that use high-speed DC circuit breakers is uncertain.

3.5.3 Frequency-Domain based Fault Location Methods

Besides time domain fault location methods, frequency domain-based methods have also been presented in the literature. These methods typically obtain the information regarding the fault location from frequency spectrum analysis of line measurements.

Compared to the conventional TW-based fault location methods, the proposed methods presented in [224, 225] eliminate the need to identify the arrival time of the surges. The proposed ideas utilise the dominant natural frequency in the spectrum analysis of TW (also known as natural frequency) which is used to calculate the wave velocity, reflection coefficients and reflection angles and then estimate fault location. These methods require single-ended voltage or current measurements, while a sampling frequency of only 100 kHz, and 50 kHz respectively is required. However, the methods have been tested for high impedance faults only up to 100 Ω.

Based on TW principles together with Hilbert-Huang Transformation and Ensemble Empirical Mode Decomposition (EEMD), a fault location method is proposed in [226]. The HHT and EEMD are used to obtain the time-frequency graph from which the arrival time of the waves and the corresponding instantaneous frequency are derived. The propagation velocity is then calculated (by using the instantaneous frequency) and together with the arrival time a double-ended technique is used to calculate the fault distance. The sampling requirement of such method is 1 MHz, while highly resistive faults have not been investigated.

Frequency domain methods eliminate the need to capture the travelling wave heads and typically require only single-ended measurements. Nevertheless, when the DC fault occurs near the ends of the transmission medium, the dominant natural frequency can reach extreme values and exceed the maximum frequency of the spectrum, resulting in dead zones at the end terminals. In addition, the dominant natural frequency can be significantly altered for faults with high fault resistance, resulting in significant location estimation errors.

3.5.4 Reflectometry

Reflectometry is a measurement technique that is used to determine the electrical lines characteristics through signal injection in the faulted line and then observing the reflected waveforms. Depending on the detected response and the captured current and voltage signatures, the fault location can be determined. Such methods can be also found in the open literature under the term “active methods”. In order to inject a signal in the faulted medium, signal pulse generators are required as well as a set of detectors for capturing the reflected signals. The signal generators typically inject high-frequency low-voltage signals to the faulted line and then the observed anomalies (due

to the presence of DC faults) are processed for fault location estimation.

Typically, reflectometry techniques can be applied on either time or frequency domain. In [227], a fault location algorithm based on stationary wavelet transform is proposed. High-frequency injected signals are captured by an oscilloscope, decomposed by wavelet transform and rescaled by multiple-scale correlation of approximations. The actual fault location is estimated through the time delay between two consecutive incidents. A fault localisation technique based on tangent distance pattern recognition and time-frequency domain reflectometry is proposed in [228]. In this method, a reference signal is initially injected into submarine cables using dedicated signal generators. Subsequently, the resulting signal from reflection to the fault location is captured, and along with the reference signal they are stored for post-fault analysis using Euclidean and tangent distance and time-frequency distribution. The accuracy of the method has been validated in practice on a HVDC cable section. Nevertheless, 8 Ghz and 312.5 MHz sampling frequencies are used for the reference and reflected signals, respectively, which implies the use of complicated and expensive equipment.

Reflectometry methods allow for the accurate fault location estimation, while also the measurement data are not affected by the protection systems utilised within the HVDC grids. Nevertheless, these methods require external equipment, which is typically a fault recorder and a signal pulse generator, and high sampling rates in the order of MHz-GHz. In addition, the use of external equipment implies the necessity for a site visit for assembly and disassembly of the equipment, a procedure which could take several days or months, while also a site visit may not be always possible.

3.5.5 Learning-based Fault Location Methods

A recent category among fault location approaches involves the application of learning-based techniques, which have been widely utilised in fault classification and location applications in AC networks. Recently, there is an increasing interest in employing such tools for fault location estimation in HVDC systems [229–234].

A learning-based method on post-fault voltage measurements sampled at 80 kHz is introduced in [230]. The fault location scheme estimates the fault distance by calculating the Pearson coefficients between existing cases (with unknown fault location) and pre-simulated voltage patterns. The method has been found to be accurate for long transmission lines and for different types of faults. However, it has been tested only for fault resistances up to 80 Ω, while obtaining a data base of training patterns may always be a challenging task.

A method based on DC current measurements obtained from a network of distributed sensors is proposed in [234]. The method utilises current measurements ob-

tained at 5 kHz to apply a conventional double-ended TW-based fault location technique. A machine learning approach is then used to reduce the distance error arising from the moderate sampling frequency.

The method in [229] is based on non-synchronous voltage measurements captured at 100 kHz on both line ends. The proposed method utilises Empirical Mode Decomposition (EMD) to extract the high-frequency component in the fault signal and then Convolutional Neural Network (CNN) to classify the data and estimate the fault location. The method has been tested for both pole-to-pole and pole-to-ground faults and it was shown that it can reliably and accurately locate line faults under fault resistance up to 5200 Ω.

In [233], a method based on Extreme Machine Learning (EML) is suggested to locate faults in multi-terminal high voltage direct current systems. S-transform and wavelet transform are utilised for extraction of the features used for the learning process. The methods require voltage and current measurements sampled at 500 kHz and the entire scheme has been validated for faults with resistances up to 100 Ω.

An alternative approach is proposed in [235], in which initially a support vector machine (SVM) classifier is utilised for identification of the faulted section. Then, traditional single-ended TW analysis is used in order to estimate the fault location. For the implementation of this method, both voltage and current measurements of one end are required. Nevertheless, the scheme has been validated only for faults with for fault resistance values of up to 70 Ω. The method in [231] is also based on SVM algorithm to estimate the location of a fault on a HVDC line. The method requires AC voltage, DC voltage and DC current measurements obtained at 1 kHz or 4 kHz (data for half cycle before and after the occurrence of a fault are used). The method has been tested in both pole-to-pole and pole-to-ground faults; however highly resistive faults have not been investigated.

Learning-based methods provide an attractive means of intrinsically understanding and extracting the underlying features on currents and voltage signatures in the event of DC faults in HVDC systems. Nevertheless, the biggest challenge for these methods is the requirement for sufficient and very often extensive data sets in order to train the employed machine-learning algorithm. Due to the limited experience and availability of DC fault records, the training data set is typically collected through extensive and iterative offline simulations (e.g. using EMTDC-type software). This raises concerns in terms of the reliability of the training process, while also the resulting learning-based solution may applicable only for the specific test system under study.

3.5.6 Challenges and Discussion

The review on the existing methods revealed that there is a wide range of options for locating DC faults in HVDC systems. Nevertheless, each category of solutions is accompanied with its own advantages and technical challenges; the latter are summarised in Table 3.4.

Table 3.4: Classification of fault location methods and technical challenges.

Fault Location Category	Technical Challenges
Travelling waves	• Need for high sampling frequencies • Need for time-synchronised measurements • Requirement for precise capture of travelling waves - Use of advanced mathematical tools • Susceptibility to highly resistive faults • Reliable communication channel (for two-ended)
Model-based	• Trade-off between accuracy and computational burden • Requirement for extended data window (>10ms)
Frequency domain	• Dead zone at the ending terminals • Susceptibility to highly resistive faults that can distort natural frequency
Reflectometry	• Need for external equipment • Extremely high frequencies (MHz or even GHz) • Site visit is essential for the assembly of testing equipment
Learning-based	• Complexity and computational burden • Data acquisition issues. Huge data set is usually required and due to limited DC fault records availability, extensive iterative simulations are essential for extracting the underlying features • Dependency on selected data and applicability only for the HVDC grid system under study

Table 3.5 summarises the measurement requirements of HVDC fault location methods and the main operation principles or algorithms used. It is evident that in comparison to HVDC protection algorithms, fault location techniques are characterised by increased demands in terms sampling frequency requirements. This is attributed to the fact that enhanced accuracy in fault location estimation is of paramount importance to expedite post-fault maintenance and reduce the downtime of the faulted component. Hence, fault location methods require finer capture of fault transients, resulting in the

utilisation of significantly higher sampling frequencies. The operation of most methods, especially when high sampling frequencies are used, is based on TW principles.

Table 3.5: Taxonomy of HVDC fault location systems according to voltage, current and sampling frequency requirements.

Method	Measurement		Sampling frequency	Operating principles & Algorithms
	Voltage	Current		
[219]	×	✓	2 MHz	TW principles, WT
[220]	✓	✓	2 MHz	TW principles, WT
[218]	×	✓	1 MHz	TW principles, Graph theory
[226]	×	✓	1 MHz	TW principles, HHT, EMD
[217]	✓	✓	1 MHz	TW principles, Modal analysis
[222]	✓	×	1 MHz	Bergeron model
[233]	✓	✓	500 kHz	WT, EML, S-Transform
[216]	×	✓	200 kHz	TW principles, WT, Logistic function
[235]	✓	×	200 kHz	WT, SVM classifier
[236]	×	✓	135 kHz	TW principles, WT
[224]	✓	✓	100 kHz	MUSIC method
[229]	✓	×	100 kHz	WT, EMD, CNN
[237]	×	✓	96 kHz	Pearson coefficient
[230]	✓	×	80 kHz	Pearson coefficient
[223]	✓	✓	50 kHz	R-L line model
[221]	✓	✓	6.4 kHz	TW principles, WT, Bergeron model
[234]	×	✓	5 kHz	TW principles, WT, Pearson coefficient
[231]	✓	✓	1-4 kHz	SVM classifier

It is worth noting that the majority of the above work proposes fault location techniques that are applicable for point-to-point HVDC links, which are commonly protected by AC circuit breakers from the AC side of the converter. This implies that there is a prolonged time window available (2-3 AC cycles) for post-fault analysis. However, HVDC grids are suggested to operate with high-speed DC circuit breakers at both ends of each transmission medium, in an effort to isolate the faulted medium as soon as possible, guarantee safety of the HVDC grid components and to minimise the detrimental effects of DC faults on the DC and AC side of the grid. Consequently, the available data windows for applying a DC fault location technique for HVDC grids can be confined to only several milliseconds after fault occurrence. Especially if hybrid DCCBs are utilised, the data window can be less than three milliseconds, thus making fault localisation a more challenging task.

In addition, an increasingly challenging task in HVDC fault location arises when the network includes hybrid lines that have segments of both overhead lines and cables. This is very common for OHL-based systems, in which small cable segments are introduced near the converter terminals, or for HVDC systems that transmit electricity across water bodies such as seas and lakes, where underground cables are used but the converter terminals are not located near the shore of the water body [220]. This issue has received very limited attention and the only solutions that attempted to tackle this

problem [220,235,236] face the same challenges of TW-based techniques. In conclusion, there is a need for development of novel fault location techniques, which can be applied to networks with hybrid feeders based on short data windows.

3.6 Review of Measurement Technologies for HVDC Protection and Location

The proper function and performance of HVDC protection and fault location algorithms is greatly dependent on the quality of measurements fed to the protection and fault location devices by the corresponding measuring schemes. One of the main observations made through the review in Sections 3.4 and 3.5 is that much of the reported work is developed on a conceptual level, while practical aspects of the proposed methods are neglected. For example, it is commonly assumed that voltage and current measurements are always accessible even when very high sampling rates are utilised. This section aims to combine the findings of the review on the available measuring technologies conducted in Chapter 2 with the measurement requirements of existing HVDC protection and fault location algorithms as these were highlighted in Tables 3.1, 3.3, and 3.5. In detail, this section constitutes a mapping of protection and fault location functions on a frequency diagram against the available voltage and current measuring technologies to illustrate the potential for applicability based on the existing technologies, ultimately unlocking insights for selecting measuring equipment based on the desirable characteristics of protection and fault location systems.

With respect to voltage measurements, there is a limited number of options (refer to Subsection 2.7.1). These mainly comprise of the RC voltage divider that achieves a high bandwidth in the order of MHz, and the hybrid optical voltage sensor that may emerge in future applications. The superior frequency response of the former, combined with its relative maturity, have rendered RC-voltage divider the main technology used in HVDC applications. By inspecting the frequency requirements of the various voltage-based protection and fault location methods, it is observed that they fall within the available bandwidth of RC-voltage divider. Hence, it can be concluded that voltage measurements for HVDC applications are considered readily accessible, indicating a competitive advantage of protection and fault location solutions that are based exclusively on voltage signals.

For current measurements, there is wider range of options, with each technology occupying a different frequency spectrum. In Figure 3.8, the current-based protection and location methods are mapped on a frequency diagram against the available current measuring techniques to illustrate the potential for applicability based on the existing

technologies. It is worth noting that the frequency range achieved by each current sensing scheme, mainly refers to the bandwidth of the primary sensor, whereas the overall bandwidth of the complete measuring system may be further restricted by the secondary converter, the corresponding data acquisition system and signal-processing electronics.

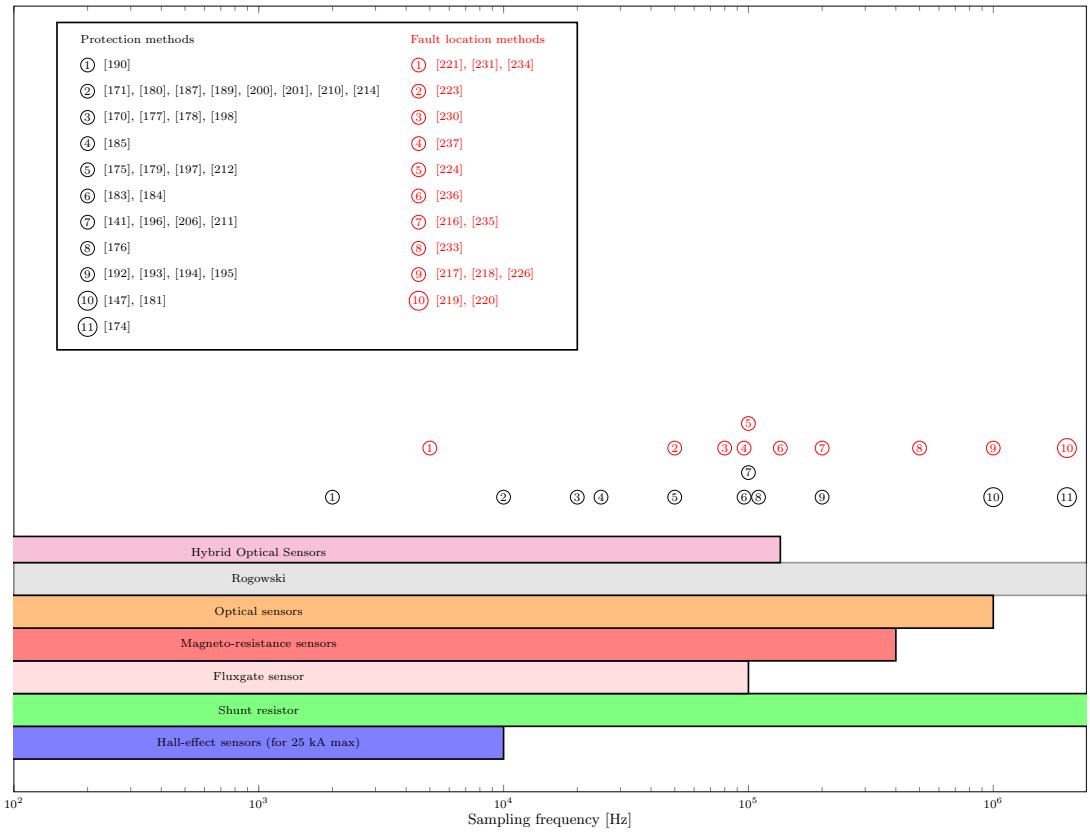


Figure 3.8: Mapping of HVDC protection and fault location methods against sampling frequency and current measuring technologies.

An initial analysis of the diagram reveals a distinctive difference in the frequency range between HVDC protection and HVDC fault location algorithms. It is evident that the majority of non-unit and unit protection solutions is concentrated in a frequency spectrum ranging from 10 kHz to 100 kHz. This is explained by the fact that DC fault detection aims to detect every probable fault within the relay's protection zone, without the need for extremely accurate capture of fast transients during DC faults and therefore, high sampling frequencies are not typically required. This is especially true for unit protection schemes, which very often rely on simplified means of comparison between current measurements from both ends of the protected transmission medium. On the contrary, the vast majority of fault location functions utilises sampling frequencies in the range of 100 kHz to 2 MHz. This is attributed to the

fact that enhanced accuracy in fault location estimation is of paramount importance to expedite post-fault maintenance and reduce the downtime of the faulted component (e.g. DC cable). Hence, fault location methods require finer capture of fault transients, resulting in the utilisation of significantly higher sampling frequencies.

Based on these findings, it is evident that there is greater variety of options among current measuring technologies for supporting current-based DC fault detection and discrimination functions. In this case, the selection of the appropriate measuring instrument can be realised according to the sensor's reliability, accuracy, longevity, dynamic range, size and weight concerns, cost etc., while it is likely that there might be multiple current sensors that satisfy the required performance criteria. In the case of fault location functions with increased sampling rates, it can be seen from the diagram that the available sensors with the capability to measure faster fault transients are significantly reduced. It is noteworthy that groups ⑨ and ⑩ approach the bandwidth capacity limit of existing current instruments. Moreover, applications with high sampling rates are also accompanied with increased requirements in terms of signal processing electronics and advanced output interfaces, noise resilience, reliability and inevitably cost. Therefore, the implementation of such high-bandwidth demanding applications with suitable current instruments is a more complex task.

Taking wavelet transform as an example, it can be noticed from the diagram and Table 3.1, 3.3, and 3.5 that it is used as the main function in several protection algorithms (groups ①-⑦), in which sampling frequencies are in most cases less or equal to 100 kHz. In addition, the same detection function has been employed in several occasions for fault location purposes (groups ① and ⑦-⑩), in which the vast majority utilises significantly higher sampling rates. Since DC protection and DC fault location are anticipated to be integral parts of future HVDC grids and given that voltage and/or current measurements are required in both cases, it is reasonable to assume that the measuring instruments will be shared for the purposes of both applications.

Therefore, a convergence between the requirements of both applications is desired. Based on the reported measuring requirements of both voltage and/or current-based methods, such a convergence seems to be achieved for sampling frequencies around 100 kHz that concentrate a significant proportion of the detection and location functions. With specific reference to DC protection and fault location applications, the IEC 61869-9 promotes the sampling frequency of 96 kHz. In relevant research investigating its performance and suitability in [144, 183, 184], it has been reported that a sampling frequency of 96 kHz is adequate for capturing DC-side fault transients and therefore it can be utilised for both HVDC protection and fault location applications. On this basis, common voltage and current measuring devices that comply with this standard can be used for both applications.

3.7 Simulation Analysis of DC Faults in HVDC Grids

In this section, an analysis of the transient phenomena that occur as a result of DC faults in HVDC grids is conducted. Initially, a representative HVDC grid test network is introduced, which was developed based on the review of HVDC technologies made in Chapter 2. The same test network will be used in the remainder of the thesis, including the simulation analysis in this section. Afterwards, a DC fault characterisation of the HVDC grid is performed with the aim to reveal the system-wide trends during such events. Then, the analysis focuses on a single protection relay location, (also used as the point of measurement), with the aim to identify the DC fault characteristics that could be useful for non-unit protection design.

3.7.1 HVDC Grid Test Network

Figure 3.9 shows the four-terminal meshed HVDC grid test network that has been modelled with PSCAD/EMTDC simulation tool. The network is operating at ±320 kV DC in a symmetric monopolar configuration.

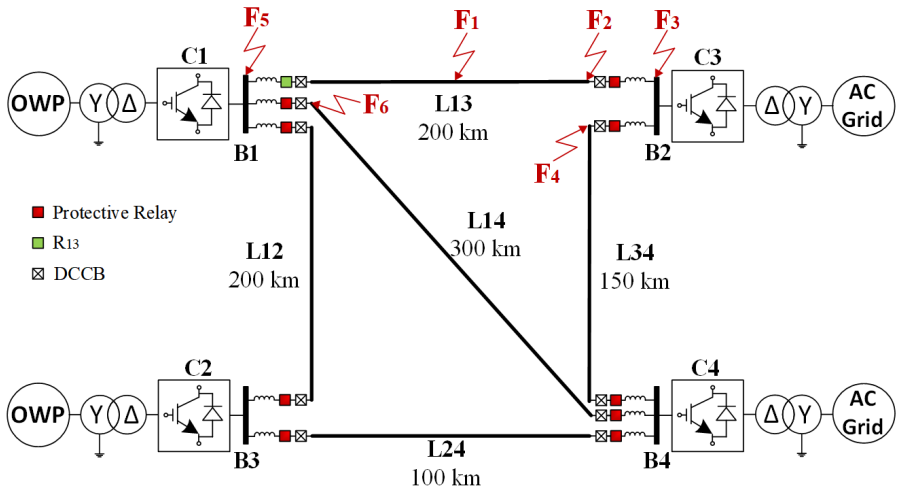


Figure 3.9: HVDC grid test network.

All converters are HB-MMCs, modelled based on the average value modelling approach including the appropriate modifications to accurately represent the converter behaviour during the blocking state as described in Subsection 2.2.5. All DC links are represented based on the frequency-dependent cable model presented in Subsection 2.6.3 using the corresponding model available in PSCAD library. The network architecture, converter protection logic and cable parameters are adopted from [81]. At the output of each converter, small capacitors (2.5 μF) are connected between each system pole with a common grounded midpoint. The distributed droop control presented in

subsection 2.4.2 is used as the power sharing control scheme of the system. In particular, converters C1 and C2 are configured to control the active power of the offshore wind farms, while converters C3 and C4 employ voltage droop control in order to regulate the DC system voltage.

Protective relays and current limiting inductors in series with DCCBs are placed at each end of all cables. The DCCBs are modelled based on the approach described in Subsection 2.5.4 with 5 ms operation speed. For the rest of this thesis, R_{ij} refers to the relay located at the end i of line L_{ij}. Similarly I_{ij} and V_{ij} correspond to current and voltage measurements at the relay location R_{ij}, respectively. Moreover, letters p and n in the subscript indicate positive pole and negative pole measurements. Unless otherwise stated, the transducer and measurement systems are assumed ideal. The main parameters of the HVDC grid and the MCCs are summarised in Table 3.6.

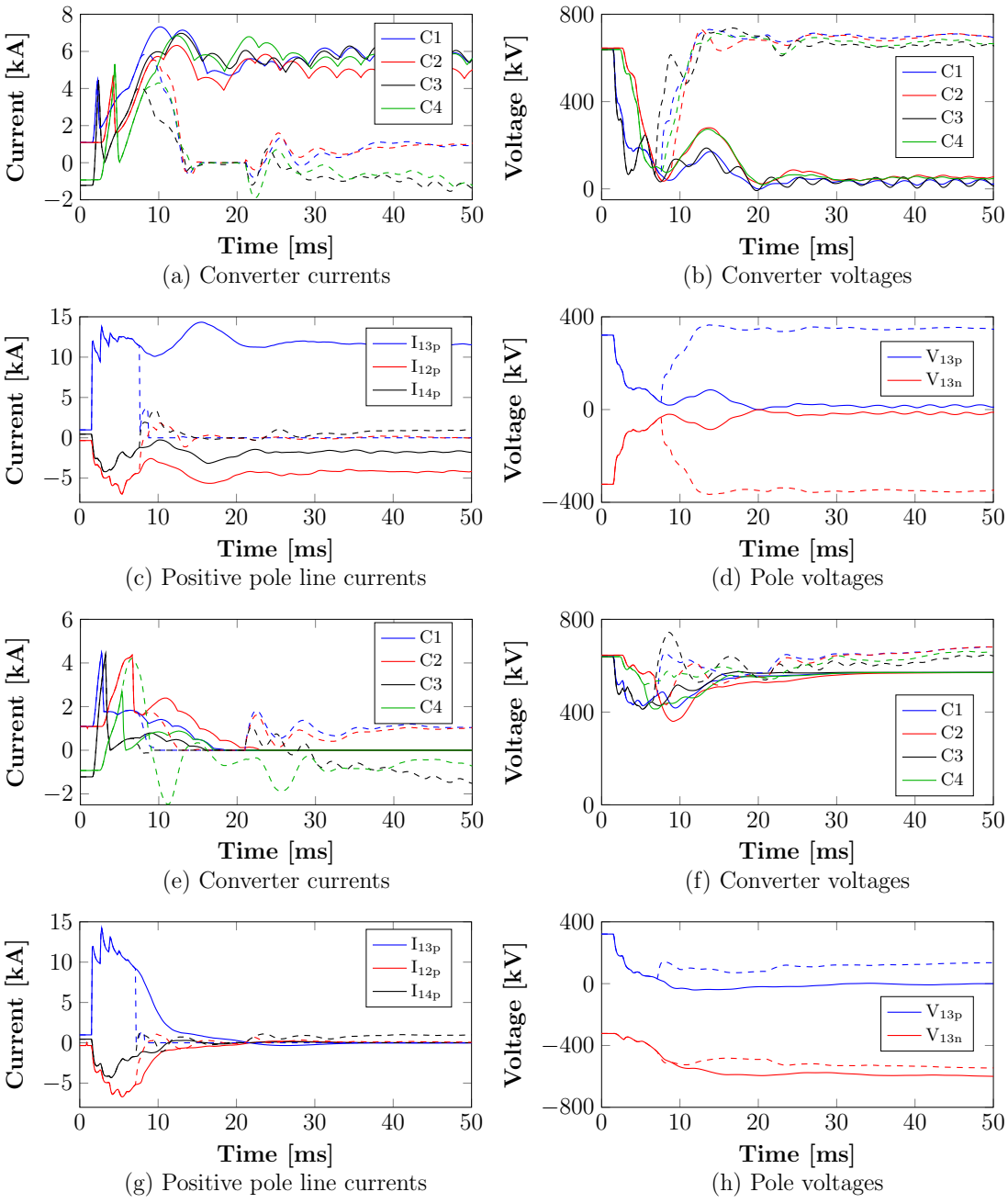
Table 3.6: HVDC grid test network and converter parameters.

Parameter	Value
Nominal DC voltage	± 320 kV
Rated power (C1∼C4)	1000 MVA
Active power setpoint (C1∼C4)	700,700,−800,−600 MW
Reactive power setpoint (C1∼C4)	100,100,100,100 MVAr
Converter arm inductance	42 mH
Converter arm resistance	0.08 Ω
Converter arm capacitance	31.42 μF

3.7.2 Characterisation of HVDC Grid Fault Response

To investigate the HVDC grid fault response, DC faults are applied at t=0 s at the midpoint of L13 at location F_1 shown in Figure 3.9, when line inductors value is set to 0 mH to show the natural response of the system. Figure 3.10 demonstrates the results for a PTP fault in 3.10(a)-(d) and a PTG fault in 3.10(e)-(h). In the figure, converter voltages and currents, and line voltages and currents are shown for both the prospective case without breaker actions (solid lines) and for the interrupted case (dashed lines).

Figures 3.10(a)-(d) show that the PTP fault leads to rapid increase and high steady-state values for all converter and line fault currents while the converter, positive pole and negative pole line voltages collapse within 20 ms from fault inception. Moreover, the three stages of the HB-MMC fault behaviour during PTP faults (as described in Subsection 3.2.2) can be noticed in 3.10(a). The SM capacitors discharge stage lasts until the converters are blocked (IGBTs turn off), i.e. at t≈2 ms for C1 and C2, and at t≈4 ms for C3 and C4, as indicated by the initial peaks of the converter currents. After the IGBTs in the converter arms turn off, the converters proceed to a transitional



(a) Converter currents (b) Converter voltages

(c) Positive pole line currents (d) Pole voltages

(e) Converter currents (f) Converter voltages

(g) Positive pole line currents (h) Pole voltages

Figure 3.10: Converter currents, converter voltages, cable currents and cable voltages for: (a)-(d) pole-to-pole fault, and (e)-(f) positive pole-to-ground fault. Solid lines correspond to the natural response of the HVDC system (without breaker actions), and dashed lines correspond to the system response when the fault is cleared by DCCBs.

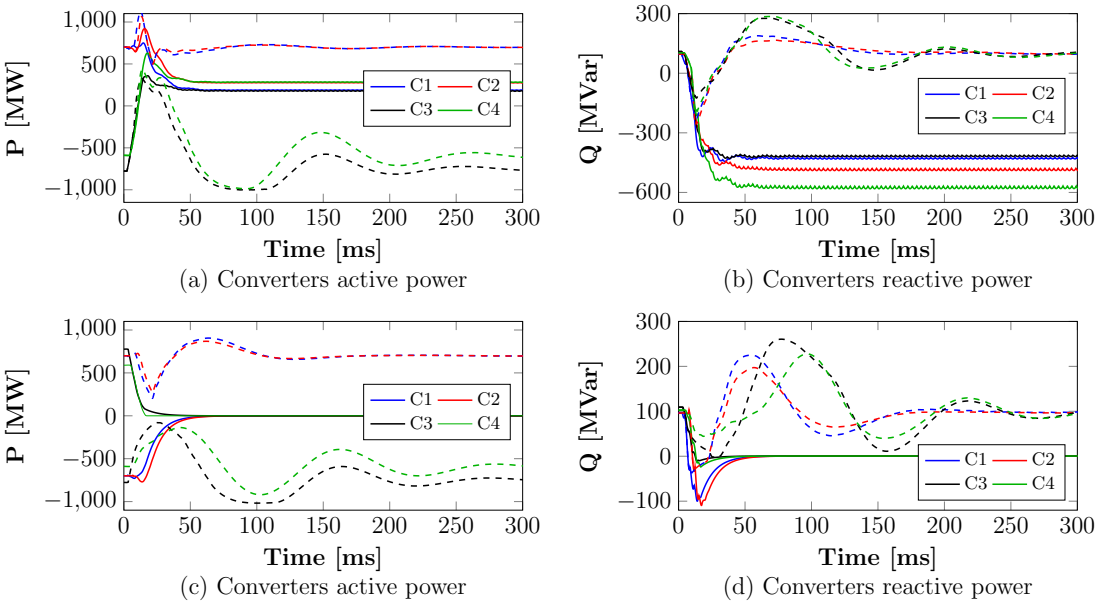
state during the arm current decay stage, followed by the grid current feeding stage in which the converter currents reach a steady state value approximately at t=20 ms.

In the interrupted case, the fault current of the faulted cable is interrupted by

the DCCBs of L13 as seen from I_{13p} in Figure 3.10(c). It is evident in this case that fast DCCBs lead to quick recovery of system voltages and currents. Following fault clearance, the converters are deblocked at t=20 ms, and the converter and pole voltages are quickly restored close to nominal values. Similarly, the converter and line currents reach a new steady state value at t≈40-50 ms.

For the PTG fault case, Figures 3.10(e) and 3.10(g) show that converters and cables demonstrate high initial transient currents but almost zero steady-state fault currents. Figure 3.10(f) illustrates that the impact of the PTG fault on converter voltages is less distinct than the PTP fault and results in reduced voltage collapse. In Figure 3.10(h) it is shown that the faulted pole voltage collapses to zero, while a persistent over-voltage is observed on the healthy pole. In the interrupted case, the DCCBs of the faulted pole are tripped (as seen from I_{13p} in 3.10(g)), and similar to the PTP fault, converter currents and voltages quickly recover to new steady-state conditions. Nevertheless, it is evident from 3.10(h) that the over-voltage on the healthy pole persists, which implies that additional pole-rebalancing measures should be taken.

To examine the impact of DC faults on the HVDC grid power transfer capability, the active and reactive powers of each converter are demonstrated in Figure 3.11(a)-(b) for the PTP fault, and in 3.11(c)-(d) for the PTG fault. The negative sign in power indicates that power is exported from the DC system to the AC networks.



(a) Converters active power
(b) Converters reactive power
(c) Converters active power
(d) Converters reactive power

Figure 3.11: Converters active and reactive power for: (a)-(b) pole-to-pole fault, and (c)-(d) positive pole-to-ground fault. Solid lines correspond to the response of the HVDC system without breaker actions, and dashed lines correspond to the system response when the fault is cleared by DCCBs.

In the prospective case, due to blocking of all converters, the active power and reactive power capability is lost for both fault types. In the interrupted case, power-controlling converters C1 and C2 experience reduced disturbances as opposed to the converters regulating the DC voltage (C3 and C4), which experience prolonged active and reactive power perturbations. It is worth noting that regardless of the type of fault, power recovery times are in the order of a few hundreds of milliseconds. This suggests that the surrounding AC networks should be in a position to tolerate such power disturbances to avoid system stability issues, otherwise, additional measures are required to mitigate the effects of DC faults. Alternatively, fault tolerant converters coupled with appropriate protection strategies can be employed to manage and expedite system restoration. This observation has led to the development of a fault management strategy for enhanced DC-side fault management in HVDC grids (based on an efficient customised MMC topology), which will be introduced in Chapter 6.

3.7.3 Impact of Fault Characteristics and Inductive Termination

The previous subsection performed an analysis of the fault response of the entire HVDC grid during different fault types (PTP or PTG) for a single fault location and fault resistance (R_f=0 Ω) without inductive termination at the line ends. In this section, the analysis is extended to investigate the effect of fault parameters along with the effect of current limiting series inductors on the fault signatures. Towards this aim, PTP faults are applied on cable L13 and DC voltage and current measurements are captured at the location of protection relay R_{13} (also shown in Figure 3.9). In addition the DCCBs are deactivated to observe the natural fault voltage and current response.

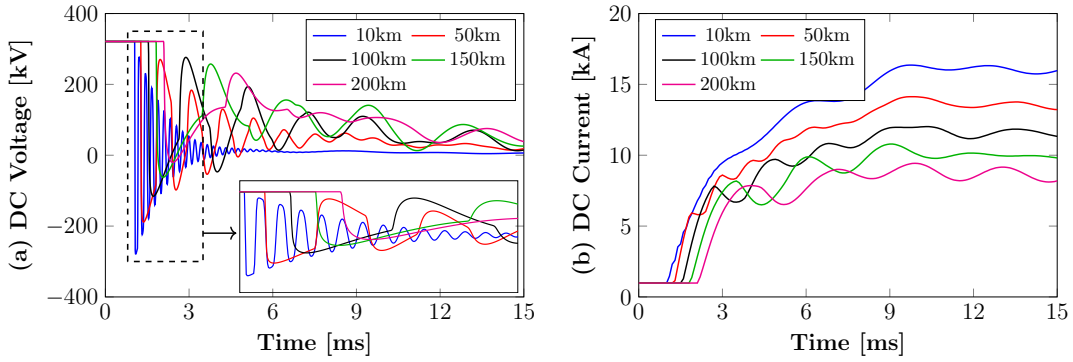


Figure 3.12: Traces of (a) DC voltage and (b) DC current for PTP faults at various points along L13.

In Figure 3.12, current and voltage profiles are shown for PTP faults with varying distances to fault when 50 mH series inductors are used. It is evident that the fault initiated travelling waves arrive at the relay location sooner for closer faults and that

shorter fault distances lead to more dense travelling wave reflections with more pronounced effect on voltage traces rather than current traces. In detail, it is shown in Figure 3.12(a) that each incident travelling wave causes a distinct sharp edge on DC voltage, a trend that becomes less prominent for increasing distances to fault, for which the changes in voltage profiles become more gradual. By observing Figure 3.12(b), it is seen that the DC current magnitude is reduced as fault distance increases. These trends are attributed to the increasing values of cable resistance and inductance in the fault path for greater distances to fault which provoke more severe attenuation on the induced travelling waves.

In Figure 3.13, current and voltage profiles are shown for PTP faults at the midpoint of cable L13 with varying fault resistances. In this case also, 50 mH series inductors are installed at all cable ends. It is observed that high fault resistance values significantly restrain the fault current magnitudes and blunt the edges on DC voltage caused by travelling wave reflections, thus also leading to reduced voltage drops. Based on these findings, it becomes evident that highly-resistive faults lead to less harmful consequences to the DC network, but on the downside, the higher the fault resistance the greater the risk for the DC fault to not be detected by the protective relay.

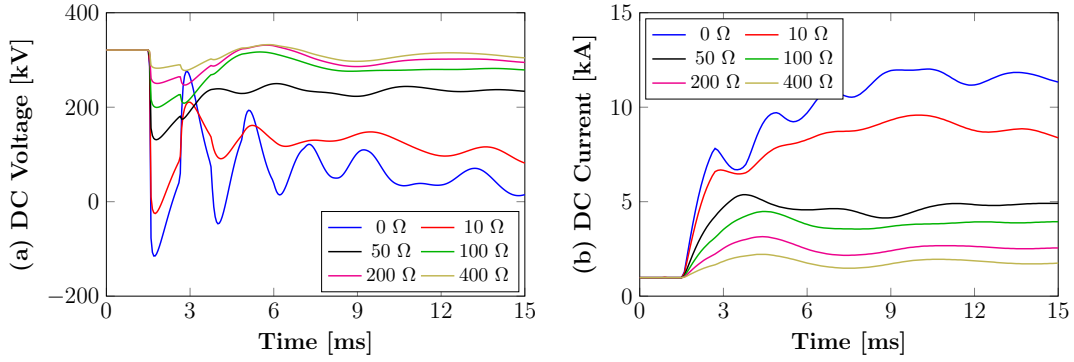


Figure 3.13: Traces of (a) DC voltage, and (b) DC current for PTP faults at midpoint of L13 with varying fault resistance.

PTP faults at the same fault location are repeated (with R_f=0 Ω) for different sizes of current limiting series inductors and the results are shown in Figure 3.14. Figure 3.14(b) displays graphically the main reason behind the utilisation of series inductors with DCCBs in HVDC grids, which is that greater sizes of series inductors lead to reduced rate of rise of fault currents, thus allowing the breakers to act before the maximum current breaking capability is exceeded (or effectively reducing the maximum current to be interrupted). In addition, in Figure 3.14(a) it is shown that an increase in the series inductor size also provokes to a small extent steeper edges on the DC voltage profiles and smooths out the DC voltage between successive travelling wave reflections

and consequently, the points of travelling wave arrivals become more distinct. From all the cases considered in this subsection, it becomes evident that in the presence of inductive termination, travelling wave reflections are more distinctive in voltage traces as opposed to current traces. For this reason, DC voltage measurements are considered more suitable to analyse the nature of DC faults and are therefore preferred for non-unit protection applications.

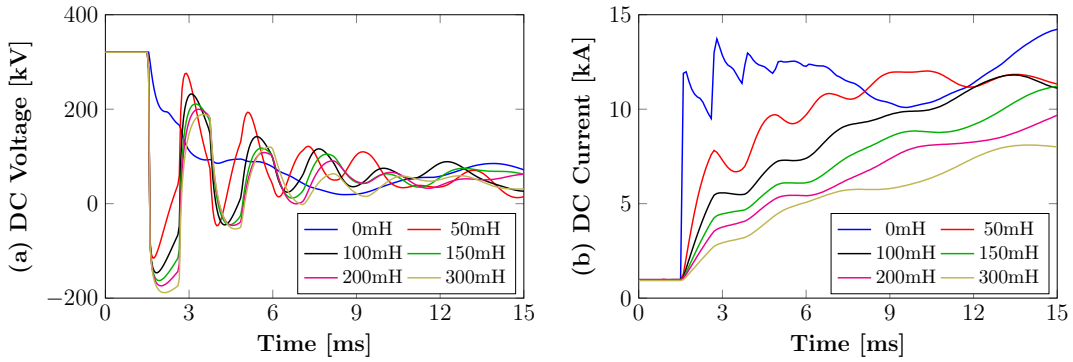


Figure 3.14: Traces of (a) DC voltage, and (b) DC current for PTP faults at midpoint of L13 for various sizes of current limiting series inductors.

3.7.4 Analysis of Non-unit Protection

In an effort to identify the challenges of non-unit protection and evaluate common existing protection algorithms, an analysis has been carried out for eight different fault scenarios that cover a range of internal and external faults (with respect to the protection zone of R_{13}, i.e. cable L13), the details of which are provided in Table 3.7. The fault location of each fault scenario in the test network is also depicted in Figure 3.9. The DCCBs are deactivated to show the natural fault response for longer duration, while 50 mH inductive termination is considered.

Table 3.7: Considered fault scenarios for analysis of non-unit protection.

Fault Scenario	Fault Location	Description
S1	F_1	Internal fault at midpoint of L13
S2	F_2	Internal fault at the end of L13
S3	F_2	Internal fault at the end of L13 (R_f=200Ω)
S4	F_2	Internal fault (PTG) at the end of L13 (R_f=200Ω)
S5	F_3	Forward external fault at bus B3
S6	F_4	Forward external fault at the start of L34
S7	F_5	Reverse external fault at bus B1
S8	F_6	Reverse external fault at the start of L14

Scenarios S1-S4 refer to DC faults that are inside the protection zone of the investigated relay R_{13}. In detail, S1 is a PTP fault at the midpoint of L13, and S2, S3, S4 refer to a solid, highly resistive PTP fault, and highly resistive PTG fault at the end of cable L13 (end of the protection zone). Fault scenarios S5 and S6 refer to forward external solid PTP faults right after the protection zone (location F_3) and at the beginning of cable L34 (location F_4), respectively. Scenarios S7-S8 correspond to reverse (backward) external PTP faults at bus B1 behind relay R_{13} and at the beginning of cable L14, respectively (locations F_5 and F_6 in Figure 3.9).

The voltage profiles (measured at the relay location) are shown in Figure 3.15(a) for the internal faults, and in Figure 3.15(b) for the external faults, respectively. An initial investigation of the voltage profiles shows that even for remote resistive internal faults (scenarios S3 and S4), there is a considerable drop in DC voltage. This explains the fact that UV has been widely used in the literature for simple DC fault detection (see Table 3.1). Nevertheless, it can be seen that the drop in DC voltage in scenarios S5-S8 is considerably higher than the voltage drop in scenarios S3-S4 and hence, discrimination between internal and external faults is not achieved by the UV criterion. Moreover, DC voltage cannot provide an indication for the direction of the fault, since reverse external and forward external faults result in similar voltage signatures.

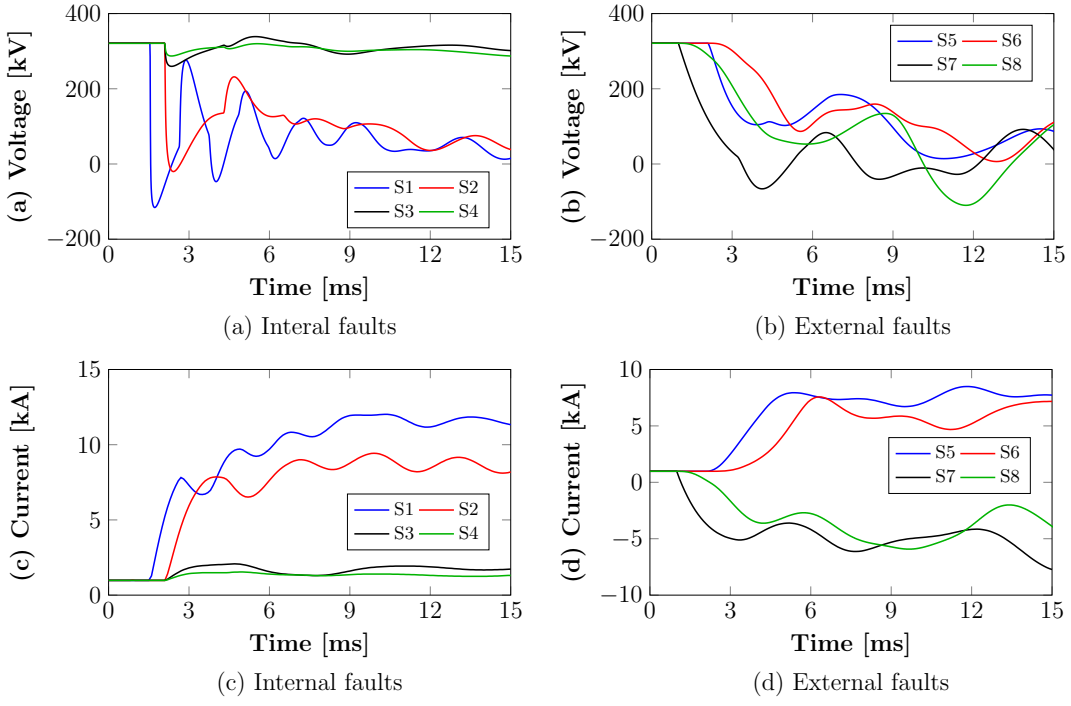


Figure 3.15: Voltage profiles for (a) internal faults (scenarios S1-S4), (b) external faults (scenarios S5-S8), and current profiles for (c) internal faults, (d) external faults.

It can be noticed from Figure 3.15(a) and 3.15(b) that the sharpness of DC voltage drop caused by the internal faults is more pronounced with respect to the voltage drop caused by external faults, in which the rate of descent of DC voltage is more gradual. This is attributed to the presence of inductor boundaries, which filter the high frequency components of voltage travelling waves originating from faults outside the protection zone of relay R_{13}.

In addition, the current profiles for the internal faults are provided in Figure 3.15(c), and for the external faults in Figure 3.15(d). By inspecting the current profiles for scenarios S3 and S4 it is evident that typical over-current protection will fail to detect these internal faults, since the maximum observed current is comparable to the nominal current. On the other hand, external fault scenarios S5 and S6 result in significantly higher fault currents. In contrast to voltage signals, the reverse faults can be identified in the current signals due to the provoked current direction reversal.

Figure 3.16 shows the output of the di/dt algorithm when it is applied at the relay measurements for all fault scenarios. Figure 3.16(a) illustrates that all forward faults produce distinctive positive changes in the di/dt output, but similar to OC, the algorithm cannot provide discrimination between internal fault scenarios S3, S4 and forward external fault scenarios S5 and S6. Moreover, 3.16(b) shows that di/dt displays distinct negative values for reverse faults. For this reason, di/dt is commonly used as a direction criterion in non-unit protection schemes, and especially in voltage-based schemes that typically cannot determine the fault direction.

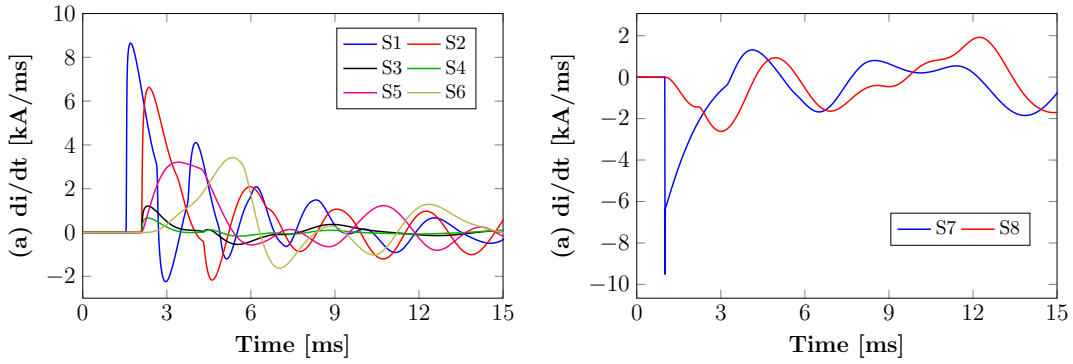
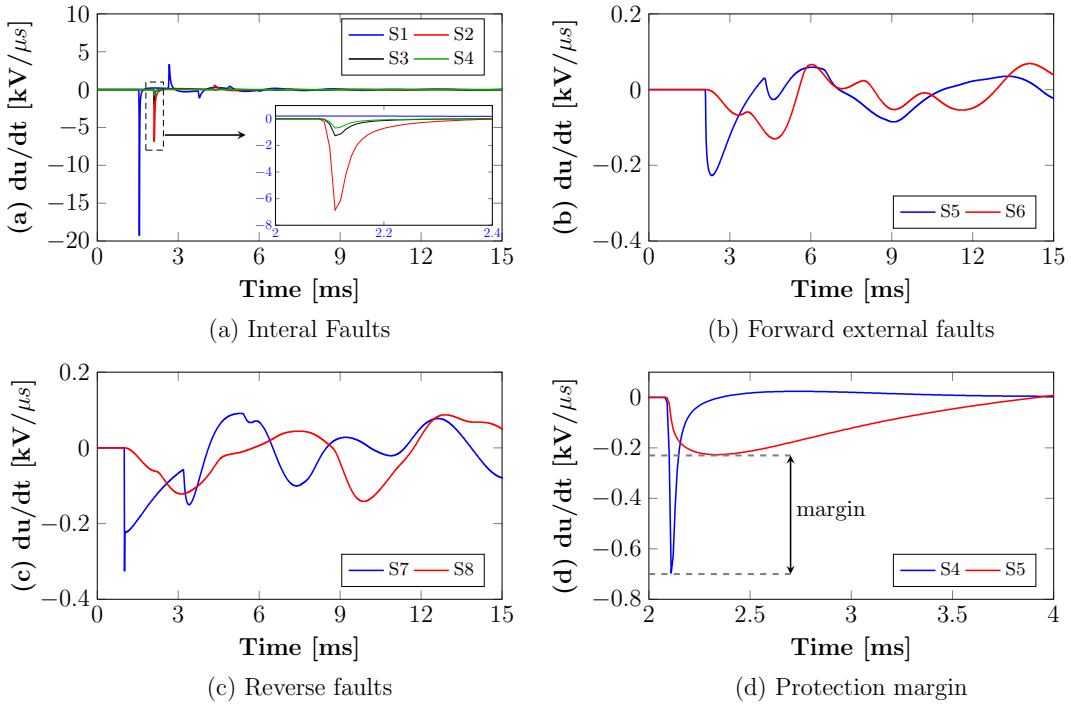


Figure 3.16: Calculated di/dt by protection relay R for: (a) forward faults (scenarios S1-S6), and (b) reverse faults (scenarios S7 and S8).

Figure 3.17 shows the output of the dv/dt non-unit protection method when it is applied at the relay measurements for all fault scenarios. Figure 3.17(a) demonstrates that for all internal fault scenarios S1-S4, dv/dt produces distinctive sharp spikes even for remote resistive faults in response to the first incident voltage wave. Although further travelling wave reflections can also be observed, they are characterised by pro-

gressively more reduced dv/dt outputs. Moreover, it is evident that fault distance, fault resistance and the type of fault influence to a great degree the results of the algorithm. The highly resistive PTG fault displays the smaller peak (negative in sign) in dv/dt output. This is expected due to the effect of fault resistance on DC voltage (as explained in the previous subsection) and the less distinctive features of PTG faults.



(a) Interal Faults (b) Forward external faults

(c) Reverse faults (d) Protection margin

Figure 3.17: Calculated dv/dt by protection relay R for: (a) internal faults, (b) forward external faults, (c) reverse external faults, and (d) scenarios S4-S5 (zoomed).

The corresponding dv/dt output for forward external faults in Figure 3.17(b) indicates a more gradual response to the external DC faults and demonstrates smaller negative spikes. Hence, by carefully setting a threshold in the region between the maximum dv/dt values for scenarios S4 and S5, discrimination between forward internal and forward external faults can be achieved. This is illustrated graphically in Figure 3.17(d), in which the dv/dt output for scenarios S4 and S5 is zoomed. The margin between the two outputs of dv/dt (or any other method) is defined in this thesis as the discrimination or protection margin. To ensure successful discriminative protection, wide protection margins are desirable. Nevertheless, it becomes evident that for the dv/dt algorithm, as in any non-unit protection algorithm, the available protection margins become significantly narrower for increasing fault resistances, fault distances or transmission medium lengths (i.e. larger protection zones). Finally, it is evident from Figures 3.17(a) and 3.17(d) that internal DC faults can be detected within a few

hundreds of μs.

For fault scenario S6 (location F4), the output of dv/dt demonstrates lower magnitude than scenario S5 (location F3) indicating that there is higher margin for discrimination. The two faults are practically at the same location with only the series inductors of L34 separating them. This implies that an increase(decrease) in series inductor size leads to enhanced(reduced) discrimination capability between internal and external faults. Consequently, the size of the inductive termination is one of the key parameters that needs to be considered in non-unit protection design stage.

Figure 3.17(c) shows that the dv/dt output for the reverse fault scenarios S7 and S8 is higher than the corresponding output for forward external faults (S5 and S6). As a result, dv/dt cannot be used on its own to form a complete protection scheme. By combining the dv/dt and di/dt detection functions as performed in [141], a complete protection scheme is formed, in which a positive di/dt indicates a forward DC fault and dv/dt is responsible for discriminating between forward internal and external faults.

Owing to its enhanced capabilities in fault signal analysis and its wide utilisation in HVDC grid protection applications (see Table 3.1), wavelet transform is selected for further evaluation. WT is implemented using the corresponding model available in PSCAD library, in which the second level and '*haar*' wavelet are selected. In a similar manner with dv/dt, the magnitude of the provided WT coefficients can form the main detection and discrimination function. In Figure 3.18 the maximum WT coefficients are displayed for all fault scenarios when WT is applied on DC voltage measurements.

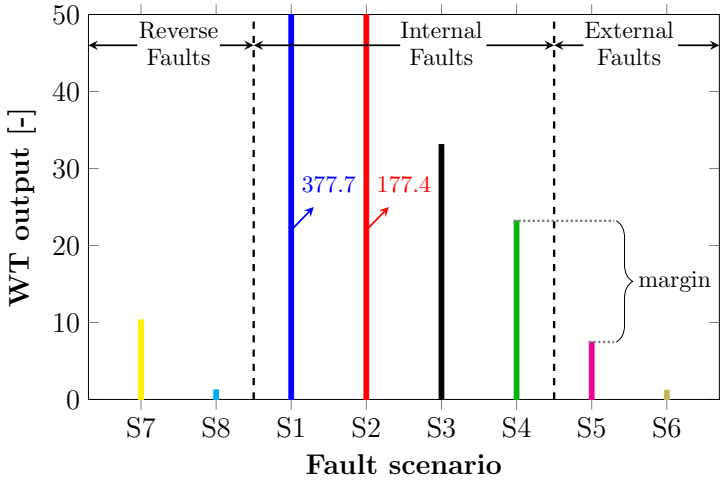


Figure 3.18: Wavelet transform output for all fault scenarios.

The results reveal that WT presents identical trends with the dv/dt algorithm. In detail, fault distance, fault resistance and type of fault adversely influence the WT output. The hardest detectable internal faults are the remote resistive faults (S3 and

S4), and the most challenging forward external fault is scenario S5, which result in a protection margin slightly higher than the one obtained with dv/dt. In this case too, an additional directional element is required to differentiate reverse DC faults.

It is worth noting that WT includes several complex configuration elements and its associated settings can play a crucial role in the method's performance in DC fault discrimination. This level of configurabillity renders WT an attractive option for HVDC non-unit protection. More details on this matter are provided in Chapter 5, where a WT-based non-unit protection scheme with optimised settings is developed for high-speed enhanced protection performance in HVDC grids.

The key takeaways from the analysis of non-unit protection conducted in this subsection are the following:

- The most significant information for non-unit protection purposes is present in the first incident voltage and current travelling waves, as subsequent wave reflections are experiencing growing attenuation.
- The fault characteristics (fault distance and resistance) diminish the amplitudes of incident current and voltage travelling waves. Therefore, distant faults or highly resistive faults are more challenging to be detected from a protection relay based exclusively on local voltage and current measurements.
- Typical over-current and under-voltage criteria are not appropriate for discriminative HVDC grid protection. Nevertheless, the drop in DC voltage even for remote resistive faults is a good indicator for initiating more advanced protection algorithms.
- When series inductors are installed, travelling waves have a more distinct impact on the shape of voltage signals as opposed to current signals. Consequently, voltage measurements are more appropriate for non-unit protection applications.
- Series inductors do not only serve as current limiters that restrain the rate of rise of the fault currents, but they also behave as natural boundary filters that dampen the sharpness of incident voltage waves. This behaviour provides a basis for discrimination between forward internal and external faults, as voltage waves originating from DC faults on other lines outside the protection zone have already passed through the faulted line's inductive termination.
- The size of current limiting series inductors is of paramount importance for the performance of non-unit protection algorithms and has a direct effect on the resulting protection margins.

- Purely voltage-based protection algorithms fail to distinguish between forward and backward DC faults. The information regarding the direction of the fault can be more readily extracted from DC current signals. In particular, di/dt can be utilised to expedite the process of determining the fault direction.
- It has been shown that both dv/dt and WT offer noticeable discrimination margins. Nevertheless, WT offers a higher degree of configurability and hence, there is greater flexibility for designing a non-unit protection algorithm.
- The inherent limitations of non-unit protection can lead to reduced protection margins depending on the length of the protected line, the inductor size and the fault characteristics. This highlights the necessity for a design methodology that ensures optimised protection settings for improved performance.

3.8 Summary

This chapter has presented the main challenges, requirements and design aspects of HVDC grid protection systems, along with a review on the existing HVDC protection and fault location solutions. Special emphasis has been paid on the implementation aspects of HVDC grid protection. The fully selective protection strategy, in which each line of the system is protected by dedicated DCCBs that work in conjunction with protection relays, is expected to be the main option for large-scale meshed grids where minimum power disruption is required. This strategy can be implemented using the decentralised approach which has been identified as a viable option for HVDC grid protection by eliminating vendor-dependence. Such an approach introduces a requirement for protection algorithms, which given the stringent time scales for DC fault clearing, are preferred to be based exclusively on local voltage and current measurements.

The review on protection revealed that there is an ongoing research activity towards the development of TW based non-unit protection methods. This trend has been supported by the insertion of series inductors in series with DCCBs that assists towards defining protection boundaries and providing the basis for discrimination between internal and external faults. It has been observed that the vast majority of the developed solutions are designed based on iterative off-line simulations using detailed models of specific HVDC test systems in EMT-type software. Nevertheless, in the absence of a common framework for the design of non-unit protection methods, their interoperability with other protection equipment is not guaranteed.

In addition, a case study was performed to identify the characteristics and challenges of non-unit protection. It has been shown that in TW-based methods, voltage signal is a better candidate for non-unit protection since TWs have a more distinct impact on

DC voltage measurements. Nevertheless, a current-based criterion (e.g. current derivative) is suggested to be included to allow for discrimination between nearby backward external and remote forward internal faults. The study revealed that the protection margins of non-unit methods are highly sensitive to fault characteristics and the size of series inductors. Moreover, highly resistive internal faults at the end of the protection zone have been recognised as the most challenging faults that need to be detected, while forward faults right outside the protection zone are the most challenging external faults. From the evaluated methods, it was shown that WT offers high potential and increased flexibility for the configuration of a non-unit protection algorithm.

The corresponding review of the existing fault location methods revealed that there is a wide range of options for locating DC faults in HVDC systems. Each of the identified method categories is accompanied with its own advantages and technical challenges. However, most of the existing methods are either designed for point-to-point HVDC links in which large measurement data sets are available due to the absence of DCCBs, or are designed for HVDC grids but have ignored the impact of high-speed DCCBs on the data window length. Furthermore, fault location in hybrid lines with both cable and OHL segments has received very limited attention.

The review also considered the sampling frequency requirements of DC protection and fault location solutions. The functions enabling protection and fault location have been mapped on a frequency diagram against the available measuring techniques to illustrate the potential for applicability based on the existing technologies. The analysis identified that voltage measurement for HVDC applications is considered readily accessible, indicating a competitive advantage of voltage-based methods. With regards to current-based methods, it has been shown that protection methods are mainly concentrated in a frequency spectrum ranging from a few kHz to 100 kHz, while fault location methods require measurements with a frequency range starting from 100 kHz and reaching up to 2 MHz. Nevertheless, a convergence between the requirements of protection and fault location is desired as it is reasonable to assume that the measuring instruments will be shared for the purposes of both applications. Such a convergence is shown to be achieved for sampling rates around 100 kHz that concentrate a significant proportion of protection and location functions.

The work and analyses presented in this chapter have contributed towards the development of HVDC protection and fault location solutions along with a methodology for non-unit protection design that will be presented in detail in the next chapters.

Chapter 4

Design of Travelling Wave based Non-unit Protection Using Frequency Domain Analysis

Owing to the fact that travelling wave propagation in HVDC grids is a heavily frequency dependent phenomenon, a methodology based on frequency domain analysis is developed as a useful means of assessing the capabilities and limitations of TW-based non-unit protection. The methodology exploits the fact that the main difference between an internal and external fault is the presence in the fault path of the current limiting series inductor that terminates each line end. The inductor acts as a high impedance element for high frequency components of transient voltage and consequently, the frequency response in each fault case is recognisably different. On this basis, a systematic analysis of both fault cases in the frequency domain can reveal significant information for protection design purposes. Towards this aim, the transient voltage at the relay location is meticulously represented in the Laplace domain by taking into account local only (in the vicinity of the relay) grid and networks components such as the transmission medium length and geometry, the number of other attached feeders to the same bus, the converter parameters, the inductive termination, the fault parameters, as well as the travelling wave behaviour of DC faults. The methodology is utilised for performing a sensitivity analysis of the above parameters in an effort to gain a deeper understanding of their impact on HVDC non-unit protection and to identify the parameters that can be adjusted to extend protection reach. Based on the findings of frequency domain analysis of DC fault transients, guidelines for non-unit protection design are proposed, including among others a generic approach for analytically calculating protection thresholds.

4.1 Introduction

The literature review of HVDC protection in Chapter 3 has highlighted that there is a growing tendency for the development of unit and non-unit protection algorithms based on travelling wave principles in which the first incident voltage and current waves are used to identify the faulted medium. Due to the significant time constraints for DC fault detection and discrimination in HVDC grids, non-unit protection becomes the preferable option in order to eliminate prolonged undesirable communication delays. Moreover, the review revealed that inductive termination of HVDC lines is exploited to define protection boundaries for non-unit protection methods. This trend has concentrated attention around the design of voltage-based methods as series inductors operate as a natural boundary for a range of frequencies of the fault initiated travelling waves, thus influencing the DC voltage traces for faults outside the protected medium as opposed to those for internal DC faults.

An important limitation of most existing non-unit protection methods is that they have been designed based on extensive offline simulations using detailed models in EMT-type software, in which only a specific HVDC system is considered and hence, their applicability in other HVDC networks is not guaranteed. Moreover, non-unit protection algorithms suffer from sensitivity issues and limited protection reach depending on the length of the lines, the DC reactor size and the fault characteristics, such as fault distance and resistance. The above underscore the necessity for a generalised methodology that offers the capability to investigate the practical limitations of non-unit protection in a flexible manner and highlight the factors which can be refined to optimise its performance for HVDC grid protection.

An appropriate tool for performing such studies is Frequency Domain Analysis (FDA), which has already been used as an analytic method for characterising the transient behaviour of DC faults in HVDC grids [238, 239]. Such analysis overcomes typical issues associated with standard EMT-type software simulations, such as the use of a single fixed network for the validation of protection systems. Nevertheless, FDA has not been used as a means of investigating the general capabilities and limitations of non-unit protection. By drawing from the work already conducted, this chapter aims to expand frequency domain analysis and develop a tool for facilitating non-unit protection design by strategically focusing the analysis on selected fault scenarios. Therefore, FDA is initially used for describing the transient voltage at the relay location in the frequency domain for the selected scenarios. Then, a methodology is presented for identifying the factors that influence the transient voltage with the aim to set up a suitable framework for the design of generalised travelling wave based non-unit protection algorithms that can be flexibly configured for any grid topology and parameters.

4.2 Frequency Domain Analysis

This chapter aims to introduce a generic tool for facilitating non-unit protection design and flexible relay configuration for any HVDC network that may be considered. Hence, to ensure general applicability of the analysis, a generic HVDC grid section is considered, as illustrated in Figure 4.1. The grid section comprises of two terminals with voltage source converters that are connected through a DC line or cable, while further n and m feeders are connected to terminal buses B1 and B2, respectively. The feeder is terminated by current limiting series inductors at both ends. The protection zone of relay R is the full length of the DC feeder between the two inductors. Based on local measurements, the protective relay should discriminate between a fault at location F_{int} at the remote end of the protected cable (internal fault) from a fault behind the series inductor at location F_{ext} that is right outside the protection zone (external fault).

As demonstrated in the case study of Chapter 3 (see Section 3.7), a solid fault at fault location F_{ext} presents the most challenging problem for discriminating as an external, since the strongest external fault transient (in the forward direction) occurs when the fault happens right outside the protection zone. Furthermore, an internal fault at the far end of the protection zone at location F_{int} with high fault resistance presents the most challenging fault case for discriminating as an internal fault, as it imposes less distinct fault signatures than faults at any other point closer to the relay location. The main difference between the two fault locations is the presence of the series inductor, which dampens the sharpness of incident voltage waves that originate from faults at F_{ext} (or beyond). The inductor acts as a high impedance element for high frequency components and consequently, the transient voltage characteristic at the relay location in each fault case is recognisably different. On this basis, focused investigation of the voltage frequency response for these two fault cases can provide significant information for differentiating between them and for protection design purposes.

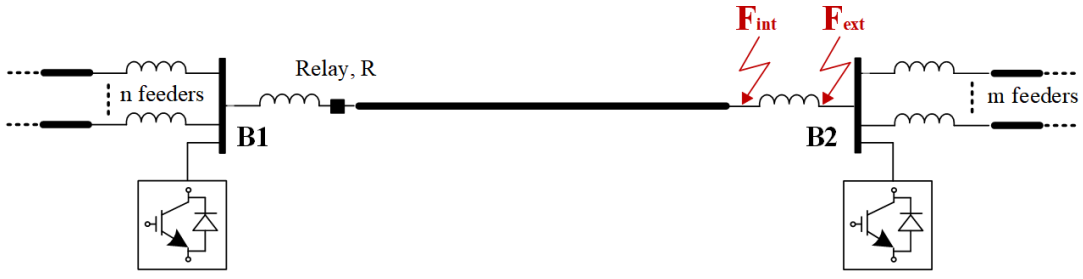


Figure 4.1: General section of a HVDC grid.

Owing to the fact that the transient phase of DC faults in HVDC grids is governed by travelling wave phenomena, which are to a great degree frequency dependent, frequency

domain analysis can be employed to analyse the frequency response of faults at F_{int} and F_{ext}. Towards this aim, common HVDC grid components should be described in the frequency domain, while the travelling wave principles have to be taken into account. In the proposed approach, the Laplace domain is used to derive the transfer functions of the transient voltage (early DC fault stage) at the relay location with respect to the fault point accounting both for internal and external faults.

4.2.1 Cable Modelling

Travelling waves that propagate over a cable or overhead line experience attenuation due to the line parameters. As explained in Chapter 2, the resistive and inductive components of a transmission line medium are heavily frequency dependent and hence, frequency dependent models are required to adequately simulate the response of the medium under fault conditions. These models operate on the basic principle that the frequency dependence of the medium can be sufficiently described by two matrix transfer functions: i) the propagation function H and ii) the characteristic admittance Y_c. These functions can be approximated using the approach described in Subsection 2.6.3. Accordingly, the common form of function H is:

$$H(s) = \sum_{m=1}^{q_m} \left(e^{-s\tau_m} \sum_{n=1}^{N} \frac{C_n}{s - P_n} \right) \tag{4.1}$$

where N is the order of the rational function, C_n are the residues, P_n are the poles, q_m is the number of group delays, and τ_m is the modal time delay of group m. Equation (4.1) serves as an approximation which is appropriate for use in the frequency domain model. The required inputs of the model are limited to a set of values of cable series impedance Z_s and cable shunt admittance (Y_s) at various frequency points. The characteristic cable impedance (Z_c) is also calculated based on these parameters by:

$$Z_c = \sqrt{\frac{Z_s}{Y_s}} \tag{4.2}$$

4.2.2 Converter Modelling

The main converter technology considered in this thesis is the MMC. The fault contribution in the initial DC fault stage of most MMC topologies, including the most widely used HB-MMC, is governed by the discharge of the distributed capacitance contained in the SMs of the converter. Since the analysis focuses exclusively on the transient phase of DC faults, before converter blocking occurs, only the capacitive discharge stage should be considered. During this stage, the converter impedance can be approximated as a series RLC model, and its frequency domain representation is given by [141]:

$$Z_{conv} = R_{eq} + sL_{eq} + 1/sC_{eq} \tag{4.3}$$

where R_{eq}, L_{eq} and C_{eq} are the converter's equivalent resistance, inductance and capacitance respectively. C_{eq} represents the total capacitance of the inserted sub-modules on all three legs of the converter. R_{eq}, L_{eq} and C_{eq} can be derived based on the corresponding arm converter parameters R_{arm}, L_{arm} and C_{arm} as:

$$R_{eq} = \frac{2}{3}R_{arm}, \quad L_{eq} = \frac{2}{3}L_{arm}, \quad C_{eq} = 3C_{arm} \tag{4.4}$$

More details on how equation (4.3) is derived are provided in Appendix A, which also describes the way different topologies can be represented in the frequency domain.

4.2.3 Transient Voltage Characteristic

To represent the voltage at the relaying point, the first incident travelling voltage wave generated at the fault location needs to be formulated in the phase domain. Using the generic section of Figure 4.1, the transient voltage measured by relay R is:

$$U_r = \mu_{\beta 1} \cdot H \cdot U'_f \tag{4.5}$$

where $\mu_{\beta 1}$ is the transmission coefficient at bus B1 and U'_f is the voltage wave at the fault point, and H which is derived from (4.1) represents the attenuation experienced by the fault voltage wave after propagating from the fault point. The refraction coefficient describes the fraction of the fault voltage wave that passes through the inductor at bus B1 and is transmitted to the network behind the series inductor. Using travelling wave theory, the refraction coefficient is calculated as follows [240]:

$$\mu_{\beta 1} = \frac{2Z_t}{Z_t + Z_c} \tag{4.6}$$

where Z_t is the terminal impedance behind the relay R (see Figure 4.1) that is calculated as in (4.7) when all transmission media have the same impedance Z_c, and series termination inductance L. Similarly, this can be generalised for any L and Zc values.

$$Z_t = Z_{conv} // \frac{(sL + Z_c)}{n} + sL \tag{4.7}$$

When a DC fault occurs between two poles of the feeder, the voltage at the fault location falls from the pre-fault nominal voltage U_{dc} to zero. The superposition theorem can be applied to derive the voltage wave at the fault location. According to the theorem, the fault network, which includes a DC voltage source at the fault location with a value equal to the pre-fault voltage with reverse polarity (U'_f=-U_{dc}), is superim-

posed to the pre-fault network. Figure 4.2 displays the equivalent fault-superimposed circuit for an internal PTP fault at location F_{int} and an external PTP fault at F_{ext}.

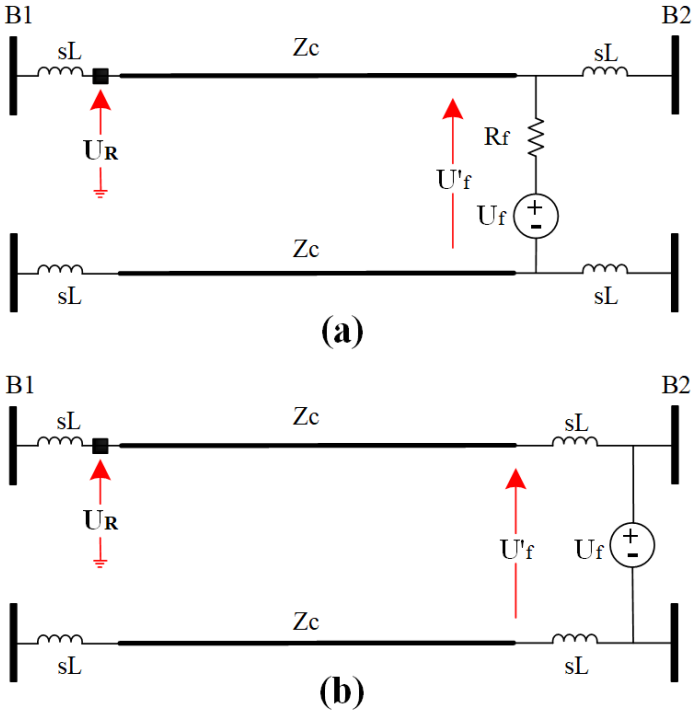


Figure 4.2: Equivalent fault-superposed circuit for: (a) a resistive internal PTP fault and (b) a solid external PTP fault.

Based on Figure 4.2(a), the fault voltage wave in the case of an internal fault is:

$$U'_{f,int} = \frac{Z_c//sL}{(R_f + 2Z_c//sL)} U_f \tag{4.8}$$

Using the superposition theorem in a similar manner for a solid fault at location F_{ext} (Figure 4.2(b)), the voltage at the fault point is given by:

$$U'_{f,ext} = \frac{Z_c}{2Z_c + 2sL} U_f \tag{4.9}$$

By substituting (4.8) and (4.9) to (4.5), the transfer function of the ratio of voltages at the relay location and the voltage at the fault point (i.e. U_r/U_f) can be derived for both fault locations F_{int} and F_{ext}, respectively, as shown by:

$$\frac{U_{r,int}}{U_f} = \mu_{B1} \cdot H \cdot \frac{Z_c//sL}{(R_f + 2Z_c//sL)} \tag{4.10}$$

$$\frac{U_{r,ext}}{U_f} = \mu_{B1} \cdot H \cdot \frac{Z_c}{2Z_c + 2sL} \tag{4.11}$$

The presented analysis focuses on PTP faults for considering the impact of worst-case external faults. Nevertheless, the approach described above for deriving the voltage transfer functions can be extended to PTG faults. It is worth noting that the analysis is only valid during the transient phase of DC faults, in which the frequency response is mainly determined by the first incident voltage wave.

Mutual Coupling Effect

Mutual coupling between the HVDC grid system poles is a phenomenon that should be taken into consideration when designing HVDC protection. It has been demonstrated in [239,241] that the mutual coupling in cable-based systems is negligible (even for bipolar configurations), especially in the first few milliseconds after fault inception. Nevertheless, the electromagnetic coupling between poles of OHL-based systems is stronger due to capacitive coupling between the conductors, as opposed to the negligible capacitive coupling between cables which are grounded at both ends [177]. Therefore, transients occurring on the faulted pole affect the healthy pole and consequently, the performance of the protection scheme.

To eliminate the mutual coupling effect between the system poles and ensure extensibility of the analysis to bipolar configurations, the phase-mode transformation is utilised, according to which the decoupled ground-mode voltage U_{r_0}, and line-mode voltage U_{r_1} are given by [241]:

$$\begin{bmatrix} U_{r_0} \\ U_{r_1} \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} U_{r+} \\ U_{r-} \end{bmatrix} \tag{4.12}$$

where U_{r+} and U_{r-} are the positive-pole and negative-pole DC voltages at the relay location. Using the superposition theorem in a similar manner, and by applying the phase-mode transformation, the transient line-mode voltages at the fault point for the cases of the internal and external fault can be obtained [242]:

$$U'_{f,int_1} = \frac{2\sqrt{2}Z_{c_1}}{2Z_{c_1} + R_f} U_f \tag{4.13}$$

$$U'_{f,ext_1} = \frac{\sqrt{2}Z_{c_1}}{Z_{c_1} + sL} U_f \tag{4.14}$$

where R_f is the fault resistance, and Z_{c_1} is the line-mode component of Z_c. By substituting (4.13) and (4.14) to (4.5), the voltage transfer function (U_{r_1}/U_f) for faults at $\mathrm{F_{int}}$ and $\mathrm{F_{ext}}$ is expressed as:

$$\frac{U_{r_1,int}}{U_f} = \mu_{B1} \cdot H \cdot \frac{2\sqrt{2}Z_{c_1}}{2Z_{c_1} + R_f} \tag{4.15}$$

$$\frac{U_{r_1,ext}}{U_f} = \mu_{B1} \cdot H \cdot \frac{\sqrt{2}Z_{c_1}}{Z_{c_1} + SL} \tag{4.16}$$

4.2.4 Validation of Frequency Domain Analysis

PSCAD detailed simulations for a HVDC grid section are compared against the results provided by the theoretical frequency domain analysis to prove the validity of the calculated transient voltage in each fault case. The cable parameters are adapted from [81], the cable length is set to 200 km, while n is set to 2. Series inductors with a value of 50 mH are placed at each cable end, while R_{eq}=0.0533 Ω, L_{eq}=0.28 mH and C_{eq}=94.26 μF. The faults occur at t=0 ms.

A step input with magnitude equal to the pre-fault pole-to-pole voltage is applied at the fault point (U_f=–U_{dc}) and then inverse Laplace transform is used on (4.10) and (4.11) to obtain a time-domain representation of the transient phase of DC faults. The results of the comparison for solid faults at both F_{int} and F_{ext} are shown in Figure 4.3. It is evident that the time-domain representations obtained based on FDA are in agreement with the detailed PSCAD simulations for the first travelling wave reflection (between 1 to 3.3 ms). During this period, the maximum difference in percentage between the two representations (using 320 kV as reference value) is 0.18% for the internal fault and 0.62% for the external fault case, thus confirming the suitability of the technique as a means of analysing DC faults in HVDC grids.

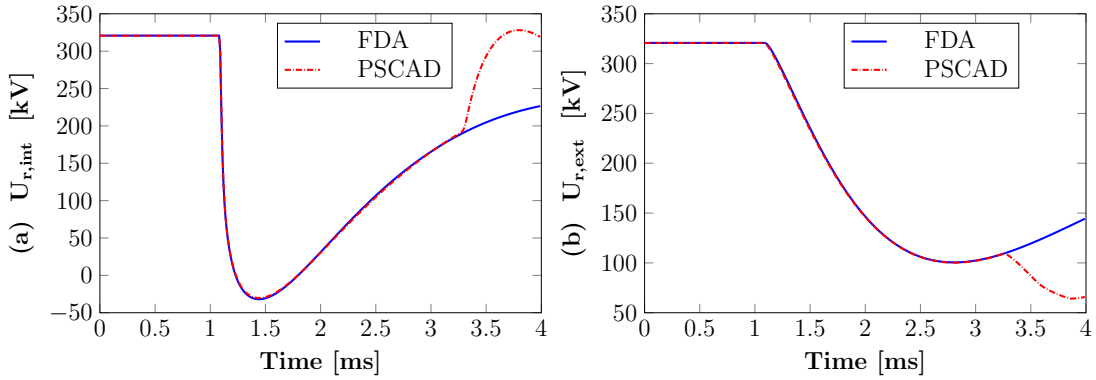


Figure 4.3: Validation of frequency domain model against PSCAD for (a) an internal solid fault, and (b) an external solid fault.

In both cases, the fault response deviates from PSCAD simulations approximately 3.3 ms after fault inception (almost 1 ms accounts for wave propagation over the 200 km cable). This is attributed to the fact that the analysis does not take into account subsequent travelling waves or other actions such as converter blocking, or breaker tripping events. Nevertheless, considering that the required speed of DC fault detection

and discrimination in HVDC grids should be in the range of a few hundreds of microseconds, it can be concluded that the information provided by frequency domain analysis is more than sufficient for designing high-speed non-unit protection algorithms.

The model is based on the assumption that the transmission line is long enough and that wave reflections from the remote terminal do not reach the relaying point within the time frame of interest. The exact period for which FDA is valid becomes smaller for shorter transmission lines as the fault location moves closer to the relay and consequently, denser travelling wave reflections occur. When aiming for DC fault detection and discrimination time of 0.5 ms, the model is adequate for over-head lines (or cables) with a minimum length of 75 km (or 32.5 km) provided that the wave propagation speed is equal to the speed of light (or half the speed of light). For the design of faster non-unit methods, FDA can be extended to even shorter mediums.

4.2.5 Methodology for Analysis of Non-unit Protection

Design and analysis of non-unit protection can be facilitated by identifying the frequency content of the transient voltage signature resulting from strategic DC fault cases. In particular, the comparison between the frequency response of the hardest detectable internal fault (a highly resistive fault at the end of the line, i.e. F_{int}) and the hardest external fault (a solid fault right outside the protection zone, i.e. F_{ext}) can shed light on the distinguishing factors between the two cases which can be exploited for non-unit protection design. Assuming lossless propagation over the DC cable of the previous subsection, Figure 4.4 presents the frequency response of the voltage transfer function under i) an internal solid fault (R_f=0 Ω), ii) a highly resistive internal fault (Rf=100 Ω) and iii) a solid external fault, when 50 mH inductive termination and a constant characteristic impedance of 28 Ω are considered.

It is evident that the fault voltage travelling wave generated after a solid DC fault at location F_{int} contains higher frequency components than the corresponding fault voltage for an external fault, in which high frequency components are filtered by the inductive termination of the medium. This is the main principle behind existing voltage-based non-unit protection methods, which has been used for discrimination between internal and external faults by exploiting the greater magnitude of high frequency components of transient voltage. Nevertheless, the relative difference in magnitude between the two frequency responses, and hence the ease with which external faults can be differentiated from internal faults, greatly depends on the various system and fault parameters.

For instance, Figure 4.4 shows that in the event of a resistive internal fault the magnitude of the voltage characteristic is decreased, leading to a low frequency region in which the frequency response for the external fault is more pronounced, while in the

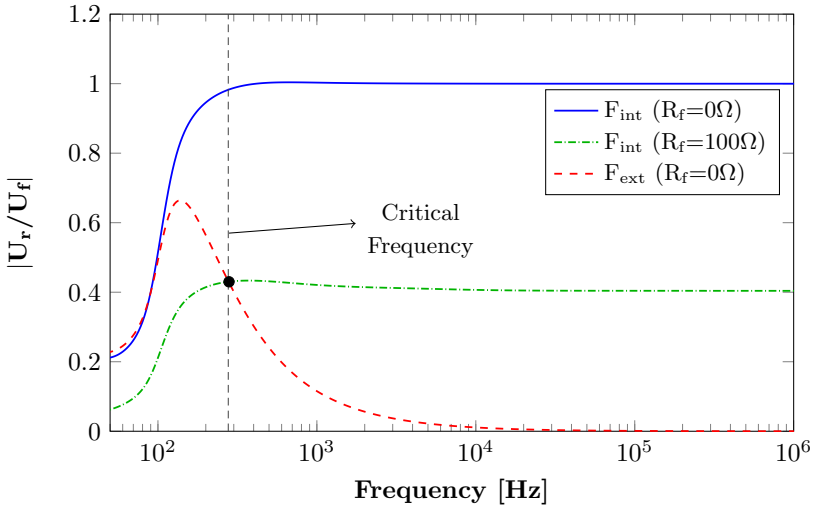


Figure 4.4: Transient voltage frequency responses of internal and external faults assuming undistorted (i.e. H=1) fault voltage travelling waves.

high frequencies the corresponding magnitude for the internal fault characteristic is higher. This implies that discrimination of resistive internal faults becomes harder and is only possible in a certain frequency spectrum. The frequency point at which the two characteristics intersect each other, and beyond which the signature of the resistive fault becomes more distinct than that of the external fault, is termed as critical frequency. The critical frequency varies depending on the examined internal fault. This frequency can serve as an indicator for selecting an appropriate sampling rate that ensures that the more valuable high frequency components of DC voltage are sufficiently captured in order to ensure that even highly resistive faults are discriminated.

Similarly, changes in other parameters may influence in different ways the frequency responses and the resulting critical frequencies. Therefore, by systematically analysing the frequency response of the voltage transfer functions for all potential grid and fault parameters, their influence can be evaluated, ultimately unlocking insights for the design of robust voltage-based non-unit protection methods. This is investigated in detail in the following section.

4.3 Impact of System and Fault Parameters on Transient Voltage Frequency Response

Based on the aforementioned mathematical formulation for the first incident voltage travelling wave, the frequency response of voltage transfer functions for faults at locations F_{int} and F_{ext} is analysed with the aim to offer valuable insight into the technical limitations of non-unit protection and an in-depth understanding of the influencing fac-

tors. The considered parameters are the fault resistance of the internal fault, the feeder length, the series inductor size, the converter arm inductance and total capacitance as well as the number of healthy feeders attached to the same bus with the faulted feeder. Both cable systems and OHL systems are considered in the analysis and the corresponding line parameters are adopted from [81] (same as in previous section) and [243], respectively. The generic HVDC grid section of Figure 4.1 is used with the parameters shown in Table 4.1, which unless otherwise specified, are used in all studies.

Table 4.1: System and fault parameters.

Parameter	Value
Medium length	200 km
No. of feeders connected at B1	2
DC inductor size	50 mH
Arm resistance	0.08 Ω
Arm inductance	42 mH
Arm capacitance	31.42 μF
Fault resistance	0 Ω

4.3.1 Fault Resistance

Figure 4.5 shows the frequency response of the voltage transfer function for internal DC faults for various fault resistances, when the faulted medium is a DC cable in Figure 4.5(a) and an overhead line in 4.5(b). A direct consequence of fault resistance is the damping of magnitude across the whole bandwidth of the transient voltage. Moreover, with increasing fault resistance, the reduction in magnitude becomes more prominent and the critical point is shifted towards a higher frequency, thus transferring the suitable frequency spectrum that contains valuable information for DC fault discrimination to higher frequencies. Based on these findings, the use of a higher sampling frequency allows for the detection of DC faults with higher fault resistances.

Figure 4.5(a) also shows the corresponding frequency response for a solid external fault (R_f=0 Ω). Since wave propagation along the cable is identical for both solid faults at F_{int} and F_{ext} (same distance to fault), the difference in voltage response is caused entirely by the filtering effect of the inductor. It is evident, that in the case of an external solid fault, the transient voltage attenuates faster in the high frequency region (above 200 Hz in this case) than that of a solid internal fault, in which there is a significant high frequency content. Nevertheless, for faults with very high fault resistance, the magnitude in the high frequency region becomes comparable to that of the external fault, thus making internal faults harder to be distinguished. For instance, the voltage characteristic for the 500 Ω internal fault is greater than the characteristic

of the external fault only in the frequency range from almost 1 kHz (critical frequency) up to 50 kHz where it decays to zero. It can be seen that the critical frequency reduces for increasing fault resistance and hence, it becomes evident for given feeder length and characteristics, there is a limit in the maximal fault resistance that can be detected regardless of the employed non-unit protection method.

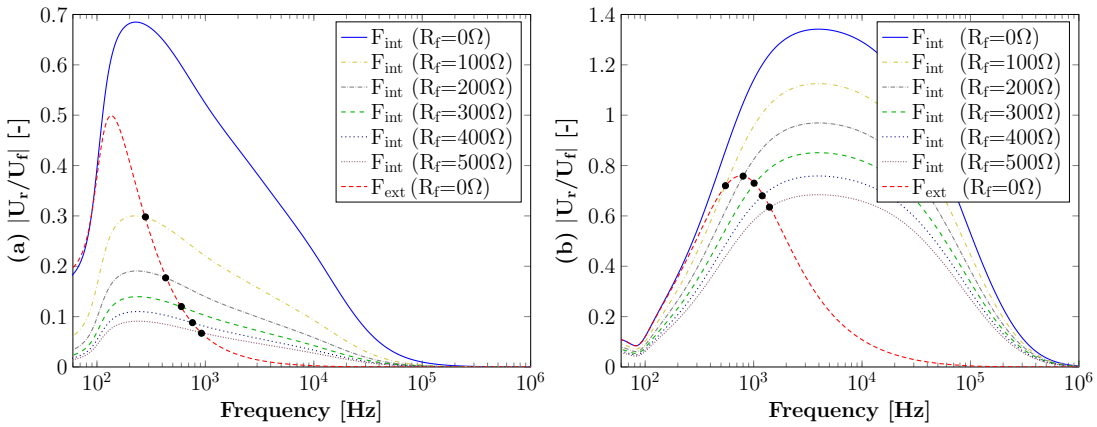


Figure 4.5: Transient voltage frequency response in the case of a solid external fault and for various fault resistances of the internal fault for (a) DC cable and (b) overhead line. The black marks indicate the critical frequency for each internal fault.

Compared to the frequency response of the undistorted fault voltage travelling wave of Figure 4.4, the shape of the transient voltage characteristic under an external fault is not significantly influenced by the attenuation caused by the cable, while the decay rate of magnitude is only marginally expedited. This indicates that for faults behind the series inductor, the impact of filtering effect of inductive termination is greater than the impact of cable attenuation.

Similar trends are observed for the OHL in Figure 4.5(b), nevertheless, it is evident that the critical frequencies for the internal faults are higher than their cable counterparts, while also the attenuation caused by the OHL parameters on the frequency response of transient voltage for highly-resistive faults is significantly smaller. These features imply that higher sampling frequencies are required to capture travelling wave phenomena in OHLs, and that the discrimination capabilities (protection margins) of any non-unit protection method are enhanced when it is used for protection of OHLs.

4.3.2 Medium Length

Figure 4.6 displays the frequency response of solid internal faults (R_f=0 Ω) at the end of the protection zone and solid external faults just outside the protection zone for different cable lengths in 4.6(a), and OHL lengths in 4.6(b). For both fault cases, greater medium length effectively means greater fault distance. It is evident from Figure 4.6(a)

that as the cable length increases, the magnitude of all transfer functions for internal faults becomes smaller, while further high frequency components are filtered out due to the low-pass characteristic of the propagation function which becomes more dominant for greater distances. This indicates that the greater the medium length, the lower the reach of the protection due to the greater attenuation caused on the waves originating from remote-end faults. To a lesser extent this is also true for the magnitude of the transfer functions for the external faults. The combined effect is that the available bandwidth for HVDC protection decreases and encompasses more lower frequencies.

Moreover, with increasing medium length, the difference between an internal and external fault becomes less distinct and consequently, there is a theoretical maximum length limit, after which the protection method will not be able to differentiate between them. Once again, similar trends are observed to a lesser extent for the OHL in Figure 4.6(b), which implies that the theoretical maximum length limit for non-unit protection is higher. It is worth noting that in both cases, the effect of medium length on critical frequency is minimal and hence, sampling frequency selection can be assumed independent of the length of the protected medium.

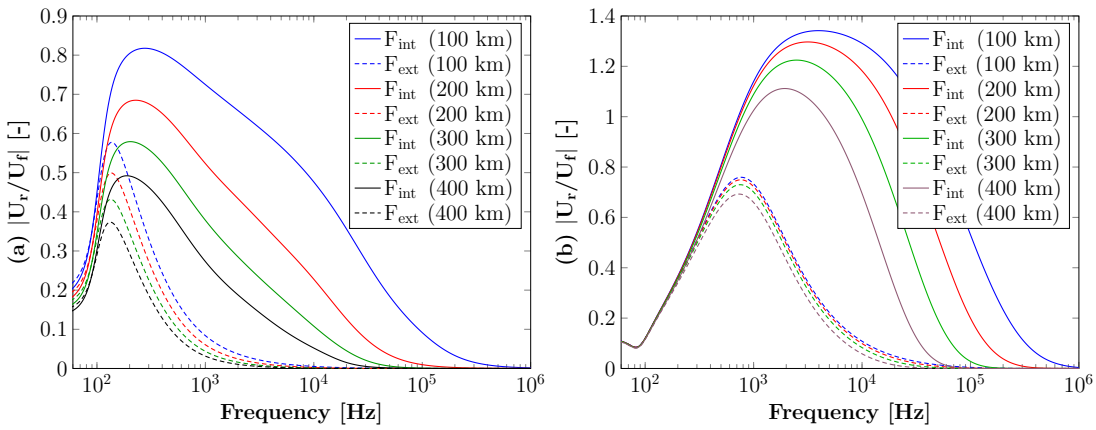


Figure 4.6: Impact of medium length on the frequency response of DC voltage for internal and external faults for (a) DC cable and (b) overhead line.

4.3.3 Series Inductor Size

Figure 4.7 demonstrates the impact of the size of series inductors on the transfer function response for both the internal and the external fault. It is evident that the inductor influences to a great extent the frequency response of both transfer functions. For the internal faults, the high frequency region (above 1 kHz) remains unaffected, since it is primarily determined by the medium characteristics. Nevertheless, the bandwidth is extended significantly in the low frequency region (below 1 kHz), while also the

magnitudes of the voltage characteristics are increased to a certain extent.

For the external faults of both Figures 4.7(a) and 4.7(b), the high frequency components of the incident travelling wave are largely attenuated due to the greater filtering effect that is introduced by the higher size of the inductor. As a result, the magnitude of the transfer function decays faster in the high frequency region. This phenomenon becomes less distinct as the inductor size increases. In addition, a reduction in the magnitude is caused across the whole bandwidth.

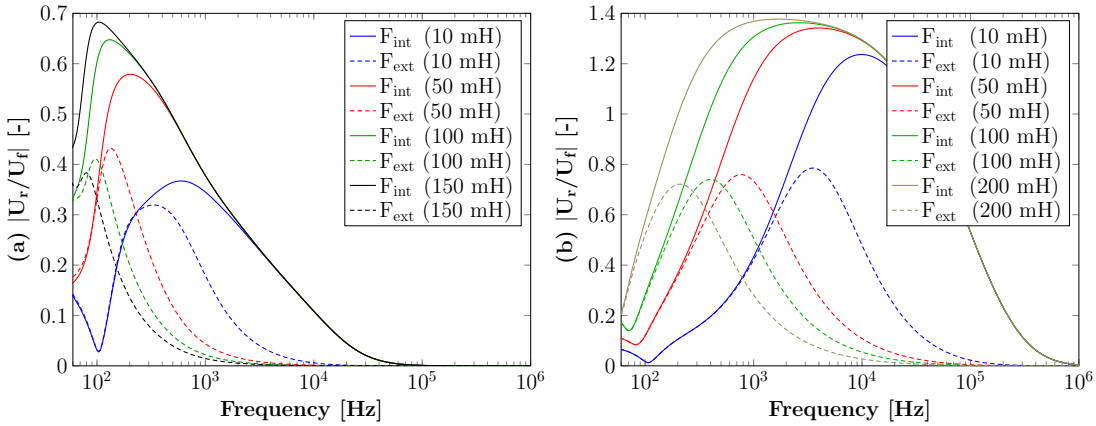


Figure 4.7: Impact of inductor size on the frequency response of DC voltage for internal and external faults for (a) DC cable and (b) overhead line.

These observations demonstrate the strength of using series reactors for non-unit protection. The benefit obtained from the use of a larger series inductor is that the magnitude of the transfer function for an internal fault is significantly higher when compared to the lower magnitude of the external fault, leading to larger margins and longer time windows for the protection method to effectively discriminate the faulted feeder. Considering the previous findings on the impact of the medium length, in the case of very long feeders, larger inductors can be employed if possible to compensate for the increased attenuation of the incident fault waves. In this way, the protection reach can be extended to ensure that the whole protection zone is covered even for faults with high fault resistance. Lastly, due to the more pronounced impact of the series inductor in the low frequency region, lower sampling frequencies may be used.

4.3.4 Arm Inductance and Capacitance

Figures 4.8 and 4.9 show the frequency response of transient voltage for different arm inductances and arm capacitances, respectively. The values of these parameters are selected based on typical inductors and cell capacitors used in HVDC grid studies. Both parameters mostly affect the lowest frequencies of the transfer functions, while

the responses in the high frequency region are identical. Since the time range considered for HVDC grid protection is in the order of a few milliseconds or less, and based on the previous results which revealed that higher frequency components (in the range of kHz) are of interest for the protection systems, the influence of the converter parameters on non-unit protection design can be neglected. This suggests that individual vendor converter designs have limited impact on HVDC protection design. This conclusion holds true for both cable- and OHL-based systems.

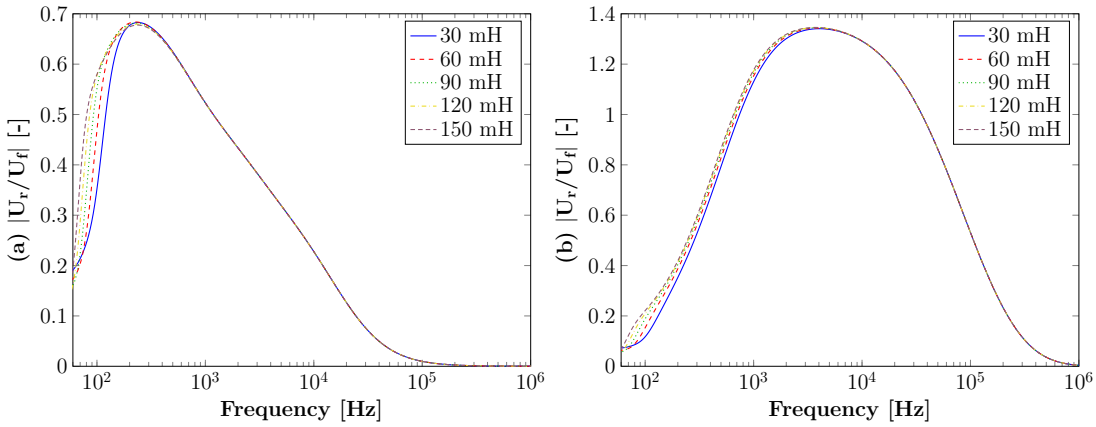


Figure 4.8: Impact of arm inductance on DC voltage frequency response (internal fault) for a (a) DC cable and (b) overhead line.

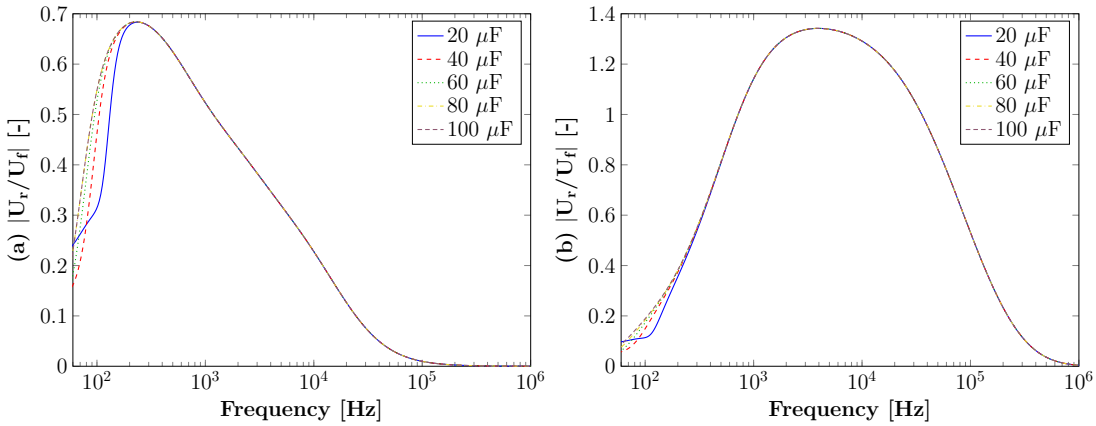


Figure 4.9: Impact of arm capacitance on DC voltage frequency response (internal fault) for a (a) DC cable and (b) overhead line.

4.3.5 Number of Feeders

The number of non-faulted feeders connected to bus B1 is varied from 1 to 4 and the resulting transfer functions are shown in Figure 4.10, when considering identical characteristic impedance for all cables in Figure 4.10(a) and for all OHLs in Figure

4.10(b). In both cases, it is evident that the influence of the number of feeders on the fault response is limited only to the low frequencies' region. Similar to the previous examined case, its impact on non-unit HVDC protection systems can be neglected without significantly affecting the results of the analysis.

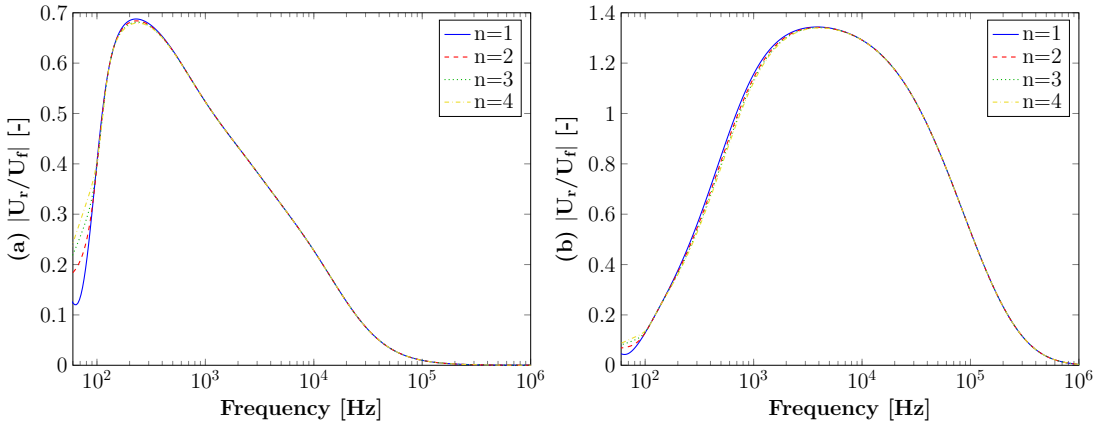


Figure 4.10: Impact of number of healthy feeders on DC voltage frequency response (internal fault) for a (a) DC cable and (b) overhead line.

4.4 Guidelines for Non-unit Protection Design

The sensitivity analysis of the previous section has revealed significant aspects of non-unit protection and the impact of different grid parameters on any non-unit algorithm that may be selected. In line with Figure 3.5 of Chapter 3 on HVDC protection design, the grid parameters such as transmission line length and characteristics, converter parameters, and system configuration are selected in the system design process. In addition, the current limiting series inductor is typically selected in the DCCB design process. Therefore as all system parameters are known in advance for a given project, frequency domain analysis of the transient voltage for faults right before and after the series inductor (protection zone limit) can be readily used to facilitate design and configuration of robust non-unit protection methods. The following paragraphs present guidelines on several aspects of non-unit protection and its underlying DC fault detection and discrimination functions.

4.4.1 Sampling Frequency and Filtering Requirements

The critical frequency (see Figure 4.4) can be used as an indicator for determining the lowest sampling frequency for which a non-unit protection method can detect and discriminate DC faults. Moreover, based on the maximum required detectable fault

resistance R_f^{max}, the sampling frequency can be obtained by comparing the transfer function for the internal DC fault (with $R_f = R_f^{max}$) with that of the solid external DC fault and ensuring sufficient margin between the two functions. To enhance security of non-unit protection, the low frequency components can be eliminated by utilising filters to manipulate the frequency spectrum of the voltage signature or by selecting signal processing techniques with inherent filtering capabilities (e.g. wavelet transform or short-time Fourier transform). It is worth noting that the results of the sensitivity analysis of Section 4.3 indicate that the 96 kHz sampling frequency suggested in IEC 61869-9 provides significant margins between highly-resistive internal faults and solid external faults for both cable-based and OHL-based systems (see Figures 4.5 and 4.6).

4.4.2 Protection Threshold Determination

Non-unit protection methods do not offer inherent selectivity and they require an optimised protection setting to ensure that the maximum protection reach is achieved and the method remains robust against external faults or other disturbances. Frequency domain analysis can be used for developing a generalised approach for directly calculating the protection threshold in a flexible manner, while avoiding extensive electromagnetic transient simulations. This approach is based on the identification of the most severe fault that may lead to maloperation of the protection relay.

As already explained, a solid fault after the series inductor is the hardest fault that should be disregarded by the relay. The application of a step input with a magnitude equal to the pre-fault pole-to-pole voltage (U_f=$-U_{DC}$) at the fault point and use of the inverse Laplace transform (ILT) yields the time-domain representation of the transient phase of PTP DC faults (as performed in Subsection 4.2.4). Based on this approach, the step response of the transfer function for the solid external fault at F_{ext} (see Figure 4.1) yields the fault response for the hardest fault. By performing the selected non-unit protection method directly on the derived time-domain expression, the corresponding protection setting can be analytically calculated. This procedure is visualised in Figure 5.6, in which voltage derivative is applied on the derived time-domain representation of the external fault based on FDA for the same grid section and parameters of Subsection 4.2.4, when a sampling frequency of 100 kHz is used.

Based on Figure 4.11(b), the protection threshold is set equal to the minimum (negative voltage derivative) value of dv/dt. It is worth reiterating that only local parameters of the components in the vicinity of the relay are required for threshold determination. The same procedure should be applied for the hardest detectable fault for each relay (based on its associated local parameters) within the HVDC grid. The protection setting may be set equal to the highest calculated threshold of all protective

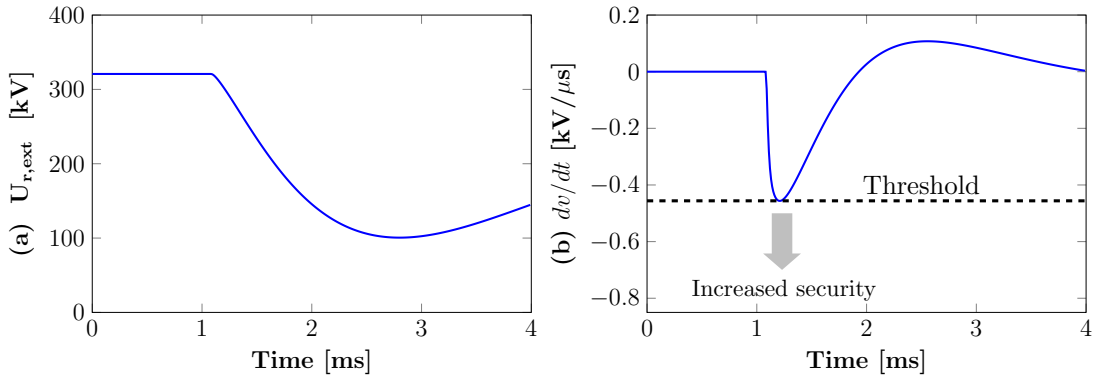


Figure 4.11: Protection threshold determination: (a) time-domain expression obtained using FDA and ILT, and (b) application of non-unit protection algorithm (dv/dt) to determine protection threshold.

relays. Alternatively, an optimised setting can be applied for each relay separately with the optional capability for dynamically changing its value whenever there is a change in the influencing factors (e.g. disconnection of a converter or an adjacent line). Moreover, a safety margin (e.g. plus 10-20%) shall be included to achieve a trade-off between sensitivity and security (as illustrated in Figure 4.11(b)). In this way a degree of immunity against noise, measurement errors and other disturbances is also provided.

4.4.3 Protection Margin Improvement

Analysis of DC faults in the frequency domain can also be used for adjusting parameters (if possible) with the aim to optimise the method's performance in terms of protection reach and margin. Nevertheless, as most of the grid parameters are determined in the project design stage and are therefore fixed, there is very limited flexibility with regards to the grid components that may be modified. The sensitivity analysis of Section 4.3 revealed that the current limiting series inductor, which is determined in the DCCB design process, is the most influencing factor for non-unit protection. Therefore, FDA can be used as a complementary tool in combination with current DCCB sizing practices for selecting the appropriate inductor size.

An example is shown in Figure 4.12, in which dv/dt is used as the non-unit protection method and applied for internal faults at location F_{int} (see Figure 4.1) for fault resistances in the range of 0-500 Ω. Moreover, dv/dt is applied for a solid external fault for two series inductor sizes, i.e. L_{dc1}=20 mH and L_{dc2}=50 mH. It is observed that a small increase of series inductor size leads to an increase of maximum detectable fault resistance, R_f^{max}, from 288 Ω for 20 mH inductor to 485 Ω for 50 mH inductor, thereby improving the overall protection margin of the method. Such analysis can be used to derive the appropriate series inductor size that satisfies the desirable method's

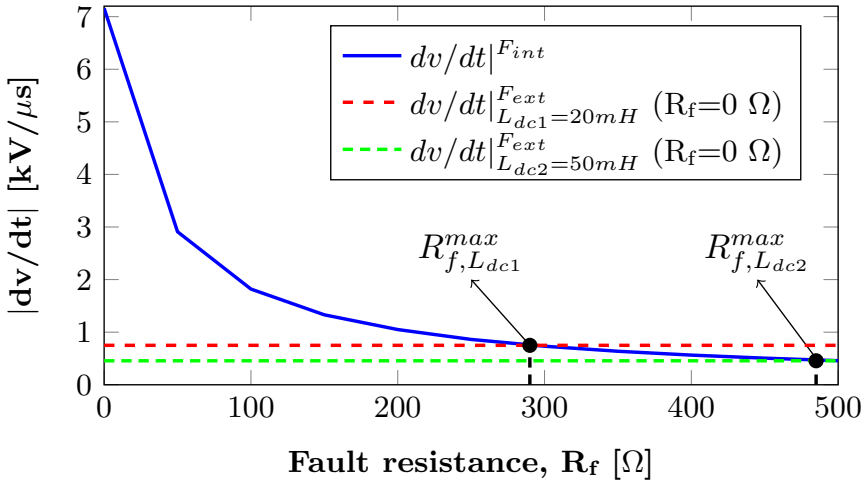


Figure 4.12: Increase of protection margin.

performance in terms of discrimination margin. Based on the observations made in Subsections 4.3.2 and 4.3.3, the benefit of this process is expected to be more pronounced for long transmission lines as an increase of the series inductor size can overcome the attenuation effect caused by a long line on the DC fault signatures of internal faults, thereby leading to extended protection reach.

4.4.4 Configuration of Non-unit Protection Algorithms

The literature review on existing DC fault detection and discrimination functions in Chapter 3 has demonstrated that a plethora of advanced signal processing techniques have been employed for non-unit protection. Such complicated algorithms typically entail the determination of several algorithm-specific configuration parameters. In current literature, these parameters are optimised through trial and error offline simulations until the suitable settings for all fault scenarios are identified. The application of FDA on strategic fault scenarios to obtain the corresponding time-domain representations can assist towards developing quantitative metrics that enable flexible configuration of the algorithm settings. The developed protection solution of Chapter 5 is a perfect example of this process, in which an analytical methodology for deriving the key parameters of the wavelet transform is presented. In this case, FDA in conjunction with ILT are used to derive the time domain expressions for an internal fault with R_f=500 Ω and for a solid external fault. A wavelet transform with different settings is then repeatedly applied on the obtained time domain expressions, and the settings that lead to enhanced performance in terms of protection margin are flexibly selected.

FDA can also be used directly as the main element of a non-unit protection algorithm. Towards this aim, single-ended sampled voltage measurements from the relay

location can be utilised to construct a frequency domain voltage characteristic for the existing fault case using continuous time transfer function identification tools. The voltage characteristic can then be compared against stored theoretical frequency domain voltage profiles of internal and external faults, which can be obtained using FDA, to determine whether the fault is internal or external. If this process is executed successfully at high speed, it can be used as a means of non-unit protection. Alternatively, this technique can be used for offline fault location applications, in which the constructed frequency domain voltage profile is repeatedly compared against theoretical profiles for various fault distances along the medium until a convergence is achieved. This forms the main principle behind the HVDC fault location method presented in Chapter 7.

4.4.5 Adaptability and Extensibility of Non-unit Protection

Due to the general applicability of the proposed framework for any non-unit protection method, functional interoperability can be achieved between different protection algorithms (embedded in different relays) running on the same network, or even the same DC bus, with each relay being responsible for its own protection zone. Moreover, the framework can be used to protect the intellectual property of different vendors as the protective relays can be configured without the need for full access on the specifics of the underlying protection logic (e.g. configuration parameters of a WT-based method). The above can be achieved by providing information regarding a limited number of parameters to the protective relays, which in turn can determine the corresponding protection settings based on the proposed framework. The only inputs required for the configuration of the relay (and for the protection algorithms that are embedded in it) are the characteristics and length of the protected medium, number of the adjacent feeders, basic converter parameters and the value of the inductive termination. Furthermore, the framework is applicable for any VSC topology if the appropriate modifications are made, and is independent of the employed DCCB technology as the required time scales for FDA (<1 ms) are significantly smaller than the operation times of typical hybrid or mechanical DCCBs (2-10 ms).

The proposed framework provides a considerable degree of extensibility in case of grid expansion as only local parameters are required for protection design. Consequently, changes in protection settings are needed only if any of the components surrounding the local DC bus is affected. In such cases, the settings of the protection method can be updated using frequency domain analysis without the need for additional complex offline transient simulation studies.

Frequency domain analysis for DC protection design is primarily concerned with fully selective protection strategies, in which DC breakers are located at all line ends

together with current limiting series inductors. Nevertheless, the methodology's principles also apply for non-selective strategies provided there is at least a small-valued inductive termination. In such strategies in which de-energisation of the entire network is permitted, simple DC fault detection algorithms (unit or non-unit) suffice to determine the occurrence of a DC fault and trigger AC-side protection or fault tolerant converter actions for clearing the fault. On this basis, design of a fast non-unit protection algorithm based on the proposed methodology is not required, although it can still be used for recognising the faulted component or as a back-up protection algorithm (e.g. in case of communication failure for a primary unit protection method).

Finally, as illustrated in Figure 4.13, the methodology is also applicable in partially selective strategies. In such cases, the objective of the designed non-unit protection method using FDA is to identify the sub-grid in which the DC fault has occurred. In the example of Figure 4.13, relay R is responsible for issuing a trip command to the adjacent DCCB if a DC fault on Line 1 is detected. In this way, power transfer between sub-grids A and B can be safely continued through Line 2. On the other hand, if a DC fault occurs in sub-grid B, no action is required by relay R.

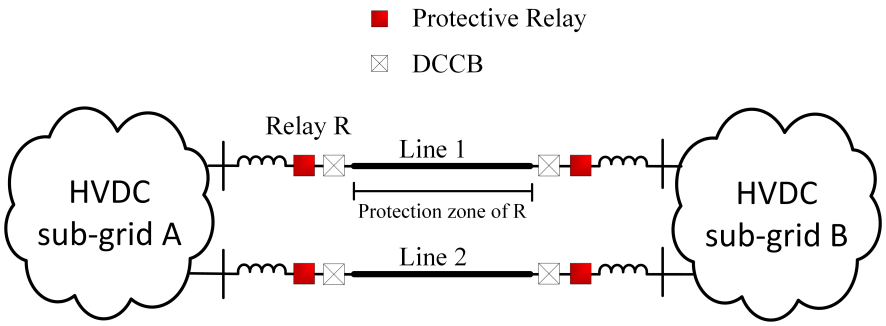


Figure 4.13: Use of non-unit protection for partially selective strategies.

4.5 Summary

The chapter has presented a methodology based on frequency domain analysis of DC faults for performing a comprehensive investigation of HVDC grid non-unit protection using travelling wave theory principles. To ensure the general applicability of the methodology, a generic HVDC grid section has been defined, in which only local parameters in the vicinity of the protection relay are required to be known. By analysing the frequency response of DC voltage at the relay location for strategically selected fault cases, recommendations and practical guidelines for voltage-based non-unit protection algorithms have been proposed. In detail, the hardest detectable internal fault (at the end of protection zone) and the hardest fault that should be classified by the relay as

external have been used to assess the general capabilities and limitations of non-unit protection and to identify the suitable frequency range for differentiating between them.

The proposed methodology enables flexible systematic investigation of grid and fault parameters that influence the voltage response for both internal and external faults. A sensitivity analysis of these parameters has been performed for both cable-based and OHL-based systems. In both cases, the length of the faulted medium (equivalent to fault distance) and fault resistance have been found to be the two main factors that limit the performance of non-unit protection, since for long lengths or high fault resistances the difference between the DC fault voltage signatures resulting from internal and external faults may be indistinguishable. The series inductor has been found to be the main grid component that influences non-unit protection as it has been demonstrated that for increasing series inductor sizes, protection margins also increase. In addition, the attenuation experienced by the incident voltage waves due to the line components can be compensated, thus leading to extended protection reach. The impact on non-unit protection of the converter parameters and the number of healthy feeders attached to the same bus with the faulted feeder was found to be negligible. The sensitivity analysis also revealed that protection margins are higher in OHL-based systems.

Furthermore, it has been shown that the proposed methodology can play an instrumental role for the design of non-unit protection algorithms that can be easily configured for any grid topology and grid parameters. First, the critical frequency, i.e. the frequency beyond which the impact of the hardest internal fault that is required to be discriminated becomes more pronounced than that of a solid external fault, is recommended as an indicator for selecting a suitable sampling frequency and defining the filtering requirements. Second, an approach for analytically deriving the protection threshold based exclusively on the prevailing local system conditions is provided. Third, a complementary tool for selecting series inductor sizes is proposed with the aim to improve protection margins. Finally, recommendations are provided for the flexible configuration of algorithm-specific settings. The proposed framework accommodates the deployment of multi-vendor HVDC grids with optimised protection systems, and renders the configuration of the selected non-unit protection methods insensitive to system parameter changes, either permanent (e.g. grid expansion) or temporary (e.g. line maintenance). As such, these enhancements provide significant benefits over conventionally designed non-unit protection solutions.

Chapter 5

Analytical Design of Wavelet Transform-based Non-unit HVDC Protection

The Wavelet Transform has been identified as one of the most effective tools for effective non-unit protection of HVDC grids. Nevertheless, the use of WT in practical protection applications has been impeded by the increased complexity in design due to the several WT-related parameters. To overcome this barrier, this chapter presents an analytical approach and detailed guidelines for WT-based non-unit protection schemes for HVDC grids using the design methodology that is based on frequency domain analysis of the transient period of DC faults that was introduced in Chapter 4. In detail, the representation of a generic HVDC grid section and the corresponding DC-side fault signatures in the frequency domain form the basis of a generalised approach for analytically designing a protection scheme based on WT and its various variants. The proposed solution is adaptive within its design stage and offers general applicability and immunity to system changes, while the protection settings are configured for optimised performance. A scheme based on Stationary WT (SWT) is designed and validated through offline simulations in PSCAD/EMTDC, while the technical feasibility of the algorithm in the real world is demonstrated through the use of real-time digital simulation and Hardware-in-the-Loop (HIL) testing. The latter constitutes the first attempt for practical implementation of SWT for HVDC protection applications.

5.1 Motivation

In current literature, the majority of non-unit protection algorithms have been designed after extensive time domain simulations to estimate the expected voltage and current

signatures and derive the protection thresholds accordingly. Therefore, the designed protection system (accounting for the method and the corresponding thresholds) is only applicable for the system conditions studied, and hence its ability to adapt to different network configurations (in terms of equipment used, converter topologies, network architecture etc.) or conditions is challenged. As a result, their general applicability is not ensured, and there are no guarantees that they will perform and operate as designed.

Signal processing techniques, and especially WT have been widely used in non-unit protection schemes [181, 182, 184, 186, 188, 189, 191, 244–246]. Due to its time and frequency localisation capability, WT can be used to extract the necessary information in specific frequency bands of the transient voltage. As explained in the previous chapter, the introduction of series inductors, impacts the frequency characteristic of the voltage signatures and hence, the resulting WT outputs (coefficients), thus providing the capability for discriminative fault detection. However, in all these implementations, very limited insight and guidelines have been provided as to how to derive an analytical approach for flexible WT design. In particular, the appropriate wavelet decomposition level, the mother wavelet and the protection thresholds are conventionally determined through extensive offline trial and error simulations. The absence of an analytical approach implies that the selected WT settings are most likely applicable only for the single test network that is being considered in each case.

Several WT-based protection methods based on Discrete Wavelet Transform (DWT) have been proposed in the literature [181, 182, 184, 186, 244, 245]. However, the effect of the downsampling process that is an essential element of DWT has not been analysed in depth. Downsampling leads to loss of information in the high frequency content of the analysed signal and may result in maloperation of the protection method. Therefore, the effect of this process should be taken into account or other WT variants can be utilised that overcome the lack of translation invariance caused by DWT. In [191], the stationary wavelet transform which demonstrates time-invariance transformation property has been used on current and voltage measurements to detect DC faults in HVDC grids. Nevertheless, the DC inductor as a boundary element is not considered and hence, selectivity of the method is not ensured.

The shift-sensitivity due to the downsampling process has been considered in [189], where the authors use two adjacent data windows for applying DWT in order to overcome this issue. A 2 ms data window length is used for applying DWT, which is deemed relatively long for HVDC grid protection. Moreover, the identification of a critical frequency beyond which the impact of highly resistive internal faults is more pronounced than the impact of external faults has been performed. This is a strong starting point for identifying the lowest suitable decomposition level than can be selected but depending on the sampling frequency of a WT-based method, there might be several levels

that satisfy this requirement.

The Real-Time Boundary SWT (RT-BSWT) has been proposed in [188,246], as an alternative method for avoiding the issues of downsampling. This method results in high speed detection and in reduced computational requirements. Nevertheless, in this method as well, the key WT parameters are mainly selected through trial and error simulations and consequently general applicability is not guaranteed.

To overcome the above limitations, this chapter introduces a generalised methodology, specifically tailored for HVDC grid non-unit protection purposes, for flexibly deriving the key parameters of WT-based methods. In contrast with existing approaches, the key parameters of WT are analytically calculated by analysing the voltage response for key DC fault scenarios in the frequency domain, using the guidelines proposed in the previous chapter. Using this approach, a non-unit protection scheme based on SWT applied on transient voltage measurements is proposed for detecting and discriminating DC faults in HVDC grids. The approach is performed separately and locally for each protection relay of the HVDC grid to obtain the optimised settings for enhanced performance in each case. In this way, general adaptability of the protection scheme to any system configuration and immunity to different system conditions is ensured.

5.2 Wavelet Transform Theory

In this section, the wavelet transform theory is presented from the point of view of HVDC protection to aid the reader to understand the non-unit protection solution that is developed and presented in this chapter. In principle, wavelet analysis involves decomposing of the examined signal over translated and dilated wavelets. A wavelet is defined as a function ψ with zero average, as described by equation (5.1) [247]. This basically means that the area underneath the wavelet function is zero and that the energy is equally distributed between positive and negative direction.

$$\int_{-\infty}^{+\infty} \psi(t) = 0 \tag{5.1}$$

WT is characterised by a dilation or scale parameter (α) and a translation or position parameter (β). The scale parameter determines the size of the window in which WT is performed. A low scale refers to a compressed wavelet (or high frequency wavelet), while a high scale refers to a stretched wavelet (or low frequency wavelet). When the wavelet is stretched for the lower frequencies, the length of the wavelet increases. This means that at lower frequencies it becomes more difficult to identify the time at which a low frequency event occurs. Conversely, when the wavelet is compressed at higher frequencies, better localisation in time is achieved owing to the reduced length

of the wavelet. In conclusion, stretched wavelets and compressed wavelets are utilised to retrieve low frequency information and high frequency information, respectively.

Translation corresponds to the action of shifting the wavelet forward in time while analysing the entire signal. In detail, the translation parameter determines the time corresponding to the centre point of each time window [248]. By manipulating the scale and position parameters, the time-frequency properties of the original signal can be identified. The wavelet transform of a signal $u(t)$ with scale α at time t is calculated through the following formula [249]:

$$WT_{(\alpha,\beta)}u(t) = \int_{-\infty}^{+\infty} u(t)\frac{1}{\sqrt{\alpha}}\psi^*(\frac{t-\beta}{\alpha})dt \tag{5.2}$$

where ψ^* is the daughter wavelet that is a scaled and shifted version of the mother wavelet function ψ. Equation (5.2) implies that WT operates in a similar manner as the Fourier Transform, where the correlation between the signal to be analysed ($u(t)$) and the analysing function (i.e. the wavelet itself) is computed for different sets of α and β parameters. In detail, wavelet transform works as follows [247]:

- For a given starting scale and mother wavelet, each point of the mother wavelet is multiplied by the corresponding point in time of the analysed signal in order to derive the wavelet coefficients. This task is performed for the entire length of the overlapping region between the two functions.
- Then for the same scale, the wavelet is translated in time so that it encompasses the entire length of the signal. Throughout the translation, wavelet coefficients are calculated as in the previous step.
- The wavelet can then be rescaled (e.g. stretched) and the two previous steps are repeated.

This procedure produces the wavelet coefficients for a range of different scales and sections of the signal (i.e. time). If the scale and position parameters are varied smoothly (continuously), then this procedure is called Continuous Wavelet Transform (CWT). In other words, CWT can work out WT coefficients at every scale starting from that of the analysed signal up to the required maximum scale, while translation of the signal is performed smoothly over the full length of the signal. The maximum scale can be chosen based on the level of detail that is required and the available computational power.

5.2.1 Characteristics of Wavelet Transform

The main strength of the WT is that it achieves adequate resolution in both time and frequency domain. In line with the Heisenberg uncertainty principle, localising an event with maximum accuracy in both frequency and time domain cannot be realised simultaneously. The selection of the scale parameter determines whether accurate time or frequency localisation is achieved. In particular, when scale α decreases, the time domain becomes narrower, but the frequency domain becomes wider. Conversely, when scale α increases, frequency domain narrows and time domain widens [248]. The impact of scale parameter on time and frequency domains is illustrated in Figure 5.1.

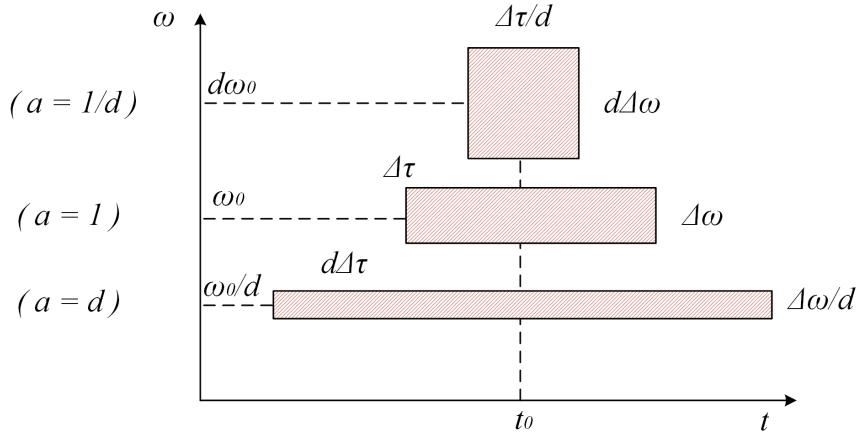


Figure 5.1: Time and frequency domains with respect to scale α.

The figure displays that the central point of time domain remains the same in all cases, while the central frequency can shift to a higher value for small scales, or to a lower value for higher scales. Specifically, when a wavelet is dilated by the scaling factor α, the new centre frequency with respect to the original centre frequency (F_c) becomes: $F_{new} = F_c/\alpha$. Due to the uncertainty principle, the time-bandwidth product should remain constant, meaning that the width of the time signal ($\Delta\tau$) and the width of the frequency signal ($\Delta\omega$) are related by a constant number. As a result of this property, the area of each box in Figure 5.1 is the same.

In the above example, the position parameter is assumed to be constant. Figure 5.2 shows the generalised case, in which the full time-frequency resolution of wavelet transform is presented. For low scales (high frequencies), where the size of the sliding window is smaller, finer time resolution is achieved, while frequency resolution is coarser. In contrast, at high scales (low frequencies) where the size of the window is greater, coarser time resolution and finer frequency resolution are obtained. These observations highlight the major advantage of WT, i.e. WT is capable of processing

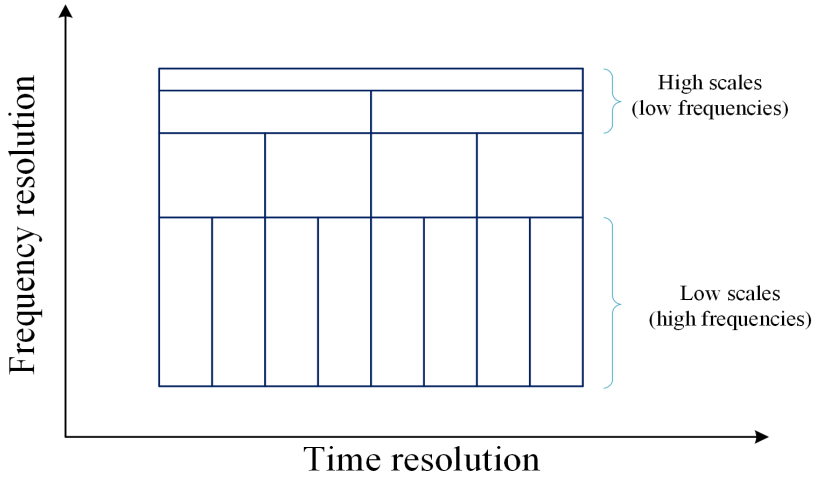


Figure 5.2: Time-frequency resolution of wavelet transform.

localised areas of a larger signal and revealing singularities in the data, such as discontinuity points, breakdown points or other trends that other signal processing techniques fail to detect. It is worth noting that different mother wavelets have different properties of time and frequency localisation. This significant feature is the main driver behind the utilisation of WT for HVDC grid protection, based on which abrupt changes in voltage and current traces can be identified.

5.2.2 Discrete Wavelet Transform

The calculation of wavelet coefficients through CWT at every possible scale involves intensive computational work and results in a large number of coefficients. Therefore, for the application of WT in real-time applications, such as DC fault detection, faster processing algorithms are required. Discrete Wavelet Transform (DWT) can be employed to provide a more efficient solution while maintaining high level of accuracy. The main difference between CWT and DWT lies in the way scale and translation parameters are defined. In detail, in DWT these parameters are discretised and can only take values based on the powers of two. This results in dyadic scales and positions that are expressed as follows:

$$\begin{aligned} \alpha &= 2^j \quad (j = 0, 1, 2, 3...) \\ \beta &= k\alpha, \quad \alpha \in Z \end{aligned} \tag{5.3}$$

Where j is the level of decomposition and k is a constant integer. This scheme can be efficiently implemented with the use of filters, as proposed by Mallat in [250]. The proposed algorithm is in fact, a two-channel sub-band coder, in which the filters that are typically used are the Quadrature Mirror Filters (QMF), where one filter is a mirror

image of the other filter around $\pi/2$. This practical filtering technique is called fast wavelet transform. The principles of fast wavelet transform are based on multiresolution analysis, according to which, the signal is passed through successive layers of low-pass and high-pass filters and each layer (or level j) produces low frequency approximation (A_j) and high frequency detail (D_j) coefficients, respectively. DWT based on multiresolution analysis is represented graphically in Figure 5.3, where $g(k)$ is the low-pass filter (LPF) and $h(k)$ is the high-pass filter (HPF).

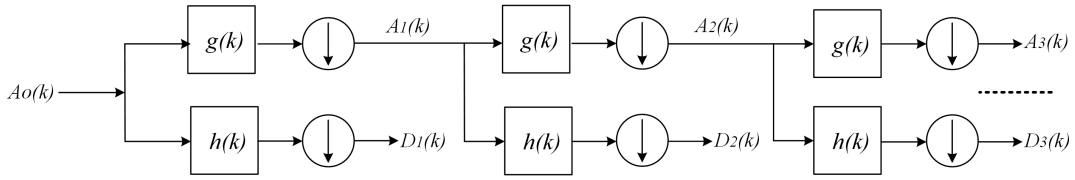


Figure 5.3: Multiresolution analysis.

The iterative analysis for a given signal of length N (samples), can be continued until an individual sample remains or equivalently, for $\log_2 N$ stages. After the signal passes through the filters of each layer, half of the samples can be discarded with limited loss of information and therefore, downsamplers are placed after the filters for increased efficiency. Downsampling is achieved by discarding every other point of the signal. The whole process is called wavelet decomposition or analysis and the outputs of each level j, are called DWT coefficients. Moreover, due to the successive filtering of the input signal, each decomposition level generates coefficients in different frequency bands. For a given sampling frequency Fs and considering Nyquist theorem, the corresponding frequency bands of the approximation and detail coefficients are given by:

$$\begin{aligned} f_{band-A_j} &= 0 \sim Fs/2 \cdot 2^j \\ f_{band-D_j} &= Fs/2 \cdot 2^j \sim Fs/2 \cdot 2^{j-1} \end{aligned} \tag{5.4}$$

It is evident that the frequency bands of wavelet decomposition can be known in advance and hence, the appropriate level can be readily selected to investigate the targeted frequencies of the signal to be processed. For the application of detecting DC faults in HVDC grids, if the transient voltage is used as an input signal for DWT and the frequency content that reveals the presence of the DC fault is known in advance or analytically determined, then the corresponding decomposition level that contains that set of frequencies can be used. Table 5.1 provides an example of the frequency bands at each level for a signal sampled at 100 kHz.

Table 5.1: Approximation and detail coefficients frequency bands for the first seven decomposition levels (base signal sampled at Fs=100 kHz).

Base signal (Fs=100 kHz)	Approximation coefficient frequency band [kHz]	Detail coefficient frequency band [kHz]
1^{st} level	0 – 25	25 – 50
2^{nd} level	0 – 12.5	12.5 – 25
3^{rd} level	0 – 6.25	6.25 – 12.5
4^{th} level	0 – 3.125	3.125 – 6.25
5^{th} level	0 – 1.56	1.56 – 3.125
6^{th} level	0 – 0.78	0.78 – 1.56
7^{th} level	0 – 0.39	0.39 – 0.78

5.2.3 Wavelet Reconstruction

The inverse process, in which the DWT outputs can be assembled back into the original signal is also possible. This process is called synthesis or wavelet reconstruction and is referred to as Inverse Discrete Wavelet Transform (IDWT). Upsamplers are used in the place of downsamplers in this case, where the outputs of the filters are lengthened by inserting zeros between successive samples (zero padding) [247]. If an input signal s has been decomposed by DWT up to the level J, then the signal can be reconstructed by adding the approximation coefficients of the J^{th} level and the detail coefficients of all decomposition levels up to level J, as shown by equation (5.5):

$$s = A_J + \sum_{j=1}^{j=J} D_j \tag{5.5}$$

The advantage offered by sequential decomposition and reconstruction of the original signal, is that the coefficients generated during the decomposition stage can be modified prior to the reconstruction stage. This process is typically used for data compression (e.g. image compression) and for removing the noise from the input signal. For example, when high frequency noise is present in voltage measurements captured from a protection relay, the detail coefficients that contain the noise, which has distinct properties under wavelet transform, can be filtered out from the signal by restricting their maximum values. In this way, a 'de-noised' version of the captured voltage can be obtained.

The selection of filters plays a crucial role in accomplishing perfect reconstruction of the original signal. Careful selection of filters for both reconstruction and decomposition stages should be made to cancel out distortion effects (aliasing) that is caused by the downsampling of the signal components during the decomposition stage. In addition, filter selection also determines the shape of the wavelets that can be used to perform

DWT and IDWT. This means that typically the coefficients of the QMF filters are designed first, which are then utilised to create a wavelet. In particular, by iteratively upsampling the filter coefficients and convolving the resulting vector with the original filter, a pattern that looks like a wavelet begins to emerge. This is the approach that has been followed to design several wavelet families such as the daubechies, coiflets, symlets etc., and is described in more detail in [247, 251].

Owing to the requirement for cancellation of the aliasing terms, specific conditions on the filter coefficients should be satisfied. As shown in Figure 5.4, one needs to define two pairs of QMF filters: one pair that consists of the decomposition filters g_D and h_D, and another one that consists of the reconstruction filters g_R and h_R. These are Finite Impulse Response (FIR) filters with a length equal to $2N$, where N is the order of the wavelet. According to QMF design principles, one filter needs to be designed first and the remaining filters can be designed based on this one [247, 251]. For example, for orthogonal wavelets, g_D is calculated as the QMF of h_D and the reconstruction filters are the time inverse of the decomposition filters.

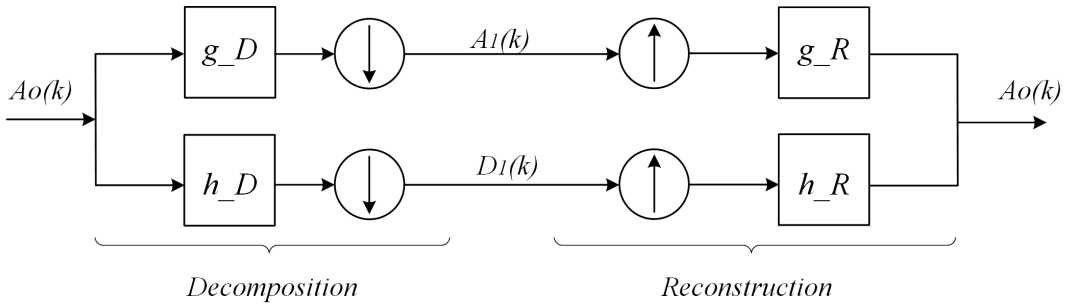


Figure 5.4: Decomposition and reconstruction filters used for wavelet transform.

Applying the process described in the previous section on the high-pass filters yields the function $\psi(t)$, or mother wavelet. Consequently, the mother wavelet is closely related to the high-pass filters and it can be used to generate the detail coefficients of DWT. By using the low-pass filter instead, a function very similar to a wavelet is yielded, i.e. the scaling function $\phi(t)$. Thus, the scaling function is associated with the low-pass filters and it is used to generate the approximation coefficients of DWT.

5.2.4 DWT principles

To explain the fundamental principles of fast wavelet transform or DWT, two arbitrary successive wavelet decomposition levels are considered $(j,\ j+1)$ in an effort to demonstrate the validity of the analysis for any pair of levels. It has been shown that the approximation coefficients at level j possess all the necessary information to produce the approximation and detail coefficients of level $j+1$. This implies that there

should be a connection between the wavelet function and the scale function ϕ for the two subsequent levels j and $j+1$. Indeed, such a relation exists and is called the twin-scale relation between ϕ and ψ. This relation is expressed by the following two equations [248]:

$$\phi\left(\frac{t}{2^j}\right) = \sqrt{2}\sum_{k=-\infty}^{\infty} g(k)\phi\left(\frac{t}{2^{j-1}} - k\right) \tag{5.6}$$

$$\psi\left(\frac{t}{2^j}\right) = \sqrt{2}\sum_{k=-\infty}^{\infty} h(k)\phi\left(\frac{t}{2^{j-1}} - k\right) \tag{5.7}$$

The twin-scale relation is a fundamental property of multiresolution analysis and is applicable to any two adjacent levels. Moreover, the relationship indicates that the scale function can be used to generate the mother wavelet. For given filters h and g, any wavelet that satisfies (5.6) and (5.7) can be used. Furthermore, because scaling and wavelet functions are mutually orthonormal, filters g and h can be obtained from [249]:

$$h[k] = \int_{-\infty}^{+\infty} \phi_{j_0,l}(t)\psi(t)dt \tag{5.8}$$

$$g[k] = \int_{-\infty}^{+\infty} \phi_{j_0,l}(t)\phi(t)dt \tag{5.9}$$

Owing to the fact that all scaling and wavelet functions for differents scales and parameters, can be obtained from $\phi(t)$ and $\psi(t)$, in a similar manner, filters g and h can be used to produce all scale and wavelet functions.

Based on the above observations, the low-frequency approximation coefficients and the high-frequency detail coefficients can be given by:

$$A_j[n] = \sum_{k=0}^{L-1} A_{j-1}[k]g_j[n-2k] \tag{5.10}$$

$$D_j[n] = \sum_{k=0}^{L-1} A_{j-1}[k]h_j[n-2k] \tag{5.11}$$

where A_j are the approximation coefficients at level j (with initial signal samples representing A_0), n is the sample index and L represents the order of the filters $g_j[k]$ and $h_j[k]$, which depends on the selected mother wavelet and decomposition level.

5.2.5 Stationary Wavelet Transform

One significant drawback of DWT for HVDC grid protection purposes is that the resulting detail coefficients differ depending on the moment the DC fault occurs. This

is caused by the downsampling process involved at each decomposition level, which leads to loss of information that is present in the high frequency content. In particular, when analyzing a fault signal with DWT up to level j, the number of different sets of coefficients that can be extracted is 2^j. To overcome this issue, DWT could be applied 2^j times while moving the data window by one sample, as performed in [189]. However, as the decomposition level increases, this solution necessitates extensive calculations.

Alternatively, the problem can be solved using the stationary wavelet transform, which is a translation invariant transform. The translation-invariance property is achieved by providing the same number of coefficients as the analysed signal at each decomposition level. This is realised by upsampling the low-pass and high-pass filters (by means of zero padding) at each decomposition level, instead of downsampling the analysed signal as in DWT [252]. The rest principles remain the same as in DWT.

SWT is less efficient than DWT and requires additional time to extract the approximation and detail coefficients. Nevertheless, when compared to the option of performing DWT 2^j times on the fault signal, the total execution time of SWT becomes equal or smaller, especially as j increases. Therefore, SWT algorithm is proposed in this thesis to eliminate the loss of information and to extract the maximum benefit from the use of wavelet transform. The approximation and detail coefficients using SWT at each level j are obtained through:

$$A_j[n] = \sum_{k=0}^{L-1} A_{j-1}[k] g_j[n-k] \tag{5.12}$$

$$D_j[n] = \sum_{k=0}^{L-1} A_{j-1}[k] h_j[n-k] \tag{5.13}$$

Detail coefficients can be employed to successfully extract the necessary information present in the high-frequency spectrum of transient voltage following a DC fault. Hence, by identifying the appropriate frequency band and wavelet, and by setting a threshold on the magnitude of the resulting detail coefficients (that contain the high frequency information) an SWT-based HVDC grid protection solution can be designed.

5.3 Analytical Design of WT-based HVDC Protection Schemes

This section presents a generalised analytical approach for deriving the main WT design parameters based on frequency domain analysis in an effort to address the WT design complexities that were identified in Section 5.1. In detail, the proposed approach involves the determination of the appropriate mother decomposition level, mother wavelet

and the corresponding protection threshold for optimised performance of WT-based non-unit protection schemes for HVDC grids. Although SWT is used, the process for selecting the parameters is valid for any WT variant. The generalised grid section of Section 4.2 with the same parameters is used as an example for validating the analysis.

5.3.1 Selection of Decomposition Level

One of the crucial parameters that needs to be determined when designing a WT-based fault detection and discrimination algorithm, is the wavelet decomposition level. The selection of the level depends on the frequency content of interest of the signal to be processed. It is evident from Table 5.1 that depending on the sampling frequency, the frequency bands of wavelet decomposition procedure can be known in advance and hence, the appropriate level can be analytically determined based on the targeted band of frequencies in the signal. Using the approach of Chapter 4 and the same generic HVDC grid section (see Figure 4.1) with the parameters of Subsection 4.2.4, the frequency response in terms of the magnitude of the transfer functions for faults at locations F_{int} (i.e. at the very end of the protected medium) and F_{ext} (i.e. at the end of the medium right outside the protection zone) are displayed in Figure 5.5.

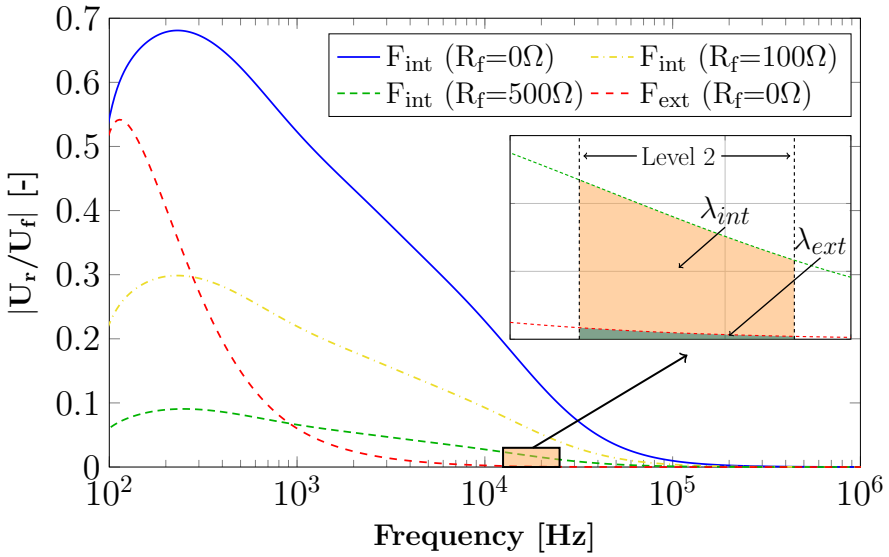


Figure 5.5: Transient voltage frequency response in the case of a solid external fault and for various fault resistances of the internal fault.

The frequency responses of the voltage transfer functions are used to identify the decomposition level (and its corresponding frequency band), in which the impact of a highly-resistive internal fault is more distinctive than that of the external fault. To quantify this impact, the areas underneath the U_r/U_f transfer functions are calculated at each level j, for a 500 Ω resistive fault at F_{int} and for a solid fault at F_{ext}, as shown

in (5.14). The areas are denoted as $\lambda^j{}_{int}$ and $\lambda^j{}_{ext}$, respectively. Based on (5.15), the level that maximises the ratio $\lambda^j{}_{int}/\lambda^j{}_{ext}$ is selected.

$$\begin{aligned} \lambda^j_{int} &= \int_{l_j}^{u_j} |U_r/U_f|_{F_{int}^{(R_f=500\Omega)}} df \\ \lambda^j_{ext} &= \int_{l_j}^{u_j} |U_r/U_f|_{F_{ext}^{(R_f=0\Omega)}} df \end{aligned} \tag{5.14}$$

$$WT_{lvl} = \max_j(\lambda^j_{int}/\lambda^j_{ext}),\ for\ 1 \leq j \leq j^{max} \tag{5.15}$$

where l_j and u_j are the lower and upper bounds of the j^{th} decomposition level, respectively that depend on the selected sampling frequency (see Table 5.1). For the example of Figure 5.5, and assuming 100 kHz sampling frequency, the level that maximises the above function is the second wavelet decomposition level, and the corresponding λ_{int} and λ_{ext} areas are shown in Figure 5.5. The same approach can be followed for any parameters of the HVDC grid section and sampling frequency.

The fault resistance limit of 500 Ω that is applied in the calculation of (5.14) aims to represent an extreme highly-resistive fault that may still be likely to occur in a HVDC system, even with very low probability. For the system presented in Section 3.7, which has a system voltage of ±320 kV, a limit of 500 Ω is selected to cover a range of events up to relatively unlikely situations. Similarly, the fault resistance limit can be adjusted on a per case basis according to the voltage and power rating of the system under consideration.

5.3.2 Threshold Selection

Non-unit protection methods do not offer inherent selectivity and they require an optimised protection setting to ensure that the maximum protection reach is achieved and that the method remains robust against external faults and other disturbances. FDA can be used for developing a generalised approach for directly calculating the protection threshold, while avoiding extensive electromagnetic transient simulations. A solid external fault is the hardest fault that should be detected and classified by the relay as an external fault for which no action is required. Hence, the voltage response of this fault is used for setting the threshold.

The required protection threshold can be determined analytically by using SWT to analyse the time-domain expression of $U_{r,ext}$, i.e. the derived voltage response for a solid external fault as performed in Subsection 4.2.4 (refer to Figure 4.3). According to Wavelet Modulus Maxima (WMM) theory [253], the threshold is equal to $WMM_{F_{ext}}$, which is the maximum point of the absolute voltage wavelet detail coefficients as shown

by:

$$WT_{th} = k \cdot WMM_{F_{ext}} = k \cdot max\big(\, |D_j(U_{r,ext})| \, \big) \tag{5.16}$$

where j is obtained using (5.15) and $D_j(U_{r,ext})$ are the j level detail coefficients which are calculated based on (5.13) with $U_{r,ext}$ as the analysed signal. In addition, k is a reliability factor that offers a safety margin and immunity against external influencing factors such as noise, measurement errors and other disturbances (here, k=5). The voltage, the SWT coefficients and the corresponding WMM for the external fault F_{ext} are displayed in Figure 5.6. Using this method for setting the threshold, it is ensured that the most critical external fault is outside the relay's protection reach, whilst reliable protection action for the weakest internal faults is guaranteed.

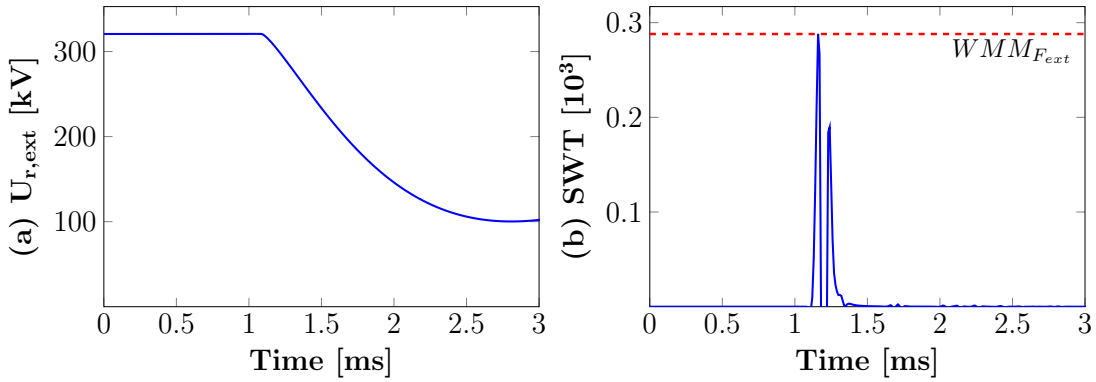


Figure 5.6: Threshold determination: (a) DC voltage profile for external fault, and (b) SWT detail coefficients and WMM.

Alternatively, wavelet energy WE_j or else the energy of the detail coefficients at level j can be used in the place of WMM as the main criterion for identifying internal faults. In this case, WE_j is given by:

$$WE_j = \int_0^{T_{window}} D_j[n]^2 dt \tag{5.17}$$

where T_{window} is the time window of voltage measurements that is used for the calculation of the energy. Similar to WMM, the protection threshold can be set by computing the wavelet energy over a time window of $U_{r,ext}$ that contains the DC fault signature.

The use of wavelet energy as a detection and discrimination function can theoretically lead to improved protection performance by exploiting more wavelet coefficients that accumulate the effect caused by the transient DC fault voltage. However, several disadvantages are introduced with the most important being the significant speed reduction of the protection algorithm as a consequence of the requirement for collection of a specific data window of voltage measurements before applying the wavelet transform.

After collection of the main dataset, the set has to be processed by WT leading to an additional time delay, while also data storage capability should be ensured. Moreover, due to the need for a large data buffer and the high number of computations that need to be performed at once, the total execution time of the algorithm is increased. Finally, additional measures must be taken to ignore or eliminate the boundary effect, according to which the WT coefficients are distorted when analysing the boundaries of the time window as the available samples are less than the filter length.

For the above reasons, the use of a direct threshold on SWT (or any other variant) detail coefficients, as calculated using equations (5.13) and (5.16), is preferred for the detection and discrimination of DC faults. In this way, a high-speed WT-based HVDC protection scheme with reduced real-time computational requirements is established.

5.3.3 Wavelet Selection

Selecting the right wavelet is of high importance for the successful implementation of WT, since each mother wavelet can lead to different operational performance of the protection solution. In current literature, WT has been widely used, but little insight has been provided as to what procedure should be followed for the determination of the appropriate mother wavelet. There are several factors that shall be considered such as, the nature of the analysed signal, the computational requirements and the application-related aspects and goals (e.g. time localisation of voltage transients in DC fault detection and location applications) [254].

An initial criterion can be based on the visual similarity between the waveform shape of the analysed signal and the selected wavelet. Moreover, symmetry and compact support are desirable properties. Wavelets with narrow compact support have better time domain localisation, which is a required feature for the analysis of short and fast transient disturbances. Each wavelet is characterised by its order (length) which is usually indicated in the name of the wavelet, e.g. *dbN* corresponds to a wavelet of the Daubechies family where the order is equal to $2N$. For most wavelets, N coincides with the number of vanishing moments. To understand vanishing moments, we should first consider the i$^{\text{th}}$ moment of a mother wavelet that is given by [254]:

$$m_i = \int_{-\infty}^{\infty} t^i \psi(t) dt \tag{5.18}$$

If equation (5.18) is equal to zero, then it can be said that the i$^{\text{th}}$ moment vanishes. If all moments within the range $0 - N$ vanish, then the mother wavelet is defined to have N vanishing moments. The higher the number of vanishing moments, the better the capability of the wavelet to represent a complex signal and consequently, the better it is in localising singularities in the signal [254]. As vanishing moments increase, the

regularity of the wavelet increases and it can produce smoother representations of the transients in the analysed signal. Moreover, a higher wavelet order N also means greater filter length and leads to better signal approximation. However, very high wavelet orders smooth the WT coefficients and result in poor time localisation properties and increased computational complexity, which hinders the feasibility of WT for real-time applications. Consequently, wavelets with 6-12 filter coefficients are considered as a trade off between computational burden and protection performance.

Quantitative approaches have been proposed for choosing the right wavelet such as, the Pearson coefficient [245], the maximum absolute error and the Root Mean Square Error (RMSE) [255] between the original signal and a reconstructed version of the original signal. However, in the context of this analysis, none of these methods offered further insight since all the remaining wavelets performed similarly well.

Based on the above discussion and considerations, the appropriate mother wavelets can be limited to a few options, but it is not possible to single out a wavelet that performs sufficiently well for any HVDC grid section. Consequently, an additional criterion is required to obtain the optimum mother wavelet. The criterion proposed in this work is the capability of different mother wavelets in providing enhanced protection margin and resiliency against highly resistive faults. For the generic section of Figure 4.1, the WMM for a DC fault at location $\mathrm{F_{int}}$ with fault resistance equal to 500 Ω (same limit as in Subsection 5.3.1) is compared against the corresponding WMM that is obtained for a solid fault at location $\mathrm{F_{ext}}$ for all the remaining wavelets. Assuming a set Ψ that comprises of all candidate mother wavelets, the wavelet $\psi \in \Psi$ that exhibits the highest ratio $WMM_{F_{int}}/\,WMM_{F_{ext}}$ is selected as shown by (5.19). The final protection threshold is then selected based on the $WMM_{F_{ext}}$ of the best performing wavelet WT_{wav} using (5.16).

$$WT_{wav} = \left\{ \psi : \max_{\psi} \left(\frac{WMM_{F_{int}}^{R_f=500\Omega}(\psi)}{WMM_{F_{ext}}^{R_f=0\Omega}(\psi)} \right) \;,\; for\ \psi \in \Psi \right\} \tag{5.19}$$

Table 5.2 presents the analytically calculated ratios (for mother wavelets of set Ψ) obtained through the analytical analysis and the corresponding ratios obtained through time-domain simulations of a detailed model in PSCAD. It is evident, that the analytical approach yields very similar results to those obtained from PSCAD, thus proving the suitability of the approach for designing WT-based HVDC protection schemes without the need for offline simulations. It is evident from Table 5.2 that wavelet $sym4$ presents the highest ratio by far and is therefore selected. Even for a very highly-resistive fault (500 Ω), $sym4$ demonstrates a WMM that is 21 times higher than the corresponding WMM for the external fault. It is evident that selecting a wavelet based on this criterion

maximises the protection margin of the protection method.

Table 5.2: Comparison of $WMM_{F_{int}}/WMM_{F_{ext}}$ ratios obtained using PSCAD simulations and the analytical approach.

Mother Wavelet	PSCAD-based Ratios	Analytical-based Ratios
db3	3.1680	3.0164
db4	1.591	1.606
db5	14.828	15.061
db6	13.671	13.916
sym3	3.1680	3.0164
sym4	**21.1450**	**21.640**
sym5	18.555	18.802
sym6	19.895	20.603
coif2	14.785	17.704
Bior 1.3	3.7132	3.7506
Bior 1.5	1.1486	1.2271
Bior 2.2	4.6164	5.0302
Bior 2.4	2.4785	2.5088

5.3.4 Proposed Protection Scheme

Based on the generalised analysis of the previous subsections, a non-unit HVDC protection scheme is proposed which comprises of two stages. Figure 5.7 shows the overall protection scheme that is employed by each relay. The first stage is a parametrisation procedure to select the optimum WT parameters (which is carried out offline) and the second stage is a real-time signal processing process (based on SWT) that is responsible for detecting internal faults.

Relay Configuration Stage

In this stage, the suitable wavelet decomposition level, mother wavelet and protection threshold are derived based on the approach that was previously presented. The determination of SWT parameters is realised locally using the FDA methodology at each relay location by taking into account the system parameters, namely, the feeder length and geometry, the number of other attached feeders to the same terminal, the converter parameters and the inductive termination. In case there is a change in the system parameters (e.g. equipment replacement, scheduled maintenance, grid expansion), the procedure is re-initiated to reconfigure the relay parameters. In this way, optimised settings for the protection scheme under all circumstances is guaranteed.

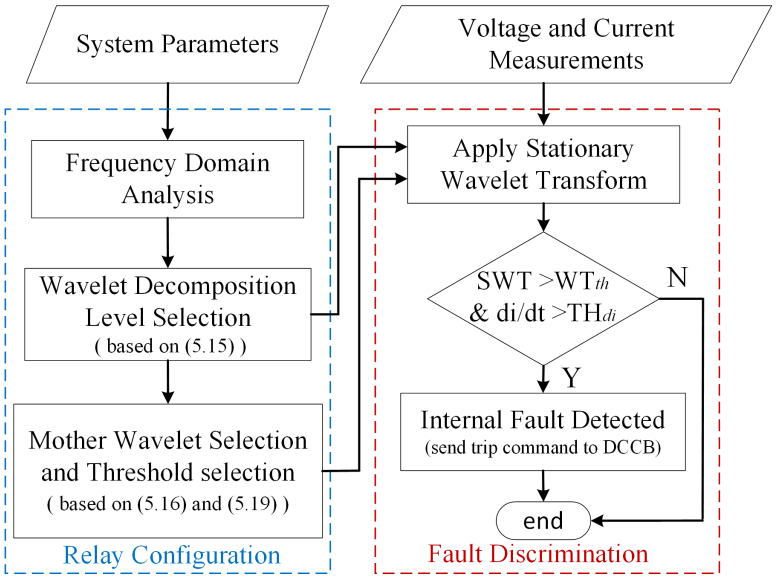


Figure 5.7: Flowchart of protection scheme.

Fault Discrimination Stage

In the second stage of the protection algorithm, selectivity is ensured by applying SWT on voltage measurements captured by the relay that is placed on the line-side of the series inductor. To guarantee selectivity, protective relays should be placed at each end of a transmission medium at both poles of the HVDC grid. In this way, only the faulted segment can be securely isolated. Since line-side pole voltage does not contain information regarding the direction of the fault, the current derivative di/dt is employed to provide directionality (i.e. distinguish between forward and backward faults). Assuming positive current as the current that flows into the feeder, a positive di/dt indicates that a fault lies in the forward direction of the protection relay (towards the other end of the DC cable), whereas a negative di/dt indicates that the fault is in the backward direction. Consequently, a positive near-zero threshold TH_{di} on current derivative is used. The calculated parameters from the first stage are utilised by SWT to successfully discriminate between internal and external faults. If the detail coefficients exceed the analytically calculated threshold WT_{th}, then an internal fault is detected. When an internal fault is confirmed, the relay sends a tripping signal to the corresponding DC circuit breaker to isolate the faulted DC line or cable. It should be noted that the protection scheme is designed to be unbound to a specific breaker technology and hence, it is not dependent on DCCB characteristics, such as breaking speed and maximum current breaking capacity.

5.4 Simulation Studies

5.4.1 HVDC Grid Test System and Methodology

The symmetrical monopolar four-terminal HVDC grid model that was developed with the PSCAD/EMTDC simulation tool and presented in Section 3.7 is used in this chapter (shown also in Figure 5.8) to validate the performance of the protection scheme. All converters are represented using the HB-MMC averaged value modelling approach that was presented in Subsection 2.2.5 of Chapter 2. The converter protection is activated when the current exceeds twice the maximum continuous IGBT current or if DC voltage drops below 0.8 p.u (with 0.1 ms delay). Protective relays with DCCBs are placed at each cable end and the latter are modelled with an operation time delay of 3 ms. The main parameters of the HVDC grid and the MCCs are summarised in Table 5.3.

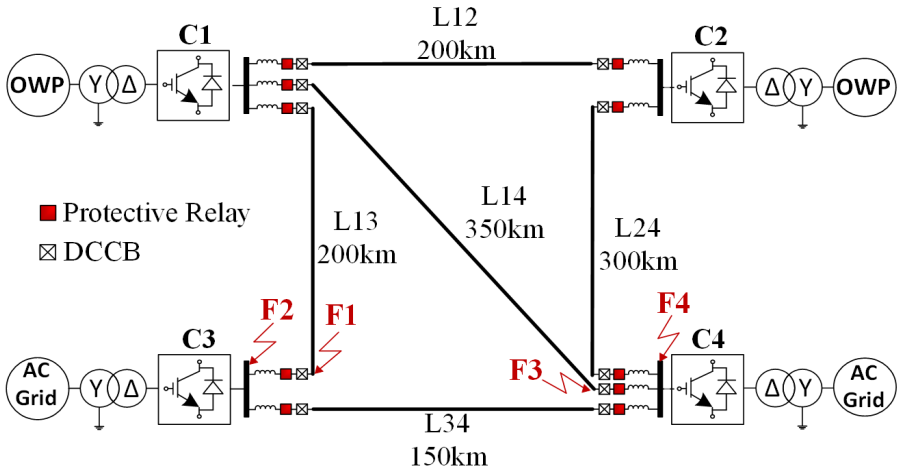


Figure 5.8: HVDC grid test system.

Table 5.3: System and converter parameters.

Parameter	Value
Nominal DC voltage	± 320 kV
Rated AC (line-to-line) voltage	360 kV
Rated power (C1∼C4)	1000 MVA
Active power setpoint (C1∼C4)	700,700,−800,−600 MW
Reactive power setpoint (C1∼C4)	100,100,−100,−100 MVAr
DC inductors	50 mH
Arm inductance	42 mH
Arm resistance	0.08 Ω
Arm capacitance	31.42 μF

The following subsections present simulation results which demonstrate the overall protection performance of the proposed method under different DC fault scenarios and operating conditions. With reference to the HVDC protection requirements set out in

Section 3.1, selectivity, sensitivity and robustness of the method are assessed in this section, while speed and reliability aspects will be considered in the real-time HIL studies in the next section. Special consideration is given to simulation results that confirm the main benefits achieved via the use of FDA methodology for configuring the SWT-based protection solution, i.e. maximised protection reach and enhanced selectivity (capability for discrimination). In doing so, the settings obtained through the offline configuration stage (FDA) are initially provided for all protection relays of the entire HVDC grid test system. Afterwards, fault studies for PTP and PTG faults are conducted in an effort to confirm the discrimination capabilities of the proposed method. The protection relay of cable L13 (at the cable end closer to C1) of the HVDC grid test system is used as the base case. In analogy to the approach followed in Chapter 4, a highly resistive internal fault at location F1, and a solid external fault at location F2 (both locations shown in Figure 5.8) are used in these studies.

To further scrutinise the method's discrimination capabilities under different conditions, a sensitivity analysis of influencing factors such as fault resistance, size of current limiting inductors, noise in voltage measurements and sampling frequency is performed to reveal their impact on the operation of the method. In these studies, the protection relays protecting both cables L13 and L14 are tested. Cable L13 is selected due to its average length (200 km), while Cable L14 is selected due to it being the longest of the entire grid. In this way, the impact of feeder length is also taken into consideration. Furthermore, a comparison with a well established protection method is carried out to highlight the relative merits of the SWT-based protection solution. Finally the robustness of the technique against external disturbances is demonstrated.

5.4.2 Relay Configuration

The relay settings with regards to SWT parameters are calculated based on the approach described in Section 5.3. In line with the recommendation provided by the review of DC instruments in Section 3.6, the sampling frequency for the proposed method is set to 100 kHz. The settings for each protective relay are cited in Table 5.4 (R_{ij} refers to the relay located at the end i of cable L_{ij}).

Since the cable characteristics, DC inductors and converter parameters of all terminals are the same, the length of the cable and the number of cables connected at the bus adjacent to the relay are the two main factors affecting the relay settings. For the relays protecting the shorter cables L12, L13 and L34, the second level is obtained by the analytical approach and used for the calculation of the coefficients. In contrast, owing to the greater attenuation that is provoked on the high frequency content of the voltage waves travelling in longer cables, the third decomposition level (lower frequency band)

is obtained through (5.15) and employed by the protection relays of cables L14 and L24. Moreover, several wavelets have been selected based on the analytical approach, thus confirming that the use of different mother wavelets at different relay locations is advantageous for improved protection performance as opposed to conventional trial and error approaches in which a single wavelet is selected for all protection relays.

Table 5.4: Relay configuration settings.

Cable	Relay	Level	Wavelet	Threshold [10^3]
L34	R_{34}	2	sym5	3.750
	R_{43}			3.756
L13	R_{13}	2	sym4	1.441
	R_{31}			1.453
L12	R_{12}	2	sym4	1.457
	R_{21}			1.453
L14	R_{14}	3	db5	2.623
	R_{41}			2.643
L24	R_{24}	3	coif2	3.475
	R_{42}			3.507

In the simulation studies, the SWT detail coefficients calculated by relay R_{ij} are denoted as SWT_{ij}. A SWT detail coefficient is calculated every time a DC voltage measurement is received using (5.13). The required number of voltage samples for the calculation of each coefficient varies depending on the selected decomposition level and mother wavelet. For instance, 16 samples are required by relays of cable L13 that use wavelet $sym4$ at level j=2. The relay configuration stage guarantees the maximum benefit and protection reach of SWT-based HVDC grid protection.

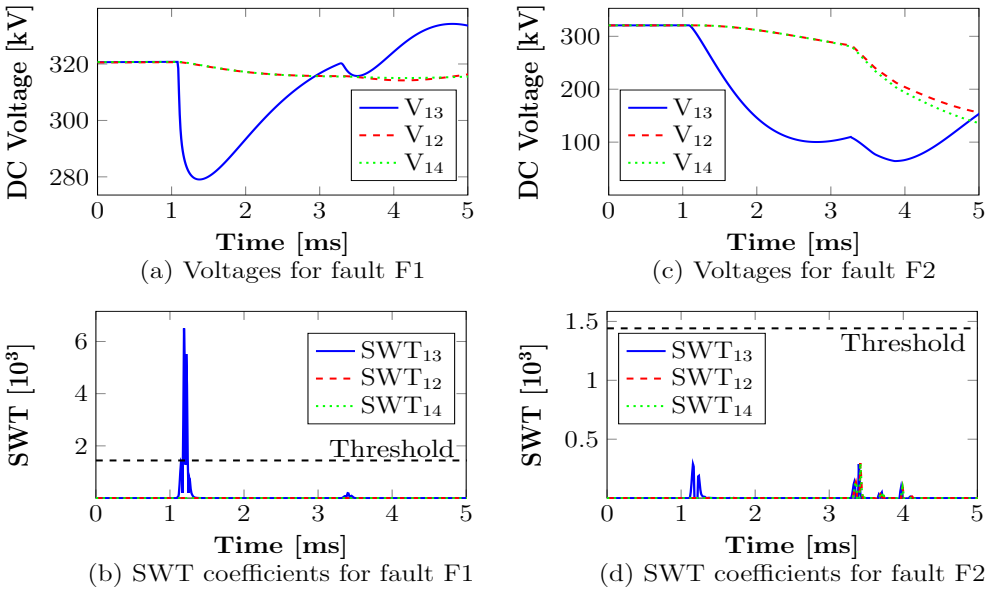
5.4.3 Selectivity of the Proposed Method

This subsection validates the performance of the protection scheme and its effectiveness in discriminating between internal and external faults. To test the method under the most challenging conditions, the hardest internal and external faults are selected. In detail, an internal high-resistive fault is applied at the end of cable L13 (location F1 in Figure 5.8), and a solid external fault is applied at location F2. Both PTP and PTG faults are investigated, while all faults occur at t=0 ms.

Pole-to-pole Faults

Figure 5.9 shows the results for PTP faults at fault locations F1 and F2. The fault resistance of the faults is 500 Ω and 0.01 Ω, respectively. In both cases, after approximately 1.1 ms (due to the time it takes for the travelling wave to reach relay R_{13}) the

DC voltage at the relay location, V_{13}, starts to fall (Figure 5.9(a) and 5.9(c)). In Figure 5.9(b), SWT_{13}, the wavelet coefficients corresponding to DC voltage V_{13} for fault F1 demonstrate a WMM of 6.23x10^3, which clearly exceeds the calculated threshold, approximately 120 μs after the fault wave reaches the relay location. Hence, an internal fault is detected at very high speed and a trip signal is sent to the associated DCCB. Moreover, the wavelet coefficients calculated by the rest relays of the same terminal (R_{12} and R_{14}) are also shown in the same figure for comparison. It is evident that there is no visible change in magnitude of these coefficients. On the contrary, SWT_{13} for the external fault at F2 (Figure 5.9(d)) has a maximum WMM of 0.288x10^3, which is well below the threshold and therefore, no trip signal is generated. Moreover, for fault F2, converter protection is activated around 3.3 ms, nevertheless, the generated SWT coefficients at this instance are well below the threshold.



(a) Voltages for fault F1 (c) Voltages for fault F2

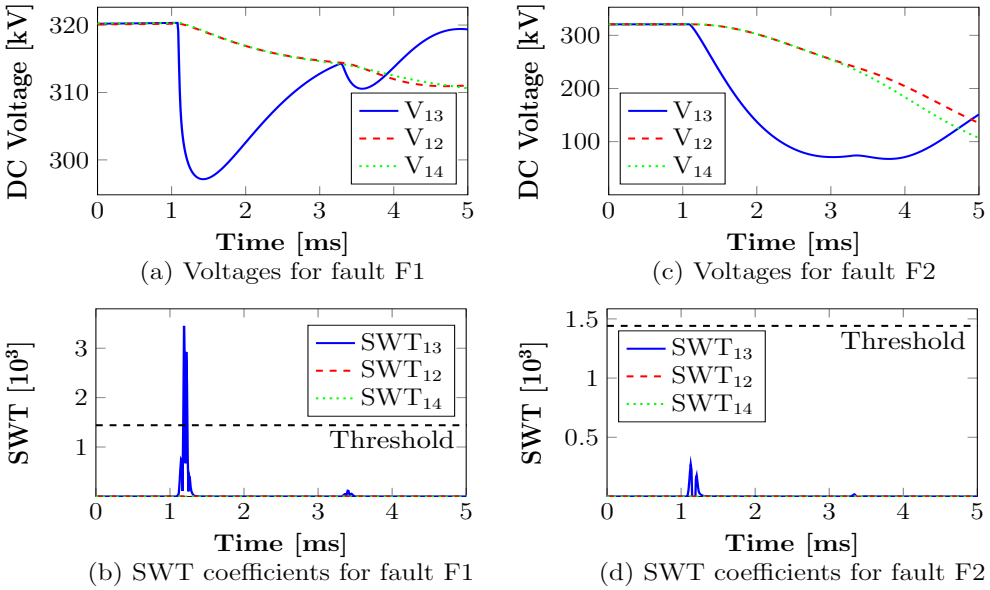
(b) SWT coefficients for fault F1 (d) SWT coefficients for fault F2

Figure 5.9: Waveforms during PTP faults at F1 (R_f=500 Ω) and F2 (R_f≈0 Ω).

Pole-to-ground Faults

A positive PTG fault is applied at fault locations F1 (Figure 5.10(a) and 5.10(b)) and F2 (Figure 5.10(c) and 5.10(d)) with the same fault resistances as in the previous scenario. For a PTG fault at F1 the derived wavelet coefficients SWT_{13} are smaller in magnitude compared to those for a PTP fault. Nevertheless, the coefficients reach a value of 3.45x10^3, thus exceeding the threshold and an internal fault is detected almost instantaneously (in less than 150 μs). Hence, the proposed method can successfully detect internal PTG faults with weaker fault transients. For fault F2 the coefficients

do not exhibit any significant change (WMM of 0.268x10^3) and no DC fault is detected. In this study also, there is no detectable change in the magnitude of SWT_{12} and SWT_{14}.



(a) Voltages for fault F1

(c) Voltages for fault F2

(b) SWT coefficients for fault F1

(d) SWT coefficients for fault F2

Figure 5.10: Waveforms during PTG faults at F1 (R_f=500 Ω) and F2 (R_f≈0 Ω).

Through the PTP and PTG fault studies, it has been confirmed that the proposed method can distinguish with ease internal highly resistive faults from external solid faults. It is remarkable that for both types of faults, there is a high margin between the magnitude of SWT_{13} for faults at F1 and F2, which implies that internal faults with even higher fault resistance can be effectively discriminated. By showcasing the method's successful operation for the farthest and very highly resistive internal fault at F1, it becomes clear that DC faults with lower fault resistance or at closer distance will also be correctly detected. This assertion will be further consolidated through the real-time HIL studies, which will be presented in the next section.

5.4.4 Influence of Fault Resistance

In this subsection, the sensitivity of the protection method is investigated, while also the maximum theoretical resistance values are identified. Figure 5.11(a) compares the WMM of SWT coefficients calculated by R_{13} for PTP and PTG DC faults at location F1 against the selected threshold to demonstrate influence of fault resistance on the protection system. The results indicate that as fault resistance increases, the magnitude of SWT coefficients diminishes due to greater attenuation of the fault voltage wave. However, even for a PTG DC fault with R_f=1000 Ω, the SWT coefficients exceed the threshold and the DC fault is successfully detected.

The same analysis is performed for cable L14 for an internal fault at F3 and external fault at F4 (see Figure 5.11(b)). The incident voltage wave experiences higher attenuation due to the greater length of L14, resulting in smaller SWT coefficients as calculated by R_{14}. Consequently, the maximum fault resistance that can be discriminated for a PTG fault is just below 500 Ω. It is promising that even when a conservative reliability factor is used for determining the protection threshold (i.e. k=5), the method still demonstrates enhanced sensitivity to highly resistive faults. These results highlight even further the enhanced protection margins and the sensitivity of the SWT-based solution achieved through the use of the analytical methodology.

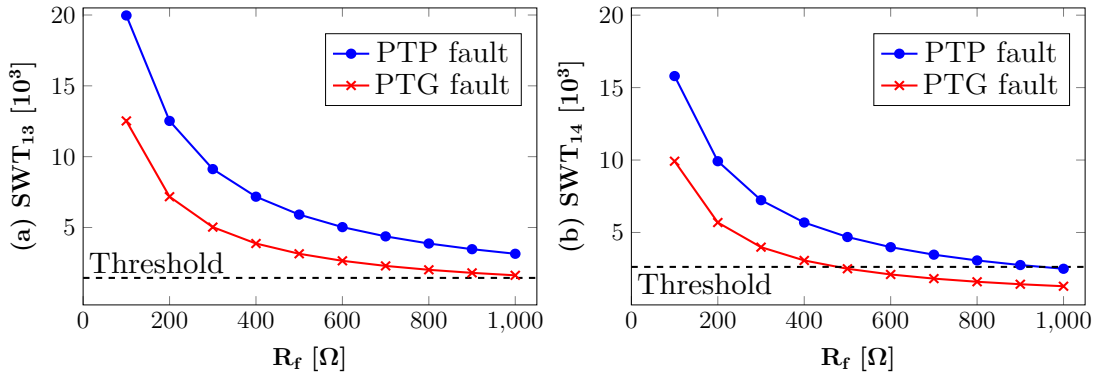


Figure 5.11: Maximum SWT coefficient as a function of fault resistance for PTP and PTG faults on cables (a) L13 and (b) L14.

5.4.5 Influence of Inductor Size

It has already been established in Subsection 4.3.3 that the size of current limiting inductors directly influences the protection reach of non-unit protection algorithms. To investigate this effect, the size of all series inductors of the HVDC grid test system is varied from 20 mH to 200 mH in steps of 20 mH, and the SWT_{13} coefficients are calculated in each case for both a 500 Ω fault at location F1 and a solid fault at location F2. The corresponding WMM_{F1} and WMM_{F2} are reported in each case, and the WMM_{F1}/WMM_{F2} ratios are shown in Figure 5.12(a). Moreover, Figure 5.12(b) shows the corresponding thresholds WT_{th} obtained through Stage I of the proposed protection method for the investigated inductor sizes.

It is evident from Figure 5.12(a) that with increasing DC inductor size, the ratio WMM_{F1}/WMM_{F2} increases proportionally indicating that the protection margin of the method is increased. From Figure 5.12(b), it is shown that the relative benefit of the filtering effect of the inductor diminishes, as smaller changes occur in the calculated threshold for increasing inductor sizes. It can be concluded that the enhanced sensitivity of the proposed method is maintained for the entire range of inductor sizes that has

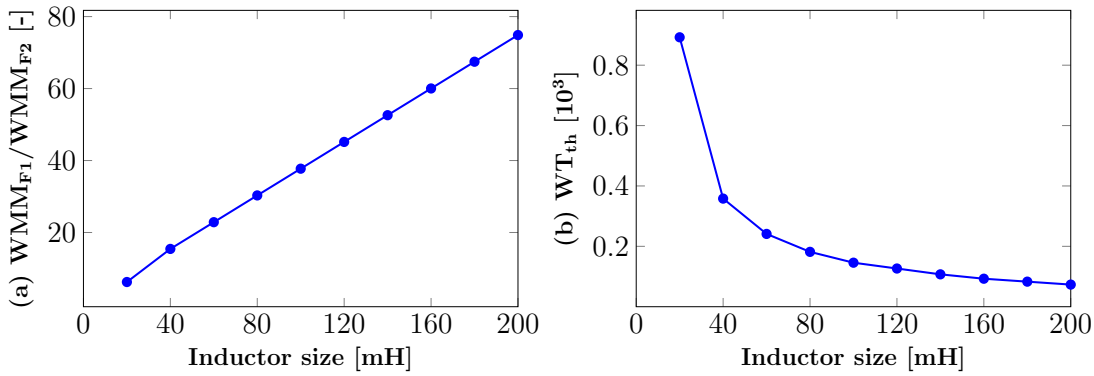


Figure 5.12: (a) WMM_{F1}/WMM_{F2}, and (b) WT_{th} as a function of inductor size.

been investigated. In detail the minimum observed WMM_{F1}/WMM_{F2} ratio is 6.24 for the case of a 20 mH inductor.

5.4.6 Influence of Noise

To demonstrate the performance of the proposed method in a noisy environment, the monitored voltage measurements for the same fault scenarios of the previous subsection are contaminated with artificial white noise to obtain different Signal-to-Noise Ratios (SNR), starting from 50 dB until 5 dB (lower dB values correspond to higher noise level). The WMMs in all cases are presented for relays R_{13} in Figure 5.13(a), and R_{14} in Figure 5.13(b). In both cases, the SWT coefficients are not affected by noise when SNR is equal or higher than 20 dB. For SNR equal or lower than 15 dB, the impact of noise becomes greater than the impact of the induced transients from the external faults F2 and F4. In these cases too, however, the SWT coefficients for the external faults do not exceed the selected thresholds.

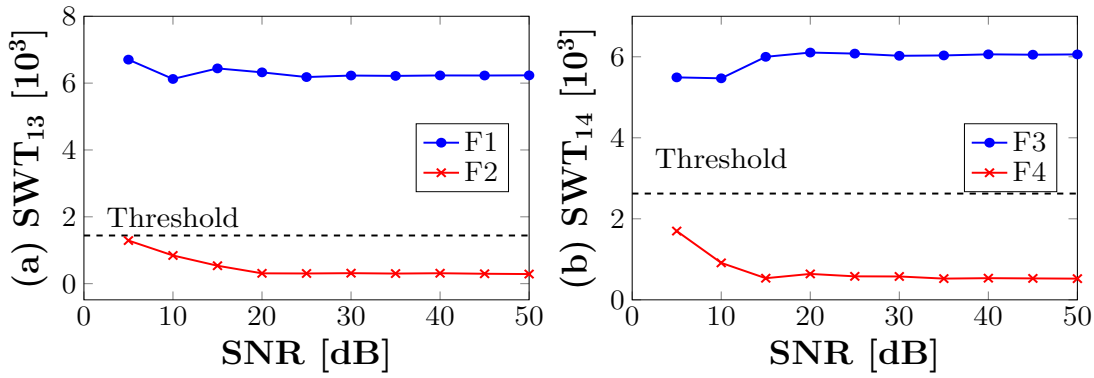
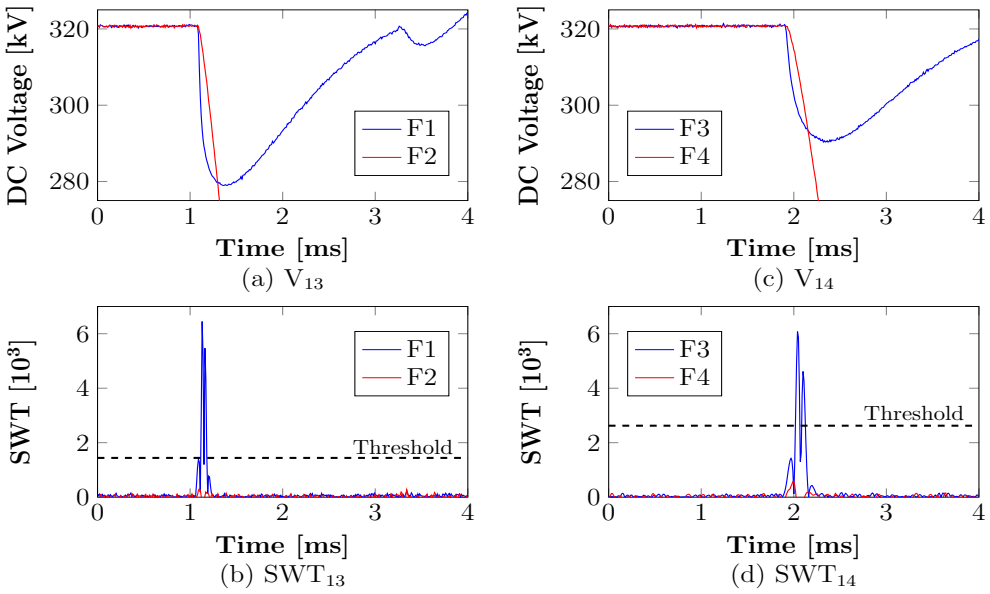


Figure 5.13: Maximum SWT coefficients at different noise levels for internal and external PTP faults on cables (a) L13 and (b) L14.

These results constitute the main driver behind the selection of a conservative reli-

ability factor. Provided the already high selectivity and sensitivity capabilities of the proposed method, k has been conservatively set to 5 to achieve a trade-off between sensitivity and resiliency to very high noise levels in voltage measurements. In a real environment, if the expected noise level is above 20 dB (which is usually the case), k can be set to a much lower value.

A detailed example is shown in Figure 5.14 for SNR=20 dB, where the DC voltage for faults F1 and F3 is zoomed to illustrate the noise impact. It is noteworthy that noise has less effect on the calculated coefficients by R_{14}. This is attributed to the fact that a lower frequency band is assigned to the third level used for the calculation of coefficients SWT_{14} and hence, high frequency noise is filtered out.



(a) V_{13} (c) V_{14} (b) SWT_{13} (d) SWT_{14}

Figure 5.14: Voltage profiles and SWT coefficients for SNR=20dB.

5.4.7 Influence of Sampling Frequency and Comparison

Faults F1 and F2 are repeated for different sampling frequencies to investigate their impact on the proposed method. The same analytical methodology of Section 5.3 can be applied for different sampling frequencies, resulting in different frequency bands and calculated thresholds. Table 5.5 cites the WMM_{F1}/WMM_{F2} ratios and the corresponding thresholds in each case for sampling frequencies ranging from 10 kHz to 100 kHz. It can be seen that lower sampling frequencies still deliver enough confidence for discriminative DC fault detection.

Moreover, the maximum detectable fault resistance for the internal fault (F1) is cited in Table 5.5 for each sampling frequency. The studies are repeated for another

voltage-based non-unit protection method for comparison. The selected method for comparison is the Rate Of Change Of Voltage (ROCOV) that was proposed in [164], and the corresponding maximum detectable fault resistances for all sampling frequencies are also derived and reported in Table 5.5. The same reliability factor (k=5) is used in all cases. It is evident that as sampling frequency decreases, the maximum detectable fault resistance is reduced. Nevertheless, the proposed method demonstrates significantly improved performance in terms of resiliency to highly resistive DC faults for all sampling rates, i.e. an improvement by a factor of 4.36 to 5.75 (from minimum to maximum).

Table 5.5: Protection thresholds, WMM_{F1}/WMM_{F2} ratios and comparison with ROCOV for different sampling frequencies.

f [kHz]	10	20	40	60	80	100
Threshold [10^3]	33.6	11.35	4.97	3.06	1.98	1.44
WMM_{F1}/WMM_{F2}	2.68	6	10.46	13.21	17.25	21.64
SWT Max R_F [Ω]	240	629	1128	1551	2044	2259
ROCOV Max R_F[Ω]	55	127	211	271	370	393

5.4.8 Robustness of the Proposed Method

In this subsection the robustness of the method against external disturbances such as, AC faults, active power changes and DCCB operation is investigated. The protection scheme should remain stable and not react during these events. A three-phase fault at the AC side of converter C1, a power order change from 800 MW to 0 MW for converter C1, and a trip event of the DCCB next to relay R_{31} (at the remote end of the protection zone with respect to relay R_{13}) are put forward for this analysis. The DC voltage is monitored by R_{13} and the measurements are displayed in Figure 5.15(a).

The corresponding SWT coefficients are illustrated in Figure 5.15(b). The three-phase fault and the power change order event have negligible impact on the coefficients' magnitude, indicating the high robustness of the proposed method. Conversely, the DCCB operation provokes a significant spike, which exceeds the corresponding WMM for a fault at F2. Therefore, it is likely that a breaker opening will cause maloperation of the protection. It is worth mentioning that operation of the DCCB that is adjacent to R_{31} with the concurrent non-operation of the DCCB next to R_{13} will only be required in the event of a DC fault on the bus behind R_{31}. Since in this scenario, there will be no power flow across the protected cable, potential maloperation of Relay R_{13} will not cause any disturbance to the operation of the HVDC grid. Nevertheless, the selected reliability factor (k=5) of the proposed method also ensures that a breaker tripping action at the remote line end does not interfere with the fault detection method.

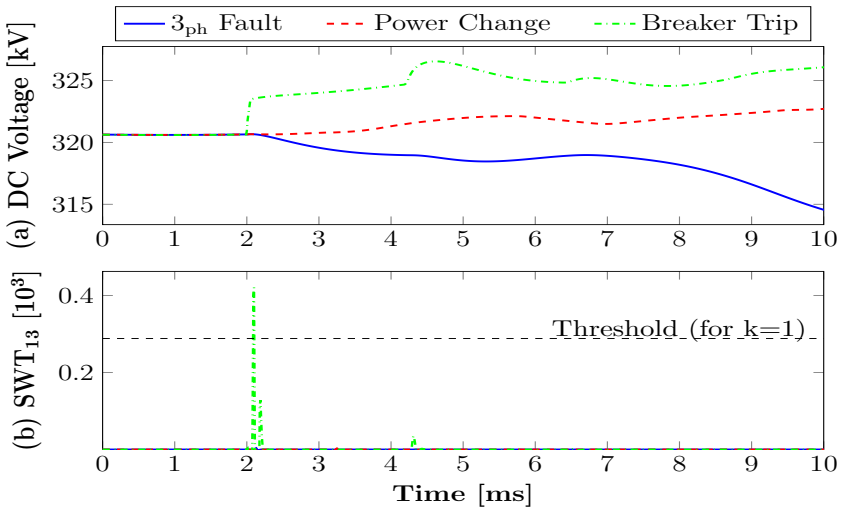


Figure 5.15: Waveforms captured by R_{13} during external disturbances: (a) DC voltages and (b) SWT coefficients.

5.5 Implementation and Validation of Real-time SWT-based Non-unit Protection

It has been shown that WT has been widely used in the technical literature, thus verifying the strength of the technique for HVDC grid protection but limited practical implementations have been reported. In particular, real-time implementation of WT has been reported for AC power system protection based on a Digital Signal Processor (DSP) [154], and a Field-Programmable Gate Array (FPGA) [155], while hardware platforms have been employed for the practical implementation of WT-based HVDC protection [184, 190, 245]. In all these applications, DWT has been utilised due to its reduced complexity. Nevertheless, the downsampling stages involved in DWT lead to loss of high frequency information which may compromise the performance in detecting and discriminating DC faults. For this reason, the use of SWT has been recommended in this thesis for increased HVDC protection performance. To date, there has been no practical validation of SWT for power system protection applications.

The purpose of this section is two-fold. First, an approach is introduced for designing an efficient real-time SWT implementation for HVDC grid protection based on DSP technology in order to demonstrate the technical feasibility of SWT for fast transient HVDC protection. Second, the suitability and the performance of the proposed SWT-based non-unit protection algorithm is confirmed through dynamic validation using real-time hardware-in-the-loop simulations under various realistic conditions. To fulfil the second objective and perform a high fidelity validation of the proposed protection technique, a representative HVDC grid model, which is identical with the one used in

the offline simulation studies, is developed using a real-time digital simulator.

5.5.1 Real-time SWT Implementation

SWT Algorithm

The SWT algorithm can be efficiently implemented with the use of discrete convolution based on Finite Impulse Response (FIR) filters [256]. In detail, the approximation and detail coefficients at each decomposition level j are calculated as the sum of the product of the N most recent input values with the N low-pass and high-pass filter coefficients, respectively. At each level j the wavelet filter coefficients are upsampled and discrete convolution is re-excecuted. This process is illustrated graphically in Figure 5.16.

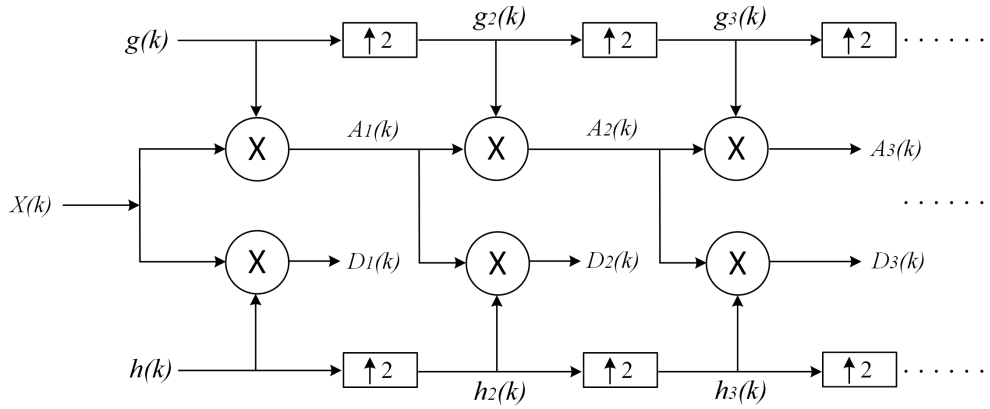


Figure 5.16: SWT algorithm.

This implementation of SWT algorithm can be extended for an arbitrary number of levels. However, due to the intrinsic computational complexity of SWT, the maximum decomposition level should not be too high because the computational delay accumulates as the level increases. Nevertheless, this is not a limiting factor for HVDC grid protection purposes since the most significant information of the transient phase of DC faults lies in the high frequency region (lower decomposition levels) of DC voltage as demonstrated in the previous sections of this chapter.

Hardware

For the hardware implementation of SWT, the Texas Instruments C2000 MCU F28379D Digital Signal Processor (DSP) has been used [257]. The device constitutes a low-cost solution for implementing efficiently and with high accuracy the SWT algorithm. The main features of the incorporated microcontroller are:

- 200 MHz dual C28xCPUs

- Dual 200 MHz programmable control law accelerators
- 1 MB Flash and 204KB RAM
- Four ADCs with selectable 16-bit/12-bit operation
- Three 12-bit DAC modules

The DSP was programmed in MATLAB-Simulink using an embedded coder support package available from TI. The first core of the hardware is assigned to calculate the SWT approximation and detail coefficients for the first two levels, while the second core is responsible for the calculation of the third level coefficients. To realise this operation, the calculated approximation coefficients for level 2 are sent from one core of the DSP to the other using inter-processor communication blocks available through the simulink TI library. As it will be demonstrated later, this configuration has proven to be effective for sampling frequencies up to 100 kHz and for mother wavelets with up to 20 filter coefficients.

Digital Real-Time Simulator

A DRTS can perform robust electromagnetic power system simulation in real-time and it can interact with external hardware via analogue and digital signals through hardware-in-the-loop simulation. Hence, the DRTS of RTDS technologies has been utilised to provide a realistic environment for the physical testing of the HVDC grid protection technique running on the DSP. The HVDC grid model used for the simulation studies is shown in Figure 5.17 and it has been developed with the use of RSCAD software that is the graphic user interface of the employed DRTS.

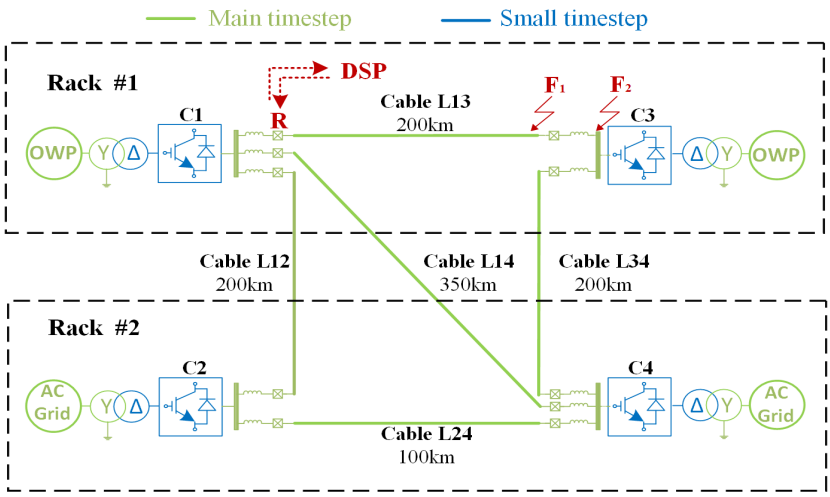


Figure 5.17: HVDC grid model in DRTS.

The HVDC grid model is designed to be identical with the model used in Section 5.4 with the parameters shown in Table 5.3. Similar to the previously used grid model, the cables are represented by frequency dependent (phase) models with the cable parameters from [81], 50 mH DC reactors are included in series with DCCBs at the ends of each cable, and the DCCB opening time is set to 3 ms.

The concept of multi-rate real-time simulation is employed to achieve greater accuracy and efficiency and consequently, two separate time steps are used. The large scale network simulations run on the main timestep of 50 μs. The AC networks and the DC cables along with the converter control systems operate at the main timestep. For greater accuracy in the representation of the converter dynamics, the MMCs are solved in the small timestep of 2500 ns. Each MMC is modelled inside a separate small timestep sub-network and requires a single core of a processor card (GPC). The accuracy of this approach in high fidelity representation of the MMC response has been confirmed in [258]. Due to the size of the simulated network, all available resources of the real-time simulator are utilised. In detail, the whole grid is split between two DRTS hardware racks that include two PB5 cards and five GPC (older generation) cards. The PB5 cards are assigned for the total network solution and the control systems, while the AC and DC power system components are assigned to the GPC cards.

To realise the multi-rate simulation concept, special interfaces available from the RSCAD library are required to migrate from the small timestep to the main timestep network and vice versa. In particular, interfacing transformers are employed to interconnect the AC networks and the Offshore Wind Plants (OWP) to the main converters, while short travelling wave line models are used to interface the converters to the main DC network. Due to the utilisation of the interface line models, which are effectively Bergeron transmission line models, the length of the DC cables is appropriately reduced to compensate for the addition of the interface lines. Finally, cables L12, L14 and L34 interface the two subsystems that run on a separate rack as shown in Figure 5.17.

Experimental Arrangement

The practical performance of the SWT hardware implementation is assessed in a hardware-in-the-loop configuration, in which the DSP that runs the algorithm emulates the operation of a protection relay by exchanging information with the HVDC grid designed within the DRTS. The experimental arrangement and the utilised hardware components are illustrated in Figure 5.18.

The DSP receives analogue DC voltage measurements at the relay point (shown as R in Figure 5.17) from an output channel provided by the analogue output card of the DRTS. The single-ended input signals are scaled down to fit the DSP operating

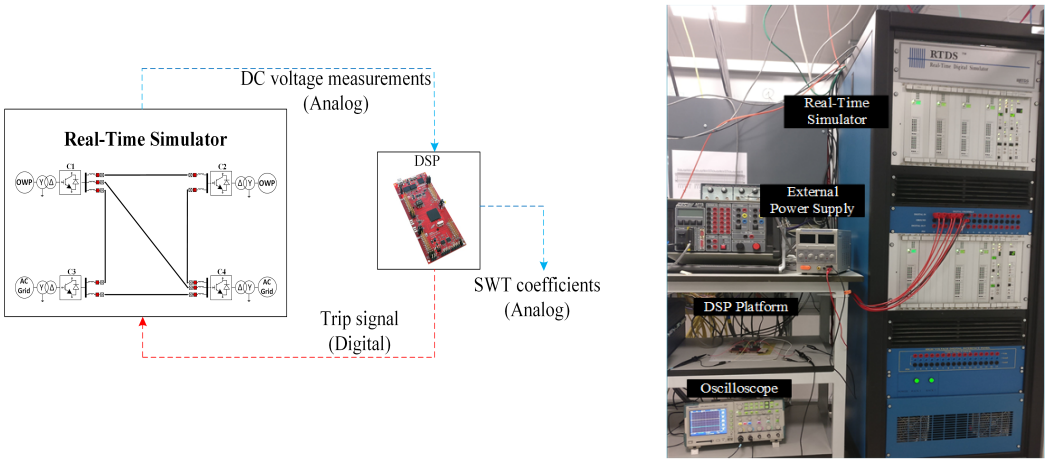


Figure 5.18: Test platform arrangement and hardware components.

range (0-3.3 V) and are sampled by the ADC module with 12-bit resolution. When an internal DC fault is detected, a digital trip signal is generated from a DSP DAC module and is sent to a digital input port of the DRTS. The signal is used to trigger the operation of the HVDC breaker next to relay R. The hardware module receives the measurements at 20 kHz and is powered by an external power supply (3.3 V). Moreover, the calculated SWT coefficients are sent to an analogue output channel of the DSP to enable real-time monitoring of the protection scheme output.

Using the DRTS network arrangement presented in the previous paragraph, the maximum sampling frequency is determined by the main time step and hence due to the use of 50 μs as the main step, 20 kHz is the maximum rate that may be achieved. An alternative approach will be introduced later for the validation of the proposed SWT-based protection solution for up to 100 kHz sampling frequency.

5.5.2 Functional Testing of SWT Implementation

This subsection aims to perform functional testing of the hardware module running the SWT algorithm and to validate the algorithm's proper operation. Towards this aim, many test cases for various DC faults have been performed, and one representative example is provided here to illustrate the correct operation of the SWT implementation. Therefore, a PTP fault with R_f=30 Ω is applied at the end of the protection zone of relay R, i.e. location F1 in the HVDC grid of Figure 5.17. The voltage measurements from DRTS are recorded, stored and directly loaded to the DSP module for playback simulation in order to investigate the hardware operation without any external effects (e.g ambient noise, failure of communication with DRTS, loss of samples etc.).

Figure 5.19(a) shows the voltage measurements (U_R) provided to the DSP during the first few ms of the DC fault and Figures 5.19(b) and 5.19(c) illustrate the detail

and approximation coefficients for all three decomposition levels, respectively. Solid lines correspond to the calculations of the hardware module (denoted as D_j and A_j), and the theoretical coefficients (denoted as Dj' and Aj') which are calculated using the MATLAB wavelet toolbox are shown with dashed lines. The wavelet coefficients are obtained using *sym4* as the mother wavelet

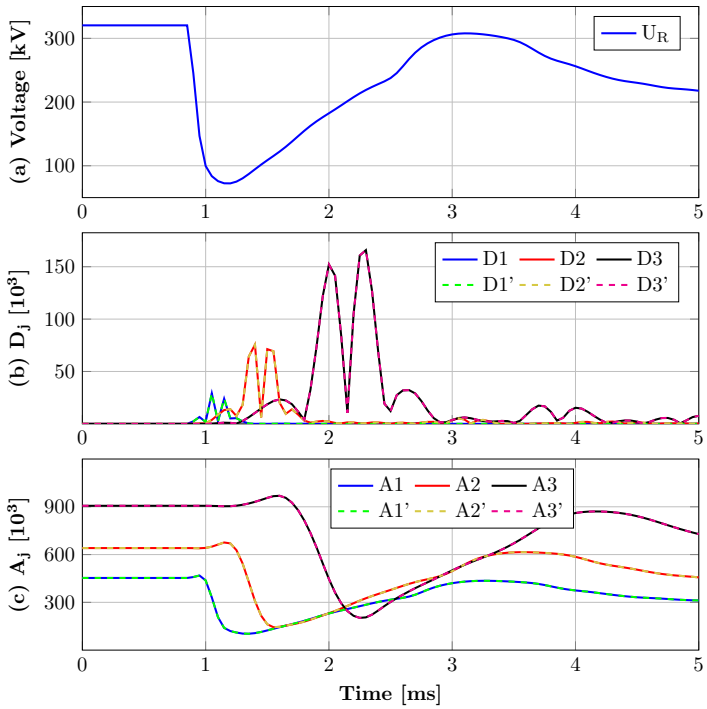


Figure 5.19: Validation of SWT implementation: (a) DC voltage measurements for an internal fault at location F1 with R_f=30 Ω, (b) calculated and theoretical detail coefficients, and (c) calculated and theoretical approximation coefficients.

The results indicate identical matching between theoretical and calculated SWT coefficients thus validating the proper operation of the DSP module. Figure 5.19 also highlights that as the level increases, the response of the algorithm becomes slower due to the greater filter lengths. This confirms the previous argument that for high-speed operation of HVDC grid protection, lower decomposition levels are preferred.

Wavelet decomposition level and mother wavelet have a significant impact on the real-time implementation of SWT both in terms of computational workload and DC fault detection speed. To investigate this impact and the capability of the hardware module to perform the SWT algorithm for longer wavelets, the same internal fault is applied repeatedly for different wavelets and levels. Table 5.6 shows the DC fault detection time in terms of the required number of main timesteps (50 μs in this case) for different wavelets with filter length ranging from 6 to 18 coefficients. For the purposes of this stundy, the fault detection time is defined as the number of timesteps it takes

for the detail coefficient to reach 30% of its maximum value. The use of timesteps instead of operation time for measuring fault detection time is chosen since in fact, the speed of the algorithm is always a fixed multiple of the timestep used. Furthermore, the operation time is dependent on the sampling rate (length of timestep) to which it is inversely proportional.

Table 5.6: Detection time for different mother wavelets and levels.

Mother Wavelet	Filter Coefficients	Detection Time [Δt] Level 2	Level 3
db3	6	5	14
db5	10	11	29
db7	14	15	39
db9	18	19	50
sym3	6	5	14
sym5	10	14	31
sym7	14	17	41
sym9	18	24	52
coif2	12	14	35
coif3	18	23	55
bior2.2	6	7	15
bior2.4	10	13	29
bior2.6	14	19	43

The results demonstrate that the hardware module can successfully perform the calculations associated with SWT algorithm within the timestep without loosing synchronisation even when longer high-pass and low-pass filters are used. Generally, as the filter length increases, the fault detection time rises. It is worth noting that this analysis only aims to validate the performance of the algorithm for different decomposition levels and wavelets without aiming for optimised protection performance in each case. The analytical approach for selecting the WT parameters and the optimised SWT-based non-unit protection algorithm is validated in the next subsection.

5.5.3 Validation of SWT-based HVDC Grid Non-unit Protection

To further corroborate the results and to evaluate the practical feasibility of the SWT-based non-unit protection method proposed in Subsection 5.3.4, dynamic validation based on hardware-in-the-loop simulations is performed in this subsection. In order to test the method for applications with increased demands in sampling frequency requirements, Cable L13 is modelled on a GTFPGA unit allowing the cable to be executed in the small timestep. Since only one GTFPGA unit is available in the current DRTS set-up in the laboratory facilities, it is possible to solve only one cable at such

low time resolution. Therefore, for Cable L13, DC voltage measurements are captured in the small-timestep network and provided to the hardware module at a rate of 100 kHz. Since the HVDC grid model in RSCAD has the same parameters with the model used in Section 5.4, the relay settings (SWT parameters and thresholds) are those cited in Table 5.4. In the conducted real-time simulation studies, special emphasis is paid on the method's performance in terms of speed, dependability (i.e. rate of successful operations), selectivity and security. These tests are selected in order to complement the findings of the offline simulation studies and to confirm the increased selectivity which is the main benefit of the SWT-based non-unit protection solution.

Speed and Dependability Tests for Internal Faults

To asses the operation speed and dependability of the proposed method, internal faults are applied repeatedly at various distances along cable L13. The mean speed of the algorithm for five repetitions at each fault location is evaluated and presented in Figure 5.20(a) when both solid DC faults (R_f≈0 Ω) and highly resistive faults (R_f=500 Ω) are applied. The operation time is measured as the time it takes from travelling wave arrival to the relay location until a trip signal is sent to the DCCB next to relay R. Moreover, the number of successful operations are recorded to check the dependability of the algorithm. Similarly, Figure 5.20(b) displays the speed or operation time when the 200 km cable L13 is replaced with a 350 km cable with the same parameters. In this case, the third wavelet decomposition level and wavelet *db*5 are derived from the analytical approach.

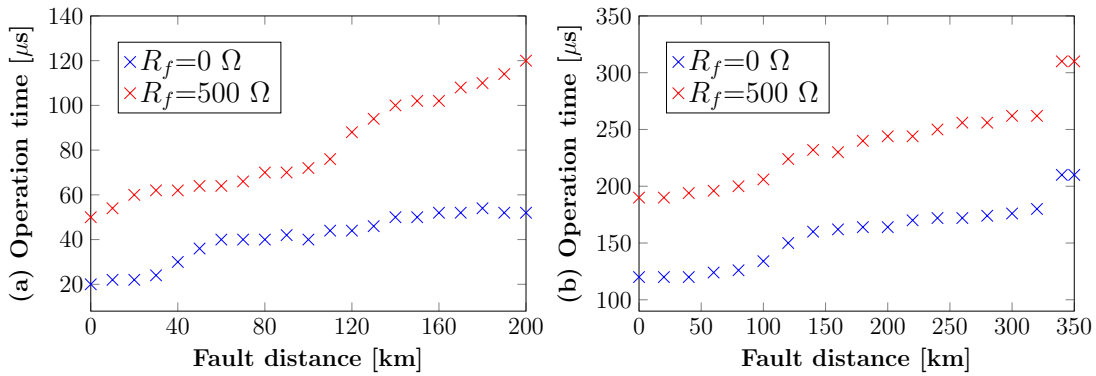


Figure 5.20: Speed of protection algorithm for different fault distances when length of cable L13 is (a) 200 km, and (b) 350 km.

The results demonstrate the high-speed operation of the SWT-based method. For the 200 km cable, solid DC faults are detected within 20-50 μs for all fault locations, whilst highly-resistive faults are detected within 50-120 μs. As a consequence of the use of the third decomposition level by the hardware module for the 350 km cable,

an increase in the fault detection speed of the algorithm can be observed from Figure 5.20(b). In detail, the operation speed varies between 120-210 μs and 190-310 μs for solid and highly resistive DC faults, respectively. Nevertheless, the algorithm retains its high-speed performance, and the speed deterioration is offset by the enhanced protection margin that is bestowed by the third level. In addition, the algorithm has been found to be 100% dependable as all applied internal DC faults have been successfully detected and discriminated. It is worth noting that the sudden increase of operation time observed in a few cases (e.g. between 320 and 340km in Figure 5.20(b)) is attributed to the mathematical operations for the calculation of SWT coefficients.

Selectivity and Security Tests

The performance of the real-time implementation of SWT in selectively discriminating internal DC faults from external faults in HVDC grids is investigated in this section. At the same time, the security of the method in terms of remaining stable under external fault conditions is assessed. For direct comparison with the offline simulations, a highly resistive PTP internal fault is applied at location F1 (R_f=500 Ω) and a solid PTP external fault at location F2 behind the DC reactor.

After numerous repetitions of both DC faults, the algorithm has been found to maintain its security and the hardware module generates a trip signal only for internal faults. An example is shown in Figure 5.21 that shows the fault voltage profile, the SWT coefficients and the trip signal for the internal fault F1. The SWT coefficients rise significantly above the threshold and hence, a DC fault is successfully detected and a trip signal is generated. The method generates a trip signal 120 μs after the fault wave reaches the terminal, which is consistent with the results shown in Figure 5.9, thereby further corroborating the offline simulations.

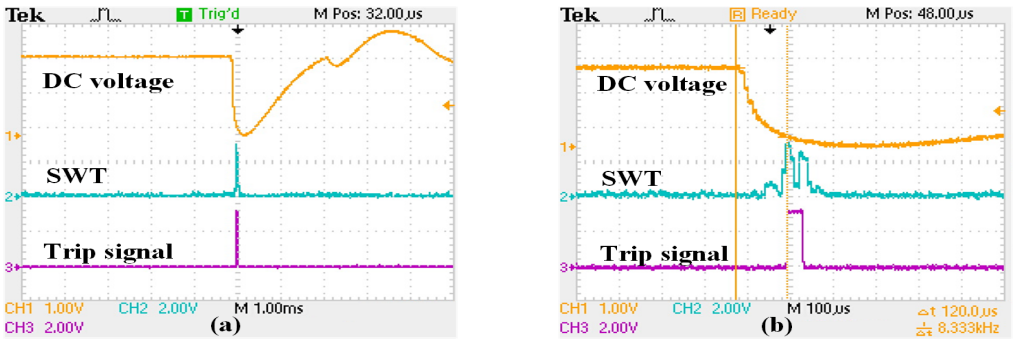


Figure 5.21: Real time simulation results for the internal fault F1: (a) overall view, (b) zoomed view.

To demonstrate the closed-loop operation and the successful coordination of the proposed method with the DCCBs that are embedded within the simulated system, the

pole currents i_{dc13p} and i_{dc13n} are shown in Figure 5.22(a). The current measurements are obtained through the RSCAD RunTime module of the DRTS. For simplicity, the digital trip signal that is generated by the DSP is used to trigger the operation of both positive and negative pole breakers of Cable L13. Moreover, the tripping signal (denoted as *BrkTrip*) and the breaker operation signal (denoted as *BrkOp*) are also captured via the DRTS and the results are shown in Figure 5.22(b). It can be seen that the fault is detected very early in the fault current rising stage. Subsequently, the DSP trip signal is received by the DRTS resulting in the operation of the breaker (3ms operation time) and in the successful fault current interruption.

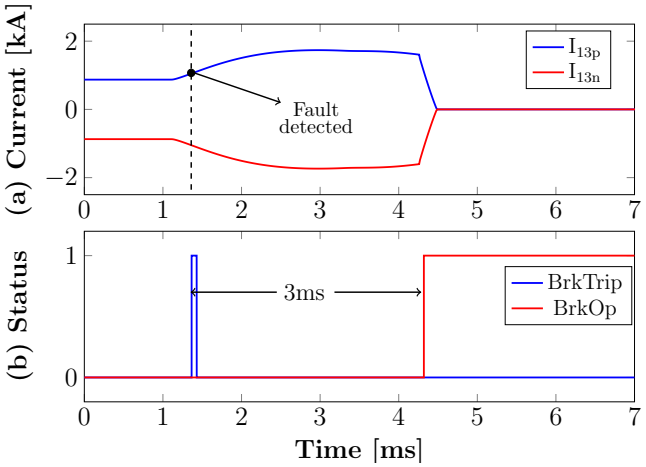


Figure 5.22: Fault current signatures during fault detection and interruption process for the internal fault F1.

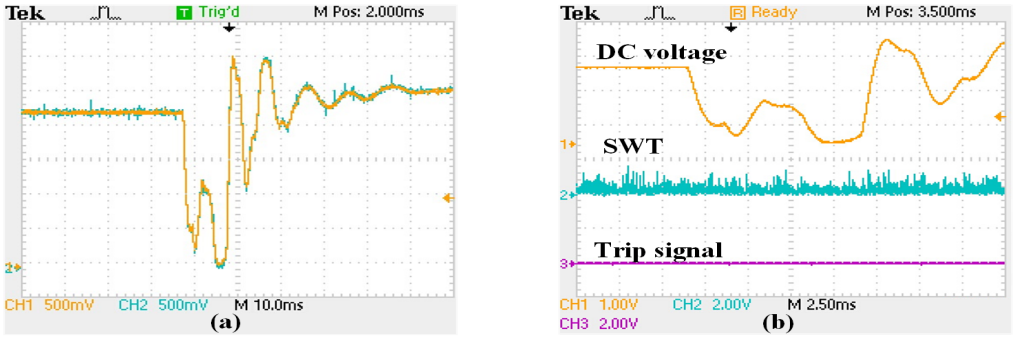


Figure 5.23: Real time simulation results for the external fault F2: (a) noise impact on measured voltage, (b) protection scheme response.

Figure 5.23 displays example results for an external fault at F2, where the voltage measurements are contaminated with noise (Figure 5.23(a)) in order to test the performance of the method in a noisy environment. Figure 5.23(b) demonstrates that the protection method does not react to the external fault, thus validating the capability

of the method to remain stable under external faults (security).

5.6 Summary

In this chapter, a fast-acting non-unit protection scheme for detecting and discriminating DC faults in HVDC grids based on wavelet transform has been presented. A generalised analytical approach, adaptable to any HVDC grid topology has been developed for deriving the main WT design parameters based on frequency domain analysis of the fault voltage transfer functions that reveals significant traits in appropriate frequency bands, which in turn are exploited for differentiating between internal and external faults. In detail, the optimum wavelet decomposition level, mother wavelet and protection threshold are flexibly derived analytically without the need for extensive offine simulations. The methodology is applied for each relay separately considering the prevailing local system conditions and grid parameters with the aim to achieve general applicability and the highest performance of the method, especially in terms of speed and selectivity. SWT has been proposed amongst the WT variants to yield the maximum benefits for HVDC grid non-unit protection.

Offline simulations conducted using a detailed 4-terminal HVDC grid modelled in PSCAD/EMTDC demonstrated the effectiveness of the proposed method, and it has been found that the scheme can provide fast, reliable and selective protection even against highly-resistive DC faults. Further analysis demonstrated robustness against external disturbances and immunity against noise, while a sensitivity analysis revealed that the method can be executed in lower sampling rates (i.e. 10 kHz).

Dynamic validation of the proposed SWT-based non-unit protection algorithm has been performed with the use of a real-time digital simulator and a low-cost hardware prototype, which are combined to form a hardware-in-the-loop configuration. An efficient SWT algorithm has been implemented based on discrete convolution and the practical feasibility of the approach has been validated using a DSP to execute the algorithm and emulate the operation of a HVDC protection relay.

The real-time simulations under various realistic conditions have confirmed the reliable operation of the protection algorithm and its enhanced performance in terms of dependability, speed, security and selectivity, while considering data acquisition issues and the computational aspects of the technique. It is worth noting that the algorithm was successfully executed at the relatively high sampling rate of 100 kHz and that no overruns were noticed. The results obtained in a low-cost relay prototyping environment provide a high level of confidence that the proposed method is effective, practical and cost-effective despite the small available scale for voltage conversion of the deployed hardware and the presence of ambient noise in voltage measurements.

Chapter 6

DC Fault Management Strategy for Continuous Operation of HVDC Grids based on Customised Hybrid MMCs

Successful deployment of HVDC grids necessitates effective DC fault handling strategies, which can minimise the severe consequences caused by DC faults on the AC and DC side of the HVDC grids. It has been identified in Chapter 3 that in HB-MMC based HVDC grids the power and voltage recovery times following the occurrence of DC faults are in the order of a few hundred milliseconds when fast and expensive hybrid DCCBs are utilised to isolate promptly the faulted zone. Therefore, this chapter investigates the enhanced DC fault performance of the Customised Hybrid Modular Multilevel Converter (CH-MMC), in which a limited number of full-bridge sub-modules is added into the arms of the conventional MMC in an effort to significantly extend the timespan between fault inception and fault clearance, thus allowing the use of relatively slow and cheaper mechanical DCCBs. By exploiting the merits of the CH-MMC, a novel dedicated DC fault handling strategy for CH-MMC based HVDC grids is proposed, which enhances the fault resiliency and security of HVDC grids for pole-to-pole faults. Moreover, the developed strategy guarantees the continuous operation of the grid during pole-to-ground DC faults, including full reactive power provision from the converter stations. The performance of the strategy is demonstrated using comprehensive electromagnetic transient simulation studies conducted on an illustrative four-terminal meshed HVDC grid through a range of scenarios with different fault current limiting inductors and DC circuit breaker operation times.

6.1 Motivation

As with any developing technology, the HVDC grid concept has its challenges, with the requirement for sufficient DC fault ride-through capability being the most prominent. It has been pointed out in Chapter 3, that when a DC short-circuit fault occurs in a HVDC grid, the distributed cell capacitors of the commonly used HB-MMC tend to contribute currents to the DC fault prior to converter blocking, while further current stresses are induced on the converter semiconductor devices by the additional distributed capacitors of the DC lines. Moreover, pole-to-ground DC faults can cause severe voltage stress on insulation of the non-faulted DC pole of a symmetrical monopole transmission line, and expose converter transformers to significant DC offsets.

Fault management strategies for HVDC grids primarily rely on the use of AC circuit breakers, DC circuit breakers or fault blocking converters. The use of ACCBs for fault clearance in HVDC grids is an economic and simple approach, which has been discussed in [154,155], where the AC grid fault current contributions are eliminated using ACCBs. Subsequently, when DC fault currents drop to zero, fast disconnectors are used to isolate the faulty DC line/cable. Nevertheless, these approaches lead to de-energisation of the DC grid and the post-fault recovery process may take several hundreds of milliseconds, which is not suitable for critical power corridors.

The second option is to incorporate fast acting DCCBs at all line ends of the HVDC grid. Hybrid DCCBs in conjunction with DC fault detection and discrimination methods have been extensively investigated for fast and selective isolation of the faulted line [141, 165, 184, 186]. In addition, coordination of the HB-MMC with hybrid DCBBs has been proposed in [202, 259], where the HB-SMs are immediately bypassed after DC fault detection in an effort to suppress the DC fault current and support the DCCBs. The main shortcoming of the above solutions is that hybrid DCCBs require designs with large footprint and high capital cost. Alternatively, mechanical DC circuit breakers can be used for fault isolation in HVDC grids at the expense of increased breaking speed but larger DC inductors are required [67, 77].

A cost analysis in the PROMOTioN project for offshore HVDC grids has demonstrated that the cost associated with DCCBs can be in the range of 5-9% of the total system cost [260]. It has been shown that the reduction in cost when using mechanical DCCBs instead of hybrid DCCBs is in the order of 15-20% per DCCB unit. It can be argued that as the size of HVDC grids increases (and hence, the number of DCCB units) the total cost reduction in absolute monetary terms decreases significantly when mechanical breakers are utilised. Moreover, it was highlighted that the volume and the weight of the DC reactor and the surge arresters used per mechanical DCCB unit are quite significant and that the cost rises for higher DC reactor size (as does its as-

sociated energy to be dissipated through the SAs). Consequently, the overall cost per mechanical breaker can be further decreased if the reactor size is reduced.

An alternative method for addressing HVDC grid vulnerability to DC faults is to use converters with fault current blocking capabilities, such as the FB-MMC [153, 261]. Unlike the HB-SMs, FB-SMs can recreate any DC voltage the DC fault may present at its DC terminal if the bipolar capability of the FB-SM is fully exploited, thus, providing greater controllability during DC faults. Fault management strategies for multi-terminal HVDC grids based on FB-MMCs have been developed using mechanical DCCBs [261, 262], or DC high-speed switches [263]. Both strategies can control fault currents and facilitate continuous operation with limited periods of power interruption.

Moreover, the conventional Hybrid MMC (H-MMC) that employs equal number of HB-SMs and FB-SMs in each arm, has been proposed to offer improved DC fault ride-through capability at reduced semiconductor losses than the FB-MMC [264]. Other hybrid topologies with similar functionality, which combine HB-SMs with FB-SMs or other SM types have also been proposed [265–267]. A fault management strategy based on the H-MMC for HVDC grids has been proposed in [243], which explores the capability to control either the converter current or the line current to clear the DC fault with limited power interruption. Despite the fault current limitation capability, the increased investment and operational costs and the higher conduction losses rarely justify the additional functionalities offered by the FB-MMC and H-MMC. It is noteworthy that the previously mentioned PROMOTioN report [260] demonstrated that when a 4-terminal HVDC grid is considered, the additional capital expenditure of the FB-MMCs (with regards to HB-MMCs) exceeds by approximately 25% the total cost associated with all mechanical DCCBs in the system (eight units protecting four cables).

To achieve an adequate, cost-effective solution for improved security of supply in hybrid AC/DC grids, an alternative approach that relies on converters with partial DC fault tolerant capability and less expensive DCCBs is required [268]. Therefore, this chapter presents a fault management strategy for handling DC faults in HVDC grids using the bespoke design of the Customised H-MMC (CH-MMC), in which the number of FB-SMs represents 25% of the total converter SMs. It has been found that the 25% ratio is sufficient to block half of the nominal DC voltage thus, enabling the strategy to achieve continuous HVDC grid operation during pole-to-ground faults, in which full controllability of the converters is maintained. For pole-to-pole faults, the proposed solution can significantly improve the DC fault survival of HVDC grids. The main contributions of this chapter are the following:

- Development of a DC fault management strategy (FMS) for HVDC grids that employ CH-MMCs with partial fault tolerant capability in order to extend the

time frame for DC fault clearance to levels compatible with mechanical DCCB operation times. This is achieved through the substantial suppression of the arm, AC and DC-side fault currents, leading to further reduction in the maximum current breaking capacity of the DCCBs. Furthermore, when the FMS is adopted, the required current-limiting role of series inductors is significantly reduced. The overall relaxation of DCCB requirements indicates that less expensive DCCBs can be used as a result of the proposed FMS.

- Through quantitative studies and qualitative considerations, it is shown that the CH-MMC leads to enhanced station and system wide performance. The CH-MMC with 25% ratio provides practical trade-offs that prioritise extension of fault clearance and high converter efficiency. At the same time the over-currents and over-voltages exerted on the semiconductor switches and SM capacitors as a result of PTP DC faults remain within tolerable levels.

- Rigorous simulation studies on an illustrative meshed HVDC grid, with detailed converter control and protection systems included, confirm the suitability of the proposed FMS in handling PTG and PTP DC faults.

6.2 Customised Hybrid Modular Multilevel Converter

The basic idea behind the CH-MMC topology with a limited number of FB-SMs has already been presented in [268], where it is shown that a 15-25% ratio of FB-SMs can limit the fault currents during pole-to-pole faults in a simplified point-to-point system. The concept is further developed in this work by extending the use of CH-MMCs in HVDC grids and developing an appropriate fault management strategy towards achieving enhanced security and resiliency against both PTP and PTG faults. In this section, the circuit topology and it associated control system that was developed and used for the work in this chapter are subsequently presented in detail.

6.2.1 Fundamentals and Circuit Topology

Figure 6.1 shows a generic diagram of the CH-MMC topology with asymmetrical ratio of FB-SMs and HB-SMs, in which N_{HB} and N_{FB} is the number of HB-SMs and FB-SMs per arm, respectively. The ratio of N_{FB} to the total number of SMs per arm, N, is denoted as R and is defined as:

$$R = \frac{N_{FB}}{N} = \frac{N_{FB}}{N_{FB} + N_{HB}} \tag{6.1}$$

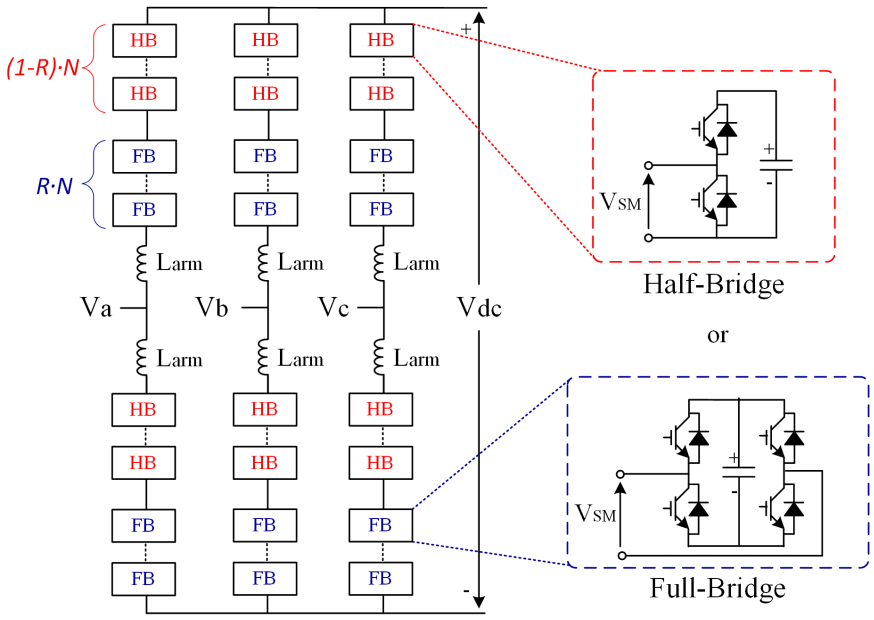


Figure 6.1: Structure of the CH-MMC topology.

Theoretically, in the CH-MMC, the ratio R could be set anywhere between 0 and 1. Nevertheless, the proposed bespoke design of the CH-MMC uses limited number of FB-SMs incorporated in its arms to extend the controllable range of DC voltage, benefiting from the combined negative voltage capabilities of the FB chain-links beyond that of the conventional HB-MMC. In this research, R=0.25 which is equivalent to 25%, is found to be beneficial for reasons that will be elaborated later. The HB and FB-SM capacitors are designed to have the same rated voltage V_{SM} as shown by:

$$V_{SM} = \frac{V_{DC}}{N} = \frac{V_{HB}}{N_{HB}} = \frac{V_{FB}}{N_{FB}} \tag{6.2}$$

where V_{DC} is the rated pole-to-pole DC voltage and V_{HB}, V_{FB} are the blocking voltages of HB and FB chain-links, respectively. For ease of explanation in the rest of the section, subscript j is used for the phase index (i.e. $j = a, b, c$) and k refers to upper and lower arm (i.e. $k = u$ for the upper arm and $k = l$ for the lower arm). Taking the upper arm as an example, the arm voltage for any phase j of the CH-MMC is given by:

$$V_{j,u}(t) = \frac{1}{2} V_{DC} \cdot (M_{AC} cos(\omega t + \delta_j) + m_{DC}) \tag{6.3}$$

where M_{AC} and m_{DC} are the AC and DC modulation index, respectively. The component M_{AC} is related to the magnitude of fundamental AC voltage and it varies in the range $0 < M_{AC} < 1$. The m_{DC} component reflects the extent at which the customised hybrid MMC can achieve operation over a wide range of DC voltages, exploiting the

bipolar output voltages of the FB-SMs. The minimum value of the DC modulation index depends on R and is given by:

$$m_{DC-min} = 1 - 2 \cdot R \tag{6.4}$$

The general relationship that describes the DC voltage range in which the CH-MMC retains controllability for a given R is

$$1 - 2 \cdot R \leq V_{DC}^{pu} \leq 1 \tag{6.5}$$

Hence, the CH-MMC can synthesise the AC voltages imposed by the AC grid as long as the DC link voltage remains within the range defined by the above inequality.

6.2.2 Converter Control

Figure 6.2 shows the control system of the CH-MMC with asymmetrical blocking voltages of the HB and FB chain-links developed for the work of this chapter. The control system consists of DC voltage or active power, and AC voltage or reactive power controllers in the outer loops along the d- and q- axes. The standard vector control is employed in the inner current loops that regulate positive and negative sequence currents, and define the AC components of the modulation functions of the arms. Nearest level modulation is used to generate the IGBT firing signals [50].

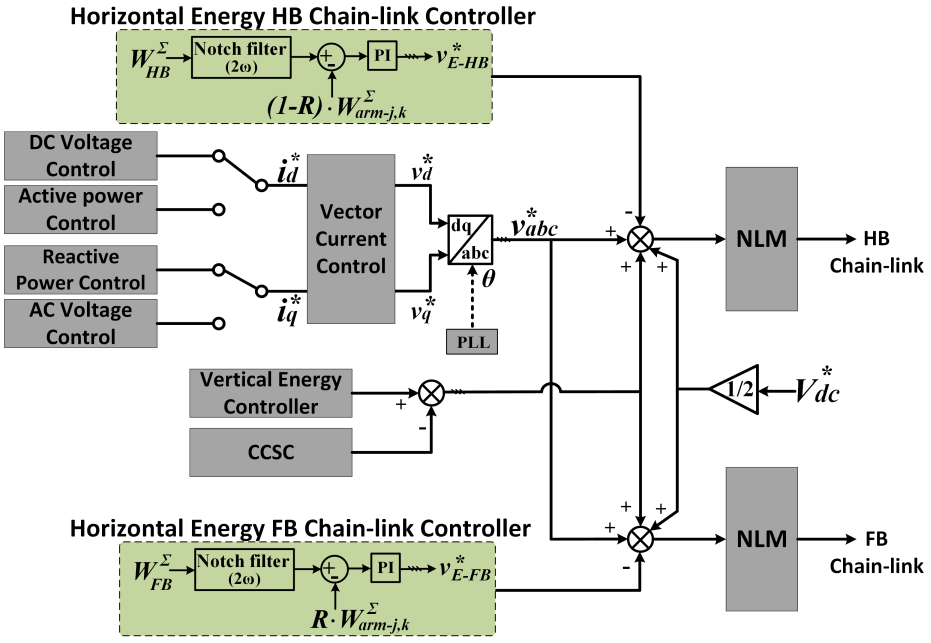


Figure 6.2: Control system of the CH-MMC.

The employed per phase circulating current suppression controllers (CCSC) modify the modulation index in an effort to suppress the second-order current harmonics from the converter arms [49, 50]. These controllers dominantly inject small second-order harmonic components into the modulation functions of the phase-legs to suppress the circulating currents, which largely contain second-order harmonic currents.

The horizontal and vertical energy balancing controllers modify the DC and AC components of the modulation functions for the HB and FB chain-links. The conventional implementation of vertical energy controller, which ensures the upper and lower arms of each phase-leg have the same total average capacitor voltage, is adopted from [49]. The per phase horizontal energy controllers ensure that all three phase-legs have the same mean DC voltage to prevent DC circulating currents between the legs.

In the CH-MMC with asymmetrical ratio of HBs and FBs (e.g. 75% HB-SMs and 25% FB-SMs), explicit horizontal energy controllers are required to ensure correct voltage or energy sharing between the FB and HB chain-link of each arm. These controllers primarily introduce a small DC component into the modulation function of the HB and FB chain-link of each arm. Typically, the set-point for the per phase horizontal controller defines the total arm blocking voltage or energy. Fundamentally, the necessary condition for SM capacitor voltage balancing is that the energy exchange between the SM capacitors of the HB and FB chain-links, and both chain-links with the AC side, must be zero as described in (6.6) and (6.7).

$$E_{HB_{j,k}} = \int_0^T \left(m_{HB} \cdot I_{arm_{j,k}}(t)\right) dt = 0 \tag{6.6}$$

$$E_{FB_{j,k}} = \int_0^T \left(m_{FB} \cdot I_{arm_{j,k}}(t)\right) dt = 0 \tag{6.7}$$

The DC offset of the modulating signal m_{HB} and m_{FB} of the HB and FB chain-link is manipulated in order to ensure that the HB and FB chain-links exchange zero net energy or active power with the AC side. Modulation index m_{HB} and m_{FB} are adjusted according to the SM energy as shown in (6.8) and (6.9).

$$W_{HB_{j,k}} = \frac{1}{N_{HB}} \sum_{n=1}^{N_{HB}} \frac{C_{SM-HB} \cdot V^2_{SM^n_{HB_{j,k}}}}{2} \tag{6.8}$$

$$W_{FB_{j,k}} = \frac{1}{N_{FB}} \sum_{n=1}^{N_{FB}} \frac{C_{SM-FB} \cdot V^2_{SM^n_{FB_{j,k}}}}{2} \tag{6.9}$$

where C_{SM-HB} and C_{SM-FB} is the capacitance of an individual HB-SM and FB-SM, while $V_{SM^n_{HB}}$ and $V_{SM^n_{FB}}$ is the voltage of the n^{th} HB-SM and FB-SM, respectively.

6.3 HVDC Grid Topology

The meshed HVDC grid illustrated in Figure 6.3 will be used to assess the performance of the proposed fault management strategy when CH-MMCs are used. The test system of Section 3.7 is employed, in which the converters are replaced with CH-MMCs with asymmetrical ratio of FB-SMs to the total number of sub-modules that can be set to an arbitrary value (between 0% and 100%). All converters are modelled based on extensively validated average value modelling, in which appropriate measures are taken to accurately represent the converter behaviour during the blocking state [60]. Details on CH-MMC modelling are provided in Appendix B. All converters have 350 sub-modules and the capacitance is calculated assuming the same minimum inertia constant of 30 ms (or 30 kJ/MVA) as suggested in [269].

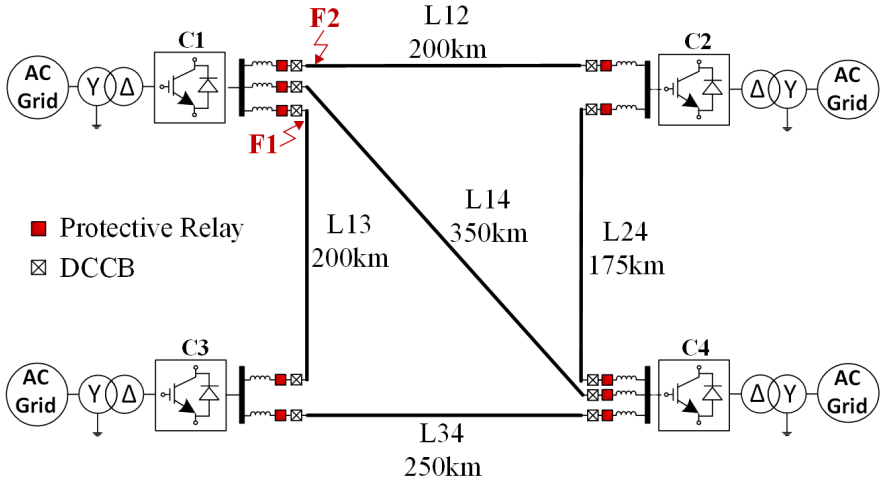


Figure 6.3: HVDC grid test system.

All transmission media are assumed to be DC cables, which are represented based on the frequency-dependent cable model available in PSCAD library, and the parameters are adopted from [81]. The network is operating at ±320 kV in a symmetric monopolar configuration, in which converters C1 and C2 are configured to control the active power, while converters C3 and C4 employ DC voltage droop control to regulate the DC system voltage. Moreover, all converters are configured to control reactive power. AC grids are modelled by a voltage source and their equivalent short-circuit impedance that comprises of a series resistance and inductance. Strong AC networks are assumed at all terminals to demonstrate the performance of the fault management strategy for high fault current levels. The main parameters of the HVDC grid and CH-MCCs with 25% ratio are summarised in Table 6.1. The converters' operating conditions are also shown in the table.

Table 6.1: System and converter parameters.

Parameter	Value
Nominal DC voltage	± 320 kV
Rated AC (line-to-line) voltage	400 kV
Short circuit ratio of AC grids	15
X/R of AC grids	10
Rated power (C1∼C4)	1000 MVA
Active power setpoint (C1∼C4)	700,700,−800,−600 MW
Reactive power setpoint (C1∼C4)	100,100,−100,−100 MVAr
Loading of L12,L13,L14,L24,L34	-90,510,280,610,-90 MW
Total number of SMs	350
Arm inductance	42 mH
Arm resistance	0.08 Ω
Total FB-SMs capacitance	125.68 μF
Total HB-SMs capacitance	41.89 μF

6.4 DC Fault Management Strategy

This section puts forward fault-ride through methods for the CH-MMC for both PTP and PTG faults, and then proceeds with the design of a comprehensive fault management strategy for CH-MMC based HVDC grids. The enhanced DC fault ride-through functionality of the CH-MMC is achieved through the customised design of ratio R in order to exploit the reverse voltage capabilities of the FB chain-links. Based on this design, a fault management strategy is developed for ensuring enhanced station- and system-wide resiliency against DC faults.

6.4.1 CH-MMC Behaviour During Pole-to-pole Faults

Pole-to-pole faults have severe consequences on the safety and operation of HVDC grid and consequently, they must be isolated as quickly as possible. It is worth reiterating that the bespoke design of CH-MMC being pursued in this chapter aims to extend the time frame for fault detection and isolation, so that effective protection coordination with slow mechanical DCCBs in the order of 5 ms to 15 ms becomes technically feasible [67, 77, 270]. The fault behaviour of the CH-MMC in this time frame for PTP faults can be divided into two stages.

Fault Current prior to Converter Blocking

This stage initiates when travelling waves induced by the fault reach the converter after a short propagation period through the transmission medium, resulting in the discharge of sub-module capacitors into the fault and causing a rapid increase of the fault current. As the converter retains controllability in this stage, equal discharge of

the SM capacitors of the arms will be observed due to the active capacitor voltage balancing algorithm. The rate at which the SM capacitors discharge is largely limited by the arm inductance and the effective DC side inductance (current limiting inductor and DC cable inductance). In the worst-case of a DC fault at converter DC terminals, the fault network can be considered as an equivalent RLC circuit as follows:

$$R = \frac{2R_{arm}}{3} + R_f, \quad L = \frac{2L_{arm}}{3} + L_{DC}, \quad C = 6 \cdot C_{arm} \tag{6.10}$$

where R_f is the fault resistance, L_{DC} is the DC current limiting inductor, R_{arm}, L_{arm} and C_{arm} are the converter's arm resistance, inductance and capacitance, respectively. The fault current flowing to the DC fault can be derived as:

$$I_f(t) = e^{-\sigma t}\left(2V_{DC}\sqrt{\frac{C}{L}}sin(\omega t) + I_0 cos(\omega t)\right) \tag{6.11}$$

where $\sigma = \frac{R}{2L}$, $\omega = \sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2} \approx \sqrt{\frac{1}{LC}}$ and I_0 is the pre-fault current. This stage lasts until the worst-case converter arm current hits the pre-set over-current threshold, or until the DC link voltage has fallen below a specified threshold.

Fault Current after Converter Blocking

This stage starts once the converter blocks, which subsequently triggers the activation of the current limiting mode. In this mode, the CH-MMC uses its FB chain-links to present increasing and opposing counter-voltages, which gradually suppress the AC side, arm and DC currents at the expense of increasing cell capacitor voltages. This mode necessitates blocking of the HB and FB chain-links as shown in Figure 6.4(a).

In the H-MMC, the total voltage formed by the series connection of all FB-SM capacitors during converter blocking is higher than the peak AC line-to-line voltage, V_{AC}^{max}, thus blocking the DC fault [264]. However, for the CH-MMC where the number of FB-SMs is suggested to be significantly less than in the H-MMC, the total reverse blocking voltage capability is less than V_{AC}^{max}. During time intervals in which any phase voltage V_{AC_j} exceeds the arm voltages, the FB chain-links in the corresponding arms of phase j conduct, and this results in the over-voltage of FB-SM capacitors. The differential equation that describes the electromagnetic transient of each phase of the CH-MMC during these time intervals is:

$$V_{AC_j}^{max} \cdot sin(\omega t) - 2V_{FB_j}^{\Sigma} = 2(R_T + R_{arm})I_j + 2(L_T + L_{arm})\frac{dI_j}{dt} \tag{6.12}$$

where R_T, L_T are the transformer leakage resistance and inductance, I_j is the current of phase j, and $V_{FB_j}^{\Sigma}$ is the total voltage of the FB chain-links of phase j. From (6.12),

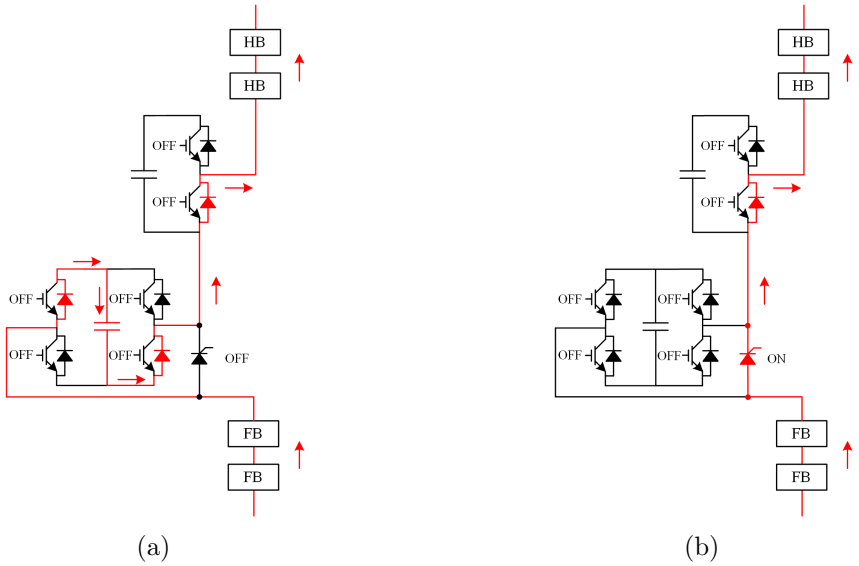


Figure 6.4: Depiction of CH-MMC arm during (a) current limiting mode, and (b) survival or fail-safe mode.

it is observed that the fault current that will be driven towards the converter from the AC grid can be controlled according to the number of FB-SMs in each arm. In detail, the lower the voltage difference between $V_{AC,j}$ and the sum of the upper and lower FB chain-link blocking voltages (and hence, the higher the ratio R), the lower the fault current. As the FB-SM capacitors charge during the conduction periods, the relative voltage difference decreases leading to further reduction of the converter current. Theoretically, when the total phase FB chain-link voltage matches V_{AC}^{max}, the fault current should drop to zero. It is worth noting that the FB chain-link blocking voltage corresponds to the total capacitor voltage per arm and can be expressed as:

$$I_j = \frac{C_{SM-FB}}{N_{FB}} \cdot \frac{V_{FB_j}^{\Sigma}(t)}{dt} \tag{6.13}$$

Accordingly, the voltage rise in the FB-SMs is determined by the magnitude of the phase current and the total capacitance of the FB-SMs, and is described by:

$$V_{FB_j}^{\Sigma}(t) = \frac{N_{FB}}{C_{SM-FB}} \int_0^t I_j dt + V_{FB_j}^0 \tag{6.14}$$

where $V_{FB_j}^0$ is the initial voltage of the FB chain-link of phase j the moment the second stage initiates. To enable the fault-ride through functionality of the converter, the capacitors should be designed to withstand overcharging for a short period of time, and for their protection, a maximum allowable limit on FB-SM over-voltage should be set, beyond which the FB-SM capacitors are bypassed using similar techniques as in

HB-SMs, e.g. dedicated thyristors [202]. In this work, the survival or fail-safe mode is activated when the worst-case arm capacitor voltage exceeds 1.6 p.u. to avoid damage from excessive over-charging of the SM capacitors beyond the safety level. In this mode, the CH-MMC resembles blocked HB-MMC, and each FB cell will be bypassed by a dedicated thyristor as shown in Figure 6.4(b). Moreover, equation (6.14) indicates that the higher the value of C_{FB} and hence, the higher the individual FB-SM capacitance C_{SM-FB}, the slower the rate of voltage increase in the FB chain-link. Consequently, another method to limit the over-voltage rate until fault clearance is to utilise capacitors of greater size. Once the fault current is cleared, all sub-module voltages will converge to their pre-fault level due to the separate employed capacitor voltage balancing control.

As shown in equation (6.13), a higher ratio of FB-SMs to the total number of sub-modules results in lower current in each arm, which in turn leads to a reduction in total fault current. To illustrate this effect, a solid PTP DC fault is applied at location F1 (as shown in Figure 6.3) on cable 13, 1 km away from converter C1 and the cable current of the faulted pole is shown in Figure 6.5(a) for different ratios (R=0,5,15,25 and 35%) of the CH-MMC, without enforcing the capacitor over-voltage limit. The current limiting inductance, L_{DC} , is set to 50 mH and the circuit breaker operation time is assumed to be t_{br}=15 ms. The fault is applied at time t=0.1 s.

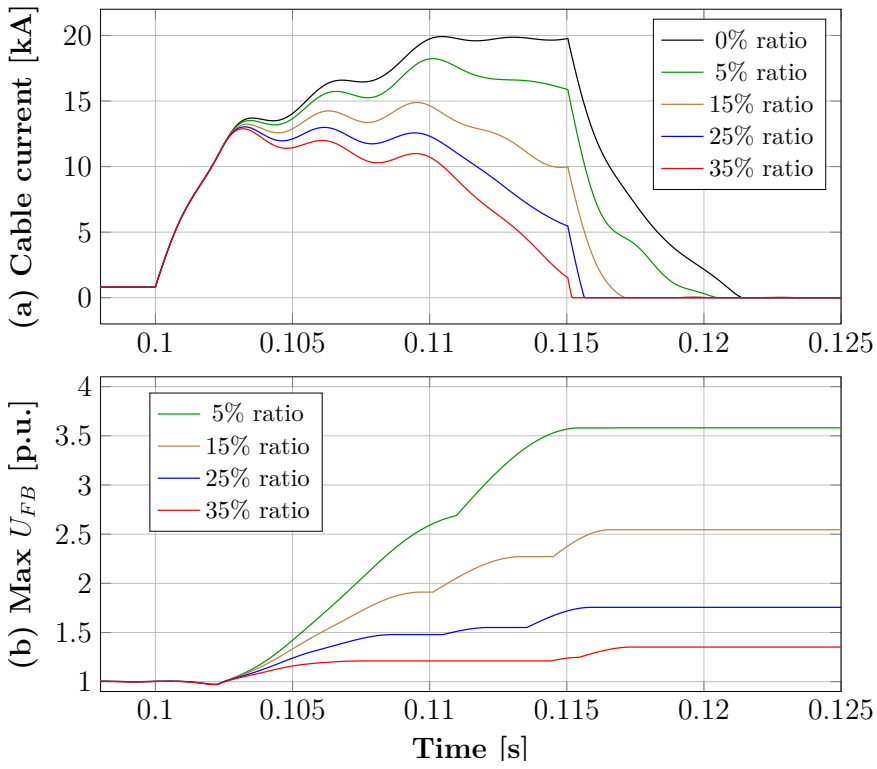


Figure 6.5: Effect of R=0,5,15,25 and 35% on (a) cable fault current and (b) maximum value of FB-SM voltages.

In the initial stage of the fault, the cable current is composed of the SMs capacitor discharge current and the current contribution from the adjacent cables. The effect of ratio R during this period is minimal and the rise of fault current is mainly determined by the DC inductor size. Around t=0.1025 s, the converter blocks, and the fault current is regulated. It is evident that in comparison with lower ratios, R=25% and R=35% lead to a more profound reduction in the fault current, which is controlled within a reasonable range until the DCCB operates at t=0.115 s.

Moreover, the maximum value of the FB-SM capacitor voltages for all arms for the entire fault duration is depicted in Figure 6.5(b) for all ratios. As the fault current flows through the FB-SMs, the capacitors continue to charge, leading to voltage increase. It is evident that ratios lower or equal to 15% lead to rapid increase of FB-SM capacitors voltage. For R=25%, even for a fault at a very short distance, an extended time window of reverse DC voltage is provided and the maximum voltage reaches 1.76 p.u. approximately 15 ms after the fault. The charging of the FB-SM capacitors is further restrained in the case of R=35%, where the voltage rises to 1.35 p.u.

Figure 6.5(a) and Figure 6.5(b) show the corresponding results of a more focused analysis of R in the range 20-30% under the same DC fault scenario. In this case, the fail-safe mode is activated when the 1.6 p.u. capacitor over-voltage limit is exceeded.

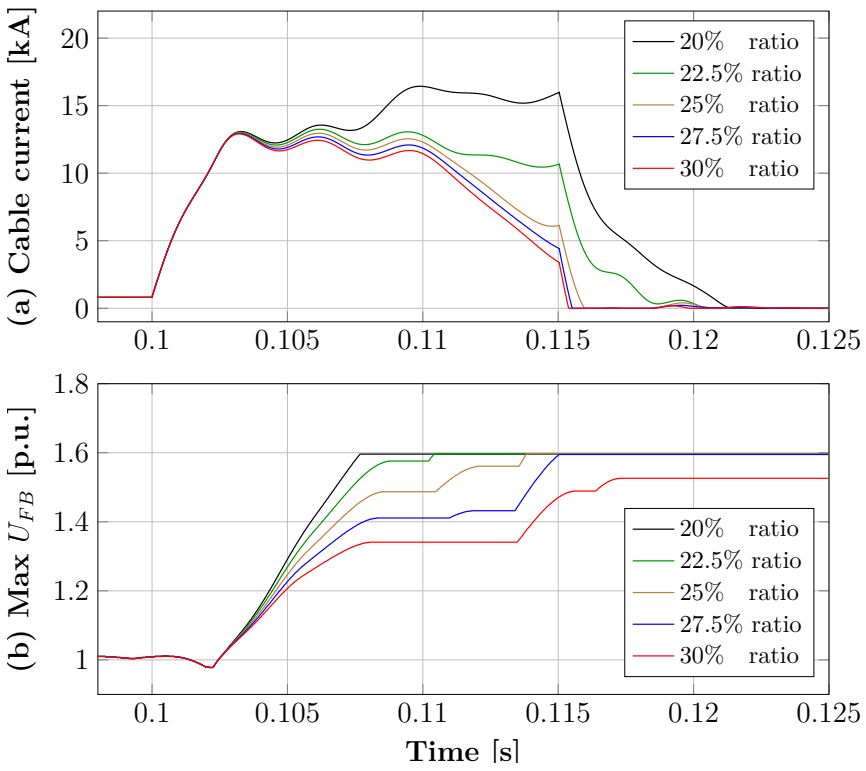


Figure 6.6: Effect of R=20,22.5,25,27.5 and 30% on (a) cable fault current and (b) maximum value of FB-SM voltages.

Figure 6.5(a) shows that the CH-MMC with R=20% fails to regulate the fault current for an extended period of time as the capacitor over-voltage limit is reached within 7.5 ms from fault inception (as seen from Figure 6.5(b)) leading to the bypass of the FB-SMs. Generally, it is evident that as the ratio increases, the time spent in the current limiting mode before transitioning to the fail-safe mode is extended. Ratios equal or above 25% can limit the fault current even after 10 ms. In detail, the 25% ratio achieves a reduction of the fault current for the entire period until the fault current is cleared, and the converter remains in the current limiting mode for 11.83 ms after fault inception. 27.5% and 30% ratios lead to similar fault currents, while in the latter case the over-voltage limit is never exceeded.

It can be argued that the significant fault current limitation bestowed by the use of at least 25% ratio indicates that the current stresses on system components are decreased and that the time provided for protection system response and fault isolation can be significantly extended; therefore, slower but less expensive DCCBs can be utilised. As a consequence of the blocking action of the converter, power transfer capability during and after fault clearance is lost, as well as the ability for ancillary services provision to the connected AC grids. Nevertheless, since the converter aims to be blocked only for a short period of time (10-20 ms) only to allow for slow mechanical DCCBs to operate, the influence on the connected AC grids can be minimised.

6.4.2 CH-MMC Behaviour During Pole-to-ground Faults

When a pole-to-ground fault occurs, the voltage of the faulted pole collapses to zero. On the other hand, the healthy pole can experience a significant over-voltage up to twice the nominal voltage. Assuming that the voltage measured on the positive and negative pole are $V_{DC,P}$ and $V_{DC,N}$ respectively, the AC voltage of phase j relative to ground, $V_{AC,j}$, can be expressed as [271]:

$$V_{DC,P} = V_{j,u} + L_{arm} \cdot \frac{dI_{arm_{j,u}}}{dt} + V_{AC,j} \tag{6.15}$$

$$V_{DC,N} = V_{j,l} + L_{arm} \cdot \frac{dI_{arm_{j,l}}}{dt} - V_{AC,j} \tag{6.16}$$

Subtracting (6.16) from (6.15) and neglecting the voltage drops in both upper and lower arm reactors yields:

$$V_{AC,j} = \frac{1}{2}(V_{DC,P} - V_{DC,N}) - \frac{1}{2}(V_{j,u} - V_{j,l}) \tag{6.17}$$

A PTG DC fault on the negative pole of will force $V_{DC,N}$ to 0 and $V_{DC,P}$ to V_{DC}, thus (6.17) becomes:

$$V_{AC,j} = \frac{1}{2}V_{DC} - \frac{1}{2}(V_{j,u} - V_{j,l}) \tag{6.18}$$

Expression (6.18) indicates that the output AC phase voltage $V_{AC,j}$ develops a DC bias of $\frac{1}{2}V_{DC}$, which exposes the converter transformer to increased voltage stresses and risk of insulation failure. An identical voltage stress would be experienced if the fault occurred on the positive pole. Moreover, this phenomenon appears regardless of transformer connection and grounding arrangement [272]. To mitigate voltage stresses on the converter transformer, maintain the nominal voltage on the healthy pole and ensure continuous operation of the HVDC grid during PTG faults, the DC voltage reference for the converter voltage controller is set to 0.5 p.u. To accomplish 50% reduced DC voltage operation during PTG DC faults, the DC components of the upper and lower arm voltage being contributed by the FB chain-links are adjusted. In this way, the minimum required number of FB-SMs to allow controlled operation at $0.5V_{dc}$ during PTG faults is 25%, as described by (6.4). Thus, the modulation functions for the upper and lower arms become:

$$m_{j,u} = M_{AC} \cdot cos(\omega t) + 0.25 \tag{6.19}$$

$$m_{j,l} = -M_{AC} \cdot cos(\omega t) + 0.25 \tag{6.20}$$

The issues that are overcome in the event of PTG faults and the benefits of using CH-MMCs with a ratio of at least R=25% in HVDC grids are as follows:

- **Healthy pole over-voltage avoidance:** The PTG voltage of the healthy pole can be maintained at nominal; hence, the risk of DC cable insulation failure is prevented, and the need for pole rebalancing is eliminated.
- **Fault current elimination.** The controlled operation at 50% of the rated DC voltage retains the ability of the converter to synthesise the full AC voltage and control active and reactive power, while also the uncontrolled AC current flow from the AC grid is eliminated. Also, the DC currents associated with the rise of the healthy DC pole voltage across the DC grid can be dramatically reduced. In cases where DCCBs of the HVDC grid are designed for interrupting fault currents originating only from PTG faults rather than PTP faults, the current breaking and energy absorption capabilities can be greatly reduced and hence use of high-speed DC switches with reduced cost and footprint is possible.
- **Mitigation of DC offset in converter transformer voltage.** In HB-MMCs, converter transformers are exposed to severe DC voltage stresses during PTG

DC faults. On the contrary, with the utilisation of the CH-MMC, the DC voltage stress on the converter transformer can be reduced to $\frac{1}{4}V_{DC}$. The DC offset can be further reduced when using a higher ratio R.

- **Continuous HVDC grid operation.** During PTG DC faults, the converter retains full control of active and reactive power exchange with the connected AC grids. Since the DC grid operates at $\frac{1}{2}V_{DC}$, it retains at least half of the rated power capability, which can lead to faster post-fault power flow restoration.

6.4.3 Proposed DC Fault Management Strategy for HVDC Grids

It has been established through the aforementioned discussions that a ratio of at least 25% achieves significant fault current limitation during PTP faults and ensures continuous converter operation during PTG faults. Therefore, to ensure both benefits, the use of CH-MMCs with at least R=25% is promoted for the proposed DC fault management strategy for CH-MMC based HVDC grids. The strategy is executed at each converter station individually and requires coordination with local protection relays. Taking converter C1 of Figure 6.3 as an example, the basic flowchart of the FMS along with the coordination scheme with the protection relays are shown in Figure 6.7. Since PTG and PTP faults require different fault handling techniques, the FMS receives information from the protection relays about whether a PTG or PTP DC fault is detected, and then activates the corresponding measures for the converter.

To detect every probable fault on any cable of the HVDC grid, protection relays are placed at both poles of each cable end. Owing to the fact that DC faults have distinctive impact on DC voltages, under-voltage is used in this chapter for fast fault detection. Protection relays monitor the DC voltage of both poles, and if the voltage falls below 90% of nominal value a DC fault is detected. If both poles are affected (in a 100 μs window) a PTP fault is detected, otherwise if only one pole is affected a PTG fault is determined.

Moreover, DC cable faults are cleared selectively to ensure continued operation of the remaining HVDC grid. Towards this aim, fault discrimination is performed by protection relays to identify the faulted cable and issue a trip command to the corresponding DCCBs, which are installed at each cable end. The HVDC non-unit protection solution of Chapter 5 can be used to offer discriminative protection at very high speed. Nevertheless, a simplified non-unit protection method based on du/dt is preferred in this chapter, in which pole voltage measurements are used with a reduced sampling frequency of 20 kHz (for simplicity). It is worth noting that du/dt is selected for illustration only, and the proposed FMS is applicable for any fault discrimination method that is employed, including unit protection techniques.

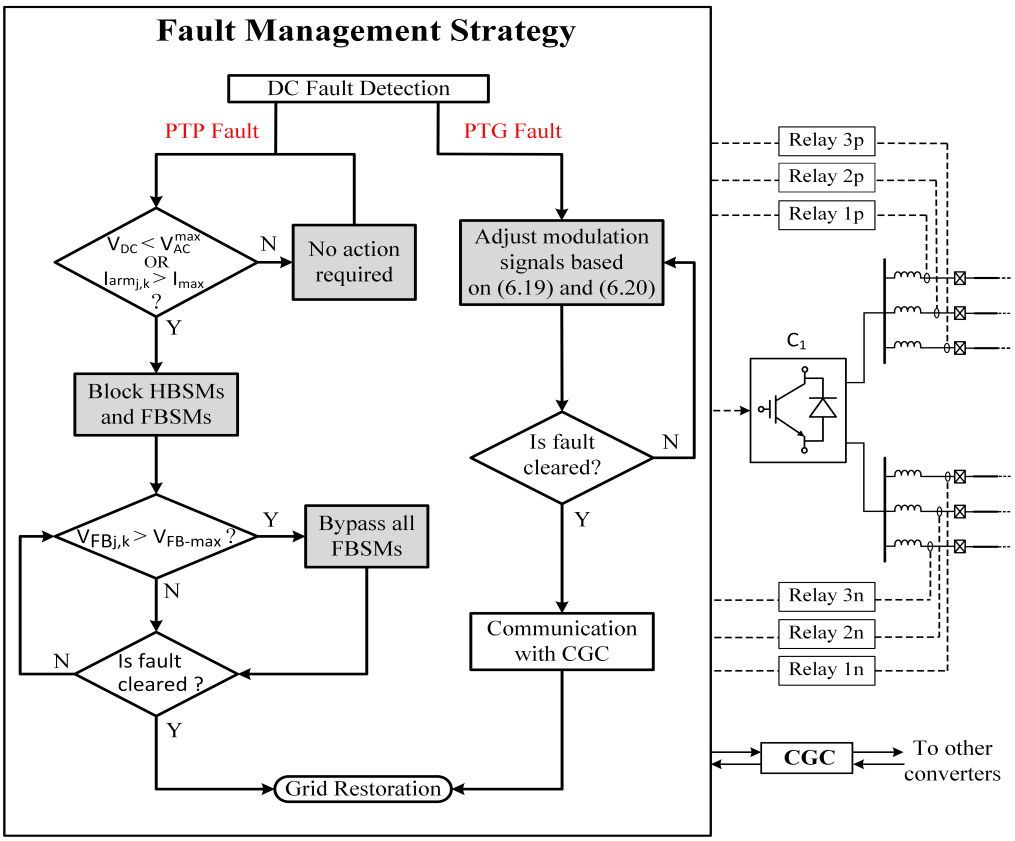
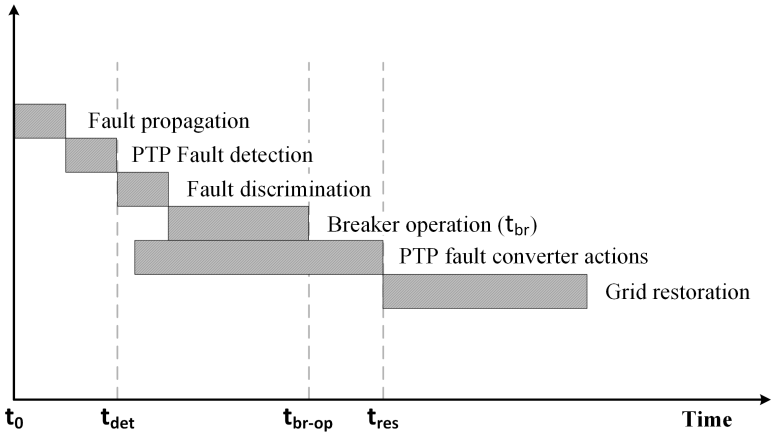


Figure 6.7: Flowchart of the proposed FMS.

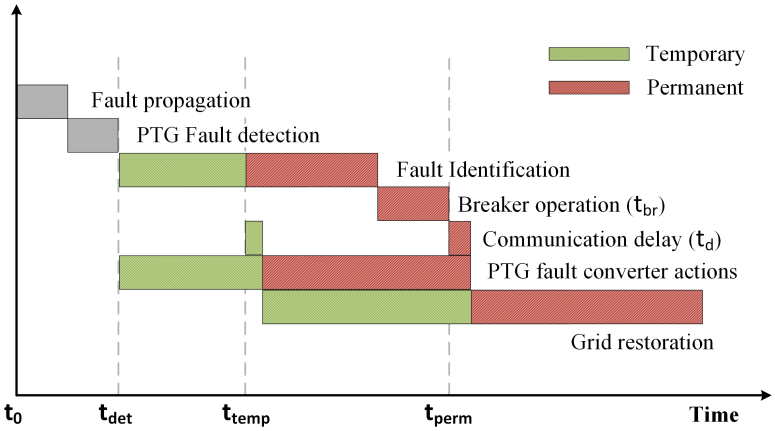
Also, a Central Grid Controller (CGC) is introduced for exchanging information between converters when required. Due to the severity of PTP DC faults and the requirement for fast fault clearance, the fault management strategy for PTP faults precludes the use of the CGC. On the contrary, in the case of a PTG fault, the CGC is employed to coordinate converter actions before commencing the grid restoration process after fault clearance. More details on the fault management strategy and the sequence of events during PTP and PTG faults are subsequently provided.

Sequence of Events for Pole-to-pole Faults

Figure 6.8(a) shows the sequence of events when the FMS is activated for a PTP fault that occurs at t_0 and starts to propagate in the HVDC grid. The fault is detected by the corresponding protection relays at instance t_{det}. Provided a PTP fault is detected, the FMS initiates when any converter arm current $I_{arm_{j,k}}$ exceeds the maximum over-current limit that is set as I_{max}=1.8 p.u., or when the DC link voltage V_{DC} falls below the peak line-to-line voltage, V_{AC}^{max}. In this way, unnecessary blocking of the CH-MMC in case of non-critical faults with limited impact (e.g. highly resistive faults) is avoided.



(a) Fault management strategy for PTP faults.



(b) Fault management strategy for PTG faults.

Figure 6.8: Sequence of events during the fault management strategy.

Following activation of the FMS for a PTP fault, the converter HB-SMs and FB-SMs will be blocked, prompting the FB chain-links to gradually recreate the reverse DC voltage as explained in Subsection 6.4.1. During this process, the voltages of all FB chain-links are continuously monitored. If any of the FB chain-link voltages exceed the maximum allowable limit V_{FB-max}=1.6 p.u., all FB-SMs of the converter are bypassed to protect the SM capacitors. When the fault is discriminated by the protective relays of the faulted cable, a trip signal is generated for the corresponding DCCBs, which trip after the operation time, t_{br}, has elapsed. The converter resumes normal operation when information is received by the corresponding relays that the fault is successfully cleared. Once the DCCBs are opened and the converter exits the strategy, grid restoration process will start, at time t_{res}. To ensure security of the FMS during PTP faults, a dead time dt=5 ms is introduced between circuit breaker operation, at t_{br-op}, and the grid restoration starting time, t_{res}. For converters in which the FMS has been activated

but are not connected to the faulted medium (discrimination of an internal fault is not a prerequisite for FMS activation), the DC fault is deemed to be cleared when time $(t_{br} + dt)$ has passed after discrimination of an external fault.

It is worth noting that fault discrimination is realised by the protection relays independently from the converter actions. Therefore, the converter may block during or after the fault discrimination stage, depending on the impact of the DC fault on converter voltage and arm currents. Moreover, the strategy can be activated for all converters of the HVDC grid or at least for the local converters (i.e. connected to the faulted medium). If blocking of only local converters is required, appropriate measures should be taken, (e.g. use of high line inductor value), for ensuring that the arm over-current or under-voltage limits of the remote converters are not violated. It should be stressed that for PTP faults, the FMS is applicable for any ratio R of the CH-MMC, while for the effective operation of the strategy during PTG faults, a ratio of at least R=25% is required.

Sequence of Events for Pole-to-ground Faults

Figure 6.8(b) shows the corresponding sequence of events when the FMS is activated for both temporary and permanent PTG faults. When the PTG fault is detected by the local protection relays, activation of the FMS is triggered at each converter terminal individually, and the modulation signals for the upper and lower arms of all grid converters are modified based on equations (6.19) and (6.20). Voltage controlling converters set DC voltage reference to 0.5 p.u., while converters that regulate active power also reduce their active power orders in proportion to the DC voltage to avoid overloading of the DC cables.

As the proposed CH-MMC design is able to retain controllability during PTG faults, the FMS remains active until the protection systems perform fault identification, (i.e. to identify whether the fault is temporary or permanent). Several fault identification techniques for HVDC grids have been proposed in the technical literature [273–275]. Therefore, for the purposes of the analysis in this chapter, it is assumed that if the fault is not deemed temporary within 180 ms $(t_{perm} - t_{det})$, then a trip command is sent to the DCCBs of the faulted medium. It is worth mentioning that this process is more relevant to OHL-based systems in which DC faults are more likely to be temporary as opposed to DC cables where faults are typically permanent.

For PTG faults, the central grid controller is utilised to ensure that all converters exit the strategy and resume normal operation almost simultaneously. The CGC receives information of when either a temporary or permanent PTG fault is cleared and then a grid restoration start signal is distributed to all converters. To account for the

communication delay between the grid controller and the converters, a conservative fixed time delay t_d=30 ms is assumed before starting the grid restoration process.

6.5 Performance of DC Fault Management Strategy

The enhanced DC fault ride-through performance of the CH-MMC and the performance of FMS during PTP and PTG faults are assessed in this section using the illustrative meshed HVDC grid of Figure 6.3. To evaluate the performance of the DC fault management strategy over a wide range of scenarios and to provide an operating envelope for the proposed strategy, several values of ratio R, current limiting inductances L_{DC}, and operating speeds of DCCBs t_{br} are tested. The selected values for L_{DC} and t_{br} correspond to typical values used in hybrid and mechanical DCCBs for HVDC grids.

Initially, a sensitivity analysis for the size of the current limiting inductance is performed and its impact on pole-to-pole fault current is investigated. Subsequently, the FMS is evaluated and the fault response of the CH-MMC based HVDC grid in terms of voltage and power recovery times is assessed and compared against conventional HB-MCC based HVDC grids. Finally, example PTP and PTG fault cases are selected and discussed including aspects related to the coordinated actions of the protection relays in an effort to further demonstrate the operation and the effectiveness of the fault management strategy for handling DC faults.

6.5.1 Impact of Series Inductor

The size of current limiting DC inductors is one of the dominant factors that determine the rate of rise of fault current, and directly affects the available time margin for protection response. To investigate this effect, 50, 100 and 200 mH DC current limiting inductors (which are commonly used values for series inductors [276]), are selected for further analysis. The maximum fault currents observed in DC cable current values are depicted in Figure 6.9, for different values of R of the CH-MMC, when a solid PTP fault is applied at location F1. This fault location has been selected due to its direct proximity with the converter (C1) and the high number of adjacent cables for increased fault current magnitudes. This study aims to reveal potential trade-offs between the ratio R of the CH-MMC, magnitude of L_{DC} and DC circuit breaker operating times. In other words, the study aims to identify potential savings in the size of minimum current limiting inductance required to enable the use of a range of existing mechanical circuit breakers, with operating times ranging from 5 ms to 15 ms [67, 77].

The observations drawn from the results in Figure 6.9 are summarised as follows:

- For R =25% and R =35%, a significant decrease in fault current is achieved when

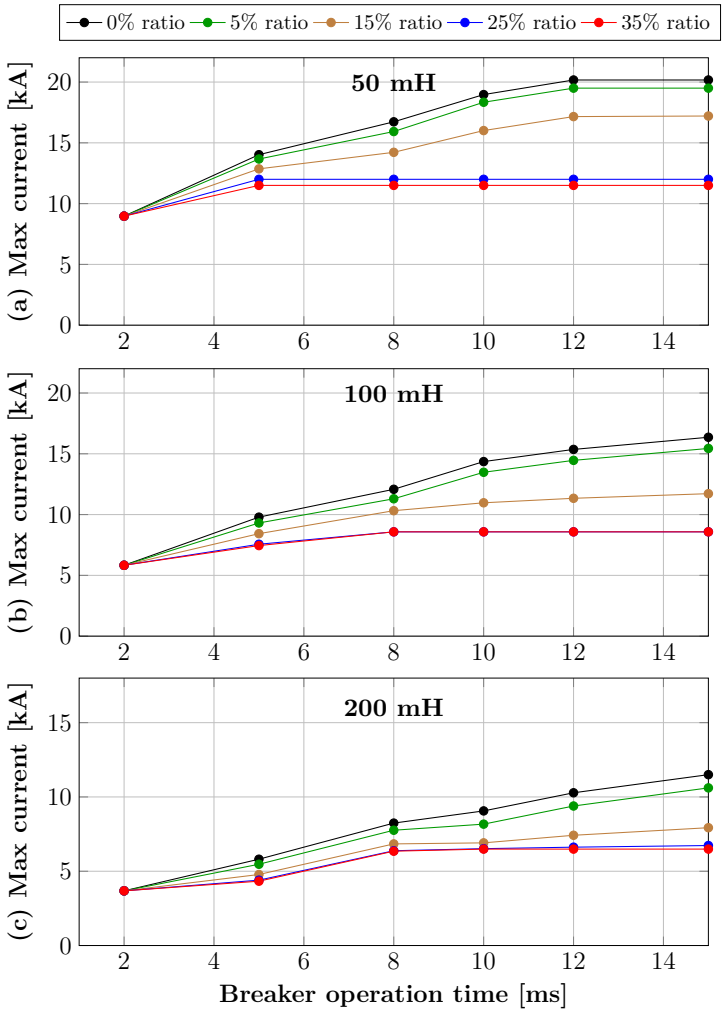


Figure 6.9: Maximum cable fault current for different R, when (a) L_{DC}=50mH, (b) L_{DC}=100mH and (c) L_{DC}=200mH

compared to R <25%.

- Compared to R=0% (i.e. typical HB-MMC), the proposed R=25% achieves a maximum reduction in peak DC fault current of 42.9%, 47.5% and 41.5% for L_{DC}=50, 100, 200 mH, respectively, when t_{br}=15 ms. Furthermore, when operating times higher than 8 ms are considered, ratios R=25% and 35% with 50 mH inductors lead to smaller fault current magnitudes than the HB-MMC with 200 mH inductors.

- The differences between R=35% and R=25% are marginal in all scenarios, and the observed current magnitudes for both ratios are almost identical for all DC circuit breaker operating times. Similar to the case shown in Figure 6.5(a), the maximum current values are observed in the early stage of the fault, i.e. within

5 ms in Figure 6.9(a) and within 8 ms for Figure 6.9(b) and 6.9(c). Afterwards, both ratios achieve successful regulation of the fault current at lower levels for an extended period of time as long as the FB-SM capacitor voltages remain below the designated limit (1.6 p.u.)

In summary, the above discussion shows that the customised current suppression capability exhibited by the FB chain-links of the CH-MMC for various R values can replace or minimise the required current-limiting role of series inductors when the proposed FMS is adopted. The reduction observed in the fault currents with the increase of R is practically meaningful as it leads to a reduction in the required DCCB current breaking capacity.

6.5.2 Fault Management Strategy Evaluation for Pole-to-pole Faults

As PTP DC faults provoke serious disruptions of power flow across HVDC grids and the surrounding AC networks, the priority is to minimise the power flow interruption by quick isolation of the faulted section; however, the cost of fast acting hybrid DCCBs to realise such an approach can be prohibitive. An alternative approach as proposed in this chapter, is to create a shielding state in which the converter terminals must contribute to minimisation of magnitude and duration of system wide power flow interruption, and facilitation of rapid resumption of power flows to pre-fault or new post-fault states. The indicators used to assess DC grid recovery from a PTP DC fault are the DC voltage and power flow recovery times. The former and the latter represent the times that DC voltage and power recover within ±5% of the nominal voltage and ±10% of the post-fault steady state power flow, respectively.

Table 6.2: Case studies for FMS evaluation for PTP faults.

Case Study	Description	Comment
A	HB-MMC (R=0%) with high L_{DC}	Local converters are allowed to block
B	CH-MMC (R=25%) with high L_{DC}	Local converters are allowed to block
C	CH-MMC (R=25%) with L_{DC}=50mH	All converters are allowed to block

This subsection assesses the extent of improvement in HVDC grid performance when the FMS and CH-MMCs are employed, considering the cases listed in Table 6.2, which are denoted by A-C. In cases A and B, converters C1 through C4 of the four-terminal HVDC grid of Figure 6.3 are simulated as CH-MMCs with R=0% and 25%, respectively, while in both cases the minimum DC side current limiting inductance that is required to

prevent blocking of remote converters is used (calculated using the approach presented in [157]). Recall that R=0 resembles conventional HB-MMC. Based on the findings of the previous subsection, Case C uses R=25% and L_{DC}=50 mH (significantly smaller than that in cases A and B) to demonstrate the broader benefits of the FMS, when temporary blocking of the FB chain-links of all CH-MMCs is permitted based on DC under-voltage or arm over-currents thresholds.

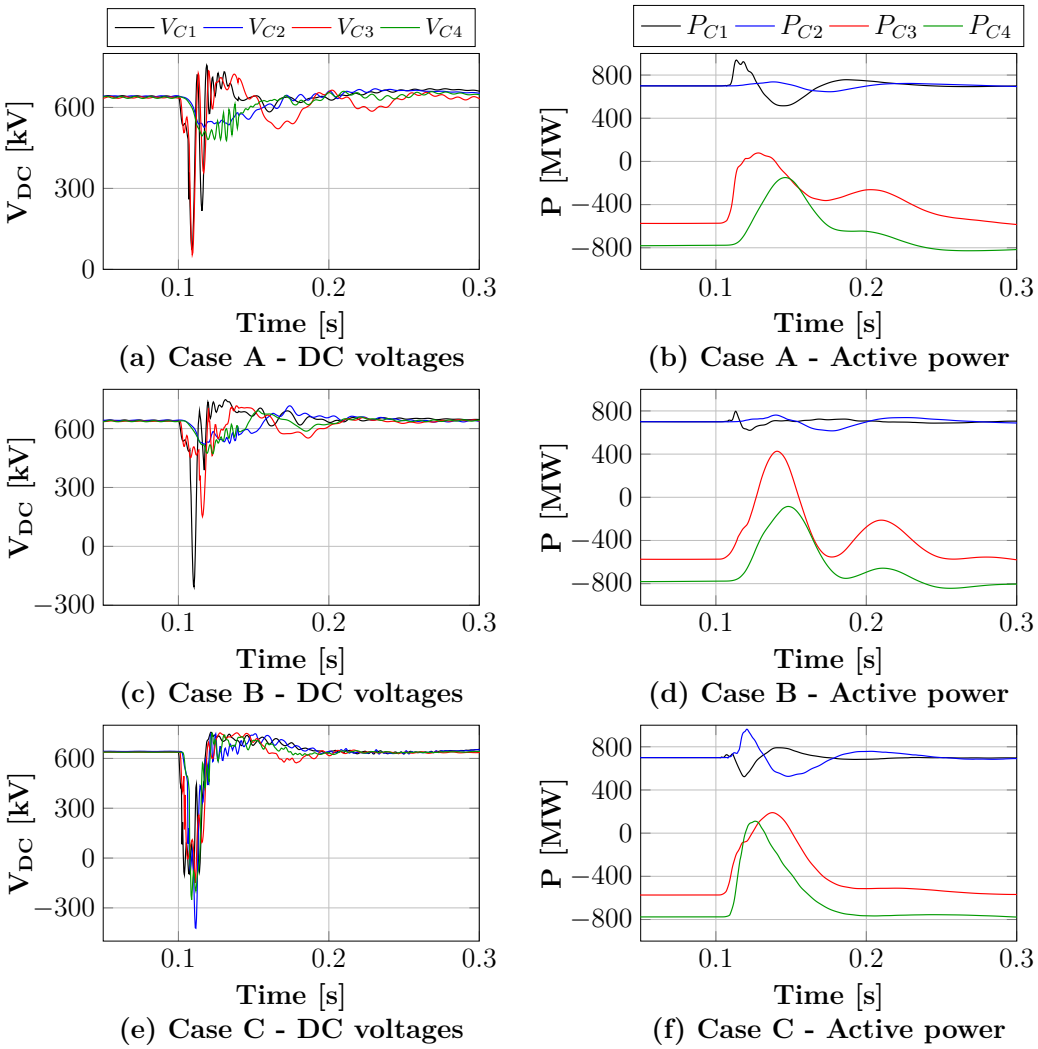


Figure 6.10: System transients for fault F1 for all case studies (t_{br}=10 ms).

Figure 6.10 presents the DC voltages of converter terminals C1 through C4 and their respective active powers for each case, when the DC grid in Figure 6.3 is subjected to a solid PTP fault at location F1 and the DCCB operating speed (t_{br}) is set to 10 ms. At this operating speed, the calculated minimum DC side current limiting series inductance to prevent blocking of remote converters (C2 and C4) is 320 mH. The main observations drawn from Figure 6.10 are:

- The continuous operation of the remote converters is maintained in cases A and B, in which DC voltage collapse is observed only at DC terminals of converters C1 and C3 (the nearest to the fault point).
- The use of CH-MMCs with R=25% in case B instead of conventional HB-MMCs leads to an improvement in voltage and power recovery time by 30% and 19%, respectively.
- Despite the temporary blocking of all converters, it is evident that case C leads to much faster power and voltage recovery times when compared with base-case A, i.e., 35% and 50.3% reduction in DC voltage and power recovery times, respectively.

Furthermore, Figure 6.11 displays the most affected arm current, the upper arm of phase A of converter C1, which is the nearest to F1. It can be seen that the use of CH-MMC leads to reduced peak arm currents during the fault. In detail, the arm current reaches a magnitude of 3.31 p.u. for case A, while the maximum observable current in case B is limited to 2 p.u. The peak arm current is further reduced to 1.8 p.u. in case C, even though a significantly smaller current limiting inductance is used.

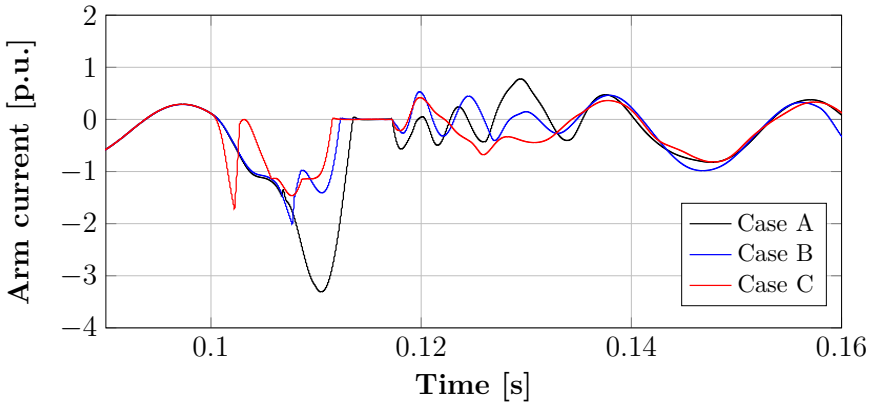


Figure 6.11: Comparison of arm currents for all case studies. The arm current shown is the upper arm of phase A.

The same PTP fault is repeated for different DCCB operating times and the observed voltage and power recovery times are summarised in Figure 6.12. For cases A and B, the derived series inductor values for t_{br}=5, 8, 10, 12, 15 ms are L_{DC}=110, 230, 320, 425 and 590 mH, respectively, while in case C, L_{DC}=50 mH. For cases A and B, as the circuit breaker operating speed increases, a higher inductor value is required to ensure continuous operation of the remote converters, while also system recovery times increase. Case C exhibits much faster recovery times than the other cases, a

trend which remains consistent for all DCCB operating times indicating that temporary blocking of all CH-MMCs leads to improved converter and system response during DC faults. In detail, the average improvement in voltage and power recovery times in case C with respect to the HB-MMC based grid (Case A) is 32.44% and 43.6% respectively. The benefits obtained from Case C also suggest that incorporation of sizeable series inductors is not required, thus reducing DCCB cost and footprint, and avoiding their interference with the upper level converter controls that may lead to erratic behaviour during post-fault recovery.

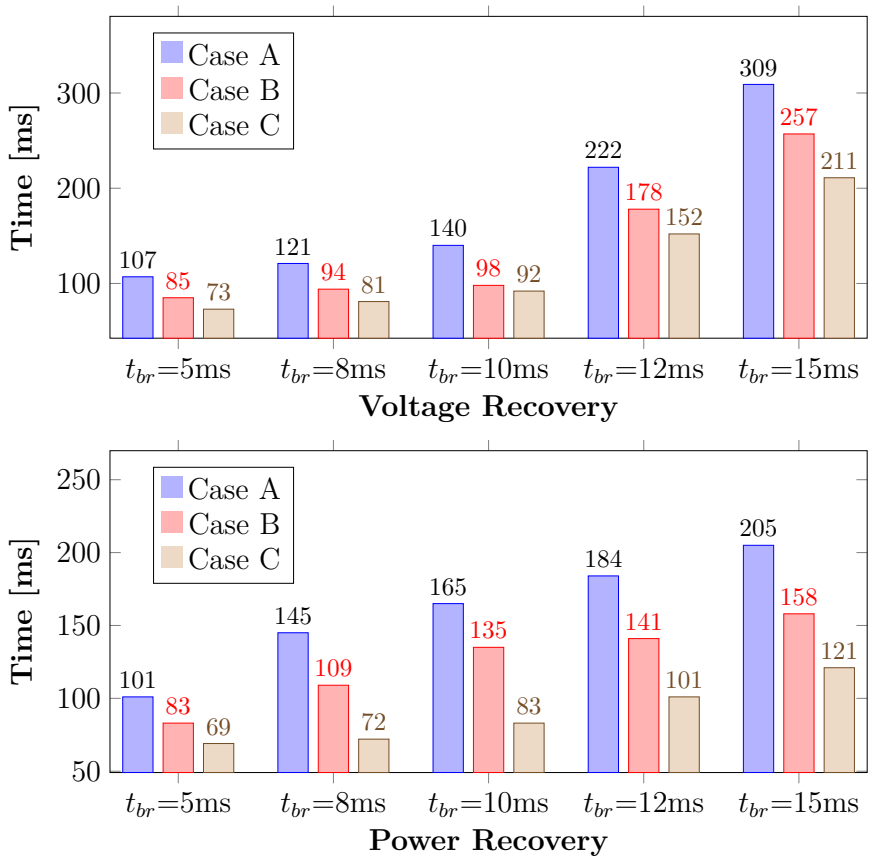


Figure 6.12: Voltage and power recovery times for all cases.

For a more rigorous performance assessment of the FMS under PTP DC faults, several fault locations are simulated, in which all converters are permitted to participate in the proposed FMS (as performed above in Case C). In the assessment, solid PTP DC faults are applied in the beginning, middle, and end of each cable of the HVDC grid. Table 6.3 summarises the average voltage and power recovery times for different t_{br} and R, with L_{DC} fixed at 50 mH. The main conclusions of this study are the following:

- Compared with HB-MMC (R=0), it is evident that the DC voltage and power recovery times reduce consistently as the ratio R increases.

- Ratio R=25% reduces power recovery times to less than four-five fundamental cycles for DCCB operating times up to 12 ms. This reinforces the benefits of the CH-MMC and the proposed DC fault management strategy, i.e. reduced protection requirements in terms of DC fault detection speed, series inductor size and breaking operation speed, without significantly compromising DC grid security during DC faults and the speed of power system restoration.

- Moreover, use of R=35% for the CH-MMC further improves system recovery time for DCCBs with operating time slower than 12 ms. Nevertheless, for faster operating times, R=25% and R=35% demonstrate small differences in voltage and power recovery times.

Table 6.3: Average voltage and power recovery times for PTP faults.

FB-SM Ratio [%]	**Voltage Recovery [ms]** DCCB speed, t_{br} [ms]					**Power Recovery [ms]** DCCB speed, t_{br} [ms]				
	5	8	10	12	15	5	8	10	12	15
0	105	125	147	235	343	100	139	162	183	209
15	92	99	124	188	266	78	126	142	151	163
25	69	77	91	149	205	65	71	81	95	116
35	67	73	86	129	188	61	68	77	86	107

6.5.3 Example Pole-to-pole Fault

For a detailed demonstration of the DC fault behaviour of a HVDC grid that employs CH-MMCs (R=25%) and operates under the fault management strategy for PTP faults, an example fault scenario is selected, in which a solid fault is applied at location F1 at time t=0.1 s, when L_{DC}=50 mH and t_{br}=8 ms.

Figure 6.13 shows the DC voltages and the calculated dv/dt at the protection relays of buses B1 (connected to C1) and B3 (connected to C3) for the first ms after fault inception. V_{ij} and dv_{ij}/dt refer to the measurements and calculations of the protection relay located at the end i of cable Lij. The under-voltage fault detection criterion is set to 0.9*V_{DC}/2=288 kV (-288 kV for negative pole), and for the fault discrimination criterion dv/dt, a conservative threshold -1 kV/μs is selected. It is evident from Figure 6.13(a) and 6.13(c) that all relays detect the DC fault, while the relays of the faulted line L13 (as seen from V_{13p} and V_{31p}) detect the fault only a few μs after the travelling waves reach their locations. Figures 6.13(b) and 6.13(d) demonstrate that only dv_{13p}/dt and dv_{31p}/dt exceed the selected threshold and consequently a DC fault on cable L13 is correctly identified.

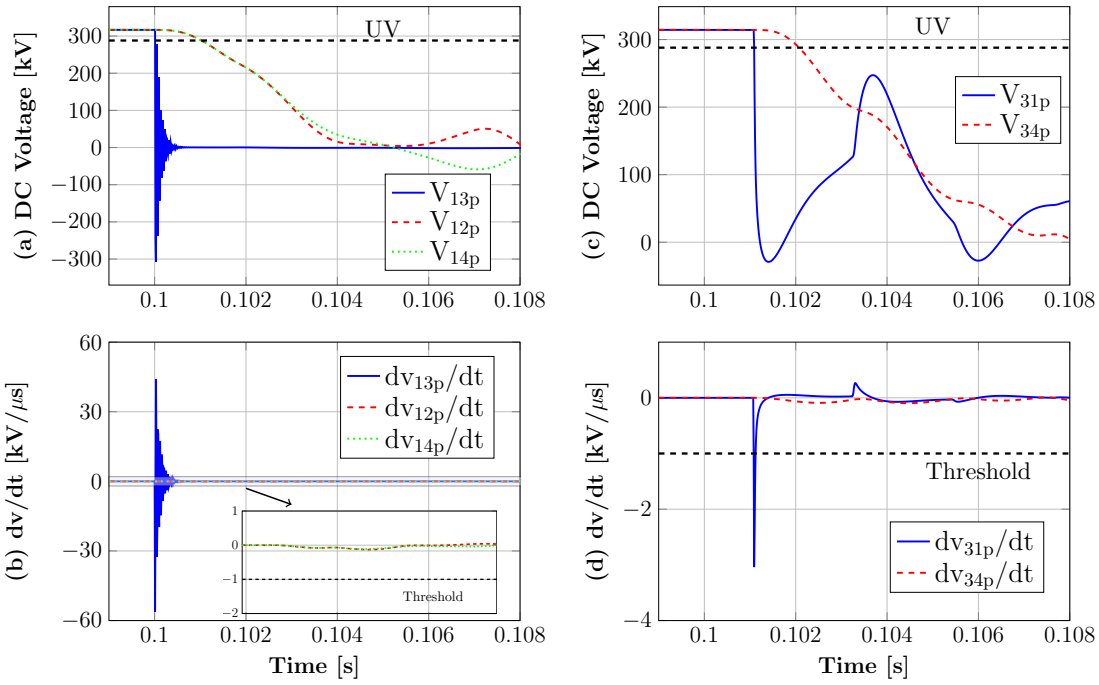


Figure 6.13: Fault detection and discrimination for PTP fault: (a) DC voltages and (b) calculated dv/dt at relays of bus B1, (c) DC voltages and (d) calculated dv/dt at relays of bus B3.

Selected system-wide simulation results are shown in Figure 6.14. Within a short time from fault inception, the PTP fault is detected by all relays of the grid and the FMS is initiated at all converters, at different time instances depending on the moment when the converter blocking criteria are satisfied. Meanwhile, protection relays of cable L13 discriminate the DC fault and send a trip command to the cable DCCBs. The main observations from Figure 6.14 are summarised as follows:

- Figure 6.14(a) shows that the activation of the FMS has led to brief collapse of DC voltages at all converter stations and to relatively fast recoveries, approximately 100 ms after fault inception.
- Figure 6.14(b) shows that the proposed FMS significantly reduces the converter DC currents and thus, the DCCBs' let-through current and required breaking capacity.
- The temporary loss of controllability over the active and reactive power exchange with the surrounding AC grids has led to brief interruption of power flows across the DC grid, which are re-established in less than 80 ms as shown in Figures 6.14(c) and 6.14(d).

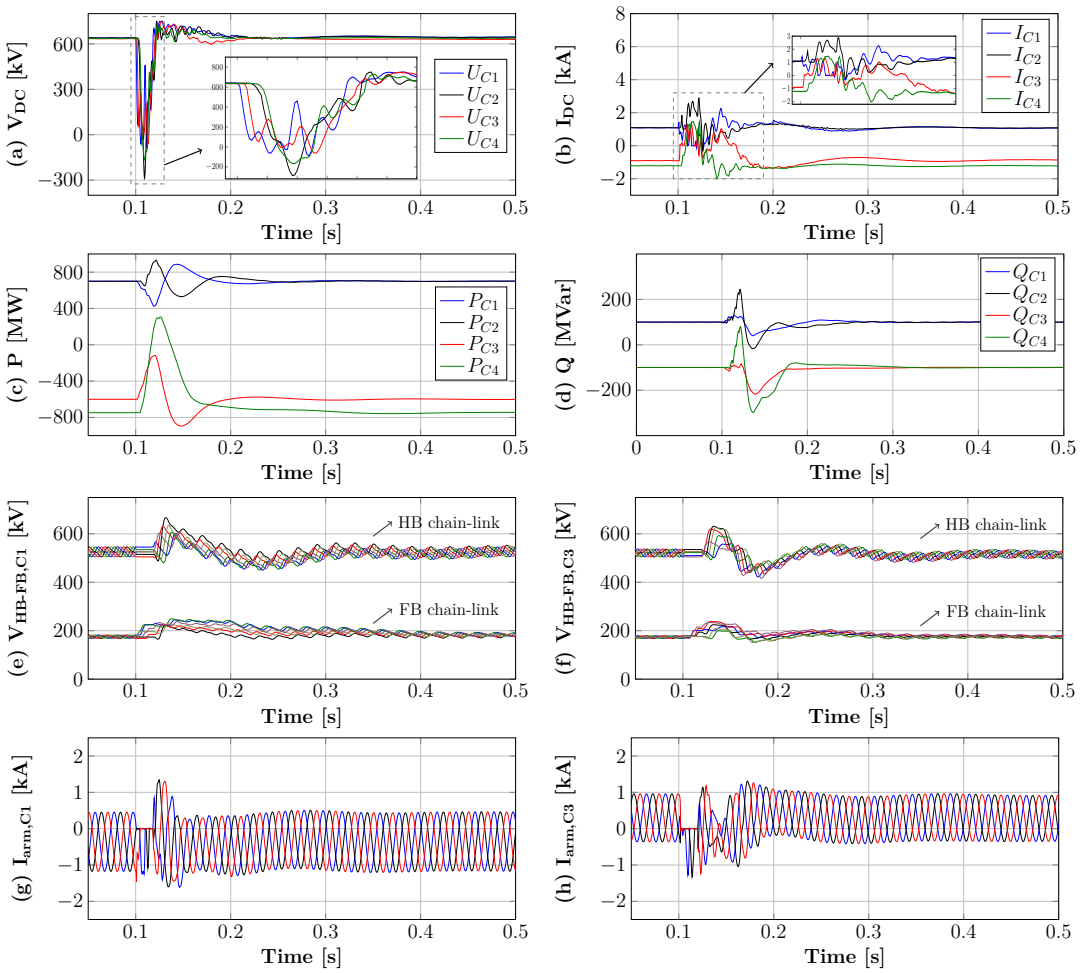


Figure 6.14: Exemplary PTP fault waveforms: (a) converter voltages, (b) converter currents, (c) active power of CH-MMCs, (d) reactive power of CH-MMCs, (e) C1 chain-link voltages, (f) C3 chain-link voltages, (g) C1 arm currents, and (h) C3 arm currents.

- Figures 6.14(e) and 6.14(f) display the DC voltages across the HB and FB chain-links of all arms for the most affected (nearest) converters (C1 and C3). It is evident that the moment the fault management strategy starts, HB-SMs are blocked, while the FB-SMs that provide counter voltages are charged by the fault current. In this way, higher counter voltages are generated in the arms of the CH-MMC, which aid to suppress the AC-side fault current contribution as well as the DC fault currents. It is worth mentioning that the capacitor over-voltage limit (1.6 p.u.) is not reached in any of the converters' arms.

- Following fault clearance, all HB and FB chain-links briefly exhibit disturbances and eventually converge to the nominal set-points as designated by the horizontal controllers.

- Figure 6.14(g) and 6.14(h) show the upper arm currents for the same converters. It is observed that converter arm currents remain within normal operating range.
- Inspecting figures 6.14 and 6.13, it is observed that DC fault detection and discrimination occur before blocking of the converters and consequently, there is no interference between the actions of protection relays and converters.

6.5.4 Example Pole-to-ground Fault

This subsection illustrates the performance of the proposed FMS when the HVDC grid is subjected to a permanent positive PTG fault at location F2 (as shown in Figure 6.3) on cable L12, 1 km away from converter C1 at 0.1 s. R, L_{DC} and t_{br} are fixed at 25%, 50 mH and 8 ms, respectively.

Figure 6.15 shows the DC voltages and the calculated dv/dt at the protection relays of buses B1 (connected to C1) and B2 (connected to C2) for the first 20 ms after fault inception. Similar to the PTP fault scenario, the DC fault is detected by all protection relays of the positive pole of the same bus (Figure 6.15(a) and 6.15(c)), but only the relays of cable L12 discriminate the fault as internal as seen from dv_{12}/dt and dv_{21p}/dt in figures 6.15(b) and 6.15(d).

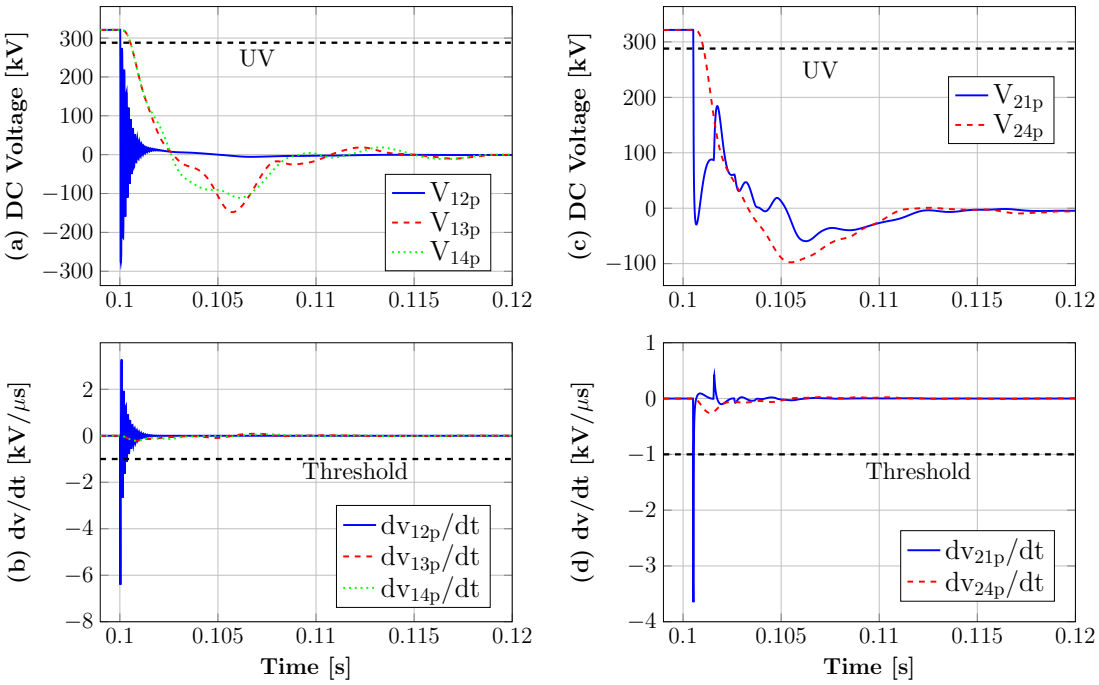


Figure 6.15: Waveforms for PTG fault (positive pole): (a) DC voltages and (b) calculated dv/dt at relays of bus B1, (c) DC voltages and (d) calculated dv/dt at relays of bus B2.

The corresponding voltage traces and dv/dt for the relays of the negative pole are shown in Figure 6.16(a) and 6.16(b), respectively. Figure 6.16(a) shows that the protection relays of the negative pole do not detect the DC fault. Since, the fault is detected only by the relays of the positive pole, a positive PTG fault is confirmed, correctly prompting the activation of the FMS for PTG faults at converters C1 and C2. Finally, Figure 6.16(b) demonstrates that there is no visible change in the calculated dv/dt by negative pole relays.

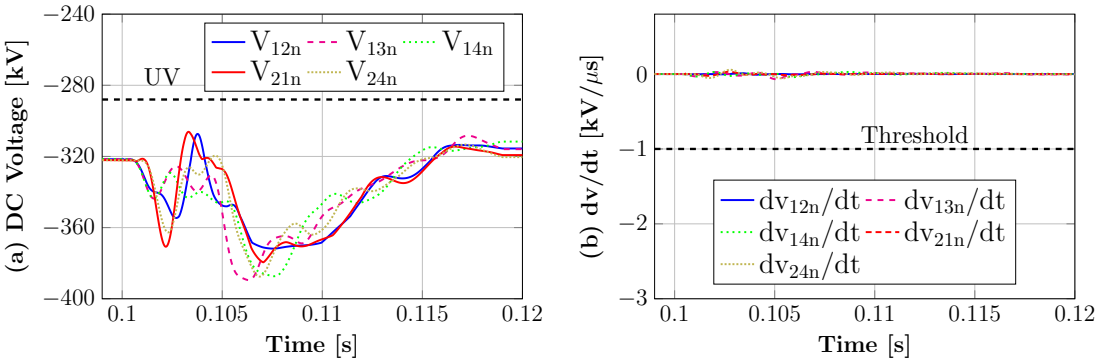


Figure 6.16: Waveforms for PTG fault (negative pole): (a) DC voltages and (b) calculated dv/dt at relays of buses B1 and B2.

Similar actions take place at terminals of C3 and C4 leading to the activation of the FMS at all converters. Selected system-wide simulation results are shown in Figure 6.17. Since the fault is not identified as temporary within 180 ms from FMS activation, a trip command is sent to the DCCBs of cable L12. For the entire fault duration, all converters participate in the fault management process and controlled continuous HVDC grid operation is retained with partial loss of power transfer capability. Following isolation of cable L12, the CGC is notified that the fault has been cleared and a grid restoration start signal is distributed to all converters (assuming 30 ms delay). The main observations from Figure 6.17 are summarised as follows:

- Figure 6.17(a) shows that all converter DC voltages are halved in a controllable manner, and after fault clearance they are simultaneously restored to nominal value as a result of the actions of the CGC.
- Figure 6.17(b) shows the positive and negative pole-to-ground voltages at the cables connected to bus B1 (DC bus of converter C1). It is evident that the DC voltages of the faulty poles are collapsed to zero, while those of the healthy poles are maintained at nominal level.
- Moreover, it can be noticed from Figure 6.17(c) that shortly after fault detection, the converter currents are controlled at the pre-fault set-points. With the em-

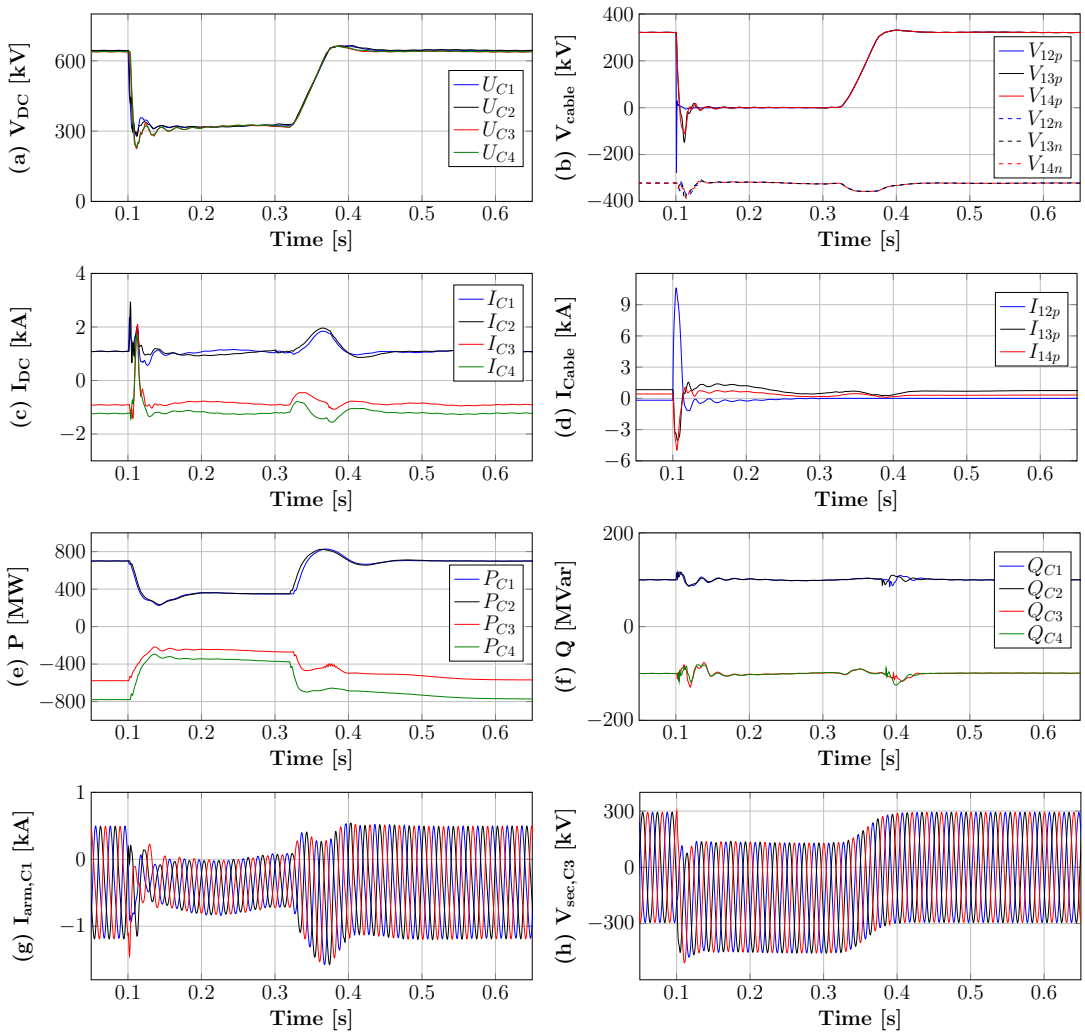


Figure 6.17: Exemplary PTG fault waveforms: (a) converter voltages, (b) cable voltages at bus B1 (c) converter currents, (d) cable currents at bus B1, (e) active power of CH-MMCs, (f) reactive power of CH-MMCs, (g) C1 arm currents, and (h) converter C3 transformer secondary voltage.

ployed FMS, the current of the faulted cable (I_{12}) decays rapidly towards zero as shown in Figure 6.17(d).

- After PTG fault detection, converters operate at almost half of the prefault power setpoints, as demonstrated in Figure 6.17(e). Once the fault is cleared, power flows are quickly re-established. Due to the continuous operation of the HVDC grid, reactive power flows are marginally affected (Figure 6.17(f)). It is evident that the proposed FMS allows the converters to retain controllability for the entire fault duration and thus, the capability to provide ancillary services to the connected AC networks.

- Figure 6.17(g) shows that the nearest converter to the fault is not experiencing current stresses in any of its arms throughout the fault period.
- The converter transformer is experiencing a DC offset equal to 1/4 of total V_{DC} (Figure 6.17(h)). Compared with a converter transformer connected to a HB-MMC, the DC offset is decreased by 50%.

6.6 Discussion

The proposed fault management strategy that is developed particularly for HVDC grids that employ the CH-MMC offers a plethora of functionalities achieved at anticipated lower capital and operational costs. Table 6.4 summarises the findings of the comprehensive quantitative studies presented in this chapter, in the form of high-level qualitative comparison, in which the ratio R of the CH-MMC is varied, with emphasis given to the following aspects: fault current contribution, breaking speed, system recovery times in PTP DC faults, and continued operation in the event of PTG DC fault. For completeness, a qualitative loss indicator, which assumes that the converter total semiconductor loss varies proportionally with ratio R, is provided in Table 6.4.

Table 6.4: Comparison between different ratios of the CH-MMC.

Performance indicator	$R = 15\%$	$R = 25\%$	$R = 35\%$
Converter fault current contribution (PTP faults)	medium	low	very low
Breaking speed requirements	high	low	very low
System recovery time (PTP faults)	low	very low	very low
Continuous operation (PTG faults)	no	yes	yes
Converter transformer DC offset (PTG faults)	high	low	very low
Converter losses	low	medium	high

It is evident that the CH-MMC with 25% ratio represents an attractive option for the practical realisation of the of the proposed fault management strategy, in which the HVDC grid PTP and PTG fault performances can be achieved at reasonable overall costs (capital and running costs). At a granular level, the sensitivity analysis has shown that the CH-MMC with R=25% offers practical compromises in terms of the magnitude of the fault currents that the mechanical DCCBs can interrupt, and the system recovery times following DC faults clearance. Furthermore, it has been demonstrated that the CH-MMC with R=35% can lower the fault currents during PTP faults and further

extend the time window for the protection systems. However, the enhanced fault performance of the CH-MMC with $R \geq 35\%$ is achieved at the expense of the increased cost of semiconductor losses over the project lifetime. It is worth stating that the overall system performance improvement in the latter case, with $R=35\%$ is marginal compared to that of $R=25\%$.

Even though $R=25\%$ has been put forward as a minimum requirement for achieving all the desired functionalities for technically sound and cost-effective HVDC grids, the final design in a particular project may differ, depending on the required balance between practical design considerations and broader system operational objectives and priorities, which are beyond those accounted for in this chapter. For example, in certain scenarios where the extended downtime is allowed, the PTP DC fault-ride-through may not be a stringent requirement. In such cases, CH-MMC with lower R ratios ($R \leq 25\%$) might be adopted, and the proposed FMS can still be used to coordinate protection actions, reduce fault currents and for the effective coordination with DCCBs with reduced requirements. However, continued operation during PTG DC faults cannot be achieved. In conclusion, the proposed FMS may be tailored according to the given requirements in order to mitigate the capital and operation costs, and ensure the desired degree of full or partial controllability during DC faults. In line with the findings of the cost analysis on protection equipment performed in [260], the reduction in breaking speed requirements and reactor sizes achieved by the use of CH-MMCs can significantly reduce the cost per DCCB unit. Nevertheless, further cost analysis would be required to estimate the exact cost savings for different ratios.

6.7 Summary

In an effort to align the security of supply requirements of HVDC grids with those of the conventional HVAC grids, while at the same time maintaining the affordability of total system cost at reasonable levels, this chapter has presented a detailed DC fault management strategy for HVDC grids that employ CH-MMCs which have the potential for partial fault tolerant capability. Adoption of the CH-MMC is motivated by an attempt to lower the cost associated with protection of HVDC grids, by devising alternative ways in which the expensive fast acting hybrid DCCBs can be replaced with slower but inexpensive mechanical DCCBs, which can isolate DC faults within 8 ms to 15 ms. Although the CH-MMC offers several avenues for performance optimisation, it has been shown quantitatively and qualitatively that the CH-MMC with 25% ratio (number of FB-SMs with respect to the total number of sub-modules per converter arm) achieves a practical and attractive trade-off between fault tolerant capability, efficiency, and cost over typical project lifetimes. This is achieved through the substantial

suppression of the magnitude of AC-side and DC-side fault currents, when the current limiting mode of the CH-MMC is invoked despite the limited number of FB-SMs.

The functions of the developed fault management strategy include coordination with local protection relays, coordination with DCCB actions, activation of the appropriate converter actions depending on whether a PTP or PTG fault is detected by the relays, and communication with the central grid controller (only for PTG faults). In addition, the FMS monitors the FB chain-link voltages in order to instruct bypassing of the FB-SMs, if the specified over-voltage limit is exceeded. Rigorous simulation studies using an illustrative four-terminal HVDC grid based on CH-MMCs have been performed to demonstrate the working principle of the FMS and the enhanced fault ride through performance of the entire HVDC grid. In detail, a number of parametric studies investigate the performance of the FMS for different: types of faults, ratios of the FB-SMs, sizes of DC side inductors and DCCB breaker operation times.

Initial parametric studies have revealed that the 25% ratio is critical for the proper operation of the proposed FMS and its effective coordination with DCCBs. Further studies have demonstrated that the FMS enables continuous operation during pole-to-ground faults, and fault-tolerant operation with minimum power flow interruption during pole-to-pole DC faults. It has been shown that the current limiting modes of the CH-MMC enable the extension of fault clearance times to levels compatible with the mechanical DCCB operation times, and significantly reduce the magnitude of fault and arm currents during pole-to-pole DC faults. In this way, the current breaking capacities of required DCCBs are reduced using significantly smaller current limiting series inductors. Also, it has been demonstrated that the proposed FMS results in improved DC voltage and power recovery times with respect to conventional HB-MMC based HVDC grids. The above-mentioned features collectively, lead to a satisfactory trade-off between cost, efficiency and DC fault-ride through capability, which renders the proposed strategy an attractive option for the technical and economical feasibility of future HVDC grids.

Chapter 7

Single-ended Fault Location for HVDC Grids Embedding High-speed DCCBs

This chapter presents a novel fault location method for HVDC grids that relies only on short data windows of single-ended voltage measurements, thus rendering the technique practically applicable to HVDC grids employing high-speed circuit breakers. Based on the available post-fault voltage traces, a frequency domain voltage profile is initially constructed, which is then iteratively evaluated against theoretical voltage profiles, synthesised with the use of travelling wave principles. The evaluation routine is based on a genetic algorithm regime, which once terminated indicates a close approximation of the feeder's fault location. The result of this process is further refined using a weighted averaging function to obtain the final fault distance estimation. The performance of the method is demonstrated using comprehensive electromagnetic transient simulation studies conducted on a four-terminal HVDC grid using PSCAD/EMTDC. The results revealed that the method can estimate the fault location with high accuracy for all transmission media types, including hybrid lines that comprise of cable and overhead line segments. Moreover, the method has been found to maintain its accuracy for very long transmission lines, highly-resistive faults and different fault types.

7.1 Motivation

HVDC grids necessitate the use of reliable HVDC protection systems to guarantee safety of the HVDC grid components and minimise the potentially detrimental effects of DC faults. Such HVDC protection systems commonly involve the use of DC circuit breakers to selectively isolate the fault as soon as possible. Following fault clearance,

the location of the fault should be accurately determined in an effort to accelerate system restoration and diminish operational costs and power outage duration.

Successful fault location becomes increasingly challenging in HVDC grids due to the short time windows between fault inception and fault clearance as a consequence of the utilisation of high-speed DCCBs with operating times in the order of 2-8 ms. Consequently, the available data windows for applying a DC fault location technique for HVDC grids is confined to only a few milliseconds after fault occurrence. Nevertheless, the majority of the fault location methods proposed in the literature (see Subsection 3.5.6) are either designed for point-to-point HVDC links in which large data measurement sets are available due to the absence of DCCBs, or have ignored the impact of high-speed DCCBs on the data window length.

In addition, an increasingly challenging task for fault location arises from the utilisation of non-homogeneous or else hybrid transmission media in HVDC systems, which include segments of both overhead lines and underground cables. In such networks, additional challenges are introduced from the unequal wave propagation speed in OHL and cables, and from the dense travelling waves reflections that occur due to the presence of multiple joint points. Most of the existing fault location solutions focus exclusively on either cable-based or OHL-based HVDC systems and only a few have been designed for non-homogeneous feeders [220, 235, 236], which are in principle TW-based techniques. Nevertheless, these methods either depend on distributed sensor technology, which increases cost and complexity, or face the usual challenges of TW-based techniques.

To overcome the aforementioned issues, this chapter proposes a fault location method for HVDC grids that can be used for any transmission line geometry including hybrid transmission media. The proposed fault location technique is single-ended, and only local voltage measurements are required, thus eliminating the need for time-synchronised measurements. The method is based on an adjustable limited post-fault data window that is selected based on the available time frame between fault inception and subsequent events arising from high-speed DCCB actions or further travelling wave reflections. From the available measurements, the frequency domain voltage characteristic is constructed. Subsequently, the fault location estimation is performed by using genetic algorithm to flexibly generate theoretical profiles until a match with the existing voltage characteristic is achieved.

7.2 Frequency Domain Profile of Transient Voltage

7.2.1 Transient Voltage Characteristic Representation

To ensure its suitability in a multi-vendor environment and the general applicability of the fault location technique that is developed in this chapter, the same generic HVDC

grid section of Chapter 4 is considered for as the fundamental starting point for the design of the technique. For convenience, the generic HVDC grid section is repeated in Figure 7.1. The section comprises of two VSC terminals that are connected through a transmission medium with a series inductor at both ends, while further ν and μ DC links are connected to terminal buses B1 and B2, respectively.

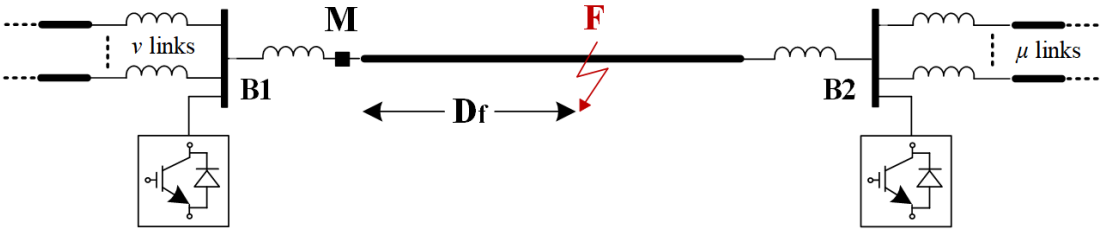


Figure 7.1: General section of a HVDC grid.

The aim of the proposed fault location method is to estimate the fault distance D_f based exclusively on local voltage measurements at the measuring point M. The frequency domain formulation of the fault voltage at M can be derived based on travelling wave principles and forms the basis for the proposed method. The approach for deriving the voltage transfer function (voltage characteristic) at the measuring point with respect to the voltage at the fault point is similar with the approach used in Chapter 4 for determining the voltage at the protective relay location. Similarly, assuming a PTP DC fault at location F of Figure 7.1 at distance D_f from M, the voltage at the measuring point M following the reflection of the first incident voltage wave is given by:

$$U_M = \mu_{B1} \cdot H_{D_f} \cdot U'_f \tag{7.1}$$

where U'_f is the voltage wave at the fault point, H_{D_f} is the propagation function representing the attenuation experienced by the voltage wave after propagating along fault distance D_f, and μ_{B1} is the transmission coefficient, which determines the fraction of the fault voltage wave that passes through L_{DC}. To eliminate the mutual coupling effect between the system poles and ensure extensibility of the analysis to bipolar configurations, the phase-mode transformation is utilised, according to which the decoupled ground-mode voltage U_{M_0}, and line-mode voltage U_{M_1} are given by [241]:

$$\begin{bmatrix} U_{M_0} \\ U_{M_1} \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} U_{M+} \\ U_{M-} \end{bmatrix} \tag{7.2}$$

Using the same assumptions, converter modelling (HB-MMC), distributed parameter frequency dependent transmission line model and inductive termination that were

assumed in Chapter 4, and applying the phase-mode transformation, the transient line-mode voltage at the fault point can be obtained:

$$U'_f = \frac{\sqrt{2}Z_{c_1}}{2(Z_{c_1} + R_f)} U_f \tag{7.3}$$

where R_f is the fault resistance, and Z_{c_1} is the line-mode component of Z_c. By substituting (7.3) to (7.1), the voltage transfer function (U_{M_1}/U_f) is expressed as:

$$\frac{U_{M_1}}{U_f} = \mu_{B1} \cdot H_{D_f} \cdot \frac{\sqrt{2}Z_{c_1}}{2(Z_{c_1} + R_f)} \tag{7.4}$$

With the converter and transmission line parameters known, the voltage transfer function depends on the fault distance (represented through H_{D_f}) and the fault resistance. It is worth mentioning that a similar analysis can be performed for deriving the voltage transfer function for pole-to-ground faults. Moreover, equation (7.4) can be generalised for hybrid transmission mediums that comprise of an arbitrary number of cable and/or OHL segments. For instance, for a fault that occurs in segment S_2 of the hybrid transmission medium of Figure 7.2 the voltage transfer function is calculated as:

$$\frac{U_{M_1}}{U_f} = \mu_{B1} \cdot \mu_{s_2 \to s_1} \cdot H_{x_1} \cdot H_{x_2} \cdot \frac{\sqrt{2}Z_{c_1}}{2(Z_{c_1} + R_f)} \tag{7.5}$$

where H_{x_1} represents the wave propagation over x_1 (whole length of segment S_1), H_{x_2} represents the wave propagation over x_2 of segment S_2, and $\mu_{s_2 \to s_1}$ describes the fraction of the fault wave that travels from S_2 to S_1. It can be seen that H_{Df} can be split into separate propagation functions that represent the distance covered by the incident travelling wave in each segment of the hybrid transmission medium. The segmentation of the propagation function is a very significant property that will be exploited later by the proposed method to locate DC faults without having to identify the faulted transmission medium segment first.

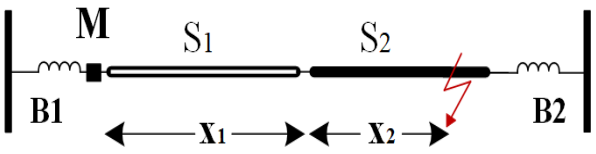


Figure 7.2: DC fault on a hybrid transmission medium.

7.2.2 Frequency Response of Voltage Transfer Function

Figure 7.3 displays the frequency response of (7.4) in terms of the magnitude of the voltage transfer function for PTP faults at various locations and various fault resistances, when L_{DC}=50 mH, R_{eq}=0.53 Ω, L_{eq}=28 mH, C_{eq}=94.26 μF, ν=2 and the faulted medium is a cable, with the parameters adopted from [81]. It is evident, that fault resistance and fault distance have a distinct and different effect on the voltage transfer function. In detail, an increase in R_f provokes a reduction in magnitude of the voltage characteristic across the whole bandwidth, while an increase in D_f moves the characteristic leftwards and downwards, indicating both a reduction in magnitude and a progressively higher attenuation in the high frequency region.

These attributes form the main principles of the developed fault location method. Given a DC fault with unknown R_f and D_f, the objective of the method is to construct the voltage transfer function based on local voltage measurements and determine the fault location from the position of the voltage characteristic in the magnitude-frequency plane.

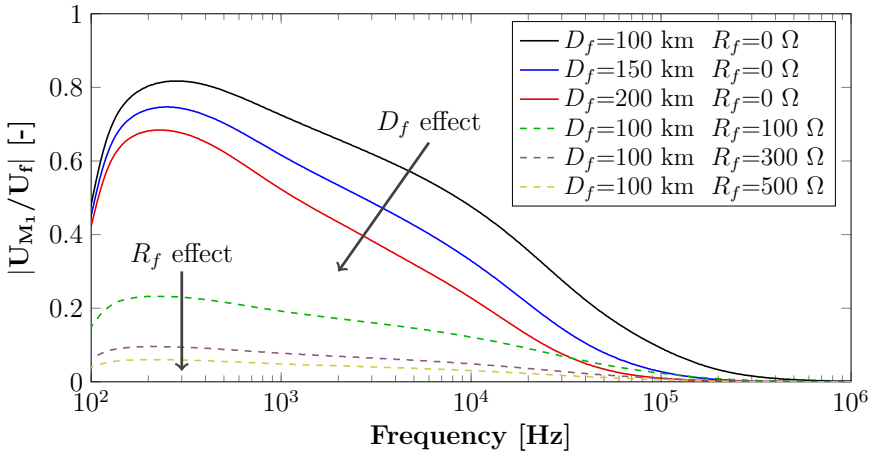


Figure 7.3: Frequency response of voltage transfer function for PTP DC faults with different fault distances and resistances on a DC cable.

Similar trends are observed when the cable is replaced with an OHL, as shown in Figure 7.4 (OHL parameters are adopted from [243]). In this case, the impact of D_f and R_f on the voltage characteristic is more distinct. Moreover, the impact of D_f is more pronounced in the high frequency region, while when compared with the corresponding voltage characteristic for DC cables (see Figure 7.3), the affected frequency band is lesser and concentrated in higher frequencies. This implies that in order for the fault distance to have a noticeable effect on the voltage characteristic, a higher sampling rate is required to capture the high frequency traits.

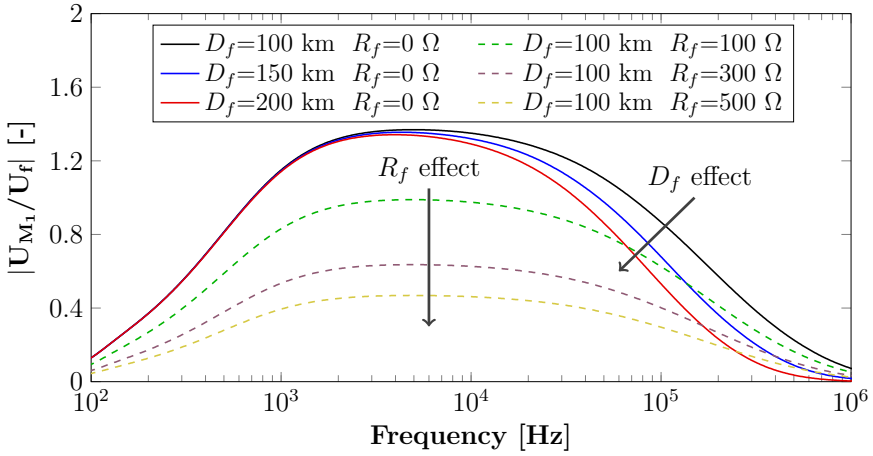


Figure 7.4: Frequency response of voltage transfer function for PTP DC faults with different fault distances and resistances on an OHL.

7.3 Proposed Fault Location Method

This subsection explains in detail the rationale behind the operation of the developed fault location method. The proposed method is only dependent on a limited set (in terms of duration) of single-end post-fault voltage measurements. The available data set is processed by a transfer function identification tool in order to construct a frequency domain profile. Subsequently, a genetic algorithm is used to identify the optimum fault distance and the corresponding theoretical frequency profile (based on the analysis of Section 7.2) that better matches the occurred fault case.

The overall flowchart of the proposed fault location scheme is illustrated in Figure 7.5. It is worth mentioning that since processing time is not of critical importance in fault location applications, the overall process is assumed to be executed offline. The method comprises of four stages, which are described in the remainder of the section. To illustrate the overall process in detail, an example solid DC fault with D_f=100 km is considered assuming the same parameters used in Section 7.2.

7.3.1 Stage I: Data Window Determination

Wavelet transform is a common tool that is used to detect signal singularities, such as travelling wave reflections in the fault signal. To mitigate the impact of the downsampling effect caused by other discrete wavelet transform variants and to avoid distortion of the induced fault transients, SWT is employed for this task. SWT typically involves greater computational burden, since all data points are utilised at each decomposition level, but it results in more accurate solutions. By denoting the sampled measurements of DC voltage as $x[k]$, the first level detailed coefficients using stationary wavelet

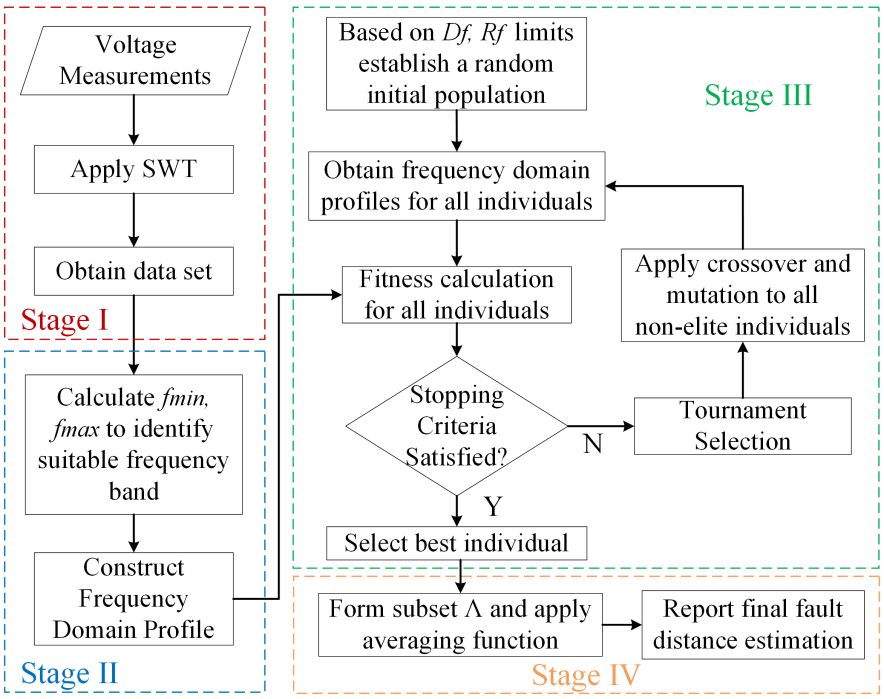


Figure 7.5: Flowchart of the proposed fault location method.

transform are obtained through:

$$D_1[n] = \sum_{k=0}^{L-1} x[k]h_1[n-k] \tag{7.6}$$

where n is the sample index and L represents the order of the high-pass filter $h_1[k]$, which depends on the selected mother wavelet (db4 has been found to be suitable for the purposes of this application). The magnitude of D_1 is used to identify the time instance at which an event occurs. The samples between two events form the main data set to be used in the next stages. The obtained data set is oversampled using cubic spline interpolation to complete the measurement set. Oversampling by a factor of 4 is utilised to ensure that there is a sufficient number of samples for Stage III, even when the fault is situated close to the line ends (down to 1 km fault distance). The fault type (PTP or PTG) can be identified with ease by the application of SWT, however, this information is assumed to be known. The data window size is constrained at 2 ms and is typically well below 1 ms (for mediums with 50-500 km length), thus rendering the proposed method practically applicable to HVDC grids employing any type of breaker technology and breaker operating speed. In addition, such a short data window ensures immunity to reflected or refracted waves from peripheral or remote lines.

It is worth noting that the objective of this stage is not to determine the actual

arrival time of the TWs but rather to identify the available suitable samples between two events. The first event is always the first incident TW (generated at the fault location) that reaches the measuring point. A subsequent event is defined as a TW reflection that originates from the fault point or the remote end of the line or any other action that is triggered by the employed DC protection systems such as, converter blocking or breaker opening. This process ensures that the analysis of the previous section is valid for the selected data window. A near-zero threshold is set on D_1 to ensure the effectiveness of this stage under noisy measurements situations. The DC voltage U_{M+} and the corresponding D_1 coefficients are illustrated in Figure 7.6 for the example DC fault of this section.

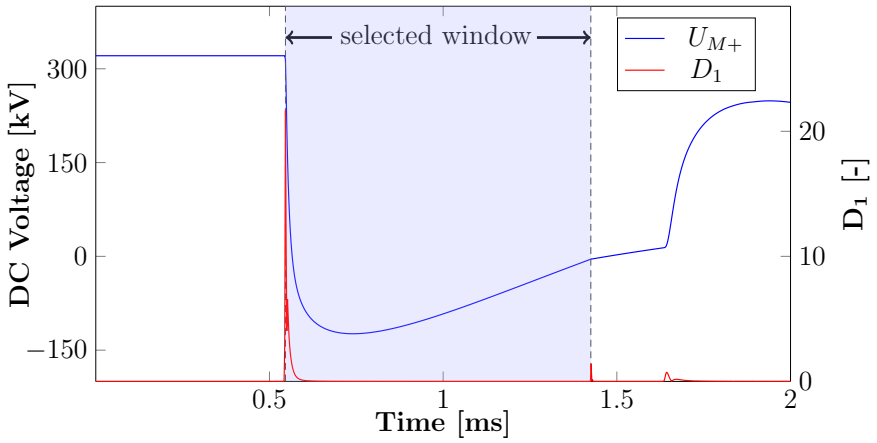


Figure 7.6: Data window determination based on D_1 coefficients.

7.3.2 Stage II: Frequency Domain Profile Construction

The objective of this stage is to estimate the continuous time transfer function and construct the frequency domain profile for the examined fault case using sampled voltage measurements. Assuming an input signal $u(t)$, and an output signal $y(t)$, we can describe the continuous-time linear system:

$$y(t) = G(s, \theta) \cdot u(t) \tag{7.7}$$

in which, $G(s, \theta)$ is the transfer function that is aimed to be identified, which is defined as:

$$G(s, \theta) = \frac{B(s)}{A(s)} = \frac{b_0 + b_1 \cdot s + ... + b_m \cdot s^m}{a_0 + a_1 \cdot s + ... + a_n \cdot s^n} \tag{7.8}$$

where a_n=1 with $n \geq m$, and s is the differential operator (dx/dt), which can be interpreted in this analysis as the Laplace operator. For the identification problem it

is also assumed that signals $y(t)$ and $u(t)$ are sampled at regular time intervals, with a sampling time of $T_s(=1/f_s)$.

In this chapter, signal u represents the step voltage generated at the fault point (i.e. U_{dc} for PTP faults or $\pm U_{dc}/2$ for PTG faults), and signal y is formed by the N voltage measurements obtained through Stage I. Hence, based on discrete time input output data $\{u(kT_s),\ y(kT_s)\}$ with $k{=}1, 2, ..., N$, the objective is to estimate the parameter vector:

$$\theta = [a_n, a_{n-1}, ..., a_0, b_m, b_{m-1}, ..., b_0]^T \tag{7.9}$$

To identify the transfer function coefficients, the simplified refined instrument variable (SRIV) method is used, where firstly, the measured signal y is passed through a prefilter L_s that is equal to $1/A(s)$, to initialise the parameters. The parameters are then updated through an iterative process using a non-linear least squares solver until the prediction error is minimised. This process is described in detail in [277], where it also shown that SRIV can provide a considerable degree of resiliency against noise. Benefiting from this feature, frequency domain voltage profiles can be constructed accurately in this stage even when noisy measurements are considered.

The result of this process is the frequency domain profile, which should be identical with the frequency response of U_{M_1}/U_f of equation (7.4), if the same fault distance and resistance is assumed. For the example fault case, the identified transfer function is plotted in Figure 7.7, along with the theoretical transfer function obtained through (7.4). It is evident that the two transfer functions (frequency domain profiles) correspond well with each other within a specific frequency band.

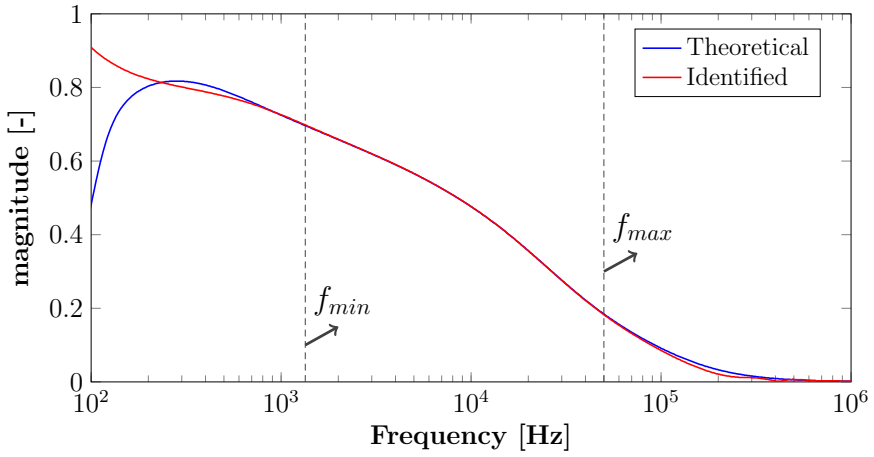


Figure 7.7: Frequency response of the identified transfer function and the theoretical transfer function (U_{M_1}/U_f) for D_f=100 km, R_f=0 Ω.

The range of this frequency band depends on the length of the data window and

the employed sampling rate. By satisfying the Nyquist theorem, the bounds of the frequency band are defined as follows:

$$f_{min} = r_1 \cdot \frac{1}{2\Delta t}, \quad f_{max} = r_2 \cdot \frac{f_s}{2} \tag{7.10}$$

where Δt is the length of the obtained time window from Stage I, and r_1 and r_2 are two reliability factors, which are introduced to further constrain the frequency band and ensure that only the accurately reconstructed part of the frequency domain profile is selected for the next stage. After thorough investigation through offline quantitative analysis, it has been found that by selecting r_1=2 and r_2=1/5, a region with a close match between theoretical and reconstructed profiles is selected in all fault scenarios. For the same example used in this section, the time window Δt is 0.882 ms (see Figure 7.6), while f_s=500 kHz. Based on these, the resulting frequency band is [1.34kHz−50kHz]. It is evident from Figure 7.7 that in this band the constructed (identified) profile and the theoretical profile closely match each other. This is the main principle of the proposed method, which seeks to estimate the fault location by comparing the profile constructed in this stage with the frequency response of equation (7.4) by iteratively trying different values of fault resistance and fault distance.

7.3.3 Stage III: Genetic Algorithm

The objective of this stage is to iteratively generate potential frequency domain profiles based on arbitrary values of fault distance and fault resistance (within an allowed set) and retrieve a single profile that better matches the corresponding profile constructed in Stage II. This problem can be defined as an optimisation problem by formulating an objective function that is aimed to be minimised. The Root Mean Square Error (RMSE) is selected as a metric of comparison to quantitatively measure the similarity between the constructed frequency domain profile and the various candidate profiles. Hence, the objective function can be expressed as:

$$f(x) = RMSE(G, F) = \sqrt{\frac{1}{M}\sum_{n=1}^{M}\Big(G_n - F_n(D_f, R_f)\Big)^2} \tag{7.11}$$

where M is the length of an evenly spaced set of frequencies from f_{min} to f_{max}, G is the profile obtained from Stage II (see Figure 7.7), and F is the candidate frequency domain profile which is a function of fault distance D_f and fault resistance R_f, which should satisfy the following criteria:

$$0 \leq D_f \leq l \quad \& \quad 0 \leq R_f \leq R_f^{max} \tag{7.12}$$

where l is the length of the faulted medium and R_f^{max} is the maximum fault resistance considered in the optimisation problem. For the realisation of (7.11), G and F are defined as vectors, which are compared for all M frequency points. All the candidate frequency domain profiles are generated iteratively by deriving the frequency response of equation (7.4) for DC cables or lines, or equation (7.5) for a hybrid medium. Lower RMSE values correspond to higher similarity between the two profiles.

To flexibly solve this problem, the genetic algorithm (GA) is used, which is a general-purpose population-based stochastic search technique based on the principles of evolution and genetic mechanisms. Due to its nature the GA significantly reduces the computational complexity and speeds up optimum solution convergence. The genetic algorithm iteratively modifies a population, which is formed by a set of candidate solutions termed as individuals, to produce a new population or generation. In each generation, every individual is assigned a quality value (based on a fitness function) and then a selection process is applied to choose the fittest individuals, called parents, to be part of the reproduction process and create the individuals of the next generation, called offsprings. In the reproduction process, the offsprings are formed through the operations of selection, crossover and mutation. The vector entries of each individual of the population are commonly referred to as genes and correspond to the variables of the optimisation problem.

One of the advantageous aspects of the genetic algorithm is that it requires no information of the properties of the objective function to be minimised and it is only dependent on the evaluation of the fitness function for each potential solution (individual) that is investigated. In addition, the algorithm offers a more flexible and selective approach in handling the optimisation problem by focusing on individuals with better fitness value, and hence with a higher probability to be closer to the optimum solution, rather than scanning the entire search space.

The optimisation problem is solved as an integer programming problem, in which equation (7.11) is directly used as the fitness function and the variables or genes are decoded as integers [278]. This means that the fault distance and fault resistance are represented by two vectors with integer elements, which correspond to actual D_f and R_f values. The two vectors range from 0 to l, and from 0 to R_F^{max}, with intervals of ΔD_f=0.1 km, and ΔR_f=1 Ω, respectively. The genetic evolution operators used by GA are subsequently described.

Selection

The selection mechanism initiates the generation of the mating pool by selecting better individuals from the current population. Initially, a specified number of individuals

with the best fitness values (lower values of (7.11)) are automatically advanced to the next generation. These individuals are called elite and their count is set to 5% of the population. A relatively large population size (50) is used in order to force the genetic algorithm to search a larger region of the solution space more thoroughly and locate the global minimum of the entire search space rather than a local minimum. In this way, the possibility of a premature convergence is eliminated. It is worth noting that the fitness function of elite individuals is not re-evaluated in the next iterations since its value has already been calculated.

For the rest of the individuals, the binary tournament selection operator is used as a reproduction operator. According to this operator, tournaments are played between two random individuals and the individual with the best fitness value survives to the mating pool. The same procedure is applied systematically until each solution has participated in exactly two tournaments. It can be understood that the best solution will win in both tournaments it participates, thus generating two copies in the mating pool. In a similar way, the worst solution will be eliminated from the next population. The employed selection mechanism ensures that the best solutions of each generation are advanced to the next generation and contribute to the genes of their offsprings.

Crossover

The crossover operator defines how the genetic algorithm combines two individuals of the parent population to generate two offsprings for the next generation. In detail, this operation enables the genetic algorithm to extract well performing genes from the parent population and recombine them into potentially superior offsprings. Laplace operator is used as the crossover function [279], according to which two offsprings, $y^i = (y^i_{D_f}, y^i_{R_f})$ and $y^j = (y^j_{D_f}, y^j_{R_f})$ of generation k, are generated from two parents $x^i = (x^i_{D_f}, x^i_{R_f})$ and $x^j = (x^j_{D_f}, x^j_{R_f})$ of generation k-1 in the following way (when taking fault distance gene as an example):

$$\begin{aligned} y^i_{D_f} &= x^i_{D_f} + \beta(x^i_{D_f} - x^i_{D_f}) \\ y^j_{D_f} &= x^j_{D_f} + \beta(x^j_{D_f} - x^j_{D_f}) \end{aligned} \tag{7.13}$$

where i, j represent two random population individuals, and β is a random number which satisfies the Laplace distribution. Crossover is responsible for the recombination of genes and the convergence speed of GA, and it is typically applied with high probability. Hence, the probability for an individual of the mating pool to be subjected to crossover is set to P_c=85%.

Mutation

Mutation ensures genetic diversity through the creation of new genes (new values of D_f and R_f), and it enables GA to search over a broader space, leading to regions not yet explored and increasing the likelihood to generate individuals with better fitness values. This is achieved by applying random changes to individual parents. This process can be interpreted as maintaining the same fault distance for a new offspring, and changing the fault resistance (or vice versa) to a value that leads to a better fit.

In this paper, the power mutator is employed for performing mutation [278], in which a solution y is sought to be created in the vicinity of a parent solution x. A random number p is generated which satisfies the power distribution, $d{=}d_1^p$, where d_1 is a uniform random number between 0 and 1, and p is the index of mutation, which is set to 4 [278]. Taking gene y_{D_f} as an example, the mutated solution is given by:

$$y_{D_f} = \begin{cases} x_{D_f} - d(x_{D_f} - D_f^{min}), & \text{if } t < r. \\ x_{D_f} - d(D_f^{max} - x_{D_f}), & \text{if } t \geq r. \end{cases} \quad \text{with} \quad t = \frac{x_{D_f} - D_f^{min}}{D_f^{max} - D_f^{min}} \tag{7.14}$$

where r is a uniformly distributed random number between 0 and 1, and D_f^{min}, D_f^{max} is the minimum and maximum length of the faulted medium. The mutation rate should be refrained to avoid the counter-productive effect of increasing the likelihood of introducing bad genes. Therefore, the mutation probability is set to P_m=2.5%.

Termination Criteria

The aforementioned genetic operations are repeated in each generation of the GA until the termination criteria are satisfied. The termination criteria are based on the maximum number of generations Ng, and the maximum number of stall generations N_{sg}. Stall generations are defined as the iterations which do not lead to further improvement of the best individual's fitness value, which means that the algorithm has attained optimal convergence.

For the example DC fault case, the evolution process of the genetic algorithm is illustrated in Figure 7.8, which displays the mean fit (mean RMSE of all population individuals) and the best fit (lowest RMSE) for each generation. It can be seen that the algorithm gradually moves to better fitness values and the best fit is found within a low number of generations. Generally, through the relevant analysis for the purposes of this application, the GA has been found to be capable of identifying the optimal

solution within 30 generations. Nevertheless, to further refrain the probability for a premature convergence, the maximum number of generations and the maximum number of stall generations are conservatively set to 100 and 25, respectively. Therefore, for the example of Figure 7.8, since optimal convergence is achieved at the 15^{th} generation, the GA terminates at the 40^{th} generation when the maximum number of stall generations is reached. The final population includes multiple copies of the optimum solution (i.e. D_f=100 km and R_f=0 Ω).

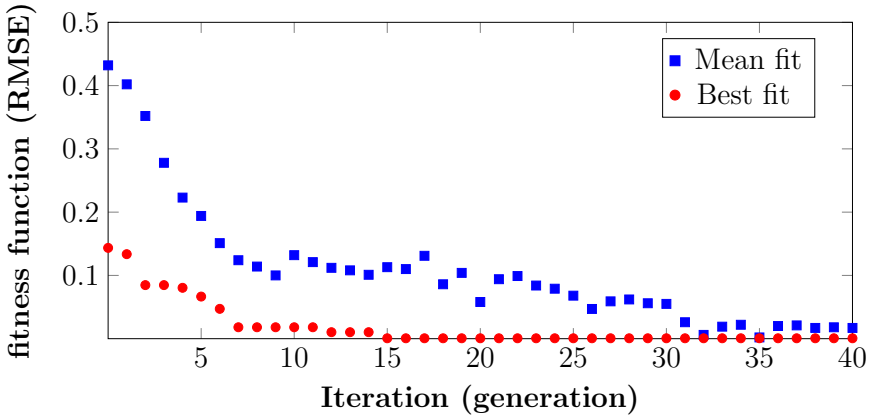


Figure 7.8: Mean and best fitness value in each GA generation.

7.3.4 Stage IV: Fault Location Estimation

In the last stage of the proposed method, the final fault location estimation is performed using the solution derived from the GA. Since GA provides the optimum fault distance that satisfies equation (7.11) as a multiple of 0.1 km, this stage is introduced to provide higher precision. This is realised by forming a subset Λ of fault distances that comprise of the optimum fault distance as well as the two previous and two next distance intervals. Subsequently, the fault location is estimated using a weighted averaging function based on exponential kernels as shown by:

$$D_{est} = \frac{\sum_{w \in \Lambda} D_f(w)\ e^{\,-RMSE(w)}}{\sum_{w \in \Lambda} e^{\,-RMSE(w)}} \tag{7.15}$$

where D_{est} is the estimated fault distance. The objective of the weighted averaging function is to apply more weight on the solutions with lower RMSE values, thus enhancing the impact of more accurate approximations to the final estimation. It is worth noting that the subset Λ is selected to have a length of 5 elements in order to ensure that the best three candidate solutions are always included in the calculation

performed by equation (7.15). Moreover, RMSE has been selected from the available similarity/distance measures due to its characteristic of applying relatively high weight to large errors and hence more accurate solutions are better revealed.

7.4 Simulation Results

7.4.1 HVDC Grid Test System and Methodology

The symmetrical monopolar four-terminal HVDC grid model that was developed with the PSCAD/EMTDC simulation tool and presented in Section 3.7 is used in this chapter to validate the performance of the proposed fault location method. The lengths and the types (cable, OHL or hybrid) of the frequency dependent transmission lines models have been modified as shown in Figure 7.9 in order to test the method for different mediums. The DCCBs placed at each line end have an operation time of 2 ms. The main parameters of the HVDC grid and the MCCs are summarised in Table 7.1.

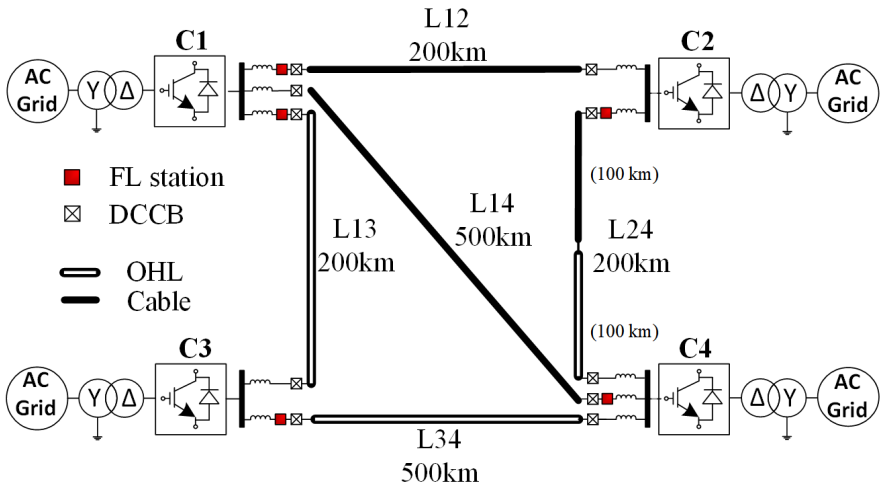


Figure 7.9: Four-terminal HVDC grid test system.

PTP and PTG faults have been simulated in all transmission media of the test system, at different locations and with fault resistances up to 500 Ω. Solid faults (i.e. 0 Ω) have been simulated with R_f=0.01 Ω. Moreover, sensitivity analysis in terms of noise contamination in voltage measurements, sampling frequency and loading conditions has been performed. Finally the findings of a performance comparison with existing fault location methods for HVDC applications are also discussed in this section. In all cases, the simulations have been carried out with a 1 μs time step and voltage measurements are captured at the fault location (FL) stations illustrated in Figure 7.9 at 500 kHz. The fault location estimation error in percentage for each fault case is calculated as:

Table 7.1: System and converter parameters.

Parameter	Value
Nominal DC voltage	± 320 kV
Rated power (C1∼C4)	1000 MVA
Active power setpoint (C1∼C4)	700,700,−800,−600 MW
Reactive power setpoint (C1∼C4)	100,100,−100,−100 MVAr
DC inductors	50 mH
Arm inductance	42 mH
Arm capacitance	31.42 μF

$$error\ [\%] = \left| \frac{D_{est} - A_f}{l_f} \right| \cdot 100\% \tag{7.16}$$

where A_f is the actual fault location and l_f is the length of the faulted transmission medium.

7.4.2 Fault Location Results for Different Transmission Line Media

In order to verify the performance of the proposed fault location method for all types of transmission media, a series of PTP and positive PTG faults are applied on a DC cable (L12), an OHL (L13) and a hybrid line (L24) and the results are summarised in Table 7.2, Table 7.3 and Table 7.4, respectively. Each feeder has 200 km length, while faults with the same fault distances and fault resistances, (0, 300 and 500 Ω) have been simulated for each medium for direct comparison.

The fault location results demonstrate that the proposed fault location method can successfully estimate the fault distance for all medium types, while in the case of the hybrid line the reported fault location always corresponds to the correct faulted segment. A similar performance is achieved for both PTP and PTG faults in all cases. Moreover, the impact of fault resistance on the method's performance is minimal, since as explained in Section 7.2, fault resistance has a different effect on the frequency domain profile than the fault distance.

For the DC cable (L12), the maximum and average error for all fault cases is 0.175% (or 0.349 km) and 0.071% (or 0.142 km), respectively. The corresponding maximum and average error for the overhead line (L13) is 0.447% (or 0.893 km) and 0.154% (or 0.307 km). The increase in the fault distance estimation error for OHLs is attributed to the faster wave propagation that results in more dense travelling wave reflections and therefore, shorter data windows are obtained in Stage I of the method. Since, the

Table 7.2: Fault location results for line L12 (200 km cable).

Fault Distance [km]	Fault Resistance [Ω]	PTP Faults Estimated distance [km]	PTP Faults Error [%]	PTG Faults Estimated distance [km]	PTG Faults Error [%]
5	0	5.156	0.078	4.857	0.072
	300	4.651	0.175	4.650	0.175
	500	4.750	0.125	4.850	0.075
20	0	19.893	0.053	20.350	0.175
	300	19.652	0.174	20.052	0.026
	500	19.501	0.249	20.051	0.026
40	0	40.061	0.031	40.193	0.096
	300	40.051	0.025	39.951	0.024
	500	40.052	0.026	40.055	0.028
60	0	59.872	0.064	60.124	0.062
	300	59.602	0.199	60.205	0.102
	500	59.600	0.200	59.983	0.008
80	0	79.927	0.036	80.124	0.062
	300	80.007	0.004	80.054	0.027
	500	80.055	0.027	80.254	0.127
100	0	100.012	0.006	100.135	0.067
	300	99.863	0.068	99.953	0.024
	500	99.858	0.071	100.052	0.026
120	0	120.109	0.055	120.145	0.072
	300	120.061	0.031	120.054	0.027
	500	120.108	0.054	120.053	0.027
140	0	140.084	0.042	140.984	0.042
	300	140.062	0.031	140.052	0.026
	500	140.058	0.029	140.001	0.001
160	0	160.083	0.042	160.074	0.037
	300	160.260	0.130	160.031	0.016
	500	160.258	0.129	160.110	0.055
180	0	180.115	0.057	179.980	0.010
	300	179.956	0.112	180.262	0.131
	500	180.097	0.049	179.762	0.119
195	0	195.322	0.161	195.068	0.034
	300	195.232	0.116	195.652	0.326
	500	195.152	0.076	195.651	0.326
Average error [%]		-	**0.073**	-	**0.068**

Table 7.3: Fault location results for line L13 (200 km OHL).

Fault Distance [km]	Fault Resistance [Ω]	PTP Faults Estimated distance [km]	PTP Faults Error [%]	PTG Faults Estimated distance [km]	PTG Faults Error [%]
5	0	5.251	0.126	5.052	0.026
	300	5.052	0.026	5.051	0.025
	500	5.250	0.125	5.151	0.075
20	0	20.098	0.049	19.864	0.068
	300	19.862	0.069	20.105	0.052
	500	19.457	0.271	19.853	0.073
40	0	40.050	0.025	40.456	0.228
	300	40.102	0.051	39.852	0.074
	500	40.062	0.031	40.072	0.036
60	0	59.718	0.141	60.002	0.001
	300	59.559	0.221	59.753	0.124
	500	59.706	0.147	59.702	0.149
80	0	80.198	0.099	79.198	0.401
	300	79.350	0.325	80.225	0.112
	500	80.110	0.055	80.007	0.004
100	0	99.664	0.168	100.398	0.199
	300	99.398	0.301	99.838	0.081
	500	99.659	0.171	100.112	0.056
120	0	120.400	0.200	120.851	0.426
	300	120.199	0.100	120.582	0.291
	500	120.166	0.083	120.377	0.188
140	0	139.531	0.235	139.888	0.056
	300	139.932	0.034	140.454	0.227
	500	140.560	0.280	139.558	0.221
160	0	159.170	0.415	159.880	0.060
	300	159.926	0.037	160.688	0.334
	500	160.334	0.167	160.008	0.004
180	0	180.615	0.307	179.798	0.101
	300	180.712	0.356	180.661	0.331
	500	180.893	0.447	180.212	0.106
195	0	195.322	0.161	194.621	0.189
	300	194.553	0.223	195.572	0.214
	500	194.880	0.060	195.787	0.107
Average error [%]		-	**0.167**	-	**0.141**

Table 7.4: Fault location results for hybrid line L24 (100 km cable segment followed by 100 km OHL segment).

Fault Distance [km]	Fault Resistance [Ω]	PTP Faults Estimated distance [km]	PTP Faults Error [%]	PTG Faults Estimated distance [km]	PTG Faults Error [%]
5	0	4.858	0.071	4.854	0.073
	300	5.051	0.025	4.950	0.025
	500	4.971	0.015	4.950	0.025
20	0	19.834	0.083	20.102	0.175
	300	20.057	0.028	20.052	0.026
	500	20.034	0.017	20.051	0.026
40	0	39.999	0.001	40.123	0.061
	300	40.011	0.006	40.014	0.007
	500	40.059	0.030	40.125	0.063
60	0	59.971	0.015	60.151	0.151
	300	60.263	0.131	59.959	0.020
	500	60.063	0.032	60.055	0.028
80	0	80.017	0.009	80.316	0.158
	300	80.064	0.032	80.155	0.077
	500	80.059	0.029	80.152	0.076
95	0	94.909	0.045	95.297	0.148
	300	95.059	0.030	95.051	0.026
	500	95.454	0.227	95.050	0.025
105	0	105.191	0.096	105.055	0.027
	300	104.764	0.118	105.032	0.016
	500	105.704	0.352	105.071	0.036
120	0	120.058	0.029	119.705	0.147
	300	120.072	0.036	119.502	0.249
	500	119.881	0.059	120.151	0.075
140	0	139.811	0.094	139.256	0.372
	300	140.272	0.136	139.954	0.023
	500	139.993	0.034	140.112	0.056
160	0	159.697	0.151	160.453	0.227
	300	160.132	0.066	160.354	0.177
	500	160.233	0.117	160.251	0.126
180	0	179.996	0.002	179.852	0.074
	300	179.976	0.012	179.252	0.374
	500	180.310	0.155	179.320	0.340
195	0	195.095	0.047	194.231	0.385
	300	195.859	0.429	195.114	0.057
	500	195.737	0.368	194.251	0.375
Average error [%]		-	**0.087**	-	**0.117**

hybrid line L24 consists of a cable and an OHL segment of equal length, the average error of the proposed method lies between the corresponding estimation errors for L12 and L13. In particular, the maximum and average error for all fault cases is 0.429% (or 0.859 km) and 0.102% (or 0.204 km), respectively.

7.4.3 Fault Location Results for Greater Line Lengths

In order to asses the effectiveness of the proposed method for longer transmission lines, a series of PTP DC faults is applied every 25 km on cable L14 and OHL L34 of the test grid of Figure 7.9. The fault distance estimation errors for both sections, which have 500 km length, are illustrated in Figure 7.10.

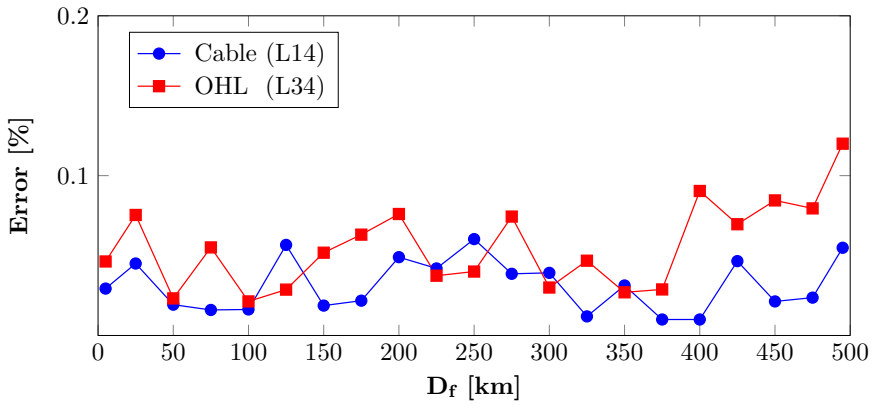


Figure 7.10: Fault location results for PTP faults ($R_f \approx 0\ \Omega$) on longer transmission media L14 (cable) and L34 (OHL).

It is evident that the estimation errors are significantly smaller in both cases, when compared to the corresponding results for their shorter counterparts (L12 and L13). In particular, the average error is 0.024% (or 0.118 km) for L14, and 0.056% (or 0.278 km) for L34. This is partly explained by the effect of the line length on the estimation error formula of (7.16). Nevertheless, longer transmission lines also result in longer available data windows for the proposed method due to the less dense travelling waves reflections, which in turn lead to more accurate fault distance estimations. It can be concluded that the proposed fault location method demonstrates superior performance for longer transmission lines.

7.4.4 Fault Location Results for a Three-segment Line

In this subsection, the fault location method is applied on a transmission line medium that comprises of three segments. For the purposes of this study, line L34 of the test grid of Figure 7.9 is replaced with a line that comprises of an 150 km OHL segment,

a 300 km cable segment, and a 150 km OHL segment. PTP faults at various points across the medium with fault resistance of 0, 300 and 500 Ω have been simulated and the results are shown in Figure 7.11.

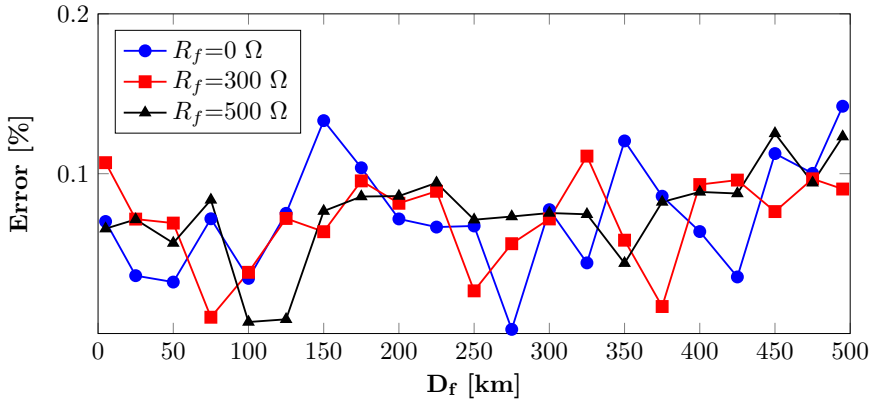


Figure 7.11: Fault location results for PTP faults on a three-segment transmission line medium.

The average and maximum error for all fault cases is 0.073% (or 0.366 km) and 0.1422% (0.711 km), respectively. In comparison to the results for the 500 km OHL that was considered in the previous subsection, it can be observed that the performance of the method is slightly degraded in terms of the errors in km (0.366 km average error as opposed to 0.278 km error for OHL). This behaviour is expected due to the higher number of segments of the transmission line, which suggests that the density of travelling wave reflections increases, thus leading to smaller available data sets. Nevertheless, the average estimation error remains low and it can be concluded that the method maintains its high accuracy for transmission mediums with several segments.

7.4.5 Impact of Sampling Frequency

Due to the dependence of the proposed fault location scheme on the length of the data window obtained through Stage I, it becomes apparent that the employed sampling frequency largely affects the performance of the method. In order to investigate this impact, cable section L12 and OHL section L13 are selected for applying PTP faults with R_f=0 Ω using 100 kHz (only for cables), 200 kHz, 500 kHz and 1 MHz sampling frequency. The estimation errors in each case are illustrated in Figure 7.12.

For both sections, it is evident that for increasing sampling frequencies the estimation error decreases. For decreasing sampling frequencies, the estimation error increases in all media due to the higher frequency of travelling wave reflections that lead to smaller data sets of post-fault voltage measurements. In detail, the average error for the cable segment is 0.08% (or 0.161 km) for 200 kHz, 0.06% (or 0.12 km)

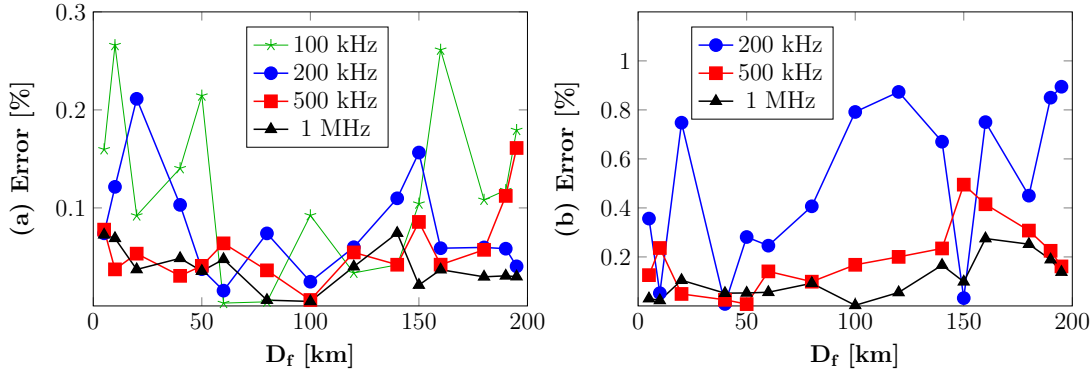


Figure 7.12: Fault location results for different sampling frequencies for (a) cable L12 and (b) OHL L13 (PTP faults with $R_f \approx 0\ \Omega$).

for 500 kHz and 0.0389% (or 0.078 km) for 1 MHz. The corresponding results for the OHL segment are 0.494% (or 0.988 km), 0.193% (or 0.386 km) and 0.106% (or 0.212 km), respectively.

A sampling frequency of 100 kHz is also possible for the execution of the method for DC cables and the resulting average error is 0.1203% (or 0.243 km). Nevertheless, use of 100 kHz sampling frequency is not possible for locating DC faults in OHLs due to the significantly reduced data windows, especially for faults close to line ends in which Stage III of the algorithm fails to construct a frequency domain profile. It can be concluded that even lower sampling rates can be used for estimating the fault distance with high accuracy for faults on DC cables, but for overhead lines, a minimum sampling rate of 500 kHz is required to ensure an average estimation error within ±0.4 km. It is worth reiterating that DC voltage measurement with sampling frequencies in the order of 500 kHz is considered readily accessible (see Section 3.6).

7.4.6 Impact of Noisy Measurements

In order to further scrutinise the performance of the proposed method, the impact of noise is considered. In particular, the simulations for PTP faults with R_f=0 Ω on line L12 are repeated and the DC voltage measurements are subjected to artificial noise with increasing amplitude in order to obtain Signal-to-Noise Ratios (SNR) of 30, 20 and 10 dB (lower dB values correspond to higher noise level). Figure 7.13 depicts the results in terms of the fault distance estimation error for each SNR along with the original test case (SNR=∞).

It can be observed from Figure 7.13 that in the majority of the cases the noisy measurements have limited effect on the final fault distance estimation. The largest deviation in the final estimation is noticed in the case of a PTP DC fault at 40 km,

in which the absolute relative difference between the original test case and the corresponding case for SNR=10, is 0.222% (or 0.444 km). In Table 7.5, the average and absolute maximum error for each SNR are also summarised. It is evident that both average and maximum errors present a marginal increase for increasing noise levels. The results demonstrate that the proposed scheme is sufficiently robust against noisy measurements. This advantage of the technique is attributed to the inherent capability of SIRV to accurately construct the transfer function (frequency domain profile) even when the input signal is contaminated with noise.

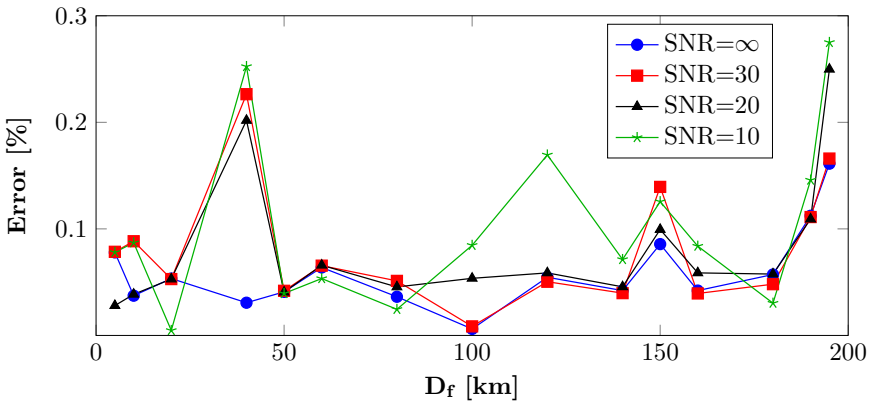


Figure 7.13: Fault location results for different SNR ratios (PTP faults with $R_f \approx 0\ \Omega$).

Table 7.5: Average and maximum errors for varying levels of noise.

Case	Average Error	Max Error
SNR=∞	0.0601	0.1612
SNR = 30	0.0804	0.2264
SNR = 20	0.0805	0.2498
SNR = 10	0.0817	0.2690

7.4.7 Impact of Transmission Line Loading

In this subsection the performance of the method for varying transmission line loading conditions is evaluated. The power set-points of the converters have been modified appropriately to achieve different DC current and hence, different loading conditions for the DC cable L12 and the OHL L12. Using this approach, the power transfer across the mediums is adjusted to 100, 300, 500 and 700 MW. Solid PTP faults are applied on both L12 and L13 and the estimation errors are shown in Figure 7.14. It is observed, that loading conditions have minimal effect on the fault location estimations for both mediums. This outcome is expected as the proposed technique primarily utilises TW

principles, and the behaviour of TWs is hardly affected by the loading conditions of the transmission medium. It is worth reiterating that only voltage measurements are required for the execution of the proposed method.

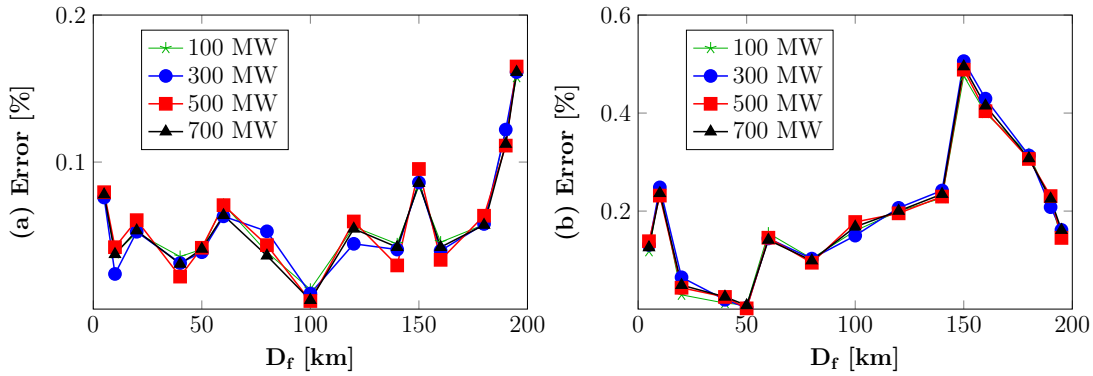


Figure 7.14: Fault location results for varying loading conditions of Line L12 (PTP faults with $R_f \approx 0\ \Omega$).

7.4.8 Comparison with Existing Methods

In order to clearly show the advantages of the proposed method, a comparison of its performance in relation to other techniques reported in the technical literature is pursued in this subsection. Table 7.6 cites the results of the compared methods in terms of number of fault cases, average and maximum errors (in km), sampling rates, fault resistance ranges, and data window sizes. From the methods that were considered in Section 3.5, only work in which the fault location estimation results are cited in numbers are used for the analysis in this subsection. In an effort to perform a fair comparison among all considered methods, only the baseline fault location results are taken into account, while the corresponding results of sensitivity analyses in terms of noise contamination and sampling frequency (which are not available for all methods) have been neglected. Similarly, only the results of Subsections 7.4.2 and 7.4.3 have been considered for the proposed method.

The results of the comparison confirm the high accuracy of the proposed technique, which demonstrates the second best performance in terms of average error in km, outperformed only by the method in [220]. Similarly, the method presents a satisfactory maximum error in comparison to the other techniques. It is worth mentioning at this point that the work presented in this chapter was rigorously tested across a wide range of operational conditions and fault cases (256), and only the method in [280] has considered a higher number of fault cases (336). In terms of sampling frequency requirements, the proposed method utilises a moderate sampling rate, while the corresponding rates

used in the rest methods range from 10 to 2000 kHz. Moreover, the maximum fault resistance considered in this chapter is at least equal or higher than the ones considered in other reported work. Resiliency against resistive faults is also a significant advantage of the proposed solution, which along with the method presented in [281], are the only ones that exhibit similar accuracy regardless of the DC fault resistance.

Table 7.6: Comparison between the proposed method and other existing fault location methods for HVDC systems.

Method	Fault Cases	Average Error [km]	Maximum Error [km]	Sampling rate [kHz]	Max R_f [Ω]	Resilient to R_f	Data size [ms]
[220]	72	0.112	0.36	2000	100	×	-
[235]	18	0.314	0.93	200	70	N/A	16
[224]	20	0.351	1.60	10	100	N/A	5
[225]	33	1.418	2.90	100	50	N/A	10
[222]	51	0.249	0.78	1000	500	×	17.76
[230]	105	1.461	16.05	80	100	×	10
[280]	336	0.323	2.58	20	500	×	5
[281]	19	0.367	0.49	1000	500	✓	N/A
[232]	100	14.5	28.45	20	100	N/A	10
[229]	59	2.92	7.89	100	500	×	12
Proposed	**256**	**0.214**	**0.86**	**500**	**500**	✓	**<2**

One of the most significant benefits of the proposed technique is that the required data window size is very limited (less than 2 ms). This attribute is considered particularly advantageous in fault location applications for HVDC grids, where the available fault records are confined by the operation speed of DCCBs, i.e. 2-8 ms for hybrid and mechanical DCCBs (see Section 2.5). It is indicative that in the test system considered in this chapter, in which the breaker operation speed is equal to 2 ms, none of the existing techniques cited in Table 7.6 would have the required number of samples to be successfully executed.

The methods presented in [220] and [235] are the only ones in the literature which have considered hybrid transmission lines. In comparison to [235], the method presented in this chapter performs better in all categories of Table 7.6. However, the method in [220] demonstrates higher accuracy in fault location estimation. Nevertheless, as it was revealed in Section 3.6, a sampling rate of 2 MHz cannot be easily achieved by existing HVDC measuring instruments. Furthermore, like any other single-ended TW-based method, wave head identification in [220] becomes harder in case of highly-resistive faults due to the attenuation caused on the TWs. In conclusion, it can be argued that the proposed method achieves a satisfactory trade-off between accuracy, resiliency to fault resistance and sampling frequency requirements.

7.5 Summary

In this chapter, two major challenges of fault location for HVDC grids have been identified. The first challenge arises from the recent trend for utilisation of fast protection systems for DC fault management in HVDC grids that lead to very short time-frames between fault inception and fault clearance and confine the available data set for executing fault location algorithms. The second challenge is associated with fault location estimation in hybrid transmission media, an issue that has generally received very limited attention. It has been pointed out that most of existing fault location methods proposed in the literature fail to deal with these challenges effectively.

To solve these problems, an advanced single-ended fault location method is presented that is suitable for locating DC faults in HVDC grids that are characterised by short post-fault data windows due to the use of high-speed DC breakers and fast acting protective actions. A frequency domain analysis of transient voltage at the point of measurement has revealed that fault distance and fault resistance introduce distinct features on the voltage profiles. Exploiting these features, a genetic algorithm driven method is employed to calculate the optimum fault distance that produces a theoretical voltage profile that best matches the voltage profile of the existing fault case. The mathematical formulation of travelling wave principles in conjunction with the flexibility offered by the genetic algorithm allow for accurate DC fault location estimation even for hybrid transmission media with an arbitrary number of segments.

A simulation-based analysis has demonstrated the effectiveness and the high accuracy of the method for any transmission line geometry across a wide range of DC fault cases including both pole-to-pole and pole-to-ground faults with up to 500 Ω fault resistance. Using 500 kHz sampling frequency, the average fault distance estimation error has been found to be 0.071% for a cable, 0.154% for an overhead line and 0.102% for a hybrid transmission line (OHL and cable segments), each with a length of 200 km. Moreover, the accuracy of the method improves for longer transmission lines due to the availability of larger measurement data sets. It was demonstrated that the proposed method maintains its high accuracy for transmission line mediums comprising of several segments (average error of 0.073% in a 500 km three-segment line). Further sensitivity analysis revealed that the scheme is robust against noise and different loading conditions, while also it has been shown that lower sampling frequencies can be used for locating DC faults in cable sections. Nevertheless, the use of a higher sampling frequency is advantageous in the case of overhead lines. Finally, a comparison with existing techniques in the technical literature revealed that the proposed method demonstrates enhanced accuracy in terms of both average and maximum error in fault location estimation.

Chapter 8

Conclusions and Future Research

HVDC grids are expected to be an integral part of future power networks towards the achievement of a net zero future through the better utilisation and integration of massive amounts of renewable energy into the interconnected AC networks, while offering a plethora of attractive features such as enhanced controllability, flexibility and redundancy, improved reliability and security, and lower investment costs. However, as with any developing technology, the HVDC grid concept is also accompanied with significant challenges, with the requirement for effective protection and fault location solutions being one of the most prominent. HVDC protection is of utmost importance to ensure the necessary reliability and security of HVDC grids, yet very challenging due to the fast nature of development of DC faults and the abrupt changes they cause in currents and voltages across the entire network that may damage the system components. In addition, timely and accurate fault location is required to minimise power outage time and elevate the total availability of the HVDC grid.

Therefore, this thesis has provided the necessary methodologies and concepts for non-unit protection design, and the implementation of protection algorithms and fault location techniques to promote the deployment of highly meshed multi-vendor HVDC grids. These concepts include: i) a technology review of DC current and voltage measuring devices from the perspective of enabling HVDC protection and fault location, ii) analytical design, development and demonstration of generally applicable non-unit protection algorithms, iii) a fault management strategy for enhanced technical and economical feasibility of HVDC grids, and iv) an enhanced fault location method for HVDC grids embedding fast acting protection equipment and/or heterogeneous transmission line media. This chapter concludes the thesis by first summarising the contributions and general outcomes of the conducted research, and second providing potential directions for future research in HVDC protection and fault location areas.

8.1 Conclusions

The new knowledge produced from the research work presented in this thesis can be condensed in four main themes, which are subsequently described in detail.

8.1.1 Identifying the Capabilities of Existing Measuring Instruments for HVDC Protection and Location Applications

A technology review of voltage and current measuring devices has been performed from the perspective of enabling HVDC protection and fault location in HVDC grids. The review in conjunction with the mapping of the sampling frequency requirements of existing DC fault detection and location solutions on a frequency diagram against the bandwidth of existing technologies have provided valuable insight into selecting measuring equipment for achieving the required sampling rate. In contrast to current measurements, it has been established that voltage measurements for HVDC applications are considered readily accessible, indicating a competitive advantage of protection solutions that are based exclusively on voltage signals. For DC current measurement, there is a wider variety of options and the final selection of the suitable technology depends primarily on the required application.

It has been shown that fault detection and protection methods are mainly concentrated in a frequency spectrum ranging from a few kHz to 100 kHz, while fault location methods require measurements with a frequency range starting from 100 kHz and reaching up to 2 MHz. It is argued that since both applications are required to be executed in parallel in HVDC grids, a convergence in their sampling frequency requirements is desirable to ensure that common measuring instruments are employed. Based on the analysis, such a convergence is achieved for sampling frequencies around 100 kHz that concentrate a significant proportion of the fault detection and location functions. Such a sampling frequency can be achieved from both voltage and current measuring technologies that are commercially available. Furthermore, this finding is identified to be well aligned with the IEC 61869-9 standard, which recommends the use of 96 kHz with specific reference to DC protection and fault location applications.

8.1.2 Analytical Design and Development of Generally Applicable and Optimised Non-Unit Protection Algorithms

Having identified the main challenges, requirements and design aspects of HVDC grid protection, it has been established that high-speed protection algorithms which should be ideally based exclusively on local measurements are required due to the stringent time scales for DC fault clearing. Furthermore, the corresponding review on the exist-

ing protection algorithms revealed that there is an ongoing research activity towards the development of non-unit protection methods that utilise travelling wave principles. It has been observed that the vast majority of the developed solutions are designed based on extensive offline simulations using specific HVDC test systems in EMT-type software. This raises concerns with regards to their general applicability to any HVDC network. Moreover, it has been highlighted that in the absence of a common framework for the design of non-unit protection methods, their interoperability with other protection equipment (DCCBs, IEDs etc.) is not necessarily guaranteed. To overcome these limitations, a more fundamental approach to the design and development of generally applicable non-unit protection algorithms is proposed in this thesis, the conclusions of which are presented in the following two subsections.

Development of Generalised Design Guidelines for Non-unit Protection

A new and generalised methodology is proposed for facilitating the design of travelling wave based non-unit protection algorithms for HVDC grids. The approach uses frequency domain analysis on strategically selected fault scenarios for performing a comprehensive investigation of the parameters that influence HVDC grid non-unit protection, and providing design guidelines. The general applicability of the methodology is ensured by basing the analysis on a generic HVDC grid section, in which only local parameters in the vicinity of the protection relay are required to be known. Such an approach eliminates typical issues associated with time domain simulations using standard EMT-type software, such as the use of a single network for the validation of protection algorithms. Moreover, it enables flexible and systematic investigation of grid and fault parameters that influence the voltage response for both internal and external faults. It has been shown that the proposed methodology can play an instrumental role for the design of travelling wave based non-unit protection algorithms which can be easily configured for any grid topology and grid parameters, while also considering multi-vendor aspects. In particular, based on the relevant analysis, the following recommendations have been formed to facilitate non-unit protection design:

- The critical frequency beyond which the impact of forward internal faults becomes more pronounced than that of external faults can be evaluated. This frequency serves as an indicator for selecting the appropriate sampling frequency and defining the filtering requirements.
- An approach for analytically deriving the protection threshold based exclusively on the prevailing local system conditions is provided.

- A complementary tool for selecting series inductor sizes is proposed with the aim to improve protection margins.
- Flexible configuration of algorithm-specific settings (for any method that may be selected) is facilitated by the proposed methodology which can be used to develop appropriate quantitative metrics for identifying the corresponding settings that ensure optimised protection performance.
- The proposed methodology supports the deployment of multi-vendor HVDC grids with optimised protection systems, and renders the configuration of the selected non-unit protection methods immune to varying system conditions.

Design and Implementation of WT-based HVDC Non-unit Protection with Optimised Selectivity and Protection Reach

A fast acting, single-ended and easily configurable non-unit protection scheme based on wavelet transform with optimised settings for enhanced protection reach and discrimination capabilities is developed in this thesis. The generalised approach introduced for configuring and implementing a WT-based solution specifically tailored for HVDC non-unit protection overcomes key technical barriers that have impeded the use of WT in practical protection applications. Example of such barriers include the complexity in design due to the multitude of WT-related parameters, and the common erroneous concept that WT implementations are characterised by increased computational burden.

To remove these barriers, an analytical approach that is adaptable to any HVDC grid topology has been developed for the first time for deriving all main WT parameters based on the methodology and the design guidelines described in the previous subsection. The key WT parameters are flexibly determined for each relay separately according to the prevailing local system conditions in order to achieve enhanced protection margins for the WT-based solution, while ensuring reduced computational requirements. This approach eliminates the need for extensive offline simulations for designing a WT-based method which is the current practice in the literature, and ensures optimised protection performance regardless of which transmission media, DCCB and converter technologies or grid topologies are employed.

An efficient SWT algorithm is also developed for real-time applications based on discrete convolution. The performance of the method has been demonstrated through both offline simulations in PSCAD/EMTDC and real-time simulations using a digital real-time simulator and a low-cost hardware prototype. The latter constitutes the first attempt for experimental implementation of SWT for HVDC protection applications.

Through these studies, the following conclusions have been drawn:

- The high-speed performance of the WT-based non-unit protection algorithm has been demonstrated. In detail, depending on the fault resistance and location, the method operates within 20-120 μs for faults on a 200 km cable, and within 120-310 μs for faults on a 350 km cable.
- It has been found that the proposed method can provide reliable and enhanced selective protection even against high-resistance DC faults (more than 500 Ω). Similar performance is achieved for both pole-to-ground and pole-to-pole faults. Moreover, the real-time simulation studies proved the method's enhanced dependability with the rate of successful correct operations being 100%, and high security with the method remaining stable under all external fault scenarios.
- Noise immunity is revealed to be one of the main advantages of the proposed technique. The employed WT configuration methodology achieves dynamic adjustment of the filtering applied to voltage measurements in an effort to extract the most valuable frequency content for discriminating internal faults. On this basis, the relative effect of noise on the generated WT coefficients is mitigated.
- The WT-based solution has been successfully implemented and executed at a sampling rate of 100 kHz, which is in line with the recommendation provided from the review of DC instruments. Further sensitivity analysis showed that the method remains highly selective for lower sampling rates (down to 10 kHz).
- A comparison of the proposed method against the widely used ROCOV (dv/dt) demonstrated a remarkable increase in the range of 4-6 times in protection margins and resilience against highly-resistive DC faults for all sampling rates that were examined.
- The hardware-in-the-loop real-time simulations have taken into consideration data acquisition issues and computational aspects of the technique, and provide a high level of confidence that the proposed method is efficient, practical and cost-effective.

8.1.3 Fault Management Strategy for Improving the Technical and Economical Feasibility of HVDC Grids

In an effort to meet the requirement for security of supply in HVDC grids, while also maintaining the total system cost at reasonable levels, a detailed DC fault management strategy is introduced for resilient HVDC grids incorporating CH-MMCs. The

CH-MMC is an efficient topology equipped with a limited number of FB-SMs that demonstrates partial fault tolerant capability. Adoption of the CH-MMC is motivated by an attempt to lower protection-related costs, by devising alternative ways in which the expensive fast acting hybrid DCCBs can be replaced with slower but inexpensive mechanical DCCBs.

The functions of the developed fault management strategy include coordination with local protection relays, coordination with DCCB actions, activation of the appropriate converter actions depending on whether a pole-to-pole or pole-to-ground fault is detected by the relays, and communication with the central grid controller for remedial grid restoration measures, (required only for pole-to-ground faults). In addition, the FMS monitors the FB chain-link voltages in order to instruct bypassing of the FB-SMs, if the specified over-voltage limit is exceeded. Detailed transient simulation studies have shown that the proposed fault management strategy allows for the continuous operation of the HVDC grid during pole-to-ground faults, and the fault tolerant operation with minimum power flow interruption under more severe pole-to-pole DC faults. In detail, the analysis revealed the following features of the strategy:

- The current limiting modes of the CH-MMC enable the extension of fault clearance times to levels compatible with the operation times of mechanical DCCBs, and significantly reduce the magnitude of line and converter arm currents during pole-to-pole DC faults.

- It has been shown that the current suppression capability of the CH-MMC can replace or minimise the required current-limiting role of series inductors, thus further reducing the cost and footprint of mechanical DCCBs. In detail, use of CH-MMCs with 25% ratio can lead to up to 40.5% reduction in peak fault currents when series inductors of only 50 mH are used.

- Parametric studies demonstrated that a 25% ratio of FB-SMs with respect to the total number of SMs per arm is adequate for the proper operation of the proposed strategy and its effective coordination with DCCBs.

- For pole-to-pole faults, the strategy results in significant improvement in converter and overall system response with respect to conventional HB-MMC based HVDC grids. In detail, voltage and power recovery times can be reduced by up to 35% and 50.3%, respectively.

- During pole-to-ground DC faults, the strategy ensures that all converters retain control of active and reactive power exchange with the AC grids. At least half of the rated power capability can be maintained leading to faster post-fault power

flow restoration. Furthermore, over-voltage of the healthy pole is avoided, and the DC voltage stress on converter transformers is mitigated by 25%.

- The strategy is not dependent on high-speed fault detection and discrimination algorithms. For illustration, a simplified non-unit protection method based on under-voltage and du/dt with a sampling frequency of 20 kHz was selected and found to be more than adequate.

- A quantitative and qualitative comparison for various ratios of FB-SMs to total SMs highlighted that the proposed strategy offers several avenues for performance optimisation of HVDC grids integrating CH-MMCs. Therefore, the strategy can be tailored according to the practical design considerations and broader system operational objectives in order to achieve a trade off between cost and the desired degree of fault-ride through capability.

8.1.4 Accurate Fault Location Method for HVDC Grids with Minimal Time Window Requirements

A novel single-ended frequency domain fault location method with improved accuracy is developed, which overcomes issues that are anticipated to be faced in future large scale HVDC grids. An extensive review on existing fault location methods highlighted that there is a range of options for locating DC faults in HVDC systems, nevertheless, the following identified challenges have not been adequately addressed:

- Current methods are either designed for point-to-point HVDC links in which large post-fault measurement data sets are available due to the slower response of their protection systems, or are designed for HVDC grids but have ignored the impact of high-speed DCCBs on the data window length.

- The application of fault location methods for heterogeneous transmission line media (or hybrid lines) that have segments of both cable and overhead lines has received very limited attention.

To address the above challenges, the proposed method is designed to operate based on an adjustable limited post-fault data window that is selected based on the available time frame between fault inception and subsequent events arising from the actions of high-speed DCCBs or other protection equipment. The same generic HVDC grid section used for the generalised non-unit protection design is employed and used as the fundamental starting point for the design of the technique, thereby ensuring its applicability for a wide range of HVDC grid equipment that may be selected during the project design stage, and its suitability in a multi-vendor environment. Based on

the available post-fault voltage traces, a frequency domain voltage profile is initially constructed, which is then iteratively evaluated against theoretical voltage profiles using a routine based on a genetic algorithm regime. The mathematical formulation of travelling wave principles in conjunction with the flexibility offered by the genetic algorithm allow for accurate DC fault location estimation for cables, OHLs and hybrid transmission media of an arbitrary number of segments. An extensive simulation-based analysis has demonstrated the effectiveness of the method across a wide range of DC fault cases, and has revealed the following key features:

- The proposed fault location method has been found to provide a high level of accuracy for any transmission line geometry including hybrid lines, and for both pole-to-pole and pole-to-ground faults. A comparison with existing techniques in the technical literature revealed that the method demonstrates improvements in terms of both average and maximum error in fault location estimation.

- Using 500 kHz sampling frequency, the average error in fault distance estimation was observed to be 0.071% for a cable, 0.141% for an overhead line and 0.094% for a hybrid transmission line, each with a length of 200 km. Furthermore, an average estimation error of 0.1422% has been observed for a three-segment line with 500 km length.

- A sensitivity analysis of the employed sampling frequency revealed that relatively accurate fault location estimation ($\approx$0.15% error) can be achieved at 100 kHz for faults on DC cables, but use of 500 kHz is recommended for applying the method for overhead lines. Nevertheless, one of the merits of the proposed method is that it relies exclusively on voltage signals, for which sampling rates in the order of 500 kHz can be readily achieved by the available voltage measuring technologies.

- In contrast to most existing methods, the proposed solution demonstrates increased resiliency against highly resistive faults. In detail, fault resistances up to 500 Ω have been found to have no effect on fault distance estimation.

- Due to the availability of longer data windows when faults at greater fault distances are required to be located, the performance of the fault location method is improved for longer transmission line media.

- The proposed scheme is robust against noisy measurements as fault location estimation errors remain unchanged for varying noise levels in voltage measurements.

- The comparison with existing methods showed that most techniques utilise data windows of 10 ms or more. On the contrary, the proposed method requires only

limited post-fault records (less than 2 ms), and is therefore practically applicable to HVDC grids that employ high-speed circuit breakers with opening times in the range of 2-8 ms.

8.2 Future Research

Based on the conducted research, several areas for future work have been identified. Therefore, potential research directions are highlighted in the following paragraphs.

8.2.1 Further Assessment of Sampling Frequency Requirements for HVDC Grid Protection and Location

The use of common voltage and current measuring devices is suggested in this thesis for both protection and fault location applications, which implies a need for convergence in their respective sampling frequency requirements. Based on current solutions, this convergence seems to occur at a sampling rate around 100 kHz, which has been identified to be suitable for many DC applications, with the exception of detailed fault location methods that typically require finer capture of fault transients. Therefore, further investigation of the adequacy of this rate for analysing transient phenomena for HVDC grid protection and fault location applications is proposed for future research.

8.2.2 Extending Frequency Domain Analysis

This thesis presented a methodology that contributed to the development of generalised design guidelines for voltage-based non-unit protection methods. The frequency domain analysis can be extended to current signals to provide further guidelines primarily for unit protection algorithms, such as travelling wave differential or other travelling wave based methods. Furthermore, the analysis focused exclusively on faults on the DC-side of HVDC grids to uncover the key factors that influence discrimination between internal and external DC faults. Although it has been shown through the evaluation studies of the proposed WT-based protection solution that external disturbances do not lead to erroneous operation of the algorithm, this may not hold true for other non-unit methods or for special cases of grid topologies and configurations. Representation of external disturbances (AC faults, power changes, line disconnections etc.) in the frequency domain will enable their investigation and ensure robustness of the selected method against such events.

8.2.3 Development of Back-up Protection Measures

The non-unit protection solution and the fault management strategy proposed in this research concern exclusively primary protection system actions. Back-up protection has received limited attention in the open literature and typically it is assumed to be achieved via AC-side equipment which need several cycles to operate. Consequently, further research is required to develop fast and effective back-up protection algorithms and strategies. In addition, the effect of breaker failure and other events that activate backup protection on the operation of the proposed fault management strategy should be further investigated to identify any modifications required to accommodate back-up protection measures, thereby ensuring survival of the HVDC grid.

8.2.4 Investigation of Fault Location Under Non-optimal Conditions

As follow-up research for the proposed fault location solution presented in this thesis, the performance of the method under non-optimal conditions could be investigated. In order to accurately estimate the fault position, the proposed method requires prior knowledge of the transmission medium characteristics it is applied to. Consequently, any discrepancy in the transmission line parameters that may result from degradation or ageing of the medium will have a direct effect on the proposed solution. A sensitivity analysis of cable/line parameter variations (e.g. wave speed, thickness and other characteristics of insulating/conducting layers etc.) is hence required to assess the consequences of potential discrepancies and determine any mitigation actions that can be applied. If available, actual transient fault record data over the lifespan of a transmission line can be used for facilitating this analysis.

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Appendices

Appendix A

Equivalent Converter Models for FDA

This appendix describes the approach which can be used to represent different converter topologies in the frequency domain. The presented equivalent models are only valid during the initial transient period of PTP DC faults after the arrival of the first incident travelling wave that travels from the fault location to the converter terminal. This short period is sufficient for the purposes of frequency domain analysis that is used in Chapter 4 for designing high-speed non-unit protection algorithms.

A.1 Equivalent Model of Two-Level Converter

Figure A.1 shows the equivalent model of the two-level converter in the frequency domain. In the transient stage of a PTP DC fault, the two-level converter can be regarded as a controlled current source as the drop of DC-link voltage is still relatively small. As a result, the grid current contribution can be ignored during this short period and the two-level converter can be regarded as a parallel connected capacitor for the purposes of frequency domain analysis. The equivalent converter impedance Z_{conv} is given by:

$$Z_{conv} = 1/sC \tag{A.1}$$

where C is the total DC-link capacitance. It is worth noting that this representation is also valid for NPC converters and any other converter topology that contains a central DC-link capacitor.

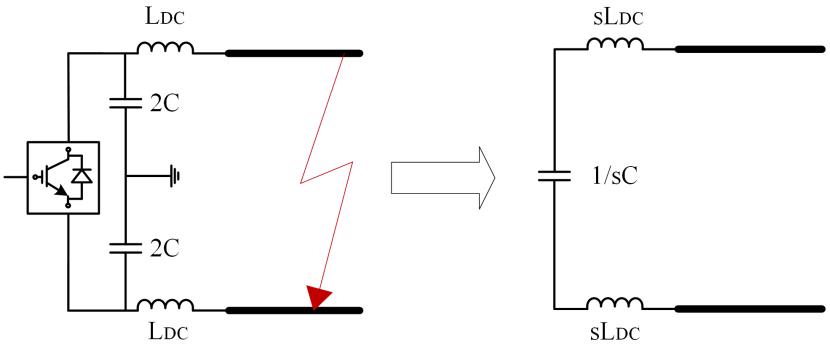

Figure A.1: Equivalent model of the two-level converter in the frequency domain.

A.2 Equivalent Model of MMCs

Figure A.2 shows the equivalent model of MMC topologies in the frequency domain. This model is valid for the most commonly used HB-MMC, FB-MMC and H-MMC, as well as for the CH-MMC described in Chapter 6. The fault current contribution of a MMC topology in the initial stage of PTP DC faults is governed by the discharge of the distributed capacitors contained in the sub-modules of the converter. This is because the MMC remains operational in the transient stage of PTP DC faults and hence, there is initially no current contribution from the AC-side of the converter. In this case, the upper and lower arm currents in each phase are almost identical and all three legs of the converter carry a part of the DC fault current.

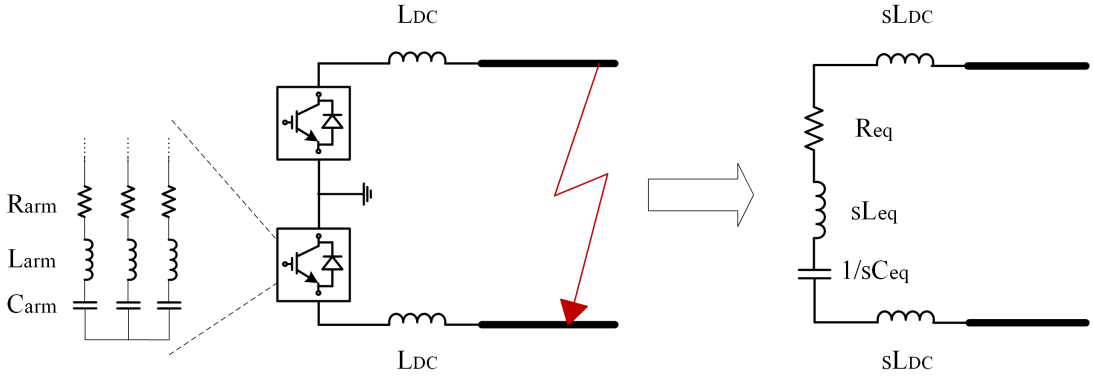

Figure A.2: Equivalent model of MMCs in the frequency domain.

As shown in Figure A.2, the converter impedance can be approximated as a series RLC model:

$$Z_{conv} = R_{eq} + sL_{eq} + 1/sC_{eq} = \frac{2}{3}R_{arm} + s\frac{2}{3}L_{arm} + \frac{1}{s3C_{leg}} \tag{A.2}$$

where R_{arm} and L_{arm} are the converter arm's resistance and inductance, respectively, while C_{leg} is the total capacitance of a converter leg, Assuming exactly half of the total SMs per converter leg remain connected at all times during normal operation of the converter, then C_{leg} is equal to arm capacitance C_{arm}.

A.3 Equivalent Model of LCCs

The work presented in this thesis including the application of frequency domain analysis has focused on VSC topologies, which have been identified in Chapter 2 to be more suitable than LCCs for facilitating the deployment of large-scale meshed HVDC grids. Nevertheless, as HVDC grids in the future may develop organically based on initially independent HVDC systems, it is likely that hybrid LCC-VSC systems will emerge as is the case in the Wudongde three-terminal system in China [195].

Frequency domain analysis can be extended to LCC-based or hybrid VSC-LCC systems. Accordingly, the equivalent model of LCCs in the frequency domain is shown in Figure A.3. During the transient stage of PTP faults in a LCC-based system, the converter's control system has not responded yet. Therefore, the equivalent model reflects the response of the DC-side system to the DC fault, and the fault component from the AC grid can be neglected for the fault analysis during this stage. As shown in Figure A.3, the converter impedance can be approximated by [193]:

$$Z_{conv} = sL_{th}//Z'_f = (2sL_{SR} + sL_l)//Z'_f \tag{A.3}$$

where Z'_f is the series combination of DC pole filters Z_f (typically series LC filters), L_{SR} is the smoothing reactor per system pole, and L_l is the leakage inductance of the three-phase transformer.

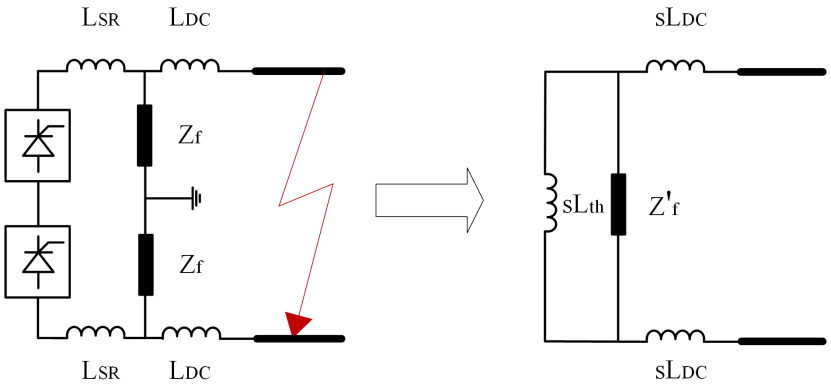

Figure A.3: Equivalent model of LCCs in the frequency domain.

Appendix B

Average Modelling of the CH-MMC

This appendix describes the averaged model for the CH-MMC that was used for the conduction of the electromagnetic transient simulation studies in Chapter 6.

Similar to HB-, FB- and H-MMCs, the CH-MMC practically adheres to the same fundamental operating principles during normal operation. As a result, the same assumptions made in Subsection 2.2.5 of Chapter 2 for the development of the HB-MMC averaged model, also apply to this MMC topology. In practice, the CH-MMC is similar in structure with the H-MMC as it also contains a HB chain-link and a FB chain-link in each arm of the converter. The principal difference is that instead of an equal number of HB-SMs and FB-SMs, the CH-MMC can have an arbitrary ratio R, i.e. the ratio of FB-SMs to the total number of sub-modules.

In the average CH-MMC model, the HB chain-link is represented in a similar manner as in the HB-MMC (see Subsection 2.2.5). Additional power electronic switches in a full bridge configuration are included to represent the FB chain-link. Both the FB and HB chain-links are shown in Figure B.1 that illustrates the averaged CH-MMC model for a single leg (phase). The additional full bridge in each arm is introduced to mimic the collective response of the FB-SMs during normal operation and converter blocking. In normal operation, auxiliary IGBTs S1 and S4 are turned on for synthesis of positive voltages, while IGBTs S2 and S3 are turned on for synthesis of negative voltages.

In analogy to the HB-MMC averaged model, controlled voltage and current sources are also used in each arm of the CH-MMC model. In the following analysis, N_{SM} is the number of total SMs, N_{HB} is the number of HB-SMs and N_{FB} is the number of FB-SMs in each converter arm. Moreover, V_{HBSM_j} is the HB-SM capacitor voltage of the j^{th} sub-module (with $j \in [0, N_{HB}]$), V_{FBSM_k} is the FB-SM capacitor voltage of the k^{th} sub-module (with $k \in [0, N_{FB}]$), and symbols U and L are used to refer to the upper

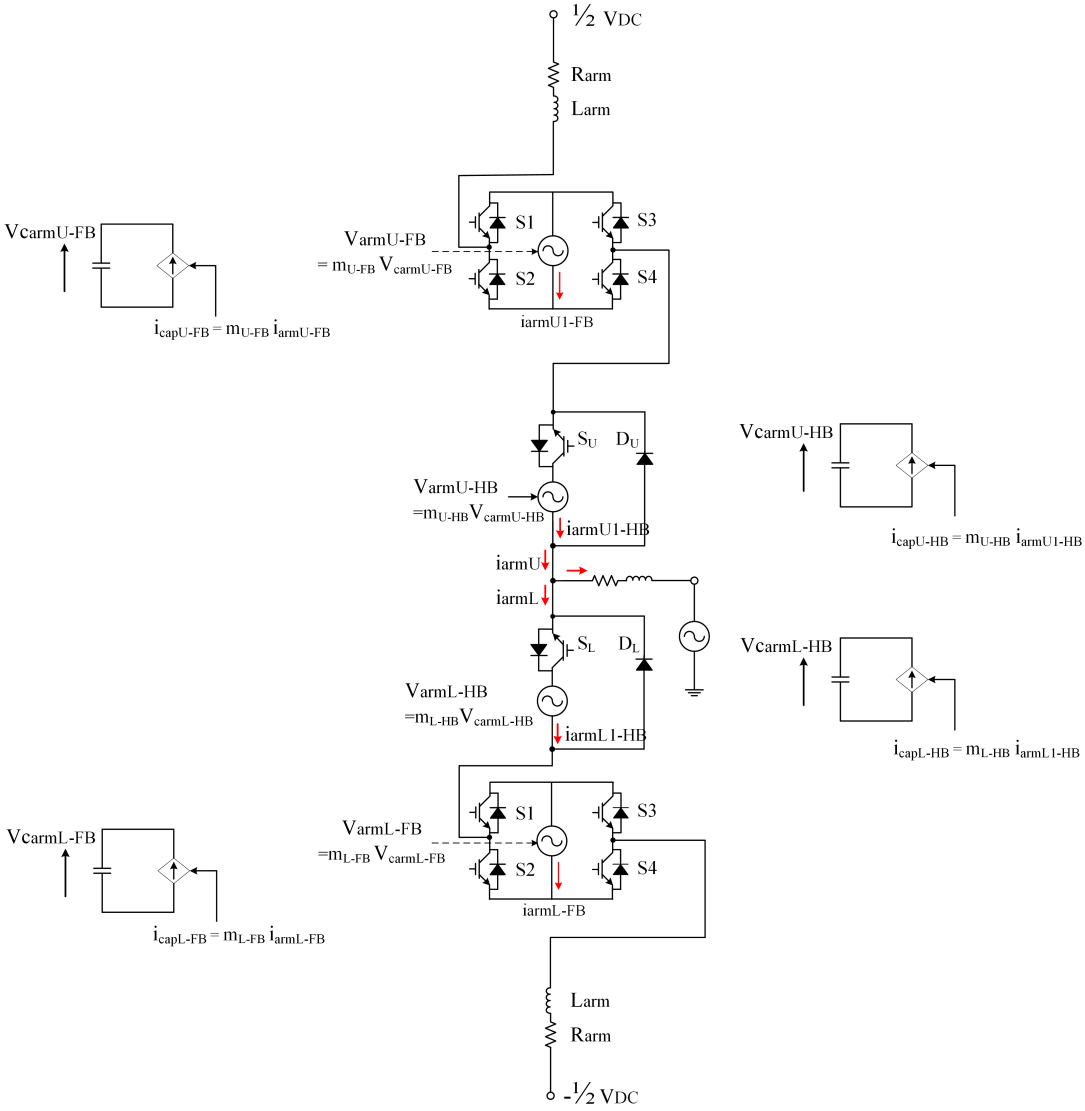

Figure B.1: Illustration of one phase of the CH-MMC average model.

and lower converter arms, respectively. Since the analysis is valid on a per phase basis, the phase notation (A,B and C) is omitted. The switching voltages across the upper arm and lower arm of the MMC, $V_{armU-HB}$ and $V_{armL-HB}$ for the HB chain-links, and $V_{armU-FB}$ and $V_{armL-FB}$ for the FB chain-links can be represented by their average voltages as follows:

$$\begin{cases} V_{armU-HB} = \sum_{j=1}^{N_{HB}} V_{HBSMU_j} \approx V_{carmU-HB} \cdot m_{U-HB} \\ V_{armL-HB} = \sum_{j=1}^{N_{HB}} V_{HBSML_j} \approx V_{carmL-HB} \cdot m_{U-HB} \end{cases} \tag{B.1}$$

$$\begin{cases} V_{armU-FB} = \sum_{k=1}^{N_{FB}} V_{FBSMU_k} \approx V_{carmU-FB} \cdot m_{U-FB} \\ V_{armL-FB} = \sum_{k=1}^{N_{FB}} V_{FBSML_k} \approx V_{carmL-FB} \cdot m_{U-FB} \end{cases} \tag{B.2}$$

where $V_{carm-HB}$ and $V_{carm-FB}$ are the total blocking voltages of the HB-SM and FB-SM capacitors in each arm, respectively, which are given by $V_{carm-HB} = \sum_{j=1}^{N_{HB}} V_{HBSM_j} \geq V_{DC} \cdot (1-R)$ and $V_{carm-FB} = \sum_{k=1}^{N_{FB}} V_{FBSM_j} \geq V_{DC} \cdot R$.

In the average model, the inter-sub-module dynamics of the converter are neglected and the SM capacitor voltages in eah arm are considered to be balanced and oscillating together. Therefore, assuming C_{HBSM} as the cell capacitance of the HB-SMs, the upper and lower arm equivalent capacitances are $C_{HB-U} = C_{HBSM}/N_{HB-U}$ and $C_{HB-L} = C_{HBSM}/N_{HB-L}$, respectively, where N_{HB-U} and N_{HB-L} is the number of HB-SM capacitors that are inserted in the power path from the upper and lower converter arm. Similarly for the FB-SMs, assuming C_{FBSM} as the FB-SM capacitance, the upper and lower arm equivalent capacitances are $C_{FB-U} = C_{FBSM}/N_{FB-U}$ and $C_{FB-L} = C_{FBSM}/N_{FB-L}$, respectively, where N_{FB-U} and N_{FB-L} is the number of FB-SM capacitors that are inserted in the power path from the upper and lower converter arm. Assuming m as the AC modulation index, N_{HB-U}, N_{HB-L} and N_{FB-U}, N_{FB-L} are approximated by:

$$\begin{cases} N_{HB-U} \approx \frac{1}{2} N_{HB}[1 - msin(\omega t + \delta)] \approx N_{HB} \cdot m_{U-HB} \\ N_{HB-L} \approx \frac{1}{2} N_{HB}[1 + msin(\omega t + \delta)] \approx N_{HB} \cdot m_{L-HB} \end{cases} \tag{B.3}$$

$$\begin{cases} N_{FB-U} \approx \frac{1}{2} N_{FB}[1 - msin(\omega t + \delta)] \approx N_{FB} \cdot m_{U-FB} \\ N_{FB-L} \approx \frac{1}{2} N_{FB}[1 + msin(\omega t + \delta)] \approx N_{FB} \cdot m_{L-FB} \end{cases} \tag{B.4}$$

Based on (B.3), the dynamics of the upper and lower arm HB-SM capacitors are given by:

$$\begin{aligned} &\frac{C_{HBSM}}{N_{HB-U}} \cdot \frac{d}{dt} V_{carmU-HB} \approx i_{armU-HB} \\ &\frac{C_{HBSM}}{N_{HB}} \cdot \frac{d}{dt} V_{carmU-HB} \approx \frac{1}{2}[1 - msin(\omega t + \delta)] \cdot i_{armU-HB} \\ &C_{arm-HB} \cdot \frac{d}{dt} V_{carmU-HB} \approx m_{U-HB} \cdot i_{armU-HB} \end{aligned} \tag{B.5}$$

$$\begin{aligned}
&\frac{C_{HBSM}}{N_{HB-L}} \cdot \frac{d}{dt} V_{carmL-HB} \approx i_{armL-HB} \\
&\frac{C_{HBSM}}{N_{HB}} \cdot \frac{d}{dt} V_{carmL-HB} \approx \frac{1}{2}[1 + msin(\omega t + \delta)] \cdot i_{armL-HB} \\
&C_{arm-HB} \cdot \frac{d}{dt} V_{carmL-HB} \approx m_{L-HB} \cdot i_{armL-HB}
\end{aligned} \tag{B.6}$$

where C_{arm-HB} is the equivalent capacitance of all HB-SMs in each converter arm. From (B.5) and (B.6), the upper and lower equivalent arm capacitor currents of the HB chain-links are approximated by:

$$\begin{cases}
i_{capU-HB} \approx C_{arm-HB} \cdot \frac{d}{dt} V_{carmU-HB} \approx m_{U-HB} \cdot i_{armU-HB} \\
i_{capL-HB} \approx C_{arm-HB} \cdot \frac{d}{dt} V_{carmL-HB} \approx m_{L-HB} \cdot i_{armL-HB}
\end{cases} \tag{B.7}$$

Similarly based on (B.4), the dynamics of the upper and lower arm FB-SM capacitors are given by:

$$\begin{aligned}
&\frac{C_{FBSM}}{N_{FB-U}} \cdot \frac{d}{dt} V_{carmU-FB} \approx i_{armU-FB} \\
&\frac{C_{FBSM}}{N_{FB}} \cdot \frac{d}{dt} V_{carmU-FB} \approx \frac{1}{2}[1 - msin(\omega t + \delta)] \cdot i_{armU-FB} \\
&C_{arm-FB} \cdot \frac{d}{dt} V_{carmU-FB} \approx m_{U-FB} \cdot i_{armU-FB}
\end{aligned} \tag{B.8}$$

$$\begin{aligned}
&\frac{C_{FBSM}}{N_{FB-L}} \cdot \frac{d}{dt} V_{carmL-FB} \approx i_{armL-FB} \\
&\frac{C_{FBSM}}{N_{FB}} \cdot \frac{d}{dt} V_{carmL-FB} \approx \frac{1}{2}[1 + msin(\omega t + \delta)] \cdot i_{armL-FB} \\
&C_{arm-FB} \cdot \frac{d}{dt} V_{carmL-FB} \approx m_{L-FB} \cdot i_{armL-FB}
\end{aligned} \tag{B.9}$$

where C_{arm-FB} is the equivalent capacitance of all FB-SMs in each converter arm. From (B.8) and (B.9), the upper and lower equivalent arm capacitor currents of the FB chain-links are approximated by:

$$\begin{cases}
i_{capU-FB} \approx C_{arm-FB} \cdot \frac{d}{dt} V_{carmU-FB} \approx m_{U-FB} \cdot i_{armU-FB} \\
i_{capL-FB} \approx C_{arm-FB} \cdot \frac{d}{dt} V_{carmL-FB} \approx m_{L-FB} \cdot i_{armL-FB}
\end{cases} \tag{B.10}$$

Equations (B.1) to (B.10) describe the operation of the converter under steady-state conditions, while the same principles also apply during PTG faults, when the FMS of

Chapter 6 is employed. For pole-to-pole faults, the blocking state of the HB chain-links is realised as described in Subsection 2.2.5 of Chapter 2. The blocking state of the FB chain-links is achieved by gating off all the IGBTs S1, S2, S3 and S4, and by setting the upper and lower arm modulation functions $m_{U-FB} = m_{L-FB} = 1$. Under these conditions, the fault current path through the CH-MMC during the current limiting mode can be seen in Figure 6.4. Based on these modifications, the HB chain-links block and the FB chain-links present increasing opposing counter-voltages (the magnitude of which depends on ratio R) by charging arm capacitors C_{arm-FB}, thus emulating the behaviour of the CH-MMC during pole-to-pole faults.