UNIVERSITY OF STRATHCLYDE
Department of Physics

Transfer printing of nitride based light emitting diodes

by

António José Marques Trindade

A thesis presented in fulfilment of the
requirements for the degree of
Doctor of Philosophy

May 2015

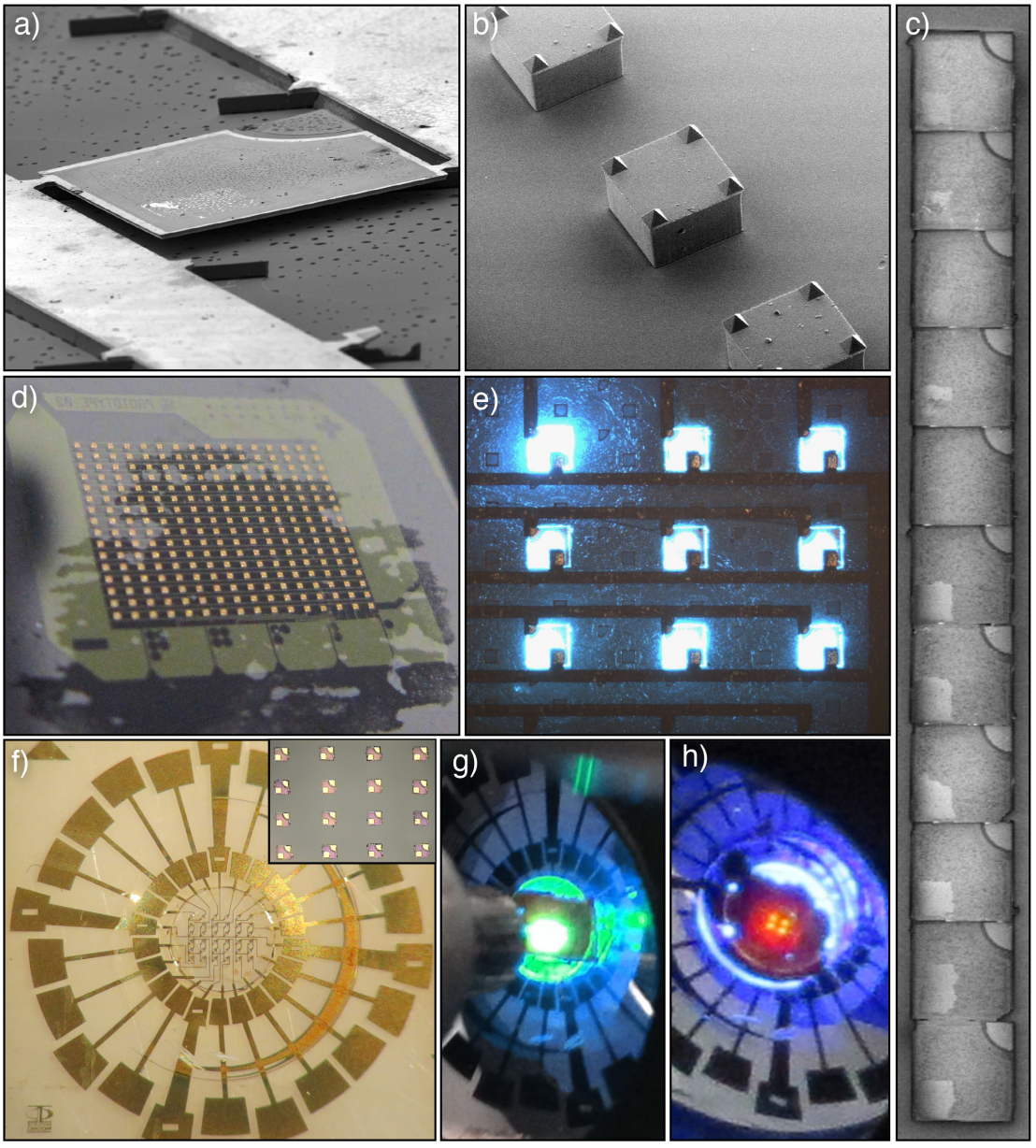
Declaration of Authorship

This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

Signed: _____

Date: _____

Frontispiece



a) a micron-size membrane LED suspended in air by two anchors, b) the elastomeric stamps that pick and transport the suspended LEDs, c) the positioning of close-spaced LEDs with nanometre precision, d) a 256 device array in a flexible plastic substrate and e) a close-up of some of the emitting pixels. In f), LEDs deposited on diamond (inset shows part of the array) as a heat efficient substrate and in g) and h) some of the applications (colour-conversion) where transfer-printed LEDs can be put to use.

Abstract

The research presented in this thesis focuses on the implementation and development of transfer printing as a novel technique for heterogeneous integration of III-nitride based light emitting diodes (LEDs) onto a wide range of substrates, whether flexible or rigid in their nature.

The initial steps towards a functioning prototype are described with the successful transfer printing of 2 μm-thick micron-size LEDs. The thin structures were assembled onto mechanically-flexible substrates in a representative 16x16 array format using a modified dip-pen nano-patterning system. Two different methods of addressing the LEDs were studied by using conductive inks on the LED bonding pads or through the use of metal tracks. Both addressing schemes are compared and studied for reliability. Individual study of the printed array elements showed blue emission centred at 486 nm with a forward-directed optical output power up to 80 μW (355 mW/cm^2) when operated at a current density of 20 A/cm^2. A relatively poor performance was observed with damage to the current spreading metal due to an alkaline wet etch step, needed during processing to yield suspended membranes. This issue was addressed by reversing the order of the major steps needed to fabricate the LEDs, which resulted in significantly improved LED performance. The capabilities of the nano-patterning system were demonstrated with successful LED placement as low as 150 nm ($\pm$14 nm) between dies. Further optimisation beyond the initial prototypes made use of heat-efficient substrates, namely fused silica and diamond, without the use of intermediary adhesion layers. Through the use of a liquid capillary bond, consistent van der Waals bonding was achieved, despite the curvature of the epitaxial layers that comprise an LED following their release from their native silicon growth substrates. The excellence of diamond as a heat-spreader allowed the printed membrane LEDs to achieve optical power output density of 10 W/cm^2 when operated at a current density of 254 A/cm^2 - a significantly higher operational regime compared to the initial prototypes. To capitalise on the new achieved performance, demonstrations of data transmission and colour conversion are shown.

Acknowledgements

I'd like to start by thanking my supervisor, Prof. Martin Dawson for the opportunity to do my PhD in the Institute of Photonics. His enthusiasm and encouragement towards my research were greatly appreciated. Thank you for everything Martin.

I would like to thank in particular to Dr. Ian Watson for his outstanding aid throughout the course of my studies. His guidance, discussions, patience, exchange of knowledge and significant contributions were highly valued and appreciated. Thank you Ian.

To Dr. David Massoubre, Dr. Enyuan Xie and Eng. Jim Small for taking the time and attention during the long cleanroom working hours to challenge me and to train me. The three of you were the pillars of my cleanroom training. Your knowledge and friendship is highly valued. Thank you so much to all of you.

To Dr. Paul Edwards for always having time to acquire SEM images during what often was very short notice. The results were great and truly helped visualising the capabilities of transfer-printing. Thank you Paul.

To Dr. Nicolas Laurand and Dr. Benoit Guilhabert for significant discussions during my studies. Thank you both.

To Eng. Ricardo Ferreira for his help and insight into the world of thermal imaging which greatly provided valuable information regarding the behaviour of LEDs and substrates. Obrigado Ricardo.

To my PhD colleagues at the Institute. Especially Caroline Foucher and Brynmor Jones. You guys were both great friends and a pleasure to work with. I truly thank you for all the nonsense (all of it!) and friendship over these last few years. Merci Ca. Diolch i ti Bryn.

I also thank my family for their support and endured sacrifices, which without, wouldn't have enabled me to have come this far. Obrigado Mãe. Obrigado Pai.

To Ana. Sabes, não sabes?

Contents

List of Figures

List of Tables

Abbreviations

AFM	Atomic force microscope
Al	Aluminium
Ar	Argon
As	Arsenide
Au	Gold
BW	Bandwidth
Cl_2	Chlorine
EBL	Electron blocking layer
E_g	Bandgap energy
EL	Electroluminescense
EQE	External quantum efficiency
E_{Vbi}	P-N junction Electric Field
E-O	Electrical-to-optical
e-h	Electron - hole pair
FWHM	Full width at half maximum
Ga	Gallium
Ge	Germanium
H	Hydrogen
HF	Hydrofluoric acid
HT	High-temperature
ICP	Inductively-coupled plasma
In	Indium
IR	Infra-red radiation
IQE	Internal quantum efficiency
ITO	Indium tin oxide
J-V	Current density - voltage
KOH	Potassium hydroxide
LED	Light emitting diodes
L-V	Optical power - voltage
LT	Low-temperature
Mg	Magnesium
MOCVD	Metal organic chemical vapour deposition
MQW	Multiple quantum well
m^*	Carrier effective mass
N	Nitride
Ni	Nickel
OH^-	Hydroxide ions
P	Phosphorous

PDMS	Polydimethylsiloxane
PECVD	Plasma enhanced chemical vapour deposition
PR	Photoresist
QCSE	Quantum confinement Stark effect
RF	Radio frequency
RIE	Reactive ion etch
SEM	Scanning electron microscope
Si	Silicon
SiC	Silicon carbide
SiN$_x$	Silicon nitride
SSL	Solid state lighting
SU8	High-aspect ratio negative photoresist
TD	Threading dislocations
Ti	Titanium
TP	Transfer printing
UV	Ultra-violet
$\boldsymbol{V_D}$	Diffusion voltage
$\boldsymbol{V_{th}}$	Threshold voltage
$\boldsymbol{W_{DH}}$	Thickness of a double-heterojunction

To Mom & Dad and in loving memory of Luz Correia.

Chapter 1

Introduction

This thesis focuses on the integration of ultra-thin micron-sized Light Emitting Diodes (LEDs) onto novel flexible and rigid substrates with an emphasis on fabrication processes and the optimisation of their performance/capabilities. As such, Chapter 1 contains a general introduction to the basic operational properties and characteristics of LEDs, especially for those based on Aluminium, Indium, Gallium, Nitride (AlInGaN) based material alloys. The chapter begins by describing the history behind LED development from the early days to the future prospects for solid-state lighting and its applications. The physics and operating principles behind LEDs are described, and the benefits and issues of growing nitride materials on silicon-based substrates are also included in the following sections.

Chapter 2 will discuss the mechanics of transfer printing (TP), the main technique used here for integration, describing the concepts and framework behind this technique. This includes a basic description of the several cleanroom processes used to achieve the fabrication of the three elements needed for TP: suspended AlInGaN-based LEDs, elastomeric stamps and patterning of alignment features on flexible/rigid substrates. The physics and chemistry behind selective anisotropic etching of silicon are also described, as this is a major process used during fabrication. The chapter concludes with an analysis of the assembly system used and the modifications performed to achieve ultra-parallel assembly and scalable device fabrication. Chapter 3 describes the TP of micro-LED arrays onto mechanically flexible substrates. The overall device architecture is described as well as the first electrical bonding attempts. The optimisation of the addressing method for the LEDs is discussed, including the switch to metal tracks and then the optoelectronic performance is reported. Finally, the chapter concludes with a demonstration of nano-precision LED placement using a modified nanolithography system. Chapter 4 describes the use of TP with liquid capillary bonding as a technique to bond the LED devices onto

rigid receiving substrates. The change in device architecture is described as well as the revised fabrication method. Due to strain relaxation, the LEDs curve when suspended, so a curvature study is performed on the devices. A summary of all the devices fabricated with this method concludes the chapter. In chapter 5, the optimisation of device performance through the use of heat-extracting substrates is described and studied. The optoelectronic performance is compared with less-thermally efficient substrates in the beginning of the chapter and the changes in the electroluminescent (EL) emission are studied. The performance of the devices for visible light communications is also studied including bandwidth measurements and data transfer. An example of direct colour-conversion with added material layers is briefly described and its potential applications discussed. The thesis closes with conclusions for the work described and future work plans that should be pursued.

1.1 Development of Light Emitting Diodes

The first LED was arguably that discovered accidentally by Henry Round in 1907 [1], who reported yellow light being produced as an electric current flowed through a crystal of Silicon Carbide (SiC). In the 1960s, LEDs began to be mass-produced and were based initially on red-emitting Gallium-Arsenide-Phosphide (GaAsP) materials closely followed by the green-emitting Gallium-Phosphide [2, 3]. These devices were used in their early days as indicator lamps and small displays in wrist watches and calculators. As with many newly-developed technologies, their power efficiency was low and required optimisation and improvement in subsequent years.

Such optimisation initially focused on broadening the coverage of the available LED wavelengths, including towards the higher-energy part of the spectrum in the blue and ultra-violet (UV). III-nitride materials proposed for such operation struggled initially to perform at the desired wavelengths due to the difficulties in obtaining good crystal quality and in producing an effective p-type doping of the GaN [4]. Thus, prior to 1990, most commercial blue LEDs were based on Silicon-Carbide (SiC). The best electrical-to-optical power-conversion efficiency attained by these devices was, however, only 0.03% [5]. The key breakthroughs in III-nitride materials began after 1986 with the significant improvement of the crystal quality by using an Aluminium Nitride (AlN) layer on sapphire prior to the deposition of the main GaN layer [6], a process or variant thereof that is nowadays an established standard to grow high-quality III-nitride structures with reduced density of defects. By then, new attempts at producing an efficient p-type GaN were being carried out by techniques of electron beam irradiation and thermal annealing [7, 8]. With these developments, efficient high-performance LEDs [9, 10] and laser diodes [11]

began to appear and paved the way to today's advanced technologies based on III-nitride materials. This opened up a wide range of new applications since the complete coverage of the entire visible spectrum was now possible.

To evaluate LED performance, one needs to evaluate the efficiency of the devices. Two important parameters are used for this: internal quantum efficiency (IQE - η_{int}) and external quantum efficiency (EQE - η_{ext}). The IQE is defined as the ratio of the number of photons emitted by the LED active region to the number of injected charge carriers. The ideal LED would in theory emit one photon *per* injected electron (and hole) although this is an idealisation and not possible to achieve. The injected carriers can either recombine radiatively (contributing to the efficiency) or through non-radiative heat-generating pathways (reducing the efficiency). The internal quantum efficiency can then be defined as:

$$\eta_{int} = \frac{P_{int}/h\nu}{I/e} \tag{1.1}$$

where P_{int} is the optical power emitted from the active region, and I is the injection current. Here $h\nu$ is the photon energy (with h being Planck's constant) and e is the elementary charge. In an ideal LED, all the photons emitted by the active region should escape the LED active area (where its light extraction efficiency would be 100%), though likewise, this is impossible to achieve. Not all the photons are able to escape the active area and be emitted into free space due to several loss mechanisms. The light extraction efficiency can therefore be represented as an extraction efficiency $\eta_{extraction}$:

$$\eta_{extraction} = \frac{P/h\nu}{P_{int}/h\nu} \tag{1.2}$$

Here, P is the optical power emitted into free space. The extraction efficiency poses a severe limitation for high-performance LEDs as it is quite difficult to achieve efficiencies higher than 50% without requiring cost-prohibitive fabrication processes [12]. The EQE refers to the ratio of photons emitted by the LED into free space compared to the number of injected charge carriers:

$$\eta_{ext} = \frac{P/h\nu}{I/e} = \eta_{int} \cdot \eta_{extraction} \tag{1.3}$$

With today's high-performance LEDs emitting throughout the visible spectrum, it is also worth mentioning the existence of both UV and Infra-Red (IR) LEDs. This extended coverage opens a wide range of applications where LEDs can be introduced, including the possibility of efficient white-light generation to compete with conventional incandescent or fluorescent light sources. This capability has initiated a whole new area of scientific research and a corresponding industry and is commonly referred to as 'solid-state lighting' (SSL). Figure 1.1 shows the EQE in the visible range of the

electromagnetic spectrum along with the human retina response (solid line, top graph). One can see that there is a disparity between the human eye's optimum sensitivity and the available colour emissions from the LEDs. The low EQE of the LEDs in the wavelength region where we have the highest sensitivity is commonly known as the *'green-yellow'* gap. While there are different methods to achieve white light, the use

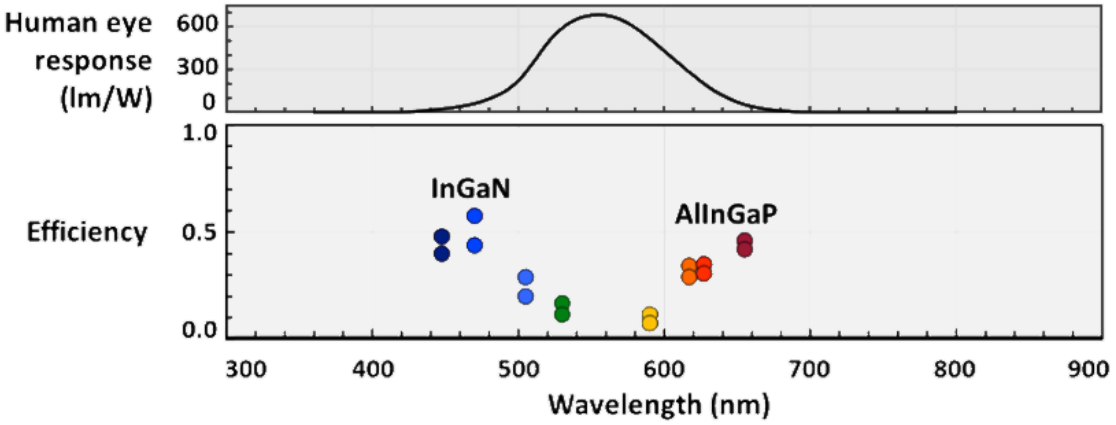


FIGURE 1.1: EQE (%) for high-performance LEDs based on III-nitride and phosphide materials vs. the human eye response through the spectrum. From [13].

of low-cost and energy-efficient light sources based on LEDs has become attractive for everyday applications and more recently as a lighting solution. It is anticipated that increases of efficiency of these devices can go as high as 63% and 90% more than that of fluorescent and incandescent lamps, respectively [14]. The efficiencies of various white light sources compared with LED-powered solid-state-lighting can be seen in Figure 1.2. The luminous efficacy here represented is the conversion efficiency from optical power to luminous flux, typically measured in the unit of lm/W. The lumen (lm) is the unit

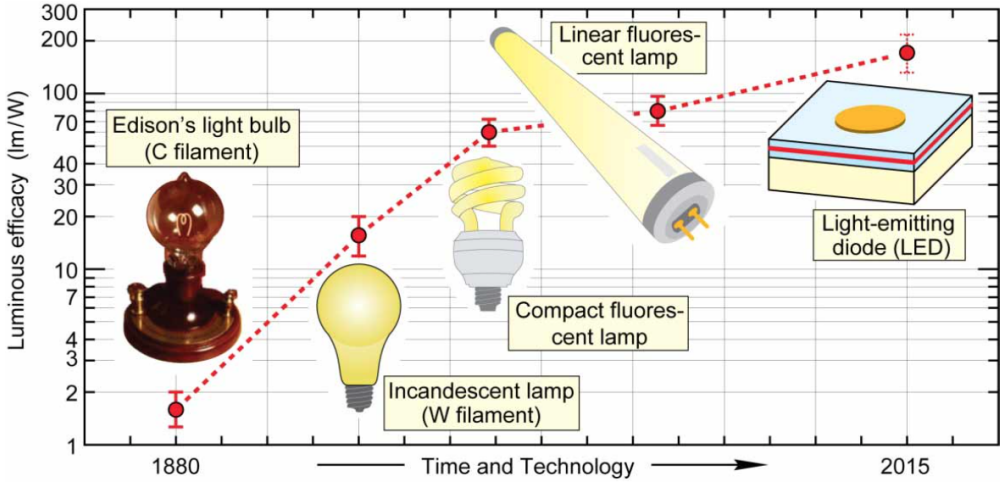


FIGURE 1.2: Comparison of the luminous efficacy of conventional lighting technologies to LED technology. Adapted from [14].

of luminous flux (or luminous power) perceived by the human retina. The low-energy

consumption, mechanical robustness, long lifetime and colour tunability represent the most appealing characteristics of these devices. Such advantages will play a crucial role in our pursuit of energy-efficiency and environmental sustainability, as incandescent and fluorescent lightbulbs are continuously being phased-out of production. Figure 1.3 shows some of the applications that LED technology is quickly becoming a part of. The high-energy efficiency and warm-white colour production are the main characteristics for use in indoor environments (a typical replacement lightbulb made of LEDs can be seen in Figure 1.3(a)). Other newly developed applications where LEDs are being implemented

FIGURE 1.3: Examples of the use of LEDs in everyday-life: (a) a typical lightbulb for indoor use, (b) contact-lenses with a miniature LED embedded display, (c) outdoor illumination, d) an example of the adoption of LEDs by the automobile industry.

include use in biotechnology sensors and diagnostic tools [15] (Figure 1.3(b)). Current high-power LEDs are already robust enough to illuminate outdoor environments much more efficiently than old incandescent and tube-discharge lamps (Figure 1.3(c)). One of the biggest adopters of LED illumination has been the automobile industry (Figure 1.3(d)). With applications both internal and external, entire vehicles lighted by LED technology are being produced by several manufacturers.

Figure 1.4 shows a typical high-power (>100 mW output power) commercial LED packaging solution for an individual LED. These are usually single-chip devices with

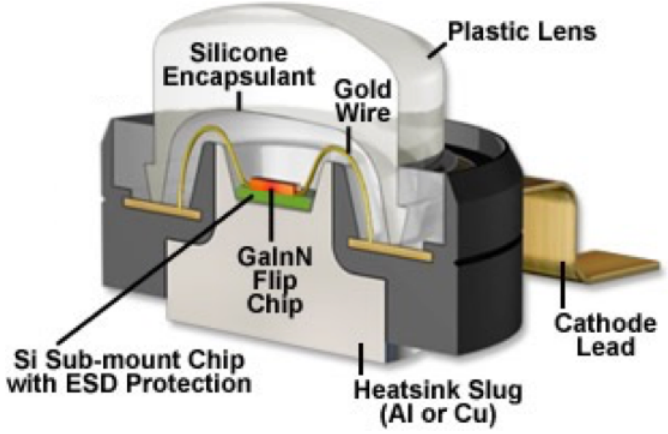


FIGURE 1.4: Generic schematic packaging of a high-power LED encapsulated by a moulded dome-shaped epoxy.

an active area ~300 x 300 μm^2, to 1 mm^2. The dies are bonded to a metal frame with

gold wires for electrical addressing. They are typically covered by a dome-shaped epoxy to aid in protecting the device and to help direct the light produced, improving the light extraction efficiency. Low-power LEDs (nW - 10's nW) do not have an integrated heatsink (in contrast to Figure 1.4) and are just encapsulated with the epoxy.

1.2 Operating principles

Materials can be classified into three types according to their capability in conducting electricity: conductors, semiconductors and insulators. The huge importance semiconducting materials have in today's electronics comes in large part from their extreme sensitivities to small concentrations of impurities. The materials composing light-emitting diodes exploit these sensitivities to bring a wide range of characteristics to optoelectronic devices. Each material can be described through an energy diagram where two distinct energy bands exist: the valence and conduction energy bands. Electrons occupying full valence bands are bound to atoms and do not contribute to the flow of charge when an external electric field is applied. On the other hand, electrons populating the conduction band are free to move throughout the material and may contribute to the net flow of charge. The difference of energy between these two energy levels is known as the *bandgap* and represents a range of forbidden energies that electrons cannot occupy. In conducting materials, these two energy bands partially overlap so it is relatively easy for some of the electrons to move through the material. For insulating materials, the gap is large and electron transitions between bands do not normally occur, although at high enough voltage levels and under certain conditions, any material is able to conduct electricity.

For semiconducting materials, the separation between these two energy bands is small ($\sim$1 eV) which means electrons can relatively easily be excited from the valence band to the conduction band. The engineering of these bands was a crucial step to attain a wide variety of useful semiconductors by changing the doping materials and concentrations.

Intrinsic semiconductors are pure materials without any added impurities. In such materials, an excited electron jumping the energy gap to the conduction band leaves a vacancy (or *hole*) behind. This vacancy can be readily filled by another nearby electron, which in its turn leaves another vacancy behind, and so on. One can imagine this process as a positive charge moving through the semiconductor. This mean that for every free negatively-charged carrier that populates the conduction band, a free positive charge is made available, thus one can conclude that intrinsic semiconductors are by their nature neutrally charged. With the inclusion of other kinds of atoms (hereafter named 'dopants'), semiconductors can however be intentionally doped to achieve a positive or negative-type semiconductor with typical dopant concentrations from 10^{15} to 10^{18} *per*

cm^3 [16, 17]. By way of example, Figure 1.5 considers the doping of Germanium (Ge). Ge has four valence electrons which in a crystal lattice means the four electrons are shared with four neighbouring atoms. If no dopants are introduced, the semiconductor has no electrons in its conduction band. Doping Ge with As atoms as 'donors' introduces a new impurity that carries an extra electron (Figure 1.5(a)). This extra electron is free to move around and thus a negatively-charged semiconductor (n-type) is created. Likewise, the insertion of dopants with fewer valence electrons (for example, Ga, which

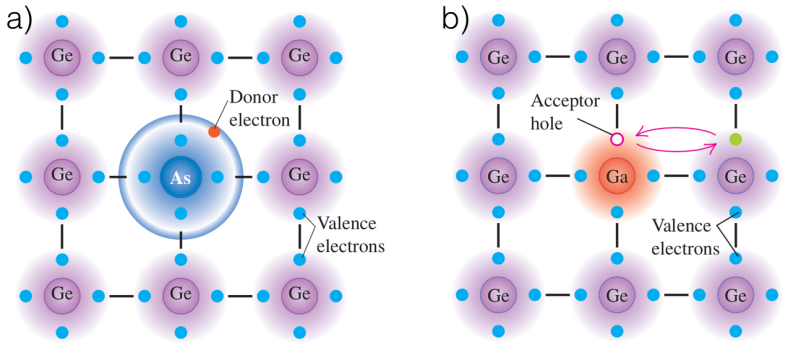


FIGURE 1.5: Schematic of a donor (n-type) semiconductor (a) where the central atom has an extra electron that does not participate in the covalent bonding. In (b) the analogous situation where the doped atom has only three valence electrons. The electron exchange through neighbouring atoms means the hole is free to move around the crystal lattice. From [17].

has only three), the material shares only three electrons with four neighbouring Ge atoms. This means that holes are made available in the lattice that will contribute to the conduction process, resulting in a positively-charged (p-type) semiconductor. Saying a semiconducting material is p-type or n-type does not mean the material has a positive or negative net charge. This labelling indicates only the majority of carriers available for conduction in the semiconductor.

For the n-type semiconductor illustrated in Figure 1.5(a), the energy level of the surplus electrons lies within the material bandgap immediately below the conduction band (Figure 1.6(a)) and is called a donor level. At room temperature, kT is about 0.025 eV which is substantially greater than the typical 0.01 eV 'depth' of the donor level. Thus at room temperature, such electrons in the semiconductor can have enough energy to be promoted to the conduction band and disperse through the material. Adding atoms (or dopants) with fewer valence electrons (such as the example in Figure 1.5(b)) has the opposite effect, where the Ga atom would prefer to establish four covalent bonds with neighbouring atoms but has only three in its valence bands. Thus, it can capture an electron from a neighbouring Ge atom to complete the bond. This means the Ge atom will be left with a hole (or missing electron) which can move throughout the crystal. The new electron that now fills the Ga atom is in a level called the acceptor level immediately above the valence band (Figure 1.6(b)). This level is generated by the Ga atom itself

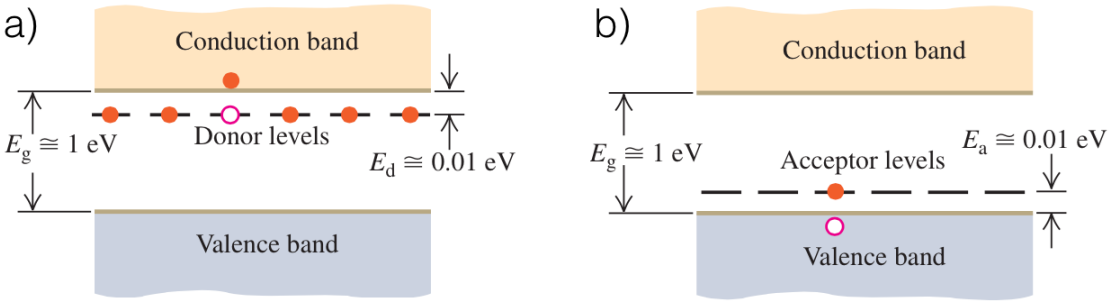


FIGURE 1.6: Energy-band diagram for an n-type semiconductor (a). As illustrated, one donor electron has been excited from the donor levels into the conduction band. In an analogous way, (b) represents the band diagram for a p-type semiconductor with an electron on the acceptor level, which leaves a hole behind. From [17].

which becomes an acceptor-atom aiming to satisfy its need to completely establish four covalent bonds. These two types of materials enable the structure that comprises a typical LED architecture at its most basic: a p-n junction.

1.2.0.1 Radiative processes

In LEDs, electrons in the higher-energy conduction band recombine with holes in the lower-energy valence band. The energy associated with this transition approximately equals the energy difference between the conduction band minimum and the valence band maximum:

$$E_{gap} = E_C - E_V \tag{1.4}$$

This energy can be released either as heat (phonons: vibrations of the crystal lattice) or preferably through photons, a process known as luminescence which is the underlying conversion of injected carriers into light emission. Thus, because the energy gap determines the emission energy, materials can be engineered with different gap energies. Semiconductor alloys comprised of several elements (AlGaP, AlGaN, GaAs,...) can therefore produce different wavelengths simply by altering the relative amount of these elements or through active-layer engineering using quantum wells as will be described in section 1.2.1.1. The bandgap energy and the wavelength (λ) of an emitted photon can be described by:

$$E = E_{gap} = \frac{hc}{\lambda} \tag{1.5}$$

where E is the energy of the emitted photon, E_{gap} the bangdap energy (described in equation 1.4), h is Planck's constant and c is the speed of light.

There are two general categories of semiconductors, namely those having direct and indirect bandgaps. A simplified energy band structure for these two types of semiconductors is illustrated in Figure 1.7. Here the horizontal axis is the crystal momentum - directly

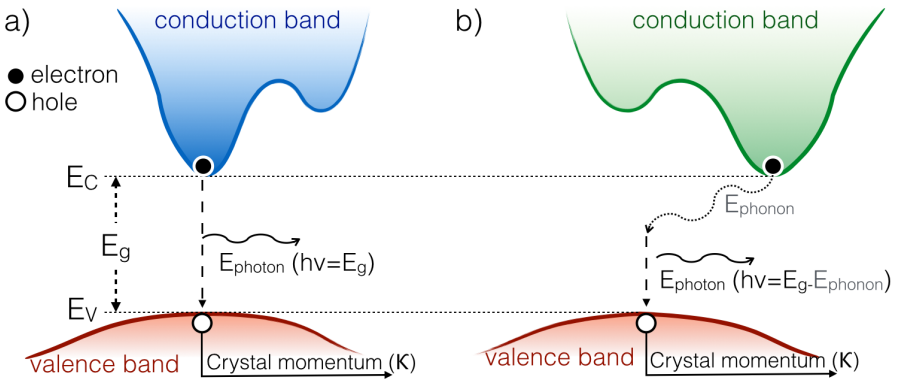


FIGURE 1.7: Band structures for (a) direct and (b) indirect bandgap semiconductors.

proportional to the electron wavenumber k - which represents the allowed momentum for electrons within the crystallographic structure. This is commonly called a *k-space* representation and for direct bandgap semiconductors, the two energy bands are aligned and coincide in k-space (Figure 1.7(a)). This favours electron transitions between energy bands without changes to the crystal momentum. Such transitions for indirect bandgap semiconductors (Figure 1.7(b)) are mismatched in k-space and require the assistance of lattice vibrations (or phonons) to conserve the momentum of the transition. Hence, electron transitions are significantly more efficient in direct bandgap semiconductors as these have higher probability for electron transitions between bands.

1.2.1 Physics of the P-N junction

The simplest LED structure is based on a p-n junction as illustrated in Figure 1.8. The two heavily doped materials are grown sequentially, with atomic layers slowly deposited (by epitaxial growth methods). This type of junction is known as a p-n diode and has a rectifying behaviour when an electric current is passed through. In a p-n junction, excess electrons from the n-type material will diffuse across its physical boundary through to the p-type layer where they will recombine with existing holes. In the same way, holes from the p-type will diffuse to the n-type material and recombine with existing free electrons. This interdifusion of charges generates a physical region at the interface of both materials known as the *depletion region*. With the diffusion of electrons into the p-type region (and vice-versa), the p-type region will acquire a negative net charge (and vice-versa for the n-type region). Thus, with the charge exchange, a potential difference between the two materials is generated at the depletion region known as the diffusion voltage (V_D), which opposes the further diffusion of electrons and holes and will ultimately balance out the diffusion by precisely V_D. Thus, V_D is the voltage that free-carriers must overcome to be able to diffuse to the neutral region of the opposing semiconductor type. This potential governs the p-n junction conductivity and for current to flow through the device, V_D has

to be overcome [12]. V_D is given by:

$$V_D = \frac{kT}{e} ln \frac{N_A.N_D}{(n_i)^2} \tag{1.6}$$

where k is the Boltzmann constant, T is the temperature, e the elementary charge, N_A the acceptor concentration, N_D the donor concentration and n_i is the intrinsic carrier density of the semiconductor. A typical p-n junction is illustrated in Figure 1.8 for a zero bias (a) and the generated depletion region is identified in yellow. The Shockley equation is used to model the behaviour of a p-n junction and describes the current-voltage characteristics (I-V) of an ideal diode:

$$I = I_s(e^{\frac{eV}{kT}} - 1) \tag{1.7}$$

with I_s being the saturation current which is given by:

$$I_s = eA \left(\sqrt{\frac{D_p}{\tau_p}} \frac{(n_i)^2}{N_D} + \sqrt{\frac{D_n}{\tau_n}} \frac{(n_i)^2}{N_A} \right) \tag{1.8}$$

where D_n,D_p are the electron and hole diffusion constants and τ_n,τ_p the minority-carrier lifetimes respectively. V is the external voltage applied to the diode. Applying a forwarding bias to the junction (Figure 1.8(b)) - i.e. positive and negative terminals on the device's p and n materials respectively - causes a net flow of electrons and holes from each region towards the junction, reducing the overall length of the depletion region which in its turn reduces the diffusion voltage at the region.

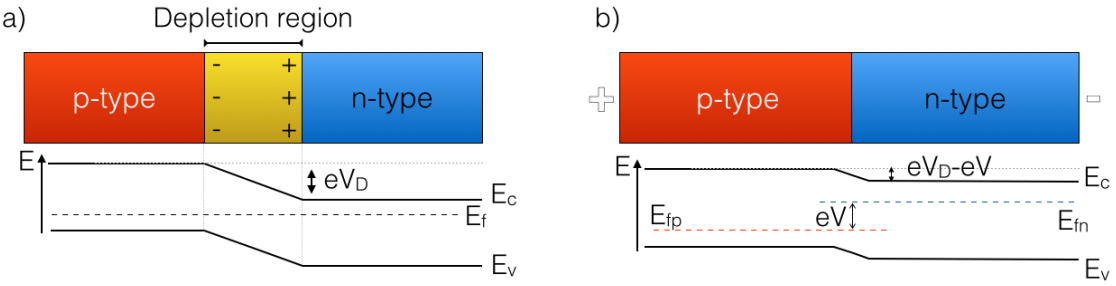


FIGURE 1.8: (a) p-n diode under zero external bias and with a depletion region at the interface. In (b), a diode under forward external bias quenches the depletion region and leaves the device in a reduced diffusion voltage state. Underneath both (a) and (b) is the respective energy diagram corresponding to each situation.

Under a forward bias condition ($V \gg kT/e$) screening of the depletion region takes place and the Shockley equation can be re-written as:

$$I_s = eA \left(\sqrt{\frac{D_p}{\tau_p}} N_A + \sqrt{\frac{D_n}{\tau_n}} N_D \right) \left(e^{\frac{eV - V_D}{kT}} \right) \tag{1.9}$$

In equation 1.9, an increase in the applied forward voltage V to match the V_D will cause a rapid increase in current flow. The voltage at the point of this significant current increase is called the threshold voltage (V_{th}), and is the point where p-n diodes change their electrical properties. The diode is considered to be at cut-off for voltages below V_{th} and to be active - or in operation - for voltages above V_{th}. For an ideal diode, this threshold voltage should be approximately the bandagap of the semiconductor material (E_g) divided by the electron charge (e):

$$V_{th} \simeq \frac{E_g}{e} \tag{1.10}$$

The overcoming of V_{th} by the external voltage initiates the injection of minority carriers through the opposing charged materials - i.e. electrons will diffuse to the p-type material and vice-versa. This carrier injection can recombine with existing opposite charge carriers in the opposing material which results in photons being emitted from an LED device. Since in practice an ideal LED can never be achieved, LEDs cannot be perfectly modelled through the Shockley equation without accounting for parasitic resistances. Such resistances have their origins in many factors such as material defects, interfacial defects between materials, electrical contact resistance from the metals on the LEDs electrodes, etc. Thus, using Ohm's law, V_{th} can be replaced by a current dependent series resistance R_S:

$$I = I_s \left(e^{\frac{e(V-IR_s)}{kT}} - 1 \right) \tag{1.11}$$

A reverse bias on the p-n diode terminals has the analogous effect on the V_D which increases significantly. At the semiconductor level, this can be seen as an expansion of the depletion region through both p and n materials which will be significant enough to impede the flow of current through the device [12].

1.2.1.1 Quantum wells and heterostructures

The main disadvantage of the simple p-n structure is owing to carrier diffusion. Carriers injected into semiconductors of the opposite conductivity type will eventually recombine. Both types of carriers have an associated diffusion length before recombining with their counterparts. The rate at which carriers recombine is given by the bimolecular recombination equation [12]:

$$R = Bnp \tag{1.12}$$

with B being the bimolecular recombination coefficient for the semiconductor and n and p, respectively, the electron and hole concentrations. This means that keeping a high concentration of carriers in very close proximity - i.e. near an LED active region - will increase radiative recombination and decrease the recombination lifetime. This is

a common characteristic for all high-efficiency LEDs as they are typically engineered around a heterostructure or a quantum-well design (Figure 1.9). In these types of LED

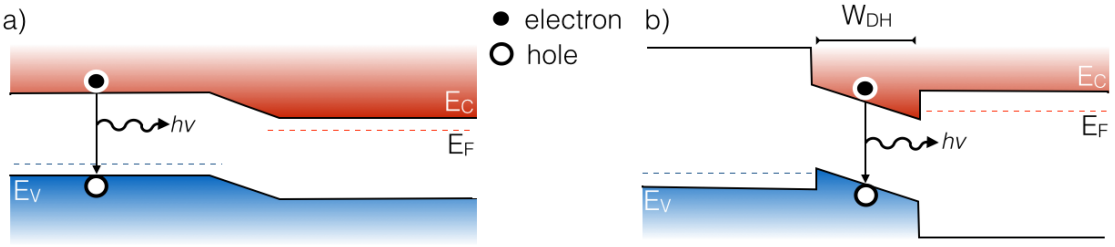


FIGURE 1.9: (a) p-n homojunction under forward bias and (b) p-i-n heterojunction under forward bias. The horizontal axis is a spatial dimension (Z) in the crystal growth direction

structures, intermediate layers are grown between the main heavily-doped p and n-type semiconductors. These layers are commonly composed of materials that have a lower bandgap energy. Thus, when compared to the higher p and n gap energies, these will act as potential wells (Figure 1.9) which charge carriers will flow to as these are more energy favourable for recombination. The large concentration of carriers in these wells (and according to equation 1.12) is therefore crucial for efficient radiative recombination and this process typically occurs within the thickness (W_{DH}) of this active region.

The thickness of this region can be significantly smaller than the diffusion length of the charge carriers. When W_{DH} becomes small enough to be comparable to the de Broglie wavelength for the motion of carriers, one must consider quantum-size effects. The de Broglie wavelength is given by:

$$\lambda = \frac{h}{p} = \frac{h}{\sqrt{2m^* kT}} \tag{1.13}$$

where m^* is the carrier effective mass and p its momentum and is typically a few nm for electrons in semiconductors. Inside the quantum well, carriers are confined in one crystal direction. In this direction, the allowed energy levels stop forming a continuous energy band and discrete and distinct energy levels are created. The quantised energy values of carriers can be then associated with a thin one-dimension potential well limited by two carrier-limiting potential barriers.

Since - in the case of an infinite potential barrier - the now confined particles cannot (in theory) leave the potential well, the permitted energy levels that carriers can occupy within the well are given by:

$$E_n = \frac{n^2 h^2}{8m^* {L_{QW}}^2} \tag{1.14}$$

where L_{QW} is the width of the potential well and n=*1,2,...* are the energy levels that can be filled by carriers. A useful deduction from equation 1.14 is that as the potential

well length is reduced (L_{QW}), the allowed energy levels become more separated which in consequence means any transitions occurring at the higher levels will generate higher-energy photons (Figure 1.10). The quantum well thickness in an LED active region

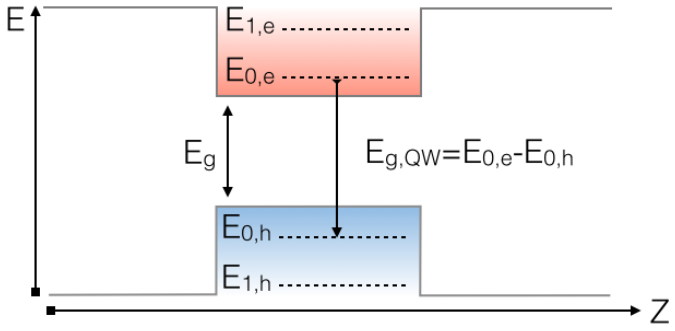


FIGURE 1.10: Schematic of a quantum well structure representing an optical transition from the lowest quantum well energy level transition. It is visible how this is slightly higher than the energy of the bandgap. Z represents distance in the growth direction.

can therefore be used to tune the desired emission wavelengths. Quantum wells can then be used to generate photons of shorter wavelengths for an LED since the energy of carriers in the well cannot equal zero (zero point energy). To help the confinement efficiency and boost radiative recombination, more than one well can be used and today's best-performing LEDs have multiple quantum-well (MQW) regions sequentially deposited on one another.

1.2.2 AlInGaN-based LEDs

1.2.2.1 III-nitride materials

The LEDs described in this thesis were produced through collaboration with the Humphreys' research group at Cambridge University (UK), which supplied the wafers used to produce the devices reported in Chapter 3 and Plessey Semiconductors Ltd., which supplied the wafers for the prototypes reported in the subsequent chapters 4 and 5. Both sources supplied epitaxially grown AlInGaN structures on specially orientated Silicon (111) wafers that were processed into blue-emitting III-nitride based light emitting diodes.

III-nitride materials have three basic binary alloys: AlN, GaN and InN, respectively. These types of alloys form stable crystalline structures in a typical hexagonal wurtzite form. The major attractiveness in this alloy-system (in contrast with the conventional cubic III-V compound semiconductors) is that the bandgap remains direct throughout the full composition range from AlN to InN. Thus, full control over the bandgap from the deep-UV to the infrared region is possible with changes of composition (Figure 1.11), a

much-desired property for functional optoelectronic devices with applications that require direct bandgap emissions (i.e. high efficiency lasers/LEDs) [18]. Table 1.1 summarises the electrical and structural properties for these binary material alloys.

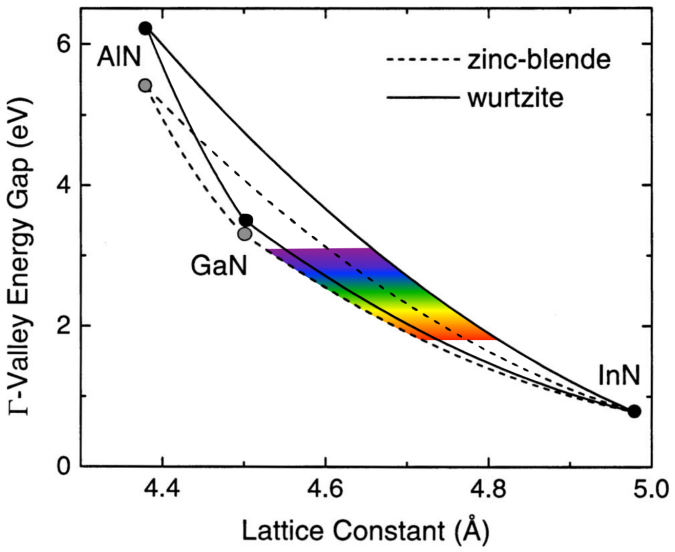


FIGURE 1.11: The energy gaps of wurtzite (solid curves) and zinc-blende (dashed) nitride semiconductor alloys and binaries (points), as a function of lattice constant for the zinc-blende form. Adapted from [19].

TABLE 1.1: Important characteristics of the AlInGaN alloy system [12, 19].

Characteristic	**Symbol**	**AlN**	**GaN**	**InN**
Lattice constant (Å)	a_o	3.112	3.191	3.545
	c_o	4.982	5.185	5.703
Bandgap energy (eV)	E_g	6.28	3.425	0.77
Electron mobility (μn)	cm^2/Vs	1500	3200	3200
Hole mobility (μp)	cm^2/Vs	14	30	-

III-nitride alloy materials are isomorphous, which means that they typically retain the same crystalline structure (hexagonal wurtzite) when combined in different alloys. The bandgap of these ternary and quaternary alloys can be engineered with changes to the relative amount of the materials making up the alloys themselves. The bandgap energy that a certain alloy can create is represented in Figure 1.11 and shows the wide range of wavelengths that III-nitride materials can cover all the way from the deep-UV to the near-IR. An attractive characteristic of the $In_xGa_{1-x}N$ alloy as represented in Figure 1.11 is that this allows a direct bangdap semiconducting material throughout the entire visible spectrum. Today's LED technology relies on this alloy material to achieve high-performance blue and green emissions.

The majority of III-nitride LED wafers are grown epitaxially by Metal Organic Chemical Vapour Deposition (MOCVD). This technique grows the crystal by using chemical reactions rather than the use of a targeted molecular beam. During growth in an

MOCVD reactor, the substrate becomes exposed to one (or several) metal-organic precursors that react and/or decompose at the substrate surface to deposit the materials. The deposition of III-nitride materials requires extremely high growth temperatures (∼1000° C) due to their significant covalent bond energy compared with other III-V materials. This limits the choice of available substrates as these have to withstand such temperatures while being both chemically and mechanically stable [20]. Most commercial GaN-based LEDs nowadays are grown on sapphire substrates although these possess a significant lattice spacing difference (16%) to the c-plane of GaN - with a 30° rotation with respect to the c-axis of sapphire to ensure the alignment of the crystalline unit cells (Figure 1.12(b)). Growing crystalline materials with such a lattice mismatch results in a high density of threading dislocations (TDs). These are known to be related to non-radiative centres which strongly reduce the light output [21]. While III-nitride

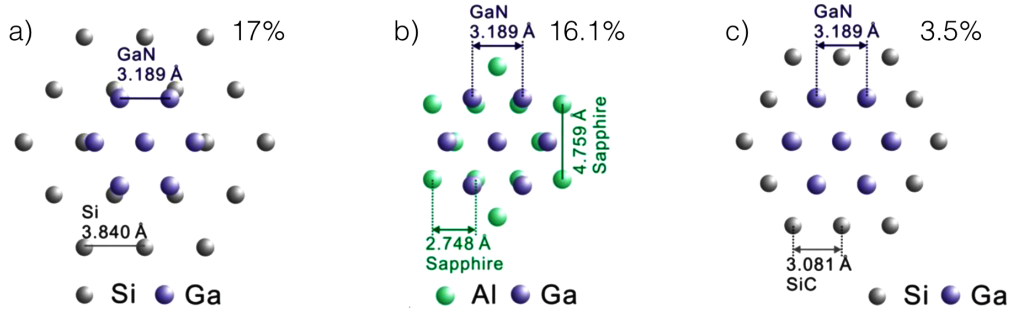


FIGURE 1.12: Epitaxial relationship and lattice mismatch between c-plane GaN and (a) Si(111), (b) sapphire (c-plane) and (c) 6H-SiC. From [22].

materials are more tolerant to TD defects than conventional III-V materials - most likely due to carrier (de)localisation effects by In-rich clusters [23, 24] - the improvement and development of new growth techniques to aid the reduction of TD defects in GaN grown on sapphire has seen considerable improvements especially with the inclusion of low-temperature nucleation layers and through material island coalescence [25, 26].

Currently, nearly all commercial AlInGaN-based LEDs are grown along the [0001] direction (c-plane) of the crystal. The high electronegativity of the nitrogen atom creates strong dipoles in the metal-nitrogen bonds which is the origin of the strong internal polarisation of III-nitride materials. Figure 1.13 shows the orientations of polar, semipolar and nonpolar planes of a crystal unit of GaN. By convention, the [0001] direction points from a metal atom to its nearest nitrogen neighbour in the direction of the highest symmetry, which is also the optical axis of the crystal - i.e. the c-axis is normal to the (0001) polar plane (Figure 1.13). The [0001] direction is a polar direction, thus generating an internal electric field across the InGaN QW that will ultimately reduce the overlap of both electron and hole wave functions, thus reducing the rate of radiative recombination. This is a phenomenon known as the quantum confined Stark effect (QCSE). In principle, the way to avoid this polarising electric field is to grow along semi- and non-polar

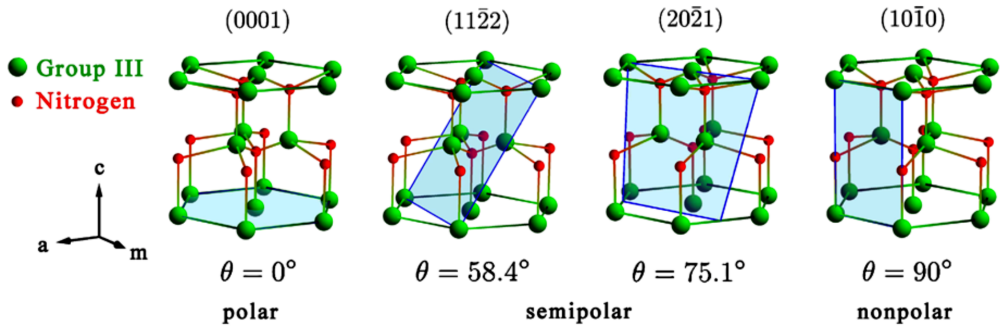


FIGURE 1.13: Orientations of c-plane (0001), semipolar (11$\bar{2}$2) and (20$\bar{2}$1)-planes and nonpolar (10$\bar{1}$0)-plane with an inclination angle θ in relation to the c-plane.From [20].

directions (the [11$\bar{2}$2], [20$\bar{2}$1] and [10$\bar{1}$0] directions illustrated in Figure 1.13). The reduced QCSE when growing in these directions should aid overall light-emission but it was found that the defect density is significantly higher [27]. The InGaN QWs which are part of the composition of an LED active region, are barely a few nanometers thick between sequences of different barrier layers (whether GaN or (reduced-In)GaN layers). Considering that the inclusion of indium in the alloy composition increases the in-plane lattice constant, the QW will therefore experience biaxial compressive strain (Figure 1.14). The thickness of the QW is required to remain below a certain critical thickness

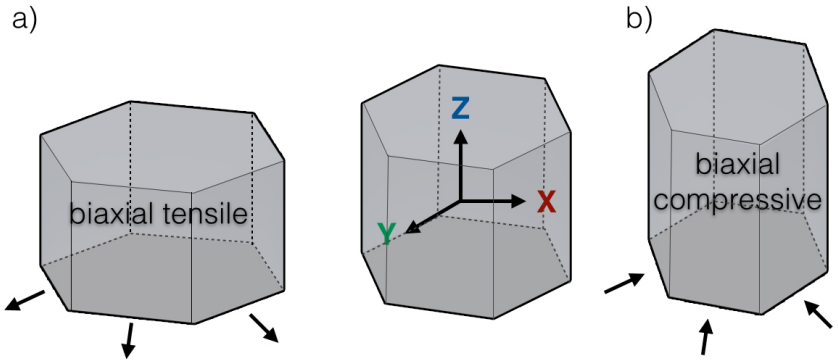


FIGURE 1.14: An example of two distorted wurtzite structures under biaxial tensile (a) and compressive (b) strain. The central figure shows the unstrained structure.

(~200$\AA$% is a typical rule of thumb for this) to avoid the formation of new TDs [20]. The resulting internal field in an InGaN QW can therefore range from 0.5 MV/cm to 3 MV/cm for a standard structure. This internal field will strongly deform the band edge in the active region affecting radiative recombination, charge transport and emission wavelength as will be seen in some of the devices presented in chapter 5. A polarising field P(C/cm^2) between the QW and a material barrier can be seen in Figure 1.15. Here, P points towards the growth direction and is therefore perpendicular to the QW [28]. This shows how a very thin (3 nm thick) QW made with a composition of $In_{0.25}Ga_{0.75}N$ can significantly distort the electron-hole wave function overlap in the well. The polarisation effect can be thought of as sheet charge layers at the interfaces between the QWs and

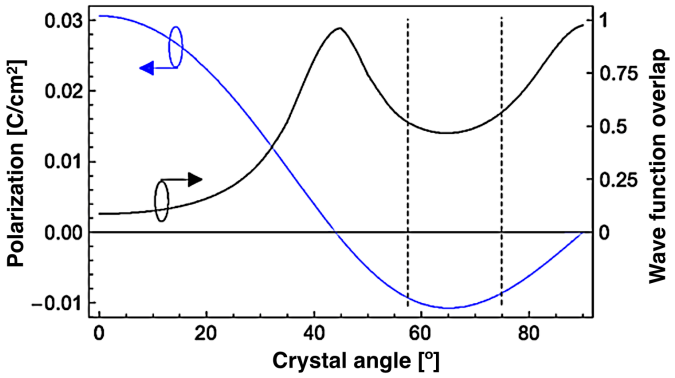


FIGURE 1.15: Polarisation field along the growth direction and corresponding wave function overlap as a function of the crystal angle for a 3 nm thick $In_{0.25}Ga_{0.75}N$ quantum well. The dashed lines indicate the semipolar $(11\bar{2}2)$ and $(20\bar{2}1)$ planes [28].

the barrier materials. For a crystal inclination of θ=45°, the different components of the piezoelectric field compensate each other, resulting in a zero polarisation field. This point shows a zero crossing of the internal field, and due to its relative proximity to the $(11\bar{2}2)$ semipolar plane - which also shows a stable growth. This is the preferred orientation for growing semi-polar LEDs with reduced QCSE, relevant for devices in the green spectral region.

1.2.2.2 Growth on Silicon

The substrates most commonly used to grow GaN-based devices are sapphire although both SiC and Si substrates have proven suitable for the growth of III-nitride materials. The LEDs produced and presented in this thesis were grown on Si substrates and the growth on this particular material will be emphasised. In order to make AlInGaN LED technology cost-competitive for illumination purposes, the processing of the materials had to be made compatible with the semiconductor industry. The semiconductor industry has a proven record/history of technologies optimised and developed to process, modify, deposit and fabricate devices on silicon substrates. This becomes crucial as a large reduction in cost per LED requires the use of larger (6" to 8" inch) Si wafers to yield the maximum number of devices for the minimum number of growth and processing runs. This is where sapphire and SiC substrates show their limitations as there is significant difficulty in producing high-quality large-area wafers. Silicon for optoelectronics has better material characteristics (thermal and mechanical) when in direct comparison with sapphire. A typical growth sequence of LED epitaxial layers onto silicon substrates is shown in Figure 1.16a), where a thick buffer layer is deposited to ensure good crystal quality. A surface photoluminescence mapping image is shown in Figure 1.16b) showing an example of the uniformity of the epitaxial layers after the growth is completed.

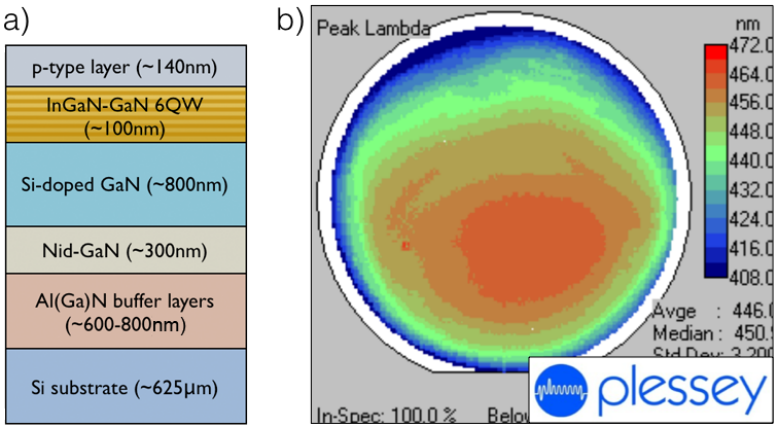


FIGURE 1.16: Typical epitaxial layer structure for LED production (a) and surface photoluminescence mapping to study layer uniformity is shown in (b). Courtesy of Plessey.

In Figure 1.17 taken from the literature, the same device architecture was fabricated on both Si and sapphire substrates [29]. The output of the LEDs on sapphire was reported to peak in optical power at lower current densities and degraded gradually as increasing currents were applied. The thermal conductivity of sapphire (k∼0.35 W/cm.K)

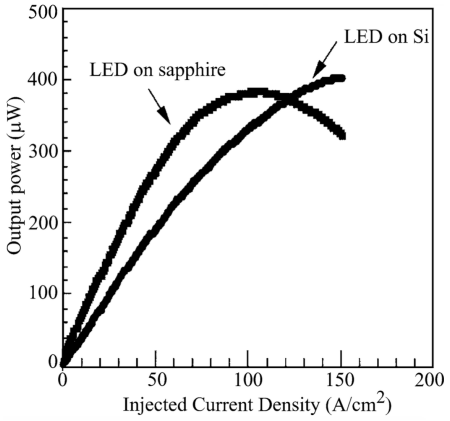


FIGURE 1.17: Comparison of the L-I curves of LEDs on sapphire and Si substrates under high-current injection. From [29].

is significantly low when compared to those on silicon (k∼150 W/cm.K) [29, 30] so it is fair to conclude that heating effects are significant in reducing the output power. The slower rise of optical power from the silicon is due to the absorption of the emission by the Si substrate itself, although the better thermal characteristics of this substrate make it ideal for devices needing to operate at high-injection currents therefore producing higher optical power [29]. However, growing GaN on Silicon substrates presents a wide range of challenges which start with some of silicon's environmental characteristics. Silicon itself, when exposed to an oxygen environment, forms a highly-stable native oxide at the surface which must be removed before any epitaxial growth can be initiated. The oxide is amorphous and removing it may add additional surface roughness which can cause

severe problems with the surface quality to accommodate the III-nitride materials growth. Due to the nature of MOCVD growth - through chemical reactions with highly-reactive precursors - Ga itself reacts with the Si substrate, creating a Ga-Si alloy which at the elevated temperatures during deposition melts the substrate, known as a a fast *melt-back* etching process. This poses as a problem since both substrate and the immediately grown film will be significantly roughened (Figure 1.18(a)). Ga can also etch into the silicon creating large pits that can propagate through all stages of subsequent material growth [31–33].

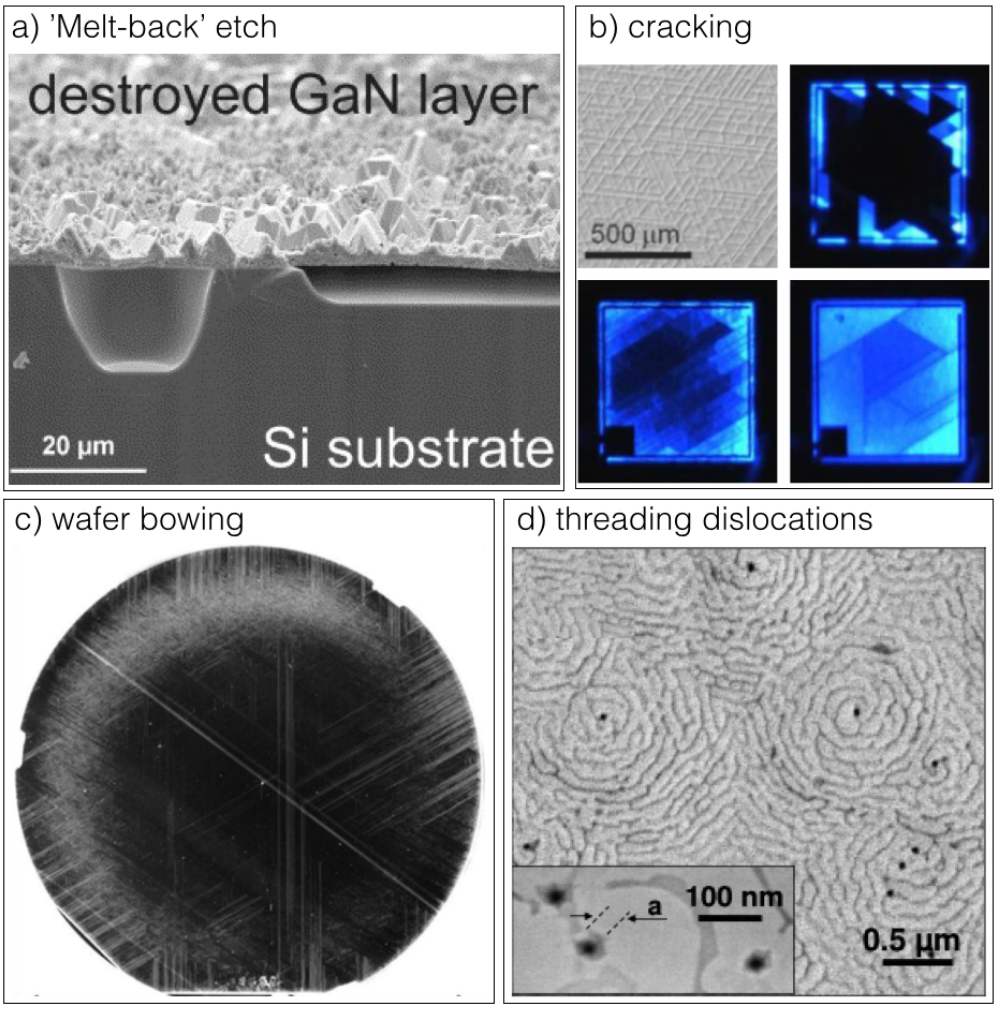


FIGURE 1.18: Typical defects observed during GaN growth on Si substrates. In (a), GaN on Si meltback etching has occurred with deep hollows on the substrate [33]. In (b) a heavily cracked GaN surface on Si is seen as are examples of completed AlInGaN-LEDs on Silicon with different levels of cracking severity [22]. In (c) the bowing effect of a poorly compensated 6" wafer during growth [34] is shown and in (d) an SEM surface image of a InGaN/GaN sample showing V-pit defects from threading dislocations during growth [35].

GaN films grown directly on Si are influenced by tensile stress during cooldown to room temperature. Significantly mismatched thermal expansion coefficients for these two

materials can induce cracking of the grown layers. Wafer cracking is a known effect that can greatly alter the emission of a device (as seen in Figure 1.18(b)) and induce severe current leakage [22]. Related to the cracking of the epitaxial films is the bowing of the wafer caused by the mismatched thermal expansion coefficients of GaN and Si (Figure 1.18(c)). Significantly, the large lattice mismatch between Si and AlGaN/GaN structures implies that if no crack-addressing measures are implemented, a significant amount of defects are to be expected. The difficulty in achieving low dislocation/crack density comes from not only the lattice mismatch but also the limited thickness of crack-free GaN that can be grown, thus limiting the use of TD/crack reduction methods which have been successfully applied when growing on sapphire and SiC substrates [22]. To overcome this issue, low-temperature (LT) ($\sim$750 ° C) AlN intermediate layers for growing AlGaN/GaN active layers on silicon were reported [36, 37]. This was considered promising as the deposition of LT-AlN intermediate layers were widely used in highly-mismatched lattice systems such as GaN and sapphire. However this was shown to be disadvantageous for Si substrates due to both high-operating voltages and series resistance for the resulting devices, an issue caused by the melt-back etching from the reaction of Si with Ga upon deposition [31, 33] which caused extremely rough surface morphology films (as seen in Figure 1.19(a)). The growth of thin AlN and AlGaN intermediate layers at high temperatures (HT) proved critical to achieve high-quality GaN films (the difference is clearly visible in Figure 1.19(b)). The HT ($\sim$1100 ° C) prevents Ga from interacting with Si, effectively avoiding the melt-back phenomena, since at high temperatures the growth changes from a three dimensional mode (seen in LT growth) to a layer-by-layer crystal growth (HT growth) [38]. Cross-sectional imaging of the AlGaN/GaN graded intermediate layer grown at HT (Figure 1.19(d)) shows no cracks or hollows at the interface between AlN and Si. In Figure 1.19(c) it is possible to see some of the major dislocations in the beginning of the GaN to bend horizontally at the GaN/SiN_x interface, due to the compressive stress caused by the larger in-plane lattice constant of GaN compared to the AlN [22]. By counting the pit density with images acquired from an atomic force microscope (AFM), the TD density can be estimated (roughly) and for III-nitride based materials, the TD density is around 10^8 cm^{-2}. With the use of a step-graded AlGaN buffer layers and a SiN_x interlayer, the quality of the grown GaN can be vastly improved. The growth and engineering of layer thickness is therefore critical to counteract this issue [31, 34, 38].

The large lattice mismatch between GaN and Si (17%) leads to dislocations in the film (Figure 1.18(d)), but III-nitride based LEDs have shown to be somewhat insensitive to the dislocation density. While LEDs can still operate and be considered high-performance, the amount of TDs has some effect on the IQE since they provide additional paths for

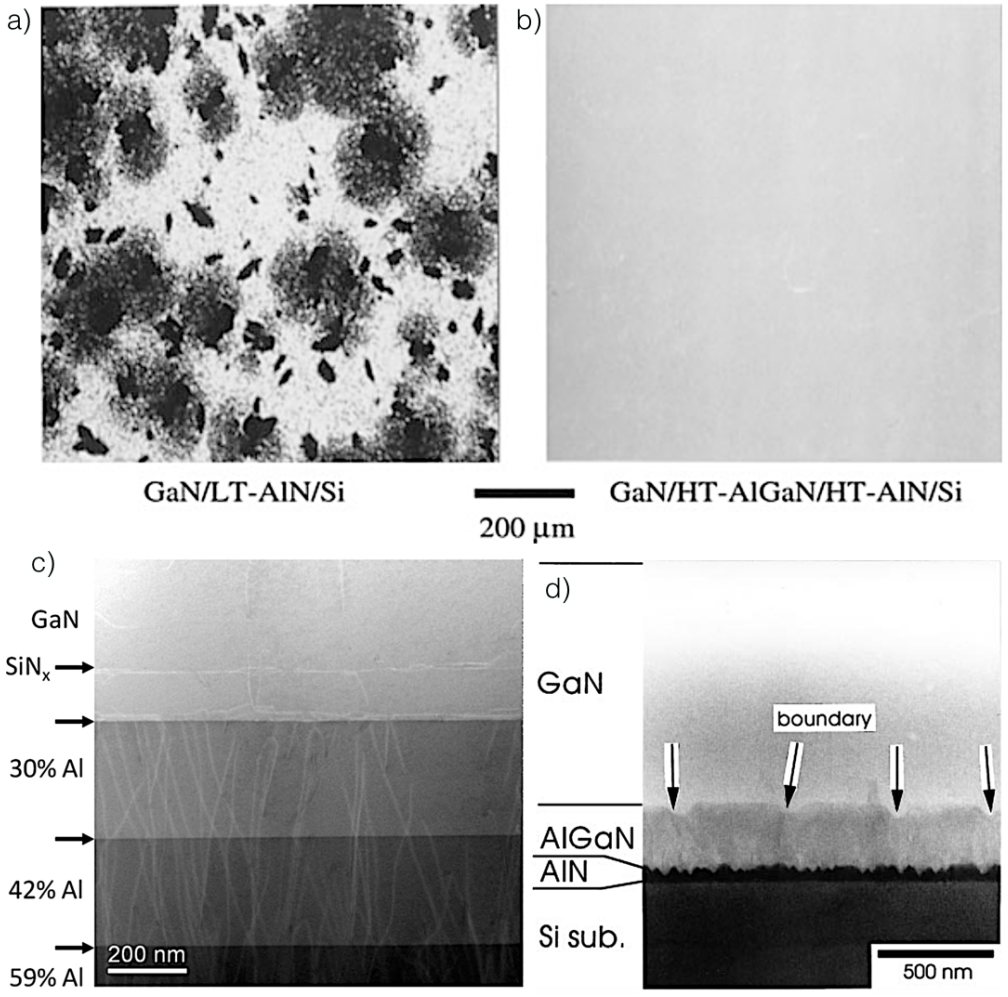


FIGURE 1.19: Crack propagation through AlN/AlGaN films: surface morphology of GaN on Si using LT-AlN (a) and HT-AlN/AlGaN (b) intermediate layers [31]. In (c), an STEM cross-section image of the uppermost portion of a step-graded AlGaN layer [22] is shown and in (d) a cross-sectional SEM image of AlGaN/AlN intermediate layers [38].

non-radiative recombination during operation. As seen in Figure 1.20(a), the defect-generated energy levels created by the dislocations are outside the bandgap of III-nitride materials so these do not act as radiative recombination centres. These dislocations are either Coulombically attractive or repulsive - depending on the dislocation type and the carrier polarity (Figure 1.20(a)). A positively charged dislocation becomes attractive to electrons but repulsive to holes. However, the continued attraction of electrons to this band's v-pits will have a screening effect on the dislocation potential, reducing the repulsive barrier for holes. Electrons and holes will then recombine non-radiatively through electron-generated intermediate states inside the dislocation line bandgap. Analogously, a negatively charged dislocation will have the same effect on hole attraction, screening and recombination. Composition fluctuations represented in Figure 1.20(b) result in localised potential minima and create an inhomogeneous bandgap in the

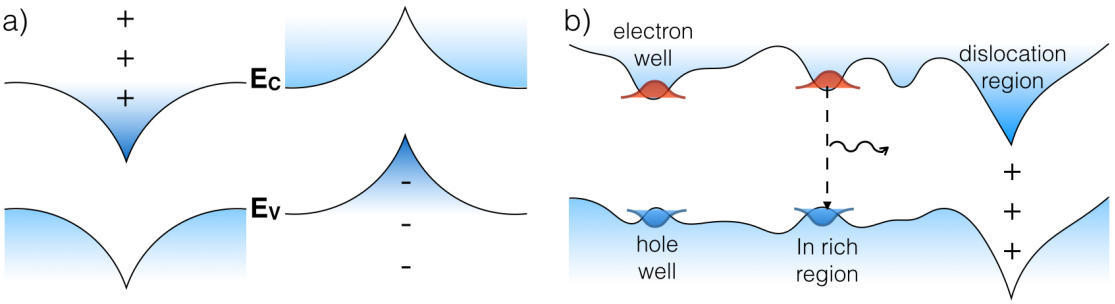


FIGURE 1.20: Proposed mechanism as to why dislocations in InGaN do not act as efficient non-radiative recombination centres: in (a), defects in the AlInGaN alloy bend the energy levels outside the bandgap. In (b), different methods for carrier confinement due to composition differences.

active layer. Carriers confined in these minima show a higher recombination rates and are prevented from diffusing to existing local dislocations. The charge screening of free carriers on the energy levels becomes more pronounced with high-injection currents where any existing inhomogeneities on the bangdap of a QW are screened through band-filling effects. While lower energy gap transitions begin the emission, further injections will aid higher energy level emissions and therefore impose a blue-shift on the peak emission wavelength. The lower-energy levels within the gap will still emit light even if the peak emission blue shifts, thus broadening the emission spectra (as is easily visible through the full width at half maximum (FWHM) of the emission spectrum).

Although it is imperative to achieve the best crystal quality, the doping of the p and n-type III-nitride materials is also crucial to achieve efficient and reliable light emission. As-grown GaN layers are typically n-type - with an electron concentration of $\sim 10^{16}$ cm^{-3} - mainly due to existing vacancies at the nitride (N) lattice points, believed to act as electron donors [39]. However, this electron concentration can be altered with the introduction of Si dopants, further increasing the electron concentration up to $\sim 10^{19}$ cm^{-3} [40]. With such active electron-donor centres (N), modifying GaN to be a p-type semiconductor is not a straightforward process. Magnesium (Mg) has been used for this purpose, but the wide availability of N-donors limits the achievement of a high-hole density p-type GaN layer (to $\sim 10^{17}$ cm^{-3})[41]. During growth, the use of Hydrogen (H) as a gas is also common within the MOCVD chamber, which in turn can chemically deactivate the Mg doping. Both Mg and H bind together and while not being electrically active, as-grown Mg(H)-GaN complexes typically require high-temperature ($\sim 600^{\circ}$ C) thermal annealing in a Nitrogen-rich environment to break existing covalent bonds between Mg and H atoms. This not only electrically activates the existing Mg centres but it also removes any existing H that is bonded with GaN in the growth process.

1.2.2.3 Polarisation effects and efficiency

As already discussed in section 1.2.2.1, III-nitride materials are typically grown in the [0001] direction, normal to the (0001) c-plane (Figure 1.13). The grown materials demonstrate intrinsic polarisation effects (due to chemical factors, i.e. Indium inclusion) and strain-induced polarisation effects (due to physical factors, i.e. lattice constants). Both types of polarisation cause charges to be distributed separately at the interfaces which induces an electric field within the material. Another source of polarisation occurs spontaneously which is intrinsic to the material itself due to the asymmetrical atomic bonding of the wurtzite crystal structure, although spontaneous polarisation effects in III-nitride materials are rather weak.

The resultant LED p-n junction internal electric field (E_{Vbi}) depends on the growth direction and layer arrangement. Considering that the p-GaN layer is usually the top layer of the structures used, the internal electric field will be opposed to the growth direction pointing towards the n-GaN/substrate ($[000\bar{1}]$ direction) [42]. Note that E_{Vbi} would have the opposite direction if the polarity of the grown layers were reversed: n-type GaN on top, p-type GaN on the bottom.

The strain a material experiences can also create opposing piezoelectric fields. In the case of compressive strain - where a material is laterally compressed - an GaInN layer grown on a relaxed GaN layer along the [0001] direction will be under compressive strain since its lattice constant is higher than the GaN (Table 1.1). The resultant piezoelectric polarisation field will be aligned with the growth direction (as illustrated in Figure 1.21 [20, 43]. An analogous case can be made for III-nitride alloys experiencing tensile strain,

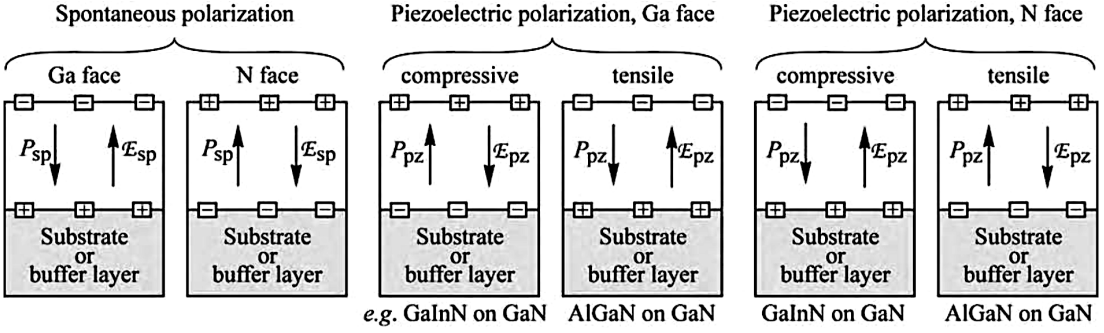


FIGURE 1.21: Surface charges and direction of electric field and polarisation field in III-nitrides for Ga and N face orientations. From [12].

where the material is forced to expand laterally (i.e. the case of growing AlGaN on a GaN buffer layer), since the smaller lattice constant will generate tensile strain on the AlGaN layer (Figure 1.21), thus opposing the growth direction. The effects of piezoelectric polarisation in AlInGaN based LEDs hence must be taken into account during growth, since the active region of these devices comprises several different composition alloys

($In_xGa_{1-x}N$ and/or $Al_xGa_{1-x}N$) with mismatching lattice constants. Thus piezoelectric effects become quite pronounced at each QW region since each is formed by thin sequential layers of different material alloys with different lattice constants. Due to this, the QW idealisation of well-defined *flat* band structures has to be abandoned and these considered to be distorted similar to a tilted triangular-shaped energy band. This distortion is quantifiable and the reduction of the bandgap at the QW is given by $eE_{pz}L_{QW}$ [44]. A visual representation of this distortion and how it affects the QW energy levels can be seen in Figure 1.22:

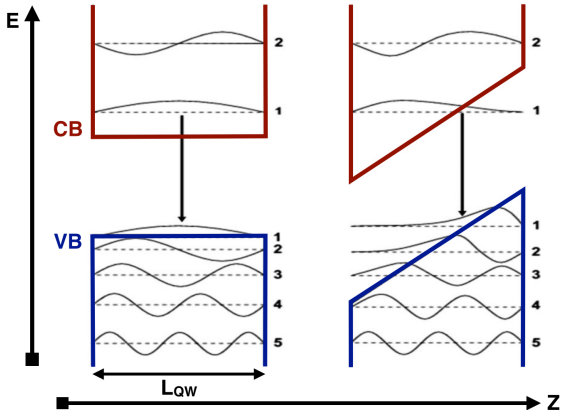


FIGURE 1.22: Band structure effects of an internal electric field in a typical QW structure. From [45].

The reduced overlap of electron-hole wave functions at the different energy levels are represented, a condition that reduces the efficiency of radiative recombination. Also, significantly, a reduction of the bandgap occurs meaning that emissions at lower external bias/charge injection will have their peak emissions at longer wavelengths, proceeding to higher-energy wavelengths as the QW are screened with further charge injections and the strain-induced polarisation influence becomes reduced.

Several methods have been proposed to reduce polarisation effects with the most common way being QW thickness reduction or heavily Si-doped n-type GaN which reduces the QW effect on distorting the wave-functions [12, 45, 46]. As mentioned, high-carrier injection reduces the polarisation effect and as seen in Figure 1.15, the growth of III-nitride materials on different planes (non-polar) shows these to be less-affected by piezoelectric effects.

As the different lattice mismatches induce different strain levels for different alloy compositions of III-nitride materials, these are a major intrinsic source of piezoelectric polarisation effects. Several researchers have been trying to circumvent this issue with alternative methods to compensate and counteract the inherent strain with the inclusion of micro-scale structures [47] during growth. Relevant findings which are presented in

this thesis in chapter 5 regarding the spectral behaviour and evolution of TP LEDs show how the emission shifts during high-carrier injection, screening the MQW internal electric fields.

1.2.3 LED Efficiency droop

Although III-nitride based materials present many advantages for visible wavelength operation, they have their drawbacks. Their operating efficiency is best at relatively low current densities (~10 A/cm^2) and reduces as the injected current is increased. This phenomenon has been labelled *efficiency droop* and has been extensively studied in recent years, in an attempt to understand why visible-light $In_xGa_{1-x}N$ LEDs and UV $Al_xGa_{1-x}N$ LEDs are systematically affected by this gradual loss in efficiency [48, 49]. The effect of efficiency droop for blue $In_xGa_{1-x}N$-based LEDs can be seen in Figure 1.23(a) for c-plane (0001) growth and in Figure 1.23(b) for m-plane ($10\bar{1}0$) growth on sapphire substrates. Thermal effects are known to have a negative impact on device performance, as the difference of the extracted optical power (excluding inherent losses) to the injected electrical power typically indicates how much is lost non-radiatively. Attempts to avoid thermal effects and device self-heating during operation mean driving the LEDs in pulsed-mode such as being driven at a repetition rate of 1 kHz and a duty cycle of 0.1% as seen in Figure 1.23(a,b) [50].

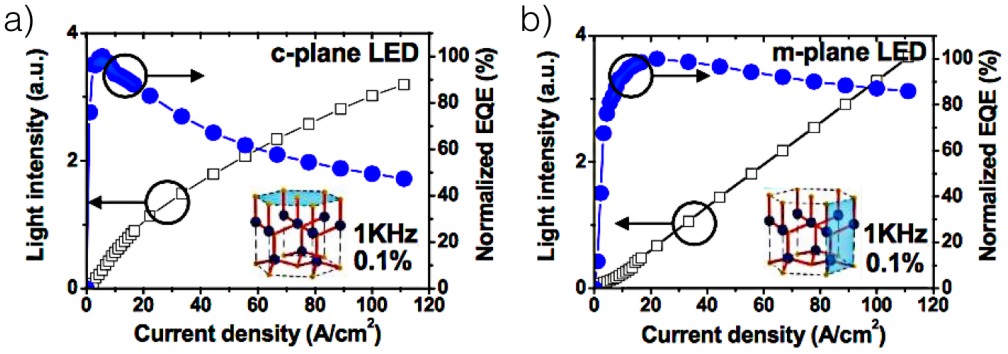


FIGURE 1.23: Electroluminescence (EL) intensity and normalised EQE as a function of forward bias current density operation for c-plane (a) and m-plane (b) LEDs, both samples having the same MQW active region and electron blocking-layer (EBL) structure. The operating duty cycle for these measurements is 0.1 %. From [50].

In a similar fashion for Si-grown LEDs (and using material from the same batch reported on Figure 1.16), Pengfei et al [51] has studied the EQE efficiency droop on devices still in their growth wafers. These show a more accentuated decay in efficiency with higher operating current densities. These were processed in a top-emitting configuration and thus, significant losses are expected to occur due to the non-optimised configuration for light extraction. Nonetheless, and contrary to the LED performance reported on Figure 1.23(a,b), during DC operation the LEDs show an significant efficiency droop at

relatively low current as seen in Figure 1.24. The peak efficiency is attained at low current

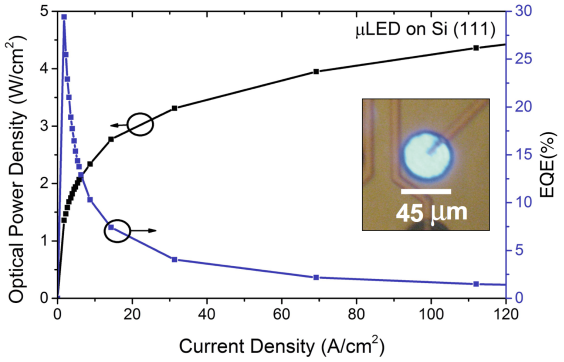


FIGURE 1.24: Optical power density and EQE as a function of forward bias current density operation for μLEDs operating in their Si growth wafer. The inset shows the pixel during operation. Adapted from [51].

densities where electron leakage effects and carrier overflow effects can be discarded. The encouraging results obtained show that further improvements for LEDs on Si are needed as to make these competitive with established sapphire-LED technologies.

While the mechanism of efficiency droop is still not fully-understood, several attempts at studying its origins and underlying mechanisms have been proposed, although none has been generally accepted. The two most recognised models will now be described. First is that of the Auger recombination, a process involving a three-carrier interaction. During electron-hole (e-h) recombination, the resultant energy (approximately close to the bandgap) is transferred to another e-h pair. The energy resulting from the transfer of energy between e-h pairs is dissipated by exciting higher-energy electrons present in the conduction band or deep-holes in the valence band [12]. The influence of Auger recombination on LED efficiency droop is commonly studied using the following equation (while neglecting any existing carrier leakage):

$$\eta_{IQE} = \frac{Bn^2}{(An + Bn^2 + Cn^3)} \tag{1.15}$$

with n being the carrier density, A being the Shockley-Read-Hall recombination, B the radiative recombination and C the Auger recombination coefficient. This non-radiative coefficient rate ($R_{Auger,nr}$) can be given by:

$$R_{Auger,nr} = C_n n^2 p \tag{1.16}$$

and

$$R_{Auger,nr} = C_p n p^2 \tag{1.17}$$

where n and p are the corresponding carrier densities and C the Auger recombination coefficient with the units $\mathrm{cm}^{-6}\mathrm{s}^{-1}$. The rate, as described by this last pair of equations,

is proportional to the square of the carrier density, with both processes modelled by equation 1.16 and 1.17 being more likely to occur in n-type semiconductors than p-type, since n-type semiconductors tend to have a higher dopant density [12]. This mechanism was first proposed by Shen *et al.* [50] where they performed efficiency droop studies with quasi-bulk InGaN layers and estimated the recombination coefficient C to be $\sim 10^{-30}\mathrm{cm}^6\mathrm{s}^{-1}$. Piprek [52] reported an extensive study on simulating different Auger recombination coefficients and their impact on LED performance as seen in Figure 1.25(a). Clearly visible are the effects that the Auger coefficient imposes on the LED efficiency

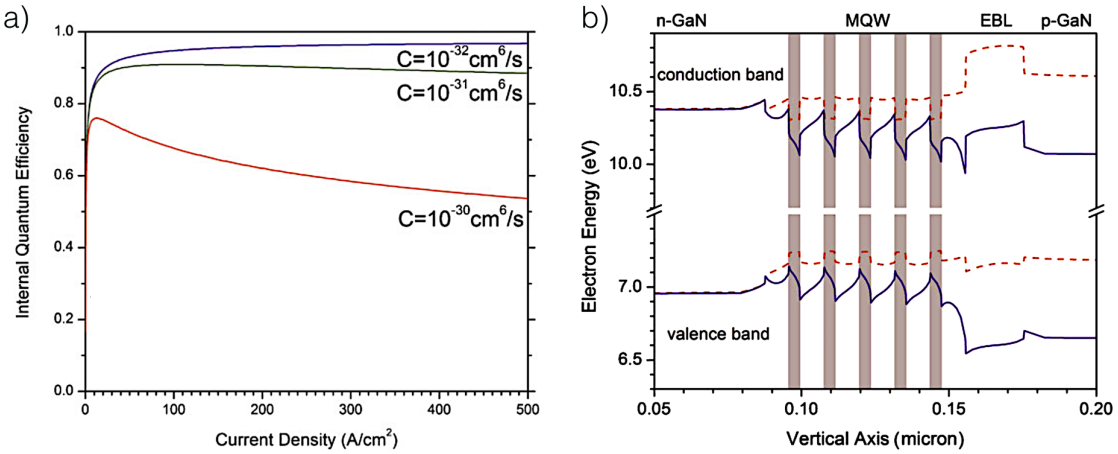


FIGURE 1.25: Parameter simulation on III-nitride based LEDs: (a) IQE plots for LEDs with different Auger recombination parameters and in (b), the simulated energy band diagram at the MQW region with (solid lines) and without (dashed lines) polarisation. From [52].

in the high-current regime, which can result in a significant droop. The study of Auger recombination continues, with new influences being considered, including photon-assisted Auger recombination [53] and indirect Auger recombination [54]. Recently, Iveland *et al.* [55] addressed $In_{0.18}GaN_{0.82}N/GaN$ LEDs and measured these with electron emission spectroscopy, where they observed Auger electrons being emitted, confirming the hypothesis of non-radiative recombination as a dominating mechanism for reducing the IQE efficiency during high current injection.

Another significant and widely known phenomenon during high-current injection is carrier leakage. Along with other pathways for carrier leakage - e.g. through defect level tunnelling [56] - failure to capture all of the injected carriers [57] into the active area is the most common issue for carrier leakage since the excess carriers will overflow and escape the MQW area. Typical III-nitride based LEDs architectures therefore include an electron blocking layer (EBL) to prevent significant carrier leakage from the MQW area. A complementary charge-trapping layer is typically introduced as a barrier to contain charge recombination within the active area, although close proximity to the MQW region sees its effects reduced (as seen in Figure 1.25(b)). This is due to the MQW polarisation

influence, and the simulated energy levels with (solid lines) and without (dashed lines) polarisation in Figure 1.25 clearly show that the introduced EBL is screened by the close proximity of the polarising fields. To be noted is a slight decrease in the conduction band energy from the n-type semiconductor in comparison to the p-type. Without an efficient EBL impeding charges from diffusing further than the active area, electron leakage during high-current injection is a significant source contributing to the efficiency droop. Schubert *et al.* [58] have shown that the use of quaternary alloys (AlGaInN) aid in the reduction of the droop effect while increasing the light output power. The droop effect is therefore supposed not to be related to the junction temperature and is related to the strong polarisation fields at the MQW active region. Kim *et al.* studied quaternary AlGaInN alloys and EBL that can both be polarisation-matched to the QWs and GaN to help reduce carrier leakage and efficiency droop during high-current injection [59].

1.3 Transfer Printing of μLEDs

Transfer-Printing (TP) at the micron scale (μTP) is a recent technology for heterogeneous assembly that enables the integration of optoelectronic devices onto non-native substrates. This technique at the microfabrication and semiconductor level was developed by John Rogers' group at the University of Illinois in Urbana Champaign [60, 61]. The most immediate analogue to this technique is ink stamping onto paper, where a stamp is wetted in an ink reservoir which then deposits the ink onto any substrate it gets into contact with. While there are several methods that are related to transfer printing (e.g. the use of ink transfer or nanoparticle printing [62]), at its heart μTP involves the integration of wide arrays of microscale-sized materials and/or devices onto different substrates by using an elastomeric *adhesive* stamp.

To prepare the devices to be transported onto new receiving substrates, they have to be processed to remove existing intermediate (and usually underlying) sacrificial layers, resulting in suspended membranes. In this work this results in the the complete set of epilayers comprising an LED being left suspended, held by sacrificial anchors that break when devices are transported with the elastomeric stamp (as shown in Figure 1.26a))[63, 64]. The fracture of the anchors releases the devices from their growth substrate so they can then be transported to the receiving substrates via the elastomeric stamp as illustrated in Figure 1.26b). The key component controlling the picking up, transport and printing of the devices is the elastomeric stamp. Its geometry and format can be tailored to accommodate a wide range of materials depending on their characteristics (device geometry, application type, material rigidity, thickness, mechanical strength, etc.)

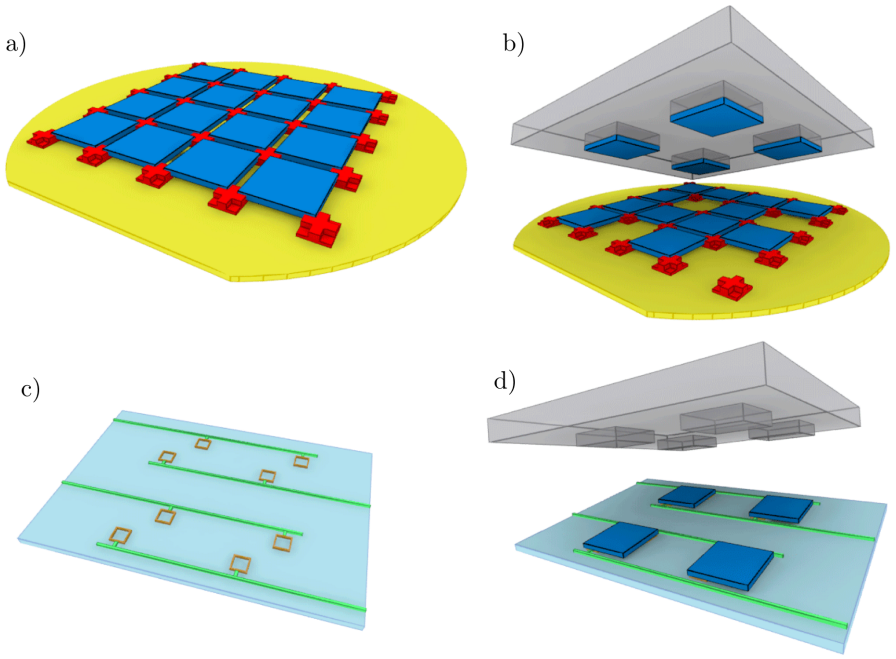


FIGURE 1.26: Transfer Printing shown step-by-step: in a) a large array of devices (blue) can be fabricated on a donor wafer and be suspended by sacrificial anchors (red). In b) the corresponding elastomeric stamp posts (grey) fracture the devices anchors at specific locations ready for transporting the devices. In c), a pre-patterned receiving substrate with alignment marks facilitates the deposition and in d) the stamp is shown free after releasing of the devices on their new receiving substrate.

[61, 65, 66]. Stamps are typically made by simply casting liquid Polydimethylsiloxane (PDMS) onto a micro-fabricated mould. The stamp or the materials can be coupled to precise translation stages to aid the manipulation of objects at a scale not possible by conventional methods. By automating the positioning and speed, devices can be transported and integrated in a massively parallel way (as exemplified schematically in Figure 1.26(a to d)). The mechanics of this process will be described in the next chapter.

The μTP technique has been employed to assemble a multitude of optoelectronic devices onto non-native substrates. Demonstrations of the technique's reliability and capabilities include efficient inorganic solar cells [67], flexible displays [68], novel laser systems [69], LED arrays [63, 64], bio-compatible sensors [70], and transistors [71].

Rogers' group has reported arrays of μm-sized LEDs deposited on both flexible and rigid substrates. These reports had a significant impact in demonstrating the challenges and engineering required to enable the integration of a wide range of optoelectronics onto a broad range of substrates. In Figure 1.27, some of these demonstrations are presented, showing arrays of broad-spaced LEDs onto flexible substrates, typically coated with adhesion enhancement layers. The group also reported the changes of the physical and electrical characteristics of the devices during operation [63, 71–74]. Some of this work has been ongoing during the time of the work described in this thesis.

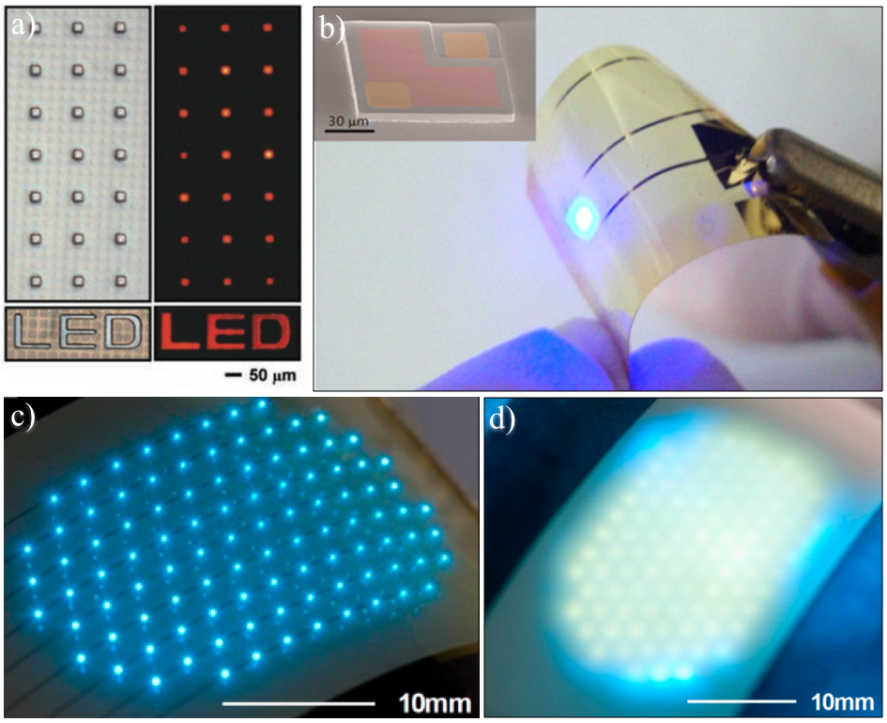


FIGURE 1.27: TP integration of LEDs as demonstrated by the Rogers group: a) integration of red-emitting GaAs LEDs onto glass, b) integration of blue-emitting AlInGaN-based LEDs onto a flexible transparent plastic film, c,d) Integration of blue-LEDs on a laminated substrate with LED-matching YAG:Ce phosphor islands and a diffuser film. From [63, 72, 73].

The thesis here-presented describes how the implementation of TP capabilities at the Institute of Photonics took place from a starting point in 2011, showing the initial steps to attain similar capabilities to other reports. The performed adaptations to the assembly system used to fabricate the devices, the improvement of the positioning capabilities and precision (note that all demonstrations in Figure 1.27 made use of broad-spaced LEDs with some publications claiming a precision accuracy of no better than $\sim$1 μm), the optimisation of the optoelectronic performance and approach to obviate the use of adhesion enhancement layers are all described. In particular this thesis reports on the use of releasable micron-sized AlInGaN-on-Si LEDs and the optimisation of their development so that devices not only could be deposited on a wide range of substrates - whether rigid or flexible - but also had reliable, efficient and consistent performance throughout their operation range. The use of what can be called a temporary adhesion enhancement layer (through capillary bonding) enabled the deposition of LEDs onto substrates including flexible silica, plastic films, self-adhesive membranes, tin foil, paper, II-VI semiconductor platelets, polymer optical fibers and patterned-sapphire.

1.4 Thesis Outline

This chapter has presented a general overview of the physics and advantages of III-nitride based LEDs as well as the objectives for the research here presented. Chapter 2 will describe the mechanics of the experimental techniques used to create transferrable light emitting devices, the framework to produce elastomeric stamps and dummy alignment generation for the receiving substrates. Chapter 3 describes the initial attempts to electrically address TP LEDs, the failure analysis for the unreliable bonding and the change to better-performing metal tracks. This chapter concludes with a demonstration of nanoscale accuracy positioning for the TP technique. Chapter 4 shows in detail the curvature of the released micron-size LEDs and estimates the adhesion bond formed with substrates by use of *temporary* capillary-forces. In chapter 5 we demonstrate the performance improvements and device optoelectronic characteristics when the LEDs were printed onto heat-efficient substrates. A thermal study was conducted to assess how the substrate influences the overall device performance. With the new operating capabilities, applications such as data transmission and colour conversion are then described. Finally, the conclusion of this thesis, including future work plans, is given in chapter 6.

Chapter 2

Mechanics of transfer printing and associated device fabrication

This chapter describes the mechanics of so-called reversible adhesion and shows how an elastomeric stamp can display a dual-behaviour depending on the speed that the translation stages of the system described later in section 2.3 are operated. The framework and equations for reliable stamp operation are described and studied, with examples of its operations shown. Estimates of the forces involved throughout the transfer printing process are obtained. The multiple techniques used for producing all of the components needed for transfer printing (i.e. stamps, LED devices) and receiving substrates) are described and the chapter concludes with an overview of the adaptations performed to the nanolithography system used for transfer-printing.

2.1 Mechanics of reversible adhesion

To transport structures at small scales ($<1\text{mm}^2$) from their growth wafers to new, capability-enhancing substrates, requires the use of tools that ensure repeatability and precise positioning of the devices throughout the full procedure. The Rogers' group has pioneered the fabrication, modelling and optimisation of PDMS elastomeric stamps which were purpose-made for transfer-printed optoelectronic integration [60, 61, 63, 75]. The main operation during TP relies on the ability to finely tune the overall adhesion force at the various materials' interfaces during pick up, transport and printing stages. Viscoelastic materials such as PDMS are mouldable by nature but can display solid properties if subject to fast movement/deformations. Elasticity in materials is itself an idealisation, restricted to a certain range of forces. When such forces are excessive, all materials will deform to an extent, and for excessive forces, even fracture [76]. When

elastomeric materials are manipulated slowly, they conform to their surroundings creating an intimate bond with any contacting surface.

The two most important interfaces for TP are illustrated in Figure 2.1 and represent a typical *pick & place* operation. Soft-viscoelastic materials are crucial for stamps as they display ideal properties to conform to flat and/or rough surfaces. The adhesion force can be kinetically controlled: a fast retraction speed - i.e. quick peeling rate - between the stamp and the devices is used for picking up materials. For device printing purposes, a low retraction speed is used, allowing the stamp to gently peel from the surface, minimising the adhesion force in the interfaces [77]. Slow retraction is used

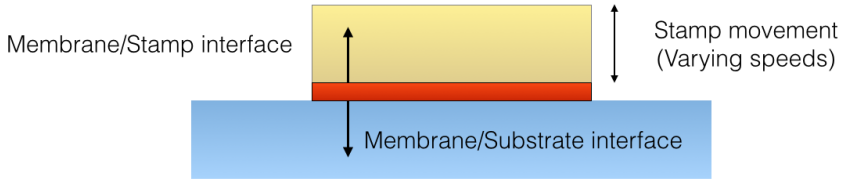


FIGURE 2.1: Simple schematic of the interfaces in a typical transfer-printing operation. The three layers (stamp, device/membrane, substrate, in descending order) generate two material interfaces. Careful or sudden retraction of the stamp defines the conditions for both printing and picking up of devices.

when on the receiving substrate, so that the adhesion force of the substrate surpasses the adhesion force of the transporting stamp sitting on top of the device. This is usually achieved with adhesion-enhancement layers (adhesive tapes, glue, spin-coated epoxies, etc.). However for substrates where these cannot be used, or the use of adhesives is undesired, the contact area on top of the devices has to be reduced to therefore ensure an inferior adhesion force when competing with the substrate adhesion force. This ensures the device is released onto the new substrate and the stamp is freed up for the next transfer operation. To reduce this area of contact before printing onto the new substrates, Kim *et al.* [63] introduced onto the stamp a set of pyramid-shaped compressible protrustions (as illustrated in Figure 2.2(a)). These tips can be compressed during pick up until the stamp roof is collapsed, significantly increasing the contact area. By roof collapse, it is meant that the pyramidal protrusions are pressed in so that the full underside of the stamp adheres to the surface of the structure to be picked up. Optical photographs of such stamps in direct contact with an LED are shown below in Figure 2.4. The collapsed area is shown darkened to aid visualisation. For the stamp configuration used, the pyramidal features are continuously working against the picked up platelet, forcing the stamps to slowly relax to their uncompressed original shape after pick up as illustrated in Figure 2.2(a) and (b). When the stamp is allowed to return to its original shape, the pyramid tips alone are responsible for suspending the devices in air.

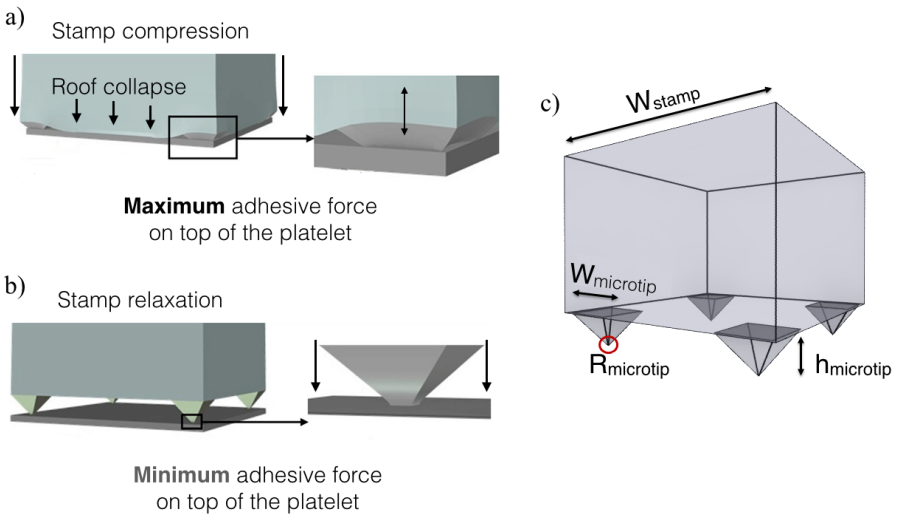


FIGURE 2.2: Schematic of an elastomeric stamp during pick & place operations. In a), the stamp is compressed against the target platelet. The roof collapses due to a load force to maximise the contact area for platelet pick up. In b), the stamp returns to its original shape and the platelet is gently retracted while being held by the pyramid tips on each corner of the stamp. In c), the dimensions relevant to elastomeric stamp design are shown. Adapted from [75].

The stamp compression described above causes significant changes in the overall contact area on the stamp/membrane interface, and a careful set of rules have to be met to guarantee reliable and repeatable operations [63]. The most important parameters for reversible adhesion in elastomeric stamp design are the micropyramid height $h_{microtip}$ (and corresponding pyramid width $W_{microtip}$, with these two being intrinsically linked as described further in section 2.2.7) and overall stamp width, W_{stamp}, as shown in Figure 2.2(c). Upon approach, when contact between the tips and the platelet is established - and there is no significant compressive force being applied - the adhesion energy is governed by the pyramid tips. Further compressions to the stamp will cause the roof to collapse, which adds a collapse potential energy, $U_{collapse}$, to the stamp. For a stamp with micropyramids (with height $h_{microtip}$, width $w_{microtip}$, tip radius $R_{microtip}$ and spacing between tips within the stamp lateral width w_{stamp}), the roof collapses onto the platelet over a length of $2c.w_{stamp}$ due to the materials' adhesion force and applied preload [75]. The factor $2c$ represents the collapse percentage on the stamp surface yielding a total potential energy U_{total} for stamp relaxation of:

$$U_{total} = U_{collapse} - 2c.w_{stamp}.\gamma \tag{2.1}$$

where γ is the work performed by the surface adhesion [75]. The percentage of roof collapse ($2c$) is determined by a reduction of the total potential energy. When the change to the total potential energy due to changes in the roof collapse percentage (c) is zero ($dU_{total}/dc = 0$), Wu *et al.* formulated the collapse as dependent on the $R_{microtip}/w_{stamp}$

ratio and the *adhesion energy* to *strain energy* ratio: $4\gamma w_{stamp}/\bar{E}.h^2_{microtip}$ [75]. Here, $\bar{E}$ relates to the plane-strain modulus of the stamp ($\bar{E}=4E/3$) and E is the stamp material Young's modulus.

For $h_{microtip} > h_{min}$, the overall potential (U_{total}) energy is positive. This means that without external preloads, the stamp's roof will not remain collapsed onto the platelet upon successful pick-up and will force the relaxation of the stamp back to its original shape. How quick the stamp shape is restored can be tuned with different pyramid heights ($h_{microtip}$). For one pyramid in each corner of a squared stamp, Wu *et al.* [75] formulated the equations 2.2 and 2.3 for the minimum and maximum pyramid height and established theoretical 3D models based on Kim *et al.*'s analytical results [63]. For the minimum pyramid height:

$$h_{min} \approx \sqrt{\left[3.04ln\left(\frac{w_{stamp}}{R_{microtip}}\right) - 4.44\right]\frac{\gamma w_{stamp}}{\bar{E}}} \tag{2.2}$$

and for the maximum pyramid height:

$$h_{min} \approx \sqrt{\left[5.14ln\left(\frac{w_{stamp}}{w_{microtip}}\right) - 1.75\right]\frac{\gamma w_{stamp}}{\bar{E}}}$$

$$\times\, exp\left\{0.371\sqrt{\frac{\gamma}{\bar{E}w_{stamp}}}\left(\frac{w_{stamp}}{w_{microtip}}\right)^2 \times \left[1 + \frac{2.08 + ln\left(\frac{P}{\sqrt{\gamma\bar{E}w^3_{stamp}}}\right)}{\sqrt{2.14ln\left(\frac{w_{stamp}}{w_{microtip}}\right) - 0.73}}\right]\right\} \tag{2.3}$$

with $\gamma = 0.155$ Nm^{-1} representing the work of adhesion on a PDMS/Si exemplar interface and P being the stamp preload, ranging from 0.001, 0.003 and 0.005 N depending on the $h_{microtips}$ [75], closely matching the experimental results of Kim *et al.* [63]. The estimated $R_{microtip}$ was 750 nm and the w_{width} considered were 100 μm. For this, equation 2.2 gives $h_{min} = 8.2$ μm.

This set of equations defines the basic framework for establishing predictable and reliable elastomeric stamp architectures. They model the maximum and minimum heights of the pyramids ($h_{microtip}$), which represent a crucial parameter of elastomeric stamp operation, as excessively-tall pyramids during compression will have a large elastic restoring force after the preload is removed (during quick stamp retraction) and can completely eject the platelet from the stamp. This can cause tilting of the platelet position, causing the platelet to be suspended at an angle, or completely ejecting the platelet. For insufficient pyramid heights, the restoring force will not be enough to cause the desired relaxation of the stamp to its original shape, meaning the roof of the stamp will remain collapsed and

the stamp may fail to release the device to be free for the next TP step. Figure 2.3(a) and (b) show the normalised modelling of the heights that allow a comfortable zone of operation for successful pick-up and printing. In Figure 2.3(a), the minimum height for

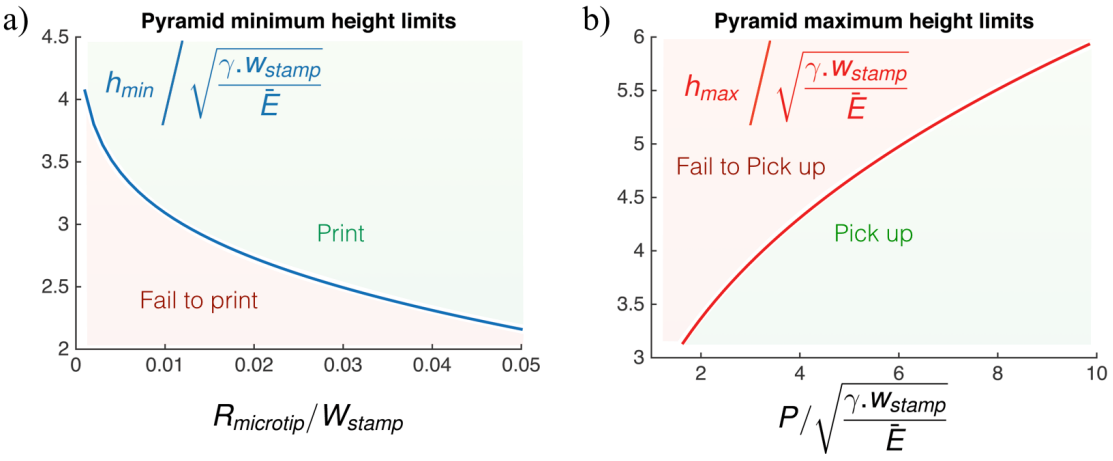


FIGURE 2.3: Normalised pyramid height calculations for elastomeric stamps: a) normalised minimum height of micropyramids vs. the normalised microtip radius $R_{microtip}$ from equation 2.2, b) the normalised maximum height of microtips vs. the normalised preload calculated from the analytical model of Wu [75].

the pyramids is normalised by $\sqrt{\frac{\gamma . w_{stamp}}{\bar{E}}}$ and shows a steady decrease as the tip radius to stamp size ratio increases. While the tip radius is rather constant due to the nature of the wet-etching of silicon (fully described in section 2.2.7), the stamp size can be varied. Thus for an increasing stamp size (considering that $w_{stamp} \gg R_{microtip}$), the minimum height required to aid the stamp return to its original shape increases accordingly. For the maximum height established by equation 2.3, the normalised maximum height requires a higher preload to ensure a successful pick-up of the platelets. The achievable maximum height ($h_{microtip}$) therefore shows a strong dependence on the required preload and there is a severe experimental limitation to forcing higher preload values on an already compressed stamp as damage to neighbouring pixels (and the stamp itself) can occur. This dataset developed by Wu *et al.* [75] enabled the implementation of these scaling laws for the elastomeric stamps produced for this work.

To estimate the areas and the magnitude of the adhesion forces involved, further calculations were made on the contact area. The pyramid size is intrinsically related to the overall roof collapse area that is in effective contact with the platelets, the latter being the highest contributing factor to successfully removing the platelets from their growth wafers. Figure 2.4(a) shows how the overall contact area changes as a compressive load is applied to the stamp through the Z (vertical) axis. The blue line represents, for comparison, the area generated by a single ideally compressed pyramid. Due to the viscoelastic nature of the stamp material, experiments have shown the roof collapsing towards the platelet (at Z~6.6 μm) before the Z movement matches the full uncompressed height (Z~8 μm) of

the pyramid (as seen in the red line). The insets in Figure 2.4(a) are top-view microscope

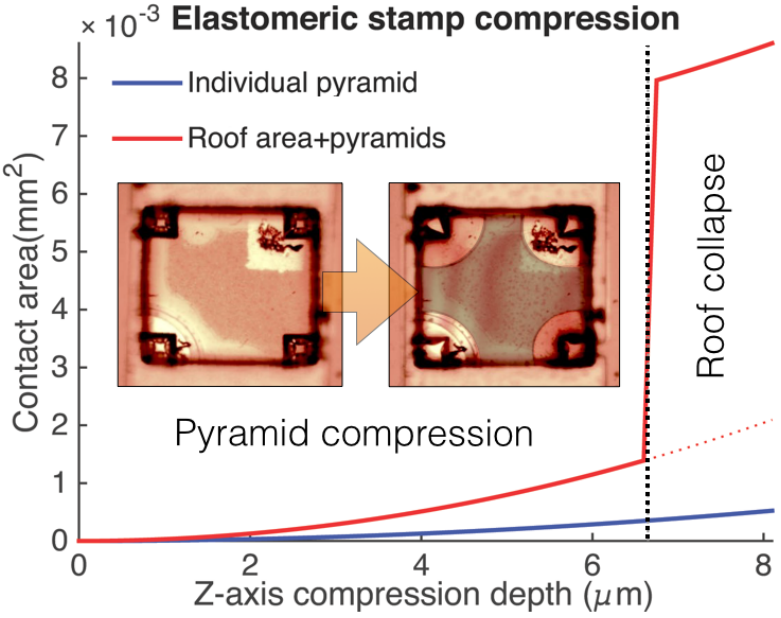


FIGURE 2.4: $100\mu m^2$ stamp contact area calculations: The contact area for an individual pyramid and four pyramids and full stamp roof collapse is shown. The inset plan-view optical images as viewed through the stamp illustrate the change from having only the pyramid tips in contact to the roof-collapse (*cross-shaped* central area) condition.

images taken through the elastomeric stamp directly positioned on top of an LED. One can see the visual difference in the contact area upon roof collapse (as described previously in Figure 2.2). The collapsed area has been darkened here to aid visualisation as this is barely perceivable due to the stamp transparency. Further compressions can be made to the stamp after this and it has been observed that this will increase the contact area but not to a significant extent. This has an undesirable effect as it also increases the compressive energy stored in each pyramid tip, thus causing faster stamp relaxation once the stamp is retracted. Depending on the pyramid height, the PDMS curing agent to polymer ratio and the elastomeric stamp surface oxidation level, this relaxation can take from 1 to 10 seconds for a stamp to fully relax. Dirt or dust particles can accelerate this process, although, these are considered to be a parasitic factor on the contact surface as it has been observed that a dust particle generates zero-adhesion areas in its immediate vicinity that can be ten times bigger than its own size. This has been observed when during the assembly of some devices as the nanolithography system used was not placed in a cleanroom environment and therefore is exposed to undesired dust particles.

Due to the nature of elastomeric materials, quick forces or perturbations are met with solid-like behaviour since the return to equilibrium shape for the stamp is a slow process. Hence, during quick retraction of an elastomeric stamp, for a brief instant the contact area is assumed to be static and stable between the stamp/platelet interface. The forces at this interface binding the materials together - after removal of any preload forces -

are mostly van der Waals' forces [76, 78] where local fluctuating atomic dipoles interact at the surface. These forces are rather weak if considering only two atoms interacting between themselves. However it is the additive nature of all the surrounding atoms interacting simultaneously that can generate a strong attractive force over a significant area. Considering a spacing h between two semi-finite sheets of the same material, the total surface interaction $U_{(h)}$ per unit area can be written as [76, 78, 79]:

$$U_{(h)} = -\frac{2\pi\rho^2 C}{12}\int_h^\infty \frac{dz}{z^3} = -\frac{A}{12\pi h^2} \tag{2.4}$$

where A is a defined constant known as the Hamaker constant, a material property with the dimensions of energy with values ~of 4.5x10^{-20} J for PDMS [79, 80]). From equation 2.4 the adhesion force $F_{(h)}$ between two flat plates at a distance h is given by:

$$F_{(h)} = -\frac{A}{6\pi h^3} \tag{2.5}$$

By using equation 2.5 we can obtain an estimate of the overall force between two flat surfaces. From the graph in Figure 2.5(a), the attractive force per unit area between two PDMS plates at a contact separation of 0.1 nm is ~2.4x10^5 N/cm^2 or ~23,700 atm. Even considering a larger separation (10 nm, i.e. 100 times higher), the adhesion force per unit area is still significant (~0.25 N/cm^2).

To estimate the adhesion force involved in picking up a platelet from its donor substrate, a separation of 0.5 nm was considered and the resulting force estimated throughout the different area variations during the process (as initially plotted in Figure 2.4). Figure

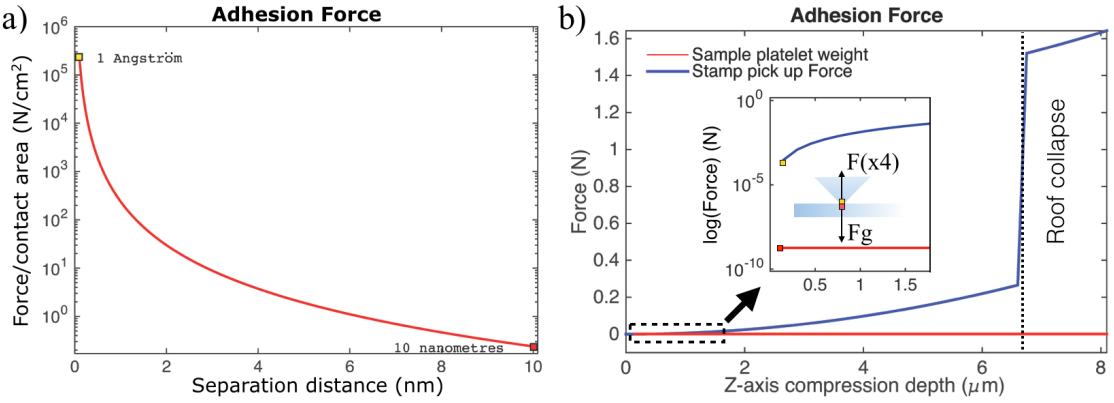


FIGURE 2.5: Adhesion force calculations: a) adhesion force *per* unit area for two flat PDMS surfaces. In b), the calculations for the force applied between two surfaces at a distance of 0.5 nm. The blue line shows the overall adhesion force during the full compression sequence. The inset shows a logarithmic scale of the highlighted area. This shows a comparison of the adhesive force exerted by the four pyramids versus the gravitational pull generated on an AlInGaN LED platelet weighing 0.185 μg.

2.5(b) shows the resulting force plot for the change in the stamp contact area. While

such calculations are subject to many uncertainties (namely fluctuations in the various Hamaker constants reported, different material interfaces, adhesion defects, etc.), the resulting values are an approximation and assume the retraction movement to be quick enough that no gap propagates throughout the stamp/membrane interface. The estimated values reveal a very strong pull from the elastomeric material contact surface, generating a force several orders of magnitude stronger than the gravitational pull on a platelet. For an LED with a volume of 100x100x3 μm^3 (see later) with the considered density of GaN of 6.15 gr/cm^3, the gravitational pull ($F_G \simeq 1.8x10^{-9}$ N) on a platelet weighing $\sim$0.185 μg is plotted as a red-line in Figure 2.4(b). This shows that the forces involved with barely any preload from the stages - where only the four pyramid tips are in actual contact - are significantly higher than gravitational effects. This demonstrates the high adhesive capability an elastomeric stamp can display when quick-retraction is employed to lift devices from their donor substrates and, furthermore, how during transport the tip-only support-configuration can be used to transfer devices between substrates. In essence, this is also the intended configuration for printing the devices onto a new substrate as any contact area on the bottom device/substrate interface is bound to be sufficient - and more effective than gravity - to overcome the force generated by the pyramid contact area on the top device/stamp interface.

2.1.1 Microstructured elastomeric stamps

A determinant of the final geometry of the protruding pyramids on the stamps are the facet angles generated by the wet etching of silicon. Silicon (100) wafers were used with exposed (100) planes. These are known not to etch vertically when exposing non-etching (111) planes. The crystalline structure of silicon and the way the different planes form when specific etchants are used results in features with an angle of 54.7° (see full details in section 2.2.7 relating the angles between planes). The elastomeric stamp pyramids made use of this peculiarity of silicon wet etching and were created by moulding techniques.

The full process of PDMS stamp fabrication is described in Figure 2.6. The process is begun with SiO_2 masking and patterning of Si (100) wafers with the features precisely aligned to expose the correct crystallographic planes. Once the SiO_2 is etched through (Figure 2.6(a)), Si (100) planes are exposed and wet etched using an alkaline Potassium Hydroxide (KOH) solution which creates pyramidal intrusions on the wafer as shown in Figure 2.6(b) (full etching details and mechanism are described in section 2.2.7). After the etching is complete, the wafer is coated with a thick photoresist (SU-8) to build the main enclosure for the body of the stamp. SU-8 is widely known in the microfabrication industry for being capable of producing high aspect-ratio features (for thicknesses $>$ 100 μm) which makes it ideal for this purpose. After resist development the opened

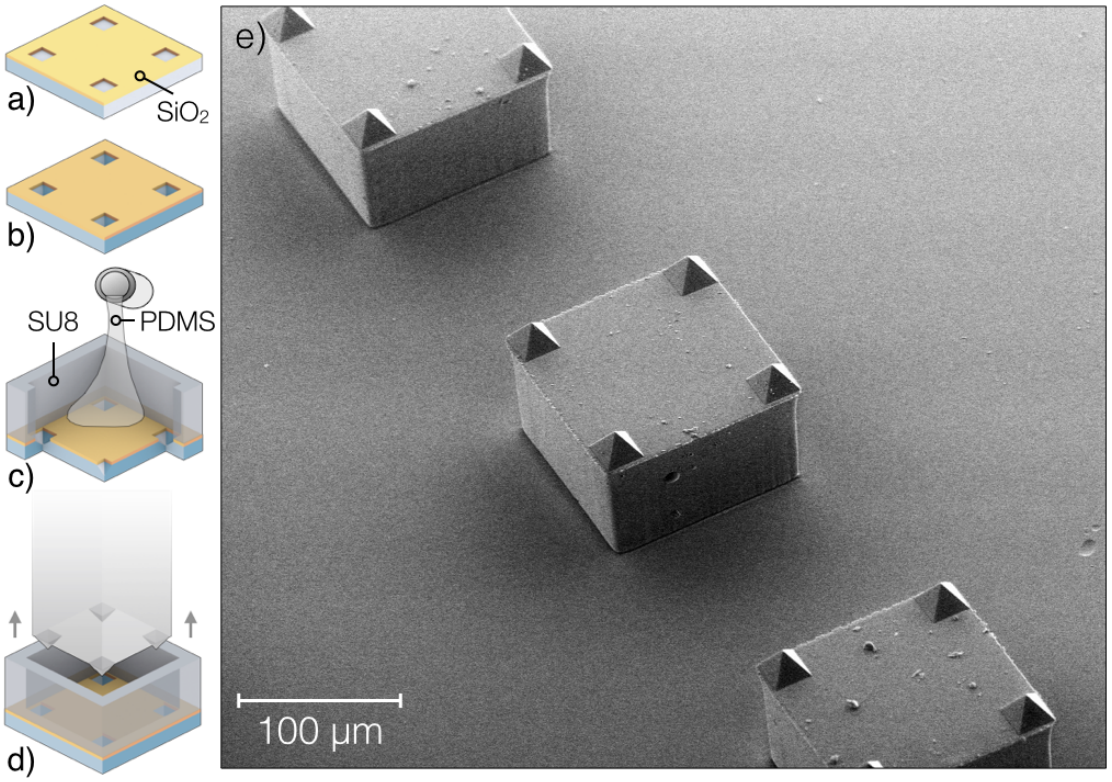


FIGURE 2.6: The micromoulding process for elastomeric stamp fabrication: a) shows the patterning of the Si wafer, b) shows the wafer after etch with completed pyramids, c) shows a cross section of a hardened SU-8 mould with liquid PDMS being poured. In d) the completed stamp is removed from its reusable mould and e) shows an SEM image of the finalised stamps after removal.

features are used as a mould/enclosure for the pouring of the liquid elastomer and curing agent. For elastomeric stamps, as previously mentioned, the material of choice is PDMS, a silicone-based material which was used in soft-lithography processes. PDMS belongs to the group of polymeric compounds commonly referred to as silicones and is optically clear, inert and non-toxic. Its widely used in the production of contact lenses due to its soft conforming and deformable nature. The base material is mixed with its curing agent typically in a weight ratio of 10:1, and after thermal annealing it can be removed from its mould as a solid viscoelastic material. PDMS molecules have extremely flexible polymer chains due to multiple repetitions of the siloxane linkages. Long entangled polymeric chains with an elevated molecular weight confer PDMS its unusually high level of viscoelasticity. PDMS can be used in its liquid state (when the n^{th} repetitions of the siloxane links are small) or combined with a curing agent (which binds to the molecules and increases the polymer backbone, i.e. elevated n^{th} repetitions). Both materials are typically obtained in a liquid state before curing and, therefore, elastomeric stamps can be designed and moulded to fit precisely the overall size of the device to be printed. However, smaller stamps can be made with outer dimensions inferior to the structures being transported with little to no significant change in their adhesion properties. This

expedient aids visibility when attempting to precisely transport small features or during high density (close-proximity) device placement.

2.1.2 Anchors test

The design of the anchors have to be in line with the design of the stamps. While the stamps have to be able to carry the LEDs among the different substrates, anchors have to be able to suspend and fracture when required. Precise engineer of their dimensions and location is critical to ensure a reliable anchor able to retain the LED in place during the entire microfabrication process, fracturing only during quick-retraction of the elastomeric stamp. Different attempted configurations for anchor design were tested and these can be seen in Figure 2.7. Rectangular anchors with different widths (10,15 and 20 μm) are

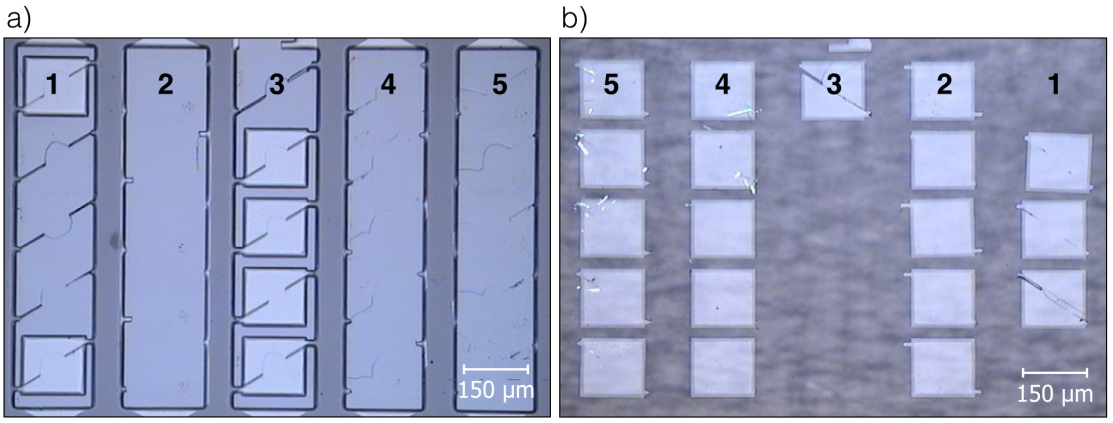


FIGURE 2.7: Geometry and size test for different anchors configuration. a) shows test platelets left on the wafer, b) shows platelets transferred by contact-printing onto a slab of PDMS. The different configurations studied were: 1: 10 μm lateral size, 2: 15 μm lateral size, 3: 20 μm lateral size, 4: triangle-in configuration, 5: triangle-out configuration.

shown in Figure 2.7(a) - 1,2 and 3 respectively. The smaller 10 μ anchors can be used but some of the devices are not released from their growth substrate. For the three attempted sizes, the best performing was the one with anchors 10 μm wide. The anchor design was seen to influence the underetching speed. The inclusion of an disruptive feature (anchor) on the anisotropic etching of Si for perfectly aligned features can affect the etch speed and expose undesired slow-underetching planes. In the case of anchor design number 2, this was the size that didn't exposed slow-etching planes, thus aiding the underetch progress.

For different geometry, triangle-shaped anchors were designed as to facilitate fracturing of these during transfer-printing. The use of a triangle allows the concentration of high mechanical-stress in a specific region (the triangle tip) when these are compressed by the elastomeric stamp. This has been demonstrated with two successful transfers (with 100

% yield) for configurations where the triangle tip is facing the platelet (4: triangle-in) as seen in Figure 2.7(a) and for triangle tips facing the column support (5: triangle-out).

A significant result with the triangle-in configuration (4) was the point of fracture to occur at the platelet sidewall. This yielded a clean fracture of the platelet while disposing of the anchor which has no operational value. The opposite was observed for the triangle-out configuration (5) where the anchors were transferred with the platelets themselves. This shows that for high-density placements of materials and/or optoelectronic devices, anchor configurations and geometry plays a significant role on the minimum spacing that can be achieved.

2.2 Fabrication of AlInGaN-based LEDs for Transfer Printing applications

2.2.1 Fabrication of ultra-thin suspended LED membranes

The creation of releasable suspended LEDs requires carefull consideration and precise engineering. The strucures being transported have somehow to be released from their growth substrate so these can be moved and assembled onto a new receiving substrate. An example of arrays of suspended AlInGaN LEDs with 50, 100 and 150 μm lateral size are shown in Figure 2.8(a,b,c). SEM imaging of a finalised suspended device ready to be transfer printed is shown in Figure 2.8(d) which clearly shows the underlying silicon substrate. The devices themselves can be seen suspended in air through a pair of sacrificial anchors devised to aid the release of the devices. The spacing of the devices has to match precisely each elastomeric stamp (Figure 2.8) so that only the desired pixels are selected for transporting to their corresponding position. The main techniques used to produce the suspended LEDs are hereafter described and the two major fabricated LED architectures are described at the beginning of Chapters 3 and 4, respectively. First, however, the main techniques used to fabricate all the elements composing a typical Transfer-Printing setup are briefly introduced.

2.2.2 Photolithography

Photolithography is the technique of choice in the semiconductor industry for pattern definition. It relies on the exposure of photosensitive materials (also known as photoresists (PR)) via lithography masks containing computer-aided patterns which. After development the resulting resist structures can be used as etching masks [81]. The exposure of the PR to UV light changes its solubility, becoming highly reactive to the corresponding

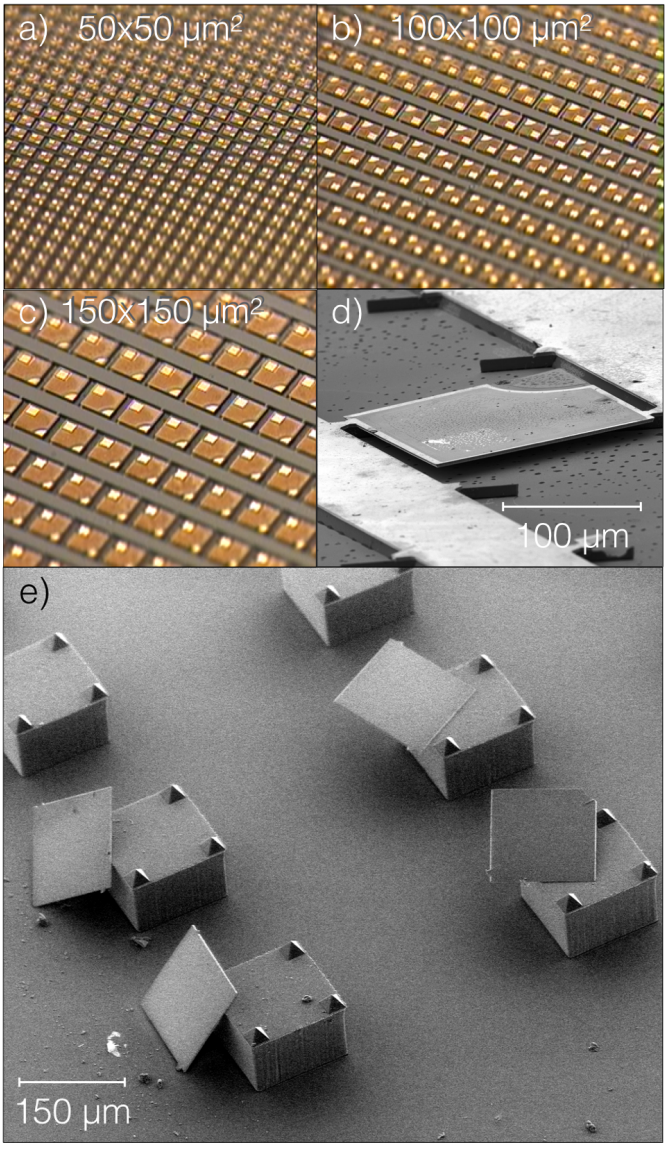


FIGURE 2.8: Suspended micron-size LEDs with different lateral sizes on their growth substrates and ready for transfer (a-c). In (d), a close-up SEM image of an LED suspended in air by two sacrificial anchors and in (e), an array of elastomeric stamps are shown along with some LED membranes.

developer once exposed. After serving its purpose, the PR can be removed and the next patterning step can take place. A simple representation of a photolithography system can be seen in Figure 2.9 where the main features are illustrated. A high-pressure short-arc mercury lamp is used as an ultra-violet light source and for the system used, where the wavelengths of interest range from 365 nm to 436 nm (Hg UV400-type). Optical elements collimate the beam ensuring an even optical power density distribution in the exposed area of the mask. Translation stages are used to adjust x,y,z positioning and also rotation. The precise alignment of the sequential exposures is critical to ensure the best development. A gap (>15 μm) between the mask and the samples has to exist to allow free movement underneath the exposing pattern (also known as proximity lithography).

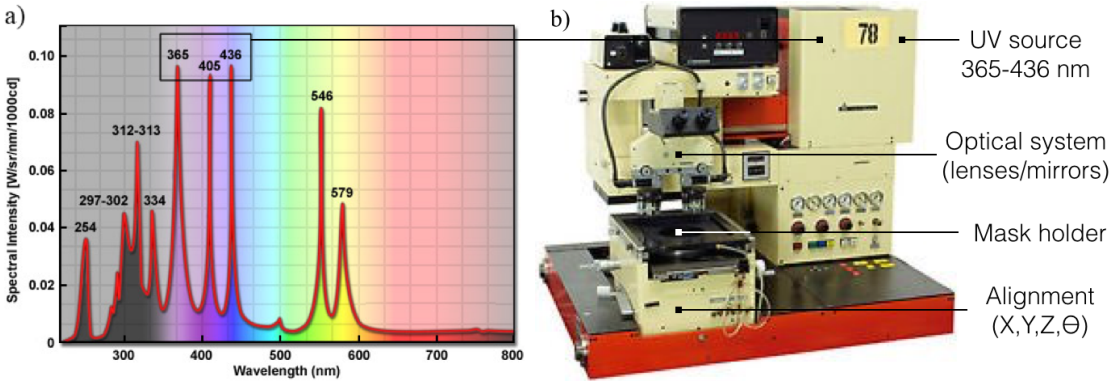


FIGURE 2.9: Typical spectra of a high pressure mercury vapour arc-discharge lamp (From [82]). In (b) the main elements composing a typical photolithography system are shown for a Karl Suss MA6 mask aligner. UV light is guided through an optical system to illuminate a mask containing both transparent and opaque areas. Depending on the type of photosensitive resist, the final pattern will be a replica of the mask or its negative.

After careful alignment and positioning, *pattern capture* occurs and contact between samples and mask is achieved to ensure the highest resolution possible on pattern transfer. The exposure of the pattern is initiated and parameters such as dosage, time and exposure gap are determined by the photosensitive material properties and thickness. The same goes for the development of the photoresist pattern. A PR-specific developer is used and depending on the material characteristics, the developer dilution and the exposure time can be altered to specific thicknesses or sidewall shaping.

Photolithography is therefore a very useful tool to define patterns on surfaces but in itself cannot be used to make those patterns permanent. To do this, multiple etching methods (both wet and dry) described hereafter can be used to engrave these patterns permanently in the processed materials [81].

2.2.3 Reactive Ion Etching - RIE

Plasma etching is usually associated with the production of vertical sidewalls due to the anisotropic nature of the etch and the directionality of the bombarding ions towards the material surface being etched. This type of etching has been widely used in the semiconductor industry and has been fine-tuned to etch high-precision and high aspect ratio features produced by photoresist-lithography patterning [81]. Plasma etching requires the use of reactive gases excited by radio-requency electromagnetic fields (RF) (typically 13.56 MHz) inside a vacuum chamber. The RF-fields generate highly-reactive ionic species from those gases that are guided to the surface. At the surface, a combination of both chemical (due to the elements reacting) and physical (due to the kinetics of ion bombardment) reactions occur. In a plasma, both ions and excited neutrals are

generated and used for etching. Ion bombardment tends to induce directionality to the etch while chemical bonds from the exposed material are broken by the chemical reaction of the ions. Some materials (such as Aluminium, Silicon, etc.) inherently possess a thin oxide layer on their surface. Before the etching process is initiated, this layer has to be removed since it may inhibit an expectable and predictable etch rate. To remove these thin native oxide layers, ion bombardment becomes crucial to expose the underlying materials being etched [81].

In Figure 2.10(a), a typical Reactive Ion Etching (RIE) chamber is represented where the areas labelled (1) and (2) represent the two electrodes that create the internal electric field (3) that will separate the different plasma species. With gas filling the chamber, ions are generated by the plasma both positively and negatively-charged (4) and in equal quantities. The ions are then accelerated towards the bottom electrode (and

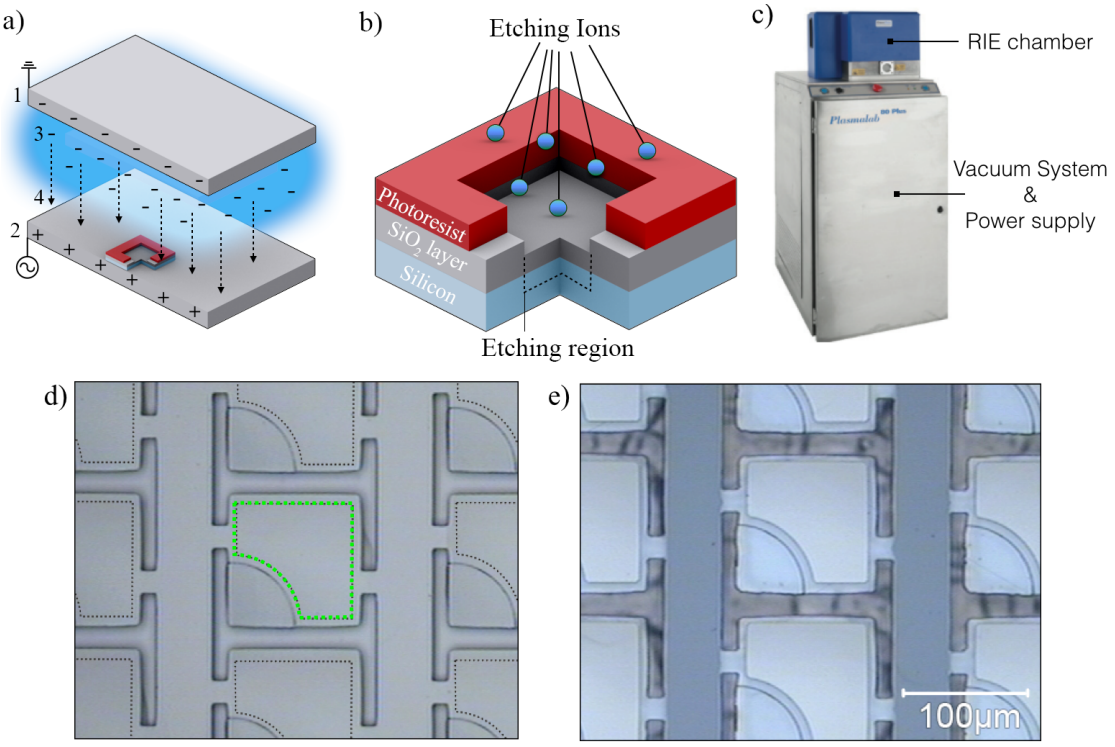


FIGURE 2.10: Schematic diagram of the main components of a Reactive Ion Etch chamber. In a) gases flow through the shower head on the top electrode (1) and the wafer is placed on the powered bottom electrode (2). The generated ions (3) hit the sample (4) and etch the exposed surfaces. In b) an example of how photoresist helps protect surfaces from the etching ions. The RIE system used (Oxford Systems Plasmalab 80 plus) is shown in c). A set of optical images of a batch of LED devices before (d) and after (e) RIE which were used to etch metal on undesired areas. As an example, the green dashed lines in d) exemplify the area protected on every pixel by a layer of PR.

corresponding sample surface) where the etching takes place. In Figure 2.10(b), the etch progress is illustrated at the sample level. A photoresist-patterned silicon oxide (SiO_2) layer on top of silicon is exposed to bombarded etching ions. The accelerated ions etch

down the oxide layer where they recombine with the SiO_2 and are dispersed. The electric field within the chamber ensures the directionality of the etch and an anisotropic etch is predominant with generated free radicals - which can cause etching in multiple directions - being highly suppressed. Etch rates can be adjusted through careful control of the bias power, gas flow, chamber pressure and temperature [81]. A pertinent example of RIE usage can be seen in Figure 2.10(c) based on LEDs being processed for transfer printing. RIE is here used to pattern a metal layer using a SiO_2 hard mask on top. A photoresist pattern is photolithographically defined (Figure 2.10(d) - dotted area) and developed. To etch the SiO_2 layer a recipe combining 5 sccm CHF_3 and 15 sccm Ar as etching gases, with 200 W of RF power at 0.03 Torr was used with an overall etch rate of 39 nm/min. Figure 2.10(e) shows the resulting metal layer after the photoresist is removed and the sample cleaned.

2.2.4 Inductively-Coupled Plasma (ICP) dry etching

An inductively-coupled plasma (ICP) dry etching system is a modified RIE system with the addition of a radial coil arrangement surrounding the plasma chamber. The variation in the coil's electric field generates varying magnetic fields by induction, allowing the creation of higher-density plasmas which results in higher etching rates when compared with a typical RIE system. An ICP dry etch system is illustrated in Figure 2.11 and the physical and chemical etching mechanisms are the same as for RIE. The etch rates achieved are, however, usually an order of magnitude higher than RIE systems and can be equally controlled by changing the coil power - and hence the magnetic field, gas flows, chamber pressure and the platen power [81]. In Figure 2.11b), a square AlInGaN LED material-based platelet array is shown before loading into an ICP chamber. Photolithography is used to cover all the patterning area except corners where quarter-circles where etched. This is a typical operation to etch down through the set of epitaxially deposited layers - p-GaN and the quantum-wells - to expose the underlying n-GaN before metal deposition. To perform this etch, a recipe combining 50 sccm of Chlorine (Cl_2) gas with a coil power of 700 W and a platen power of 300 W resulted in a etch rate of $\sim$1000 nm/min.

2.2.5 Electron Beam evaporation

The full fabrication of LEDs requires steps for adding materials, in this case with the purpose of creating metal-based connections for current to flow efficiently through the devices. These are typically used as current spreading layers and/or bonding pads to facilitate device packaging/wirebonding. An established method for metal deposition

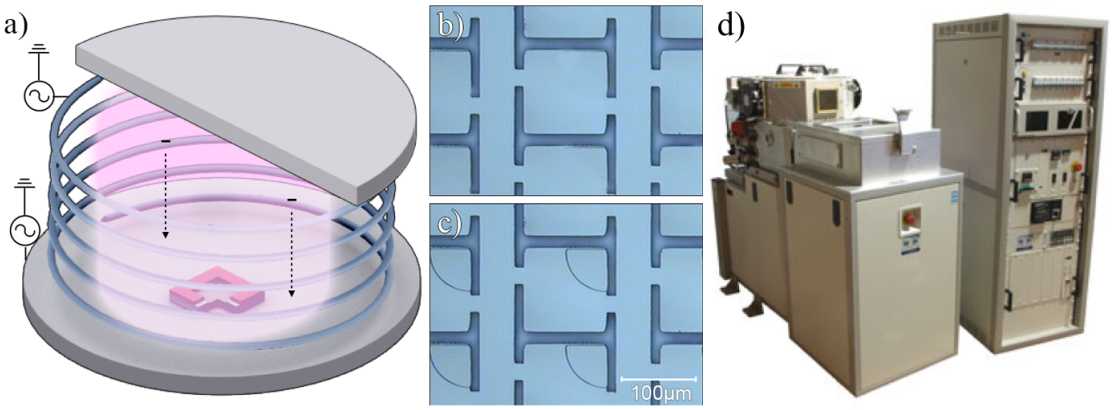


FIGURE 2.11: Schematic diagram of the main components in an Inductively Coupled Plasma chamber. A coil is used together with the two platens to create high-density plasma regions, achieving higher etch rates. In b,c) are photographs of a set of devices before etching with ICP (top) and after (bottom). As an example, the quarter of a circle depicted in c) was the only area not protected by layer of PR and thus is being etched. The ICP system shown in d) (STS ICP etcher) was used to etch through the epilayers, exposing the n-GaN.

is through an electron-beam (e-beam). A schematic of an e-beam chamber for physical vapour deposition of metals is shown in Figure 2.12a). Such e-beam systems are the tool of choice when the required temperatures for metal evaporation are too high to use conventional thermal evaporation. A tungsten filament is heated when a passing current flows through its electrodes. The heating causes thermionic emission of electrons from the filament chamber. A set of magnetic plates accelerates the beam out of the chamber and deflects it $\sim$270° where it reaches a graphite crucible containing the metal to be evaporated. When the electrons strike the metal in the crucible, their kinetic energy is transformed very rapidly into other forms (i.e. X-rays and secondary electron emissions) within the target material. The overall thermal energy produced from this collision causes the metal to heat up and the sublimated material is ejected from the crucible area to coat the samples [81].

An e-beam system requires a high pressure operating environment (below 10^{-4} Torr) since lower pressures cause significant scatter of the ejected vapour trail and in some cases failure to coat the samples. In Figures 2.12b and c), before and after optical photographs of a thin current-spreading metal deposition (total of 100 nm of palladium) can be seen. Due to the rotating substrate holder, the deposited films are slowly and sequentially deposited. This enables the precise control of the metal thickness deposited, with achievable deposition rates as low as 1 nm/minute. Depending on the final layer thickness, this process can be relatively quick (e.g. to deposit 20 nm for top-emitting LEDs) or much longer (e.g. to deposit 100 nm for *flip-chip* architecture LEDs). Typical evaporated metal films are usually under tensile stress, in the range of 100 MPa to 1 GPa [81].

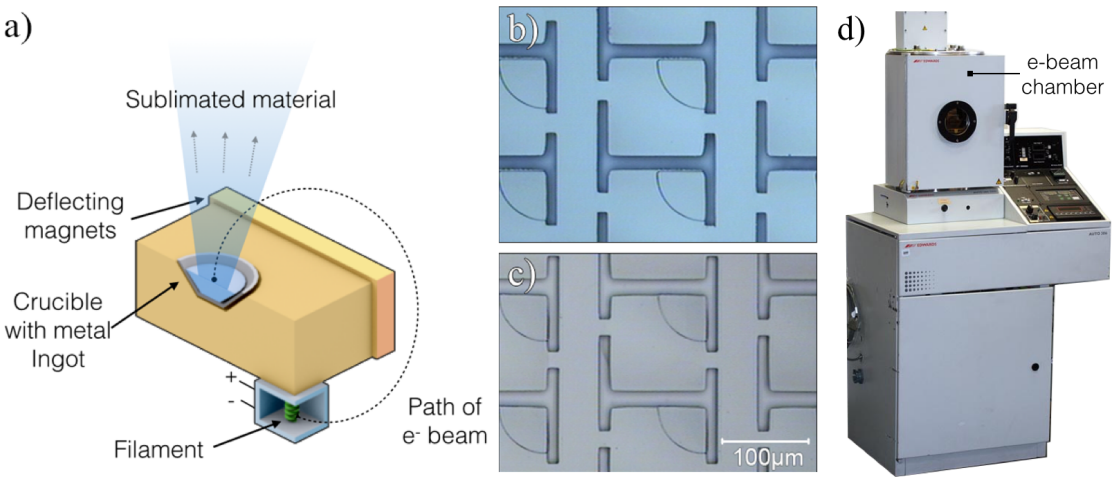


FIGURE 2.12: Schematic diagram of the main components in the chamber of an electron-beam deposition system. In a), electrons generated by a filament are accelerated and their path is deflected by a set of magnets which guide the electrons towards a carbon crucible containing metal. The sublimation of the material causes it to eject vertically, coating the samples on top. In b) and c) are shown images of a set of devices before (top) and after (bottom) e-beam metal deposition. In d), the used Edwards e-beam metal deposition system used is pictured.

2.2.6 Metal Sputtering

For the deposition of thick bonding pads, metal sputtering is the technique of choice. This is one of the most important physical vapour deposition (PVD) tools available. A schematic of a sputter chamber can be seen in Figure 2.13a). A high-pressure vacuum chamber (∼1 to 10 mTorr) is filled with Argon (Ar) gas. With a bias applied to the electrodes, Ar^+ ions from the generated plasma will strike the negative-biased electrode. This electrode (cathode) contains the metals being evaporated. Upon collision, the accelerated ions will interact with the target and slow down. As a result of these collisions, atoms from the target are ejected upwards where the samples are located - just beneath the top electrode (anode) [81]. Sputtered atoms will experience many collisions until they reach the samples. The ejected particles have to successfully travel through the plasma created to eject them. The thermalisation of these high-energy particles will reduce their energy and temperature, reducing the overall deposition rate on the samples. This provides both accurate thickness control and prevents high-energy and excessively high-temperature particles from reaching the samples, causing defective depositions and/or material damage [81]. In Figure 2.13b) and c) is the result from a sequential sputter metal deposition of 50 nm of Titanium (Ti) followed by 200 nm of Gold (Au). For the Ti, a DC current of 6 A was applied for 3 minutes while for the Au, a 4 A current was applied for 2 minutes. This results in deposition rates of 17 nm/min and 85 nm/min, respectively.

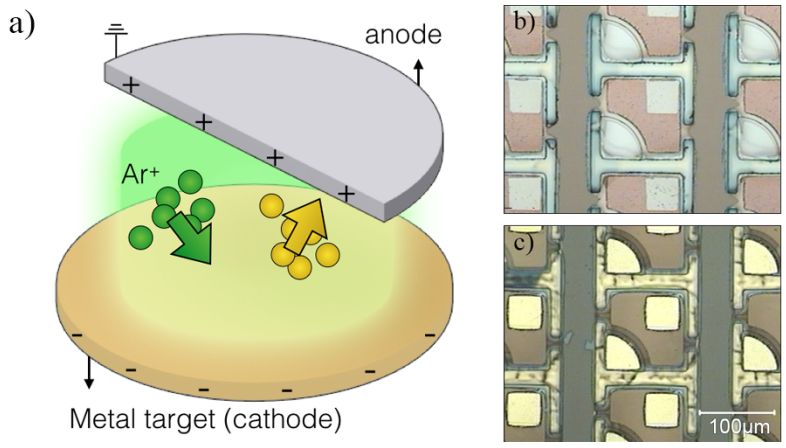


FIGURE 2.13: Schematic diagram of the main components in a metal sputtering system chamber. A pair of electrodes (one containing the metal being deposited) generate Ar^+ ions that bombard the metal target, *sputtering* metal atoms towards the samples being held on the top. In b,c) are shown photographs of a set of devices where thick metal pads were deposited (yellow squares and quarter of a circle in c) on the LEDs' electrodes.

While evaporated metals are usually subject to tensile stress, sputtered films once deposited can be under tensile or compressive stress. The ionic bombardment during deposition has a severe effect on many of the thin film properties [81]. The technique itself is a more complex process than evaporation and stress tailoring for thick films can be achieved by performing changes to the bias power, argon gas pressure injected in the chamber, sputtering gas mass during the process and the processing temperature [81].

2.2.7 Wet etching and underetching

Wet etching methods are typically faster than dry etching methods, albeit with less controllable etch rates. While dry methods are useful to ensure the isotropy of the etching progress (usually with vertical profile sidewalls), wet methods are known for their anisotropic effects such as with specially-oriented Si wafer planes as will be demonstrated in this section. Silicon has the diamond cubic crystal structure and the main crystallographic directions relevant to this work are shown in Figure 2.14 along with their corresponding perpendicular crystal planes. The most important parameter in the orientation-dependent etching of Silicon is the atomic packing and available bonds in the crystal plane [83]. The low-index planes - (100), (110), (111) - and their position in the crystal lattice are represented in Figure 2.14. The crystallographic directions of each plane allow a clear representation of the atomic lattice packing as seen along these directions. The three directions present a very distinct surface morphology. Due to Si's four-fold symmetry, (111) planes are at equal distances to the (100) planes and at 90° to each other. These planes intersect the (100) planes at an angle of 54.74°. Si

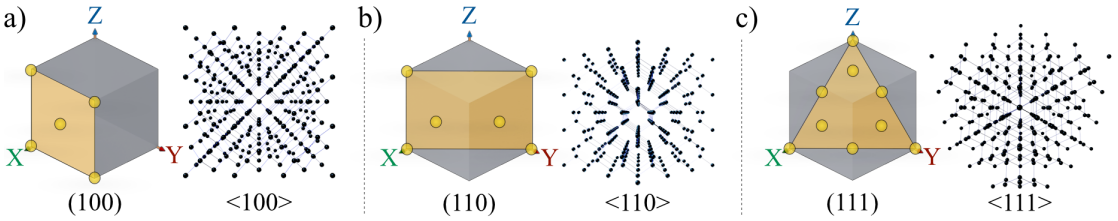


FIGURE 2.14: Silicon crystal atomic planes (3D cube) and crystallographic directions (atomic lattice) for a)(100), b)(110) and c)(111) low-index planes, respectively. The highlighted atoms are those composing the highlighted plane.

wafer orientations are labelled according to the plane normal to the wafer surface. When specially-oriented Si (100) wafers are masked with flat-aligned parallel or perpendicular patterns - in this case, in relation with the (110) planes - the etch proceeds down until (111) planes are exposed and then stops (or no significant etch in comparison with other planes is observed) [83].

The highest observed atomic packing density is observed for the $\langle 111 \rangle$ direction, with the $\langle 110 \rangle$ direction showing less dense packing. One could therefore infer the etch rate to be considerably faster in the $\langle 110 \rangle$ direction when compared to both $\langle 100 \rangle$ and $\langle 111 \rangle$ directions. This is due to the number of dangling bonds and back bonds of the silicon atoms comprising the surfaces of the planes. For the (100) unit-plane, the atom in the centre of the face has two dangling bonds and two back-bonds. The (110) planes have three dangling bonds and three back bonds (two of which are exposed) that can react. This means that any surrounding atoms with a high-enough atomic number bonding with these dangling bonds will polarise the Si atom while weakening the back bonds, resulting in an elevated etch rate. The same is not observed for Si (111) planes where only 1 dangling bond exists and is supported by three non-exposed back bonds. The three back bonds are below the plane surface and engage with neighbouring atoms, creating a tight atomic bond that results in a much slower etch rate. This means that for anisotropic etching, the number of dangling bonds plays a crucial role in the etch rates of the different planes [84, 85]. At the atomic level, the removal of the exposed atoms on the Si surface is a complex process that can involve both chemical and electrochemical processes. When Si wafers are prepared throughout processing, the native oxide is typically removed to ensure stable and predictable etch-rates. The removal of this oxide (usually a few nanometres thick) leaves the Silicon surface Hydrogen-terminated [86] as illustrated in Figure 2.15(a).

The molecular model in Figure 2.15 shows how the alkaline chemical etch attacks exposed Si atoms through sequential oxidation and etching reactions. The rate at which the etch progresses occurs at two etch-limiting speeds: a slow oxidation step (Figure 2.15a)) of hydrogen-terminated sites and a fast etching of hydroxyl-terminated silicon

(Figure 2.15b)). Oxidation (Figure 2.15a)) occurs when hydrogen-terminated (H-) sites are oxidised resulting in hydroxyl-terminated (OH-) silicon. This is due to the higher difference of electronegativity of Oxygen atoms (3.44 in the Pauling scale) when compared to Silicon atoms (1.90). Hydrogen itself has a higher electronegativity number (2.20)

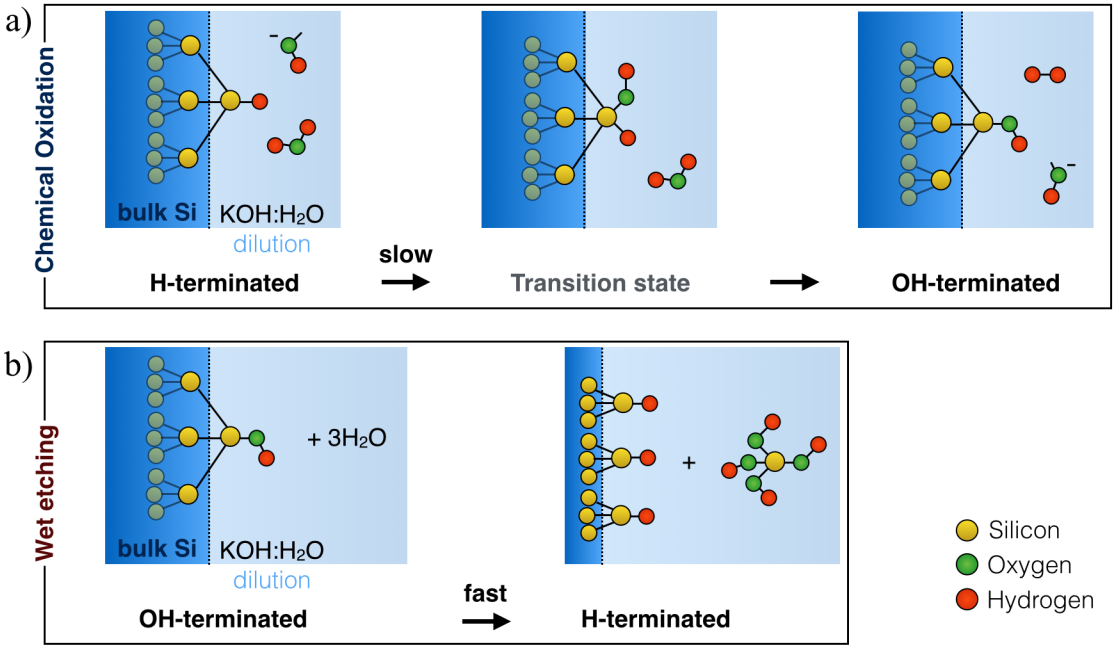


FIGURE 2.15: Diagram of the etching of Silicon in alkaline solutions. In a) is shown the first oxidation step for a H-terminated Si atom. The following transition state is considered to be the etch-rate-limiting (slow reaction). The reaction results in the silicon atom being terminated with an hydroxyl ion (OH^-). The final step of the reaction (b) results in the dissolution of $Si(OH)_x$ and reveals newly exposed silicon atoms which are hydrogen-terminated. Adapted from [87].

than Si and is quite effective at filling in incomplete surface bonds of silicon atoms. The removal of the Si atom (as a $Si(OH)_4$ byproduct) occurs due to the electronegativity difference that polarises the exposed atom with an exposed bond and weakens the surrounding backbonds of the Si atom [86–90].

Silicon (111) planes etch the slowest compared to all orientations and represents an absolute minimum in the etch rate function of Silicon [83, 91]. Silicon (100) and (110) are therefore faster etching planes that will etch until Si (111) planes are exposed. Depending on the etching solution parameters, the etch rates for these two planes are one to two orders of magnitude faster than that of Si (111) planes [92]. Depending on the different angles and exposed planes, the use of orientation-dependent etch solutions can be used to exploit different geometries (other than simple planar) and complex structures. For this work, Si (100) and (111) specially orientated wafers were used to produce some of the structures needed for transfer-printing. Si (100) wafers, were used to create the pyramidal recesses as part of a mould (as described in section 2.1.1). To expose the (100) planes to the etch solution, vertical features on the mask were aligned with the

TABLE 2.1: Silicon orientation-dependent etch rates using KOH solutions (34wt.%, 70°C,[92])

Orientation	Etch rate (μm/min)
100	0.629
110	1.292
111	0.009

$\langle 110 \rangle$ direction and masked using a hard SiO_2 layer. The etch progresses normal to the exposed surface as illustrated in Figure 2.16(a). The masked features will slowly close on themselves during the progress of the etching as new (111) planes are exposed. The etching of features on this type of wafer is usually safe from overetching as this is considered a self-stopping etch. For perfectly squared patterns (here intended for this work), the final recess geometry will resemble a pyramid where the angles between the surface planes and the recessed sidewalls is 54.7°. The overall angle between two planes can be obtained using the planes' angle equation:

$$A.B = |A||B|cos(\Theta) \tag{2.6}$$

As an example here, the angle between (111) planes and (100) can be obtained using equation 2.7:

$$arccos\left(\frac{(111).(100)}{|(111)|x|(100)|}\right) = 54.74^{\circ} \tag{2.7}$$

This equation can be then used to calculate the angles between the three main planes of interest for the produced features: (100), (110) and (111). The angles between these planes are represented in Table 2.2

TABLE 2.2: Calculated angles between planes in degrees for the first Miller indices.

Planes	**(100)**	**(110)**
(100)	-	45.0
(011)	90.0	60.0
(111)	54.7	35.5

For the underetching procedure in this work, Si (111) wafers were used. The high anisotropy presented during the exposure to KOH wet etch is ideal to fabricate suspended releasable material layers. It simplifies the fabrication and allows an elevated density of devices otherwise unobtainable if this the etch were to be isotropic in nature. The approach taken requires a deep RIE etch to expose a significant portion of the underlying material (several times larger than the epistructure thickness). This aids the etch progress by exposing a larger material surface as well as aiding the etch solution circulating underneath the suspended layers. Quite opposite to the Si (100) surfaces if exposed to KOH, as the etch progresses normal to the (110) planes, the exposed (111) planes will

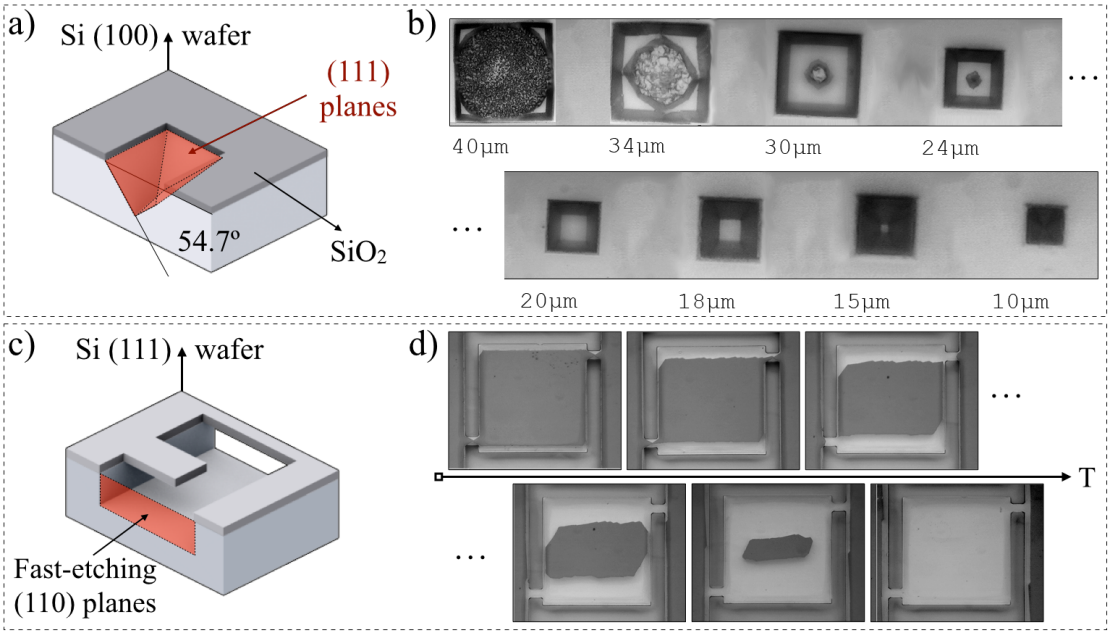


FIGURE 2.16: Wet etch of Si (100) and (111) wafers in a KOH solution. For (100) wafers (a), the etch creates pyramidal features recessed on the substrates. The etch progression can be seen in b) for squared masks of different lateral size. For Si (111) wafers as illustrated in c), the wet etch progresses along the fast etching (110) planes. The underetch progression for a 150x150μm^2 platelet is shown in d).

guide the etch and prevent further downward and lateral etching. Once the underetch is complete, the new parallel (111) surface underneath the suspended epilayers can be considered as nearly atomically flat and virtually with the same etch rate [93].

Significantly, on underetching the backside of the devices remains smooth, as illustrated by Figure 2.17(b,c). Atomic force microscopy over 40 x 40 μm^2 areas indicated a typical 0.8 nm averaged root mean square roughness, approaching closely to the resolution limit of the system used. The well-known polarity-specific etch behaviour of KOH and similar solutions would normally be expected to have produced a rough surface, featuring hexagonal micropyramidal protrusions, on direct contact with the III-nitride epilayers [94, 95]. GaN surface chemistry defines how the etching affects the surface parameters with different polarities. Ga-polar and N-polar crystals have different bonding states at their surfaces [96]. The etching mechanism of N-polar GaN in KOH baths involves the adsorption of hydroxide ions (OH^-) by the surface reacting with the Ga atoms. The opposite reaction is observed on Ga-polar GaN with OH^- ions being repulsed since the three available dangling bonds are nitrogen-filled thus preventing the hydroxide ions from interacting with the Ga atoms [97]. The full chemistry and physics of the etching mechanism has been reported and described elsewhere [96, 97].

To explain the observation of the smooth under surface, it is reasonable to infer, however, that a thin interfacial SiN_x layer [98] formed during the MOCVD process provides

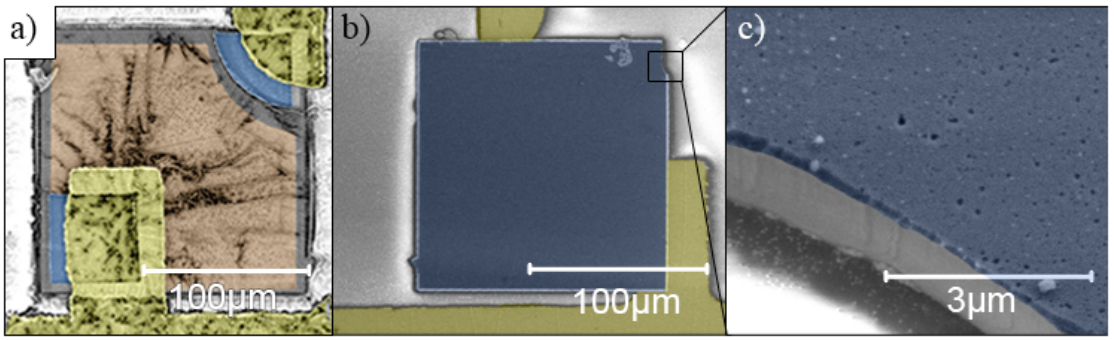


FIGURE 2.17: Colourised scanning electron microscope images: a) top view of a single pixel, yellow areas represent the deposited metal tracks, beige areas the current spreading layer and blue areas correspond to the P and N electrodes; b) image of the backside (i.e. n-side) of an LED in a finished device, grey here represents the buffer layer that interfaces with the Si wafer; (c) detail of the indentation at the upper right corner, resulting from breakage of an anchor, and giving a fracture section through epilayers not exposed to the KOH etch. This higher magnification oblique view shows the overall smoothness of the back surface, and the curved fracture edge.

advantageous protection of the III-nitride material from the wet etching. This layer occurs due to the natural diffusion of nitrogen atoms into the silicon substrate during growth [98, 99]. The etching of this layer by the KOH solution is not measurable here as the etch rate of silicon nitride is below 1 nm per hour [100] a feature that makes SiN_x layers a widely used KOH-resistant hard-mask in industry.

2.2.8 Rigid and flexible substrates

Due to the versatility of the TP technique, LEDs can in principle be printed onto a wide variety of substrates. Throughout the entire process, compatibility between the LED spacing during fabrication, the stamp positioning and the deposition areas is crucial, especially if multiple devices per pick-up are simultaneously transferred from their donor substrate to the receiving substrate. While the device spacing is defined during mask design, this is not so visible during fabrication and assembly. Having alignment marks on the receiving substrates therefore helps ensure accurate alignment throughout the printing process. In Figure 2.18 a dummy alignment circuit - which is a replica of the final circuit that will be used to address the LEDs - can be seen. This can be made with a simple photo-resist pattern left on the substrate before adhesion enhancement layers are deposited and can be removed later during the process if devices are operated on a membrane and peeled-of from their supporting substrate.

Figure 2.18 shows a PET film with a patterned Indium Tin Oxide (ITO) interconnecting circuit. The final ITO pattern can itself be used as both alignment and addressing circuit if no intermediate adhesion layers are used. The use of this dummy circuit is described in more detail in the following chapter.

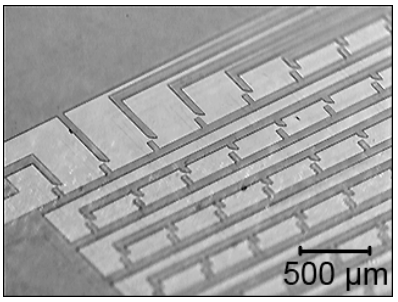


FIGURE 2.18: Dummy circuit patterning on PET substrates. The darker regions match the final interconnecting circuit.

2.3 NanoInk NLP 2000 nanolithography system

The NanoInk NLP 2000 dip-pen nanolithography system (Figure 2.19(a)) is widely used by researchers to easily and quickly create patterns on materials with features ranging from sub-μm to 10 μm in size. The easy-to-use computer interface along with pre-defined patterning setups can quickly deliver the implementation of a design or concept. This makes the system an ideal tool for quick prototyping of small features in a wide range of materials [101]. Due to the high-precision translation stages - with advertised positioning accuracies of $\pm$25 nm - this system was judged to offer improved accuracy for the transfer printing of thin-film semiconductor structures, without sacrificing fabrication throughput or scalability. The precise positioning capabilities offer a significant area scaling for TP and can print devices in a printing area up to 10x10 cm^2. To achieve this area, precise translation XYZ translation stages can be used with tip and tilt increments as shown in Figure 2.19(b). The system's microscope features an optical resolution below to 1 μm with motorised digitally controlled zoom and focus (all the available imaging options are shown in Figure 2.19(c)). Environmental control of the atmosphere during processing is also available within the software as well as programing options to automate the assembly of the devices (top icons in Figure 2.19(b)). The precise control of the stages and the embedded imaging system are therefore critical characteristics to ensure the optimal positioning of structures onto new substrates. Extensive options with the computer-aided design software allows step-by-step control and automation [101]. A full description of the system and its capabilities have been included as an Appendix.

2.3.1 Custom adaptations of the NLP 2000 for Transfer-Printing

The NLP 2000 system as supplied commercially uses a set of individual or arrayed probes made of Silicon Nitride (SiN_x) that are similar to the cantilever-shaped tips used by typical atomic force microscopes [101]. These tips can be wetted in matched liquid reservoirs where, upon retraction, existing surface tension at the tip (within a

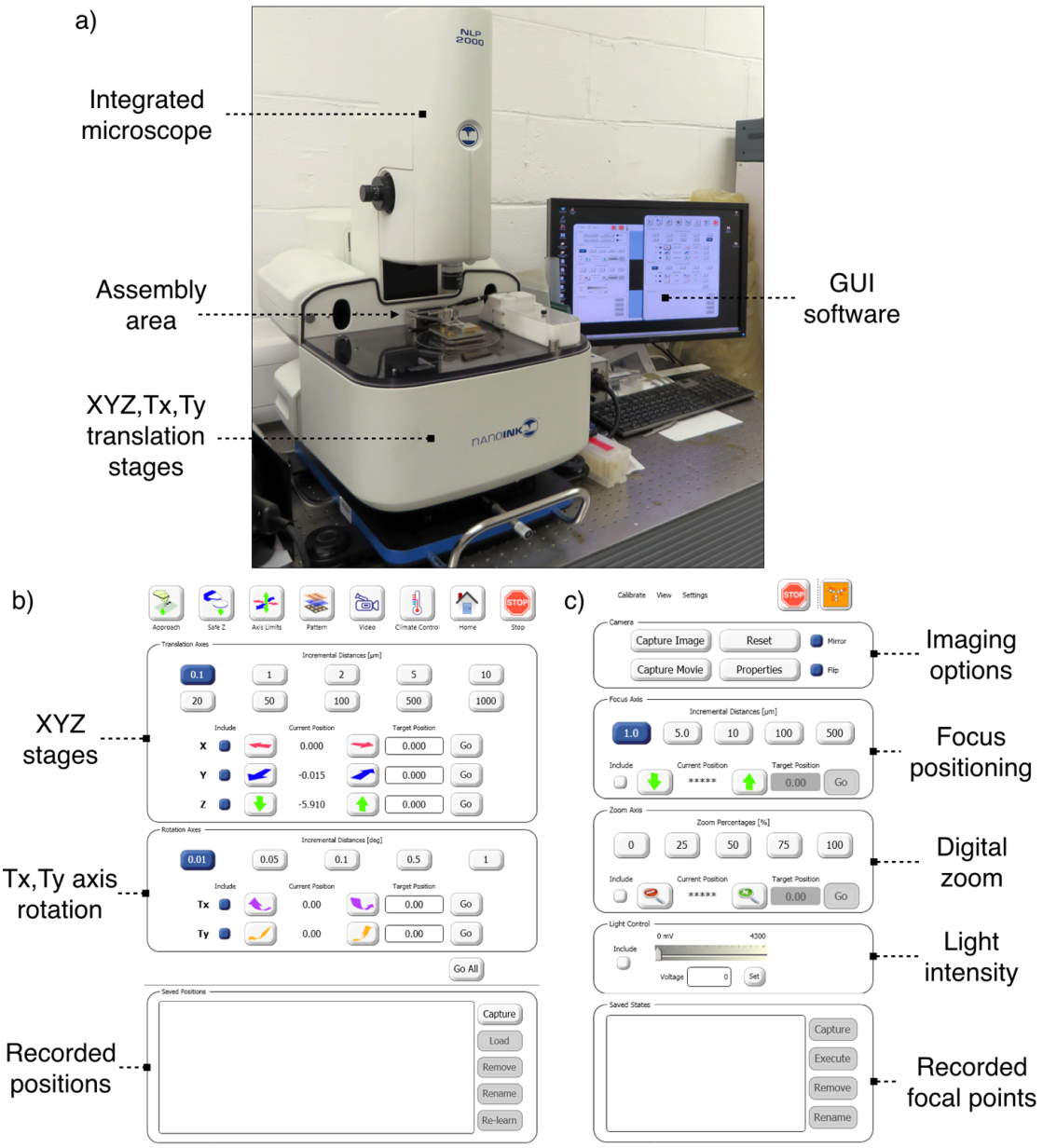


FIGURE 2.19: Nanoink NLP 2000 nanolithography system main components shown in a). In b) the graphical user interface to control of the translation stages is shown and in c) the available imaging options that control the integrated microscope are shown.

limited range of viscosity) condenses the liquid droplets at the tip extremities. The translation stages are moved to place the tips in contact with the target substrates and the inking/printing patterning process takes place by simple physical contact between tip and substrate. Figure 2.20(a) shows an array of tips being wetted in microfluidic wells with black ink. In Figure 2.20(b), a representation of the bottom of the tips is shown, where these can be used individually or as an array. The array tips are shown in Figure 2.20(c) printing a pattern onto a substrate. The modifications made to this system to permit ultra-precision transfer-printing are shown in Figure 2.20(d) to (g).

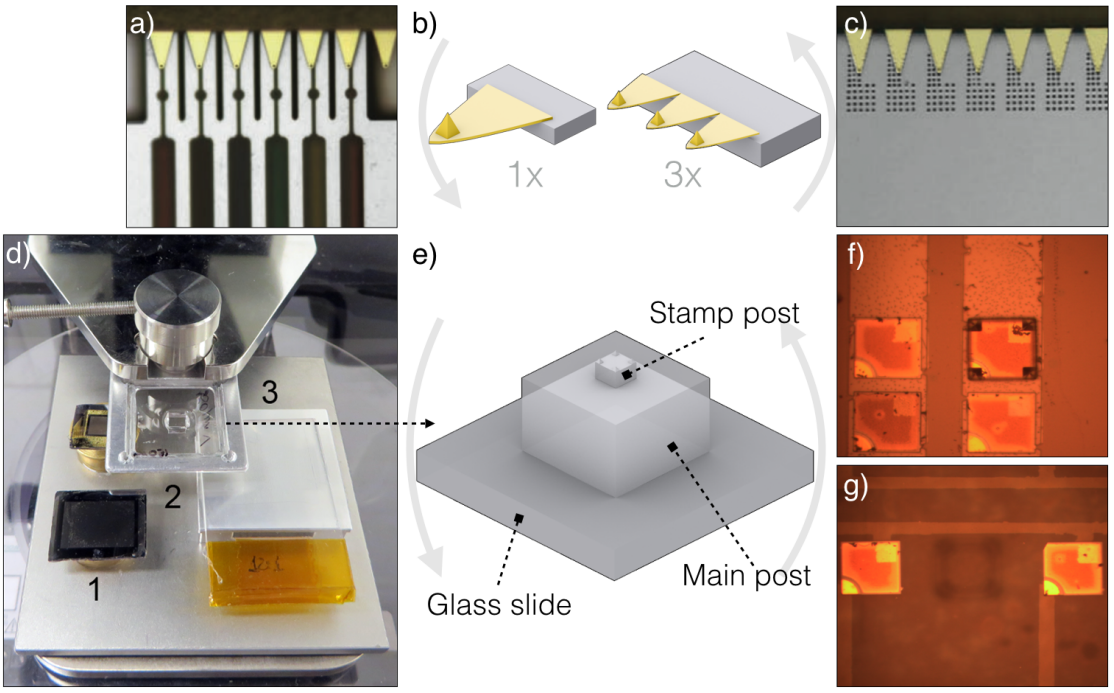


FIGURE 2.20: Nanolithography system adaptations: a) plan view of an array of as-supplied tips directly over microfluidic wells, b) a flipped representation of an individual tip and an array of tips, c) array of tips printing a pattern on a substrate. In d) the adaptations performed are shown where (1) a processed silicon wafer (donor substrate) with suspended InGaN LEDs, (2) shows the custom-made elastomeric stamp holder with an optically transparent glass slide holding the stamp, (3) a receiving substrate with an alignment circuit, e) shows a flipped schematic of the elastomeric stamp with its support glass slide. In f) the stamp can be seen picking up an LED from (1) and releasing it (g) into a receiving substrate.

The high-precision positioning capabilities and high optical microscope resolution were available as a starting platform so there was no need to build a custom-designed system from scratch. The modifications may be summarised as:

(a) replacing the standard stage by a custom stage

(b) replacing the tip holder with a stamp holder

(c) replacing the liquid reservoirs by suspended membrane LEDs

The numbered items in Figure 2.20(d) represent the the main changes to the system. A custom stage was made to accommodate the supporting stages for both donor substrates and acceptor substrates (items #1 and #3 respectively in Figure 2.20(d)). The main link between these two substrates is the elastomeric stamp holder (item #2 in Figure 2.20(d)). As seen in Figure 2.20(f,g) the system can operate at the individual level, transporting devices individually from their donor to acceptor substrates. A schematic of an individual stamp in its holder is shown flipped in Figure 2.20(e) where the stamp is shown bonded to a carrier glass slide. It is imperative that the materials used are optically transparent to

facilitate both picking up of the devices and placing them accordingly. However the main advantage of transfer-printing is the simultaneous parallel transfer of multiple devices per operation, offering high throughput device transfer and assembly. This can be seen in Figure 2.21(a) and (b) where fabricated elastomeric stamps as previously described in this chapter are shown transferring arrays of devices simultaneously. With the described

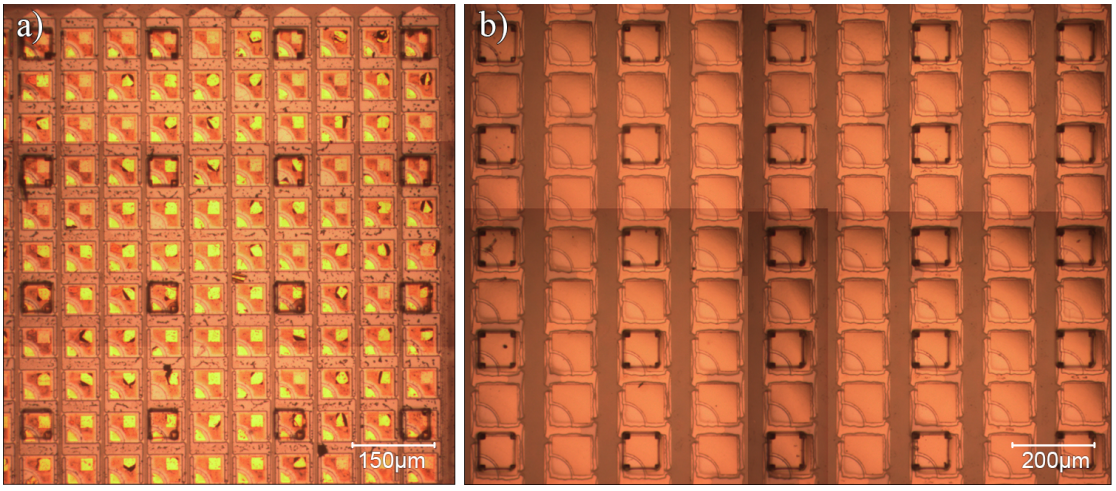


FIGURE 2.21: Composite of images showing 4x4 and 5x5 arrays of stamps picking up multiple LEDs simultaneously for parallel printing: (a) 60 μm-size LEDs and (b) 100 μm-size LEDs are shown on their donor substrates ready for being picked up by position-matched elastomeric stamps. The view in both cases is looking down vertically onto the devices and the positioning of the stamps can be clearly seen. The underlying device arrays are similar to those shown in Figure 2.8.

adaptations to the original system configuration, GaN micro-LEDs could therefore be transfer printed in a high-throughput parallel assembly. Each pick-and-place operation can be performed at around 10 seconds per placement, limited only by the operational speed of the translation stages.

In this chapter, the adaptations made to the nanolithography system used were described and the links between the different components that take part in a transfer-printing process were identified and described. The basic elements and techniques used for micofabrication have now all been presented. The full fabrication processes and sequences for the two main LED architectures investigated will be described in the beginning of Chapters 3 and 4, respectively.

Chapter 3

Transfer printing of micro-LED arrays onto mechanically flexible substrates with nanoscale accuracy

In this chapter, the capabilities of the modified NanoInk NLP 2000 system are explored and demonstrated. The system's high placement accuracy and large-area scalability enables advanced heterogeneous integration of optoelectronic devices by using multiple sets of appropriately fabricated micro/nano-structures. The high accuracy achieved represents a critical advance in order to realise high-density arrays of optoelectronic devices. No prior transfer printing research has to our knowledge specifically addressed this precision issue, and the best reported placement accuracies beforehand were ∼1 to 3 μm [68, 102], inadequate to target submicron integration concepts and/or (high fill factor) device arrays.

To demonstrate the capabilities of our approach, ultra-thin AlInGaN micro-LEDs (each 150x150 μm^2 in area) were first transfer printed onto mechanically-flexible plastic substrates in various configurations. These included 16x16 device arrays with large spacing and, to demonstrate the positioning accuracy, linear LED strips with device spacings from 1 μm halved sequentially down to 62.5 nm. The minimum achieved positioning was found to be limited only by the roughness of the device sidewalls. An overview of the receiving substrate preparation will be given in section 3.1 followed by a description of the fabricated transfer-printed LEDs in section 3.2. Two initial methods to electrically address the devices were attempted using two types of conductive inks, and these are described in sections 3.3 and 3.4, respectively. The final approach to address the devices

with the use of flexible thin metal tracks is described in section 3.4 and the optoelectronic performance of the resulting devices is described in section 3.5. The chapter concludes with the demonstration of nano-scale transfer-printing by sequential deposition of LED's in columns (described in section 3.6). The positioning limitations are described for the smallest device spacing attempted.

3.1 Prototype 01 - Substrate architecture

The first device prototyped was intended as a proof of concept and encompasses the deposition of ultra-thin LEDs onto a flexible film of Polyethylene terephthalate (PET) with a thin adhesion enhancement layer of PDMS spin-coated on top. PET is a polymer-based plastic material that can be made of different thicknesses for a wide range of applications. It is used in research laboratories as an optically-clear flexible substrate and is available with layers already deposited or with different surface properties (such as oxide coatings, dielectrics, surface treatments, etc.). Here, 0.125 mm thick PET substrates coated with indium tin oxide (ITO) were used to accommodate a full 16x16 printed LED array (total of 256 devices) with horizontal and vertical device spacing of 350 μm and 210 μm, respectively. The overall circuit design and electrode positioning can be seen in Figures 3.1(a) and (b). To act as a dummy alignment circuit, a photoresist pattern mimicking the overall circuit layout was deposited which aided placement during transfer-printing operations. Dummy alignment marks are typically used during mask-

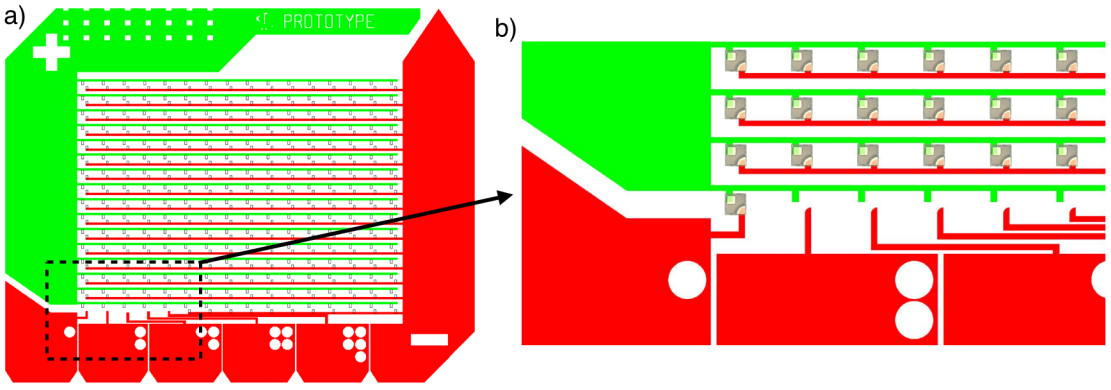


FIGURE 3.1: Interconnecting circuit design for Prototype 01. This circuit allows the addressing of a broad area array (total of 256 devices) and five individually addressable devices (represented on the bottom by five individual n-pads)(a). In (b), a magnification of the highlighted area showing the pads to address the LEDs. The circuit is used both as alignment and as certifier, to ensure the LEDs are placed in the correct electrode configuration.

aligning steps in photolithography procedures and the same analogy was used here. Due to the large area available for printing and the major concern being the precise LED placement to match the corresponding (to be transferred) electrical addressing circuit,

the alignment circuit employed was a copy of that same circuit. This provides consistent feedback on the device positioning in large area printing as the optical microscope of the NLP-2000 system has a reduced field of view. As described before, this design matches the finalised electrode patterning that will be used to address the devices and this layout will be used for both bonding methods described hereafter.

3.2 150 μm^2 LED architecture

The LED architecture here described followed a typical approach for transfer-printed devices in that the LEDs were fully processed before the complete underetching of the Silicon growth wafer. The LED epitaxial structures were grown in an MOCVD reactor on Si (111)-oriented wafers [99] and were processed into 2 μm-thick micron-sized LEDs. A cross-sectional schematic of the epistructure as well as the experimental procedure used to fabricate the arrays of suspended AlInGaN LEDs for transfer printing are shown in Figure 3.2. For the growth (University of Cambridge) as-supplied Si wafers were thermally annealed to remove the native SiO_2 layer. This was followed by growth of an AlN nucleation layer which acts as a barrier to Ga reacting with the Si substrate (the large lattice mismatch between Si and Ga and the different thermal expansion coefficients for both materials during growth typically results in a poor crystal quality without this engineered layer interface). A thick (~600 to 800 nm) Al(Ga)N buffer layer was then deposited to control the stress, followed by typical LEDs epilayers: Si-doped GaN as the n-GaN, InGaN-GaN MQW (6 QW's) for the active region and Mg-doped GaN as the p-GaN [34, 98, 99]. Top-emitting (i.e. through the p-GaN) device fabrication began with

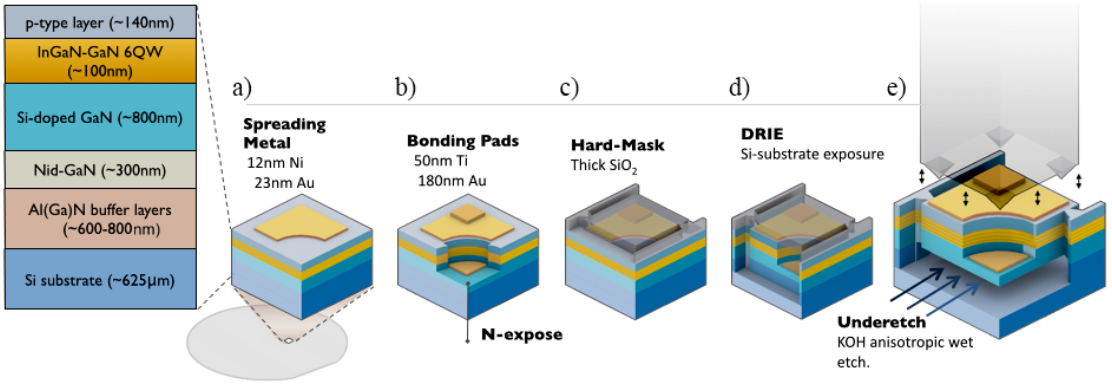


FIGURE 3.2: Schematic of the epitaxial structure and fabrication process for an individual suspended-membrane GaN on Si μLED. The left-hand figure represents (not to scale) the as-grown structure processed as follows: (a) Ni/Au current spreading layer deposition and patterning, (b) n-GaN exposure and opaque Ti/Au metal pad deposition, (c) SiO_2 mask deposition and patterning, (d) deep etching through the epilayers and into the Si substrate, (e) underetching of the Si substrate yielding devices supported by two sacrificial anchors. The grey overlay above e) represents the elastomeric stamp.

lithographic patterning of a semitransparent current-spreading metal (Figure 3.2(a)) - Ni/Au, with thicknesses of 12 nm/23 nm respectively - prepared using electron-beam deposition and subjected to annealing in an air environment to oxidise the Ni component. Inductively coupled plasma etching was then used to expose the underlying n-GaN layer of the p-i-n heterostructure (Figure 3.2(b)). Metal sputter deposition followed to produce opaque contacts on top of the current-spreading layer and onto the newly exposed n-GaN - Ti/Au with thicknesses of 50 nm/180 nm, respectively. To define the device lateral dimensions and most importantly the supporting *'anchors'*, a 1 μm-thick silicon dioxide (SiO_2) layer was deposited using plasma-enhanced chemical vapour deposition (PECVD) and patterned to protect the devices for deep etching through to the substrate (Figure 3.2(c)). RIE was used to continue etching deep into the Si substrate, thus exposing fast-etching Si-plane sidewalls. These were removed during the wet etch step (Figure 3.2(d)). To underetch the devices to prepare for their later release from the native substrate, anisotropic wet etching using 60 % w/w aqueous KOH solution at 80 °C was used. Si planes (110) perpendicular to patterned supporting anchors were preferentially etched (at a rate of ∼3.5 μm/min) while slower-etching (111) planes defined the vertical sidewalls. After completion of the underetching step, devices were held suspended above an air gap by two diagonally opposed sacrificial anchors, following the approach of [63]. The total thickness of the suspended devices after removal of the backing substrate is approximately 2 μm, characteristic of the Cambridge growth process and thinner than alternative GaN/Si growth structures typically reported by other groups [63, 72, 73].

SiO_2 is widely used as a mask in the microfabrication industry due to its low etch rate (<100 times less than Si) in alkaline KOH baths [100]. A SiO_2 (∼1 μm thick) layer was used as a hard-mask to protect the pixels during underetching and to help protect the deposited metals. Any existing residual SiO_2 was removed after process completion in a buffered hydrofluoric acid (HF) and DI water solution. After standard wafer cleaning, the micro-LEDs were ready to be transfer printed using pixel size-matched elastomeric stamps, as illustrated schematically in Figure 3.2(e). The overall intended metal protection provided by the oxide layer proved to be inadequate in practice. Metals deposited on top of the devices began to peel-off and visible damage to the current-spreading layer was observed both during fabrication and subsequent device operation after transfer printing (Figure 3.3). It is clear that during the underetching step, this protective layer can be laterally etched and/or its adhesion to the epitaxial layers severely compromised. After processing, attempts at driving the devices with the electrical probe-station did, however, result in light being emitted, thus showing no SiO_2 was left covering/protecting the devices.

The current-spreading layer comprised Ni/Au and, after the full underetch, displayed an elevated surface roughness Figure 3.3(a). Throughout the array, the most visibly

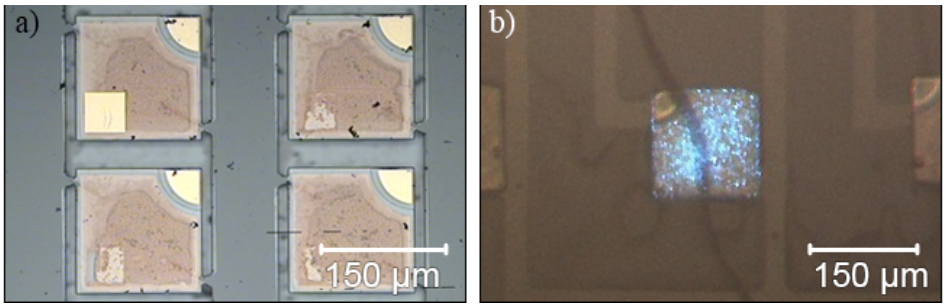


FIGURE 3.3: Insufficient SiO_2 coverage for metals on top of the LEDs: a) damage to the current spreading layer where an increase in roughness is visible as is the peeling off of bonding P-pad contacts (square pad). The damage to the metals (and the LEDs) becomes visible during operation as seen in (b), close to turn-on voltage (3.3 V).

damaged pad is the P-bonding pad (Ti/Au), with multiple devices being left only with a residual metal trace as visible in Figure 3.3(a). The peeling off of the pads indicates a problematic interface bond between the current spreading layer and the pad itself. Since both metal depositions are followed by a rapid thermal annealing step, different thermal expansion coefficients for the two metals might be damaging the interface in-between. This does not seem to affect the n-bonding pad since, here, the bond is direct to the n-GaN. While photolithography is a highly-directional technique (i.e. vertical), a lateral etching or edge-effects (i.e. thinner thickness) of the protective SiO_2 layer might be the cause of the premature coating failure. Since the sidewalls are vertical, the effectiveness of the coating is questionable since deposition on such directions for elevated heights is known to be severely reduced [81] as will also be seen for the next architecture reported in chapter 4.

3.3 Bonding with conductive epoxy/ink

For the first prototype, it was intended to use an interconnecting circuit created on the substrate itself. The flexible PET films (Sigma Aldrich prod. #749729) used were supplied already coated with a 100 nm layer of sputtered ITO. The use of this oxide is widely established in the microelectronics industry due to several advantages (transparency to visible light, low surface roughness and low surface resistivity (< 60 $\Omega/\square$)). To use this conductive layer, LEDs were initially deposited onto a receiving substrate with a dummy alignment circuit coated with PDMS on top as an adhesion enhancement layer (Figure 3.4(a)). This alignment circuit also replicated the layout of the final device metallisation, so the LEDs could be placed appropriately for later alignment to the addressing circuit layer. Transfer Printing of the full 256 devices (16x16 array) was performed by sixteen sequential *pick & place* operations of 16 LEDs each (using 4x4 stamps) with a yield of 100% in the transfer of devices. Upon completion

of the array, modified stamps - containing vertical posts with pyramids at the end - matching the location of the P and N electrodes of the LEDs (as illustrated on Figure 3.4(c)) were placed on the NanoInk stamp-holder. Using the modified stamps, two device

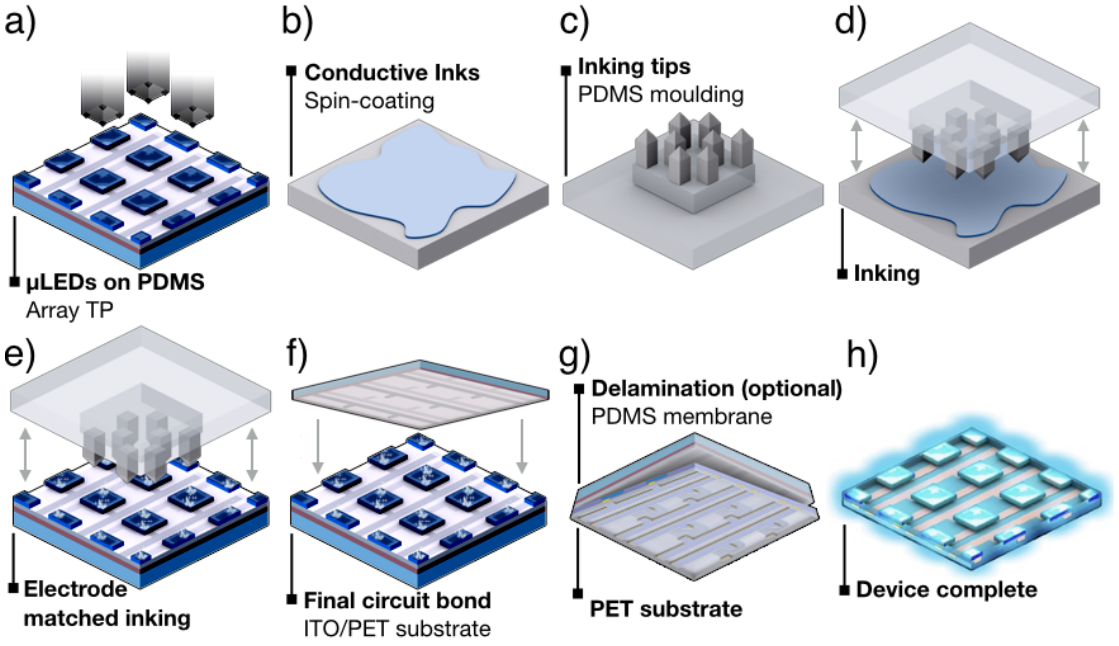


FIGURE 3.4: Transfer printing of LEDs onto a dummy alignment substrate in a), b) shows a thin film of conductive ink thinned down through spin-coating, c) shows a representation of the inking stamp design with two posts *per* LED, d) shows the inking of the posts which after wetting are used to ink the electrodes of each LED (e), f) shows the patterned ITO substrate being placed and g) the delamination after UV and thermal cure. In h) the device is ready to be debonded and addressed through the ITO conductive tracks.

bonding attempts were made using two different types of conductive inks spin coated onto a glass substrate as seen in Figure 3.4(b): a conductive epoxy (Norland #NCA130) and commercial silver ink (RS Silver Ink #186-3600). These were used in their liquid state and after dipping the modified stamp, inking of the electrode areas of the LEDs was performed (Figure 3.4(e)). In Figure 3.4(f), the substrate containing the final patterned interconnecting circuit is placed on top of the transfer printed LEDs and sandwiches the device.

A PET substrate containing the alignment circuit was flipped over (with the ITO tracks facing the devices) and transported by an adapted stamp, placing the inverted surface with the exposed patterned ITO circuit in direct contact with the ink droplets and LEDs. Upon contact, devices were flooded with UV light (curing for 6 hours) followed by a thermal curing step (~80° C for 8 hours) to evaporate the ink solvents and strengthen (solidify) the bond. After the thermal cure, peeling-off from the alignment substrate was performed (Figure 3.4(g)) so that where devices could be addressed through the

conductive ITO tracks. A 2x2 inking stamp design was used so that per inking transfer, 4 LED electrodes (a total of 2 per LED were) inked at each transfer.

The complete fabricated array of devices can be seen in Figure 3.5(a) with inked electrodes before the negative substrate is placed on top. As seen in Figure 3.5(b), de-bonding

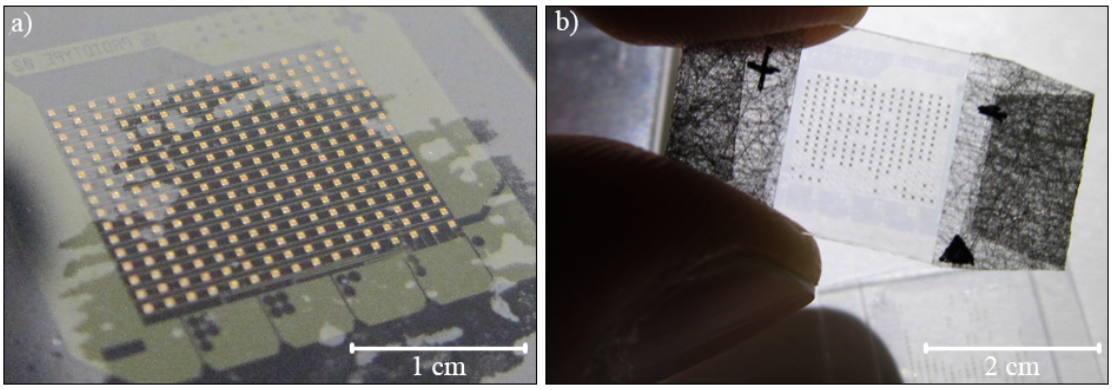


FIGURE 3.5: a) Photograph of a 16x16 transfer printed array of LEDs on PET before the substrate with the electrical tracks is bonded; b) shows the de-bonding of a conductive substrate from the alignment substrate. Unsuccessful bonding was observed for both types of conductive inks used.

unfortunately resulted in an incomplete array with 70 of the 256 devices transferred failing to bond to their new substrate - a 27% failure rate for the substrate transfer process. In the background of Figure 3.5(b), behind the scale bar, devices that failed to bond with the new carrier substrate are seen on the dummy substrate. Both conductive epoxy and silver ink devices have shown similar transfer failure rates, a direct result of the defective bonding from the cured epoxy/ink droplets and/or by the competing effect displayed by the PDMS adhesion-enhancement layer and the strong adhesion it has on the backside of the transfer-printed devices. While thermal curing can cause the PDMS to expand and shrink upon cooling down to room temperature (making it *'wrinkly'*), the elastic nature of this material allows it to fully conform to the LEDs. The adhesion of a completely flat PDMS surface in direct contact with the LED backside can easily surpass any weaker/defective droplets of rigid epoxy/ink at each of the electrodes. For the successfully bonded devices, the result of addressing via the substrate's ITO tracks is shown in Figure 3.6(a). Despite the large number of devices successfully bonded to the new carrier substrate, only a small fraction showed light emission (∼20 LEDs), and these at considerably different intensities. This could be a result of different electrode-ITO bond resistivity, different damage to the devices during processing, missing p-pads removed during the alkaline etch, etc. No short-circuits were observed as due to the nature of the circuit (with both serial and parallel configurations in use) this would have caused complete device failure (no light emission). From microscopic observations, no misalignments were observed in the positioning of the LEDs relative to their corresponding electrodes. When different bending curvatures are applied to the substrate, a faint flickering is observed by

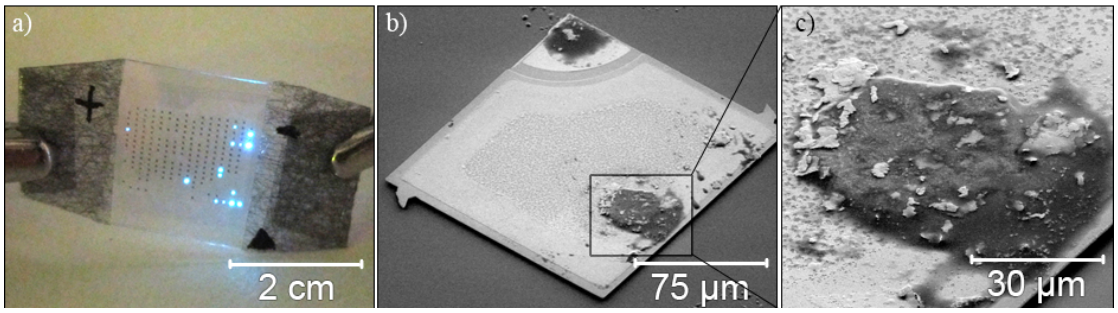


FIGURE 3.6: Addressing of the LEDs successfully bonded to the ITO tracks a). An average of 20 pixels show stable light emission when the substrate is not flexed; b) SEM imaging of an LED with inked electrodes after UV-light and thermal curing; c) close-up of a conductive ink droplet after curing.

some pixels while others start/stop emitting light. This indicates an inconsistent and defective contact between the interconnecting circuit and the electrodes of the LEDs. Further observations to assess the origin of these defects were made by scanning electron microscopy (SEM) where the pixels were imaged after inking the corresponding electrodes and all the curing steps (both UV-light and thermal) had been performed. After the solvent evaporation from the metal inks, SEM imaging of the surface of the bonding droplets showed different-sized metal flakes within a (now-cured) dispersing material which forms a dark coloured residue (Figure 3.6(b,c)). For effective electrical contact to occur, a continuous and steady path for current to flow is required, but this does not appear to have been achieved consistently here. A further sample with a 3x3 array of LEDs was placed on a curved backsurface as seen in Figure 3.7(a). For the ease of

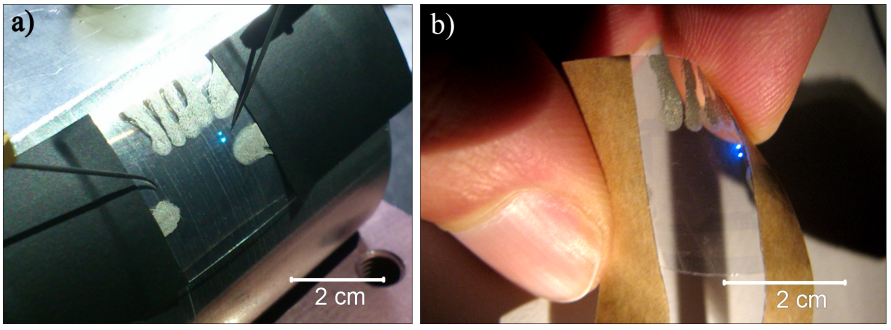


FIGURE 3.7: Bending of the ITO/PET substrate. In a) the completed device is being probed with needle tips on a curved support with a bending radius of ∼5 cm. In b) the same sample is flexed but addressed with conductive tape for ease of manipulation.

manipulation, the two main electrodes were addressed with conductive adhesive tape and the substrate was further bent to a lower radius of curvature. The intermittent contact that conductive inks provide upon bonding can be seen in both Figure 3.7(a) and (b), where different bending radius causes different intensity emissions on both of the emitting LEDs while the remaining seven LEDs on the array did not display any light emission under any curvature condition. To overcome these contacting issues, ensure repeatability

and stability, and to simplify the device assembly without substrate exchanges, metal tracks were then introduced as a way to address the devices. This approach is described below.

3.4 Prototype 02 - Addressing via metal tracks

in improving the way the LEDs were addressed, no changes were made to the method by which these were deposited onto their flexible substrates. This meant that a PDMS adhesion-enhancement layer was again used on the receiving substrate (LEDs are shown as deposited in Figure 3.8(a)). Adding metal tracks on top of the devices meant these needed to be electrically insulated on their sidewalls to prevent possible device failure. As such, covering the sidewalls while exposing only the electrodes meant these could be operated on their receiving substrate directly and thus the debonding step present in the previous electrode inking method was made redundant. Sequential transfer printing

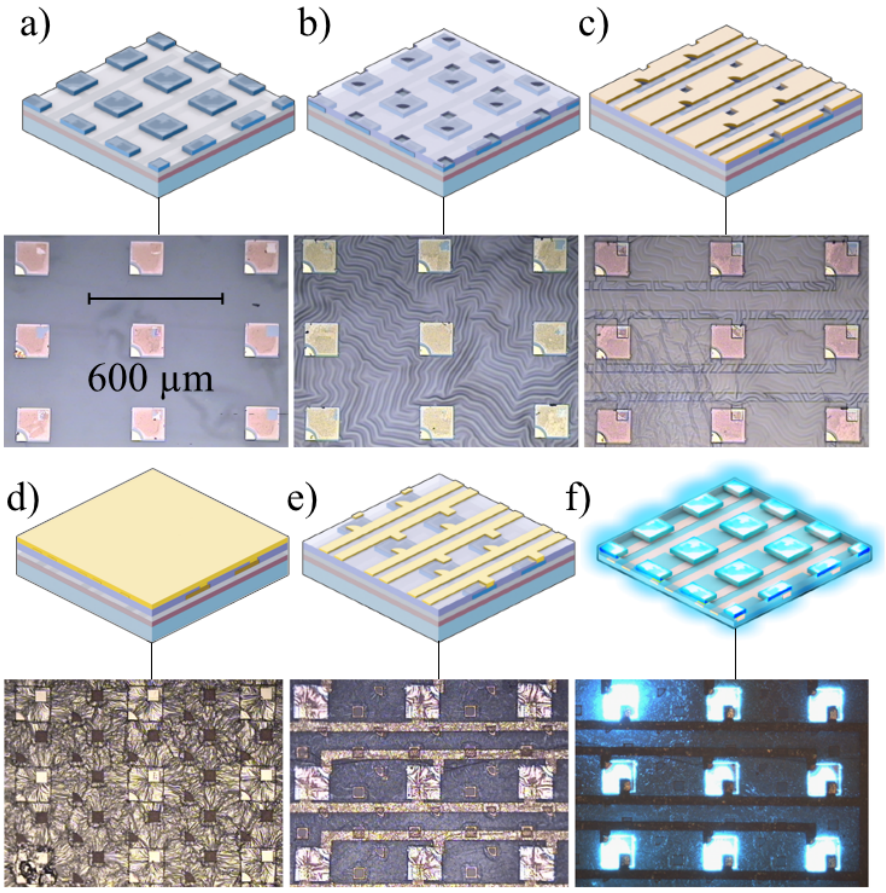


FIGURE 3.8: Schematic diagrams and top-view optical microscope images of the full fabrication sequence using metal tracks: a) LEDs transfer printed onto a PDMS/PET coated substrate; b) SiO_2 deposition for electrical insulation; c) photoresist layer exposing tracks and electrodes; d) full-device metal coating; e) removal of undesired metal and photoresist; f) finalised device under operation.

yielded a 100% complete array. This was also (as before) a 16x16 device array with a horizontal and vertical device spacing of 350 μm and 210 μm, respectively (Figure 3.8(a) to (f)). As mentioned above, addressing transfer-printed LEDs by metal tracks requires electrical insulation since the epilayer sidewalls are exposed. PDMS, being an organic-based compound, does not survive typical PECVD SiO_2 depositions, which are typically performed at 300 °C. Therefore a low-temperature (100 °C) SiO_2 dielectric layer of approximately ∼350 nm thickness was deposited and patterned by RIE to expose (open) the existing electrodes on each device (Figure 3.8(b)). Due to the thermal expansion of the PDMS layer during deposition, areas between the LEDs become *wrinkled* after cool-down to room temperature (visible in Figure 3.8(b)). After opening of the electrode pads (Figure 3.8(c)), a full-area metal deposition was performed as seen in Figure 3.8(d) and a patterning step followed to define metal tracks (comprising Ti/Au, thicknesses 50 nm/280 nm, respectively) 40 μm wide as a final interconnecting circuit for the elements of the array (Figure 3.8(e)). Finally, the micro-LED array was encapsulated by another PDMS layer and thus can be operated directly on the PET substrate or peeled-off as a membrane-like device with an embedded fully-functioning addressable micro-LED array (Figure 3.8(f)).

3.5 IV and LI performance

Figure 3.9(a) shows the current density versus voltage (J–V) characteristics from an individual reference micro-LED pixel during the various fabrication stages described above, acquired using needle probe-station for the steps before connecting via metal tracks. The initial turn-on voltage of a typical pixel is approximately 2.8 V. With the removal of the supporting Si substrate backplane, yielding a suspended device, this value increased to 3 V. These values are compatible with reported literature results [63, 65] where changes in the slope (and turn-on voltage) are seen after the supporting substrate is removed. The observed changes to the electrical characteristics of the LEDs may have their origins due to several factors: the exposure to the alkaline wet etch can cause adverse reactions to the epitaxial layers. As a result of this etch, the removal of the underlying Si substrate means the epistructures will undergo strain relaxation effects. The use of dry etching processes as well as the use of grown SiO_2 through PECVD are known to have adverse effects on the final LED performance, mostly due to Mg-doped complexes becoming passivated (i.e. electrically inactive) within the p-GaN layer. Transfer-printing of a device onto a PDMS substrate induced another increase in the turn-on voltage to 3.4 V. This increase is presumably the result of the increase in specific contact resistance during the successive processing steps. However, the differential resistance above turn-on was not significantly affected by these steps.

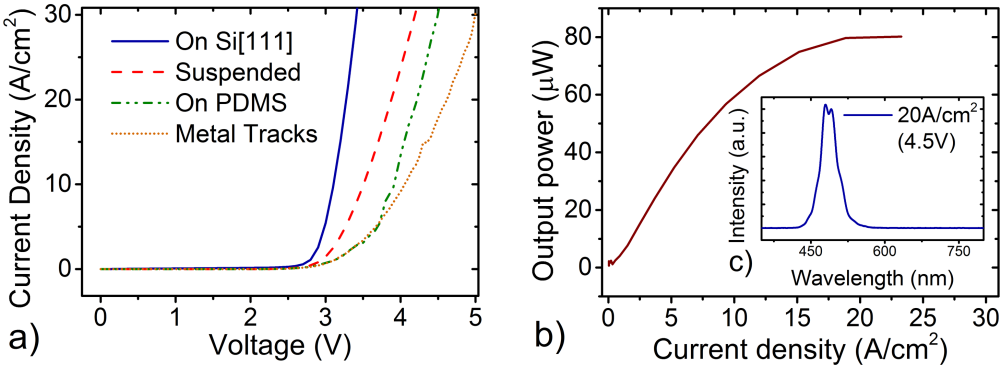


FIGURE 3.9: (a) J-V characteristics at several different processing steps and (b) L-J performance of a single pixel, with an inset (c) displaying the electroluminescent emission spectrum of a pixel driven at 20 A/cm^2 (4.5 V).

Once the devices were addressed through metal tracks (i.e. in their final transfer-printed configuration) a change in the slope was observed, resulting from the additional series resistance of the tracks, changing the device operation resistance (from the original tip-probing ∼126 Ω) to ∼263 Ω. Turn-on voltage was unaffected compared to the previous processing step.

Figure 3.9(b) shows a typical optical output power versus current density (L-J) characteristic, measured using a power meter with a calibrated Si photodiode detector (0.9 cm diameter) placed in close proximity (1.5 cm) to a metal-track addressed LED. A Lambertian emission profile was assumed, to convert the collected optical power into values quoted for the full forward hemisphere. The LEDs can be driven up to 20 A/cm^2 before thermal roll-over. At this driving current, the total forward optical output power is 80 μW per pixel, corresponding to 355 mW/cm^2 at each device surface. The EL emission of a single pixel was acquired by an optical fibre-coupled spectrometer aligned with the emitting surface. The emission is observed to be centred at 486 nm (37 nm FWHM) and is composed of two major peaks (Figure 3.9(c)) which are attributable to the high refractive index contrasts between the thin GaN-based epilayers (n∼2.3), air (n∼1) and the PDMS (n∼1.4) substrate, resulting in Fabry-Perot interferences [34, 99]. This would not be expected to be present if roughening of the backside surface during underetching had been severe.

3.6 LED nano-positioning

To assess the high-accuracy positioning capabilities of the transfer printing system, LED devices were placed sequentially in multiple columns (a total of 3) on a PET/PDMS substrate (Figure 3.10(a)). These devices were transfer printed individually from the donor Si (111) wafer and positioned on the receiving substrate using a set of pre-calculated

coordinates in the user interface control software (see Chapter 2) of the adapted dip-pen nanolithography system. The settings were chosen to give varied target spacings between the devices, starting from 1 μm, and reducing by successive factors of two down to 62.5 nm. The effective separation between devices was measured in plan-view by SEM imaging

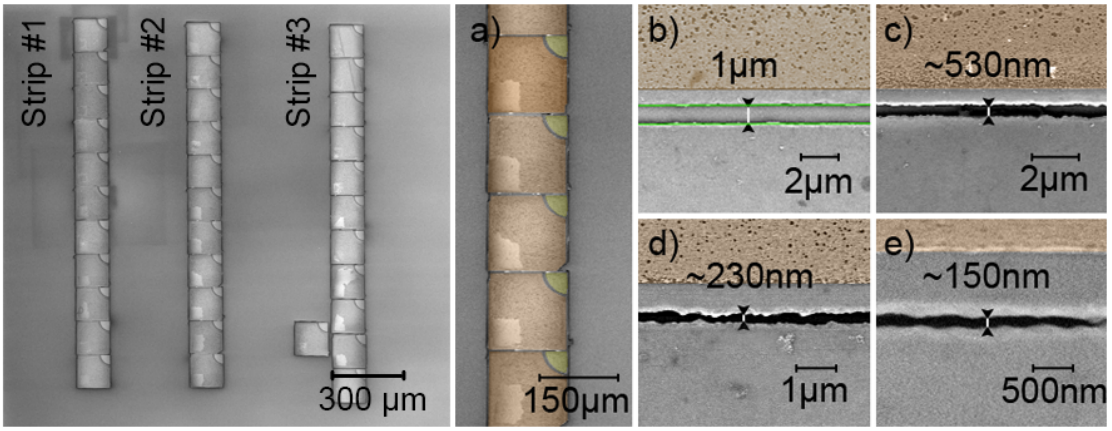


FIGURE 3.10: SEM imaging of side-by-side printed nano-positioned LEDs. A total of three strips were deposited: in (a), a colourised strip close-up of the targeted spacings ranging from 1μm to 150nm (b),(c),(d),(e)); in (b), an example of the measurement lines (green coloured), fitted to the imaged device boundaries over 30-40 μm distances used to estimate the spacing, is shown.

(Figure 3.10(b) through e)) with a large-field detector. Although the device sidewalls do not display perfect verticality, oblique-view imaging confirms the slopes are such that the top surface in this orientation represents the point of closest approach (i.e. the device edges have an inward slant). The microscope's software image analysis functions were used to measure device separations through image processing tools, specifically by superimposing best-fit linear boundaries on the acquired images over typical lateral distances of 30 to 40 μm. The effective spacings between devices were thus measured and confirmed with a set of close-up image acquisitions (Figure 3.10(b-e)). The measurements as described were repeated on three nominally identical arrays of devices.

Numerical results illustrating the high degree of placement accuracy are summarised in Table 3.1. Deviations from the exact programmed positions were observed and can

TABLE 3.1: Comparison between the intended (software input) device spacing and that obtained after the automated transfer positioning, averaged from measurements on three different arrays.

Intended Positioning (nm)	Obtained (nm)
1000	1011 ($\pm$62.5 nm)
500	530 ($\pm$48 nm)
250	230 ($\pm$28 nm)
125	150 ($\pm$14 nm)
62.5	NA

be expected due stages positioning inaccuracies. These deviations can also be extended to the viscoelastic behaviour of the elastomeric stamp used to transport the devices. Differences in relaxation rates between the four pyramids present on each stamp body (i.e. slightly different retraction speeds between pyramids) can occur since height differences exist within the LEDs structure. The contact with different materials by the roof of the stamp can result in different localised relaxation rates. These can affect the printing precision as differences, since, an unbalanced stamp relaxation immediately after roof de-collapse can cause slight movements of the platelets. More importantly, as described before, dust particles between the stamp/LED interface can negatively affect the printing precision. This can occur since after stamp relaxation only a small area of contact - the sum of the four pyramid tip areas - is holding the devices to the stamp. Therefore the slightest perturbation at this scale is prone to disturb the original stamp-to-LED alignment during pick-up resulting in tilted or edge-overlapping LEDs being deposited. For nano-positioning accuracies, to ensure the highest level of repeatability and reliability in the original stamp-to-LED alignments, different PDMS compositions should be used (towards softer compositions) to guarantee a slow and smooth return-to-original shape of the elastomeric stamp. Nonetheless, remarkable printing accuracies has been achieved, ∼x10 more accurate than the best previous reports. For the reported placement accuracy, a ratio of 12:1 of PDMS to curing agent was used. This was found to be the best mixture as to ensure a very slow relaxation of the stamp upon picking up of the LEDs. High-ratios of PDMS to its curing agent are known to change the viscosity and the speed that elastomeric stamps return to their original shape. This was to ensure the least perturbation of the original stamp-LED alignment that can occur immediately after the pick up of an LED.

The minimum 150 nm (±14 nm) spacing attained by the nanopositioning system is presently limited by the side-wall roughness of each LED device (as seen through a larger imaged area of the sidewalls in Figure 3.11), itself mainly caused by lithography limits and edge faceting during the exposure to the KOH etch. The peak-to-peak roughness

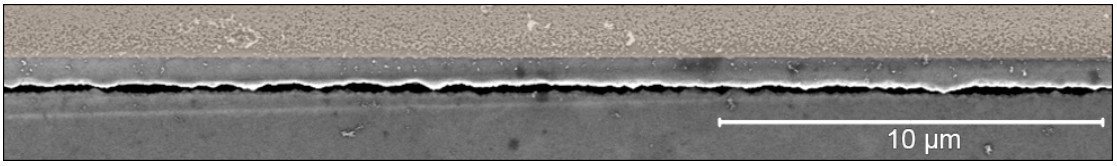


FIGURE 3.11: Two LEDs in close proximity. A wider view is shown here to provide an idea of the roughness along the entire sidewall which was the limiting factor to the positioning accuracy.

of these side-walls was measured by SEM and found to be higher than the successful minimum placement distance, resulting therefore in devices overlapping each other when attempting to create gaps of 62.5nm. We note, however, that positioning accuracy in the

few 10's of nm range should be possible with this adapted system if these issues can be addressed.

3.7 Summary

In summary, transfer printing with 150 nm (±14 nm) minimum spacing of ultra-thin GaN-based micro-LEDs onto mechanically-flexible PET/PDMS substrates was demonstrated. The 2 μm-thick devices were positioned in array configurations by parallel transfer and were characterised electrically and optically. The devices could be driven up to a current density of 20 A/cm^2 before reaching thermal roll-over and had a turn-on voltage ∼3.5 V after transfer. The forward optical output power was up to 80 μW per device, or 355 mW/cm^2 at the device surface. The nanoscale transfer printing accuracy was obtained by using an adapted commercial nano-patterning system, which was shown to be suited for a prototyping-level, high-throughput, automated printing process with large-area scalability. The steps taken to fabricate the prototypes described in this chapter established many of the fabrication processes for the upcoming chapters and devices. To address the initially observed poor performance, the LED microfabrication sequence was inverted and changes were made to the way devices were bonded to their new receiving substrates without using adhesion enhancement layers. These issues are thoroughly described in Chapter 4.

Chapter 4

Adhesiveless transfer-printing through liquid capillary bonding

Transfer printing of optoelectronic devices onto a range of substrates can result in added functionality and improve some of the devices' electrical, optical and/or mechanical characteristics. As the technique matures and is optimised, thin membranes of suspended materials can be achieved in a variety of ways, most commonly - in the case of LEDs - by underetching the growth substrate [63] (as described earlier) or by laser lift-off [73]. Both methods can yield thin membranes of materials that can be released and assembled onto new substrates. For the electrically-driven epilayers that comprise a typical LED device, removal of the growth substrate means disposing of its original heatsinking layer. Considering the quantum efficiency of GaN-based LEDs, a considerable portion of the injected electrical power is converted into Joule heating. During the operation of transfer-printed devices, heat is generated and strongly confined to the LED volume which poses a severe limitation on device lifetime, efficiency and reliability [73, 103]. Given that small LED dies can reach temperatures of up to 150 °C [104] under DC bias, these elevated temperatures can result in undesired effects on the electroluminescent (EL) emission (red-shifted emission peak, optical power degradation (emission droop) and in some cases, permanent damage [73, 103, 105, 106]). This becomes problematic because typical receiving substrates for transfer-printed optoelectronics have adhesion enhancement layers to aid the release of the LEDs from the transporting stamps [66]. Most of these layers are soft polymer-based materials, with poor thermal conductivities (e.g. for PDMS, 0.15 W/m.K [107]). The ideal adhesive layer would be temporary, in the sense that it can be removed immediately after serving its purpose, leaving no intermediate layers interfacing between devices and substrates. This would allow the active materials and substrates to exchange heat more efficiently – in this case, from the device to the carrying substrate (or heatsink), making it possible to operate devices at

higher current densities and thus higher optical power output without the associated thermal drawbacks.

To address these issues, the TP of 100x100 μm^2 blue-emitting micron-size LEDs (micro-LEDs) was developed to make use of liquid capillary bonding methods. Devices emitting around 465 nm were assembled in a 6x6 array format onto solid substrates - namely single-crystal diamond platelets (200 μm thick) and thick optical-grade silica (1 mm thick), for the demonstration of solvent-assisted bonding onto rigid inorganic substrates.

4.1 Prototype 03 - Substrate Architecture

The third prototype series in this work focused on optimising the LED fabrication procedure and improving the overall device performance. The arrangement of devices and the corresponding probe pad configuration were designed to accommodate a 3 mm diameter diamond platelet as a heat-management substrate. For this, a 6x6 device array (total of 36 devices) was transfer printed with a device horizontal and vertical spacing of 340 μm and 240 μm, respectively. The overall device layout can be seen in Figure 4.1. The full array was built inside the diamond area and all the electrical addressing pads were moved away from the inner radius and placed outside this area to facilitate processing, handling and probing. The inner pads enable precise addressing using probe tip needles, while the external pads were placed to facilitate wirebonding. A total of four negative bias electrodes (as indicated in Figure 4.1(b)) were placed for redundancy and devices can be addressed using any of these as they are interconnected and shared by all the LEDs in the array. The remaining pads represent positive electrodes with higher-radius pads identifying 2x2 device arrays (a total of four) per device to the others which are for single pixels.

4.2 100 μm^2 LED architecture

Contrary to the previous arrangement (reported in section 3.2), this LED device architecture was fabricated in *flip-chip* format to improve the overall output optical power. Fabrication was initiated with ICP GaN etching to expose the n-GaN layer (Figure 4.2(a)), but to avoid metal damage - as seen in Figure 3.3(b) - the underetch step was introduced in the early stages of device fabrication. This meant that any material depositions (especially of metals) would not be affected by the alkaline etch. Nonetheless, to aid in protecting the GaN epi-layers as well as reinforce the structural rigidity of suspended structure as much as possible during the wetting process, a 1 μm thick SiO_2

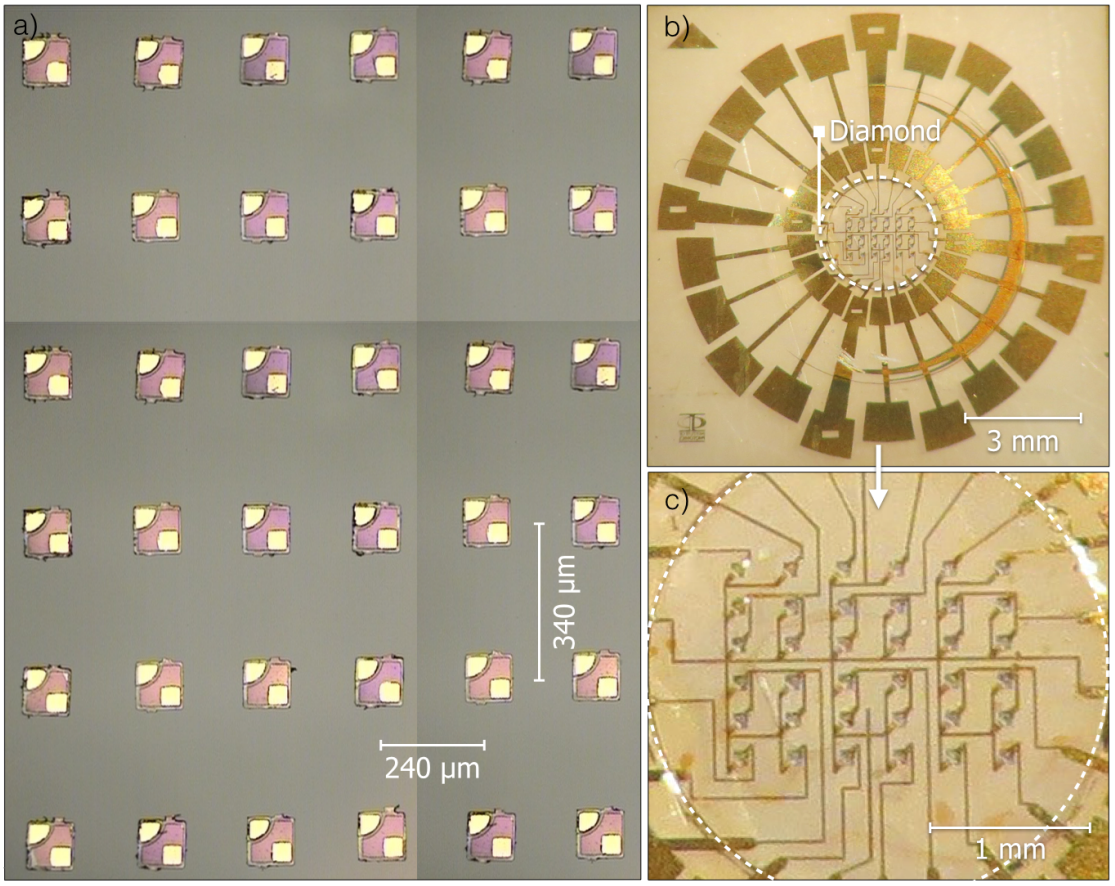


FIGURE 4.1: A composite image of a 6x6 array of devices (a). In b), the full device and its interconnecting circuit is imaged. In c), the full array showing that the addressing of 1x1 or 2x2 devices simultaneously is possible.

layer was deposited and patterned with the mask defining both the pixel area and the supporting sacrificial anchors as seen in Figure 4.2(b). The SiO_2 layer was etched by RIE followed by a long ICP etch to etch through the epi-layers. Upon exposure of the underlying Si wafer, a deep RIE etch was once again used to drill through the Si, opening enough clearance for the wet process. A 60% w/w KOH wet etch was used to anisotropicaly etch the substrate underneath the epilayers, resulting (again) in suspended structures (Figure 4.2(c)). The process was followed by a 90-nm-thick palladium current spreading layer deposition, promptly annealed after RIE patterning as illustrated in Figure 4.2(d). This completed the device fabrication, ending with membrane-like LED structures suspended with an air gap underneath and ready to be transfer-printed as seen in Figure 4.2(e). No thick metal bonding pad deposition were required since the devices were to be addressed by metal tracks, which form both interconnecting circuit and LED electrode bonding pads. A better overall device yield was achieved as a result of this inverted fabrication process, with no damage to the metal deposited on top of the p-GaN. A significant improvement in the device performance and reliability was noticed as will be described in the following sections.

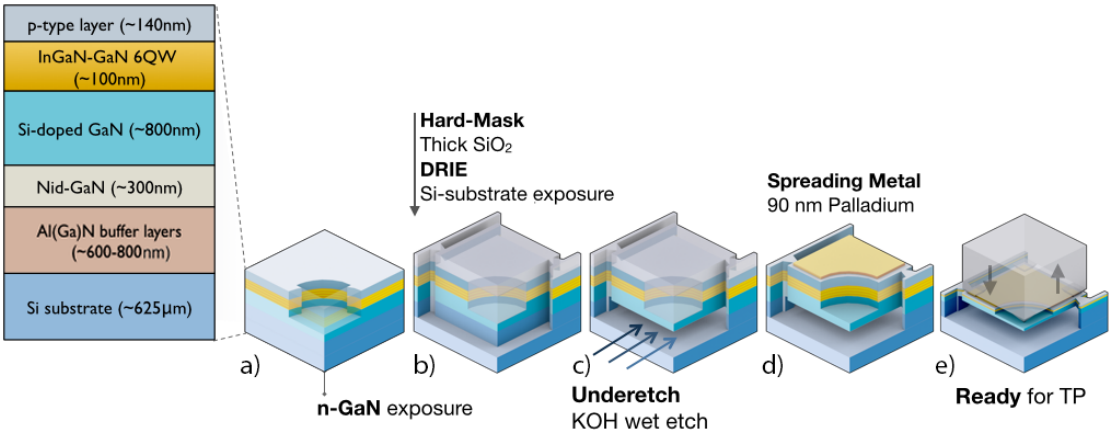


FIGURE 4.2: Schematic of the epistructure and modified fabrication process for an individual μLED. The left-hand figure represents (not to scale) the as-grown structure, processed as follows: (a) n-GaN exposure; (b) thick SiO_2 deposition and deep RIE etch to the Si substrate; (c) anisotropic underetching of the underlying substrate resulting in devices suspended by sacrificial anchors; (d) thick Pd current spreading layer deposition and thermal annealing; (e) finalised devices being picked by an the elastomeric stamp. The epistructures were provided by Plessey.

4.3 Adhesiveless Transfer Printing

As mentioned above, one of the main ways to improve TP devices is through the use of heat-efficient substrates. To fully capitalise on this approach, a good bond between the heat generating volume (i.e. the epilayers) and the substrate has to exist. This can be achieved if there are no intermediate layers in between to negatively impact the heat flow between the materials. To do this, the use of liquid capillary bonding was implemented without any major changes to the described architecture of either the stamps or the LEDs. In liquid capillary bonding [108] an appropriate solvent is placed between two flat surfaces and through pressure and/or evaporation, the two surfaces are drawn together for a robust van der Waals' bond. After successful pick-up from the donor wafer (Figure 4.3(a)), wetting of the LED backplane is performed: a pipette is used to release small droplets of acetone on a pre-cut typical cleanroom wipe (Figure 4.3(b)). The capillary forces involved during the stamp compression of the LED on the receiving substrate are sufficient to force the device removal from the stamp (Figure 4.3(c)). The overflow of the solvent plays a crucial role in the pixel positioning. For any misalignments that may occur during wetting and transport, the stamps in a half-height pyramid compression configuration can be used to adjust the positioning of the LED laterally within the overflowed wetted area. This is an advantage over the use of adhesion enhancement layers, where printing is always at a fixed position and cannot be adjusted afterwards.

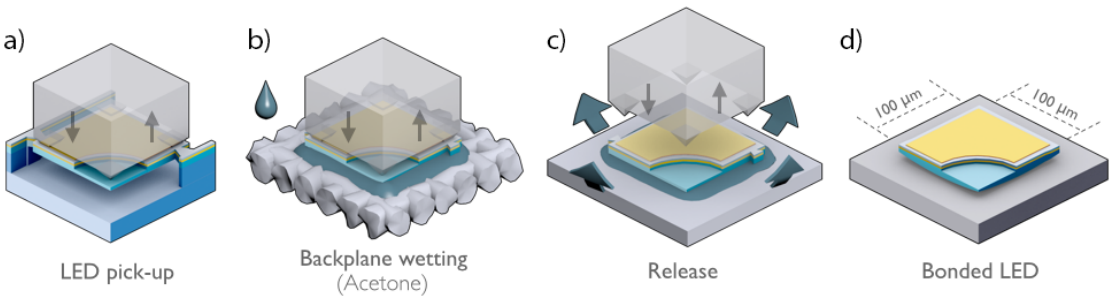


FIGURE 4.3: Schematic of the liquid capillary adhesion TP process: (a) represents the pick-up of a suspended device using an elastomeric stamp. After pick-up, the LEDs are compressed against an acetone-wetted cloth (b) and released when the backside gets in contact with a receiving substrate (c). The excess of solvent aids the positioning and release of the LED from the transporting stamp. In (d), after thermal annealing, the LED is left bonded to the new substrate.

4.4 LED curvature study

After successful pick-up from the donor wafer and wetting of the backplane and transport to the receiving substrate, compressing the devices onto the new substrate causes a lateral solvent overflow from the backside wetted surface of the device as seen in Figure 4.4(a). Retraction of the stamp releases the device on the receiving substrate and frees the stamp for the next transfer procedure. The overflowing solvent reflows underneath the LED area, instantly evaporating near its edges as seen in Figure 4.4(b). The lack of metal on the n-electrode permits viewing of a set of underlying optical interference fringes. After thermal annealing at 50 °C to evaporate the remaining liquid, the devices are left

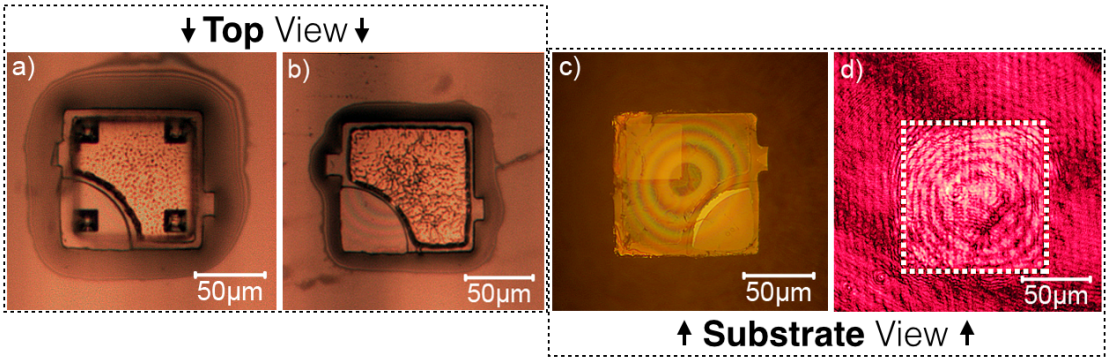


FIGURE 4.4: An LED capillary bonded onto a diamond substrate. (a) after the wetting of the LED backplane, contact is made with the receiving substrate; (b) the stamp retraction allows the liquid to reflow underneath the LED; (c) after a quick thermal cure and imaging through the backside, interference rings under each pixel are visible under white light illumination; (d) imaging the LEDs using laser light provides useful information for calculating the backplane curvature.

bonded by van der Waals' forces at the interface area between device and substrate. Careful observation of the deposited LEDs through the substrate, (Figure 4.4(c)), reveals a pattern of circular interference rings in the geometric centre of the LEDs. The two

surfaces in contact (i.e. diamond or optical-grade silica and the micro-LED backplane) display similar surface RMS (root-mean-square) roughness at the interface, i.e. ∼1 and 0.8 nm, respectively, as measured by an AFM. As described previously, the smoothness of the LED under surface is aided by the protecting SiN_x layer [34, 64, 99]. This extremely low roughness results in two tightly bonded surfaces resisting mechanical vibrations and surviving the multiple wet-processing steps necessary to complete the device fabrication. Imaging the devices through the backside of the receiving substrate reveals the full pattern of interference rings as seen in Figure 4.4(d). This indicates a curvature of the released LED dies which prevents full contact of the backplane area between the dies and the host substrate. Contact seems to be limited to the LED central region. This effect is attributable to the strain present in the GaN epi-layers which will be described in section 4.4.5.

4.4.1 Interference rings calculations

The method to investigate the observed curvature of the LED dies after deposition used the imaged interference rings under monochromatic and coherent (653 nm laser diode) light (Figure 4.5(a)). Broad-emission light sources are not appropriate to perform these measurements since their emission comprises a multitude of simultaneously emitted wavelengths. The observed rings on the two close-proximity surfaces (as seen in Figure 4.4(d)) are fringes occurring when light passes through a convex surface (i.e. LED platelet) in contact with a flat plane (i.e. the rigid substrate) and gets reflected back. The area not in contact varies from zero in the central region to a calculated height in the

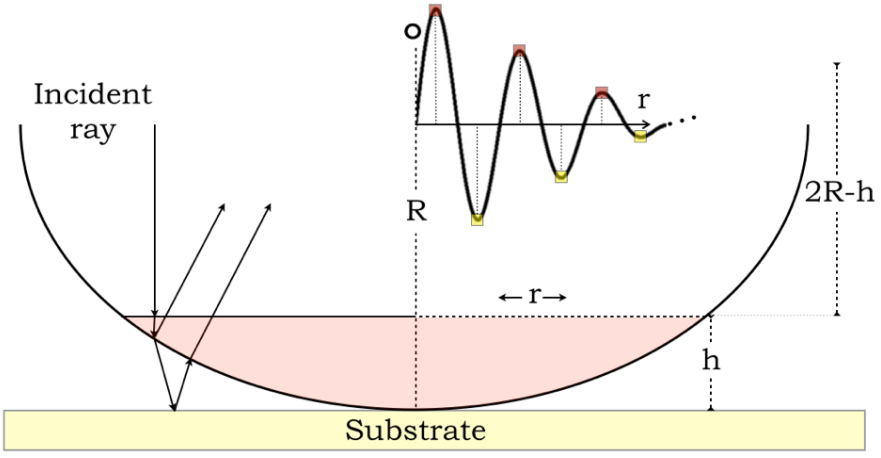


FIGURE 4.5: Schematic for a perpendicularly incident light ray on a convex shape/plane interface being reflected from both the bottom of the curved surface and the top of the flat surface. From the maximum and minimum points detected in (a) using monochromatic light enables the detection of maximum (highlighted as red squares) and minimum (highlighted in yellow). These are identified and used to calculate interference modes.

outer limits. The height can be precisely estimated with the use of the monochromatic

light (Figure 4.5(a) and 4.6(b)) to resolve the maximum and minimum points of the interference pattern. Considering the square shape of the deposited LEDs, any distance r from the central area – or area of contact - will be two times the actual height between the dies and the flat substrate. The interference rings obtained are circular proving that although square in shape, the backplane curvature is symmetrical with respect to the centre of the LEDs. An example of several extracted profile lines from an imaged pixel can be seen in Figure 4.6(b). The red and yellow squares represent maximum

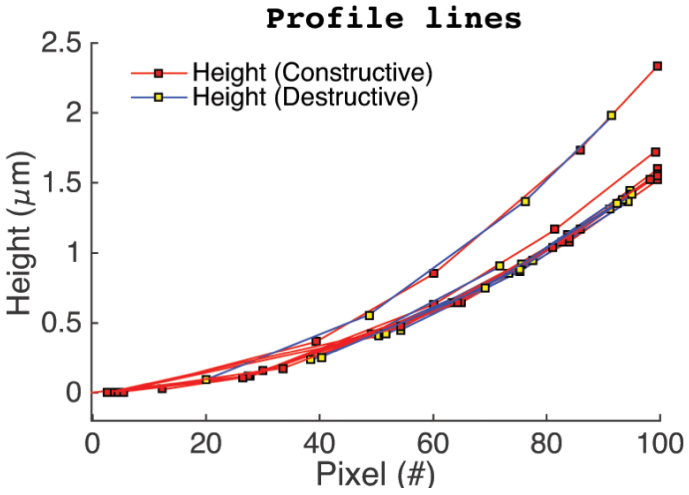


FIGURE 4.6: By using monochromatic light, profile lines are extracted from the centre of the LED towards the sidewalls where maximum (highlighted as red squares) and minimum (highlighted in yellow) values are used to calculate interference modes.

and minimum detection points of constructive and destructive interference, respectively. Considering the circular shape of the interference pattern, the radius of any obtained ring is therefore given by:

$$(2R - h)\, h = r^2 \tag{4.1}$$

Equation 4.1 can be rewritten so that

$$2Rh - h^2 = r^2 \tag{4.2}$$

Since h^2 is considerably smaller when compared with $2Rh$, it can be disregarded, simplifying equation 4.2 to

$$2Rh = r^2 \tag{4.3}$$

where the path difference $2h$ for the incident light can be correlated to r^2/R. This means that equation 4.4

$$\frac{r^2}{2R} = h \tag{4.4}$$

can be used to relate the detected radius r of the maximum and minimum points with the overall radius of curvature R. From the interference patterns, an observed bright ring

− and therefore a ring where constructive interference is detected − occurs for

$$2hn = \left(m + \frac{1}{2}\right)\lambda \tag{4.5}$$

where n is the refractive index of air (n=1) and λ the wavelength of the incident light. Substituting equation 4.4 into equation 4.5, one gets

$$\frac{r^2}{R} = \left(m + \frac{1}{2}\right)\lambda \tag{4.6}$$

Solving equation 4.6 for r, gives

$$r = \sqrt{\left(m + \frac{1}{2}\right)\lambda R} \tag{4.7}$$

where *m=0,1,2,...* and r is the radius of the m^{th} observed ring away from the contact area. The first mode (m=0) occurs on the first bright ring and therefore

$$N_{th}ring - 1 = \#mode \tag{4.8}$$

For the destructive interference, where the path difference between the rays is $m\lambda$, we have

$$2hn = m\lambda \tag{4.9}$$

Substituting equation 4.4 and solving for r results in

$$r = \sqrt{m\lambda R} \tag{4.10}$$

where *m=1,2,...* and r is the radius of the m^{th} ring. The *0* mode refers to a radius of zero and therefore is the geometrical position of the dark fringe at the centre of the interference pattern. Considering the curved backplane height to be h=r^2/*2R* (equation 4.4) and solving for R gives the overall radius of curvature of the platelet using both constructive and destructive interference modes. Thus, with multiple profile lines heading towards different directions on the pixels, the overall backplane height can be spatially reconstructed using the interfering modes as seen in Figure 4.7. The effective contact area (colourless part of the mesh in Figure 4.7) in the central region was found to be 14±2% of the total pixel area and the radius of curvature (R) averaged 2 mm *per* pixel. This technique can also reveal further information regarding pixel positioning and tilting. The use of this method for reconstructing the backplane curvature does have its own drawbacks, however, as it is extremely sensitive to image artefacts. In characterising multiple dies by analysing their captured interference patterns, some showed equivalent contact areas to those seen in Figure 4.7, while others showed a smaller contact area or

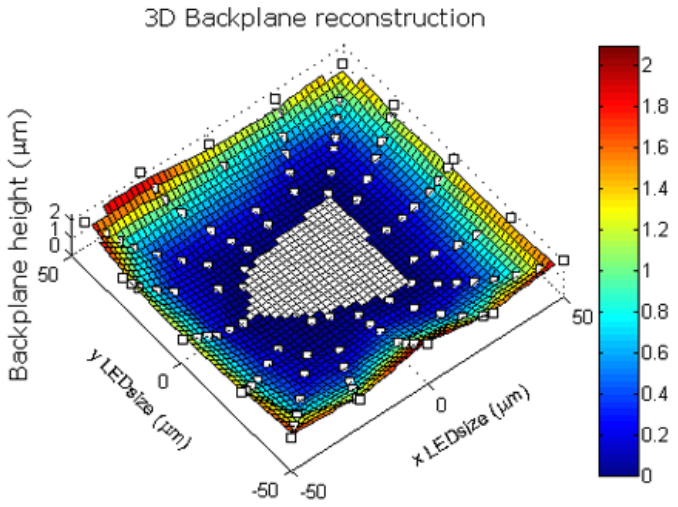


FIGURE 4.7: The backplane height is reconstructed as a surface mesh for a reference pixel. The colourless region indicates the area where contact is assumed to occur.

were susceptible to positioning distortions.

While, generally, the calculated heights and curvature for the capillary bonded TP LEDs are similar to the ones seen in Figure 4.7, exceptions do occur. In Figure 4.8(a) an imaged pixel from a different wafer batch shows a reduced contact area (6±2%). The higher degree of curvature for this platelet could be an indicator of an altered strain zone, possibly indicating an area susceptible to a higher level of strain. In Figure 4.8(b),

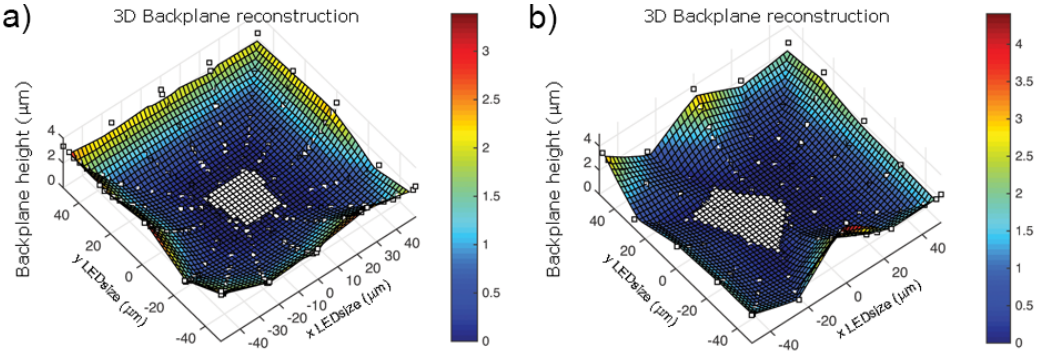


FIGURE 4.8: Imaging of two platelets displaying reduced (6±2%) (a) and defective (b) contact areas. The use of interference patterns to measure curvature radius has shown to be extremely sensitive to artefacts.

one can see one of the main advantages in utilising interference patterns for curved backplane reconstructions. Often, particles that are on the receiving substrate will affect the positioning of the devices. These include any residual photoresist - from the subsequent processing after underetching - that might be trapped under the device where the dry etch tools cannot effectively act. From experimental observations, any existing imbalance from the stamp decollapse when releasing the devices can leave the device tilted. This can occur due to the existence of excessive solvent underneath. Any areas

where the solvent evaporates last will cause a longer-lasting capillary bond and will force the pixel to retain a tilted orientation. This is usually suppressed once devices are electrically insulated, where the deposition of a thick PR can cause the re-balancing of the platelets and reset their contact area to their geometric centre. Resetting of the platelet positioning to establish the central area as the contact area can also be obtained with a further compression from the elastomeric stamp. Poor (or severely reduced) contact area with the substrates have been identified as a major issue for premature pixel roll-over and degradation during operation.

4.4.2 AFM measurements

Interference patterns are useful if the distances being measured are on the order of the wavelengths being used. With shorter wavelength sources a different pattern would be imaged and more information regarding the central area in contact could be obtained. However, to further determine the backplane curvature in this area, a profile scan measured by AFM was performed (45 μm in length) as close as possible to the geometric centre of a flipped over pixel so the backplane was the uppermost surface. The central area was measured and the fit extended over the entire lateral size of a pixel (Figure 4.9). The overall fit by a polynomial of degree 2 adjusts to the raw measured data:

$$height(\mu m) = 1.149 + 0.012x - 3.733x10^{-4}x^2 \tag{4.11}$$

By zeroing and adjusting the measurement to the minimum height as the centre of the backplane curvature, the AFM height scan matches the interference ring height reconstruction for the area surrounding the centre of the pixel (with ± 2 μm displacement fluctuations). However, the performed AFM measurement (and corresponding fit) cannot

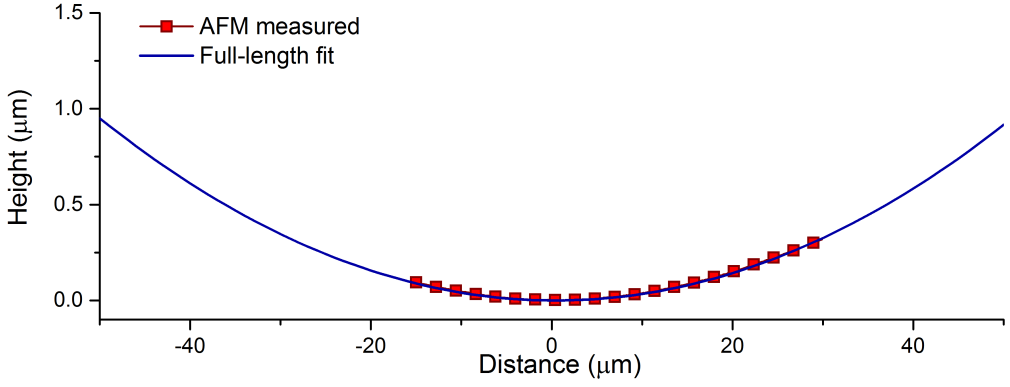


FIGURE 4.9: AFM profile measurement (red dots) of the central curvature of a flipped over LED die with the fit extended to the full size of the die (blue line).

be seen as an absolute representation of the complete backplane curvature since the measured points lay on the parabola apogee.

4.4.3 SEM imaging

Further observations were made using SEM imaging on the sidewall of a TP LED platelet. At oblique imaging angles (Figure 4.10(a)), the platelet can be seen to be bowed as there is a shadowing effect visible in the outer edges of the LEDs. Further reduction of the SEM tilting angle (from 45° to 21° degrees) as seen in Figure 4.10(a) and (b), allowed a better examination of the spacing between the platelet and the substrate. While SEM

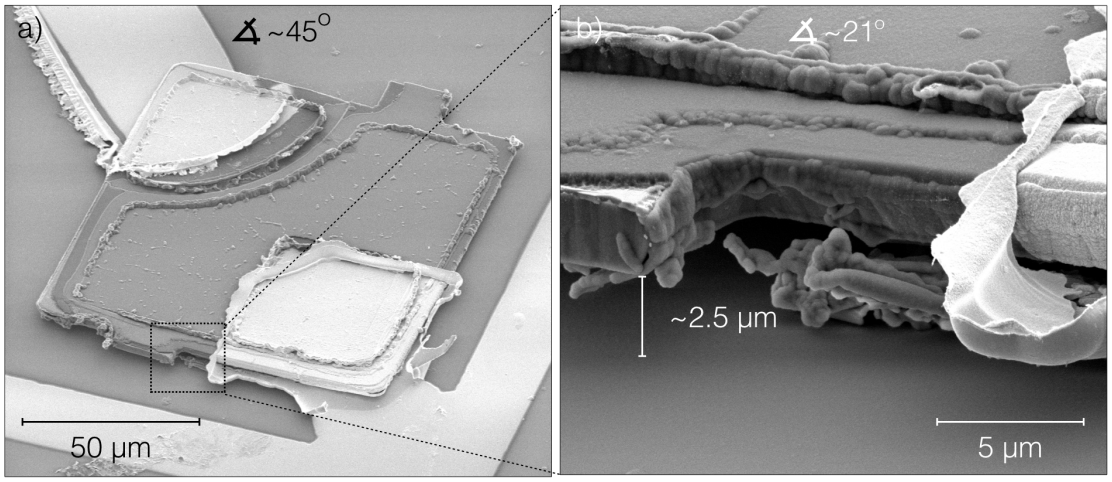


FIGURE 4.10: SEM image (a) of a micro-LED deposited on silica addressed by Ti/Au metal tracks. The highlighted area is magnified in (b) and viewed with a lower tilt angle, providing an estimated height from the backside edge of the pixel to the substrate of approximately 2.5 μm.

imaging at high tilting angles do not provide reliably accurate measurements, it is worth noting that the observed heights at the platelets extremities do seem to be in close agreement to those of the interference rings method. To be noted in Figure 4.10(b)is residual photoresist underneath the sidewalls which was not removed during the plasma etch. The protective effect provided by the sidewall (*etch shadowing*) limits the action of directional plasmas used to clean photoresist residue. A further significant observation from SEM imaging was confirmation of the insufficient electrical insulation provided by the SiO_2 deposition at the device edges. In Figure 4.11(a), the deposited SiO_2 layer for electrical insulation of the LED sidewalls is seen not to extend to the device edges.

The negative slope of the sidewalls of the LEDs - a result of the wet etching procedure - impedes successful SiO_2 device insulation for an air-exposed metal track addressing scheme. Any metal deposition on such devices will inadvertly metal-coat the sidewalls shorting the LEDs during operation. This effect was not observed in the Prototype 01 devices reported in section 3.1 due to the malleable nature of the PDMS adhesive layers used. This meant that no height gaps existed between the device sidewalls and the underlying substrates. To circumvent the undesired effects of these height gaps as observed on the rigid substrates, a thick top insulating layer was deposited. For this

SU-8 was the photoresist of choice, as seen in Figure 4.11(b), due to its capabilities in producing high-aspect ratio and elevated thickness features. Here, a 6 μm thick SU-8 layer was deposited to attain full-device insulation.

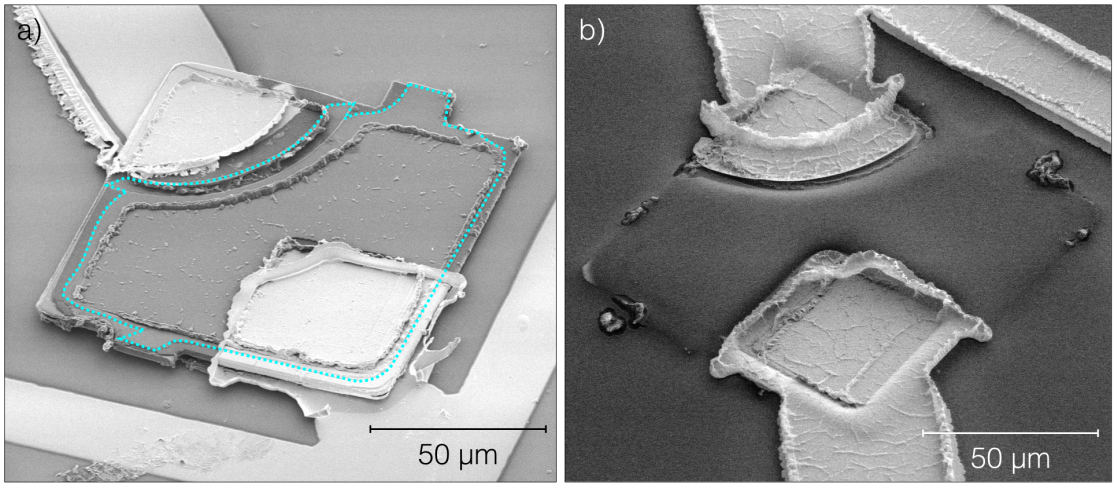


FIGURE 4.11: SEM imaging of two insulation approaches: a) shows failure to fully insulate the platelets successfully. The blue-cyan dashed line shows the area where SiO_2 coating formed after deposition; b) shows an attempt using thick SU-8 photoresist coatings covering laterally the exposed device sidewalls.

4.4.4 van der Waals LED/substrate interfacial forces

The adhesion forces maintaining a platelet in a fixed position on its new substrate have to be high enough to withstand further dry and wet fabrication steps. Equation 2.5 was applied to the following calculations and adjusted for the Hamaker constant of the interfacing materials between the TP platelets and the receiving substrates. The Hamaker constants reported by Bergstrom *et al.* for these materials were $\sim$0.48x10^{-20} J, $\sim$6.3x10^{-20} J, $\sim$16.7x10^{-20} J and $\sim$22.0x10^{-20} J for SiO_2, Silica, SiN_x and diamond, respectively [109]. By using equation 2.5 to estimate the force *per* unit contact area, the plot in Figure 4.12(a) is obtained. Since the Hamaker constant is a convenient way to represent the magnitude of the interacting surface forces, it is not a surprise that diamond and SiN_x are the materials yielding the higher interacting force per unit area. This becomes especially evident at higher separations ($\sim$ 10 nm) where SiO_2 and Silica are able to generate an attractive surface force of *only* 1 N/cm^2. When compared at this distance, both SiN_x and diamond can still generate adhesion forces which are nearly one order of magnitude higher. In Figure 4.12(b) the adhesive force generated by two close-proximity plates of different materials is plotted. The effective contact area was obtained from the interference rings calculations (in section 4.4.1) and the performed backplane reconstruction assumes an effective flat contact area ($\sim$14$\pm$2%) for a platelet area of 100x100 μm^2. As expected, due to their higher Hamaker constant, both SiN_x and

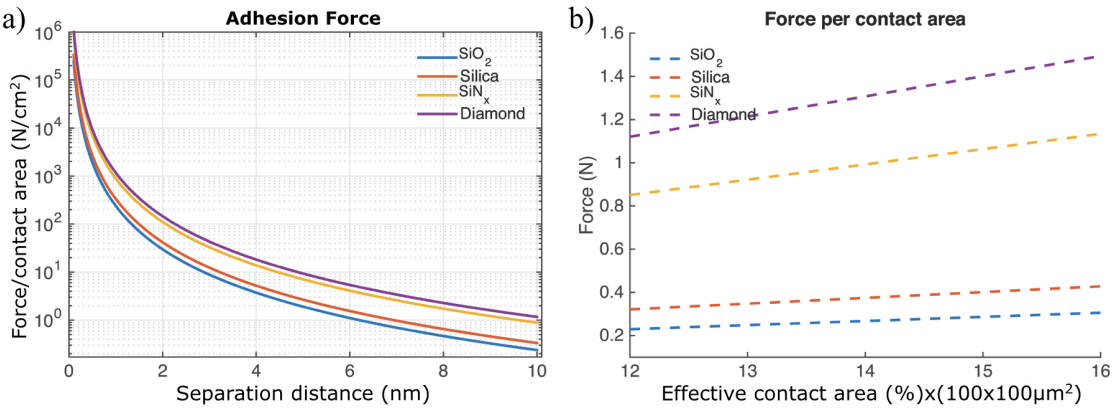


FIGURE 4.12: Adhesion force calculations *per* unit area for two flat surfaces is shown in (a). In b), the force generated by two platelets in close proximity (∼0.5 nm) is shon, considering the typical contact area between platelet and substrate estimated by the interference rings measurements.

diamond generate the highest force for the considered batch of materials. Considering the substrates where the LEDs were deposited and that the LED underlayer is SiN_x, this is an important result. Since both materials display similar surface roughness (RMS of 0.8 nm for SiN_x and 1 nm for diamond - AFM measured), these two materials are bound to create a very strong bond when in close proximity. One must consider the idealistic nature of the van der Waals formula which is valid only for interactions between two parallel objects. Despite these uncertainties, the van der Waals force keeping these materials bonded to their interfacing contact area is several orders of magnitude above the gravitational pull on these platelets, meaning these can be flipped over after solvent evaporation without detaching from their substrate.

4.4.5 Strain management

The overall curvature of the processed devices has its origins in the different properties of the material alloys (AlGaN, InGaN, AlN, Si-GaN) that comprise the LED epilayers. While Si (111) wafers are of the preferred orientation for the growth of wurtzite nitrides (due to their three-fold symmetry at the surface), growing GaN-based materials onto these wafers presents major challenges. The sequential MOCVD epitaxial depositions of different material alloys create multiple competing compressive and tensile strains between layers. Also, with Si and GaN being the main materials, these two have greatly different thermal expansion coefficients which becomes an issue during high-temperature growth and subsequent cooling-down [100]. For high-performance optoelectronic devices, the critical thickness to achieve crack-free GaN layers require these to be at least thicker than 1 μm. Considering that typical doping impurities such as Mg and Si (used to dope p-GaN and n-GaN, respectively) can also contribute significantly to the tensile stress of

GaN [110, 111], there needs to be careful thought given to the layer structure, sequencing and thickness during growth.

The major source of cracking observed in GaN film deposition comes from the tensile stress present during the growth at high-temperatures. The tensile stress caused by Si doping can be perceived via a crystallite coalescence model [112]. This crack-closure mechanism acts as an efficient source of tensile stress in the early stages of polycrystalline film growth. During the initial precoalescence stage, the film experiences compression due to the capillary forces on the deposited island surfaces. As the deposition proceeds and material islands grow in size, the force exerted decreases and relaxation occurs. As islands coalesce at their local interfaces, the overall tensile stress quickly outgrows the compressive during the initial stage for thicker layers [112]. To address the issue of tensile stress and consequent cracking, the inclusion of AlN and AlGaN layers have proven effective. AlGaN graded layers have minimal relaxation during growth and subsequent GaN layers are highly compressed. The layer compression decreases during cooling down to room temperature mostly due to the thermal expansion mismatch between the GaN and silicon as mentioned before [38, 113]. Other methods such as substrate engineering have been employed by the microelectronics industry to improve and ensure crack-free growth GaN on Si. Nitrogen ion implantation (N^+) through a thin AlN interfacial layer on Si (111) substrates has shown to significantly reduce the epitaxial layers stress (as much as 80%) reducing cracking and improving optical properties [114]. It was found that ionic implantation induces structural changes and introduced partial disorder in the substrate which then aids in relieving the stress of the GaN film.

The concept of using AlGaN stress management layers is to introduce enough compressive stress into the epilayers during high-temperature growth to compensate the tensile stress induced by post-deposition cooling down. The larger in-plane lattice parameter of GaN compared to AlN means AlGaN layers will be under compressive stress when grown on relaxed AlN substrate-to-epi interfacial layers. This compressive stress induces convex bowing of the Si wafer counteracting concave bowing upon cooling down after growth. The Al fraction can be either step-graded or continuously graded, with both methods being equally efficient in inducing compressive stress during growth [34, 115]. From our own material grower's experimental data [34] with in-situ curvature measurements performed during the growth procedure, the wafer concave/convex bowing can be seen in Figure 4.13. The data shows clearly the effects that the multiple layers have on the overall wafer curvature (bowing). In the early stages of the deposition it is clear that the AlN layer deposition causes significant tensile stress that progressively increases the wafer concave bowing, possibly due to the island coalescence mechanism previously described [112]. Throughout the deposition, continuous compressive stress was introduced during the growth of the AlGaN buffer layer and the following Si-GaN layer, inverting the wafer

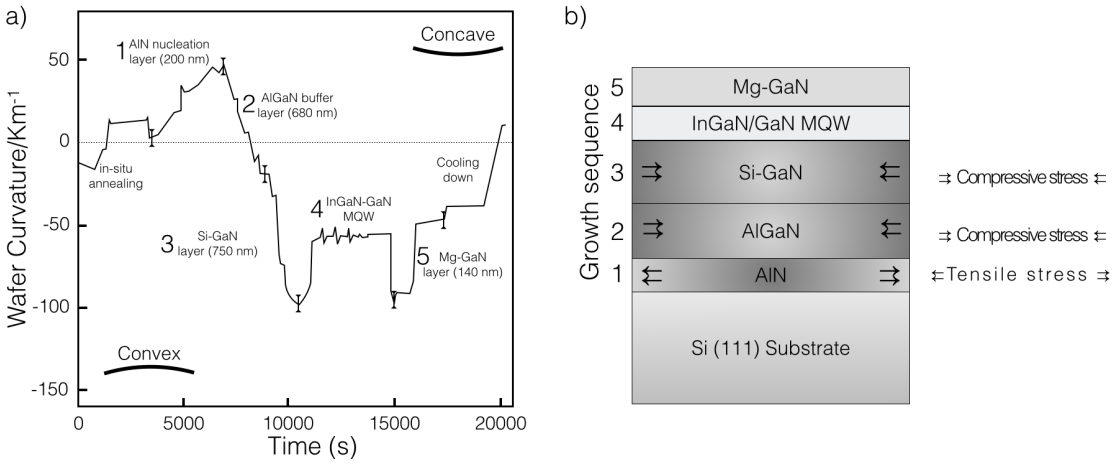


FIGURE 4.13: In-situ wafer curvature measurements during growth of an ≈1.8 μm thick GaN LED structure on a 6-inch Si (111) wafer (a) (Adapted from [34]), in (b) the competing compressive and tensile stresses are represented (layers not on scale) throughout the epitaxial growth sequence.

bowing from concave to convex. Thicker buffer layers allow the posterior growth of crack-free GaN layers due to the additional compressive stress introduced. As the plot of Figure 4.13(a) shows, it is possible to engineer pre-strained epitaxially-grown layers to achieve flat, non-bowing wafers when these are cooled down to room temperature, minimising any potential effects from existing stresses.

With the major thickness of the overall process concentrated in the Si wafer, this material (the growth substrate itself) largely counteracts the strain generated by the epitaxial layers. Removing this supporting substrate from underneath the thin layers during a wet etch procedure induces cracks on the epitaxial layers as illustrated in Figure 4.14(a). The removal of the underlying Si(111) substrate generates visible cracking of the epilayers, creating defects that intersect at 60° angles - which also matches the preferred cleaving direction of Si (111) wafers - showing the epilayers are subject to large tensile stresses at room temperature. In Figure 4.14(b), the same layers from the same batch are shown processed with the inclusion of a stress compensation layer, deposited to counteract crack appearance and bowing of the platelets, while reinforcing the structural integrity of the suspended platelets during the substrate removal. SiO_2 has been widely used by the microfabrication industry as a hard mask/insulation layer, though not necessarily as a deformable structural element. Due the nature of PECVD deposition at high temperature (300 °C), the effects of the compressive stress induced by SiO_2 [116–119] on top of the epilayers can efficiently eliminate the propagation of visible cracks, resulting in crack-free suspended epitaxially grown membranes. The efficacy of this method yields (as will be shown in chapter 5) perfect crack-free and uniform emission devices. No bowing, or bending of the anchors diagonally opposed corners, have been observed after using this layer, which, to be effective, has to have a matching thickness comparable to the

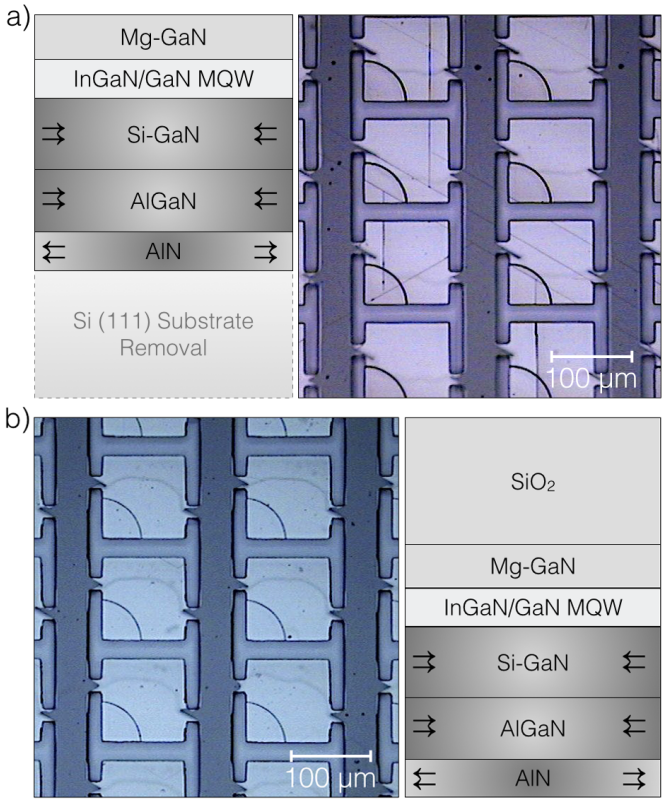


FIGURE 4.14: Epitaxial structure of GaN-on-Si wafers during underetching of an ∼2 μm thick LED structure without any structural reinforcement (a). In (b) the same underetching procedure is shown with the use of a SiO_2 layer on top.

thickness of the epilayers. The deposited SiO_2 layers can be removed after the completed underetching procedure. Due to the capillary phenomena occurring underneath the suspended membranes, where a form of microfluidic channel is created, the use of dry etching methods was preferred.

4.4.6 Completed devices on multiple substrates

With the above procedures having been established, the way was now open to print LED devices onto a wide range of substrates. The various substrates used are summarised in this section. First of all, to obtain a performance comparison with the devices reported in Chapter 3, a new device on a PET substrate with a PDMS thin film adhesion layer was fabricated with the newly available epistructure (Figure 4.2) and new LED size. This arrangement can be seen in Figure 4.16(a) with the inset illustrating the fabricated TP LED array. Since no height gaps exist on these devices printed onto polymers, and to ensure equal processing to the devices reported in Chapter 3, SiO_2 coverage was used to electrically insulate the LEDs, instead of an SU-8 encapsulation layer. All the other devices described below, however, include an SU-8 encapsulation layer, in the manner of Figure 4.11(b).

Figure 4.16(b) shows a completed device array on 50-μm-thick flexible silica glass with 2x2 LEDs under operation. This substrate was used to study the LED performance on a flexible inorganic material. Despite showing initially good promise as a substrate for

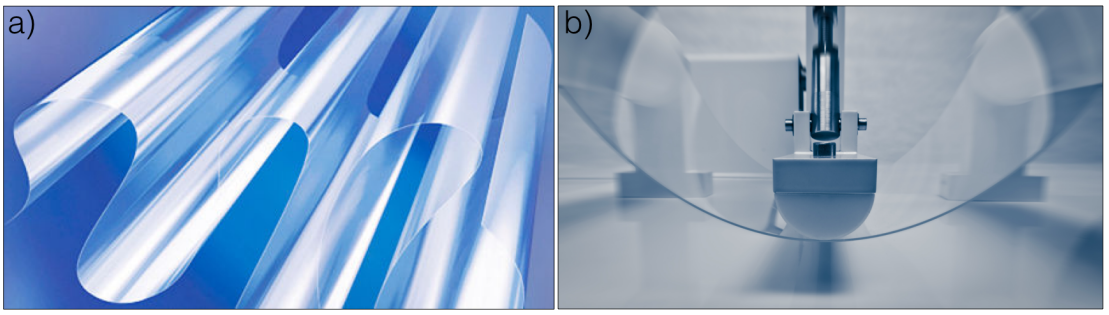


FIGURE 4.15: Photos of flexible glass substrates from Schott. In a) an ultra-thin glass substrate behaves as an ultra-flexible membrane, in b) bending tests on thicker versions purposely-built for flexible displays. From [120].

improved LED performance, due to the brittleness of the material (silica) and the size of the overall device (~1x1 cm^2), light flexing of the thin silica at such scales caused cracking and fracture of the substrate. Tests performed to validate the use of thin silica as a substrate that can be flexed, showed that these should be kept at at least 5x5 cm^2 of overall area.

Figure 4.16(c) shows a device on a thick (0.5 mm) optical-grade silica substrate with 2x2 LEDs under operation. This was used as a different (thicker) silica-based rigid substrate that would be used as the standard of performance for devices TP on silica.

Figure 4.16(d) shows a device completed on a single-crystal Diamond platelet. The disk inside the internal set of metal pads shows the platelet location and the inset is a partial representation of the TP LED array. Of all the tested substrates, this is the device containing the best material for heatsinking purposes, which due to the higher thermal conductivity of diamond resulted in the best optoelectronic performance, as will be reported in Chapter 5.

Figure 4.16(e) shows an array of 2x2 LEDs in operation on a substrate topped with an oxide-based distributed Bragg reflector (DBR). TP of devices on substrates with emission enhancing capabilities is now possible where, in the case of DBR-mirrored substrates, the LEDs can form a resonant cavity which ultimately can enhance and alter the EL emission from the device.

For colour-conversion purposes applicable for example in microdisplays or for visible light communications, Figure 4.16(f) and (g) show semiconductor photoluminescent platelets being optically pumped by the diamond device (in Figure 4.16(d)). While attempts at depositing the LEDs directly on the II-VI semiconductor platelets were quite

successful, problems arose during lithography steps due to the high-roughness of the substrate itself. As such, these were transferred to a silica slide and placed in direct contact with the substrate of the printed LEDs. Further details of the II-VI platelets are given in the following chapter. In Figure 4.16(g), a similar approach is shown with a red AlInGaP-based colour converting platelet.

The upcoming Chapter 5 reports on the performance optimisation brought by the two most heat-efficient substrates (diamond and silica) while making a performance comparison with the devices printed onto polymer.

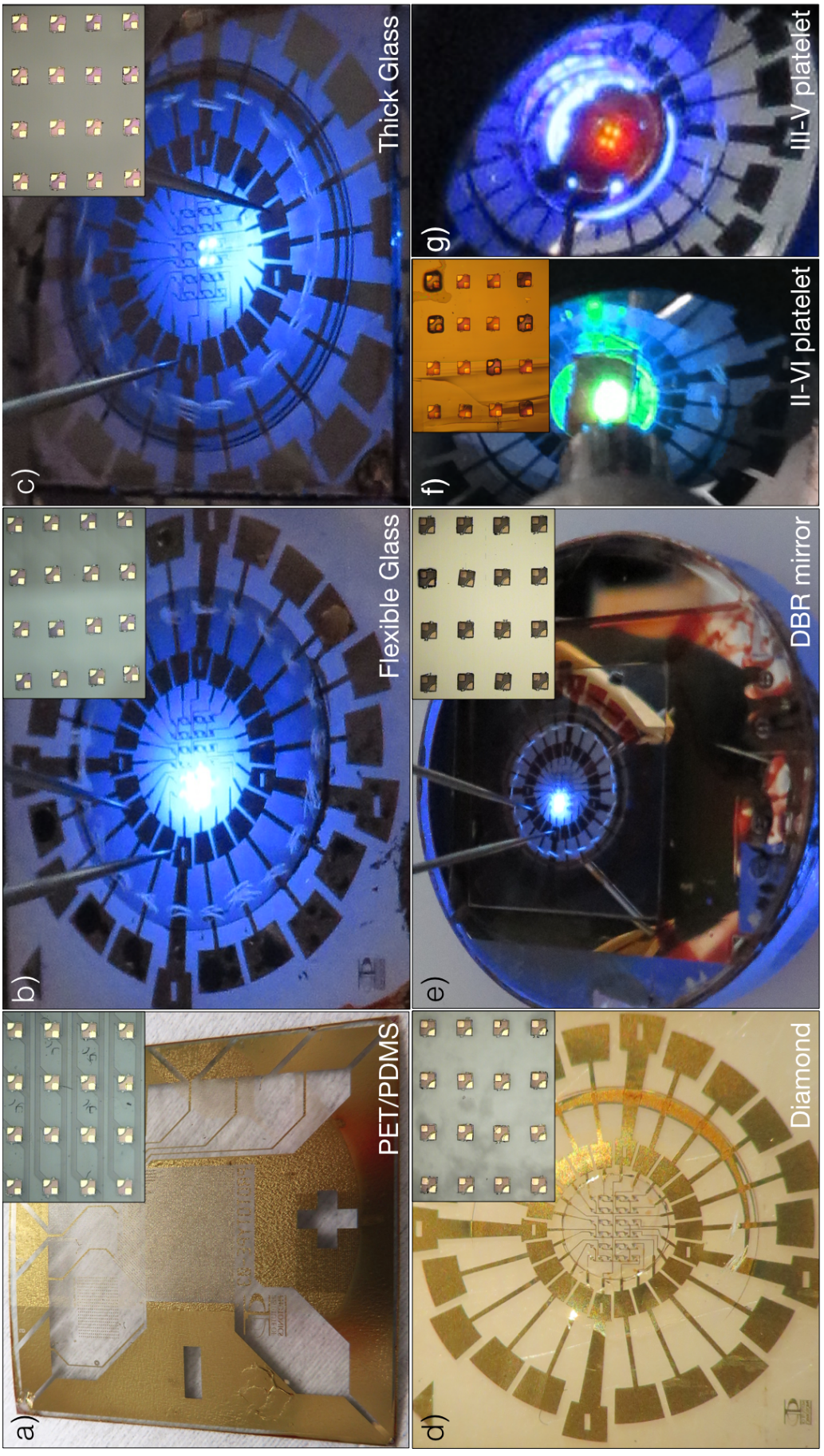


FIGURE 4.16: Summary of completed TP devices (a) on polymer with adhesion enhancement layers for comparison purposes to Chapter 3, (b,c,d) capillary-bonded to heat-managing substrates, (e) bonded to an oxide-based DBR mirror and (f) inorganic colour-converting semiconductor platelets with capillary bonded TP pixels and pumped by a capillary bonded device. While arrays of 6x6 devices were produced for all the devices, detailed image captures of the platelets required a magnification level where only 4x4 devices were visible.

Chapter 5

Micro-LEDs transfer printed onto thermally efficient substrates

In this chapter the relatively low performance of the devices reported in chapter 3 is addressed, to improve the optoelectronic properties of TP LEDs. The effects of membrane damage and cracking have been addressed as described in chapter 4. Here the poor heat management capabilities of the substrates and intermediate layers are addressed, since otherwise, after printing, LEDs quickly reached their L-I roll-over condition. Kim *et al.* [73] recently studied the performance of different-sized TP LEDs on flexible polymer substrates and showed the operating temperatures to be the determining factor in LED emission power droop. The spectral shifts and changes to the turn-on voltages observed hinted at damage to the epistructures during operation at high-temperatures. It is to be noted that such observations were based on the use of intermediate adhesion-enhancement layers [73].

To address these issues while disposing of the heat-inefficient adhesion-enhancing layers, devices were fabricated following the procedures reported in section 4.2 and capillary-bonded to their receiving substrates following the method described in section 4.3. The full device was then insulated according to the findings in section 4.4.3 with the use of a high-aspect ratio PR (SU-8). In this chapter device operation for the substrates with the highest performance is described and their thermal properties analysed. Thermal imaging measurements were undertaken to measure the operating temperatures and the spectral behaviour of the devices was also studied. The relevance of the results for applications including visible light communications is described later in this chapter.

5.1 Prototype 04 - Device Architecture

To act as an electrical insulation layer for the devices here reported, a 10 μm-thick SU-8 layer was deposited and patterned before Ti/Au metal tracks were deposited on top. An overview of the environment surrounding each LED can be seen in Figure 5.1(a) for adhesion enhanced (left hand side) and capillary-bonded (right hand side) devices. Devices being operated in different configurations (single (1x1) or quad (2x2)) can be seen in Figure 5.1(b) through (d). While Si as the growth substrate can act as a heatsinking

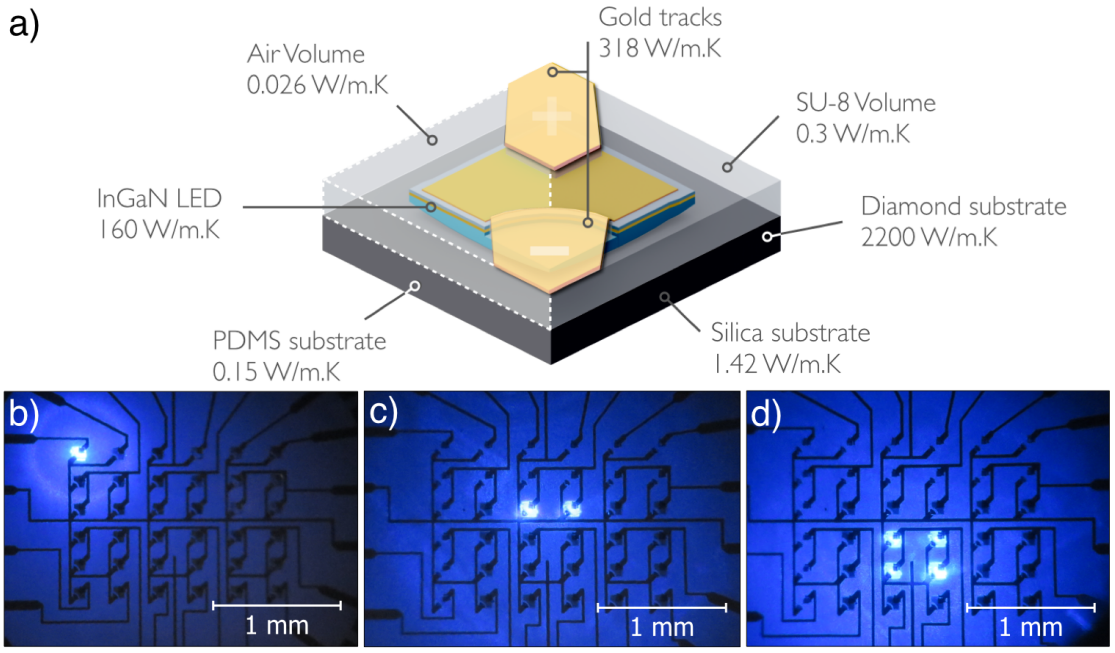


FIGURE 5.1: Thermal conductivities of various materials surrounding a transfer-printed LED: the left half section of the device (dashed contour) illustrates the air-exposed baseline devices deposited on PDMS adhesion enhancement layers. The right half section represents the best performing substrates (diamond and silica) with improved heat dissipation SU-8 encapsulation on top. Different device operation configurations for 1x1 and 2x2 LEDs are possible as seen in (b),(c) and (d) respectively.

material (the thermal conductivity of Si is ~150 W/m.K [30]), this material is removed during the underetching fabrication step. Silicon substrate removal is also a requirement for the use of *flip-chip* device architectures where the emitted light emerges from the n-GaN side. Removing this substrate causes the heat generated during device operation by any TP device to be confined to the volume of the GaN epilayers (~160 W/m.K [74]) and insufficient thermal dissipation occurs in the air-exposed section of the device top surface. Printing onto polymers or other substrates using adhesion enhancement layers compromises performance as it has been studied and described. In the case of liquid capillary bonded TP micro-LEDs, the devices are in direct contact with two different thermal conductivity materials: the substrate underneath - diamond (~2200 W/m.K [121]) or optical-grade silica (~1.4 W/m.K [122]) - and the upper insulation layer - SU-8

(∼0.3 W/m.K [123]). The considerable differences in the thermal conductivities of the different substrates play a crucial role on the device performance as will be described in the upcoming sections. To highlight the results obtained, devices printed onto PDMS will be used for comparison purposes.

5.2 Electrical and Optical Performance

Figure 5.2 shows the voltage (J-V) and optical power density (J-L) versus current density for the LEDs transfer printed on diamond and silica as shown at the end of chapter 4. For performance comparison purposes, Figure 5.2 also has the J-V plots and optical power of a reference micro-LED on a PET substrate (device (a) in Figure 4.16). The reference device contained air-exposed pixels (no SU-8 overlayer) deposited on the PET substrate with a 20-μm-thick intermediate PDMS adhesion layer. Such a device operated at a maximum driving current density of 30 A/cm^2 producing an optical power density of 55 mW/cm^2 before roll-over and permanent damage to the pixel was observed. This is a comparable result to that shown in Figure 3.9. While the devices deposited onto adhesion enhancement layers are not able to reach the operating level (high-injection of current densities at elevated operating voltages) of devices on more heat-efficient substrates, the J-V curve displays a premature turn on, an indication of alternative current pathways or effects of deep transition levels in the bulk of the different semiconducting materials [12]. Devices deposited on PDMS are more inclined to display parasitic effects where higher shunt and series resistances severely deform the characteristic J-V curves before, near and after their turn-on point. This is evident as the optical power density curve follows a similar trend to the other devices but the J-V curve does not, so the devices will reach their limit much earlier. It is also possible that the LEDs deposited on adhesion enhancement layers on flexible substrates experience additional strain. As described previously, GaN devices printed from Si are curved due to the strain release with removal of the original silicon substrate. The viscoelastic nature of the adhesion enhancement layer and its far greater thickness (20 μm) compared to the membrane LEDs could introduce some strain. While GaN is quite brittle as a material, the high aspect ratio that lateral dimensions have over the overall device thickness makes it susceptible to small deformations, which at this scale might be a further source of defects at the epilayers and their interfaces.

All the LEDs transfer printed on the rigid inorganic substrates without added adhesion enhancing layers display identical turn-on voltages (around 3.4 V). This indicates good ohmic contact and good performance from the current spreading layer (Figure 5.2(a)). The device operation can be divided in two regions, a current density regime where the

operational limits of air-exposed LEDs are achieved (<30 A/cm^2 - left of the dashed red line) and a high-current density regime at the right of the dashed red line (>30 A/cm^2). Above 30 A/cm^2 the LED operation starts being affected by temperature. L-J curves

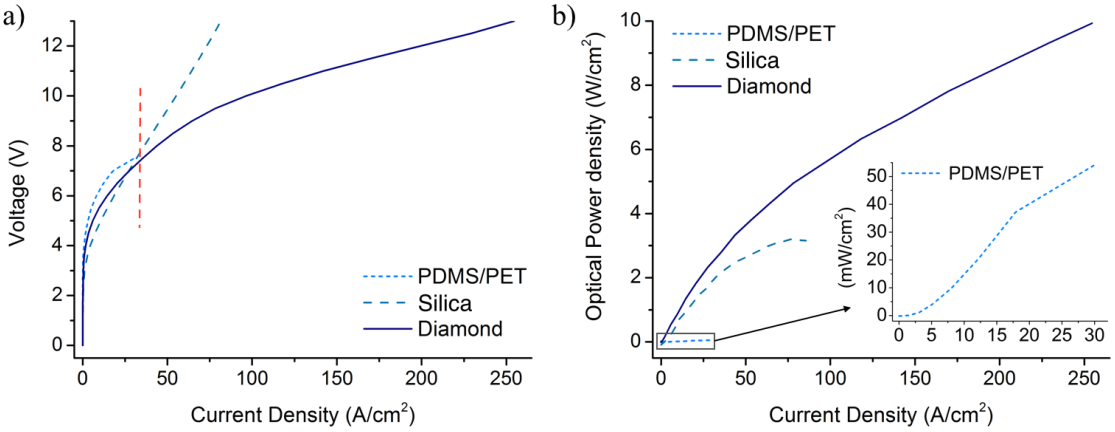


FIGURE 5.2: Comparison of J-V (a) and J-L (b) curves of a single GaN LED pixel on, respectively, diamond, silica and PDMS/PET substrates. The inset shows a magnification of the optical power density for PDMS/PET substrate devices since these achieved a maximum of only 55 mW/cm^2 at 30 A/cm^2.

were acquired with the devices in direct contact with a calibrated Si photodiode detector, capturing only the light going through the supporting substrate. From Figure 5.2 the maximum measured values for optical power density were 10 W/cm^2 at 255 A/cm^2 (I=20 mA), 3.2 W/cm^2 at 77 A/cm^2 (I=6 mA) and 0.055 W/cm^2 at 31.5 A/cm^2 (I=2.5 mA) for devices on diamond, silica and PDMS, respectively. Those LEDs deposited on the silica substrate produced an optical power inferior to their diamond counterparts and started to reach saturation around 78 A/cm^2. From the early stages of the high-operation regime and due to insufficient heat-spreading from the silica substrate, the J-V curve is affected and devices show inferior rectifying diode behaviour with a significant series resistance (1.4 kΩ) when compared with devices operated on diamond (250 Ω). The heat generated from device operation increases non-radiative recombination within the active areas, preventing further increases in the optical power. This is usually accompanied by a saturation followed by a decrease in the emitted optical power as is visible when currents higher than 50 A/cm^2 are injected into silica-deposited devices (Figure 5.2(b)). However, repeated driving up to 80 A/cm^2 showed no damage to the LEDs on silica. This shows that silica as a substrate has the ability to extract some of the generated heat from the LED when compared to devices in contact with adhesion enhancement layers. The results are important given the interest in integrating GaN LEDs with glass for display purposes.

Devices TP onto diamond consistently outperformed those on other substrates. The measured emitted optical power (10 W/cm^2) *per* LED was nearly three times higher when compared to the maximum power obtained on the silica substrate (Figure 5.2) and

represents a significant breakthrough, outperforming other reports of transfer-printed devices on adhesion enhancement layers (for an equal pixel size) by a factor of 10 [73]. This is a comparison with the devices reported by Kim *et al.* where AlInGaN-based LEDs were originally grown on sapphire substrates and detached via laser-lift of, although these were still deposited onto PET substrates containing thin adhesion enhancement layers [73]. Although, as a significant direct comparison with the LEDs grown on Si hereby reported on this thesis, Kim *et al.* obtained significantly higher (x20) optical power densities. Achieving high-brightness from localised light-emitting sources remains a crucial requirement for emerging applications such as optogenetics, cochlear implants with imbibed optoelectronics, colour conversion, optical communications, etc. [124–128]. These results are also crucial for solid-state-lighting applications where high-power emissions are required.

5.2.1 Spectral effects in electroluminescence (EL)

The very different heat-spreading properties of diamond and silica are expected to affect the spectral behaviour shown by LEDs operating at increasing dc drive currents. To study this, electroluminescence spectra were recorded with a fibre-coupled spectrometer. Figure 5.4 shows the behaviour of the EL peak wavelength with current density and the inset illustrates typical spectra at relatively low current density. The peak EL emission

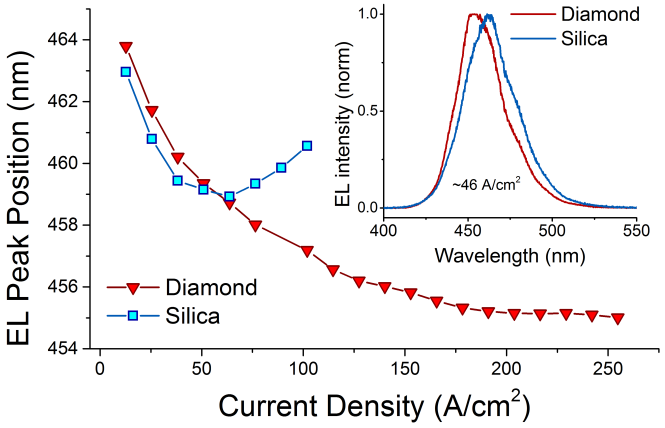


FIGURE 5.3: EL peak shift of representative individual single LEDs as a function of increasing injected current on diamond (red triangles) and silica (blue squares). The inset shows representative EL spectra at 46 A/cm^2 for both substrates.

of the transfer-printed devices shifted over a full range of 464 to 455 nm ($\Delta\lambda$=9 nm) and of 463 to 459 nm ($\Delta\lambda$=4 nm) on diamond and silica, respectively. The corresponding injected current densities ranged from 12 to 100 A/cm^2 for silica, and to a maximum of 256 A/cm^2 for diamond. In the case of LEDs on silica, the peak wavelength blue-shifts

initially, with a reversal to a red shift above 50 A/cm^2 similar in trend to other reports of InGaN/GaN based LEDs [103].

A more complete view of the spectral changes at high drive currents can be seen in Figure 5.4(a) and (b). In both it is possible to discern a fringe structure super-imposed on the main emission peak. These have been reported by others [64, 129, 130] for AlInGaN based LEDs and have been attributed to Fabry-Perot cavity interference fringes. In these plots, both the peak emission and the FWHM points are highlighted to aid interpretation. As initially plotted in Figure 5.3 and further in Figure 5.4, the two devices show distinct

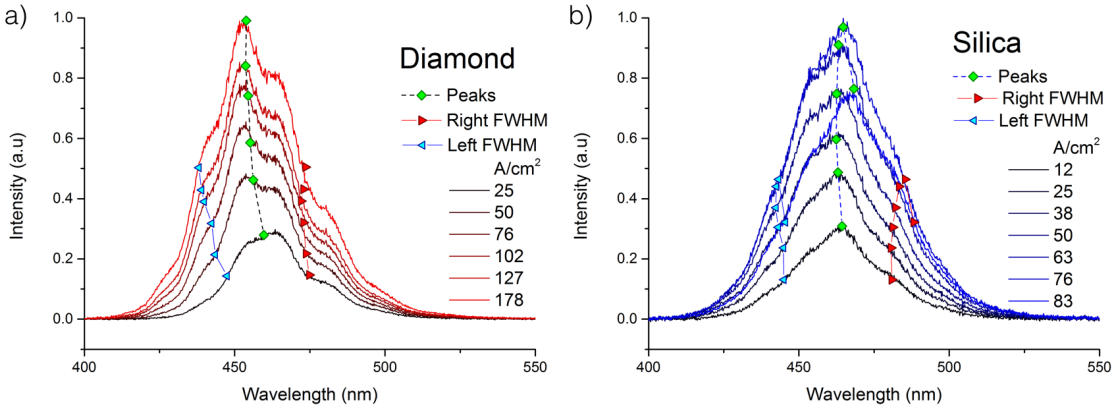


FIGURE 5.4: EL spectra with identified peaks of emission and left/right identifiers of the FWHM at each measured current density for (a) diamond and (b) silica substrates. A similar evolution for the left limit on both substrates is observed and differing evolution for the right limit on the silica substrate forces a red-shift in the emission.

behaviours during operation. On diamond, a predominant blue-shift is observed in the spectra.

The observed blue shift in polar (0001)-oriented device structures, such as those used in this study, can be attributed to carrier screening of quantum confined Stark effect (QCSE) piezoelectric fields in the MQW active region. Though spontaneous polarisations in nitride-based materials exist even in the absence of any external influences (from existing strain or applied electric fields) [131], a compressively-grown strained InGaN layer in the [0001] direction will have the same piezoelectric polarisation aligned with that direction [20, 43]. Considering that the top-side of the LEDs is p-type (Mg-doped) and the bottom n-type, both the built-in field of the LED and the applied bias electric field will be aligned from the grown GaN layers towards the substrate - i.e. in the [000-1] direction. As seen in Figure 5.3 and now Figure 5.4(a,b), with the increase in the applied bias, the initial blue shift is observed due to an opposing compensation of the existing piezoelectric field in the MQW region, an indication that this field was set against the externally applied bias. This confirms the strained state InGaN/GaN MQWs experience and the resulting piezoelectric field pointing from the epi-layers towards the substrate. Since these effects are known to distort the existing energy bands, increasing the external

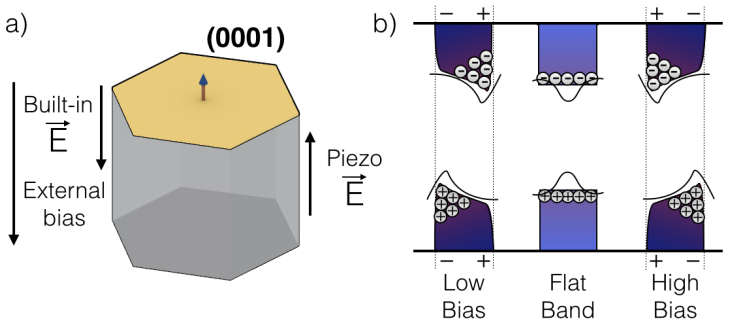


FIGURE 5.5: Visualisation and alignment of competing electric fields in a unit cell with the growth direction (0001) (a). The external bias presumes the p-GaN to be the top layer of the LED. In (b), the different spatial polarisation that MQWs can experience depending on the applied external bias.

bias with an external current source counteracts the internal piezoelectric fields and the carrier screening in its turn flattens the energy bands, effectively generating a larger bandgap - i.e. blue shift - and improving overlap of the e-h wave functions [132–134]. The intermediate stage between the blue-to-red shift where no shift occurs is the point where the external bias is thought to completely compensate the piezoelectric field [43]. The increase of injected carrier density in the LEDs is closely related to thermal effects, due to parasitic resistances of the metals and semiconductor materials themselves and the I^2R dependence of Joule heating [12]. Further increase to the bias brings the bands back to a distorted condition which therefore decreases the existing bandgap [132, 135], although it remains a challenge to fully distinguish which is the predominant effect. Hot injected carriers can carry enough energy to escape the MQW confinement which means the QCSE energy band screening becomes less effective [43, 136]. Localised heating during operation causes strong competitive red shift effects - including bandgap shrinkage - which become dominant at higher injected current densities and due to the device's own self-heating effect [103, 104].

Variations in layer thicknesses are known to cause broadening of the spectra under high-carrier injection with added energy tail-states with lower transition energies. For AlInGaN-based LEDs, the dominant contribution has its origin on the high-Indium (In) content in the MQW layers. Small In-rich clusters can aggregate during growth which may induce deep traps, generating localised exciton-trapping areas (behaving similarly to a quantum-dot) [20, 137–142]. The lower tail-states will be the initially filled with carriers emitting at lower energies (as illustrated in Figure 5.6(a)), as these are more energy-favourable. This effect is screened during high-carrier injection as higher-energy states become filled and begin emitting [105]. This is a significant contributor for the observed blue shift in Figures 5.4(a) and (b) as current increases. Alongside with lower In content regions, band filling effects can introduce powerful blue-shifts to EL emissions of LEDs. Inhomogeneities in the active area, thickness fluctuations, stress gradients

have been studied by Akimova *et al.* [143] and identified as partially responsible for the spectral broadening of EL emissions during high injection currents.

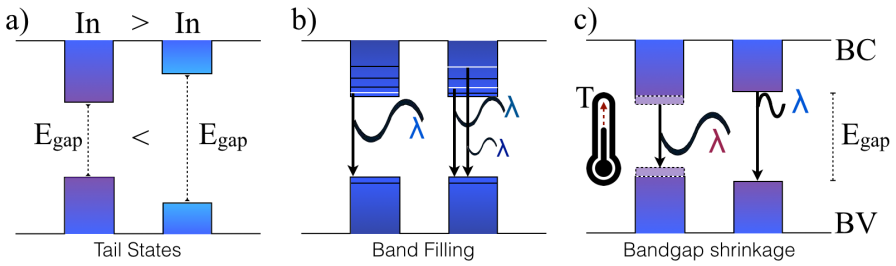


FIGURE 5.6: Additional effects governing LED EL emission. In (a) the existence of tail states due to In thickness fluctuations, in (b) the filling of higher energy levels with increased carrier injection. In (c) a schematic of a thermally-assisted bandgap reduction.

Consequentially, operating LEDs at high-currents generates competing spectral effects mainly due to the ohmic heating of the devices. This is known as thermally activated bandgap shrinkage [144] (as depicted in Figure 5.6(c)). Heating can induce dilation of the semiconducting material lattice and introduce additional (non-radiative) electron-lattice interactions [20, 132, 145]. This is a property inherent and unavoidable to any semiconducting material used in light emitting devices. Increasing the injection current eventually causes the devices EL intensity to reach a saturation threshold. At such point, the non-radiative recombination of the injected carriers starts to overcome existing radiative recombinations - this is known as the rollover point. Radiative recombination can be severely suppressed by non-radiative interactions within the active layers, identifiable by the subsequent major red-shift of the EL peak and typical loss of optical power [145, 146].

The spectral peak shift behaviour of the emission observed for the TP LED devices mimics published results by several groups and is associated with simultaneous multiple competing effects in the active layers [73, 103–106, 145, 146].

Through the light output measurement of the devices, the EQE for each was calculated and is plotted in Figure 5.7. The peak for the EQE for both LEDs is noticed to occur at fairly low current densities (∼15 A/cm^2). Both LEDs then undergo a decrease with increasing current density injection. While with diamond-deposited LEDs, the EQE seems to progress to a lower decay rate as the current is increased, the silica-LEDs EQE decay seems to occur at a constant rate. Due to the poor thermal environment that devices on silica experience, the observed constant rate of decay can therefore be associated with the increase of the LED temperature as these approach their maximum operational current densities (∼80 A/cm^2). Further carrier injection on both substrates highlight the operational limit of the LEDs in their corresponding environments, eventually reaching their limits.

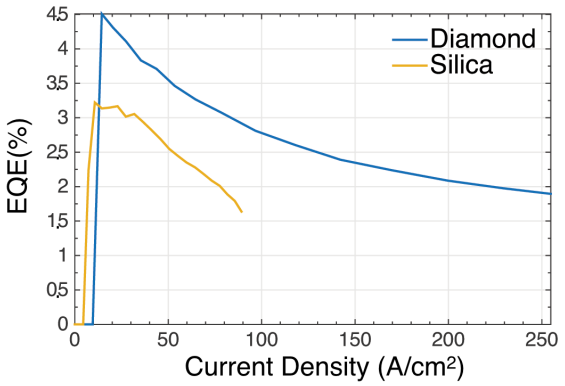


FIGURE 5.7: EQE versus current density for LEDs on diamond and silica substates.

For a comparison with devices on Si (this work was made by Pengfei et al. [51]), the optical power density as well as the EQE was plotted as it can be seen in Figure 5.8. These were circular-shaped μm-sized LEDs that were not underetched and therefore all the epitaxial layers were left on their growth substrate. The calculated EQE for

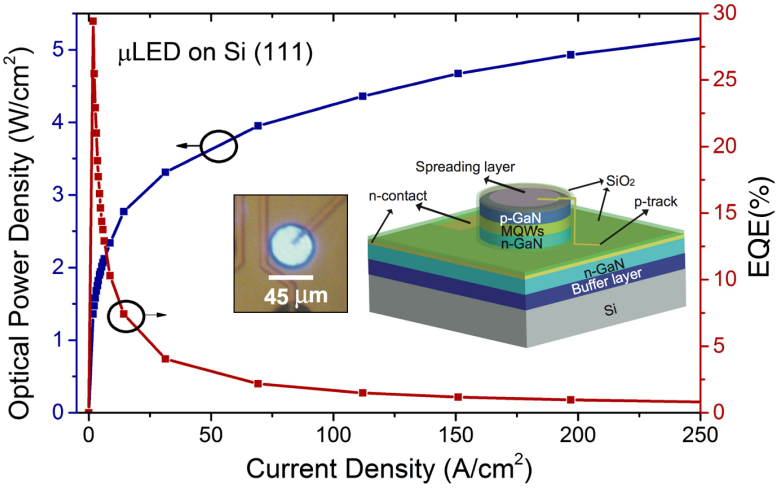


FIGURE 5.8: EQE and optical power density versus the injected current density for devices processed in their growth wafer. From [51].

LEDs kept on their original substrate largely surpasses the one for LEDs during the initial carrier injection though it quickly decays as current density in the active area increases. Considering that devices kept in their original substrates will always have a more perfect bond/interface between layers than devices only bonded by van der Waals forces, this could indicate a limitation of the epilayers. The significant thermal conductivities between the best performing material (diamond) and Si, both devices decay to similar EQE values when passing 50 A/cm^2 of injected current, showing that a better heatsink brings no advantage for the EQE.

For the same current density (and after 50 A/cm^2), devices transfer printed on diamond have displayed higher power densities (nearly twice as much when compared to devices

on diamond in Figure 5.2(b)) although these are qualitative comparisons as the LEDs reported on Si are both in fabricated in a top-emitting configuration and in a blue-absorbing substrate. Both constrain the measurement of the true optical power and respective losses during operation [51]. Nonetheless, Pengfei et al. have shown that these LEDs could be driven up to 7 kA/cm^2 emitting a maximum optical power density of ~8.8 W/cm^2. This shows that the processing of devices for TP doesn't have a significant impact in performance as these can achieve higher optical power with much less current density.

5.3 Thermal Analysis

5.3.1 Pulsed operation

To further explore the operational characteristics of the LEDs and their emission shift with reduced influence from temperature-related effects, they were operated in pulsed driving conditions. The EL emissions were thus measured for both diamond and silica-deposited devices operated at a duty cycle. A duty cycle is defined as $D=\tau/t_0$ where τ is the pulse duration and t_0 the period of the pulse. A 10% duty cycle, i.e. of 10 ms pulse and 100 ms delay, was used to minimise the device self-heating and study the changes in the optical characteristics at high injection currents. The acquired EL pulsed spectra are shown in Figure 5.9. For devices on diamond substrates and in direct comparison with

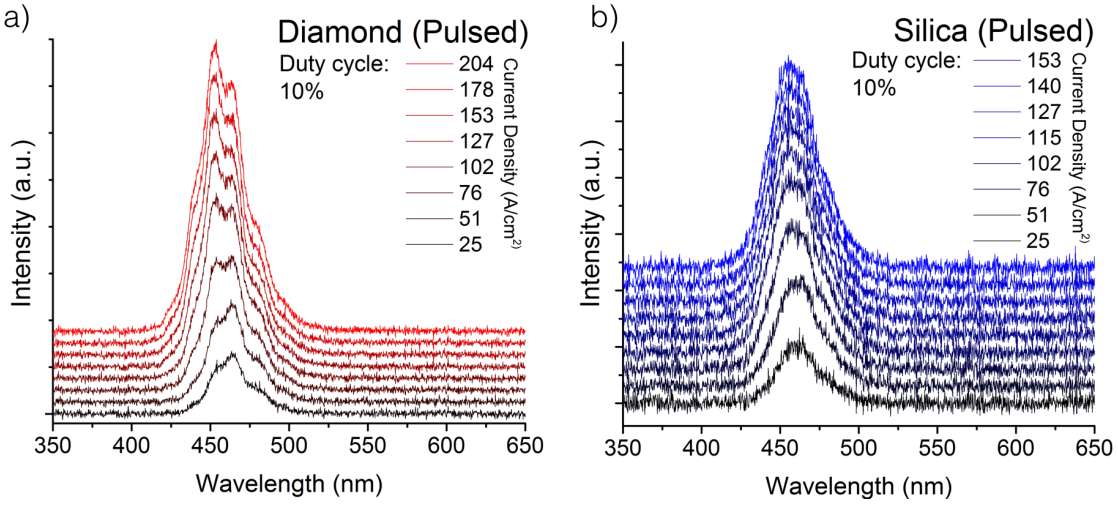


FIGURE 5.9: EL spectra for LEDs TP onto Diamond (a) and Silica (b) substrates during pulsed operation with a 10% duty cycle. The spectra are offset vertically to aid visualisation.

the CW mode shown on Figure 5.4(a), Figure 5.9(a) shows that in pulsed operation little effect is seen with increased current density, as expected due to the remarkable capacity

this substrate has in managing heat. Similar behaviour was observed for devices on silica substrates in both CW and pulsed modes, as it can be compared in Figure 5.4(b) and Figure 5.9(b).

The reduction of self-heating effects by driving the LEDs in pulsed operation mode enabled the devices on silica substrates to operate up to nearly twice as high a current density (160 A/cm^2) then when operated in CW mode (where roll-over was achieved at ∼80 A/cm^2 as shown before in Figure 5.4(b)). The new extended operational regime can be seen in Figure 5.9(b).

For both substrates in pulsed operation, the EL emission peak shift for LEDs on diamond substrates display an expected blue-shift throughout the increase of current injection, which can go up to ∼10 nm (as seen in Figure 5.9(a) and Figure 5.10(a)). LEDs on silica substrates in their new higher-current regimes matched the observed blue shift ∼6 nm (Figure 5.9(b) and 5.10(b)) seen in diamond substrates.

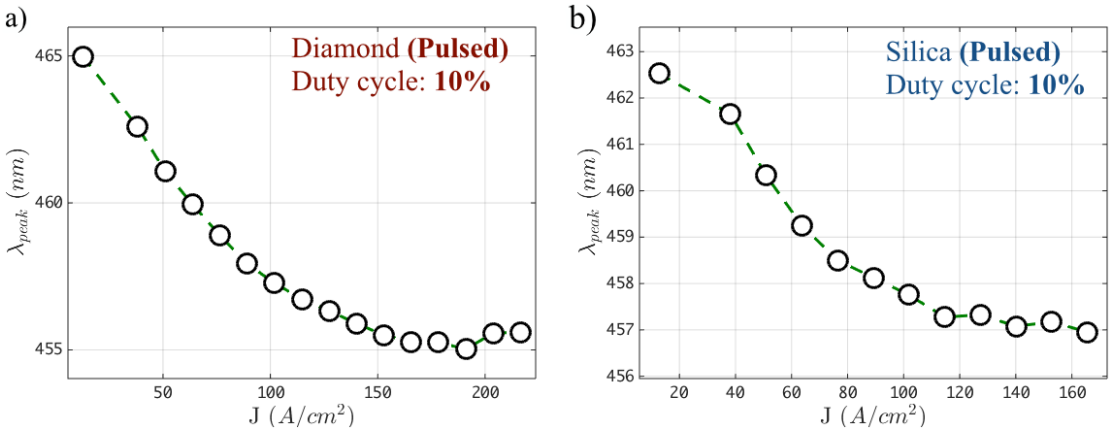


FIGURE 5.10: EL peak wavelength change with increasing current density for a duty cycle of 10% for both (a) diamond-deposited and (b) silica-deposited LEDs.

Due to the new-found regime with pulsed operation, TP LEDs on silica substrates can display equivalent peak-shift behaviour to those TP onto diamond substrates. This is a significant result as TP LEDs in silica can also be driven in pulsed mode at relatively high-currents without significant degradation to their emission properties when compared with TP devices onto diamond substrates. Thus, the use of diamond substrates can be made redundant if devices - depending on the intended application - can be operated in pulsed-mode.

5.3.2 Thermal Camera imaging

To understand how two very different thermal conductivity substrates can affect the device performance, the operating pixel temperature at increasing current densities was

measured with a calibrated infrared-imaging thermal camera (Figure 5.11). Although the camera acquisition was calibrated for the emissivity of GaN-based materials, the images show how a temperature gradient propagates through two distinct substrates. A

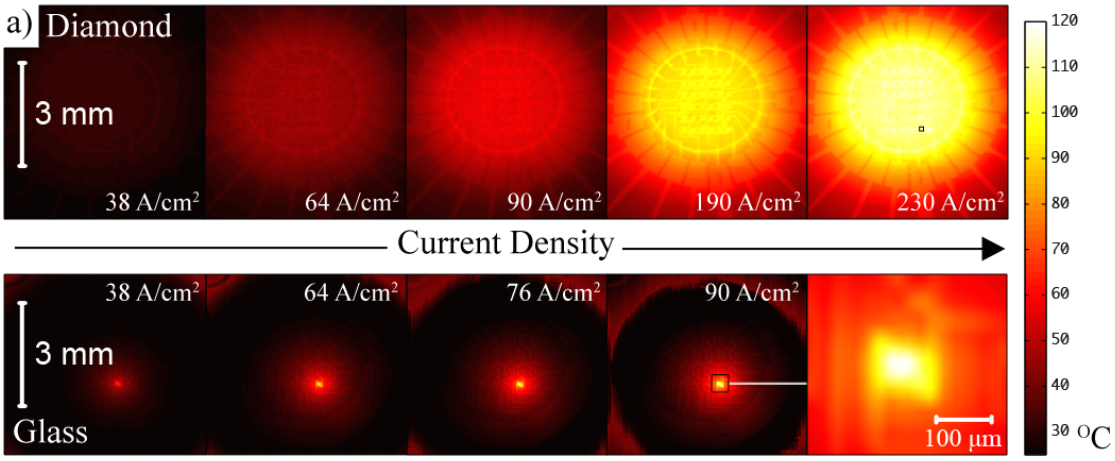


FIGURE 5.11: Thermal imaging of LED arrays with a single device powered on diamond (top) and silica (bottom). The emitting LED is identified in the last diamond frame as a black dot. The last frame of the silica-substrate row shows a magnified view of the die and its metal interconnection tracks. The captured images show the measured temperature corrected for the LED material (GaN); the rest of the image should be interpreted as a relative comparison. A movie of these measurements in real-time can be viewed at [147]

single pixel was addressed in both cases to estimate its operating temperature against the driving current density. With such a high thermal conductivity, diamond acts as a true heat-spreader quickly distributing heat throughout the entire substrate dimensions (3 mm ø). Localised hot spots are not distinguishable since any rise in temperature is quickly diffused throughout the full substrate (Figure 5.11 - top strip). Despite being thin (50 nm Ti + 200 nm Au) compared to the overall device size, the device-addressing metal tracks are known to act as passive heatsinks [63] - with Au having twice the thermal conductivity of GaN - and this phenomenon is visible for both substrates (Figure 5.11). However since the camera is calibrated for the GaN emissivity, this could also be a thermal artefact arising from the metal emissivity and the calibration procedure. Metal tracks on the lower thermal conductivity substrate (i.e. silica), show a higher temperature in the immediate area surrounding the emitting pixel. This illustrates the compromised heat management, generating a high-temperature area in the immediate vicinity of the addressed LED. The challenge of managing heat dissipation on silica becomes an issue since any heat generated is restricted to a smaller area where the maximum operating temperature for the silica (120° C) is achieved at a current density of merely 90 A/cm^2. This is seen in Figure 5.11 (bottom strip) and Figure 5.12. To reach an equivalent temperature, pixels deposited on diamond can be operated up to 230 A/cm^2, an operating current 2.5 times higher. The measured temperatures at the different current densities show a steeper

temperature rise on silica substrates as expected, with diamond providing a much wider operating current range (Figure 5.12). The fitted lines and resulting equations show

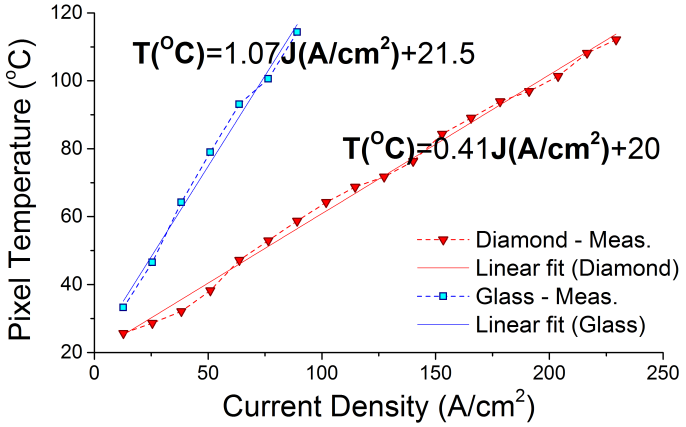


FIGURE 5.12: Measured dependence of LED temperature on the injected current density.

that a device on silica heated up to ∼110 °C at half the injected current density when compared to its diamond counterpart during dc operation. These temperature values are in accord with other results in the published literature [58, 73, 74, 104]. Note that no heatsink was attached to either substrate in these demonstrations. Therefore the further improvements expected for diamond when the heat is not only spread but extracted are yet to be demonstrated.

5.4 Bandwidth measurements and data transfer

The use of LEDs for data transmission has been around for a few decades now. Low-cost IR LEDs have been commonly used for low-bit rate communications (at up to ∼155 Mbit/s) from short distances up to a few km. Free-space indoor communications using arrays of GaAs-based LEDs has been demonstrated successfully and these have also proven reliable when coupled with polymer-based optical fibres (POF) for short distance (∼10's m) guided wave communications [148, 149].

With the lighting industry evolving towards LED-based solid-state-lighting, there is now the possibility of visible light communications (VLC), where the LED lighting fixtures can also be used for optical wireless data communication. Here, micro-LED GaN devices can be advantageous. The combination of LED die sizes 10-100 times smaller in area than those of typical commercial GaN-based devices and their ability to sustain high dc current densities has facilitated high modulation speeds (>1 Gb/s) [128, 150]. Given

the current densities shown for TP GaN LEDs on diamond, this further encouraged the study of their performance under fast modulation.

To measure the bandwidth capabilities, the LEDs were electrically driven by a mixed signal containing AC and DC components. A schematic of the experimental setup to measure the LEDs bandwidth can be seen in Figure 5.13. As illustrated, the DC component was introduced by a typical DC power source and the AC component added by a network analyser system. The AC component consisted of an added fixed-amplitude sine wave with a linear frequency sweep (i.e. chirped). Both components were combined with a typical three-way terminal bias-tee. The LED optical output was focused on the active area of a fast photodiode receiver (with a >1 GHz bandwidth). The AC-coupled output produced by the photodetector was fed back to the network analyser which recorded the amplitude of the electrical input from the photodiode as a function of frequency, thus enabling the comparison of the original AC signal to the frequency response of the LED. Since electrical power is proportional to the the electrical current squared, (I^2),

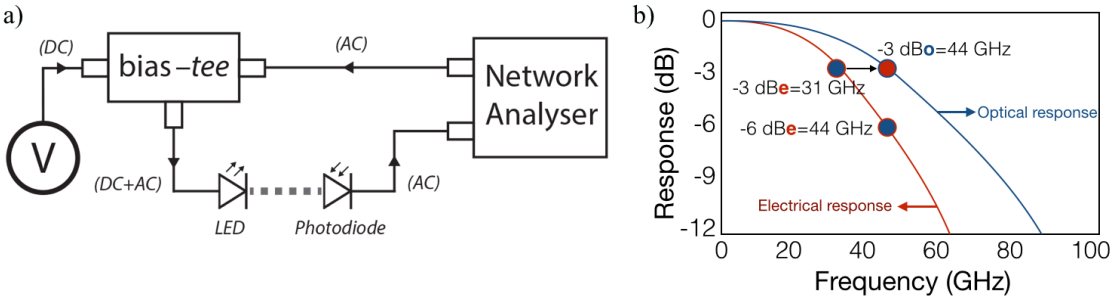


FIGURE 5.13: Setup configuration for BW measurements a). The distance of the LED to the photodetector is ∼1 metre. In (b), the relationship between both optical and electrical spectra can be seen. From [151]

the measured electrical power output from the photodetector is also proportional to the square of the micro-LED output power. Thus, electrical-to-optical (E-O) modulation bandwidths (BW) are conventionally measured using the optical -3 dB criteria, where the measured optical power becomes half its initial value (i.e., the optical -3 dB data point is equivalent to the -6 dB electrical point [151]).

A small LED size naturally enhances BW capabilities by minimisation of capacitive contributions. As the injected carrier density increases, however, it is accompanied by a significant increase in BW with current density which has been attributed to a reduction in differential carrier lifetime [128]. Figure 5.14 shows the initial increase of BW with current density for devices on both diamond and silica. Devices on both silica and diamond displayed similar performance for current densities under 50 A/cm^2. Above this point roll-over became evident for devices on silica, which are thus limited to a maximum BW of ∼55 MHz. The BW of devices on diamond continued to increase at much higher current densities, up to a plateau at 200 A/cm^2, showing a maximum BW

of 154 MHz. These maximum observed BW values establish a performance benchmark for transfer printed devices for optical communications, that could be further improved by fabricating smaller LEDs for use in the TP process [73].

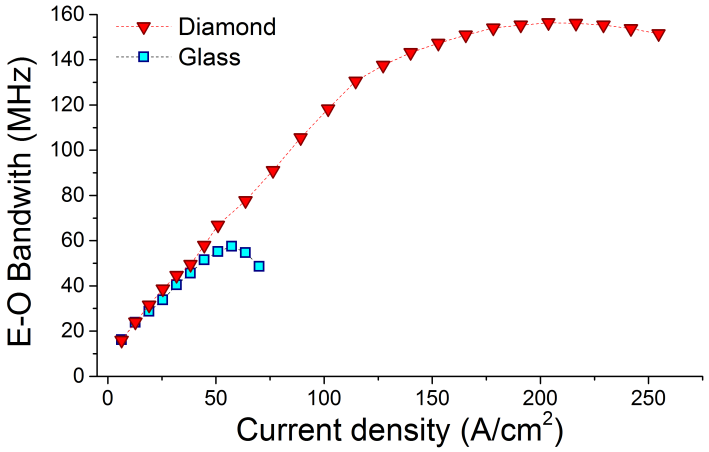


FIGURE 5.14: E-O modulation bandwidths as a function of dc drive current density of representative GaN LEDs deposited onto diamond and silica.

Interesting comparisons can also be made between the results in Figure 5.14 and previous BW measurements on micro-LEDs fabricated from similar epitaxial material, but tested when still on their Si growth substrate [51]. These were circular in shape and of 45 μm diameter. The previous non-transferred devices attained BWs of 190 MHz at relatively low current densities around 6 A/cm^2. However, they displayed an unusual temporary saturation of bandwidth increase in this current density range, before moderate further BW increases at higher current densities attributed to heating effects and associated lowering of series resistance [51]. The smoother initial BW increase with current density shown by the transfer-printed devices resembles typical results from conventional GaN-on-sapphire devices [128]. These observations suggest that alteration of the strain state of QWs by removal of the Si substrate may influence the recombination dynamics of carriers significantly.

To further demonstrate the potential of the transfer-printed devices for VLC, tests were made of the optical transmission of data. For these measurements, the LEDs were probed with the setup shown in Figure 5.13(a) with their optical emission equally acquired by the photodiode as discussed in section 5.4. The DC current was mixed with an AC on-off keying modulation signal, although in this case the AC signal was a pseudo-random bit sequence (PRBS) of 2^7-1 bits provided by a bit error rate test (BERT) system, which introduced a peak-to-beak modulation of 2 V. The DC current density provided to the LEDs was 128 A/cm^2 and 73 A/cm^2 for devices on diamond and silica respectively, well within the high-current injection regime for both devices. Lower currents inhibit

data transmission at elevated data rates due to the slower response of the LEDs in a low current regime [12]. The opposite can also be expected for LEDs in poor thermal environments (such as silica substrates) where over-heating effects would imply device degradation and failure in the most extreme cases.

The eye-diagrams in Figures 5.15 and 5.16 provide a visual representation of the received signal and give an idea on the quality of the signal, the noise and how *good* the 'open eye' is, an indicator of error-free transmission. Devices on diamond displayed open eye diagrams

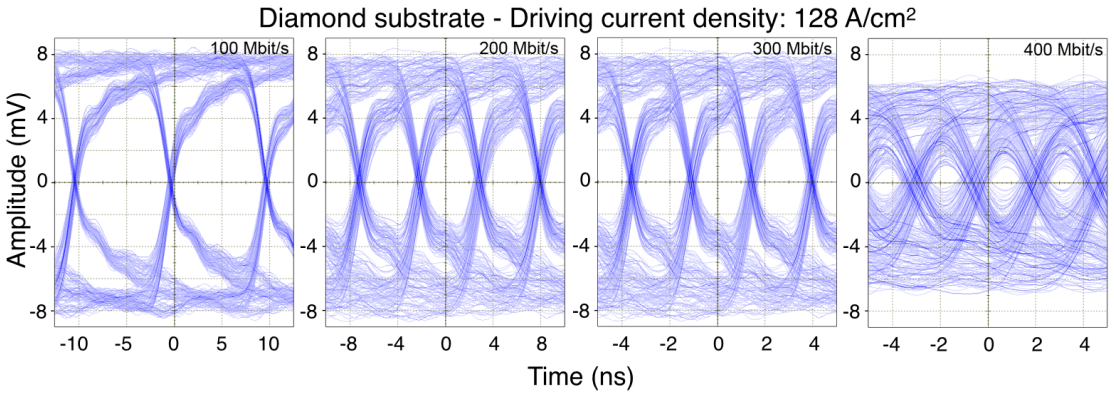


FIGURE 5.15: Eye diagrams from TP LEDs on diamond substrates. The LEDs were driven at 128 A/cm^2 with a PRBS length of 2^7-1 bits. Open-eye diagrams were obtained for multiple bit-rates, ranging over 100, 200, 300 and 400 Mbits/s.

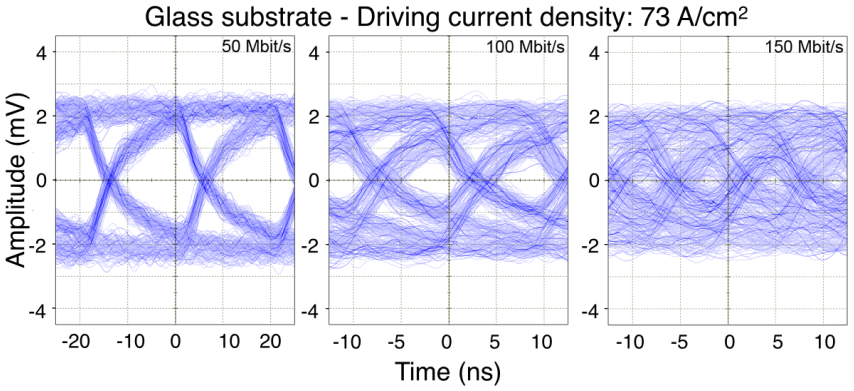


FIGURE 5.16: Eye diagrams from TP LEDs on silica substrates. The LEDs were driven at 73 A/cm^2 with a PRBS length of 2^7-1 bits. Open-eye diagrams were obtained for 50 and 100 Mbits/s, although the data stream was not error-free at 150 Mbits/s.

at data-rates up to 400 Mbit/s, correlating with error-free data transmission. In contrast, devices on silica showed eye closure above 100 Mbit/s, which was virtually complete at 150 Mbit/s. The superior performance of the devices on diamond is again ultimately attributable to this material's effectiveness as a heat spreader, allowing operation of the LEDs at higher dc current densities.

5.5 Colour conversion with II-VI semiconductor materials

As mentioned in section 4.4.6, applications of GaN devices can also benefit from the integration of colour converting/mixing materials. Possible uses include full-colour micro-displays and/or multi-wavelength or white visible light communications. II-VI compound semiconductors offer versatile colour converters for use with III-nitride semiconductors [152]. Epitaxially grown II-VI CdMgZnSe MQW membranes were therefore used as a demonstrator to show the integration of a blue LED with a green emitting colour converter. These II-VI membranes can be wet-etched down to the active region, discarding their growth substrate and typical buffer layers and can be engineered during growth to cover the entire visible spectrum, offering a promising approach to white-light generation.

The used II-VI semiconductor structure design contains a total of 9 QWs and Figure 5.17(a-c) shows the designed platelet structure and composition. These were provided by Maria Tamargo's group in the City University of New York (CUNY) in collaboration with Brynmor E. Jones, from the Institute of Photonics. The used materials were optimised for optically-pumped laser action rather then LED colour conversion, but nonetheless allowed a simple proof of concept demonstration to be undertaken. The etched material platelet

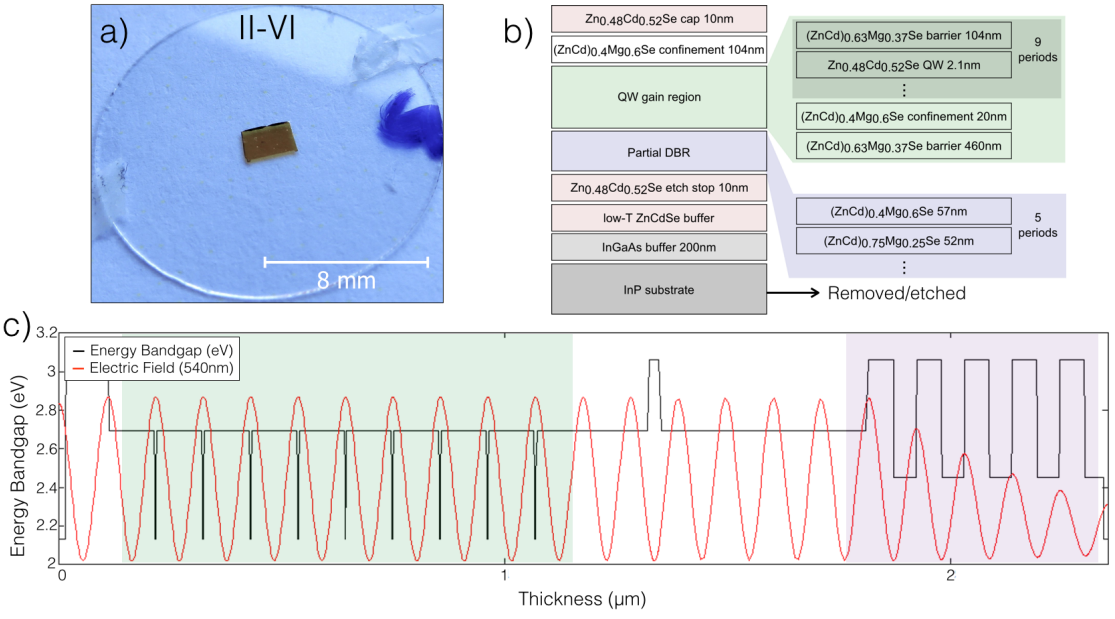


FIGURE 5.17: II-VI platelet capillary bonded to a glass substrate a), in b) the layer composition: 9 QWs and a partial 5 period distributed Bragg reflector (DBR) to aid in setting the electric field in anti-node positions. Any residual pumping is absorbed by the lower 2.5 eV bandgap material within the DBR, contributing to non-radiative recombination by generating heat (c).

was capillary bonded to a thin glass slide and placed in direct contact with the emitting side of the fabricated device containing TP LEDs on diamond substrates. To ensure the illumination as much of the platelet as possible, one of the 2x2 arrays of TP LEDs

devices was used. Figure 5.18(a) shows the J-V and J-L curves of these pump arrays. The four pixels were operated simultaneously at their peak optical performance (63 A/cm^2) and the resulting combined maximum optical power was ∼18 W/cm^2. The J-L curve displays a slight saturation at the highest current density, a factor that is confirmed by the EL emission spectrum in Figure 5.18(b), where a loss in the emission peak intensity is observed. Several tests with AlInGaN LEDs on sapphire (∼40 W/m.K) substrates with matching sized pixels performed by our group showed that for spacings between pixels higher than one pixel size (i.e. 100 μm), the heating of each device is independent and does not generate visible temperature overlap on its immediate neighbours. For the devices in this architecture (full-details given in section 4.1), pixel spacing is much larger than one pixel size (340 μm horizontally and 240 μm vertically). The considerable

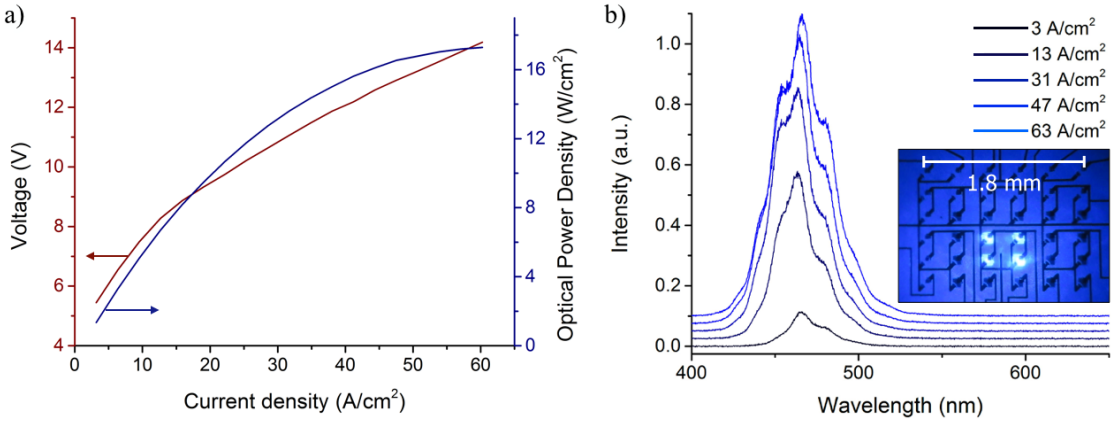


FIGURE 5.18: Comparison of J-V and J-L curves (a) of a 2x2 TP LED array used as an optical pump source, deposited on diamond substrate. In (b), the spectral evolution the EL emission for different current densities. The inset shows the pump devices under operation.

difference between diamond's thermal conductivity and that of sapphire generated heat can definitely act as a shared limiting factor for both the limited optical power as well as the observed spectral behaviour. While the heat spreading capabilities for one single pixel under operation are beneficial, this can be undesirable for multiple pixel operation. This was also something clearly visible in Figure 5.11(a) where for a single LED was being operated, the high-effectiveness of diamond's heat conduction meant that neighbouring pixels would be exposed to nearly the same temperature as the powered LED despite being in an off-state. This imposes a significant limitation on how hard the devices can be driven with a shared heatsink. At the driving current density (63 A/cm^2) at which the array is being operated, a saturation of the optical power is seen in Figure 5.18(a) with the EL emission confirming thermally-assisted degradation effects and intensity loss (Figure 5.18(b)). This hints at an overlap of the temperature gradient created by each LED which can artificially increase the temperatures that devices are experiencing

during operation. To avoid damage to the device, it was chosen not to drive devices past this current density.

The EL emission was acquired similarly to previous experiments using a fibre-coupled spectrometer perpendicularly to the emitting surface and centred on the II-VI platelet area (the fibre tip can be seen aligned to the surface in the inset of Figure 5.19(a)). The setup order was as follows: 4xTP LED/II-VI platelet/optical spectrometer (0.5 cm separation). The measured EL emission can be seen in Figure 5.19(a) where the LEDs were driven up to 63 A/cm^2. To aid visualisation, each individual emission intensity is normalised. As shown in Figure 5.19(a), the absorption of the barrier material (pink dashed line) is low at the LEDs emission wavelength, which means that most of the light generated from the LEDs is not being absorbed. Any light passing through the

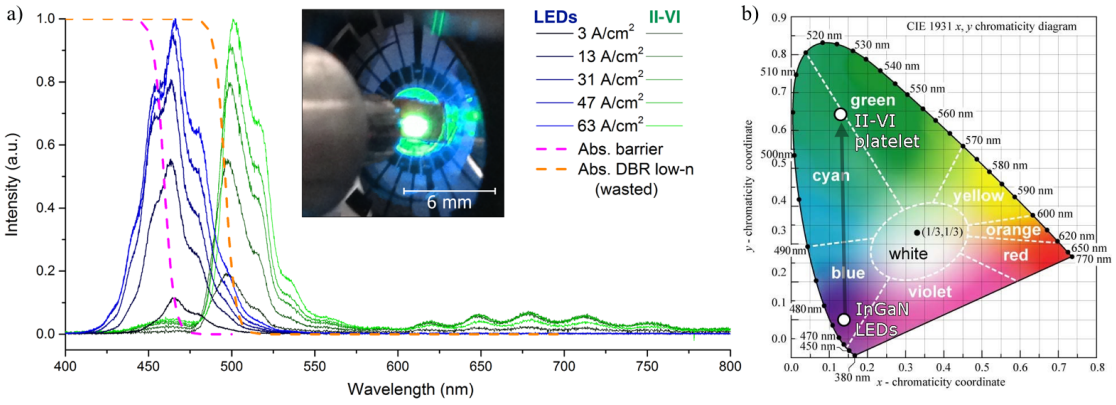


FIGURE 5.19: Colour conversion examples using a II-VI platelet: in (a) the EL emission of the LEDs (blue) and II-VI platelets (green) are shown overlayed. The LED-to-II-VI emission peaks are all shifted towards lower energies by ∼34 nm. In (b) the CIE 1934 diagram shows the shifting of the emission from the the InGaN LEDs used to the new emission when overlayed by the II-VI platelet.

barrier material is subsequently absorbed by the low-index (n=2.5) DBR layer at 2.5 eV (orange dashed line). Any light absorbed in the DBR is wasted and generates heat, which, since the platelets were not optimised for these pump wavelengths, will result in low green emission (less than 50% of the light gets absorbed by the QW region). At the low-energy region of the spectrum, five distinct residual broad peaks can be seen in which their intensity is reduced with increased optical pump energy. These are thought to be luminescence peaks from the ZnCdSe capping layer (positioned at 2.13 eV or 666 nm) and their broad nature may have its origin in the peaks being modulated by reflections of the existing DBR region.

We have shown elsewhere that II-VI platelets can be fast modulators when pumped with LEDs on sapphire. Green emission was modulated up to ∼145 MHz and shown to be limited by the modulation speed of the GaN pump LED used [127]. As the silicon-grown and transfer-printed LEDs used here have shown for equal current densities to outperform

their sapphire counterparts in terms of E-O bandwidth (Figure 5.14), this illustrates a promising prospect to integrate colour converters onto GaN-based LEDs for VLC applications.

The overall shift in the perceived colour can be seen in Figure 5.19(b) on the CIE 1931 diagram. CIE chromaticity diagrams are widely used as a tool to aid the visualisation of how the human eye perceives colour - the gamut of human vision - with a given emission spectrum. Here, near the region of x,y=(0.14,0.05) is represented the colour perceived by the human eye by the emitting spectrum of the unfiltered InGaN LEDs (with a peak emission at 465 nm). Correspondingly, near the chromaticity coordinates x,y=(0.13,0.64) with the main peak emission measured at 502 nm is the filtered emission of the LED light passing through the II-VI platelet.

5.6 Colour conversion with III-V semiconductor materials

To further continue the study of colour conversion using optically pumped semiconductor platelets, III-V compound semiconductors were used in an equivalent way as described previously in section 5.5. Epitaxially grown III-V AlInGaP MQW membranes were capillary bonded to glass substrates (as seen in Figure 5.20(a)) to be used as a demonstrator to show further integration of a blue LED with a red emitting colour converter. The processing of these platelets is similar to its II-VI counterparts where the membrane can be wet-etched down to the active region, resulting in the release of their growth substrate.

The used III-VI semiconductor structure contains 6 QWs and Figure 5.20(b) shows the designed platelet structure and composition. These were grown by Dr. Andrey Krysa's group from the University of Sheffield. These materials were optimised to be optically pumped with an absorption ∼450 nm and the QWs engineered to emit ∼630 nm. To optically pump the epistructures, a 2x2 array of LEDs on diamond was also used.

The normalised emission intensities can be seen in Figure 5.21. The LEDs were driven up to 127 A/cm^2 and the emission going through the platelet was measured centred at 468 nm. A faint emission peak is observed around 650 nm as shown on the inset of Figure 5.21 (red lines). The significantly low intensity can have its origin from multiple effects, most significantly during the wet processing. After the release of the membranes from their growth substrates and capillary bonded to the glass slides, cracks/fractures are observed as well as uneven bonding areas, all of which can be caused by significant strain relaxation of the epistructure and cause severe degradation of the membrane performance. Also, significantly, upon release from their growth substrates and buffer

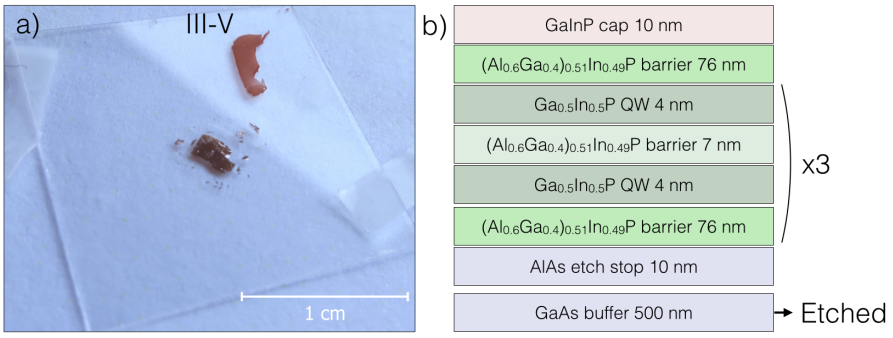


FIGURE 5.20: III-V semiconductor platelet capillary bonded to a glass substrate (a). In b) the structure is comprised of 6 QWs between two barrier layers and an etch-stopping layer.

layer, the platelets are only ∼370 nm thick which may also be insufficient to efficiently absorb the a significant portion of the incident light from the LED pump source.

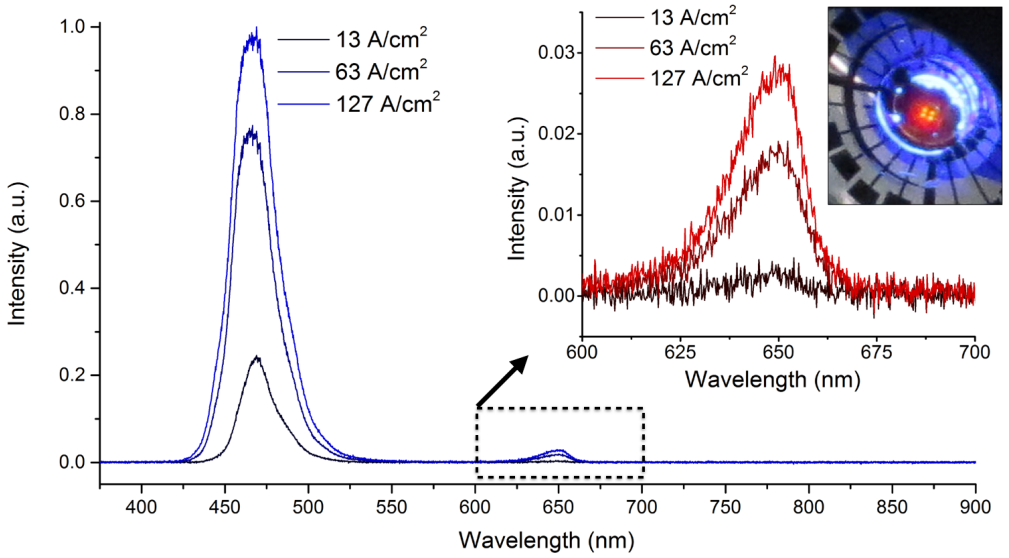


FIGURE 5.21: Colour conversion example using a III-V platelet. The EL emission of the LEDs and the platelets (blue) is shown. The inset shows a magnification of the area where a red emission peak is observed at significant low intensity. An image of the platelets being optically pumped by the LED array is shown.

While for the naked eye and as imaged on the included photograph in Figure 5.21 there is perceptible colour conversion, the change on the CIE chromaticity diagrams is barely perceptible due to the significant differences in intensities of the two observed emission peaks.

Nonetheless, a demonstration of the use of TP LEDs for colour conversion purposes has been shown and the fast modulation speeds for II-VI and III-V semiconductor platelets as well as their reliability have shown great potential to be used for both colour conversion and fast bandwidth modulation for visible light communications [127]. New colour converters containing with ZnCdSe strained QWs can be used for the complementary

red light emission [153] and are being studied. Due to the nature of TP as an additive manufacturing technique, the straight-forward integration of LEDs with pixel-matched colour conversion material for the use of white-light, displays, and other novel applications should be exploited further.

Chapter 6

Conclusions and future work

The work presented in this thesis focused on the heterogeneous integration of GaN LED devices onto a wide range of substrates. The most significant development was the implementation of ultra-high-accuracy and high-throughput Transfer-Printing capabilities using an adapted nano-lithography system. This built on the elastomeric stamps with reversible adhesion approach pioneered by Rogers, but has introduced new performance capabilities. Furthermore, it was shown that polymeric adhesion enhancement layers normally used in such applications can be discarded for successful transfer printing, opening up new structural assembly capabilities and new performance regimes.

Chapter 1 provided a general introduction to LED properties and characteristics, in particular those based on III-nitride materials. The operating principles of electrically addressed LEDs were described together with the physics of the P-N junction and the improvements that quantum well structures bring to boost device efficiencies. The characteristics of III-nitride material-based alloys were also presented. This material system has shown to be extremely versatile as it can cover the entire range of the visible spectrum with appropriate compositional changes. The growth of polar III-nitride semiconductors was described and tensile and compressive strain effects were discussed. The growth of the epitaxial layers for this work was performed on Silicon wafers, thus the relevant growth challenges were discussed. Due to the significant lattice mismatch of the epitaxial material to the substrate, several undesired effects (meltback etching, cracking, severe wafer bowing, threading dislocations...) can affect the material growth and result in poor LED performance. The efficiency droop mechanism was also introduced. The carrier recombination due to lattice-defects, Auger recombination and electron leakage are amongst the possibilities causing this effect. Chapter 1 finished with a brief state-of-the-art summary on what has been reported and achieved in relation to the transfer printing of LEDs onto foreign receiving substrates.

For the development and implementation of the reported transfer printing capabilities, a wide range of experimental techniques were used in a cleanroom environment. Chapter 2 described these techniques. Suspended LED arrays were fabricated by multiple wet and dry processes which revolve around the three main steps of photolithography: patterning, exposure and development. Several procedures to etch different materials as well as deposition were described. Since one of the main techniques for producing suspended membrane-like LEDs is the underetch of the underlying substrate (Silicon), a thorough study on how this material interacts with alkaline wet-etch solutions was described. Also, most importantly, Chapter 2 introduced the mechanics of reversible adhesion, a crucial framework for the fabrication of reliable elastomeric stamps. The adaptations performed to the nanolithography system were also described.

Chapter 3 introduced the entire architecture for producing 150x150 μm^2 LEDs and the corresponding addressing circuit was also described. Initial attempts at addressing the devices with the use of conductive epoxies/ink were detailed and a failure analysis was performed to understand the poor reproducibility and performance of the final devices. Changing to a metal tracks addressing scheme was described as well as the new fabrication method to construct membrane-like mechanically flexible polymer substrates with embedded optoelectronics. The IV and LI characteristics of single LEDs were studied to infer the changes in performance during the most significant processing steps. The transfer printing of devices with a higher level of spatial precision than previous reports by other groups was accomplished and it was found that the remaining limiting factor for the positioning accuracy was the sidewall roughness of the LED membranes rather than the capabilities of the TP itself. The poor performance of the devices in terms of electrical and optical power meant changes to the fabrication procedure were required.

Chapter 4 introduced the necessary steps to tackle the poor performance, with an inversion of the fabrication processes, where the Si underetch was performed first and not on finished devices. The architecture for producing 100x100 μm^2 LED devices in this manner was thoroughly described and the full transfer printing process without resorting to the use of adhesion enhancement layers was introduced. The LEDs were found to be curved due to strain-release of the epilayers upon removal of the underlying silicon substrate. A full study to characterise this curvature was performed using interference ring calculations and backplane reconstruction techniques, and AFM scan and SEM imaging of the outer regions of a TP platelet. Van der Waals force calculations were performed in an attempt to study the bond strength that ensures LED platelets were fixed to their new substrates. To address the difficulties encountered during microfabrication with this new type of material, strain management layers were used both to counteract cracking and to structurally reinforce the suspended epitaxial membranes during subsequent processing

steps. A multitude of completed devices was therefore reported printed onto PDMS, thin flexible glass, thick glass, a DBR mirror, diamond, II-VI and III-V semiconductor platelets.

Chapter 5 makes use of the devices developed and reported in Chapter 4, where in-depth characterisation was performed on the two-better performing substrates (diamond and silica respectively). The change to the architecture of the addressing circuit was described and the electrical and optical performance of devices was discussed. The observed peak shift during high-current operation and temperature increase was studied to infer the different phenomena influencing the LED emission. Thermal analysis (imaging and temperature measurement) was performed with the use of a thermal camera and further experimental measurements with the LEDs in pulsed-mode operation were performed. Owing to the extended current-injection capabilities that LEDs on diamond and silica were capable of, bandwidth studies and colour-conversion tests were performed as a brief demonstration of some of the capabilities of TP LEDs.

6.1 Future Work

In terms of future prospects for the TP of LEDs and other devices/materials onto new receiving substrates, one should take advantage of the innovative capabilities that TP offers for device integration. As an additive fabrication technique, in particular without the requirement of adhesion enhancement layers as demonstrated here, new forms of mechanical stacking and assembly became possible.

The use of smaller sized LEDs will offer significant advantages, supporting higher current densities and emitting at higher optical power densities. As imaged in Figure 6.1(a-c), the underetch of 50x50 μm^2 LEDs has been demonstrated already, requiring only further optimisation of the elastomeric stamps required for TP. As previously reported

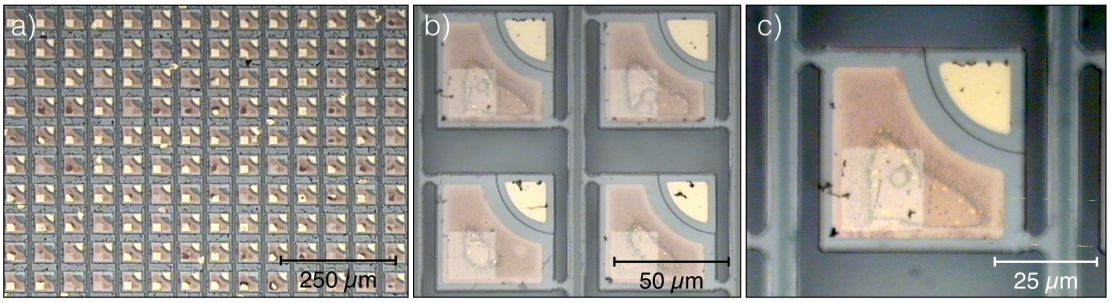


FIGURE 6.1: Underetch of 50x50 μm^2 LEDs at different magnifications: in a), an overview of part of the array, in b) a magnification showing a 2x2 array of suspended devices and in c) an individual suspended LED.

in section 5.4 and in comparison with larger LED sizes, the use of smaller pixels enables

their modulation at higher speeds, ideal in their use for applications in visible light communications. LEDs with microscale lateral dimensions can be attractive to a wide range of other applications as well. However, further reductions in pixel-size (below 50x50 μm^2) become increasingly challenginf on both LED fabrication and that of the corresponding elastomeric stamp. Strain-related effects and micro-cracks on the LEDs are more severe at smaller scales, where the use of (thicker) strain-management and structural reinforcement layers had to be used in order to achieve successful fabrication. One of the major difficulties comes from the limits on producing suitable elastomeric stamps. The aspect ratio of the stamps' post height has to be carefully tailored to ensure a reliable SU-8 patterning and development. At this scale, ensuring the full development of the posts becomes challenging as the existence of small pyramids causes further issues on developing the photoresist. The active area can be tailored to be as small as the available photolithography bench tool allows, within a base-platelet size. This might further aid heat-management for TP devices, however with a significant amount of unused material area. This configuration is ideal for wide-device spacing (and is also flexible substrate-compatible) but it is not suitable for high-density placement of devices.

The implemented TP technique combined with reduction in the LED sizes make the use of TP LEDs promising for integration and application in neural optogenetic probes. A layout of such probes, fabricated without TP, reported by McAlinden *et al.* [154] is shown in Figure 6.2(a-c). Optogenetics as a technique makes use of light-sensitive proteins to control neural activity. These proteins create action potentials in mammalian neurons when activated with 460 nm light. This wavelength range is well within the emission profile reported by the TP LEDs in this thesis (∼468 nm). Pixel size reduction

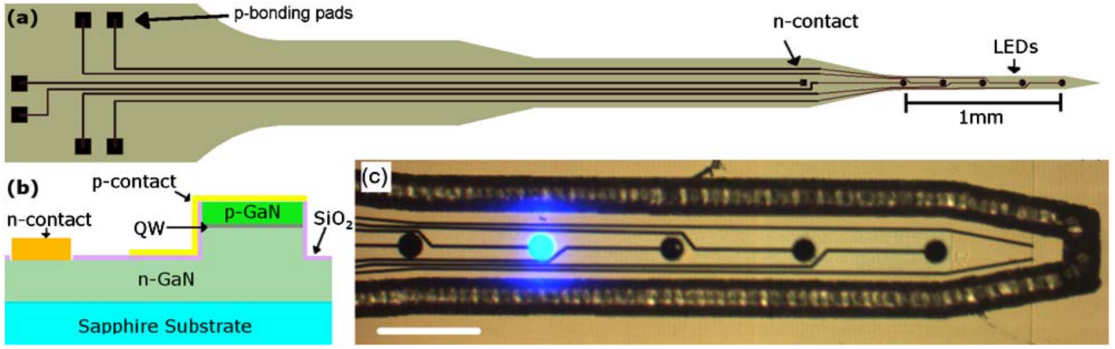


FIGURE 6.2: A layout of an optogenetic probe in a) showing the electrical contacts to address the LEDs at the tip, in b), a cross-sectional schematic of the fabricated devices comprising the substrate and epilayers, in c) the tip of the five LEDs with an individual LED powered on. From McAlinden *et al.* [154].

for TP LEDs is crucial if it is to be used for these applications as this can enable the use of more light sources per probe and/or create probes at smaller scales which then become less intrusive to the brain's soft tissue. Due to to the nature of TP, and

since the current limitation on the number of LEDs per probe is the metal contacts, LEDs can be deposited on both top and bottom surfaces of the probes and be addressed independently. The slightest local temperature variation can adversely affect the neuronal activity so LEDs during operation should not heat the neuronal tissue by more than 1 °C. While it has been shown in McAlinden's work that μLED probes can be produced to limit the local temperature increase to ~0.5 °C, increasing the power applied to the LEDs quickly reaches the allowed temperature threshold. The work developed in this thesis has shown that LEDs can be TP to virtually any substrates, which means that the use of heat-efficient substrates such as diamond for optogenetic probes is at hand which can further improve the required thermal management to least perturb any brain functions. A schematic of an optogenetic probe concept is shown in Figure 6.3 containing transfer printed LEDs on both sides of the substrate. Combined with the

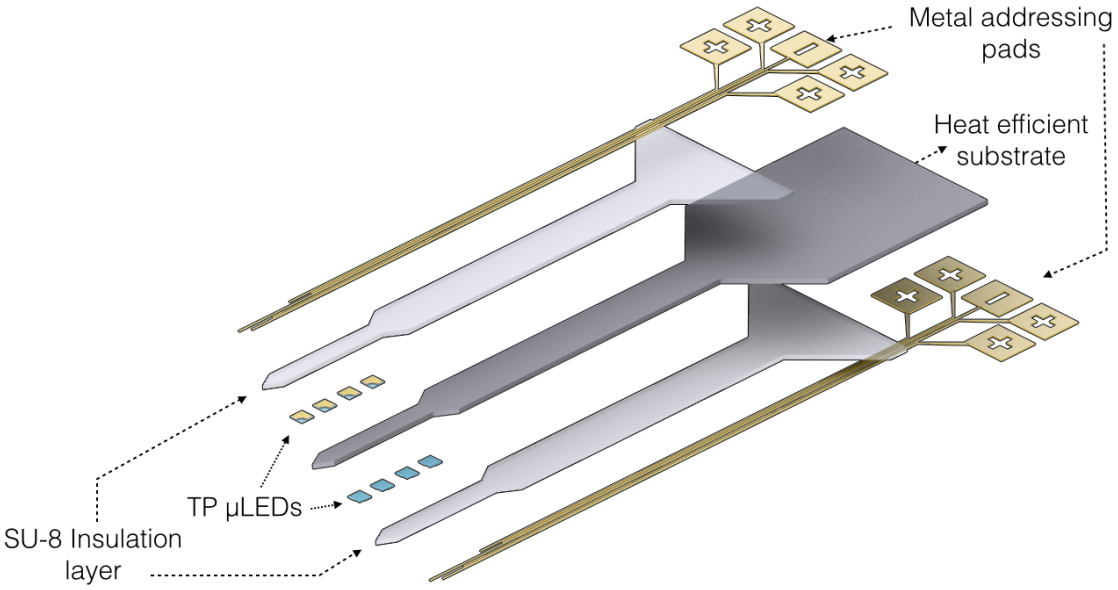


FIGURE 6.3: An exploded layout of an optogenetic probe with lights sources on both sides of a heat-efficient substrate, enabled by the TP technique here reported.

nanoscale precision reported in Chapter 3 for precise pixel placement and the developed heat-efficient architecture in Chapter 4, both developments aid in heat management as the use of the top insulating layer (comprised of a layer of SU-8 photoresist) means the epi-layers - which are the source of the generated heat - are thermally insulated from the neuronal tissue. Thus, TP LEDs on high-efficient thermal substrates should enable the use of higher levels of power with reduced thermal drawbacks.

The use of thermal-efficient substrates becomes of interest where the target applications require high-optical power. As shown in Chapter 5, for high-speed VLC data transmission, the use of LEDs requires driving these at high injection current densities. The work undertaken has shown the performance of a single TP LED for this purpose, reaching transmission rates up to 400 MBits/s. A method to increase significantly the bandwidth

capacity is through the use multiple-input multiple-output (MIMO) spatial multiplexing. The idea behind MIMO focuses on the modulation of individual LEDs simultaneously for a high-speed parallel wireless data transmission. To address multiple LEDs for this purpose, the use of complementary metal-oxide-semiconductor (CMOS)-controlled LED arrays has been reported by our group [128, 155]. A CMOS driving board enables easy modulation of the LEDs via a computer interface and with TP onto CMOS as an integration technique, individual LEDs can be precisely positioned for high-density integration.

The TP of LEDs onto 'light enhancing' substrates has also been shown in Figure 4.16(e) in Chapter 4. The use of Resonant-Cavity LEDs (RCLEDS) has been developed since the early 1990's [156] which makes use of a microcavity to enhance the spontaneous emission properties, intensity and spectral purity of the emitted light. An RCLED consists of a resonant cavity with a thickness in the order of the emitting wavelength enclosing and an active layer with its corresponding MQWs. Light generated by the LEDs confined between the two mirrors makes up a Fabry-Perot resonator where both constructive and destructive interference occurs, altering the original LED emission properties. With an appropriate cavity design, the preferential propagation direction for the photons can be forced from total internal reflection and towards the existing light-extraction cone, thus significantly improving the extraction efficiency. Using TP as a technique to create RCLEDs through mechanical assembly means cavities no longer need to be grown as part of the epistructure. Since multiple LED types (i.e. different materials, different MQWs configurations) can be sourced from different wafers during TP, a single substrate can now contain a multitude of different resonant-cavites, each with its own singular optical properties.

The development of transfer-printed cavities could also enable the fabrication of vertical cavity surface emitting lasers (or VCSELS). Here, a high finesse cavity can be assembled, possibly including intra-cavity contacts. A schematic for a VCSEL device is shown in Figure 6.4(a). A number of gain layers is represented in Figure 6.4(b). These are usually comprised of MQWs but also layers of quantum dots, can be placed within the semiconductor subcavity to provide gain. An optical standing wave is set up with the MQWs placed at the electric field antinodes for maximum efficiency. This arrangement of the active layers is called resonant periodic gain [157]. TP enables the deposition of wide arrays of materials and/or devices as shown representatively in Figure 6.4(c). Thus a VCSEL device can be comprised of multiple individual emitters which can enable high-power emissions and significantly increase the overall efficiency.

Further integration with optical devices has been shown with the integration of TP LEDs onto the end of a polymer optical fiber (POF). The first demonstrations of optical

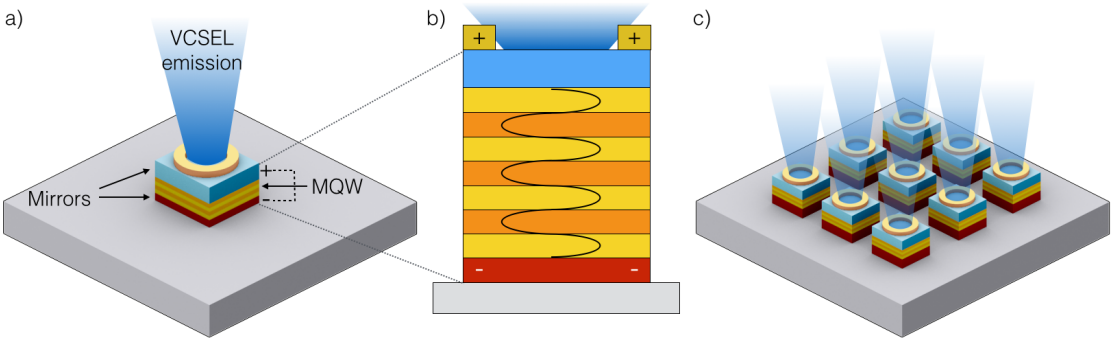


FIGURE 6.4: A schematic of a VCSEL: in a) an example is shown of a TP VCSEL onto a heat-efficient substrate, in b) a magnification of the gain region (resonant cavity) with a representation of a standing wave, in c) an example of an array of VCSELs with the combined emission of multiple devices.

communications using a POF as a propagation medium have been previously shown with the use of micron-size LEDs [158, 159]. The most critical part of the setups used for these demonstrations rely on the precise alignment of the micro-LEDs with the core of the POF to ensure the best possible error-free data transmission. As seen in Figure 6.5, a capillary bonded TP LED was transferred to the core of a POF. The capillary bonding

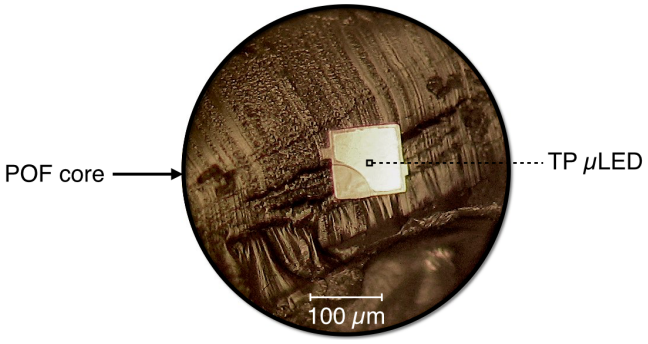


FIGURE 6.5: A capillary bonded TP LED sits on the core of an unpolished polymer optical fiber.

method was the same as the one reported on Chapter 4 and it is possible to see from Figure 6.5 the versatility of capillary bonding LEDs even on extremely rough surfaces, as the core of the fibre was not polished for the first initial attempts. The capabilities shown pave the way to use integrated light sources directly on the transport media, making the use of alignments stages during operation redundant.

One of the most significant results obtained is the way a shared heatsink influences neighbouring LEDs (even in their off-state) due to the induced temperature increase. This does not become significant unless LEDs are driven in their high-current regime, where neither good or poor heat-conductive substrates will make a difference if multiple pixels are addresses simultaneously. The additive nature of transfer-printing should play a role to circumvent this issue as LED-size tailored heatsinking platelets can be used

to assist the heat management of the emitting pixels. The laser or saw-dicing of small diamond or silica platelets can be performed to be initially deposited onto new substrates. Since these are to act as a heatsinking layer, they can be easily deposited onto adhesion enhancement layers. This ensures heat-generation from the LEDs will be transferred to this underlying platelet, while the deposition of the platelets onto adhesive layers will contribute to insulate each pixel from neighbouring influences. This also paves the way to have some form of heat management onto flexible substrates as the methods here reported (via shared heatsink) are not compatible with flexible-substrates.

A further area of improvement for the capillary bonding method is to resort to the use of microfluidics systems. A fluid well and a microfluidic needle-inspired injection system was designed to optimise the way LEDs are wetted on their backside, here illustrated in Figure 6.6. Different supporting configurations were made as to see which yielded the

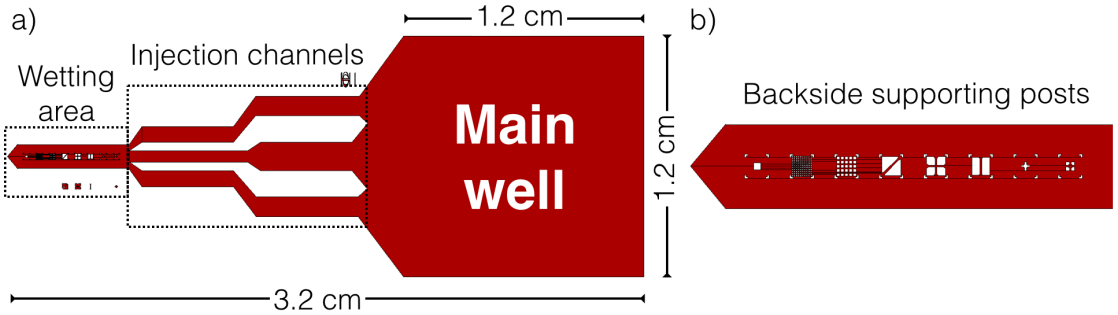


FIGURE 6.6: LED Backside wetting microfluidic system schematic. In a) the full design can be seen with a main well large enough to accommodate a large amount of fluid to prevent sudden evaporation, the injection channels are designed to drain the liquids from the main well into the wetting area where different backside supports (as seen in b)) to which LEDs can be compressed agains can be used for wetting of the backside for capillary bonding.

best wetting without damaging the adhesion of the platelets and the elastomeric stamp during wetting operations. Issues with solvent reflow on the stamp-LED interface are typically common due to surface unevenness of the rough fibres of the used clean-room cloth (as reported on Chapter 4) as well as to prevent excessive solvent on the cloth during approach, as the solvent makes the fibres expand. The microfluidic system was designed to address both of these issues. While here is represented a system for a single stamp/LED transfer, this can be easily extrapolated to an array configuration to take full advantage of the high device throughput that TP enables.

The above describes just a few of the applications areas for TP techniques which will be the focus of ongoing work. As for a broader implementation of TP as a manufacturing technique, its main advantage comes from its scalability. As illustrated for optogenetic probes and some of the produced devices for this thesis, TP can be used as an individual pixel-placing technique or adapted to perform at a much broader scale. The produced

16x16 array device on Chapter 3 was built in sixteen sequential transfers using a 4x4 stamp. Upscaling the size of both the stamps and the donor wafers used for an industrial-size TP system, larger, quicker and faster builds can be achieved for (as an example here) the display industry.

Building displays (even nowadays) is a lengthy and complicated task which is also very time-consuming. To create a full TFT array, at least five masking processes (and developments) are required for one single pixel (red (R), green (G) or blue (B)). This means that to create an entire RGB display, at least 15 masking steps are required. This excludes photolithography maskings to produce the interconnecting circuit to address the display's pixel array. Add multiple steps to include sealants, surface rubbing, liquid crystals depositions, polarising layers, integrated controller circuit, backlight inclusion and others, a modern display will take in average a day to produce. By using transfer-printing as an assembly technique, emphasis can be made on simply producing the required pixel colours (R,G,B) to build the display (Figure 6.7). This is also a step forwards to create further energy-efficient displays as (in similarity with Organic LED displays), each pixel emits its own light, making the use of a white backlight redundant. Considering the time

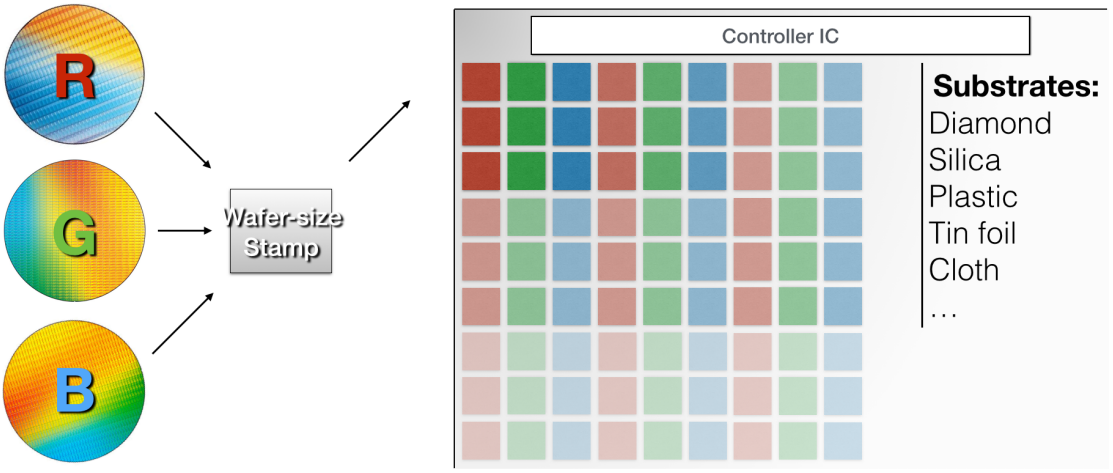


FIGURE 6.7: An approach to display manufacturing using transfer-printing as the main technique.

to perform a TP operation using our laboratory-scale system (~10 s), it is fair to assume that industrial-size can not only deliver faster speeds as well as a significant increase in throughput in the amount of pixels that can be transferred. The limiting factor for the amount of pixels that can be transfer-printed per operation is limited by the wafer size and corresponding stamp-size. For a 12" wafer, with 50 μm size LEDs (with 15 μm spacing between pixels), a total of $\sim$ 3500 x 3500 LEDs can be made within the wafer production area.

A third of these are used per transfer to create the RGB elements of a display, which means that a stamp can be tailor made to transfer 1167 horizontal pixels per transfer.

To build a full-size display (with a pixel count of 1920x1080, an entire active matrix pixel array for an HD display can be built on any substrate with four sequential TP transfers per colour (a total of 12). Further pixel sidewall insulation and addressing circuit would be the slowest part of the manufacturing process, while still being quicker than current industrial standards.

TP can therefore be complementary to other assembly techniques where it can excel on small applications and reduced size device/material assemblies, or be versatile enough to be upscaled to industrial sizes, thus offering multiple advantages such as time saving within a production line (where time = money), more energy efficient and simplified devices. The technique has a disruptive potential and can outperform established methods not only in accuracy, scalability and adaptability, from niche to industrial-size applications.

References

[1] H. J. Round, "A note on carborundum," *Electrical World*, no. 19, p. 309, 1907.

[2] W. Groves, A. Herzog, and M. Craford, "The Effect of Nitrogen Doping on $GaAs_{1-x}P_x$ Electroluminescent Diodes," *Applied Physics Letters*, vol. 19, pp. 184–186, Sep 1971.

[3] R. A. Logan, H. G. White, and W. Wiegmann, "Efficient green electroluminescence in nitrogen-doped GaP p-n junctions," *Applied Physics Letters*, vol. 13, no. 4, pp. 139–141, 1968.

[4] R. B. Jain and H. P. Maruska, "How it really happened: The history of p-type doping of gallium nitride," *physica status solidi (a)*, vol. 204, no. 6, pp. 1970–1976, 2007.

[5] J. A. Edmond, H.-S. Kong, and C. H. C. Jr., "Blue LEDs, UV photodiodes and high-temperature rectifiers in 6H-SiC," *Physica B: Condensed Matter*, vol. 185, no. 1-4, pp. 453 – 460, 1993.

[6] H. Amano, N. Sawaki, I. Akasaki, and Y. Toyoda, "Metalorganic vapor phase epitaxial growth of a high quality GaN film using an AlN buffer layer," *Applied Physics Letters*, vol. 48, pp. 353–355, Feb 1986.

[7] H. Amano, M. Kito, K. Hiramatsu, and I. Akasaki, "P-Type Conduction in Mg-Doped GaN Treated with Low-Energy Electron Beam Irradiation (LEEBI)," *Japanese Journal of Applied Physics*, vol. 28, no. 12A, p. L2112, 1989.

[8] S. Nakamura, M. Senoh, and T. Mukai, "Highly P-typed Mg-doped GaN films grown with GaN buffer layers," *Japanese Journal of Applied Physics*, vol. 30, no. Part 2, No. 10A, pp. L1708–1711, 1991.

[9] S. Nakamura, M. Senoh, and T. Mukai, "High power InGaN GaN double heterostructure violet light emitting diodes," *Applied Physics Letters*, vol. 62, no. 19, pp. 2390–2392, 1993.

[10] S. Nakamura, T. Mukai, and M. Senoh, "Candela class high brightness InGaN AlGaN double heterostructure blue light emitting diodes," *Applied Physics Letters*, vol. 64, no. 13, pp. 1687–1689, 1994.

[11] S. Nakamura, M. Senoh, S. ichi Nagahama, N. Iwasa, T. Yamada, T. Matsushita, H. Kiyoku, and Y. Sugimoto, "InGaN-Based Multi-Quantum-Well-Structure Laser Diodes," *Japanese Journal of Applied Physics*, vol. 35, no. 1B, p. L74, 1996.

[12] E. F. Schubert, *Light Emitting Diodes*. Cambridge University Press, 2nd ed., 2006.

[13] Phillips Lumileds, Luxeon Rebel ES Color Portfolio Datasheet - Available at: http://www.philipslumileds.com/products/luxeon-rebel/luxeon-rebel-color.

[14] J. K. Kim and E. F. Schubert, "Transcending the replacement paradigm of solid-state lighting," *Opt. Express*, vol. 16, pp. 21835–21842, Dec 2008.

[15] D.-H. Kim, N. Lu, R. Ghaffari, Y.-S. Kim, S. P. Lee, L. Xu, J. Wu, R.-H. Kim, J. Song, Z. Liu, J. Viventi, B. de Graff, B. Elolampi, M. Mansour, M. J. Slepian, S. Hwang, J. D. Moss, S.-M. Won, Y. Huang, B. Litt, and J. A. Rogers, "Materials for multifunctional balloon catheters with capabilities in cardiac electrophysiological mapping and ablation therapy," *Nat Mater*, vol. 10, pp. 316–323, 04 2011.

[16] N. W. Ashcroft and N. D. Mermin, *Solid State Physics*. Brooks/Cole, 1976.

[17] H. D. Young and R. A. Freedman, *University Physics with Modern Physics*. Pearson Higher Education, 11th ed., 2003.

[18] S. W. Kaun, M. H. Wong, U. K. Mishra, and J. S. Speck, "Molecular beam epitaxy for high-performance Ga-face GaN electron devices," *Semiconductor Science and Technology*, vol. 28, no. 7, p. 074001, 2013.

[19] I. Vurgaftman and J. R. Meyer, "Band parameters for nitrogen-containing semiconductors," *Journal of Applied Physics*, vol. 94, no. 6, pp. 3675–3696, 2003.

[20] Tae-Yeon, S. Jung, H. Hiroshi, H. Amano, and Morkoc, *III-Nitride Based Light Emitting Diodes and Applications*. Springer Topics in Applied Physics, 2013.

[21] D. Cherns, S. J. Henley, and F. A. Ponce, "Edge and screw dislocations as non-radiative centers in InGaN/GaN quantum well luminescence," *Applied Physics Letters*, vol. 78, no. 18, pp. 2691–2693, 2001.

[22] D. Zhu, D. J. Wallis, and C. J. Humphreys, "Prospects of III-nitride optoelectronics grown on Si," *Reports on Progress in Physics*, vol. 76, no. 10, p. 106501, 2013.

[23] C. J. Humphreys, "Does In form In-rich clusters in InGaN quantum wells?," *Philosophical Magazine*, vol. 87, no. 13, pp. 1971–1982, 2007.

[24] D. Watson-Parris, M. J. Godfrey, R. A. Oliver, P. Dawson, M. J. Galtrey, M. J. Kappers, and C. J. Humphreys, "Energy landscape and carrier wave-functions in InGaN/GaN quantum wells," *physica status solidi (c)*, vol. 7, no. 7-8, pp. 2255–2258, 2010.

[25] D. Koleske, M. Coltrin, K. Cross, C. Mitchell, and A. Allerman, "Understanding GaN nucleation layer evolution on sapphire," *Journal of Crystal Growth*, vol. 273, no. 1–2, pp. 86 – 99, 2004.

[26] S. Figge, T. Böttcher, S. Einfeldt, and D. Hommel, "In situ and ex situ evaluation of the film coalescence for GaN growth on GaN nucleation layers," *Journal of Crystal Growth*, vol. 221, no. 1-4, pp. 262 – 266, 2000. Proc Tenth Int Conf Metalorganic Vapor Phase Epitaxy.

[27] C. F. Johnston, M. J. Kappers, and C. J. Humphreys, "Microstructural evolution of nonpolar (11-20) GaN grown on (1-102) sapphire using a 3D-2D method," *Journal of Applied Physics*, vol. 105, no. 7, pp. –, 2009.

[28] W. G. Scheibenzuber, *GaN-Based Laser Diodes: Towards longer wavelengths and short pulses*. Springer Theses, 2012.

[29] T. Egawa, B. Zhang, and H. Ishikawa, "High performance of InGaN LEDs on (111) silicon substrates grown by MOCVD," *Electron Device Letters, IEEE*, vol. 26, pp. 169–171, March 2005.

[30] J. Dargys, A. Kundrotas, *Handbook on physical properties of Ge, Si, GaAs and InP*. Vilnius, Lithuania: Science and Encyclopedia Publishers, 1994.

[31] H. Ishikawa, K. Yamamoto, T. Egawa, T. Soga, T. Jimbo, and M. Umeno, "Thermal stability of GaN on (111) Si substrate," *Journal of Crystal Growth*, vol. 189–190, no. 0, pp. 178 – 182, 1998.

[32] K. Werner, A. Beyer, J. Oelerich, S. Baranovskii, W. Stolz, and K. Volz, "Structural characteristics of gallium metal deposited on Si (001) by MOCVD," *Journal of Crystal Growth*, vol. 405, no. 0, pp. 102 – 109, 2014.

[33] A. Dadgar, M. Poschenrieder, J. Bläsing, O. Contreras, F. Bertram, T. Riemann, A. Reiher, M. Kunze, I. Daumiller, A. Krtschil, A. Diez, A. Kaluza, A. Modlich, M. Kamp, J. Christen, F. Ponce, E. Kohn, and A. Krost, "MOVPE growth of GaN on Si (111) substrates," *Journal of Crystal Growth*, vol. 248, no. 0, pp. 556 – 562, 2003. Proceedings of the eleventh international conference on Metalorganic Vapor Phase Epitaxy.

[34] D. Zhu, C. McAleese, K. K. McLaughlin, M. HÃeberlen, C. O. Salcianu, E. J. Thrush, M. J. Kappers, W. A. Phillips, P. Lane, D. J. Wallis, T. Martin, M. Astles, S. Thomas, A. Pakes, M. Heuken, and C. J. Humphreys, "GaN-based LEDs grown on 6-inch diameter Si (111) substrates by MOVPE," *Proc. SPIE*, vol. 7231, pp. 723118–723118–11, 2009.

[35] U. Jahn, O. Brandt, E. Luna, X. Sun, H. Wang, D. S. Jiang, L. F. Bian, and H. Yang, "Carrier capture by threading dislocations in (In,Ga)N/GaN heteroepitaxial layers," *Phys. Rev. B*, vol. 81, p. 125314, Mar 2010.

[36] S. Guha and N. A. Bojarczuk, "Ultraviolet and violet GaN light emitting diodes on silicon," *Applied Physics Letters*, vol. 72, no. 4, pp. 415–417, 1998.

[37] C. A. Tran, A. Osinski, R. F. Karlicek, and I. Berishev, "Growth of InGaN/GaN multiple-quantum-well blue light-emitting diodes on silicon by metalorganic vapor phase epitaxy," *Applied Physics Letters*, vol. 75, no. 11, pp. 1494–1496, 1999.

[38] H. Ishikawa, G.-Y. Zhao, N. Nakada, T. Egawa, T. Jimbo, and M. Umeno, "GaN on Si Substrate with AlGaN/AlN Intermediate Layer," *Japanese Journal of Applied Physics*, vol. 38, no. 5A, p. L492, 1999.

[39] S. C. Jain, M. Willander, J. Narayan, and R. V. Overstraeten, "III-nitrides: Growth, Characterization, and Properties," *Journal of Applied Physics*, vol. 87, no. 3, pp. 965–1006, 2000.

[40] S. Nakamura, T. Mukai, and M. Senoh, "In situ monitoring and Hall measurements of GaN grown with GaN buffer layers," *Journal of Applied Physics*, vol. 71, no. 11, pp. 5543–5549, 1992.

[41] G. Wu, T. Hsieh, and T. Kweisan, "Crystal quality and electrical properties of p-type GaN thin film on Si (111) substrate by metal-organic chemical vapor deposition MOCVD," *Journal of Achievements in Materials and Manufacturing Engineering*, vol. 24, no. 1, pp. 193–197, 2007.

[42] C. Lai, T. Hsu, W.-H. Chang, K.-U. Tseng, C.-M. Lee, C.-C. Chuo, and J.-I. Chyi, "Piezoelectric Field-Induced Quantum-Confined Stark Effect in InGaN/GaN Multiple Quantum Wells," *physica status solidi (b)*, vol. 228, no. 1, pp. 77–80, 2001.

[43] K. L. Bunker, R. Garcia, and P. E. Russell, "Scanning electron microscopy cathodoluminescence studies of piezoelectric fields in an InGaN/GaN quantum-well light-emitting diode," *Applied Physics Letters*, vol. 86, no. 8, pp. –, 2005.

[44] P. Perlin, C. Kisielowski, V. Iota, B. A. Weinstein, L. Mattos, N. A. Shapiro, J. Kruger, E. R. Weber, and J. Yang, "InGaN/GaN quantum wells studied by

high pressure, variable temperature, and excitation power spectroscopy," *Applied Physics Letters*, vol. 73, no. 19, pp. 2778–2780, 1998.

[45] J.-H. Ryou, P. Yoder, J. Liu, Z. Lochner, H. Kim, S. Choi, H. J. Kim, and R. D. Dupuis, "Control of Quantum-Confined Stark Effect in InGaN-Based Quantum Wells," *Selected Topics in Quantum Electronics, IEEE Journal of*, vol. 15, pp. 1080–1091, July 2009.

[46] T. Deguchi, A. Shikanai, K. Torii, T. Sota, S. Chichibu, and S. Nakamura, "Luminescence spectra from InGaN multiquantum wells heavily doped with Si," *Applied Physics Letters*, vol. 72, pp. 3329–3331, Jun 1998.

[47] H.-S. Chen, D.-M. Yeh, Y.-C. Lu, C.-Y. Chen, C.-F. Huang, T.-Y. Tang, C. C. Yang, C.-S. Wu, and C.-D. Chen, "Strain relaxation and quantum confinement in InGaN/GaN nanoposts," *Nanotechnology*, vol. 17, no. 5, p. 1454, 2006.

[48] Y. Yang, X. A. Cao, and C. Yan, "Investigation of the Nonthermal Mechanism of Efficiency Rolloff in InGaN Light-Emitting Diodes," *Electron Devices, IEEE Transactions on*, vol. 55, pp. 1771–1775, July 2008.

[49] H. Hirayama, S. Fujikawa, N. Noguchi, J. Norimatsu, T. Takano, K. Tsubaki, and N. Kamata, "222-282 nm AlGaN and InAlGaN-based deep-UV LEDs fabricated on high-quality AlN on sapphire," *physica status solidi (a)*, vol. 206, no. 6, pp. 1176–1182, 2009.

[50] S.-C. Ling, T.-C. Lu, S.-P. Chang, J.-R. Chen, H.-C. Kuo, and S.-C. Wang, "Low efficiency droop in blue-green m-plane InGaN/GaN light emitting diodes," *Applied Physics Letters*, vol. 96, no. 23, pp. –, 2010.

[51] P. Tian, J. J. D. McKendry, Z. Gong, S. Zhang, S. Watson, D. Zhu, I. M. Watson, E. Gu, A. E. Kelly, C. J. Humphreys, and M. D. Dawson, "Characteristics and applications of micro-pixelated GaN-based light emitting diodes on Si substrates," *Journal of Applied Physics*, vol. 115, no. 3, pp. –, 2014.

[52] J. Piprek, "Efficiency droop in nitride-based light-emitting diodes," *physica status solidi (a)*, vol. 207, no. 10, pp. 2217–2225, 2010.

[53] B. Pasenow, S. W. Koch, J. Hader, J. V. Moloney, M. Sabathil, N. Linder, and S. Lutgen, "Auger losses in GaN-based quantum wells: Microscopic theory," *physica status solidi (c)*, vol. 6, no. S2, pp. S864–S868, 2009.

[54] E. Kioupakis, P. Rinke, K. T. Delaney, and C. G. Van de Walle, "Indirect Auger recombination as a cause of efficiency droop in nitride light-emitting diodes," *Applied Physics Letters*, vol. 98, no. 16, pp. –, 2011.

[55] J. Iveland, L. Martinelli, J. Peretti, J. S. Speck, and C. Weisbuch, "Direct Measurement of Auger Electrons Emitted from a Semiconductor Light-Emitting Diode under Electrical Injection: Identification of the Dominant Mechanism for Efficiency Droop," *Phys. Rev. Lett.*, vol. 110, p. 177406, Apr 2013.

[56] N. I. Bochkareva, V. V. Voronenkov, R. I. Gorbunov, A. S. Zubrilov, Y. S. Lelikov, P. E. Latyshev, Y. T. Rebane, A. I. Tsyuk, and Y. G. Shreter, "Defect-related tunneling mechanism of efficiency droop in III-Nitride Light-Emitting Diodes," *Applied Physics Letters*, vol. 96, no. 13, pp. –, 2010.

[57] X. Ni, X. Li, J. Lee, S. Liu, V. Avrutin, Ü. Özgür, H. Morkoç, A. Matulionis, T. Paskova, G. Mulholland, and K. R. Evans, "InGaN staircase electron injector for reduction of electron overflow in InGaN light emitting diodes," *Applied Physics Letters*, vol. 97, no. 3, pp. –, 2010.

[58] M. F. Schubert, J. Xu, J. K. Kim, E. F. Schubert, M. H. Kim, S. Yoon, S. M. Lee, C. Sone, T. Sakong, and Y. Park, "Polarization-matched GaInN/AlGaInN multi-quantum-well light-emitting diodes with reduced efficiency droop," *Applied Physics Letters*, vol. 93, no. 4, pp. –, 2008.

[59] M.-H. Kim, M. F. Schubert, Q. Dai, J. K. Kim, E. F. Schubert, J. Piprek, and Y. Park, "Origin of efficiency droop in GaN-based light-emitting diodes," *Applied Physics Letters*, vol. 91, no. 18, pp. –, 2007.

[60] E. Menard, K. J. Lee, D.-Y. Khang, R. G. Nuzzo, and J. A. Rogers, "A printable form of silicon for high performance thin film transistors on plastic substrates," *Applied Physics Letters*, vol. 84, no. 26, pp. 5398–5400, 2004.

[61] M. A. Meitl, Z.-T. Zhu, V. Kumar, K. J. Lee, X. Feng, Y. Y. Huang, I. Adesida, R. G. Nuzzo, and J. A. Rogers, "Transfer printing by kinetic control of adhesion to an elastomeric stamp," *Nat Mater*, vol. 5, pp. 33–38, 01 2006.

[62] T.-H. Kim, K.-S. Cho, E. K. Lee, S. J. Lee, J. Chae, J. W. Kim, D. H. Kim, J.-Y. Kwon, G. Amaratunga, S. Y. Lee, B. L. Choi, Y. Kuk, J. M. Kim, and K. Kim, "Full-colour quantum dot displays fabricated by transfer printing," *Nat Photon*, vol. 5, pp. 176–182, 03 2011.

[63] H.-S. Kim, E. Brueckner, J. Song, Y. Li, S. Kim, C. Lu, J. Sulkin, K. Choquette, Y. Huang, R. G. Nuzzo, and J. A. Rogers, "Unusual strategies for using indium gallium nitride grown on silicon (111) for solid-state lighting.," *Proceedings of the National Academy of Sciences of the United States of America*, vol. 108, pp. 10072–10077, June 2011.

[64] A. J. Trindade, B. Guilhabert, D. Massoubre, D. Zhu, N. Laurand, E. Gu, I. M. Watson, C. J. Humphreys, and M. D. Dawson, "Nanoscale-accuracy transfer printing of ultra-thin AlInGaN light-emitting diodes onto mechanically flexible substrates," *Applied Physics Letters*, vol. 103, no. 25, p. 253302, 2013.

[65] S. Kim, A. Carlson, H. Cheng, S. Lee, J.-K. Park, Y. Huang, and J. A. Rogers, "Enhanced adhesion with pedestal-shaped elastomeric stamps for transfer printing," *Applied Physics Letters*, vol. 100, no. 17, pp. –, 2012.

[66] S. Kim, J. Wu, A. Carlson, S. H. Jin, A. Kovalsky, P. Glass, Z. Liu, N. Ahmed, S. L. Elgan, W. Chen, P. M. Ferreira, M. Sitti, Y. Huang, and J. A. Rogers, "Microstructured elastomeric surfaces with reversible adhesion and examples of their use in deterministic assembly by transfer printing," *Proceedings of the National Academy of Sciences*, vol. 107, no. 40, pp. 17095–17100, 2010.

[67] J. Yoon, S. Jo, I. S. Chun, I. Jung, H.-S. Kim, M. Meitl, E. Menard, X. Li, J. J. Coleman, U. Paik, and J. A. Rogers, "GaAs photovoltaics and optoelectronics using releasable multilayer epitaxial assemblies," *Nature*, vol. 465, pp. 329–333, 05 2010.

[68] C. A. Bower, S. Member, E. Menard, S. Bonafede, J. W. Hamer, and R. S. Cok, "Transfer-Printed Microscale Integrated Circuits for High Performance Display Backplanes," *IEEE Transactions on components, packaging and manufacturing technology*, vol. 1, no. 12, pp. 1916–1922, 2011.

[69] J. Justice, C. Bower, M. Meitl, M. B. Mooney, M. A. Gubbins, and B. Corbett, "Wafer-scale integration of group III-V lasers on silicon using transfer printing of epitaxial layers," *Nat Photon*, vol. 6, pp. 610–614, 09 2012.

[70] J. Viventi, D.-H. Kim, L. Vigeland, E. S. Frechette, J. A. Blanco, Y.-S. Kim, A. E. Avrin, V. R. Tiruvadi, S.-W. Hwang, A. C. Vanleer, D. F. Wulsin, K. Davis, C. E. Gelber, L. Palmer, J. Van der Spiegel, J. Wu, J. Xiao, Y. Huang, D. Contreras, J. A. Rogers, and B. Litt, "Flexible, foldable, actively multiplexed, high-density electrode array for mapping brain activity in vivo," *Nat Neurosci*, vol. 14, pp. 1599–1605, 12 2011.

[71] H.-J. Chung, T.-i. Kim, H.-S. Kim, S. A. Wells, S. Jo, N. Ahmed, Y. H. Jung, S. M. Won, C. A. Bower, and J. A. Rogers, "Fabrication of Releasable Single-Crystal Silicon-Metal Oxide Field-Effect Devices and Their Deterministic Assembly on Foreign Substrates," *Advanced Functional Materials*, vol. 21, no. 16, pp. 3029–3036, 2011.

[72] S.-I. Park, Y. Xiong, R.-H. Kim, P. Elvikis, M. Meitl, D.-H. Kim, J. Wu, J. Yoon, C.-J. Yu, Z. Liu, Y. Huang, K.-c. Hwang, P. Ferreira, X. Li, K. Choquette, and J. A. Rogers, "Printed Assemblies of Inorganic Light-Emitting Diodes for Deformable and Semitransparent Displays," *Science*, vol. 325, no. 5943, pp. 977–981, 2009.

[73] T.-i. Kim, S. Hyun Lee, Y. Li, Y. Shi, G. Shin, S. Dan Lee, Y. Huang, J. A. Rogers, and J. Su Yu, "Temperature- and size-dependent characteristics in ultrathin inorganic light-emitting diodes assembled by transfer printing," *Applied Physics Letters*, vol. 104, no. 5, 2014.

[74] Y. Li, Y. Shi, J. Song, C. Lu, T.-i. Kim, J. A. Rogers, and Y. Huang, "Thermal properties of microscale inorganic light-emitting diodes in a pulsed operation," *Journal of Applied Physics*, vol. 113, no. 14, p. 144505, 2013.

[75] J. Wu, S. Kim, W. Chen, A. Carlson, K.-C. Hwang, Y. Huang, and J. A. Rogers, "Mechanics of reversible adhesion," *Soft Matter*, vol. 7, pp. 8657–8662, 2011.

[76] B. Lautrup, *Physics of Continuous Matter: Exotic and Everyday Phenomena in the Macroscopic World*. Institute of Physics Publishing, 2005.

[77] M. B. Tucker, D. R. Hines, and T. Li, "A quality map of transfer printing," *Journal of Applied Physics*, vol. 106, no. 10, pp. –, 2009.

[78] R. A. L. Jones, *Soft Condensed Matter*. ISBN: 978-0-19-850590-7, Oxford Master Series in Physics 6, 2002.

[79] E. Cheung, M. Karagozler, S. Park, B. Kim, and M. Sitti, "A new endoscopic microcapsule robot using beetle inspired microfibrillar adhesives," in *Advanced Intelligent Mechatronics. Proceedings, 2005 IEEE/ASME International Conference on*, pp. 551–557, July 2005.

[80] C. J. Drummond and D. Y. C. Chan, "van der Waals Interaction, Surface Free Energies, and Contact Angles: Dispersive Polymers and Liquids," *Langmuir*, vol. 13, no. 14, pp. 3890–3895, 1997.

[81] S. Franssila, *Introduction to Microfabrication*. ISBN: 978-0-470-74983-8, Wiley, 2nd ed., 2010.

[82] Fundamentals of Mercury Arc Lamps.

[83] K. E. Bean, "Anisotropic Etching of Silicon," *IEEE Transactions on Electron Devices*, vol. ED-25, no. 10, 1978.

[84] S. S. Singh and P. Pal, "A New Model for the Etching Characteristics of Corners Formed by Si{111} Planes on Si{110} Wafer Surface," *SCIRP Engineering*, vol. 5, no. 11A, 2013.

[85] P. Pal and S. S. Singh, "A simple and robust model to explain convex corner undercutting in wet bulk micromachining," *Micro and Nano Systems Letters*, vol. 1, no. 1, 2013.

[86] D. GrÃef, M. Grundner, and R. Schulz, "Reaction of water with hydrofluoric acid treated Silicon(111) and (100) surfaces," *Journal of Vacuum Science & Technology A*, vol. 7, no. 3, pp. 808–813, 1989.

[87] Q. D. Nguyen, "Electrochemistry in anisotropic etching of silicon in alkaline solutions Electrochemistry in anisotropic etching of silicon in alkaline solutions," 2007.

[88] J. J. Kelly and H. G. Philipsen, "Anisotropy in the wet-etching of semiconductors," *Current Opinion in Solid State and Materials Science*, vol. 9, no. 1–2, pp. 84 – 90, 2005.

[89] P. Allongue, "Molecular Imaging and Local Density of States Characterization at the Si(111)/NaOH Interface," *Phys. Rev. Lett.*, vol. 77, pp. 1986–1989, Sep 1996.

[90] M. A. Gosálvez, "Atomistic modelling of anisotropic etching of crystaline silicon," 2003.

[91] H. Seidel, L. Csepregi, A. Heuberger, and H. Baumgärtel, "Anisotropic Etching of Crystalline Silicon in Alkaline Solutions: I . Orientation Dependence and Behavior of Passivation Layers," *Journal of The Electrochemical Society*, vol. 137, no. 11, pp. 3612–3626, 1990.

[92] M. Shikida, K. Sato, K. Tokoro, and D. Uchikawa, "Comparison of anisotropic etching properties between KOH and TMAH solutions," in *Micro Electro Mechanical Systems, 1999. MEMS '99. Twelfth IEEE International Conference on*, pp. 315–320, Jan 1999.

[93] R. Oosterbroek, J. Berenschot, H. Jansen, A. Nijdam, G. Pandraud, A. van den Berg, and M. Elwenspoek, "Etching methodologies in <111>-oriented silicon wafers," *Microelectromechanical Systems, Journal of*, vol. 9, pp. 390–398, Sept 2000.

[94] W. Guo, J. Xie, C. Akouala, S. Mita, A. Rice, J. Tweedie, I. Bryan, R. Collazo, and Z. Sitar, "Comparative study of etching high crystalline quality AlN and GaN," *Journal of Crystal Growth*, vol. 366, pp. 20–25, Mar. 2013.

[95] D. Zhuang and J. Edgar, "Wet etching of GaN, AlN, and SiC: a review," *Materials Science and Engineering: R: Reports*, vol. 48, no. 1, pp. 1 – 46, 2005.

[96] D. Li, M. Sumiya, K. Yoshimura, Y. Suzuki, Y. Fukuda, and S. Fuke, "Characteristics of the GaN Polar Surface during an Etching Process in KOH Solution," *physica status solidi (a)*, vol. 180, no. 1, pp. 357–362, 2000.

[97] J. L. Rouviere, J. L. Weyher, M. Seelmann-Eggebert, and S. Porowski, "Polarity determination for GaN films grown on (0001) sapphire and high-pressure-grown GaN single crystals," *Applied Physics Letters*, vol. 73, no. 5, pp. 668–670, 1998.

[98] G. Radtke, M. Couillard, G. A. Botton, D. Zhu, and C. J. Humphreys, "Scanning transmission electron microscopy investigation of the Si(111)/AlN interface grown by metalorganic vapor phase epitaxy," *Applied Physics Letters*, vol. 97, no. 25, p. 251901, 2010.

[99] D. Zhu, C. McAleese, M. Haberlen, C. Salcianu, T. Thrush, M. Kappers, A. Phillips, P. Lane, M. Kane, D. Wallis, T. Martin, M. Astles, N. Hylton, P. Dawson, and C. Humphreys, "Efficiency measurement of GaN-based quantum well and light-emitting diode structures grown on silicon substrates," *Journal of Applied Physics*, vol. 109, no. 1, p. 014502, 2011.

[100] Brigham Young University, Integrated Microfabrication Lab, http://www.cleanroom.byu.edu/KOH.phtml.

[101] NanoInk NLP 2000 Datasheet/Product brochure, http://acs-t.com/, 2014.

[102] J.-H. Ahn, H.-S. Kim, K. J. Lee, S. Jeon, S. J. Kang, Y. Sun, R. G. Nuzzo, and J. A. Rogers, "Heterogeneous three-dimensional electronics by use of printed semiconductor nanomaterials.," *Science (New York, N.Y.)*, vol. 314, pp. 1754–1757, Dec. 2006.

[103] J. Senawiratne, A. Chatterjee, T. Detchprohm, W. Zhao, Y. Li, M. Zhu, Y. Xia, X. Li, J. Plawsky, and C. Wetzel, "Junction temperature, spectral shift, and efficiency in GaInN-based blue and green light emitting diodes," *Thin Solid Films*, vol. 518, no. 6, pp. 1732 – 1736, 2010.

[104] Z. Gong, S. Jin, Y. Chen, J. McKendry, D. Massoubre, I. M. Watson, E. Gu, and M. D. Dawson, "Size-dependent light output, spectral shift, and self-heating of 400 nm InGaN light-emitting diodes," *Journal of Applied Physics*, vol. 107, no. 1, 2010.

[105] X. Cao, S. LeBoeuf, and T. Stecher, "Temperature-dependent electroluminescence of AlGaN-based UV LEDs," *Electron Device Letters, IEEE*, vol. 27, pp. 329–331, May 2006.

[106] Z. G. Ju, S. T. Tan, Z.-H. Zhang, Y. Ji, Z. Kyaw, Y. Dikme, X. W. Sun, and H. V. Demir, "On the origin of the redshift in the emission wavelength of InGaN/GaN

blue light emitting diodes grown with a higher temperature interlayer," *Applied Physics Letters*, vol. 100, no. 12, 2012.

[107] J. E. Mark, *Polymer Data Handbook*. No. 9780195181012, Oxford University Press, 2009.

[108] Z. L. Liau, "Semiconductor wafer bonding via liquid capillarity," *Applied Physics Letters*, vol. 77, no. 5, pp. 651–653, 2000.

[109] L. Bergstrom, "Hamaker constants of inorganic materials," *Advances in Colloid and Interface Science*, vol. 70, no. 0, pp. 125 – 169, 1997.

[110] L. T. Romano, C. G. Van de Walle, J. W. Ager, W. Gatz, and R. S. Kern, "Effect of Si doping on strain, cracking, and microstructure in GaN thin films grown by metalorganic chemical vapor deposition," *Journal of Applied Physics*, vol. 87, no. 11, pp. 7745–7752, 2000.

[111] Y. Fu, D. A. Gulino, and R. Higgins, "Residual stress in GaN epilayers grown on silicon substrates," *Journal of Vacuum Science & Technology A*, vol. 18, no. 3, pp. 965–967, 2000.

[112] W. D. Nix and B. M. Clemens, "Crystallite coalescence: A mechanism for intrinsic tensile stresses in thin films," *Journal of Materials Research*, vol. 14, pp. 3467–3473, 1999.

[113] H. Marchand, L. Zhao, N. Zhang, B. Moran, R. Coffie, U. K. Mishra, J. S. Speck, S. P. DenBaars, and J. A. Freitas, "Metalorganic chemical vapor deposition of GaN on Si(111): Stress control and application to field-effect transistors," *Journal of Applied Physics*, vol. 89, no. 12, pp. 7846–7851, 2001.

[114] M. Jamil, J. R. Grandusky, V. Jindal, F. Shahedipour-Sandvik, S. Guha, and M. Arif, "Development of strain reduced GaN on Si (111) by substrate engineering," *Applied Physics Letters*, vol. 87, no. 8, 2005.

[115] G. Steude, B. K. Meyer, A. Galdner, A. Hoffmann, A. Kaschner, F. Bechstedt, H. Amano, and I. Akasaki, "Strain Modification of GaN in AlGaN/GaN Epitaxial Films," *Japanese Journal of Applied Physics*, vol. 38, no. 5A, p. L498, 1999.

[116] D. You, Y. Tang, J. Xu, X. Li, X. Li, and H. Gong, "Effects of tensile stress induced by SiO_2 passivation layer on the properties of AlGaN GaN heterostructure photodiode," *Applied Physics Letters*, vol. 89, no. 6, 2006.

[117] J. Sharpe, W.N., J. Pulskamp, D. Gianola, C. Eberl, R. Polcawich, and R. Thompson, "Strain Measurements of Silicon Dioxide Microspecimens by Digital Imaging Processing," *Experimental Mechanics*, vol. 47, no. 5, pp. 649–658, 2007.

[118] K. Mackenzie, D. Johnson, M. DeVre, R. Westerman, and B. Reelfs, "Stress Control of Si-based PECVD Dielectrics," *Meeting Abstracts*, vol. MA2005-01, no. 9, p. 406, 2006.

[119] D. L. Smith, "Controlling the plasma chemistry of silicon nitride and oxide deposition from silane," *Journal of Vacuum Science & Technology A*, vol. 11, no. 4, pp. 1843–1850, 1993.

[120] Schott North America, http://www.us.schott.com.

[121] "Delaware Diamond Knives."

[122] L. van der Tempel, G. P. Melis, and T. C. Brandsma, "Thermal Conductivity of a Glass: I. Measurement by the Glass-Metal Contact," *Glass Physics and Chemistry*, vol. 26, no. 6, pp. 606–611, 2000.

[123] "MicroChem SU-8 Photoresists datasheet."

[124] J. G. McCall, T.-i. Kim, G. Shin, X. Huang, Y. H. Jung, R. Al-Hasani, F. G. Omenetto, M. R. Bruchas, and J. A. Rogers, "Fabrication and application of flexible, multimodal light-emitting devices for wireless optogenetics," *Nat. Protocols*, vol. 8, pp. 2413–2428, 12 2013.

[125] G. Yang, Y. Jung, C. V. Cuervo, F. Ren, S. J. Pearton, and J. Kim, "GaN-based light-emitting diodes on graphene-coated flexible substrates," *Opt. Express*, vol. 22, pp. A812–A817, May 2014.

[126] C. Goßler, C. Bierbrauer, R. Moser, M. Kunzer, K. Holc, W. Pletschen, K. Köhler, J. Wagner, M. Schwaerzle, P. Ruther, O. Paul, J. Neef, D. Keppeler, G. Hoch, T. Moser, and U. T. Schwarz, "GaN-based micro-LED arrays on flexible substrates for optical cochlear implants," *Journal of Physics D: Applied Physics*, vol. 47, no. 20, p. 205401, 2014.

[127] J. M. M. Santos, B. E. Jones, P. J. Schlosser, S. Watson, J. Herrnsdorf, B. Guilhabert, J. J. D. McKendry, J. D. Jesus, T. A. Garcia, M. C. Tamargo, A. E. Kelly, J. E. Hastie, N. Laurand, and M. D. Dawson, "Hybrid GaN LED with capillary-bonded II-VI MQW color-converting membrane for visible light communications," *Semiconductor Science and Technology*, vol. 30, no. 3, p. 035012, 2015.

[128] J. McKendry, D. Massoubre, S. Zhang, B. R. Rae, E. Gu, R. Henderson, A. Kelly, M. Dawson, and R. P. Green, "Visible-Light Communications Using a CMOS-Controlled Micro-Light-Emitting-Diode Array," *Journal of Lightwave Technology*, vol. 30, no. 1, pp. 61–67, 2012.

[129] S. Chichibu, T. Azuhata, T. Sota, and S. Nakamura, "Spontaneous emission of localized excitons in InGaN single and multiquantum well structures," *Applied Physics Letters*, vol. 69, no. 27, pp. 4188–4190, 1996.

[130] T. Y. Lin, "Converse piezoelectric effect and photoelastic effect in InGaN/GaN multiple quantum wells," *Applied Physics Letters*, vol. 82, no. 6, pp. 880–882, 2003.

[131] A. Hangleiter, "Optical properties and polarization fields in the nitrides," *Journal of Luminescence*, vol. 87–89, pp. 130–134, 5 2000.

[132] Y. K. Su, G. C. Chi, and J. K. Sheu, "Optical properties in InGaN/GaN multiple quantum wells and blue LEDs," *Optical Materials*, vol. 14, pp. 205–209, 7 2000.

[133] S. F. Chichibu, A. C. Abare, M. S. Minsky, S. Keller, S. B. Fleischer, J. E. Bowers, E. Hu, U. K. Mishra, L. A. Coldren, S. P. DenBaars, and T. Sota, "Effective band gap inhomogeneity and piezoelectric field in InGaN/GaN multiquantum well structures," *Applied Physics Letters*, vol. 73, no. 14, pp. 2006–2008, 1998.

[134] S. De, A. Layek, S. Bhattacharya, D. Kumar Das, A. Kadir, A. Bhattacharya, S. Dhar, and A. Chowdhury, "Quantum-confined Stark effect in localized luminescent centers within InGaN/GaN quantum-well based light emitting diodes," *Applied Physics Letters*, vol. 101, no. 12, pp. –, 2012.

[135] L.-H. Peng, C.-W. Chuang, and L.-H. Lou, "Piezoelectric effects in the optical properties of strained InGaN quantum wells," *Applied Physics Letters*, vol. 74, no. 6, pp. 795–797, 1999.

[136] C. K. Wang, Y. Z. Chiou, T. H. Chiang, and T. K. . . Lin, "Investigating the Effect of Piezoelectric Polarization on GaN-Based LEDs with Different Prestrain Layer by Temperature-Dependent Electroluminescence," *International Journal of Photoenergy*.

[137] J. K. Sheu, T.-W. Yeh, G. Chi, and M. J. Jou, "Luminescence of the InGaN/GaN blue light-emitting diodes," 2000.

[138] P. G. Eliseev, P. Perlin, J. Lee, and M. Osiński, "Blue temperature-induced shift and band-tail emission in InGaN-based light sources," *Applied Physics Letters*, vol. 71, no. 5, pp. 569–571, 1997.

[139] S. F. Chichibu, H. Marchand, M. S. Minsky, S. Keller, P. T. Fini, J. P. Ibbetson, S. B. Fleischer, J. S. Speck, J. E. Bowers, E. Hu, U. K. Mishra, S. P. DenBaars, T. Deguchi, T. Sota, and S. Nakamura, "Emission mechanisms of bulk GaN and InGaN quantum wells prepared by lateral epitaxial overgrowth," *Applied Physics Letters*, vol. 74, no. 10, pp. 1460–1462, 1999.

[140] Y. Narukawa, Y. Kawakami, M. Funato, S. Fujita, S. Fujita, and S. Nakamura, "Role of self-formed InGaN quantum dots for exciton localization in the purple laser diode emitting at 420 nm," *Applied Physics Letters*, vol. 70, no. 8, pp. 981–983, 1997.

[141] L.-W. Ji, T.-H. Fang, and T.-H. Meen, "Effects of strain on the characteristics of InGaN-GaN multiple quantum-dot blue light emitting diodes," *Physics Letters A*, vol. 355, pp. 118–121, 6 2006.

[142] C.-H. Chen, S.-J. Chang, and Y.-K. Su, "High-Indium-Content InGaN/GaN Multiple-Quantum-Well Light-Emitting Diodes," *Japanese Journal of Applied Physics*, vol. 42, no. 4S, p. 2281, 2003.

[143] I. V. Akimova, P. G. Eliseev, M. A. Osinski, and P. Perlin, "Spontaneous emission from a quantum-well GaN/InGaN/AlGaN heterostructure at high pump currents," *Quantum Electronics*, vol. 26, no. 12, p. 1039, 1996.

[144] X. A. Cao, S. F. LeBoeuf, L. B. Rowland, C. H. Yan, and H. Liu, "Temperature-dependent emission intensity and energy shift in InGaN/GaN multiple-quantum-well light-emitting diodes," *Applied Physics Letters*, vol. 82, no. 21, pp. 3614–3616, 2003.

[145] Y.-F. Wu, "High-Temperature Electroluminescence of InGaN/GaN Light-Emitting Devices with Multiple Quantum Barriers," *Advances in Condensed Matter Physics*, vol. 2012, p. 7, 2012.

[146] T. Mukai, M. Yamada, and S. Nakamura, "Current and Temperature Dependences of Electroluminescence of InGaN-Based UV/Blue/Green Light-Emitting Diodes," *Japanese Journal of Applied Physics*, vol. 37, no. 11B, p. L1358, 1998.

[147] A. J. Trindade, B. Guilhabert, E. Y. Xie, R. Ferreira, J. J. D. McKendry, D. Zhu, N. Laurand, E. Gu, D. J. Wallis, I. M. Watson, C. J. Humphreys, and M. D. Dawson, "Heterogeneous integration of gallium nitride light-emitting diodes on diamond and silica by transfer printing," *Opt. Express*, vol. 23, pp. 9329–9338, Apr 2015.

[148] D. O'Brien, G. Faulkner, E. Zyambo, K. Jim, D. Edwards, P. Stavrinou, G. Parry, J. Bellon, M. Sibley, V. Lalithambika, V. Joyner, R. Samsudin, D. Holburn, and R. Mears, "Integrated transceivers for optical wireless communications," *Selected Topics in Quantum Electronics, IEEE Journal of*, vol. 11, pp. 173–183, Jan 2005.

[149] C. Okonkwo, E. Tangdiongga, H. Yang, D. Visani, S. Loquai, R. Kruglov, B. Charbonnier, M. Ouzzif, I. Greiss, O. Ziemann, R. Gaudino, and A. Koonen, "Recent

Results From the EU POF-PLUS Project: Multi-Gigabit Transmission Over 1 mm Core Diameter Plastic Optical Fibers," *Lightwave Technology, Journal of*, vol. 29, pp. 186–193, Jan 2011.

[150] D. Tsonev, H. Chun, S. Rajbhandari, J. McKendry, S. Videv, E. Gu, M. Haji, S. Watson, A. Kelly, G. Faulkner, M. Dawson, H. Haas, and D. O'Brien, "A 3-Gb/s Single-LED OFDM-Based Wireless VLC Link Using a Gallium Nitride μm LED," *Photonics Technology Letters, IEEE*, vol. 26, pp. 637–640, April 2014.

[151] Advanced Photonix, Inc. http://advancedphotonix.com/hsor/application-notes/bandwidth-terminology/, Accessed Feb. 2015.

[152] M. A. Haase, J. Xie, T. A. Ballen, J. Zhang, B. Hao, Z. H. Yang, T. J. Miller, X. Sun, T. L. Smith, and C. A. Leatherdale, "II-VI semiconductor color converters for efficient green, yellow, and red light emitting diodes," *Applied Physics Letters*, vol. 96, no. 23, pp. –, 2010.

[153] M. Tamargo, W. Lin, S. Guo, Y. Guo, Y. Luo, and Y. Chen, "Full-color light-emitting diodes from ZnCdMgSe/ZnCdSe quantum well structures grown on InP substrates," *Journal of Crystal Growth*, vol. 214–215, no. 0, pp. 1058 – 1063, 2000.

[154] N. McAlinden, D. Massoubre, E. Richardson, E. Gu, S. Sakata, M. D. Dawson, and K. Mathieson, "Thermal and optical characterization of micro-led probes for in vivo optogenetic neural stimulation," *Opt. Lett.*, vol. 38, pp. 992–994, Mar 2013.

[155] S. Zhang, S. Watson, J. McKendry, D. Massoubre, A. Cogman, E. Gu, R. Henderson, A. Kelly, and M. Dawson, "1.5 gbit/s multi-channel visible light communications using cmos-controlled gan-based leds," *Lightwave Technology, Journal of*, vol. 31, pp. 1211–1216, April 2013.

[156] E. F. Schubert, Y. Wang, A. Y. Cho, L. Tu, and G. J. Zydzik, "Resonant cavity light-emitting diode," *Applied Physics Letters*, vol. 60, no. 8, pp. 921–923, 1992.

[157] M. Raja, S. Brueck, M. Osinski, C. Schaus, J. McInerney, T. Brennan, and B. Hammons, "Resonant periodic gain surface-emitting semiconductor lasers," *Quantum Electronics, IEEE Journal of*, vol. 25, pp. 1500–1512, Jun 1989.

[158] T. Matsuoka, T. Ito, and T. Kaino, "First plastic optical fibre transmission experiment using 520 nm leds with intensity modulation/direct detection," *Electronics Letters*, vol. 36, pp. 1836–1837, Oct 2000.

[159] J.-M. Wun, C.-W. Lin, W. Chen, J.-K. Sheu, C.-L. Lin, Y.-L. Li, J. Bowers, J.-W. Shi, J. Vinogradov, R. Kruglov, and O. Ziemann, "Gan-based miniaturized cyan light-emitting diodes on a patterned sapphire substrate with improved fiber coupling

for very high-speed plastic optical fiber communication," *Photonics Journal, IEEE*, vol. 4, pp. 1520–1529, Oct 2012.

Publications

[1] **A. J. Trindade**, B. Guilhabert, D. Massoubre, D. Zhu, N. Laurand, E. Gu, I. M. Watson, C. J. Humphreys and M. D. Dawson, *"Nanoscale-accuracy transfer printing of ultra-thin AlInGaN light-emitting diodes onto mechanically flexible substrates"*, Applied Physics Letters, 103, (253302) 201, 2013, doi: http://dx.doi.org/10.1063/1.4851875

[2] **A. J. Trindade**, B. Guilhabert, E. Y. Xie, R. Ferreira, J. J. D. McKendry, D. Zhu, N. Laurand, E. Gu, I. M. Watson, C. J. Humphreys and M. D. Dawson, *"Heterogeneous integration of gallium nitride light-emitting diodes on diamond and silica by transfer printing"*, Optics Express, Vol. 23, Issue 7, 2015 doi: http://dx.doi.org/10.1364/OE.23.009329

Conference Presentations

[1] **A. J. Trindade**, B. Guilhabert, E. Y. Xie, R. Ferreira, J. J. D. McKendry, D. Zhu, N. Laurand, E. Gu, I. M. Watson, C. J. Humphreys and M. D. Dawson, "Transfer Printing of ultra-thin micro-LEDs via capillary bonding", Oral presentation at the UK Nitrides Consortium, 2015, United Kingdom.

[2] **A. J. Trindade**, B. Guilhabert, D. Massoubre, D. Zhu, N. Laurand, E. Gu, I. M. Watson, C. J. Humphreys and M. D. Dawson, "Transfer-Printed ultra-thin LEDs via capillary-bonding onto flexible and rigid substrates", Oral presentation at the IEEE Photonics Conference 2014, San Diego, USA. doi: http://dx.doi.org/10.1109/IPCon.2014.6995470

[3] **A. J. Trindade**, B. Guilhabert, D. Massoubre, D. Zhu, N. Laurand, E. Gu, I. M. Watson, C. J. Humphreys and M. D. Dawson, "Nano-positioning Transfer Printing of AlInGaN Light-Emitting Diodes in various substrates", Oral presentation at the SPIE Photonics West 2014 - San Francisco, USA.

[4] **A. J. Trindade**, B. Guilhabert, D. Massoubre, D. Zhu, N. Laurand, E. Gu, I. M. Watson, C. J. Humphreys and M. D. Dawson, "Nano-positioning Transfer Printing of AlInGaN Light-Emitting Diodes", Oral presentation at the IEEE Photonics Conference 2013, Seattle, USA. doi: http://dx.doi.org/10.1109/IPCon.2013.6656512

[5] **A. J. Trindade**, B. Guilhabert, D. Massoubre, D. Zhu, N. Laurand, E. Gu, I. M. Watson, C. J. Humphreys and M. D. Dawson, "Precision Transfer Printing of AlInGaN Light-Emitting Diodes", Oral presentation at the UK Semiconductors 2013, Sheffield, United Kingdom.

Nanoscale-accuracy transfer printing of ultra-thin AlInGaN light-emitting diodes onto mechanically flexible substrates

A. J. Trindade,[1,a)] B. Guilhabert,[1] D. Massoubre,[1,b)] D. Zhu,[2] N. Laurand,[1] E. Gu,[1] I. M. Watson,[1] C. J. Humphreys,[2] and M. D. Dawson[1]
[1]*Institute of Photonics, SUPA, University of Strathclyde, 106 Rottenrow, Glasgow G4 0NW, United Kingdom*
[2]*Department of Materials Science and Metallurgy, University of Cambridge, 27 Charles Babbage Road, Cambridge CB3 0FS, United Kingdom*

(Received 3 November 2013; accepted 26 November 2013; published online 17 December 2013)

The transfer printing of 2 μm-thick aluminum indium gallium nitride (AlInGaN) micron-size light-emitting diodes with 150 nm ($\pm$14 nm) minimum spacing is reported. The thin AlInGaN structures were assembled onto mechanically flexible polyethyleneterephthalate/polydimethylsiloxane substrates in a representative 16 $\times$ 16 array format using a modified dip-pen nano-patterning system. Devices in the array were positioned using a pre-calculated set of coordinates to demonstrate an automated transfer printing process. Individual printed array elements showed blue emission centered at 486 nm with a forward-directed optical output power up to 80 μW (355 mW/cm^2) when operated at a current density of 20 A/cm^2. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4851875]

Mechanically flexible and conformable optoelectronics and photonics is an important topic of research, opening up many exciting scientific and technological opportunities.[1] A recent and attractive approach to flexible photonics is based on the fact that inorganic structures such as semiconductors can be tailored to bend or flex if they are sufficiently thin.[2] The "transfer printing" of such thin inorganic devices directly onto non-rigid (e.g., polymeric) substrates results in hybrid integration combining the advantageous properties of organic and inorganic materials, offering an optimized flexible photonics platform. This approach has recently enabled the demonstration of mechanically flexible arrays of inorganic light-emitting diodes (LEDs) and related components with a wide range of applications including conformable displays,[3,4] image sensors,[5] illumination solutions and biomedical instrumentation[1,6] as well as optical communication systems.[6–8]

To capitalize fully on the capabilities of inorganic semiconductors for flexible photonics, it will be essential to assemble structures by transfer printing with very high (ideally nano-scale) placement accuracy and preferably also large-area scalability. Indeed, advanced photonic devices often depend on precise spatial combination of micro/nano-structures, either to manipulate the behavior of light (e.g., in micro-resonators, gratings and photonic crystals) or to integrate heterogeneous components such as lasers, waveguides, and photodetectors.[9] High accuracy is also critical in order to realize high-density arrays of such devices. No transfer printing research has so far specifically addressed this issue, and the best reported placement accuracies are $\sim$1–3 μm,[10,11] inadequate to target the aforementioned submicron integration concepts and/or (high fill factor) device arrays. Consequently, there is a need to further enhance the accuracy of transfer printing of thin-film semiconductor structures, without sacrificing fabrication throughput or scalability.

To address this issue, we report here scalable pick-and-place transfer printing of inorganic semiconductor device structures onto mechanically flexible substrates with the highest reported positioning accuracy. The aluminum indium gallium nitride (AlInGaN)-based devices used were grown on a silicon (Si) substrate, which is used in a sacrificial manner during the process flow. Transfer printing was realized using a commercial dip-pen nano-patterning system (NanoInk Inc. NLP2000) converted into a computer-controlled transfer printer.[12] The system uses a 5-axis stage (3 linear and 2 goniometers) combined with high-accuracy optical encoders. The resulting system offers large area coverage (100 $\times$ 100 mm^2) while maintaining, manufacturer specified, a positioning accuracy as small as $\pm$25 nm. In addition, extensive computer-aided design software allows step-by-step control and automation.[12] To demonstrate the capabilities of our approach, ultra-thin AlInGaN micro-LEDs (each 150 $\times$ 150 μm^2 in area) were assembled on mechanically flexible plastic substrates in various configurations including a 16 $\times$ 16 array and with minimum spacing between devices of 150 nm, limited by the roughness of the device-sidewalls. The process is aided by smooth lower surface of GaN-on-Si suspended membranes, which we propose is protected during the aggressive wet etch process used in substrate removal to underetch devices via a thin interfacial silicon nitride (SiN_x) layer, formed during epitaxial growth.

The LED epitaxial structures used were grown by metal organic vapor phase epitaxy (MOVPE) on Si (111)-oriented wafers[13] and were processed into 2 μm-thick micron-sized LEDs. A cross-sectional schematic of the epistructure used is given in Figure 1.

The experimental procedures to fabricate arrays of suspended AlInGaN LEDs for transfer printing are also summarized schematically in Figure 1. Device fabrication was initiated with lithographic patterning of semitransparent current-spreading metal (Figure 1(a)); nickel (Ni)/gold (Au), thicknesses 12 nm/23 nm) prepared using electron-beam deposition, and subjected to annealing in an air environment to

a)antonio.trindade@strath.ac.uk
b)Current address: Queensland Micro and Nanotechnology Centre, Griffith University, 170 Kessels Road, Nathan QLD 4111, Australia.

oxidize the Ni component. Inductively coupled plasma etching was used to expose the underlying n-GaN layer of the p-i-n heterostructure (Figure 1(b)). Metal sputter deposition followed to produce opaque contacts on top of the current-spreading layer and onto the newly exposed n-GaN (Titanium (Ti)/Au, thicknesses 50 nm/180 nm). To define the device lateral dimensions, and allow creation of supporting "anchors," a 1 μm-thick silicon dioxide (SiO_2) layer was deposited using plasma-enhanced chemical vapor deposition (PECVD) and patterned to protect the devices for deep etching through to the substrate (Figure 1(c)). Reactive-ion etching (RIE) was then used to continue etching into the Si substrate, thus exposing the Si sidewalls attacked during the following wet etch step (Figure 1(d)).

To underetch the devices to prepare for their later release from the native substrate, anisotropic wet etching using 60% w/w aqueous potassium hydroxide (KOH) solution at 80 °C was used. Anisotropic etching of Si planes (110) perpendicular to patterned supporting anchors were preferentially etched (~3.5 μm/min) while slower-etching (111) planes defined vertical sidewalls. After completion of the underetching, devices were held suspended above an air gap by two diagonally opposed sacrificial anchors.[6] The total thickness of the devices after removal of the backing substrate is close to 2 μm.

The SiO_2 deposited over the LED current spreading layer and contacts resisted the KOH etching sufficiently to protect the metal layers during the underetching step. Residual SiO_2 was removed after process completion in buffered hydrofluoric acid solution. After standard cleaning, the micro-LEDs were ready to be transfer printed, involving pick-up by an elastomeric stamp and mechanical fracture of the thin anchors (Figure 1(e)). Stamps[14] were made from polydimethylsiloxane (PDMS) by a micromolding technique, and featured pyramidal protrusions at each corner (Figure 1(e)). Molds were fabricated from Si (100) wafers—wet etched to create pyramidal recesses—and cells of SU-8 photoresist to define the main body of the stamp (~100 μm thickness). The completed stamps were peeled from their mold and placed on a cover glass. To improve adhesion and avoid lateral play, melted wax was placed around the stamp and the cover glass edges to create a permanent bond with the custom-made stamp support. This support was then mounted on the magnetic transfer arm of the nanolithography system.[12]

Micro-LEDs were transfer printed in a high-throughput parallel assembly (Figure 2(a)). Each pick-and-place operation can be performed at ~10 s per placement, limited only by the operational speed of the translation stages.[12] Multiple device arrays were transfer printed onto PDMS-coated (~100 μm) polyethyleneterephthalate (PET) substrates (~500 μm), with individual, serial, or parallel electrical addressing schemes. To achieve this, the PET substrate was patterned in the form of a dummy interconnecting circuit that mimics the final metallization mask for alignment purposes during transfer printing.[12] An adhesion-enhancing layer (PDMS, ~50 μm thick) was coated on top of the dummy circuit. Interconnection of multiple devices by metal tracks requires the devices to be electrically insulated. A low-temperature (100 °C) SiO_2 dielectric layer (~350 nm)

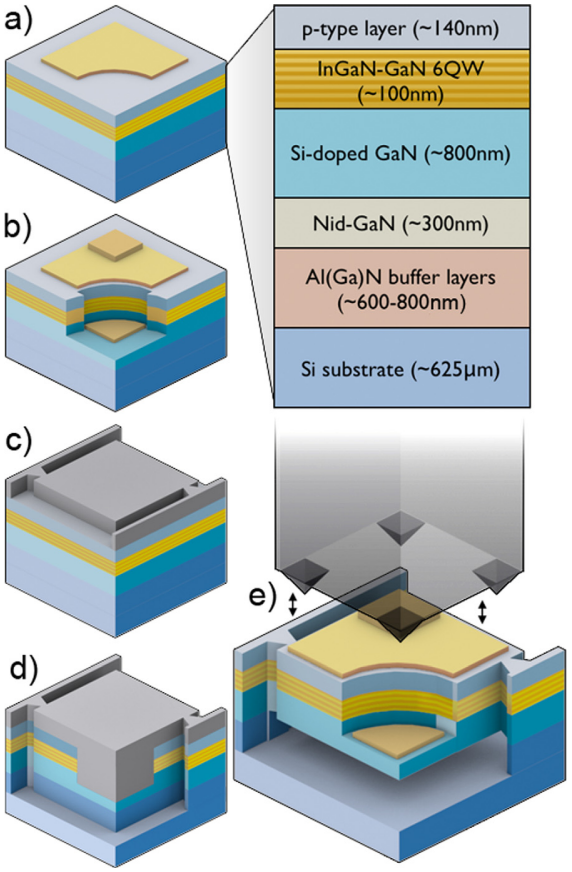


FIG. 1. Schematic of the fabrication process for an individual μLED. The left-hand figure represents (not to scale) the as-grown structure processed as follows: (a) Ni/Au current spreading layer deposition and patterning, (b) n-GaN exposure and opaque Ti/Au metal pad deposition, (c) SiO_2 mask deposition and patterning, (d) deep etching through the epilayers and into the Si substrate, and (e) underetching of the Si substrate yielding devices supported by two sacrificial anchors. The grey overlay above (e) represents the elastomeric stamp.

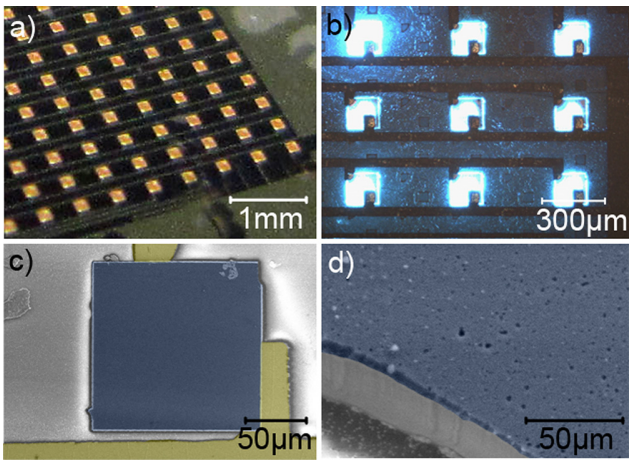


FIG. 2. (a) Optical micrograph of a 16 × 16 transfer printed array of LEDs on PET, (b) close-up of devices under operation, (c) colorized SEM image of the backside (i.e., n-side) of an LED on a finished device, and (d) detail of the indentation at the upper right corner, resulting from breakage of an anchor, and giving a fracture section through epilayers not exposed to the KOH etch. This higher magnification oblique view shows the overall smoothness of the back surface, and the curved fracture surface.

was deposited by PECVD and patterned by RIE to expose the existing electrodes on each device.[12] A patterning step followed to create metal tracks (Ti/Au, thicknesses 50 nm/280 nm), from which the final interconnecting circuit was defined. Finally, the micro-LED array was encapsulated by another PDMS layer and thus can be operated on the PET substrate or peeled-off as a thin PDMS membrane with embedded micro-LED arrays.[12]

Sequential transfer printing yielded a 100% complete array (here, by way of example, a 16 ∼ 16 array), with horizontal and vertical device spacings of 350 μm and 210 μm, respectively (Figures 2(a) and 2(b)). 40 μm wide metal tracks were used to interconnect the elements of the array as seen in Figure 2(b).

Significantly, the backside of underetched devices remains *smooth*, as illustrated by Figure 2(c). Atomic force microscopy over 40 ∼ 40 μm^2 areas indicated typical 0.8 nm averaged root mean square roughness, approaching closely to the resolution limit of the system used. The well-known polarity-specific etch behavior of KOH and similar solutions would normally be expected to have produced a rough surface, featuring hexagonal micropyramidal protrusions, on direct contact with the III-nitride epilayers.[15] It is reasonable to infer here that a thin interfacial SiN_x layer[16] formed during the MOVPE process provided advantageous protection of the III-nitride material from the wet etching.

Figure 3(a) shows the current density versus voltage (*J*–*V*) characteristics from an individual reference micro-LED pixel at various fabrication stages, acquired using needle probes for the steps before connecting to the metal tracks. The initial turn-on voltage of a typical pixel is approximately 2.8 V. With the removal of the supporting Si substrate backplane, yielding a suspended device, this value increased to 3.0 V. Transfer-printing of a device onto a PDMS substrate induced another increase on the turn-on voltage to 3.4 V. This increase in the turn-on voltage is presumably the result of the increase in specific contact resistance during the successive processing steps. However, the differential resistance above turn-on was not significantly affected by these steps. Once the devices were addressed through metal tracks (i.e., in the final transfer-printed configuration) a change in the slope was observed, resulting from the additional series resistance of the tracks. Turn-on voltage was unaffected compared to the previous processing stage.

Figure 3(b) shows a typical optical output power versus current density (*L*-*J*) characteristic, measured using a power meter with a calibrated Si photodiode detector (0.9 cm diameter) placed in close proximity (1.5 cm) to the metal-track addressed LEDs. A Lambertian emission profile was assumed to convert the collected optical power into values quoted for the full forward hemisphere. The LEDs can be driven up to 20 A/cm^2 before thermal roll-over. At this driving current, the total forward optical output power is 80 μW per pixel, corresponding to 355 mW/cm^2 at each device surface. The electroluminescence (EL) spectrum of a single pixel was acquired by an optical fiber-coupled spectrometer (OceanOptics USB4000) aligned with the emitting surface. The emission is centered at 486 nm (∼37 nm full-width-at-half-maximum) and is composed of two major peaks (Figure 3(c)) which are attributable to the high refractive index contrasts between the thin GaN-based epilayers, air and the PDMS substrate,[13,17] causing Fabry-Perot interferences which would not be present if roughening of the backside surface during underetching had been severe.

To assess the high-accuracy positioning capabilities of the system used, devices were placed sequentially in a row on a PET/PDMS substrate (Figure 4(a)). These devices were transfer printed individually from the starting "donor" Si (111) substrate and positioned on the receiving substrate

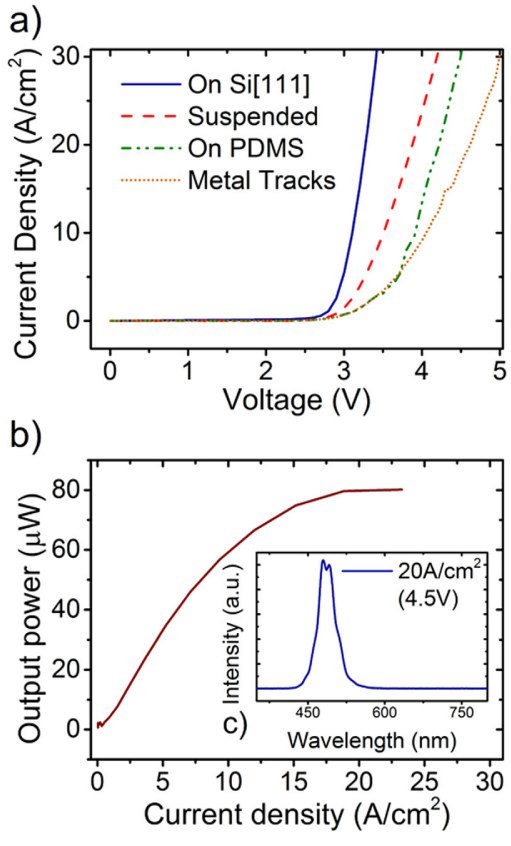


FIG. 3. (a) *J*-*V* characteristics throughout several different processing steps and (b) *L*-*J* performance of a single pixel, with an inset (c) displaying the electroluminescent emission spectrum of a pixel driven at 20 A/cm^2 (4.5 V).

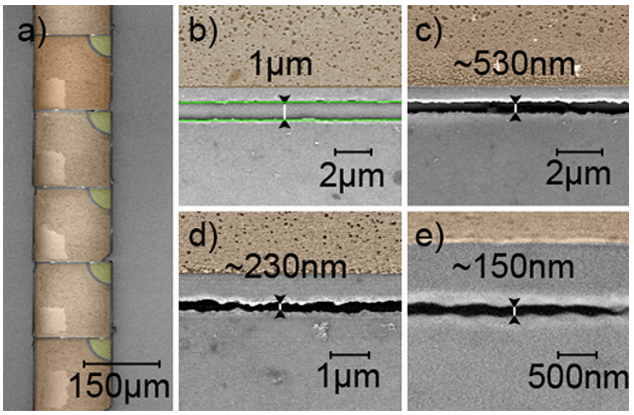


FIG. 4. Colorized SEM imaging of nano-positioned LEDs: (a) Strip of positioned devices, with targeted spacings ranging from 1 μm to 150 nm ((b)–(e)); in (b). An example of the measurement lines (green coloured), fitted to the imaged device boundaries over 30–40 μm distances used to estimate the spacing, is shown.

TABLE I. Comparison between the intended (software input) device spacing and that obtained after the automated transfer positioning, averaged from measurements on three different arrays.

Intended (nm)	Obtained (nm)
1000	1011 (±62.5 nm)
500	530 (±48 nm)
250	230 (±28 nm)
125	150 (±14 nm)
62.5	NA

using a pre-calculated set of coordinates in the system control software. These were chosen to give varied target spacings between the devices, starting from 1 μm, and reducing by successive factors of two down to 62.5 nm.

The effective separation between devices was measured in plan-view by a FEI Sirion™ 200 Scanning Electron Microscope (SEM) (Figure 4) with a large field detector. Although the device sidewalls do not display perfect verticality, oblique-view imaging confirms the slopes are such that the top surface in this orientation represents the point of closest approach. The microscope's image analysis functions were used to measure device separations, specifically by superimposing best-fit linear boundaries on images acquired over typical lateral distances of 30 to 40 μm. The effective spaces between devices were thus measured and confirmed with a set of close-up image acquisitions (Figures 4(b)–4(e)). The measurements as described were repeated on three nominally identical arrays of devices. Numerical results illustrating the high degree of placement accuracy are summarized in Table I.

Deviations from the programmed positions were observed and can be expected due to the viscoelastic behavior of the elastomer stamp used to transport the devices. Specifically we suggest that differences in non-linear relaxation between the four pyramids present on each stamp body, i.e., slightly different retraction rates between pyramids, caused differences in tilt and/or lateral shifts. The minimum 150 nm (±14 nm) spacing attained by our system is presently limited by the side-wall roughness of the LED devices, itself mainly caused by lithography limits and faceting during the exposure to the KOH etch. The peak-to-peak roughness of these side-walls was measured by SEM and found to be higher than the successful minimum placement distance, resulting therefore in devices overlapping each other when attempting to create gaps of 62.5 nm.

In summary, transfer printing with 150 nm (±14 nm) minimum spacing of ultra-thin GaN-based micro-LEDs to mechanically-flexible PET/PDMS substrates was demonstrated. The 2 μm-thick devices were positioned in array configurations by parallel transfer, and were characterized electrically and optically. The devices could be driven up to a current density of 20 A/cm^2 before reaching thermal roll-over and had a turn-on voltage ~3.5 V after transfer. The forward optical output power was up to 80 μW per device, or 355 mW/cm^2 at the device surface. The nanoscale transfer printing accuracy was obtained by using an adapted commercial nano-patterning system, which was shown to be suited for a high-throughput, automated printing process with large-area scalability. This approach is expected to have wide applicability in nano-accuracy heterogeneous integration.

The authors thank Dr P.R. Edwards, University of Strathclyde Department of Physics, for his expert assistance in the SEM imaging and interpretation. This work was supported by EPSRC grants EP/K00042X/1, EP/I029141/1, EP/F05999X/1, and EP/I012591/1.

[1]D.-H. Kim, R. Ghaffari, N. Lu, and J. A. Rogers, Annu. Rev. Biomed. Eng. **14**, 113 (2012).
[2]J. Viventi, D.-H. Kim, L. Vigeland, E. S. Frechette, J. A. Blanco, Y.-S. Kim, A. E. Avrin, V. R. Tiruvadi, S.-W. Hwang, A. C. Vanleer, D. F. Wulsin, K. Davis, C. E. Gelber, L. Palmer, J. Van der Spiegel, J. Wu, J. Xiao, Y. Huang, D. Contreras, J. A. Rogers, and B. Litt, Nat. Neurosci. **14**, 1599 (2011).
[3]S.-I. Park, Y. Xiong, R.-H. Kim, P. Elvikis, M. Meitl, D.-H. Kim, J. Wu, J. Yoon, C.-J. Yu, Z. Liu, Y. Huang, K. Hwang, P. Ferreira, X. Li, K. Choquette, and J. A. Rogers, Science **325**, 977 (2009).
[4]T. Kim, K. Cho, E. K. Lee, S. J. Lee, J. Chae, J. W. Kim, D. H. Kim, J. Kwon, G. Amaratunga, S. Y. Lee, B. L. Choi, Y. Kuk, J. M. Kim, and K. Kim, Nat. Photonics **5**, 176 (2011).
[5]Y. M. Song, Y. Xie, V. Malyarchuk, J. Xiao, I. Jung, K.-J. Choi, Z. Liu, H. Park, C. Lu, R.-H. Kim, R. Li, K. B. Crozier, Y. Huang, and J. A. Rogers, Nature **497**, 95 (2013).
[6]H. Kim, E. Brueckner, J. Song, Y. Li, S. Kim, C. Lu, J. Sulkin, K. Choquette, Y. Huang, R. G. Nuzzo, and J. A. Rogers, Proc. Natl. Acad. Sci. U.S.A. **108**, 10072 (2011).
[7]D.-H. Kim, N. Lu, R. Ghaffari, and J. A. Rogers, NPG Asia Mater. **4**, e15 (2012).
[8]J. Justice, C. Bower, M. Meitl, M. B. Mooney, M. A. Gubbins, and B. Corbett, Nat. Photonics **6**, 610 (2012).
[9]W. Zhou, Z. Ma, W. Yang, S. Chuwongin, Y.-C. Shuai, J.-H. Seo, D. Zhao, H. Yang, and R. Soref, International Conference on Information Photonics (IEEE, 2011), Vol. 4, pp. 1.
[10]J.-H. Ahn, H.-S. Kim, K. J. Lee, S. Jeon, S. J. Kang, Y. Sun, R. G. Nuzzo, and J. A. Rogers, Science **314**, 1754 (2006).
[11]C. A. Bower, S. Member, E. Menard, S. Bonafede, J. W. Hamer, and R. S. Cok, IEEE Trans. Compon. Packag. Manuf. Technol. **1**, 1916 (2011).
[12]See supplementary material-Figure S1-at http://dx.doi.org/10.1063/1.4851875 for an overview of the adapted positioning system, a close-up image of the stages and transferring arm, Figure S2 for a schematic of a flexible device assembly, and a video of the transfer printing of suspended LEDs from their native substrates to a flexible substrate using a 4 × 4 elastomeric stamp.
[13]D. Zhu, C. McAleese, M. Haberlen, C. Salcianu, T. Thrush, M. Kappers, A. Phillips, P. Lane, M. Kane, D. Wallis, T. Martin, M. Astles, N. Hylton, P. Dawson, and C. Humphreys, J. Appl. Phys. **109**, 014502 (2011).
[14]S. Kim, J. Wu, A. Carlson, S. H. Jin, A. Kovalsky, P. Glass, Z. Liu, N. Ahmed, S. L. Elgan, W. Chen, P. M. Ferreira, M. Sitti, Y. Huang, and J. A. Rogers, Proc. Natl. Acad. Sci. U.S.A. **107**, 17095 (2010).
[15]W. Guo, J. Xie, C. Akouala, S. Mita, A. Rice, J. Tweedie, I. Bryan, R. Collazo, and Z. Sitar, J. Cryst. Growth **366**, 20 (2013).
[16]G. Radtke, M. Couillard, G. A. Botton, D. Zhu, and C. J. Humphreys, Appl. Phys. Lett. **97**, 251901 (2010).
[17]D. Zhu, C. McAleese, K. K. McLaughlin, M. Häberlen, C. O. Salcianu, E. J. Thrush, M. J. Kappers, W. A. Phillips, P. Lane, D. J. Wallis, T. Martin, M. Astles, S. Thomas, A. Pakes, M. Heuken, and C. J. Humphreys, Proc. SPIE **7231**, 723118 (2009).

Heterogeneous integration of gallium nitride light-emitting diodes on diamond and silica by transfer printing

A. J. Trindade,[1,*] B. Guilhabert,[1] E. Y. Xie,[1] R. Ferreira,[1] J. J. D. McKendry,[1] D. Zhu,[2,3] N. Laurand,[1] E. Gu,[1] D. J. Wallis,[2,3] I. M. Watson,[1] C. J. Humphreys,[2] and M. D. Dawson[1]

[1]*Institute of Photonics, SUPA, University of Strathclyde, 106 Rottenrow, Glasgow G4 0NW, UK*
[2]*Department of Materials Science and Metallurgy, University of Cambridge, 27 Charles Babbage Road, Cambridge CB3 0FS, UK*
[3]*Plessey Semiconductors Ltd, Tamerton Road, Roborough, Plymouth, Devon, PL6 7BQ, UK*
[*]*antonio.trindade@strath.ac.uk*

Abstract: We report the transfer printing of blue-emitting micron-scale light-emitting diodes (micro-LEDs) onto fused silica and diamond substrates without the use of intermediary adhesion layers. A consistent Van der Waals bond was achieved via liquid capillary action, despite curvature of the LED membranes following release from their native silicon growth substrates. The excellence of diamond as a heat-spreader allowed the printed membrane LEDs to achieve optical power output density of 10 W/cm^2 when operated at a current density of 254 A/cm^2. This high-current-density operation enabled optical data transmission from the LEDs at 400 Mbit/s.

OCIS codes: (250.0250) Optoelectronics; (120.6810) Thermal effects; (060.4510) Optical communications.

References and links

1. H. S. Kim, E. Brueckner, J. Song, Y. Li, S. Kim, C. Lu, J. Sulkin, K. Choquette, Y. Huang, R. G. Nuzzo, and J. A. Rogers, "Unusual strategies for using indium gallium nitride grown on silicon (111) for solid-state lighting," Proc. Natl. Acad. Sci. U.S.A. **108**(25), 10072–10077 (2011).
2. T. Kim, S. Hyun Lee, Y. Li, Y. Shi, G. Shin, S. Dan Lee, Y. Huang, J. A. Rogers, and J. Su Yu, "Temperature- and size-dependent characteristics in ultrathin inorganic light-emitting diodes assembled by transfer printing," Appl. Phys. Lett. **104**(5), 051901 (2014).
3. J. Senawiratne, A. Chatterjee, T. Detchprohm, W. Zhao, Y. Li, M. Zhu, Y. Xia, X. Li, J. Plawsky, and C. Wetzel, "Junction temperature, spectral shift, and efficiency in GaInN-based blue and green light emitting diodes," Thin Solid Films **518**(6), 1732–1736 (2010).
4. Z. G. Ju, S. T. Tan, Z.-H. Zhang, Y. Ji, Z. Kyaw, Y. Dikme, X. W. Sun, and H. V. Demir, "On the origin of the redshift in the emission wavelength of InGaN/GaN blue light emitting diodes grown with a higher temperature interlayer," Appl. Phys. Lett. **100**(12), 123503 (2012).
5. Z. Gong, S. Jin, Y. Chen, J. McKendry, D. Massoubre, I. M. Watson, E. Gu, and M. D. Dawson, "Size-dependent light output, spectral shift, and self-heating of 400 nm InGaN light-emitting diodes," J. Appl. Phys. **107**(1), 013103 (2010).
6. S. Kim, J. Wu, A. Carlson, S. H. Jin, A. Kovalsky, P. Glass, Z. Liu, N. Ahmed, S. L. Elgan, W. Chen, P. M. Ferreira, M. Sitti, Y. Huang, and J. A. Rogers, "Microstructured elastomeric surfaces with reversible adhesion and examples of their use in deterministic assembly by transfer printing," Proc. Natl. Acad. Sci. U.S.A. **107**(40), 17095–17100 (2010).
7. E. James, Mark, Polymer Data Handbook, (Oxford University, 1999), pp. 424.
8. Z. L. Liau, "Semiconductor wafer bonding via liquid capillarity," Appl. Phys. Lett. **77**(5), 651 (2000).
9. D. Zhu, C. McAleese, K. K. McLaughlin, M. Häberlen, C. O. Salcianu, E. J. Thrush, M. J. Kappers, W. A. Phillips, P. Lane, D. J. Wallis, T. Martin, M. Astles, S. Thomas, A. Pakes, M. Heuken, and C. J. Humphreys, "GaN-based LEDs grown on 6-inch diameter Si (111) substrates by MOVPE," Proc. SPIE **7231**, 723118 (2009).
10. D. Zhu, C. McAleese, M. Haberlen, C. Salcianu, T. Thrush, M. Kappers, A. Phillips, P. Lane, M. Kane, D. Wallis, T. Martin, M. Astles, N. Hylton, P. Dawson, and C. Humphreys, "Efficiency measurement of GaN-based

#235263 - $15.00 USD Received 26 Feb 2015; revised 30 Mar 2015; accepted 30 Mar 2015; published 2 Apr 2015

quantum well and light-emitting diode structures grown on silicon substrates," J. Appl. Phys. **109**(1), 014502 (2011).
11. H. R. Shanks, P. D. Maycock, P. H. Sidles, and G. C. Danielson, "Thermal conductivity of Silicon from 300 to 1400°K," Phys. Rev. **130**(5), 1743–1748 (1963).
12. A. J. Trindade, B. Guilhabert, D. Massoubre, D. Zhu, N. Laurand, E. Gu, I. M. Watson, C. J. Humphreys, and M. D. Dawson, "Nanoscale-accuracy transfer printing of ultra-thin AlInGaN light-emitting diodes onto mechanically flexible substrates," Appl. Phys. Lett. **103**(25), 253302 (2013).
13. Y. Li, Y. Shi, J. Song, C. Lu, T. Kim, J. A. Rogers, and Y. Huang, "Thermal properties of microscale inorganic light-emitting diodes in a pulsed operation," J. Appl. Phys. **113**(14), 144505 (2013).
14. R. P. Mildren and J. R. Rabeau, Optical Engineering of Diamond, (Wiley-VCH, 2013), Ch. 2 and 11.
15. C. Kittel, "Interpretation of the thermal conductivity of glasses," Phys. Rev. **75**(6), 972–974 (1949).
16. J. J. D. McKendry, D. Massoubre, S. Zhang, B. R. Rae, R. P. Green, E. Gu, R. K. Henderson, A. E. Kelly, and M. D. Dawson, "Visible-light communications using a CMOS-controlled micro-light-emitting-diode array," J. Lightwave Technol. **30**(1), 61–67 (2012).
17. P. Tian, J. J. D. McKendry, Z. Gong, S. Zhang, S. Watson, D. Zhu, I. M. Watson, E. Gu, A. E. Kelly, C. J. Humphreys, and M. D. Dawson, "Characteristics and applications of micro-pixelated GaN-based light emitting diodes on Si substrates," J. Appl. Phys. **115**(3), 033112 (2014).
18. X. A. Cao, S. F. LeBoeuf, and T. E. Stecher, "Temperature-dependent electroluminescence of AlGaN-based UV LEDs," IEEE Electron Device Lett. **27**(5), 329–331 (2006).
19. MicroChem SU-8 Photoresists datasheet", http://www.microchem.com

1. Introduction

Transfer printing (TP) is a rapidly emerging technique for heterogeneous integration in electronics and optoelectronics [1–5]. In TP, soft elastomeric stamps are typically used to 'pick and place' device structures from their native growth substrate to a dissimilar receiving substrate, allowing the creation of novel hybrid device technologies. An important example of the application of this approach is in printing inorganic light-emitting diodes (LEDs), where pre-fabricated LED membrane devices can for example be transferred onto receiving substrates such as those based on polymers, enabling new forms of flexible displays [6]. As the technique matures and is optimized, thin membranes of suspended LED materials can be achieved in various ways, most commonly by directional wet etching of the growth substrate, here termed under-etching [1], or by laser lift-off [2]. However, a general issue for devices based on epitaxial multilayers is that removal of the substrate eliminates a natural heat-sink retained in conventional fabrication. This issue is severe for the important case of gallium nitride (GaN) based LEDs, in which, despite continuing efficiency improvements, most electrical input energy is dissipated as heat. Even for conventional devices in thermal contact with the growth substrate, operation under direct-current (dc) bias results in undesired thermal effects on the electroluminescence (EL), namely red spectral shifts and reduced optical output power (T-droop effect), while irreversible degradation of devices may also occur [3,4]. Reduction of the die size provides systematic improvement in heat dissipation, but does not eliminate these problems [5]. Heat dissipation from transfer-printed GaN-LEDs becomes a more pronounced issue when flexible polymeric materials are used as the receiver substrate, because these have lower thermal conductivities than inorganic materials used as the native growth substrate. Thermal effects in such a situation have been studied previously [2]. Regardless of the choice of receiver substrate in TP, the process flows normally feature adhesion-enhancement layers on the receiving substrates to aid the release of the LEDs from the transporting stamps [6]. Conventionally, these layers are organic materials, with poor thermal conductivities, κ (e.g. for polydimethylsiloxane (PDMS), κ ~0.15 W/m.K [7]). Therefore adhesion-enhancement layers impede heat dissipation from operating devices even if the underlying substrate has a relatively high thermal conductivity.

The attractive alternative to the use of a conventional adhesion-enhancement layer, which we report in this paper, is to use a transient layer of a volatile liquid [8]. The liquid film aids release of devices from the transporting stamps, as in a conventional process. Subsequently, capillary forces during evaporation of the liquid enable formation of a robust Van der Waals bond between the transferred devices and receiving substrate, with no permanent intermediate layer to add thermal resistance, or changes in refractive index, at the interfaces. This study

#235263 - $15.00 USD Received 26 Feb 2015; revised 30 Mar 2015; accepted 30 Mar 2015; published 2 Apr 2015

utilized high-performance GaN LED epistructures on Si (111) substrates [9,10]. While Si can act as a reasonably effective heat-sinking material in conventional devices (κ ~149 W/m.K [11]), this material is removed during the under-etching fabrication step, using potassium hydroxide (KOH) solution, needed in the TP process flow [12]. We compared two receiver substrates with thermal conductivities much higher and much lower than that of the GaN-based LED die (κ ~160 W/m.K for GaN [13]), namely diamond (κ ~2200 W/m.K [14]) and optical-grade silica glass (κ ~1.42 W/m.K [15]). The benefits of diamond as a heat spreader were investigated by comparing the dc characteristics of LEDs on these two receiver substrates. This part of our study included the use of thermal imaging to infer device operating temperatures, and to observe the transient heating effects under increasing dc drive currents. The ability of LEDs to operate at high dc current densities is also relevant to the emerging application of visible light communications (VLC) with LED sources [16]. In a typical situation where the data signal is superposed on a dc component, the modulation bandwidth of an LED increases with dc current up to a critical point [16,17]. As it is clearly of interest to see how transfer printed devices perform for VLC applications, we undertook comparison of the modulation bandwidths and data transmission characteristics of devices on diamond and silica.

2. Experimental results

We report the TP in array formats of 100x100 μm^2 LEDs (micro-LEDs) emitting around 465 nm onto single-crystal diamond platelets [14] (200 μm thick) and fused silica substrates (500 μm thick). We concentrate on LEDs of such small dimensions here by reason of applications described later in the paper, but note that scaling to larger areas [2] should in principle be possible if strain compensation issues specific to GaN/Si are addressed. The GaN micro-LED structures and process flow, together with the mechanical transfer system and PDMS stamps, are as described previously [12]. Here, however, capillary bonding was achieved by introducing an intermediate step to the TP process, in which the backside of the devices being transferred is wetted with a suitable liquid as shown in Fig. 1.

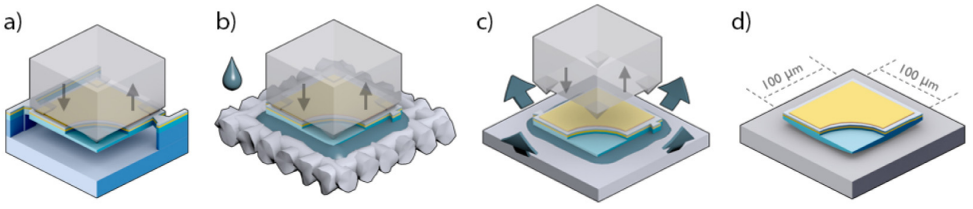


Fig. 1. Schematic of transfer printing using capillary bonding. The left-hand figure represents the pick-up of a suspended device using an elastomeric stamp (a). Upon pick-up, LEDs are compressed against an acetone-wetted cloth (b) and released when the backside contacts receiving substrate (c). The excess of liquid aids the positioning and release of the LED from the transporting stamp. After thermal curing, the LED is bonded to the new substrate (d).

After pick-up from the donor wafer as per Fig. 1(a), the backside is wetted on an acetone-impregnated standard cleanroom wipe as shown in Fig. 1(b). Quick retraction of the stamp removes the LED die from the wipe with its backside still wet, and it is then deposited onto the receiver substrate, shown in Fig. 1(c). The transparency of the stamps allows the TP process to be followed visually, and Fig. 2(a) confirms overflow of excess liquid to the sides of the LED die when it is compressed against the receiving substrate. Slow retraction of the stamp causes the liquid to partially reflow back underneath the die, and provide initial adhesion between the die and the receiving substrate, through liquid capillarity. This stage is shown in Fig. 2 (b). Subsequent evaporation of liquid proceeds from the outside of the die, and during this step the forces at the retreating meniscus bring the two surfaces into intimate contact [8]. While no specific tests have been performed at this time to assess the placement

#235263 - $15.00 USD Received 26 Feb 2015; revised 30 Mar 2015; accepted 30 Mar 2015; published 2 Apr 2015

accuracy in detail, the LEDs are printed using the same mechanical system we have previously shown to be capable of sub-micrometer placement [12], and we note that the printed dies hold their positioning during slow stamp retraction and later after the solvent has been evaporated.

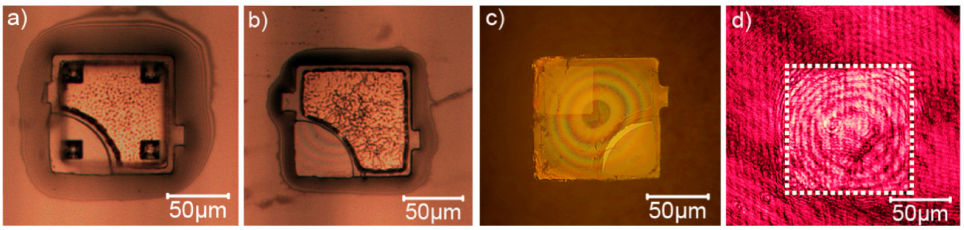


Fig. 2. Images illustrating the process of capillary bonding of individual LEDs onto rigid substrates. Parts (a) and (b) are optical microscope views through the transparent stamp at successive stages: (a) after wetting of the LED backside, contact is made with the receiving substrate; (b) stamp retraction allows the liquid to reflow underneath the LED. Parts (c) and (d) are views through the substrate showing interference effects from an air gap left round after liquid evaporation and bonding in the central region: (c) colored fringes visible under white light; (d) fringes observed under laser light.

After moderate heating to 50°C to evaporate any remaining liquid, the devices are left bonded by Van der Waals forces over the contact area with the receiving substrate. Both combinations of surfaces brought into contact (i.e. diamond or silica substrates, and the micro-LED backside) display similar root-mean-square roughness values of ~1 nm as measured by atomic force microscopy (AFM). We have previously attributed the smoothness of the micro-LED bonding surface to a protective SiN_x layer formed between the Si substrate and the AlN growth initiation layer [17]. This layer can largely protect the underside of the III-nitride die from attack by the KOH etch solution used to remove the Si substrate. Such low roughness results in two tightly-bonded surfaces robust to mechanical disturbance, and surviving multiple wet-processing steps necessary to complete the device fabrication. However, imaging of the devices through the back of the receiving substrate reveals a pattern of interference rings associated with an air gap as shown in Fig. 2(c) and 2(d). This observation correlates with curvature of the LED dies, which limits contact to the central region of the LED. Such curvature is reasonable to expect after removal of the Si substrate beneath the LED epistuctures. The epistructures are engineered such that the total epi-layer/Si substrate system is approximately strain balanced. This requires compressive strain to be introduced into the AlGaN buffer layers using lattice mismatch to counteract the tensile strain introduced by the thermal expansion difference between the nitride layers and the Si substrate on cooling from the growth temperature. After removal of the Si substrate this residual compressive strain in the AlGaN buffer layers then induces the concave curvature seen, as it acts against the topmost GaN layers in the LED stack.

The method to investigate the observed curvature of the LED dies after deposition used the imaged interference rings under monochromatic and coherent (653nm-emitting laser diode) light, exemplified in Fig. 2(d), and standard analysis of optical interference. The height of the die-substrate air gap was spatially reconstructed, allowing visualization of the backplane curvature over a full die as illustrated in Fig. 3(a). Essential information regarding the die positioning and tilting can be obtained from such measurements. The effective contact area, corresponding to the colorless mesh in Fig. 3(a), in the central region of a sample LED was found to be 14 ± 2% of the total die area and a radius of curvature averaging 2 mm per die (assuming a spherical curvature).

#235263 - $15.00 USD Received 26 Feb 2015; revised 30 Mar 2015; accepted 30 Mar 2015; published 2 Apr 2015

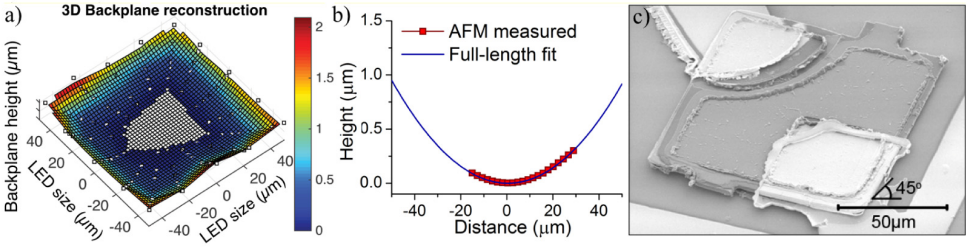


Fig. 3. Backplane curvature measurements. In (a), the calculated height of the air gap between a bonded LED and the substrate is represented as a mesh reconstructed by the photographed interference pattern. The colorless central area indicates where contact is assumed to occur. In part (b), an AFM line scan over the central area of an unbonded LED die is shown and extrapolated with a parabolic fit. Part (c) shows an SEM image of a micro-LED transfer printed onto a rigid substrate (at 45° tilt), and connected to Ti/Au metal tracks.

To further analyze the backplane curvature, an AFM profile scan was performed (45μm in length) on a flipped-over die where the central area was measured and fitted over the entire lateral size of the die as shown in Fig. 3(b). By zeroing the measurement to the minimum height as the center of the backplane curvature, the AFM height scan matches the interference rings height reconstruction for the area surrounding the center of the die (with ± 2 μm lateral fluctuations). However - towards the edges of the reconstructed backplane - higher curvature zones can be seen as per Fig. 3(a), indicating that the radius of curvature is not constant. SEM imaging provided a qualitative assessment of the height at the extremities of ~2.5 μm closely matching the values attained by the interference-based measurements.

To act as an electrical insulation layer and encapsulation for the devices on diamond and silica receiver substrates, an SU-8 epoxy photoresist layer of 10 μm post-cure thickness was deposited and patterned. Metal tracks, comprising 200 nm of Au above 50 nm of Ti, were deposited next, contacting the LED through localized apertures in the SU-8. The media surrounding LED dies in such a situation are shown in the right-hand part of Fig. 4(a).

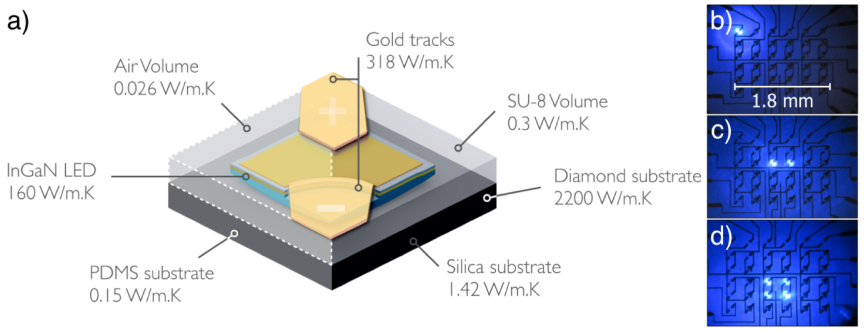


Fig. 4. Thermal conductivities of media surrounding the respective transfer-printed LEDs (a): The left half-section of the device illustrates the air-exposed baseline devices deposited on PDMS adhesion enhancement layers. The right half-section represents the case of the better performing substrates (diamond and silica) with improved heat dissipation and volumetric SU-8 (κ ~0.3 W/m.K [19]) encapsulation on top. Full device arrays can be seen in the microscope images in parts (b), (c) and (d) with configurations of 1, 2 and 4 active LEDs respectively.

As well as introducing the capillary-assisted TP of LEDs onto diamond and silica, we also fabricated for reference identical device structures onto PDMS/polyethylene terephthalate (PET) flexible substrates as previously demonstrated [17]. The media surrounding dies in this case are shown in the left-hand part of Fig. 4(a). 6x6 device arrays were assembled onto each substrate with alternative LED driving configurations as pictured in Fig. 4(b)-(d).

#235263 - $15.00 USD Received 26 Feb 2015; revised 30 Mar 2015; accepted 30 Mar 2015; published 2 Apr 2015

Figure 5 shows the operating voltage (V) and the optical output power density (L) of three representative LEDs as a function of the current density (J). L-J curves were acquired with the devices in direct contact with a calibrated Si photodiode detector, capturing only the light going through the supporting substrate. Characteristics of a reference micro-LED bonded to a PET polymer substrate with a 20-µm PDMS intermediate adhesion layer are included for comparison with those of the devices on diamond and bulk silica substrates. The devices on the PDMS/PET substrates were in direct thermal contact with air on one side, while those bonded to the inorganic receiver substrates were encapsulated with SU-8 epoxy as described above. The reference devices operated at a maximum drive current density of 30 A/cm^2, producing an optical output power density of 55 mW/cm^2 before permanent damage was observed. This limited performance is attributable to a poor environment for heat dissipation. The media on opposite sides of the LED dies, air and PDMS, both have lower thermal conductivities than their counterparts in the encapsulated devices bonded to inorganic substrates. LEDs on all three substrates display similar turn-on voltages (~4.5 V), indicating good ohmic contacts, and effective performance from the thin metal current-spreading layer over the p-GaN. A maximum current density of 255 A/cm^2 was measured without significant thermal roll-over on diamond substrates, representing a major improvement when compared to similar devices on soft intermediate layers (~30 A/cm^2) [2,12] .

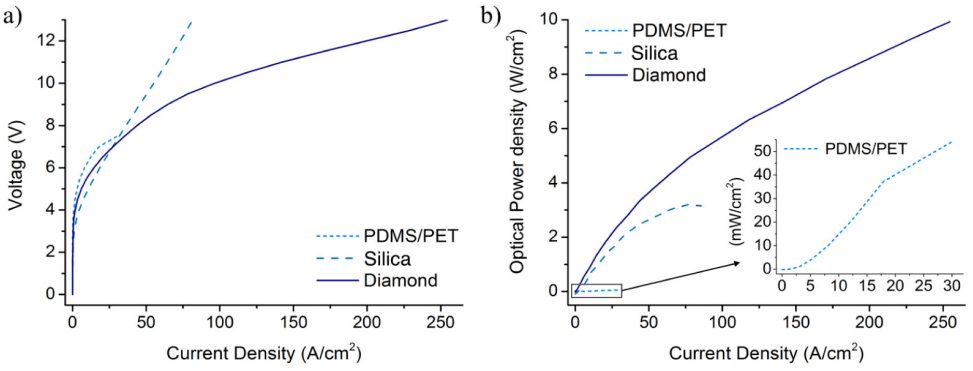


Fig. 5. Characteristics of an individual LED in operation on different substrates. In (a), J-V curves for individual LEDs on PDMS/PET, silica and diamond substrates, respectively. In (b) the corresponding L-J with the inset showing a magnification of the device emission on the PDMS/PET substrates used as a baseline comparison achieving a maximum optical power density of 55 mW/cm^2.

The maximum values for optical power density in Fig. 5 for devices on inorganic receiver substrates were 10 W/cm^2 at 255 A/cm^2 (I = 20 mA) and 3.2 W/cm^2 at 77 A/cm^2 (I = 6 mA) for devices on diamond and silica respectively. LEDs on silica gave a maximum optical power inferior to their counterparts on diamond, and started to reach saturation from thermal rollover after 78 A/cm^2. However, repeated drives up to 80 A/cm^2 showed no damage to the LEDs, in contrast to the irreversible damage suffered by devices on PDMS/PET above 30 A/cm^2. LEDs on diamond consistently outperformed those on the other substrates, due to its orders of magnitude higher thermal conductivity. The maximum optical power density *per* LED (10 W/cm^2) was nearly three times higher than that obtained from devices on silica. This represents a significant advance, outperforming previously reported transfer-printed devices with an equal die size by a factor of 10 [2].

To better understand how the two very different thermal conductivities of diamond and silica affected the device performance, the temperature distribution across LED arrays was measured with a calibrated thermal infrared camera, viewing through the substrate [Fig. 6(a)] and focusing on the plane of the LEDs. The camera acquisitions accounted for the emissivity of the GaN in the wavelength range of 1.5 to 5µm and the false-color representation of

#235263 - $15.00 USD Received 26 Feb 2015; revised 30 Mar 2015; accepted 30 Mar 2015; published 2 Apr 2015

temperature is referenced to the emissivity of GaN. The images show semi-quantitatively the much greater effectiveness of heat spreading in the array on diamond. At the highest current density no hot spots are evident, in contrast to the hot spot around the powered LED on glass, and there is a comparable temperature rise across the full diameter (3 mm) of the diamond substrate.

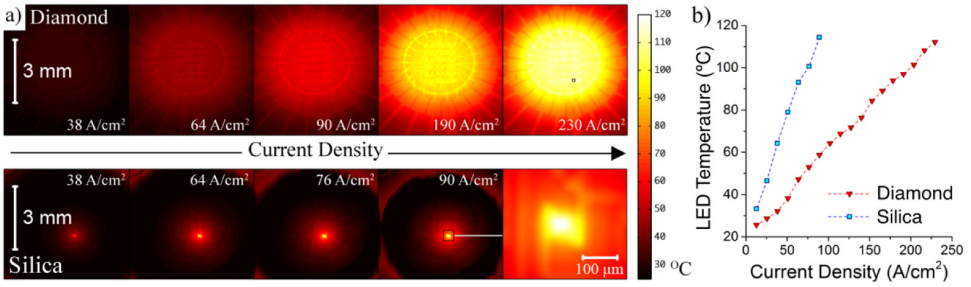


Fig. 6. (a) Thermal imaging of LED arrays with a single device powered on diamond (top) and silica (bottom). The emitting LED is identified in the last diamond frame as a black dot. The last frame of the silica-substrate row shows a magnified view of the die and its metal interconnection tracks. The captured images show the measured temperature corrected for the LED material (GaN); the rest of the image should be interpreted as a relative comparison. Part (b) shows the dependence of LED temperature on the injected current density (see Media 1).

Figure 6(a) also suggests the apparently enhanced temperature rise along the metal interconnection tracks. This is considered to be mainly an artifact arising from the metal emissivity and the calibration procedure, although a significant role for aluminum interconnection tracks in lateral heat transport in similar LED arrays has been proposed and simulated previously [1]. Figure 6(b) shows estimates of the temperature of the powered LED die as a function of drive current density for the two substrates, and shows an approximate linear dependence in each case. Devices are estimated to reach a maximum operating temperature of ~115°C. This is reached by devices on silica at an injection current density of 90 A/cm^2. LEDs on diamond attain a similar temperature only at 230 A/cm^2, a current density 2.5x higher. Representative heat-propagation visualization is available (see Media 1) showing real-time heat propagation with 1mA current increments on both substrates.

The very different heat-spreading properties of diamond and silica are expected to affect the spectral shifts shown by LEDs operating at different dc drive currents. Therefore electroluminescence spectra were recorded with a fiber-coupled spectrometer. Figure 7 shows how the peak EL wavelength shifted, and the inset illustrates typical spectra at relatively low current density. The peak EL emission of the transfer-printed devices shifted over a full range of 464 to 455 nm ($\Delta\lambda$ = 9 nm) and of 463 to 459 nm ($\Delta\lambda$ = 4 nm) on diamond and silica, respectively. The corresponding injected current densities ranged from 12 to 100 A/cm^2 for silica, and to a maximum of 256 A/cm^2 for diamond. In the case of LEDs on silica, the peak wavelength blue-shifts initially, with a reversal to a red shift above 50 A/cm^2 as similar to other reports of InGaN/GaN based LEDs [8]. The blue shift in polar (0001)-oriented device structures, as used here, are usually attributed to carrier screening by piezoelectric fields in the quantum well (QW) active region. Localized heating meanwhile causes strong competitive red shift effects - including bandgap shrinkage - which become dominant at higher injected current densities [8] and due to the devices own self-heating effects [10].

#235263 - $15.00 USD Received 26 Feb 2015; revised 30 Mar 2015; accepted 30 Mar 2015; published 2 Apr 2015

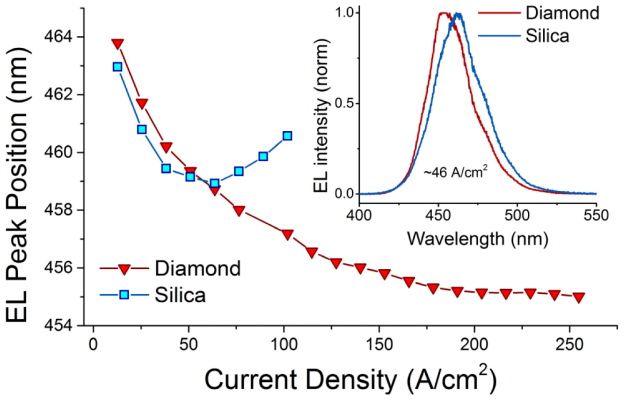


Fig. 7. EL peak shift of a representative single LEDs as a function of increasing injected current on diamond (red triangles) and silica (blue squares). The inset shows representative EL spectra at 46 A/cm2 for both substrates.

In the case of LEDs on diamond, a continuous blue shift is the net observable trend. Because these devices reached similar temperatures to those on silica at the highest current densities, the bandgap shrinkage contribution will be similar. It is likely that strain effects in the QWs, associated with thermal expansion mismatches between the III-nitride dies and underlying substrate, play a role in the markedly different spectral shift behavior [9]. The transition observed from initial blue shifts to red shifts parallels several previously published reports, which discuss contributing mechanisms in more depth, and their investigation with a wide range of techniques [2–4,18].

The combination of LED die sizes 10-100 times smaller in area than those of typical commercial GaN-based devices, and the ability to sustain high dc current densities through effective heat dissipation on diamond, motivated further fast-modulation measurements relevant to visible light communications (VLC) applications. A key parameter for VLC is the electrical-to-optical (E-O) modulation bandwidth (BW), which is conventionally measured using a −3 dB criterion. A small LED size naturally enhances BW by minimization of capacitive contributions, but a decrease in the differential carrier lifetime in GaN-based QWs as carrier density rises also gives a significant increase in BW with current density [16]. BW measurements on transfer-printed devices were acquired in a similar fashion to that reported elsewhere, applying a modulation signal on a constant dc bias [16]. Figure 8 shows the expected initial increase of BW with current density for devices on both diamond and silica.

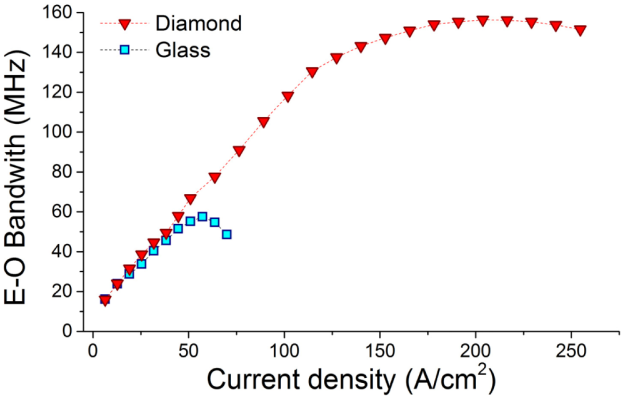


Fig. 8. E-O bandwidths as a function of dc drive current density of representative LEDs deposited onto diamond and silica.

#235263 - $15.00 USD Received 26 Feb 2015; revised 30 Mar 2015; accepted 30 Mar 2015; published 2 Apr 2015

Devices on both silica and diamond displayed similar performance for current densities under 50 A/cm^2. Above this point roll-over became evident for devices on silica, which are thus limited to a maximum BW of ~55 MHz. The BW of devices on diamond continued to increase at much higher current densities, and to plateau at 200 A/cm^2, corresponding to a maximum BW of 154 MHz. These maximum observed BW values, which establish a performance benchmark for transfer printed devices for optical communications, that could be further improved by fabricating smaller LEDs for use in the TP process. Interesting comparisons can also be made between the results in Fig. 8, and previous BW measurements on micro-LEDs fabricated from similar epitaxial material, but tested on the Si growth substrate [17]. These were circular in shape, and of 45 μm diameter. The previous non-transferred devices attained BWs of 190 MHz at relatively low current densities around 6 A/cm^2. However, they displayed an unusual temporary saturation of bandwidth increase in this current density range, before moderate further BW increases at higher current densities attributed to heating effects, and associated lowering of series resistance [17]. The smoother initial BW increase with current density shown by the transfer-printed devices resembles typical results from conventional GaN-on-sapphire devices [16]. These observations suggest that alteration of the strain state of QWs by removal of the Si substrate may influence the recombination dynamics of carriers significantly.

To further demonstrate the potential of the transfer-printed devices for VLC, tests were made of the optical transmission of data in a back-to-back configuration. The resulting eye diagrams are shown in Fig. 9. A simple on-off keying modulation scheme was used with a dc bias for the device on diamond of 10.5 V, and of 5.7 V for the device on the silica. A peak-to-peak modulation of 2 V was used in both configurations, and pseudo-random sequences of 2^7-1 bits were employed, as in previous work [16].

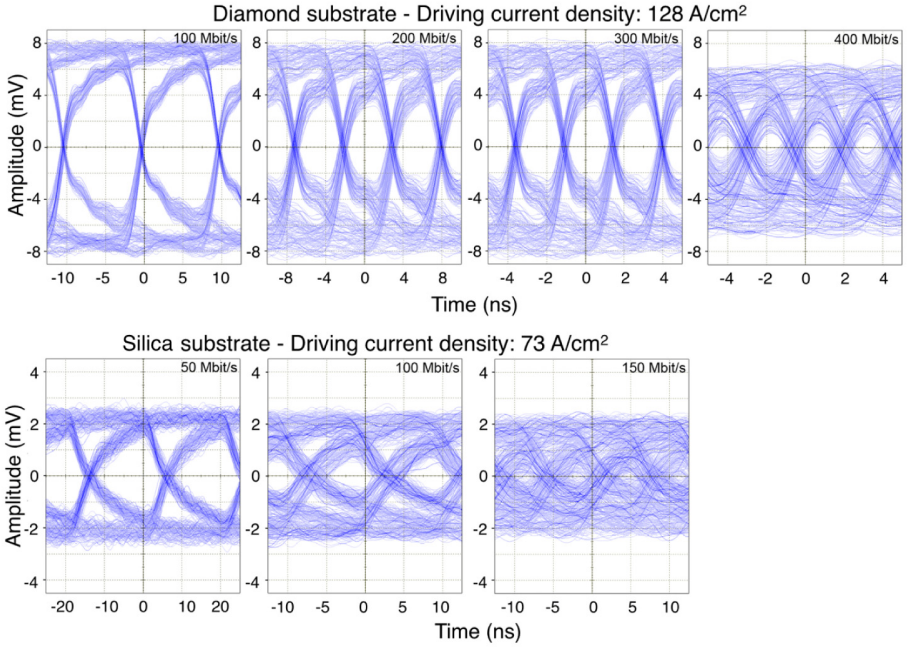


Fig. 9. Data-transmission measurements from representative LEDs deposited onto diamond (top row) and silica (lower row). The eye diagrams were acquired with the same dc applied current throughout.

Devices on diamond displayed open eye diagrams at data-rates up to 400 Mbit/s, correlating with error-free data transmission. In contrast, devices on silica showed eye closure

#235263 - $15.00 USD Received 26 Feb 2015; revised 30 Mar 2015; accepted 30 Mar 2015; published 2 Apr 2015

above 100 Mbit/s, which was virtually complete at 150 Mbit/s. The superior performance of the devices on diamond is again ultimately attributable to this material's effectiveness as a heat spreader, allowing operation of the LEDs at higher dc current densities.

3. Summary

Micro-transfer printing combined with liquid capillary bonding is demonstrated as a technique to directly integrate active device membranes to novel rigid substrates without adhesive interlayers. The technique retains the scalability and potentially nanometer positioning accuracy we have demonstrated previously [12], but brings additional benefits in direct contact to functional substrates including those possessing high thermal conductivity. As an important example of the use of this technique, the electrical and optical characteristics of 100 x 100 μm^2 blue-emitting GaN LEDs transfer printed in array format onto diamond and silica receiver substrates are compared, and demonstrate the major benefits of diamond as a heat-spreading material. Devices on diamond were driven at dc current densities up to 254 A/cm^2 without reaching thermal roll-over, or suffering permanent damage. A maximum optical output power density of 10 W/cm^2 was recorded from devices on diamond substrate, which is more than three times the optical power density of counterpart devices on silica (3.2 W/cm^2). The response of the devices to fast modulation, involving superposition of a data signal on a dc offset, was also studied, motivated by applications in optical data transmission. The effective heat dissipation offered by diamond allowed devices to attain maximum electrical-to-optical modulation bandwidths of 154 MHz at dc current densities of ~200 A/cm^2. The same devices achieved a highly competitive back-to-back data transmission rate of 400 Mbit/s at a dc current density of 128 A/cm^2.

The LED structures used in this study were optimized for conventional large-area LED fabrication, where the wafer-scale properties are most important. In future studies we will investigate how the strain profile in the layer stack can be modified to reduce the curvature of the micro-LEDs and improve the contact area, which should bring further benefits to the optoelectronic performance of the devices. We note finally that our technique of LED transfer printing onto diamond has the potential to take advantage of commercial-scale polycrystalline diamond substrates or the cost-economies to be expected from scaled up single-crystal CVD growth of diamond.

Acknowledgments

The authors thank Dr. P.R. Edwards, University of Strathclyde Department of Physics, for his assistance in the SEM imaging acquisition, and Dr. Anthony Kelly and Scott Watson, University of Glasgow, for support in the data transmission and bandwidth measurements. This work was supported by EPSRC grants EP/K00042X/1, EP/I029141/1, EP/F05999X/1, and EP/I012591/1.

Appendices

Apendix A:

NLP 2000 nanolithography system datasheet

Desktop Nano Lithography Platform System (NLP 2000)

User Friendly, Desktop Nanolithography Platform

NLP 2000 System is a user-friendly and easy to operate desktop nanolithography instrument capable of depositing a wide variety of materials with sub-micron accuracy and precision. With MEMS devices and deposition protocols with the NLP 2000 System's printing and automation software, users can create custom patterned substrates in under an hour. It is designed to serve the increasing need for large area depositions of nanoarrays, this Dip Pen Nanolithography-based system is the first system capable of fabrication of sub-micron features over large substrates. With a dynamic range of deposited features sizes ranging from sub-100 nm to over 10 µm, the NLP 2000 brings truly unique capabilities to the world of nanofabrication. It is an ideal instrument for nano-engineering and biomaterials applications which require 1-10 micron printing and imaging capabilities, such as:

- Multiplexed protein printing
- Biosensor functionalization
- Cell micro and nanopatterning studies
- Polymer patterning, including ethylene glycol and acrylic

Features and Benefits

Along with the ability to create patterns of nano- to micron-scale features from many materials, benefits of the NLP 2000 System include:

- Rapid fabrication of multi-component patterns with 1-10 micron feature sizes
- Automated, precise, co-planar patterning of areas as large as 40 mm x 40 mm
- Functionalization of pre-existing microstructures
- Process monitoring & control using high resolution optical microscopy & environmental chamber
- User-friendly software
- Materials deposition protocols

Advanced Creative Solutions Technology, LLC.
200 Howard Ave Suite # 236, Des Plaines, IL 60018 P: 630-780-6407 F: 630-423-9581
clienteservice@acs-t.com
www.acs-t.com

Standard Components

- NLP 2000 System stage, optics, and controller
- M-type Multiprobe Arrays, Reservoirs, and substrates
- Getting Started Guide, User Manual & CD
- 1 year warranty, parts & labor
- Localized environmental chamber
- Integrated vibration isolation feet
- Extended Limited Warranty, 1 year

Automated, Precise Patterning of Large Areas

In addition to a large 40 mm x 40 mm XY stage, The NLP 2000 System includes everything needed for users to begin to rapidly pattern large surface areas after only minimal training. The NLP 2000's three encoded piezo-driven linear stages (XYZ) and 2 encoded goniometer stages (Tx and Ty) make precise, rapid, large area patterning repeatable. Automated leveling controls, standard patterning routines, and software scripting capabilities simplify, control and automate long deposition runs.

Microstructure Functionalization

Using the NLP 2000 System's high resolution stages, sub-micron optical resolution and simple patterning interface, scientists can easily functionalize sensors, sensor arrays, microcontact printing stamps, microfluidic devices, or other pre-fabricated microstructures. The NLP 2000 System easily resolves features less than a micron in size, enabling system alignment to these pre-fabricated microstructures.

Controlled Patterning Environment

To fully monitor & control the patterning process, the NLP 2000 System features a high resolution optical microscope, and environmental chamber, and vibration isolation. Integrated environmental controls allow the user control and log temperature, humidity, and other unit parameters for immediate or subsequent analysis and correlation with printing. In addition, the NLP 2000 is compatible with commercial passive and active vibration isolation tables.

System Specifications

High Resolution Stage Specifications					
Description	**X-axis**	**Y-axis**	**Z-axis**	**Tx**	**Ty**
Range	50 mm	50 mm	10 mm	± 5°	± 5°
Encoder Resolution	5 nm	5 nm	5 nm	0.15 mDeg	0.15 mDeg
Stage Repeatability(High Resolution Mode)	± 25 nm	± 25 nm	± 75 nm	± 0.25 mDeg	± 0.25 mDeg
Stage Repeatability (Low Resolution Mode)	± 150 nm	± 150 nm	± 75 nm	± 0.25 mDeg	± 0.25 mDeg

Imaging Control Specifications					
Optical Imaging Specifications	10X Objective M Plan APO	Optical resolution < 1 um	Motorized digitally controlled zoom and focus	Digitally controlled halogen illumination system	0% zoom: 844 x 629 um^2 100% zoom: 143 x 110 um^2

Environmental Control Specifications					
Localized Environmental Control	Software controlled temperature & humidity	Heating temperature range: (ambient + 20°C)	Cooling temperature range: (ambient - 2°C)	Temperature stability: +/- 0.5 °C	Humidity range: (10-90% RH) Humidity stability: +/- 0.5% RH

Patterning Specifications	
Throughput	System throughput is application-dependant; typical examples for printing an array of 2 micron protein spots spaced 10 microns apart with various multi-"pen" tip arrays, assuming re-inking every 10 spots:

"Pen" Type	*"Pen" Tips/ Array*	*Time (min)*	*Patterned Area (mm^2)*	*Number of Spots*
12 pen M-type array	12	30	0.1	1,000
48 pen M-type array	48	30	0.4	4,000

Feature Size	100 nm – 10 microns
Coefficient of Variation	5-20% consistency (depends on printing material & protocol optimization)
Leveling	Stage leveling wizard
Optical Pattern Registration to Substrate	1 micron

Software Specifications					
Pattern Design	Patterning of orthogonal dots and lines	Arrays of dots and lines	Inkmap import of Bitmaps	Pattern preview window	Inkmap for import of bitmap patterns
Feature Size Control	User defined dot dwell time; user defined line patterning speed				
Stage Movement	XYZ increments preset or user-defined	Tip & Tilt increments preset or user-defined	Ability to capture and store X, Y, Z, Tx and Ty stage positions	Tip approach	Tip retract safe position
Pen Array/Sample Leveling Routines	Leveling using 3 point capture to optically define the substrate surface plane				

Consumables, Printing Materials & Substrates

Multi-pen Arrays & Reservoirs

Arrays of "pen" tips are optimized for DPN deposition of one or more printing materials in large-area patterns. "Pen" tip arrays are made of silicon nitride and contain A-frame and diving board shaped cantilevers. "Pen" tips are loaded using Inkwell reservoirs.

Printing Materials & Substrates

The NLP 2000 System is capable of depositing and imaging molecular materials and liquids with viscosities ranging from 1-20,000 cP on variety of substrates.

Supported printing materials:

- Proteins
- Nucleic acids
- Antigens
- Lipids
- Nanoparticles
- Polyethelyne glycol
- UV-curable polymers
- Heat-curable polymers
- Glycerol
- Silanes

Compatible substrates:

- Silicon
- Silicon dioxide
- Silanized surfaces
- Amine functionalized slides
- Metals
- PDMS
- Hydrogels
- Polystyrene
- Catalysts
- Thiols

Proven Protocols and Support

Leveraging years of experience and expertise in nanolithographic techniques and applications, ACS Technology is committed to developing and thoroughly testing deposition protocols for a multitude of scientifically important materials (including DNA, hydrogels, polymers, silanes, thiols, and nanoparticles). These protocols, and accompanying inks, substrates and pens, are made available to NLP 2000 customers, and are accompanied by a variety of levels of customer support including e-mail, phone, remote desktop, on-site, and forums.

Ordering Information

Item Name: System, NLP 2000
Part #: E-A1004

Learn more about ACS Technology products and services at www.acs-t.com. Or call us at 847-813-5042.