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Control of an H-bridge Modular Multilevel Converter for Reliable Operation of DC Transmission Systems

by

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This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

Signed: Chao Chen

Date: 27/06/2014

Dedicated to my family

Abstract

This thesis presents improved modulation and control schemes for an H-bridge modular multilevel converter (MMC) that can be used to enhance the transient response of DC transmission systems. The schemes enable H-bridge MMC cell capacitor voltages to be regulated independent of the DC link voltage in a DC transmission system, and also permit operation with variable DC link voltage, down to zero voltage, with full control over active and reactive power exchange. The proposed schemes also offer protection functionality during a pole-to-pole DC fault by restraining the DC fault current magnitude in the converter arms to a level compatible with the current rating of the converter switching devices. The modulation and control schemes use the perturbations in the cell capacitor voltages and common mode currents of an individual phase to eliminate the second-order harmonics from each converter arm. This is achieved without a dedicated controller for suppression of the second-order harmonics. The validity of the proposed modulation and control schemes is confirmed using simulations and experimentation in open and close loop using a scaled down H-bridge MMC. Their viability in DC transmission systems is assessed using simulation of point-to-point and multi-terminal DC networks; this includes power transmission with reduced DC link voltage and survival from permanent and temporary DC faults with DC link controlled recharging following fault clearance. The major practical implication of the proposed modulation and control schemes is that they offer the possibility for voltage source converter based DC transmission systems to ride-through DC faults without the need for expensive and fast DC circuit breakers, as is being pursued by HVDC manufacturers. This thesis demonstrates the possibility of operation without converter blocking, without risk of converter damage from excessive current stresses. In this manner, a converter station of the DC transmission system can be used during a DC fault to provide voltage support to an AC grid.

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List of Symbols

C	Capacitance of cell capacitor (μF)
i_1	Upper arm current (A)
i_2	Lower arm current (A)
i_{1sav}	Average current through each cell capacitor of the upper arm (A)
i_{2sav}	Average current through each cell capacitor of the lower arm (A)
i_{abc}	Grid current matrix in *abc* frame (A)
i_{arm}	Arm current (A)
i_{dc}	Common mode current (A)
i_{dqo}	Matrix of transferred current vectors in *dqo* frame (A)
I_m	Magnitude of the H-bridge MMC output current (A)
i_o	H-bridge MMC output current (A)
i_{si}	Transient current of the i^{th} H-bridge cell (A)
K	*abc* frame to *dqo* frame matrix transfer function
K_{1av}	Average switching states of the upper arm cell
K_{2av}	Average switching states of the lower arm cell
k_i	Integral gain of the common mode current control loop
$K_i(t)$	Transient switching states of the i^{th} H-bridge cell
k_p	Proportional gain of the common mode current control loop
L	Load inductor (H)
L_a	Inductance of the arm reactors (H)
m	Modulation index
m_a	AC component of the upper and lower arm voltage references
m_{abc}	AC components matrix of arm voltage references in *abc* frame
m_d	DC component of the upper and lower arm voltage references
R	Load reactor (Ω)
R_a	Resistance of the arm reactors (Ω)
R_s	DC link resistance (Ω)
u_{dqo}	AC components matrix of arm voltage references in *dqo* frame
v_1	Upper arm voltage (V)

v_2	Lower arm voltage (V)
v_{1c}	Cell capacitor voltage of upper arm (V)
v_{2c}	Cell capacitor voltage of lower arm (V)
v_{abc}	Grid voltage matrix in *abc* frame
V_c	Sum of the upper and lower arm voltages (V)
v_{cell}	Output voltage of each cell (V)
v_{ci}^{n}	n^{th} harmonic component of cell capacitor voltage (V)
V_{DC}	DC link voltage (V)
v_{dqo}	Matrix of transferred voltage vectors in *dqo* frame
v_g	Grid voltage (V)
V_m	Magnitude of the grid voltage (V)
v_o	Converter output voltage (V)
α_i	Integral gain of the fundamental grid current control loop
α_p	Proportional gain of the fundamental grid current control loop
β_i	Integral gain of the cell capacitor voltages controller
β_p	Proportional gain of the cell capacitor voltages controller
δ	Phase angle difference between AC grid voltage and current (*rad*)
φ	Power factor
τ_c	Time constant for off-grid condition
ω	Angular velocity (*rad/s*)

List of Abbreviations

AC	Alternative Current
APR	Active Power Regulator
BPWM	Bipolar Pulse Width Modulation
CCC	Capacitor-Commutated Converter
CSC	Current Source Converter
DC	Direct Current
DCVR	DC Voltage Regulator
DSP	Digital Signal Processor
GTO	Gate Turn-Off
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
LCC	Line-Commutated Converter
MLC2	Multilevel-Clamped Multilevel Converter
MMC	Modular Multilevel Converter
MPPT	Maximum Power Point Tracking
NPC	Neutral Point Clamped
PLL	Phase Lock Loop
PS-PWM	Phase-shifted Carrier Pulse Width Modulation
PWM	Pulse Width Modulation
SAF	Series Active Filter
SPWM	Sinusoidal Pulse Width Modulation
STATCOM	Static Synchronous Compensator
SVM	Space Vector Modulation
TSO	Transmission System Operator
UPWM	Unipolar Pulse Width Modulation
VSC	Voltage Source Converter

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Chapter 1. Introduction

The electricity supply industry is facing unprecedented challenges. The sector faces both increasing demand and the need to exploit clean energy resources which are necessary to meet CO2 emission targets and mitigate climate change.[1]. Renewable energy is geographically constrained to locations with high clean energy resources (wind, sunlight, etc.). A high voltage direct current (HVDC) transmission system offers attractive features that are suitable for renewable energy interfacing and alternative current (AC) grid interconnection[2]. Therefore, high voltage converters with high conversion efficiency and fault tolerance have gained attention from power electronics researchers.

1.1 **Background**

AC generation, transmission, and utilization have dominant since the beginning of the 20th century [3]. However, under certain circumstances, a DC transmission system is more competitive. This DC type of approach is more economical and efficient for large power transmission over long distances, for renewable energy interfacing and grid interconnection. The breakeven distance for a HVDC transmission system is estimated in a range of 300-400 miles for overhead lines and 50-75 miles for submarine cables [4, 5]. HVDC transmission systems provide attractive features compared with AC networks, such as system transient stability, compatibility to AC grids with different frequencies, and tolerance to AC voltage oscillation [6].

Since the 1960s, several semiconductor switching devices have been used in HVDC transmission systems; the most commonly used are the silicon controlled rectifier (thyristor), the Gate Turn-off (GTO) Thyristor, and the Insulated Gate Bipolar Transistor (IGBT) [7]. The first conversion system developed for HVDC transmission was the line commutated current source converter (LCC) using mercury arc valves as the main switching devices [8]. The replacement of mercury arc valves by the silicon controlled rectifier (thyristor) led to the further development of the LCC [9]. The thyristor based LCC was firstly applied to HVDC transmission system in the early 1970s. The development of self-commutated devices (GTO and IGBT) with high voltage and power ratings facilitated the application of the voltage source converter (VSC) into HVDC transmission systems [10, 11].

The conventional VSC based HVDC transmission system overcomes the drawbacks of the LCC based HVDC system. Different from the LCC based HVDC system, the VSC based HVDC system can regulate the active and reactive powers independently and can be operated over the full range of power factors regardless of system impedance [12, 13]. The system switching frequency is increased by utilising self-commutated switches which improves the transient stability of the VSC based HVDC system. However, the system suffers from the high power losses and poor performance during a DC link fault [14]. For conventional VSCs such as two-level or three-level converters (that use series connected power semiconductor devices to withstand the voltage stress that is in excess of the voltage rating of single switch), the power quality is traded against increased switching losses and a larger system footprint [15].

Multilevel converter topologies have reduced the voltage stress on each switching device without the need to series connected power semiconductor switches, improved the power quality, and decreased the effective device switching frequency [16]. These features result in reduced switching losses and a smaller AC side filter requirement. Conventional multilevel converter topologies are applicable to medium voltage applications but are unsuitable for HVDC transmission systems [17].

The diode-clamped multilevel converter can generate a large number of output voltage levels to improve the output voltage quality [18]. But it suffers from DC link voltage sharing imbalance for more than three output voltage levels, thus the external circuitry is required to balance the DC link string of capacitors [19]. Similarly, the flying capacitor multilevel converter has bulky DC link capacitors and a complicated capacitor balancing scheme that limit its application [20]. The conventional H-bridge cascaded multilevel converter is generally applied to the static synchronous compensator (STATCOM) and the medium voltage drives [21]. It requires independent DC source for each of the H-bridge cell and common DC link is absent. Therefore, this approach is not applicable for HVDC system.

The modular multilevel converter (MMC), which uses half bridges, is applicable for HVDC transmission system. As the voltage levels increase, the voltage stress on each switching device and the switching losses are significantly decreased, and the converter AC side filter can be reduced or even eliminated due to the improved power quality [22-24]. The main disadvantages of this topology are that it has no capability to ride through a DC fault and cannot operate so as to inject active power to the AC grid when the DC link voltage collapse [25].

The cascaded H-bridge modular multilevel converter (H-bridge MMC) has the same features as the half-bridge MMC except for higher power losses. The topology allows the system to ride through a DC fault by eliminating inrush current from the AC side and can inject active power into the AC grid during DC link voltage collapse. The cell capacitor voltages can be balanced under any condition without external circuitry.

1.2 **Motivation**

Novel VSC based HVDC transmission systems should operate with low power losses, have low output voltage harmonic components, have a small footprint and involve minimal system complexity. Importantly, the system should be capable of riding through DC and AC faults, as well as operate over the full DC link voltage range (zero to rated V_{DC}). Conventional multilevel converters and hybrid H-bridge cascaded multilevel converters do not fulfil these requirements. Modular multilevel converters are the only solution for a VSC based HVDC system, fulfilling the required functions.

The half-bridge MMC can synthesize a large number of output voltage levels and is capable of being extended to any voltage level. The lack of DC fault ride-through capability and vulnerable to DC link voltage oscillation are the major factors hampering its wider HVDC system exploitation. The H-bridge MMC can meet all the demands of the VSC based HVDC transmission system with DC and AC fault ride-through capability and the robust to operate over the full range of DC link voltage (0 to rated V_{DC}). Thus, the control scheme and cell capacitor voltage balancing strategy for the H-bridge MMC have emerged as key factors. These allow the converter to suppress common mode circulating current harmonics and cell capacitor voltage ripple in normal operation, eliminate inrush current and provide voltage support to AC grid during a DC fault, and inject active power to AC grid when the DC link voltage collapses. The reliability and scalability of the control scheme and capacitor voltage balancing strategy should be ensured. The main drawback is increased losses, associated with an increased number of semiconductors.

1.3 **Objectives**

In this research, fundamental operational principle and cell capacitor voltage balancing strategy of the H-bridge MMC are investigated. The common mode and differential mode current control schemes are proposed to achieve the following functions:

- The harmonic components of the arm currents and magnitude of the circulating current of the H-bridge MMC in each phase are suppressed during normal operation.

- Inrush current from AC side of H-bridge MMC is eliminated and the converter is operates to provide voltage support to the grid during a DC link fault.
- Cell capacitor voltages should be stabilized around the rated value under any condition, over the full range of DC link voltage and power factors.
- The H-bridge MMC can be operated in buck or boost mode over the full range of the DC link voltage with a control scheme able to inject active power to the grid during DC link voltage collapse.
- Multilevel voltage output should be achieved with comparatively low *dv/dt*.
- The control scheme should be extendable to any voltage level and should improve system transient stability.
- The grid current voltage should be phase synchronized to attain maximum active power transmission.

1.4 **Thesis Organization**

This thesis is organized into seven chapters:

Chapter 1 briefly presents the background of the HVDC transmission system and the converter topologies that may be suitable for a HVDC system. The motivation and objectives of this research are presented.

Chapter 2 has a detailed literature survey of HVDC transmission systems and the conventional converter topologies for such systems. The feature of each type of the converters is discussed and the fundamental operational principles are analyzed.

Chapter 3 introduces multilevel converters topologies suitable for HVDC transmission systems. Their features are discussed and compared.

Chapter 4 presents the fundamental operation principle, modulation scheme and cell capacitor balancing strategy, for the MMC. The operation principle is derived in mathematical functions and the current path through the H-bridge cells during each transient is illustrated. The operation principle, modulation scheme and cell capacitor balancing strategy are validated by both in simulation and experimentally.

Chapter 5 proposes an improved control scheme that includes common mode current control and differential mode current control. The control scheme fully exploits the subtractive and additive switch states of the H-bridge MMC to eliminate inrush

current during a DC fault, to inject active power into the grid during DC link voltage collapse, and to maintain capacitor voltage balance. Mathematical analysis of the capacitor voltage ripple and energy storage is presented. Both simulation and experimental results confirm the effectiveness of the control scheme.

Chapter 6 presents a *dq* control scheme and common mode current control scheme for the two-terminal, three-phase, H-bridge MMC based HVDC system and a multi-terminal three-phase H-bridge HVDC system. The performances of two-terminal and four-terminal H-bridge MMC based HVDC systems during normal operation, AC grid fault, DC link fault, and active power injection are validated by simulation.

Chapter 7 draws general conclusions and presents recommendations for future research.

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Chapter 2. Conventional HVDC Transmission System Converter Topologies

This chapter presents a detailed literature survey of HVDC transmission systems and the conventional converter topologies for such systems. The survey mainly focuses on conventional line commutated converters (LCC) and voltage source converters (VSC). The feature of each converter type is discussed and the fundamental operational principle is analyzed. Limitations of conventional converters are described to facilitate further research.

2.1 **Introduction**

The conventional AC transmission system has proved effective in power transmission and distribution [1, 2]. For normal applications, the cost of an AC system is attractive [3]. However, the AC system limitations are: not suitable for interconnection of the AC grids with different frequencies and high power losses in long distance transmission utilising overhead lines or subsea cables.

HVDC transmission systems are recognized by the transmission system operators (TSOs) as the technology that has lower power losses in long distance transmission and have the capability of interconnecting AC grids with different frequencies [4]. Furthermore, HVDC transmission systems can extend the dynamic rating of ageing AC power networks [5].

Thyristor line commutated converters (LCC) are used in second generation classical HVDC systems. This thyristor technology is used worldwide and has been universally accepted by power industries over the last six decades. Its advantage is low conversion losses and high overload capacities. The switching frequencies of the LCCs are restricted to the AC grid (50Hz in UK) due to their line-commutation nature. The main disadvantages of LCC-HVDC transmission systems are:

- LCC requires large passive filters to mitigate the low order frequency harmonics and an additional damping network to suppress the circulating current. This increases converter losses.
- Since the switching frequency of the LCC is that of the AC grid, the dynamic response is slow.
- Control of active and reactive powers is coupled, which increases control scheme complexity.
- AC network source impedance has significant effect on the operating range of the line commutated converters.
- The installation and maintenance costs are high due to the large footprint of LCCs.
- It is vulnerable to AC grid disturbance, which may temporarily shut down the system [6].

The voltage source converter based high voltage direct current (VSC-HVDC) transmission systems that typically utilize IGBTs within their converters, has recently drawn attention from power industries and researchers [7]. Although LCCs with thyristors as the main switches are still economical for bulk power handling, VSC-HVDC systems offer more benefits than the conventional thyristor based LCC-HVDC approaches:

- Active and reactive powers can be controlled independently in VSC-HVDC systems due to the de-coupled regulation of the amplitude and phase angle of the AC terminal voltage of the VSC.
- The VSC-HVDC has a faster dynamic response; which is beneficial to enhancement of the AC network transient stability.
- Since an external voltage source for commutation is not required for a VSC, the system can operate over the full range, regardless of the AC network source impedance.
- Self-commutated devices can be operated at medium frequency, which allows the VSC-HVDC system to use a pulse width modulation strategy. The harmonics are separated from the fundamental power frequency; thus AC filter sizing can be decreased. Consequently, the system footprint is expected to be smaller than the conventional LCC-HVDC system.
- VSC-HVDC system has the capability to ride through an AC fault and help AC system recovery when the fault is cleared [6, 8, 9].

However, the earlier installed VSC-HVDC has the drawback of higher switching losses than with LCC-HVDC. Furthermore, it is vulnerable to DC link pole to pole faults.

2.2 HVDC transmission system application

The uses of HVDC transmission systems has proven to be a feasible solution for special conditions such as long distance bulk power transmission, off-shore wind farm interfacing, AC grid interconnection, and multi-terminal power distribution.

2.2.1 Long Distance Bulk Power Transmission

Point-to-point connection has been the traditional application of the HVDC transmission systems for long distance bulk power transmission displayed in **Figure 2-1**. In this context, the LCC is considered mature technology with a proven track

record. LCC is still the main technology being used in bulky power transmission, and the maximum power rating of recently installed LCC-HVDC is 7.2GW, ± 800kV [10]. At present VSC-HVDC is competitive when the maximum power rating is less than 1000MW [11]. However, VSC technologies are developing; VSC-HVDC is expected to compete with LCC-HVDC in the near future in the area of long distance back to back bulk power transmission.

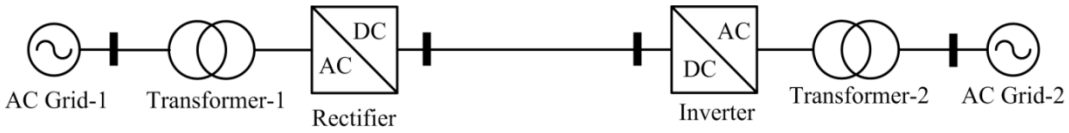

Figure 2-1. Point-to-point HVDC transmission system

2.2.2 Off-shore wind farm interfacing

For off-shore wind farm implementation, the HVDC transmission system offers better features than the AC transmission system such as: costs of the capital equipment and losses are lower than the AC system when the distance is greater than 50km; power flows are fully controllable; the system is capable of operating in parallel with AC networks and it has a quick dynamic response [12]. In [12-14], VSC-HVDC is tendered as the better transmissions system in this application for the improvement of machine control capability, system stability, AC fault ride-through capability, and the ability to handle three-phase unbalanced load [15]. Compared with LCCs, VSCs have a smaller footprint, lower cost at the same power rating, and are more suitable for multi-terminal HVDC transmission system, which is considered to be the better solution for large scale off-shore wind farms [16].

There are variable solutions to interconnect an off-shore wind farm to the AC grid via HVDC transmission system, such as park coupling, cluster coupling, common DC bus based clusters and hybrid multi-terminal system [17], displayed in Figure 2-2 and Figure 2-3.

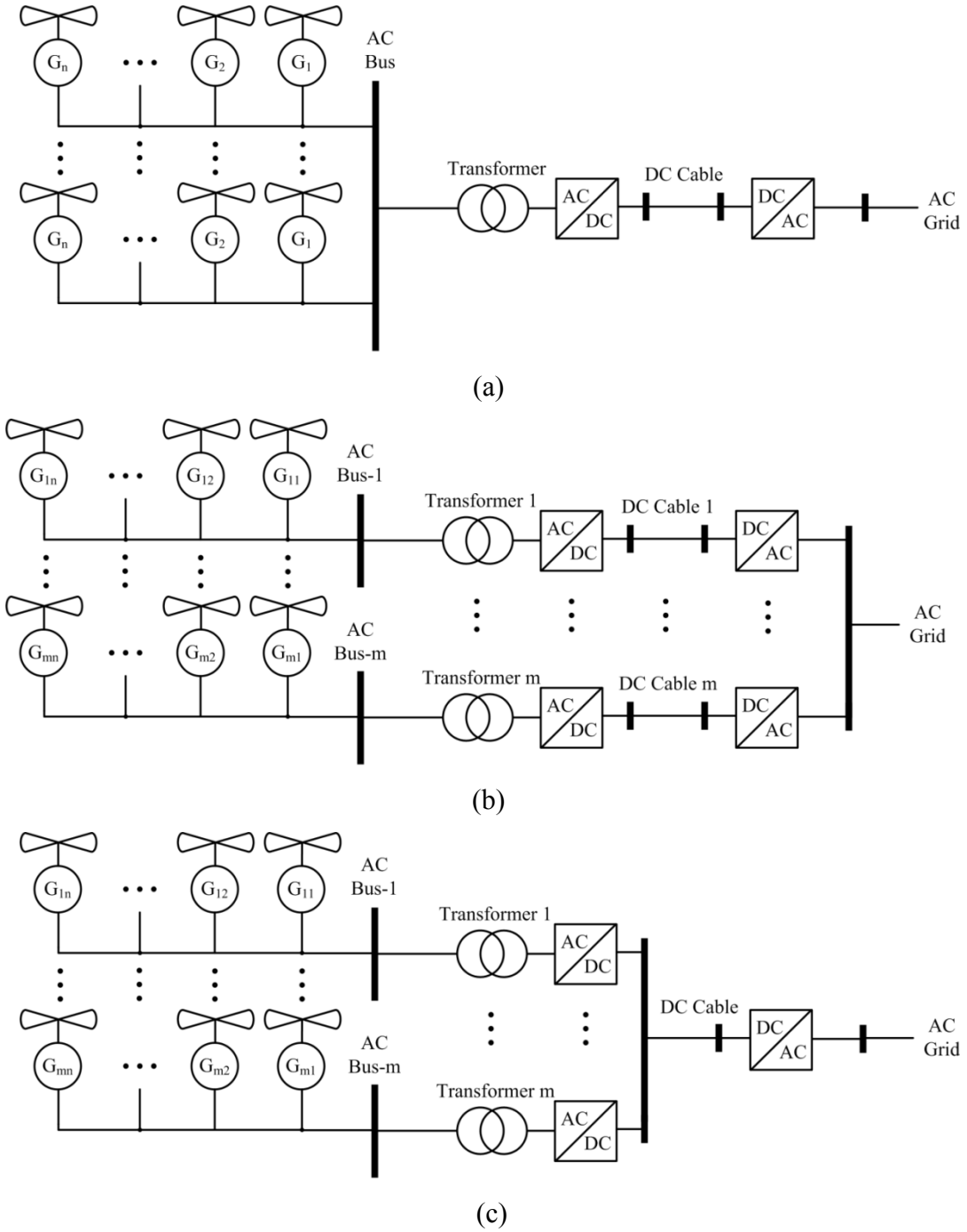

Figure 2-2. HVDC transmission system for wind turbines interconnection: (a) park coupling, (b) cluster coupling, and (c) cluster coupling with common DC bus

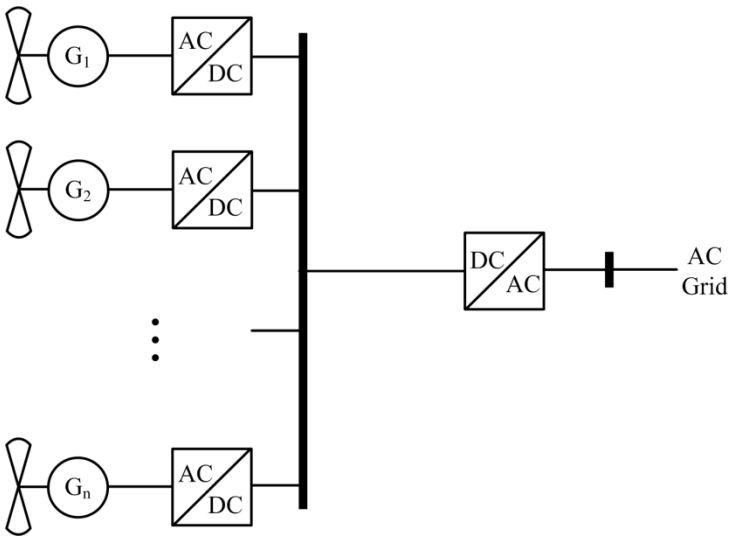

Figure 2-3. Hybrid multi-terminal system for wind turbines interconnection

2.2.3 Multi-terminal HVDC power distribution

The application of the multi-terminal HVDC transmission system for power distribution has gained the attention from researchers and power companies. Several solutions have been presented for such implementation [18]. Multi-terminal VSC-HVDC displayed in Figure 2-4 is considered to be the most promising transmission system for power distribution, not only from an economical point of view but also from stability [19] and power quality [20] standpoints.

Re-assessment of the fundamental principles of power distribution, such as system parameter calculation and power flow estimation, is required for the integration of multi-terminal HVDC into the power system. Such application also opens new research areas in system protection and fault ride-through, such as interrupting DC faults, isolating DC cables from DC faults, and regulating the DC link voltage from AC network disturbances [21].

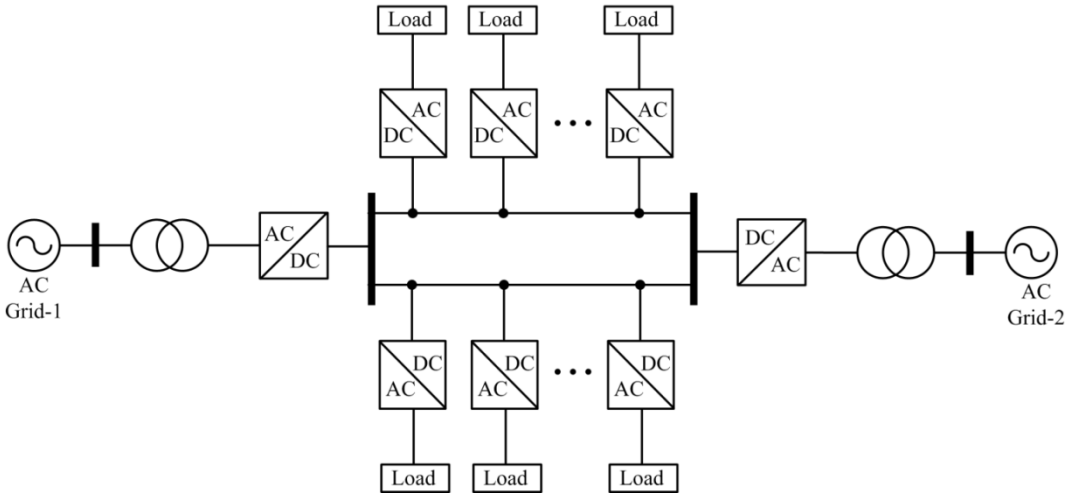

Figure 2-4. A multi-terminal VSC-HVDC distribution system

2.3 Conventional converter topologies for AC/DC conversion

Converters for the interfacing of HVDC transmission systems are introduced in this section, these include the line commutated converter (LCC) and the half-bridge voltage source converter. The H-bridge voltage source converter, Z-source converter, and other possible converters that can be used for AC/DC conversion are discussed briefly. The basic topologies and derivatives of these converters are also investigated.

2.3.1 Line commutated converter

The three-phase line commutated converter (also known as Graetz converter) in Figure 2-5(a) has been generally utilised in conventional LCC-HVDC transmission systems due to its high power capacity, and its economical technology with sufficient reliability [22]. Figure 2-5(b) illustrates the back to back HVDC transmission system based on the LCC that suffers from the low order frequency harmonics which necessitate large AC and DC filters [23]. Passive filters are implemented to suppress the low order harmonics due to their low cost and high efficiency. However, the disadvantages of passive filters are: affected by system impedance, susceptible to source and load resonance, and only applicable to specific frequencies [24]. For this reason, active compensators have been suggested to overcome the disadvantages of passive filters shown in Figure 2-6 [24]. Active filters can compensate the distorted current waveforms generated by an LCC but at the price of increased power losses [25]. As a strong synchronous AC network is necessary for LCC commutation, the capacitor-commutated converter (CCC) with series connected capacitors between the

converter output node and the AC grid or transformers displayed in Figure 2-7, has been proposed for weak AC networks [26].

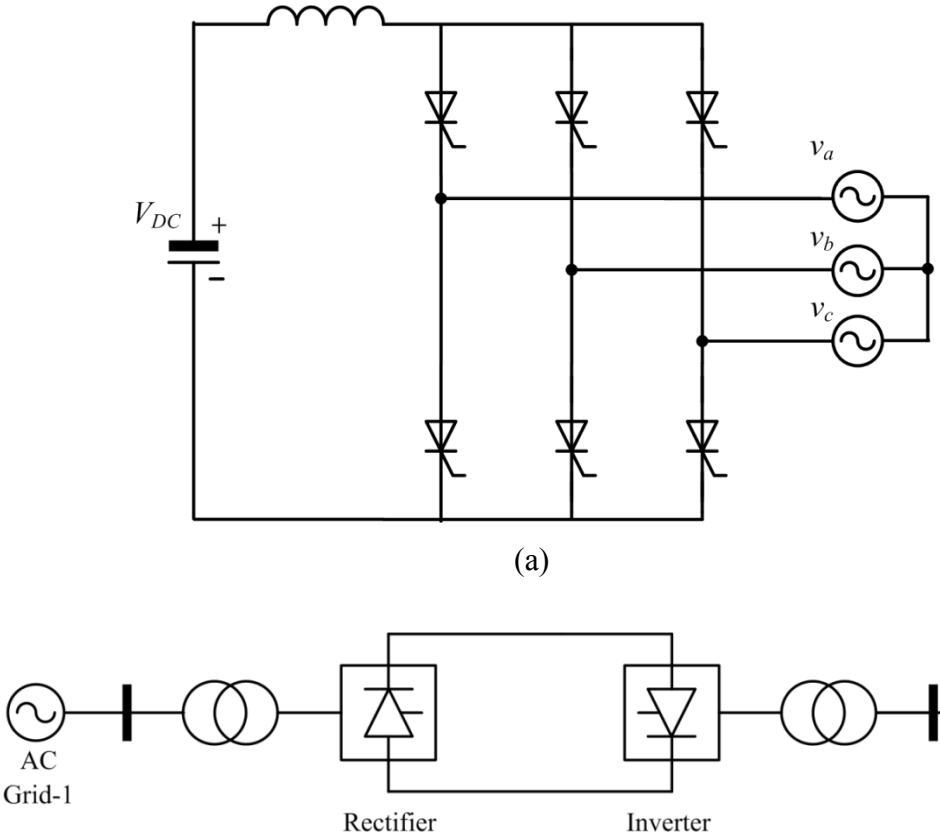

Figure 2-5. LCC based HVDC system: (a) three-phase line commutated converter and (b) back to back LCC HVDC transmission system

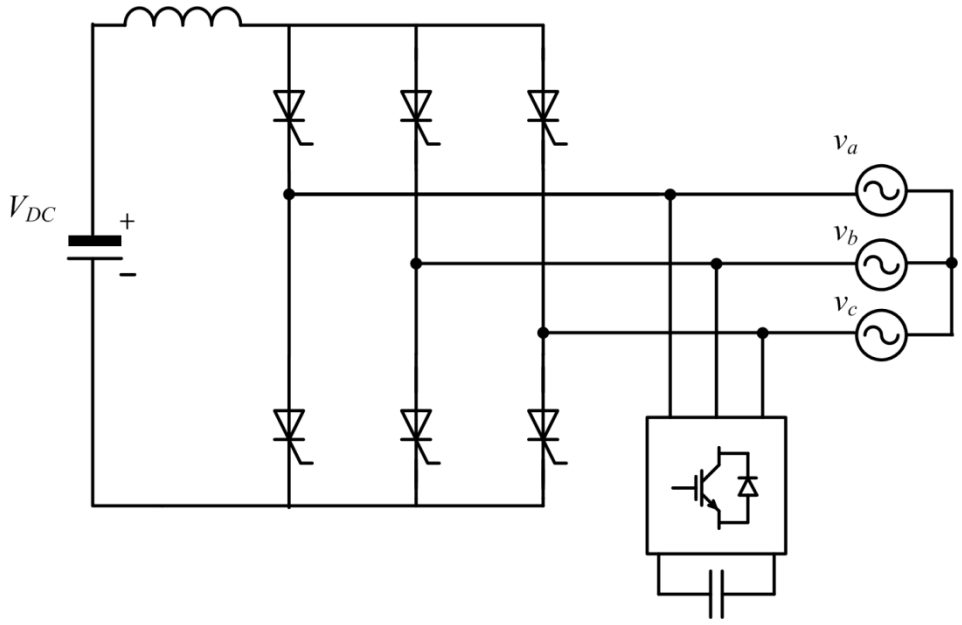

Figure 2-6. Line commutated converter with active compensator

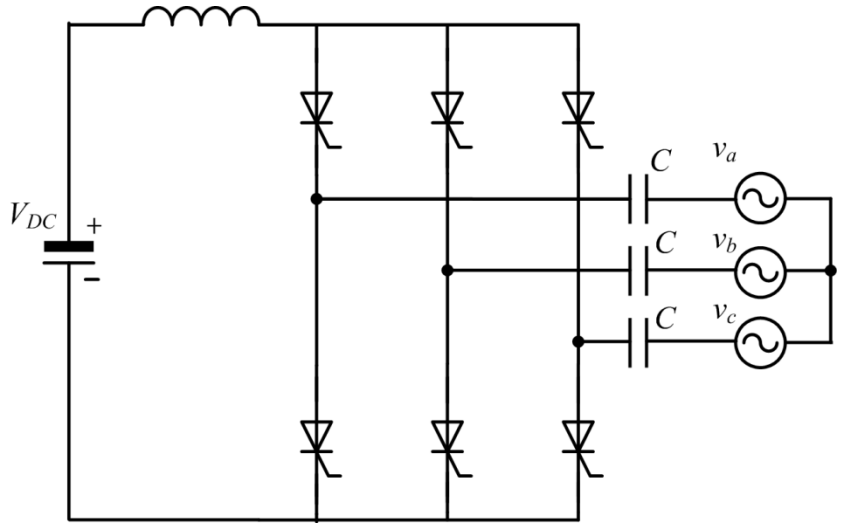

Figure 2-7. Capacitor-commutated converter

2.3.2 Conventional three-phase half-bridge voltage source converter

The three-phase half-bridge VSC topology (also known as two-level converter) in Figure 2-8 has been widely used in HVDC transmission system for AC grid interconnection and renewable energy interfacing [27, 28]. It uses a pulse width modulation (PWM) or space vector modulation (SVM) strategy to synthesize the two-level (bipolar) output voltage waveforms at a switching frequency of no more than 2kHz. In medium voltage DC applications and HVDC transmission systems, the main switching devices are series connected self-commutated switches (mostly IGBTs) that withstand the high voltage stress that is much larger than the maximum voltage rating of a single IGBT. This increases the switching and conduction losses. The AC side filter size, conversion losses, and dynamic response are the key factors that determine the converter switching frequency. At the DC side of three-phase half-bridge VSC, a large decoupling capacitor is required to stabilize the DC link voltage, which is critical for HVDC application [29]. These capacitors are usually heavy, bulky and expensive and limit system life-time [30]. Furthermore, the half-bridge VSC has a high *dv/dt* that causes unwanted EMC disturbance, and has no ability to ride through DC faults and cannot inject active power into the AC grid when DC link voltage collapses to a low value (between 0 to V_{DC}).

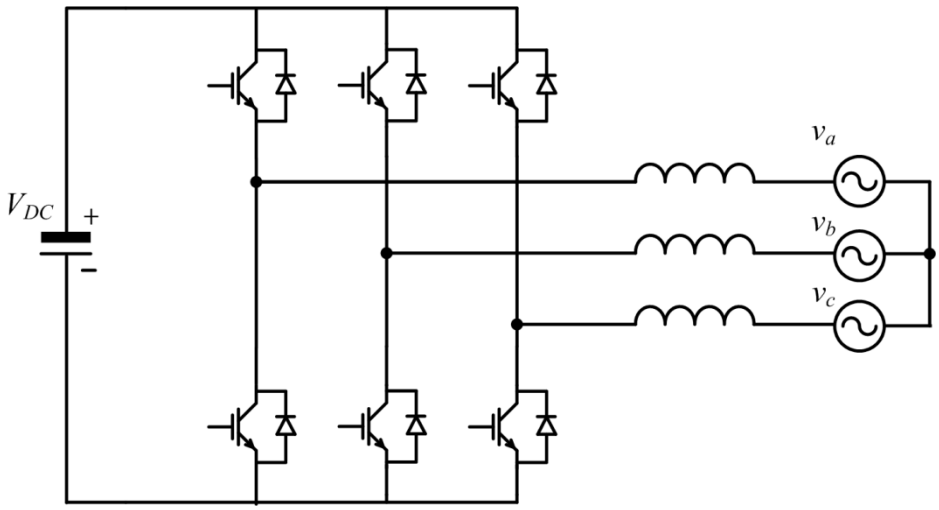

Figure 2-8. Three-phase half-bridge VSC topology

2.3.3 Conventional three-phase H-bridge voltage source converter

H-bridge VSCs are normally used in single phase AC systems. However, three-phase H-bridge VSCs can be utilized in the application of a Series Active Filter (SAF) [31, 32], a Dynamic Voltage Restorer (DVR) [33, 34], and a STATCOM [35]. Different from half-bridge VSCs, the H-bridge VSCs can generate three-level (unipolar) output phase voltage by using a unipolar pulse width modulation (UPWM) scheme which reduces the voltage stress on each switching device to half that of the stress on half-bridge VSC devices that utilized bipolar pulse width modulation (BPWM) [36]. However, conventional H-bridge VSCs still require bulky DC link capacitors and passive AC filters, and cannot ride through DC faults or inject active power into the AC grid during DC link voltage collapse.

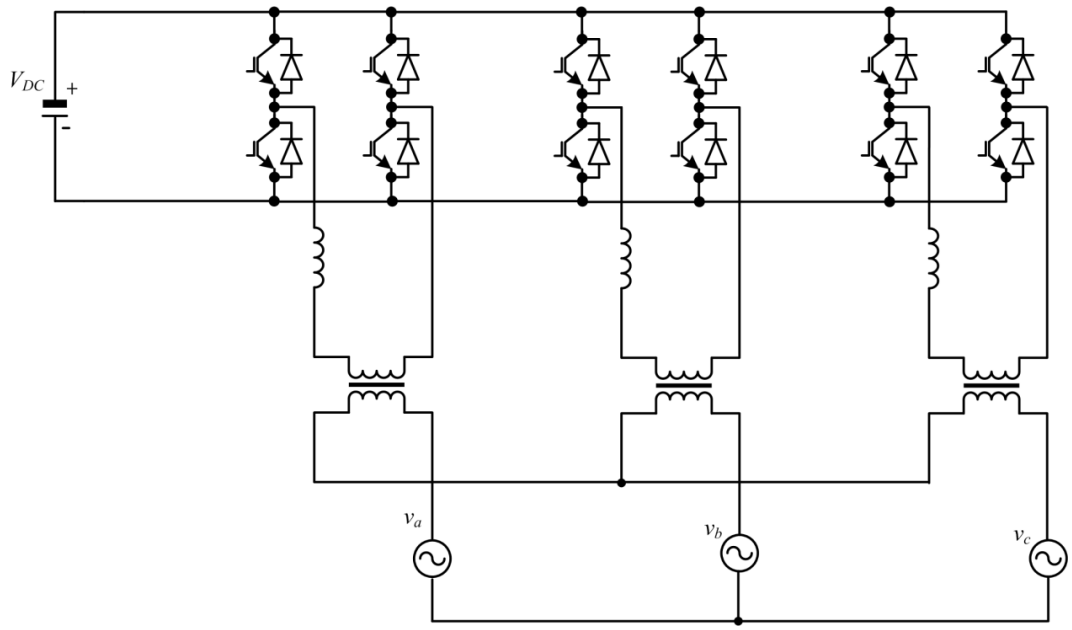

Figure 2-9. Three-phase H-bridge VSC with transformers for grid connection

2.3.4 Z-source converter

Figure 2-10 shows the Z-source converter topology, which can operate in buck and boost modes when creating a DC link voltage [37, 38]. A unique impedance network is employed with two inductors and capacitors. A DC link boost converter can be eliminated by utilising the Z-source converter in the HVDC transmission involving renewable energy interfacing [39]. However, it would be difficult to adapt this converter to medium and high voltage systems due to IGBT limitations. The poor DC fault ride-through performance is also considered to be disadvantages of this topology.

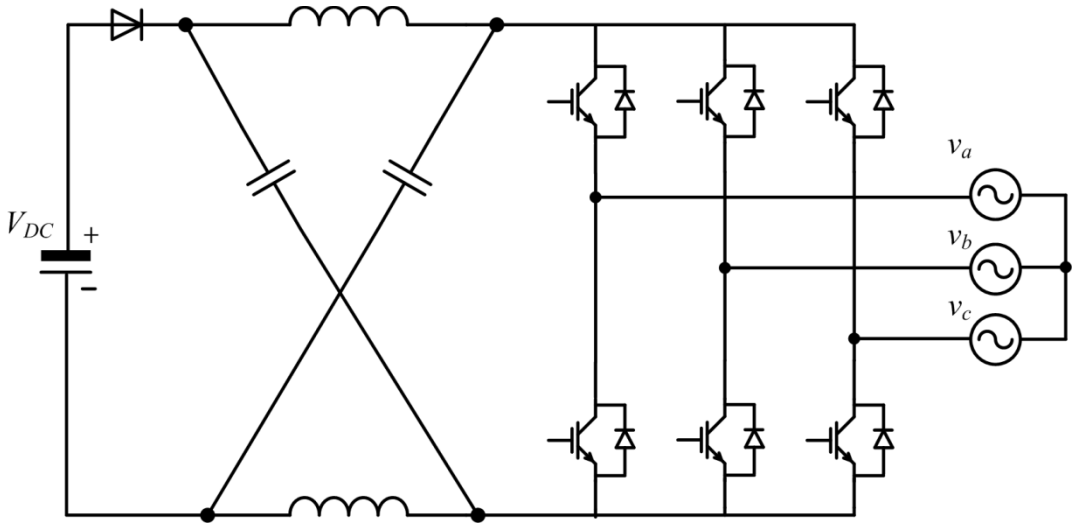

Figure 2-10. Z-source converter

2.3.5 Other converter topologies

The current source converter in Figure 2-11 has been proposed for renewable energy interfacing by power electronics researchers [40]. Different from voltage source converter topologies, series connected diodes and IGBTs are used in each phase to block reverse current from the AC grid, resulting in increased conduction losses [41]. It has poorer performance than the voltage source converter when utilising a PWM scheme. A large DC link capacitor is replaced by a large DC link inductor, which compared to the VSC improve system lifetime. The converter can block inrush current from the AC grid during a DC link fault and is capable of interrupting an AC side fault. However, the voltage stress on each switching device and a high *dv/dt* limit its application to high voltage transmission. The current source converter requires a large passive filter and may cause AC grid voltage disturbance during certain transients [42].

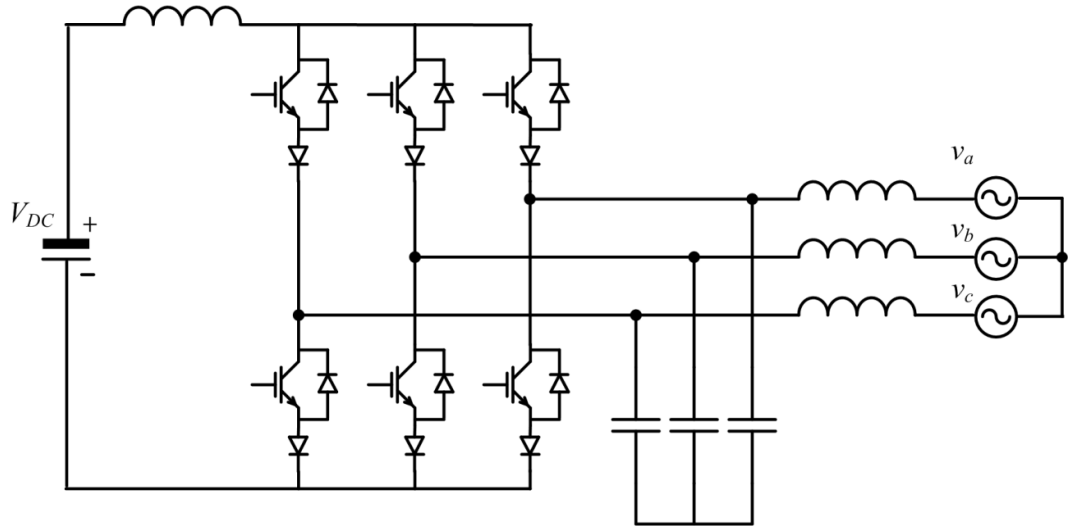

Figure 2-11. Three-phase current source converter with IGBTs as the main switching devices

The matrix converter topology has been presented as an alternative to the conventional voltage source converter, for off-shore wind farm interfacing application [43, 44]. An matrix of controlled bidirectional switches are used as the main power elements to interconnect the generator with the grid [45]. Independent control of voltage magnitude, frequency, phase angle and power factor can be achieved [46]. No DC link capacitors exist, since there is no DC link [45]. However, the fault ride-through and input and output decoupling cannot be achieved owing to the absence of intermediate energy storage (decoupling) elements.

2.4 **Summary**

This chapter briefly described the converters for the HVDC transmission system; including line commutated current and self commutated voltage source converters. Attributes and limitations of each topology were discussed, including their implication from a system prospective during normal operation and AC and DC faults. Also their appropriateness for renewable energy interfacing and AC grid interconnection was considered.

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Chapter 3. Multilevel Converters Topologies for HVDC Transmission Systems

This chapter discusses multilevel converter topologies for HVDC transmission systems. The investigation mainly focuses on three multilevel converter topology types: traditional multilevel converters (diode clamped multilevel converters and flying capacitor multilevel converters), hybrid cascaded multilevel converters, and modular multilevel converters. The unique features of these multilevel converter topologies are discussed and a state of art comparison between them is presented.

3.1 **Background**

For the future power industry applications for medium and high voltage direct current transmission systems, voltage source converters are thought to be the better option than the line commutated converter [1]. However, conventional voltage source converters still suffer from the significant drawbacks such as previously stated, and poor performance during DC link faults [2, 3].

Recently, attention has been paid to multilevel converters that provide some attractive features: lower voltage stress on the switching devices, low *dv/dt*, and the low order frequency harmonics are significantly suppressed thereby decreasing the AC side filter size [4, 5]. Therefore, different topologies of multilevel converters have been proposed by researchers.

The diode-clamped multilevel converter was proposed by Nabae *et al*. in 1980 [6] and extended to *N* levels by Bhagwat in 1983 [7]. The flying capacitor multilevel converter was introduced by T.A. Meynard *et al*. in 1992 [8]. Both suffer from voltage imbalance of the DC link capacitors, system complexity with an increasing number of levels, and susceptible to system impedance effects [9, 10].

The half-bridge modular multilevel converter (half-bridge MMC) proposed in [11] has several advantages: minimum conversion power losses compared with other VSC based approaches, can be extended to any number of voltage levels, cell capacitor voltage balancing capability, and system redundancy [12]. However, the half-bridge MMCs have no ability to block inrush AC current during a DC fault and can only be operated in the buck mode that cannot provide active power to the AC grid when DC link voltage collapses below the peak of the line AC voltage [13].

The H-bridge modular multilevel converter (H-bridge MMC) has the capability to ride through DC faults and can provide voltage support to the AC grid during the fault period[13]. The H-bridge cell can generate bipolar output voltage ($\pm V_c$, *0*) while the half-bridge cell only produces $+V_c$ and *0*. These features make the H-bridge MMC attractive for implementation into HVDC transmission systems and renewable energy interfacing.

The hybrid cascaded H-bridge multilevel converter was proposed in [14]. It synthesizes multilevel output voltage waveforms with the minimum number of cells and has limited capability to interrupt a DC fault by blocking the system from AC side inrush current [15]. However, the voltage stress on each switching device is

identical to that of the conventional half-bridge VSC that limits its application on the medium and high voltage transmission systems.

3.2 **Diode Clamped Multilevel Converter**

The diode clamped multilevel converter employs clamping diodes and cascaded DC capacitors. For each phase of the *N*-level diode clamped multilevel converter, $(N-1)$ capacitors are connected in series across the dc bus, $2\times(N-1)$ series connected switches are utilized, and $(N-1)\times(N-2)$ diodes are used to clamp the switch voltages. The approach synthesizes *N* levels in the phase voltage in normal operation [16].

The single phase three-level diode-clamped converter in Figure 3-1 consists of four self commutated switching devices IGBTs (T_1, T_2, T_3 and T_4) and their freewheeling diodes (D_1, D_2, D_3 and D_4) to enable bi-directional current flow capability. The voltage stress on each DC link capacitor is $\frac{1}{2}V_{DC}$ while the neutral point *G* is set between the two DC link capacitors. The DC link capacitors are charged or discharged when current i_g flows into the neutral point that causes neutral-point voltage distortion [9].

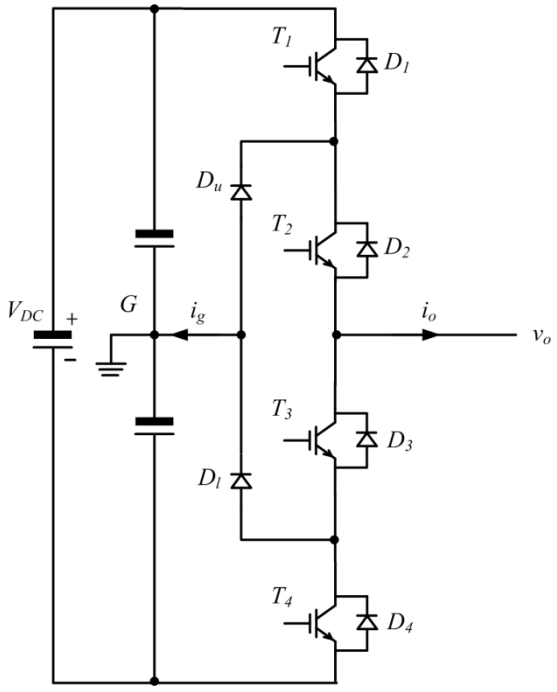

Figure 3-1. Single phase three-level diode-clamped converter

The output voltage v_o is synthesized by three switching combinations. When T_1 and T_2 are on and T_3 and T_4 are off, the output voltage v_o is equal to $½V_{DC}$. When T_2 and T_3 are on, and the other switches are off, the output voltage v_o is 0. When T_3 and T_4 are on, the output voltage v_o is $-½V_{DC}$. In each switch state, diode D_u and D_l are utilized to clamp the voltage stress to $½V_{DC}$ on each switch that is turned off [17]. Table 3-1 summarises the possible switching combinations for the single phase three-level diode-clamped converter where "1" represents "*on*" and "0" represents "*off*".

Table 3-1 Switching combinations of a single phase three-level diode-clamped converter

T_1	T_2	T_3	T_4	Output voltage v_o
1	1	0	0	$½V_{DC}$
0	1	1	0	0
0	0	1	1	$-½V_{DC}$

The diode-clamped converter suffers from topology structure complexity that makes it difficult to be extended to high voltage levels and the number of the clamping diode is $(N-1) \times (N-2)$ which also limits the practical use in high voltage-level applications[18]. For more than three levels, the DC link voltage sharing imbalance becomes problem which requires external circuitry and capacitor voltage balancing methods to maintain each DC link capacitor voltage constant [19].

3.3 **Flying capacitor multilevel converter**

Different from the diode-clamped converter, the flying capacitor multilevel converter uses the capacitors combined with switches to generate different output voltage levels through adding or subtracting of the capacitor voltages [20]. For an *N*-level flying capacitor multilevel converter, theoretically, the voltage stress on each switching device is equivalent to the voltage rating of each capacitor. Therefore, the *N*-level converter requires $(N-1)$ dc-link capacitors as well as $½(N-1) \times (N-2)$ flying capacitors for each phase. The structure of single phase three-level flying capacitor multilevel converter is shown in Figure 3-2. The switching combinations

are listed in table that can synthesize three output voltage levels: $\pm\frac{1}{2}V_{DC}$, *0*. A "1" represents "*on*" and "0" represents "*off*" [21, 22].

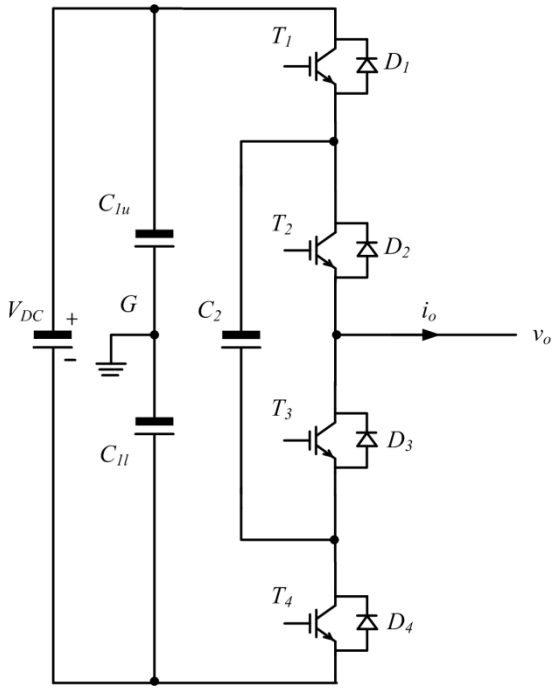

Figure 3-2. Single phase three-level flying capacitor multilevel converter

Table 3-2 Switching combinations of a single-phase three-level flying capacitor multilevel converter

T_1	T_2	T_3	T_4	Output voltage v_o
1	1	0	0	$\frac{1}{2}V_{DC}$
1	0	1	0	0
0	1	0	1	0
0	0	1	1	$-\frac{1}{2}V_{DC}$

Instead of eliminating the DC side passive components (capacitors or inductors), the flying capacitor multilevel converter requires a large number of storage capacitors at the DC side. Thus, it is unrealistic to implement such topology in a high voltage transmission system owing to the large footprint, high cost of the bulky capacitors [23], and vulnerability to the system impedance effects. Furthermore, the complexity of the control scheme and DC link voltage imbalance also limit its application in medium voltage transmission systems [24].

3.4 Conventional cascaded multilevel converter

The conventional cascaded H-bridge multilevel converter is composed of the series connected H-bridge cells that requires an independent DC supply for each H-bridge cell displayed in Figure 3-3 [25]. The cascaded multilevel converter is not suitable for HVDC transmission systems due to the absence of a common DC link. However it is applicable for photovoltaic grid integration [26] and electric hybrid vehicles [27].

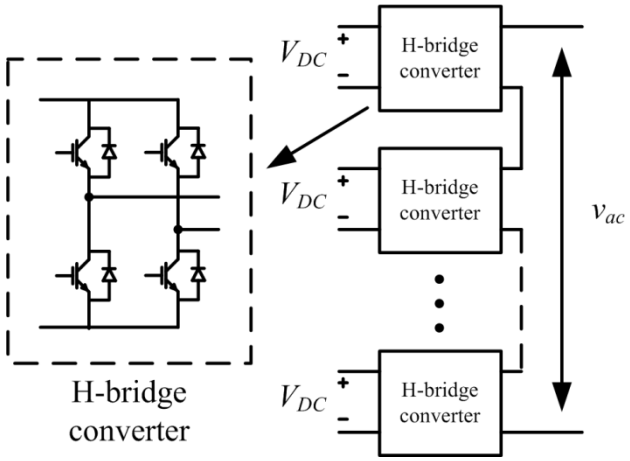

Figure 3-3. Conventional cascaded H-bridge multilevel converter

3.5 Hybrid H-bridge cascaded multilevel converter

Figure 3-4 shows the single phase hybrid H-bridge cascaded multilevel converter with N H-bridge cells per phase. It can synthesize up to $4N+1$ output voltage levels relative to the neutral point "n". The two-level converter stage which consists of the main switches T_1 and T_2 generates bipolar output voltage waveforms at node "L" with a PWM scheme and the cascaded H-bridge cells at the AC side are operated as a series connected active filter to suppress the voltage harmonics produced by the two-level converter block [15, 28]. The voltage rating of each H-bridge cell capacitor is $\frac{V_{DC}}{2N}$ that is equivalent to the voltage stress on each switch of the H-bridge cells [14].

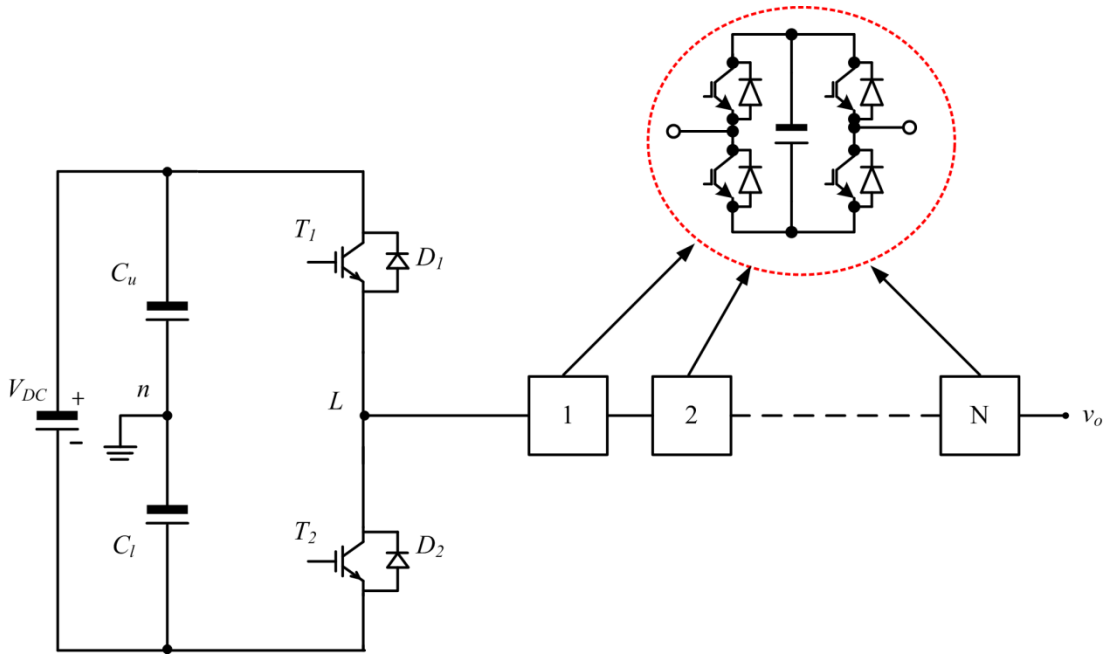

Figure 3-4. Single-phase hybrid H-bridge cascaded multilevel converter

The two-level converter stage can be operated at low switching frequency since the AC side cascaded H-bridge cells can effectively improve the output voltage waveforms. However, this is a trade-against an increase of the H-bridge cells switching frequency which is much higher than the switching frequency of the two-level converter block [14, 29]. Asynchronism of the two-level converter block and the H-bridge cells may create fifth and seventh harmonics that require low order frequency AC filters. As the H-bridge cells and the main switches of the two-level converter block conduct the full load current during normal operation, high conduction losses are expected. The overall conversion losses of the hybrid H-bridge cascaded multilevel converter are greater than the modular multilevel converter [5, 15]. During a DC fault, all the main switches and the H-bridge cell switches are turned off, whence cell capacitors present reverse voltage to suppress the inrush current from the AC grid. Therefore, no active and reactive powers are exchanged between the AC grid or DC side (when the DC link voltage collapses due to the DC fault) [30]. Although the hybrid cascaded multilevel converter offers DC fault blocking capability (blocking of the inrush current from AC grid during a DC fault), it is unable to control the inrush current during system restart as its concentrated DC link capacitance needs to be charge from AC side. Thus, post-fault recovery is impractical for the hybrid H-bridge cascaded multilevel converter. Furthermore, the

main switches T_1 and T_2 of the two-level converter block experience a voltage stress of V_{DC} that limits the application of this topology in HVDC transmission systems.

3.6 **Half-bridge modular multilevel converter**

The single-phase modular multilevel converter with half-bridge cells (or chopper cells) in the upper and lower arms is displayed in Figure 3-5. It consists of n half-bridge cells per arm that can synthesize $n+1$ output voltage (v_o) levels. The voltage rating of each cell capacitor is maintain at V_{DC}/n, thus the voltage stress on each switching device is restrained to V_{DC}/n. The converter output voltage can be near pure sinusoidal with a large number of cells. Arm inductors are implemented to suppress the harmonic components in the arm currents and limit the inrush current during a DC side fault. All the switching states can be utilized to affect cell capacitor voltage balance except for the switching states that produce $\pm½V_{DC}$. When the converter output current is positive ($i_o > 0$), the selected upper arm capacitors will be charged and selected lower arm capacitors are discharged, and vice versa [12]. SPWM [31] and phase-shifted carried modulation [32] are two major modulation schemes that have been implemented to control the half-bridge MMC, combined with a cell capacitor voltage balancing strategy [33].

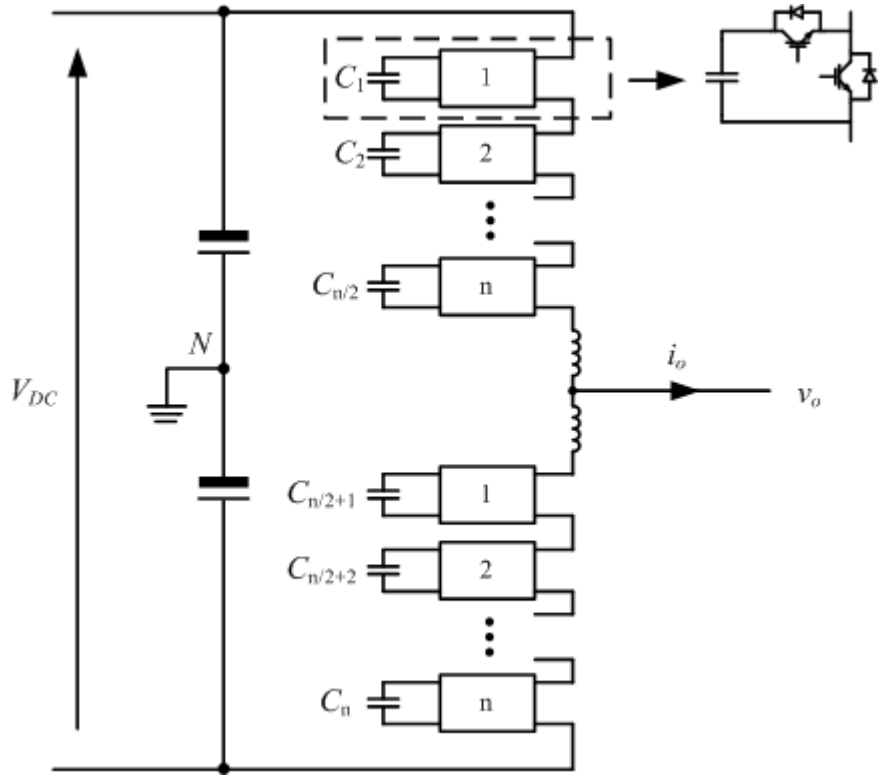

Figure 3-5. Single-phase half-bridge modular multilevel converter

The advantage of the half-bridge MMC are: voltage stress on each switching device is restrained to V_{DC}/n, bulky DC link capacitors are eliminated (the neutral point is set at the mid-point of the stray capacitance), the switching frequency can be greatly reduced with a large number of cells - this decreases switching losses, the AC components of the arm currents flow through the switches are equivalent to $½i_o$ which reduces the conduction losses, and the footprint of the AC filters can be minimised due to the improved output voltage waveforms [34]. However, the topology is not capable of riding through a DC fault (neither permanent nor temporary fault). In renewable energy interfacing applications, the half-bridge MMC cannot be controlled when the DC link voltage collapses to a low level (between 0 to V_{DC}) which generally exists and may be caused by wind speed variation or sunlight change. It also suffers from arm current harmonics and a circulating current in each phase that increases conduction losses. Furthermore, the cell capacitors of the half-bridge cells are used to provide power to the grid under some circumstances, this feature may increase the system footprint.

3.7 **H-bridge modular multilevel converter**

The H-bridge modular multilevel converter has similar advantages as the half-bridge MMC, such as low voltage stress on each switch, elimination of the bulky DC link capacitors, low switching frequency and AC side filters can be decreased or even eliminated. However, the conversion losses of the H-bridge MMC are higher than the half-bridge MMC due to the increased number of switching devices at the same system power rating. But the H-bridge MMC is capable of riding through a DC fault (either temporary or permanent fault) by suppressing inrush current from AC side with reversed cell voltages and can maintain cell capacitor voltages at the rated value. Such capability, as well as post-fault recovery, active power injection into AC grid over the full range of the DC link voltage (0 to V_{DC}) by utilising the unique feature of H-bridge cells, will be studied in detail in this thesis. Thus, this topology is highly attractive for multi-terminal HVDC transmission systems; and medium voltage applications such as renewable energy interfacing where variable DC link voltage operation is beneficial for maximum power extraction. The novel control schemes that facilitate these capabilities are considered in chapters 5 and 6.

3.8 **Other multilevel Converter topologies**

The H-bridge alternative arm modular multilevel converter presented in [35] has the ability to interrupt a DC fault with comparatively lower conversion losses than the hybrid H-bridge cascaded multilevel converter and H-bridge MMC. But the converter suffers from a large inrush current when the phase currents are not synchronised with the fundamental phase output voltages and post-fault recovery is slower than the H-bridge MMC. Thus, the topology is not applicable for high power application.

A hybrid multilevel converter with H-bridge cells connected across the DC link is presented in [36]. The main disadvantage of this topology is that the voltage stress on each switching devices varies with modulation index; therefore, it is not suitable for variable voltage applications, and this limits its application in HVDC systems. From a device point of view, the five-level MMC provides more voltage levels with the same number of cells per arm compared with the half-bridge MMC. It can block the inrush current during a DC fault but HVDC system application may be hindered due to the bulky footprint and system configuration complexity.

The mixed cell modular multilevel converter provides a compromise between conversion losses and system protection. It requires the same number of cells as the H-bridge MMC to interrupt a DC link pole to pole fault. However, DC fault ride-through capability is limited by the number of H-bridge cells and it is unable to provide the added features the H-bridge MMC provides, as will be discussed in chapters 5 and 6.

Multilevel-Clamped Multilevel Converter (MLC2) was proposed by P. Rodriguez *et al*. in 2011 [37]. The converter operational principle is to combine the multilevel clamp concept with a neutral-point-clamped (NPC) converter to increase the output voltage levels without additional system complexity. However, power losses and capacitor voltage balancing were not addressed.

3.9 **Comparison**

The comparison of HVDC systems based on the LCC, the conventional VSC, the hybrid H-bridge cascaded multilevel converter, the half and the H-bridge MMC is presented in Table 3-3.

Table 3-3 Comparison of HVDC systems based on different converter topologies

	LCC	Conventional VSC	Hybrid H-bridge Cascaded multilevel	Half-bridge MMC	H-bridge MMC
Switching device	Thyristor	IGBT	IGBT	IGBT	IGBT
Switching loss	Negligible	High	Moderate	Low	Moderate
On-state loss	Low	Moderate	High	Moderate	High
Active power control	Discontinuous ±10% to ±100%	Continuous 0 to ±100%	Continuous 0 to ±100%	Continuous 0 to ±100%	Continuous 0 to ±100%
Independent control of active and reactive power	No	Yes	Yes	Yes	Yes
Reactive power demand	50% to 60%	No	No	No	No
AC filters	Large	Small	No	No	No
AC fault ride through ability	Possible with high risk of commutation failure	Excellent	Excellent	Excellent	Excellent
DC fault ride through ability	Excellent	Poor	Moderate	Poor	Excellent
Capability of operating at boost mode during DC link voltage collapse	No	No	No	No	Yes

3.10 **Summary**

This chapter presented a brief review of the traditional and state of the arts multilevel converter topologies for HVDC transmission systems. The review covered the diode clamped multilevel converter, the flying capacitor multilevel converter, the hybrid H-bridge cascaded multilevel converter, the half-bridge MMC, and the H-bridge MMC. The features and shortcoming of each topology were discussed and a detailed comparison between these converters were summarised in a Table 3.3.

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Chapter 4. H-bridge MMC operational principle and voltage balancing strategy

This Chapter investigated the principle of operation, modulation, cell capacitor balancing methods and power path, therein extending the study of multilevel modular converters, MMC. The modulation technique is based on sinusoidal pulse width modulation (SPWM), and the DC link capacitor balancing method is discussed in detail and verified by Simulink simulations. The capacitor voltage balancing method does not require an external reference; yet it distributes the DC link voltage equally between the cell capacitors. This reduces the inrush current during starting and the method is capable of maintaining cell capacitor voltage balance during unbalanced MMC operation and any faults.

4.1 **Background**

Multilevel converters have drawn interest in the electrical power industry in recent years. They offer features that are suited to high-voltage drive systems and power system applications such as high voltage dc (HVDC) transmission, reactive power compensation equipment, power conditioning, active power filtering, and so on [1]. The unique structure of multilevel VSCs allow them to operate at high voltages with low harmonic content without the use of filter circuits, and without the need to increase the switching frequency [2-7].

Diode-clamped multilevel converters have low *dv/dt* compare to two-level converters (at the switching frequency) and low common mode voltage [8-12]. For more than three levels, they suffer from voltage imbalance of the DC link capacitors; this problem increases complexity with an increased number of levels [13-18]. The effect of stray inductance in the clamping paths is also a problem.

The half-bridge modular multilevel converters, proposed in [19], is simpler than the conventional cascaded four-switch H-bridge-based converter and has several advantages, such as modular extension to any number of levels and redundancy [2, 9, 15, 20-22]. But it does not have the reverse current block capability.

The MMC that uses H-bridge cells has recently gained attention from the industry and researchers. The application of H-bridge cells in each arms of the converter introduces new switching states which allow voltage imbalance correction among cell capacitors at any moment in a cycle due to the bipolar feature of H-bridge cell. This feature can increase the MMC output voltage levels by changing the polarity of converter cells to create an extra voltage state. Thus the cell capacitor voltage ripple is decreased as well as the size of the capacitors. Different from the half-bridge cell MMC, the H-bridge MMC can block reverse current from the AC side to the DC side in the case of a DC fault.

4.2 **Structure and switching states selection of H-bridge MMC**

Figure 4-1 shows one cell of an H-bridge MMC. When switching devices S_1, S_2 are on and S_3, S_4 are off (or S_3, S_4 are on and S_1, S_2 are off), output voltage is $v_{cell}=0$. When switching devices S_1, S_4 are on and S_2, S_3 are off, the voltage $v_{cell}=V_s$. Depending on the current direction and the switch states, the cell capacitors will be charged or discharged. The switching state, the power flow, and the effect on capacitor voltage is summarised in Table 4-1('1' represents on '0' represents off).

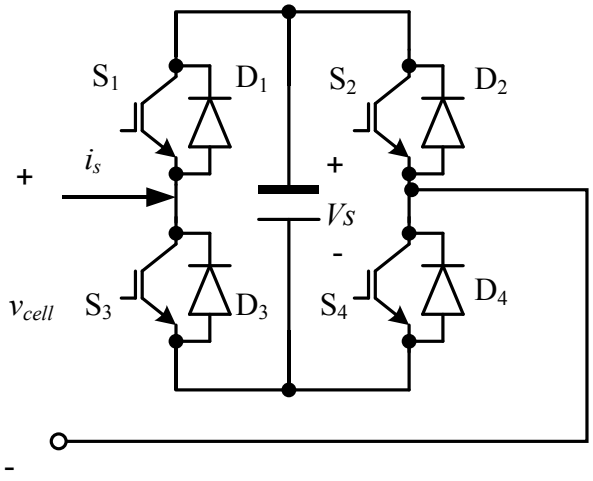


Figure 4-1. Modular multilevel converter H-bridge cell

Table 4-1. Switch states of an H-bridge cell

S_1	S_2	S_3	S_4	Current direction	Power path	V_{cell}	Capacitor voltage
1	0	0	1	$i_s>0$	D_1, D_4	V_s	charging
1	0	0	1	$i_s<0$	S_1, S_4	V_s	discharging
0	0	1	1	$i_s>0$	S_3, D_4	0	unchanged
0	0	1	1	$i_s<0$	D_3, S_4	0	unchanged
1	1	0	0	$i_s>0$	D_1, S_2	0	unchanged
1	1	0	0	$i_s<0$	S_1, D_2	0	unchanged
0	1	1	0	$i_s>0$	S_2, S_3	$-V_s$	discharging
0	1	1	0	$i_s<0$	D_2, D_3	$-V_s$	charging

From Table 4-1, the output voltage function of a single H-bridge cell is:

$$v_{cell} = K_{cell} \times V_s \tag{4.1}$$

where v_{cell} is the output voltage of an H-bridge cell and K_{cell} is the switching function of the H-bridge cell which can be written as:

$$K_{cell} = \begin{cases} 1 & when\ S_1 = S_4 = 1, S_2 = S_3 = 0 \\ 0 & \begin{array}{c} when\ S_3 = S_4 = 1, S_1 = S_2 = 0 \\ or\ S_1 = S_2 = 1, S_3 = S_4 = 0 \end{array} \\ -1 & when\ S_2 = S_3 = 1, S_1 = S_4 = 0 \end{cases} \tag{4.2}$$

where for the states of S_1, S_2, S_3 and S_4, '1' represents on, '0' represents off.

Figure 4-2 shows the three-phase H-bridge MMC with n cells per arm. Each phase of the converter can generate up to $2n+1$ levels at the output terminals 'a', 'b' and 'c' relative to the neutral point. The average voltage across each cell capacitor is V_{DC}/n and the maximum voltage stress across each switching device is limited to one cell capacitor voltage. The transient arm voltages that synthesize the corresponding phase voltages of the H-bridge MMC are composed of the transient output voltages of the cells in the upper and lower arms. For phase a, the arm voltages are:

$$\begin{aligned} v_{1a} &= \sum_{i=1}^{n} K_{1ai} V_{s1ai} \\ v_{2a} &= \sum_{i=1}^{n} K_{2ai} V_{s2ai} \end{aligned} \tag{4.3}$$

where v_{1a} and v_{2a} donate the upper and lower arm voltages respectively, K_{1ai} and V_{s1ai} donate the i^{th} upper arm cell switching function and transient capacitor voltage (consisting of a DC component V_{DC}/n and AC components) and K_{2ai} and V_{s2ai} donate the i^{th} lower arm cell switching function and transient capacitor voltage. The equations of the arm voltages of phases b and c are similar to equation (4.3). The common mode currents generated by the transient voltage imbalance and instantaneous differential between the sum of upper and lower arm voltages and DC link voltage are limited by arm inductor L_a. For H-bridge MMC reliability, a voltage balancing strategy must regulate each cell capacitor voltage.

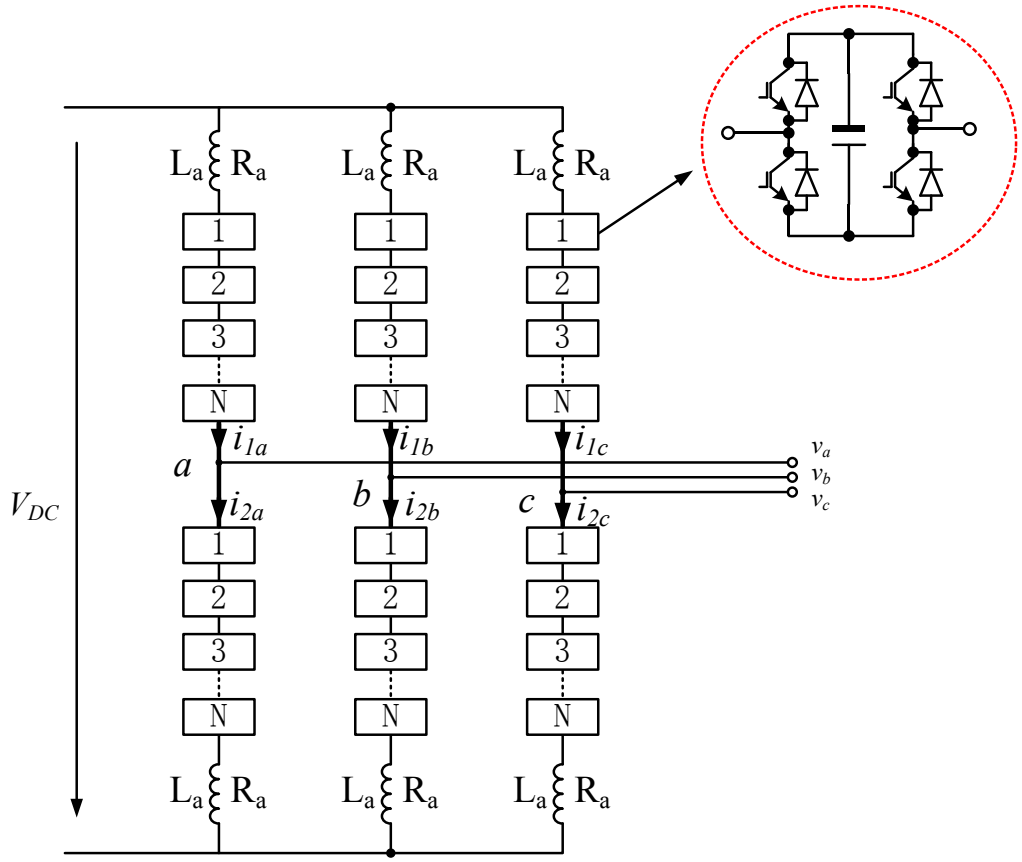


Figure 4-2. Three-phase of the *N*-level H-bridge MMC

A single phase H-bridge MMC with two cells per arm is shown in Figure 4-3. The circuit output voltage can be synthesized by the input DC link voltage and voltage of cell capacitors that are inserted in serial with the DC link voltage source. Different voltage levels can be achieved by turning on the appropriate switches. Each cell capacitor voltage is $½V_{DC}$, thus maximum voltage stress on each switch device is $½V_{DC}$. To explain how the H-bridge multilevel waveform voltage is synthesized, the DC source neutral point is used as the output voltage reference. As shown in Figure 4-3, there are six switch combinations to synthesize a three-level voltage between the output node and the DC link neutral point:

1. For voltage level $V_o = ½V_{DC}$, bypass all upper cell capacitors (turn on S_{11}, S_{12}, S_{21} and S_{22}) and connect in all lower cell capacitors (turn on S_{31}, S_{34}, S_{41} and S_{44}).
2. For voltage level $v_o = 0$, there are four switch combinations:
   (1) S_{11}, S_{14}, S_{21}, S_{22}, S_{31}, S_{34}, S_{41} and S_{42} on.
   (2) S_{11}, S_{12}, S_{21}, S_{24}, S_{31}, S_{34}, S_{41} and S_{42} on.
   (3) S_{11}, S_{14}, S_{21}, S_{22}, S_{31}, S_{32}, S_{41} and S_{44} on.

(4) S_{11}, S_{12}, S_{21}, S_{24}, S_{31}, S_{32}, S_{41} and S_{44} on.

(5) For voltage level $v_o = -½V_{DC}$, connect in all upper cell capacitors (turn on S_{11}, S_{14}, S_{21} and S_{24}), bypass all lower cell capacitors (S_{31}, S_{32}, S_{41} and S_{42} off).

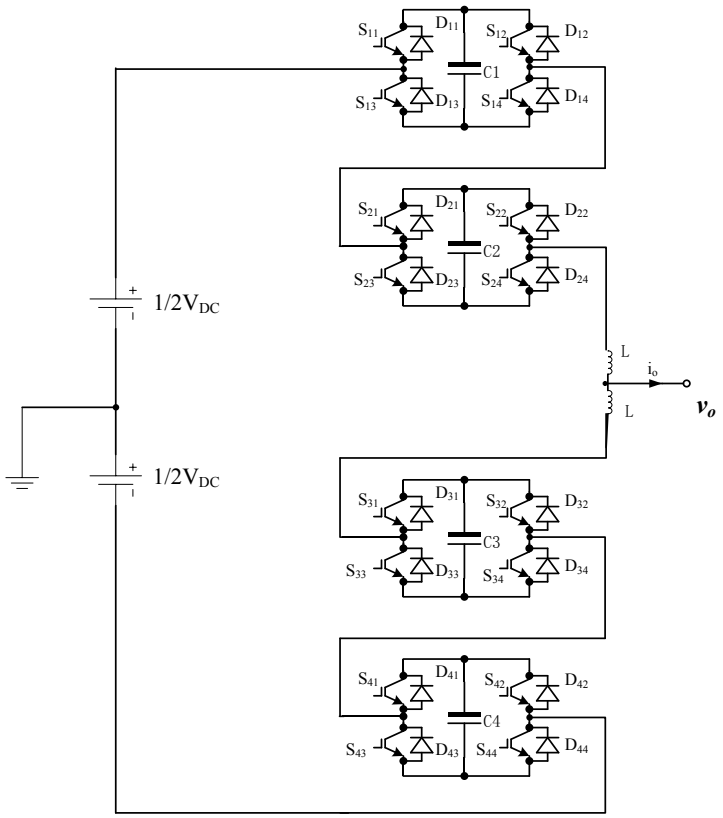


Figure 4-3. Single phase H-bridge modular multilevel converter

Table 4-2 lists the voltage levels and their corresponding switch states. 1 represents the switch is on, and 0 means the switch is off. In order to maintain equal voltage stress on the switching devices, the voltage across each cell capacitor must be maintained at $½V_{DC}$.

Table 4-2 Switch combinations for H-bridge multilevel converter

Output voltage v_o	S_{11}	S_{12}	S_{13}	S_{14}	S_{21}	S_{22}	S_{23}	S_{24}	S_{31}	S_{32}	S_{33}	S_{34}	S_{41}	S_{42}	S_{43}	S_{44}	
$½V_{DC}$	1	1	0	0	1	1	0	0	1	0	0	1	1	0	0	1	
0	1	0	0	1	1	1	0	0	1	0	0	1	1	1	0	0	(1)
	1	1	0	0	1	0	0	1	1	0	0	1	1	1	0	0	(2)
	1	0	0	1	1	1	0	0	1	1	0	0	1	0	0	1	(3)
	1	1	0	0	1	0	0	1	1	1	0	0	1	0	0	1	(4)
$-½V_{DC}$	1	0	0	1	1	0	0	1	1	1	0	0	1	1	0	0	

4.3 **Theoretical basis of normal operation control strategy**

Figure 4-4 shows a linear model of one phase leg of the H-bridge MMC in Figure 4-3. The H-bridge cells in the upper and lower arms are replaced by two ideal controlled voltage sources which are related to the arm voltages. In order to take into account the cell capacitor dynamics, lumped capacitors C_1 and C_2 corresponding to the total capacitance of the upper and lower arms are implemented. Two current sources regulated by the arm currents are utilised to charge or discharge the capacitors C_1 and C_2. This simplified model aims to illustrate the fundamental MMC theory and its control and capacitor voltage balancing strategy.

Using Kirchhoff current and voltage laws, algebraic and differential equations that describe steady state and internal dynamics of the MMC are:

$$i_o = i_1 - i_2 \tag{4.4}$$

$$\tfrac{1}{2}V_{DC} - v_1 - v_o = R_a i_1 + L_a \frac{di_1}{dt} \tag{4.5}$$

$$\tfrac{1}{2}V_{DC} - v_2 + v_o = R_a i_2 + L_a \frac{di_2}{dt} \tag{4.6}$$

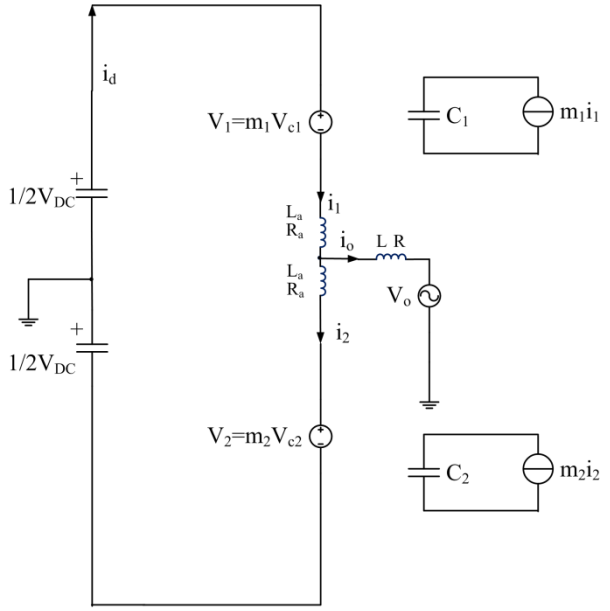
where i_1 and i_2 are MMC upper and lower arm currents, V_{DC} is the DC link voltage, v_1 and v_2 are voltage developed across the entire cell capacitors of the upper and lower arms, v_o is the output phase voltage relative to virtual supply mid-point, and R_a and L_a are the resistances and inductance of the arm reactors.

Subtracting (4.6) from (4.5), gives

$$-v_1 + v_2 - 2v_o = R_a(i_1 - i_2) + L_a \frac{d(i_1 - i_2)}{dt} \tag{4.7}$$

After combining (4.4) and (4.7):

$$-v_1 + v_2 - 2v_o = R_a i_o + L_a \frac{di_o}{dt} \tag{4.8}$$



m_1: modulation waveform for upper arm cells

m_2: modulation waveform for lower arm cells

V_{c1}: voltage across cell capacitor C_1

V_{c2}: voltage across cell capacitor C_2

Figure 4-4. Linear model of single phase multilevel converter.

Equation (4.8) relates output phase current i_o to inverter output voltage v_o and upper and lower arm voltages v_1 and v_2. This equation shows that in order to synthesize pure sinusoidal ac output phase current i_o, the left side of (4.8) must purely sinusoidal, this means $-v_1+v_2-2v_o$ must be a pure AC sinusoidal form. If arm reactor is sized properly and sufficiently small, the voltage drop across the upper and lower arm reactors will be much smaller than that developed across their corresponding cell capacitors v_1 and v_2. Therefore, the left side of (4.8) can be approximated as:

$$-v_1 + v_2 \approx 2v_o \tag{4.9}$$

Adding equation (4.5) into (4.6), gives:

$$V_{DC} - (v_1 + v_2) = R_a(i_1 + i_2) + L_a \frac{d(i_1 + i_2)}{dt} \tag{4.10}$$

If the left side of the equation (4.10) is controlled to be pure DC, the sum of the upper and lower arm currents i_1+i_2 must be a DC current; therefore:

$$i_1 + i_2 = 2i_{dc} \tag{4.11}$$

This means equation (4.10) can be re-arranged as:

$$V_{DC} - (v_1 + v_2) = R_a i_{dc} + L_a \frac{di_{dc}}{dt} \tag{4.12}$$

If v_1+v_2 is controlled to be higher than V_{DC}, the power flow will be from the AC side to the DC side; when it is lower than V_{DC} the power flow is in the opposite direction. Thus v_1+v_2 is regulated at V_c:

$$v_1 + v_2 = V_c \tag{4.13}$$

This permits the converter output voltage to be expressed as: $v_o=½mV_c\sin\omega t$, whence equation (4.9) is re-arranged as:

$$-v_1 + v_2 = mV_c \sin \omega t \tag{4.14}$$

where m is the modulation index.

After solving (4.13) and (4.14), the voltages across the upper and lower arms are:

$$\begin{aligned} v_1 &= \tfrac{1}{2} V_c (1 - m \sin \omega t) \\ v_2 &= \tfrac{1}{2} V_c (1 + m \sin \omega t) \end{aligned} \tag{4.15}$$

Equation (4.15) provides the mathematical proof of the complementary operation of the H-bridge MMC arms. From (4.15), the modulation waveforms for the upper and lower arms can be resolved into DC and AC components as:

$$\begin{aligned} m_1 &= (1 - m \sin \omega t) = m_d - m_a \\ m_2 &= (1 + m \sin \omega t) = m_d + m_a \end{aligned} \tag{4.16}$$

where $m_d=1$ and $m_a=m\sin\omega t$. Similarly, the upper and lower arm currents of the MMC are resolved into difference and common mode components as:

$$\begin{aligned} i_1 &= i_{d1} + i_{o1} \\ i_2 &= i_{d2} - i_{o2} \end{aligned} \tag{4.17}$$

After substituting (4.17) into (4.4):

$$(i_{d1} - i_{d2}) + (i_{o1} - i_{o2}) = i_o \tag{4.18}$$

The DC component of equation (4.18) must vanish in order to synthesize sinusoidal output current i_o: this means $i_{d1} - i_{d2} = 0 \Rightarrow i_{d1} = i_{d2} = i_d$.

Similarly, substitute (4.17) into (4.11):

$$(i_{d1} + i_{d2}) + (i_{o1} + i_{o2}) = i_{dc} \tag{4.19}$$

For the common mode current in (4.19) to be a pure DC current, as assumed, its AC fundamental component $i_{o1}+i_{o2}$ must vanish; therefore $i_{o1}=-i_{o2}$. Substituting $i_{o1}=-i_{o2}$, yields $i_{o1}=½i_o$ and $i_{o2}=-½i_o$, showing:

$$i_1 = i_{dc} + \tfrac{1}{2} i_o$$
$$i_2 = i_{dc} - \tfrac{1}{2} i_o \tag{4.20}$$

Equation (4.20) is the mathematical proof of the current distribution in the MMC arms, which is universally accepted and widely used in the literature.

From (4.12) and (4.13), i_{dc} can be written as:

$$i_{dc} = K_1 e^{-\frac{R_a}{L_a}t} + \frac{V_{DC} - V_c}{2R_a} \tag{4.21}$$

Substituting (4.14) into (4.8):

$$i_o R_a + L_a \frac{di_o}{dt} = -2v_o + mV_c sin\omega t \tag{4.22}$$

Assuming the load consists of an inductor L and a resistor R, then:

$$v_o = i_o R + L \frac{d\, i_o}{dt} \tag{4.23}$$

Substituting (4.23) into (4.22):

$$i_o R_a + L_a \frac{di_o}{dt} = -\,(2i_o R + 2L \frac{di_o}{dt}) + mV_c sin\omega t \tag{4.24}$$

Considering $R_T = 2\left(\tfrac{1}{2}R_a + R\right)$ and $L_T = 2\left(\tfrac{1}{2}L_a + L\right)$, then (4.22) can be derived as:

$$i_o R_T + L_T \frac{di_o}{dt} = mV_c sin\omega t \tag{4.25}$$

From (4.25), i_o can be written as:

$$i_o = K \exp\left[-\left(\tfrac{1}{2}R_a + R\right)t \Big/ \left(\tfrac{1}{2}L_a + L\right)\right] + \frac{\frac{1}{2}mV_c}{\sqrt{\left(\tfrac{1}{2}R_a + R\right)^2 + \left(\tfrac{1}{2}L_a + L\right)^2}} \sin(\omega t + \varphi) \tag{4.26}$$

where $\varphi = arctan\dfrac{R_T}{\omega L_T}$.

From equation (4.26), the steady state load current i_o is determined by V_c, combined resistances and inductances of the load and arm reactors, and the modulation index. The decay of the transient component of i_o is determined by the combined time constant $\tau_c = \left(\tfrac{1}{2}L_a + L\right)\Big/\left(\tfrac{1}{2}R_a + R\right)$. In normal operation, V_c is maintained at rated value, thus i_o can be regulated by the modulation index.

4.4 Sinusoidal pulse width modulation (SPWM) for H-bridge MMC

Carrier-based PWM is used to separately control each phase of the H-bridge MMC and to allow the line-to-line voltage to be developed implicitly [23]. These carrier-based PWM schemes are derived from the carrier disposition strategy [24, 25]. For H-bridge MMC with two cells per arm, 2 triangular carriers with the same frequency and amplitude are arranged. The sinusoidal references that are related to the upper and lower arm voltages of each phase are compared with the carriers to determine the switching combinations.

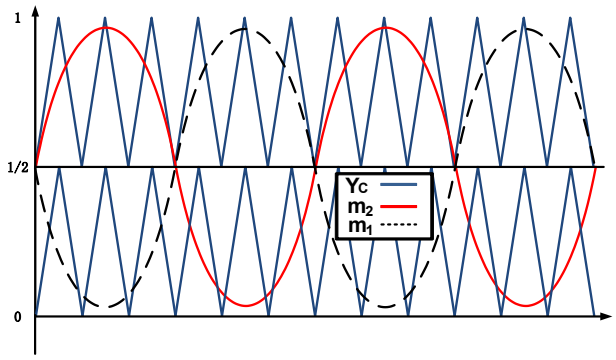


Figure 4-5. Carrier and reference waveforms for upper and lower arm voltages

For voltage balancing between the upper and lower arm capacitors, the references are complimentary and the modulation index for the upper and lower arm voltages are identical. When the upper arm reference signal m_1 is greater than the upper triangular signal, the transient equivalent upper arm voltage v_1 equals V_{DC}, and when the reference signal is less than the lower carrier, the transient equivalent upper arm voltage v_1 equals 0. The last condition is that the transient equivalent upper arm voltage v_1 equals $½V_{DC}$. The PWM principle for the lower arm voltage v_2 is similar to that of v_1, but the generated voltage value of v_2 is opposite to v_1 due to the upper and lower arm voltage references being complimentary. From equation (4.9), the output voltage of H-bridge MMC can be synthesized by v_1 and v_2, as: $-v_1 + v_2 = 2v_o$. When v_o= 0, the corresponding transient upper and lower arm voltages are:

$$v_1 = v_2 = ½V_{DC} \tag{4.27}$$

These conditions can be generated by 4 switching combinations that are referred to as redundant switch states. These states are used to balance the cell capacitor voltages.

4.5 Cell capacitor voltage balancing

When output voltage is zero, the upper capacitors are charged by the upper arm current during the positive half of the load current ($i_o>0$), the lower capacitors are discharged by the lower arm current. When the output current is negative ($i_o<0$) the upper capacitors discharge whereas the lower capacitors charge due to the upper and lower arm currents respectively. Figure 4-6 shows capacitor loading when the output voltage is zero, with all possible switch states.

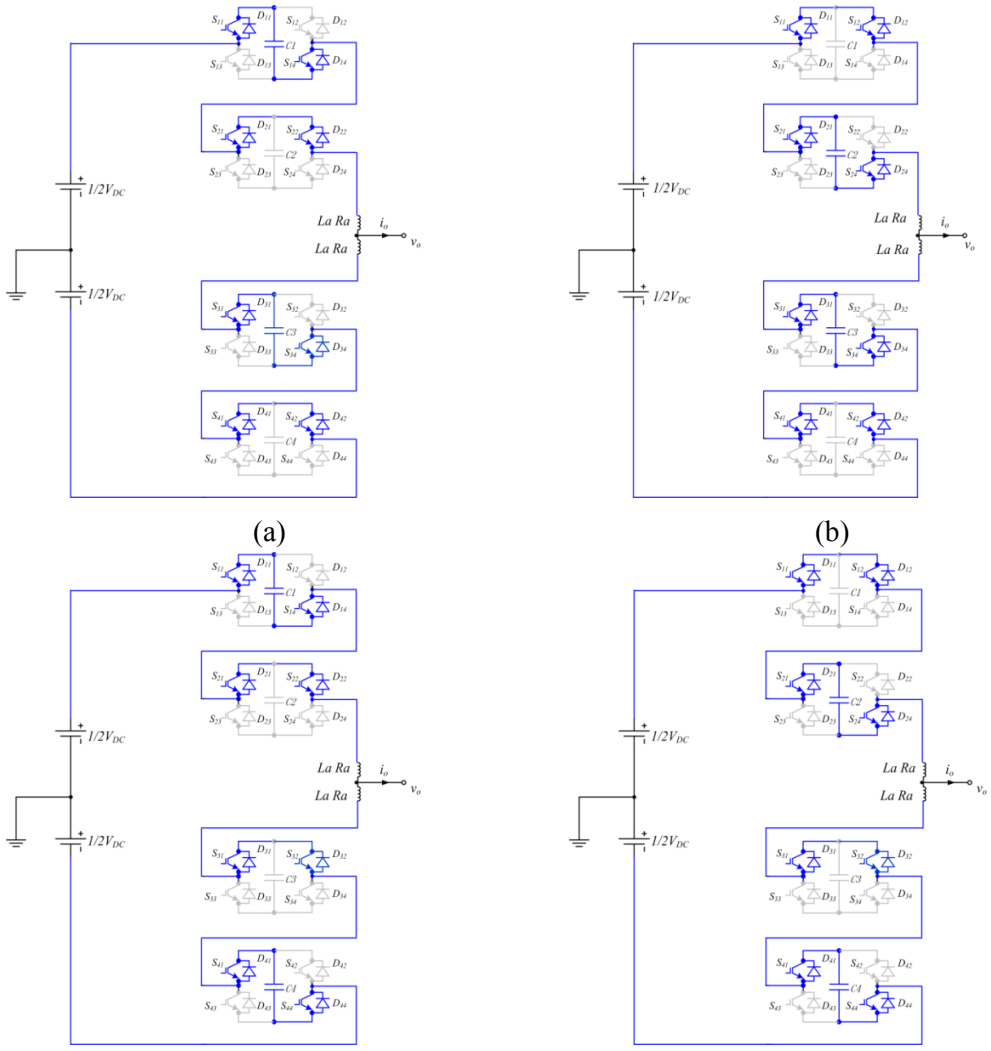


Figure 4-6. Current path at zero voltage level state for capacitor voltage balancing

The current paths shown in Figure 4-6 (a) to (d) represent the redundant switch states (1), (2), (3) and (4) in Table 4-2 which demonstrate the cell capacitor voltage balancing process while the upper and lower capacitors are alternatively used to supply load power. Both modulation schemes, such as carrier-based or space vector modulation, must use the voltage balancing strategy with the switch combinations

periodically to compensate the unbalance capacitor voltages. Table 4-3 summarizes all the switch states and their effect on each capacitor voltage.

Capacitor voltage balancing method for a three-level H-bridge MMC can be summarized as follows:

1. Classify the upper and lower capacitors with the maximum and minimum voltage using

$$\begin{aligned} V_{upper\_max} &= max\left(V_{c1}, V_{c2}\right), \\ V_{upper\_min} &= min\left(V_{c1}, V_{c2}\right), \\ V_{Lower\_max} &= max\left(V_{c3}, V_{c4}\right), \\ V_{Lower\_min} &= min\left(V_{c3}, V_{c4}\right). \end{aligned} \tag{4.28}$$

2. If output current i_o>0, select a switch state that charges the upper capacitor retaining the minimum voltage and discharges the lower capacitor retaining the maximum voltage.
3. If output current i_o<0, select a switch state that discharges the upper capacitor with the maximum voltage and charges the lower capacitor with the minimum voltage.

Table 4-3 Effect of redundant switch states on capacitor voltage

Switch states	Current direction	Current path	Connected capacitors
(1) 1001110010011100	i_o>0	D_{11}, D_{14}, D_{21}, S_{22}, S_{31}, S_{34}, S_{41} and D_{42}	C_1↑ and C_3↓
	i_o<0	S_{11}, S_{14}, S_{21}, D_{22}, D_{31}, D_{34}, D_{41} and S_{42}	C_1↓ and C_3↑
(2) 1100100110011100	i_o>0	D_{11}, S_{12}, D_{21}, D_{24}, S_{31}, S_{34}, S_{41} and D_{42}	C_2↑ and C_4↓
	i_o<0	S_{11}, D_{12}, S_{21}, S_{24}, D_{31}, D_{34}, D_{41} and S_{42}	C_2↓ and C_4↑
(3) 1001110011001001	i_o>0	D_{11}, D_{14}, D_{21}, S_{22}, S_{31}, D_{32}, S_{41} and S_{44}	C_1↑ and C_4↓
	i_o<0	S_{11}, S_{14}, S_{21}, D_{22}, D_{31}, S_{32}, D_{41} and D_{44}	C_1↓ and C_4↑
(4) 1100100111001001	i_o>0	D_{11}, S_{12}, D_{21}, D_{24}, S_{31}, D_{32}, S_{41} and S_{44}	C_2↑ and C_3↓
	i_o<0	S_{11}, D_{12}, S_{21}, S_{24}, D_{31}, S_{32}, D_{41} and D_{44}	C_1↓ and C_3↑

The voltage balancing strategy based on (1) to (4) is implemented within the modulator; the instants at which switching from one combination to another occurs is based on the voltage level across each capacitor. By this method cell capacitor voltage balance is maintained.

4.6 Current Control scheme for grid connection with Phase lock loop

In a grid connection mode, the single-phase H-bridge MMC output AC current i_o is phase synchronized with the grid voltage v_g while the magnitude of MMC output voltage v_o is stabilized at the set value. Based on equations (4.9) and (4.15), the magnitude of v_o can be determined by controlling modulation index m of AC components of upper and lower arm voltage references m_1 and m_2. For regulating the AC current i_o, the grid voltage phase angle is calculated by a phase lock loop. The fundamental current control diagram is shown in Figure 4-7.

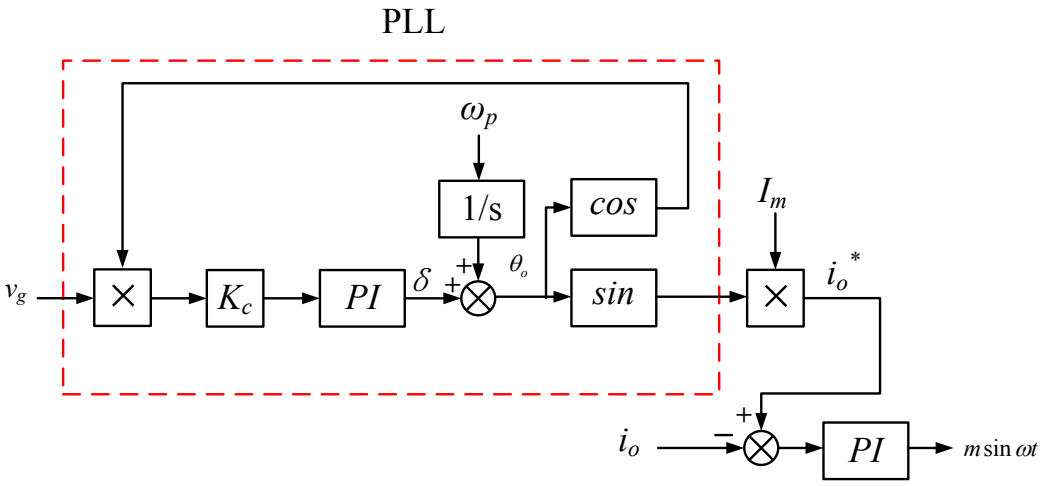


Figure 4-7. Control diagram for AC fundamental current i_o

The grid voltage $v_g = \frac{1}{2} m V_m \sin\omega t$ is multiplied by generated phase lock loop output $\cos\theta_o$:

$$v_g \times \cos\theta_o = \tfrac{1}{2} V_m \left[\sin(\omega t - \theta_o) + \sin(\omega t + \theta_o) \right] \tag{4.29}$$

where θ_o consists of the PI output angle δ and the expected frequency ω_p:

$$\theta_o = \delta + \omega_p t \tag{4.30}$$

Substituting (4.30) into (4.29):

$$v_g \times \cos\theta_o = \frac{1}{2} V_m [\sin((\omega - \omega_p)t - \delta) + \sin((\omega + \omega_p)t + \delta)] \tag{4.31}$$

For a grid connected system, the frequency of grid voltage is constant. Thus the difference between the expected frequency and the grid voltage frequency can be ignored when the control system is stabilized: $\omega_p=\omega=2\pi f$. (4.31) can be deduced as:

$$v_g \times cos\theta_o = \frac{1}{2}V_m[-sin\delta + sin(2\omega t + \delta)] \tag{4.32}$$

Equation (4.32) consists of a second harmonic component which can be eliminated by a low pass filter. Hence, the linearized input for the PI is:

$$v_g \times cos\theta_o = -\tfrac{1}{2}V_m sin\delta \tag{4.33}$$

While δ is small, $sin\delta \approx \delta$. At steady state, the difference between the expected phase angle and the grid voltage phase angle δ, reduces to zero. The peak current reference I_m multiplied by $sin\theta_o$ is set to be the grid current reference. When $\delta = 0$, $sin\theta_o$ becomes $sin\omega t$, the reference for grid current is $I_m \sin\omega t$ which is phase synchronised with the grid voltage v_g.

The generated AC components of the modulation references of the upper and lower arm voltages are the inputs to the SPWM control block. The switch combinations are determined by the SPWM control signals and cell capacitor voltage balancing strategy to synthesize v_1 and v_2, as displayed in Figure 4-8.

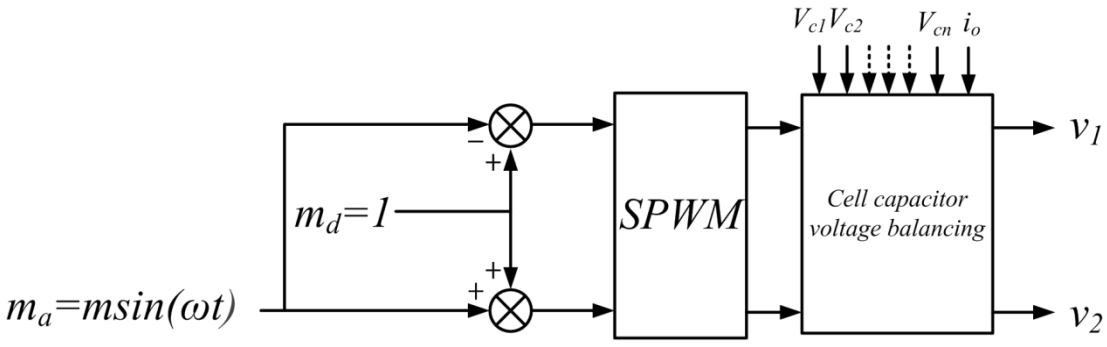


Figure 4-8. SPWM control diagram for the upper and lower arm voltages

4.7 **Simulation**

The capability of the single phase H-bridge MMC to operate at different load power factors and modulation indices at off-grid conditions is validated by the simulations, and at grid-connected conditions the control scheme is verified with H-bridge MMC

at variable operating conditions with different cell numbers. Sinusoidal PWM with phase disposition carriers and the cell capacitor voltage balancing scheme are implemented to control the converter to generate the desired output and to maintain cell capacitor voltage balancing. Table 4-4 summarises the converter parameters used for simulations in this section. The capacitance and arm inductance values are set to suppress the ripple components of capacitor voltages and arm currents. They are also related to the DC fault protection that will be described in Chapter 5.

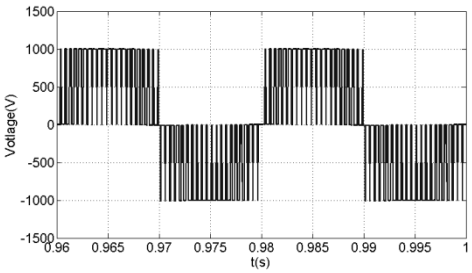
Table 4-4 Simulation parameters

Converter rating	40kW
Modulation indices	0.8 and 0.9
Capacitance	4.7mF
Switching frequency	2.1kHz
DC link voltage	2kV
Arm inductance	3.3mH
Rated frequency	50Hz
Grid voltage $V_{gp\text{-}p}$	850V

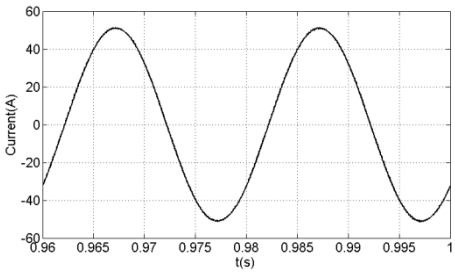
4.7.1 Simulations of three-level H-bridge MMC

I. Off-grid condition

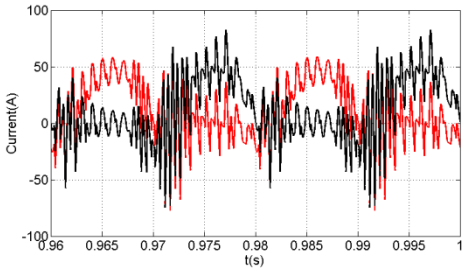
Figure 4-9 shows the simulation results when the three-level H-bridge MMC operates at 0.9 modulation index and 0.8 power factor lagging. The output voltage waveforms in Figure 4-9(a) shows the converter generated output voltage. Figure 4-9(b) shows that the output current is regulated and maintained sinusoidal. Figure 4-9(c) and (d) illustrate the arm currents and the common mode current that contain harmonic components which can be suppressed by the control scheme presented in next chapter. Figure 4-9(e) displays the cell capacitor voltages that are balanced at the set point.



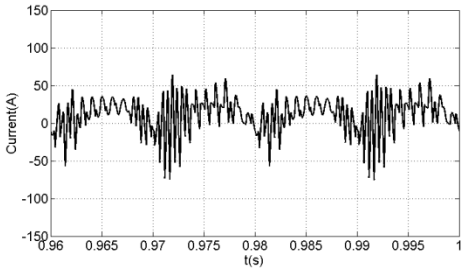
a) Output voltage of H-bridge MMC



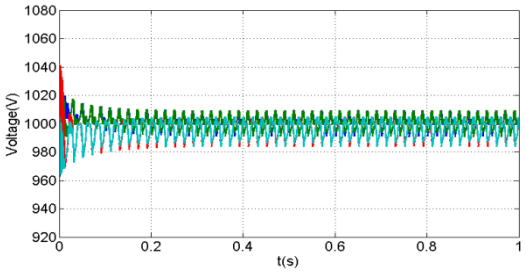
b) Output current waveform



c) Upper and lower arm current waveform



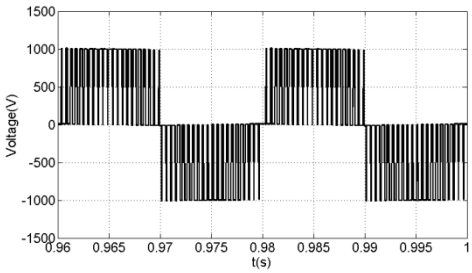
d) Common mode current ($i_{dc}=½(i_1+i_2)$)



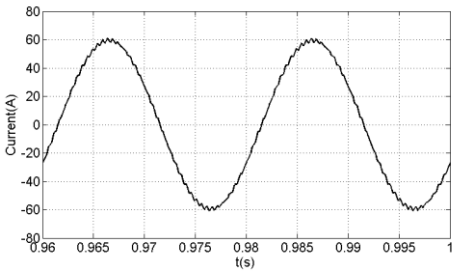
e) Cell capacitor voltage of the upper and lower arms

Figure 4-9. Waveforms when three-level MMC is simulated at 0.9 modulation index and 0.8 power factor lagging.

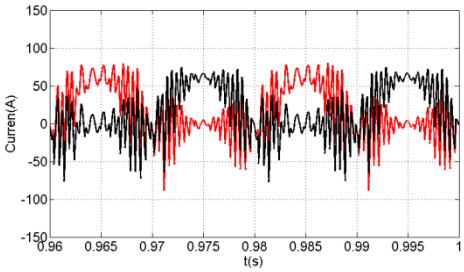
Figure 4-10 shows when the converter is operated at 0.8 modulation index and 0.9 power factor lagging. The H-bridge MMC is able to operate with cell capacitor voltages balanced and generates output current with low harmonic components at high power factor. These features illustrate that the H-bridge MMC is capable of operating over wide modulation index range regardless of the load power factor.



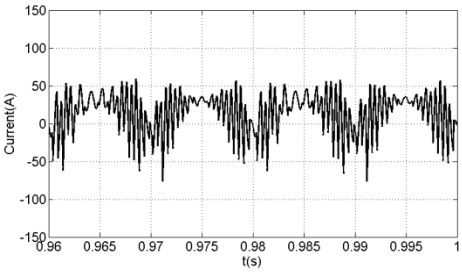
a) Output voltage of H-bridge MMC



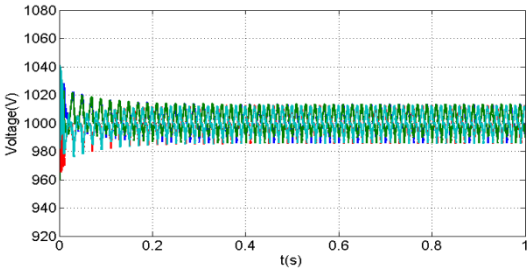
b) Output current waveform



c) Upper and lower arm current waveform



d) Common mode current ($i_{dc}=½(i_1+i_2)$)

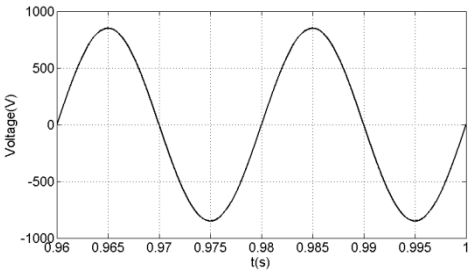


e) Cell capacitor voltages of the upper and lower arms

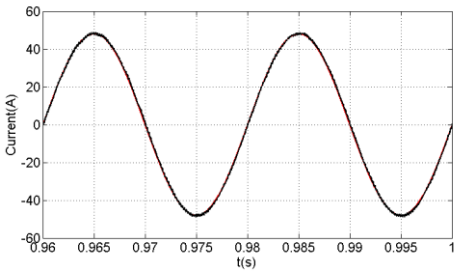
Figure 4-10. Waveforms when three-level modular converter is simulated at 0.8 modulation index and 0.9 power factor lagging.

II. Grid-connected condition

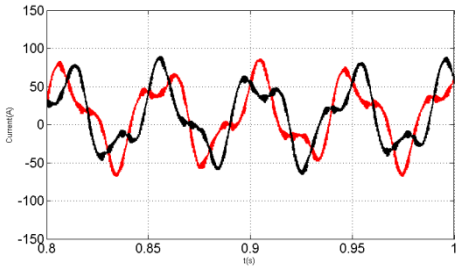
The H-bridge MMC is connected to the AC grid with phase lock loop to verify energy exchange during normal operation. The grid voltage peak magnitude is $V_{gp\text{-}p}$ = 850V while other parameters remain those of the off-grid condition. Figure 4-11(a) and (b) show the converter AC terminal voltage and the output current i_o follows the reference i_o^* that is generated by the control loop in Figure 4-7. Figure 4-11(c) and (d) illustrate that the arm currents and common mode current contain low frequency harmonics which can be eliminated by the control strategy presented in next chapter. Capacitor voltage balancing is seen in Figure 4-11(g).



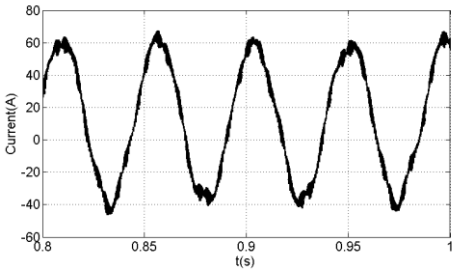
a) Grid voltage



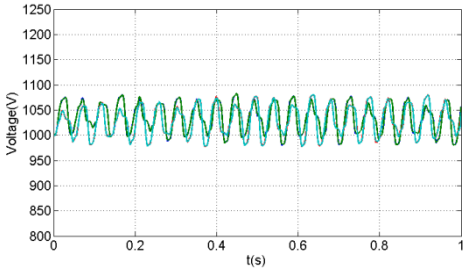
b) Current waveform converter injects into grid and its reference



c) Upper and lower arm current waveform



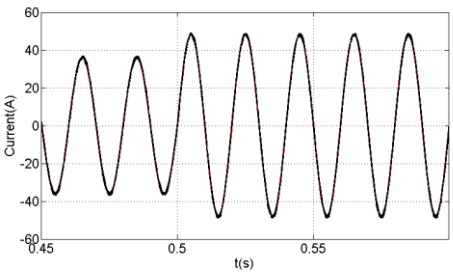
d) Common mode current ($i_{dc}=½(i_1+i_2)$)



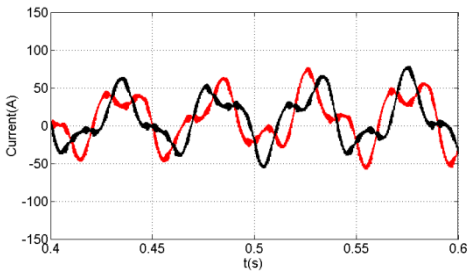
e) Cell capacitor voltage of the upper and lower arms

Figure 4-11. Selected simulation waveforms when illustrative version of the single-phase H-bridge MMC is controlled with the presented control scheme in Figure 4-7 at unity power factor

Figure 4-12 shows the simulation results when an output current step change is applied at t=0.5s, where the initial peak current is 36A and the increased current is 54A. The output current is tightly regulated during the full period which demonstrates that the control strategy is viable over the full modulation index range.

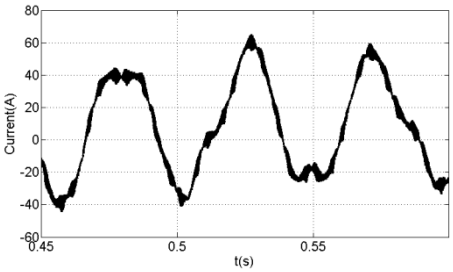


a) Current waveform converter injects into grid and its reference zoomed around the instant where step change is applied to



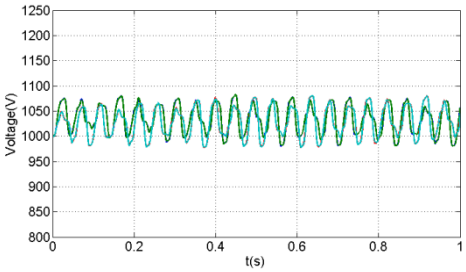
b) Upper and lower arm currents zoomed around the instant where step change is applied to the peak of the reference

the peak of the reference current



c) Common mode current (i_{dc}=½(i_1+i_2))and and its reference sets by the DC voltage regulator that controls cell capacitor voltage of the upper and lower arms

output current



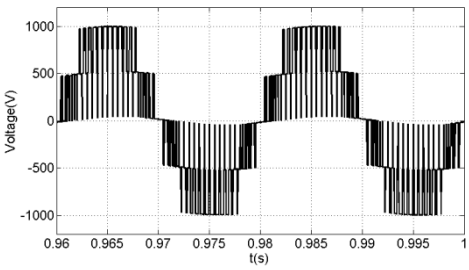
d) Cell capacitor voltage of the upper and lower arms

Figure 4-12. Simulation waveforms when at t=0.5s a step change is applied that increases the output peak reference current from I_m=36A to 54A.

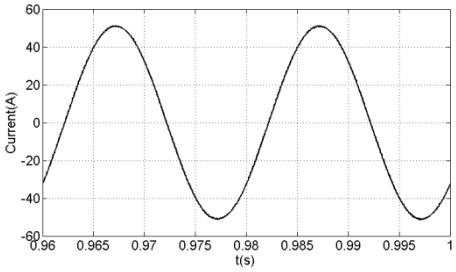
4.7.2 Five-level H-bridge MMC simulations

I. Off-grid condition

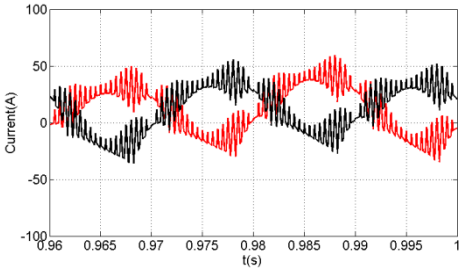
The five-level output voltage is synthesized when exploiting the bi-polarity feature of the MMC H-bridge cells, with two cells per arm. The H-bridge MMC operates at 0.9 and 0.8 modulation index with 0.8 and 0.9 power factor respectively. Figure 4-13 and Figure 4-14 show that the output voltage and current while the harmonic components in the arm currents and common mode current cannot be eliminated by increasing the output voltage levels.



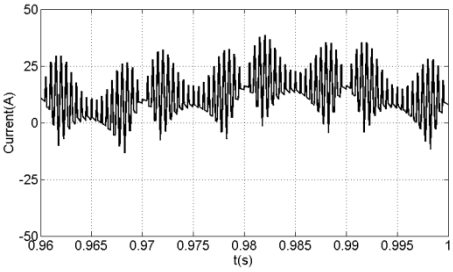
a) Output voltage of H-bridge MMC



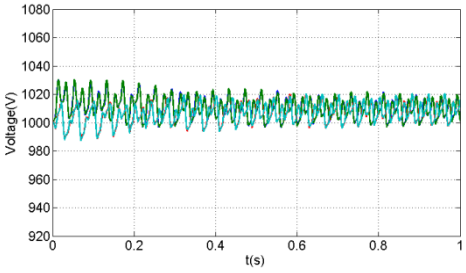
b) Output current waveform



c) Upper and lower arm current waveform

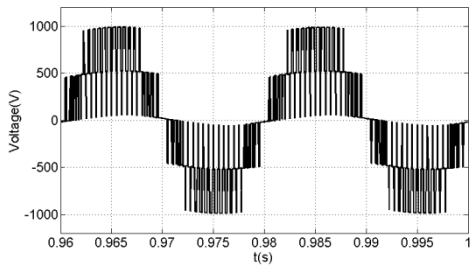


d) Common mode current (i_{dc}=½(i_1+i_2))

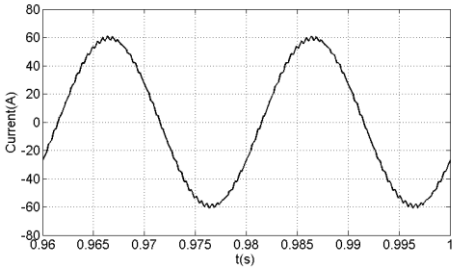


e) Cell capacitor voltage of the upper and lower arms

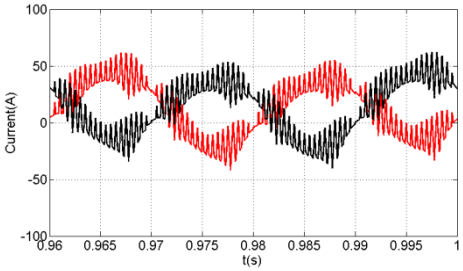
Figure 4-13. Waveforms when a five-level H-bridge MMC is simulated at 0.9 modulation index and 0.8 power factor lagging



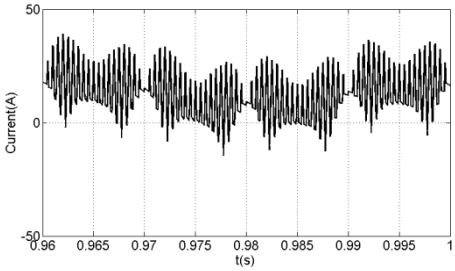
a) Output voltage of H-bridge MMC



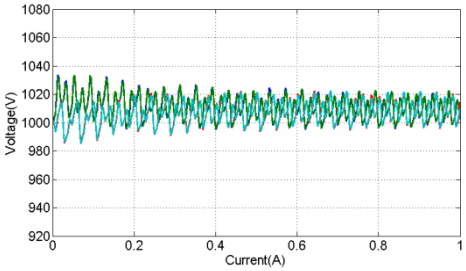
b) Output current waveform



c) Upper and lower arm current waveform



d) Common mode current (i_{dc}=½(i_1+i_2))



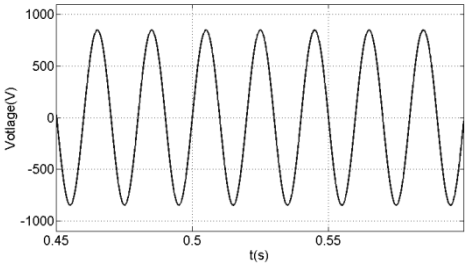
e) Cell capacitor voltage of the upper and lower arms

Figure 4-14. Waveforms when five-level H-bridge modular converter is simulated at 0.8 modulation index and 0.9 power factor lagging

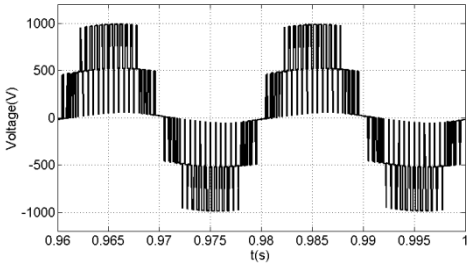
II. Grid-connected condition

The H-bridge MMC is connected to the AC grid with a phase lock loop while the parameters are as for the grid connection case of three-level H-bridge MMC. The step change is applied at t=0.5s. As shown in Figure 4-15, the output current is

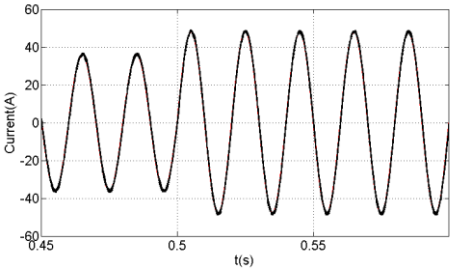
tightly regulated during the full period and the converter output voltage is stabilized which illustrates that the control strategy is viable for any number of H-bridges. The harmonic components in the upper and lower arm currents and the oscillating magnitude of the common mode current remain identical to the three-level H-bridge MMC grid connected case.



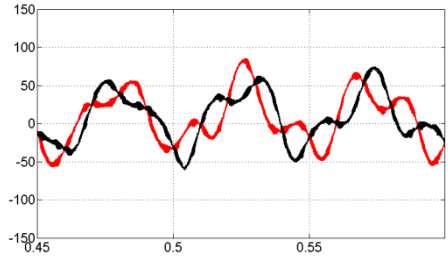
a) Grid voltage



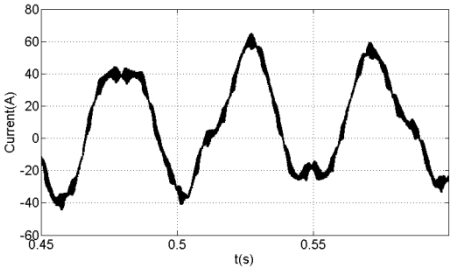
b) Output voltage of H-bridge MMC relative to the supply mid-point



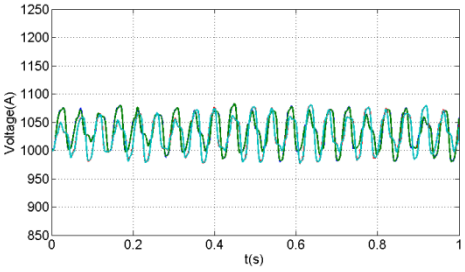
c) Current waveform converter injects into grid and its reference zoomed around the instant where step change is applied to the peak of the reference current



d) Upper and lower arm currents zoomed around the instant where step change is applied to the peak of the reference output current



e) Common mode current (i_{dc}=½(i_1+i_2))

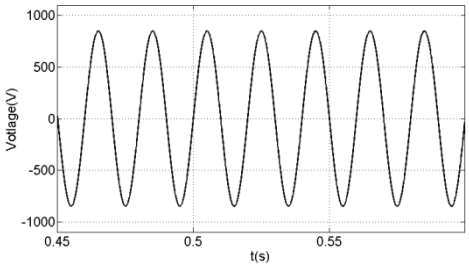


f) Cell capacitor voltage of the upper and lower arms

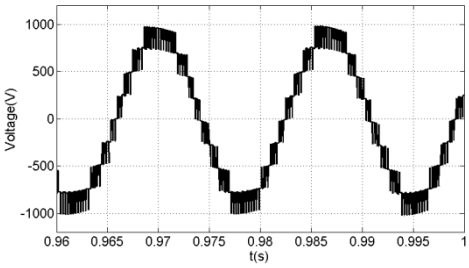
Figure 4-15. Simulation waveforms when at t=0.5s step change is applied that increases the output peak reference current from I_m=36A to 54A for a five-level H-bridge MMC

4.7.3 Nine-level H-bridge MMC simulations

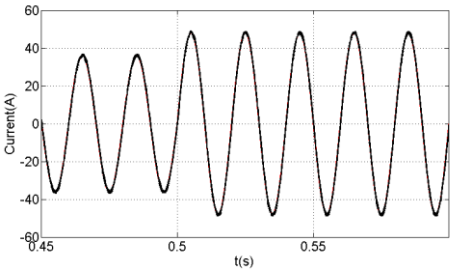
A nine-level H-bridge MMC with four cells per arm is connected to an AC grid to validate the viability of the control scheme and voltage balancing method, with a different number of cells per arm. The converter output AC current is phase locked with the grid voltage in Figure 4-16(a) and (b), while the output voltage relative to the converter neutral point is nine-levels in Figure 4-16(c). The cell capacitor voltages remain balanced while the voltage magnitude and ripple decrease to half of the H-bridge MMC with two cells per arm. However, the distortion in the arm currents and the common mode current are not significantly improved.



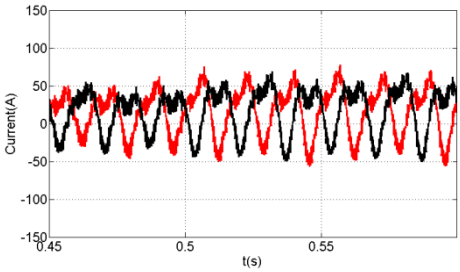
a) Grid voltage



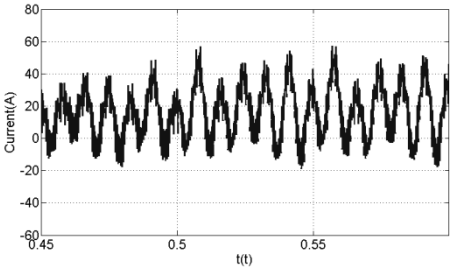
b) Output voltage of H-bridge MMC relative to supply mid-point



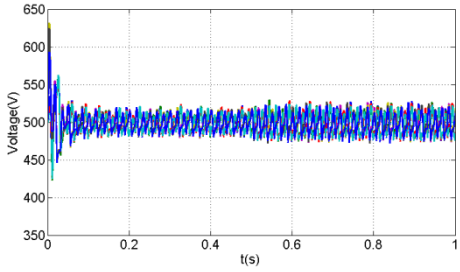
c) Current waveform converter injects into grid and its reference zoomed around the instant where step change is applied to the peak of the reference current



d) Upper and lower arm currents zoomed around the instant where step change is applied to the peak of the reference output current



e) Common mode current (i_{dc}=½(i_1+i_2))



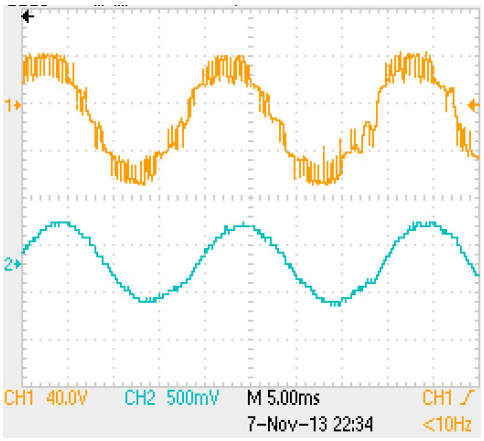
f) Cell capacitor voltage of the upper and lower arms

Figure 4-16. Simulation waveforms when at t=0.5s step change is applied that increases the output peak reference current from I_m=36A to 54A, for a nine-level H-bridge MMC

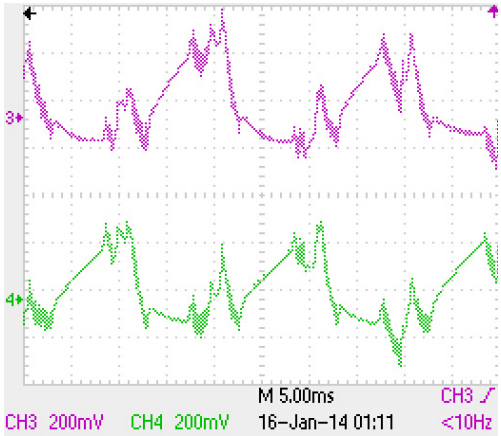
4.8 Experimental validation

This section provides experimental validation of the control scheme and simulation results presented. The practical results are obtained from a single-phase H-bridge MMC that is shown in Fig A-1 (Appendices section) with a 100V DC link voltage, 4,7mF cell capacitors, and 3.3mH arm inductance. The converter is controlled by the operational principle presented in section 4.1 with SPWM in Figure 4-5 for an off-grid condition and with a phase lock loop (PLL) in Figure 4-7 for grid connection. An Infineon Technology Tri-core microcontroller TC 1796 is used to program the modulation and capacitor voltage balancing strategy.

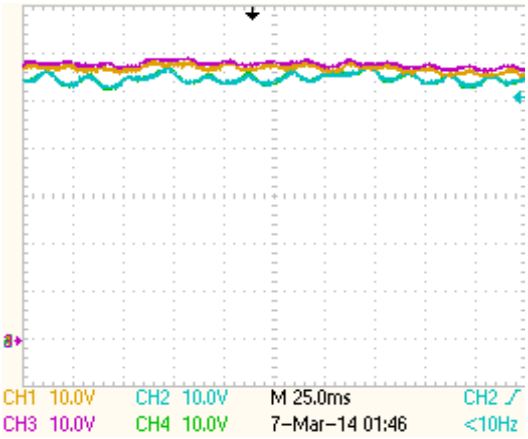
Figure 4-17 shows the experimental results at 0.9 power factor lagging. The converter operates successfully in an off-grid condition with high quality output current and cell capacitor voltages balanced. Figure 4-18 is the experiment results during a grid connected condition. The grid voltage and current are synchronised by the AC current control loop, utilizing its upper and lower arm inductors as low-pass filters. This confirms the viability of the operational principle and capacitor voltage balancing method, grid connected where the switching frequency and power factor are restrictive features, although the upper and lower arm currents and common mode current include harmonic components.



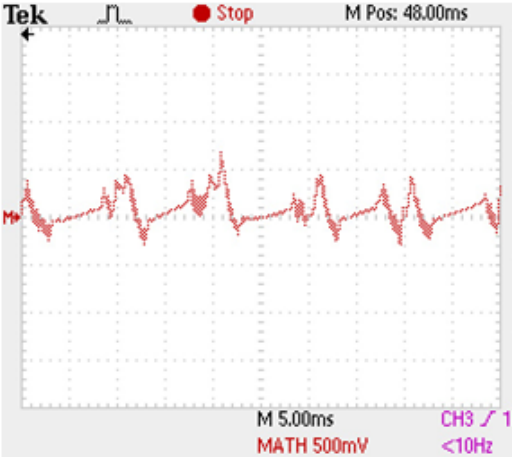
a) Output voltage and current of H-bridge MMC(scale: 5ms/div, 40V/div,5A/div)



b) Upper and lower arm currents (scale: 5ms/div, 2A/div)

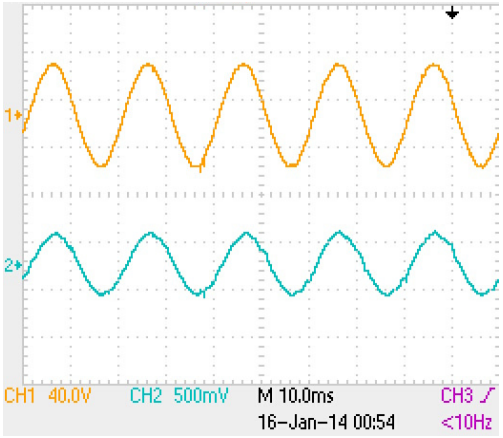


c) Cell capacitor voltage of the upper and lower arms (25ms/div, 10V/div)

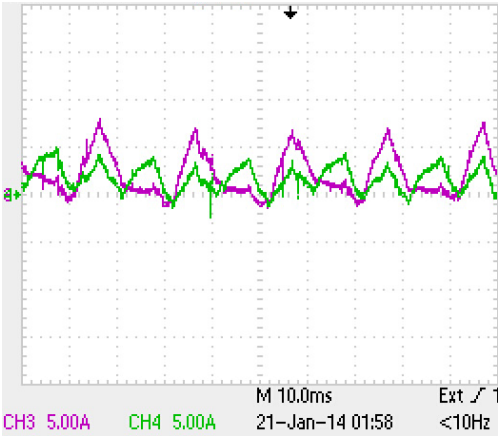


d) Common mode current (i_{dc}=½(i_1+i_2)) (5ms/div, 5A/div)

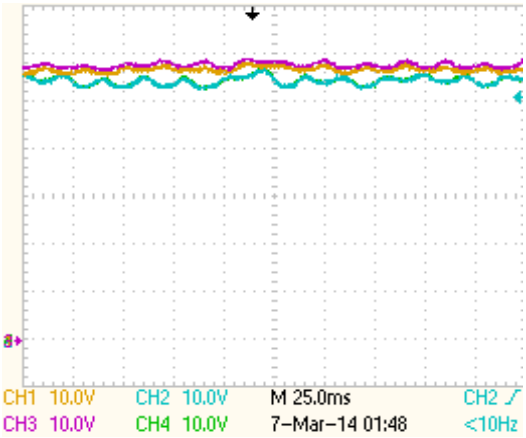
Figure 4-17. Waveforms from the single-phase five-level H-bridge MMC at 0.9 modulation index and 0.9 power factor.



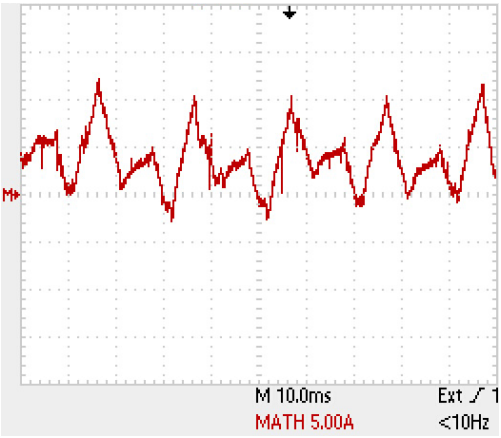
a) Grid voltage and current of H-bridge MMC(scale: 10ms/div, 40V/div,5A/div)



b) Upper and lower arm currents (scale: 10ms/div, 5A/div)



c) Cell capacitor voltage of the upper and lower arms (25ms/div, 10V/div)



d) Common mode current (i_{dc}=½(i_1+i_2)) (5ms/div, 5A/div)

Figure 4-18. Waveform from the single-phase five-level H-bridge MMC grid-connection at unity power factor.

4.9 **Summary**

This chapter analyzed the H-bridge MMC operational principle, cell capacitor voltage balancing strategy, and AC current control scheme, with a phase lock loop for grid connection. The capability and advantages of the presented control scheme have been validated by simulations as well as experimentation. As the H-bridge MMC is the only MMC able to provide cell voltage bi-polarity, it has been selected as representative for this investigation. The results demonstrate that the H-bridge MMC offers the following features: capability of operating at different modulation indices and power factors, low voltage stress on the switching devices (equivalent to the cell capacitor voltage), and can be extended to different voltage levels. These confirm the H-bridge MMC is suitable for HVDC systems, medium voltage machine drives, off-shore wind farm interconnection, etc.

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Chapter 5. New control scheme for the H-bridge MMC with Fault Ride-through and System Recovery Capability

This chapter presents an control strategy that improves fundamental grid current control associated with the AC power control, cell capacitor ripple, and differential and common mode current harmonic components in the arms of the H-bridge MMC. This control scheme exploits the subtractive and additive switch states of the H-bridge MMC to maintain the capacitor voltage balance when converter DC link voltage collapses during DC faults. The significance of this control scheme is that it permits the H-bridge MMC to ride through a DC fault without the need for converter blocking to provide reactive and active power support to the AC grid, as has being presented in the literature. Furthermore, this chapter provides further MMC fundamental theory discussion, including logical and mathematical derivation of the relationships that governed its operation and modulation. The validity of the presented control scheme is confirmed using simulations and experimentation.

5.1 **Background**

In the last decade, large-scale offshore wind farms have been adopted by the countries around the North Sea as a mean to reduce CO_2 and greenhouse gas emissions. As a result, new VSC-HVDC transmission systems are being built to transmit these powers to the mainland AC grids. VSC-HVDC transmission links is now recognized by transmission system operators (TSOs) as the technology that can extend the dynamic rating of the ageing AC power networks, and resolve many issues in their heavily meshed power systems, such as loop power flow and congestion.

The trends towards smart grids and multi-terminal HVDC networks necessitate development of new breeds of reliable VSCs that are efficient and resilient to AC and DC network faults. Half and H-bridge MMCs can meet some of the necessary requirements. [1-11]. From a multi-terminal HVDC network prospective, converter topologies that can survive DC network faults with minimum impact on the AC side voltage and power system stability are most likely to be adopted. New breeds of VSCs that offer DC fault blocking capability are the H-bridge MMC, mixed cells MMC, three-level and five-level cells MMC, H-bridge alternative arm MMC, and the hybrid cascaded with AC and DC H-bridge cells converter [5, 12-18]. There are several factors that may influence the choice between these new breeds of VSCs such as, semiconductor losses, footprint, and management of the internal cell faults [4, 19-25]. Considering these tradeoffs, the mixed cell MMC (with 50% H-bridge and 50% half-bridge) [26], H-bridge alternative arm MMC [27], and three-level cells [28] and five-level MMC [29] offer DC fault blocking capability, with lower semiconductor losses than the H-bridge MMC [30-32]. However, this chapter identifies that the H-bridge MMC can ride through DC network faults with and without converter blocking. This chapter presents a new control scheme that explores the possibility of riding through DC faults, without the need for converter blocking and without exposing the converter switches to risk of damage. The importance of this control scheme is that it allows the converter to support the AC network during DC network faults instead of being a burden. Riding through a DC fault without converter blocking is made possible using a combination of the presented control scheme and full exploitation of the bi-polar capabilities of the H-bridge MMC cells. An illustrative version of the H-bridge MMC with two-cells per arm (single-phase) is

used in the simulation and experimentation to demonstrate the viability of the presented control scheme. The demonstrations consider normal operation and DC fault emulation. Additional simulations illustrate control scheme performance during typical DC faults. These simulations and experimental results will show that the control scheme is able to restrain the current stresses in converter arms during DC faults; hence, the risk of converter failure during a DC fault is significantly reduced.

5.2 Improved control system for normal operation and low DC voltage ride-through

The control scheme is first developed for a single phase H-bridge MMC, and then extended to the three-phase H-bridge MMC by regulating each phase independently. Based on the fundamental operational principle and voltage balancing strategy presented in Chapter 4, it was concluded that the references for the upper and lower arm voltages are:

$$m_1 = m_d - m_a = m_d - m\sin\omega t \tag{5.1}$$

$$m_2 = m_d + m_a = m_d + m\sin\omega t \tag{5.2}$$

where m is a fixed modulation index related to grid voltage amplitude (or fundamental of the converter terminal voltage). In the proposed control method, m_d is adjustable and is determined by the common mode current control loop while m_a is regulated by the differential mode current control loop, displayed in Figure 5-1. To demonstrate the control strategy of common and differential current control, the following derivations are presented.

Figure 5-2 illustrates a version of the single-phase H-bridge MMC connected to the grid, where R and L represent the interfacing inductance or series impedance of the interfacing transformer. Considering the converter ac side, the differential that describes the electromagnetic transient is:

$$\frac{di_o}{dt} = -R\diagup L\, i_o + \frac{v_o - v_g}{L} \tag{5.3}$$

For current control design, let $u = v_o - v_g$ where u is estimated from the proportional-integral controller by forcing the ac current converter exchanges with the grid, to follow a given reference:

$$u = \alpha_p(i_o^* - i_o) + \alpha_i \int (i_o^* - i_o)dt \tag{5.4}$$

where α_p and α_i represent the proportional and integral gains.

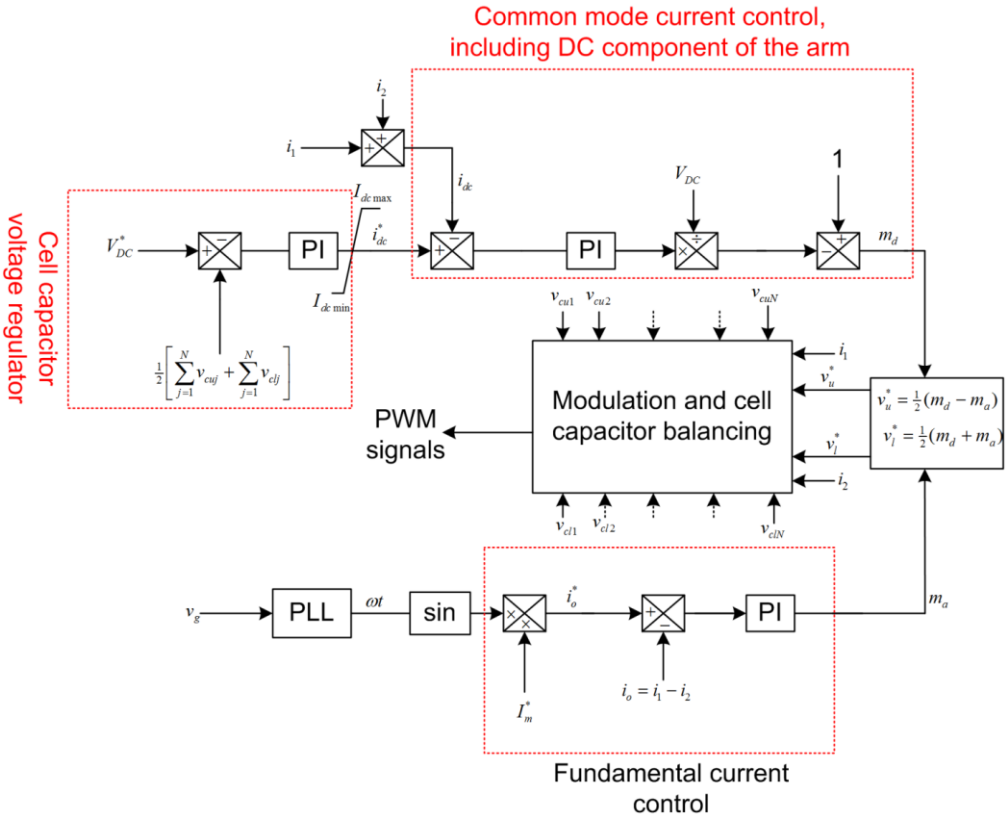


Figure 5-1 Control diagram for the DC and AC components of the arm voltage references

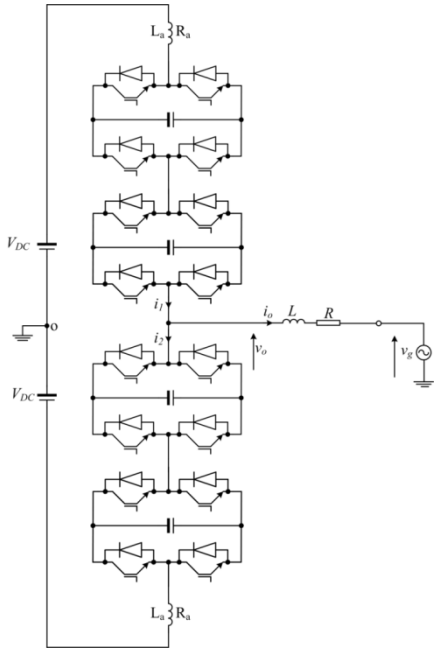


Figure 5-2. Schematic diagram illustrating grid connection of a single-phase H-Bridge MMC

To facilitate control design using state space, the integral part of (5.4) is replaced by an artificial control variables z, therefore $z = \int (i_o^* - i_o)dt$. Based on the definition of z, equation (5.3) and (5.4):

$$\frac{d}{dt}\begin{bmatrix} i_o \\ z \end{bmatrix} = \begin{bmatrix} -(R+\alpha_p)/L & 1/L \\ -\alpha_i & 0 \end{bmatrix}\begin{bmatrix} i_o \\ z \end{bmatrix} + \begin{bmatrix} \alpha_p/L \\ \alpha_i \end{bmatrix} i_o^* \tag{5.5}$$

After Laplace manipulation of (5.5):

$$\frac{i_o(s)}{i_o^*(s)} = \frac{\frac{\alpha_p}{L}s + \frac{\alpha_i}{L}}{s^2 + \frac{(\alpha_p + R)}{L}s + \frac{\alpha_i}{L}} \tag{5.6}$$

The current controller integral gains can be obtained by comparing the denominator of (5.6) to a standard second-order system. On this basis, $\alpha_p = 2\xi\omega_n L - R$ and $\alpha_i = \omega_n^2 L$, where the damping factor ξ and natural frequency ω_n are set according to the desired control objectives. For the given definition of *u* as well as the relationship between arm voltages (v_1, v_2) and the converter output voltage v_o displayed in equation (4.9) and (4.14), the ac component of the modulating signal of the upper and lower arm voltage references is: $m_a = V_o / \frac{1}{2}V_{DC}{}^* = (u + v_g) / \frac{1}{2}V_{DC}{}^*$, where $V_{DC}{}^*$ is the rated DC link voltage. During DC link collapse $V_{DC}{}^*$ is maintained at its original desired value. Thus the converter output current i_o is regulated by controlling the upper and lower arm voltages to synthesize the desired output voltage v_o. The resultant block diagram for the fundamental ac current controller is shown in Figure 5-1.

For design of the arm common mode current component, which is predominantly DC current, equation (4.12) is rewritten as:

$$\frac{di_{dc}}{dt} = -R_a/L_a\, i_{dc} + (V_{DC} - V_c)/L_a \tag{5.7}$$

where V_c represents the desired cell capacitor voltage of the upper and lower arms for a given power flow, obtained from a PI controller, by letting $u_d = V_{DC} - V_c$, with u_d defined as:

$$u_d = k_p(i_{dc}^* - i_{dc}) + k_i \int (i_{dc}^* - i_{dc})dt \tag{5.8}$$

After replacing the integral part of (5.8) by λ_d and manipulation of (5.7), the state space equation that can be used for selection of the DC current controller gains k_p and k_i, is:

$$\frac{d}{dt}\begin{bmatrix} i_{dc} \\ \lambda_d \end{bmatrix} = \begin{bmatrix} -(R_a + k_p)/L_a & 1/L_a \\ -k_i & 0 \end{bmatrix}\begin{bmatrix} i_{dc} \\ \lambda_d \end{bmatrix} + \begin{bmatrix} k_p/L_a \\ k_i \end{bmatrix} i_{dc}^* \tag{5.9}$$

The PI controller gains for the common mode current controller can be obtained by specifying a damping factor and natural frequency in similar manner as for the fundamental ac current controller. From the definition of the u_d, the DC component of the modulation index m_d is: $m_d = V_c/V_{DC} = (V_{DC} - u_d)/V_{DC} = 1 - u_d/V_{DC}$. The block diagram that summarizes the DC current controller of the MMC arms results.

The reference of the common mode current i_{dc}^* is obtained from the outer controller that regulates the sum of the cell capacitor voltages of the upper and lower arms. This controller is designed based on the differential equations that describe dynamics of the cell capacitor voltages of each arm as:

$$C\frac{dv_{c1}}{dt} = \tfrac{1}{2} i_1 (m_d - m_a) \tag{5.10}$$

$$C\frac{dv_{c2}}{dt} = \tfrac{1}{2} i_2 (m_d + m_a) \tag{5.11}$$

where C represents the equivalent cell capacitor per arm, and v_{c1} and v_{c2} represent the sum of the cell capacitor voltages of both arms.

Adding (5.10) and (5.11), gives:

$$C\frac{d}{dt}(v_{c1} + v_{c2}) = \tfrac{1}{2} m_d (i_1 + i_2) - \tfrac{1}{2} m_a (i_1 - i_2) \tag{5.12}$$

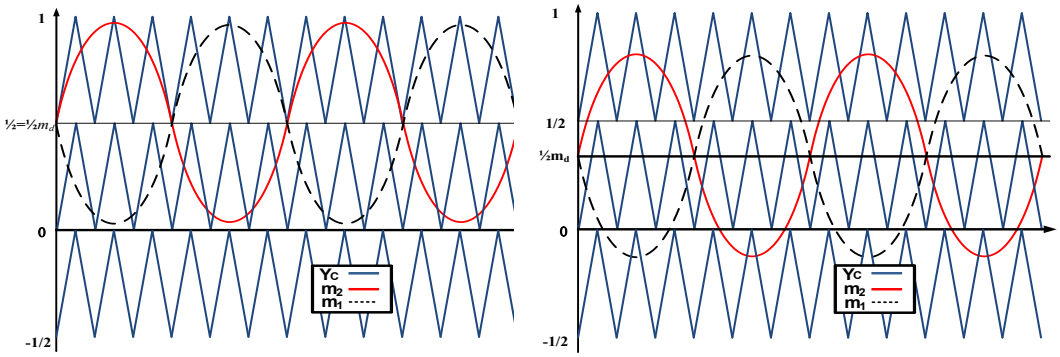
The terms $i_1 + i_2$ in equation (5.12) represents the common mode current that contains DC and 2nd harmonic currents in the MMC arms. For control design, the DC current reference i_{dc}^* is obtained from a PI controller as:

$$i_{dc}^* = \beta_p (V_{DC}^* - \tfrac{1}{2}(v_{c1} + v_{c2})) + \beta_i \int (V_{DC}^* - \tfrac{1}{2}(v_{c1} + v_{c2}))dt \tag{5.13}$$

where β_p and β_i represent the proportional and integral gains of equation (5.13). After replacing the integral part of (5.13) by Z_v, the closed state space that can be used for selection of the DC voltage controller gains is:

$$\frac{d}{dt}\begin{bmatrix}(v_{c1}+v_{c2})\\ Z_v\end{bmatrix}=\begin{bmatrix}-\frac{1}{2}\beta_p/C & 1/C\\ -\frac{1}{2}\beta_i & 0\end{bmatrix}\begin{bmatrix}(v_{c1}+v_{c2})\\ Z_v\end{bmatrix}+\begin{bmatrix}\beta_p/C\\ \beta_i\end{bmatrix}V_{DC}^{*} \tag{5.14}$$

The resultant block diagram in Figure 5-1 summarizes different MMC controllers. By exploiting the bi-polar capability of the H-bridge cells and the controller in Figure 5-1, the H-bridge MMC can operate reliably in steady state, and during AC and DC network faults. The significance of this control structure is that it allows the H-bridge MMC to ride through a DC fault without any uncontrolled inrush current from the AC side, and DC and AC currents in the converter upper and lower arms are controlled, even when the DC link collapses to zero. When the DC link voltage is suppressed to zero, as during a typical pole-to-pole DC short circuit fault, the active power the converter exchanges with the grid must be reduced to zero to avoid discharge of the cell capacitors. Both MMC arms continue to operate as a two parallel cascaded multilevel converter based STATCOM. This implies that converter blocking is no longer necessary; rather, during a DC fault, the MMC converter can operate to provide voltage support to the AC grid. Additionally, the presented control scheme in Figure 5-1 also suppressed the 2nd harmonic in the MMC arms, because by regulating the cell capacitor voltages, the DC voltage and common current controllers modulate the dc component of the modulation function m_d in manner that cancels the 2nd harmonics from the arm currents. Also, the control strategy facilitates active power exchange with the AC grid with a variable DC link voltage over a wide range (theoretically, from 0 to rated V_{DC}).



a) Normal operation b) Low DC voltage ride through operation

Figure 5-3. Carrier and reference waveforms for upper and lower arm voltages

Figure 5-3(a) shows the conventional PWM implementation for the MMC. Figure 5-3(b) displays the modifications introduced to implement PWM with sinusoidal references, which is used in conjunction with the control scheme in Figure 5-1. The DC component of the modulation index m_d is determined by the energy flow between the DC link and the cell capacitors. When the converter DC link voltage is suppressed, the DC component of the modulating function 'm_d' drops, causing the modulating signals of the upper and lower arms to become negative. This triggers the H-bridge switch states that insert cell capacitor voltages in the opposite or same direction as the converter DC link voltage ($½V_{DC}±vc_1$, $½V_{DC}±vc_2$, $½V_{DC}±vc_3$ and $½V_{DC}±vc_4$). In this manner, the converter AC output voltage magnitude can be maintained greater than the DC supply; thus preventing uncontrolled inrush current from the AC side to the DC side and allows the converter to inject active power to AC grid in a boost mode while the DC link voltage is suppressed.

5.3 DC power network post-fault recharging

The H-bridge MMC has the unique feature that it can reverse the cell voltage polarity; thus, power can flow to the AC side even though the DC link voltage is suppressed. This is achieved whilst maintaining cell capacitor voltage balancing, even during a DC side fault. Once the fault is cleared, the H-bridge cell capacitors remain charged and the cells can be modulated to control the recharge of the DC link capacitor from the AC side, without the use of AC side contactors and line resistors. By exploiting the redundant switch states available within the converter, controlled recharge of the DC link plus cable stray capacitance can be achieved while maintaining cell capacitor voltage balance.

From equation (5.3) and the fundamental current control loop shown in Figure 5-1, the grid current can be set by controlling the AC components of the upper and lower arm voltages. Thus determining the magnitude and direction of power flow between the DC side and the H-bridge MMC.

From equation (5.7), the power exchange between the DC link and the H-bridge MMC can be controlled by regulating the common mode current i_{dc}. It can be achieved by controlling the DC component m_d based on the equation (5.9). During the recharging period, the DC component of i_{dc} is set negative due to power transfer from the H-bridge MMC to the DC link. Thus the recharging strategy can be implemented by controlling the modulation indices to control the differential and

sum of the arm voltages. There are seven switch combinations for DC link capacitance recharging listed in Table 5-1, including the corresponding AC side voltage, where v_1 and v_2 represent the voltages of upper and lower arms respectively. Switch state 1 means that the switch is on, and 0 is for the off state.

Table 5-1 Switch states for DC link voltage recharging

charging voltage from converter AC terminal	S_{11}	S_{12}	S_{13}	S_{14}	S_{21}	S_{22}	S_{23}	S_{24}	S_{31}	S_{32}	S_{33}	S_{34}	S_{41}	S_{42}	S_{43}	S_{44}
v_o	1	1	0	0	1	1	0	0	1	0	0	1	1	0	0	1
	1	0	0	1	1	0	0	1	1	1	0	0	1	1	0	0
v_o+v_1	1	0	0	1	1	1	0	0	1	0	0	1	1	0	0	1
	1	1	0	0	1	0	0	1	1	0	0	1	1	0	0	1
$v_o - v_2$	1	0	0	1	1	0	0	1	1	0	0	1	1	1	0	0
	1	0	0	1	1	0	0	1	1	1	0	0	1	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

5.4 **Ripple components and energy storage analysis**

5.4.1 Ripple components

Based on Figure 4-1, equation (4.1) and equation (4.2), the single H-bridge cell and its switching function are used to derive the cell capacitor voltage ripple functions when the common mode and differential mode current control loops are incorporated. According to the analysis in section 4.2, for the i^{th} cell of an H-bridge MMC with n cells per arm, the switching states are:

$$K_i(t) = \begin{cases} 1, & when\ S_1\ and\ S_4\ is\ on, S_2\ and\ S_3\ is\ off \\ 0, & when\ S_1\ and\ S_2\ is\ on, S_3\ and\ S_4\ is\ off \\ 0, & when\ S_3\ and\ S_4\ is\ on, S_1\ and\ S_2\ is\ off \\ -1, & when\ S_2\ and\ S_3\ is\ on, S_1\ and\ S_4\ is\ off \end{cases} \tag{5.15}$$

where $K_i(t)$ determines the transient switching states of the i^{th} H-bridge cell. Then the transient current i_{si} through the i^{th} cell capacitor is:

$$i_{si} = K_i(t) \times i_{arm} \tag{5.16}$$

where i_{arm} represents the arm currents, if the H-bridge cell is in the upper arm, $i_{arm}= i_1$, else $i_{arm}= i_2$. The voltage ripple of the cell capacitor is:

$$v_{ci}^{k} = \frac{i_{si}^{k}}{jk\omega C} \tag{5.17}$$

where v_{ci}^{k} is the k^{th} harmonic component of the cell capacitor voltage, C is the capacitance of the cell capacitor, and ω is the fundamental angular frequency of the grid. By implementing the control scheme in Figure 5-1, the harmonic components of arm currents and common mode current are significantly suppressed. Then it can be assumed that both arm currents only consist of a DC component and a fundamental AC component. The harmonics of cell capacitor voltage are suppressed accordingly. Since the output current of H-bridge MMC is phase synchronized with grid voltage and tightly regulated to be sinusoidal, it can be expressed as $i_o = I_m \sin \omega t$. Substituting this into equation (4.20):

$$\begin{aligned} i_1 &= i_{dc} + \tfrac{1}{2} I_m \sin \omega t \\ i_2 &= i_{dc} - \tfrac{1}{2} I_m \sin \omega t \end{aligned} \tag{5.18}$$

To synthesize the both arm voltages, the switching function must follow the arm voltage references at any transient of the switching cycle, thus the switching function of each arm cells can be derived as:

$$\sum_{i=1}^{n} K_{1i}(t) = \frac{1}{2} n(m_d - m \sin \omega t) \tag{5.19}$$

$$\sum_{i=1}^{n} K_{2i}(t) = \frac{1}{2} n(m_d + m \sin \omega t) \tag{5.20}$$

where $K_{1i}(\mathrm{t})$ represents the switch states of the upper arm cell and $K_{2i}(\mathrm{t})$ represents the switch states of the lower arm cell. Dividing (5.20) by n, the average switch states of each H-bridge cell is:

$$K_{1av} = \frac{1}{2}(m_d - m \sin \omega t) \tag{5.21}$$

$$K_{2av} = \frac{1}{2}(m_d + m \sin \omega t) \tag{5.22}$$

K_{1av} and K_{2av} represent the average switch states of the upper and lower arm cells respectively. Different from the switch states of half-bridge cells, K_{1av} and K_{2av} of H-bridge cells consist of the adjustable common mode component m_d that is

generated by the common mode control loop in Figure 5-1. The value of m_d varies between -1 to 1, making K_{1av} and K_{2av} either positive or negative. This represents the unique bi-polarity feature of H-bridge cell which allows it to operate over the full DC link voltage range.

Substituting (5.21) and (5.18) into (5.16), the average current i_{1sav} through each cell capacitor of the upper arm is:

$$\begin{aligned} i_{1sav} &= \frac{1}{2}(i_{dc} + \frac{1}{2} I_m \sin \omega t)(m_d - m \sin \omega t) \\ &= \frac{1}{2} i_{dc} m_d - \frac{1}{8} I_m m + (\frac{1}{4} m_d I_m - \frac{1}{2} i_{dc} m) \sin \omega t + \frac{1}{8} I_m m \cos 2\omega t \end{aligned} \tag{5.23}$$

Substituting (5.22) and (5.18) into (5.16), the average current i_{2sav} through each cell capacitor of the lower arm is determined:

$$\begin{aligned} i_{2sav} &= \frac{1}{2}(i_{dc} - \frac{1}{2} I_m \sin \omega t)(m_d + m \sin \omega t) \\ &= \frac{1}{2} i_{dc} m_d - \frac{1}{8} I_m m + (\frac{1}{2} i_{dc} m - \frac{1}{4} m_d I_m) \sin \omega t + \frac{1}{8} I_m m \cos 2\omega t \end{aligned} \tag{5.24}$$

In steady state, assuming the converter is lossless and cell capacitor voltages are balanced, and the DC offset of each cell capacitor voltage is stabilized at the rated value; from equation (5.17), (5.23) and (5.24) the average voltage ripple of arm cell capacitors can be written:

$$v^1_{1cav} + v^2_{1cav} = (\frac{m_d I_m}{4\omega C} - \frac{i_{dc} m}{2\omega C}) \cos \omega t + \frac{I_m m}{16\omega C} \sin 2\omega t \tag{5.25}$$

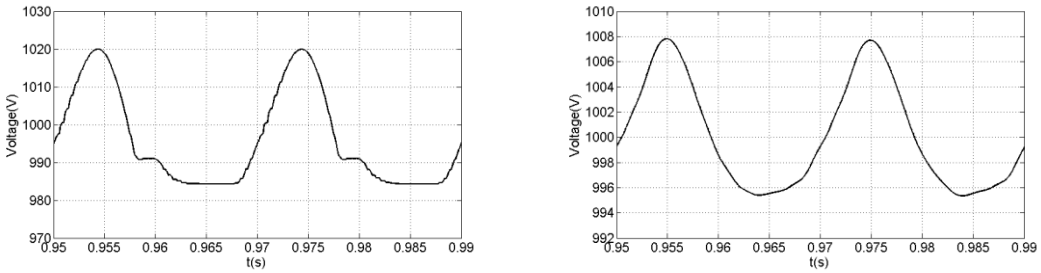
$$v^1_{2cav} + v^2_{2cav} = (\frac{i_{dc} m}{2\omega C} - \frac{m_d I_m}{4\omega C}) \cos \omega t + \frac{I_m m}{16\omega C} \sin 2\omega t \tag{5.26}$$

where v^1_{1cav} and v^2_{1cav} donate the average fundamental and second order harmonic components of upper arm cells, v^1_{2cav} and v^2_{2cav} are the average fundamental and second order harmonic components of lower arm cells. If the cell capacitor parameters are identical and the characteristics of switching devices are similar, the voltage ripple of each upper arm cell capacitor is equivalent to the average ripple components of the upper arm in equation (5.25) and the voltage ripple of each lower arm cell capacitor is equivalent to the average ripple components of the lower arm in equation (5.26). Therefore, the upper and lower arm cell capacitor voltages are:

$$v_{1c} = \frac{V_c}{n} + (\frac{m_d I_m}{4\omega C} - \frac{i_{dc} m}{2\omega C})\cos\omega t + \frac{I_m m}{16\omega C}\sin 2\omega t \tag{5.27}$$

$$v_{2c} = \frac{V_c}{n} + (\frac{i_{dc} m}{2\omega C} - \frac{m_d I_m}{4\omega C})\cos\omega t + \frac{I_m m}{16\omega C}\sin 2\omega t \tag{5.28}$$

where V_c represents the sum of the desired cell capacitor voltages of the upper and lower arms described in (5.7), v_{1c} and v_{2c} are cell capacitor voltages of upper and lower arm. Equations (5.27) and (5.28) demonstrate that the fundamental harmonic components of the capacitor voltages can be suppressed by adjusting the DC component m_d of the upper and lower arm voltage references and the harmonics of higher than second-order are reduced. Thus by utilising the differential and common mode current control scheme in Figure 5-1, the capacitor voltage ripple components are suppressed compared with that without the control scheme illustrated in Figure 5-4. This may facilitate reduced capacitor sizing and the reduction of converter cost.



a) Voltage of upper arm capacitor without the control scheme in Figure 5-1

b) Voltage of upper arm capacitor with the control scheme in Figure 5-1

Figure 5-4. Voltage waveforms across upper arm capacitor of a five-level H-bridge MMC in a grid-connected mode

5.4.2 Energy storage analysis

For each cell capacitor, the energy stored in any transient can be estimated by using the cell capacitor voltages calculated in equations (5.27) and (5.28). Each energy is:

$$e_{1cell} = \tfrac{1}{2} C v_{1c}^2 \tag{5.29}$$

$$e_{2cell} = \tfrac{1}{2} C v_{2c}^2 \tag{5.30}$$

where e_{1cell} and e_{2cell} donates the energy storage in each upper arm cell and lower arm cell respectively. As the DC offset of each cell capacitor voltage is considered stabilized at the rated value, the energy that is related to the DC offset of each cell capacitor voltage is:

$$E_{cell} = \tfrac{1}{2} C \left(\frac{V_c}{n} \right)^2 \tag{5.31}$$

Thus e_{1cell} and e_{2cell} become:

$$e_{1cell} = E_{cell} + \Delta e_{1cell} \tag{5.32}$$

$$e_{2cell} = E_{cell} + \Delta e_{2cell} \tag{5.33}$$

E_{cell} donates the constant component of the energy stored in each cell capacitor while Δe_{1cell} and Δe_{2cell} donate the energy variation of each cell capacitor in the upper arm and lower arm. For an H-bridge MMC with *n* cells per arm, the constant component of the energy storage of each arm can be derived from equation (5.31):

$$E_m = \tfrac{1}{2} nC\left(\frac{V_c}{n}\right)^2 \tag{5.34}$$

The transient energy of each arm is:

$$e_{1a} = \tfrac{1}{2} nCv_{1c}^2 = E_m + \Delta e_{1a} \tag{5.35}$$

$$e_{2a} = \tfrac{1}{2} nCv_{2c}^2 = E_m + \Delta e_{2a} \tag{5.36}$$

e_{1a} and e_{2a} donate the energy stored in the upper arm and lower arm, while Δe_{1a} and Δe_{2a} donate the energy variations in the upper and lower arm respectively. From (5.35) and (5.36), the maximum energy stored in each arm is determined by the peak of the cell capacitor voltages of the upper and lower arms while the maximum energy variation is also reached at this value.

In order to estimate the peak value of the cell capacitor voltage, equations (5.27) and (5.28) are differentiated:

$$v_{1c}^{'}(\omega t) = \left(\frac{i_{dc}m}{2\omega C} - \frac{m_d I_m}{4\omega C}\right)\sin\omega t + \frac{I_m m}{8\omega C}\cos 2\omega t \tag{5.37}$$

$$v_{2c}^{'}(\omega t) = \left(\frac{m_d I_m}{4\omega C} - \frac{i_{dc}m}{2\omega C}\right)\sin\omega t + \frac{I_m m}{8\omega C}\cos 2\omega t \tag{5.38}$$

Defining $A = \frac{i_{dc}m}{2\omega C} - \frac{m_d I_m}{4\omega C}$ and $B = \frac{I_m m}{8\omega C}$, then equations (5.37) and (5.38) simplify to:

$$\begin{aligned} v_{1c}^{'}(\omega t) &= A\sin\omega t + B\cos 2\omega t = A\sin\omega t + B - 2B\sin^2\omega t \\ v_{2c}^{'}(\omega t) &= -A\sin\omega t + B\cos 2\omega t = -A\sin\omega t + B - 2B\sin^2\omega t \end{aligned} \tag{5.39}$$

The extreme voltages of the upper and lower cell capacitor voltages are:

$$\sin\omega t_{1u} = \frac{A+\sqrt{A^2+8B^2}}{4B}, \quad \sin\omega t_{2u} = \frac{A-\sqrt{A^2+8B^2}}{4B}$$
$$\sin\omega t_{1l} = \frac{-A+\sqrt{A^2+8B^2}}{4B}, \quad \sin\omega t_{2l} = \frac{-A-\sqrt{A^2+8B^2}}{4B} \tag{5.40}$$

where t_{1u} and t_{2u} are the extreme voltages of the upper arm capacitor voltages, t_{1l} and t_{2l} are the extreme voltage of the lower arm capacitor voltages. For each upper arm cell capacitor voltage, in the region $-1 < \sin\omega t < \frac{A-\sqrt{A^2+8B^2}}{4B}$ and $\frac{A+\sqrt{A^2+8B^2}}{4B} < \sin\omega t < 1$, the value of v_{1c} is monotonically decreasing, while for $\frac{A-\sqrt{A^2+8B^2}}{4B} < \sin\omega t < \frac{A+\sqrt{A^2+8B^2}}{4B}$, the value of v_{1c} is monotonically increasing. Thus the peak value of v_{1c} is obtained at the extreme when $\sin\omega t_{1u} = \frac{A+\sqrt{A^2+8B^2}}{4B}$. Similarly the peak value of v_{2c} is obtained at the extreme value $\sin\omega t_{1l} = \frac{-A+\sqrt{A^2+8B^2}}{4B}$. They can be described as:

$$v_{1c\max} = \frac{V_c}{n} - A\cos\omega t_{1u} + 2B\sin 2\omega t_{1u}$$
$$v_{2c\max} = \frac{V_c}{n} + A\cos\omega t_{1l} + 2B\sin 2\omega t_{1l} \tag{5.41}$$

Substituting (5.41) into equations (5.35) and (5.36), the maximum energy variation of the upper and lower arms is:

$$\begin{aligned}\Delta e_{1a\max} &= \frac{1}{2}nCA^2\cos^2\omega t_{1u} + 2nCB^2\sin^2 2\omega t_{1u} + 2CBV_c\sin 2\omega t_{1u} \\ &\quad - 2nCAB\sin 2\omega t_{1u}\cos\omega t_{1u} - ACV_c\cos\omega t_{1u} \\ \Delta e_{2a\max} &= \frac{1}{2}nCA^2\cos^2\omega t_{1l} + 2nCB^2\sin^2 2\omega t_{1l} + 2CBV_c\sin 2\omega t_{1l} \\ &\quad + 2nCAB\sin 2\omega t_{1l}\cos\omega t_{1l} + ACV_c\cos\omega t_{1l}\end{aligned} \tag{5.42}$$

The energy variation is equivalent to the integral of the transient power flow in each arm. From (5.1) and (5.2), the upper and lower arm voltages are:

$$v_1 = \tfrac{1}{2}V_c(m_d - m\sin\omega t)$$
$$v_2 = \tfrac{1}{2}V_c(m_d + m\sin\omega t) \tag{5.43}$$

Multiply equation (5.18) by (5.43), the power flows of upper and lower arms are:

$$P_1 = \frac{1}{2}V_c[m_d i_{dc} + (\frac{1}{2}I_m m_d - i_{dc} m)\sin\omega t - \frac{1}{2}I_m m\sin^2\omega t]$$
$$P_2 = \frac{1}{2}V_c[m_d i_{dc} + (i_{dc} m - \frac{1}{2}I_m m_d)\sin\omega t - \frac{1}{2}I_m m\sin^2\omega t] \quad (5.44)$$

where P_1 and P_2 represent the upper and lower arm transient power flows. If the H-bridge MMC is lossless, the input power from DC link to the converter is equivalent to the output power from the converter to the grid in steady state. The DC terminal voltage of the H-bridge MMC is equal to the sum of the upper and lower arm voltages, then the equation of input and output power of the converter is:

$$P_{in} = (v_1 + v_2)i_{dc} = V_c m_d i_{dc} = \frac{1}{4}V_c m I_m = P_{out} \quad (5.45)$$

From equation (5.45):

$$m_d i_{dc} = ¼ m I_m \quad (5.46)$$

Substituting (5.46) into (5.44):

$$P_1 = \frac{1}{2}V_c[(\frac{1}{2}I_m m_d - i_{dc} m)\sin\omega t + \frac{1}{4}I_m m\cos 2\omega t]$$
$$P_2 = \frac{1}{2}V_c[(i_{dc} m - \frac{1}{2}I_m m_d)\sin\omega t + \frac{1}{4}I_m m\cos 2\omega t] \quad (5.47)$$

Integrating (5.47), the energy variation is:

$$\Delta e_{1a} = \frac{V_c}{2\omega}[(i_{dc} m - \frac{1}{2}I_m m_d)\cos\omega t + \frac{1}{8}I_m m\sin 2\omega t]$$
$$\Delta e_{2a} = \frac{V_c}{2\omega}[(\frac{1}{2}I_m m_d - i_{dc} m)\cos\omega t + \frac{1}{8}I_m m\sin 2\omega t] \quad (5.48)$$

From equation (5.48), the energy variation of the upper and lower arms can be calculated by the system power ratings, rated cell capacitor voltage values, DC link voltage, and the grid voltage, regardless of the cell capacitance. Based on equation (5.42) and the previous analysis, the maximum energy variation is attained when $t=t_{1u}$ for the upper arm and $t=t_{1l}$ for the lower arm. Substituting (5.48) into (5.42):

$$\frac{V_c}{2\omega}[(i_{dc} m - \frac{1}{2}I_m m_d)\cos\omega t_{1u} + \frac{1}{8}I_m m\sin 2\omega t_{1u}] = \begin{bmatrix} \frac{1}{2}nCA^2\cos^2\omega t_{1u} + 2nCB^2\sin^2 2\omega t_{1u} \\ +2CBV_c\sin 2\omega t_{1u} - 2nCAB\sin 2\omega t_{1u}\cos\omega t_{1u} \\ -ACV_c\cos\omega t_{1u} \end{bmatrix}$$
$$\frac{V_c}{2\omega}[(\frac{1}{2}I_m m_d - i_{dc} m)\cos\omega t_{1l} + \frac{1}{8}I_m m\sin 2\omega t_{1l}] = \begin{bmatrix} \frac{1}{2}nCA^2\cos^2\omega t_{1l} + 2nCB^2\sin^2 2\omega t_{1l} \\ +2CBV_c\sin 2\omega t_{1l} + 2nCAB\sin 2\omega t_{1l}\cos\omega t_{1l} \\ +ACV_c\cos\omega t_{1l} \end{bmatrix} \quad (5.49)$$

Since $A = \frac{i_{dc} m}{2\omega C} - \frac{m_d I_m}{4\omega C}$ and $B = \frac{I_m m}{8\omega C}$, as defined in (5.39), substitution into (5.49), the minimum capacitance of each cell capacitor can be calculated. The size and cost of the converter is restricted by the capacitance and energy capability of cell capacitors while the maximum energy variation of each arm is not related to the number of cells per arm. Thus the converter overall sizing and cost is limited to some extend, regardless of the number of cells per arm.

5.5 **Simulation**

This section presents Simulink simulations for the H-bridge MMC as an off-grid inverter and a grid connected inverter. The power circuit is constructed using power electronics building blocks from the Simpower System library, and the control system depicted in Figure 5-1. The modulator block in Figure 5-1 employs sinusoidal PWM with phase disposition carriers, and a cell capacitor voltage balancing scheme that relies on cell rotation based on cell capacitor voltage magnitudes, arm current polarities and the voltage level to be synthesized. A controlled voltage source is utilised to simulate the DC link under the conditions including normal operation, permanent DC link fault, temporary DC fault and active power injection by adjusting the DC voltage value.

The objective is to validate the performance of the presented control strategy during normal operation and DC link voltage collapse. Table 5-2 summarises the converter parameters used for the medium voltage demonstration in this chapter (simulation). However, the presented control scheme remains valid for HVDC applications.

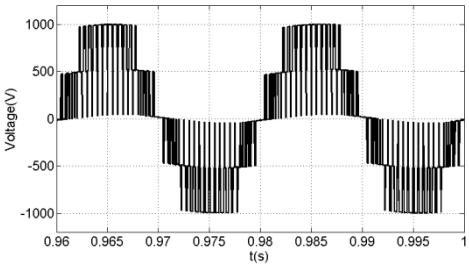
Table 5-2: Simulation parameter values

Converter rating	40kW
Modulation indices	0.8 and 0.9
Capacitance	4.7mF
Switching frequency	2.1kHz
DC link voltage	2kV
Arm inductance	3.3mH
Rated frequency	50Hz
Grid voltage $V_{gp\text{-}p}$	850V

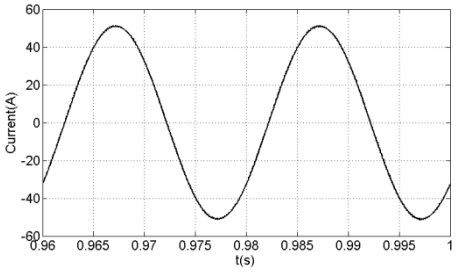
5.5.1 Five-level H-bridge MMC

I. Normal operation of off-grid condition

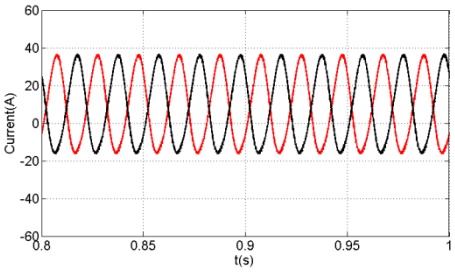
Figure 5-5 shows the simulation results when the five-level H-bridge MMC operates at 0.9 modulation index and 0.8 power factor lagging. Figure 5-5(a) and (b) show the converter terminal voltage relative to the midpoint and output current. The upper and lower arm currents and the expanded version in Figure 5-5(c) and (d) demonstrate that the harmonic components are almost eliminated. Figure 5-5(e) and (f) display that the common mode current magnitude and ripple are greatly suppressed by the control scheme. The ripple components of the cell capacitor voltages are decreased while the capacitor voltages remain balanced. Compared with the simulation waveforms without utilising the control strategy in Figure 4-13(c), (d) and (e), the quality of the arm currents and common mode current have been significantly improve which results in the suppression of cell capacitor voltage ripple.



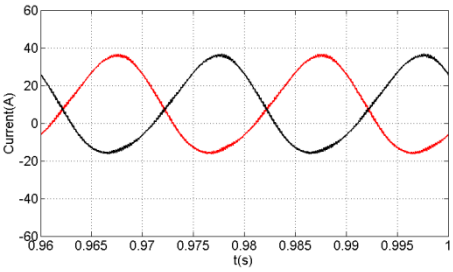
a) Converter terminal voltage



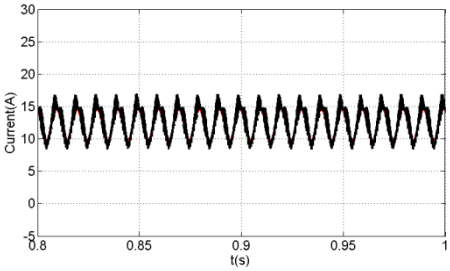
b) Inverter output current



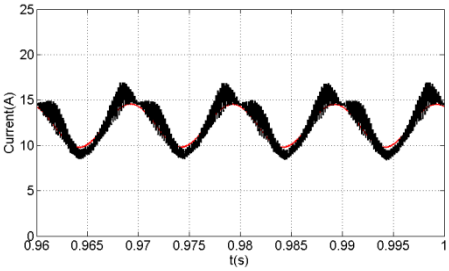
c) Upper and lower arm currents



d) The expanded version of upper and lower arm currents

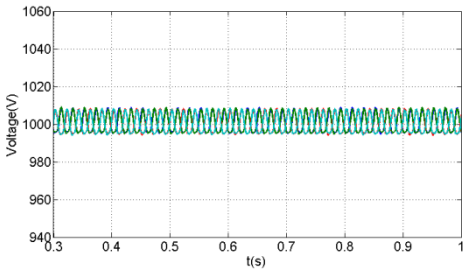


e) Common mode current (i_{dc}=½(i_1+i_2))and and its reference sets

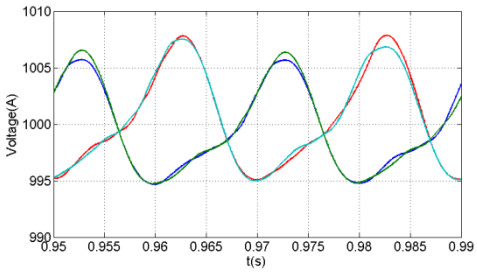


f) The expanded version of common mode current (i_{dc}=½(i_1+i_2))

by the DC voltage regulator that controls cell capacitor voltage of the upper and lower arms



g) Cell capacitor voltage of the upper and lower arms

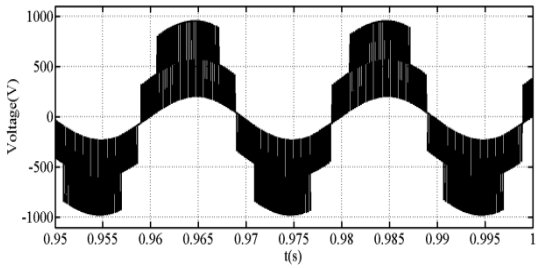


h) The expanded version of cell capacitor voltage of the upper and lower arms

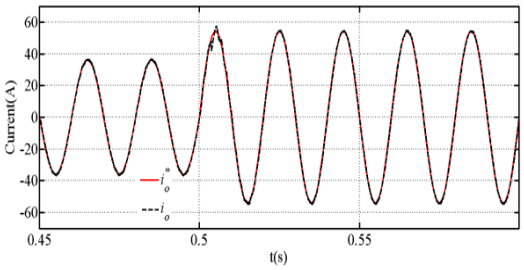
Figure 5-5. Simulation waveforms when the five-level H-bridge MMC is operated at 0.9 modulation index and 0.8 power factor lagging.

II. Normal operation of grid connection

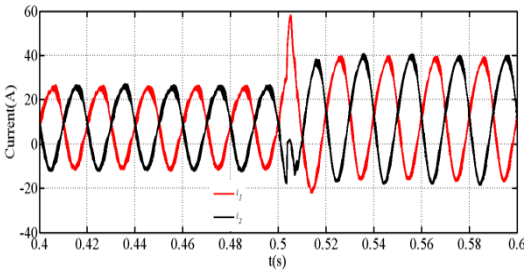
Figure 5-6 shows simulation results when the initial peak current the H-bridge MMC injects into grid is 36A and is increased to 54A at t=0.5s. Figure 5-6(a) shows the converter terminal voltage. Figure 5-6(b) shows the output current i_o superimposed over its reference i_o^* when the inverter operates at unity power factor, as illustrated in the block diagram in Figure 5-1. The plot for the upper and lower arm currents in Figure 5-6(c) shows the 2nd harmonic current component in both arms is significantly suppressed, as previously explained. The common mode current plot in Figure 5-6(d) shows that the presented control scheme significantly improves the dynamic response of the dc power flow. The fast dynamic response of the common mode current shown in Figure 5-6(d) reduces transient over-voltages observed on the DC side as a result of temporary power imbalance between AC and DC powers during drastic action, such as an immediate reduction of the AC side power as normally required during AC network faults. Figure 5-6(e) shows the cell capacitor voltages are regulated around their desired set-point, including when the step change is applied to the output current. Compared with the grid-connected simulation waveforms, without the control strategy in Figure 4-15(d), (e) and (f), the arm currents and common mode current quality have been improved while the cell capacitor voltages are balanced and the ripple components are suppressed. Based on these results it can be concluded that the presented control scheme is suitable for a wide range of applications, as it has a much faster dynamic response than with traditional approaches.



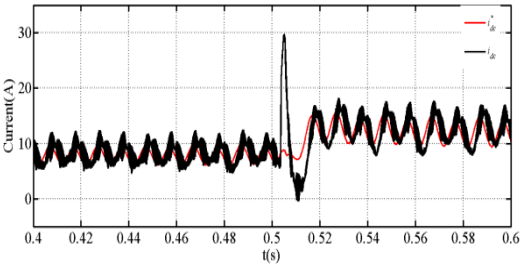
a) Converter terminal voltage relative to supply mid-point



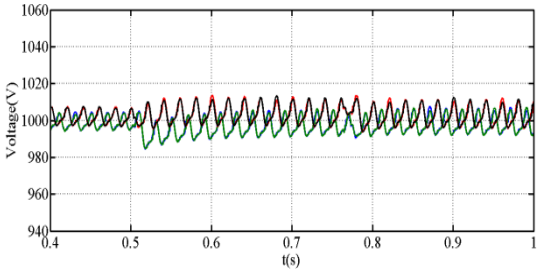
b) Current waveform converter injects into grid and its reference zoomed around the instant where step change is applied to the peak of the reference current



c) Upper and lower arm currents zoomed around the instant where step change is applied to the peak of the reference output current



d) Common mode current (i_{dc}=½(i_1+i_2))and and its reference sets by the DC voltage regulator that controls cell capacitor voltage of the upper and lower arms



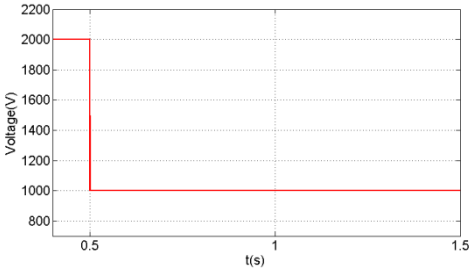
e) Cell capacitor voltage of the upper and lower arms

Figure 5-6. Selected simulation waveforms when illustrative version of the single-phase H-bridge MMC is controlled with the control scheme in Figure 5-1, and at t=0.5s a step change is applied that increases the output peak reference current from I_m=36A to 54A.

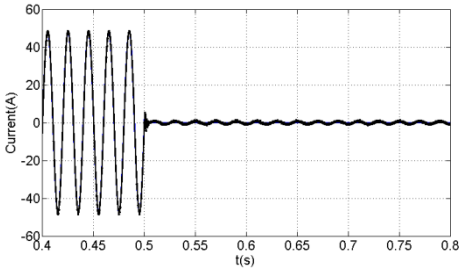
III. DC voltage suppression test (DC fault emulation)

This subsection simulates converter behaviour during a DC fault by reducing its DC link voltage to different values below its rated voltage when the peak of the grid AC voltage remains at 850V. Simulation results from this test are displayed in Figure 5-7 and Figure 5-8 when the converter output current (output active power) is reduced to zero, the control scheme in Figure 5-1 forces the converter arm currents and the common mode current (dc plus harmonics) to zero even when the DC link voltage is suppressed, see Figure 5-8 and Figure 5-7(a), (b), (c) and (d). Thus the entire

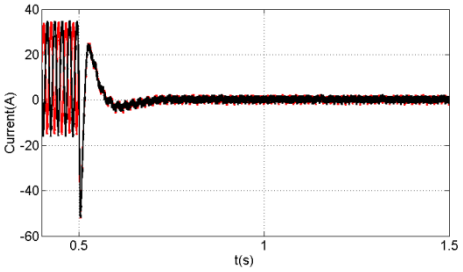
converter P-Q envelope can be used to provide reactive power support to the AC grid. Figure 5-8 and Figure 5-7(e) show the cell capacitor voltages are maintained at the pre-fault level despite the DC link voltage being suppressed to less than the AC voltage peak. This example shows that the control scheme in Figure 5-1 avoids the need for converter blocking in such cases, provided the bi-polar capability of the H-bridge MMC cells is utilized.



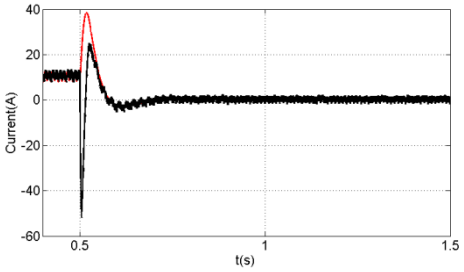
a) DC link voltage



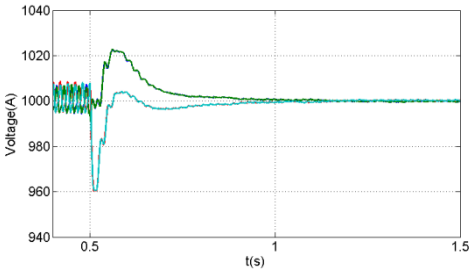
b) Inverter output current



c) Upper and lower arm currents

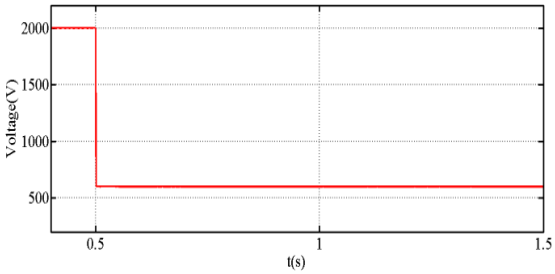


d) Common mode current

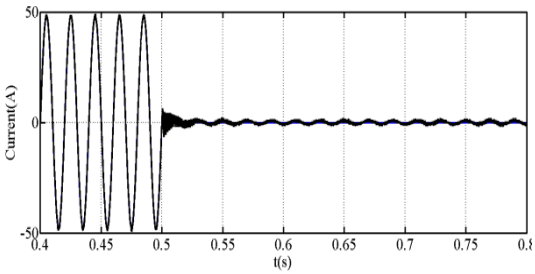


e) Cell capacitor voltages

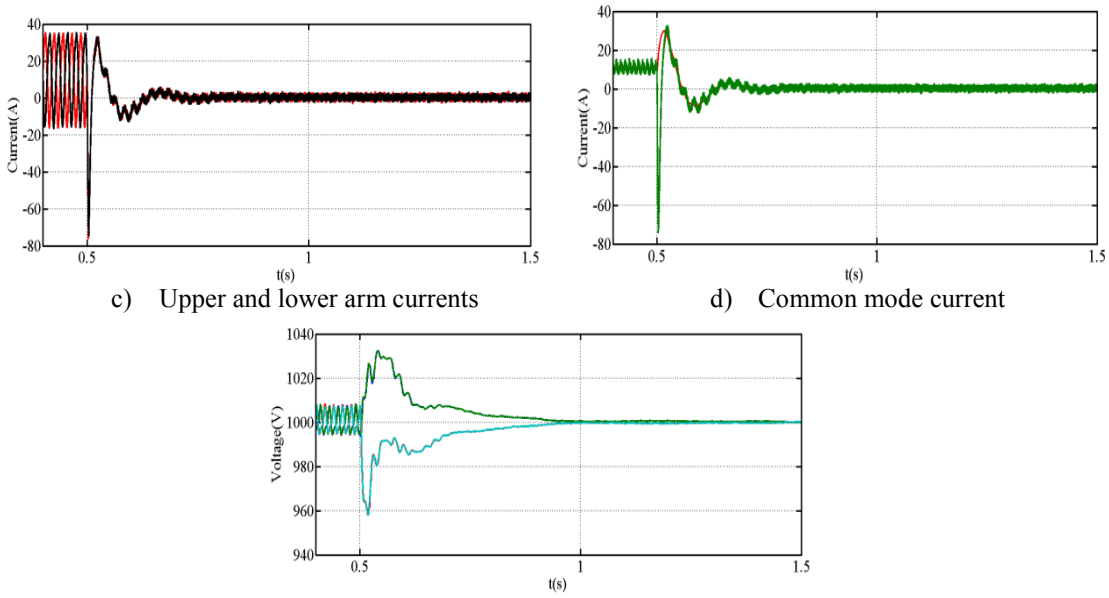
Figure 5-7. Simulation waveforms showing the improved behaviour of the H-bridge MMC during a DC fault (DC link voltage collapsed to 50% of rated value) when adopting the control scheme in Figure 5-1



a) DC link voltage



b) Inverter output current



c) Upper and lower arm currents

d) Common mode current

e) Cell capacitor voltages

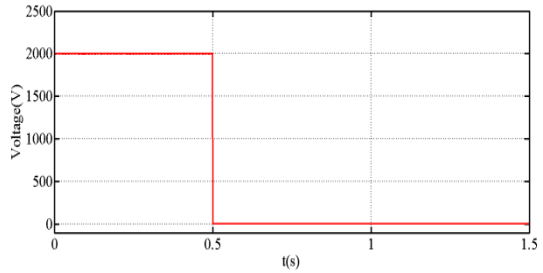
Figure 5-8. Simulation waveforms showing the improved behaviour of the H-bridge MMC during a DC fault (DC link voltage collapsed to 30% of rated value) when adopting the control scheme in Figure 5-1

IV. Typical cases of DC fault emulation

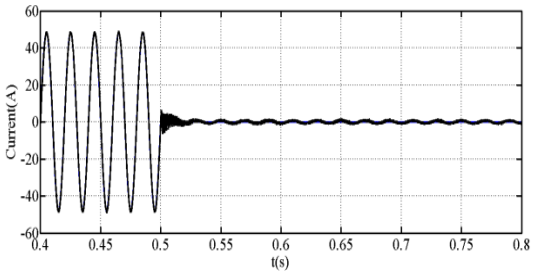
This section demonstrates the control scheme restraining a rapid rise of AC and DC currents in the converter arms and in-feed inrush AC current from the grid, when converter DC link voltage is suppressed, as during a DC fault. This reduces the risk of device failure, without the need for converter blocking, as advocated in [8, 15, 33-35]. A permanent DC short circuit fault is applied at the DC terminals of the H-bridge MMC being studied at t=0.5s, and the reference current the converter injects into the AC grid is reduced to zero immediately after DC fault is applied and remains zero during the fault period.

Figure 5-9 (a) and (b) show converter DC link voltage and AC output current during a permanent pole-to-pole DC short circuit fault. Although the converter DC link voltage drops to zero, uncontrolled AC inrush current from the AC grid is avoided because of the control scheme in Figure 5-1. This is because the H-bridge MMC reverses the polarities of its cell capacitors in order to present a virtual DC link voltage equal to pre-fault condition, which is higher than the rectified DC voltage peak; thus the converter remains controllable as the relationship between its DC link, modulation index, and AC voltage remain intact. Figure 5-9 (c) and (d) show that despite the permanent collapse of the DC link voltage, arm currents and the

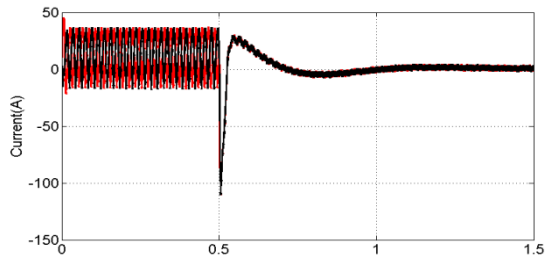
converter's common mode remain controlled. There is zero fundamental current from the AC grid and the common mode current is fully controlled by the DC loops that regulate cell capacitor voltages and the common mode current. Figure 5-9 (e) shows that cell capacitor voltage balance is maintained even when the DC link voltage is zero.



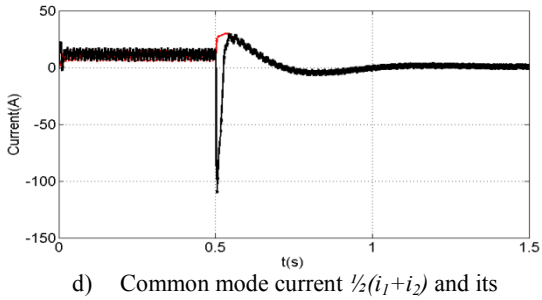
a) DC voltage across converter terminals



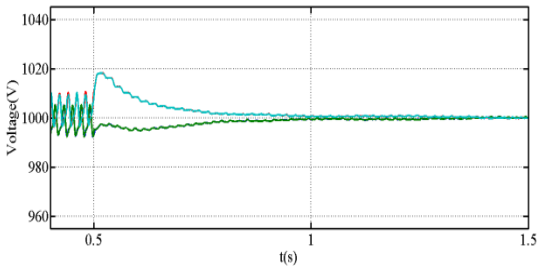
b) Current waveform converter injects into AC grid



c) Upper and lower arm currents



d) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator



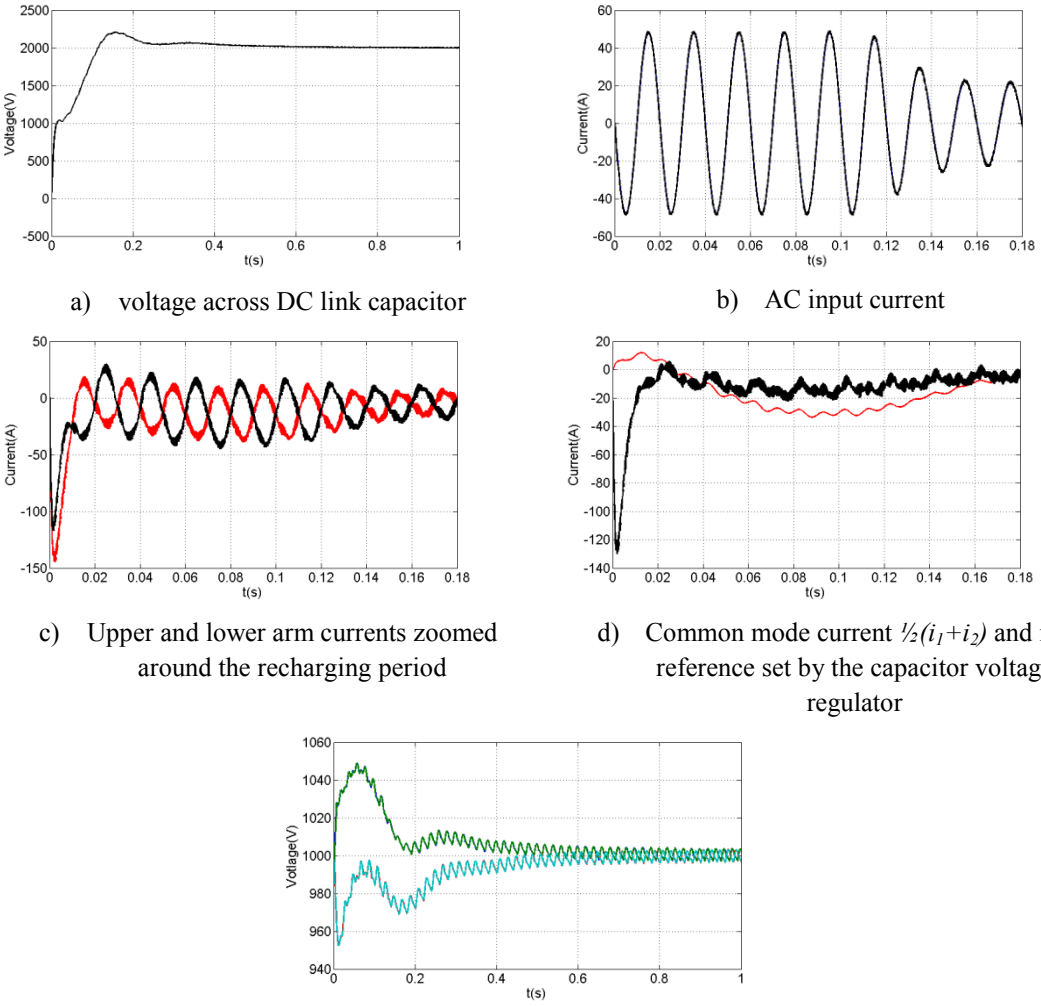
e) Cell capacitor voltages

Figure 5-9. Waveforms illustrate the effectiveness of the control scheme during a permanent pole-to-pole DC short circuit fault, in restraining AC and DC currents in the converter upper and lower arms, and elimination of the uncontrolled in-feed current from the grid, without converter blocking

V. DC network Post-fault Recharging

As illustrated in Figure 5-7, Figure 5-8 and Figure 5-9(e), the cell capacitor voltages are constrained at the rated value during a DC link fault. Thus when the DC fault is cleared, the DC link can be recharged from the AC side, without any external circuitry, by implementing the recharging strategy presented in section 0. Figure 5-10(a) and (b) show successful recharging of the H-bridge MMC DC voltage from 0

to V_{DC}, with sinusoidal AC side input currents and controlled DC charging current as demonstrated in Figure 5-10(c) and (d). Figure 5-10(e) shows that the voltages across the cell capacitors are maintained at the desired level at the end of the charging period. When the DC link voltage is fully charged, the dc link current reduces to the sum of the arm current DC components. At this stage the converter operating mode can be switch to the normal operating mode. Based on these results, it can be concluded that the presented charging scheme may facilitate post-fault DC grid restoration.



a) voltage across DC link capacitor

b) AC input current

c) Upper and lower arm currents zoomed around the recharging period

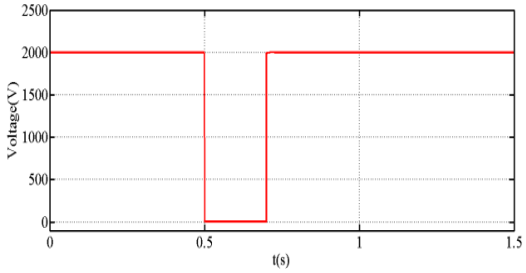
d) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator

e) Cell capacitor voltages

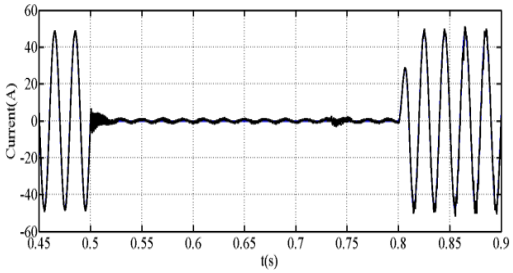
Figure 5-10. Waveforms illustrate the recharging of the DC network from the AC grid without external circuitry while the inrush current and common mode current are regulated

VI. Temporary DC fault emulation with instantaneous DC link voltage recovery

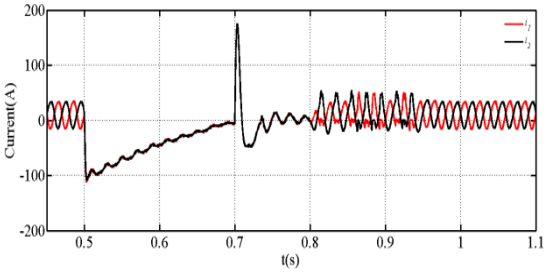
For further demonstration, the case of temporary DC fault is considered where the DC fault is applied at t=0.5s, and cleared at t=0.7s. When the temporary fault is cleared, the DC link rated voltage is re-established instantaneously. Converter output power (peak fundamental of the output AC current) is reduced to zero at t=0.5s and restored to the pre-fault value at t=0.8s. The results for the temporary DC short circuit fault are displayed in Figure 5-11. The waveforms presented are in line with the previous case that considered a permanent DC fault, except the system recovers quickly to operate normally when the fault is cleared, with current and voltage stresses in the converter devices are controlled.



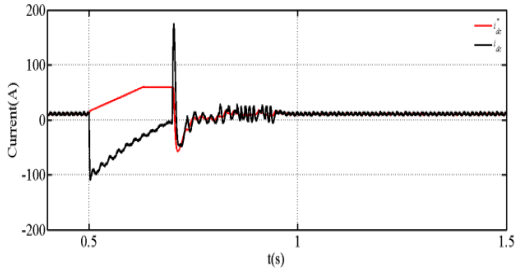
(b) DC voltage across converter terminals



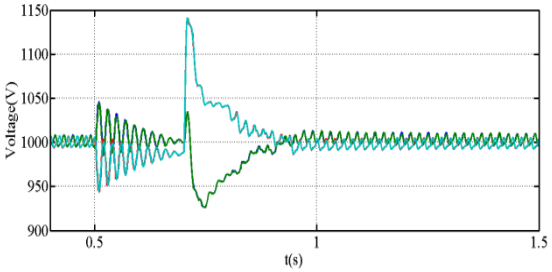
(c) Snapshot of the inverter output AC current zoomed around the instants where DC link is suppressed as a result of temporary DC short circuit fault



(d) Upper and lower arm currents zoomed around the DC fault period



(e) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator

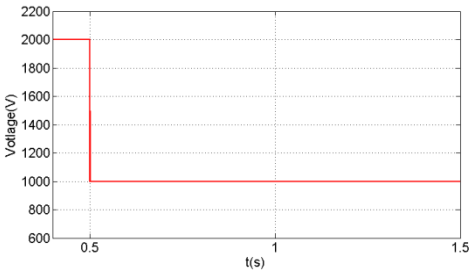


(f) Cell capacitor voltages

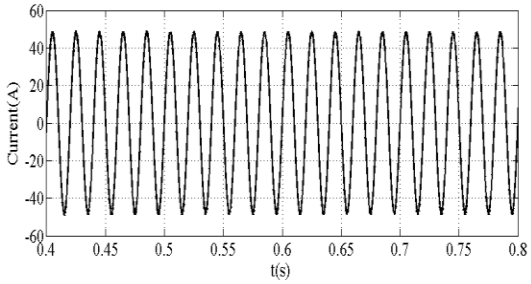
Figure 5-11. Waveforms illustrating the effectiveness of the control scheme during a temporary DC short circuit fault in restraining AC and DC currents in the converter upper and lower arms, and the elimination of the uncontrolled in-feed current from the grid, without converter blocking

VII. Active power injection into the AC grid when the H-bridge MMC operates in a boost mode during DC voltage sag

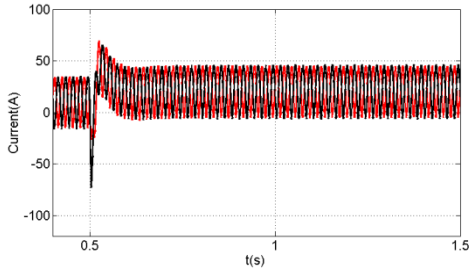
As displayed in Figure 5-12 and Figure 5-13, the converter DC link voltage is reduced to 50% and 30% of its rating, while the peak of the grid AC voltage remains at 850V. The MMC peak output current is set to the normal operation level (54A). Figure 5-12 and Figure 5-13(b) show the output AC current is maintained sinusoidal and phase locked. Figure 5-12 and Figure 5-13 (c) and (d) display that the magnitude of the arm currents and common mode current are controlled by the strategy. The capacitor voltages are balanced in Figure 5-12 and Figure 5-13 (e).



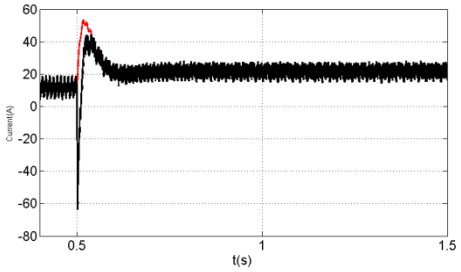
a) DC link voltage



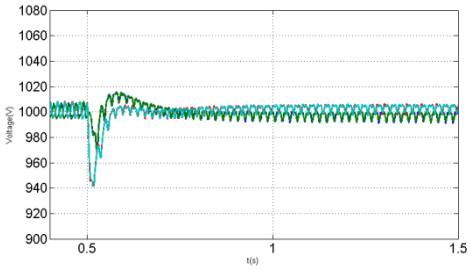
b) Inverter output current



c) Upper and lower arm currents

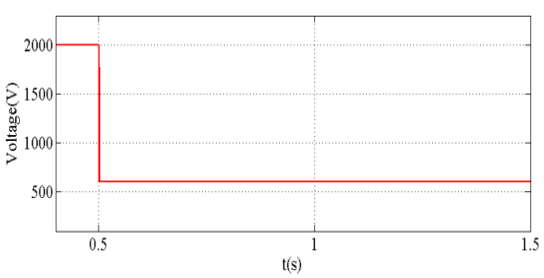


d) Common mode current $\frac{1}{2}(i_1+i_2)$ and its reference set by the capacitor voltage regulator

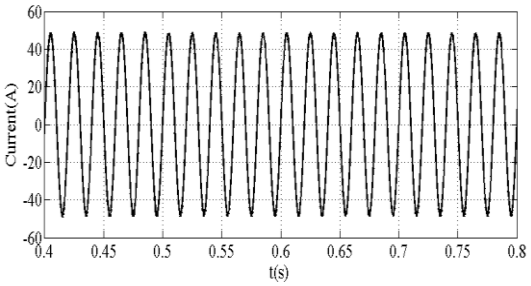


e) Cell capacitor voltages

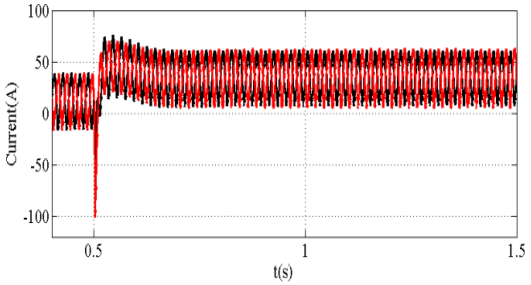
Figure 5-12. Simulation waveforms when the DC link voltage is reduced by 50% when peak grid voltage is 850V and the grid current is maintained stable



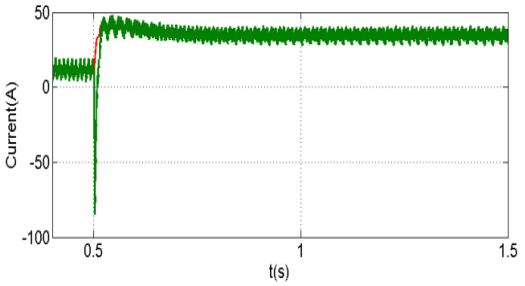
a) DC link voltage



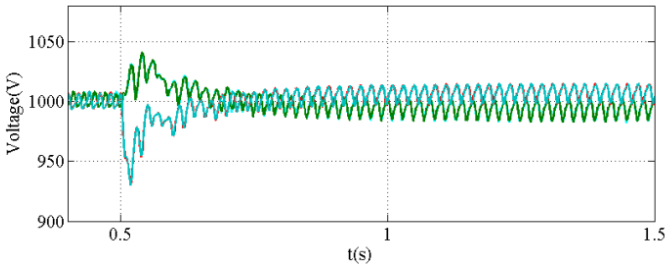
b) Inverter output current



c) Upper and lower arm currents



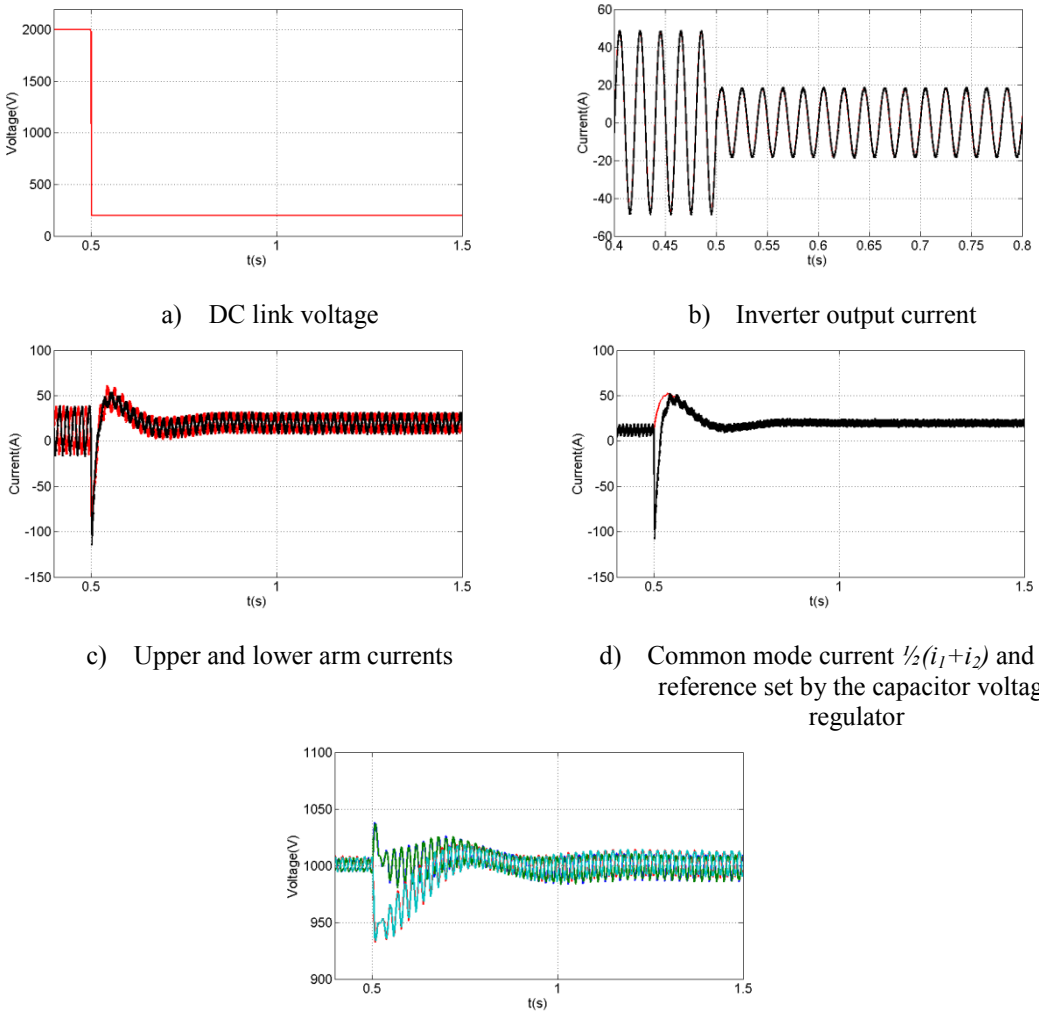
d) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator



e) Cell capacitor voltages

Figure 5-13. Simulation waveforms when the DC link voltage is reduced to 30% of its rating, when peak grid voltage is 850V and grid current is maintained stable

From Figure 5-12 (d) and Figure 5-13(d), the common mode current magnitude increases when DC link voltage is suppressed to a lower value. This feature restrains the maximum active power injected into the grid due to the limitation of the peak of common mode current. Thus the magnitude of the H-bridge MMC output AC current is decreased to maintain the peak arm currents and common mode current lower than the maximum rating. Figure 5-14 shows the step change of output current is applied when DC link voltage is suppressed to 10% at time t=0.5s. Figure 5-14 shows the output current is decreased to 30% of the rated magnitude and superimposed over its reference i_o^* when the inverter operates at unity power factor. Figure 5-14(c) and (d) shows that the arm currents and common mode current magnitudes are restricted while the cell capacitor voltages are regulated around the set point in Figure 5-14(e).



a) DC link voltage

b) Inverter output current

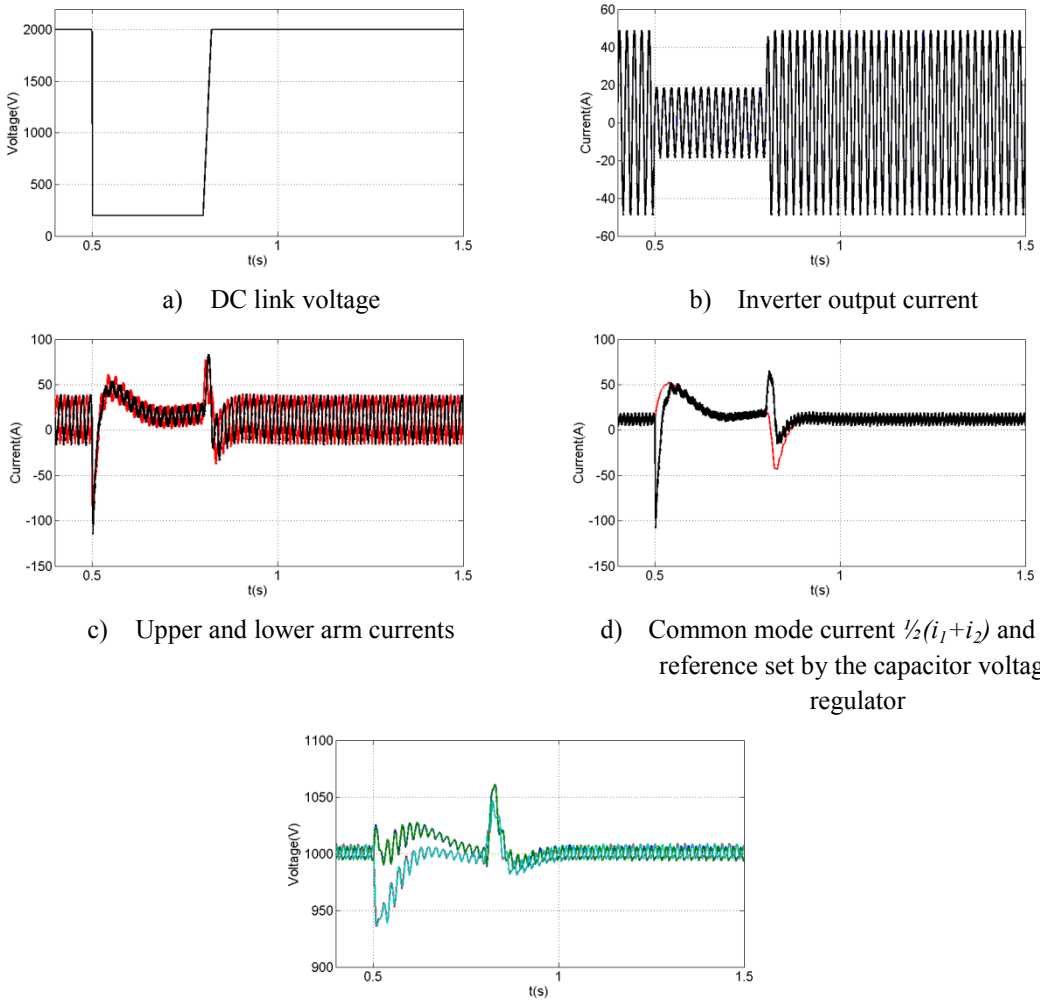
c) Upper and lower arm currents

d) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator

e) Cell capacitor voltages

Figure 5-14. Simulation waveforms when the DC link voltage is reduced to 10% and the peak grid voltage is 850V, where the magnitude of grid current is decreased to 30%

Figure 5-15 displays the case when a temporary DC fault is applied, as the DC link voltage collapsed to 10% at $t=0.5$ and recovered to rated voltage at t=0.8s. The output current magnitude is suppressed to 30% when the fault is applied and restored to the pre-fault value at t=0.9s in Figure 5-15(a). The arm currents and common mode current peak values are regulated and the quick dynamic response of the control loop restrains the common mode current overshoot in Figure 5-15(c) and (d). Cell capacitor voltages are balanced by utilising the common mode control loop in Figure 5-15(e).



a) DC link voltage

b) Inverter output current

c) Upper and lower arm currents

d) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator

e) Cell capacitor voltages

Figure 5-15. Simulation waveforms during a temporary DC fault while the DC link voltage is reduced to 10% and the magnitude of grid current is decreased to 30%

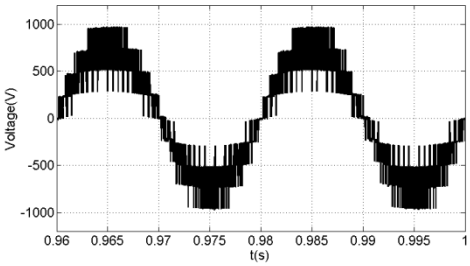
5.5.2 Nine-level H-bridge MMC

In this section, the control scheme is implemented on a H-bridge MMC with 4 cells per arm. The viability of the strategy applied to H-bridge MMC at different voltage levels is validated by the simulation results. The circuit parameters are identical to the previous section while each cell capacitor voltage rated value is $¼V_{DC}$.

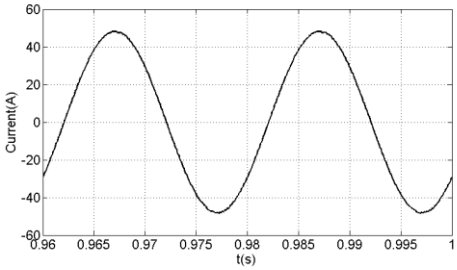
I. Normal operation in an off-grid condition

Figure 5-16 shows the simulation results when the nine-level H-bridge MMC operates at 0.9 modulation index and 0.8 power factor lagging. Figure 5-16(a) and (b) displays the synthesized output voltage and output current. The arm currents, common mode current, and their expanded versions in Figure 5-16(c), (d), (e) and (f)

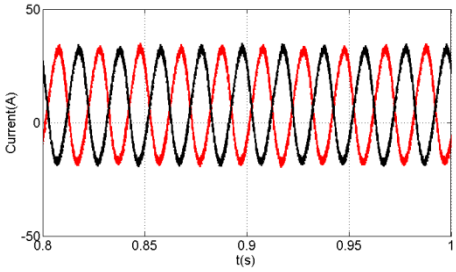
illustrate that the control strategy is applicable to the nine-level H-bridge MMC for the suppression of the harmonic components and the common mode current. Figure 5-16(g) displays that the voltages and the harmonic distortion across the cell capacitors are reduced to half those of the five-level H-bridge MMC.



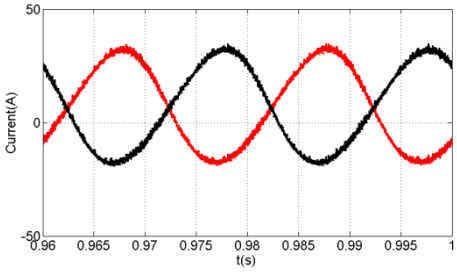
a) Converter terminal voltage



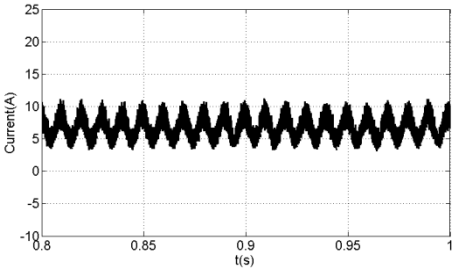
b) Converter output current



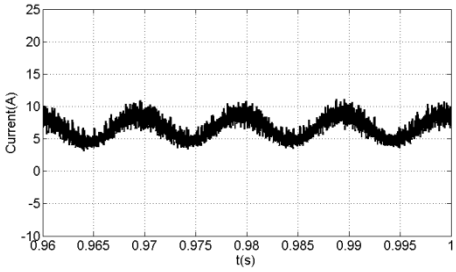
c) Upper and lower arm currents



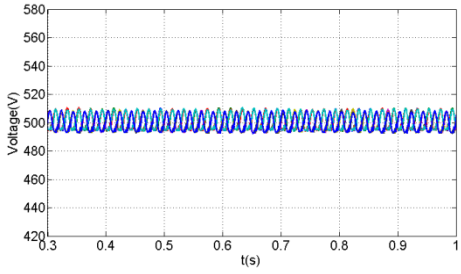
d) Expanded version of upper and lower arm currents



e) Common mode current (i_{dc}=½(i_1+i_2)) and its reference set by the DC voltage regulator that controls cell capacitor voltage of the upper and lower arms



f) Expanded version of Common mode current (i_{dc}=½(i_1+i_2)) and its reference

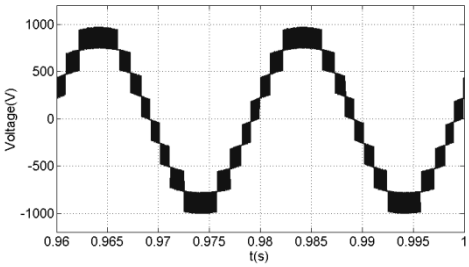


g) Cell capacitor voltage of the upper and lower arms

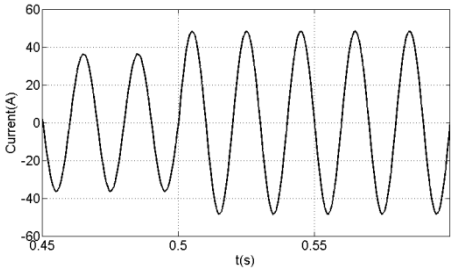
Figure 5-16. Simulation waveforms when a nine-level H-bridge MMC is operated at 0.9 modulation index and 0.8 power factor lagging.

II. Normal operation of grid connection

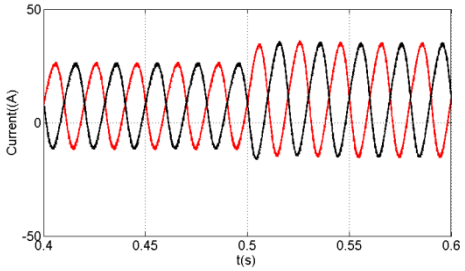
Figure 5-17 shows a step change of the H-bridge MMC output current applied at time t=0.5s where the original 36A magnitude is increased to 54A. Figure 5-17(b) displays that the output current follows the reference generated by the differential current (fundamental current) control loop illustrated in the block diagram in Figure 5-1. The arm currents and common mode current illustrated in Figure 5-17(c) and (d) are significantly improved compared with Figure 4-16(d) and (e) for the suppression of the harmonics. Cell capacitor voltage ripple is suppressed due to the elimination of the common mode current harmonics.



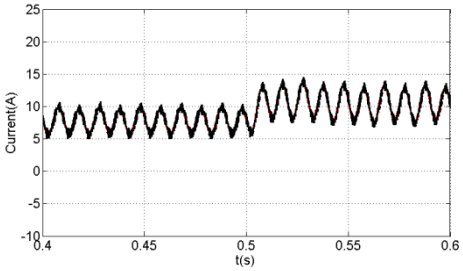
a) Converter terminal voltage



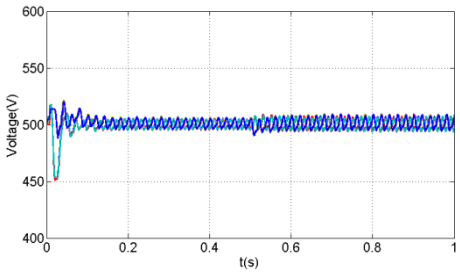
b) Converter output current



c) Upper and lower arm currents zoomed around the instant where step change is applied to the peak of the reference output current



d) Common mode current (i_{dc}=½(i_1+i_2))and its reference sets by the DC voltage regulator that controls cell capacitor voltages

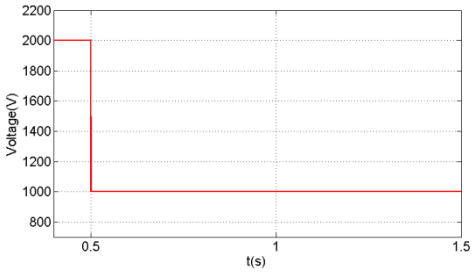


e) Cell capacitor voltage of the upper and lower arm

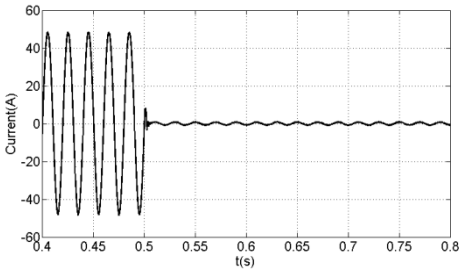
Figure 5-17. Selected simulation waveforms when the single-phase nine-level H-bridge MMC is controlled with the control scheme in Figure 5-1, and at t=0.5s the output peak reference current is step increased from I_m=36A to 54A.

III. DC voltage suppression test (DC fault emulation)

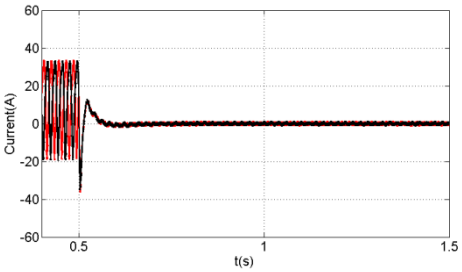
The nine-level H-bridge MMC behaviour is simulated during a DC fault when the DC link voltage is suppressed and the grid voltage magnitude remains constant. Illustrated in Figure 5-18 and Figure 5-19 (b), (c) and (d) converter output current is reduced to zero during the fault to eliminate inrush current while the arm currents and common mode current are forced to zero by the common mode control loop in Figure 5-1. The cell capacitor voltages are stabilized at the pre-fault level regardless of the DC link voltage in Figure 5-18 and Figure 5-19(e). The simulation results show that the control scheme is suitable for the H-bridge MMC with an increased number of cells, at any voltage level.



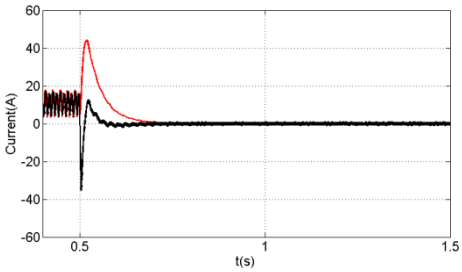
a) DC link voltage



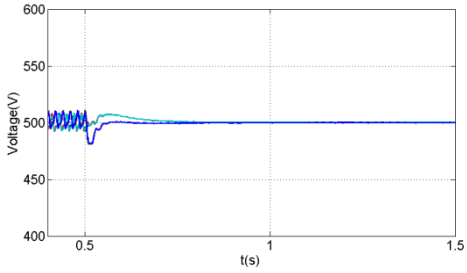
b) Inverter output current



c) Upper and lower arm currents

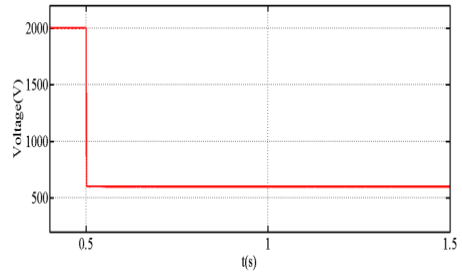


d) Common mode current and its reference

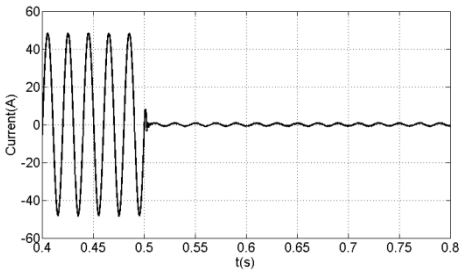


e) Cell capacitor voltages

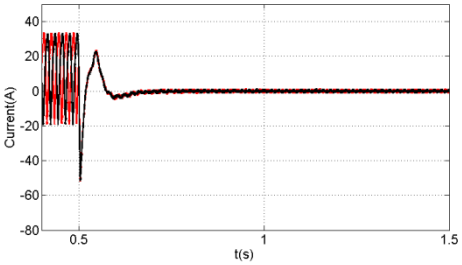
Figure 5-18. Simulation waveforms that show the improved behaviour of the nine-level H-bridge MMC during a DC fault (DC link voltage collapsed to 50%) when adopting the control scheme in Figure 5-1



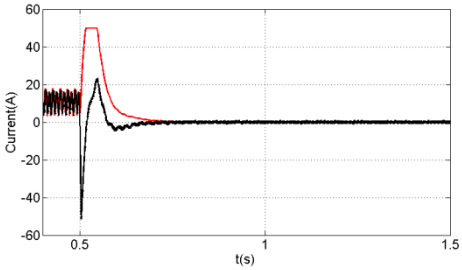
a) DC link voltage



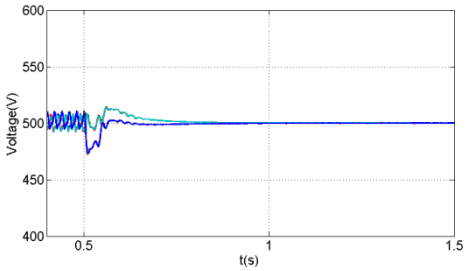
b) Inverter output current



c) Upper and lower arm currents



d) Common mode current $\frac{1}{2}(i_1+i_2)$ and its reference set by the capacitor voltage regulator



e) Cell capacitor voltages

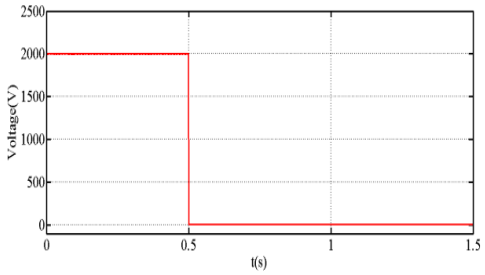
Figure 5-19. Simulation waveforms that show the improved behaviour of the nine-level H-bridge MMC during a DC fault (DC link voltage collapsed to 30%) when adopting the control scheme in Figure 5-1

IV. Typical cases of DC fault emulation

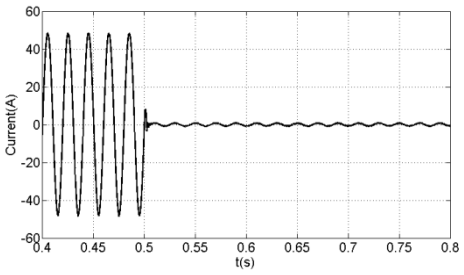
This section validates the control scheme for the restraining the inrush current, arm currents, and common mode current during a permanent DC fault when the DC link voltage collapses to zero. The fault is applied to DC link at t=0.5s, and the reference current converter injection into the AC grid reduces to zero immediately after DC fault is applied and remain at zero during the entire fault period.

Figure 5-20 (a) and (b) show converter DC link voltage and AC output current during permanent pole-to-pole DC link voltage suppression. The inrush current from the AC grid is regulated to zero with the control scheme in Figure 5-1. Figure 5-20 (c) and (d) show that the arm currents and its common mode remain controlled, with

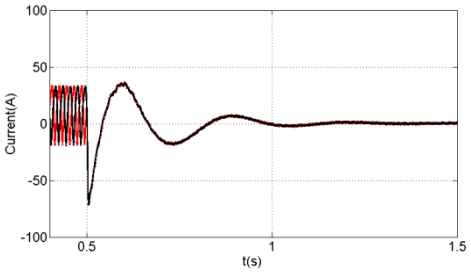
zero fundamental current from the AC grid, and the common mode current is controlled by the DC loops that regulate cell capacitor voltages and the common mode current. The cell capacitor voltages are maintained at the pre-fault level to provide voltage support to the AC network in Figure 5-20(e), by utilizing the proposed control scheme.



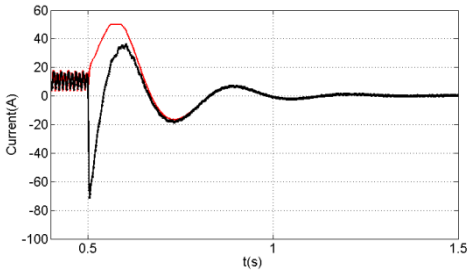
a) DC link voltage



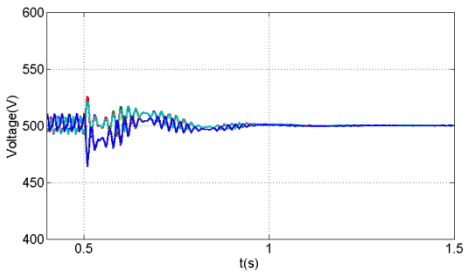
b) Inverter output current



c) Upper and lower arm currents



d) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator



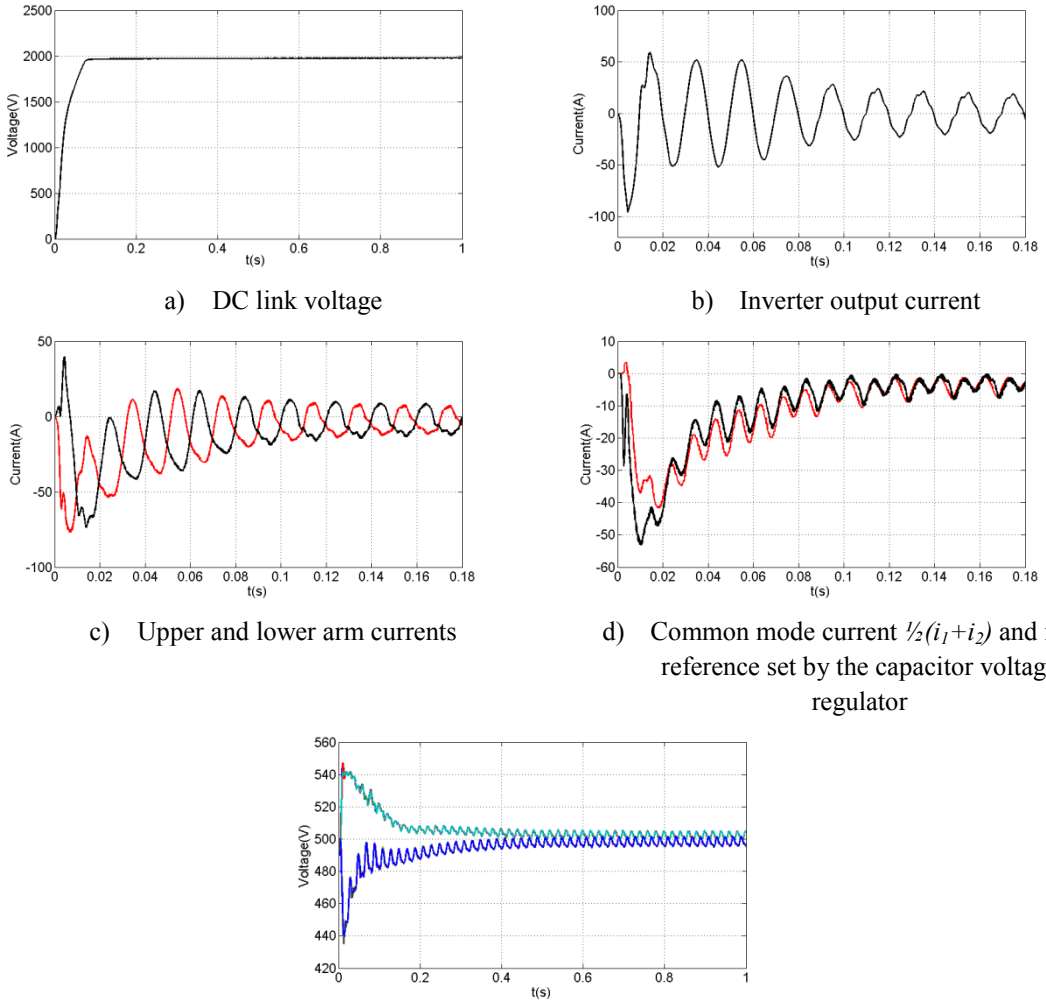
e) Cell capacitor voltages

Figure 5-20. Waveforms illustrating control scheme effectiveness during a permanent pole-to-pole DC short circuit fault, where the AC and DC currents in nine-level H-bridge MMC upper and lower arms are constrained, with no uncontrolled in-feed current from the grid

V. DC network Post-fault Recharging

DC network post-fault recharging with a nine-level H-bridge MMC is investigated in this section. The simulation results in Figure 5-21 shows that the DC link is recharged from the AC side without any external circuitry, when DC fault is cleared and cell capacitor voltages remain at the rated value. Figure 5-21(a) and (b) show

successful ramping-up of the H-bridge MMC DC voltage from zero to rated voltage with sinusoidal input currents from the AC side. Controlled arm currents and common mode current are demonstrated in Figure 5-21(c) and (d). Figure 5-21(e) shows that the voltages across the cell capacitors are maintained at the desired level at the end of the charging period. These simulation results validate that the control scheme for DC link recharging can be implemented to H-bridge MMCs with different voltage levels and cells per arm.



a) DC link voltage

b) Inverter output current

c) Upper and lower arm currents

d) Common mode current $\frac{1}{2}(i_1+i_2)$ and its reference set by the capacitor voltage regulator

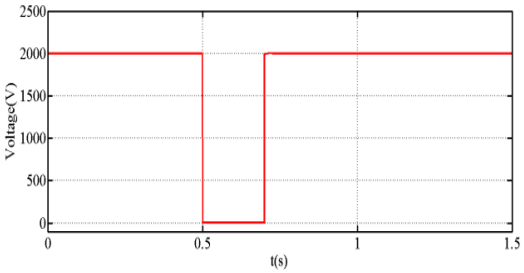
e) Cell capacitor voltages

Figure 5-21. Waveforms illustrate the DC network recharging from the AC grid without external circuitry during which the inrush current and common mode current are regulated

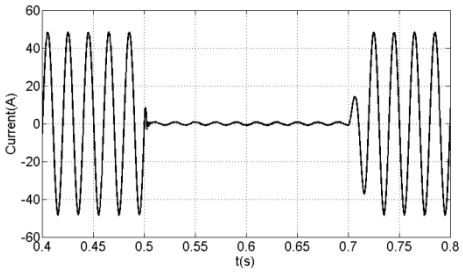
VI. Temporary DC fault emulation with instantaneous DC link voltage recovery

For the nine-level H-bridge MMC, a temporary DC fault is applied at t=0.5s, and cleared at t=0.7s. Converter output power (the output AC current fundamental peak)

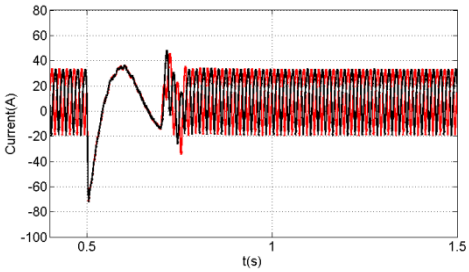
is reduced to zero at t=0.5s and restored to the pre-fault value at t=0.8s. As shown in Figure 5-22, the waveforms are consistent with the previous case that considered a permanent DC fault, but here the system recovers quickly when DC fault is cleared.



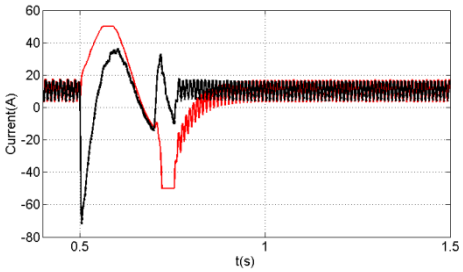
a) DC link voltage



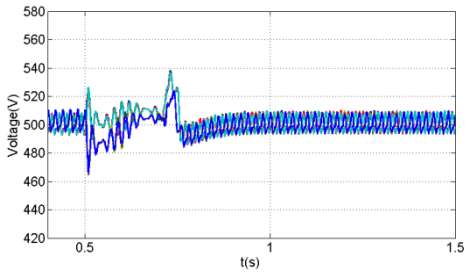
b) Inverter output current



c) Upper and lower arm currents



d) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator



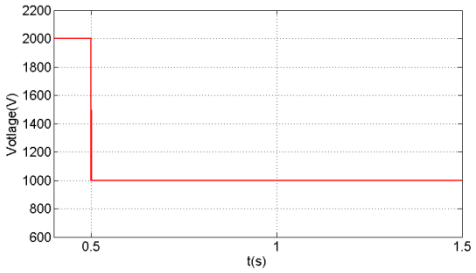
e) Cell capacitor voltages

Figure 5-22. Waveforms illustrate the control scheme effectiveness during a temporary DC short circuit fault in restraining AC and DC currents in the converter upper and lower arms, and elimination of the uncontrolled in-feed current from the grid, without converter blocking

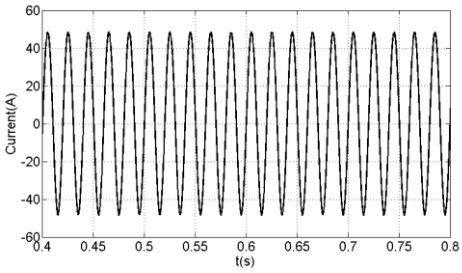
VII. Active power injection into the AC grid when the H-bridge MMC operates in a boost mode during DC voltage sag

Figure 5-23 and Figure 5-24 illustrate when the converter DC link voltage is reduced to 50% and 30% of the rated voltage, while the grid AC voltage peak remains at 850V. The MMC peak output current is set to the normal operation mode, 54A. The output current is regulated to follow its reference while the arm currents and common

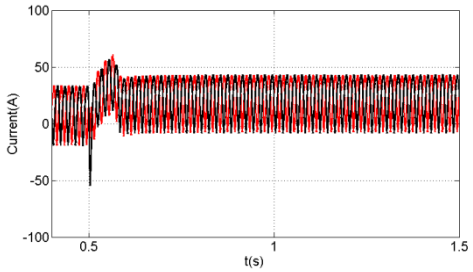
mode current are restrained below the peak magnitude value in Figure 5-23 and Figure 5-24(b), (c) and (d). The capacitor voltages oscillate around the rated value throughout.



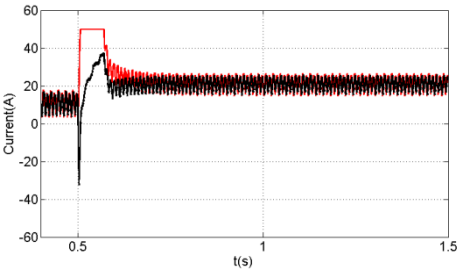
a) DC link voltage



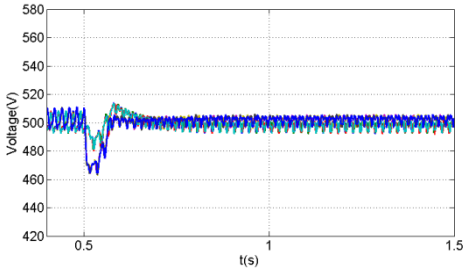
b) Inverter output current



c) Upper and lower arm currents

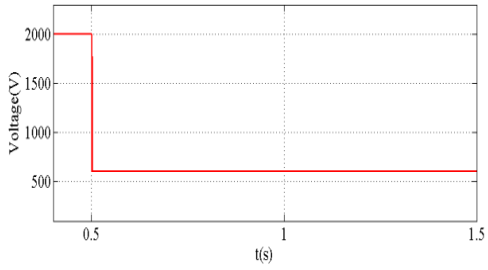


d) Common mode current $\frac{1}{2}(i_1+i_2)$ and its reference set by the capacitor voltage regulator

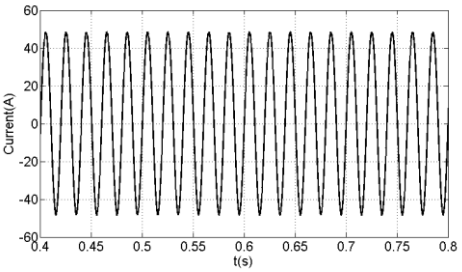


e) Cell capacitor voltages

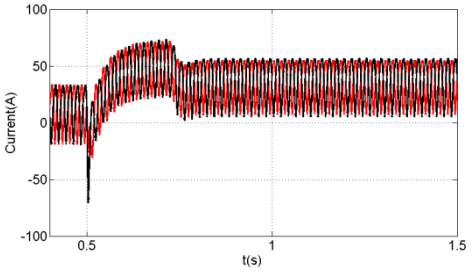
Figure 5-23. Simulation waveforms when the DC link voltage is reduced to 50% and the peak grid voltage is 850V, with the grid current maintained stable



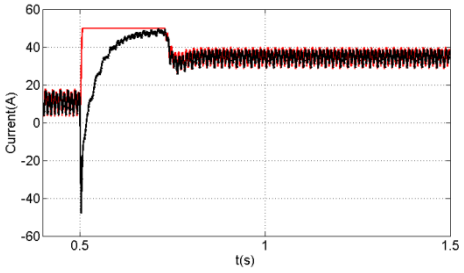
a) DC link voltage



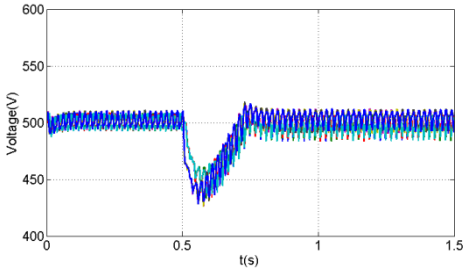
b) Inverter output current



c) Upper and lower arm currents



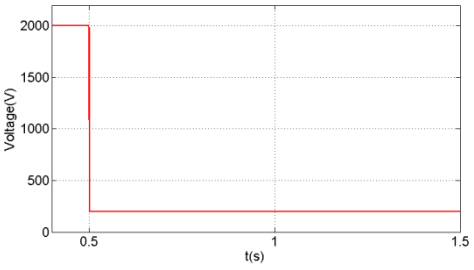
d) Common mode current $\frac{1}{2}(i_1+i_2)$ and its reference set by the capacitor voltage regulator



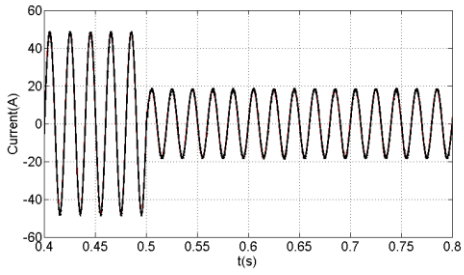
e) Cell capacitor voltages

Figure 5-24. Simulation waveforms when the DC link voltage is reduced to 30% and the peak grid voltage is 850V, with the grid current maintained stable

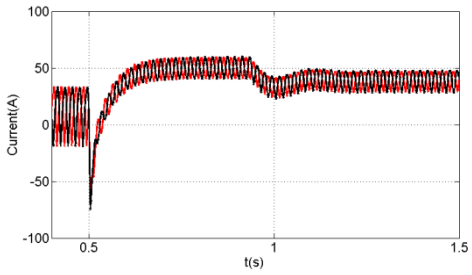
To limit the maximum arm currents and common mode current, the output current magnitude is reduced. Figure 5-25 shows the step change of output current applied when DC link voltage is suppressed to 10% at t=0.5s. Figure 5-25(b) shows the output current is decreased to 30% and superimposed over its reference i_o^* when the inverter operates at unity power factor. Figure 5-25(c) and (d) shows that the magnitudes of the arm currents and common mode current are restricted while the cell capacitor voltages are regulated around the set point in Figure 5-25(e).



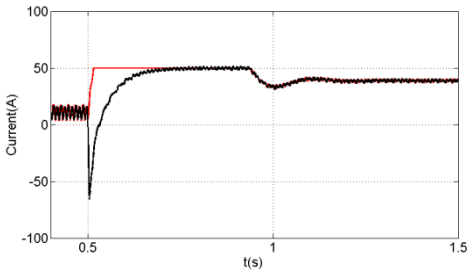
a) DC link voltage



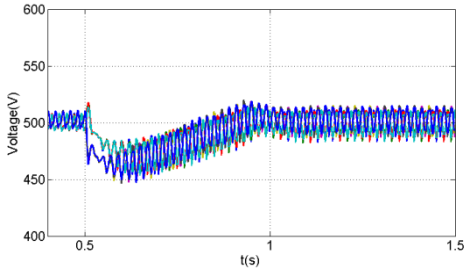
b) Inverter output current



c) Upper and lower arm currents



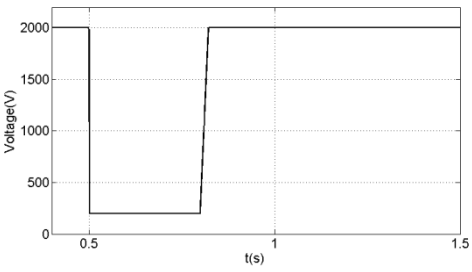
d) Common mode current $\frac{1}{2}(i_1+i_2)$ and its reference set by the capacitor voltage regulator



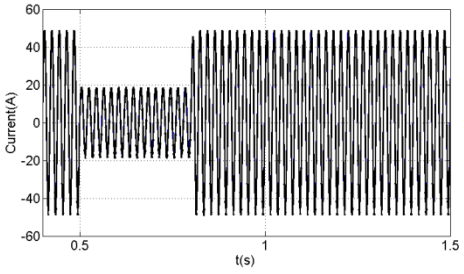
e) Cell capacitor voltages

Figure 5-25. Simulation waveforms when the DC link voltage is reduced to 10% and the peak grid voltage is 850V, where the magnitude of grid current is decreased to 30%

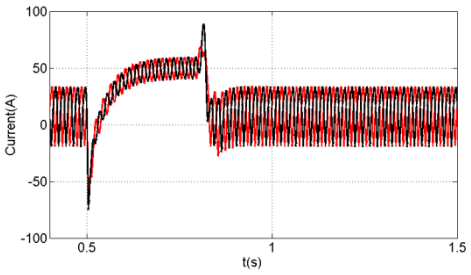
Figure 5-26 displays a temporary DC fault applied as DC link voltage collapsed to 10% at t=0.5s and recovery to rated value at t=0.8s. The magnitude of output current of nine-level H-bridge MMC is suppressed to 30% when the fault is applied and restored to the pre-fault value at t=0.9s in Figure 5-26 (a). The peak arm currents and common mode current are regulated and the quick dynamic response of the control loop restrains the common mode current overshoot in Figure 5-26(c) and (d). Cell capacitor voltages are balanced by utilising the common mode control loop in Figure 5-26(e).



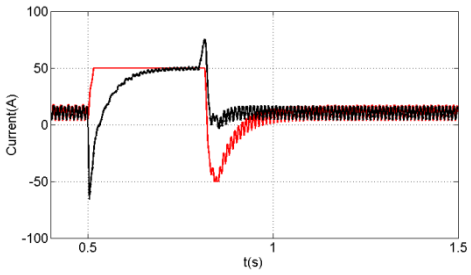
a) DC link voltage



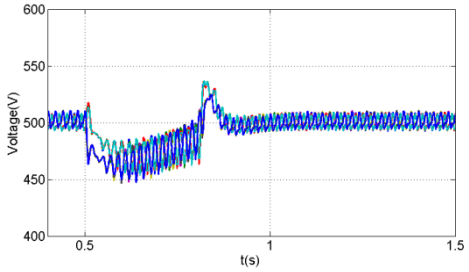
b) Inverter output current



c) Upper and lower arm currents



d) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator



e) Cell capacitor voltages

Figure 5-26. Simulation waveforms during a temporary DC fault while the DC link voltage is reduced to 10% and the magnitude of grid current is decreased to 30%

5.6 **Experimental validation**

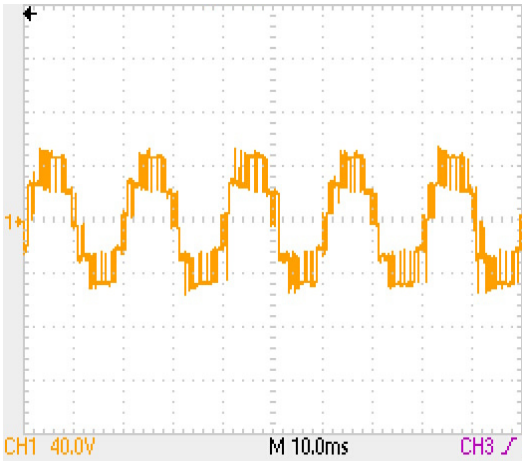
This section provides experimental validation of the control scheme using a scaled prototype of a single-phase five-level H-bridge MMC that is shown in Figure A-1, with 4.7mF cell capacitors and 6mH arm inductance. A programmable DC voltage supply is used to provide variable DC link voltages under different conditions (100V as the rated DC link voltage). The converter is connected to the AC grid, with a 46V peak, through a 5mH interfacing reactor, and controlled using SPWM with a 2.1kHz switching frequency. An Infineon Technology Tri-core microcontroller TC 1796 executes the modulation and capacitor voltage balancing strategy.

5.6.1 **Normal operation**

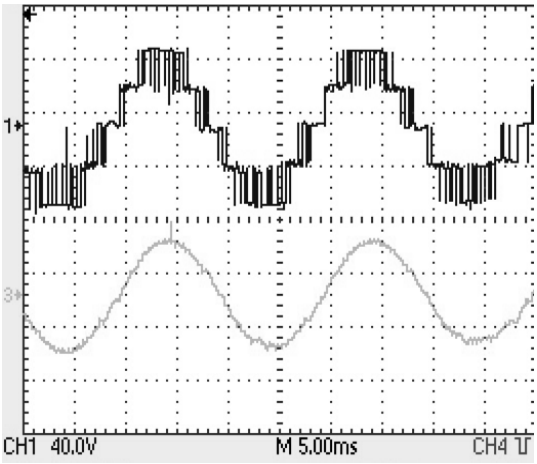
I. Off-grid condition

This case presents experimental results obtained in an off-grid condition while the modulation index is 0.9 and power factor is 0.9 lagging. Figure 5-27(b) illustrates the converter output voltage and current relative to the neutral point while the current magnitude is 4A. Figure 5-27(c) displays converter upper and lower arm currents, where the upper and lower arm currents are regulated sinusoidal, identical to the

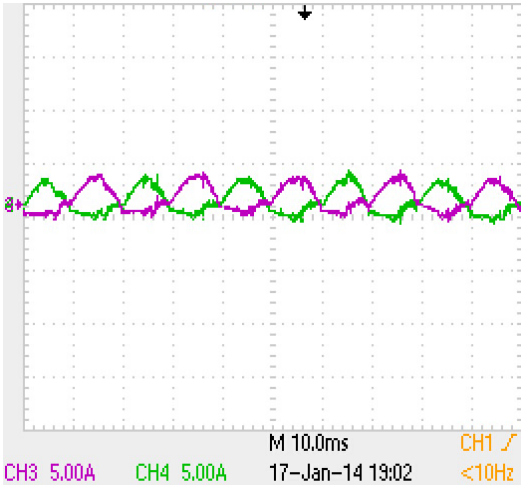
simulation results. Figure 5-27(d) demonstrates that the harmonic components and the common mode current magnitude is significantly suppressed by the control scheme. Figure 5-27(e) shows the cell capacitor voltages are balanced while the voltage ripple has been decreased due to suppression of the arm current harmonics. Compared with the experimental results displayed in Figure 4-17, the arm currents and common mode current are significantly improved while cell capacitor voltage ripple is suppressed.



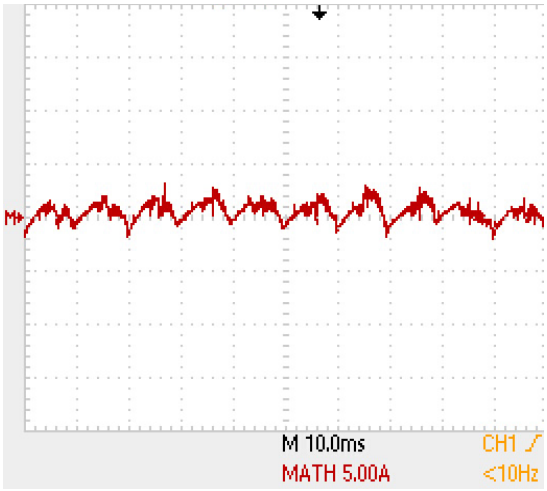
(a) Voltage waveform at converter terminal, measured relative to supply mid-point (v_o)



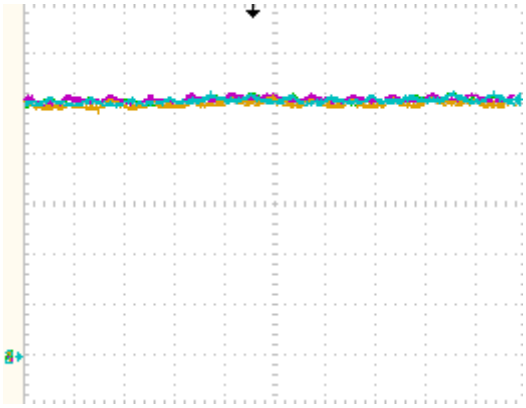
(b) Output voltage and H-bridge MMC output current (i_o)



(c) Upper and lower arm currents



(d) Common mode current (i_1+i_2), which includes DC and harmonic complements of the arm current

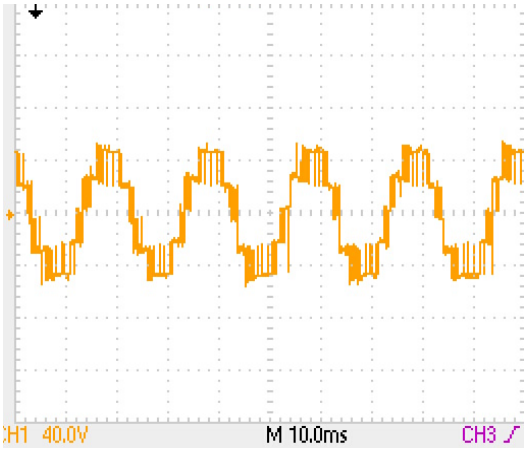


(e) Cell capacitor voltages of the H-bridge cells

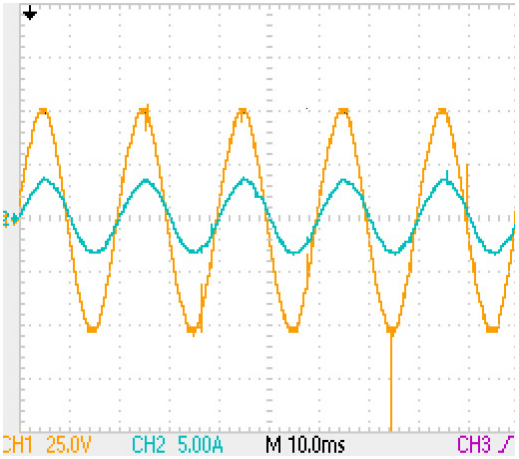
Figure 5-27. Experimental waveforms demonstrating the viability of the control scheme during off-grid normal operation (100V DC link voltage, 2.1kHz switching frequency, and grid voltage 46V peak)

II. Grid-connected condition

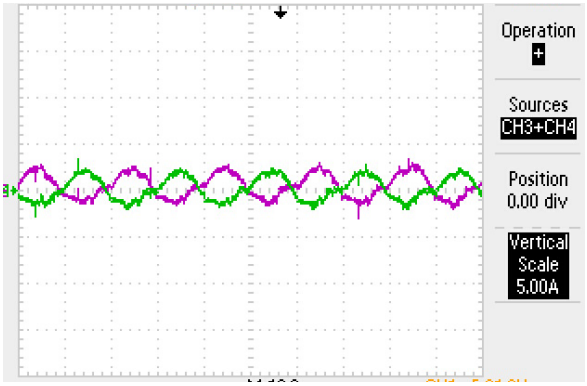
This case presents experimental results when a single-phase H-bridge MMC injects 4A peak into AC grid, at unity power factor. Figure 5-28(a) shows the H-bridge MMC terminal voltage relative to supply mid-point. Figure 5-28 (b) shows the inverter output current and AC grid voltage waveforms at the point of common coupling are in phase, where i_o has a 4A peak reference. Figure 5-28 (c) presents the converter upper and lower arm currents, which are nearly sinusoidal, superimposed over a DC offset, as previously demonstrated in the simulation section. Figure 5-28(d) shows the cell capacitor voltages of the H-bridge MMC are maintained around $½V_{dc}$. Figure 5-28 (e) displays the common mode current i_1+i_2, which is the typical image of its reference provided by the outer cell capacitor voltage regulator shown in Figure 5-1. As the cell capacitor voltages vary, the common-mode current i_{dc} is modulated with a 2nd harmonic as shown in Figure 5-28(e) in order to inject the necessary harmonics in the modulating signals of the upper and lower arm to suppress the 2nd harmonic from the both arm currents, as previously illustrated in simulation section (Figure 5-6 (c) and (d)). Compared with the experimental results displayed in Figure 4-18, the harmonic components and magnitude of the arm currents and common mode current during grid-connected condition have been significantly suppressed while the cell capacitor voltage ripple is decreased.



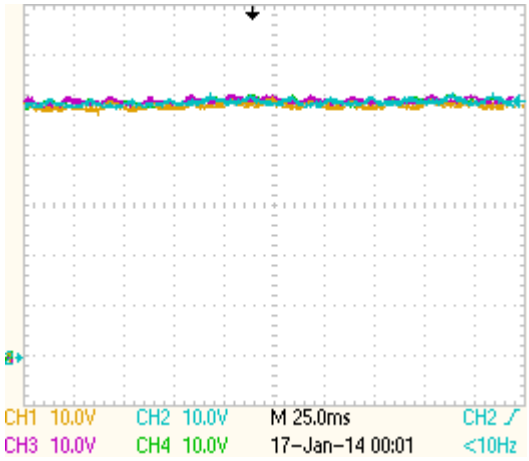
(a) Voltage waveform at converter terminal, measured relative to supply mid-point, v_o



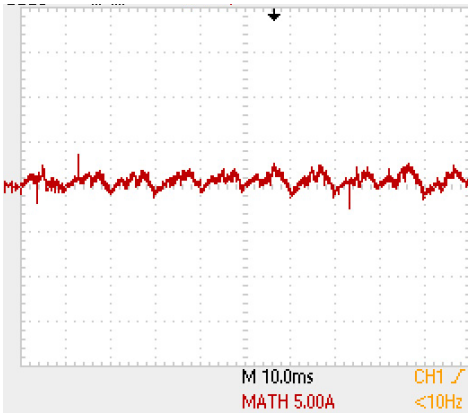
(b) Grid voltage and H-bridge MMC output current i_o



(c) Upper and lower arm currents



(d) Cell capacitor voltages of the H-bridge cells

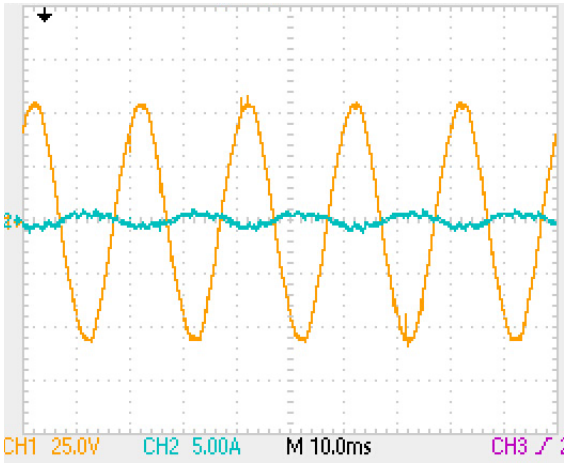


(e) Common mode current i_1+i_2, which includes DC and harmonic complements of the arm current

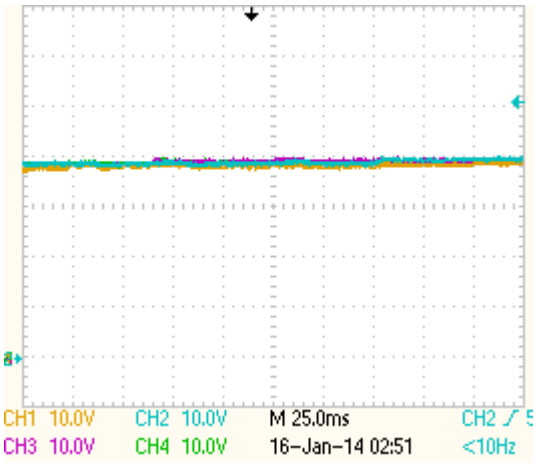
Figure 5-28. Experimental waveforms demonstrating the viability of the control scheme during grid connected-normal operation (100V DC link voltage, 2.1kHz switching frequency, and 46V peak grid voltage)

5.6.2 Operations under low DC voltage

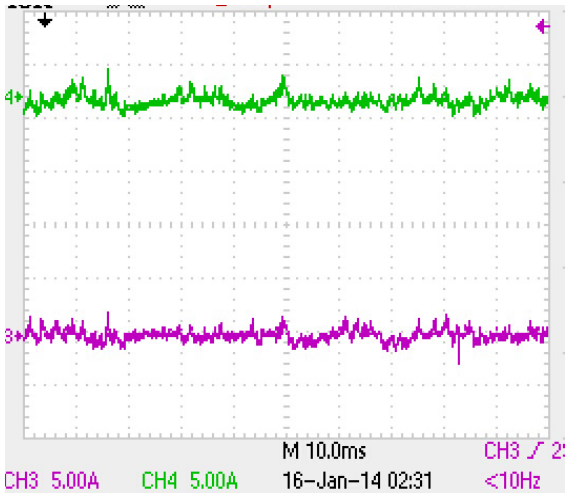
The section provides experimental validation of the simulation results in Figure 5-8 when the converter DC link voltage is reduced to 30% (30V), with the AC grid voltage remaining at 46V peak. As the output current is reduced to near zero in Figure 5-29(a), the magnitude of the arm currents and common-mode current are all minimised in Figure 5-29(c) and (d), with only active power provided to the cell capacitors to maintain them at rated voltage, Figure 5-29(b). Uncontrolled inrush current from the AC grid is eliminated. This confirms that converter blocking is not necessary, as demonstrated in Figure 5-8, provided the control scheme in Figure 5-1 is adopted and all redundant switch states of the H-bridge MMC are fully exploited.



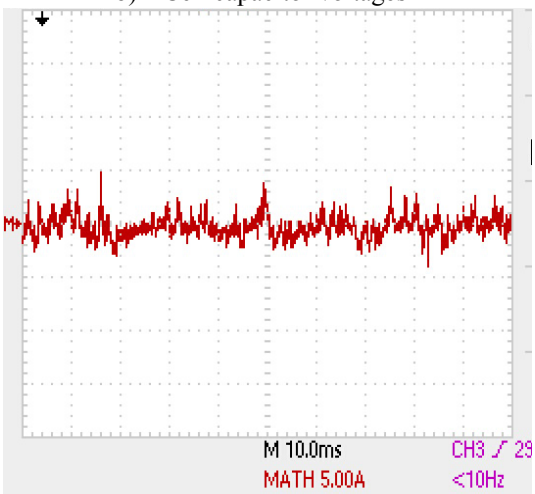
a) Grid voltage and inverter output current



b) Cell capacitor voltages



c) Upper and lower arm currents

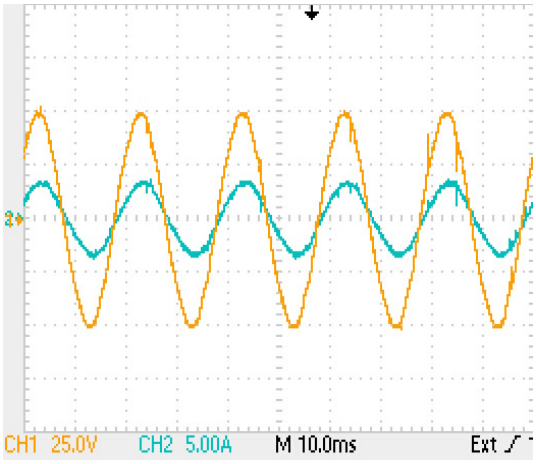


d) Common mode current i_1+i_2, which includes DC and harmonic complements of the arm current

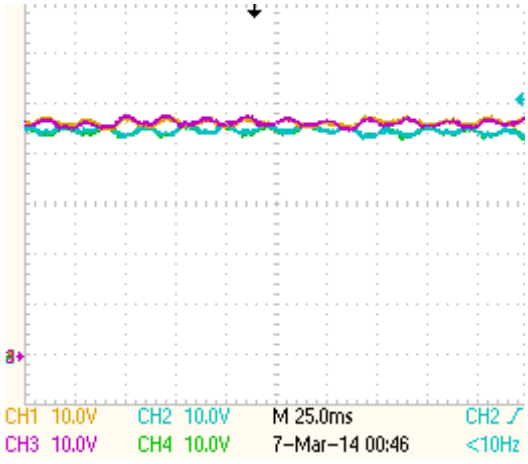
Figure 5-29. Waveforms when the H-bridge MMC emulates behaviour during a DC side fault (DC link voltage is reduced to 30% (30V) with a 46V peak grid voltage)

5.6.3 Demonstration of active power injection into the AC grid when the H-bridge MMC operates in boost mode

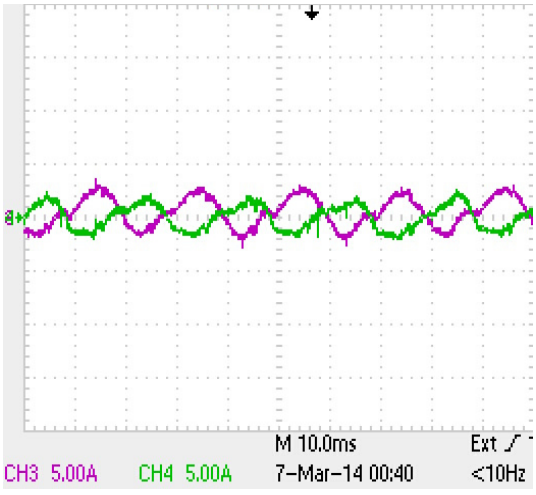
This section illustrates the control scheme enabling the H-bridge MMC to operate in a boost mode (when converter DC link voltage is less than peak of the phase AC voltage). For demonstration, converter DC link voltage is reduced to 70% and 50%, while the grid voltage remains at 46V, with the DC loop that regulates cell capacitor voltages continuing to maintain them at rated voltage. In this example, the reference current peak is set to 4A. With the proposed control strategy, the current waveforms the converter injects into the AC grid remains sinusoidal and fully controlled in phase with grid voltage, while cell capacitor voltage balancing is maintained and arm currents and the common mode current all have low harmonic distortion, see Figure 5-30 and Figure 5-31 (a), (b), (c) and (d). This confirms that the H-bridge MMC can fully controlled the active power to the AC grid over a wide range of DC link voltages (buck and boost modes), unlike VSCs discussed in the literature.



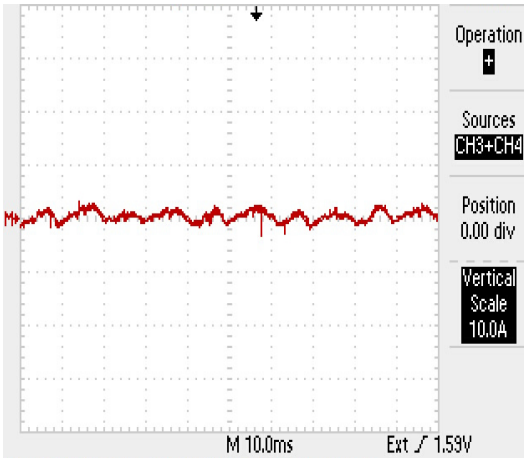
a) Grid voltage and inverter output current



b) Cell capacitor voltages



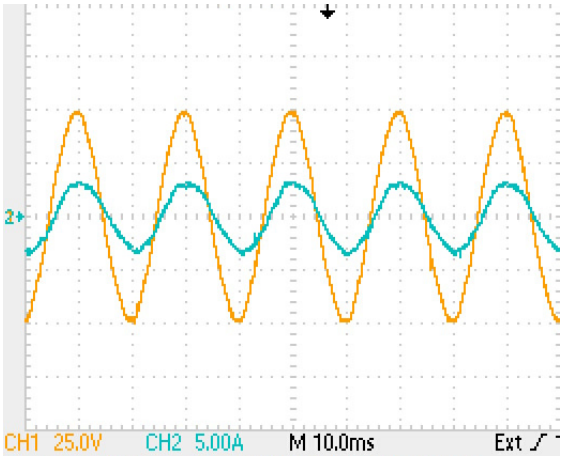
c) Upper and lower arm currents



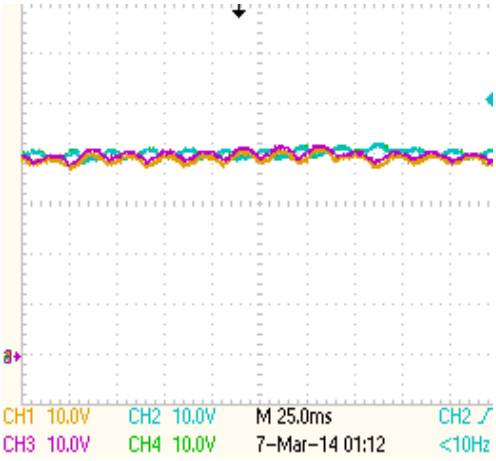
d) Common mode current i_1+i_2, which includes DC and harmonic complements

of the arm current

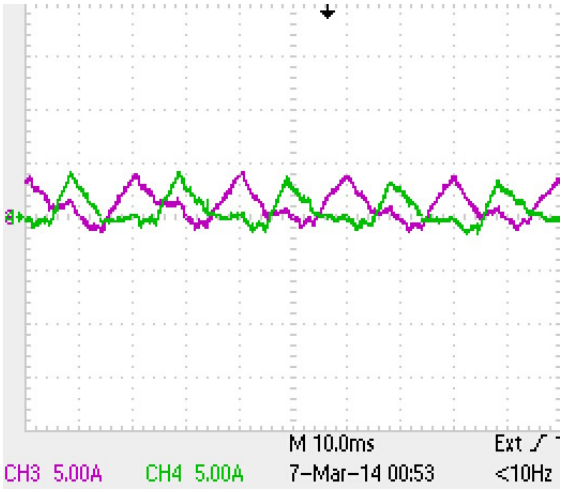
Figure 5-30. Waveforms from the test that emulates H-bridge MMC behaviour during a DC side fault (DC link voltage is reduced to 70% (70V) when peak grid voltage is 46V) and grid current is maintained stable



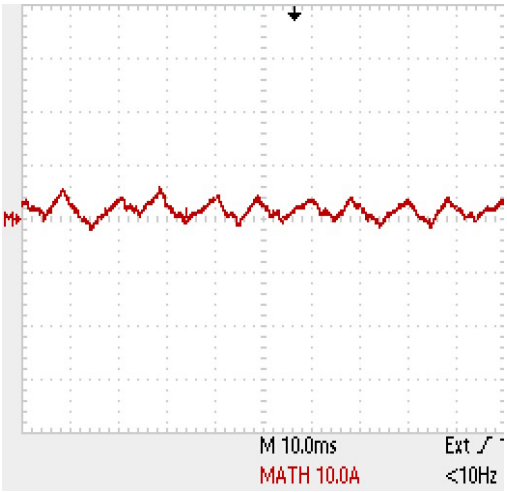
a) Grid voltage and inverter output current



b) Cell capacitor voltages



c) Upper and lower arm currents

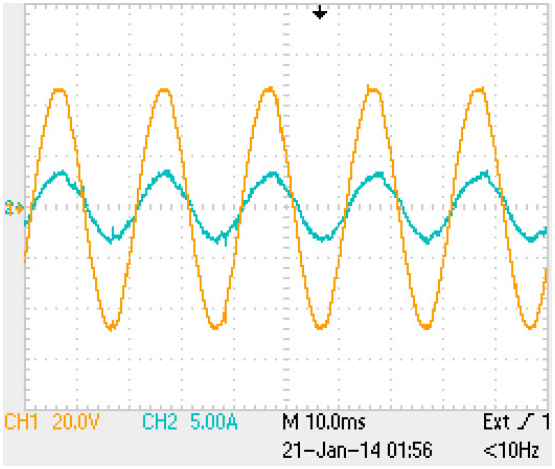


d) Common mode current i_1+i_2, which includes DC and harmonic complements of the arm current

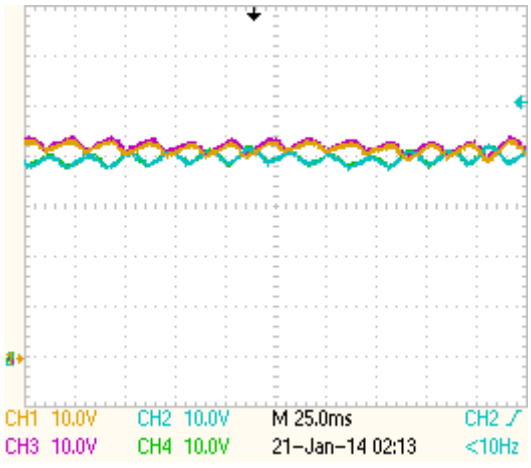
Figure 5-31. Waveforms from the test that emulates H-bridge MMC behaviour during DC side fault (DC link voltage is reduced to 50% of its rated (50V) when peak grid voltage is 46V) and grid current maintained stable

From Figure 5-32, when DC link voltage is suppressed to a low level, the arm currents no longer tend to be sinusoidal as in normal operation, see Figure 5-32 (c). Figure 5-32 (d) shows the resultant common mode current during operation in a boost mode. But the converter output current remains sinusoidal and synchronized with grid voltage in Figure 5-32(a) while the cell capacitor voltages remain balanced. Based on these results it can be concluded that when the control scheme provided in

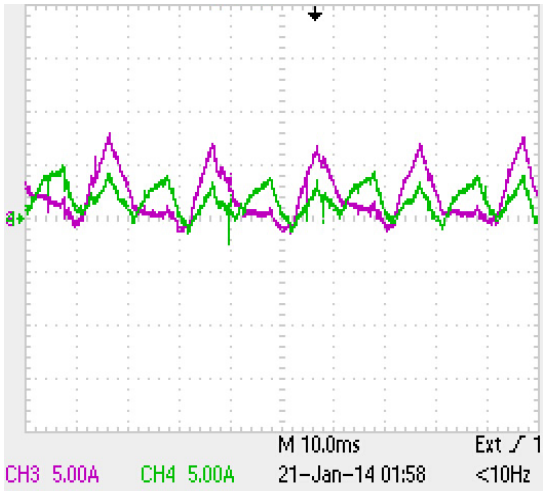
Figure 5-1 is adopted and all redundant switch states of the H-bridge MMC are fully exploited, H-bridge MMC becomes an alternative to the converters currently being used in medium voltage applications where maximum power tracking is normally used to maximize the return on investment, without the use of a DC/DC converter.



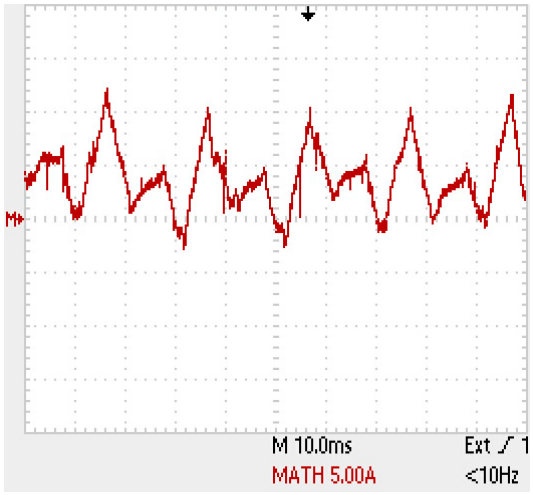
a) Grid voltage and inverter output current



b) Cell capacitor voltages



c) Upper and lower arm currents

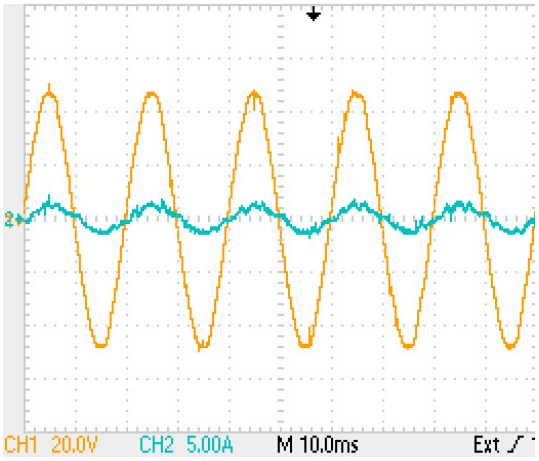


d) Common mode current i_1+i_2, which includes DC and harmonic complements of the arm current

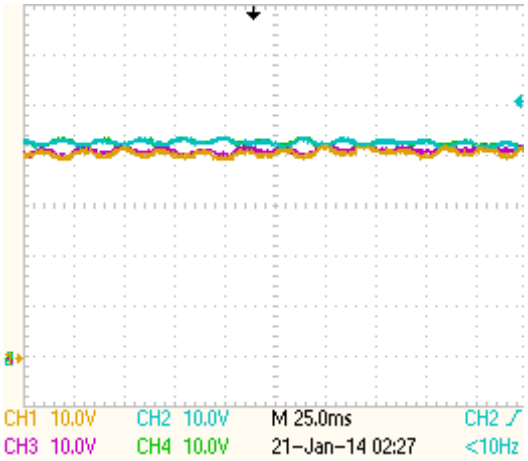
Figure 5-32. Waveforms when the H-bridge MMC emulates behaviour during a DC side fault (DC link voltage is reduced to 30% (30V) when peak grid voltage is 46V) and grid current maintained stable

To limit the maximum arm currents and common mode current, the magnitude of output current is reduced. The experimental results in Figure 5-33(a) illustrate that the output current is decreased to 50% (2A) when the converter operates at unity power factor. Figure 5-33(c) and (d) displays that the magnitudes of the arm currents and common mode current are suppressed while the cell capacitor voltages are

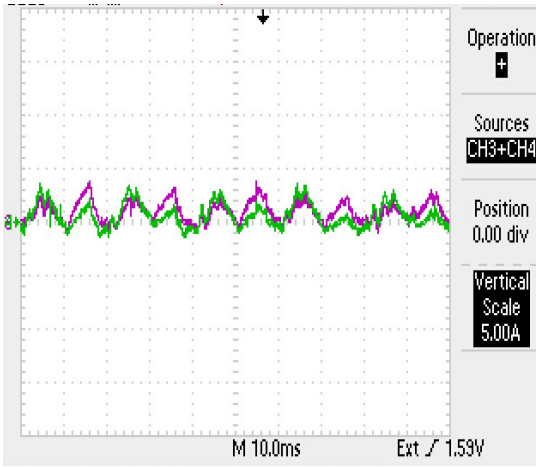
regulated around the set point with low voltage ripple, in Figure 5-33(b). This feature facilitates the application of the H-bridge MMC in maximum power point tracking (MPPT) applications that is generally required in renewable energy transmission systems, without the use of a DC/DC converter.



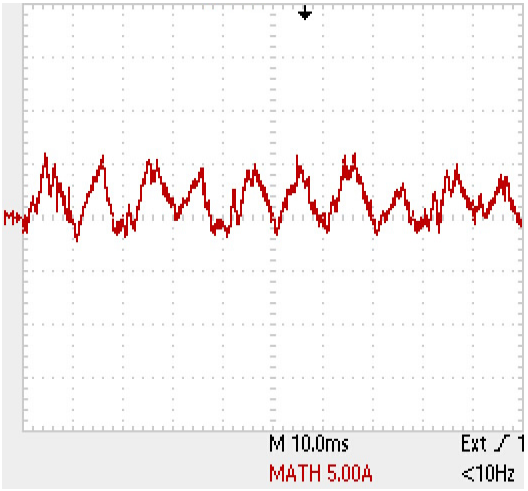
(a) Grid voltage and inverter output current



(b) Cell capacitor voltages



(c) Upper and lower arm currents



(d) Common mode current i_1+i_2, which includes DC and harmonic complements of the arm current

Figure 5-33. Waveforms from the test that emulates H-bridge MMC behaviour during a DC side fault (DC link voltage is reduced to 30% (30V) when peak grid voltage is 46V) and the grid current is 2A

5.7 **Summary**

This chapter presented a common mode current and differential mode current control scheme that permits the H-bridge MMC to operate over the full range of modulation indices and load power factor in an off-grid condition, and unity power factor in a grid-connected condition. The controller also enables the H-bridge MMC to ride through a DC fault and to recover quickly when the fault is cleared, without any external circuitry and without uncontrolled ac inrush current. The converter can provide active power to the grid while the DC link voltage is suppressed to less than the peak line voltage, by utilizing the control scheme. The validity of the presented control strategy was confirmed by simulation and experimentation, while system scalability to high voltage applications and increased number of cells per arm, was investigated. The advantage of the control scheme in Figure 5-1 compared with the normal control scheme presented in Chapter 4 can be concluded as:

- It suppresses harmonic distortion and magnitude of the arm currents and common mode current, with the common mode current control loop in Figure 5-1. Thus the ripple components of the cell capacitor voltages, power losses, and energy storage requirement of each arm are decreased, based on the analysis in section 5.4. This may facilitate reduced cell capacitor sizing.
- The control scheme utilizes the unique feature of a H-bridge cell to generate bi-polarity output voltage to suppress inrush current during a DC fault and provides controlled re-establishment of DC network without external circuitry. With a permanent DC fault, it allows the H-bridge MMC to provide voltage support to the grid. In both cases, the cell capacitor voltages are regulated and balanced around the rated value.
- With a normal control strategy, the converter operates in a buck mode. With the common mode current and differential mode current control scheme, the H-bridge MMC is capable of operating in both buck and boost modes. Theoretically, the converter can provide active power to the grid over the full range of the DC link voltages (0 to V_{DC}). This feature allows the H-bridge MMC to be implemented in medium voltage renewable energy transmission such as PV and off-shore wind farms which generate output voltage that varies over a wide range without the use of a DC/DC converter.

- Black-start capability can be achieved by the control scheme, without the need for external circuitry to charge the cell capacitors.

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[1] S. Xu, A. Huang, X. Ni, and R. Burgos, "AC circulating currents suppression in modular multilevel converter," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, 2012, pp. 191-196.

[2] F. H. Khan and L. M. Tolbert, "Bi-directional power management and fault tolerant feature in a 5-kW multilevel dc-dc converter with modular architecture," *Power Electronics, IET,* vol. 2, pp. 595-604, 2009.

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Chapter 6. Application of H-bridge MMC in DC transmission System

This chapter investigates the possibility of controlled survival and recovery of the voltage source converter (VSC) based high-voltage dc (HVDC) transmission system from DC side faults, without exposing converter stations to the risk of failure, and without collapse of the connected AC networks. This is achieved by controlling the VSC arm currents and voltages, full exploitation of the bipolar capability of the MMC H-bridge cells to facilitate controlled operation of the VSC-HVDC link with variable DC link voltage from zero to rated voltage. In this manner, the risk of uncontrolled AC current in-feed from the AC side to the DC side is avoided when the converter stations are not blocked during the DC fault period. This may have significant implications in the development of the overhead HVDC links and multi-terminal DC grids, especially in situations where DC circuit breakers are replaced by relatively cheap isolators.

6.1 **Introduction**

Half and H-bridge MMCs have emerged as attractive topologies for medium and high voltage applications. These topologies offer the following features: can be extended to high voltage without exposing the converter transformer to extreme *dv/dt*'s, as with the NPC; their modular structure enables converter internal fault management, while the system remains operational; and low semiconductor losses[1]. Additionally, the use of distributed cell capacitors in the half-bridge MMC improves its DC fault ride-through capability as the magnitude of uncontrolled AC in-feed currents that may flow in the converter switching devices during DC fault is significantly reduced (due to the significant reduction in DC side energy storage). The H-bridge MMC can eliminate the flow of uncontrolled AC in-feed current to the DC side during a DC fault, by blocking the converter switches. Although this feature is attractive, the H-bridge MMC incurs higher semiconductor losses than the half-bridge MMC (2.35 times those of the half-bridge MMC, according to ABB [1]). This makes justification for its HVDC application challenging. Although there are several alternative converter topologies that offer limited DC fault short circuit ride-through capability, with relatively low semiconductor losses[2-7], half and H-bridge MMCs remain the industry preferred topologies.

There are studies published on different aspects of MMCs that address key challenges at high and medium voltages [8-26]. For example, the basic operational principle, modulation and capacitor voltage balancing of the MMC are discussed in [18, 23, 24, 27, 28]. The authors in [18, 27, 28] adopted the use of a single reference per phase for both sinusoidal PWM and staircase modulation with the nearest voltage levels. Also, these authors have demonstrated the possibility of using output phase currents rather than the arm current for control and capacitor voltage balancing. However, the use of a single reference increases number of switch combinations that can be used to maintain cell capacitor voltage balancing, which make modulator generalization more challenging.

The use of two reference signals per phase (one per arm) for controlling the MMC using pulse width (level shifted phase disposition) and staircase modulation, is proposed in [16]. This approach is widely used because it makes MMC modulation generalisation simpler that in [18, 27, 28], and programming of the converter modulation and capacitor voltage balancing strategies is simpler.

The authors in [29] presented a Lagrange multiplier based power control in the ABC frame for the MMC that optimizes the common mode current or capacitive energy oscillations. This control is able to minimize the common mode current oscillations by estimating the desired current references analytically, after considering the differential mode current and energy per phase. The drawback of this control approach is that it uses the differential and common mode energies as inputs to the outer control loop that regulates active power that enhances the complexity.

The use of phase-shifted carriers PWM (PS-PWM) for the MMC where each cell is controlled independently, including regulation of the cell capacitor voltages is discussed in [30, 31]. This approach generates high quality output voltage at a reduced switching frequency per cell, and simplifies overall MMC control as time consumed for cell capacitor voltage sorting is not needed. However, its main drawbacks are: switching of more than one voltage level is unavoidable, and cell capacitor voltages tend to diverge from the desired set-point when the system is subjected to minor transients[32-34].

References [31, 35-37] present an improved control strategy which is applicable to half and H-bridge MMCs that uses PS-carrier PWM with a number of control loops for cell capacitor voltages, arm current balancing, common mode current suppression, and individual cell capacitor voltage balancing, to ensure stable system operation, independent of operating conditions. The validity of the control approach in [31, 35-37] is confirmed using simulation and experimentation. However, the increased control reliance in order to maintain cell capacitor voltage balancing leads to system collapse from any control system malfunction, which is not the case with traditional approaches. This approach is therefore less likely to be adopted in HVDC applications.

Reference [38] develops fundamental switching frequency modulation and capacitor voltage balancing that is suitable for high and medium voltage MMC applications. The authors in [38] show that the proposed approach ensures each switching devices operates at the fundamental frequency (low switching), with cell capacitor voltages maintained stable. The main shortcoming is that these increase the energy requirement per sub-module capacitor several fold compared to pulse width and staircase modulations in order to ensure cell capacitor voltage ripple remains within

an acceptable range (233kJ/MVA compared to (30 to 40)kJ/MVA given [39]). This shortcoming eliminates the prospect of this approach in practical systems.

Given the pros and cons (semiconductor loss) of the H-bridge MMC, this chapter explores the unexploited possibilities within the H-bridge MMC circuit structure to enable operation with a DC link voltage that can be varied from *0* to V_{DC}, including operation with zero DC link voltage. Exploitation of these new operating modes offers the following possibilities: the H-bridge MMC DC link can to ride through DC faults without converter blocking; controlled recharge of the DC cables following a temporary DC short circuit fault; and operation in a hybrid DC grid where line commutated HVDC converters and VSC based H-bridge MMCs operate harmoniously, with opportunity to vary the DC link voltage when necessary. To demonstrate the possibility of the H-bridge MMC in HVDC applications, the system simulations that demonstrate operation with variable DC link voltage, survival from a permanent DC fault and controlled DC cables recharging from a temporary DC fault are investigated. This chapter also provided detailed discussion of the different H-bridge MMC operating modes and their potential uses in DC transmission systems.

6.2 Three-phase H-bridge MMC and modulation strategy

Figure 6-1 shows a three-phase MMC with two H-bridge cells per arm. Capacitor C_m and the switching devices of each cell support $½V_{DC}$ (V_{DC} is the input dc link voltage) during normal operation and transient over-voltages during network disturbances. Therefore, each arm must be capable of blocking the full DC link voltage V_{DC}. Unlike the unipolar cells of the half-bridge MMC, each bipolar cell of the H-bridge MMC can generate three voltage levels $\pm½V_{DC}$ and 0. This allows the cell capacitors of the H-bridge MMC to be inserted in the same or opposite polarities ro the DC link voltage (added or subtracted from DC link voltage V_{DC}) to generate different voltage levels at the converter output poles '*a*', '*b*' and '*c*' relative to the notional supply mid-point.

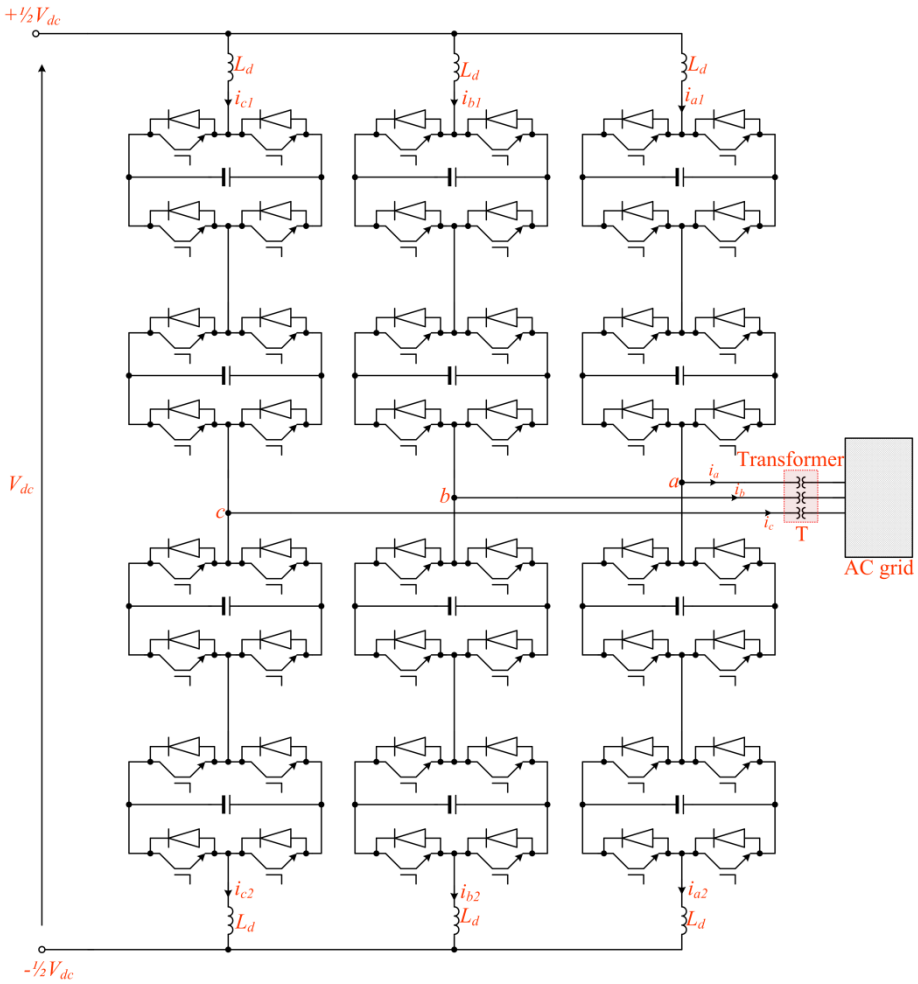


Figure 6-1. A three-phase H-bridge MMC with two cells per arm

Figure 6-2 shows the PWM strategy used for controlling the three-phase H-bridge MMC. Based on the analysis in Section 5.2, consider phase *a* as an example, the upper and lower arm modulation functions are described as $v_{a1}=½V_{DC}(m_d+m_a)$ and $v_{a2}=½V_{DC}(m_d-m_a)$, $m_a=M\sin\omega t$ and $-1\leq m_d\leq 1$ where M is a fixed modulation index and m_d is the adjustable DC offset. As the DC link voltage is regulated around its rating, $0\leq v_{a1}/V_{DC}\leq 1$ and $0\leq v_{a2}/V_{DC}\leq 1$ as m_d will be regulated around 1. In this operating mode (buck mode), voltage levels at converter output poles are generated by insertion of the full-bridge cell capacitors in an opposing polarity to that of the DC link voltage (subtractive states). In this mode, insertion of the cell capacitors with the same polarity as the DC link (additive states) is permissible only during intermediate voltage levels to enhance cell capacitor voltage balancing. When DC link voltage is reduced below the peak of the line-to-line voltage, H-bridge MMC operates in boost mode. In this mode, insertion of the H-bridge cell capacitors with

the same polarities as that of the DC link voltage (additive states) is used so that to allow the cell capacitors of the converter arms to be used as a virtual DC link, provided the sum cell capacitor voltages of each arm is regulated at rated voltage (even though when the DC link is suppressed to zero as happens during DC side fault). With the modulation strategy depicted in Figure 6-2 H-bridge MMC can exchange both active and reactive powers with the grid in buck and boost modes. Nonetheless, when the DC link voltage is suppressed to zero, injection of the active power into grid will lead to discharge of the cell capacitors, therefore, active power command must be reduced to zero (allowing H-bridge MMC to operate as double-star static synchronous compensator). Notice that as DC link voltage reduces modulation function DC component m_d also decreases, allowing normalized version of the modulation functions of the upper and lower arms to cross the time axis to negative, and the time spent at negative represents the period given cell capacitor need to be reversed (added to dc link voltage). As proposed in Section 5.2, Figure 6-3 shows the key per phase control loop that adjusts m_d, and regulates cell capacitor voltages of the upper and lower arms and common-mode current i_d. This control loop plays an important role during dc side fault as it restraints the magnitude of the fault current each converter arm may experience. Additionally, it eliminates the second harmonics current from converter arms as tries to regulate the voltage across the upper and lower arms as depicted in Figure 6-3.

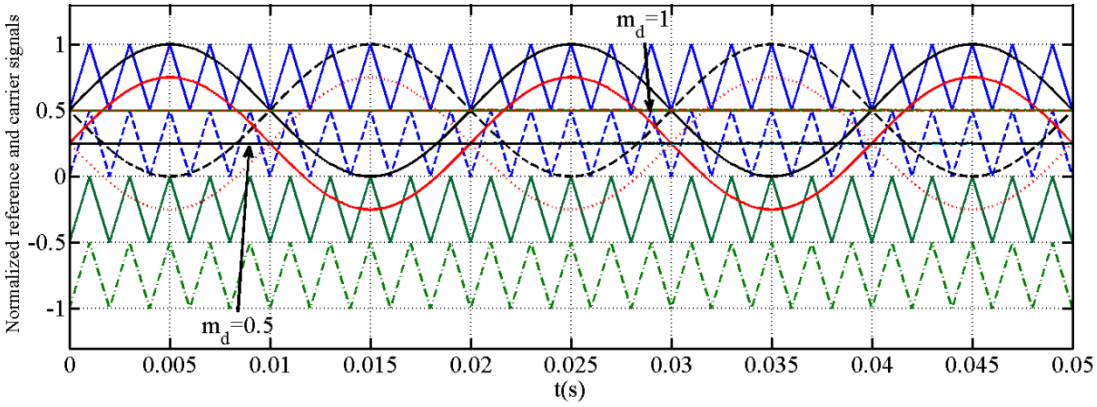


Figure 6-2. illustration of the H-bridge MMC pulse width modulation strategy

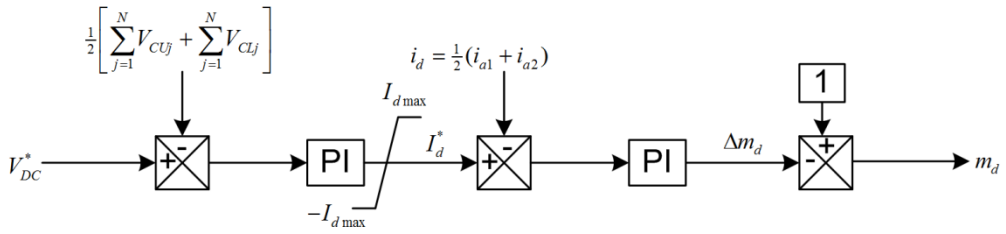


Figure 6-3. Per phase control for m_d adjustment (common mode current control)

6.3 Analysis and control scheme of the back to back H-bridge MMC DC transmission system

Based on the operational principle in Section 5.2 and modulation index in Section 6.1, a control strategy for a back to back DC transmission system with H-bridge MMC is proposed in this section. The system allows DC link fault ride-through and post-fault self-recovery without converter blocking or a DC circuit breaker while still maintaining cell capacitor voltages at the rated value to provide voltage support to the grid. Furthermore, the control strategy allows the |H-bridge MMC to exchange active power with the AC grid with variable DC link voltage (theoretically, from 0 to rated V_{DC}).

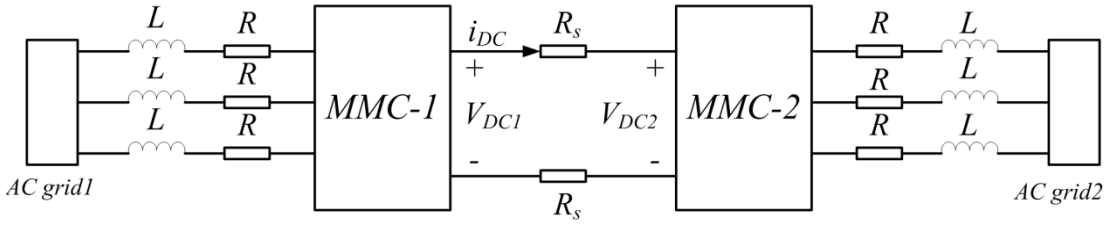


Figure 6-4. Back to back DC transmission system with H-bridge MMCs

Figure 6-4 shows the back to back DC transmission system with H-bridge MMCs at the AC terminals. H-bridge MMC-1 is operated as the DC link voltage regulator (DVR) to maintain the DC link voltage at the rated value and to transfer power from AC grid1 to the DC link. H-bridge MMC-2 is operated as an active power regulator (APR) to control the active power injected into AC grid2 from the DC link. L and R donate the interfacing inductance or series impedance of the interfacing transformer of each phase while R_s represent the DC link cable resistance.

The control loop in Figure 6-5 aims to control the grid currents, regulate the DC link voltage and determine the active power transferred to the grid by using a phase lock loop (PLL) and a *dqo* controller. From equation 5.3, the relationship between the

three-phase injected grid current and the grid voltage at H-bridge MMC-1 AC terminal, can be described as:

$$\begin{aligned}\frac{di_{a1}}{dt} &= -R/L\, i_{a1} + \frac{v_{a1} - v_{a1g}}{L} \\ \frac{di_{b1}}{dt} &= -R/L\, i_{b1} + \frac{v_{b1} - v_{b1g}}{L} \\ \frac{di_{c1}}{dt} &= -R/L\, i_{c1} + \frac{v_{c1} - v_{c1g}}{L}\end{aligned} \tag{6.1}$$

where i_{a1}, i_{b1} and i_{c1} donate the injected grid currents, v_{a1}, v_{b1} and v_{c1} are the H-bridge MMC-1 AC terminal voltages relative to the virtual mid-point of the DC link, and v_{a1g}, v_{b1g} and v_{c1g} represent the voltages of AC grid1. Similarly, the relationship between the output grid currents and grid voltages at H-bridge MMC-2 AC terminals can be written as:

$$\begin{aligned}\frac{di_{a2}}{dt} &= -R/L\, i_{a2} + \frac{v_{a2} - v_{a2g}}{L} \\ \frac{di_{b2}}{dt} &= -R/L\, i_{b2} + \frac{v_{b2} - v_{b2g}}{L} \\ \frac{di_{c2}}{dt} &= -R/L\, i_{c2} + \frac{v_{c2} - v_{c2g}}{L}\end{aligned} \tag{6.2}$$

where i_{a2}, i_{b2} and i_{c2} donate the output grid currents, v_{a2}, v_{b2} and v_{c2} donate the H-bridge MMC-2 AC terminal voltages relative to the virtual mid-point of the DC link, and v_{a2g}, v_{b2g} and v_{c2g} represent the AC grid2 voltages.

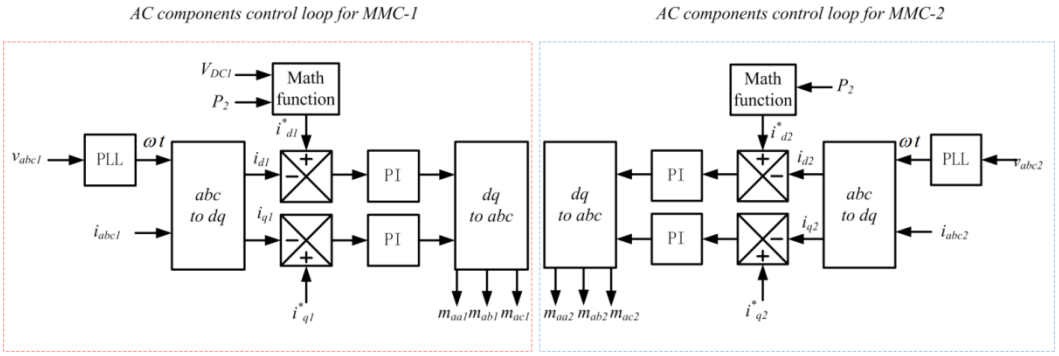


Figure 6-5. Three-phase AC component control

Assuming the AC grid voltages of MMC-1 and MMC-2 are identical, v_{a2g}=v_{a1g}= v_{ag}, v_{b2g}=v_{b1g}= v_{bg} and v_{c2g}=v_{c1g}= v_{cg}, the parameters in the *abc* frame can be transferred into *dqo* frame with:

$$i_{qdo} = K\, i_{abc}$$
$$v_{qdo} = K\, v_{abc} \tag{6.3}$$

where i_{dqo} and v_{dqo} represent the matrix of transferred current and voltage vectors in the *dqo* frame, i_{abc} and v_{abc} is the original grid current matrix and voltage matrix in *abc* frame, *K* is:

$$K = \sqrt{\tfrac{2}{3}}\begin{bmatrix} \cos\omega t & \cos(\omega t - \tfrac{2}{3}\pi) & \cos(\omega t + \tfrac{2}{3}\pi) \\ \sin\omega t & \sin(\omega t - \tfrac{2}{3}\pi) & \sin(\omega t + \tfrac{2}{3}\pi) \\ \tfrac{1}{\sqrt{2}} & \tfrac{1}{\sqrt{2}} & \tfrac{1}{\sqrt{2}} \end{bmatrix} \tag{6.4}$$

Thus equations (6.2) and (6.1) can be expressed in the *dq* synchronous reference frame, assuming the *d*-axis is aligned with v_{ag}:

$$\begin{bmatrix} \frac{di_{d1}}{dt} \\ \frac{di_{q1}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 \\ 0 & -\frac{R}{L} \end{bmatrix}\begin{bmatrix} i_{d1} \\ i_{q1} \end{bmatrix} + \begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix}\begin{bmatrix} i_{d1} \\ i_{q1} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix}\begin{bmatrix} v_{d1} - v_{dg1} \\ v_{q1} - v_{qg1} \end{bmatrix} \tag{6.5}$$

$$\begin{bmatrix} \frac{di_{d2}}{dt} \\ \frac{di_{q2}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 \\ 0 & -\frac{R}{L} \end{bmatrix}\begin{bmatrix} i_{d2} \\ i_{q2} \end{bmatrix} + \begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix}\begin{bmatrix} i_{d2} \\ i_{q2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix}\begin{bmatrix} v_{d2} - v_{dg2} \\ v_{q2} - v_{qg2} \end{bmatrix} \tag{6.6}$$

where ω is the grid voltage angular frequency, equations (6.5) and (6.6) describe the dynamics of the H-bridge MMCs AC side variables in terms of their *dq* frame components. They can be used for control design of the fundamental current control loop. Let:

$$u_{dk} = \omega i_{qk} + \frac{1}{L} v_{dk} - v_{dgk} \quad k = 1, 2 \tag{6.7}$$

$$u_{qk} = -\omega i_{dk} + \frac{1}{L} v_{qk} - v_{qgk} \quad k = 1, 2 \tag{6.8}$$

Therefore equations (6.5) and (6.6) can be simplified to:

$$\frac{di_{dk}}{dt} = -\frac{R}{L} i_{dk} + u_{dk} \tag{6.9}$$

$$\frac{di_{qk}}{dt} = -\frac{R}{L} i_{qk} + u_{qk} \tag{6.10}$$

Based on equation (6.9), the *d* components of H-bridge MMC-*k*'s grid currents can be regulated. u_{dk} will be estimated from the proportional-integral controllers by

forcing the *d* components of the AC currents the converters exchange with the grids, to follow the given reference values as:

$$u_{dk} = \nu_{pk}(i_{dk}^{*} - i_{dk}) + \nu_{ik}\int (i_{dk}^{*} - i_{dk})dt \tag{6.11}$$

where ν_{pk} and ν_{ik} represent the proportional and integral gains. Replacing the integral part of (6.11) by γ and manipulation of (6.9), the state space equations that can be used for selection of the i_{dk} component controller gains ν_{pk} and ν_{ik} is obtained.

$$\frac{d}{dt}\begin{bmatrix} i_{dk} \\ \gamma \end{bmatrix} = \begin{bmatrix} -(R+\nu_{pk})/L & 1/L \\ -\nu_{ik} & 0 \end{bmatrix}\begin{bmatrix} i_{dk} \\ \gamma \end{bmatrix} + \begin{bmatrix} \nu_{pk}/L \\ \nu_{ik} \end{bmatrix} i_{dk}^{*} \tag{6.12}$$

On this basis, the damping factor and natural frequency can be set according to the desired control objectives. Similarly, u_{qk} can be estimated from the proportional-integral controllers:

$$u_{qk} = \chi_{pk}(i_{qk}^{*} - i_{qk}) + \chi_{ik}\int (i_{qk}^{*} - i_{qk})dt \tag{6.13}$$

where χ_{pk} and χ_{ik} represent the proportional and integral gains. Replace the integral part of (6.13) by τ and manipulation of (6.10), the state space that can be used for selection of the i_{qk} component controller gains χ_{pk} and χ_{ik} is obtained.

$$\frac{d}{dt}\begin{bmatrix} i_{qk} \\ \tau \end{bmatrix} = \begin{bmatrix} -(R+\chi_{pk})/L & 1/L \\ -\chi_{ik} & 0 \end{bmatrix}\begin{bmatrix} i_{qk} \\ \tau \end{bmatrix} + \begin{bmatrix} \chi_{pk}/L \\ \chi_{ik} \end{bmatrix} i_{qk}^{*} \tag{6.14}$$

From (6.14), the damping factor and natural frequency can be set correspondingly. Based on this discussion, the block diagrams that summarize the *dq* current component controllers of the H-bridge MMCs are developed.

For maximum active power transmission, the grid currents at both AC terminals of the H-bridge MMCs are phase synchronized with the grid voltages. Thus the reference of i_{qk} for the *dq* current components controller of H-bridge's MMC-1 and MMC-2 is set to be zero.

The power transferred through each H-bridge MMC can be described as:

$$V_{DC1} i_{DC} = (\mathrm{v}_d\, i_{d1} + \mathrm{v}_q\, i_{q1}) \tag{6.15}$$

$$V_{DC2} i_{DC} = (\mathrm{v}_d\, i_{d2} + \mathrm{v}_q\, i_{q2}) \tag{6.16}$$

While V_{DC1} and V_{DC2} are the DC link voltages at MMC-1 side and MMC-2 side, i_{DC} is the DC link current. Based on this analysis, the system is operated at unity power factor with PLL control, $i_{qk}=0$, then equations (6.15) and (6.16) can be derived as:

$$V_{DC1} i_{DC} = \mathrm{v}_d \; i_{d1} = P_1 \tag{6.17}$$

$$V_{DC2} i_{DC} = \mathrm{v}_d \; i_{d2} = P_2 \tag{6.18}$$

whree P_1 and P_2 are the powers conducted by H-bridge MMC-1 and H-bridge MMC-2. Ignoring the AC component of i_{DC}, the relationship for V_{DC1} and V_{DC2} is:

$$V_{DC2} = V_{DC1} - 2R_s i_{DC} \tag{6.19}$$

Substituting (6.18) into (6.19):

$$V_{DC2}^2 + 2R_s P_2 - V_{DC1} V_{DC2} = 0 \tag{6.20}$$

Disregarding the negative solution of equation (6.20), the DC link voltage for MMC-2 is:

$$V_{DC2} = \frac{1}{2}\left(V_{DC1} + \sqrt{V^2{}_{DC1} - 8R_s P_2}\right) \tag{6.21}$$

The rated V_{DC1} calculated by equation (6.17) is set to be the voltage reference of the common mode control loop in Figure 6-3 for H-bridge MMC-1 and is maintained constant while the real DC link voltage varies over a wide range (from 0 to rated V_{DC}). Meanwhile, voltage reference V_{DC2} of common mode control loop for H-bridge MMC-2 is determined by the rated value of V_{DC1} and the transient power transferred from H-bridge MMC-2 to its AC grid. Thus cell capacitor voltages are stabilized and the DC link current is regulated by the difference between V_{DC1} and V_{DC2} over the full range of DC link voltages regardless of the AC grid voltage.

Based on equations (6.17), (6.18) and (6.21), the relationship between the *d* component of the grid current to H-bridge MMC-1 and the DC side voltage V_{DC1}, is:

$$i_{d1}^* = \frac{2V_{DC1} \cdot P_2}{v_d (V_{DC1} + \sqrt{V^2{}_{DC1} - 8R_s P_2})} \tag{6.22}$$

i_{d1}^* is set to be the reference of the transferred *d* axis component of the grid current to H-bridge MMC-1, while i_{d2}^* calculated in equation (6.18) is the reference of the *d* component of the grid current from H-bridge MMC-2. From this definition, the AC components of the modulating signals in ABC frame for each H-bridge MMC can be obtained by transformation of u_{dk} and u_{qk} from the *dq* frame to the *abc* frame:

$$\begin{bmatrix} m_{aak} \\ m_{abk} \\ m_{ack} \end{bmatrix} = \begin{bmatrix} \cos\omega t & \sin\omega t \\ \cos(\omega t - \frac{2}{3}\pi) & \sin(\omega t - \frac{2}{3}\pi) \\ \cos(\omega t + \frac{2}{3}\pi) & \sin(\omega t + \frac{2}{3}\pi) \end{bmatrix} \begin{bmatrix} u_{dk} \\ u_{qk} \end{bmatrix} \tag{6.23}$$

where *k=1 or 2,* m_{aak}, m_{abk} and m_{ack} represent the AC components of the modulation signals for the phases of H-bridge MMC-k. Modulation references for the upper and lower arm voltages of each phase are determine by the DC components $m_{d1,}$ m_{d2} and the AC components m_{aa1}, m_{ab1}, m_{ac1}, m_{aa2}, m_{ab2} and $m_{ac2.}$ They are exploited to generated SPWM signals with the cell capacitors balancing scheme illustrated in Figure 6-6.

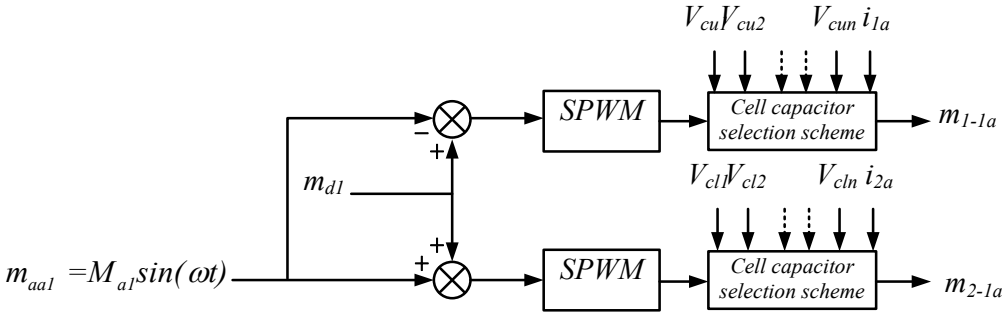


Figure 6-6. Modulation reference waveforms for phase *a* of MMC-1

By exploiting the bi-polar capability of the MMC H-bridge cells and the controller in Figure 6-3 and Figure 6-5, a H-bridge MMC DC transmission system can operate reliably in steady state, and during AC and DC network faults. The significance of the control structure is that it allows the back to back DC transmission system to ride through a DC fault without any uncontrolled inrush current from the AC side, and the DC and AC currents in each converter arm is controlled, even when the DC link collapses. When the DC link voltage is suppressed to zero, as during a typical pole-to-pole DC short circuit fault, the active power the two converters exchange with the grid must be reduced to zero to avoid cell capacitor discharge. The MMC upper and lower arms operate as a two parallel cascaded multilevel converter based STATCOM. This implies that converter blocking is no longer necessary; rather, during a DC fault, the two MMC converters can be operated to provide voltage support to the AC grid. Additionally, the control scheme in Figure 6-3 and Figure 6-5 eliminates the need for a separate controller for suppression of the 2nd harmonic in the MMC arms, because by regulating the cell capacitor voltages, the DC voltage and common current

controllers modulate the dc component of the modulation function m_d in a manner that cancels the 2nd harmonics from the arm currents. Also, the control strategy facilitates H-bridge MMC active power exchange with the AC grid, with a variable DC link.

6.4 Performance evaluation of a back to back H-bridge MMC DC transmission system

This section evaluates the performance of an H-bridge MMC based back-to-back DC transmission system in Figure 6-4 that operates based on the proposed operational scheme, in conjunction with the control system of Figure 6-5 and Figure 6-6. The back-to-back DC transmission system is constructed using power electronics building blocks from the Simpower System library and the modulator block in Figure 6-6 employs sinusoidal PWM with phase disposition carriers, and a cell capacitor selection scheme that relies on cell rotation based on cell capacitor voltage magnitude information, arm currents polarities, and the voltage level to be synthesized.

The objective of this section is to validate the performance of the presented control strategy during normal operation, AC grid fault, DC link voltage polarity reversal and DC link voltage collapse. Table 5-2 summarises system parameters used for medium voltage demonstration in this section (simulation). However, the presented control scheme remains valid for high voltage applications.

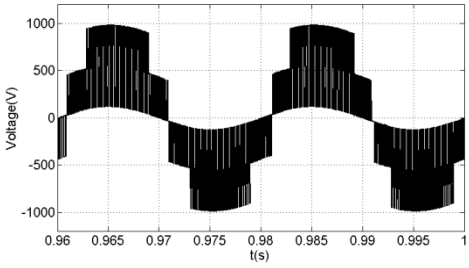
Table 6-1: Simulation parameters

System rating	65kW
Cell Capacitance	4.7mF
Switching frequency	2 kHz
DC link voltage	2kV
Arm inductance	3.3mH
Rated frequency	50Hz
Grid voltage $V_{lp\text{-}p}$	1041V

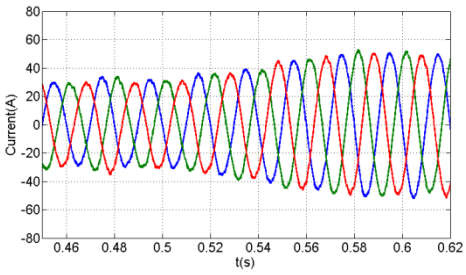
6.4.1 Normal Operation

In normal operation, H-bridge MMC-1 is operated as DC voltage regulator to stabilize the DC link voltage and to maintain the power injected from the AC Grid-1 to DC link at unity power factor. H-bridge MMC-2 is controlled as an active power regulator to inject rated active power to AC Grid-2. Figure 6-7 and Figure 6-8 show simulation results obtained when the power associated with an initial peak current of 30A is exchanged between AC Grid-1 and AC Grid-2 via the H-bridge MMC back to back DC transmission system and the current is increased to 50A at time t=0.5s. Figure 6-7(a) shows converter AC terminal voltage. Figure 6-7(b) shows the three-phase input currents i_{abc1} superimposed over their references i^*_{abc1}, which is determined by the DC side voltage of H-bridge MMC-1 and the required output power of H-bridge MMC-2, as illustrated in the block diagram in Figure 6-5. Figure 6-7(c) and (d) show the common mode current and the upper and lower arm currents of H-bridge MMC-1 phase-*a*, respectively. The common mode current 2nd harmonic components, the upper lower arm currents are significantly suppressed, as explained previously and the dc power flow dynamic response is greatly improved. The DC link voltage plot in Figure 6-7(e) illustrates that the DC voltage is regulated at the rated value. Figure 6-7(f) shows the cell capacitor voltages are controlled around their desired set-point, including when the output current step change is applied.

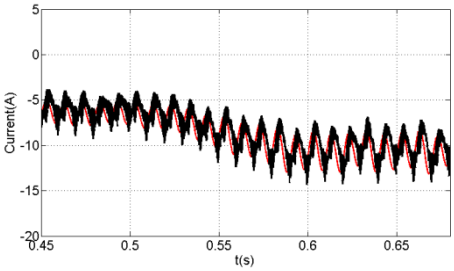
Figure 6-8(a) displays the AC side output voltage of H-bridge MMC-2. Figure 6-8(b) shows that the three-phase currents injects from H-bridge MMC-2 to AC Grid-2 is phase locked with the grid voltage to maintain unity power factor, as described in Figure 6-5. The harmonics of the arm currents and common mode current are suppressed, as illustrated in Figure 6-8(c) and (d), since the control loop for the common mode current is the same as for H-bridge MMC-1. Figure 6-8(e) shows the cell capacitor voltages are regulated around the set point, including at the step change.



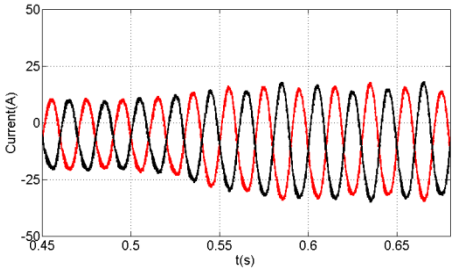
a) MMC-1 AC terminal voltage relative to supply mid-point



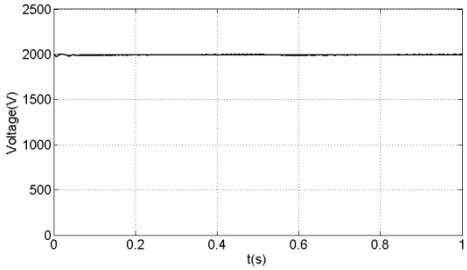
b) Three-phase current waveforms inject from grid to MMC-1 where step change is applied to the peak of the reference current



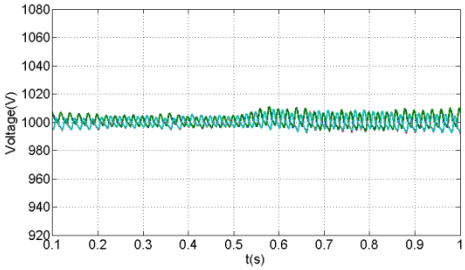
c) Common mode current (i_{dc}=½(i_1+i_2)) of MMC-1 phase a and its reference sets by the DC voltage regulator that controls cell capacitor voltage of the upper and lower arms



d) Upper and lower arm currents zoomed around the instant where step change is applied to the peak of the reference output current(MMC-1 phase *a*)

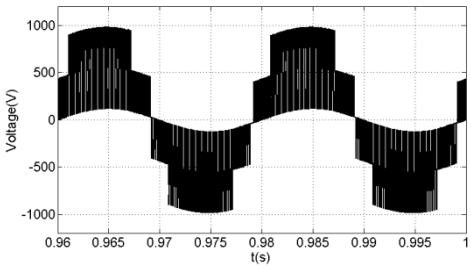


e) DC link voltage V_{DC1}

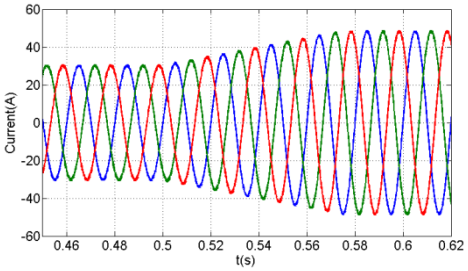


f) Cell capacitor voltage of the upper and lower arms of MMC-1 phase *a*

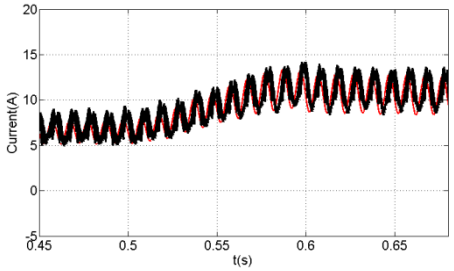
Figure 6-7. Simulation waveforms when three-phase H-bridge MMC-1 is controlled with the control scheme in Figure 6-3 and Figure 6-5, and at t=0.5s, a step change is applied that increases the peak reference current from I_m=20A to 40A.



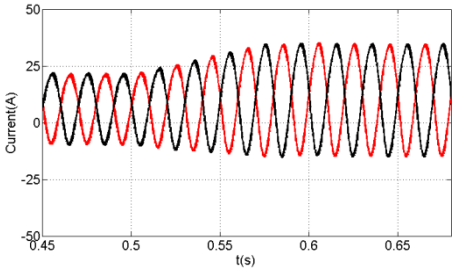
a) MMC-2 AC terminal voltage relative to supply mid-point



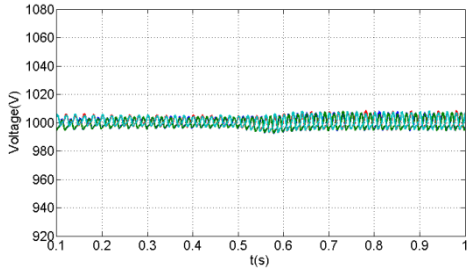
b) Three-phase current waveforms inject from MMC-2 to grid where step change is applied to the peak of the reference current



c) Common mode current (i_{dc}=½(i_1+i_2)) of MMC-2 phase *a* and its reference sets by the DC voltage regulator that controls cell capacitor voltage of the upper and lower arms



d) Upper and lower arm currents zoomed around the instant where step change is applied to the peak of the reference output current(MMC-2 phase *a*)

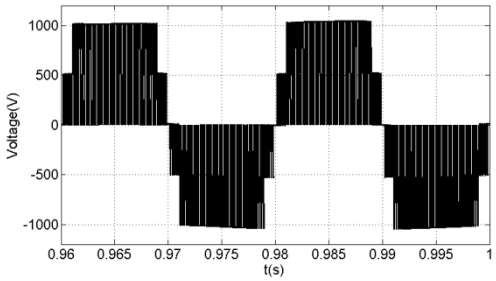


e) Cell capacitor voltage of the upper and lower arms of MMC-2 phase *a*

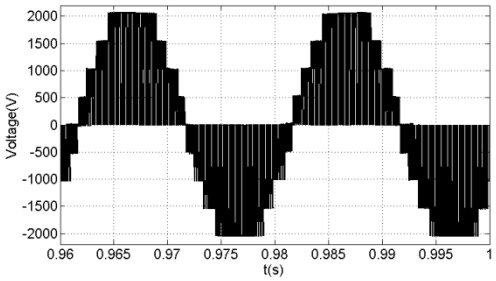
Figure 6-8. Simulation waveforms of the three-phase H-bridge MMC-2 is controlled with the control scheme in Figure 6-3 and Figure 6-5, and at t=0.5s a step change is applied that increases the peak reference current from I_m=20A to 40A.

6.4.2 Normal operation with third harmonic injection

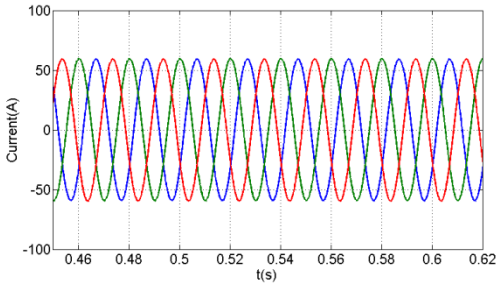
To extend the modulation linear range beyond unity for SPWM, a third harmonic injection method can be implemented into the proposed control scheme, while maintaining the AC components of arm currents sinusoidal. For illustration of this possibility, a two-cell per arm version of an H-bridge MMC is simulated when 3rd harmonic injection is used, and the modulation index is 1.15. Figure 6-9 shows that the use of 3rd harmonic injection does not interfere with the performance of the proposed scheme. Figure 6-9(a) and (b) respectively display the output phase and line voltages when the modulation index is m=1.15. Figure 6-9(c) shows the three-phase currents the H-bridge MMC injects into the AC side, with good quality arm currents and common mode current, as displayed in Figure 6-9(d) and (e). Cell capacitor voltages are balanced and regulated around the rated value as shown in Figure 6-9(f).



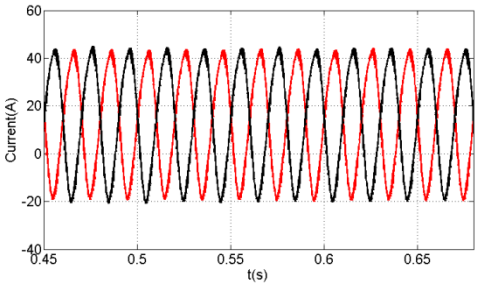
a) AC terminal voltage relative to supply mid-point of H-bridge MMC phase *a*



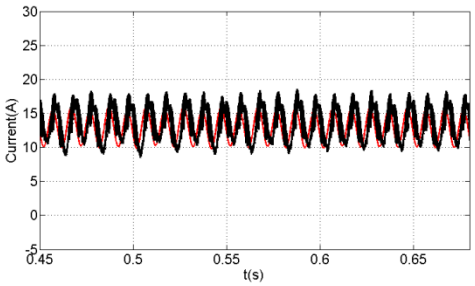
b) Output Line-to-line voltage of H-bridge MMC



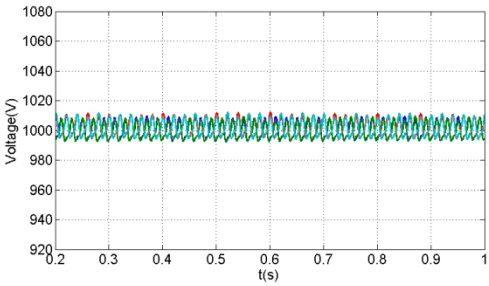
c) Output current waveforms



d) Upper and lower arm currents of H-bridge MMC phase *a*



e) Common mode current (i_{dc}=½(i_1+i_2)) of MMC-1 phase a and its reference sets by the DC voltage regulator



f) Cell capacitor voltage of the upper and lower arms of MMC-1 phase *a*

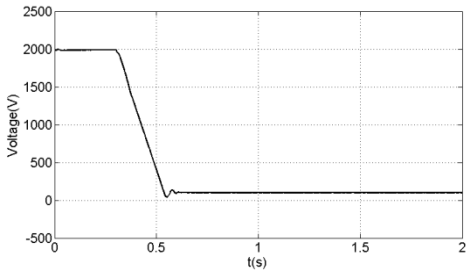
Figure 6-9. Waveforms demonstrate operation of the H-bridge MMC with extended modulation index m=1.15, using third harmonic injection.

6.4.3 DC fault emulation

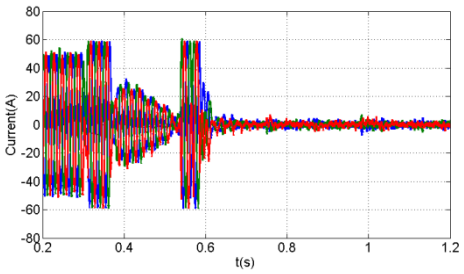
The dynamic response of the DC transmission system and performance of the control strategy are studied when the DC link voltage is suppressed as during a DC fault. For this study, the DC link is discharged by H-bridge MMC-1 to simulate the DC short circuit fault at t=0.3s, and the reference grid currents for the system AC terminals are reduced to zero immediately when the fault is applied and remains at zero during the entire fault period. The H-bridge MMCs are operated independently to suppress inrush current from each AC side and to prevent power flow between the DC link and the grid when DC link voltage collapsed. Again the MMCs can provide voltage support to the AC grid during the fault.

Figure 6-10(a), (b) and (c) show system DC link voltage and AC terminal currents of MMC-1 and MMC-2 during a permanent pole-to-pole DC short circuit fault. Uncontrolled AC inrush current is avoided with the control scheme in Figure 6-5 and Figure 6-3; MMC-1 is operated to discharge DC link stray capacitance to minimize the impact during the decreasing DC link voltage. When the DC link voltage collapses to zero, the H-bridge MMCs cell polarities have been reversed to provide a

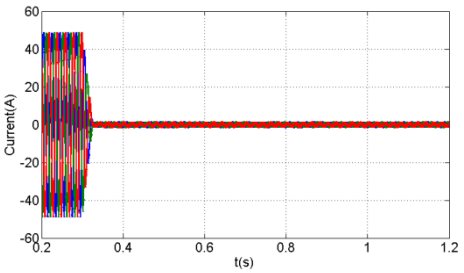
virtual DC voltage identical to the pre-fault situation. Thus, converter remains controllable as the relationship between its DC link, modulation index and AC voltage remain intact. Figure 6-10(d) and (e) show that the arm currents are under control when the DC link voltage completely collapses. Figure 6-10(f) and (g) display that the common mode currents are regulated with no inrush current injected into the DC link. Figure 6-10(h) and (i) show the voltage balance of the cell capacitors, of both H-bridge MMCs, is maintained at both DC terminals even at zero DC link voltage. Based on the simulation results, the rapid rise of AC and DC currents in the converter arms, and inrush AC current injected into the DC link, have been restrained. Thus, risk of device failure is avoided, without the need for the converter blocking advocated in [4, 40-43].



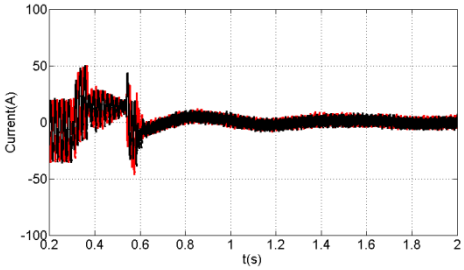
a) DC link voltage



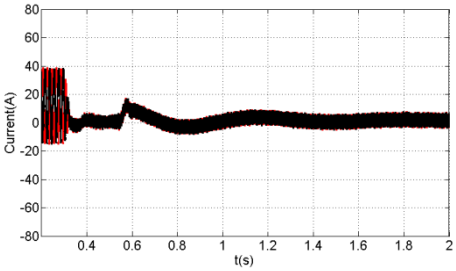
b) Three-phase AC terminal current waveforms of MMC-1



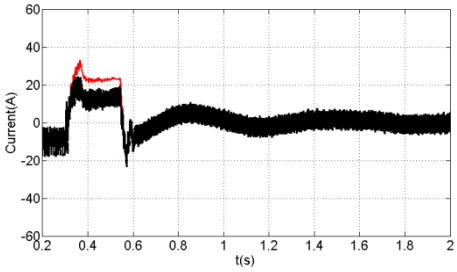
c) Three-phase AC terminal current waveforms of MMC-2



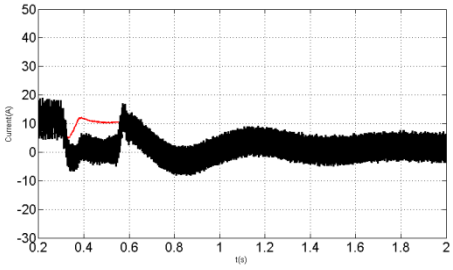
d) Upper and lower arm currents zoomed around the DC fault period of MMC-1 phase a



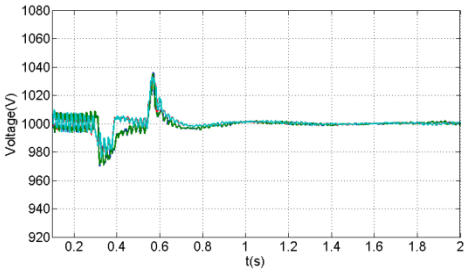
e) Upper and lower arm currents zoomed around the DC fault period of MMC-2 phase *a*



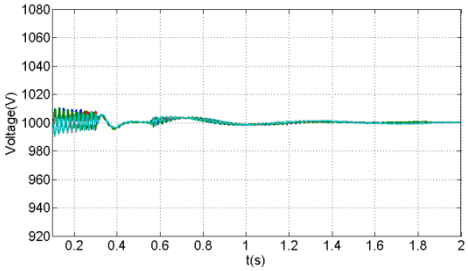
f) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-1 phase *a*



g) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-2 phase *a*



h) Cell capacitor voltages of MMC-1 phase *a*

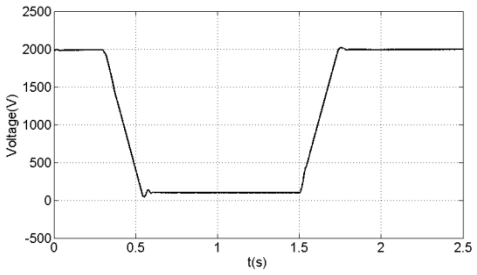


i) Cell capacitor voltages of MMC-2 phase *a*

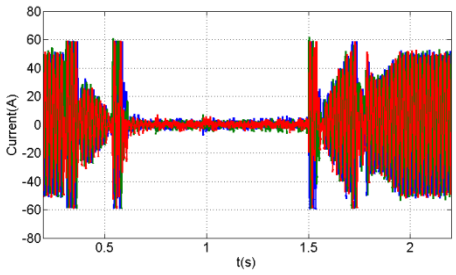
Figure 6-10. Waveforms illustrate the effectiveness of the control scheme during a permanent pole-to-pole DC short circuit fault in restraining AC and DC currents in both arms of H-bridge MMCs, and elimination of the uncontrolled in-feed current into the DC link from the grid, without converter blocking

6.4.4 DC fault ride-through with post-fault recovery

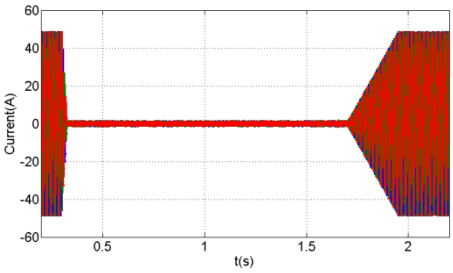
The case of a temporary DC fault is assessed where the DC link is discharged by H-bridge MMC-1 at t=0.3s, and recovered at t=1.5s. H-bridge MMC-1 re-establishes the DC link voltage by injecting restrained charging current to the DC link capacitance from AC Grid-1 in the period t=1.5s to t=1.8s. The results for the temporary DC short circuit fault are displayed in Figure 6-11**.** Figure 6-11(a), (b) and (c) show that the system DC link voltage recovers quickly to normal operation when the fault is cleared and the AC terminal currents of MMC-1 and MMC-2 are controlled. Figure 6-11(d), (e), (f) and (g) illustrate the arm and common mode currents are regulated throughout the whole period. Cell capacitor voltages are balanced in Figure 6-11(h) and (i). The waveforms presented are in line with the previous case that considered a permanent DC fault, except the system recovers when the fault is cleared, with current and voltage stresses in H-bridge MMC devices and DC link are controlled.



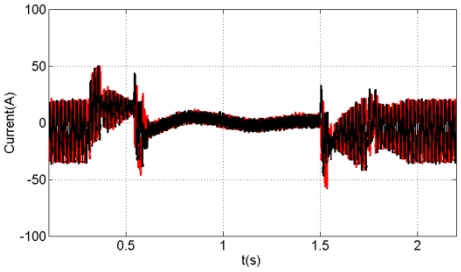
a) DC link voltage



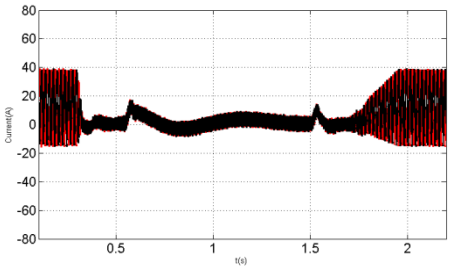
b) Three-phase AC terminal current waveforms of MMC-1



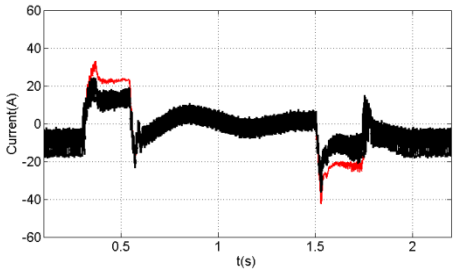
c) Three-phase AC terminal current waveforms of MMC-2



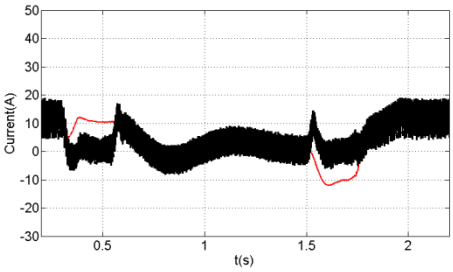
d) Upper and lower arm currents zoomed around the DC fault period of MMC-1 phase a



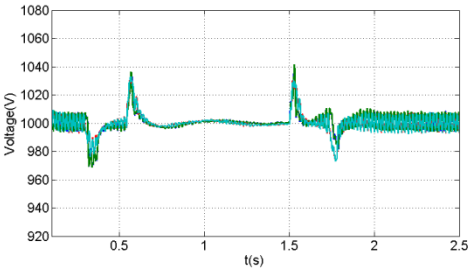
e) Upper and lower arm currents zoomed around the DC fault period of MMC-2 phase *a*



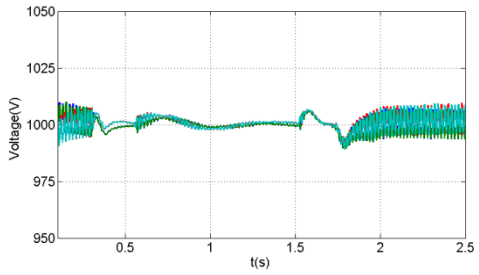
f) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-1 phase *a*



g) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-2 phase *a*



h) Cell capacitor voltages of MMC-1 phase *a*

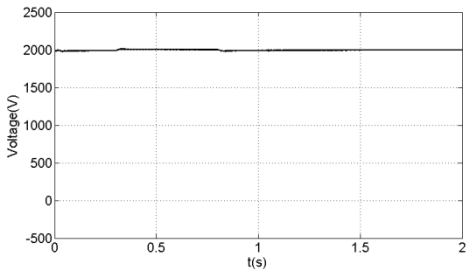


i) Cell capacitor voltages of MMC-2 phase *a*

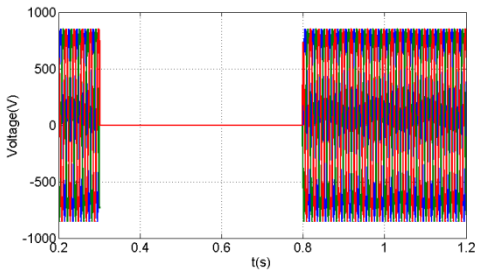
Figure 6-11. Waveforms illustrate the control scheme, during a temporary DC short circuit fault, restraining AC and DC currents in both arms of the H-bridge MMCs, and elimination of the uncontrolled in-feed current to the DC link from the grid, without converter blocking

6.4.5 AC fault emulation

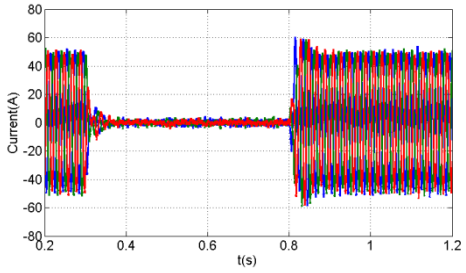
To evaluate the transient performance of the H-bridge MMC back to back DC transmission system, a three-phase AC fault is applied on AC grid2 at t=0.3s and cleared at t=0.8s. The results are displayed in Figure 6-12. The control scheme suppresses the grid currents at two AC terminals during three-phase fault and recovers quickly while the cell capacitor voltages are balanced and common mode currents at both H-bridge MMCs are regulated. This feature may facilitate the H-bridge MMC-2 to provide voltage support and reactive power to AC grid2 without the risk of over-current in the switching devices. Figure 6-12(a) shows the DC link voltage is maintained stable while the AC grid2 voltage is suppressed to zero in Figure 6-12(b). The grid currents of both bridges are restrained and only transfer reactive power between AC grid1 and AC grid2 in Figure 6-12(c) and (d). Figure 6-12(e), (f), (g) and (h) illustrate the arm currents and common mode currents of both H-bridge MMCs are tightly controlled. Voltages across the cell capacitors are shown in Figure 6-12(i) and (j).



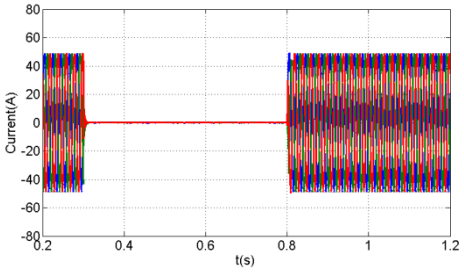
a) DC link voltage



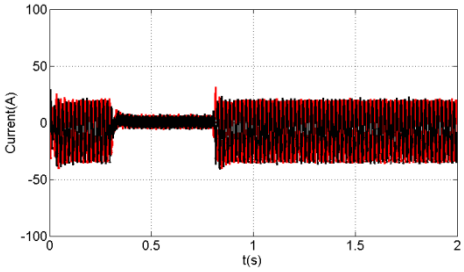
b) Three-phase AC voltage waveforms of AC grid2



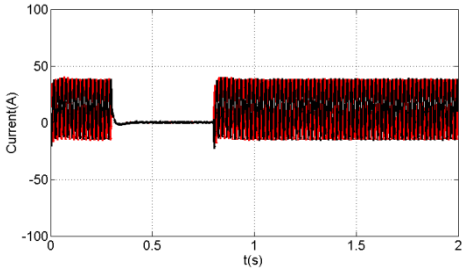
c) Three-phase AC terminal current waveforms of MMC-1



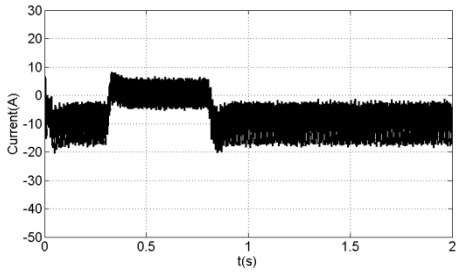
d) Three-phase AC terminal current waveforms of MMC-2



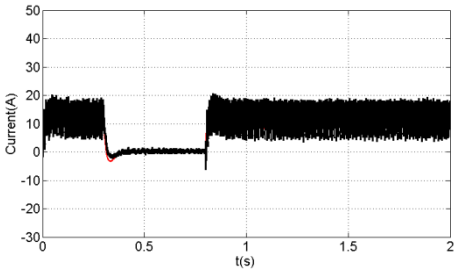
e) Upper and lower arm currents zoomed around the AC fault period of MMC-1 phase *a*



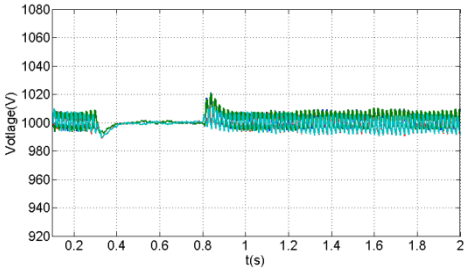
f) Upper and lower arm currents zoomed around the AC fault period of MMC-2 phase a



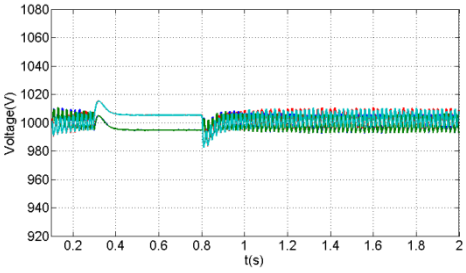
g) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-1 phase *a*



h) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-2 phase *a*



i) Cell capacitor voltages of MMC-1 phase *a*

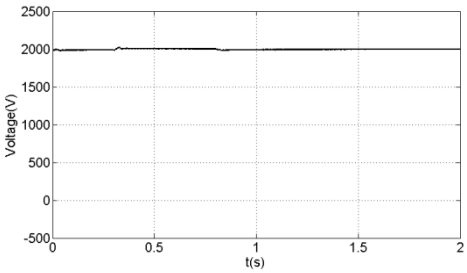


j) Cell capacitor voltages of MMC-2 phase *a*

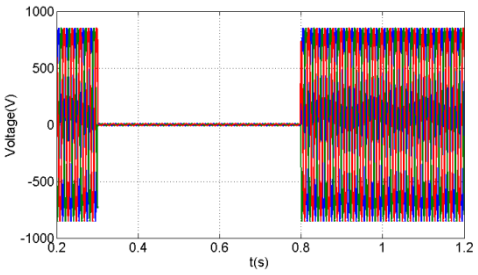
Figure 6-12. Waveforms illustrate control scheme performance during a temporary three-phase AC grid2 fault, where the AC and DC currents in upper and lower arms of H-bridge MMCs are restrained

Figure 6-13 illustrates when the three-phase fault is applied to AC grid1 at t=0.3s and cleared at t=0.8s. In this case, H-bridge MMC-1 is operated to provide voltage support to AC grid1 while H-bridge MMC-2 is operated to stabilize the DC link

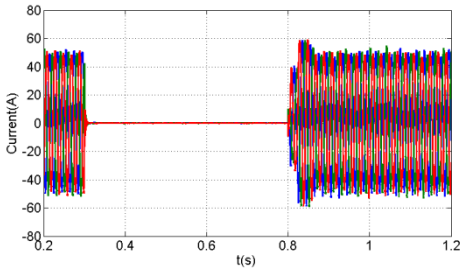
voltage by transferring power between AC grid2 and the DC link. Similar to the AC grid2three-phase fault, the DC link voltage is stabilized and grid currents are minimised in Figure 6-13(a), (b), (c) and (d). The arm currents and common mode currents are suppressed; only providing energy support to maintain the cell capacitor voltages at the rated values in Figure 6-13(e), (f), (g), (h), (i) and (j).



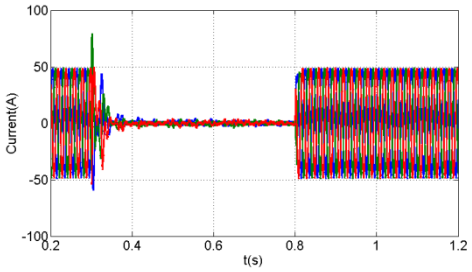
a) DC link voltage



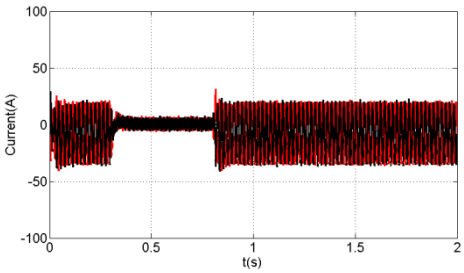
b) Three-phase AC voltage waveforms of AC grid1



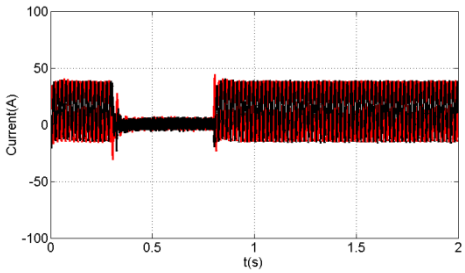
c) Three-phase AC terminal current waveforms of MMC-1



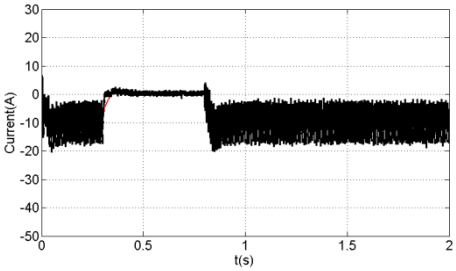
d) Three-phase AC terminal current waveforms of MMC-2



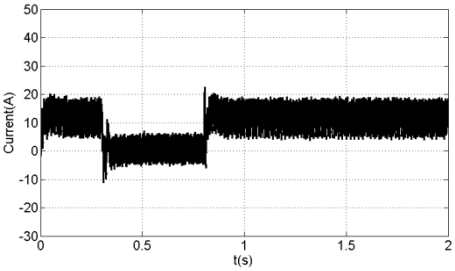
e) Upper and lower arm currents zoomed around the AC fault period of MMC-1 phase *a*



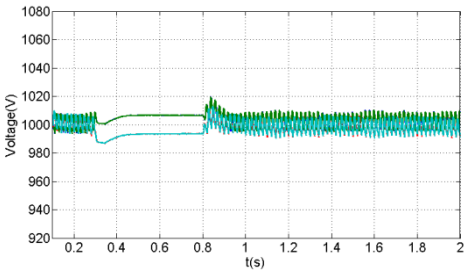
f) Upper and lower arm currents zoomed around the AC fault period of MMC-2 phase *a*



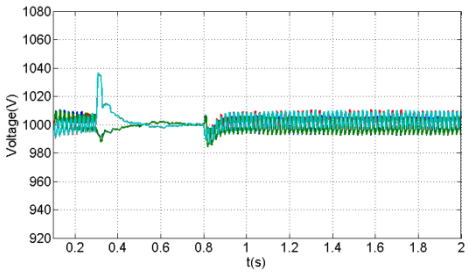
g) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-1 phase *a*



h) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-2 phase *a*



i) Cell capacitor voltages of MMC-1 phase *a*

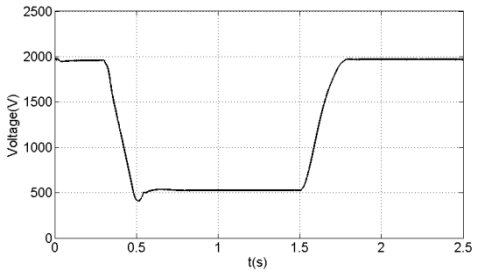


j) Cell capacitor voltages of MMC-2 phase *a*

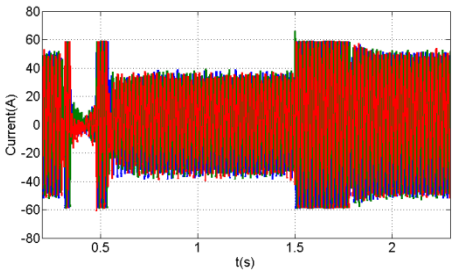
Figure 6-13. Waveforms illustrate the effectiveness of the control scheme during a temporary three-phase AC grid1 fault, where the AC and DC currents in upper and lower arms of H-bridge MMCs are restrained

6.4.6 Active power injection into the AC grid when the H-bridge MMC operates in a boost mode during DC voltage sag

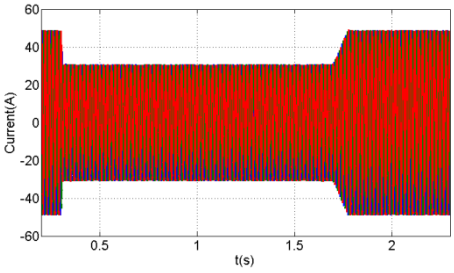
Figure 6-14 displays the case when the DC link voltage collapsed to 30% at t=0.5s and recovers to rated value at t=1.5s. The magnitude of the grid current is suppressed to 60% when the fault is applied and restored to the pre-fault level at t=1.7s in Figure 6-14 (b) and (c). The peak value of arm currents and common mode current of each phase of both H-bridges are regulated and the quick dynamic response of the control loop restrains the common mode current overshoot in Figure 6-14 (d), (e), (f) and (g). Cell capacitor voltages are balanced by utilizing the common mode control loop in Figure 6-14(h) and (i).



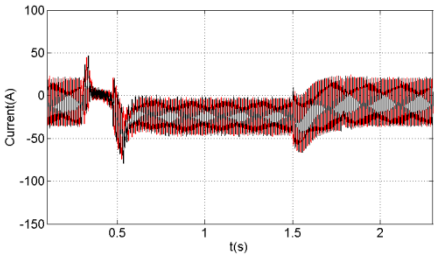
1. DC link voltage



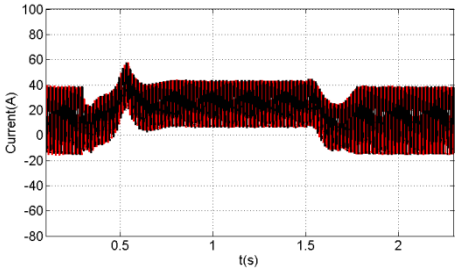
2. Three-phase AC terminal current waveforms of MMC-1



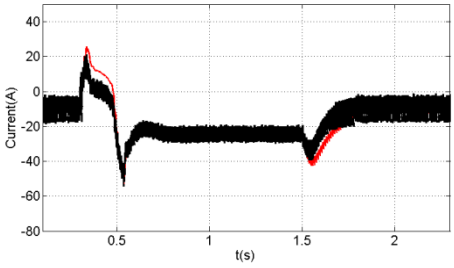
3. Three-phase AC terminal current waveforms of MMC-2



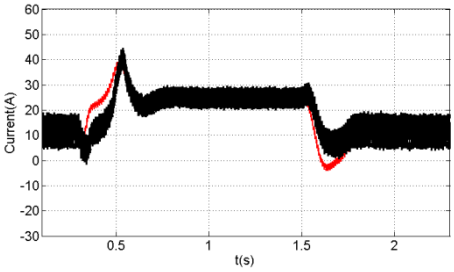
4. Upper and lower arm currents zoomed around the DC fault period of MMC-1 phase *a*



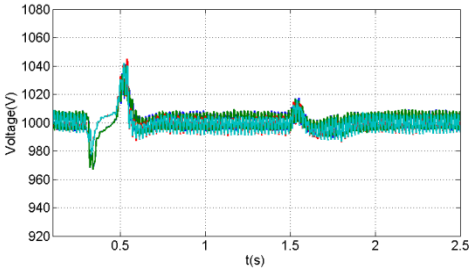
5. Upper and lower arm currents zoomed around the DC fault period of MMC-2 phase *a*



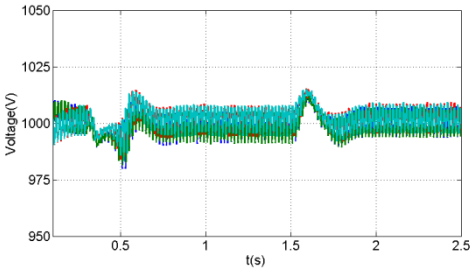
6. Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-1 phase *a*



7. Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-2 phase *a*



8. Cell capacitor voltages of MMC-1 phase *a*



9. Cell capacitor voltages of MMC-2 phase *a*

Figure 6-14. Simulation waveforms during a temporary DC fault while the DC link voltage is reduced to 30% and the grid current magnitude is decreased to 60%

6.5 Performance evaluation of the back to back H-bridge MMC HVDC transmission system

This section evaluates the performance of an H-bridge MMC based back to back HVDC system that operates based on the control scheme of Figure 6-5 and Figure

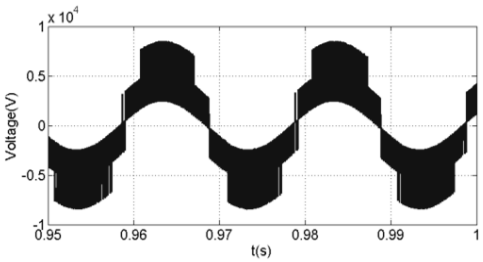
6-6. Detailed switching models are established with Matlab Simulink to validate HVDC system performance during normal operation, an AC grid fault, DC link voltage polarity reversal, and DC link voltage collapse. Table **5-2** summarises the simulation system parameters used for high voltage demonstration in this section.

Table 6-2: Simulation parameters

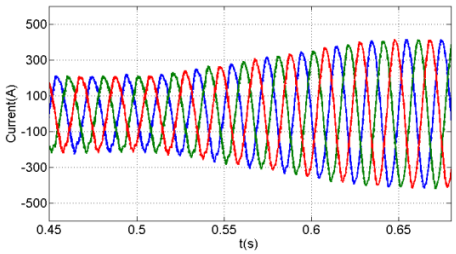
System rating	7MW
Cell Capacitance	4.7mF
Switching frequency	2 kHz
DC link voltage	18kV
Arm inductance	3.3mH
Rated frequency	50Hz
Grid voltage $V_{lp\text{-}p}$	7360V

6.5.1 Normal Operation

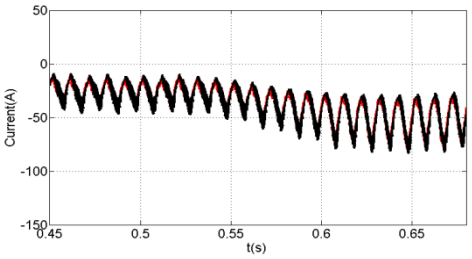
Similar to the medium voltage case, the MMC-1 is operated as a DC voltage regulator to stabilize the DC link voltage and to maintain the power injected from the AC Grid-1 to the DC link at unity power factor and MMC-2 is controlled as an active power regulator to inject rated active power into AC Grid-2 during normal operation. Figure 6-7 and Figure 6-8 show simulation results when the initial peak current is 200A and the current is increased to 400A at time t=0.5s. Figure 6-7(a) and Figure 6-8(a) display the output voltage of both H-bridges relative to the mid-point of the DC link. The three-phase currents quickly respond to the step change of the grid current references in Figure 6-7(b) and Figure 6-8(b). The arm currents and common mode currents have low harmonic components while their magnitudes are suppressed in Figure 6-7(c), (d) and Figure 6-8(c), (d). The DC link voltage is stabilized in Figure 6-7(e) and cell capacitor voltages are balanced in Figure 6-7(f) and Figure 6-8(e).



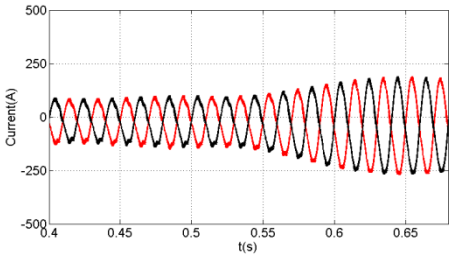
a) MMC-1 AC terminal voltage relative to supply mid-point



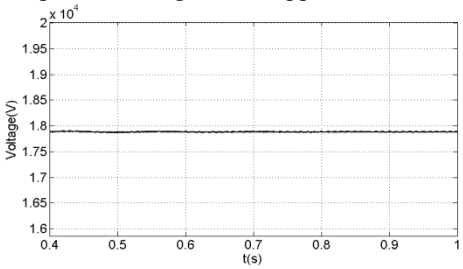
b) Three-phase current waveforms inject from grid to MMC-1 where step change is applied to the peak of the reference current



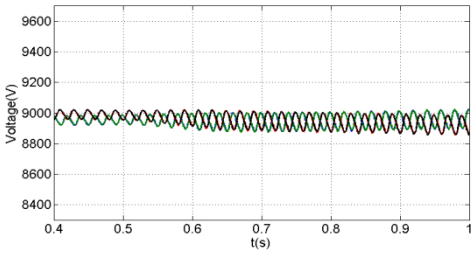
c) Common mode current (i_{dc}=½(i_1+i_2)) of MMC-1 phase a and its reference sets by the DC voltage regulator that controls cell capacitor voltage of the upper and lower arms



d) Upper and lower arm currents zoomed around the instant where step change is applied to the peak of the reference output current(MMC-1 phase *a*)

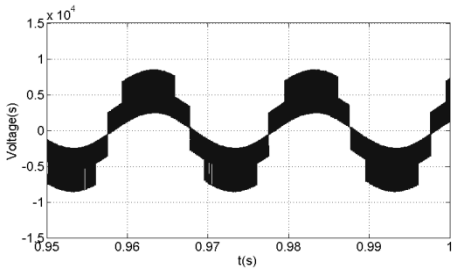


e) DC link voltage V_{DC1}

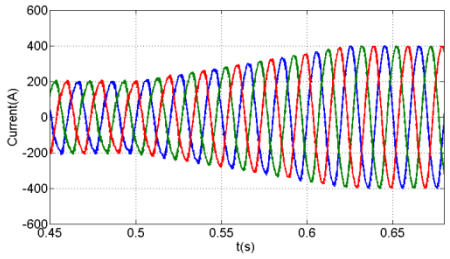


f) Cell capacitor voltage of the upper and lower arms of MMC-1 phase *a*

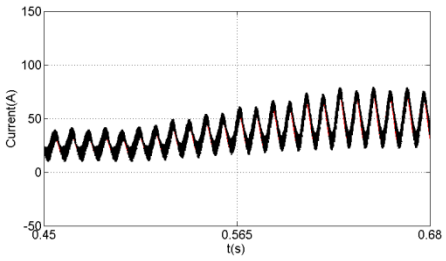
Figure 6-15. Simulation waveforms when the three-phase H-bridge MMC-1 is controlled with the control scheme in Figure 6-3 and Figure 6-5, and at t=0.5s a step change is applied that increases the peak reference current from I_m=200A to 400A.



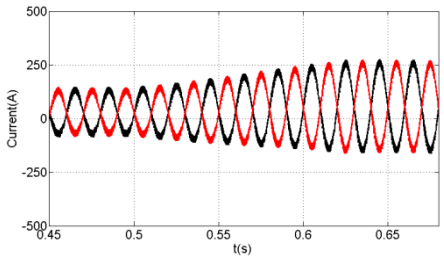
a) MMC-2 AC terminal voltage relative to supply mid-point



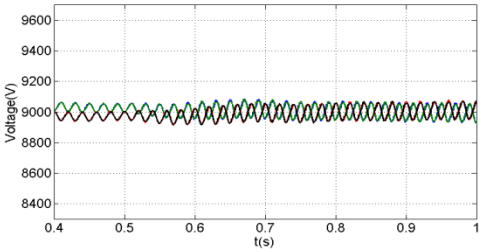
b) Three-phase current waveforms inject from MMC-2 to grid where step change is applied to the peak of the reference current



c) Common mode current (i_{dc}=½(i_1+i_2)) of MMC-2 phase *a* and its reference sets by the DC voltage regulator that controls cell capacitor voltage of the upper and lower arms



d) Upper and lower arm currents zoomed around the instant where step change is applied to the peak of the reference output current(MMC-2 phase *a*)

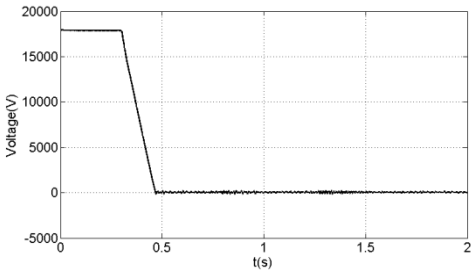


e) Cell capacitor voltage of the upper and lower arms of MMC-2 phase *a*

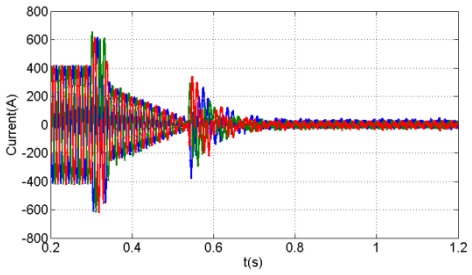
Figure 6-16. Simulation waveforms when the three-phase H-bridge MMC-2 is controlled with the control scheme in Figure 6-3 and Figure 6-5, and at t=0.5s a step change is applied that increases the peak reference current from I_m=200A to 400A.

6.5.2 DC fault emulation

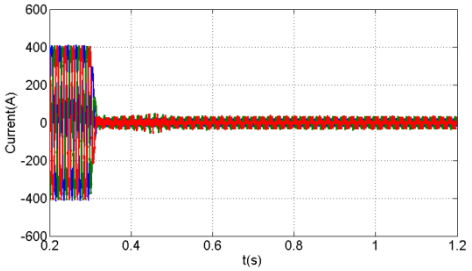
A permanent DC short circuit fault is applied across the DC link of the H-bridge MMC back to back HVDC system at t=0.3s. The grid currents for the system AC terminals are reduced to zero immediately the DC fault is applied and remain at zero during the entire fault period. Uncontrolled inrush currents are eliminated, as illustrated in Figure 6-17(b) and (c), while the DC link voltage i collapses in Figure 6-17(a). The arm currents and common mode currents are regulated and suppressed during the fault period in Figure 6-17(d), (e), (f) and (g). Cell capacitor voltages are maintained at rated value to provide voltage support to the grid in Figure 6-17(h) and (i).



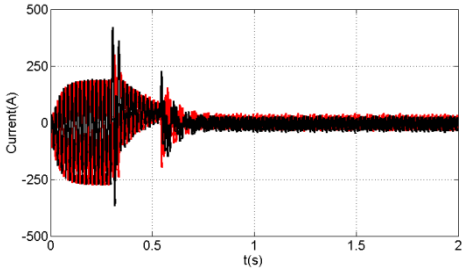
a) DC link voltage



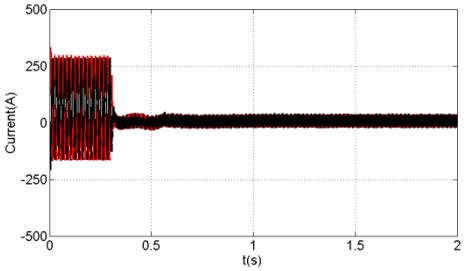
b) Three-phase AC terminal current waveforms of MMC-1



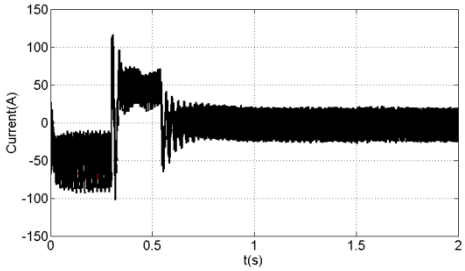
c) Three-phase AC terminal current waveforms of MMC-2



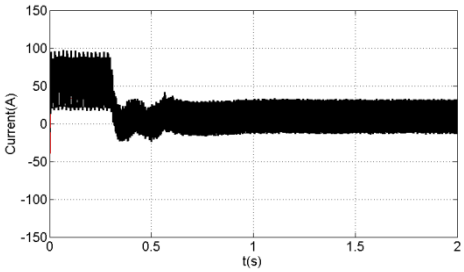
d) Upper and lower arm currents zoomed around the DC fault period of MMC-1 phase *a*



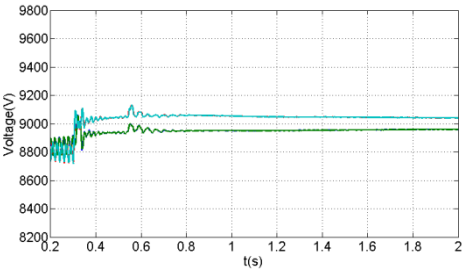
e) Upper and lower arm currents zoomed around the DC fault period of MMC-2 phase *a*



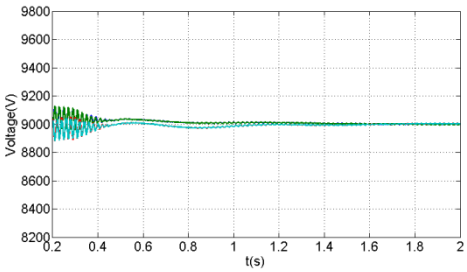
f) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-1 phase *a*



g) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-2 phase *a*



h) Cell capacitor voltages of MMC-1 phase *a*

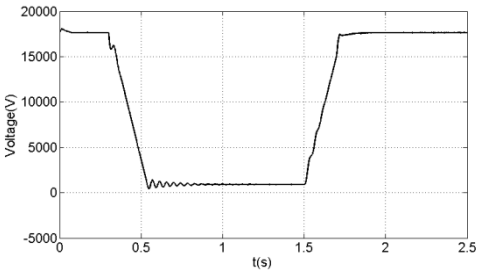


i) Cell capacitor voltages of MMC-2 phase *a*

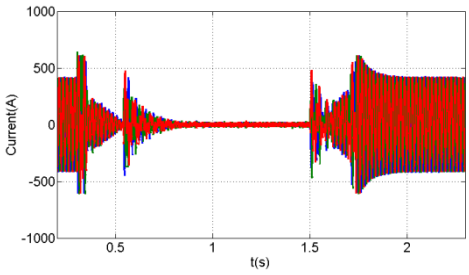
Figure 6-17. Waveforms, with the presented control scheme, during a permanent pole-to-pole DC short circuit fault, where the AC and DC currents in both arms of H-bridge MMCs are restrained, with elimination of the uncontrolled in-feed current to DC link from the grid, without converter blocking

6.5.3 DC fault ride-through with post-fault recovery

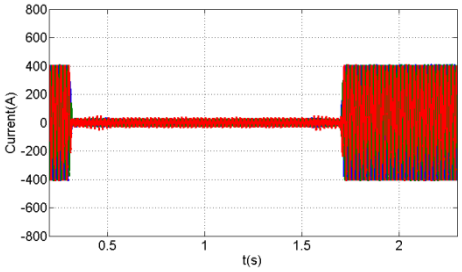
A temporary DC fault case is tested where the DC fault is applied at t=0.3s and cleared at t=1.5s. The active power flow between AC grid1 and AC grid2 is reduced to zero at t=0.3s and restored at t=1.8s; illustrated by Figure 6-18. Figure 6-18(d), (e), (f) and (g) illustrate the arm currents and common mode currents are regulated through the period. Cell capacitor voltages are balanced during the stage shown in Figure 6-18(h) and (i). The system is recovered utilizing the DC network post-fault recharging strategy without any difficulties in terms of cell capacitor voltage balancing, over currents in either arm and grid distortion.



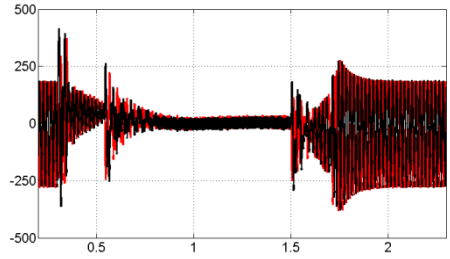
a) DC link voltage



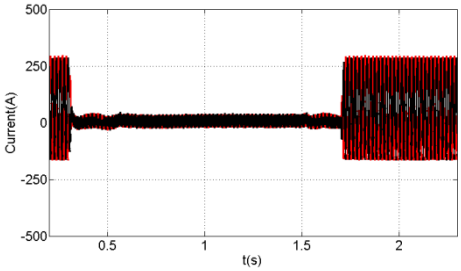
b) Three-phase AC terminal current waveforms of MMC-1



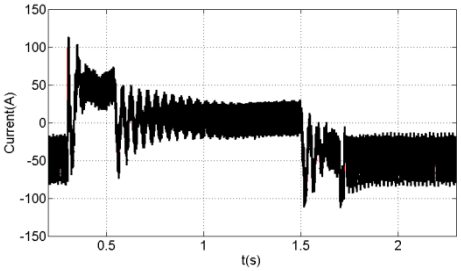
c) Three-phase AC terminal current waveforms of MMC-2



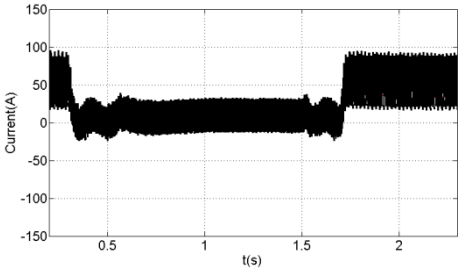
d) Upper and lower arm currents zoomed around the DC fault period of MMC-1 phase *a*



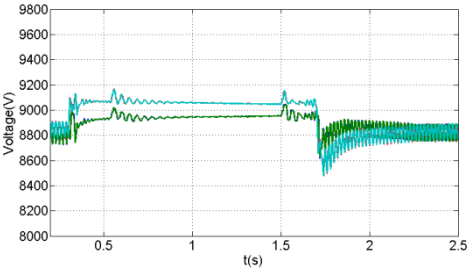
e) Upper and lower arm currents zoomed around the DC fault period of MMC-2 phase *a*



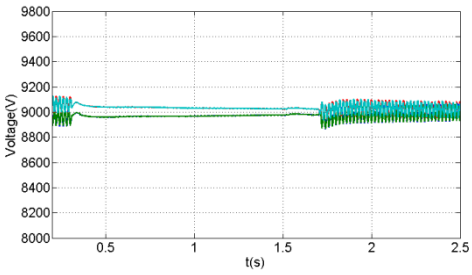
f) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-1 phase *a*



g) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-2 phase *a*



h) Cell capacitor voltages of MMC-1 phase *a*

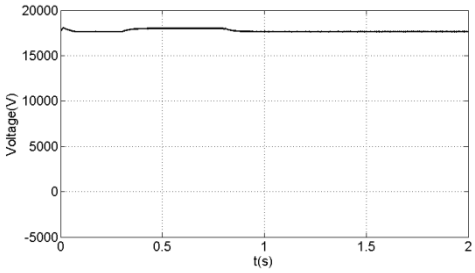


i) Cell capacitor voltages of MMC-2 phase *a*

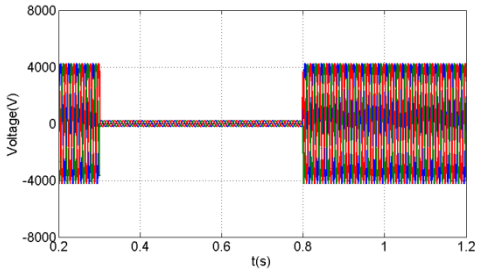
Figure 6-18. Waveforms during a temporary DC short circuit fault where the AC and DC currents in both arms of H-bridge MMCs are restrained, with elimination of any uncontrolled in-feed current to the DC link from the grid, without converter blocking

6.5.4 AC fault emulation

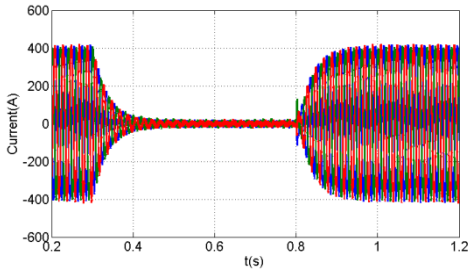
To evaluate the transient performance of the back to back HVDC system, a three-phase AC fault is applied on AC grid2 at t=0.3s and cleared at t=0.8s in Figure 6-19, and the three-phase AC grid1 fault is emulated in Figure 6-20 during the same period. The simulation results illustrate that the control scheme is capable of interrupting an AC grid fault and suppresses the AC terminal currents, the arm currents and common mode currents during fault period in Figure 6-19 and Figure 6-20(b), (c), (d), (e), (f), (g) and (h), while the DC link voltage is stabilized and cell capacitor voltages are balanced in Figure 6-19 and Figure 6-20(a), (i) and (j).



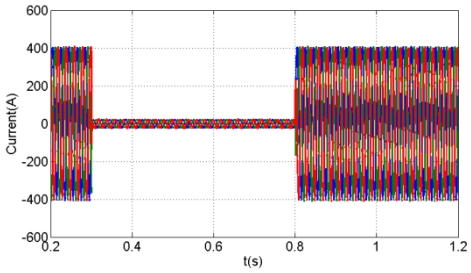
a) DC link voltage



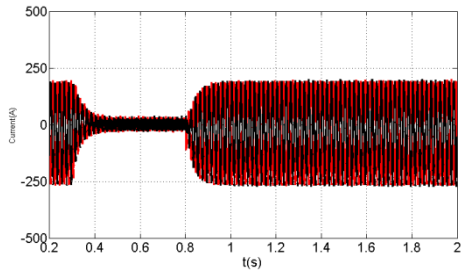
b) Three-phase AC voltage waveforms of AC grid2



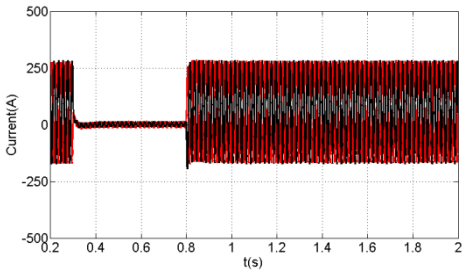
c) Three-phase AC terminal current waveforms of MMC-1



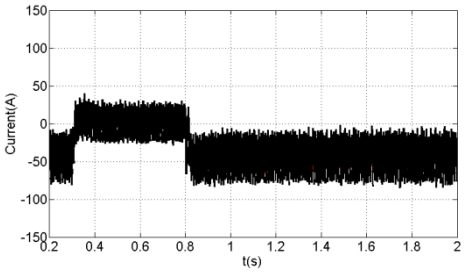
d) Three-phase AC terminal current waveforms of MMC-2



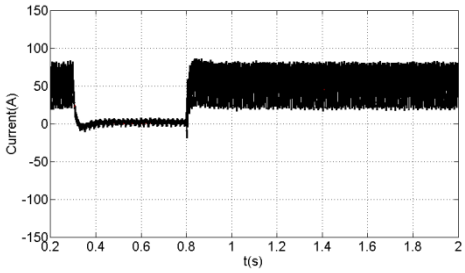
e) Upper and lower arm currents zoomed around the AC fault period of MMC-1 phase *a*



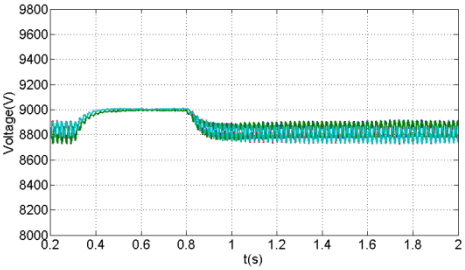
f) Upper and lower arm currents zoomed around the AC fault period of MMC-2 phase *a*



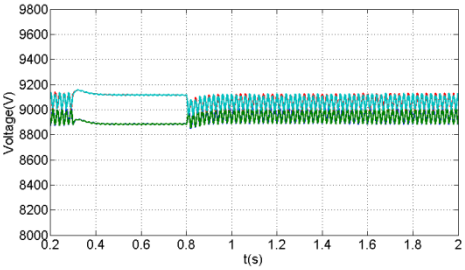
g) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-1 phase *a*



h) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-2 phase *a*

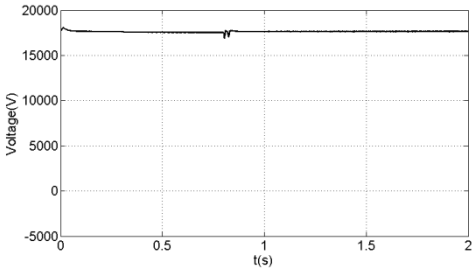


i) Cell capacitor voltages of MMC-1 phase *a*

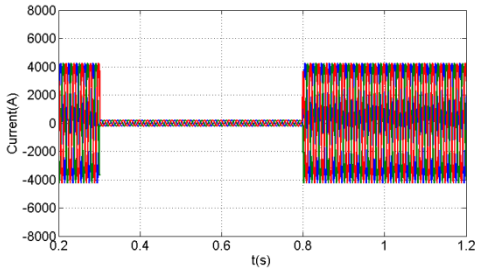


j) Cell capacitor voltages of MMC-2 phase *a*

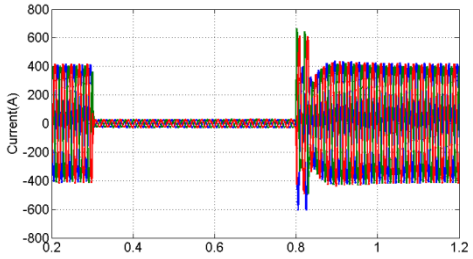
Figure 6-19. Waveforms during a temporary three-phase AC grid2 fault, where the AC and DC currents in both arms of the H-bridge MMCs are restrained



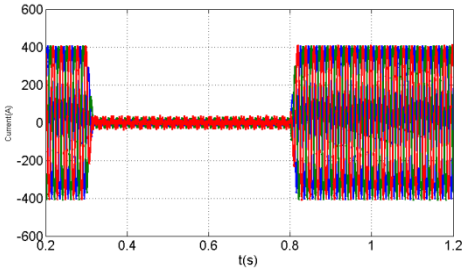
a) DC link voltage



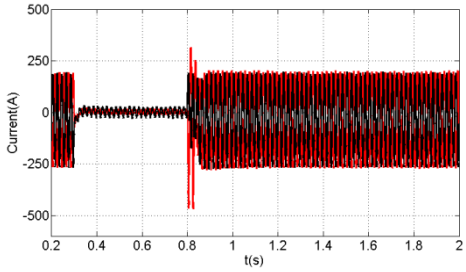
b) Three-phase AC voltage waveforms of AC grid1



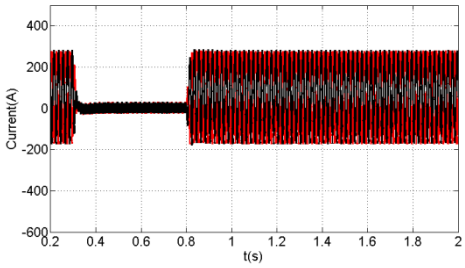
c) Three-phase AC terminal current waveforms of MMC-1



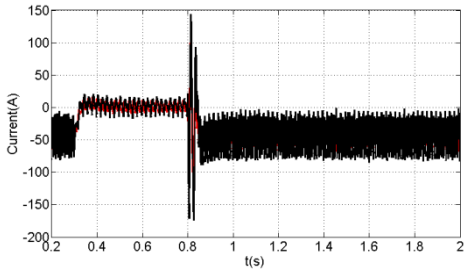
d) Three-phase AC terminal current waveforms of MMC-2



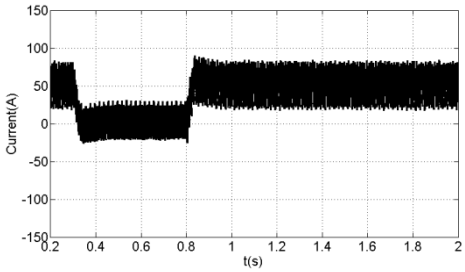
e) Upper and lower arm currents zoomed around the AC fault period of MMC-1 phase *a*



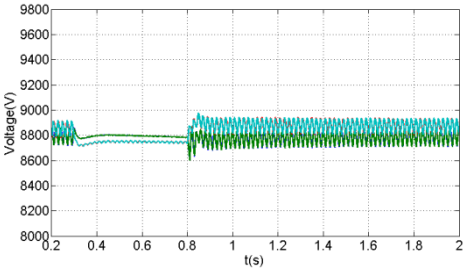
f) Upper and lower arm currents zoomed around the AC fault period of MMC-2 phase *a*



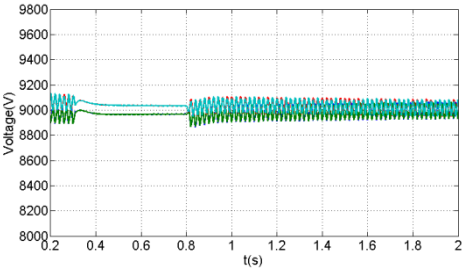
g) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-1 phase *a*



h) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-2 phase *a*



i) Cell capacitor voltages of MMC-1 phase *a*

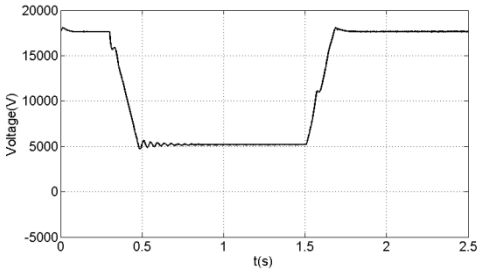


j) Cell capacitor voltages of MMC-2 phase *a*

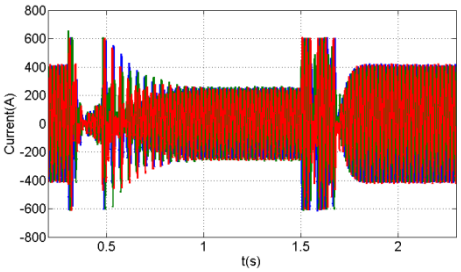
Figure 6-20. Waveforms during a temporary three-phase AC grid1 fault, where the AC and DC currents in both arms of H-bridge MMCs are restrained

6.5.5 Active power injection into the AC grid when an H-bridge MMC operates in a boost mode during DC voltage sag

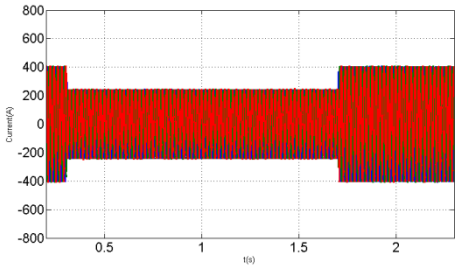
Figure 6-21 displays the DC link voltage collapse to 30% at t=0.5s and its recovery to rated value at t=1.5s. The grid current magnitude is suppressed to 60% when the fault is applied and restored to the pre-fault level at t=1.7s in Figure 6-21(b) and (c). The arm currents and common mode currents are regulated and the control scheme fast response suppresses the overshoot of the common mode currents during the DC link voltage collapse and the restoration transients in Figure 6-21(d), (e), (f) and (g). Cell capacitor voltages are balanced and oscillate around the set value in Figure 6-21(h) and (i).



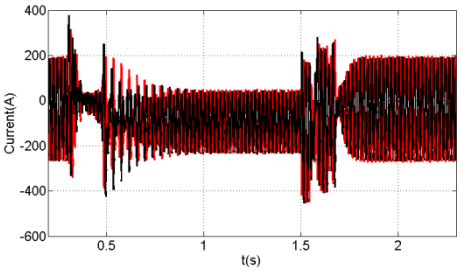
a) DC link voltage



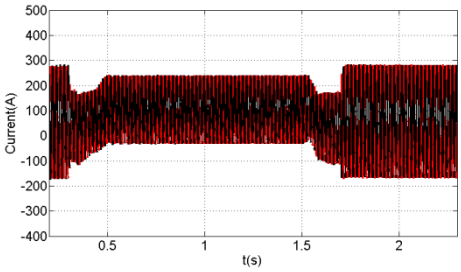
b) Three-phase AC terminal current waveforms of MMC-1



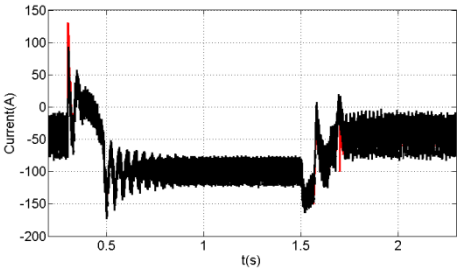
c) Three-phase AC terminal current waveforms of MMC-2



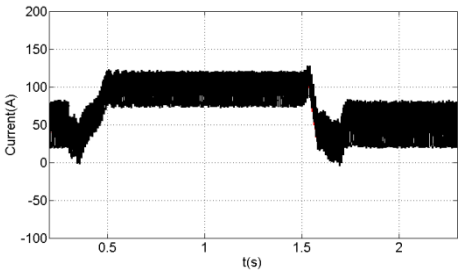
d) Upper and lower arm currents zoomed around the AC fault period of MMC-1 phase *a*



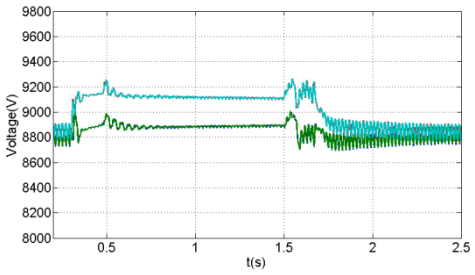
e) Upper and lower arm currents zoomed around the AC fault period of MMC-2 phase *a*



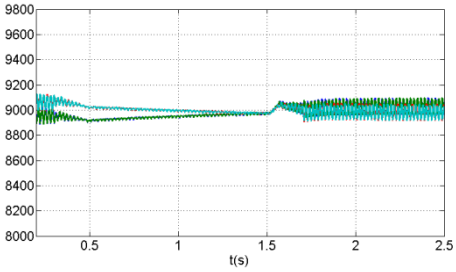
f) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-1 phase *a*



g) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-2 phase *a*



h) Cell capacitor voltages of MMC-1 phase *a*



i) Cell capacitor voltages of MMC-2 phase *a*

Figure 6-21. Simulation waveforms during a temporary DC fault where the DC link voltage is reduced to 30% and the grid current magnitude is decreased to 60%

6.6 **Four-terminal HVDC system**

In order to further demonstrate the validity of the proposed control strategy, the four-terminal system in Figure 6-22 is simulated. H-bridge converters MMC-1 and MMC-3 operate as DC link voltage regulators (DCVR) to maintain the DC link voltages at 18kV, while H-bridge converters MMC-2 and MMC-4 operate as active power regulators (APR) into the DC pool. The four-terminal H-bridge MMC DC network is constructed by using power electronics building blocks from the Matlab Simpower System library. The control schemes in Figure 6-5 and Figure 6-6 are adopted. Table 6-3 summarises the system parameters used in this section (simulation).

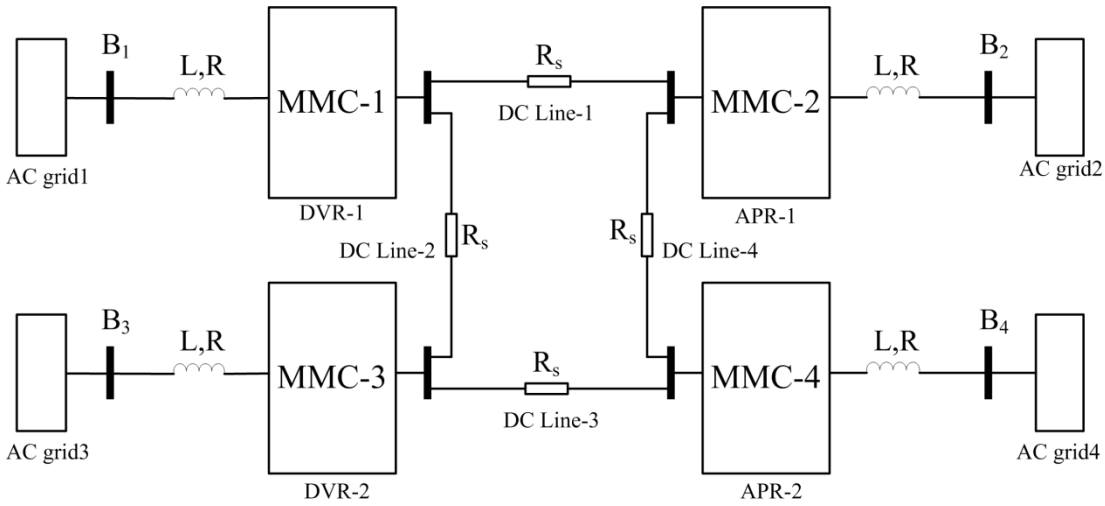


Figure 6-22. Four-terminal H-bridge MMC DC transmission system

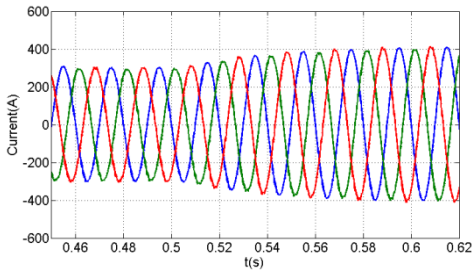
Table 6-3 Simulation parameters

System rating	28MW
Cell Capacitance	4.7mF
Switching frequency	2 kHz
DC link voltage	18kV
Arm inductance	3.3mH
Rated frequency	50Hz
Grid voltage $V_{lp\text{-}p}$	7360V

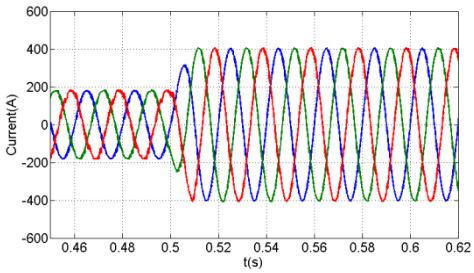
6.6.1 Normal Operation

Figure 6-23 shows simulation when a step change is applied to the three-phase current reference magnitudes of H-bridge MMC-2, as the initial 200A peak current is increased to 400A at t=0.5s, whilst the peak AC current of the H-bridge MMC-4 is maintained at 400A. H-bridge MMC-1 and MMC-3 operate to regulate their DC link voltage at 18kV and exchange active power between the DC networks and AC grid1 and AC grid 3. Figure 6-23(a), (b), (c) and (d) show that the three-phase currents of the all the MMCs have a quick response to the reference current step change of MMC-2. Figure 6-23 (e) to (l) show the currents and the arm currents of the H-bridge MMCs phase-*a* respectively. The harmonic components and magnitudes of common mode currents and arm currents are suppressed and the dynamic response of the DC power flow is improved. Figure 6-23(m), (n), (o) and (p) show the cell capacitor voltages are controlled around their set-point, including when the step change is

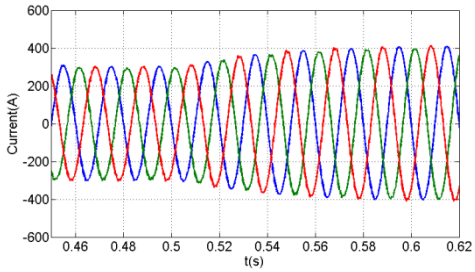
applied to the output current. Figure 6-23(q) illustrates that the DC voltage is regulated at the rated value.



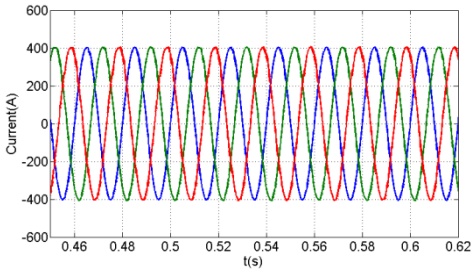
a) Three-phase AC terminal current waveforms of MMC-1



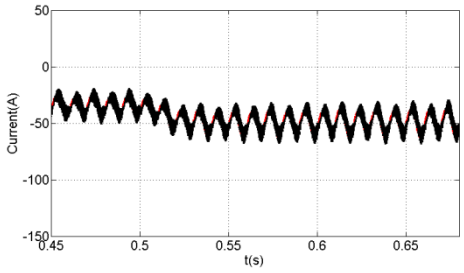
b) Three-phase AC terminal current waveforms of MMC-2



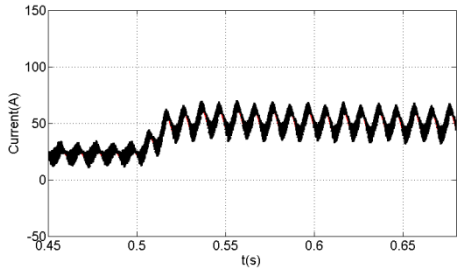
c) Three-phase AC terminal current waveforms of MMC-3



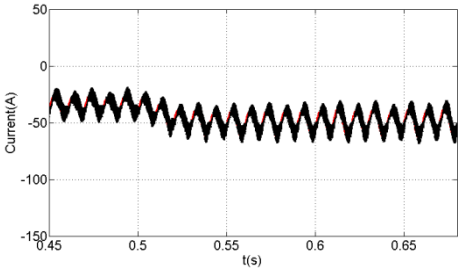
d) Three-phase AC terminal current waveforms of MMC-4



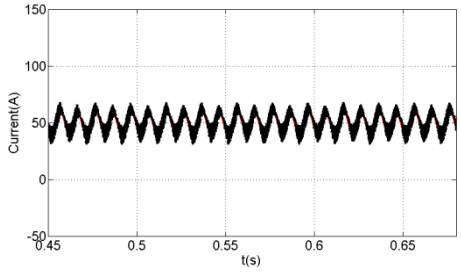
e) Common mode current (i_{dc}=½(i_1+i_2)) of MMC-1 phase *a* and its reference sets by the DC voltage regulator that controls cell capacitor voltage of the upper and lower arms



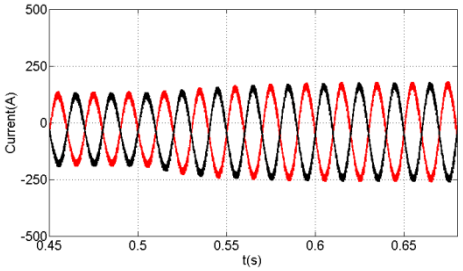
f) Common mode current (i_{dc}=½(i_1+i_2)) of MMC-2 phase *a* and its reference sets by the DC voltage regulator that controls cell capacitor voltage of the upper and lower arms



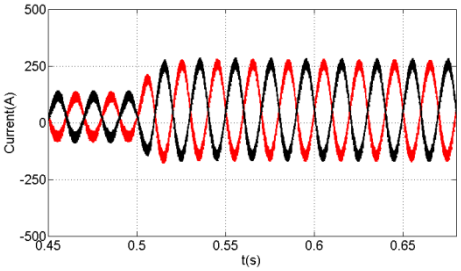
g) Common mode current (i_{dc}=½(i_1+i_2)) of MMC-3 phase *a* and its reference sets by the DC voltage regulator that controls cell capacitor voltage of the upper and lower arms



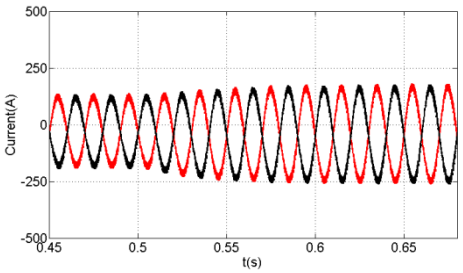
h) Common mode current (i_{dc}=½(i_1+i_2)) of MMC-4 phase *a* and its reference sets by the DC voltage regulator that controls cell capacitor voltage of the upper and lower arms



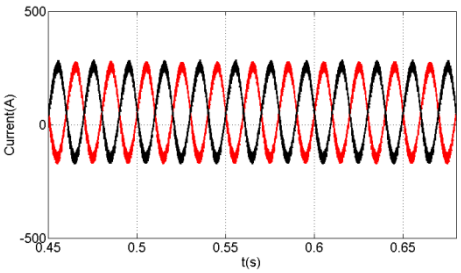
i) Upper and lower arm currents zoomed around the instant where step change is applied to the peak of the reference output current (MMC-1 phase *a*)



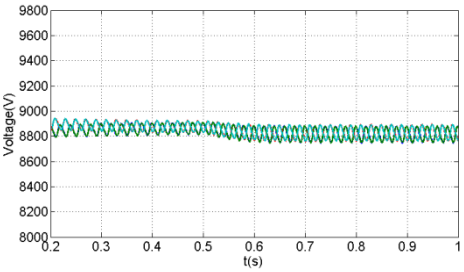
j) Upper and lower arm currents zoomed around the instant where step change is applied to the peak of the reference output current (MMC-2 phase *a*)



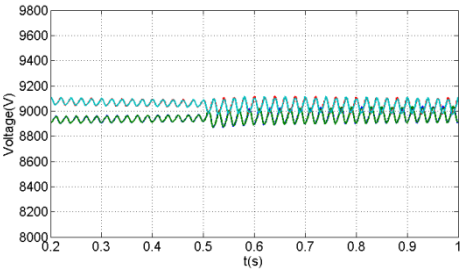
k) Upper and lower arm currents zoomed around the instant where step change is applied to the peak of the reference output current (MMC-3 phase *a*)



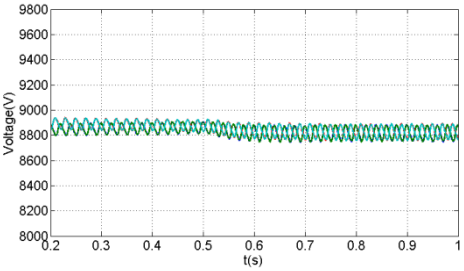
l) Upper and lower arm currents zoomed around the instant where step change is applied to the peak of the reference output current (MMC-4 phase *a*)



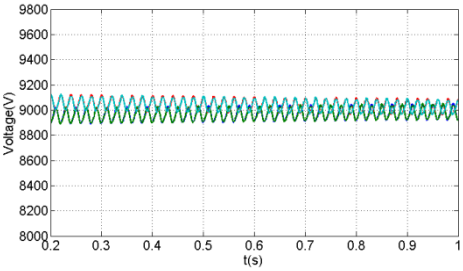
m) capacitor voltage of the upper and lower arms of MMC-1 phase *a*



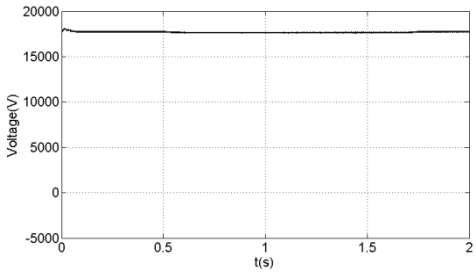
n) capacitor voltage of the upper and lower arms of MMC-2 phase *a*



o) capacitor voltage of the upper and lower arms of MMC-3 phase *a*



p) capacitor voltage of the upper and lower arms of MMC-4 phase *a*

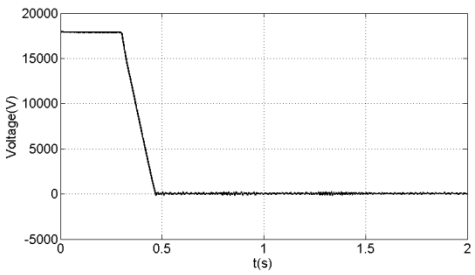


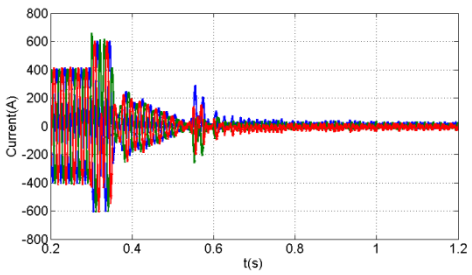
q) DC link voltage of DC line-1, line-2, line-3 and line-4

Figure 6-23. Simulation waveforms for the four-terminal H-bridge MMC DC transmission system, based on the control scheme in Figure 6-5 and Figure 6-6, and at t=0.5s a step change is applied to H-bridge MMC-2 that increases the peak reference current from I_m=200A to 400A.

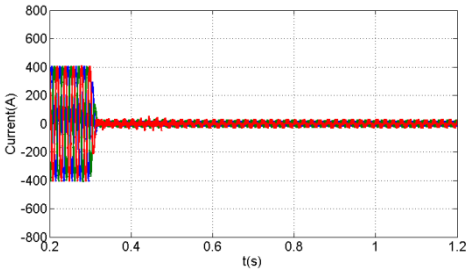
6.6.2 DC fault emulation

This case examines the response of the four-terminal DC network to a permanent DC fault applied at t=0.3s. The DC link voltages at all converter terminals collapse to zero. By utilising the control scheme in Figure 6-5 and Figure 6-6 with reference active powers (currents) set to zero, each H-bridge MMC operates as an independent STATCOM suppressing the inrush current from both the AC and DC sides. Furthermore, the MMCs can provide voltage support to AC grids during the DC link fault if their reactive power capabilities are exploited. Figure 6-24 (a) shows the DC link voltages on the DC lines. Figure 6-24(b), (c), (d) and (e) show the AC terminal currents of the H-bridge MMCs during the permanent pole-to-pole DC short circuit fault. Uncontrolled AC inrush current from AC grid is avoided. H-bridge MMC-1 and MMC-2 performed a controlled discharge of the DC link cable stray capacitance, without exposing their converter switches to excessive current stresses. Figure 6-24 (f) to (m) show that the arm currents and common mode currents are controlled and the DC components of common mode currents are suppressed to zero to maintain no power exchange between the DC links and H-bridge MMCs AC sides. Figure 6-24 (n), (o), (p) and (q) illustrate that the cell capacitors are regulated at their rated value. The limited voltage drift from the set point is due to control system tuning.

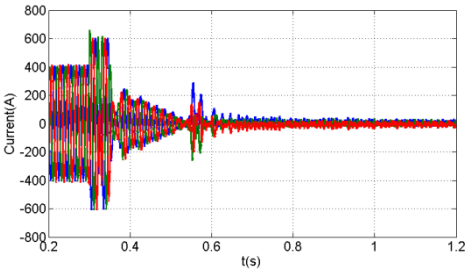




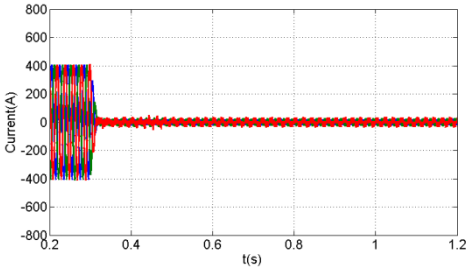
a) DC link voltage of DC line-1, line-2, line-3 and line-4



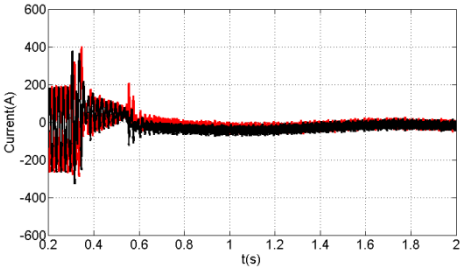
b) Three-phase AC terminal current waveforms of MMC-1



c) Three-phase AC terminal current waveforms of MMC-2



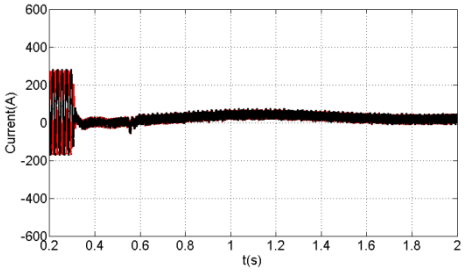
d) Three-phase AC terminal current waveforms of MMC-3



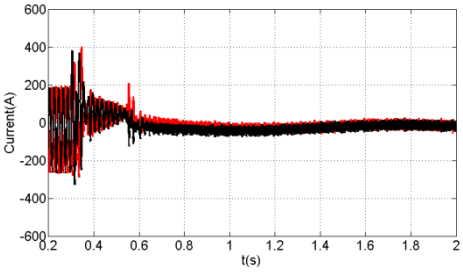
e) Three-phase AC terminal current waveforms of MMC-4

f) Upper and lower arm currents zoomed around the DC fault period of MMC-1 phase *a*

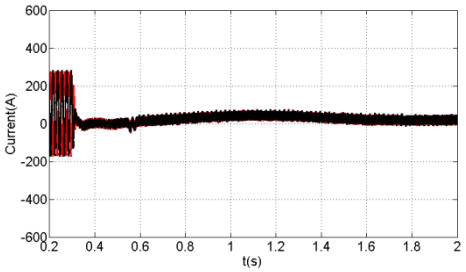
g) Upper and lower arm currents zoomed around the DC fault period of MMC-2 phase *a*



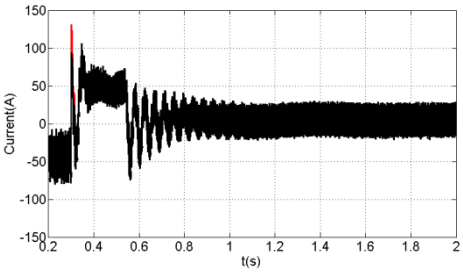
h) Upper and lower arm currents zoomed around the DC fault period of MMC-3 phase *a*

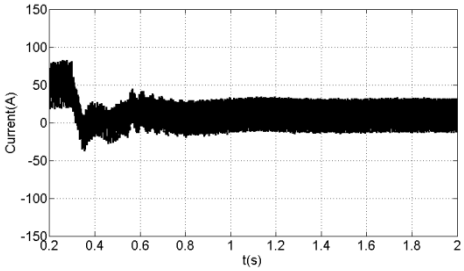


i) Upper and lower arm currents zoomed around the DC fault period of MMC-4 phase *a*

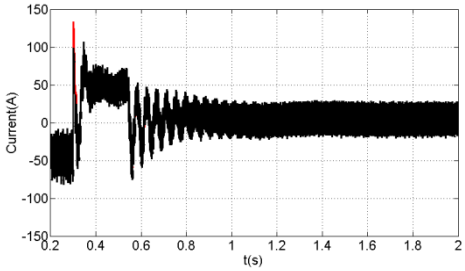


j) Common mode current $\frac{1}{2}(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-1 phase *a*

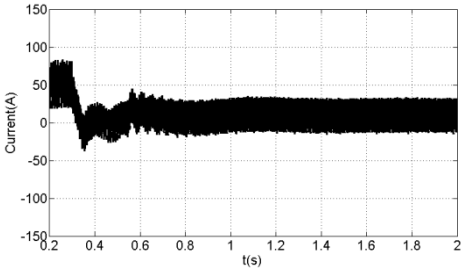




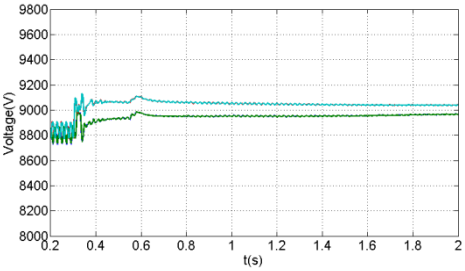
k) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-2 phase *a*



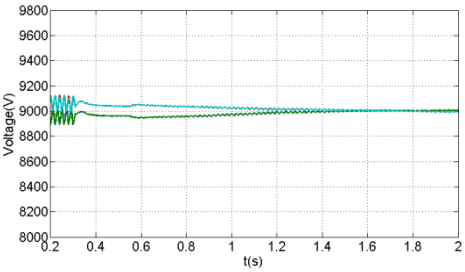
l) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-3 phase *a*



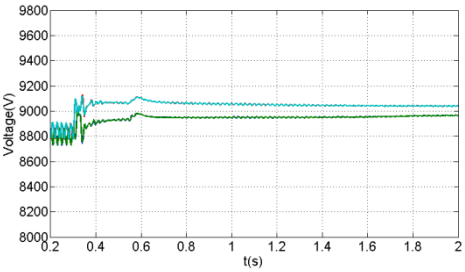
m) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-4 phase *a*



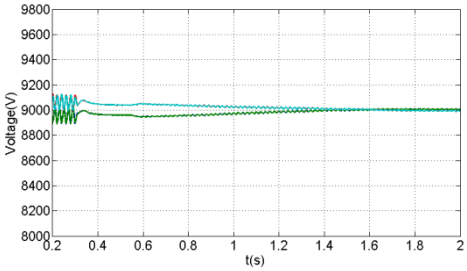
n) Cell capacitor voltages of MMC-1 phase *a*



o) Cell capacitor voltages of MMC-2 phase *a*



p) Cell capacitor voltages of MMC-3 phase *a*

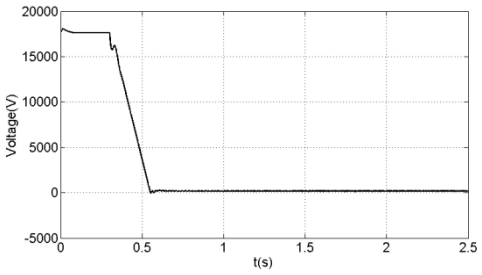


q) Cell capacitor voltages of MMC-4 phase *a*

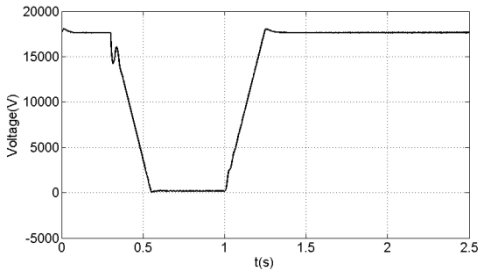
Figure 6-24. Waveforms during a permanent pole-to-pole DC short circuit fault, and restraining of the AC and DC currents in both arms of H-bridge MMCs, and elimination of the uncontrolled in-feed current to DC link from the grid, without converter blocking

6.6.3 Single DC line fault ride-through

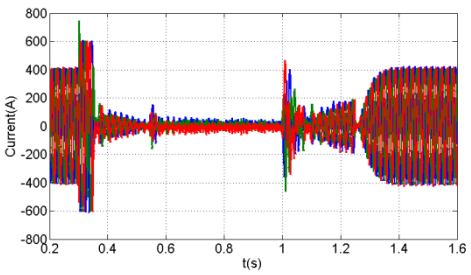
This case examines H-bridge MMC response when a permanent pole to pole DC fault is applied to DC line-1 at time t=0.3s, with the fault line isolated at 1.5s. After DC line-1 isolation, controlled recharge of the collapsed DC link is performed, minimising any semiconductor current surge as the DC cable stray capacitors charge. This is a necessary step before restoring the system to normal operation. To facilitate DC line-1 isolation, all the H-bridge MMCs continue to be operated with zero DC link voltages to allow low-voltage DC circuit breakers or simply isolators to disconnect the faulty line while the DC voltage is at zero. By using the DC network post-fault recharging strategy and the control scheme in Figure 6-5 and Figure 6-6, the DC transmission system can be re-established without external circuitry, once DC line-1 is isolated. Figure 6-25(a) shows the DC link voltage of DC line-1 collapses at t=0.3s and remains at zero after DC link-1 is isolated from the DC link. Figure 6-25(b) shows the DC link voltages of the remaining DC lines decrease to zero and are restore to their pre-fault rated voltages when DC line-1 is isolated from the DC link. Figure 6-25(c), (d), (e) and (f) display that the AC terminal currents of H-bridge MMCs are fully controlled. Figure 6-25(g) to (n) illustrate that the arm currents and common mode currents are regulated, with all cell capacitor voltages balanced at the rated value in Figure 6-25(o), (p). (q) and (r).



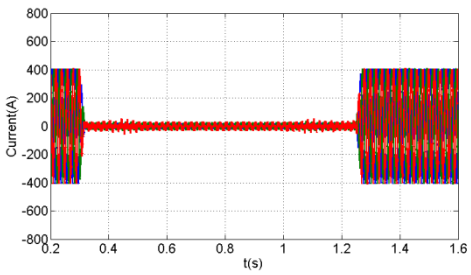
a) DC link voltage of DC line-1



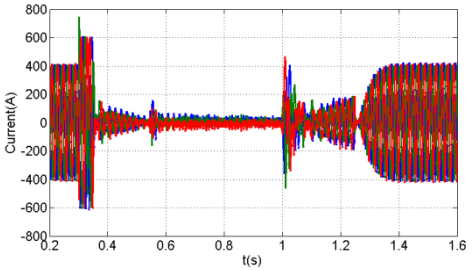
b) DC link voltage of DC line-2, line-3 and line-4



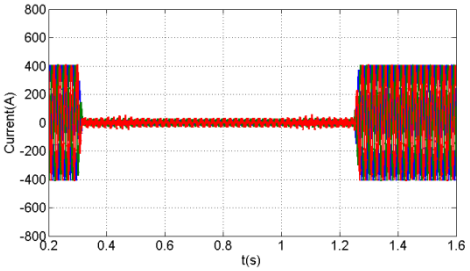
c) Three-phase AC terminal current waveforms of MMC-1



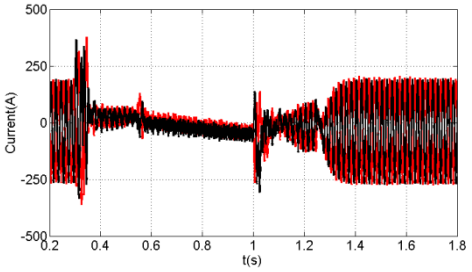
d) Three-phase AC terminal current waveforms of MMC-2



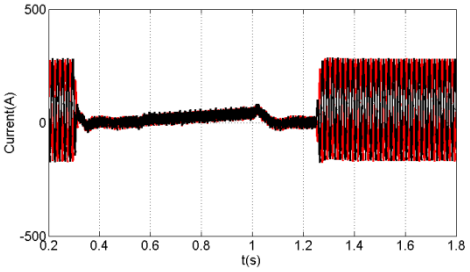
e) Three-phase AC terminal current waveforms of MMC-3



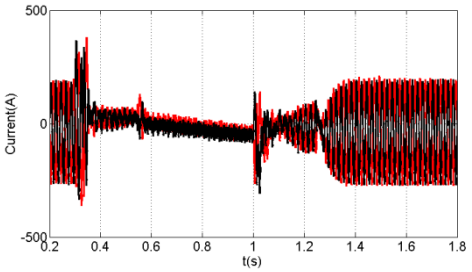
f) Three-phase AC terminal current waveforms of MMC-4



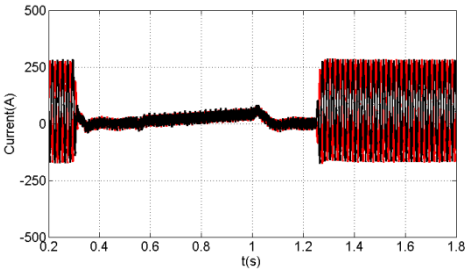
g) Upper and lower arm currents zoomed around the DC fault period of MMC-1 phase *a*



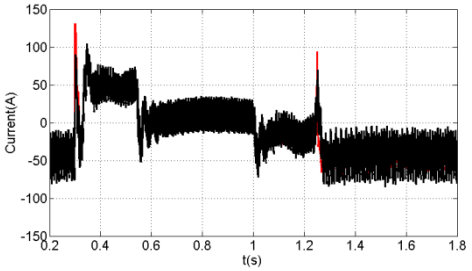
h) Upper and lower arm currents zoomed around the DC fault period of MMC-2 phase *a*



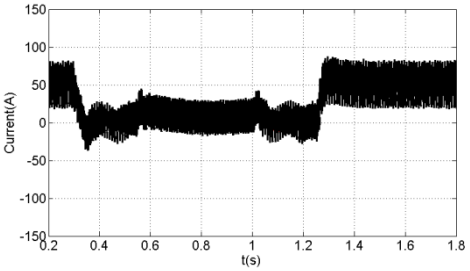
i) Upper and lower arm currents zoomed around the DC fault period of MMC-3 phase *a*



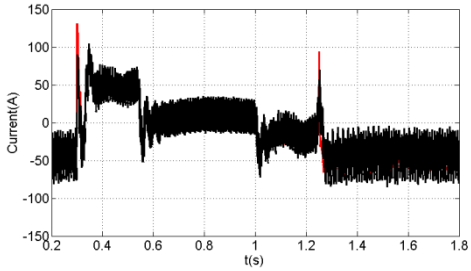
j) Upper and lower arm currents zoomed around the DC fault period of MMC-4 phase *a*



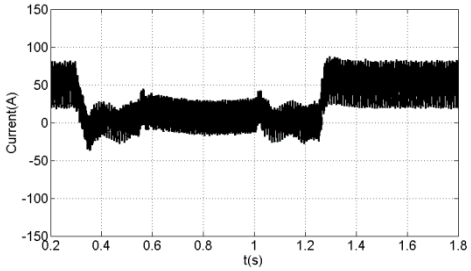
k) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-1 phase *a*



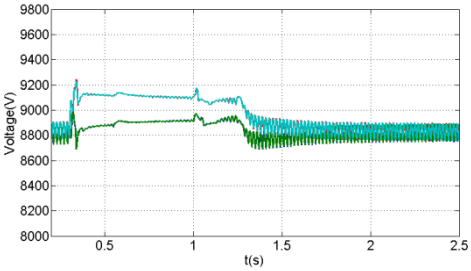
l) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-2 phase *a*



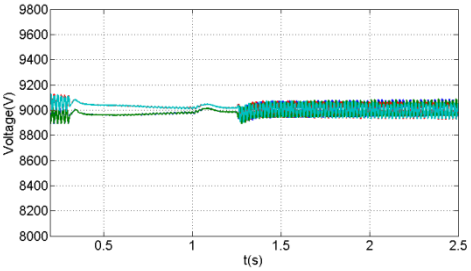
m) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-3 phase *a*



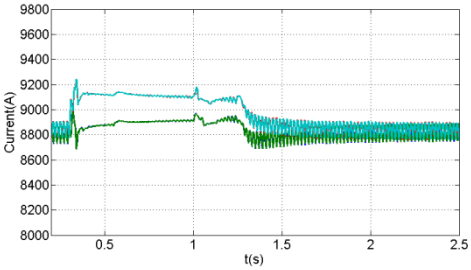
n) Common mode current $½(i_1+i_2)$ and its reference set by the capacitor voltage regulator of MMC-4 phase *a*



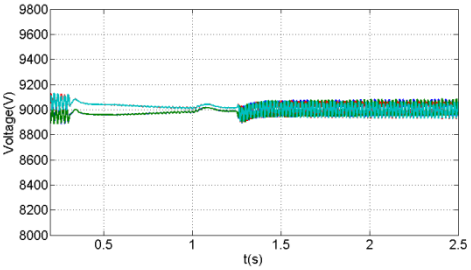
o) Cell capacitor voltages of MMC-1 phase *a*



p) Cell capacitor voltages of MMC-2 phase *a*



q) Cell capacitor voltages of MMC-3 phase *a*



r) Cell capacitor voltages of MMC-4 phase *a*

Figure 6-25. Waveforms illustrate the effectiveness of the control scheme during a DC short circuit fault in DC line-1, with AC and DC currents in both arms of H-bridge MMCs restrained, and elimination of uncontrolled in-feed current to DC link from the grid, without converter blocking

6.7 **Summary**

This chapter investigated H-bridge modular multilevel converters in back to back and multi-terminal DC transmission systems. Utilising a *dq* control scheme, the common mode and differential mode control loops in Figure 6-3 and Figure 6-5 enable independent H-bridge MMC control during normal operation, DC link or AC grid fault ride-through, and active power injection during DC link voltage sag. The simulation results of the back to back H-bridge MMC medium voltage DC transmission system and back to back H-bridge MMC HVDC transmission system establish that the control scheme allows both DC transmission system to operate with

low harmonic components in the arm currents and common mode currents of H-bridge MMCs while cell capacitor voltages remain balanced. In case of a DC fault or AC fault, the H-bridge MMCs of the back to back DC transmission system can interrupt any inrush current from the AC grid and suppress the DC components of the common mode currents and arm currents (thus eliminating power exchange between the AC grid and DC link), while cell capacitor voltages are still maintained at their set point. The back to back DC transmission system is capable of transferring active power between different AC grids via the DC link when the DC link voltage has collapsed to lower value (between 0 to V_{DC}). This feature may facilitate system implementation for renewable energy interconnection. In the multi-terminal HVDC system, the proposed control strategy improves control flexibility and allows the system to ride through a pole to pole DC fault, as with the back to back HVDC system. When the DC fault is applied to a single DC line, the control scheme reduces the DC link voltages to zero to facilitate isolation of the faulted DC line, and allows system re-establishment without external circuitry.

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[42] G. P. Adam, K. H. Ahmed, S. J. Finney, K. Bell, and B. W. Williams, "New Breed of Network Fault-Tolerant Voltage-Source-Converter HVDC Transmission System," *Power Systems, IEEE Transactions on,* vol. 28, pp. 335-346, 2013.

[43] G. P. Adam, S. J. Finney, K. Bell, and B. W. Williams, "Transient capability assessments of HVDC voltage source converters," in *Power and Energy Conference at Illinois (PECI), 2012 IEEE*, 2012, pp. 1-8.

Chapter 7. Conclusion

7.1 General conclusion

In recent years, modular multilevel converter (MMC) has gained wide acceptance from power system industry as a suitable technology for large power evacuation efficiently and reliably. Although half-bridge and H-bridge MMCs have predominantly similar characteristics, half-bridge MMC is widely used because it has lower semiconductor losses compared to that of H-bridge MMC. Despite the aforementioned disadvantage, this thesis investigated new control strategies for the H-bridge MMC that can be used to provide additional features that may justify its adoption instead of half-bridge MMC in wide range of applications. These features may put H-bridge MMC as front runner of HVDC transmission systems and networks, and grid interfacing of renewable energy.

Chapter 1 highlighted the motivations and objectives of this thesis, including general discussions on HVDC transmission systems and its benefits. Chapters 2 presented brief review of the conventional current and voltage sources converters for HVDC applications, focusing on the attributes and limitations that are relevant to high-voltage applications. Chapter 3 provided high level discussions of the recent multilevel converters proposed for HVDC applications, including those based on mixed topologies (known as hybrid converters). This chapter has presented comparison between selected converter topologies, which are more likely to be adopted in real world future applications. Chapter 4 presented comprehensive discussions of the H-bridge MMC that include its operating principle, modulation and cell capacitor voltage balancing, and supported by simulations and experimentations. This chapter aimed to provide the necessary background knowledge about H-bridge MMC to be used in subsequent chapters. Chapter 5 presented a new control strategy for the H-bridge MMC that enable operation with variable DC link voltage from 0 to rated DC operating voltage (VDC). This implies that it can ride-through DC fault, without the need for converter blocking. The presented control scheme is validated using simulation and experimentations in open and closed loop as grid connected inverter. Chapter 6 provided further substantiation on the usefulness of the proposed control strategy when in point-to-point DC transmission systems, and multi-terminal DC networks. This chapter used simulation

to demonstrate the improved DC fault ride-though of the point-to-point and multi-terminal DC networks that can be achieved when the proposed control strategy is implemented in all converter stations. This chapter summarises the overall contributions of this thesis as detailed in the following sections.

7.2 **Author's contribution**

The author's contribution can be summarised as:

- A new control scheme that includes common and differential mode current control has been proposed. By exploiting the bipolar capability of H-bridge cells, the control scheme allows the H-bridge MMC to operate in a buck or boost mode. The harmonics of the arm currents and common mode current are suppressed in normal operation. The control scheme can be extended to any voltage level and power rating.
- During a DC link fault, the H-bridge cell voltage polarities are reversed to suppress any inrush current from the AC side of H-bridge MMC without converter blocking. The H-bridge MMC can be operated to provide voltage support to the AC grid.
- Active power injection is achieved when the DC link voltage collapses (between 0 to V_{DC}). Arm currents, common mode current and cell capacitor voltages are regulated.
- A cell capacitor voltage balancing strategy was presented. Cell capacitor voltages can be balanced at the rated value under any circumstances. Scalability of the strategy is validated by simulation and experimental results.
- A common mode control loop was applied to each phase of the H-bridge MMCs in a HVDC transmission system. A solid three-phase AC fault and DC fault ride-through, active power injection during DC link voltage suppression and normal operation, are all achieved. For the multi-terminal H-bridge MMC HVDC system, the control scheme allows the system to be operational when a permanent pole to pole fault is applied to a single DC link. In such applications, the DC link is isolated where the pole to pole fault occurs, and then the system is re-established without external circuitry once the fault DC link is isolated.

7.3 **Suggestions for future research**

The research undertaken in this thesis addressed some challenges in the control schemes of the H-bridge modular multilevel converter in terms of DC fault ride-through, active power injection during DC voltage collapse, arm current harmonic suppression and cell capacitor voltage balancing. Suggestions for future research are:

- The H-bridge MMC can be operated in a buck or boost mode and is able to inject active power into the AC grid when the DC voltage collapses. This feature is suitable for renewable energy interfacing in a low voltage ride-through condition, avoiding the need for a *DC/DC* converter. Therefore, maximum power point tracking (MPPT) should be achieved by the H-bridge MMC that can be applied to exploit maximum power from off-shore wind farms and photovoltaic cells at variable DC link voltages.
- Further investigation is required to analyze the hybrid DC transmission system that consists of LCC based HVDC transmission lines and H-bridge MMC based HVDC lines, with opportunity to reverse the DC link voltage when necessary. The DC offsets of the arm voltage references should be carefully selected in order to maintain the direction and the rated value of the power transmission.

Appendices

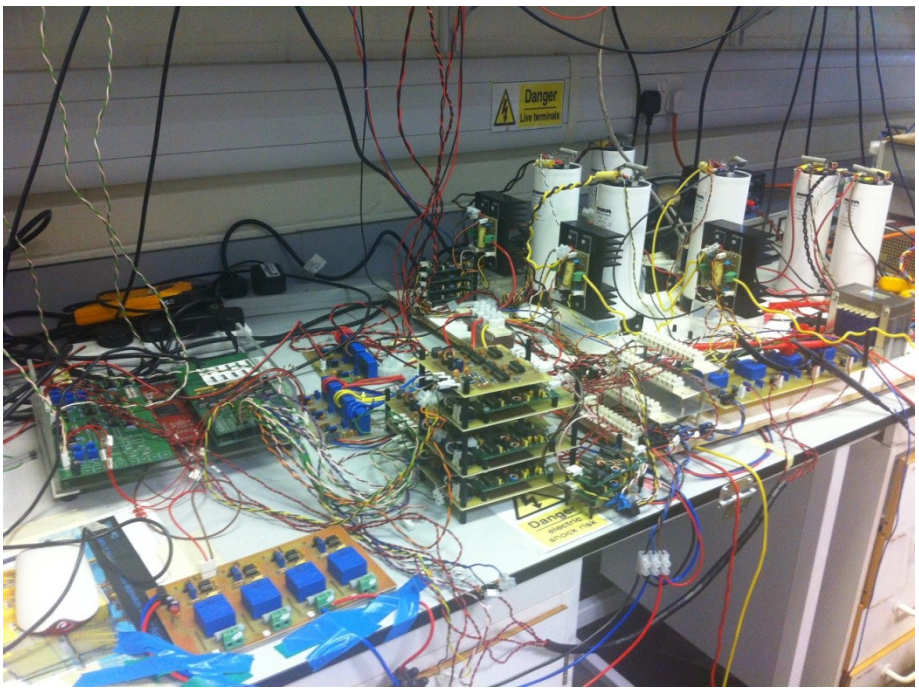
The appendices show details of the practical implementation. The test rigs, circuit boards as well as program codes are presented. The list of tables and figures, and the author's publications are also included.

Appendix A Experimental Configuration

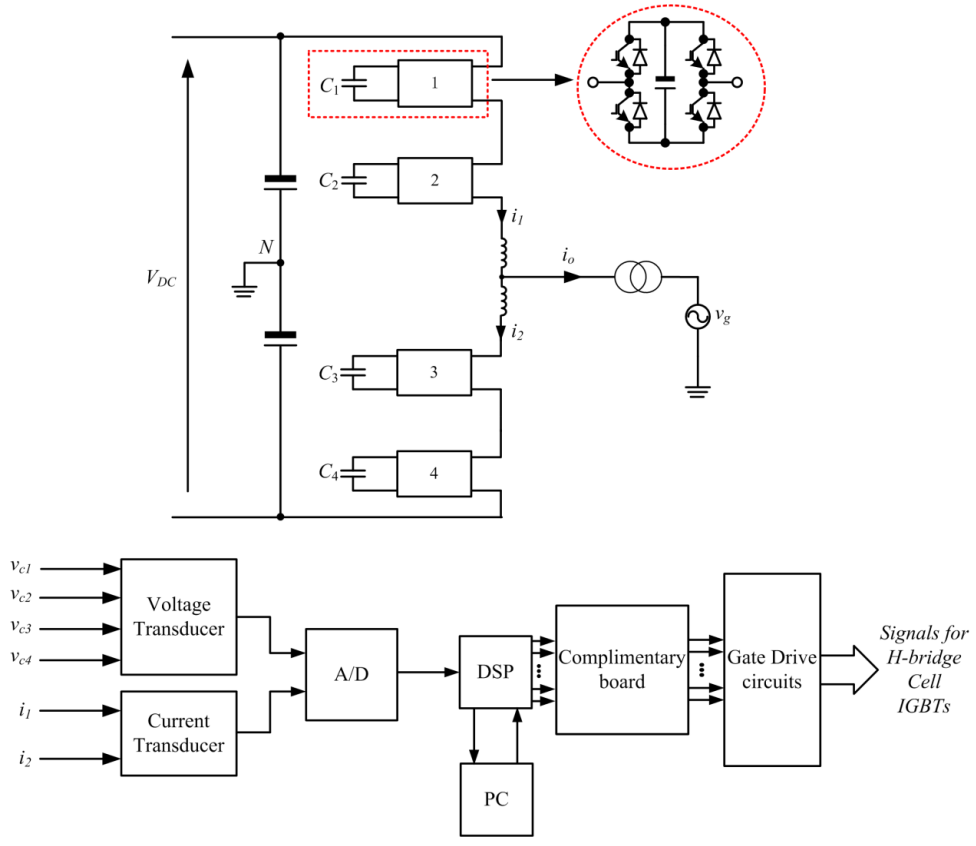
A.1 Test rig

The test rig displayed in Figure A-1 is set to verify the operational principle, cell capacitor voltage balancing strategy and the improved control scheme for single-phase H-bridge MMC with two cells per arm. It mainly includes the following components:

- 100V DC voltage source
- Four 4.7mF cell capacitors
- four H-bridge cells that consists of four IGBTs per cell
- TriCore 1796B digital signal processor (DSP)
- DSP Interfacing circuit
- Two 3.3 mH inductors
- Complementary signal generating boards
- Gate drive circuits
- Voltage and current measurement circuits



(a)



(b)

Figure A-1 Test rig for single-phase H-bridge MMC: (a) test rig photograph and (b) schematic diagram

A.2 Test rig components

The main components used in the practical implementations are introduced in this section.

A.2.1 Digital signal processor

The main task of the digital signal processor (DSP) is to sense the circuit analogue signals and to generate the required switching pattern driving signals for power electronic devices according to the implemented software algorithm. The 32-bit *TriCore*1796B DSP shown in Figure A-2 is employed as the controller for all practical implementations.

The main features of the DSP related to the practical implementation are listed below:

- High-performance 32-bit super-scalar *TriCore* V1.3 CPU with 4-stage pipeline
  –Superior real-time performance
  –Strong bit handling
  –Fully integrated DSP capabilities
  –Single precision Floating Point Unit (FPU)
  –150 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  –16 Kbyte Parameter Memory (PRAM)
  –32 Kbyte Code Memory (CMEM)
- Multiple on-chip memories
  –2 Mbyte Program Flash Memory with ECC
  –128 Kbyte Data Flash Memory usable for EEPROM emulation
  –192 Kbyte on chip SRAM
  –16 Kbyte Instruction Cache
  –16 Kbyte BootROM
- 32-bit External Bus Interface Unit (EBU) with
- High performing on-chip bus structure
- Versatile On-chip Peripheral Units

  –Two General Purpose Timer Array Modules (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management

–Two 16-channel Analog-to-Digital Converter units (ADC) with selectable 8-bit, 10-bit, or 12-bit resolution

–One 4-channel Fast Analog-to-Digital Converter unit (FADC) with concatenated comb filters for hardware data reduction: supporting 10-bit resolution, min. conversion time of 280ns

- 123 digital general purpose I/O lines, 4 input lines
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 and 2 (CPU, PCP3, DMA)
- Power Management System
- Clock Generation Unit with PLL
- Core supply voltage of 1.5 V
- I/O voltage of 3.3 V
- Full automotive temperature range: -40° to +125°C

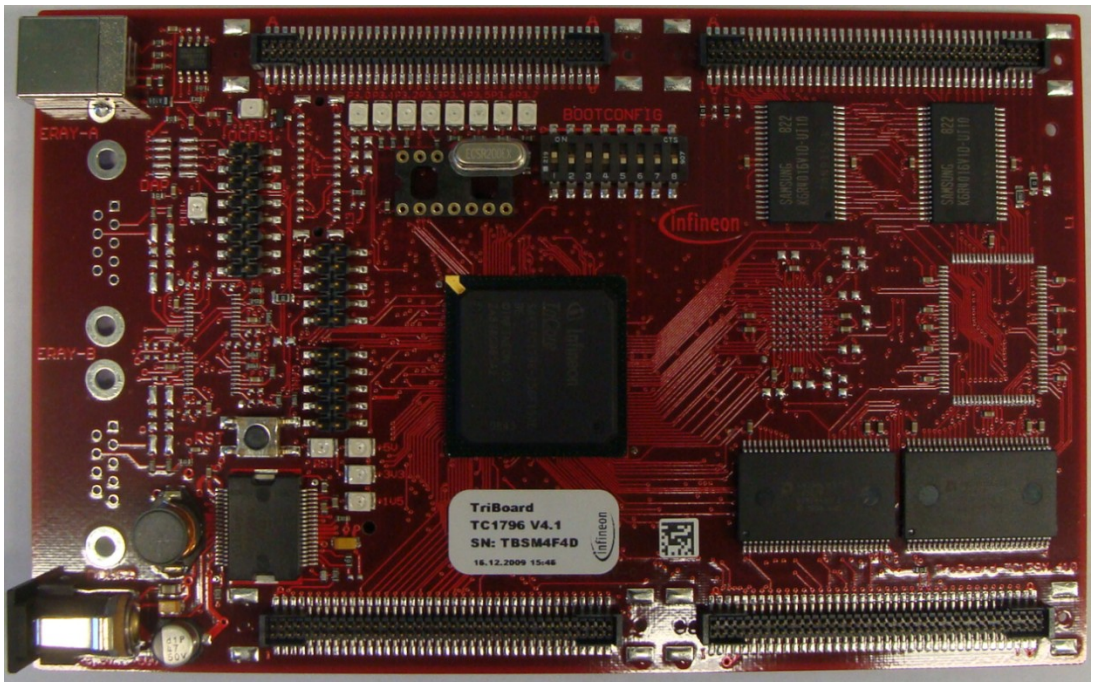


Figure A-2 DSP :32-bit *TriCore*1796B

A.2.2 Interface circuits

Two interface boards are used to electrically isolate the DSP from external circuits using optocouplers due to protection reasons. One board isolates the ADC channels of the DSP from the voltage and current transducer circuits; while the other one isolates the PWM channels on the DSP from the driving circuits. The photo of the

interface boards is shown in Figure A-3, with their circuit schematics shown in Figure A-4 and A-5.

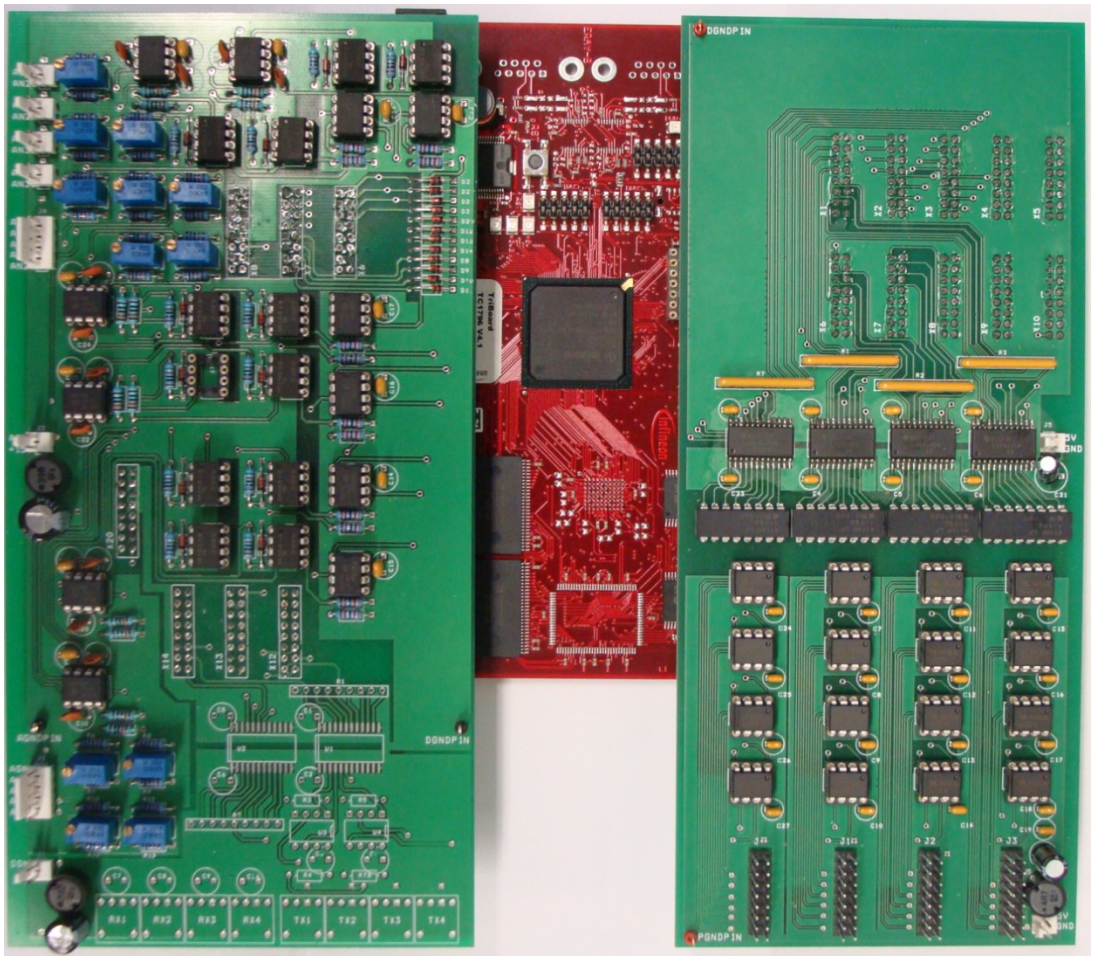
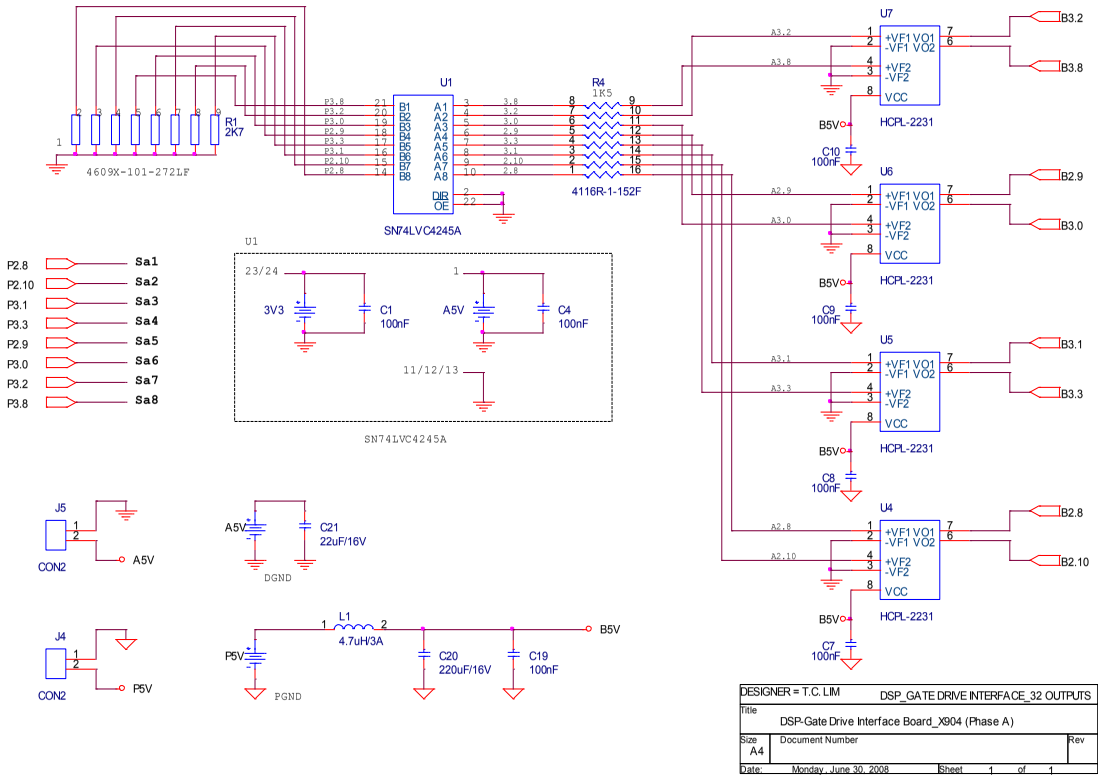


Figure A-3 Interfacing boards


R1
2K7
4609X-101-272LF
U1
SN74LVC4245A
R4
1K5
4116R-1-152F
P2.8
P2.10
P3.1
P3.3
P2.9
P3.0
P3.2
P3.8
Sa1
Sa2
Sa3
Sa4
Sa5
Sa6
Sa7
Sa8
U1
3V3
C1
100nF
A5V
C4
100nF
SN74LVC4245A
J5
CON2
A5V
C21
22uF/16V
DGND
J4
CON2
P5V
L1
4.7uH/3A
C20
220uF/16V
C19
100nF
B5V
PGND
U7
U6
U5
U4
HCPL-2231
C10
100nF
C9
100nF
C8
100nF
C7
100nF
B3.2
B3.8
B2.9
B3.0
B3.1
B3.3
B2.8
B2.10
DESIGNER = T.C. LIM
DSP_GATE DRIVE INTERFACE_32 OUTPUTS
DSP-Gate Drive Interface Board_X904 (Phase A)
Size A4
Document Number
Rev
Date: Monday, June 30, 2008
Sheet 1 of 1

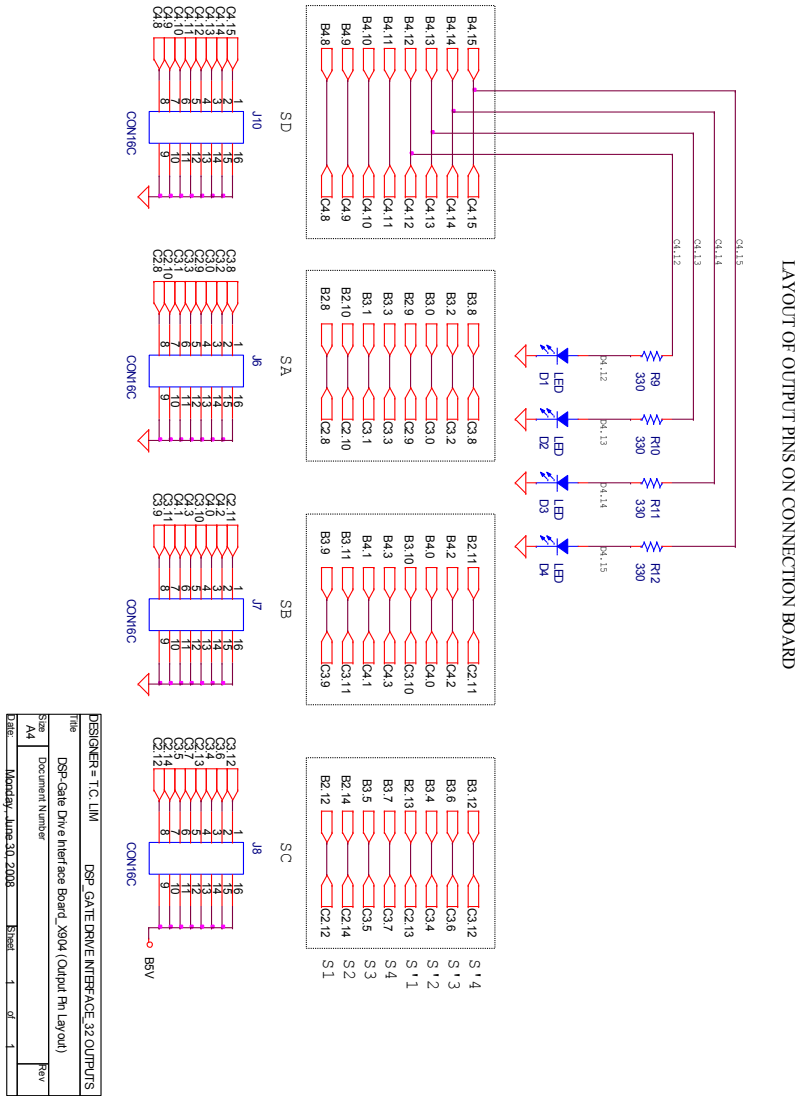


Figure A-4 Interface circuit schematic for PWM channels

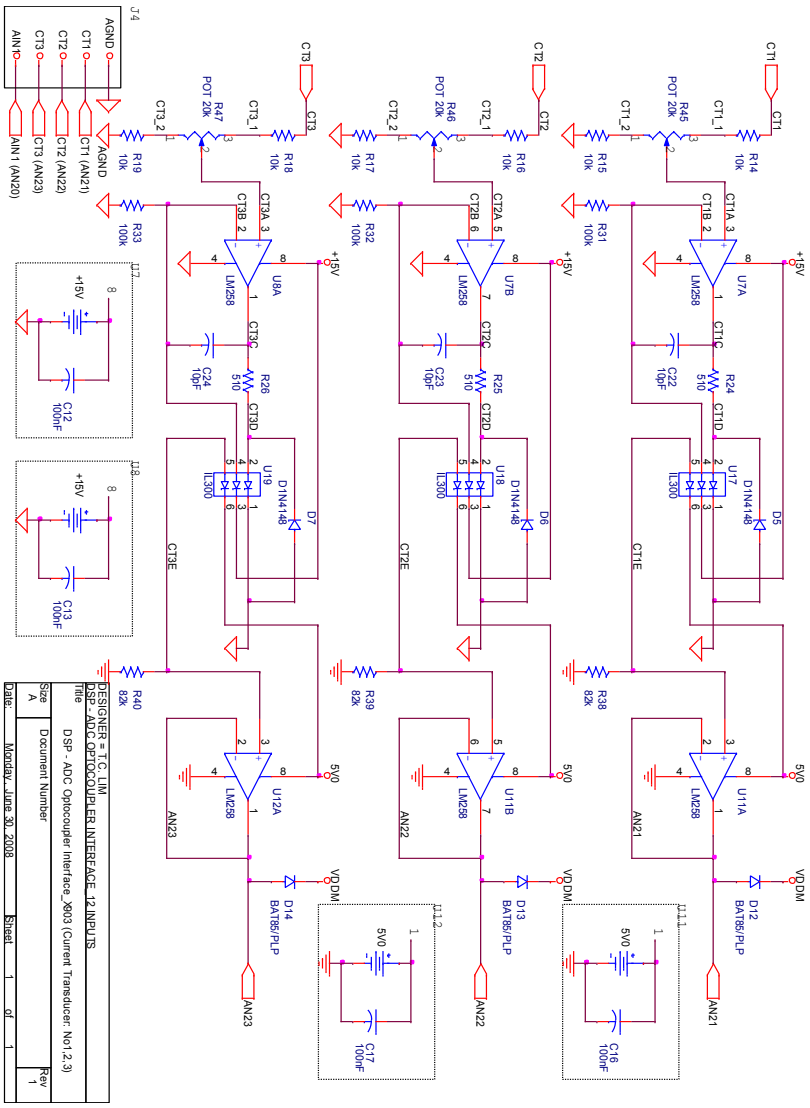


Figure A-5 Interface circuit schematic for ADC channels

A.2.3 Gate drive circuit

The gate drive circuit should be able to supply enough gate drive voltage and to source enough current for the switching devices to operate. The electrical isolation between the interface circuit and gate drive circuit is implemented using optocoupler. Figure A-6 shows the gate drive circuit photo and Figure A-7 shows the circuit schematic.

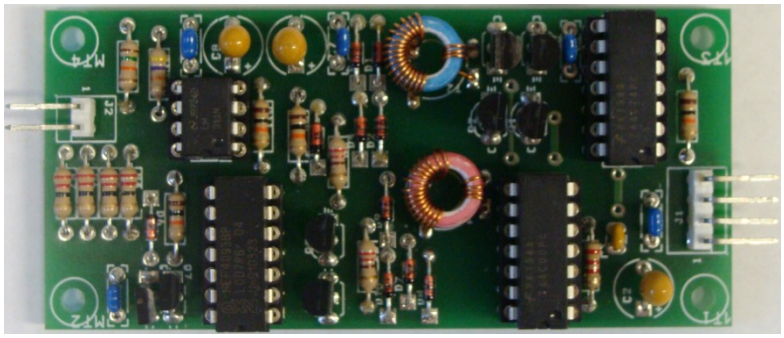


Figure A-6 Gate drive circuit photo

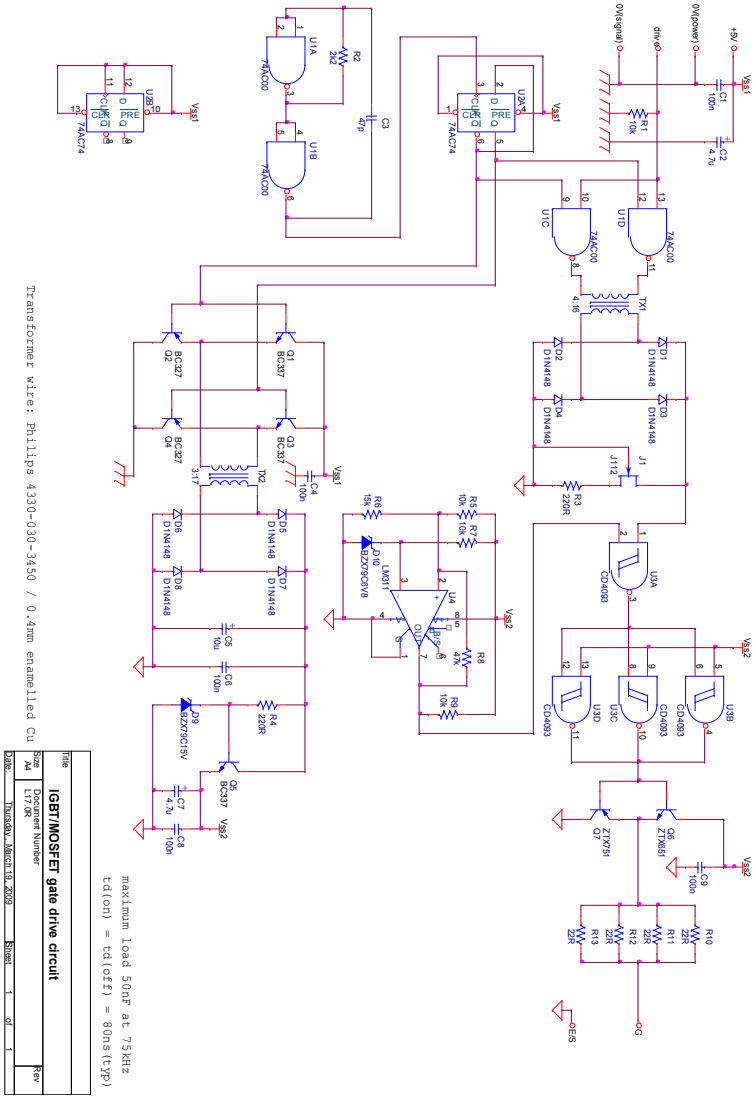


Figure A-7 Gate drive circuit schematic

A.2.4 Current and voltage transducer circuit

An accurate current data is required for the controller. The current transducer circuit schematic is shown in Figure A-8. The transducer used is Hall Effect current sensing device LA55P, which has high accuracy, good linearity and optimized response time with its features attached below. The photo of both transducers is given in Figure A-10.

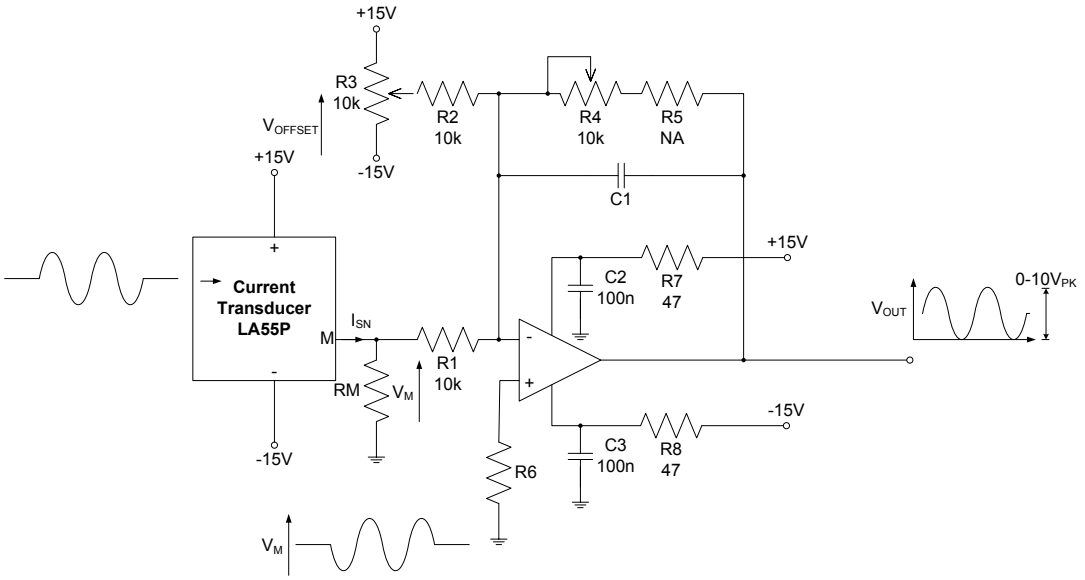


Figure A-8 Current transducer circuit schematic

The voltage transducer circuit schematic is shown in Figure A-9. The voltage transducer LV25P uses Hall Effect to measure the voltage signal.

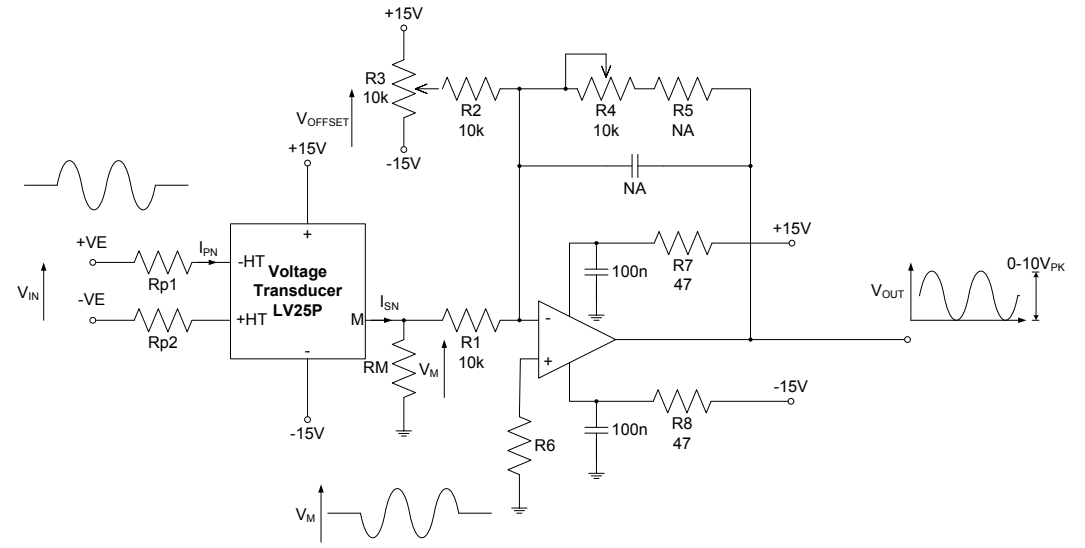
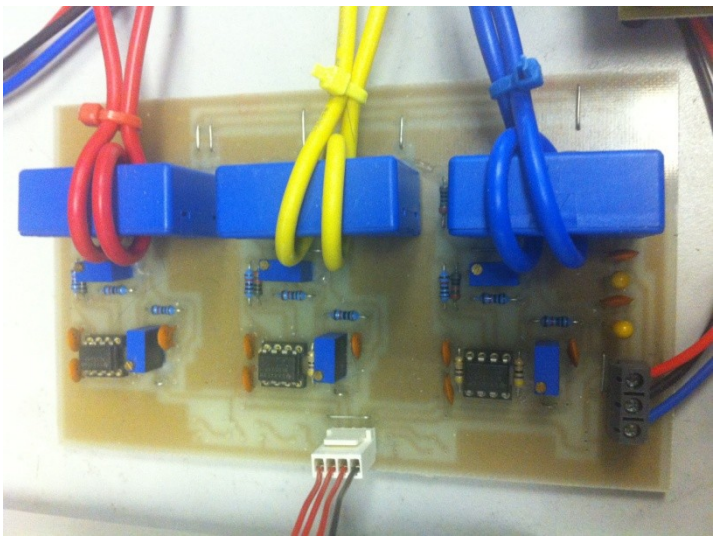


Figure A-9 Voltage transducer circuit schematic



(a)

(b)

Figure A-10 Photo of voltage and current transducers: (a) current transducers and (b) voltage transducers

A.2.5 Complementary Signal Generating Board

The complementary signal generating boards are used for generate complementary signals for two IGBTs in the same leg with 1μs dead time as shown Figure A-11 and Figure A-12.

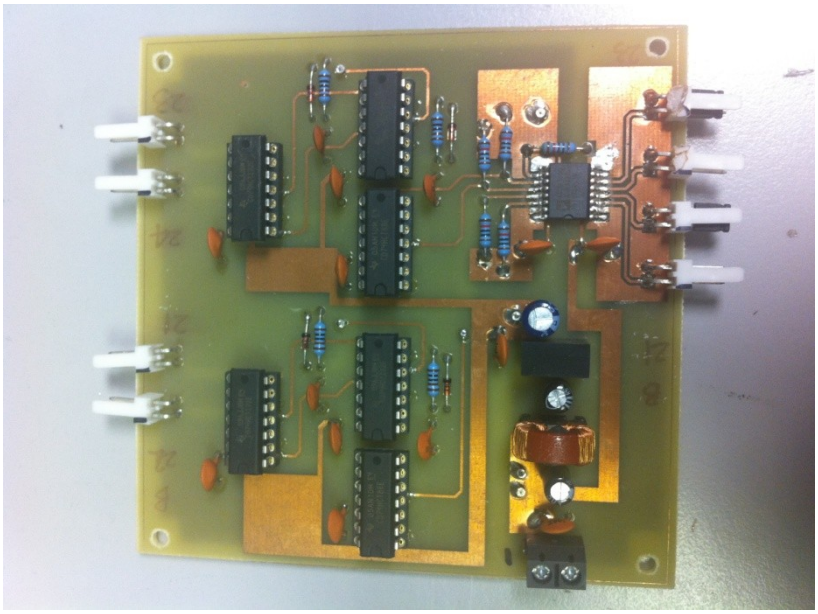
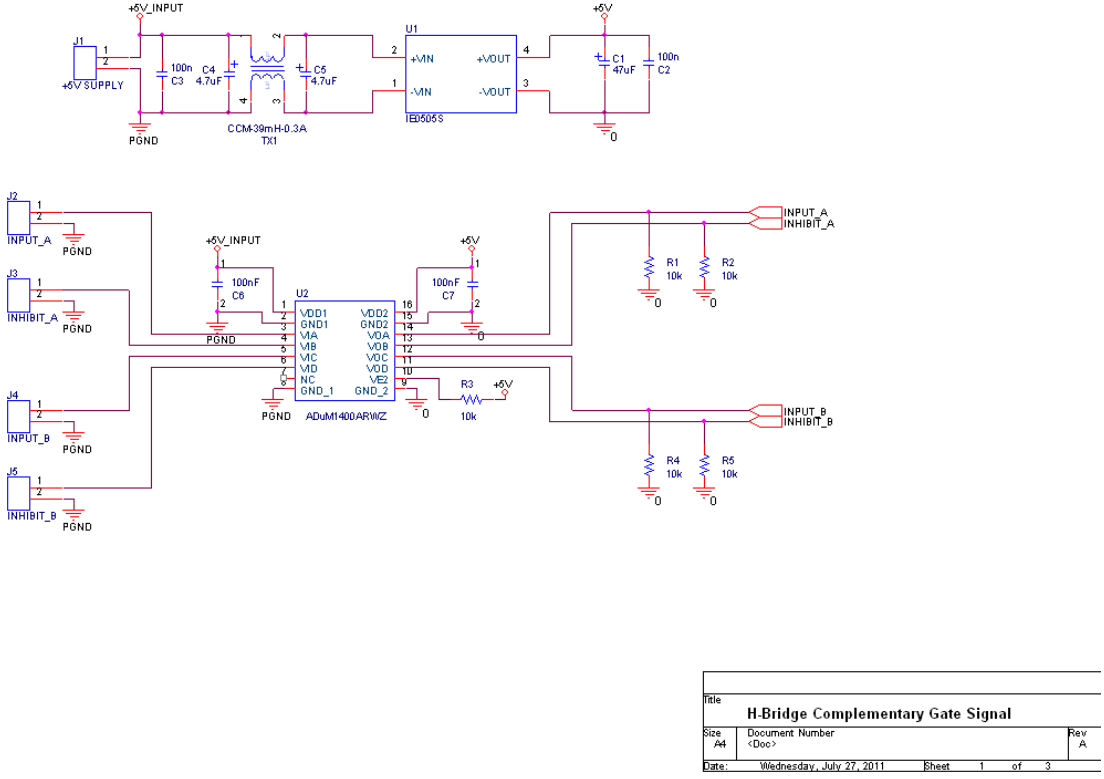


Figure A-11: Photo of complementary signal generating board.



Title	H-Bridge Complementary Gate Signal	
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Date: Wednesday, July 27, 2011	Sheet 1 of 3	

Figure A-12 Complementary gate signal generating board circuit schematic.

Appendix B Programme Code

B.1 H-bridge MMC with fundamental operational principle simulation code

B.1.1 Three-level H-bridge MMC code

```
function y = PWM_FCN(t,u)
va=u(1);vb=u(2);vc=u(3);
Vc1=u(4);Vc2=u(5);Vc3=u(6);Vc4=u(7);Ia=u(8);
%SPWM Modulation
fc=2100;
xc=2*pi*fc*t;
yc1=0.5*((2/pi)*asin(sin(xc))+1);
yc2=0.5*((2/pi)*asin(sin(xc))-1);
%Balancing
Ku_max=max(Vc1,Vc2);Ku_min=min(Vc1,Vc2);
KL_max=max(Vc3,Vc4);KL_min=min(Vc3,Vc4);

%Phase A
UP=[0 0 1 0 0 0 1 0 1 0 0 1 1 0 0 1];LW=[1 0 0 1 1 0 0 1 0 0 1 0 0 0 1 0];
A=[0 0 1 0 0 0 0 0 1 0 0 0 1 0 0 1];B=[0 0 0 0 0 0 1 0 1 0 0 0 1 0 0 1];
C=[0 0 0 0 0 0 1 0 1 0 0 1 1 0 0 0];D=[0 0 1 0 0 0 0 0 1 0 0 1 1 0 0 0];
E=[1 0 0 1 1 0 0 0 0 0 0 0 0 1 0];F=[1 0 0 0 1 0 0 1 0 0 0 0 0 0 1 0];
G=[1 0 0 1 1 0 0 0 0 0 1 0 0 0 0 0];H=[1 0 0 0 1 0 0 1 0 0 1 0 0 0 0 0];
if(va>=yc1)
   sa=UP;

elseif(va<yc1&&va>=yc2)
   if(Ia>0)
      %During +ve current
      if(Vc1==Ku_min)
         if(Vc3==KL_max)
            sa=C;
         else
            sa=B;
         end
      else
         if(Vc3==KL_max)
            sa=D;
         else
            sa=A;
         end
      end
   else
      %During -ve current
      if(Vc3==KL_min)
         if(Vc1==Ku_max)
            sa=E;
         else
            sa=F;
         end
```

```
        else
            if(Vc1==Ku_max)
                sa=G;
            else
                sa=H;
            end
        end
    end
else
    sa=LW;
end

y =sa;
```

B.1.2 Five-level H-bridge MMC code

```
function [T11_r,T11_f,T13_r,T13_f, T21_r,T21_f,T23_r,T23_f] = fcn(va,Ia,Vc1,Vc2,Ts,DT)
if(va>=0.5&&va<=1)
    Td=2*-Ts*(1/2-va);
    if(Ia>=0)
        if(Vc1<Vc2)
            T11_r=DT;T11_f=Ts-DT;
            T13_r=Ts/2;T13_f=Ts/2;
            T21_r=DT;T21_f=Td-DT;
            T23_r=Ts/2;T23_f=Ts/2;
        else
            T21_r=DT;T21_f=Ts-DT;
            T23_r=Ts/2;T23_f=Ts/2;
            T11_r=DT;T11_f=Td-DT;
            T13_r=Ts/2;T13_f=Ts/2;
        end
    else
        if(Vc1>Vc2)
            T11_r=DT;T11_f=Ts-DT;
            T13_r=Ts/2;T13_f=Ts/2;
            T21_r=DT;T21_f=Td-DT;
            T23_r=Ts/2;T23_f=Ts/2;
        else
            T21_r=DT;T21_f=Ts-DT;
            T23_r=Ts/2;T23_f=Ts/2;
            T11_r=DT;T11_f=Td-DT;
            T13_r=Ts/2;T13_f=Ts/2;
        end
    end
```

```
elseif(va>1)
   T11_r=DT;T11_f=Ts-DT;
   T13_r=Ts/2;T13_f=Ts/2;
   T21_r=DT;T21_f=Ts-DT;
   T23_r=Ts/2;T23_f=Ts/2;
else
   Td=2*Ts*(va);
   if(Ia>=0)
      if(Vc1<Vc2)
         T11_r=DT;T11_f=Td-DT;
         T13_r=Ts/2;T13_f=Ts/2;
         T21_r=Ts/2;T21_f=Ts/2;
         T23_r=Ts/2;T23_f=Ts/2;
      else
         T21_r=DT;T21_f=Td-DT;
         T23_r=Ts/2;T23_f=Ts/2;
         T11_r=Ts/2;T11_f=Ts/2;
         T13_r=Ts/2;T13_f=Ts/2;
      end
   else
      if(Vc1>Vc2)
         T11_r=DT;T11_f=Td-DT;
         T13_r=Ts/2;T13_f=Ts/2;
         T21_r=Ts/2;T21_f=Ts/2;
         T23_r=Ts/2;T23_f=Ts/2;
      else
         T21_r=DT;T21_f=Td-DT;
         T23_r=Ts/2;T23_f=Ts/2;
         T11_r=Ts/2;T11_f=Ts/2;
         T13_r=Ts/2;T13_f=Ts/2;
      end
   end

end
```

B.1.3 Nine-level H-bridge MMC code

```
function [c1,c2,c3,c4] = fcn(YC,Va,Ia,Vcap) % (upper arm switching combinations)
N=length(YC)/2;
%Nc=length(YC);
% VS=zeros(N,1);
VS=sort(Vcap);
S1=zeros(1,N);S3=zeros(1,N);
S2=zeros(1,N);S4=zeros(1,N);
if(Va>=YC(1))
   %1
   for II=1:N
      S1(II)=1;S3(II)=0;
   end
elseif(Va<YC(1)&&Va>=YC(2))
   %3/4
   if(Ia>=0)
      for II=1:N
         if(Vcap(II)==max(Vcap))
            S1(II)=1;S3(II)=1;
         else
            S1(II)=1;S3(II)=0;
         end
      end
   else
      %Ia<0
      for II=1:N
         if(Vcap(II)==min(Vcap))
            S1(II)=1;S3(II)=1;
         else
            S1(II)=1;S3(II)=0;
         end
      end
   end
elseif(Va<YC(2)&&Va>=YC(3))
   %1/2
    if(Ia>=0)
      for II=1:N
         if(Vcap(II)==VS(N)||Vcap(II)==VS(N-1))
            S1(II)=1;S3(II)=1;
```

```
            else
                S1(II)=1;S3(II)=0;
            end
        end
    else
        %Ia<0
        for II=1:N
            if(Vcap(II)==VS(1)||Vcap(II)==VS(2))
                S1(II)=1;S3(II)=1;
            else
                S1(II)=1;S3(II)=0;
            end
        end
    end
else
    %1/4
    if(Ia>=0)
        for II=1:N
            if(Vcap(II)==VS(4)||Vcap(II)==VS(3)||Vcap(II)==VS(2))
                S1(II)=1;S3(II)=1;
            else
                S1(II)=1;S3(II)=0;
            end
        end
    else
        %Ia<0
        for II=1:N
            if(Vcap(II)==VS(1)||Vcap(II)==VS(2)||Vcap(II)==VS(3))
                S1(II)=1;S3(II)=1;
            else
                S1(II)=1;S3(II)=0;
            end
        end
    end
end
c1=[S1(1) S2(1) S3(1) S4(1)];
c2=[S1(2) S2(2) S3(2) S4(2)];
c3=[S1(3) S2(3) S3(3) S4(3)];
c4=[S1(4) S2(4) S3(4) S4(4)];
```

```
function [c5,c6,c7,c8] = fcn(YC,Va2,Ia2,Vcap2) % (lower arm switching combinations)
N=length(YC)/2;
%Nc=length(YC);
% VS=zeros(1,N);
VS=sort(Vcap2);
S5=zeros(1,N);S6=zeros(1,N);
S7=zeros(1,N);S8=zeros(1,N);
if(Va2>=YC(1))
   %1
   for II=1:N
      S5(II)=1;S7(II)=0;
   end
elseif(Va2<YC(1)&&Va2>=YC(2))
   %3/4
   if(Ia2>=0)
      for II=1:N
         if(Vcap2(II)==max(Vcap2))
            S5(II)=1;S7(II)=1;
         else
            S5(II)=1;S7(II)=0;
         end
      end
   else
      %Ia2<0
      for II=1:N
         if(Vcap2(II)==min(Vcap2))
            S5(II)=1;S7(II)=1;
         else
            S5(II)=1;S7(II)=0;
         end
      end
   end
elseif(Va2<YC(2)&&Va2>=YC(3))
   %1/2
    if(Ia2>=0)
      for II=1:N
         if(Vcap2(II)==VS(N)||Vcap2(II)==VS(N-1))
            S5(II)=1;S7(II)=1;
         else
```

```
            S5(II)=1;S7(II)=0;
        end
    end
  else
    %Ia2<0
    for II=1:N
      if(Vcap2(II)==VS(1)||Vcap2(II)==VS(2))
        S5(II)=1;S7(II)=1;
      else
        S5(II)=1;S7(II)=0;
      end
    end
  end
else   %1/4
  if(Ia2>=0)
    for II=1:N
      if(Vcap2(II)==VS(4)||Vcap2(II)==VS(3)||Vcap2(II)==VS(2))
        S5(II)=1;S7(II)=1;
      else
        S5(II)=1;S7(II)=0;
      end
    end
  else
    %Ia2<0
    for II=1:N
      if(Vcap2(II)==VS(1)||Vcap2(II)==VS(2)||Vcap2(II)==VS(3))
        S5(II)=1;S7(II)=1;
      else
        S5(II)=1;S7(II)=0;
      end
    end
  end
end
c1=[S5(1) S6(1) S7(1) S8(1)];
c2=[S5(2) S6(2) S7(2) S8(2)];
c3=[S5(3) S6(3) S7(3) S8(3)];
c4=[S5(4) S6(4) S7(4) S8(4)];
```

B.2 H-bridge MMC with new control scheme simulation code

B.2.1 Five-level H-bridge MMC code

```
function [T11_r,T11_f,T13_r,T13_f, T21_r,T21_f,T23_r,T23_f,Toff] = fcn(va,Ia,Vc1,Vc2,DT,Ts)
if(va>=0.5&&va<1)
   Td=2*-DT*(1/2-va);
   if(Ia>=0)
      if(Vc1<Vc2)
         T11_r=0;T11_f=DT-0;
         T13_r=DT/2;T13_f=DT/2;
         T21_r=0;T21_f=Td-0;
         T23_r=DT/2;T23_f=DT/2;
         Toff=1;
      else
         T21_r=0;T21_f=DT-0;
         T23_r=DT/2;T23_f=DT/2;
         T11_r=0;T11_f=Td-0;
         T13_r=DT/2;T13_f=DT/2;
         Toff=1;
      end
   else
      if(Vc1>Vc2)
         T11_r=0;T11_f=DT-0;
         T13_r=DT/2;T13_f=DT/2;
         T21_r=0;T21_f=Td-0;
         T23_r=DT/2;T23_f=DT/2;
         Toff=1;
      else
         T21_r=0;T21_f=DT-0;
         T23_r=DT/2;T23_f=DT/2;
         T11_r=0;T11_f=Td-0;
         T13_r=DT/2;T13_f=DT/2;
         Toff=1;
      end
   end
elseif(va<0&&va>=-0.5)
   Td=2*DT*(0.5+va);
   if(Ia>=0)
      if(Vc1>Vc2)
      T11_r=DT/2;T11_f=DT/2;
```

```
        T13_r=Td+0;T13_f=DT-0;
        T21_r=DT/2;T21_f=DT/2;
        T23_r=DT/2;T23_f=DT/2;
        Toff=1;
        else
        T21_r=DT/2;T21_f=DT/2;
        T23_r=Td+0;T23_f=DT-0;
        T11_r=DT/2;T11_f=DT/2;
        T13_r=DT/2;T13_f=DT/2;
        Toff=1;
        end
    else
        if(Vc1<Vc2)
            T11_r=DT/2;T11_f=DT/2;
            T13_r=Td+0;T13_f=DT+0;
            T21_r=DT/2;T21_f=DT/2;
            T23_r=DT/2;T23_f=DT/2;
            Toff=1;
        else
            T21_r=DT/2;T21_f=DT/2;
            T23_r=Td+0;T23_f=DT-0;
            T11_r=DT/2;T11_f=DT/2;
            T13_r=DT/2;T13_f=DT/2;
            Toff=1;
        end
    end
elseif(va<-0.5&&va>=-1)
    Td=2*DT*(1+va);
    if(Ia>=0)
     if(Vc1>Vc2)
        T11_r=DT/2;T11_f=DT/2;
        T13_r=0;T13_f=DT-0;
        T21_r=DT/2;T21_f=DT/2;
        T23_r=Td+0;T23_f=DT-0;
        Toff=1;
     else
        T21_r=DT/2;T21_f=DT/2;
        T23_r=0;T23_f=DT-0;
        T11_r=DT/2;T11_f=DT/2;
        T13_r=Td+0;T13_f=DT-0;
```

```
        Toff=1;
      end
    else
      if(Vc1<Vc2)
        T11_r=DT/2;T11_f=DT/2;
        T13_r=0;T13_f=DT+0;
        T21_r=DT/2;T21_f=DT/2;
        T23_r=Td+0;T23_f=DT+0;
        Toff=1;
      else
        T21_r=DT/2;T21_f=DT/2;
        T23_r=0;T23_f=DT+0;
        T11_r=DT/2;T11_f=DT/2;
        T13_r=Td+0;T13_f=DT+0;
        Toff=1;
      end
    end
elseif(va>=1)
    Td=2*-DT*(1/2-va);
          T11_r=0;T11_f=DT-0;
          T13_r=DT/2;T13_f=DT/2;
          T21_r=0;T21_f=Td-0;
          T23_r=DT/2;T23_f=DT/2;
          Toff=0;

else
    Td=2*DT*(va);
    if(Ia>=0)
       if(Vc1<Vc2)
          T11_r=0;T11_f=Td-0;
          T13_r=DT/2;T13_f=DT/2;
          T21_r=DT/2;T21_f=DT/2;
          T23_r=DT/2;T23_f=DT/2;
          Toff=1;
       else
          T21_r=0;T21_f=Td-0;
          T23_r=DT/2;T23_f=DT/2;
          T11_r=DT/2;T11_f=DT/2;
          T13_r=DT/2;T13_f=DT/2;
          Toff=1;
```

```
    end
  else
    if(Vc1>Vc2)
      T11_r=0;T11_f=Td-0;
      T13_r=DT/2;T13_f=DT/2;
      T21_r=DT/2;T21_f=DT/2;
      T23_r=DT/2;T23_f=DT/2;
      Toff=1;
    else
      T21_r=0;T21_f=Td-0;
      T23_r=DT/2;T23_f=DT/2;
      T11_r=DT/2;T11_f=DT/2;
      T13_r=DT/2;T13_f=DT/2;
      Toff=1;
    end
  end
end
```

B.2.2 Nine-level H-bridge MMC code

```
function [c1,c2,c3,c4] = fcn(YC,Va,Ia,Vcap)% (upper arm switching combinations)
N=length(YC)/2;
%Nc=length(YC);
% VS=zeros(N,1);
VS=sort(Vcap);
S1=zeros(1,N);S3=zeros(1,N);
S2=zeros(1,N);S4=zeros(1,N);
if(Va>=YC(1))
    %1
    for II=1:N
        S1(II)=1;S3(II)=0;
    end
elseif(Va<YC(1)&&Va>=YC(2))
    %3/4
    if(Ia>=0)
        for II=1:N
            if(Vcap(II)==max(Vcap))
                S1(II)=1;S3(II)=1;
            else
                S1(II)=1;S3(II)=0;
            end
        end
    else
        %Ia<0
        for II=1:N
            if(Vcap(II)==min(Vcap))
                S1(II)=1;S3(II)=1;
            else
                S1(II)=1;S3(II)=0;
            end
        end
```

```
    end
elseif(Va<YC(2)&&Va>=YC(3))
    %1/2
     if(Ia>=0)
        for II=1:N
            if(Vcap(II)==VS(N)||Vcap(II)==VS(N-1))
                S1(II)=1;S3(II)=1;
            else
                S1(II)=1;S3(II)=0;
            end
        end
    else
        %Ia<0
        for II=1:N
            if(Vcap(II)==VS(1)||Vcap(II)==VS(2))
                S1(II)=1;S3(II)=1;
            else
                S1(II)=1;S3(II)=0;
            end
        end
    end
elseif(Va<YC(3)&&Va>=YC(4))
    %1/4
    if(Ia>=0)
        for II=1:N
            if(Vcap(II)==VS(4)||Vcap(II)==VS(3)||Vcap(II)==VS(2))
                S1(II)=1;S3(II)=1;
            else
                S1(II)=1;S3(II)=0;
            end
        end
    else
        %Ia<0
        for II=1:N
            if(Vcap(II)==VS(1)||Vcap(II)==VS(2)||Vcap(II)==VS(3))
                S1(II)=1;S3(II)=1;
            else
                S1(II)=1;S3(II)=0;
            end
        end
    end
elseif(Va<YC(4)&&Va>=YC(5))
    for II=1:N
        S1(II)=1;S3(II)=1;
    end
elseif(Va<YC(5)&&Va>=YC(6))
    %-1/4
    if(Ia>=0)
        for II=1:N
            if(Vcap(II)==VS(1)||Vcap(II)==VS(2)||Vcap(II)==VS(3))
                S1(II)=1;S3(II)=1;
            else
                S1(II)=0;S3(II)=1;
            end
        end
    else
        %Ia<0
        for II=1:N
            if(Vcap(II)==VS(4)||Vcap(II)==VS(3)||Vcap(II)==VS(2))
                S1(II)=1;S3(II)=1;
```

```
            else
                S1(II)=0;S3(II)=1;
            end
        end
    end
elseif(Va<YC(6)&&Va>=YC(7))
    %-/2
    if(Ia>=0)
        for II=1:N
            if(Vcap(II)==VS(1)||Vcap(II)==VS(2))
                S1(II)=1;S3(II)=1;
            else
                S1(II)=0;S3(II)=1;
            end
        end
    else
        %Ia<0
        for II=1:N
            if(Vcap(II)==VS(4)||Vcap(II)==VS(3))
                S1(II)=1;S3(II)=1;
            else
                S1(II)=0;S3(II)=1;
            end
        end
    end
elseif(Va<YC(7)&&Va>=YC(8))
    %-3/4
     if(Ia>=0)
        for II=1:N
            if(Vcap(II)==VS(1))
                S1(II)=1;S3(II)=1;
            else
                S1(II)=0;S3(II)=1;
            end
        end
    else
        %Ia<0
        for II=1:N
            if(Vcap(II)==VS(4))
                S1(II)=1;S3(II)=1;
            else
                S1(II)=0;S3(II)=1;
            end
        end
    end
else
    for II=1:N
        S1(II)=0;S3(II)=1;
    end
end
for II=1:N
    S2(II)=1-S1(II);S4(II)=1-S3(II);
end
c1=[S1(1) S2(1) S3(1) S4(1)];
c2=[S1(2) S2(2) S3(2) S4(2)];
c3=[S1(3) S2(3) S3(3) S4(3)];
c4=[S1(4) S2(4) S3(4) S4(4)];
```

```
function [c5,c6,c7,c8] = fcn(YC,Va2,Ia2,Vcap2) % (lower arm switching combinations)
N=length(YC)/2;
%Nc=length(YC);
% VS=zeros(1,N);
VS=sort(Vcap2);
S5=zeros(1,N);S6=zeros(1,N);
S7=zeros(1,N);S8=zeros(1,N);
if(Va2>=YC(1))
   %1
   for II=1:N
      S5(II)=1;S7(II)=0;
   end
elseif(Va2<YC(1)&&Va2>=YC(2))
   %3/4
   if(Ia2>=0)
      for II=1:N
         if(Vcap2(II)==max(Vcap2))
            S5(II)=1;S7(II)=1;
         else
            S5(II)=1;S7(II)=0;
         end
      end
   else
      %Ia2<0
      for II=1:N
         if(Vcap2(II)==min(Vcap2))
            S5(II)=1;S7(II)=1;
         else
            S5(II)=1;S7(II)=0;
         end
      end
   end
elseif(Va2<YC(2)&&Va2>=YC(3))
   %1/2
    if(Ia2>=0)
      for II=1:N
         if(Vcap2(II)==VS(N)||Vcap2(II)==VS(N-1))
            S5(II)=1;S7(II)=1;
         else
            S5(II)=1;S7(II)=0;
```

```
            end
        end
    else
        %Ia2<0
        for II=1:N
            if(Vcap2(II)==VS(1)||Vcap2(II)==VS(2))
                S5(II)=1;S7(II)=1;
            else
                S5(II)=1;S7(II)=0;
            end
        end
    end
elseif(Va<YC(3)&&Va>=YC(4))
    %1/4
    if(Ia2>=0)
        for II=1:N
            if(Vcap2(II)==VS(4)||Vcap2(II)==VS(3)||Vcap2(II)==VS(2))
                S5(II)=1;S7(II)=1;
            else
                S5(II)=1;S7(II)=0;
            end
        end
    else
        %Ia2<0
        for II=1:N
            if(Vcap2(II)==VS(1)||Vcap2(II)==VS(2)||Vcap2(II)==VS(3))
                S5(II)=1;S7(II)=1;
            else
                S5(II)=1;S7(II)=0;
            end
        end
end
elseif(Va2<YC(4)&&Va2>=YC(5))
    for II=1:N
        S5(II)=1;S7(II)=1;
    end
elseif(Va2<YC(5)&&Va2>=YC(6))
    %-1/4
    if(Ia2>=0)
        for II=1:N
```

```
            if(Vcap2(II)==VS(1)||Vcap2(II)==VS(2)||Vcap2(II)==VS(3))
                S5(II)=1;S7(II)=1;
            else
                S5(II)=0;S7(II)=1;
            end
        end
    else
        %Ia<0
        for II=1:N
            if(Vcap(II)==VS(4)||Vcap(II)==VS(3)||Vcap(II)==VS(2))
                S1(II)=1;S3(II)=1;
            else
                S1(II)=0;S3(II)=1;
            end
        end
    end
elseif(Va<YC(6)&&Va>=YC(7))
    %-/2
    if(Ia>=0)
        for II=1:N
            if(Vcap(II)==VS(1)||Vcap(II)==VS(2))
                S1(II)=1;S3(II)=1;
            else
                S1(II)=0;S3(II)=1;
            end
        end
    else
        %Ia<0
        for II=1:N
            if(Vcap(II)==VS(4)||Vcap(II)==VS(3))
                S1(II)=1;S3(II)=1;
            else
                S1(II)=0;S3(II)=1;
            end
        end
    end
elseif(Va<YC(7)&&Va>=YC(8))
    %-3/4
     if(Ia>=0)
        for II=1:N
```

```
            if(Vcap(II)==VS(1))
                S1(II)=1;S3(II)=1;
            else
                S1(II)=0;S3(II)=1;
            end
        end
    else
        %Ia<0
        for II=1:N
            if(Vcap(II)==VS(4))
                S1(II)=1;S3(II)=1;
            else
                S1(II)=0;S3(II)=1;
            end
        end
    end
else
    for II=1:N
        S1(II)=0;S3(II)=1;
    end
end
for II=1:N
    S2(II)=1-S1(II);S4(II)=1-S3(II);

end
c1=[S5(1) S6(1) S7(1) S8(1)];
c2=[S5(2) S6(2) S7(2) S8(2)];
c3=[S5(3) S6(3) S7(3) S8(3)];
c4=[S5(4) S6(4) S7(4) S8(4)];
```

B.2.3 DC link Post-fault recharge of H-bridge MMC

```
function y = PWM_FCN(t,u)
va=u(1);vb=u(2);vc=u(3);
Vc1=u(4);Vc2=u(5);Vc3=u(6);Vc4=u(7);Vdc1=u(8);Vdc2=u(9);Ia=u(10);Idc=u(11);
Idc2=u(12);
%SPWM Modulation
fc=2100;
xc=2*pi*fc*t;
yc1=0.5*((2/pi)*asin(sin(xc))+1);
yc2=0.5*((2/pi)*asin(sin(xc))-1);
```

```
%Balancing
Ku_max=max(Vc1,Vc2);Ku_min=min(Vc1,Vc2);
KL_max=max(Vc3,Vc4);KL_min=min(Vc3,Vc4);

%DC current
Im=1.3; Im2=0-Im;
%Capacitor voltage
Vm=120;v1=va-Vdc1*1e-3;v2=va+Vdc2*1e-3;

%Phase A
NU=[0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0];
UP=[1 0 1 0 1 0 1 0 0 0 0 0 0 0 0 0];LW=[0 0 0 0 0 0 0 0 1 0 1 0 1 0 1 0];
A=[1 0 0 1 1 0 0 1 0 0 0 0 0 0 0 0];B=[0 1 1 0 0 1 1 0 0 0 0 0 0 0 0 0];
C=[0 0 0 0 0 0 0 0 1 0 0 1 1 0 0 1];D=[0 0 0 0 0 0 0 0 0 1 1 0 0 1 1 0];
E=[1 0 1 0 1 0 1 0 1 0 0 1 1 0 0 1];G=[1 0 0 1 1 0 0 1 1 0 1 0 1 0 1 0];
H=[1 0 1 0 1 0 1 0 1 0 0 1 0 0 0 0];I=[1 0 0 1 0 0 0 0 1 0 1 0 1 0 1 0];
J=[1 0 1 0 1 0 1 0 0 0 0 0 1 0 0 1];K=[0 0 0 0 1 0 0 1 1 0 1 0 1 0 1 0];
if(va>=0)
   if(Vdc1<Vm)
      if(Idc<Im)

            if(KL_max>120)
              sa=E;
            else
               if(Vc3==KL_max)
               sa=A;
               else
                  sa=A;
               end
            end
      else
         sa=NU;
      end
   else
   sa=NU;
   end
else
   if(Vdc2<Vm)
      if(Idc2<Im)
```

```
            if(Ku_max>120)
               sa=G;
            else
               if(Ku_max==Vc1)
               sa=C;
               else
                  sa=C;
               end
            end
        else
            sa=NU;
        end
    else
        sa=NU;
    end
end
y =sa;
```

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Appendix D Summary of relevant Published Work by Author

[1] Chao Chen, G. P. Adam, S. J. Finney, and B. W. Williams, "Post–DC Fault Recharging of the H-bridge Modular Multilevel Converter," The IET conference on AC and DC power transmission (ACDC 2012), Birmingham, 2012.

Abstract

This paper presents a new recharging strategy for the DC link capacitors of the H-bridge modular multilevel converter (HB-M2C) following DC side faults. The recharging strategy investigated in this paper focuses on the charging algorithm that ensures a controlled charge of the DC link capacitors, while ensuring that voltages across H-bridge cell capacitors remain balanced, and within the switching devices operating limits. This control strategy may limit any potential inrush current from AC side during re-energizing of the DC link following DC side fault, without the need of any external circuitry or charging resistors. This may improve the fast recovery of the power networks from DC side fault and minimize the impact on the AC grids. To demonstrate the technical feasibility of the proposed recharging scheme, an H-bridge modular multilevel converter with reverse power blocking capability is simulated.

[2] Chao Chen, G. P. Adam, S. J. Finney, and B. W. Williams, "DC Power Network Post-fault Recharging with an H-bridge Cascaded Multilevel Converter," Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE, Long Beach, 2013.

Abstract

This paper proposes an algorithm for controlled recharge (from the ac side) of the dc link capacitors of a H-bridge cascaded multilevel converter, while ensuring that the voltages across H-bridge cell capacitors remain balanced and tightly within their operating limits. The proposed recharging scheme potentially eliminates any external circuitry needed to start and shutdown the dc grid, and restart following a dc fault. Therefore, it may facilitate HVDC network fast recovery from the DC side faults, with minimal impact on the ac side and risk of power converter failure due to current

surge or voltage sag. In addition, this paper presents mathematical analysis that can be used in the development and understanding of DC link capacitor charging and its associated effects. Simulations from detailed switch and average models of the H-bridge cascaded converter are used to validate the proposed charging and discharging algorithm.

[3] Chao Chen, G. P. Adam, S. J. Finney, and B. W. Williams, "H-bridge Modular Multilevel Converter: control strategy for improved DC fault ride-through capability without converter blocking," IEEE Transactions on Power Electronics, submitted.

Abstract

This paper presents a control scheme that separates control of the fundamental current associated with AC power control from the DC and harmonic components in the arms of the H-bridge modular multilevel converter (MMC). Additionally, this control scheme fully exploits the subtractive and additive switch states of the H-bridge MMC to maintain capacitor voltage balance when the converter DC link voltage collapses during DC faults. The significance of this control scheme is that it permits the H-bridge MMC to ride through DC faults without the need for converter blocking, as is presented in the open literature. This paper provides comprehensive discussion of MMC fundamental theory, including a logical mathematical derivation of the relationships that governed its operation and modulation. The validity of the presented control scheme is confirmed using simulations and experimentation.

[4] Chao Chen, G. P. Adam, S. J. Finney, and B. W. Williams, "Full-bridge Modular Multilevel Converter with Extended Operating Range, Improved DC Fault Ride-Through, and Controlled Recharge of the DC link Cable Following DC Fault Clearance," IEEE Transactions on Power Electronics, submitted.

Abstract

This paper investigates the possibility of controlled survival and recovery of the full-bridge modular multilevel converter (FB-MMC) high-voltage DC transmission system during DC side faults, without exposing the converter switching devices to risk of failure or collapse of the connected AC networks. This is achieved by

controlling the arm currents and voltages, and fully exploiting the bipolar capability of the FB-MMC cells to control operation of the VSC-HVDC link with variable DC link voltage from 0 to rated DC voltage. In this manner, the risk of uncontrolled AC current in-feed to the DC side is avoided, with both HVDC converter stations not blocked but operational during the entire DC fault period. This research may have significant implication in the development of overhead HVDC links and multi-terminal DC grids, especially when DC circuit breakers can be replaced by relatively cheap low-voltage isolators. Besides DC fault survival, this paper presents the possibility operating the FB-MMC from bi-polar DC link voltages; thus, creating the possibility of complex hybrid DC grids with reversible DC link voltage where conventional line commutated current source converters can operate alongside voltage source converters. Operation of the FB-MMC with reversible DC link voltage is validated using simulations and experimentation, while the DC fault survival is validated using simulations. The results are discussed, with major findings highlighted.