University of Strathclyde

Department of Electronic and Electrical Engineering

Protection Strategy in Active DC Power Distribution Networks

by

Chunpeng Li

A thesis presented in fulfilment of the
requirements for the degree of

Doctor of Philosophy

2020

This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

Abstract

Environmental incentives to combat climate change are providing the motivation to improve the energy efficiency of power distribution systems and integrate state-of-the-art renewable technologies. DC distribution networks are receiving considerable attention in the literature because they offer a simple and flexible interface between these modern resources and consumers. However, many technical challenges relating to the design and standardisation of DC protection devices still exist that must be overcome prior to widespread adoption. Since DC fault current develops rapidly, many high-speed protection schemes tailored for DC networks have been proposed. However, few of them have considered the difficulties in practical implementation. This thesis will present the implementation challenges and propose corresponding protection schemes to address the issues.

In seeking to achieve this aim, the work presented within this thesis makes three main contributions. This thesis has firstly improved the reliability of the high-speed DC differential protection scheme. The main implementation challenge of this scheme is that a short time synchronisation error may cause a significant current difference error, resulting in a false-trip problem when a fault occurs outside the protected zone. This thesis has proposed a "multi-sample differential (MSD) protection scheme" to ensure the protection stability for external zone faults (i.e., the relays must not operate) whilst maintaining sensitivity for internal zone faults (i.e., the relays must operate) by examining multiples measurement samples.

Secondly, the difficulty in realising high-speed DC distance protection is that measurement of rate-of-change of current can be severely affected by even low-level noise, resulting in a failure in fault detection. This thesis has presented the methodology for selecting the appropriate sampling time of the numerical derivative as well as the cut-off frequency of low-pass current measurement filters.

Although high-speed protection schemes can effectively isolate faults quickly, their implementation requires many advanced devices, which may not be economical for low-power and low-cost DC networks. Finally, this thesis has proposed a "modulated low fault-energy (MLE) protection scheme" that employs fault current limiters (FCL) at the grid energy sources and mechanical circuit breakers (MCB) elsewhere throughout the distributed network. This deployment can constrain the fault current to a low-energy level that enables a longer time window for the downstream MCBs to realise protection with a lower total implementation cost.

Drawing conclusions from this PhD research, the author advocates that more consideration should be given to implementation challenges when designing protection schemes in DC distribution networks. Excessive pursuit of ultrafast fault isolation speeds can lead to over-cost and protection instability issues in practice. A prospective protection scheme must compromise between the high-speed protection requirements in theory and the reliable but economical requirements in practice, to accelerate the realisation of large-scale DC grids in future.

Contents

List of Figures

List of Tables

Glossary of Abbreviations

AC	Alternating Current
ADC	Analogue-to-Digital Converter
ASIC	Application Specific Integrated Circuit
CT	Current Transformer
DAB	Dual Active Bridge
DC	Direct Current
DG	Distributed Generator
di/dt	Rate-of-Change of Current
EMI	Electromagnetic Interference
ESS	Energy Storage System
ETO	Emitter Turn-Off Thyristor
EV	Electric Vehicle
FCL	Fault Current Limiter
FIR	Finite Impulse Response
FLC	Fixed Latest Channel
FOCS	Fibre-Optic Current Sensors
FPGA	Field Programmable Gate Array
GPS	Global Positioning System
HCB	Hybrid Circuit Breaker
HRF	High-Resistance Fault
HVDC	High-Voltage Direct Current
IDMT	Inverse Definite Minimum Time
IGBT	Insulated Gate Bipolar Transistor
KVL	Kirchhoff's Voltage Law
LCC	Line-Commutated Converters
LED	Light-Emitting Diode
LoM	Loss-of-Main
LRF	Low-Resistance Fault
LVDC	Low-Voltage Direct Current
MCB	Mechanical Circuit Breakers
MG	Microgrid
MLE	Modulated Low fault-Energy
MMC	Modular Multi-Level Converter

MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPPT	Maximum Power Point Tracking
MSD	Multi-Sample Differential
MVDC	Medium-Voltage Direct Current
NF	No-Fault
NTP	Network Time Protocol
OSF	Optimised Sampling Frequency
PEC	Power Electronic Converter
PTP	Precision Time Protocol
PV	Photovoltaic
PWM	Pulse Width Modulation
RES	Renewable Energy Resource
RoCoF	Rate-of-Change of Frequency
SNR	Signal-Noise-Ratio
SSCB	Solid-State Circuit Breaker
SSFCC	Solid-State Fault Current Controller
TDL	Tapped Delay Line
TES	Time Synchronisation Error
ULC	Unfixed Latest Channel
VSC	Voltage Source Converter
VSM	Virtual Synchronous Machine
VT	Voltage Transformer
WT	Wind Turbine

Acknowledgements

I would like to offer sincere thanks to Prof. Graeme Burt for the opportunity to undertake this research work. Sincerest gratitude and thanks also go to Dr. Patrick Norman for his patient guidance, research suggestions, technical support, and kind supervision. I would like especially express my gratitude to Dr. Puran Rakhra for his friendly help on my research and great advice on my writing skills. I could never achieve this without their help.

Thanks go to all my colleagues within the UTC research team for their input to the research project. My gratitude extends to the University and the National Physical Laboratory (NPL) for their technical and financial support over the duration of this project.

To my family and friends, thank you for all your encouragement and support over the years. I will always remember the happiness I have enjoyed with my friends in Glasgow and be proud of playing a role in our rock band. Special thanks go to my parents, Jinxiang Li and Ying Pan. Thank you so much for all your understanding and supporting my life during my long period of study. It is all your encouragement that allows me to focus on the work I love without any worries. This thesis is dedicated to them.

Chapter 1

Introduction

1.1 Motivation and Objectives

In recent years, as the use of fossil fuels has an increasingly serious impact on the environment, remedial policies addressing environmental and energy issues have been pursued globally. The associated technologies for renewable elements[1] are rapidly becoming research hotspots and present great prospects. The world's major governments are strongly ambitious in achieving a cleaner and sustainable future. For example, Danmark targets to reach 50% renewable energy by 2030 as the first step, and eventually achieve 100% clean energy by 2050 [1]. In the UK, the energy contribution from the renewable energy resources (RES) to the total energy consumption has reached 15% by 2020 as planned [2], and the UK government also announced that diesel and petrol vehicle sale would be banned by 2040 [3]. China, as a large manufacturing country, has the world's largest electricity production (6.5×10^{15} Wh in 2017). Even if achieving clean energy reform is challenging, the Chinese government has proposed the plan yet that non-fossil energy in total primary energy consumption will increase from 15% to 20% by 2030 [4].

With the participation of many renewable energy sources (RES), the traditional

[1]Renewable element is a general term for electrical components related to renewable sources and clean energy, e.g., PV panels, wind turbines, energy storage systems, electrical vehicles, etc.

AC power grid is transforming from centralised to decentralised generation network [5]. The decentralised structure will allow the customers to generate electricity for their own use or even make profits by selling electricity to the grid. Meanwhile, the decentralised structure enables a wide use of clean energy that may make a great contribution to reducing carbon emission. To exploit the advantages, the revolution of decentralised power generation is rolling out rapidly. Nowadays, many of the world's leading companies and manufacturers are taking action to promote progress. The top PV panel manufacturers, such as SunPower [6] and Tesla [7], are selling household roof solar systems with a grid connection solution that could reduce household electricity cost by up to 60%. Concerning the electric vehicle (EV) industry, Tesla has constructed the Gigafactory in Shanghai which will produce 500,000 electric vehicles (EV) each year after its completion [8]. In the foreseeable future, many novel applications are being installed into the power system, such as photovoltaic (PV) generators, wind turbines, energy storage systems (ESS), EV chargers, etc.

In order to integrate renewable elements into the power system, advanced power electronic converters (PEC) are required to match the electricity forms between sources, network and loads [9]. In the modern power system, an increasing number of converter stations are operating for integrating large-scale solar and wind farms in the main AC grid. However, the participation of PEC-based distributed generators (DG) may have negative impacts on the main AC grid. The traditional machinery generators normally provide enough rotational inertia to maintain the rate-of-change of frequency (RoCoF) to a relatively low value during power unbalance conditions. Since PEC-based RESs do not provide rotational inertia, large-scale deployment of RESs may lead to faster frequency changes during power change events [10, 11]. To prevent loss-of-mains (LoM) protection cutting off the RESs and aggravating the frequency drop during system turbulence, the national grid has raised the LoM trip threshold from 0.125 to 1 Hz/s [12]. Additionally, the use of RESs may lead to a problem of reduced sensitivity of the protection system [13]. In the traditional centralised power system, the short-circuit fault will be isolated when the feed-in current is higher than a pre-set threshold. The

participated DGs may contribute a part of fault current thus reducing the current fed from the main grid, and cause blinding of feeder protection [14]. Furthermore, the interconnection of many PEC-based DGs may lead to a decline in power quality [15]. Since the converter is usually composed of switching devices, it can cause harmonics which result in waveform distortion. The low-quality electricity may make electronic devices malfunction or could even damage electrical equipment [16].

In order to optimise the connections of DGs and mitigate their drawbacks discussed above, the concept of microgrid (MG) has been proposed. A microgrid is a small power generation and distribution network sources, generally composed of distributed power, energy storage devices, energy conversion devices, related loads, monitoring and protection devices [17]. A microgrid normally connects and operates synchronously with the main AC grid utility, but can also be disconnected and be working in an "islanded" mode [18]. Microgrids may operate in the form of AC, DC or hybrid AC/DC power, but it is still debated which power form is more suitable for future microgrids [19]. AC supporters believe that the controversy between Edison and Tesla in the late 19th century has already proved that AC has greater advantages [20], and the existing home appliances and electrical equipment are mostly designed for AC systems. However, DC supporters argue that the AC system won because of the lack of power electronics technology at that time, and the use of AC was only a compromise on the need to use transformers for long-distance transmission. In recent years, due to the progress of power electronics technology, PECs can flexibly convert between AC and DC and regulate voltage, thus voltage transformation is no longer a decisive concern. HVDC transmission system has been proved to have many advantages and has been widely used in long-distance transmission projects [21]. In distribution networks, since many renewable elements and electronic loads inherently operate with DC power, DC systems may have great prospective to become the right platform for the next-generation power distribution networks.

The DC power distribution network is generally named as a low-voltage direct cur-

rent (LVDC) system. An LVDC system normally integrates renewable elements and loads through PECs and may be interconnected to the main AC grid through a DC-AC PEC. It also typically features local control and power management systems, and thus is commonly regarded as an independent source or load in the main AC grid. When an LVDC system has enough power generation capacity to supply all local loads, it can be disconnected from the main grid and operated in the "islanded" mode. The LVDC systems with islanding operation function can also be called DC microgrids (DCMG).

An example of DCMG is shown in Figure 1.1 to illustrate the basic network structure. Typical applications for DCMG may include renewable elements and DC electronic devices, such as PV panels, wind turbines (WT), ESSs, LED lighting systems, residential electronic loads, etc. The sources and loads are connected to the DCMG through suitable converters according to their features. These converters are configured with local and centralised control algorithms to provide power balance regulation and energy management. Comparing the traditional method of directly connecting DGs to

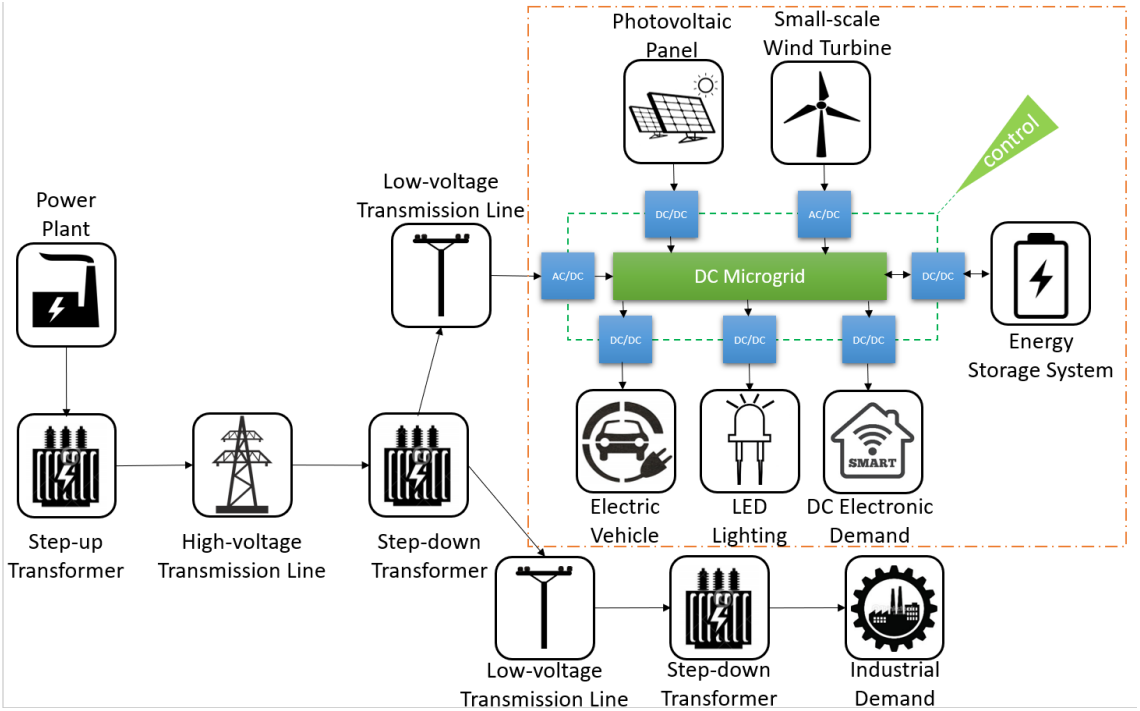

Figure 1.1: Schematic diagram of an example DC microgrid [22].

the main AC grid, the use of DCMG can exploit the following benefits.

(i) *Deploying DCMG can reduce the number of required power conversion stages.* Most civil electrical devices inherently operate in DC, such as EV batteries, energy storage batteries, LED lights, heating equipment, etc. At the same time, most of the RESs operate in DC mode or must be converted into DC mode. If the traditional AC network is adopted, the process of DC-AC-DC must be experienced from power supply to load. This process will increase the cost of the converter and cause additional energy loss. However, DCMGs could integrate most RESs and loads through DC-DC stages. As DC-DC PECs are typically simpler and more efficient than DC-AC PECs [23], using DCMGs would save much investment and energy dissipation during power conversions.

(ii) *DCMG may be more suitable for connecting plug-and-play renewable elements.* Integrating DC elements into an AC network requires both voltage and frequency control, which requires complex control methods to adjust active and reactive power. However, in a DC microgrid, power can be controlled by adjusting voltage only, and synchronisation is not of concern. Adopting simple control strategies is conducive to realising convenient or even plug-and-play applications. Additionally, since a DCMG has an independent energy management system, excess generated energy by the RESs may be stored in local ESS devices. The excess energy no longer has to be exported to the main grid thus DCMGs may reduce the energy losses of power transmission. During peak hours (e.g., when many EVs require fast charging), the main AC grid and the local ESSs could provide energy together which may also reduce generation pressure of the main grid.

(iii) *Employing DCMG can mitigate the negative effects of DGs on the main grid.* The direct connection of DGs to the AC grid may reduce system stability and cause protection blinding problems. The DCMG is an independent small network coupled with the AC grid that can prevent the propagation of disturbances between systems [9]. When insufficient grid power is detected (e.g., system fre-

quency is falling sharply, or electricity price is increasing), the interface PEC may automatically restrain the drawn power to decrease the risk of system collapse. With the local control strategy, DCMG may consume the locally stored energy in priority or even shed the inessential loads. Furthermore, during severe fault conditions in the DCMG, the interface PEC may block the fault current in-feeding in order to prevent any adverse impact on the main AC grid. A DCMG is usually equipped with an independent protection system to selectively isolate internal faults.

(iv) *DCMG may maintain energy supply in a case grid outage.*
The use of RESs and ESSs enable the DCMG operating in the islanded mode during the main AC grid failure conditions. The microgrid controllers could regulate the bus voltages and allocate the energy to the demands according to the levels of importance. During short power interruption, the ESSs may provide backup energy to the full loads until the main grid is recovered. In the case of long-term grid failure, the centralised controller may abandon some lower priority demands to remain the vital loads available, such as lifts and emergency lighting devices. This may reduce the risk of an entire power system outage and prevent hazards under extreme situations, such as grid black-out and natural disasters.

Although the application of LVDC networks may bring the above benefits to the power system, they not yet been widely used in infrastructure. To date, LVDC is only applied in small-scale networks including electronic equipment and critical networks. The power allocation in many electronic facilities, such as personal laptops and mobile phones, can generally be considered as using a micro LVDC network. An inner power controller is usually employed to convert the power from the AC socket to different DC voltages and energise the corresponding chips and components. When the facility is unplugged, the battery must take over and ensure the power supply is uninterrupted. LVDC networks have also been applied in some critical applications, such as telecommunication (48V), aircraft (28-270 V), data centre and marine power systems [24, 25]. With recent advances in complementary technologies such as PECs, RESs, ESSs, EVs

and LED lighting systems, it is expected that LVDC for residential use would gain more popularity as a result of key performance advantages over more conventional AC distribution in future [9]. The fundamentals of a DC microgrid are reviewed in more detail in Chapter 2, and a model of DC microgrid has been built in Chapter 4 to better characterise the system response under fault conditions.

Before a more widespread LVDC application can be achieved, comprehensive standards and methodologies must be established to realise safe performance and reliable operation. One of the major challenges is to develop standardised protection technologies. As the fault response of a DC system fault is different from the AC grid fault, most of the conventional protection methods are not available for LVDC systems. The integration of PECs with capacitive input and output filters can result in extremely high-magnitude transient currents in the event of DC network faults [26]. As significantly large fault current transients increase the risk of damaging vulnerable elements of PECs, it is commonly proposed that DC faults must be isolated prior to the transient peak using ultra-fast protection hardware [25-27]. The peak of fault transient usually appears in several microseconds, such as a typical 2 ms [27], which is too fast to be achievable using conventional protection devices in the AC system (typically over 60 ms) [26]. Accordingly, a series of fast operating devices have been developed to realise a faster operation speed and shorter fault clearing time for LVDC systems, including measurement sensors, processing relays, solid-state circuit breakers (SSCB), and communication links. However, these devices may have physical limitations that must be considered for designing protection schemes, such as measurement noise, processing speed, and communication delay. Meanwhile, the hardware cost is also a considerable aspect of future practical use. Furthermore, in contrast to established HVDC networks, LVDC systems are often multi-terminal networks, requiring more complex fault location and protection discrimination. The requirement of ultra-fast protection speed may hinder protection coordination to be realised in a large-scale LVDC network. Conventional AC protection coordination may be realised by setting a longer operation time on upstream devices which allows the downstream devices to isolate a minimum faulty

zone, such as IDMT [28] and PMAR (re-closer + fuse) [29] protection. However, this strategy is often not feasible for DC networks, since protection system operation before the fault current transient peak is desirable for these systems.

From the literature, many tailored protection schemes are proposed to realise protection discrimination with ultrafast speed. These protection methods can detect and locate the fault at the initiation of the fault, using smart algorithms to analyse or compare the voltage and current responses. Typical high-speed protection schemes can be catalogued into three types that are overcurrent, differential, and distance protection methods, which will be reviewed in detail in Chapter 3.

1.2 Justification of Research and Thesis Outline

Whilst many researchers have made substantial efforts in developing theoretically effective LVDC protection strategies, more research is needed to consider the impact of practical metrology constraints on these schemes. From a review of the literature (Chapter 3) and model-based analysis of DC microgrid systems' fault response (Chapter 4), the pertinent metrology issues and requirements are identified and described in Section 3.5 of this thesis, before potential solutions are then proposed and evaluated.

More specifically, time synchronisation error (TSE) is identified as a key measurement challenge for high-speed differential protection. As the DC fault develops with a steep slope, a very short TSE may still cause a high current difference that can result in false trips of the protection system. In Chapter 5, a novel differential protection algorithm, the Multiple Sample Differential (MSD) protection scheme, is proposed to overcome the stability issue caused by the TSE.

For schemes that require a measurement of the signal rate-of-change, such as high-speed overcurrent and distance protection, obtaining real-time derivatives of signals is a

challenge. The rate-of-change measurement includes voltage derivative ($\mathrm{d}v/\mathrm{d}t$), current derivative ($\mathrm{d}i/\mathrm{d}t$) and even second-order derivatives ($\mathrm{d}^2v/\mathrm{d}t^2$ and $\mathrm{d}^2i/\mathrm{d}t^2$), however, the computation of derivative is very sensitive to even low-level noise and very small interferences may lead to a measurement failure. Chapter 6 presents optimisation methods to obtain effective rate-of-change of measurements.

Furthermore, in general, the reliability of high-speed protection is vulnerable to electromagnetic interference (EMI) and coding error that are ubiquitous in reality. Since the time-decision window of high-speed protection is very short, high-speed schemes may have poor tolerance to the interference and error, thus leading to false trips. Even if these problems could be mitigated with smart algorithms and advanced hardware, the cost of the protection system will be greatly increased. Accordingly, high-speed protection may be usable for the critical high-power DC networks but is less attractive for low-power systems. Alternatively, protection schemes based on fault current limiters (FCL) have been proposed in the literature as a means to avoid the need for ultrafast fault clearance. FCLs may be implemented using a full-bridge converter [30], superconducting fault current limiter [31], or solid-state fault current limiter [32]. The use of FCL allows downstream relays to have a longer time-decision window to realise protection coordination. This also enables the use of conventional mechanical circuit breakers (MCB), facilitating a reduction in the number of SSCBs needed to reduce cost. The longer time window may also improve the tolerance ability to measurement errors of the protection relays, and hence better protection stability can be achieved. However, under the "FCL+MCBs" structure, the corresponding protection coordination of MCBs has not been sufficiently investigated. The protection coordination strategies in existing literature are still based on current comparisons [32, 33], but these may still require complex communication links for multi-terminal LVDC distribution networks. Inspired by inverse definite minimum time (IDMT) protection in conventional AC systems, a novel non-communication coordinated protection scheme, called "Modulated Low Fault-Energy (MLE) Protection" is proposed in Chapter 7. The MLE protection scheme is an effective design of graded overcurrent protection for current-limited DC

systems. The fault current limiting is implemented by modulating a solid-state SSCB whilst the MCBs operate with a derived numerical methodology to achieve protection coordination.

Finally, the main contributions of this thesis are summarised in Chapter 8. In addition, conclusions on the PhD research are drawn, and candidate areas for further research are suggested and discussed.

1.3 Summary of Key Contributions

The key contributions of this thesis can be summarised as follows:

- The first-of-its-kind formal capture of the metrology challenges associated with the practical implementation of DC protection schemes is presented. Due to the different characteristics of DC fault responses, many high-speed protection schemes have been proposed to isolate short-circuit faults in an ultrafast speed. However, the schemes must be supported by high-fidelity measurement systems, the challenges of which had not been previously identified in the research literature.

- A new protection scheme, "multi-sample differential (MSD) protection scheme" is proposed in order to address the instability issue caused by time synchronisation errors in modern ultra-fast high-speed DC differential protection schemes. Whilst conventional methods may mal-operate when a fault out-with the protected zone occurs, the MSD protection is shown to remain stable, with only a short reduction in operating speed for faults within the protected zone. The effectiveness of this method is verified using both simulation models and a dedicated benchtop hardware rig.

- Methods to optimise the accuracy of measuring the rate-of-change of current ($\mathrm{d}i/\mathrm{d}t$) for high speed DC non-unit protection schemes are proposed. These so-

lutions address key challenges related to the sensitivity of $\mathrm{d}i/\mathrm{d}t$ measurements to even low levels of noise, which may cause a protection failure. The proposed methods enable the selection of an optimised sampling frequency and the application of suitable finite impulse response (FIR) filters. The design principles are obtained by mathematical derivation and their effectiveness is validated with MATLAB simulations.

- A new protection scheme, "modulated low fault-energy (MLE) protection scheme", is proposed in Chapter 7 to achieve moderate-speed protection coordination in DC networks. Whilst optimised high-speed protection schemes are effective, many advanced devices must be employed, which may result in unacceptably high costs for low-power LVDC applications. Inspired by the IDMT graded overcurrent protection for AC grids, the proposed method employs an "FCL + MCBs" structure, where each device operates independently in terms of local measurement, eliminating the need for complex communication links. This effectiveness of this method is validated with both MATLAB/Simulink modelling and FPGA-based hardware tests on bench-top DC rigs.

1.4 Publications

- C. Li, P. Rakhra, P. Norman, G. Burt, P. Clarkson, "Metrology requirements of state-of-the-art protection schemes for DC microgrids," *IET the Journal of Engineering*, vol. 2018, no. 15, pp. 987-992, Oct 2018. (3rd year)

- C. Li, P. Rakhra, P. Norman, G. Burt, and P. Clarkson, "Multi-sample differential protection," Sep 2019. [*Submitted to IEEE Journal of Emerging and Selected Topics in Power Electronics*] (4th year)

- C. Li, P. Rakhra, P. Norman, P. Niewczas, G. Burt, and P. Clarkson, "Practical computation of $\mathrm{d}i/\mathrm{d}t$ for high-speed protection of DC microgrids", in *IEEE Second International Conference on DC Microgrid, Nuremberg, Germany*, pp. 153-159, Jun 2017. (2nd year)

- C. Li, P. Rakhra, P. Norman, P. Niewczas, G. Burt and P. Clarkson, "Modulated Low Fault-Energy Protection Scheme for DC Smart Grids," in *IEEE Trans. on Smart Grid*, vol. 11, no. 1, pp. 84-94, Jan 2020. (3rd year)

Chapter 2

Overview of DC Power Networks

With regard to traditional AC systems, DC power networks consist of much-specialised hardware and control strategies [34]. Before conducting the research on DC network protection, it is necessary to study the fundamental operating principles of the DC networks according to the literature. In this chapter, the author will briefly introduce the necessary background, including the network fundamentals, frequently used components, power electronic converters and power management control methods.

2.1 LVDC Network Fundamentals

2.1.1 Network Topologies

In general, typical topologies of DC distribution network can be classified into single-bus and multi-bus configurations [9]. The single-bus LVDC network is a simple topology which is commonly applied in compact networks. As shown in Figure 2.1, both sources and loads are connected directly on a single bus forming a compact DC network. Since a single-bus LVDC is easily implemented, it has already been applied in many small-scale DC applications. As shown in Figure 2.2, the hybrid wind-solar street lighting system is a typical example that integrates a small-scale PV panel, a wind turbine, and an ESS onto a signal DC bus to energise the street lights [35, 36]. Many power management algorithms have been developed for ensuring lighting throughout a complete

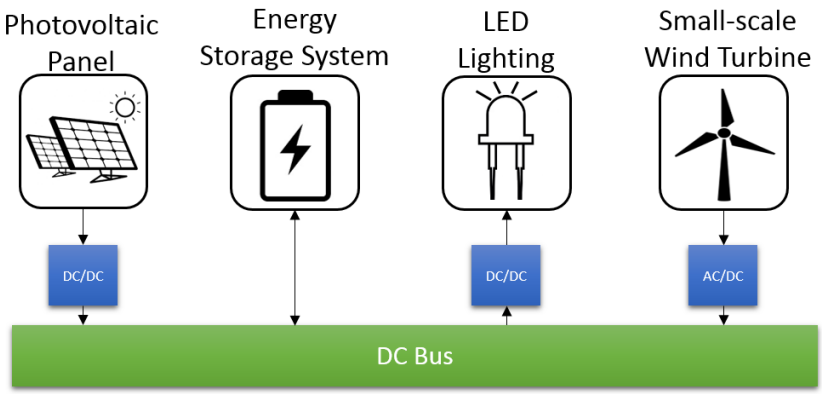

Figure 2.1: Single bus DCMG with ESS directly connected to the common DC bus.

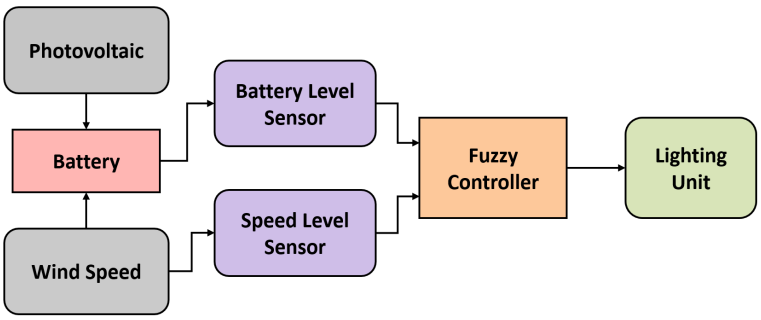

Figure 2.2: Example of hybrid wind-solar street lighting system.

night [37, 38]. Besides, this single-bus LVDC configuration is commonly applied in the traditional negative 48 V telecom power system as shown in Figure 2.3.

However, as the battery is directly connected to the main bus, the voltage on the DC bus depends mostly on the state of charge (SoC) [39], which may limit its application only to singular bus systems [40]. Additionally, as the SoC of the ESS is unregulated, the frequent charging and discharging may accelerate the wear of the stationary battery [41]. Accordingly, the connection of the ESS through a dedicated DC-DC converter to regulate the voltage on the DC bus (Figure 2.4) enables more flexible control strategies and multiple DC bus configurations.

Multiple-bus DCMGs, as shown in Figure 2.5, are deployed to realise large-scale networks with higher power availability and system reliability [9]. The multiple DC

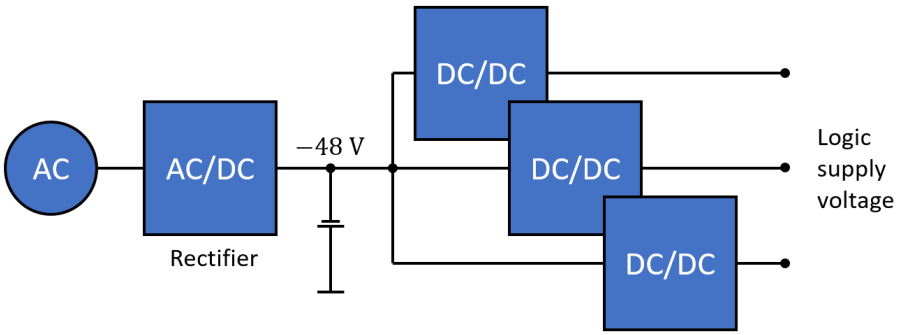

Figure 2.3: Example of basic telecom power system.

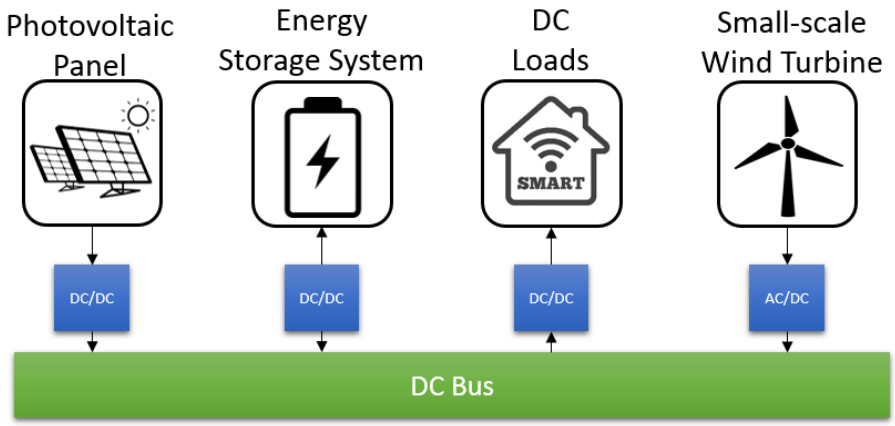

Figure 2.4: Single bus DCMG with ESS connected to the common DC bus through a dedicated converter.

bus topology enables energy complementary between DC buses. It is not necessary to balance the power with a single bus, whilst the remote sources or loads may be available for regulating the local bus voltage. In addition, DC power systems can be made more reliable by using multiple buses since this configuration may provide redundancy during fault conditions. After a fault is cleared, multiple configuration options may be available for maintaining the power supply to the loads [42].

Multiple bus LVDC networks can be designed as different topologies, typically including radial and ring structures. The radial structure LVDC networks integrate multiple "DC clusters" onto one common bus, as shown in Figure 2.6. In [43], Dragicevic has presented that radial structure has good flexibility for reconfiguring the existing

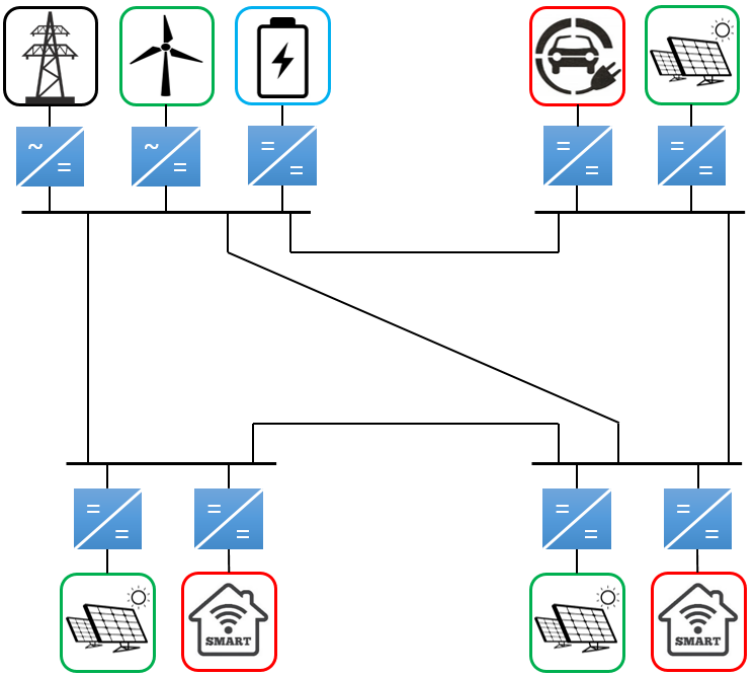

Figure 2.5: Multiple bus DCMG with all components connected through dedicated converter interfaces.

DC architectures, and in each DC cluster, the radial structure can also be deployed to implement hierarchical networks with different voltage levels using power electronic converters. Based on this structure, many researchers have proposed associated hierarchical control strategies to ensure reliable operation of multiple DC clusters [44-48]. On the other hand, the ring-bus LVDC structure, as shown in Figure 2.7, is also a hotspot of research because it has a better resilience during fault conditions [49]. After a fault is detected and cleared by the nearest protection devices, the power to other loads can still be supplied through the alternative path. Many fault detection schemes are presented in the literature which isolate the minimum abnormal segment in ring-bus LVDC networks [49-51].

2.1.2 Voltage-Level Selection

According to the IEC 60038 standard, LVDC systems are defined as those with voltage levels below 1500 V, whilst the voltage levels for different appliances in LVDC networks

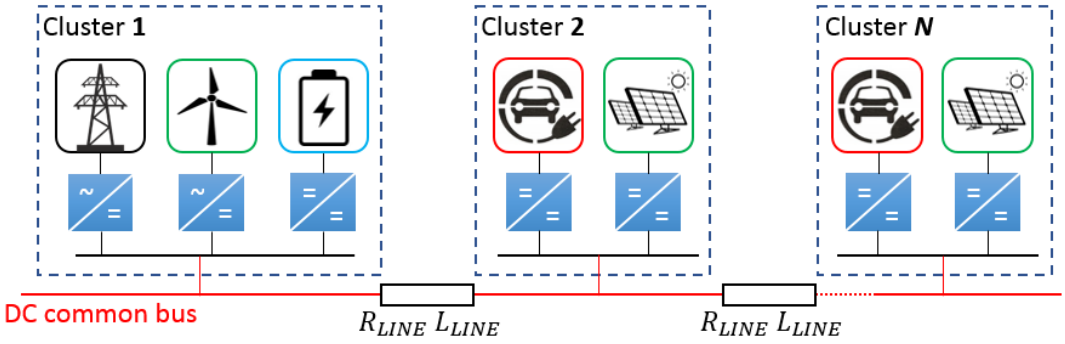

Figure 2.6: Radial structure DC network integrating multiple MG clusters.

Table 2.1: Typical voltage-level selection scheme in LVDC networks.

Power Level	Typical Power	Voltage Selection	Typical Applications and Components
Low-power Loads	< 0.4 kW	24–48 V	Electronic devices (Wi-Fi routers, phone chargers, computers, TVs, DVD players, Hi-Fi systems, led lights)
Medium-power Element	0.4–10 kW	230–400 V	Appliances in kitchens (e.g., stove, oven, dishwasher) and laundry rooms (e.g., washing machine, dryer, iron).
High-power Elements	≥ 10 kW	≥ 538 V	DGs (PV panels, WTs), ESSs, elevators, and EV chargers.

are required to be specified. The lack of a commonly agreed voltage standard impedes a wider implementation of LVDC networks [24]. With a compromise between grid compatibility, safety and efficiency, Rodriguez-Diaz [24] has suggested three voltage ranges for the DC sources and loads in terms of their rated power (summarised in Table 2.1).

2.1.3 Grid-Tied Mode and Islanded Operation Mode

LVDC networks may operate with the AC-grid connected, or in islanded mode (the latter are named DC microgrids (DCMG) [52]. Regarding the grid-tied mode, DCMGs can be interconnected with existing AC infrastructures through a DC-AC converter interface. Since the AC grid generally has a large capacity for balancing power, the grid-tied DCMG may present better power availability [53]. However, during a distur-

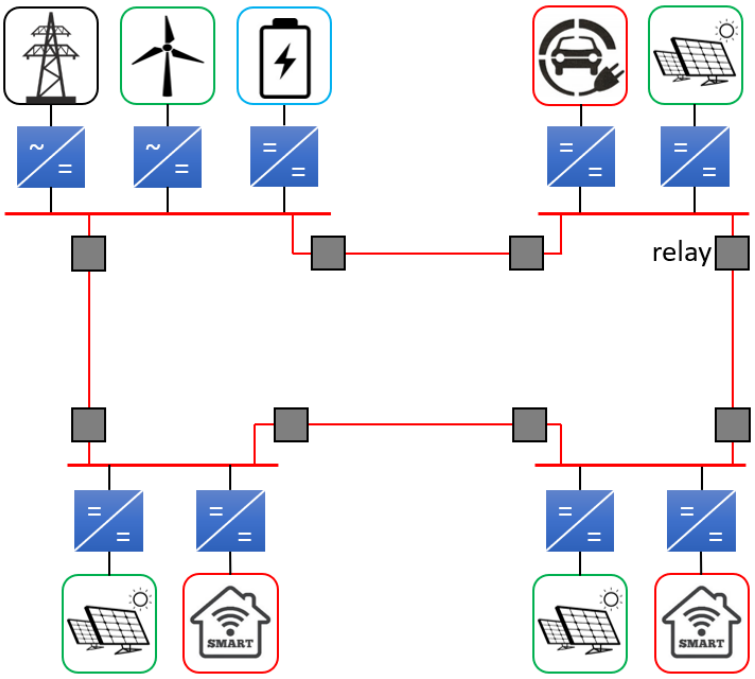

Figure 2.7: Ring structure DC networks.

bance event on the AC grid or where the customer cannot remain connected to the main grid (e.g., remote developing regions [54]), a DCMG may operate in islanded mode only relying on the internal energy resources (DGs and ESSs).

The grid-tied DCMG requires AC-DC converters connected at the interface of the AC and DC networks. As the interface converter may be assigned to regulate the main voltage and balance power for DCMG as shown in Figure 2.8 (a), it is normally required to have a sufficient capacity to ensure the power supply under the full-load, no DG condition. Accordingly, DCMG instability should not occur as a result of power shortage. To maximise the use of clean energy, the RES may generate the maximum power if possible, and the ESSs should store the surplus power and peak shift for the AC grid. When the DCMG has a high risk of loss-of-main, it may be necessary for the ESS to store backup energy.

The off-grid DCMG must ensure the long-term power generation is higher than

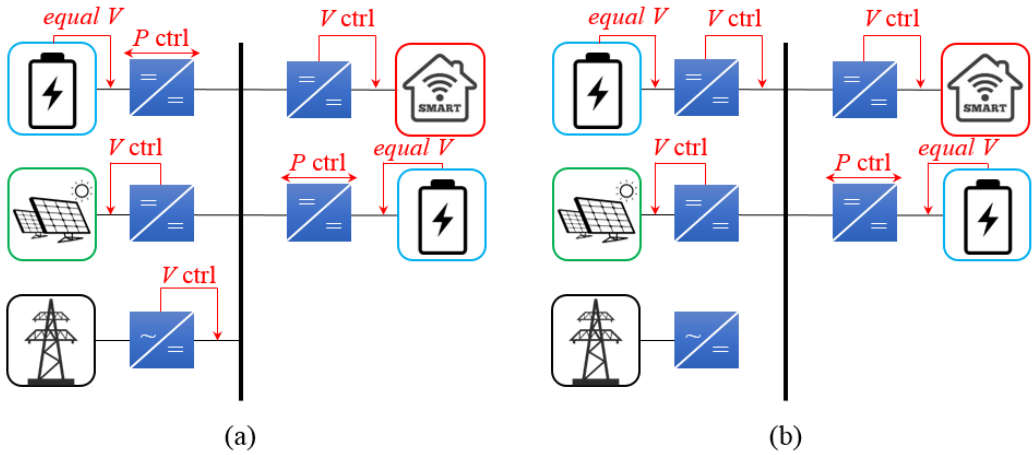

Figure 2.8: Illustration of voltage regulation of DCMGs in (a) grid-tied mode; (b) islanded mode.

consumption. As shown in Figure 2.8 (b), ESS can be used to regulate the main voltage. When the ESS is low, the generation power must be sufficient to supply the load, otherwise, the network may black-out. When the ESS is partially charged, the DGs should generate the maximum power, and the ESS should absorb or inject energy the power difference. When the ESS is fully charged, the generation power of DGs must be controlled to match the consumption power.

2.2 Frequently-Used Components

The most important advantage of a DC power network includes higher reliability and efficiency, simpler control and natural interface with renewable energy sources, and electronic loads and energy storage systems. With the rapid emergence of these components in modern power systems, the importance of DC in today's society is being transformed to a whole new level [9]. This section will introduce pertinent components in future DCMG.

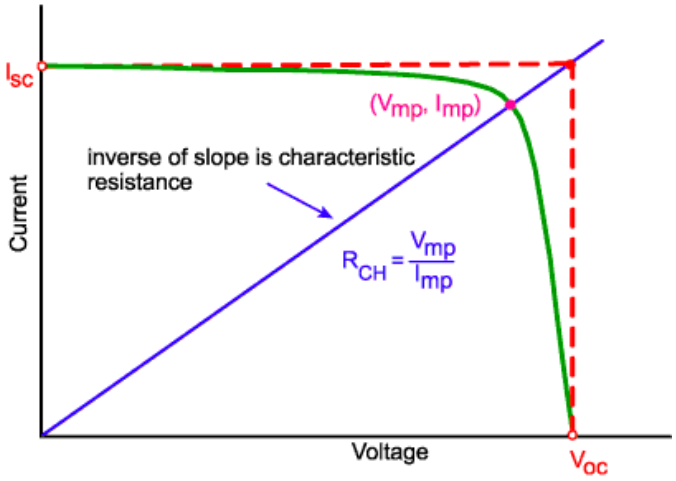

Figure 2.9: Typical I-V characteristic of a PV array.

2.2.1 Integration of Photovoltaic Panels

Photovoltaic (PV) solar panels absorb sunlight as a source of energy to generate electricity. A PV module is typically packaged with 6×10 photovoltaic solar cells. Each module can be connected in series to increase the open-circuit voltage (V_{OC}) or in parallel to increase short-circuit current (I_{SC}) [28]. As shown in Figure 2.9, the output power of a PV array depends on the output equivalent resistance. The maximum power point is named as (V_{mp}, I_{mp}). As the PV array is connected into a system, the associated converter normally needs to adjust its terminal voltage to search for the maximum power point (MPP). This technology is called "maximum power point tracking (MPPT)" [28].

Currently, the best-quoted energy conversion efficiency of a PV module is 22.3-22.7%, as achieved by new commercial products of SUNPOWER [55]. Average solar irradiance is about 1 kW/m^2. The most efficient mass-produced solar modules have power density values of up to 223 W/m^2 [55]. Taking the area of a standard football field (7140 m^2) as an example, if it is covered by PV panels, the energy generated in one peak hour is 1592 kWh, which can provide energy for 80 Tesla Model S cars to be driven for 100 km (100 km power consumed is 19.9 kWh [56]).

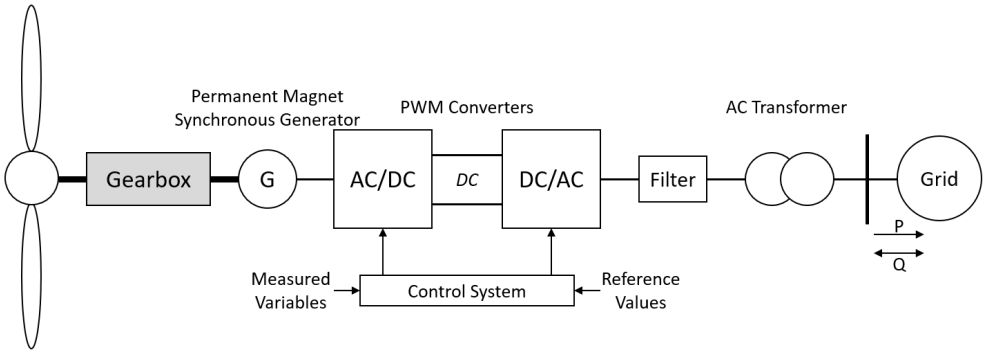

Figure 2.10: Schematic diagram of general wind power grid connection method.

2.2.2 Integration of Wind-Turbine

Wind energy is another significant renewable energy that is commonly applied in the power grid. To date, the largest onshore wind farms are mainly built in China and the US, and the largest offshore wind farms are mainly are in the UK and European countries [57]. The capacity of the world's largest wind farms is from hundreds to thousands of MW [58]. Since wind energy is intermittent and varied, the output voltage and frequency are unstable. The integration of wind farms requires back-to-back converters, which have a complex topology and control system as shown in Figure 2.10 [59]. Accordingly, a wind farm normally centralises more than one hundred wind turbines to minimise the cost.

A DC microgrid only requires one AC-DC rectifier section with a lower cost and simpler control system [9]. This will increase the flexibility of connecting the small-scale and decentralised wind turbines.

2.2.3 Integration of Energy Storage System

An energy storage system (ESS) is used to capture energy produced at one time for use later. Energy can be converted and stored in multiple forms, such as chemical, gravitational potential, electrical potential, kinetic energy, etc. In the conventional power system, the low-capacity stored energy is commonly used for residential backup as emergency energy, called uninterruptible power supply (UPS) [60]. In a modern power

system, as the renewable energy sources (RES) are popularised, high-capacity energy storage devices are required to maintain system stability with the virtual synchronous machine (VSM) [61], because the RES normally has low inertia energy. Additionally, ESS may enable peak-shifting and the maintaining of RES operation with maximum power generation [62]. Lead-acid batteries are generally used in high-power applications, mainly for UPS [63], traditional vehicle batteries [64], and surplus energy of PV and wind generators [65]. Rechargeable dry batteries can also be used in low-power applications; including nickel-metal hydride batteries, lithium-ion batteries, etc [66].

Since DC microgrids generally integrate many RESs, it is significant to utilise ESSs for peak-shifting. In the system without ESSs, the RESs need to adjust generation power to balance the load power all the time. When the generation is not enough to meet local demand, the DC microgrid must absorb energy from the AC grid or abandon some non-essential loads, otherwise, the DC grid voltage would collapse. Accordingly, ESSs are beneficial to store the surplus energy during valley-load/peak-generation time and provide power during peak-load/valley-generation time. Applying ESSs in DCMG will enhance the system ability of islanded operation [65].

2.2.4 Integration of Fast EV Charging Stations

In recent years, the industry of electric vehicles and charging technologies has developed very rapidly [67]. The governments of different countries present great ambitions in transitioning the traditional transports into electric vehicles and building the EV charging infrastructures [3]. The leading manufactures, such as Tesla [68] and BMW [69], are developing and popularising the fast-changing technologies. Concerning from the side of the power system, if the energy that was provided by fuel oil will be supplied from the power system, the requirement of system capacity will rapidly increase. Furthermore, fast charging equipment may consume high power in a short period (each Tesla supercharger consumes 72-250 kW [68]), which is challenging for both power dispatch and transmission lines. A potential solution is employing peak-shift using ESSs

at the customer-side. The energy can be charged into the battery during times with a lower electricity unit price and then used to charge the vehicles at maximum speed when needed [70]. A DC microgrid is a very compatible platform for managing the power between ESSs and EVs [71]. Additionally, the motivation of encouraging electric vehicles is reducing air pollution and carbon emission. However, assuming most of the energy for the EVs is generated with fossil fuels, the use of EV will make little sense of protecting the environment [72]. Employing DC microgrids for EVs is beneficial as it provides an easier connection between RESs and EVs to release the burden of power transmission and reduce energy loss [9].

2.3 Applied Power Electronic Converters

The power electronic converter (PEC) is a component that interconnects different forms of electrical energy systems [73]. The core components of PECs are the solid-state electronic switching devices that are controlled to realise the conversion of different types of electrical energy. The topology of a PEC and the associated electronic components have a long development history that can be traced back to 1900s [74]. As shown in Figure 2.11, the development of PEC used for HVDC technology has experienced the era of the mercury-arc valve and thyristor [74], and the latest technology is the voltage source converter (VSC) composed of isolated gate bipolar transistors (IGBT) [75]. The world's first commercial HVDC transmission system, the Gotland HVDC link, was implemented by ABB in 1954 [76]. The converter initially employed mercury-arc valves that validated the feasibility of HVDC transmission technology [76]. In 1970, the stations were supplemented with thyristor valves so that the voltage and capacity were raised [76]. Since 1997, due to the invention of the fully controllable IGBT switches, the HVDC converters began to adopt the VSC structure [76]. Nowadays, many transnational HVDC links are operating or under construction worldwide to enable grid interconnections and the integration of large-scale renewable power generations [77].

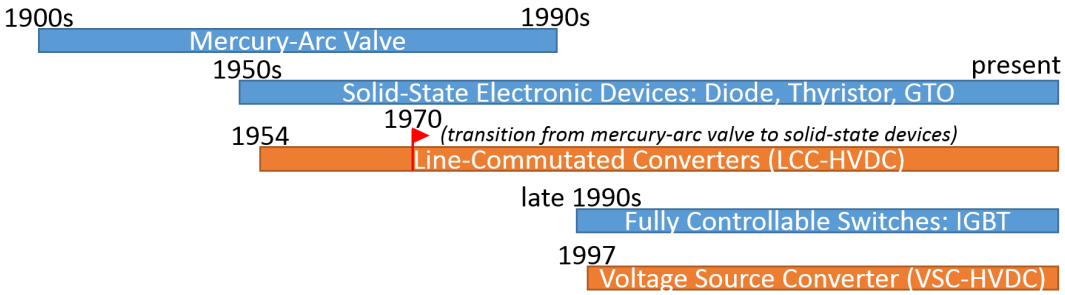

Figure 2.11: History of power electronic devices and PECs for HVDC projects.

In recent years, following the success of HVDC, PECs are increasingly being applied to distribution networks to implement multi-terminal LVDC power distribution networks. For LVDC networks or DC microgrids, PECs are the interfaces that connect multiple energy sources and system zones. There exist many topologies of PECs for different applications, but these can be roughly catalogued into AC-DC and DC-DC converters. The AC-DC converters are applied to connect AC and DC elements, such as interfacing to the AC grid and integrating AC DGs [78, 79], whilst the DC-DC converters are applied to connect different DC elements, such as interconnecting DC subsystems with different voltage levels and integrating DC energy sources [80, 81]. According to the topology of PECs, the power transfer direction may be unidirectional or bidirectional [82-86]. For the areas that always generate or consume power, the employed PEC is only required to achieve unidirectional power transmission, whilst for those with flexible power such as energy storage and the main grid, the PEC must be able to provide bidirectional power transfer.

2.4 Power Management Control

Power management control is required to coordinate the power transfer between each component in order to maintain normal operation in DC microgrids. This requires the PECs to be controlled according to the pre-set control schemes. In AC systems, the rate of change of frequency (RoCoF) reflects whether the system is power balanced [87]. This is because when the power generation is insufficient, the synchronous speed (frequency)

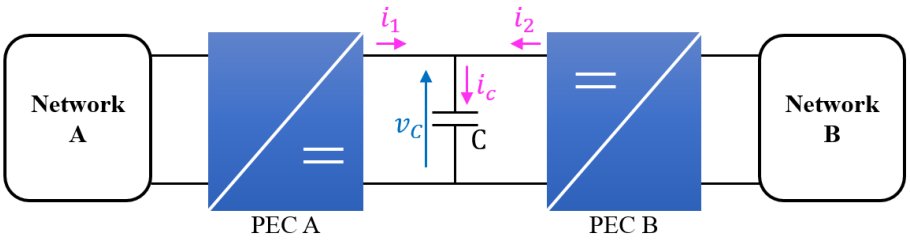

Figure 2.12: Illustration of fundamental control principle in DC networks.

decreases and releases the kinetic energy of the rotors [88]. For DC systems, however, at any busbar, the change of voltage reflects whether the power is balanced. The link capacitors of the PECs discharge to release the stored energy [89]. The equivalent link capacitor in a DC network is shown in Figure 2.12 as an example, and according to the characteristics of the capacitor, the net current flowing into this bus (i_C) determines its link voltage. That is,

$$v_c = \frac{\int i_c \mathrm{d}t}{C}. \tag{2.1}$$

In steady-state, the inflow (i_1) and outflow ($-i_2$) currents on each bus remain equal and the capacitor charge remains stable to maintain the bus voltage. However, when the Network B increases its power absorption through PEC B, that is, the current flowing out ($-i_2$) is greater than the inflow current (i_1), the capacitor will gradually discharge to release its stored energy ($E_C = 0.5CV^2$). Once bus voltage drop is measured, the associated converter (PEC A) must increase the input power (current) immediately from the Network A to prevent the bus voltage collapsing. Accordingly, the basic principle of DC control is: in a node, there can be multiple PECs to release or absorb power as required, but there must be a PEC to maintain power balance according to the voltage displacement.

2.4.1 Power and Voltage Control

Power control is commonly used for delivering constant power between buses as required [10]. The converter compares the instantaneous product of the voltage and current with the set-point to adjust its current let-through so that it achieves the de-

sired power transfer. In DC microgrid, power control may be typically employed to manage ESSs and collect power from RESs [90]. For example, in some cases (e.g., the grid electricity price is low), the DC microgrid may be expected to absorb and store energy in ESSs. This can be achieved by modifying the power transfer set-point of the ESS converter. Additionally, regarding solar generation, the output power of a PV panel is related to its output current (in Figure 2.9) [28], requiring dynamic power control. The associated converter may keep varying the current let-through and search for the maximum power set-point [91].

However, while controlling power transfer, each bus voltage must be stabilised by at least one converter with voltage control. The converter with voltage control is required to monitor and regulate the bus voltage by providing or absorbing extra power dynamically. In the conventional operating strategy of DC microgrid, for the period of grid-connected mode, the main AC grid converter normally operates in the voltage-controlled mode. Whilst the microgrid switches to the islanded mode, the local ESS is used to take over the voltage control [90, 92].

2.5 Droop Control

The concept of droop control is derived from the droop speed control in the AC systems which is used to balance power generation and load power [87]. In the DC network, the strategy is also valid to balance power, but because the voltage acts as an indicator, it is also named as voltage droop control for the DC system [89]. Compared with the voltage control, droop voltage control can enable bus-voltage regulation with multiple converters.

Recalling the AC grid, the response of the generator to the load change has three stages. When the load is suddenly increased and is higher than the generation power, the rotor will quickly release kinetic energy to the load and decelerated. Accordingly,

the system frequency will start to decrease. Then, in the second stage, since the generators in the system detect the decrease of frequency, the turbine governor will raise the mechanical power automatically in terms of the pre-set droop speed control. Since the generation power is turned up to balance the load power, the frequent stops changing and settles at a sub-nominal frequency. In the third stage, the droop characteristic needs to be centrally controlled to move the frequency back to the nominal frequency [93].

In a similar manner, the energy resources in the DC network take the change of voltage as the reference of power balance [94]. When the load power is increased, the link capacitor in the network discharges to release the stored energy. In the second stage, since the energy resources detect the voltage change, the converter needs to adjust the power transfer. In the third stage, centralised control is needed to adjust the droop characteristic to move the voltage back to its original value [95].

2.6 Summary of Chapter 2

This chapter has reviewed the LVDC energy network in general. Firstly, the LVDC network can be composed of single or multiple buses; the voltage level is selected according to the typical power of applications; DC microgrids may operate in grid-tied or islanded mode. Secondly, LVDC networks are designed to conveniently integrate many renewable components, including PV panels, wind turbines, ESSs and EV chargers. Thirdly, LVDC networks may require AC-DC and DC-DC power electronic converters to connect the components in different voltages. Finally, in order to enable energy power transfer between each component and maintain normal voltage, appropriate control strategies must be adopted, such as power control, voltage control and droop control.

Chapter 3

Literature Review on LVDC Network Protection and Investigation of Real-World Implementation Challenges

In Chapter 2, the basic structure of the LVDC power system was reviewed. This reveals that the LVDC network is a converter-dominated grid, and the transient voltage stability is maintained by the converter link capacitors. The structural differences of the LVDC power network will lead to different fault characteristics from traditional AC power grid; hence, the traditional AC measurement and protection approaches are no longer suitable for LVDC networks. In order to enable secure LVDC applications, it is necessary to design reliable protection schemes. LVDC faults can be catalogued into several types, including short-circuit faults, breakage faults, arc faults, abnormal voltage faults, etc. This thesis only focuses on the short-circuit faults which may cause severe hazards. From the literature, researchers have characterised the fault response of DC systems and proposed a range of novel LVDC protection strategies. This chapter will provide a review of short-circuit fault behaviour, DC protection hardware, and state-of-the-art protection schemes.

It is observed that most of the protection strategies of LVDC advocate using high-speed approaches to detect and isolate the short-circuit fault, so as to protect the converter from being damaged by high-magnitude transient fault currents. However, this requires the support of many advanced devices, such as the transducers with a high sampling frequency, high-speed processors, and a large number of ultrafast circuit breakers. Furthermore, due to the limitations of hardware and the impact of the real environment, it may be difficult for the high-speed protection schemes to achieve good reliability in long-term practical application. An alternative approach considered in the literature is the use of fault current limiters (FCL) to quickly restrain the growth of fault current at the sources, in conjunction with moderate-speed protection schemes to cut off short-circuit faults in the distributed network. However, most of the literature only focuses on the implementation of FCL, and more research work about designing proper protection coordination schemes is still required. Accordingly, at the end of this chapter, the main research gaps will be analysed and the implementation challenges of existing LVDC protection schemes will be identified. These issues are the key motivations of this thesis that will be investigated and addressed in the following chapters.

3.1 Review of Short-Circuit Fault Behaviours in LVDC Networks

In contrast to AC systems, DC networks do not employ a sinusoidal voltage with a single frequency. As such, the fault impedance cannot be represented with a complex number to simplify the calculation. Accordingly, transient analysis of DC faults must instead consider the fundamental theory of RLC circuits. The short-circuit fault characteristics in VSC-based DC networks were firstly investigated by Yang [26], who divided a typical DC system fault into three stages: capacitor-discharging, freewheeling, and grid-feeding. The voltage and current responses during the capacitor-discharging stage are derived using time-domain analysis. Fletcher [25] has drawn the same conclusion using the Laplace-domain analysis to simplify the mathematical derivation. This section

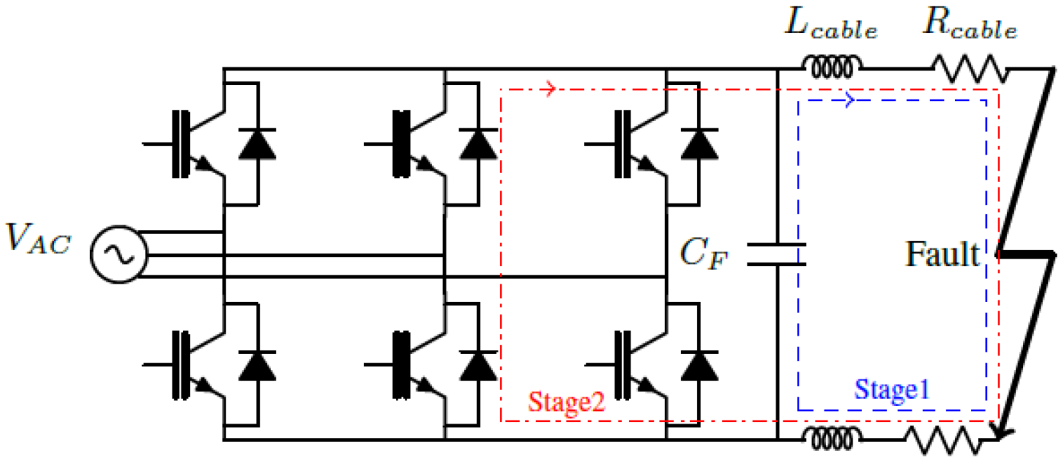

Figure 3.1: Circulation stages of a VSC pole-to-pole fault.

will briefly review the short-circuit fault behaviours with the mathematical deduction to clarify the basic requirements of LVDC protection.

Figure 3.1 illustrates the typical equivalent circuit of a pole-to-pole short-circuit fault in a DC network based on the two-level VSC [23]. On the DC side, the resistance and inductance are used to represent the impedance of the cable and the fault resistance is R_f. When the short-circuit fault occurs on the DC line, the VSC and its link capacitor will respond according to the fault impedance. Figure 3.2 shows a diagram of typical voltage and current responses to a range of fault resistance, in which the grid-feeding current is disabled for a clearer representation of the fault responses.

During Stage 1, a high-magnitude transient current caused by the discharge of the capacitor occurs, lasting from the fault initiation to the zero-voltage condition. Applying Kirchhoff's Voltage Law to the RLC circuit in Figure 3.1, a characteristic equation can be derived to obtain the current solution, that is

$$\frac{\mathrm{d}^2 i(t)}{\mathrm{d}t^2} + \frac{R}{L}\frac{\mathrm{d}i(t)}{\mathrm{d}t} + \frac{1}{LC} i(t) = 0, \tag{3.1}$$

where R, L, C are the total equivalent resistance, inductance, and capacitance of the fault path, and $i(t)$ is the current response.

Fletcher [25] has explained the method for solving this differential equation in Laplace-domain by substituting the boundary conditions, i.e., initial current, $i(0)$, and initial capacitor voltage, $v_C(0)$. To simplify the representation of the current expression, it is necessary to predefine two parameters: α is the damping factor, defined as $\alpha = R/2L$; ω_0 is the resonant radian frequency, defined as $\omega_0 = 1/\sqrt{LC}$. The relative magnitudes of α^2 and ω_0^2 determine the form of the current response, where $\alpha^2 > \omega_0^2$, $\alpha^2 = \omega_0^2$ and $\alpha^2 < \omega_0^2$ represent overdamped, critical and underdamped fault responses respectively.

In the overdamped condition where the fault resistance is high, the current response can be estimated by

$$i(t) \approx \frac{v_c(0)}{L(s_1 - s_2)}(e^{s_1 t} - e^{s_2 t}), \tag{3.2}$$

where $s_{1,2}$ are the roots of the characteristic Equation 3.1 which are equal to

$$s_{1,2} = -\alpha \pm \sqrt{\alpha^2 - \omega_0^2}. \tag{3.3}$$

This behaviour is evident in Figure 3.2. The voltage and current in the overdamped condition remain positive until both reach the steady-state simultaneously, as shown in the case of $R_f = 1\ \Omega$.

In the underdamped condition where the fault resistance is low, the characteristic roots have an imaginary part. After simplifying, the current for highly underdamped condition ($\alpha^2 < \omega_0^2, R_f \approx 0$) can be expressed by

$$i(t) \approx \frac{v_c(0)}{L\omega_d} e^{-\alpha t} \sin(\omega_d t), \tag{3.4}$$

where ω_d is named damped resonant frequency defined as $\omega_d = \sqrt{\omega_0^2 - \alpha^2}$. In this condition, the voltage reaches zero before the current arrives at the steady-state, as shown in the case of $R_f = 1\ \text{m}\Omega$ and $500\ \text{m}\Omega$ in Figure 3.2.

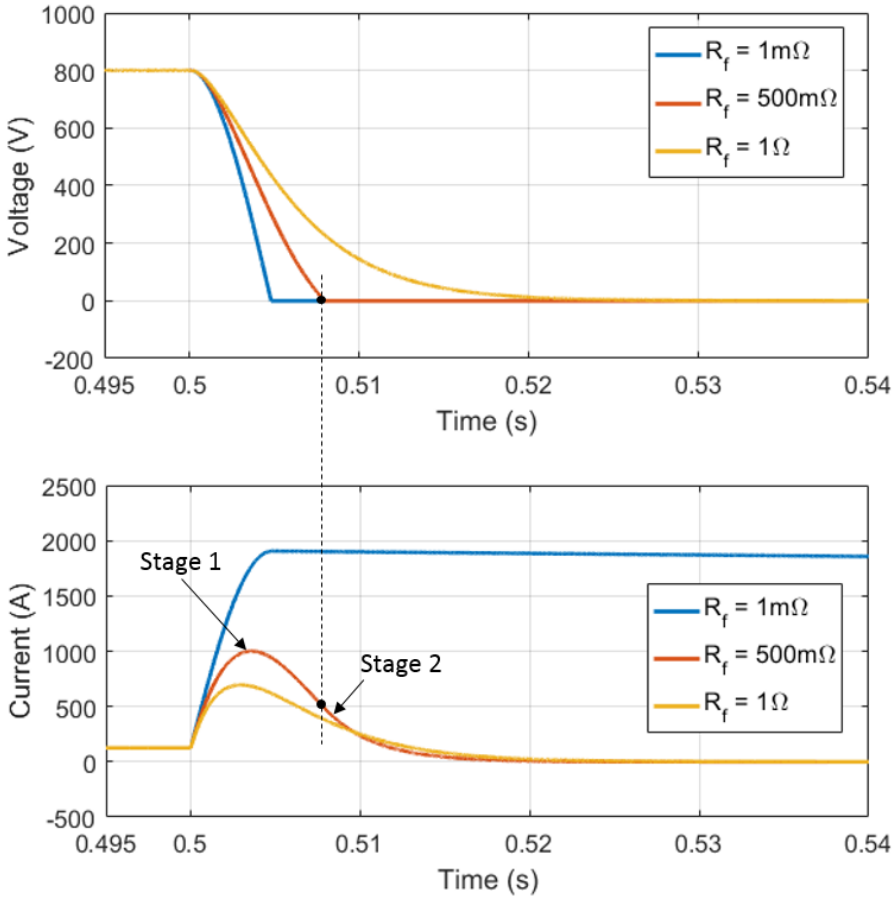

Figure 3.2: Voltage/current profiles of a pole-to-pole fault (disabled converter infeed).

Observing the current waveforms in Figure 3.2, the peak current appears during Stage 1, and low-resistance faults (underdamped condition) may result in higher peak values. The protection must be designed to fit the worst case, that is highly underdamped conditions ($R_f \approx 0$). In this case, the fault current may increase rapidly to the peak value and then slowly decay to zero. The protection must operate quickly before the fault current develops to an extreme value. However, as the rate-of-change of current ($\mathrm{d}i/\mathrm{d}t$) is usually high, the available time window for protection operation is very narrow (typically several milliseconds). It may be particularly challenging to achieve fault detection and isolation in such a narrow time window.

The rate-of-change of current can be deduced by calculating the derivative of the current expression. For low-resistance faults, according to Equation 3.4, the rate-of-change of current can be expressed as

$$\frac{\mathrm{d}i(t)}{\mathrm{d}t} \approx \frac{v_c(0)}{L} \cos(\omega_0 t). \tag{3.5}$$

Assigning the value of $\mathrm{d}i/\mathrm{d}t$ zero, the peak point of the fault current can be calculated, that is $(\frac{\pi}{2\omega_0}, \frac{V_C(0)}{L\omega_0})$. For example, assuming $L = 100$ μH and $C = 100$ mF, the peak current of a low-resistance fault appears as fast as 5 ms.

Stage 2 is defined as the freewheeling stage, lasting from the zero-voltage condition to the steady-state current condition. This situation only occurs in the case of low resistance faults, during which the fault current circulates through the antiparallel diodes within the converter, as illustrated in Figure 3.1. The current value may be high when switching path, which may damage the converter diodes if the protection fails to clear the fault during Stage 1 [23].

Stage 3 is the grid feeding stage. After reaching the steady-state current condition, the primary side of the converter provides the fault current contribution through the antiparallel diodes of the converter [23]. This stage was disabled in Figure 3.2 as the profiles of the grid feeding current depends on the characteristics of the AC side network.

In summary, during Stage 1 of a DC fault, the current may rapidly develop to an extremely high level, which may damage the converter diode when entering Stage 2. This requires the DC protection system to detect the fault and operate in an ultra-fast speed (typically less than 2 ms [27]). However, advanced protection hardware is necessarily required to implement reliable and fast protection in LVDC systems.

3.2 Review of Protection Hardware

The above analysis concludes that DC protection must provide an ultrafast operation speed or the DC microgrid technologies will need to be suitably overrated to safely ride through stages 1-2 of the fault profile. Salomonsson [27] has derived that DC faults should be cleared within 2 ms. By way of comparison, in AC networks, a typical instantaneous overcurrent operation time is more than three cycles (around 60 ms) [96], and even longer for a non-instantaneous trip [97]. This indicates that DC protection must utilise advanced hardware to achieve such fast action. This section will review the available DC protection devices, including transducers, signal processing units and circuit breaking devices, for realising high-speed DC network protection.

3.2.1 Measurement Transducers

Accurate current and voltage measurements are significant for ensuring secure protection operation. The conventional AC system employs current and potential transformers (CT and PT) as the measurement transducers. The principle is to use the alternating magnetic flux, generated by the alternating current of the primary side, to induce a scaled smaller alternating current at the secondary side [98]. However, as the flux induced by DC is invariant during steady-state that cannot induce the secondary current, conventional CTs and PTs are not suitable for DC system measurement.

The commonly used component for measuring DC flux is the Hall effect transducer, which can induce a Hall effect voltage linearly according to the magnitude of steady-state flux [99]. The schematic diagram of the DC Hall effect current sensor is shown in Figure 3.3, consisting of an iron core and a Hall effect semiconductor. The primary current (I_{DC}) to be measured is put through the iron core, and the Hall effect semiconductor is fed with a constant current (I_0). The iron core will collect the flux induced by the primary current (I_{DC}) to polarise the current flowing through the Hall effect semiconductor (I_0). Due to the non-uniform distribution of the charge, a Hall effect

voltage (V_h) will be induced between the sides of the semiconductor. The physical relationship between the Hall effect voltage (V_h) and the measured current (I_{DC}) can be expressed with the Ampere's Current Law and Hall effect formula, which are

$$\oint H \cdot \mathrm{d}l = I_{DC} + \iint \frac{\partial D}{\partial t} \cdot \mathrm{d}S, \tag{3.6}$$

$$B = \mu H, \tag{3.7}$$

$$V_h = \frac{BI_0}{enw}, \tag{3.8}$$

where H is magnetic field strength (A/m); I_{DC} is the primary current (A) to be measured; D is electric displacement field (C/m^2); B is magnetic flux density (Wb/m^2 or V $\cdot$ s/m^2); n is the charge carrier density (m^{-3}); e is the charge of an electron (C), w is the width of the semiconductor (m) (shown in Figure 3.3); I_0 is the control current (A), and V_h is Hall effect voltage (V). During the steady-state, combining Equation 3.6, 3.7 and 3.8, I_{DC} can be measured with a linear relation to V_h, where

$$I_{DC} = \frac{elnw}{\mu I_0} V_h. \tag{3.9}$$

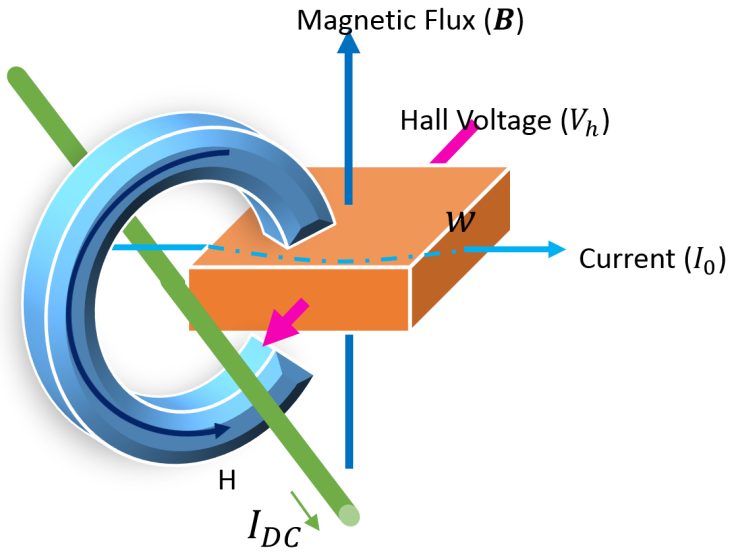

Figure 3.3: Schematic diagram of a Hall effect current sensor.

Similarly, the Hall effect voltage transducer utilises a known resistance to convert the voltage into a small current. By increasing the number of turns on the primary side, the flux induced by this current is amplified and applied to Hall effect semiconductors. In the same way, Hall effect semiconductors can also induce a linear Hall effect voltage (V_h), from which the primary voltage can be measured indirectly.

Many manufacturers have produced high-quality DC Hall effect transducers, such as LEM [100], Tamura [101], and Honeywell [102]. The accuracy of current measurement can reach over 99% [99], and advanced technologies such as closed-loop structure are applied to avoid non-linear measurement and magnetic saturation issues [103].

Hall effect transducer is the most commonly used in LVDC network applications, however, for the high-current scenarios, fibre-optic current sensor (FOCS) produced by ABB can be an alternative option. The FOCS utilises the Faraday's Effect that the polarisation direction of light changes in the magnetic field to measure the current, where the schematic diagram is shown in Figure 3.4 [104]. FOCS can measure up to 600 kA and achieve a higher measurement accuracy (over 99.9%). In addition, the use of fibre optic can also prevent the problem of magnetic saturation and interference from external electromagnetic noises [105].

3.2.2 Circuit Breaking Devices

In the conventional AC network, mechanical circuit breakers (MCB) are typically used to isolate short-circuit faults, which can be cleared at the next current zero-crossing point. However, for DC networks, solid-state circuit breakers (SSCB) are needed to achieve a higher speed protection operation to the DC faults without the zero-crossing point. Power MOSFETs [108] are generally used as the solid-state protection switches under low-voltage and low-power applications, however, for the high-voltage or high-power scenarios, single or multiple series IGBTs [109] are required to interrupt the higher fault currents. However, since the high current flowing through the solid-state device during the no-fault condition may cause high power losses, hybrid circuit break-

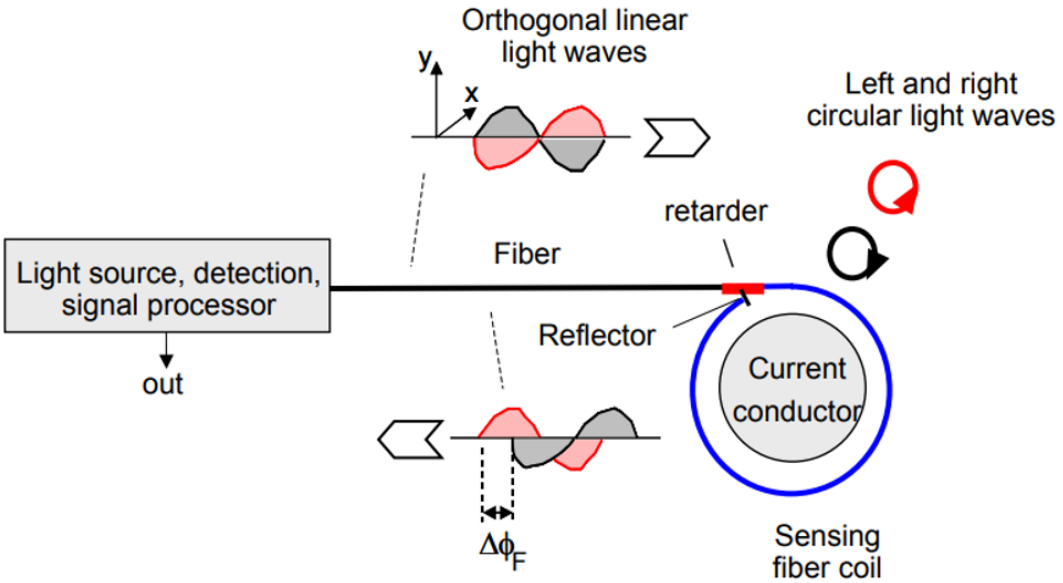

Figure 3.4: Schematic diagram of a FOCS [104].

ers (HCB) [110] have also designed to combine the design advantages of both solid-state and mechanical-breaker technologies. A typical configuration is shown in Figure 3.5. The current flows through the MCB during the normal condition. When the fault occurs, the MCB will open and switch the current to the SSCB path, then the SSCBs will operate to interrupt the fault current quickly. In this manner, both fast operating times and low on-state conduction losses can be realised.

As shown in Figure 3.6, Fletcher [25] has summarised the protection operating time of different circuit breakers. The pure SSCB can achieve fault current interruption less than ten microseconds, whilst the HCB and MCB can operate from hundreds of microseconds to a hundred milliseconds. The type of circuit breakers must be selected according to the specific speed requirements while designing protection schemes.

3.2.3 Signal Processing Units

Conventional AC protection applies electromagnetic relays, which have been proved reliable in long-term practical applications. Electromagnetic protection uses the elec-

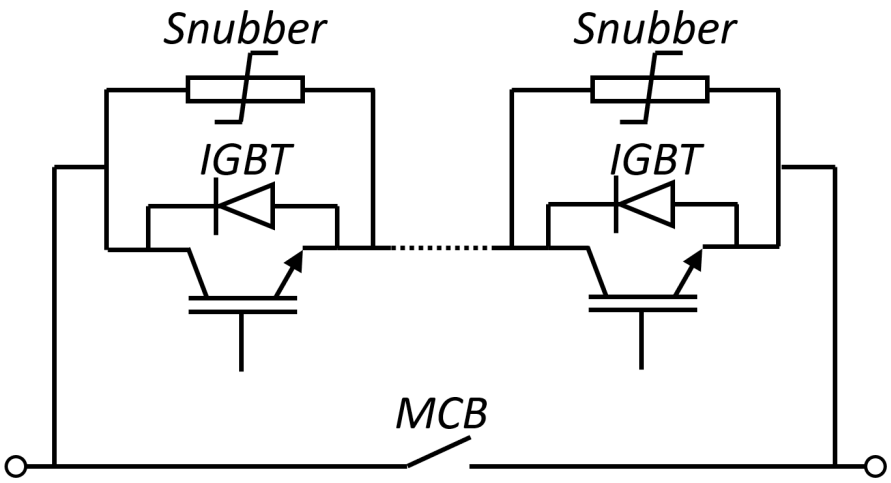

Figure 3.5: Example hybrid circuit breaker design.

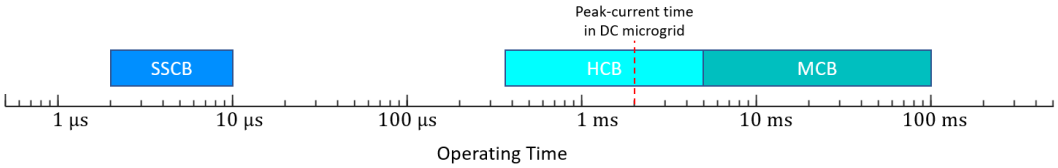

Figure 3.6: Comparison of circuit breaker operating time for DC protection.

tromagnetic force produced by the secondary current of CT to move the armature, and trigger the circuit breaker during the fault condition. Recently, with the development of processors, numerical relays have been introduced to conduct more complex computations for achieving smarter protection schemes. The numerical relay generally consists of filters, ADC, CPU, and memory. The measured signals of CTs and PTs are sampled and processed with the preset algorithm. The numerical relay is based on numerical computation that enables more complex functionalities than the electromagnetic relays. However, since microprocessors adopt serial computation, they may cause time delays due to a large number of program steps. This may not meet the requirement of high-speed fault detection.

For LVDC networks, Field Programmable Gate Arrays (FPGA) [111] can be alternatively employed to achieve a faster signal processing speed. The FPGA is a toolkit for implementing functions by reconfiguring logic gates. Since the input and output are

associated through a logic circuit rather than based on CPU computation, the FPGA processes the input signals in parallel and possesses nanosecond-level propagation delay. After validating the FPGA design, the logic gates in use can be encapsulated as Application-Specific Integrated Circuit (ASIC) [112]. ASIC can be mass-manufactured at a lower average cost and installed in practical electrical relays.

3.3 Review of Literature on LVDC Protection Schemes

The above reviews show that LVDC protection has demanding requirements for fault detection and operation time. Although advanced protection hardware is available for taking high-speed actions, reliable LVDC protection algorithms are vital for tripping the circuit breaker rapidly at the appropriate position when a fault occurs.

3.3.1 Type I: High-Speed Overcurrent Protection Schemes

Before the concept of DC microgrid was proposed, there already existed many small-scale DC electricity applications such as the wiring and electrical equipment for vehicles, which require protection solutions. These were mainly realised with instantaneous overcurrent protection devices, such as fuses and electromagnetic switches [25]. Such devices require no separate components for measurement, relay processing, and current breaking, however, the drawbacks are also obvious. On one hand, these devices are difficult to coordinate for backup protection, and cannot realise large-scale network protection. On the other hand, these devices are frequently employed effectively in battery-based DC networks, but the protection speed is not fast enough that it can be applied in VSC-based network protection, as described in Section 3.1.

After the invention of solid-state switches, such as Emitter Turn-off Thyristor (ETO), MOSFET, IGBT, etc., ultra-fast protection was achievable [23]. The work presented by Mahajan and Baran in [113] represents one of the most comprehensive

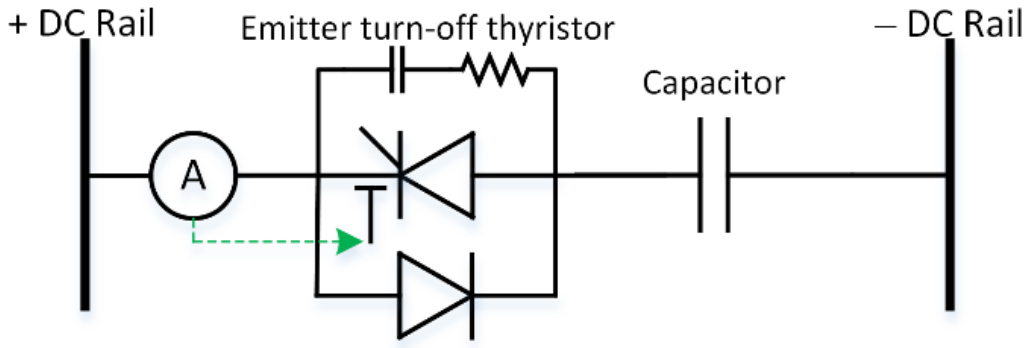

Figure 3.7: ETO-based capacitive discharge circuit breaker.

efforts to design a protection scheme for a VSC interfaced network. For the issue of capacitive discharge, the authors propose the use of instantaneous overcurrent protection for solid-state power electronic switches to interrupt capacitive discharge currents. This is achieved through the connection of an ETO device in series with the capacitive element, as shown in Figure 3.7. The operating principle is based on the current sensing of the ETO which is compared to a threshold. When the discharging capacitor current crosses this threshold, a hard turn-off is initiated which limits any further increase and interrupts the current in 3-7 μs.

Whilst this approach is suitably fast-acting to solve the issue of capacitive discharge for the network described in Section 3.1, the ultrafast protection operation is far less effective when higher levels of protection selectivity are desired. The conventional time-based protection coordination strategies, such as Inverse Definite Minimum Time (IDMT) overcurrent protection [114] in the AC grid, are not feasible because of the high-speed protection requirement in DC networks. For ensuring that only the local protection operates for a fault at a particular location in the network, differential and non-unit protection schemes have been proposed.

3.3.2 Type II: High-Speed Differential Protection Schemes

In distribution networks with many DGs, the differential protection strategy is the most direct way to isolate the fault zone regardless of current direction. High-speed

differential protection for DC distribution systems was firstly implemented by Fletcher, achieving a short operation time of 7.373 μs [115]. It utilises the natural characteristics of DC differential current measurements to significantly reduce fault detection times, and hence meet requirements for DC converter protection (2 ms). This method measures the boundary currents of a protected zone and utilises a communication link to compare the currents based on Kirchhoff's current law, such that

$$\Delta i = i_1(t) + i_2(t). \tag{3.10}$$

Figure 3.8 illustrates the schematic diagram of the internal and external faults. When the sum of currents is greater than a threshold setting, it indicates that a fault exists within the protected zone. When the sum is a low value, it indicates that the network is healthy or there exists an external fault for which the local protection should keep stable. This method offers ultrafast protection with effective selectivity. However, this method requires many SSCBs and communication links with the ensuing high installation costs. Additionally, it does not inherently provide backup protection in the event of device trip-failure.

To overcome the issue of no backup protection, Monadi [116] reinforced this method with a zonal design, as shown in Figure 3.9. This scheme conducts a current comparison not only between the nearest relays but also between further relays in the event of a failure of low-level zone protection. However, in order to realise effective backup protection, the protection devices have to complete the progress of fault detection, at-

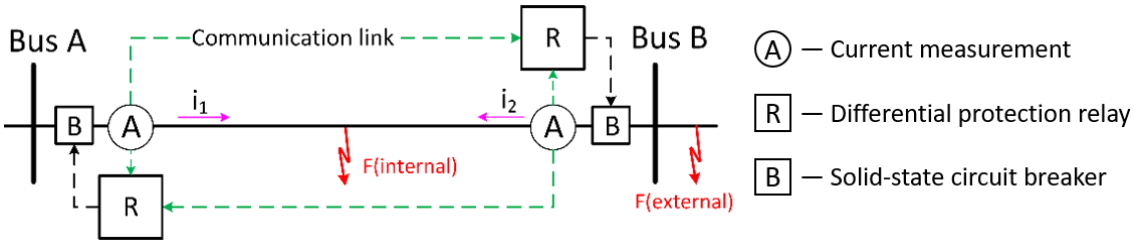

Figure 3.8: Illustration of internal and external faults.

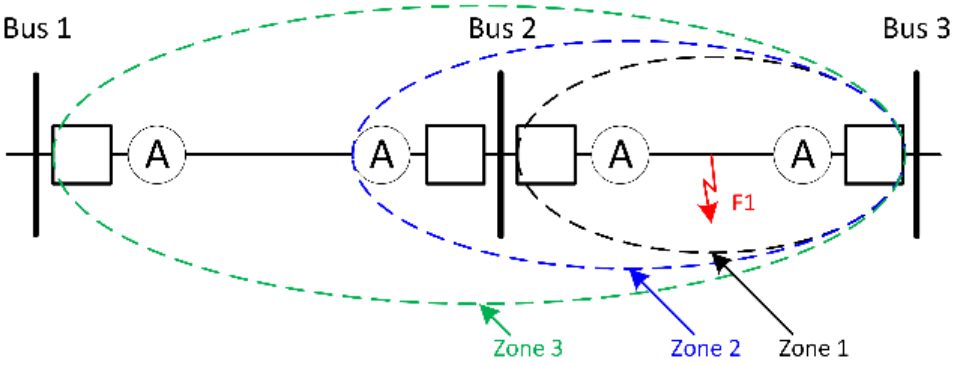

Figure 3.9: Differential scheme with backup protection [116].

tempting operation in Zone 1, detecting the failure of operation, attempting operation in Zone 2, etc. in the very narrow time window. Therefore, it is challenging to implement this protection scheme in practice.

As for the issue of requiring a large number of SSCBs, Monadi [33] also proposed a centralised protection strategy, as shown in Figure 3.10. This scheme only utilises SSCBs at the boundaries of large zones and terminals of VSCs, while applying only common mechanical isolators on the distribution lines. As a fault occurs, the SSCB operates rapidly to isolate the faulted zone, while the isolators locate the faulted line based on differential protection. Since the zone has been de-energised with the SSCBs, the mechanical isolators can easily isolate the faulted line within a relaxed time-window. After the fault is cleared, the SSCBs will reclose to re-energise the healthy part of the network zone. This scheme enables the probability of realising secure protection schemes for large-scale DC microgrids, but with a dependence on reliable, high-bandwidth data transmission.

In order to minimise the amount of data transmitted through communication links, Emhemed and Burt [117] proposed a directional-based protection scheme for LVDC distribution networks, as shown in Figure 3.11. This scheme employs a centralised protection device to gather and process data on current directions rather than values. When the currents on the two ends of a line are detected as flowing in opposite

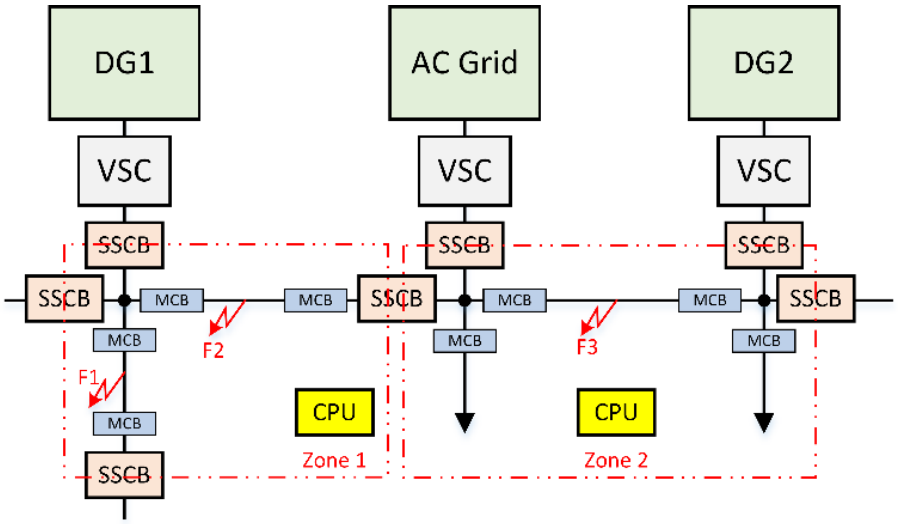

Figure 3.10: Differential scheme with backup protection [33].

directions, it indicates that a short-circuit fault has occurred within the zone. The centralised digital relay unit can offer effective backup protection, but also poses a risk as the failure of the central unit will cause the entire protection system mal-functional. Additionally, since the protection is only based on the current direction, it may be ineffective for detecting high-impedance faults.

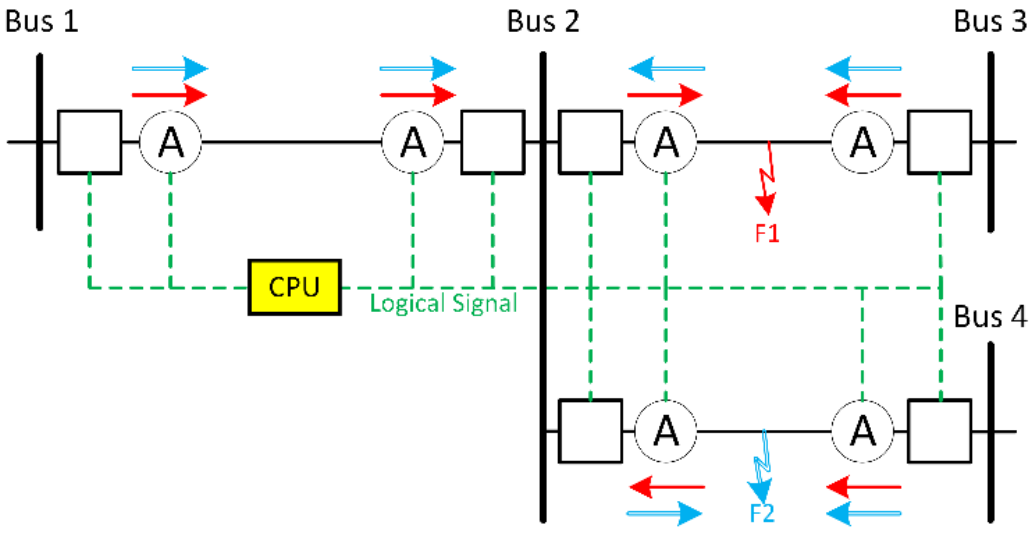

Figure 3.11: Illustration of directional protection operation [117].

3.3.3 Type III: High-Speed Distance Protection Schemes

Type II protection schemes require the support of a high-reliability high-bandwidth communication system, which may have implementation challenges for low-power LVDC network. Hence, another type of protection is proposed which utilises the rate-of-change of a local measurement. A patent utilising initial rate-of-change of current ($\mathrm{d}i/\mathrm{d}t$) was granted by Fletcher in [118] for an LVDC protection application. According to Kirchhoff's voltage law,

$$\frac{\mathrm{d}i(t)}{\mathrm{d}t} = \frac{v_{C_F}(t) - i_L(t)R}{L}. \tag{3.11}$$

At the initiation of a short-circuit fault, that is $t = 0^+$, the term $i_L(t)R$ is approximately zero and can, therefore, be neglected. Accordingly, the cable inductance, which represents the distance from the capacitor to the fault location, can be derived by the pre-fault voltage and the initial $\mathrm{d}i/\mathrm{d}t$ measurement, where

$$L \approx \frac{v_{C_F}(0^+)}{\mathrm{d}i(0^+)/\mathrm{d}t}. \tag{3.12}$$

Since this method utilises the initial characteristics of the fault transient, it can theoretically estimate fault distance within the first two samples after fault initiation, enabling the operation of protection at lower current levels. Additionally, this protection method can offer effective backup protection by discriminating the fault locations. However, the drawbacks include that this protection principle does not allow any shunt capacitors, which are commonly employed in PECs and electronic loads, to be connected in the protected zone, and the capacitance of long cable may also affect the effectiveness of the distance estimation. Additionally, in the case that the measurement of the initial $\mathrm{d}i/\mathrm{d}t$ value is non-accurate, delayed or missed, the estimation result may be a failure.

In order to overcome the risk of missing the initial $\mathrm{d}i/\mathrm{d}t$ measurement, Feng has reinforced the scheme with Linear Regression [119]. Measuring the voltage, current and $\mathrm{d}i/\mathrm{d}t$ every 20-100 μs, the simultaneous equations can be solved to determine R and L, whereby

$$\begin{bmatrix} L \\ R \end{bmatrix} = (A^T A)^{-1} A^T B,$$
$$\text{where } A = \begin{bmatrix} \frac{\mathrm{d}i}{\mathrm{d}t}(0) & i(0) \\ \frac{\mathrm{d}i}{\mathrm{d}t}(1) & i(1) \\ ... & ... \\ \frac{\mathrm{d}i}{\mathrm{d}t}(N) & i(N) \end{bmatrix} \quad \text{and } B = \begin{bmatrix} v(0) \\ v(1) \\ ... \\ v(N) \end{bmatrix}. \tag{3.13}$$

This method not only overcomes the risk of missing the initial fault point, but also is capable of distinguishing low-resistance and high-resistance faults. Since Equation 3.11 contains two unknowns, R and L, at least two sets of measurements are needed to solve the equations. In order to avoid errors and contingencies, this method uses multiple sets of measurements to find the linear regression solutions of R and L. However, a downside to this method is that it takes a longer time to detect a fault. Other methods based on $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}^2i/\mathrm{d}t^2$ [120] have also been proposed in the literature but have not been proven in practice.

3.3.4 Type IV: DC Network Protection using Fault Current Limiting Strategies

Although the high-speed DC protection method can cut off the fault current quickly, it may be difficult to be implemented in practical applications. Firstly, high-speed protection must employ high-cost SSCBs or HCBs. Especially for distribution networks, the wide use of solid-state devices may lead to high installation costs, hindering LVDC popularisation. Secondly, since the time window for determining the location of faults is very short, it may cause difficulty in protection coordination. Furthermore, due to the small number of fault detection samples, the protection operation may be vulnerable to the real-world electromagnetic interference and sampling error, resulting in protection stability issue.

Due to the shortcomings of high-speed protection, some researchers advocate util-

ising fault current limiters (FCL) to avoid the need for ultrafast protection schemes. FCLs may be implemented using a full-bridge converter [30], superconducting fault current limiter [31], or solid-state fault current limiter [32]. Using such devices, downstream relays will gain a longer time-window to realise protection coordination with conventional MCBs. A method proposed by Qi in ABB Inc. utilises an upstream inductive solid-state FCL to limit fault current and downstream MCBs to select the fault location using differential/directional protection schemes [32]. The number of SSCBs needed is dramatically reduced, but comparison-based protection schemes still rely on communication systems.

3.4 Analysis of Main Research Gaps from Literature Review

According to the review above, several research opportunities related to DC network protection can be observed. Firstly, fault current response in a complex PEC-based LVDC network is difficult to predict when more than one converter source is accounted for. More specifically, although the current profile of a DC fault can be derived mathematically as mentioned in Section 3.1, calculating the fault current responses in complex DC networks is still challenging as the PEC and filter capacitors may also contribute part of the fault current. Accordingly, it is necessary to build a simulation model for the convenience of analysing fault responses from different components in LVDC networks. In Chapter 4, a DC microgrid model with significant DC components will be built and the fault current responses will be validated based on this model.

By reviewing the protection strategies in the literature, Section 3.3 has catalogued the existing LVDC protection schemes into 4 types, in which three are dedicated to directly isolating the fault at high-speed, whilst the fourth advocates the use of fast fault current limiters (FCL) coordinated with conventional moderate-speed mechanical circuit breakers (MCB). With regards to the former, the main advantage is that these methods will cut off the faulty zone quickly so that the fault will have a minimal impact

on the healthy sections in the network. However, even though many researchers have made substantial efforts in developing theoretically effective high-speed LVDC protection strategies, few of them have considered the challenges for practical implementation. This poses several research challenges and opportunities, which are listed as below.

The main implementation challenge of realising high-speed overcurrent protection is that advanced hardware must be employed to complete fault isolation before the peak current, which normally appears after several milliseconds as stated in Section 3.3.1. As the failure of protection before the peak current may lead to a protection blinding problem, it is necessary to investigate the hardware requirements for selecting suitable devices. Furthermore, time grading overcurrent protection will be difficult to realise in a high-speed fashion. The operating time in AC networks may reach a second-level time scale that can provide enough time margins to achieve backup protection, whilst in the DC system, the short time-window prevents the realisation of DC overcurrent protection coordination.

The main difficulty in realising high-speed differential protection schemes is ensuring fast and reliable communication. As mentioned in Section 3.3.2, these sort of methods adopt direct signal comparison to determine the fault location so that protection discrimination can be achieved quickly. However, high-speed protection usually requires accurate measurement synchronisation, and a short time synchronisation error (TSE) may result in poor protection stability. However, a precise clocking system is hardly achievable in practice. It is necessary to research the impact of TSE to protection stability and make necessary improvements in the associated algorithms to address the instability issue.

The rate-of-change of current ($\mathrm{d}i/\mathrm{d}t$) is required in many distance protection schemes as mentioned in Section 3.3.3. As the fault distance is proportional to the cable inductance which cannot be seen in the steady-state condition, a $\mathrm{d}i/\mathrm{d}t$ measurement is usually utilised for estimating the cable inductance on the fault path. However,

high-speed $\mathrm{d}i/\mathrm{d}t$ is very sensitive to the impact of noise in practice. Even very low noise-levels may cause the $\mathrm{d}i/\mathrm{d}t$ measurement results to be heavily masked by noise, potentially leading to protection operation failure. Therefore, it is necessary to optimise the approach of measuring $\mathrm{d}i/\mathrm{d}t$ to improve the reliability of DC distance protection.

Apart from the high-speed schemes, an alternatively available strategy is the moderate-speed protection using the FCL. Since high-speed protection must utilise many advanced devices, it may not be economically suitable to be applied in low-power DC distribution networks. Accordingly, fast FCL has been introduced to restrain the rise of fault current and allow a longer protection operating time, thus reducing the number of high-speed components used for fault isolation. Also, the longer protection time restores the possibility of implementing overcurrent protection coordination in LVDC networks. Compared to the differential protection strategy, grading overcurrent protection can realise protection discrimination without communication systems, hence potentially achieving lower cost but higher reliability for practical application. However, most of the current research focuses on the topologies of FCL devices in the literature, but more research is needed to design downstream protection coordination strategies.

3.5 Identification of Metrology Challenges and Requirements

Following the classification of DC microgrid protection schemes presented above, this section analyses the metrology challenges and derive requirements (where applicable) for each type of protection scheme class. Type I, DC overcurrent protection must employ advanced current transducers and A/D converters to ensure adequate samples are obtained before the capacitor discharging current develops to the peak value. Based on the fault current analysis in Section 3.1, the current transducer must possess the following two features:

a. Wide measurement bandwidth. To ensure the measured current is sufficiently accurate to the real fault current, the bandwidth of measurement must be higher than the fault current bandwidth. The highest fault current bandwidth appears in the condition of a low-impedance short-circuit fault ($R \approx 0$), that is $\omega_0/2\pi$, typically 200 Hz.

b. High sampling frequency. As the numerical comparison is conducted by a digital processor, the A/D converter must utilise a high sampling frequency for taking fast protection actions. The sampling time setting depends on the peak time and the number of sample captures required before the time of the current peak. Defining the desired number of samples as N, the minimum sampling rate, f_S, can be derived, such that

$$f_s = \frac{N}{0.25T_0} = \frac{N}{0.5\pi\sqrt{LC}}. \tag{3.14}$$

For example, assuming the natural frequency of a fault is 250 Hz ($T_{peak} = 1$ ms), and the desired number of samples before the peak current is 1000, the minimum sampling rate is 1 MHz, which is high in practical applications.

Concerning Type II, the four protection schemes that have been reviewed in Section 3.2 commonly adopt a differential protection strategy based on communication links. The major challenge of Type II protection schemes is time synchronisation measurement, because even a short time synchronisation error may result in protection mal-operation. For example, Fletcher [115] demonstrated that small synchronisation errors can cause significant differential errors, as shown in Figure 3.12. According to Equation 3.5, if the rate-of-change of current ($\mathrm{d}i/\mathrm{d}t$) before the peak is approximated as V_C/L, the maximum error caused by the imperfect synchronisation can be derived, whereby

$$\Delta i_e = \frac{V_C}{L}\Delta T_e. \tag{3.15}$$

Δi_e must be lower than the threshold setting to ensure the protection is stable for

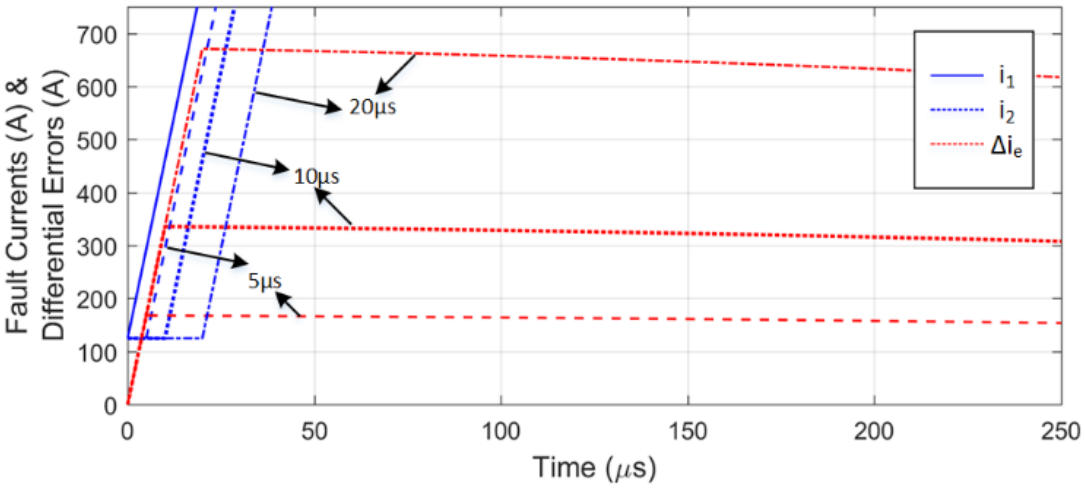

Figure 3.12: Illustration of the time synchronisation issue [115].

external faults. However, assuming the order of the practical network parameters in Table 3.1 are applied, the requirement of time synchronisation measurement may be as narrow as $\Delta T_e < 1$ µs. This is a comparative level to an inherent physical delay over a distance of 300 m.

The major metrology challenge for Type III, distance protection schemes, is the acquisition of rate-of-change of current ($\mathrm{d}i/\mathrm{d}t$). The rate-of-change of a signal is usually obtained by numerical derivative computation, but this method is extremely sensitive to very small noise. For example, it is assumed that a 100 A steady-state current is differentiated with a time step of 1 µs. When there is a 1% error between two successive samples, the error of $\mathrm{d}i/\mathrm{d}t$ will reach as high as 10^6 A/s. However, white noise inherently exists in reality that cannot be eliminated by the current transducer; hence, signal processing is required for optimising the derivative computation. The acquisition of high fidelity $\mathrm{d}i/\mathrm{d}t$ requires the use of short sampling time. However, the use of an

Table 3.1: Example of network parameters.

V_C	L	$I_{Threshold}$ setting
10^3 V	10×10^{-6} H	10^2 A

extremely short sampling time will magnify the noise by numerical derivative computation, while excessively long sampling times will result in attenuated $\mathrm{d}i/\mathrm{d}t$ results and time delays. Meanwhile, a digital low-pass filter could also be employed to constrain the high-frequency noise before the numerical derivative computation. Therefore, the measured signal must be pre-processed to obtain a sensible $\mathrm{d}i/\mathrm{d}t$ rather than directly differentiated.

Type IV is a moderate speed protection strategy based on an FCL + MCB structure, and hence does not require the support of many advanced measurement devices. As this method has a longer time-window for detecting the faults, it has better tolerance to the contingent error and natural noise in practical applications. However, though much research on the implementation of fast FCLs has been conducted, as mentioned in Section 3.3.4, the methods of achieving protection coordination strategies economically using the MCB relays in the power distribution network have not been fully considered in the literature.

Table 3.2 summarises the advantages and drawbacks of the four types of LVDC protection schemes and the probable challenges of real-world implementation. The table has also introduced the issues to be addressed in the next three chapters. Chapter 5 will propose a novel protection scheme, "Multi-Sample Differential (MSD) protection scheme", to address the issue that inherent time synchronisation error may lead to maloperation when an external-zone fault occurs. Chapter 6 will propose recommendations for pre-processing the measured signal in distance protection, in order to obtain a more accurate and reliable $\mathrm{d}i/\mathrm{d}t$ results. Chapter 7 has proposed a new protection scheme, "Modulated Low Fault-Energy (MLE) protection scheme", to achieve moderate-speed protection coordination with a low cost based on the FCL + MCB structure.

Table 3.2: Summary of protection schemes.

Type	**Scheme Name**	**Advantage**	**Disadvantage**	**Implementation Challenge**
Type I: Overcurrent protection	Fuse/EM switch	Compact	Slow Difficult in realising selectivity	N/A
	ETO-SSCB	High-speed	No selectivity	High bandwidth High sampling rate (>1 MHz)
Type II: Differential protection	Differential	High-speed High selectivity	Provides no backup protection Require large number of SSCBs Need communication links	Require accurate time-synchronised measurement (synchronisation error<5 μs)
	Differential with backup	Provides backup protection	Require large number of SSCBs Need communication links	
	Centralised	Less usage of SSCBs Provides backup protection	Need communication links	
	Directional	Less data transmission Provides backup protection	Not sensitive to high R faults Risk of using centralised relay	
Type III: Rate of change protection	Initial $\mathrm{d}i/\mathrm{d}t$	High-speed Selectivity No need for communication	Risk of missing initial sample Shunt capacitor not allowed Not reliable with signal sample	Derivative computation of $\mathrm{d}i/\mathrm{d}t$ is extremely sensitive to the noise.
	Multiple $\mathrm{d}i/\mathrm{d}t$	Higher reliability Both R & L are detectable	Shunt capacitor not allowed	
Type IV: FCL-based protection	FCL+Differential	No high-speed devices needed Ride through transient fault	Need reliable fast FCL Need communication links	Implementation of protection coordination economically

3.6 Summary of Chapter 3

This chapter has reviewed the protection of LVDC systems, including DC fault characteristics, available protection devices, and existing protection schemes.

First of all, from the review of DC fault behaviour, the major risk of DC faults is caused by the high-magnitude fault current generated by the capacitor discharge. During the short-circuit fault conditions, the high current from capacitor discharge may quickly damage the converter diodes. Hence DC circuit breakers must operate quickly (in several milliseconds) to prevent the occurrence of excessive current.

The second section reviewed the hardware composition of DC protection, including measurement, circuit breaker and signal processing. It was noted that DC transducers mainly employ the Hall effect sensors instead of conventional CTs and PTs. DC circuit breakers need to employ SSCB and HCB to achieve high-speed protection, whilst MCBs cannot reach a high-speed operation. The signal processing is achieved by microprocessor or FPGA. Microprocessors are suitable for more complex computation, whilst FPGAs can achieve a faster operation speed.

The third section has reviewed the LVDC protection schemes from the literature. The high-speed LVDC protection schemes can be divided into three categories: overcurrent protection, differential protection and distance protection. Additionally, LVDC protection can also deploy FCLs at sources to limit fault currents so that the MCBs are enabled to isolate the fault zone with medium speed. A literature-gap analysis is undertaken with reference to these protection classes, and key shortcomings associated with each approach are identified.

Finally, considering the impact of environmental interference, such as electromagnetic noise and communication delay, on high-speed protection, the author has proposed the probable measurement challenges and requirements associated with a real-world

implementation of advanced state of the art DC system protection schemes from the literature. It is concluded that overcurrent protection must employ higher sampling rate metrology to prevent the missing of the peak of the fault current; differential protection requires a highly-synchronised current measurement as a small displacement error may cause a false trip; distance protection requires accurate rate-of-change of current but small noise may cause a severe error to the measurement results. Additionally, as the high-speed methods may be inherently sensitive to environmental interference, the author advocates the use of FCLs and MCBs in tandem. Though many fault current limiting devices are proposed to enable a longer time for fault selection, more research on designing matching protection coordination schemes is still required.

Chapter 4

Analysis of DC Fault Response with DC Microgrid Modelling

As reviewed in the previous chapter, the structure of DC power networks is different from traditional AC networks, containing many unique devices and components. Also, though the fault response of DC fault in a simple RLC circuit can be mathematically derived as described in Section 3.1, it is difficult to calculate the fault behaviour in a complex DC network. Accordingly, to facilitate the research on fault behaviours and protection schemes, it is necessary to model DC microgrids as a test-bench for observing network characteristics under different conditions.

This chapter presents models of key DC microgrid components including commonly-used PECs, PV panels and ESS equipment, according to the corresponding mathematical principles. By combining these components, a single-bus DC microgrid model has been realised in MATLAB/Simulink to demonstrate the basic operating principles and enable the research of electrical protection. The combined DC microgrid model is designed to achieve the following functionalities:

1. The LVDC network needs to include multiple renewable elements and loads, which should be driven with the proper PECs. These converters must be deployed with proper control methods to achieve normal operation. In terms of Section 2.4, the

AC-grid tied converter will adopt the voltage control strategy to maintain the power balance, whilst the converters in the other branches are set in the power control mode. The inclusion of closed-loop control systems allows the PEC impact on fault responses to be captured, enabling an investigation into the interaction of protection and control systems.

2. In order to prevent the initial connection of PEC-driven sources from affecting the stability of the system, power filters are connected beside the PECs and tuned to damp the system oscillation. This will help the network to restore the steady-state rapidly after connecting a new power source.

3. For the issue of network grounding, this LVDC model is an isolated system with the negative pole grounded. LVDC networks may employ various grounding topologies, which lead to different fault currents. Employing the negative pole grounded topology may enable similar fault behaviours under pole-to-pole and pole-to-ground fault conditions, for offering the convenience of unified protection design.

4.1 Two-Level AC-DC Voltage Source Converter

An AC-DC converter is a significant device for interfacing AC and DC sections in the modern power grid. It is widely applied to integrate different forms of energy resources and can be realised by a range of different topologies. For high-voltage and high-power occasions, such as HVDC long-distance power transmission, line commutated converter (LCC) and modular multilevel converters (MMC) are often used, whilst for LVDC applications, a two-level VSC structure is usually employed. The topology of a two-level VSC is shown in Figure 4.1, which consists of six pulse bridges. On each bridge, the VSC employs one or multiple series solid-state switching devices that are driven by a controller [34].

According to the mathematical model and the vector control strategy in reference [9], an average model of a two-level VSC is implemented, which has been shared to

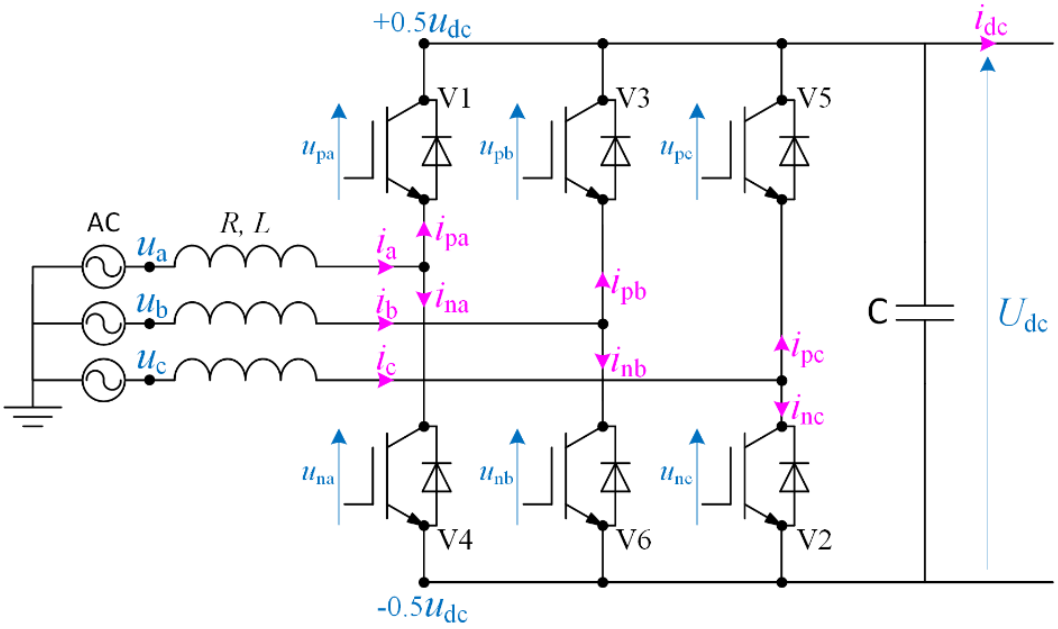

Figure 4.1: Topological structure of the three-phase two-level VSC.

Table 4.1: Relevant parameters of the VSC model.

Parameter Name	**Symbol**	**Value**
Nominal AC voltage (line-line rms)	V_{abc}	400 V
Nominal AC current	I_{abc}	100 A
Nominal DC voltage (pole-pole)	V_{dc}	$400\sqrt{3}$ V
Nominal DC current	I_{dc}	100 A
DC load (matched)	R_{dc}	$400\sqrt{3}/100$ Ω
AC voltage base	$V_{ac_{BASE}}$	$400\sqrt{2}$ V
AC current base	$I_{ac_{BASE}}$	100 A
DC voltage base	$V_{dc_{BASE}}$	$400\sqrt{3}$ V
DC current base	$I_{dc_{BASE}}$	100 A
Power base	S_{BASE}	$400\sqrt{3} \times 100$ VA

MathWorks file exchange centre [35]. As shown in Figure 4.2, the model consists of three equivalent voltage sources on the AC side and an equivalent current source on the DC side. The voltages of the controlled AC sources are equivalent to the voltages of three phases that are produced by controlling the solid-state switches on each bridge. The three control AC voltage signals are computed by vector control algorithm [9], according to the desired active and reactive power, where the details of the control

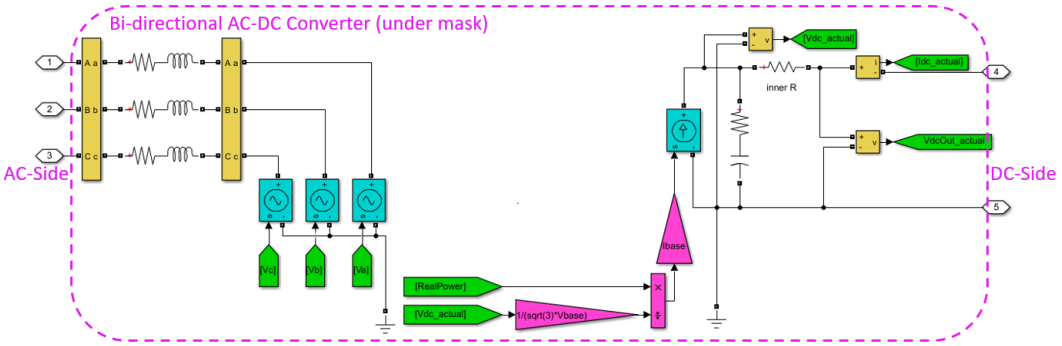

Figure 4.2: Topological structure of an average two-level VSC model.

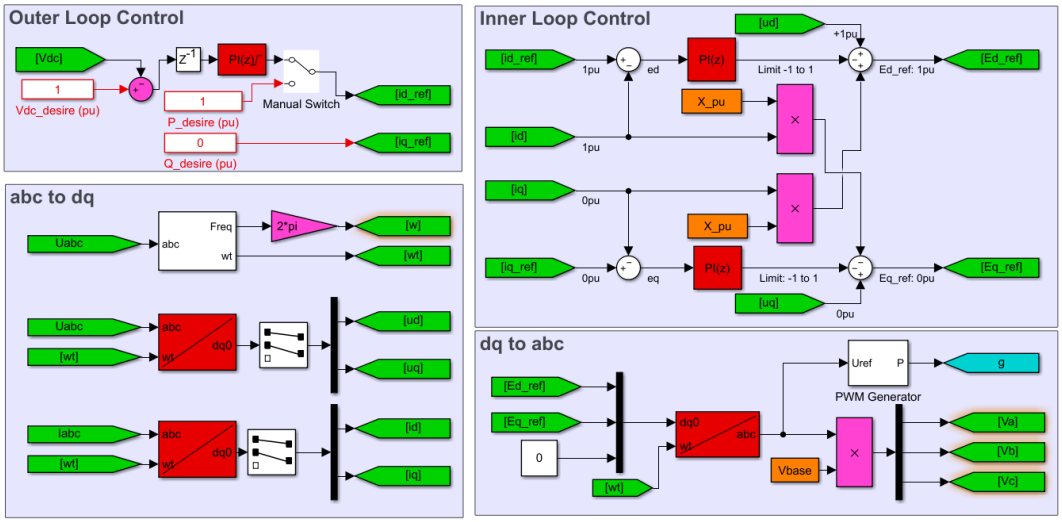

Figure 4.3: Details of the VSC control model.

model are illustrated in Figure 4.3. The vector control transforms the three-phase signals from the Cartesian coordinate system to the d-q coordinate system in order to decouple active and reactive power regulation. On the DC side, the infeed current is controlled to provide the same active power as the AC side. The relevant parameters of this average VSC model are shown in Table 4.1.

In order to verify the effectiveness of this VSC model, the desired active power, DC voltage, and reactive power settings will be varied, and the measured results checked for consistency with the desired values. The waveforms of active power, DC voltage, and reactive power in the model are shown in Figure 4.4 to present the change of setting

values and the measurement results. At $t = 0$, the VSC is set to the PQ control mode in default where $P = 1$ pu, $Q = 0$ pu. The result shows that the measurement values of active and reactive power are approximately the same as the setting values. From Table 4.1, since the DC side is connected to a matching load resistor ($R = S_{BASE}/I^2_{dc_{BASE}}$), the ideal value of the DC voltage should be 1 pu. However, because the DC cable contains a small line loss, the measurement value of the DC voltage is slightly lower than the ideal value. At $t = 2$, 4, and 6 seconds, the setting value of reactive power is adjusted to 0.6 pu, -0.6 pu and back to zero for verifying if the VSC can respond correctly. The results show that the measured value of reactive power can follow the change of settings, and it has minimal impact on the value of active power outputted. This indicates that the vector control algorithm applied in this VSC model has effectively decoupled the control between active and reactive power. At $t = 10$ seconds, the desired active power is adjusted to 1.5 pu to verify the effectiveness of active power regulation. The result shows that adjusting active power will not affect reactive power, and the measured value of active power and DC voltage has reached the expected values ($P = 1.5$ pu, $V_{dc} = \sqrt{1.5} \approx 1.22$ pu). At $t = 20$ seconds, the VSC is switched to the VQ control mode, where $V_{dc} = 1$ pu, $Q = 0$ pu, to verify the effectiveness of DC voltage control and reactive power control in this mode. The result shows that the voltage rises to exactly 1 pu, whilst the active power is slightly higher than 1 pu due to the existence of power loss. From $t = 22$ to 26 seconds, the measured value of reactive power can also effectively follow the change of the setting value without affecting the values of active power and DC voltage in the VQ control model.

4.2 DC-DC Converters

Since DC microgrids may employ multiple DC voltage levels for different electrical applications, DC converters are required to link the zones and form a large-scale LVDC network. DC-DC converters can be implemented with many different topologies, and according to the voltage levels, rated power and application occasions, they may consist of different power electronic devices, such as IGBTs and power MOSFETs [23]. As a

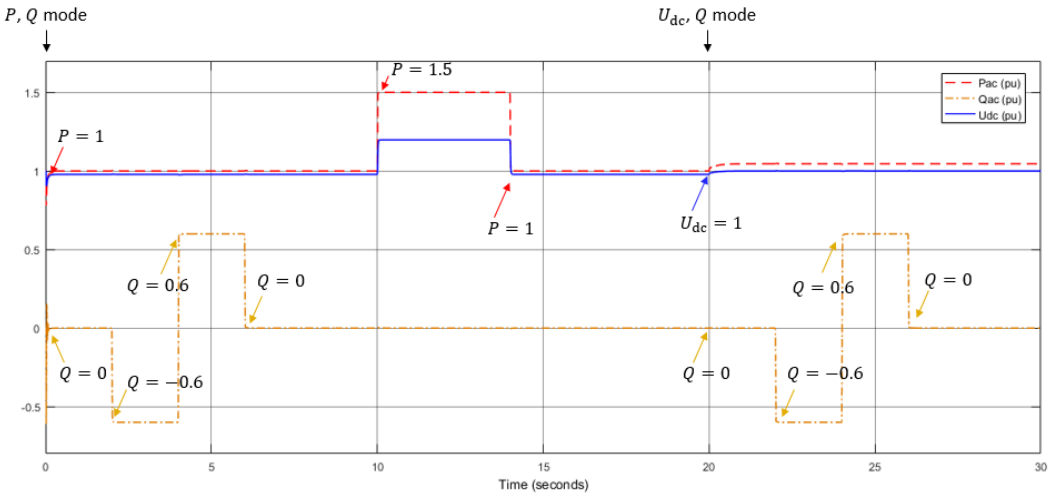

Figure 4.4: Validation results of the 2-level VSC model.

typical DC microgrid model may integrate PV panels, ESSs, and low-voltage loads, it is necessary to model the essential DC-DC converters. Accordingly, this section will demonstrate the models of Buck, Boost, and Dual-Active-Bridge DC-DC converters.

4.2.1 Buck DC-DC Converter

A buck DC-DC converter [123] is a unidirectional step-down converter that may be employed for delivering power from the source to the demand. Figure 4.5 shows the topology of a DC converter that consists of a capacitor, inductor, diode and a solid-state switch. The controller usually adopts a pulse width modulation (PWM) control strategy to adjust the voltage ratio between the input and output sides. This voltage ratio can be derived from the duty cycle of the modulation switch, that is

$$\frac{V_o}{V_d} = D \tag{4.1}$$

where D represents the duty cycle of the switch, that is $D = t_{ON}/(t_{ON} + t_{OFF})$, and as the duty ratio is in the range of 0 to 1, the output voltage (V_o) is lower than the input voltage (V_d). The PWM modulation signal is generated by comparing the desired duty cycle value (D) with a high-frequency sawtooth waveform. This modulated signal is used to control the switch so that the voltage ratio control is realised.

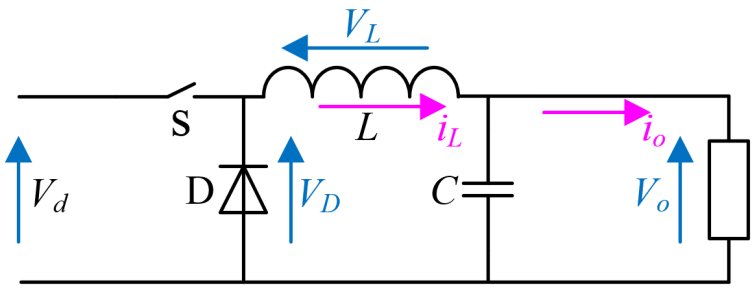

Figure 4.5: Topological structure of the buck DC-DC converter.

A buck converter model is shown in Figure 4.6, in which an ideal switch is employed to represent the IGBT. The selection of inductance and capacitance parameters will affect the ripple value of current and output voltage, which can be calculated by [123]

$$\Delta I_L\% = \frac{|\Delta I_L|}{I_L} = \frac{R_L T(1-D)}{L}, \tag{4.2}$$

$$\Delta V_o\% = \frac{T^2(1-D)}{8LC}, \tag{4.3}$$

where T represents the period time of PWM, and R_L is the load resistance. Accordingly, in this model, assuming the ripples of current and voltage are to be constrained to 10% and 1%, the inductance and capacitance should be set to 5 mH and 1.25 mF respectively. To verify this model, the duty cycle (D) of the switch is set to 0.5; the input voltage is set to 1 pu; the low-voltage side is connected to a 1 Ω load resistor. The relevant parameters of this model are summarised in Table 4.2, and Figure 4.7 presents the waveforms of the simulation results. The steady-state output voltage and current are nearly equal to 0.5, which accords with the expectation, and the ripples of voltage and current are equal to 1% and 10% of the steady-state levels. These results indicate that the model can achieve the desired requirements.

Table 4.2: Relevant parameters of the buck DC-DC converter model.

V_d	V_o	D	V_D	R_D	ESR_C	L	C	R_L	f
1	0.5	0.5	0	1 mΩ	0	5 mH	1.25 mF	1 Ω	1 kHz

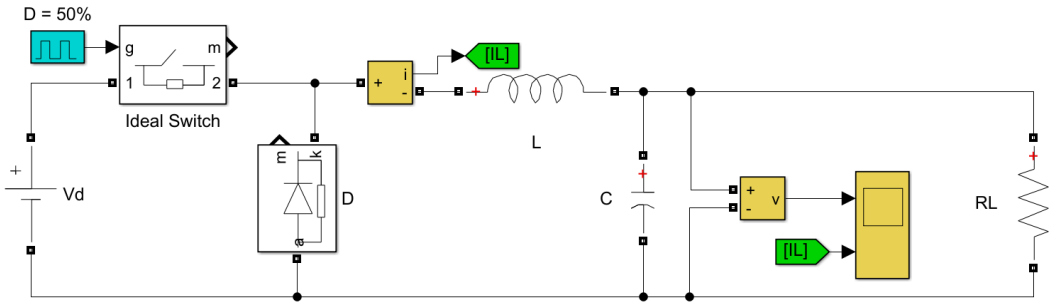

Figure 4.6: Topological structure of a buck DC-DC converter model.

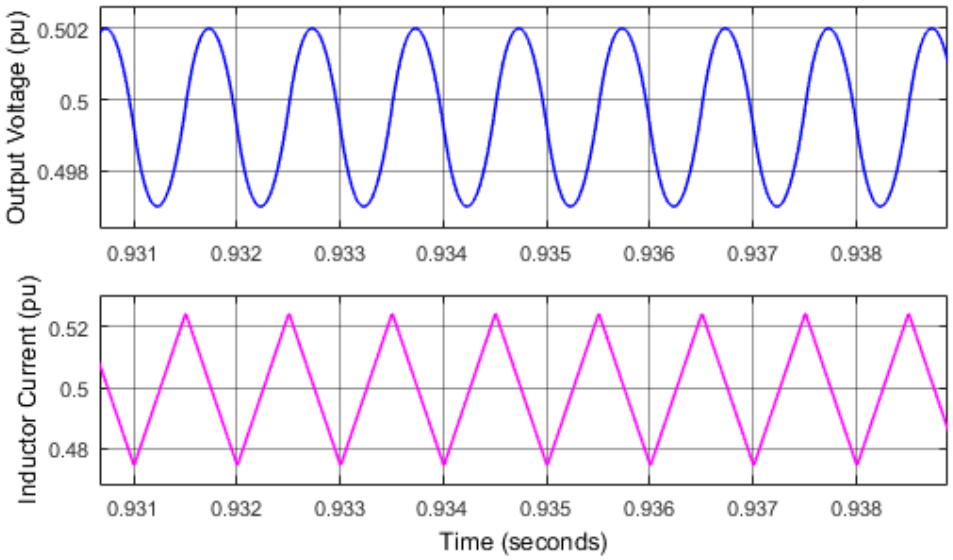

Figure 4.7: Validation results of the buck DC-DC converter model.

In addition, for specific applications, such as charging the battery in EVs, buck DC-DC converters may be required to transfer a constant power, that is switching from the voltage control mode to the power control mode. In this case, a closed-loop PI controller may be applied to realise a constant power transfer by continuously adjusting the voltage ratio. A power controlled buck converter model has been built and shared to the MathWorks [124]. As shown in Figure 4.8, the low-voltage side is connected to a simple battery model that consists of a voltage source and an internal resistance. The converter is required to transfer a specific power. Accordingly, a PI controller is employed, which determines the duty cycle by comparing the desired value of the power transfer with the measured value.

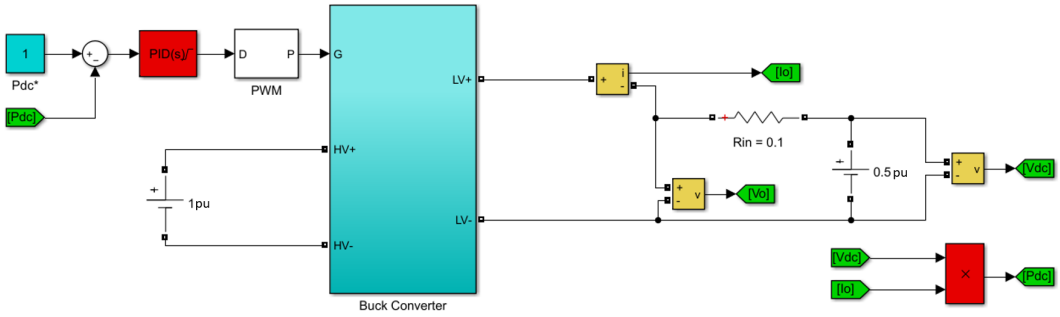

Figure 4.8: Closed-loop power control mode of a buck DC-DC converter.

The desired power (P_{dc}^{*}) is initially set at 1 pu, and after 0.5 seconds, the power is adjusted to 2 pu. From the simulation results shown in Figure 4.9, the output voltage only presents a little increase, but the current is doubled, thus the power is raised from 1 to 2 pu. Therefore, the modelled closed-loop control can realise control of power regardless of the form of the load.

4.2.2 Boost DC-DC Converter

A boost DC-DC converter [123] is a unidirectional step-up converter. Typical applications include providing power from a low-voltage DC generator to the DC network. Figure 4.10 presents the topological structure of the boost converter, which contains the same components as the buck converter, whilst the connection is different. Similarly, the operating voltage ratio can also be derived from the duty cycle but using a different formula, that is

$$\frac{V_o}{V_d} = \frac{1}{1-D} \tag{4.4}$$

As the duty cycle (D) is in the range of 0 to 1, the output voltage (V_o) is higher than the input voltage (V_d). A boost converter model is built as shown in Figure 4.11. To constrain the ripples of current and voltage, the inductance and capacitance are selected according to

$$\Delta i_{in}\% = \frac{DT(1-D)^2 R_L}{L}, \tag{4.5}$$

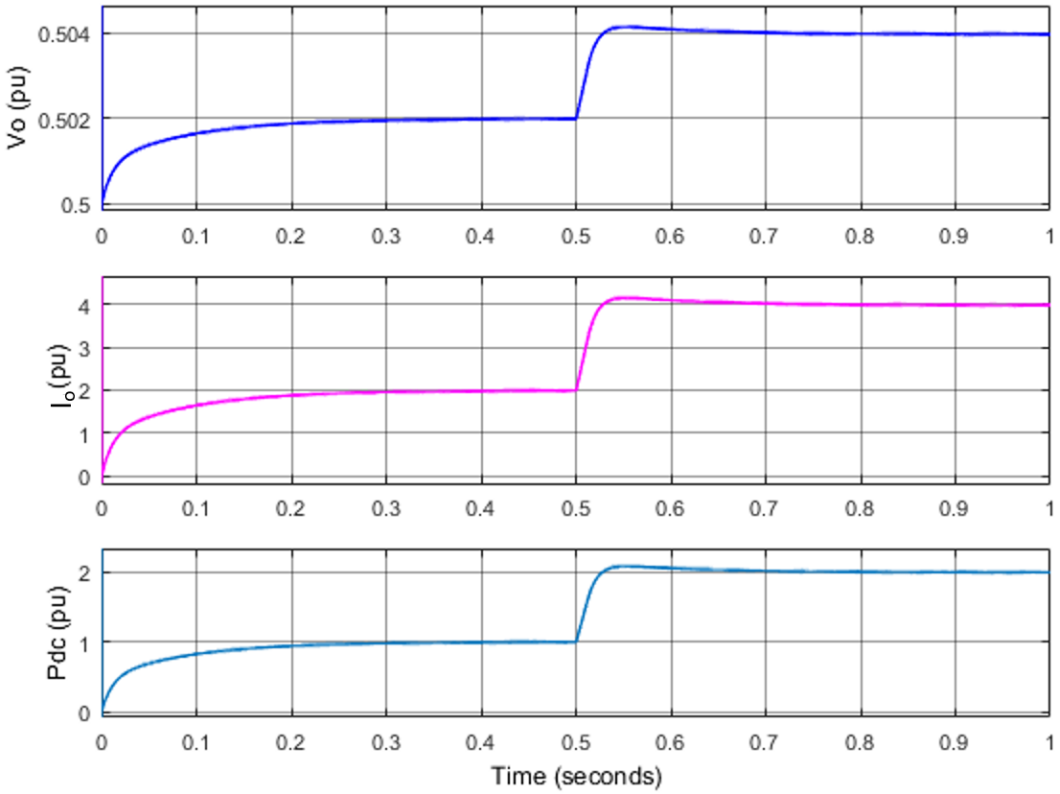

Figure 4.9: Simulation results of (a) output voltage (b) output current and (c) output power in the power control mode.

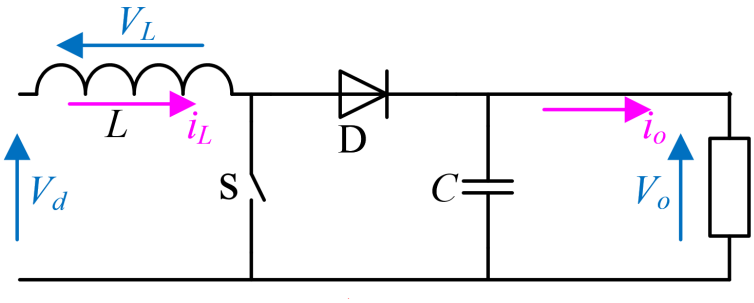

Figure 4.10: Topological structure of the boost DC-DC converter.

$$\Delta V_o\% = \frac{DT}{R_L C}. \tag{4.6}$$

Assuming both ripples are constrained to 1%, the inductance and capacitance are selected to 12.5 mH and 50 mF. The relevant parameter assignments are shown in Table 4.3.

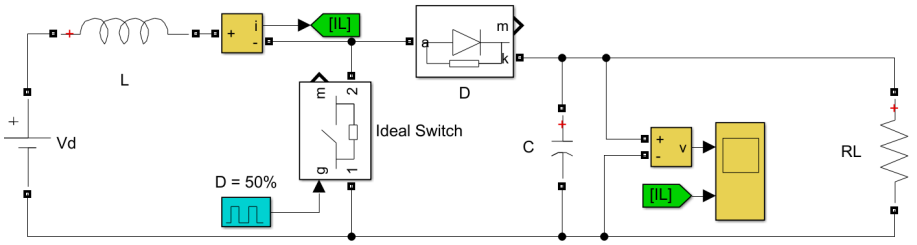

Figure 4.11: Topological structure of a boost DC-DC converter model.

Table 4.3: Relevant parameters of the boost DC-DC converter model.

V_d	V_o	D	V_D	R_D	ESR_C	L	C	R_L	f
1	2	0.5	0	1 mΩ	0	12.5 mH	50 mF	1 Ω	1 kHz

To verify the operation of the model, assuming that the duty cycle (D) is set to 0.5, the secondary voltage should be twice of the primary voltage according to Equation 4.4. The simulation traces are shown in Figure 4.12. The output voltage is twice of the input voltage as expected; the output current (I_O) is also doubled; the input current through the inductor (I_L) is equal to 4 pu to ensure the power balance on both sides of the converter.

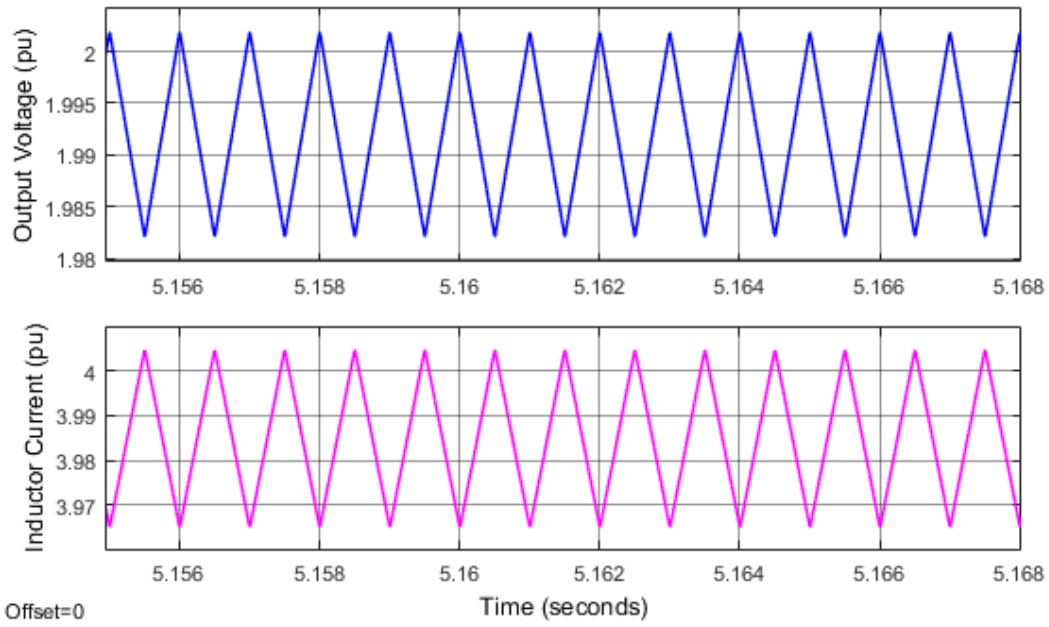

Figure 4.12: Validation results of the boost DC-DC converter model.

4.2.3 Dual-Active-Bridge DC-DC Converter

For applications such as ESS power management, bi-directional power delivery may be required. Dual-active-bridge (DAB) converters can realise bi-directional power transfer with constant voltages on both sides [125]. Figure 4.13 presents the topological structure that consists of four solid-state switches and a filter capacitor on each side, as well as one link inductor and a high-frequency transformer in the middle. Assuming the voltages on both sides are fixed, the switches on both sides will modulate the voltages into square waves in the middle stage of the converter. Recalling the operating principle of generators in the traditional AC grid, the power delivered to the grid is controlled by adjusting the phase difference of the sinusoidal-wave voltages across the link inductor. Similarly, the power transfer of the DAB converter can be controlled by adjusting the phase difference of the square-wave voltages across the inductor in DAB, where the power can be computed by [125]

$$P_{square} = \frac{nV_1V_2}{2\pi^2 f_S L}\varphi(\pi - \varphi), \tag{4.7}$$

where V_1 and V_2 are the DC voltage of each side; n is the turn ratio of the transformer, L is the inductance of the link inductor, f_S is the signal frequency of the square wave, and φ is the phase difference of the square-wave voltages across the inductor.

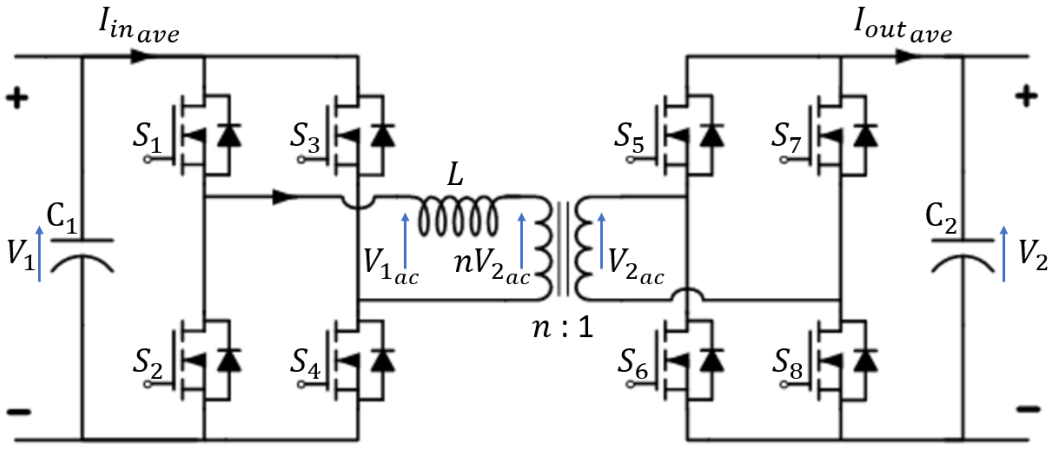

Figure 4.13: Topological structure of the Dual-Active-Bridge DC-DC converter.

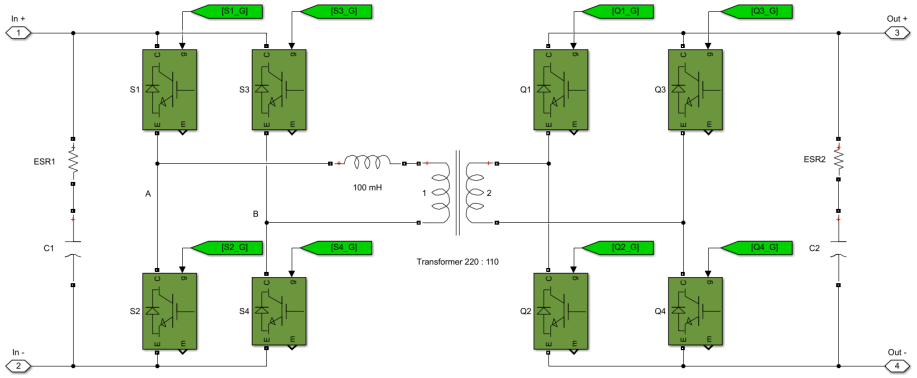

Figure 4.14: Simulink model of a DAB converter.

Table 4.4: Relevant parameters of the DAB converter model.

V_1	V_2	n	f_S	L	φ
220 V	110 V	220:110	1 kHz	100 mH	$-\pi$ to π rad

Figure 4.14 presents the topological structure of a DAB converter model, which is assumed to be connected to a 220/110 V DC system and the detailed parameters are shown in Table 4.4. Figure 4.15 demonstrates the control system of this model, where T_{hs} is the half-cycle time that is 0.5 ms in this case. The phase-shift ratio (D) is defined as the phase-shift angle divided by π, that is $D = \varphi/\pi$. Therefore, Equation 4.7 can be simplified as

$$P_{square} = \frac{nV_1V_2}{2f_SL}D(1-D). \tag{4.8}$$

To verify the correctness of this model, the phase-shift ratio (D) sweeps from -1 to $+1$, and the power transfer of the DAB converter is measured and the result is shown in Figure 4.16. According to Equation 4.7, the maximum power appears at $\varphi = \pi/2$, that is $D = 0.5$, and the maxima is calculated by

$$P_{square} = \frac{2 \times 220 \times 110}{2\pi^2 \times 1000 \times (100 \times 10^{-3})} \frac{\pi}{2} \left(\pi - \frac{\pi}{2}\right) = 60.5 \text{ W}. \tag{4.9}$$

As shown in Figure 4.16, the power transmission reaches its maximum value of 60 W as D is equal to 0.5. This result indicates that the DAB converter model is shown in Figure 4.14 is effective.

4.3 Renewable Components

Since an important motivation of using DC microgrids is to facilitate the integration of distributed renewable energy sources, it is necessary to also model typical renewable components. Accordingly, after modelling the necessary PECs, this section will introduce the modelling process of PV panels and ESS arrays.

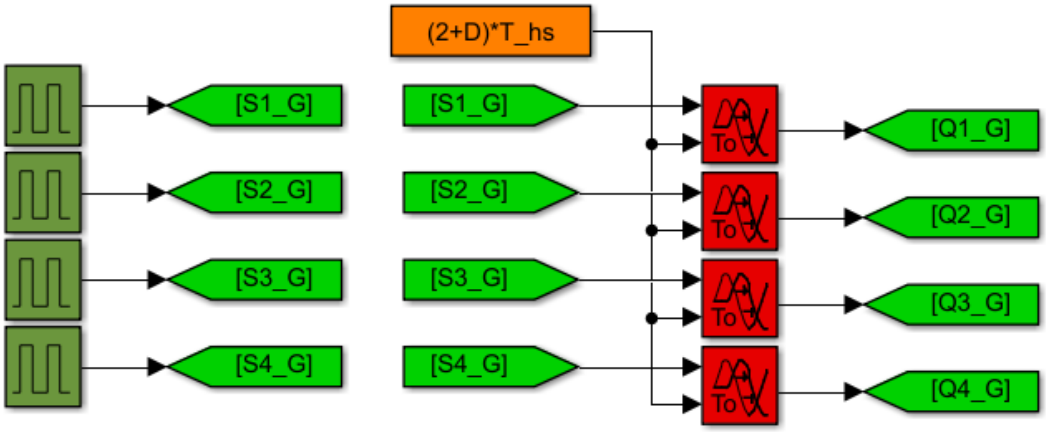

Figure 4.15: Details of the DAB converter control model.

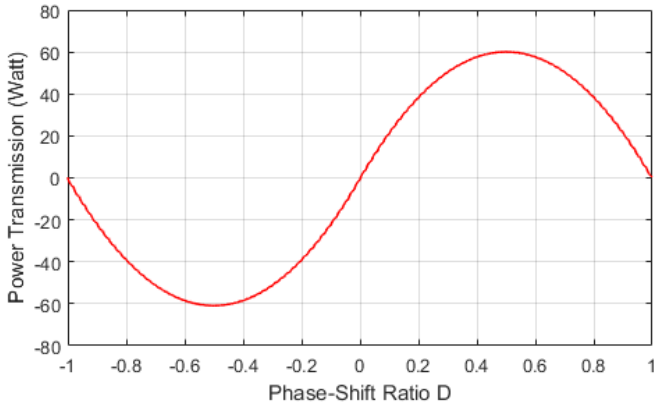

Figure 4.16: Validation results of the DAB converter model.

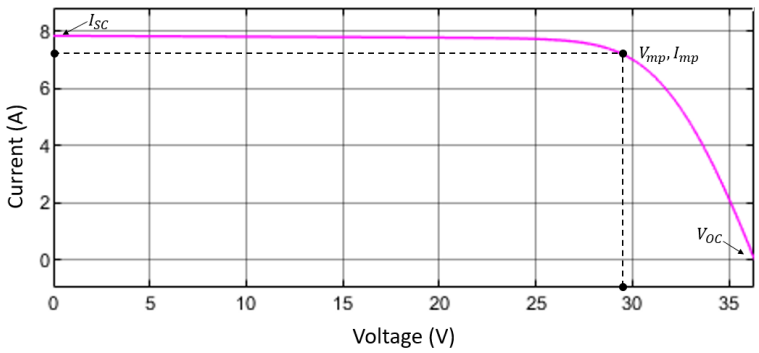

Figure 4.17: Typical I-V characteristic diagram of the PV panel.

4.3.1 PV Panels

The photovoltaic (PV) panel is a typical DC energy source that is being rapidly popularised. Since the energy conversion of PV panels is a physical process, it is necessary to establish an equivalent circuit to enable modelling. The characteristic of current and voltage was determined experimentally as shown in Figure 4.17 [126]. According to this characteristic curve, an equivalent circuit was proposed as shown in Figure 4.18 [126]. The circuit consists of a current source, controlled current source, and series and shunt internal resistances. The current source provides a constant current (I_L) that is related to the solar illumination intensity, and the internal resistances depend on the property of the PV panels. The controlled current through the diode is determined by the temperature and the voltage [126], that is in accordance with

$$I_d = I_0 \left[exp\left(\frac{V_d}{V_T}\right) - 1 \right], \tag{4.10}$$

$$V_T = \frac{kT}{q} \cdot nT \cdot N_S. \tag{4.11}$$

where the parameters are explained, and the values are assigned in Table 4.5 [126].

According to the equivalent circuit in Figure 4.18 and the parameter assignments in Table 4.5, the PV panels can be modelled as shown in Figure 4.19 to approximate the current-voltage characteristic curve. The model can be encapsulated in a subsystem, with the inputs of illumination intensity and temperature and the output of the electri-

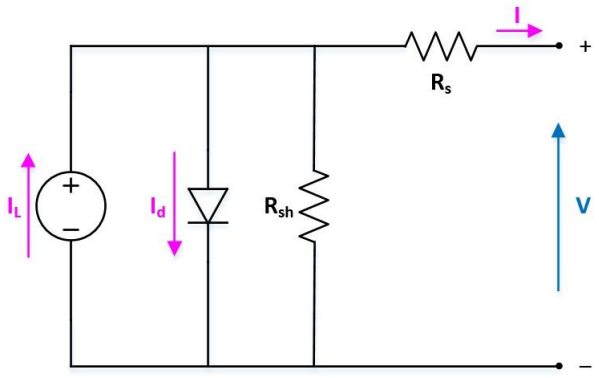

Figure 4.18: Equivalent circuit of a PV module.

Table 4.5: Relevant parameters of the PV panel model in Figure 4.19.

Name	**Symbol**	**Typical Values**
Light-generated current of each cell	I_L	7.8654
Equivalent series resistance (Ω)	R_s	0.39381
Equivalent shunt resistance (Ω)	R_{sh}	313.0553
Diode current (A)	I_d	(computed)
Diode voltage (V)	V_d	(measured)
Diode saturation current (A)	I_0	2.9259×10^{-10}
Diode ideality factor	nI	1.0
Boltzmann constant (J/K)	k	1.3806×10^{-23}
Charge of an electron (C)	C	1.6×10^{-19}
Cell temperature (K)	T	298.15
Number of cells per module	N_{cell}	60
Number of modules connected in series	N_S	2
Number of strings of series-connected modules that are connected in parallel	N_P	100

cal port. To verify the correctness of this model, as shown in Figure 4.20, the PV panel is connected to a controlled voltage source, of which the value varies from 0 to 72 V. Figure 4.21 demonstrates the results of current and power variation with the external voltage. By observing the measured value of PV output current, it indicates that the response of this model is consistent with the curve in Figure 4.17. In addition, it can be seen from the power curve that in the process of voltage rise, the output power of PV panel increases gradually and decreases rapidly after reaching the highest point.

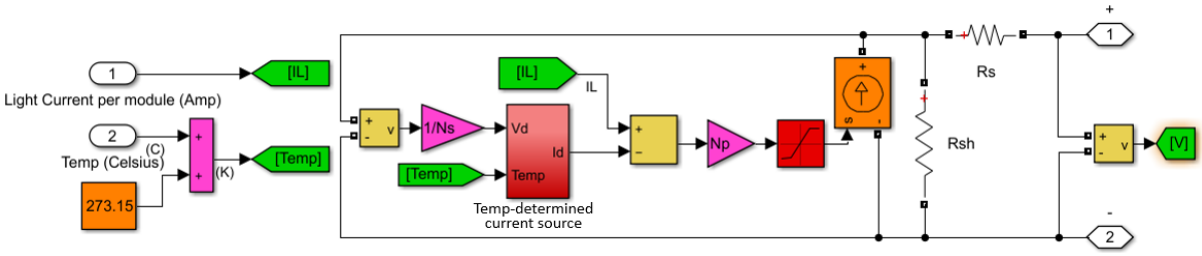

Figure 4.19: The model based on the equivalent circuit of PV panels.

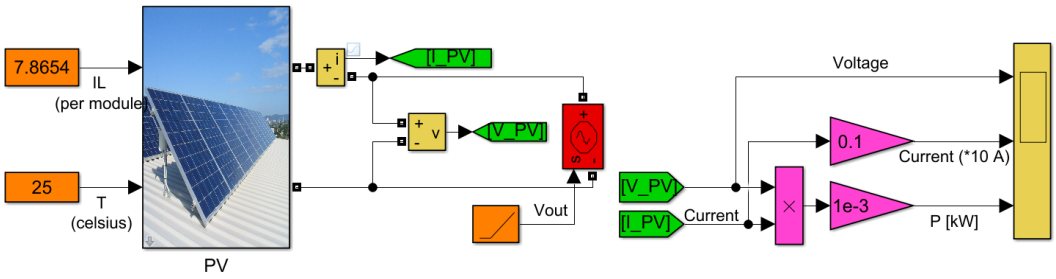

Figure 4.20: Test platform for the model of PV panels.

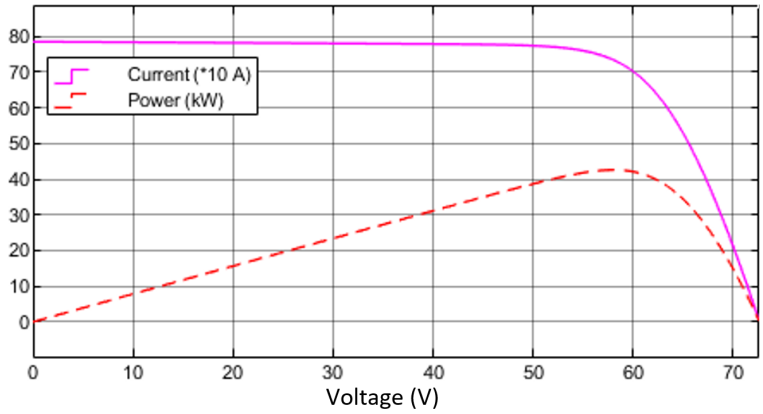

Figure 4.21: Validation results of the model of the PV panels.

4.3.2 Energy Storage Systems

Another important component of DC microgrid is the Energy Storage System (ESS), because it can manage energy flexibly and maintain normal voltage during the islanded condition. This section will take lithium-ion batteries as an example to model an ESS according to its mathematical model. As illustrated in Figure 4.22 [39], the equivalent circuit of ESS consists of one internal resistance and one controlled voltage source. The

Table 4.6: Relevant parameters of the ESS model in Figure 4.24.

Name	Symbol	Typical Value
Nonlinear votlage (V)	E_{charge} & $E_{discharge}$	0 to 1.2 E_0
Constant nominal votlage (V)	E_0	12
Polarization constant (V/(Ah))	K	0.0075265
Low frequency current dynamics (A)	i^*	(measured)
Extracted capacity (Ah)	it	(computed)
Maximum battery capacity (Ah)	Q	6
Exponential votlage (V)	A	0.61167
Exponential capacity $(\text{Ah})^{-1}$	B	11.308
Number of battery-cells connected in series	N_S	20
Number of strings of series-connected battery-cells that are connected in parallel	N_P	100

internal resistance of ESS is a constant determined by the type of battery, whilst the controlled voltage depends on the state-of-charge (SoC). For lithium-ion batteries, the value of the controlled voltage source under charging and discharging mode can be derived by the integration of the measured current. These are [39]

$$E_{charge} = E_0 - K \cdot \frac{Q}{it + 0.1Q} \cdot i^* - K \cdot \frac{Q}{Q - it} \cdot it + A \cdot \exp(-B \cdot it), \tag{4.12}$$

$$E_{discharge} = E_0 - K \cdot \frac{Q}{Q - it} \cdot i^* - K \cdot \frac{Q}{Q - it} \cdot it + A \cdot \exp(-B \cdot it), \tag{4.13}$$

where the parameters are explained and assigned with typical values, as shown in Table 4.6.

According to the equivalent circuit and mathematical model shown in Figure 4.22 and the typical parameter values given in Table 4.6, an ESS model is established. The equivalent circuit model is shown in Figure 4.23, and the implementation of the mathematical model is built according to Equation 4.12 and 4.13 and shown in Figure 4.24 which .

To verify the correctness of the ESS model, the electrical interface of the ESS model is connected to a constant current source of 10 A to observe whether the voltage and SoC can change correctly. The simulation result is shown in Figure 4.25. Initially, when

the battery is almost fully charged, the voltage will be slightly higher than the rated voltage. When SoC is between 20% and 95%, the voltage is almost constant. When the SoC is low (less than 20%), the voltage will drop sharply.

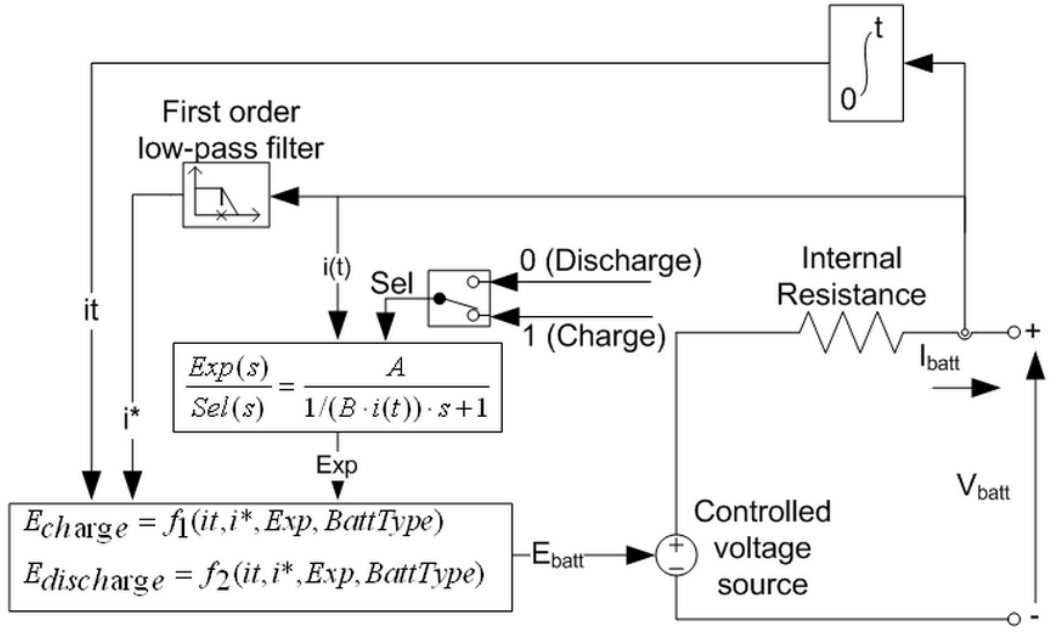

Figure 4.22: Equivalent circuit and the mathematical model of the ESS [39].

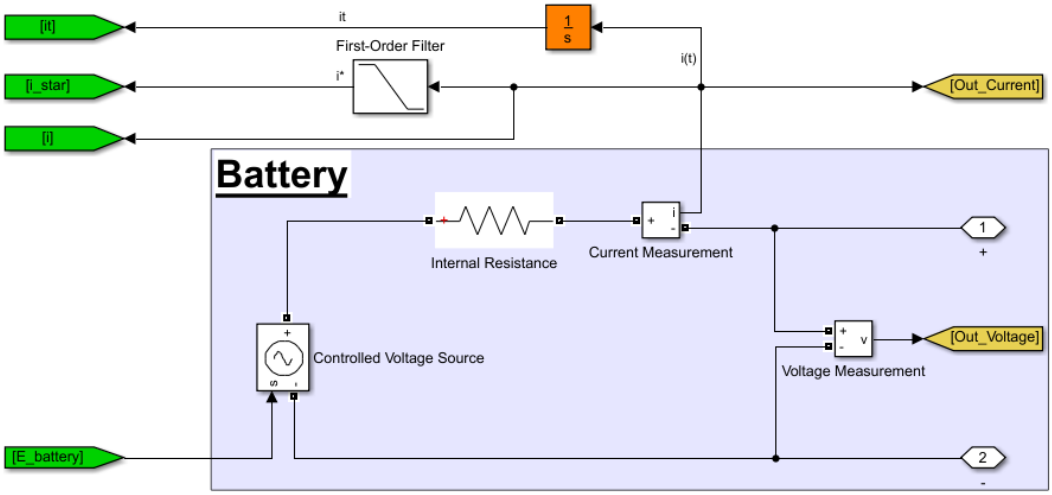

Figure 4.23: The model based on the equivalent circuit of ESS.

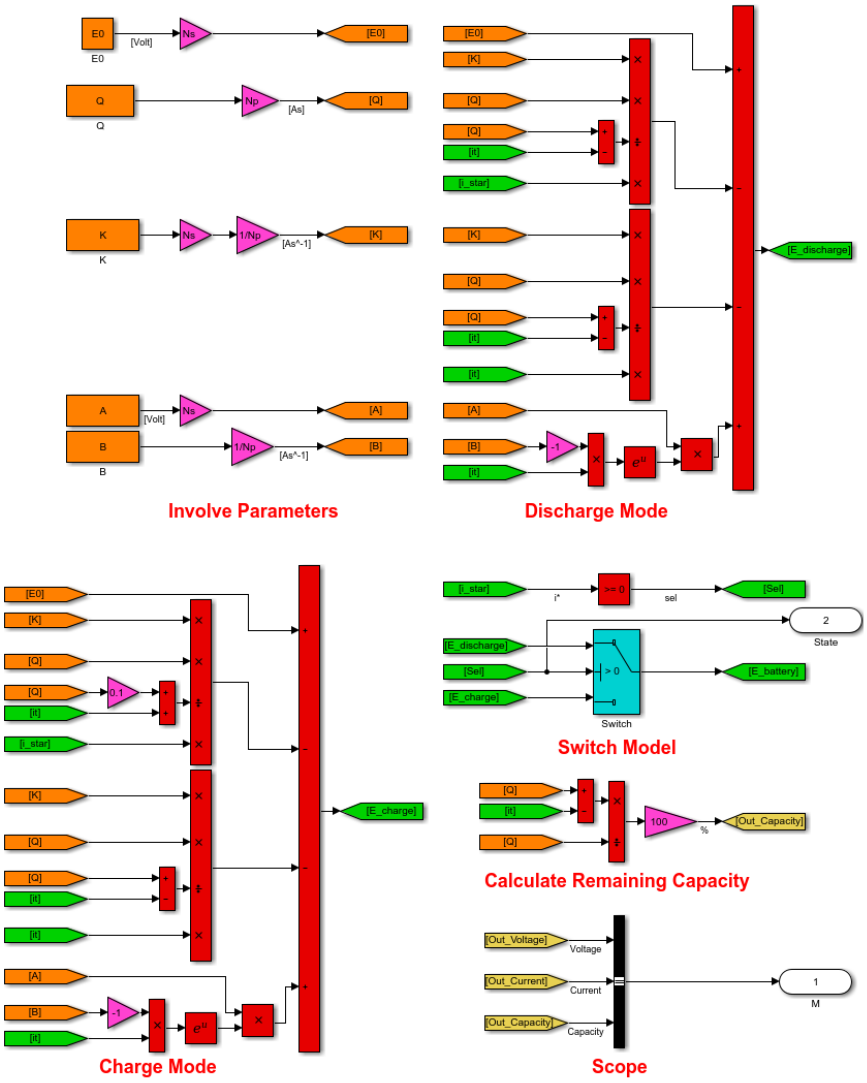

Figure 4.24: Implementation of the mathematical model of the ESS.

4.4 Implementation of a Single-Bus LVDC Network by Integrating Components

By combining the mentioned models in each section of this chapter, a single bus LVDC network can be implemented. This compact LVDC model is shown in Figure 4.26 [122], which integrates the AC grid, PV panels, battery arrays, and two DC loads.

The top subsystem is the grid infeed block which consists of a three-phase AC source

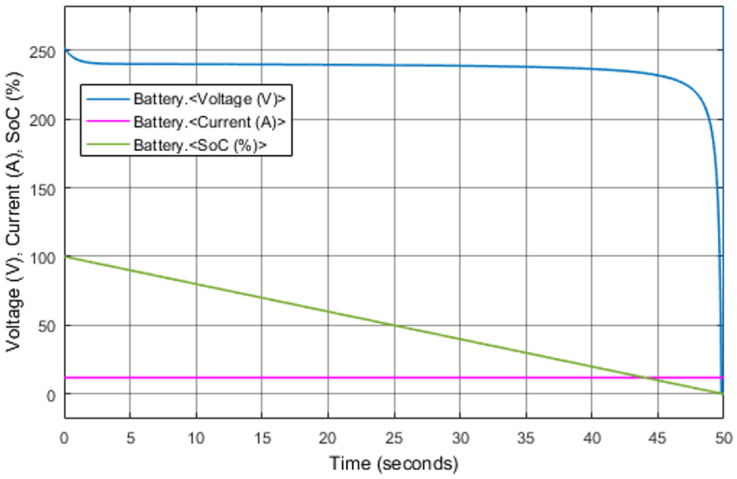

Figure 4.25: Validation results of the model of the ESS.

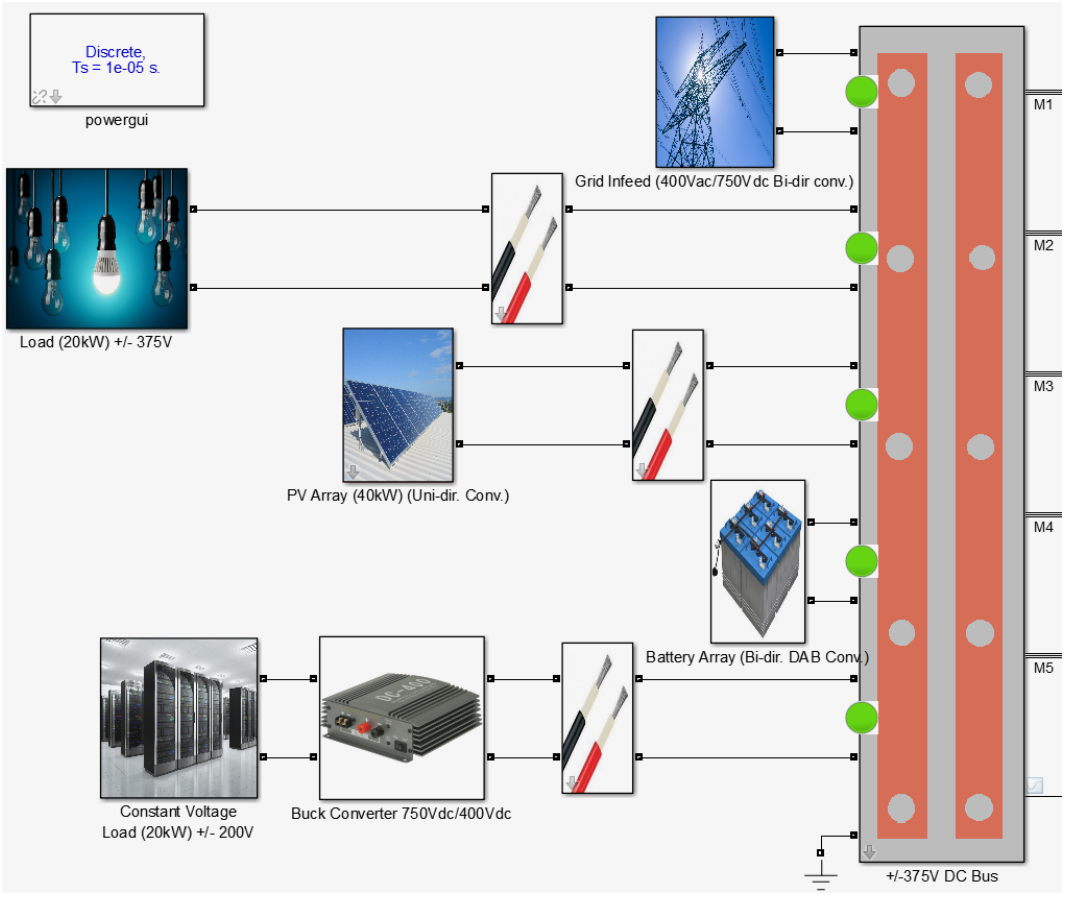

Figure 4.26: Single-bus LVDC network model.

and a two-level bidirectional AC-DC VSC. The converter applies DC voltage control to maintain the DC system voltage at 750 V, thus ensuring the power balance of the DC system. The first load block is connected to the DC bus through a 1 km line, which absorbs 20 kW power from the system. Due to the existence of line impedance, the load terminal may present a small voltage drop, which may cause the actual consumed power to be slightly less than its rated power. The PV array block consists of 2 series $\times$ 100 parallel PV modules. The characteristic curves are shown in Figure 4.21 in Section 4.3.1, where the maximum output power is approximately 42 kW. To reduce the computational pressure of this DCMG model, the PV array is designed to output a constant 40 kW power to the two loads in the DC system rather than employing the maximum power point tracking (MPPT) control strategy. To realise this, a DC-DC boost converter is required [91] to control the voltage ratio to maintain the PV-side voltage at approximate 52 V. The battery array block consists of 100 packs in parallel, and each pack contains 20 cells in series. As the rating of each battery-cell is 12 V and 6 Ah, the battery array is 240 V and 600 Ah, where the characteristic curves are shown in Figure 4.25 in Section 4.3.2. Since the battery voltage is different from the DC system voltage, a DC-DC converter is required to control the power transfer. The DAB converter is a suitable choice because the voltages on both sides are constant and bidirectional power transfer is required to charge and discharge the battery array [38]. The second load block is a 400 V 20 kW DC constant voltage load that is also connected to the 750 V DC bus via a 1 km line. This load is assumed to require exactly 400 V, provided through a buck DC-DC converter. Due to the presence of line impedance, the high voltage side of the converter may be slightly less than 750 V, hence the converter needs to control the voltage ratio to ensure the low-voltage side is maintained at 400 V.

In order to verify this model, the five components are sequentially connected to the DC system. Figure 4.27 presents the power transfer between each component and the microgrid, and Figure 4.28 illustrates the voltage change on the bus during the progress. At $t = 0.2$ seconds, the grid block is connected onto the bus so that the DC

voltage is under control and maintained at 750 V DC. At $t = 0.4$ seconds, load 2 is connected. Since the load voltage is controlled to ± 200 V, the total consumed power is slightly higher than 20 kW due to the power loss on the cable. In the meantime, as the grid block is controlled to maintain the nominal voltage, the generated power will provide the exact demand power of the load. The DC voltage presents a short-term fluctuation then quickly recovers to steady-state. At $t = 0.6$ seconds, load 1 is connected. Due to the voltage drop across the cable, the load voltage is slightly lower than its nominal voltage, hence the consumed power is slightly less than 20 kW. Similarly, the grid block will provide the balanced power of the total demand, and the voltage presents a short change. At $t = 0.8$ seconds, the PV array is switched on to provide a constant 40 kW power. As the grid-tied AC-DC converter operates under the DC voltage-controlled mode, the grid block reduces the power infeed to a very low level to maintain a normal voltage. At $t = 1$ seconds, the grid block is disconnected so that the DC bus loses voltage control. Accordingly, the voltage keeps decreasing until the grid is reconnected at $t = 1.2$ seconds. At $t = 1.4$ seconds, the battery array is switched on. The battery first operates in the charge mode, where the grid will provide equal power. At $t = 1.6$ seconds, by adjusting the DAB, the battery is switched to the discharge mode, then the DC network will output the excess power to the AC grid system through the bidirectional AC-DC converter. Throughout the process, the voltage remains stable and the voltage fluctuations on the DC bus do not exceed 5%.

4.5 Validation of Fault Current Responses in LVDC Networks

Section 4.4 has established the DC microgrid (MG) model and verified the functionality of the control system. This model provides the convenience of observing any circuit responses in the DC network during events. Based on this model, this section will present a case study to compare the simulation results to the calculated theoretical fault responses presented in Section 3.1.

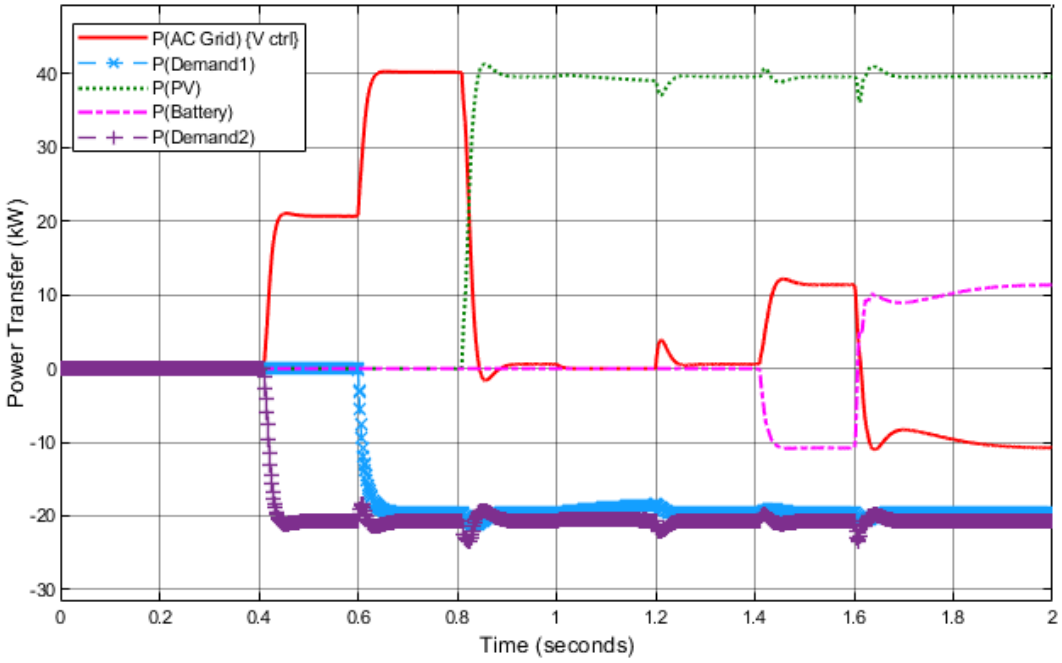

Figure 4.27: Example of power transfer between each component in the DC microgrid.

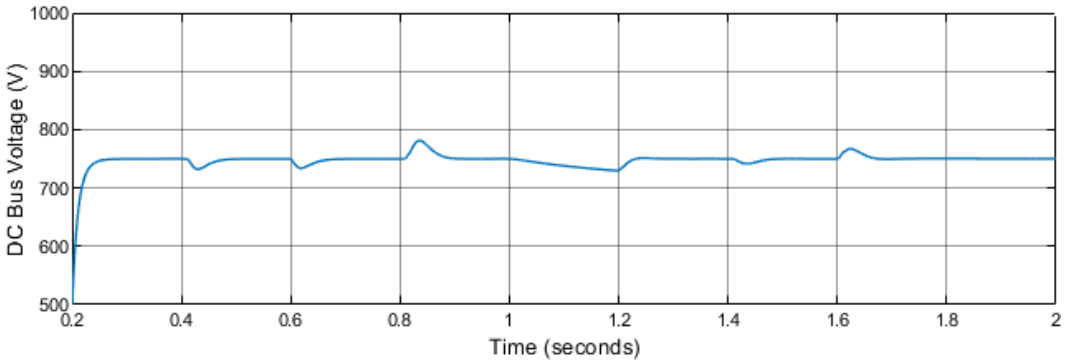

Figure 4.28: DC bus voltage of the DC microgrid model.

The test platform will adopt the model mentioned in Section 4.4, however, to avoid the fault current developing in an infinite slope, cables of different lengths are added between each of the network components and the main bus as shown in Figure 4.29, where the cable parameters are according to [115]. A low-impedance fault (1 mΩ) is applied to the main distribution busbar, and the simulated fault current response on each branch is measured and compared with the theoretical waveform according to Equation 3.2 and 3.4.

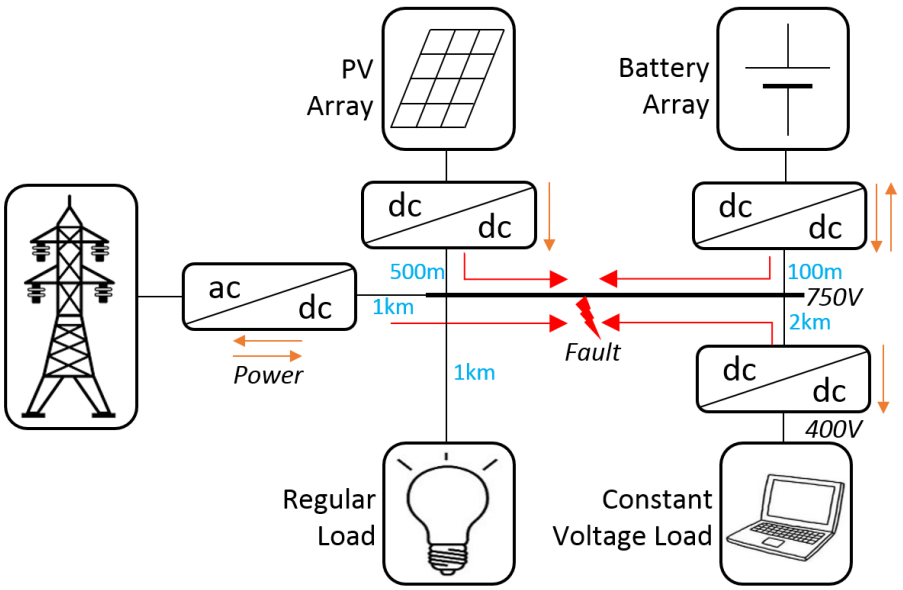

Figure 4.29: Diagram of the DC microgrid model.

The simulation results from the active branches are shown in Figure 4.30 with the solid-line plots, and the calculation results are presented with the blue plots. These comparisons indicate that the fault current behaviour prior to the occurrence of the first peak shows good alignment. (The regular load branch does not provide a transient fault current as it has no capacitor at the demand-side.) Although after the peak value, the two curves show a trend of separation which is because the PECs will try to restore the voltage, and this aspect of behaviour is not captured in the theoretical analysis. The further analysis presented in Table 4.7 summarises the comparison of simulation and calculation results of the peak magnitude and peak time for the fault current measured at each branch. The results obtained show that the errors of all theoretical predictions are less than 10% from that of the simulated responses. The close similarity between theoretical calculation and simulation results indicates that the capacitor discharge dominates the fault current transient. Accordingly, the following conclusions can be deduced:

1. For low impedance short circuit faults, where there is a sufficient decoupling between the responses of individual branches of the DCMG, the transient fault

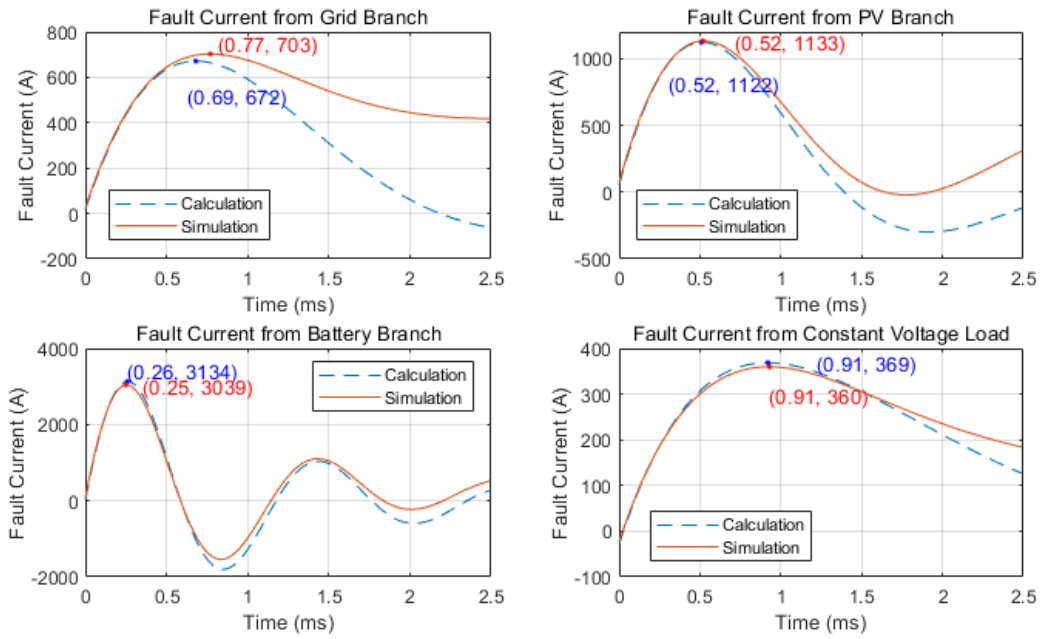

Figure 4.30: Comparison between the theoretical fault response and simulation results of DCMG fault response at grid feeder.

Table 4.7: Comparison of theoretical and simulated peaks.

Branch	**Theoretical Calc.**	**Simulation**	**Errors**
AC Grid	(0.69 ms, 672 A)	(0.77 ms, 703 A)	(10%, 4.6%)
PV Array	(0.52 ms, 1122 A)	(0.52 ms, 1133 A)	(0, 1.0%)
Battery Array	(0.26 ms, 3134 A)	(0.25 ms, 3039 A)	(3.9%, 3.0%)
Const. Volt. Load	(0.91 ms, 369 A)	(0.91 ms, 360 A)	(0, 2.4%)

current can be reliably approximated by the presented analysis of the nearest RLC circuit.

2. The converter contribution of fault current in response to a low-impedance fault does not greatly impact on the magnitude of the first current peak associated with the capacitor discharge.

Therefore, in a multi-terminal DCMG, it can be assumed that the current response before the peak point can be approximated in accordance with the calculation results of RLC circuit discharge. Hence, it can be used as a simple model for designing DC protection schemes without considering the current contribution from the PEC unless

those protection schemes rely on an accurate representation of the PEC fault current infeed after a collapse of the main bus voltage.

4.6 Summary of Chapter 4

This chapter has presented a single-bus DC microgrid model for analysing DC microgrid behaviours during different events. The model involves the key components that are commonly utilised in DC distribution networks, including the AC grid, PV panels, batteries, and low-voltage DC loads. Each component is interconnected with the corresponding power electrical converter.

The AC grid is configured to control the voltage on the main bus through a two-level AC-DC converter, whilst the other components can be controlled to release or absorb a specific power. From the validating results, the AC grid branch can adjust the transferred power to maintain the normal voltage regardless of changing the consumed or generated power of the system. This indicates the control system of this model is effective to maintain the normal operation of the DC network.

Based on this model, a short-circuit fault is applied to the main bus to validate the fault response of each PEC. The results show that the fault current before the peak value is nearly consistent with the theoretical calculation results (RLC discharge). The fault current after the peak point gradually separates apart from the theoretical result as the PEC will contribute more current due to dynamic control. However, for the consideration of fast-acting protection schemes where fast-growing DC fault current needs to be restrained or isolated before the peak current value occurs, the fault current can be assumed as an RLC discharge. Therefore, in the later chapters, a single capacitor is used to represent the contribution of the PEC for validating the effectiveness of high-speed LVDC protection schemes.

Chapter 5

Proposed Multi-Sample Differential Protection Scheme in DC Microgrids

Section 3.5 briefly explained how a short time synchronisation error (TSE) may cause protection stability issues when an external zone fault occurs. One solution is to use more advanced hardware to overcome time synchronisation errors. However, reliable microsecond-level time synchronisation is difficult to achieve [127]. Even if it is achieved, a large number of more expensive components are needed, which is not conducive to the spread of large areas of low-power LVDC distribution network [128, 129]. An alternative solution is to overcome the impact of TSE on differential protection from the aspect of the algorithm. However, concerning high-speed protection, it is a challenge to ensure the protection stability, but also maintain the protection sensitivity of protection in case of internal-zone faults.

This chapter will firstly quantify the impact of TSE on protection stability, and explain the reasons why conventional solutions are not feasible to address the issue for high-speed protection. Accordingly, a new Multi-Sample Differential (MSD) protection scheme is proposed in this chapter to address the protection instability issue whilst

maintaining protection sensitivity for achieving more reliable high-speed LVDC differential protection.

5.1 Analysis of the Protection Instability Issue in Conventional High-speed LVDC Differential Protection

5.1.1 Quantification of the Impact of Time Synchronisation Error

Figure 5.1 illustrates a fundamental differential protection structure that is applied to an example DC network [115]. The relays at A and B will operate when each detects the current difference between its local and remote signals exceeding a predefined threshold. Accordingly, the current difference can be expressed as

$$\Delta i = i_1(t) + i_2(t - \Delta t), \tag{5.1}$$

where i_1 and i_2 are the current measurements at A and B respectively; t represents the time after the fault occurs; Δt is the time of communication delay from B to A; Δi is the calculated current difference.

During an internal fault condition, the current difference, Δi, will increase rapidly to reach the predefined trip-threshold, causing the relay to trip. For an external fault condition, the current difference will theoretically be zero and the relay will remain sta-

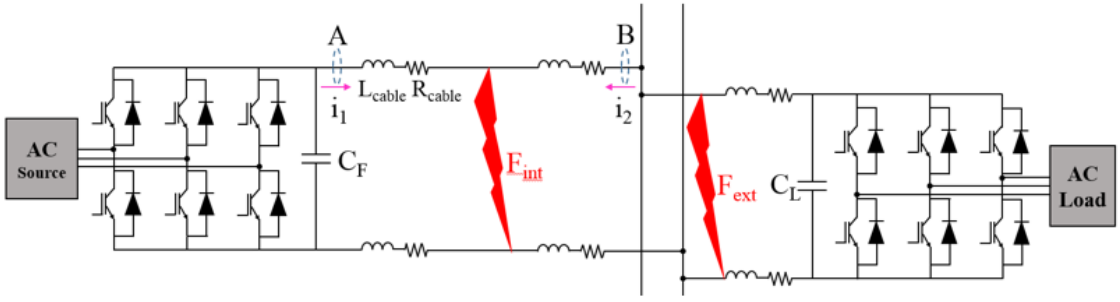

Figure 5.1: Equivalent configuration of current differential protection scheme [115].

Table 5.1: DC microgrid network parameters.

$V_{C_F}(0)$	$i_L(0)$	R (per meter)	L (per meter)	C_F	$C_{F_{ESR}}$	d_{AB}
400 V	125 A	0.64 mΩ	0.34 μH	56 mF	2 mΩ	35 m

ble (i.e., the relays must not operate.). However, where current measurements are not exactly synchronised, a high di/dt from an external fault may result in a large current difference error that causes an undesired trip, causing protection instability issues.

Consider the simulated DC network structure illustrated in Figure 5.1 with circuit parameters shown in Table 5.1. The differential protection relay at point A compares the local measured signal (measured at point A) and the remote received signal (transmitted from point B). An external fault, F_{ext}, is applied after 50 μs of simulation time, and a communication delay of 5 μs is applied to the remote measurement relative to the local measurement, as shown in Figure 5.2 (a). The results of the current difference between these two measurements are presented in Figure 5.2 (b). It is clear from this difference calculation that a short-term communication delay may cause a high current difference error during an external fault.

As indicated in Figure 5.2 (b), assuming the tripping threshold is 100 A, this current difference error will break the threshold and cause a relay mal-operation. Furthermore, the excessive current difference error may last for several hundred microseconds before it falls lower than the threshold.

The peak value of the current difference error under fault conditions can be quantified in terms of the circuit parameters under the fault condition. In the case of an ideal pole-to-pole short-circuit fault, the fault current response may be represented by a sinusoidal function [25] that can be expressed as

$$i(t) \approx \frac{v_{C_F}(0)}{L\omega_0} \sin(\omega_0 t), \tag{5.2}$$

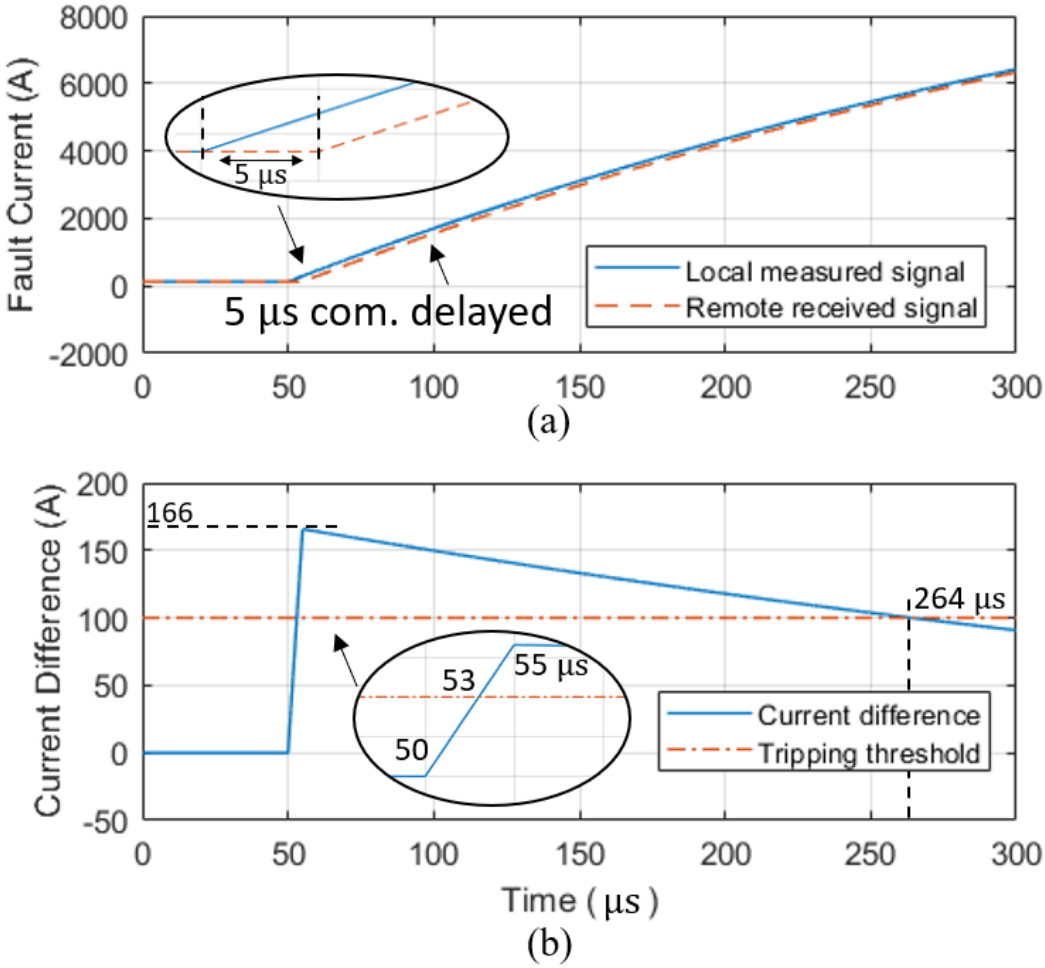

Figure 5.2: An example of (a) fault current measurements with communication delay, (b) current difference caused by TSE.

where $v_{C_F}(0)$ is the pre-fault voltage of link capacitor; L is the cable inductance from the capacitor to the fault; and ω_0 is the natural frequency of the fault.

Substituting Equation 5.2 into 5.1, the current difference error shown in Figure 5.2 (b) can be expressed as

$$\Delta i(t) = \begin{cases} \frac{v_{C_F}(0)}{L\omega_0} \sin(\omega_0 t), & (t < \Delta t) \\ \frac{v_{C_F}(0)}{L\omega_0} \left[\sin(\omega_0 t) - \sin(\omega_0 (t - \Delta t))\right], & (t \geq \Delta t) \end{cases}. \tag{5.3}$$

Applying the trigonometric equivalence formula

$$\sin\alpha - \sin\beta = 2\sin\frac{\alpha-\beta}{2}\cos\frac{\alpha+\beta}{2}, \tag{5.4}$$

Equation 5.3 as $t \geq \Delta t$ can be represented as

$$\Delta i(t) = \frac{v_{C_F}(0)}{L\omega_0} \cdot 2\sin\frac{\omega_0\Delta t}{2}\cos\left(\omega_0 t - \frac{\omega_0\Delta t}{2}\right), \quad (t \geq \Delta t). \tag{5.5}$$

Since $\sin x$ can be approximated to x when $x \ll \pi/2$, the current difference equations in Equation 5.3 can be simplified to

$$\Delta i(t) = \begin{cases} \frac{v_{C_F}(0)}{L}t, & (t < \Delta t) \\ \frac{v_{C_F}(0)}{L}\Delta t \cdot \cos\left(\omega_0 t - \frac{\omega_0\Delta t}{2}\right), & (t \geq \Delta t) \end{cases}. \tag{5.6}$$

From Equation 5.6 as $t < \Delta t$, Δi will initially develop rapidly and reach its peak at $t = \Delta t$, where the peak value $\Delta i_{\max} \approx \frac{v_{C_F}(0)}{L}\Delta t$. After the peak point, Δi will decay in terms of Equation 5.6 as $t \geq \Delta t$. Making derivative of Equation 5.6 as $t \geq \Delta t$,

$$\frac{\mathrm{d}\Delta i(t)}{\mathrm{d}t} = -\omega_0\frac{v_{C_F}(0)}{L}\Delta t \cdot \sin\left(\omega_0 t - \frac{\omega_0\Delta t}{2}\right), \quad (t \geq \Delta t), \tag{5.7}$$

it can be found that the decreasing rate is a very small negative number. Consequently, Δi will decay at a much slower rate than the initial increasing stage of the current difference profile. Accordingly, the high current difference error may last much longer in comparison to the desired high-speed trip-time.

5.1.2 Review of Conventional Solutions

There are a number of established solutions to this synchronisation error, which are summarised and discussed below.

Compensation Strategy

Conventional optical fibre based AC differential teleprotection employs IEEE Std C37.94-2017 [130], where the bitstream rate is 2048 kbps ± 100 ppm. Each data frame is allocated with 256 bits, resulting in a frame rate that is 8000 Hz ± 100 ppm. Each frame includes a unique 16-bit header to allow the receiver to synchronise the 256-bit frame. That is, each frame is marked with a local timestamp when captured. Then, the frames with the same timestamp are regarded as synchronised regardless of the communication delay. However, microsecond-level accuracy is still rarely achievable because of the clock drift. Due to the 100 ppm error tolerance, the number of frames per second is in the range of 7999.2 to 8000.8. Assuming the local and remote frame rates are 8000 and 8000.5 Hz, the data misalignment can occur, as illustrated in Figure 5.3.

In Figure 5.3, the frames marked with the same number represent those which share the same header. However, the frames may not correctly synchronise as the accumulation of clock drift will cause an increasingly large TSE. In this example, as each frame will accumulate a 7.8 ns time drift, 641 samples (80.13 ms) will cause a problematic 5 μs TSE. Dealing with this issue, the IEC 61850 [131] adopts IEEE C37.118 [132] to transmit synchrophasor information, in which NTP (Network Time Protocol) [133] or Precision Time Protocol (PTP) [134] is employed to calibrate the clock with the Delay Request-Response Mechanism (also known as Ping-Pong method). However, a typical NTP client polls the remote NTP server for calibrating every several minutes so that the target accuracy is few milliseconds [133]. The millisecond-level TSE is tolerable for AC network teleprotection, but DC network may require sub-microsecond accuracy

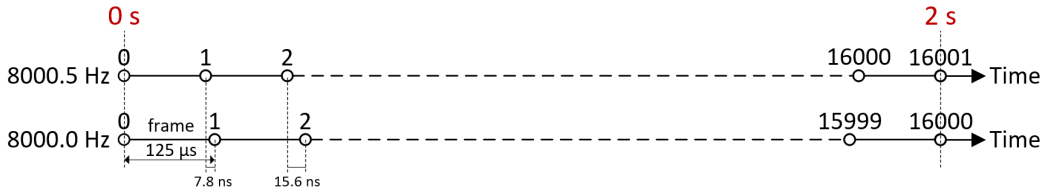

Figure 5.3: Explanation of clock drift.

according to the DC fault analysis. However, the implementation of sub-microsecond precision must be supported by advanced hardware, such as PTP, GPS-linked clock [135], and atomic clock [129]. Hence, whilst these technologies are effective in realising precise time synchronisation measurement in HVDC network travelling wave protection with GPS as presented in [135], these technologies may be considered too expensive for a distribution power network.

Widen Decision-Making Time-Window

A wider decision-making time-window can be employed to tolerate the impact of time synchronisation error. The relay should only trip when all the samples within the time-window exceed the tripping threshold. However, this action will reduce the detection speed during internal fault conditions. From the example shown in Figure 5.2 (b), the time-window should be set longer than 200 μs to avoid a false-trip during this external fault condition. Hence, this will also result in a minimum 200 μs trip time for internal fault conditions, which may be not acceptable in a high-speed protection scheme.

High Threshold Setting

A higher tripping threshold setting could make the protection relays more stable. However, this will also decrease the protection sensitivity for internal high-impedance fault detection. As shown in Figure 5.2 (b), the threshold should be set over 200 A to avoid the false-trip, but the protection may then fail to detect internal faults with an impedance of higher than 2 Ω. A typical arc fault resistance is considered between 0.01 and 5 Ω [136], which indicates that a high current threshold setting may lead to the risk of protection blindness to an arc fault.

To address the issue of protection stability for external faults, a multiple sample differential (MSD) protection scheme is proposed to improve protection stability and hence enable higher speed and sensitivity. This approach employs a one-dimensional

array for each current measurement channel which stores a predefined number of previous samples. The differential protection relay compares all the combinations of samples from the arrays, in which at least one precisely aligned comparison exists. During no-fault or external fault conditions, there exists at least one absolute value of combination lower than the preset current threshold. The converse-negative proposition must also be true: only if the absolute values of all combinations exceed the threshold, an internal fault is signified, and the relay must operate immediately. Accordingly, the stability issue caused by TSE can be addressed. This section will introduce the MSD protection scheme, propose the methodology for selecting the size of the array for each measurement channel, and the number of required differential calculations to reduce computational overhead.

5.2 Proposed Multiple Sample Differential Protection Scheme

High-speed differential protection may be applied to three configurations, including radial, teed and multi-terminal circuit structures, as shown in Figure 5.4, 5.5 and 5.6. Note that in all these cases, at the boundary of the differential zone, the direction of current flow into the zone is defined as positive. Regardless of the circuit structure, differential protection consists of one local measurement and one or more remote measurements. Assuming N_C is the number of measurement channels of any given differential protection structure, $N_C = 2$ represents a radial differential zone, $N_C = 3$ represents a teed differential zone, and $N_C \geq 4$ represents a multi-terminal differential zone structure.

5.2.1 Array Size Selection for Measurement Channels

Figure 5.7 presents an example of a three-channel relay including one local measurement and two remote measurements with different latencies. The sample alignments marked with the same number represent the ideally synchronised current samples captured at

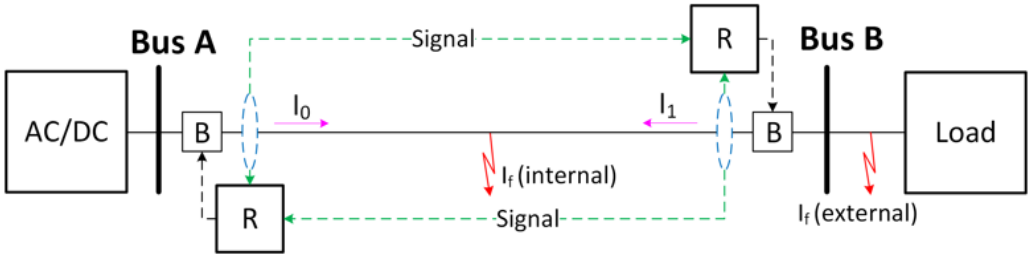

Figure 5.4: Differential protection of radial structure.

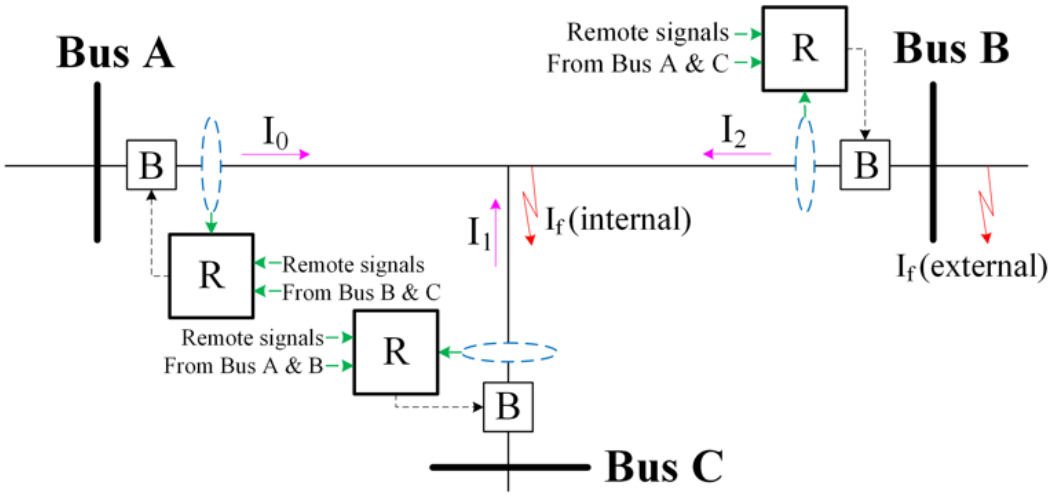

Figure 5.5: Differential protection of teed structure.

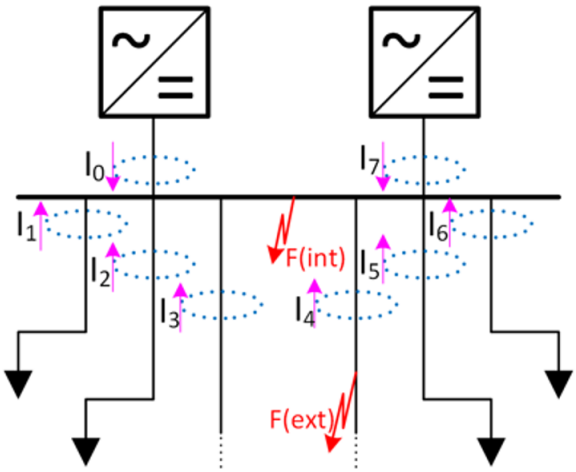

Figure 5.6: Differential protection of multi-terminal structure.

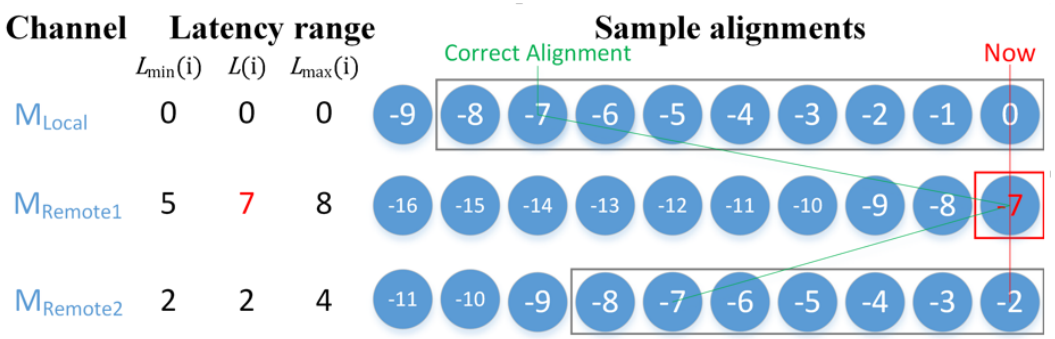

Figure 5.7: Example of signal alignment in a three-channel.

their local measurements. Note, the numbers presented are the sample number identifiers and not the measured current values. During signal propagation, an undefined latency may occur between the differential relay and its remote measurements. An example of latencies is shown in Figure 5.7, in which i is the individual measurement channel; $L_{\max}(i)$, $L_{\min}(i)$, and $L(i)$ are the maximum possible, minimum, and actual latencies of each channel with respect to the number of samples.

The selected array size must be wide enough such that at least one set of correctly aligned samples is included. This can be determined by $L_{\max}$ and $L_{\min}$ of each channel. If $L_{\max}$ of a given channel is the greatest compared to the other channels, this channel is known as the latest-channel. However, the latest-channel may be fixed or unfixed depending on its potential latency range. If the latency range of the latest-channel ensures that it is always the most delayed in comparison to all other remote channels, then this channel may be defined as a fixed latest channel (FLC). For example, channel M_{R1} in Figure 5.8 has a potential latency range of between 5 and 8 sample delays, whereas M_{R2} has a potential latency range between 2 and 4 sample delays. Accordingly, M_{R1} is guaranteed to always be more delayed than M_{R2}. However, if there is an overlap between the potential latency ranges of measurement channels, the current latest-channel is defined as being an unfixed latest-channel (ULC). As shown in Figure 5.9, the latency range of channel M_{R1} is modified between 1 and 8 samples, it has overlaps with the latency range of channel M_{R2}. Since channel M_{R1} still has the maximum possible delay ($L_{\max}$) but cannot be guaranteed to always be more delayed than M_{R2},

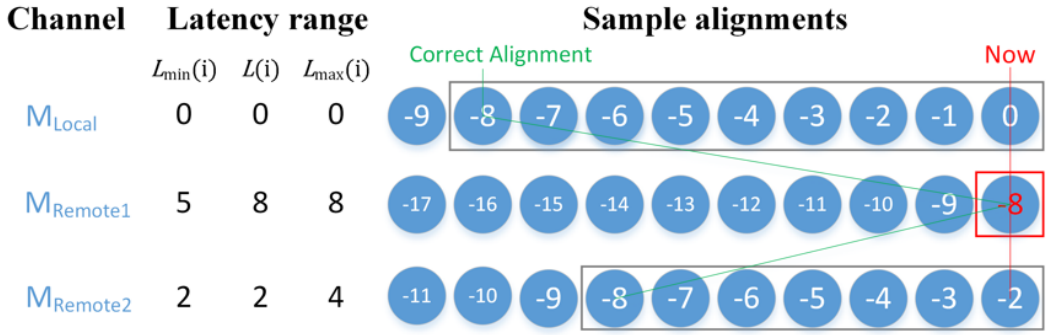

Figure 5.8: Array size selection with a FLC.

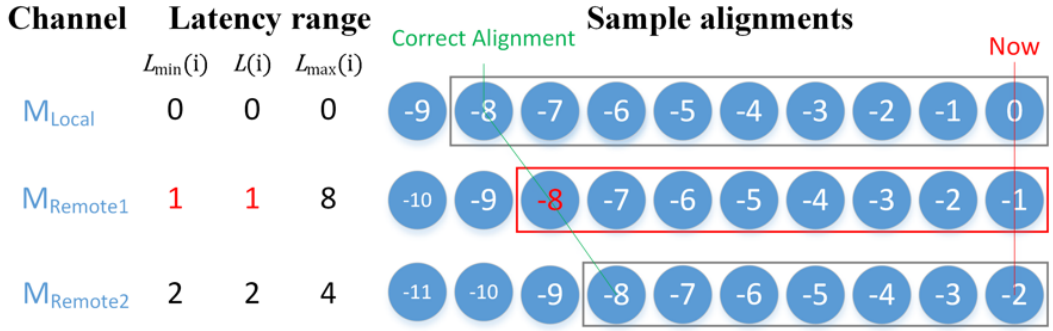

Figure 5.9: Array size selection with a ULC.

channel M_{R1} is regarded as an ULC.

By defining the number of samples stored in the array of channel i as $N_S(i)$, only one sample is required to be stored for the FLC. This is because FLC always provides the global latest sample from all channels which must be aligned with the local and other remote channels. The latest sample of the FLC defines the size of the array of the other remote measurement channels and the local channel correctly aligned. Considering the case shown in Figure 5.8, M_{R1} is an FLC array which includes only one sample in its array. The array size selections for the other channels must ensure the correct alignment of this sample exists. Accordingly, the criteria of array size selection for each non-FLC is defined in terms of the maximum and minimum latency of each channel, such that

$$N_S(i) = L_{\max}(\text{FLC}) - L_{\min}(i) + 1, \tag{5.8}$$

where $L_{\max}(\text{FLC})$ is the maximum latency of the FLC channel, and $L_{\min}(i)$ is the minimum latency of channel i ($i = 0$ for the local channel).

In the case that channel M_{R1} is a ULC as shown in Figure 5.9, the criteria of array size selection must be applied to all the measurement channels, whereby

$$N_S(i) = L_{\max}(\text{ULC}) - L_{\min}(i) + 1, \tag{5.9}$$

where $L_{\max}(\text{ULC})$ is the maximum latency of the ULC channel. Figure 5.8 and Figure 5.9 show examples of array size selection with rectangular blocks for both FLC and ULC conditions.

5.2.2 Sample Processing for Detecting Internal Faults

After the array size of each channel is selected using Equation 5.8 or 5.9, the relay should process the measurement signals to determine if an internal fault is detected.

The storage of sample values in each channel array is achieved by shift register technology. A tapped delay line (TDL) [137] may be employed to update the sample values S_j in each array. Figure 5.10 illustrates an array of size N_S that stores the latest samples in array positions from S_0 to S_{N_S-1}. When a new sample fills position S_0, the other samples will be transposed forward, and the earliest sample at position S_{N_S-1} is discarded.

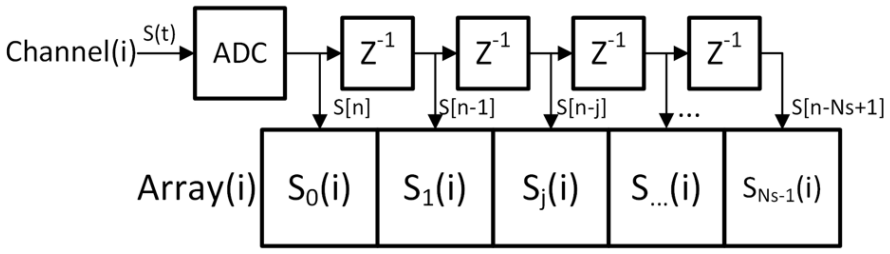

Figure 5.10: Tapped delay line of input signal from Channel i.

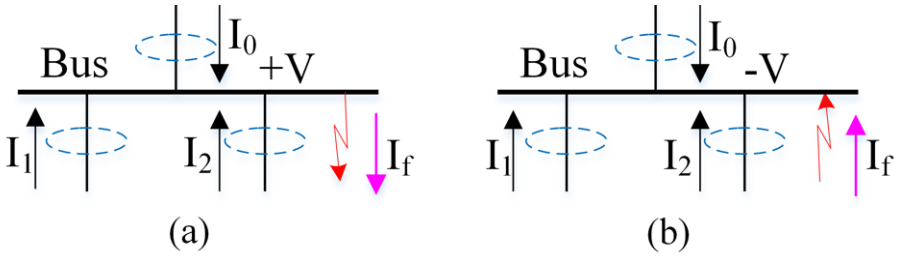

Figure 5.11: Types of (a) Current-out fault, (b) Current-in fault.

The principle of fault detection can be derived using contraposition theory: if there is no internal fault, there exists at least one summation of all possible array positions (which hence represents the correct alignment of samples) that is lower than the trip threshold. This is a true statement, so the converse-negative proposition is also true: if all summations exceed the trip threshold, then an internal fault exists. This principle is summarised in Table 5.2 , where $S_j(i)$ is the value of the sample at position j in channel i, and THR is the preset current difference trip threshold. Thereby, the operating principle of an internal fault may be expressed as

$$\forall \left| \sum_{i=0}^{N_C-1} S_j(i) \right| > THR. \tag{5.10}$$

Taking a sample from each channel, the protection relay should calculate the sum of all combinations, and operate if the values of all combinations are out of the range of $(-THR, THR)$.

However, summating all possible combinations of array positions may require considerable computational overhead. The number of combinations, C, may be determined

Table 5.2: Contraposition of operation principle.

If no internal fault,		then $\exists$	$\left\|\sum_{i=0}^{N_C-1} S_j(i)\right\|$	$\leq THR.$
If $\forall$	$\left\|\sum_{i=0}^{N_C-1} S_j(i)\right\|$	$> THR,$	then internal fault detected.	

by the array size of each channel, whereby

$$C = \prod_{i=0}^{N_C-1} N_S(i). \tag{5.11}$$

Consequently, the total number of combinations may be an extremely large number, if the number of channels, N_C, or the array size in each channel, N_S, is large. The example shown in Figure 5.9 results in $9 \times 8 \times 7 = 504$ combinations, however the array size in practice may be significantly larger. This may be demanding for the relay processors to realise high-speed operation. Accordingly, it is necessary to reduce the required computational overhead by optimising the algorithm.

Considering a single DC line, differential faults can be categorised as either current-out or current-in variants, as shown in Figure 5.11. During the current-out fault conditions (Figure 5.11 (a)) where the net current is positive, the protection relay should operate immediately when all summed combinations are greater than a preset positive threshold. Similarly, during current-in fault conditions (Figure 5.11 (b)), the relay should operate when all summed combinations are lower than a preset negative threshold.

Thereby, the operating principle in Equation 5.10 can be simplified and described in terms of these two conditions, whereby the selection of critical values (maxima and minima) takes place prior to the summation of computations, such that

$$\sum_{i=0}^{N_C-1} \min_{i,\, j=0\rightarrow N_S-1} \{S_j(i)\} > THR, \tag{5.12}$$

or

$$\sum_{i=0}^{N_C-1} \max_{i,\, j=0\rightarrow N_S-1} \{S_j(i)\} < -THR. \tag{5.13}$$

Consequently, the simplified operating principle requires the separate selection of the critical value of each array, followed by the summation to compare with the preset current threshold. In this example, instead of computing the 504 combinations, the

computation becomes selecting the maximum and minimum sample value from each of the three channels; adding the maximum and minimum values; and comparing the two summed critical values with the threshold respectively. Therefore, this optimised algorithm can dramatically reduce the computational overhead.

The logic flow-chart of this optimised MSD protection algorithm is illustrated in Figure 5.12. At every sampling instance, the local and remote measurement signals are fed into a TDL via an ADC and stored as an array of a pre-assigned length as defined by Equation 5.8 and 5.9. The maximum and minimum values from each array are selected and summed. According to Equation 5.12 and 5.13, the protection relay should operate when either the sum of maxima is lower than the negative current threshold, or the sum of minima is higher than the positive current threshold.

Considering hardware implementation, the function described in Figure 5.12 can be

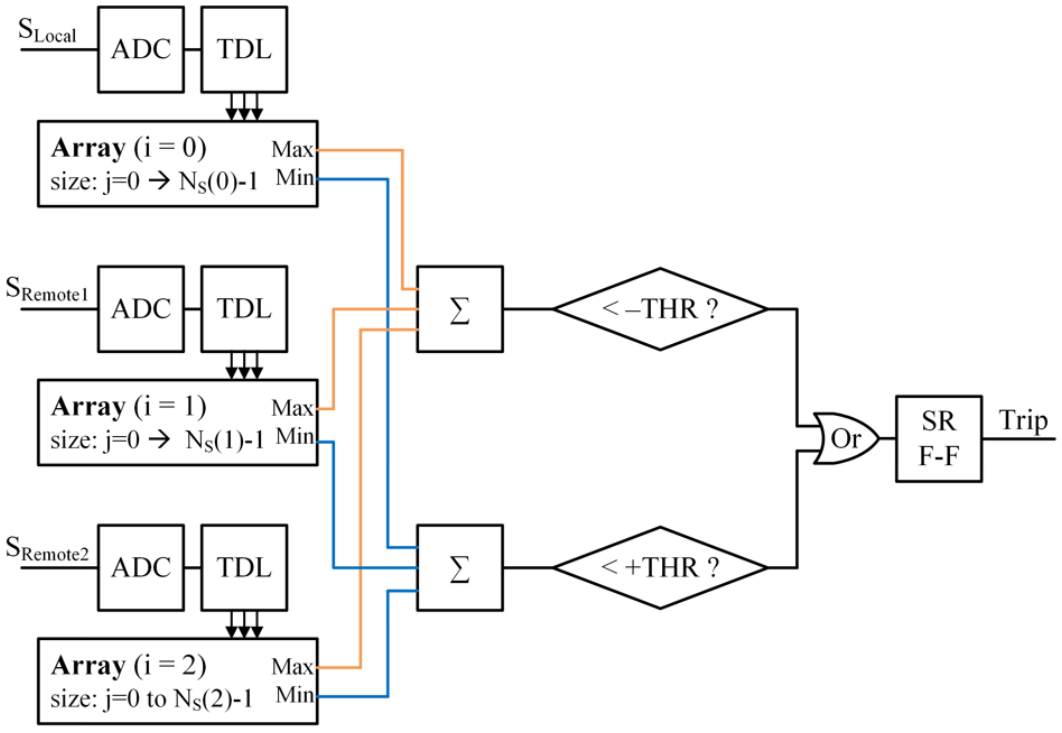

Figure 5.12: Protection algorithm of multi-sample differential protection scheme.

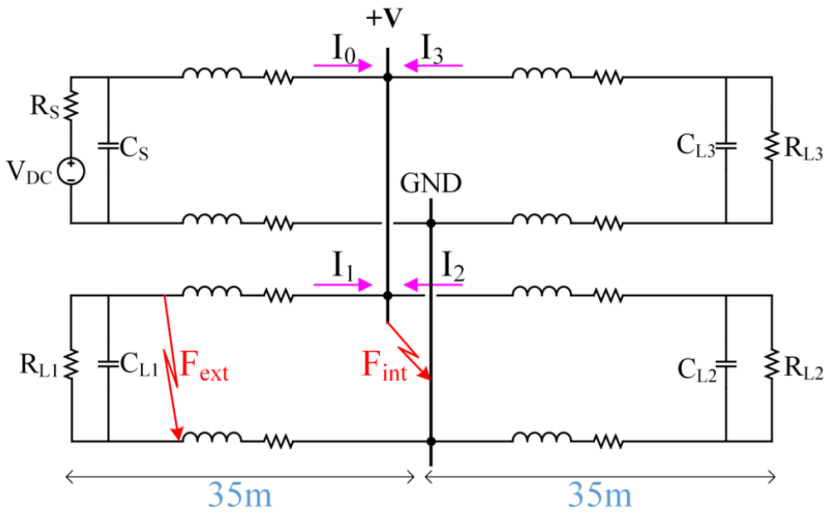

Figure 5.13: Circuit configuration of bus protection.

designed with Field Programmable Gate Array (FPGA), and eventually encapsulated into an Application-Specific Integrated Circuit (ASIC) that can be mass-produced. Compared with processors, the use of logic circuits can realise faster operation speed and lower costs [138].

Additionally, the use of the sample array provides more tolerance of accidental sampling errors. In this manner, the threshold (THR) does not need to be set high to overcome the impact of current difference caused by TSE as mentioned in Figure 5.2 (b). The THR setting only needs to consider the persistent noise to ensure protection stability.

5.3 Algorithm Validation with Simulation

To verify the effectiveness of the proposed method, a multi-terminal bus-bar protection scheme is considered. According to the conclusion drawn in Chapter 4, the fault current response of a PEC before the peak value can be represented by an RLC discharge. Figure 5.13 presents a schematic diagram of the representative DC power network, constructed within the MATLAB/Simulink environment, used for this case study. A

DC supply provides power to three active loads through the four-terminal bus-bar with internal and external fault cases considered. A comparison between uncompensated high-speed differential and MSD protection is undertaken to demonstrate the improvement of protection stability for external faults.

The DC source shown in Figure 5.13 is representative of a grid-connected voltage source converter. At the demand side, paralleled RC loads are employed to represent active loads, which may include converter-interfaced renewable energy resources, or energy storage systems. To validate the sensitivity of the MSD protection algorithm, a low-resistance external fault and a high-resistance internal fault are injected sequentially into the network.

As shown in Table 5.3, the details of circuit parameters are referred from [115] and [139], the voltage and current are normalised to unity, and the nominal current is evenly distributed to the three loads. The internal fault resistance is set high to validate protection sensitivity and the external fault resistance is set low to validate protection stability.

To implement the differential protection relay for the bus-bar, the current signals from all four channels are sent to a central relay with different latencies. An example of latencies of the current measurements are shown in Table 5.4. Since I_1 is the FLC, the array size of I_1 is 1. Assuming the sampling time, T_S, is equal to 5 µs. The array size (N_S) selections for other channels as defined by Equation 5.8 are also presented in Table 5.5.

Table 5.3: Element parameters.

V_{DC}	R_S [139]	C_S & $C_{L1,2,3}$	R, L (each line) [115]
1 pu	0.02 Ω	56 mF	11.2 mΩ, 5.95 µH
$R_{L1,2,3}$	$I_{n1,2,3}$	$R_{F_{int}}$	$R_{F_{ext}}$
3 Ω	0.333 pu	1 Ω	1 mΩ

5.3.1 Validation Results

The MSD algorithm is evaluated in simulation to validate the performance for external and internal faults on the network, as shown in Figure 5.13. The stability and sensitivity of this method is then compared to conventional uncompensated high-speed differential protection.

The current responses of the four measurement channels for an external fault condition are shown in Figure 5.14 (a). Figure 5.14 (b) shows the uncompensated sum of all 4 channels using a conventional differential protection scheme. The current difference, Δi, exceeds the current threshold (TRH set as ± 0.1 of load current) in 25 µs, and then falls below the threshold after 1.23 ms. Therefore, conventional high-speed differential protection may cause a false-trip during external fault conditions. Figure 5.14 (c) shows the maximum and minimum sums from the MSD protection algorithm shown in Figure 5.12. It is evident that the 'maxSum' trace never breaches the '$-TRH$' boundary and the 'minSum' trace never exceeds the '$+TRH$' boundary. Accordingly, the MSD protection method will avoid a false-trip for external fault conditions.

For an internal fault condition, the current response from each channel is shown in Figure 5.15 (a). Using a conventional high-speed differential protection method, the protection relay will detect the fault as fast as 5 µs as shown in Figure 5.15 (b). How-

Table 5.4: Latencies of each channel and array size selection.

Channel Number (I_i)	Min Latency	Ave Latency	Max Latency	Array Size Selection (N_S) for the Channel
I_0	0	0	0	9
I_1	30 µs	35 µs	40 µs	1
I_2	20 µs	25 µs	30 µs	5
I_3	10 µs	15 µs	20 µs	7

ever, using the MSD method, the fault can effectively be detected but with a reduced speed of 40 μs as indicated in Figure 5.15 (c). Though the fault detection time using the MSD method is 35 μs longer than the conventional high-speed differential method, it can address the instability issue and be effective in ensuring sensitivity to internal faults, compared to the method of widening the fault detection time-window.

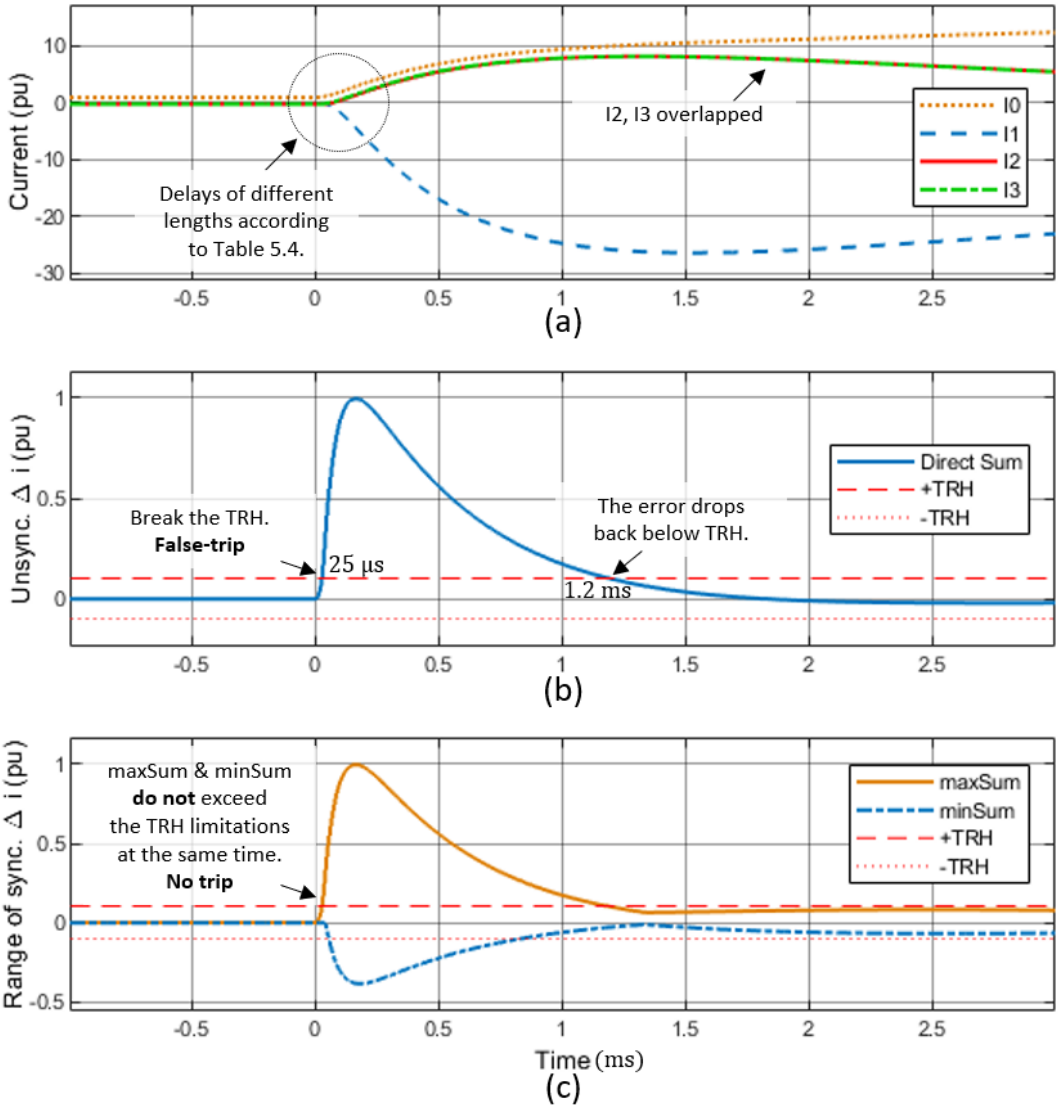

Figure 5.14: Simulation results for an external fault condition with (a) current response of all measurement channels, (b) direct sum of unsynchronised currents using conventional method, (c) maximum and minimum sum using MSD method.

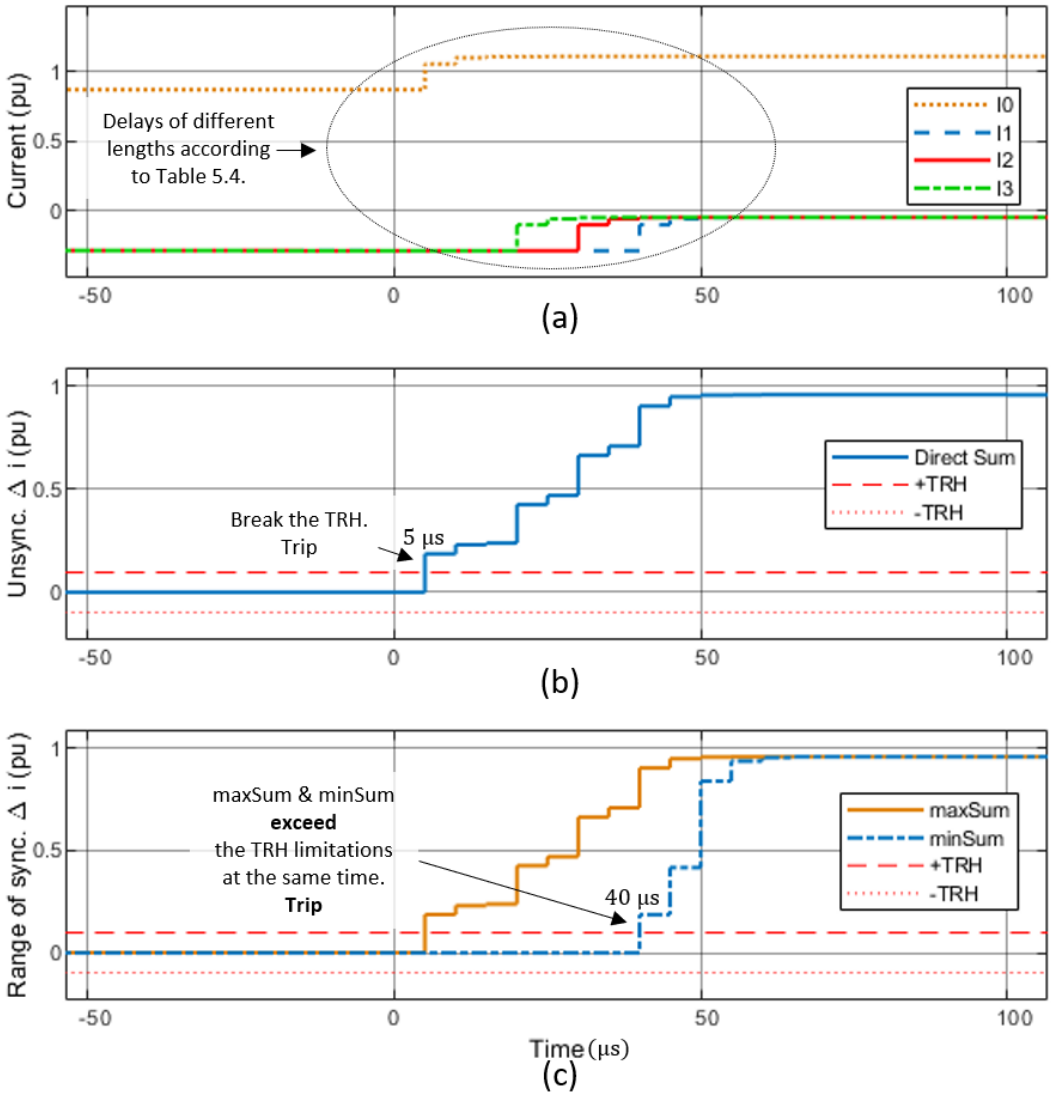

Figure 5.15: Simulation results for an internal fault condition with (a) current response of all measurement channels, (b) direct sum of unsynchronised currents using conventional method, (c) maximum and minimum sum using MSD method.

5.3.2 Discussion

The MSD method offers significantly better protection sensitivity compared with the other methods mentioned in Section 5.1.2. Using a wider decision-making time-window to address the protection instability issue, a window longer than 1.2 ms must be selected to avoid a false-trip under the external fault condition, as shown in Figure 5.14 (b). However, this will result in an equivalent time delay in detecting an internal fault.

Using the MSD method, the relay will remain stable during the external condition, and reacts as fast as 40 μs in detecting the internal fault, as shown in Figure 5.15 (c).

Comparing with the method that increases the trip threshold, it must be selected as high as 1.2 times of the load current to avoid the false-trip in Figure 5.14 (b). However, during the low-resistance internal fault condition, this will cause a delay in detection and a higher fault current for the breaker to trip. This may require a higher breaker rating and lead to greater damage caused at the location of the fault. Additionally, the MSD method does not require a high threshold setting to deal with the TSE, but only needs a very low threshold to deal with EM noise, cable capacitance, and ADC rounding error.

5.4 Experimental Validation

5.4.1 Experimental Setup

To further verify the effectiveness of the proposed MSD method, an experiment was conducted on a low-voltage electrical DC network test-bench shown in Figure 5.16. A corresponding schematic diagram is illustrated in Figure 5.17. This system consists of three DC feeders using inductors to represent distribution lines, and is equipped with voltage and current measurements, and solid-state protection switches devices at each feeder terminal. Short-circuit faults may be applied at each feeder or on the interconnecting busbar.

The experimental methodology is presented in Table 5.5, whereby faults applied to Branch A and Bus BB will be investigated respectively to represent two-terminal and three-terminal zones. In each case, internal and external faults are applied to observe the behavior of both protection methods. For each test, a capacitor located at Bus A representative of the filter of a PEC (charged to 20 V) is discharged through the fault. A short-circuit fault is applied at the corresponding network positions in Table

5.5. The energy stored in the capacitor will consequently release fault current through the shorted path, which can be measured using Hall-effect current sensors. The current measurement signals are conditioned to provide different latencies to evaluate both methods. The trip signals from both methods are digital outputs and are observed using an oscilloscope. The oscilloscope also measures the capacitor voltage and in-feeding current at Bus A without any delay.

To implement virtual communication delays and differential protection algorithms, two separate FPGA-based controllers are employed. The current measurement signals at the boundaries of protection zone are sent to FPGA controller 1, which is programmed to generate identical delayed signals as outputs. These delayed signals are wired to FPGA controller 2, which is programmed with the multi-sample and conventional high-speed differential protection methods running concurrently. Both trip signals are output for observation, but only one is selected to actuate the corresponding operation switches shown in Table 5.5. Details of experimental hardware are listed in Table 5.6.

5.4.2 Hardware Implementation of Signal Delay

The delay function in FPGA controller 1 is implemented using the circular buffer as shown in Figure 5.18, where the latest samples are written successively whilst the output sample reads the register behind with a fixed delay interval representing each channel delay. Latencies of 0, 30, 60 μs are deployed to three measurement channels. As the loop time is set to 10 μs, the delay intervals are set to 0, 3, 6 respectively.

Table 5.5: Methodology of algorithm testing.

Protection Zone	Operation Switches	Fault Type	
		Internal	External
Branch A	A1 & A2	A_F	C_F
Bus BB	A2, B2 & C2	BB_F	C_F

Table 5.6: Details of experimental hardware.

	Function	Hardware	Experiment Test Settings
1	Power supply	Adjustable DC power supply, 0-30 V [140]	Set to 20 V constant voltage
2	Capacitor	Aluminium electrolytic capacitor, 2200 µF, 100 Vdc , EPCOS [141]	Charge to 20 V
3	Disconnect supply prior to fault	Semikron SKM 111AR MOSFET [108]	100 V, 200 A nominal (600 A max)
4	Current measurement	LEM HAS 200-S [100]	measurement ratio: 50 A/V
5	Voltage measurement	LEM LV 25-P [100]	measurement ratio: 5.7 V/V
6	Representative cable inductor	Murata 15222c	2.2 µH ±20%, 4.2 mΩ
7	Representative load	Panel mount fixed resistor	6.6 Ω
8	FPGA controller 1	NI cRio-9014 [111]	Loop time = 10 µs
9	FPGA controller 2	NI cRio-9024 [111]	Loop time = 15 µs
10	Analogue input	NI 9223 [111]	Loop time corresponding to FPGA target
11	Analogue output	NI 9269 [111]	
12	Digital I/O	NI 9401 [111]	
13	Signal capture	Tektronix OSC MSO 2004B	1 GS/s/channel

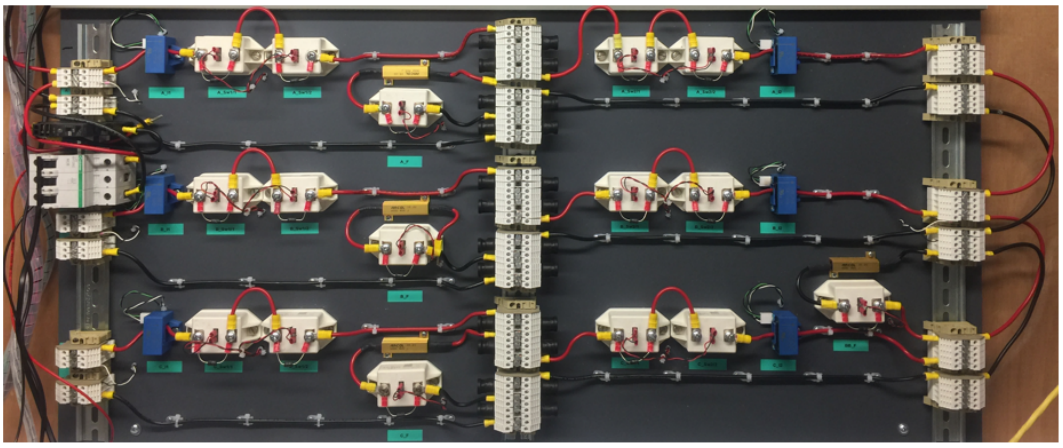

Figure 5.16: Illustration of hardware for algorithm testing.

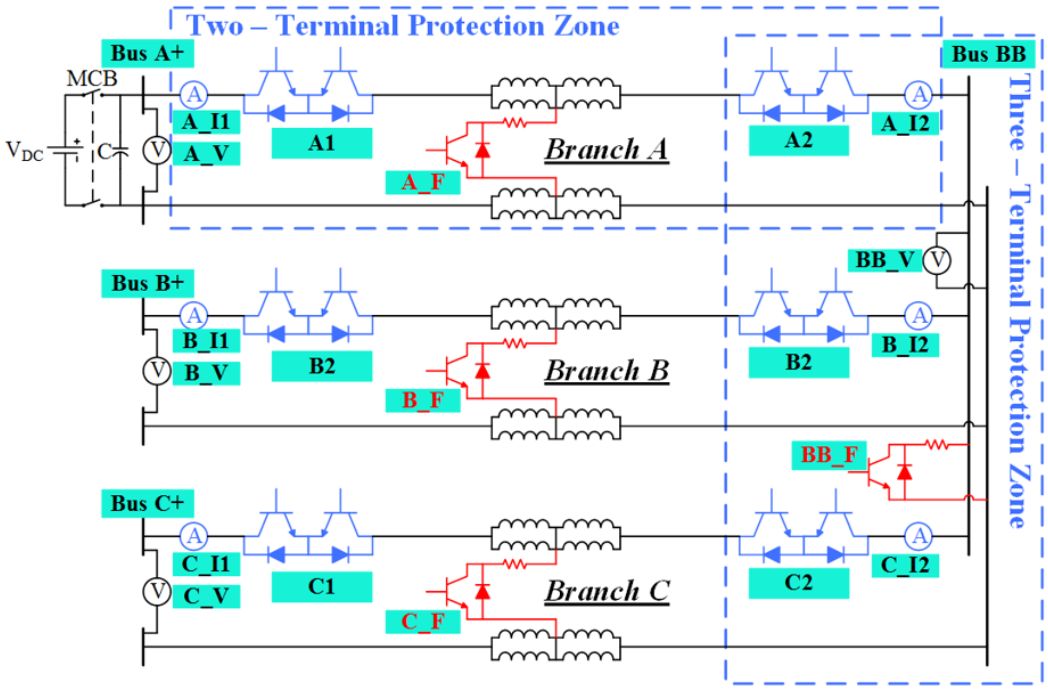

Figure 5.17: Primary electrical layout of DC network.

However, due to hardware limitations, the output signals may not deliver perfectly precise latencies. Accordingly, a testing experiment was conducted to inspect processing latency errors. A signal generator is used to provide a saw-tooth waveform that is sampled synchronously by three ADCs. As shown in Figure 5.19, the processing delay results in an additional 10 to 20 μs delay greater than the assigned latencies, which

Figure 5.18: Circular buffer implementation for delay line.

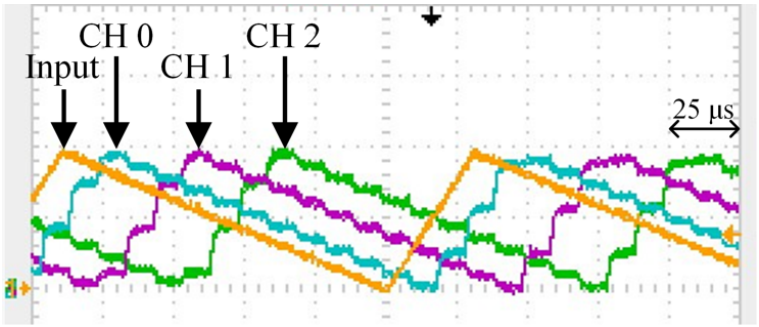

Figure 5.19: Waveform of delayed signals.

Table 5.7: Latency of each channel.

	Latency produced by FPGA 1	Resulted latency in FPGA 2 (number of samples)	N_S setting (two-term. case)	N_S setting (three-term. case)
Local (Channel 0)	10-20 µs	0-2 samples	5	7
Remote1 (Channel 1)	40-50 µs	2-4 samples	1	3
Remote2 (Channel 2)	70-80 µs	4-6 samples	N/A	1

must also be considered while assigning the parameters of the MSD protection method. The three measurement channels are allocated as local, remote 1 and remote 2 channels with total latencies displayed in Table 5.7.

5.4.3 Hardware Implementation of Protection Algorithms

Two independent loops are programmed in FPGA controller 2 to compare the performance of conventional differential protection and the proposed MSD protection method. Since the loop time of FPGA controller 2 is 15 µs, the delayed signals from FPGA controller 1 can be represented in terms of number of samples as indicated in Table 5.7. These ranges can be used to calculate the N_S setting (the number of samples stored in the array of each channel) according to Equation 5.8. Table 5.7 also shows the derived N_S settings for both two-terminal and three-terminal cases. As the latency ranges

have no overlap, the N_S setting of the FLC can be assigned to one. Note that the non-optimised N_S setting for the FLC would normally be 3.

Two-Terminal Structure

The results of two-terminal radial protection are shown in Figure 5.20. It is clear from Figure 5.20 (a) and Figure 5.20 (b) that both methods react quickly to the internal

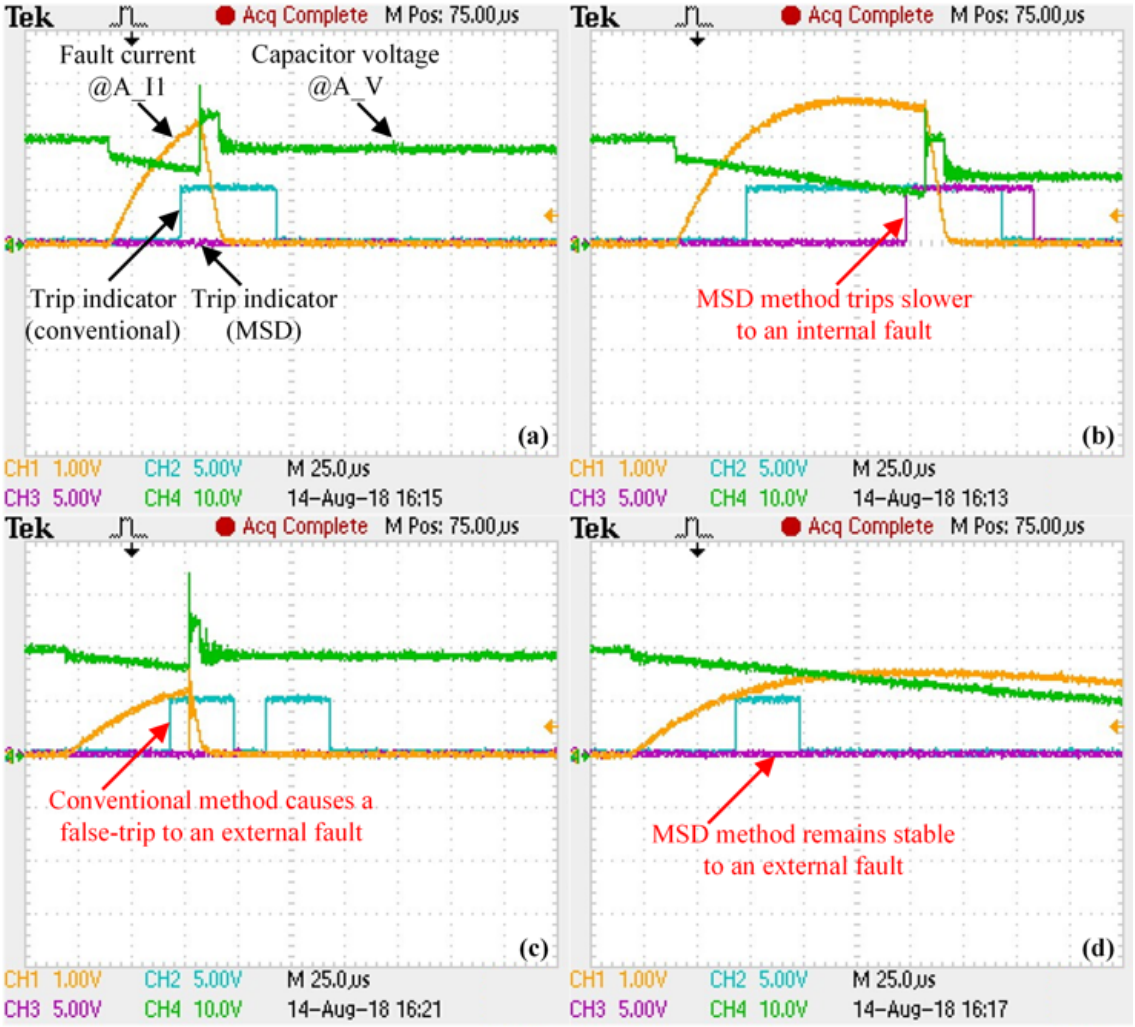

Figure 5.20: Experimental results of two-terminal differential protection with (a) internal fault using conventional method, (b) internal fault using MSD method, (c) external fault using conventional method, (d) external fault using MSD method.

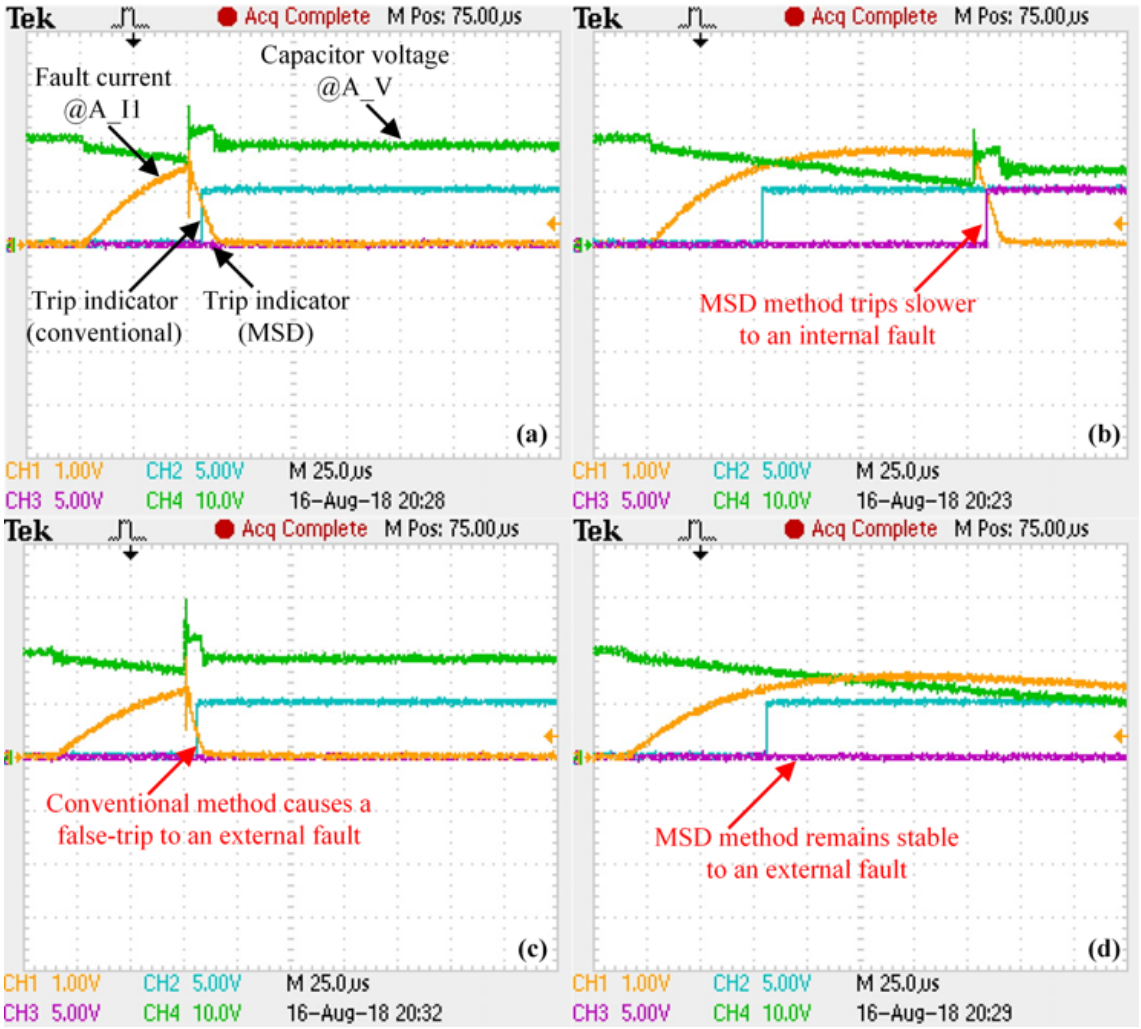

Figure 5.21: Experimental results of three-terminal differential protection with (a) internal fault using conventional method, (b) internal fault using MSD method, (c) external fault using conventional method, (d) external fault using MSD method.

fault. The conventional differential protection method reacts in 35 µs, and the MSD protection method reacts in 110 µs. However, for external fault conditions, as shown in Figure 5.20 (c) and Figure 5.20 (d), the conventional method causes a false-trip whilst the MSD method remains stable to the external fault.

Three-Terminal Structure

Similarly, the results of three-terminal teed protection are shown in Figure 5.21. Figure 5.21 (a) and Figure 5.21 (b) show that both methods react quickly to the internal

fault. The conventional differential protection method reacts in 50 μs, while the MSD protection method is slightly slower at 160 μs. However, similar to the two-terminal radial case, for the external fault condition, the conventional method causes a false-trip whilst the MSD method remains stable as shown in Figure 5.21 (c) and Figure 5.21 (d).

From the results of both cases, the MSD method provides better protection stability than using conventional differential protection. Although the trip-time for internal fault conditions is increased, sensitivity to internal faults remains sufficient with detection speeds within the sub-millisecond range.

5.5 Summary of Chapter 5

This chapter has presented the proposed a Multi-Sample Differential (MSD) protection method to address the instability issue caused by the time synchronisation error (TSE) of high-speed differential protection schemes in DC distribution networks. It was shown that even a microsecond-level TSE will result in a false-trip for external fault conditions. Furthermore, the current difference error caused by TSE may remain high for a long period, which signifies that widening the decision-making time-window may not address the resultant false-trip scenario. The proposed MSD method realises reliable stability for external fault conditions when considering latency ranges from multiple measurement channels.

By analysing multiple sampling points, only if the information indicates that the over-threshold current difference is not caused by TSE in the case of an external fault, the MSD protection relay will output a trip signal immediately. Therefore, the MSD method will not have a serious negative impact on the protection sensitivity when an internal fault occurs (i.e. the protection should operate). Additionally, considering the aspect of practical implementation, this chapter has also optimised the computational overhead. Accordingly, the logic of the MSD method can be simply realised by a digital circuit, which will not cause a significant manufacturing cost. Using FPGA

programming, the tool of converting logic into a digital circuit, an experiment has been conducted to demonstrate that a 25 μs TSE will cause a mal-operation using conventional high-speed differential protection. However, using MSD method can avoid the false-trip problem, and ensure the protection sensitivity when an internal-zone fault occurs.

Chapter 6

Proposed Approaches of Optimising Rate-of-Change Measurement for LVDC Network Protection Applications

In Section 3.3, several high-speed distance protection strategies for DC microgrids were reviewed. Distance protection commonly requires accurate measurement of the dynamic rate-of-change of current ($\mathrm{d}i/\mathrm{d}t$) to compute the fault inductance and estimate the fault distance [118, 119, 142, 143]. However, according to the brief analysis in Section 3.4, the measurement of $\mathrm{d}i/\mathrm{d}t$ may be very sensitive to the impact of current noise, where even a very small noise may cause intolerable errors. This issue may cause difficulty in realising reliable distance protection schemes. Accordingly, computationally deriving $\mathrm{d}i/\mathrm{d}t$ using non-ideal and noisy current measurement signals is a practical challenge that needs to be addressed prior to implementing such protection functions.

This chapter will firstly demonstrate the severe influence of small error on the $\mathrm{d}i/\mathrm{d}t$ measurement in terms of a case study, then propose two approaches of restraining the effect of noise and achieving effective $\mathrm{d}i/\mathrm{d}t$ measurement.

6.1 Numerical Computation for Obtaining Rate of Change of Current ($\mathrm{d}i/\mathrm{d}t$)

In order to obtain a typical fault current response, this case study takes the equivalent DC network in [115] as an example, where the circuit configuration is the same as Figure 3.1 in this thesis and the corresponding network parameters are shown in Table 6.1. According to the conclusion drawn in Section 4.5, that the converter can be represented as an equivalent capacitor for investigating the current response of a DC fault, an equivalent simulation model can be built in Figure 6.1 to generate an ideal fault current profile.

To understand the noise in the actual environment, the current and voltage responses of an RLC discharge was obtained from an initial experiment in the lab. From the results shown in Figure 6.2, the noise in the actual environment is high enough that can be visually observed. Similarly, in this case study, in order to investigate the effect of very small noise, the noise level is assumed to be set at the level just observable.

Using the simulation model in Figure 6.1, a short-circuit fault is applied after 0.25 ms of simulation time at an equivalent distance of 35 m from the filter capacitor. The resultant fault current waveform is plotted in Figure 6.3. Meanwhile, Figure 6.3 also

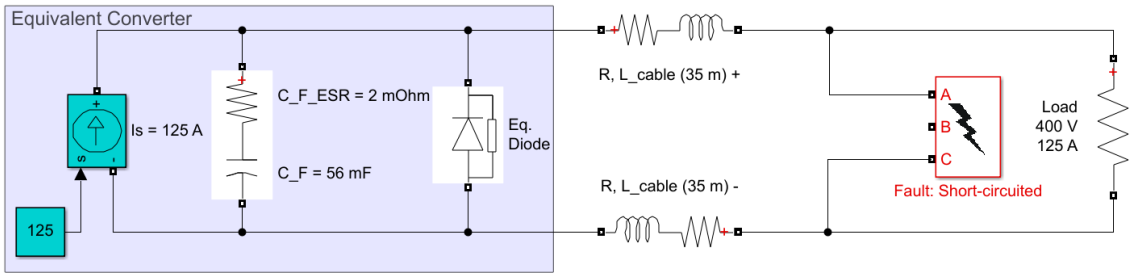

Figure 6.1: The equivalent circuit of a converter with a pole-to-pole fault.

Table 6.1: DC microgrid network parameters.

$v_{C_F}(0)$	$i_L(0)$	R/m	L/m	C_F	$C_{F_{ESR}}$	d_f
400 V	125 A	0.64 mΩ	0.34 μH	56 mF	2 mΩ	35 m

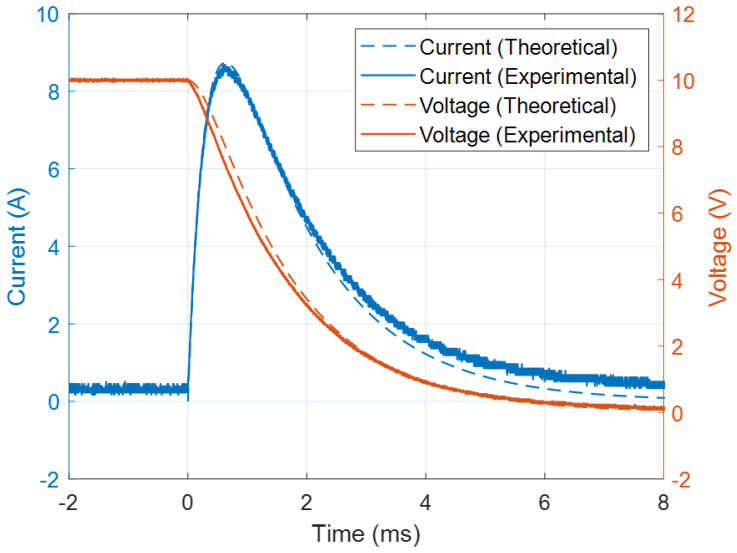

Figure 6.2: An example of measuring current and voltage response signals in practice.

shows the fault current transient with white noise satisfying $X \sim \mathcal{N}(0, 20^2)$ augmented on to the measurement of this transient. As evident from this figure, the noise is observable but does not heavily distort the waveform.

Assuming the current transient waveform of Figure 6.3 is sampled using an analogue to digital converter (ADC), a numerical derivation of $\mathrm{d}i/\mathrm{d}t$ can be obtained, where

$$\frac{\mathrm{d}i(t)}{\mathrm{d}t} = \frac{i(t) - i(t - \Delta T)}{\Delta T}. \tag{6.1}$$

However, this direct numerical method of determining $\mathrm{d}i/\mathrm{d}t$ results in a severely noisy signal that masks the $\mathrm{d}i/\mathrm{d}t$ of the fault current transient. This is evident in Figure 6.4 whereby $\mathrm{d}i/\mathrm{d}t$ of the fault current transient shown in Figure 6.3 is derived for both waveforms (with and without noise) using Equation 6.1 with an assumed ADC sampling frequency of 1 MHz. Given that ΔT is 1 µs, the rate-of-change of the noisy current waveform amplifies the existence of noise. This poor result of $\mathrm{d}i/\mathrm{d}t$ measurement is unlikely to lead to an effective distance protection operation.

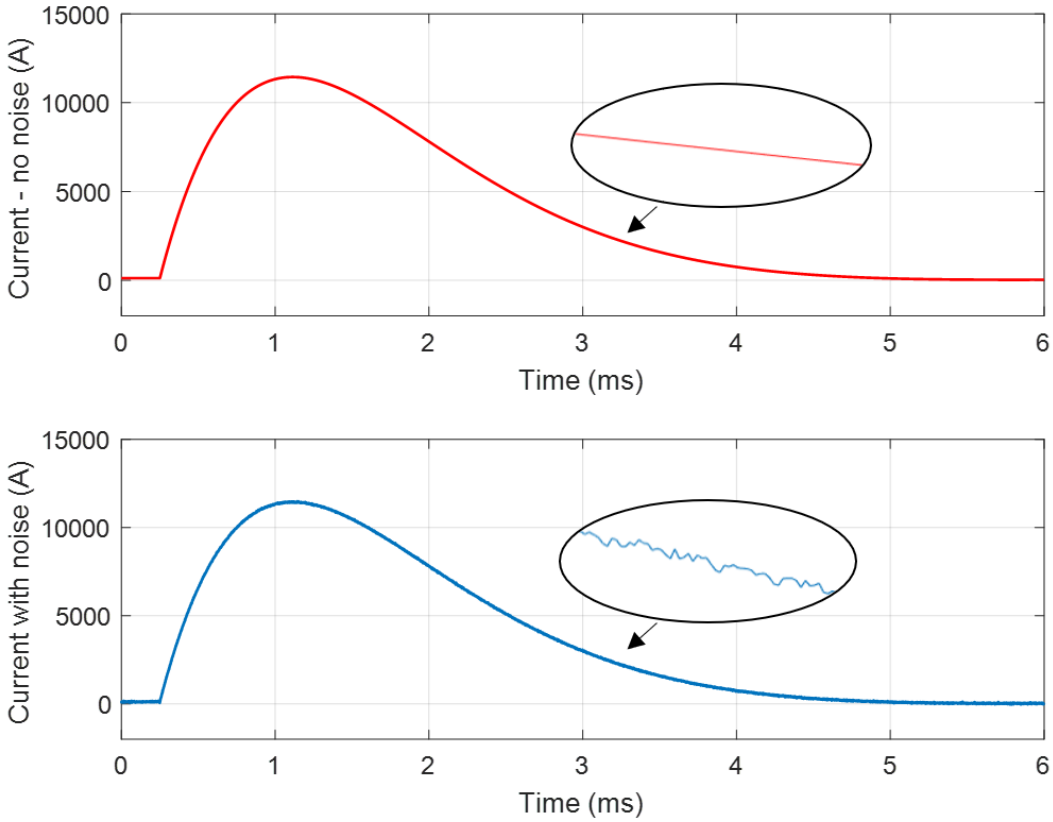

Figure 6.3: Fault current response with injected noise.

6.2 Optimised Method of di/dt Measurement

In order to resolve the challenge associated with obtaining an accurate di/dt measurement using noisy current data, this section will propose two approaches and uses the example shown in Figure 6.3 to validate the effectiveness of improvement. In addition, it may be necessary to apply both approaches to improve the di/dt measurement where there exists high noise in the current measurement signal. At the end of this section, an example will be given where very high noise is injected into the current measurement signal, and the consequence of using both approaches will be presented.

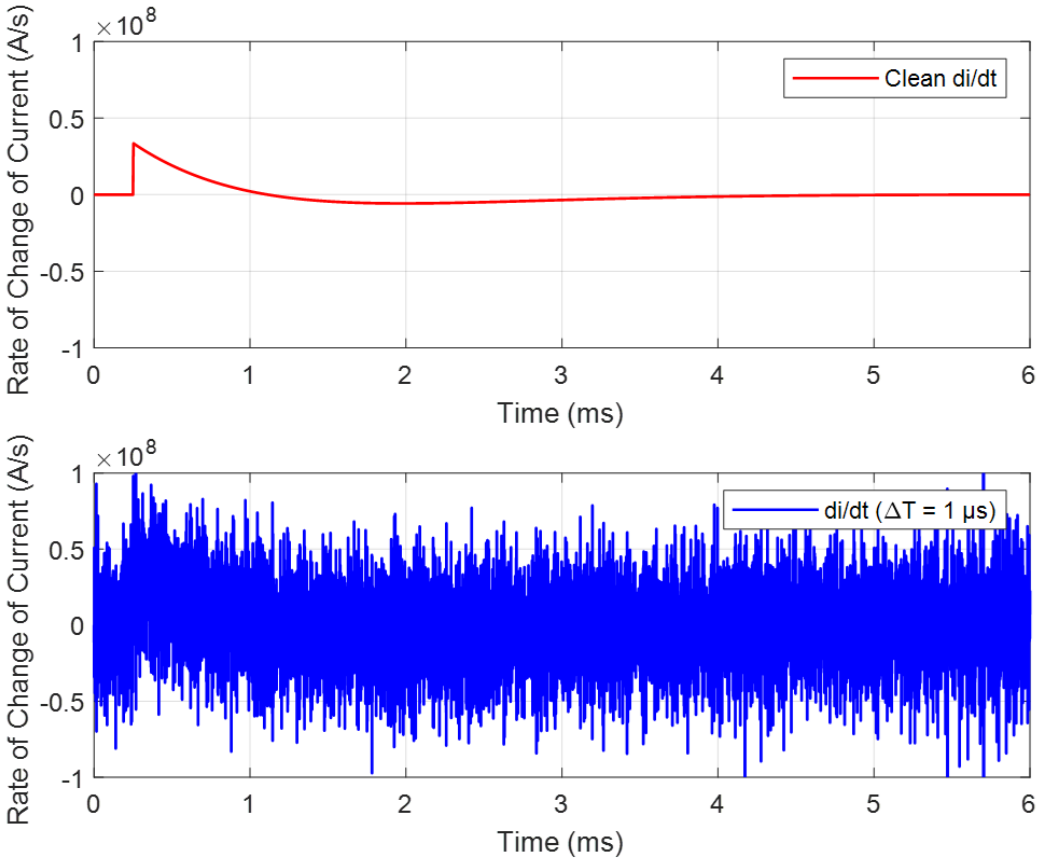

Figure 6.4: A failure of $\mathrm{d}i/\mathrm{d}t$ computation with injected noise.

6.2.1 Optimised Sampling Frequency (OSF) Selection

High-speed distance protection often requires high fidelity $\mathrm{d}i/\mathrm{d}t$ measurement results, so the step time (ΔT) is expected to be a very small value. However, in terms of Equation 6.1, as there is an error in the current measurement (the numerator), too small time step size (the denominator) may enlarge the effect of this error. Accordingly, the first approach aims to constrain the effect of noise by selecting the optimal time step of numerical computation. If the computational time step is defined as M times the sampling period ΔT, the computation equation can be represented as

$$\frac{\mathrm{d}i_n}{\mathrm{d}t} = \frac{i[n] - i[n-M]}{M\Delta T}. \tag{6.2}$$

To test the sensitivity of this approach $M\Delta T$ was selected to be 20 μs, 100 μs, and

400 μs respectively. As shown in Figure 6.5, the $\mathrm{d}i/\mathrm{d}t$ computation result suppresses the effect of noise as a function of the increasing time steps. However, it is evident that larger time steps decrease the accuracy of the initial $\mathrm{d}i/\mathrm{d}t$ computation both in terms of attenuating the peak value and delaying the peak time of $\mathrm{d}i/\mathrm{d}t$ computation, which may be a significant reference for distance protection operation. Therefore, it is important to find the minimum value of $M\Delta T$ so that the $\mathrm{d}i/\mathrm{d}t$ error can be restrained within a suitable range.

Assuming a white noise distribution of $X[n] \sim \mathcal{N}(0, \sigma^2)$, the time step may be selected so that the worst error of $\mathrm{d}i/\mathrm{d}t$ computation of two successive samples is constrained within $\pm\varepsilon$ with a probability of 98%. Since the two successive samples are independent, the difference satisfies $x[n] - x[n-1] \sim \mathcal{N}(0, 2\sigma^2)$. Looking up the Standard Normal Table,

$$P(-2.33\sqrt{2}\sigma < x[n] - x[n-1] < 2.33\sqrt{2}\sigma) = 0.98, \tag{6.3}$$

assuming the limits are set to

$$-\varepsilon < \frac{x[n] - x[n-1]}{M\Delta T} < \varepsilon, \tag{6.4}$$

the 98% confidence error function of the $\mathrm{d}i/\mathrm{d}t$ computation to the time step can be derived, where

$$\varepsilon = \frac{2.33\sqrt{2}\sigma}{M\Delta T}. \tag{6.5}$$

For example, when setting $M\Delta T = 25$ μs, the limitation of 98% $\mathrm{d}i/\mathrm{d}t$ computations on the pure white noise signal is calculated as $\pm\varepsilon = \pm 2.636 \times 10^6$ A/s as shown in Figure 6.6. The result verifies the assumption that 5858 out of 6000 samples (97.63%) are within the designed limits.

Therefore, assuming the noise level (σ) and the required $\mathrm{d}i/\mathrm{d}t$ error limitation ($\pm\varepsilon$) are known, the formula for selecting the step size ($M\Delta T$) to limit 98% samples within

this range can be expressed as

$$M\Delta T = \frac{2.33\sqrt{2}\sigma}{\varepsilon}. \tag{6.6}$$

In this scenario, the actual peak value of $\mathrm{d}i/\mathrm{d}t$ in Figure 6.4 is 3.36×10^7 A/s. This can be derived from the circuit structure using Equation 3.5. Assuming ε is within

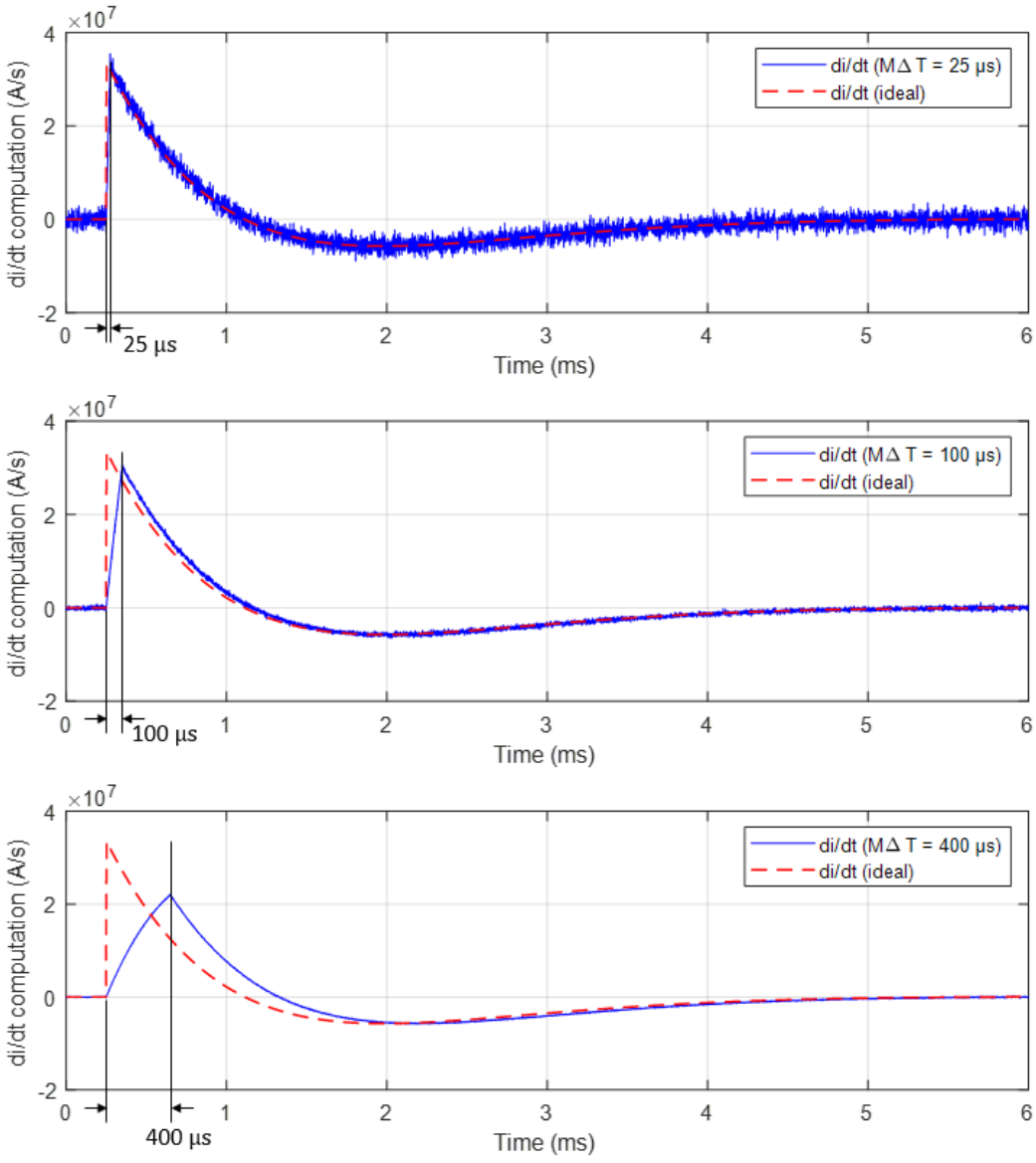

Figure 6.5: $\mathrm{d}i/\mathrm{d}t$ computation results with different sampling frequencies.

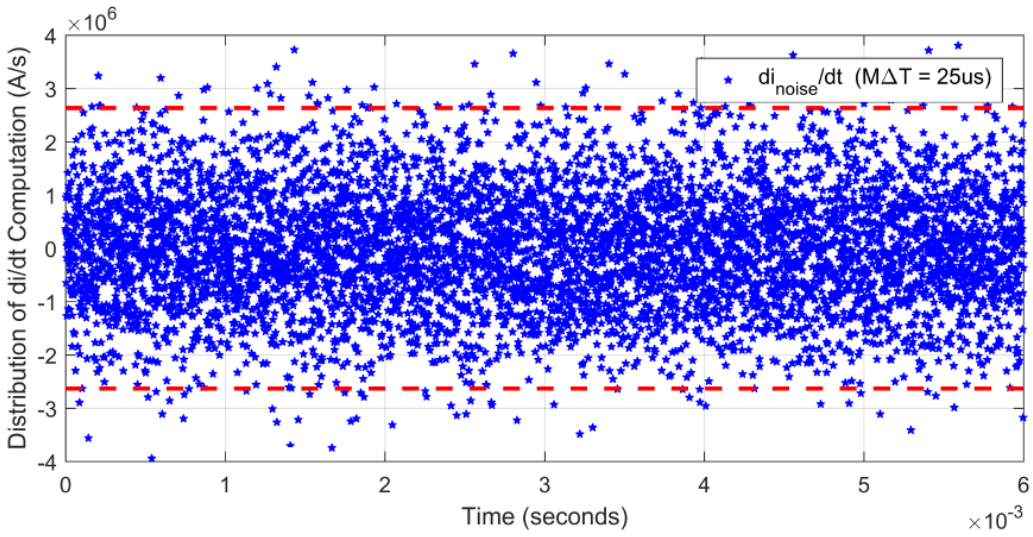

Figure 6.6: di/dt computation errors when $M\Delta t = 25$ µs.

±10% of ideal di/dt signal, i.e. $\pm 3.36 \times 10^6$ A/s, in terms of Equation 6.6, the step size ($M\Delta T$) should be set greater than 19.6 µs.

This method enables careful selection of the time step to realise an effective di/dt computation of a noisy current measurement signal. Furthermore, this method may be easily embedded into hardware such as microcontrollers and FPGAs. The primary drawback associated with this method is that the peak of di/dt may be attenuated and the delay to the peak may decrease the sensitivity of any protection system that utilises di/dt for fault detection. According to Figure 6.5, the delayed peak time is equal to the length of $M\Delta T$, hence as $M\Delta T$ has to be set high due to high noise, the protection operation time may be severely extended. Accordingly, this method may be better suited for processing low-noise current signal.

6.2.2 Finite Impulse Response (FIR) Filter

To deal with the case with higher noise, the second proposed method to facilitate an accurate fault current transient measurement applies the use of an FIR filter prior to di/dt computation. This method is considered as a DC short circuit fault current has

a limited frequency-bandwidth due to network characteristics, and so high-frequency components of noise may be filtered out. Applying a Fourier transform on Equation 3.2 and 3.4, the frequency distribution of overdamped and underdamped fault current signals are commonly derived as

$$I(\omega) \approx \frac{v_{C_F}}{L} \cdot \frac{1}{\omega_d^2 + (\alpha + j\omega)^2}. \tag{6.7}$$

where $\alpha = \frac{R}{2L}$; $\omega_0 = \frac{1}{\sqrt{LC}}$; $\omega_d = \sqrt{\omega_0^2 - \alpha^2}$ that includes an imaginary part during the overdamped conditions. Applying the cable inductance and filter capacitance parameters in Table 6.1, the frequency-domain fault current response can be plotted. In this case, $L = 0.34 \times 35 = 11.9$ μH; $C = 56$ mF. Assuming the fault resistances are 1, 24, 100 mΩ, the frequency-domain responses can be sketched as shown in Figure 6.7. Whether the fault causes an overdamped or underdamped transient, the main frequency content is within the range of 10 Hz to 2 kHz, and the natural frequency (f_0) of the RLC circuit can be calculated by

$$f_0 = \frac{1}{2\pi\sqrt{LC_F}}, \tag{6.8}$$

that is 195 Hz in this case.

While designing a low-pass filter, the cut-off frequency (f_C) should be selected to avoid the distortion of the original fault current signal but suppressing the high-frequency noise. Therefore, the principle of selecting the FIR filter is that the cut-off frequency (f_C) should be higher than the upper limit of the main frequency (2 kHz) of the fault current signal, and 10 kHz is selected in this case.

Table 6.2 presents the parameters of three low-pass FIR filters as examples and the corresponding frequency response plots as shown in Figure 6.8. The signals in Figure 6.3 are preprocessed by these three filters respectively, and then the numerical derivative will be carried out with the same time step (1 μs) using Equation 6.1. As a consequence, Figure 6.9, 6.10 and 6.11 show the performances of using these three

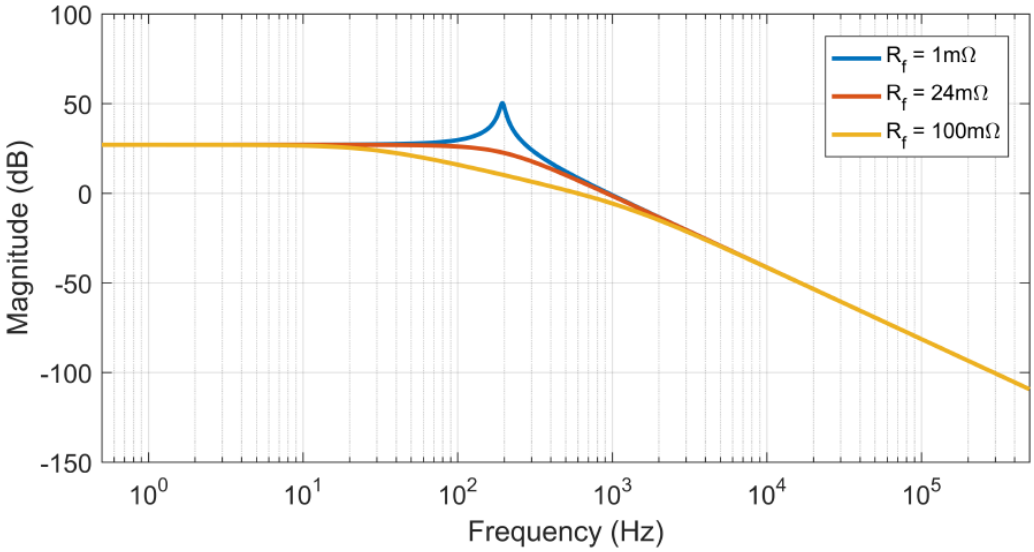

Figure 6.7: Spectrum of short-circuit faults with different fault resistances.

low-pass FIR filters, where the same computational time step ($M\Delta T$) is applied. The results with the same $M\Delta T$ indicate that the di/dt measurement result using the lowest cut-off frequency (10/110 kHz) shows the smoothest feature. The advantage of using FIR is that the peak value of di/dt is not suppressed where the same computational time step ($M\Delta T$) is applied, and the delay time is short. The number of delayed samples caused by FIR filter is equal to half of the designated N_{order}, that is $24/2 \times 1$ µs = 12 µs in this case. However, since the cut-off frequency is limited in the sense that this cannot be set lower than the main frequency of the fault current, it is difficult to achieve a smooth di/dt result if using an FIR filter only. If there is high noise in the signal, two approaches may be combined together to suppress the interference of noise.

Table 6.2: Parameters of filter design.

Type	$f_{sampling}$	f_{pass}	f_{stop}	N_{order}
FIR	1 MHz	300 kHz	400 kHz	24
FIR	1 MHz	100 kHz	200 kHz	24
FIR	1 MHz	10 kHz	110 kHz	24

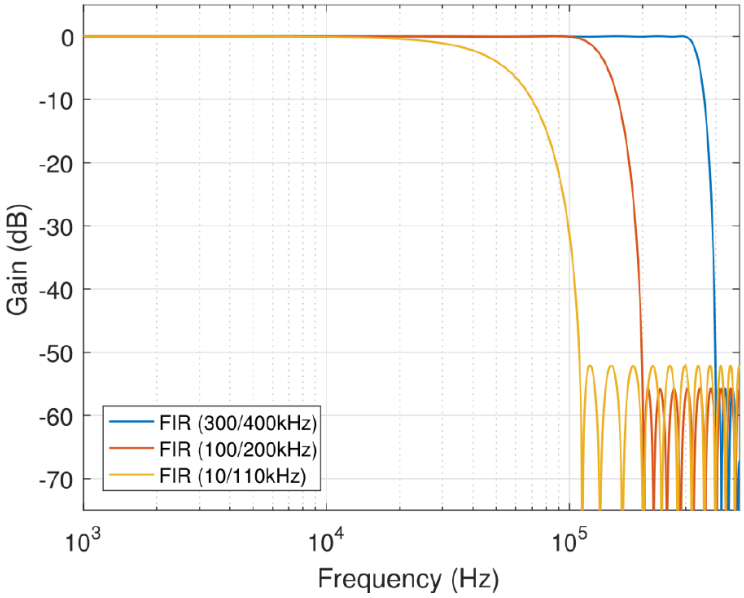

Figure 6.8: Frequency responses of FIR low-pass filters.

6.2.3 Evaluation of di/dt Result by Combining Both Approaches

According to Figure 6.5 and Figure 6.9, both approaches are capable of effectively depressing the errors in di/dt computation. The first method optimises the computing step time in terms of the variance of the noise signal so that the di/dt computation error can be limited within a specific range. The second method applies a low-pass FIR filter with a designed cut-off frequency to remove high-frequency noise content from the current signal to improve the quality of the di/dt computation. The first method is simpler in design and can quantify the error level, but excessive requirements may attenuate the peak di/dt signal and decrease the accuracy of when the maximum di/dt occurs. Accordingly, it is more suitable for coping with low-power noise. The second method employs an FIR filter that cannot quantify the error level, but does not decrease or severely delay the di/dt peak. This method is therefore feasible for processing current transient signals with high-power noise. Taking the advantages of both methods, better performance can be obtained by combining them together. For example, since the signal-noise-ratio (SNR) may be as low as that shown in Figure 6.12 (a) whose $\sigma \sim 500$. In practical applications, when a sensor is required to have a large measurement range,

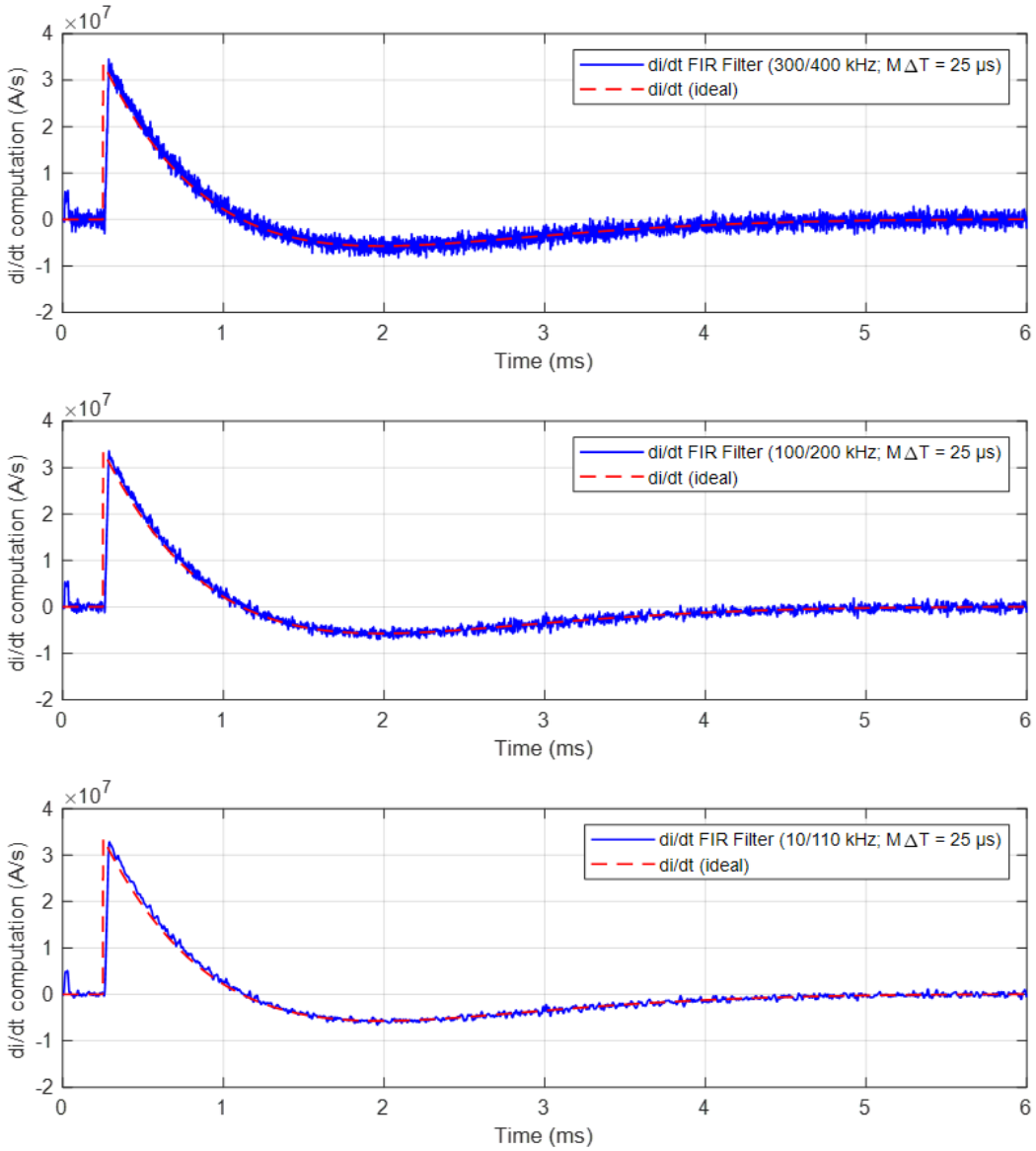

Figure 6.9: Result of $\mathrm{d}i/\mathrm{d}t$ computations with low-pass FIR filters ($M\Delta T = 25\ \mu s$).

the noise level will be very high because of the high transducer burden resistance. Although a very high noise level may lead to inaccurate measurement of normal current, the sensor can measure extremely high current for calculating $\mathrm{d}i/\mathrm{d}t$ without saturation during fault conditions. However, in this case, neither of the methods used in isolation may be effective to restrain the impact of noise. A lowpass filter may be applied first to constrain the high-frequency noise, as shown in Figure 6.12 (b). Then, the optimal

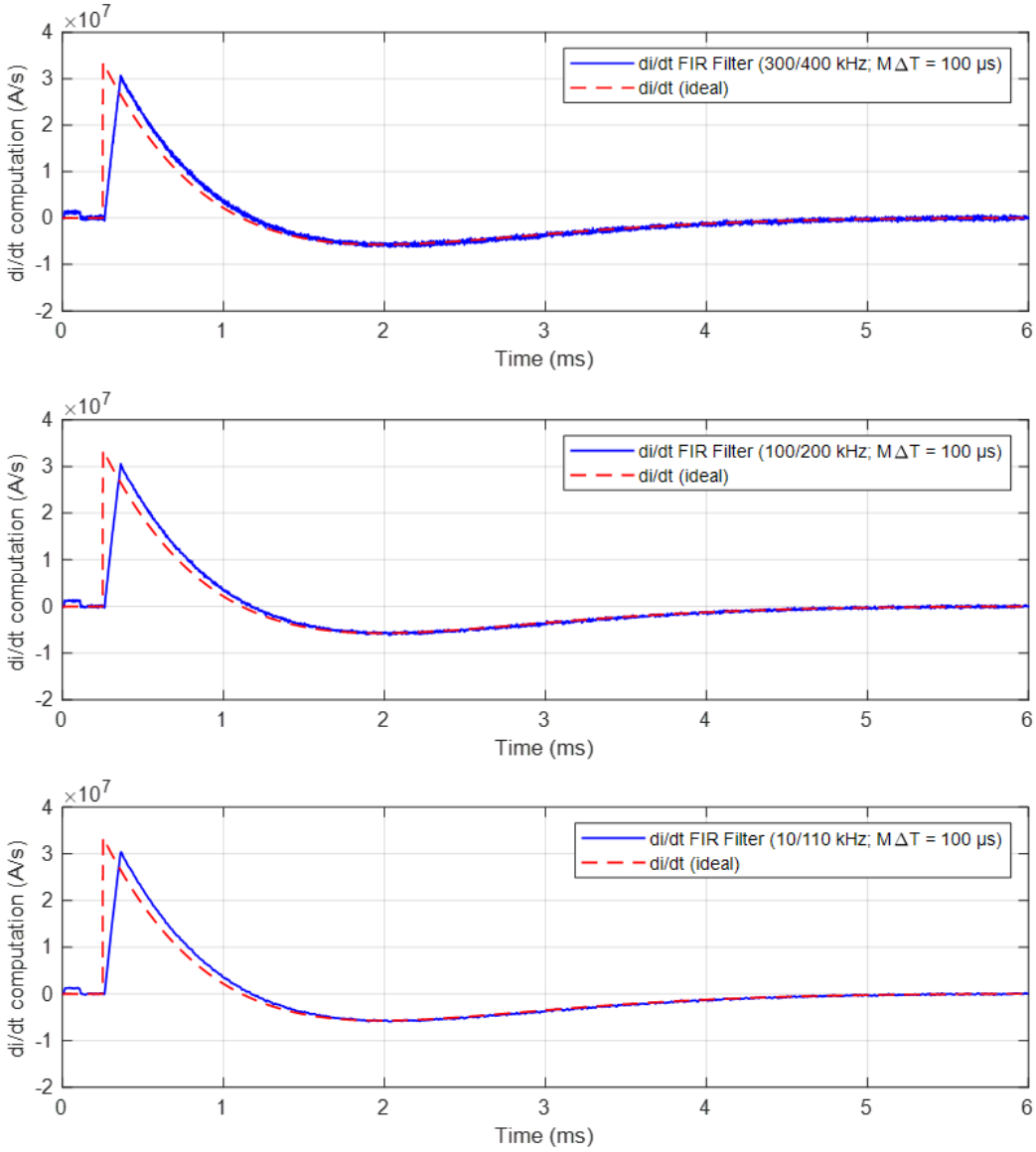

Figure 6.10: Result of $\mathrm{d}i/\mathrm{d}t$ computations with low-pass FIR filters ($M\Delta T = 100\ \mu s$).

selection of the computational time step may be applied. According to Equation 6.6, the computational time step should have been selected as 625 μs. However, such a long time step may cause a significantly delayed and attenuated $\mathrm{d}i/\mathrm{d}t$ peak point. Assuming the maximum acceptable delay time is 50 μs, $M\Delta T$ can be selected as 50 μs. Figure 6.12 (c) demonstrates the resulting $\mathrm{d}i/\mathrm{d}t$ waveform when applying a combination of these methods. Although the peak time is delayed by 50 μs, the error of the peak point

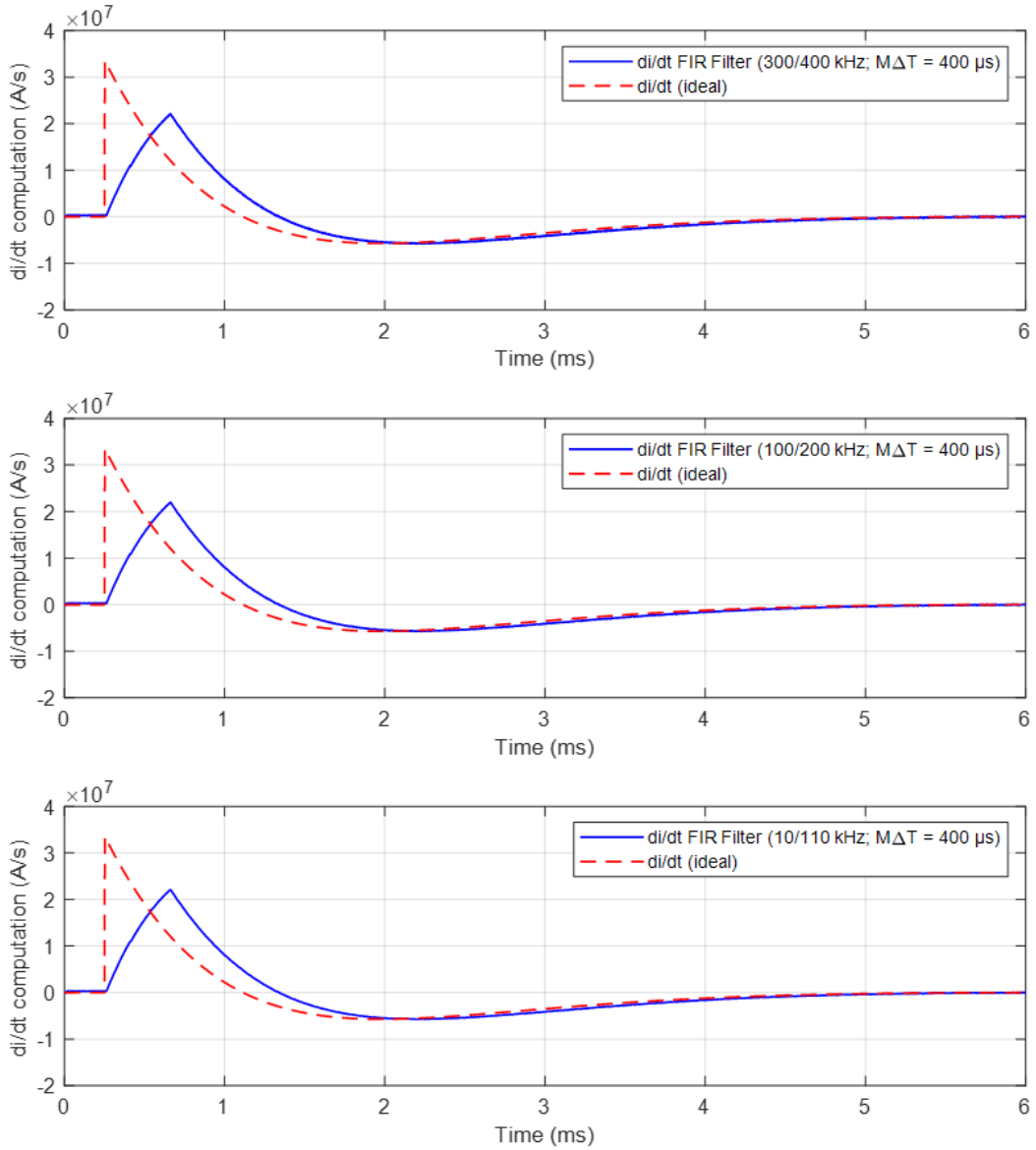

Figure 6.11: Result of di/dt computations with low-pass FIR filters ($M\Delta T = 400$ µs).

is not very high compared to the ideal case. This result is not realisable by using either method individually.

Regardless of the results obtained using the OSF method, the filter method, or the combination of both, the di/dt computation may be suitable to recognise the peak point of di/dt. However, none of these methods results in a di/dt signal produced from

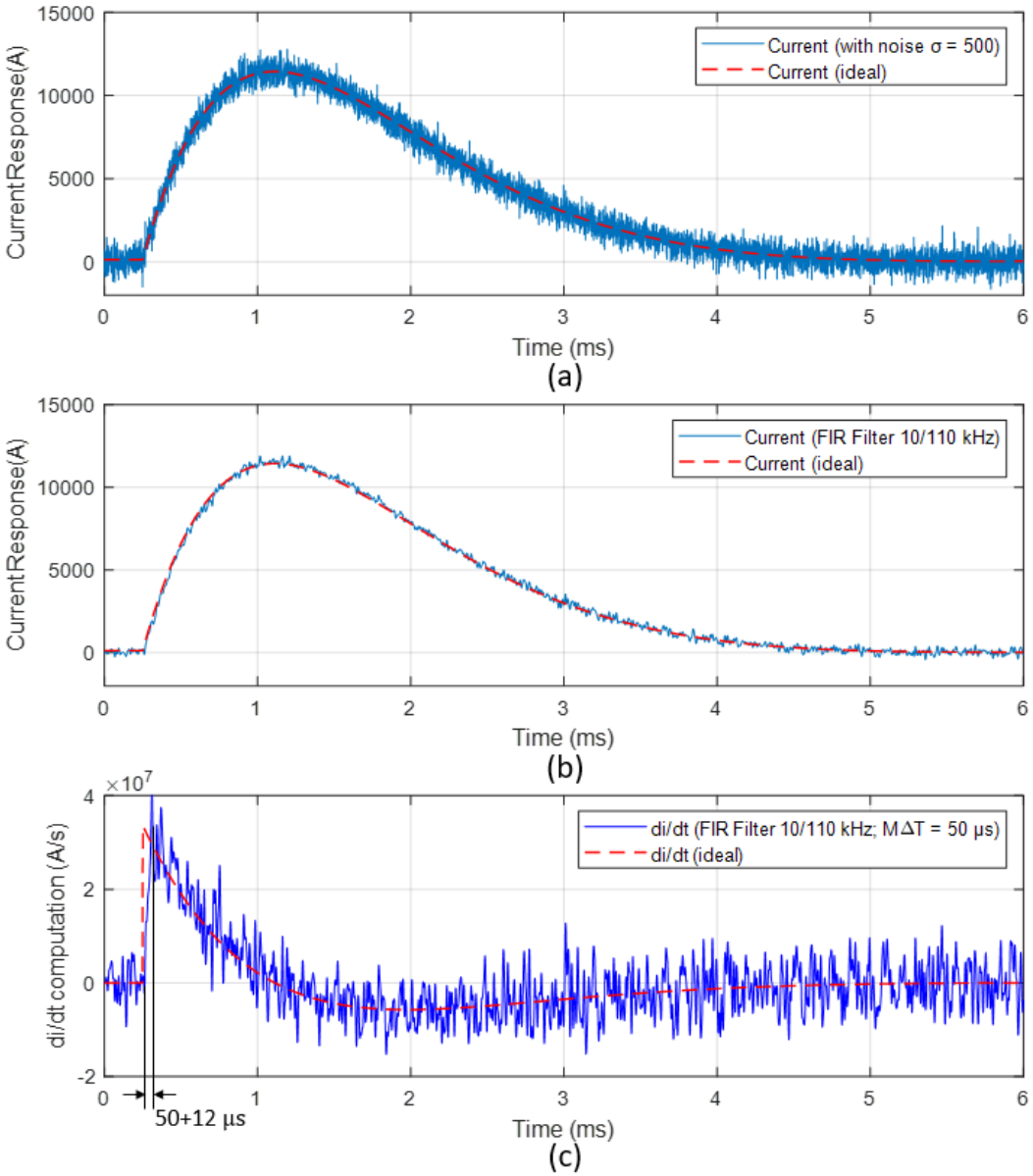

Figure 6.12: di/dt computation for lower SNR signal with combination of the 2 methods: (a) original current signal; (b) current signal after FIR filter; (c) di/dt computation with filter and longer time step.

a current measurement that contains noise that is ideal in nature. Accordingly, DC protection relays that utilise di/dt should be designed to make tripping decisions based on several successive samples rather than one single sample to allow for suppression of noise and error samples.

6.3 Summary of Chapter 6

The accuracy of $\mathrm{d}i/\mathrm{d}t$ measurement is significant as it is commonly used in the DC distance protection method and impacts the effectiveness of the fault distance estimation. However, the measurement of $\mathrm{d}i/\mathrm{d}t$ is very sensitive to even a very small noise. Dealing with this issue, this chapter has proposed two approaches for optimising $\mathrm{d}i/\mathrm{d}t$ computation of short circuit faults within DC networks by optimising the sampling frequency and designing an FIR filter. The selection of the sampling frequency depends on the tolerable error limitation and delayed time, and the selection of the FIR cut-off frequency is in terms of the main frequency of the original fault current. Both approaches were verified through simulation case studies. Additionally, as a high-level noise is including in the measured current signal, both approaches may be applied together to obtain clean and effective $\mathrm{d}i/\mathrm{d}t$ results. The accurate measurement of $\mathrm{d}i/\mathrm{d}t$ has the potential to make a significant contribution to the network protection of DC microgrids through high-speed distance protection schemes.

Chapter 7

Proposed Modulated Low Fault-Energy Protection Scheme for DC Smart Grids

In Sections 3.4 and 3.5, the implementation challenges of high-speed differential and distance protection were analysed, and the corresponding solutions to address these issues were proposed in Chapters 5 and 6. However, it is also clear that realising high-speed fault isolation requires the use of a large number of advanced devices. For the case of HVDC and MVDC applications, these schemes may be feasible as the system rating is relatively high and the system structure is simple. Whilst for LVDC networks, since the structure is normally complex, many relays on different power distribution lines may be required. In this case, employing all high-speed devices in the protection scheme may represent an economically feasible solution.

In order to compromise the requirement of PECs for high-speed protection whilst avoiding the need for widespread high-speed operation hardware, moderate-speed protection schemes have been proposed in the literature. The general principle of these schemes is to employ fault current limiters (FCL) at the terminal of PEC-based power sources to restrain the fault current to a low-level, whilst utilising mechanical circuit

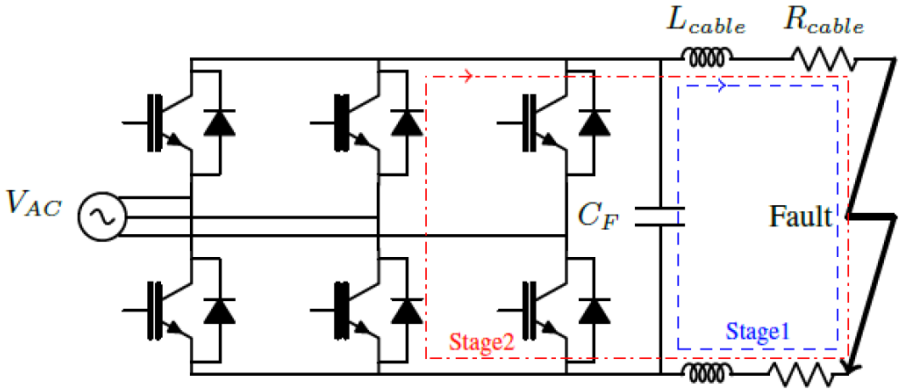

Figure 7.1: Circulation stages of a VSC pole-to-pole fault.

breakers (MCBs) to isolate the faulty line in the distribution network. However, existing schemes have focussed on the operating strategy for the FCL and have not considered the opportunities or communications-free coordination of the MCBs and FCL. As such, a Modulated Low Fault-Energy (MLE) Protection Scheme to realise moderate-speed protection is proposed in this chapter, in which a longer allowed MCB operation time-window is realised to restore the use of time-based overcurrent protection coordination. The MLE protection scheme adopts a similar strategy to the commonly-used IDMT protection scheme [114] that has been widely applied for decades in AC system.

7.1 MLE Protection Concept

The MLE protection scheme is composed of a single upstream SSCB and multiple downstream slower-acting MCBs. The SSCB and MCBs consist of a solid-state fault current controller (SSFCC) and associated MCB-relays respectively. The concept of the MLE protection scheme can be demonstrated on the example network shown in Figure 7.2, and is described further in the following sections.

7.1.1 Protection Algorithm of SSFCC

The SSFCC is installed at the output terminals of the VSC capacitor. This device employs a high-frequency current transducer, a relay processor, and an SSCB. The

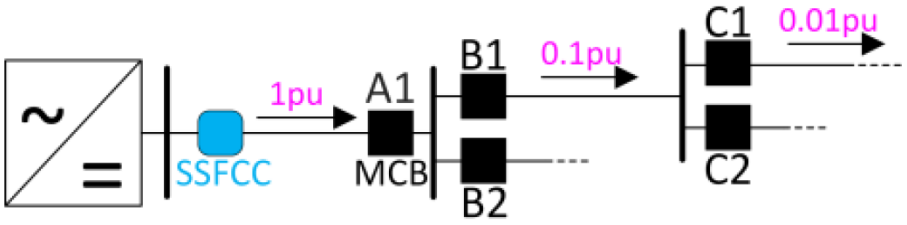

Figure 7.2: Example network.

SSFCC topology consists of two anti-series MOSFET or IGBT/diode-pair devices enabling bidirectional current blocking.

The operating principle of the SSFCC and expected current-limiting behaviour is shown in Figure 7.3. In the no-fault (NF) condition, where the current flow is no greater than the rated current of the network, the SSFCC will remain closed. If a high-resistance fault (HRF) occurs on the network, in which the resulting fault current slightly exceeds the nominal setting (i.e., 1.2 to 4 times of the nominal current flow through the SSFCC in this example), the SSFCC will also remain closed and leaves the downstream MCBs to trip on overcurrent. However, in the event of a low-resistance fault (LRF), where the current is detected to exceed a predefined 'high' threshold setting, the SSFCC will begin to control the fault current let-through by modulating. The duty-cycle of switching is actively controlled to constrain the average current to a predefined safe level that limits damage to components within the fault path. When the instantaneous current settles to non-fault levels, it indicates that one of the downstream MCBs has isolated the faulted section of the network. The SSFCC thereby remains closed to restore steady-state power to the system. However, if the SSFCC keeps modulating for an extended period, it indicates that all the downstream relays have failed to isolate the fault. Under these conditions, the SSFCC shall remain open to de-energise the network from this location as a failsafe coordinated backup. The response time of the SSCB is typically in nanoseconds and the conduction loss is normally negligible. Taking Semikron SKM 111AR MOSFET [108] as an example, the response time is as short as 270 ns, and the typical drain-source resistance of two anti-series MOSFET/diode-pair is 14 mΩ. Accordingly, the short response time and low power

loss will enable the use of the SSCB as a fault current limiter.

Regarding the setting criteria, let V_n and I_n be the nominal voltage and current of the system; $I_{S_{SSCB}}$ is the modulating current threshold of the SSFCC; $I_{control}$ is the target average current let-through for LRF conditions; T_{ON} and T_{OFF} are the on and off times of the SSFCC during each duty-cycle; and T_L is the fail-safe modulating time before hard turn-off. Table 7.1 shows the relay settings of an example MLE configuration.

The nominal voltage (V_n) and current (I_n) are assumed to be unity. The modulating current threshold ($I_{S_{SSCB}}$) must be set to ensure that transient fault currents do not damage downstream cables and components. The converter must, therefore, have sufficient overhead capacity to supply overloaded conditions. The target average current ($I_{control}$) should be set to a safe level, but must be higher than the nominal current, to ensure that the downstream network voltage will recover after the fault is

Table 7.1: Example setting of SSFCC.

V_n	I_n	$I_{S_{SSCB}}$	$I_{control}$	T_L
1	1	$4I_n$	$1.2I_n$	1 sec

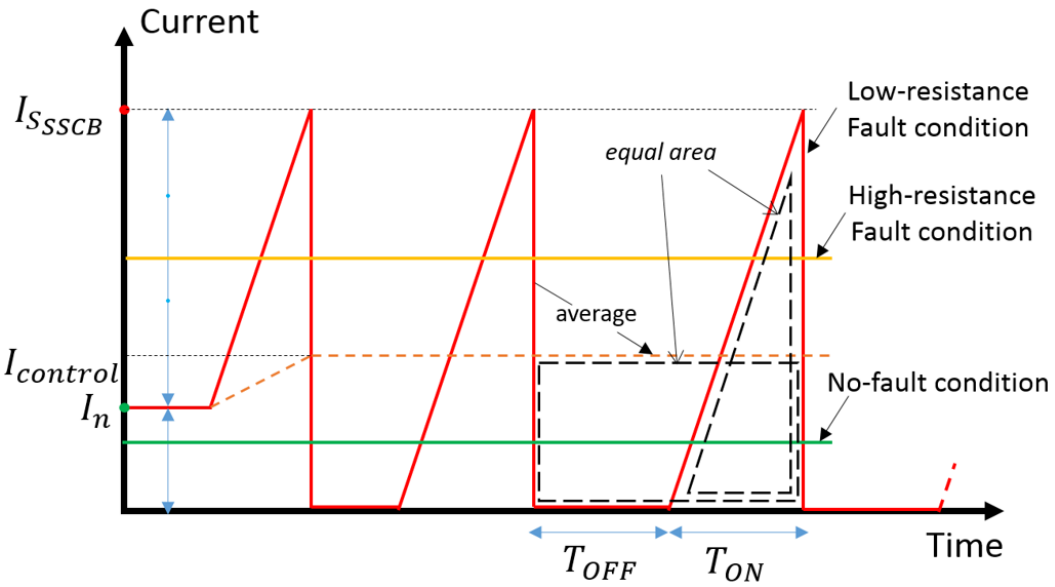

Figure 7.3: Representation of the current profile associated with SSFCC control.

cleared (accounting also for the impact of constant power loads on network voltage restoration). T_L must be set to ensure the downstream MCB-relays and backup devices have sufficient time to discriminate fault locations. Since T_{ON} depends upon the fault-path circuit parameters, which are essentially uncontrollable, the moving average current is controlled by adjusting the off-time of the solid-state switch (T_{OFF}).

The initial discharge current of every cycle can be approximated to a linear increment with a slope of V_n/L_f according to Equation 3.5, where L_f is the inductance of the fault path. Accordingly, the fault current during each on-period may be presented as

$$i(t) \approx \frac{V_n}{L_f} t, \tag{7.1}$$

where $t = 0$ for each re-closing moment of the SSFCC. As the instantaneous current reaches the overcurrent threshold, the SSCB will open and block fault current. Substituting $i(t) = I_{S_{SSCB}}$ in Equation 7.1, the on-period becomes

$$T_{ON} \approx \frac{I_{S_{SSCB}}}{V_n/L_f}. \tag{7.2}$$

The off-period is controlled to limit the average fault current to $I_{control}$. Considering each modulation cycle in Figure 7.3, equating the rectangular area by $I_{control}$ and the triangle area by fault current, such that

$$(T_{ON} + T_{OFF}) \cdot I_{control} \approx \frac{1}{2} I_{S_{SSCB}} T_{ON}, \tag{7.3}$$

the off-period may be calculated as an equation, that is

$$T_{OFF} \approx \frac{1}{2} \left(I_{S_{SSCB}} T_{ON} / I_{control} \right) - T_{ON}. \tag{7.4}$$

Under the low-resistance fault conditions, the SSFCC should modulate with this off-period (T_{OFF}) to achieve the same average fault current of $I_{control}$.

7.1.2 Protection Algorithm of MCB-Relays

For conventional electromechanical and microprocessor-based AC relays, the IDMT characteristics are derived from a formula that complies with BS142 and IEC 60255 standards. It is generally defined as [114]

$$t_{trip} = \frac{K}{\left(\frac{I_f}{PS \cdot I_S}\right)^{\alpha} - 1} \cdot TMS, \tag{7.5}$$

where t_{trip} is the trip-time; TMS is the time multiplier setting; I_f is the RMS-value of AC fault current; I_S is the value of relay current setting; PS is the relay plug setting; α and K are constants.

A DC equivalent version of an IDMT protection scheme can be applied to the downstream MCB-relays within this system. As the SSFCC will limit fault current to a level lower than the trip threshold, $I_{S_{SSCB}}$, the very inverse characteristic curve [114] is selected for such systems, where α is unity. Hence, the MCB-relay trip characteristic becomes

$$t_{trip} = \frac{KTMS}{\frac{\overline{I_f}}{PS \cdot I_{S_{MCB}}} - 1} \tag{7.6}$$

where K and TMS are combined as one setting, $KTMS$; $\overline{I_f}$ is the moving average value of DC fault current; and $I_{S_{MCB}}$ is the overcurrent threshold setting of the MCB. For each MCB-relay, $I_{S_{MCB}}$ is normally set marginally higher than the nominal load current flowing through this branch, e.g., $1.2I_n$, and $KTMS$ and PS are adjustable to realise protection coordination.

Since the fault current will be modulated during an LRF condition, MCB-relays will require a means to compute the moving average current value and execute the protection algorithm. This may be implemented using DSP hardware. Equation 7.6 can be presented in a numerical form, such that

$$inc = \left(\frac{\overline{I_f}}{PS \cdot I_{S_{MCB}}} - 1\right) \cdot \frac{C_T \cdot T_{S_{MCB}}}{KTMS}, \tag{7.7}$$

and

$$t_{trip} = \frac{CT}{inc} \cdot T_{S_{MCB}}, \tag{7.8}$$

where $T_{S_{MCB}}$ is the sampling time of the numerical relay; C_T is the counting threshold; and inc is the incremental value at every sample. The trip-time is affected by the $KTMS$ and PS settings only, and is independent of $T_{S_{MCB}}$ and C_T settings, as evident in equations 7.7 and 7.8.

The $KTMS$ setting enables the grading of trip-times between MCB-relays at different downstream locations, whilst the PS setting enables the coordination of trip-times between LRF and HRF conditions of an individual MCB-relay. Hence, PS is a voltage-controlled setting which is unity in NF and HRF conditions, and equal to a voltage-dependent coefficient, $k_{V_{dep}}$, in LRF conditions. Accordingly, PS may be expressed as

$$PS = \begin{cases} 1, & V_{MCB} \geq 0.8V_n \\ k_{V_{dep}}, & V_{MCB} < 0.8V_n \end{cases} \tag{7.9}$$

where V_{MCB} and V_n are the measured local voltage and nominal local voltage respectively.

Protection strategy for high-resistance or overloading faults

Figure 7.4 shows a schematic of a representative DC system to demonstrate the operation of the MLE protection strategy for high-resistance or overloading faults. At any time, the current flowing through any MCB-relay may be defined as $I(local)$, whilst the sum of the nominal currents of all other branches may be defined as $I_n(other)$. During HRF conditions, such as that shown in Figure 7.4, the current through all upstream MCB-relays will exceed their respective trip thresholds. However, the current through the SSFCC will be insufficient to trigger its modulation action. i.e. $I_{S_{MCB}} < I(local) < I_{S_{SSCB}} - I_n(other)$. Under such conditions, the network will remain at its nominal voltage, and so the voltage-controlled PS setting will remain at

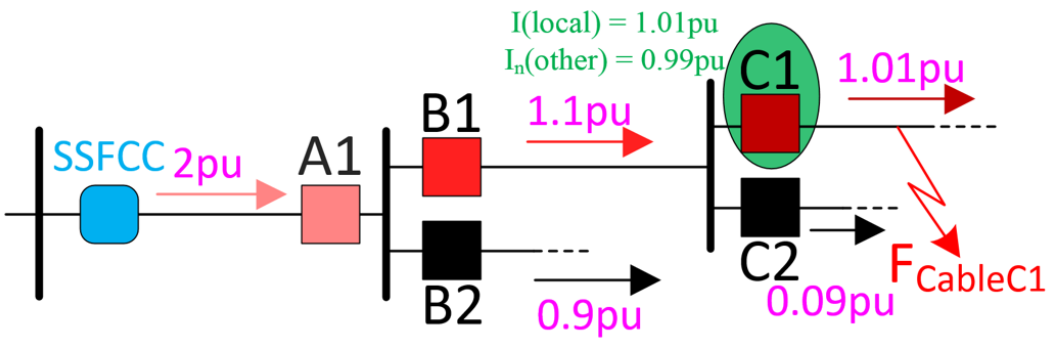

Figure 7.4: Schematic of $I(local)$ and $I_n(other)$ of an MCB-relay.

unity according to Equation 7.9.

Substituting PS in Equation 7.6 with this value and defining $I(local)/I_{S_{MCB}}$ as M_f (which represents the multiple of the local MCB trip threshold), an overcurrent condition can be signified when $M_f > 1$. Rearranging Equation 7.6 and defining $t_{trip}/T_{S_{MCB}}$ as N_{trip}, the trip-time in terms of the number of samples becomes

$$N_{trip} = \frac{KTMS}{T_{S_{MCB}}\,(M_f - 1)}. \tag{7.10}$$

The inversely-proportional relationship between N_{trip} and M_f is presented in Figure 7.5, where $T_{S_{MCB}}$ is assumed to be 1 ms. Therefore, in the HRF fault condition, trip-times can be adjusted by varying only the $KTMS$ setting of each MCB-relay to realise protection coordination.

Protection settings for short-circuit or low-resistance faults

In the event of low-resistance or short-circuit faults (LRF condition), where the fault resistance is below a critical value (R_{f_C}), the SSFCC will begin to modulate and regulate the moving average current to $I_{control}$. The critical fault resistance may be defined as

$$R_{f_C} = \frac{V_n}{I_{S_{SSCB}} - I_n}. \tag{7.11}$$

Since the fault path is a low-resistance network with a low average fault-current, the voltage of the system will collapse. The collapsed local voltage is thereby a Boolean metric for an MCB-relay PS setting to transition to the LRF state.

The voltage-dependent coefficient ($k_{V_{dep}}$) of a MCB-relay is a value from 0 to 1, enabling a faster trip-speed in comparison to HRF condition trip-speeds. Under the LRF condition, the MCB-relay compares its local moving average current with a reduced current threshold, due to the use of $k_{V_{dep}}$. Accordingly, the multiple of the local MCB trip threshold, M_f, becomes $I(local)/(k_{V_{dep}} \cdot I_{S_{MCB}})$. Substituting this in Equation 7.10 will enable protection coordination for low-resistance faults to be realised by adjusting $KTMS$.

The coefficient $k_{V_{dep}}$ may be tuned to obtain the desired local trip-time for each MCB under LRF conditions. A lower value of $k_{V_{dep}}$ will enable a faster MCB trip response, however, a minimum time margin between coordinating devices must be kept to ensure effective selectivity. Too rapid a trip-time may reduce this time margin by causing upstream MCBs to be excessively sensitive to fault current. This may result in false-tripping, impacting the stability and security of the protection system.

Furthermore, considering that the network voltage is collapsed and that all loads are de-energised, the trip-time under low-resistance fault conditions should be selected such that it is no greater than the minimum trip-time under high-resistance fault conditions. This minimum trip-time occurs when the equivalent network-resistance, during a high-resistance fault, approaches the critical fault resistance (R_{f_C}) [144] of the system.

Accordingly, $k_{V_{dep}}$ may be optimally tuned such that the trip-time under critical high-resistance faults (nominal voltage sustained) and low-resistance faults (network voltage collapsed) is continuous. In the event of an HRF where voltage is sustained,

the local MCB current will be in the range of

$$I_{S_{MCB}} < I(local) < I_{S_{SSCB}} - I_n(other), \tag{7.12}$$

This range of local MCB current measurement can be rearranged to represent $I(local)$ in terms of a multiple of its trip threshold, M_f, such that

$$1 < M_f(HRF) < \frac{I_{S_{SSCB}} - I_n(other)}{I_{S_{MCB}}}. \tag{7.13}$$

During LRF conditions where voltage is collapsed, $I(local)$ becomes $I_{control}$. Accordingly, M_f, under these conditions can be derived as

$$M_f(LRF) = \frac{I_{control}}{I_{S_{MCB}} \cdot k_{V_{dep}}}. \tag{7.14}$$

Equating the maximum $M_f(HRF)$ and $M_f(LRF)$, $k_{V_{dep}}$ can be derived as

$$k_{V_{dep}} = \frac{I_{control}}{I_{S_{SSCB}} - I_n(other)}. \tag{7.15}$$

When configuring the MLE protection scheme for a DC distribution network, appropriate values of $KTMS$ must be assigned to coordinate trip-times between each MCB-relay. The principle for assigning $KTMS$ in terms of its target trip-time can be obtained by re-arranging Equations 7.6, where

$$KTMS = T_{trip}\left(\frac{I(local)}{k_{V_{dep}} \cdot I_{S_{MCB}}} - 1\right). \tag{7.16}$$

7.1.3 Protection System States

The behaviour of the protection system during NF, LRF and HRF states is summarised in Table 7.2. To configure the MLE protection system for the DC network in Figure 7.2, Figure 7.6 illustrates the characteristic between the trip-times in terms of samples and the local average current measurement of different MCB current ratings. In this example, all $KTMS$ are set to unity; $I_{S_{MCB}}$ of each relay are set 1.2 times its local

nominal current; $T_{S_{MCB}}$ is set to 1 ms; and $k_{V_{dep}}$ is set by Equation 7.15. Taking Relay B1 as an example, the characteristic curve in Figure 7.5 indicates actions of different MCB-relays in the three protection states. When the local current through an MCB is measured to be under its overcurrent setting, the MCB will remain stable. When the local current exceeds the MCB overcurrent setting, and the total current through the SSFCC is less than the modulation threshold that triggers current limiting, the MCB-relay will operate in HRF state. As shown in Figure 7.6, MCBs with low nominal current ratings are more sensitive to overloading. Accordingly, selective protection coordination may be deployed that includes effective fail-safe backup protection that is graded in a deterministic manner. When the total current reaches the SSFCC current threshold, the modulation action will be triggered and the average current will be regulated to a reduced level. This will cause the network voltage to collapse, triggering all MCBs to transition into the LRF state. The MCB-relay will then operate on the LRF curve and operate at the point of $I_{control}$.

Due to the optimally tuned $k_{V_{dep}}$ coefficient, the MCB trip-time for a low-resistance fault is designed to be equal to its local minimum trip-time under the HRF state. This will maintain the effective coordination and backup functionality of the protection system when operating in the LRF state.

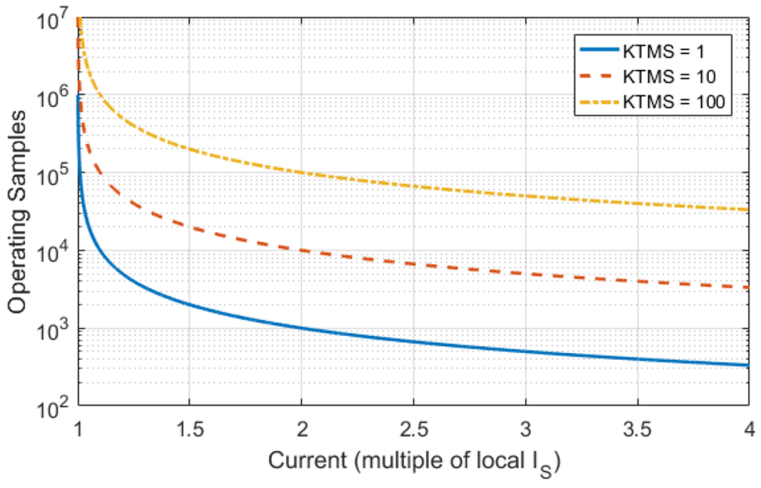

Figure 7.5: Relationship between M_f and N_{trip}.

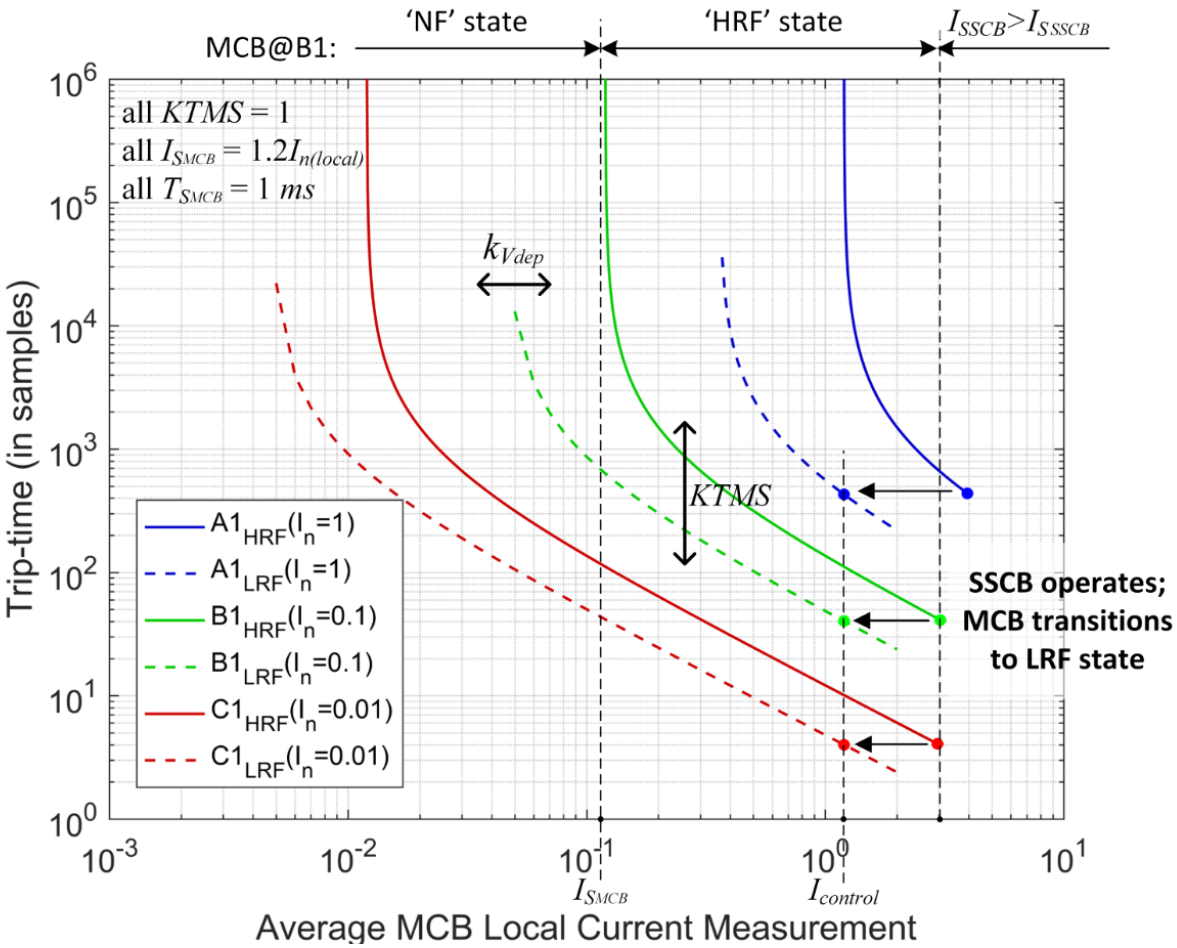

Figure 7.6: The characteristic curve of local MCB-relays.

Table 7.2: Protection system states.

Protection System States	SSFCC		MCB-Relay	
	Behaviour	Current Range	Average Voltage	Behaviour
NF	Stable	$I \leq I_n$	Normal	Reset counter
HRF	Stable	$I_n < I < I_{S_{SSCB}}$	Normal	Trip until counter full
LRF	Modulating	$\overline{I} \approx I_{control}$	Collapsed	Decrease I_S, trip until counter full

7.1.4 Analysis of Power Supplied to the Fault

In the HRF state, the SSFCC will remain on and the network voltage will remain at nominal levels. Accordingly, the power dissipated in the fault can be derived, where

$$P_f = V_n^2/R_f. \tag{7.17}$$

In the LRF state, with the SSFCC modulating, the power dissipated in the fault may be determined by analysing the energy dissipated in each-cycle divided by the period of each cycle, where

$$P_f = \frac{E_{cycle}}{T_{cycle}} = \frac{\int_0^{T_{ON}} i^2(t) R_f \, \mathrm{d}t}{T_{ON} + T_{OFF}}. \tag{7.18}$$

Substituting Equation 7.1, 7.2 and 7.4 into 7.18, the fault power can be derived, where

$$P_f = \frac{\int_0^{\frac{I_{S_{SSCB}}}{V_n/L_f}} (V_n/L_f)^2 t^2 R_f \, \mathrm{d}t}{\frac{1}{2} I_{S_{SSCB}} \cdot \frac{I_{S_{SSCB}}}{V_n/V_f}/I_{control}} = \frac{2}{3} R_f I_{S_{SSCB}} I_{control}. \tag{7.19}$$

Combining Equation 7.17 and 7.19,

$$P_f = \begin{cases} V_n^2/R_f, & R_{f_C} < R_f < +\infty \\ \frac{2}{3} R_f I_{S_{SSCB}} I_{control}, & 0 < R_f \leq R_{f_C} \end{cases}. \tag{7.20}$$

In Equation 7.20, it can be observed that P_f is inversely-proportional to R_f in the HRF state, and proportional to R_f in the LRF state. The maximum fault power occurs when R_f is approximately equal to R_{f_C}, and is different for both cases due to the SSCB current limiting operation.

Accordingly, for the case study presented in this chapter, where $I_{S_{SSCB}}$ is set to 4 pu., and $I_{control}$ is set to 1.2 pu., the highest fault power in the HRF state is 3 pu., and 1.07 pu. in the LRF state. This is potentially an order of magnitude lower than if a non-MLE protection method is used.

7.2 Verification of MLE Operation with Simulation

The effectiveness of the MLE protection scheme is verified through simulation using a model of an example DC network represented in Figure 7.7. This model consists of one SSFCC at position A1 and 5 MCBs at downstream feeder locations that operate in coordination to provide backup protection in both HRF and LRF states. The SSFCC settings are defined in Table 7.1, whilst the MCB-relay settings are described in Table 7.3.

In Table 7.3, $T_{trip}(target)$ is the target trip time of each relay in the LRF state. $k_{V_{dep}}$ is set by Equation 7.15, and $KTMS$ is set by Equation 7.16. The time margin of each target trip time is reserved to 20 ms, which must be set higher than the MCB

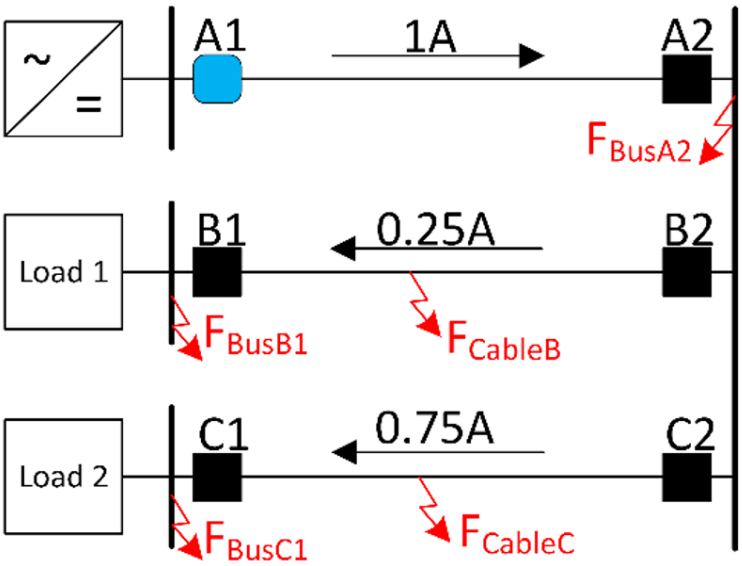

Figure 7.7: Sample network.

Table 7.3: Example setting of MCB-relays.

	B1	B2	C1	C2	A2
$T_{S_{MCB}}$	1 ms				
I_n	0.25	0.25	0.75	0.75	1
$I_{S_{MCB}}$	0.3	0.3	0.9	0.9	1.2
$k_{V_{dep}}$	0.37	0.37	0.32	0.32	0.3
$T_{trip}(target)$	20 ms	40 ms	20 ms	40 ms	60 ms
$KTMS$	0.196	0.393	0.063	0.126	0.140

interruption time to avoid mis-coordination.

Taking an LRF case as an example, Figure 7.8 presents the instantaneous current responses measured at Relay A2, during the initiation of the fault. The current is modulated, and the length of off-time in each cycle is adjusted by the SSFCC to achieve the steady-state moving average current, $I_{control}$. Figure 7.9 presents the actions of Relay A2. As shown in Figure 7.9 (a), the moving average current is controlled to approximately $1.2I_n$, whilst the average voltage is almost zero. As shown in Figure 7.9 (b), the relay will calculate the increment, inc, every 1 ms according to Equation 7.7 and 7.9. The number in the counter will accumulate each increment value, as shown in Figure 7.9 (c), until it exceeds the counter threshold setting, C_T triggering the trip signal as shown in Figure 7.9 (d). The results indicate that the actual trip time is the same as the target trip time shown in Table 7.3.

As shown in Figure 7.7, multiple fault scenarios are evaluated with variable fault resistances from 1 to 1000 mΩ at different locations. Breaker operations are disabled so that the trip-time of backup MCB-relays can be observed. The trip-time of the main relays in each fault scenario is recorded in Table 7.4. Additionally, in order to demonstrate protection coordination, the trip-time of the main relay and backup relays for each fault scenario is plotted in Figure 7.10. The power dissipated in each fault scenario is shown in Figure 7.11.

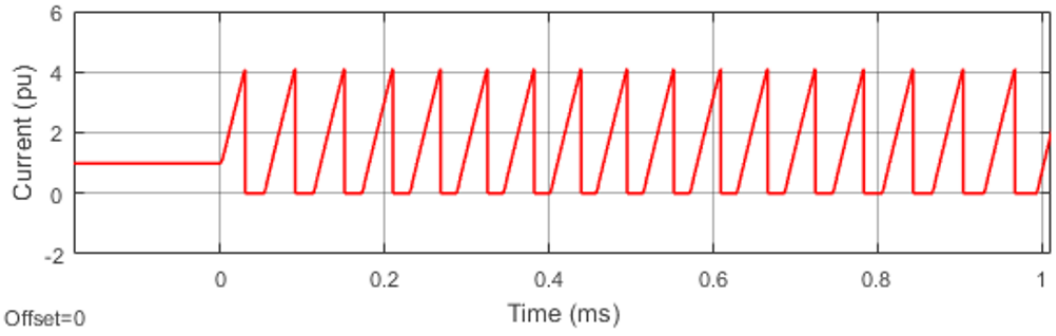

Figure 7.8: Instantaneous responses of Relay A2 under LRF condition.

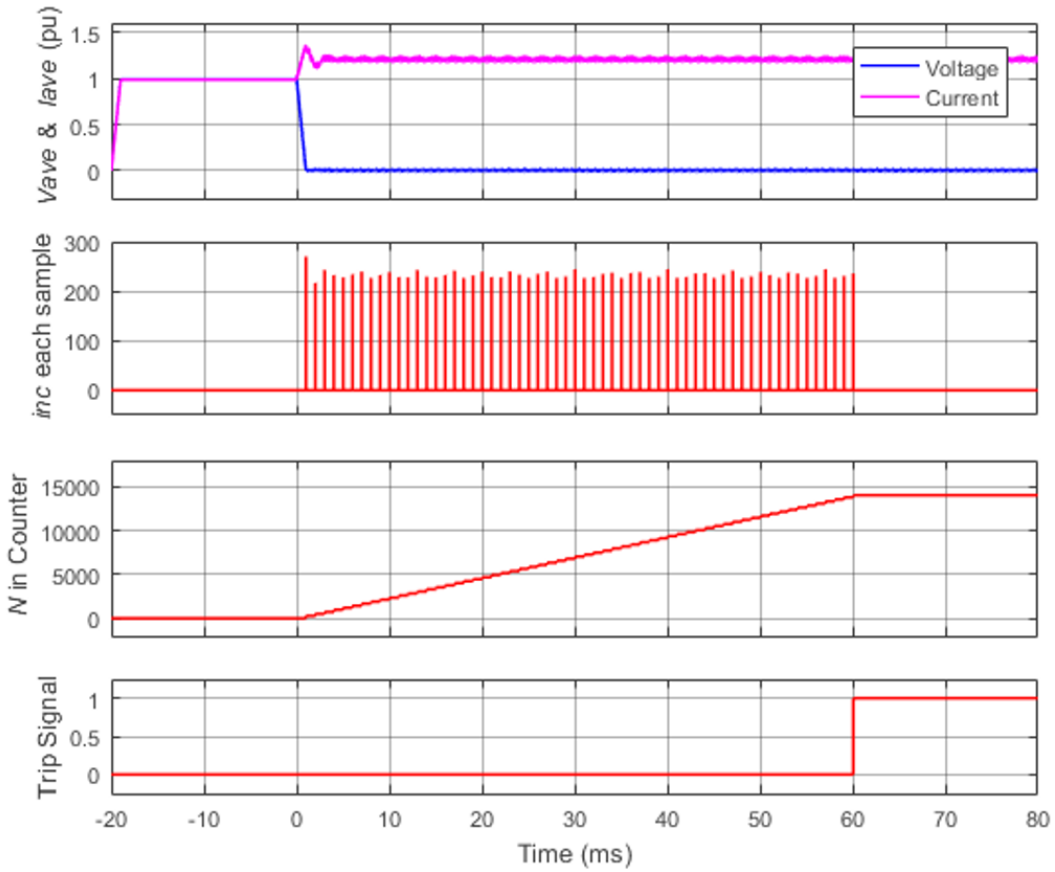

Figure 7.9: Actions of Relay A2, a) moving average voltage and current, b) the increment of each sample, c) the accumulated number in the counter, d) trip signal.

Figure 7.10 shows that when the fault resistance is lower than the critical resistance (which in this case is 333.3 mΩ), the protection system operates in the LRF state where the trip-time remains nearly constant. When the fault resistance is greater than the critical resistance, the protection system operates in the HRF state where the trip-times of all the MCBs gradually increase as a function of higher resistance. Figure 7.11 illustrates the fault power in terms of fault resistance at different locations. It indicates that the peak fault power is limited to 3 pu., and occurs at the critical resistance point.

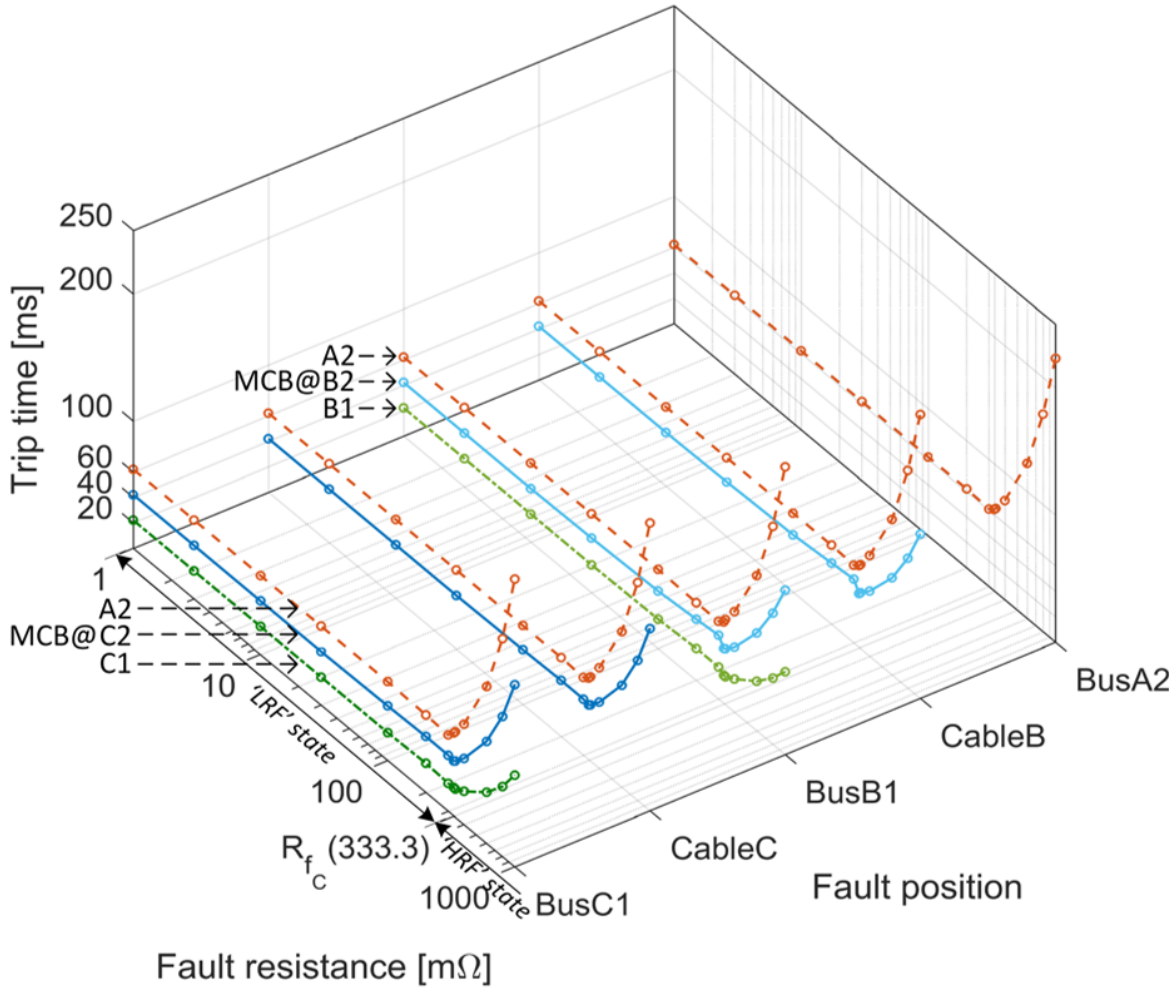

Figure 7.10: Result of protection trip-time and backup trip-time.

7.3 Hardware Implementation of MLE Protection

This section presents the experimental validation of the MLE protection scheme on a low-voltage DC distribution system within a laboratory environment, as shown in Figure 7.12. Details of the experimental hardware are provided in Table 7.5. The DC distribution system has been configured to form the same architecture as illustrated in Figure 7.7. The system is equipped with distributed voltage and current transducers, and solid-state switches to perform protection actions. A VSC is connected at Bus A1 supplying power to a 6.6 Ω load located at Bus C1. The switch by Bus A1 employs the SSFCC algorithm whilst all other downstream switches apply the MCB-relay al-

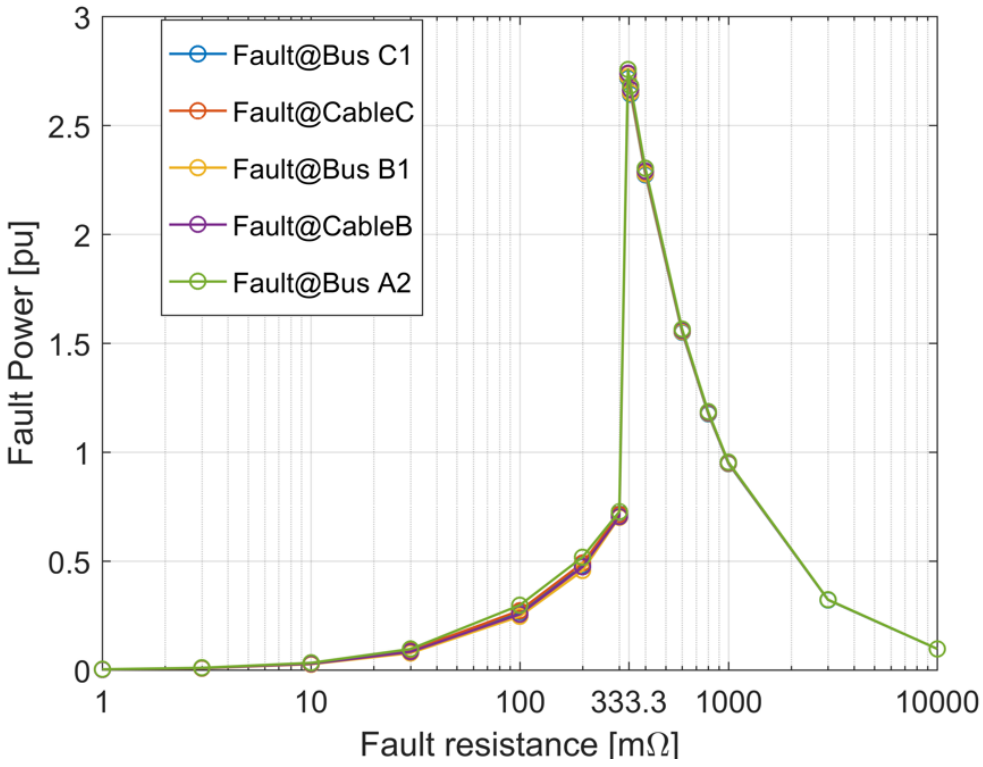

Figure 7.11: Fault power dissipation.

Table 7.4: Trip-time of the main protection MCB-relay for variable resistance faults at each position.

Fault Pos.	**Bus B1**	**Cable B**	**Bus C1**	**Cable C**	**Bus A2**
Main Relay	B1	B2	C1	C2	A2
R_f (mΩ)	Trip-time (ms)				
1	22	42	22	42	62
2	22	42	22	42	62
10	22	42	22	42	62
30	22	43	22	42	62
100	23	45	22	43	62
200	25	48	23	44	62
300	25	50	22	44	61
330	22	42	22	43	64
340	22	44	22	44	66
400	26	51	26	52	78
600	39	76	40	80	122
800	52	102	55	110	171
1000	65	129	72	143	223

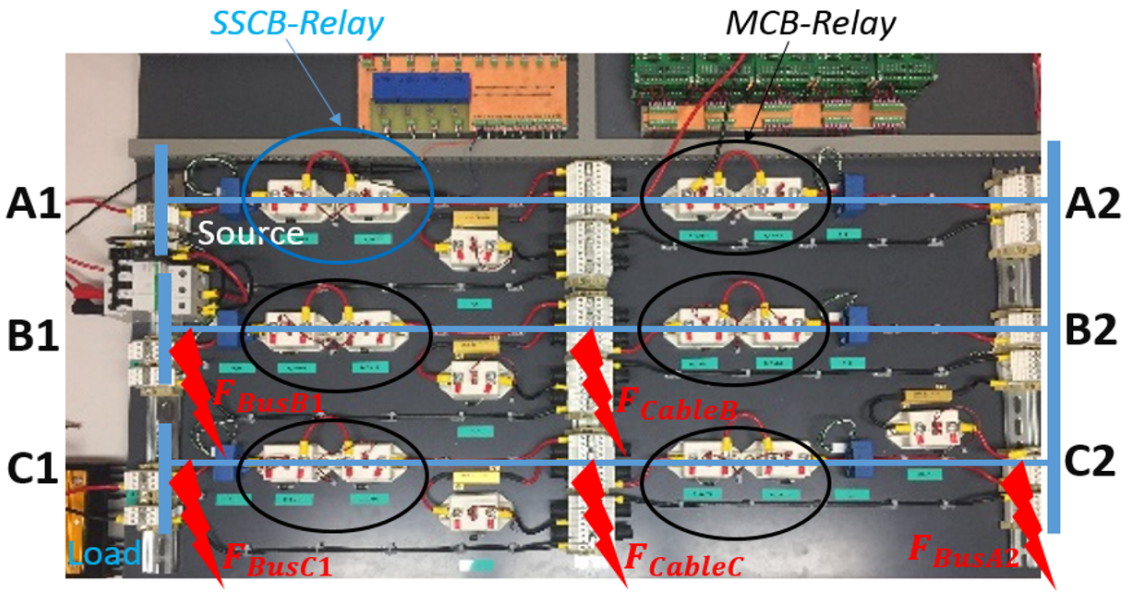

Figure 7.12: DC rig setup.

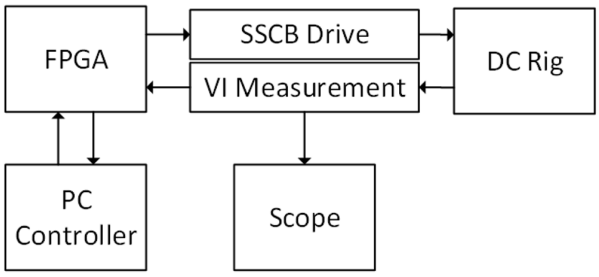

Figure 7.13: Experiment layout.

gorithm, emulating electromechanical protection devices. Data from the transducers is acquired centrally as shown in Figure 7.13.

The central processor employs an FPGA-based controller which is used to capture measurement data from transducers and to control the power switches. Each switch is controlled independently based on its local voltage and current measurements. The SSFCC at A1 executes its protection function with a 1 MHz high-speed control loop, while the MCB-relays conduct the protection algorithm with a 1 kHz low-speed loop using a moving average of the current profile.

Table 7.5: Details of experimental hardware.

	Function	**Harware**	**Experiment Test Setting**
1	Power supply	MDL TOE-7621 320 W 100 kHz DC power supply	Set to 24 V constant voltage
2	Disconnect supply prior to fault	Semikron SKM 111AR MOSFET	100 V, 200 A nominal (600 A max)
3	Current measurement	LEM HAS 200-S	50 A/V measurement ratio
4	Voltage measurement	LEM LV 25-P	5.7 V/V measurement ratio
5	Representative cable inductor	Murata 15222c	2.2 μH ±20% (4.3 mΩ)
6	Representative load	Panel mount fixed resistor	6.6 Ω
7	FPGA processor	NI cRio-9024	Control loop time is 1 μs
8	Analogue input	NI 9223	
9	Analogue output	NI 9269	
10	Digital I/O	NI 9401	
11	Signal capture	Tektronix OSC MSO 2004B	1 GS/s/channel

The virtual relays employed on the FPGA controller are programmed according to the proposed setting strategy, however, due to hardware limitations, the SSFCC employs a fixed open-time in each duty-cycle rather than controlling the output current with a dynamic open-time. Accordingly, this is a preliminary qualitative experiment verifying the effectiveness of protection coordination using the MLE approach.

As shown in Figure 7.7, rail-to-rail short-circuit faults are sequentially injected at Bus C1, Cable C, Bus B1, Cable B, and Bus A2, respectively to verify the performance of protection discrimination. Additionally, the voltage at Bus A1 is continually monitored to ensure the link voltage of the DC source does not decrease to zero.

Table 7.6 shows the trip-position and trip-time results for the short-circuit faults at different positions. The results indicate that only the nearest upstream MCB-relay will act to isolate the fault, as desired, and that the trip-time is graded to provide effective backup protection.

Table 7.6: Protection operation results.

Fault position	Bus B1	Cable B	Bus C1	Cable C	Bus A2
Trip-position	B1	B2	C1	C2	A2
Trip-time	1 ms	5 ms	1 ms	5 ms	8 ms

Figure 7.14 presents voltage and current waveforms measured at Bus A1 when the fault is applied. As a fault occurs on the network, the SSFCC at Bus A1 starts to modulate the current causing the voltage of the VSC to be maintained above zero, intrinsically protecting the anti-parallel diodes. The average current is limited to non-detrimental levels, enabling the slower downstream MCBs to operate in coordination. Additionally, the modulated fault current provides zero-current periods which improves the reliability of MCBs when interrupting fault current.

As observed in Figure 7.14, large current transients are produced when the SSFCC at Bus A1 interrupts the current. They can be restrained by connecting a snubber in parallel with the SSCB. A soft turn-off with ramp current decay could also be deployed to avoid transient over-voltage. In addition, since the fault current response of a real DC power distribution system is unpredictable, a dynamic closed-loop current controller may also be implemented to realise a more accurate average fault current let-through.

Nevertheless, these transients have not impacted on the coordinated operation of MCBs in this case because the moving average measurement is not dramatically affected by the transient current.

7.4 MLE Applications in Other Grid Configurations

The MLE protection scheme has been demonstrated on a passive radial DC grid in the previous sections, however, renewable energy generation is widely used in LVDC distribution networks and some applications may adopt loop-type DC grids. These ap-

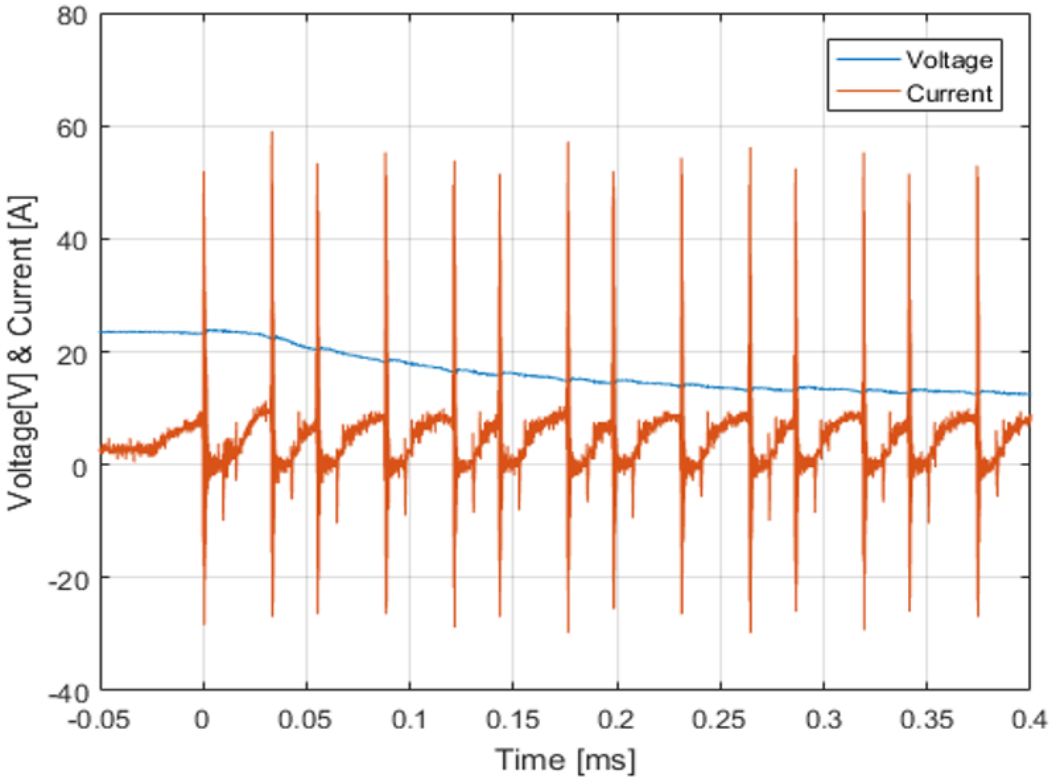

Figure 7.14: Voltage and current waveform under a short-circuit fault.

plications may cause the fault current to be supplied from several sources, or in the case of a loop-type network, from two fault paths. For LRF conditions, it is expected that directional MCB-relays can be utilised to achieve fast and coordinated fault isolation. However, for some HRF conditions, the measured fault current through the MCB-relays may actually be lower than the nominal rated current. To ensure the MCB-relay can operate with the designed speed, the following two solutions are proposed.

7.4.1 Application in Loop-Type DC Grids

Equivalent model method

The MLE protection scheme is feasible for protecting loop-type DC grids using an equivalent model method. As shown in Figure 7.15 (a), the current fed into Node A is equivalent to the summation of the clockwise and anticlockwise currents, I_{cw} and

I_{a-cw}. Using Kirchhoff's current law, if I_{cw} is measured and then added to the measured current at each relay using a dedicated communication system, the loop-type DC grid can be equivalent to a radial grid as shown in Figure 7.15 (b). Accordingly, the settings of each relay can be determined using the MLE method to realise coordinated protection in the anticlockwise direction. For example, if a fault occurs at Bus D in Figure 7.15 (b), Relay D1 will provide primary protection, whilst Relay C2, C1, B2, B1 and A will provide backup protection.

The protection coordination in the clockwise direction can be realised in the same manner. I_{a-cw} may be added to each relay to realise an equivalent clockwise radial network. Accordingly, each relay will have two settings and will operate based on the equivalent current direction.

Alternative to communication

As communications may increase the cost and complexity of LVDC protection for the loop-type topology, two mechanical reclosers may be employed to temporarily interrupt the fault current on each path and realise coordinated protection in clockwise and anticlockwise direction successively.

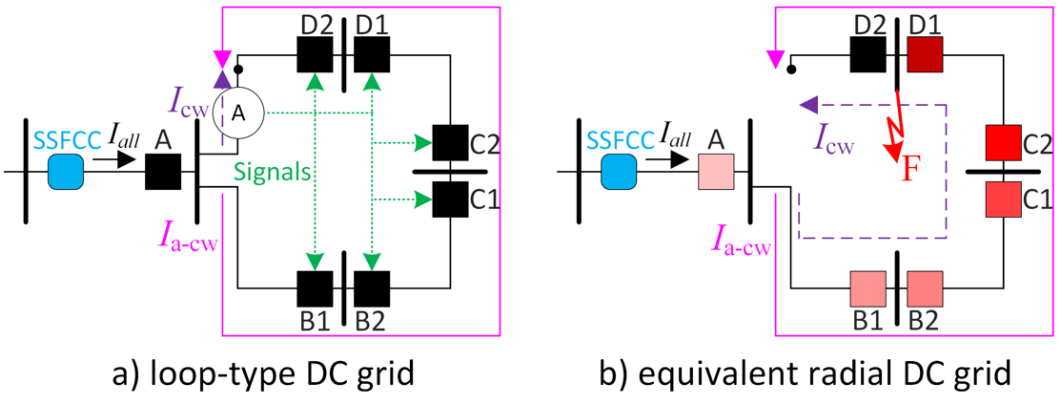

Figure 7.15: Equivalent model method in loop-type DC grids.

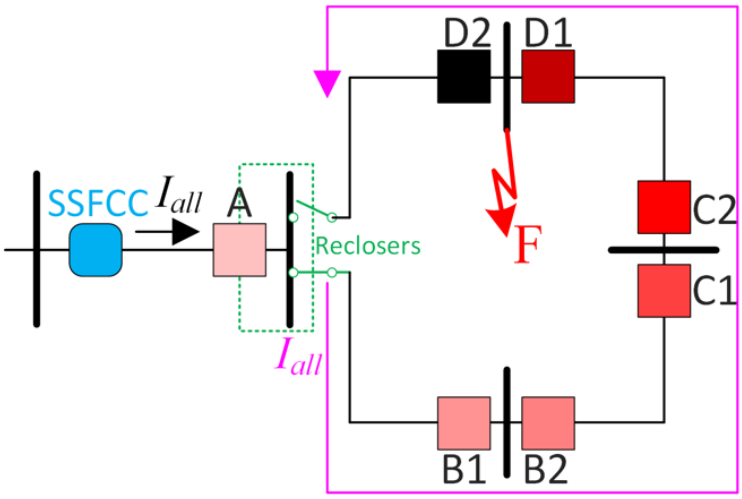

Figure 7.16: Equivalent model method with reclosers.

As shown in Figure 7.16, the two reclosers are installed at Bus A and controlled in terms of the current measurement at Relay A. If an overcurrent is detected at Relay A, one of the reclosers will be opened immediately so that the loop-type grid is reconfigured to form a radial network. The MCB-relays will operate in coordination in terms of the MLE protection scheme.

After the overcurrent through Relay A is cleared, the first recloser is closed again and the other recloser is opened to enable the coordinated protection in the other direction in the same manner. When the fault is isolated through both fault paths, both reclosers are returned to the on position to reinstate the power supply.

Compared to the equivalent model approach, this method can avoid the use of long-distance communication links, which may be not reliable. However, the drawback of this method is requiring two additional mechanical circuit breakers with local communication. The deployment of the reclosers may cause extra cost, and this may cause the downstream relays to operate slower as the reclosers may operate with a delay. Furthermore, due to the reclosers operating in turns, part of the ring network may suffer a short-term power outage.

7.4.2 Participation of Distributed Generators

To accommodate distributed generators (DG) on LVDC networks, a supplementary protection function can be added to ensure the MLE protection operates as intended. The participation of DGs must maximally maintain the inherent fault current through the downstream MCB-relays within the fault path. As shown in Figure 7.17, during HRF conditions, the fault current through the near-fault MCB-relays (B1 and C1) is determined from the nominal voltage and its downstream equivalent resistance only. Since the voltage drop across the primary feeder is still negligible during HRF conditions, the DG will have no impact on the current through the downstream MCB-relays. However, to accommodate LRF conditions and avoid the potential for the DG contributing additional fault current, the DG could employ a fast-speed breaker to block its current infeed quickly to minimise the impact to the MCB-relays' operating time. This may be implemented using a grid-side under-voltage detection threshold mechanism.

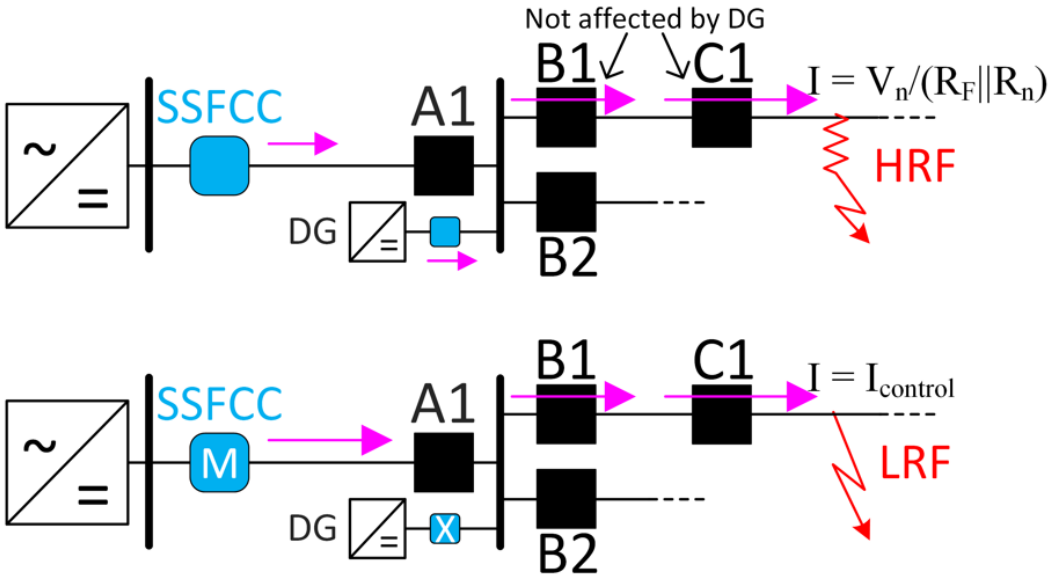

Figure 7.17: Participation of DGs.

7.4.3 Connection with downstream DC-DC Converters

DC-DC converters can provide a supply to independent radial DC networks. Such converters, such as the topology shown in Figure 7.18, employ filter capacitors that may rapidly discharge during short-circuit fault conditions. To mitigate this issue, an SSFCC may also be used to impede high fault current to avoid fully discharging the capacitor. Accordingly, protection coordination can be realised using the same methodology presented in the previous sections. If the DC-DC converter also features a capacitive filter on the input side to the converter, a fast-acting SSCB can be employed to prevent excessive current contributions from this to the wider grid under LRF conditions (similar to the proposed approach for DGs).

7.5 Summary of Chapter 7

For grid application DC distribution networks, a DC-version overcurrent protection scheme based on the "FCL + MCBs" structure has been proposed that provides effective coordination within a moderate operating speed. This is achieved by coordinating one fast current-limiting upstream device and a number of downstream moderate operating speed voltage-dependent breakers. The FCLs are installed beside the PEC-driven sources to restrain the fault current from developing to a high-level, and also ensure the link voltage of the PEC remains non-zero, preventing the anti-parallel diodes from being damaged by the inverse fault current. This manner also allows the downstream protection relays to isolate the fault in distribution lines with a moderate speed. A

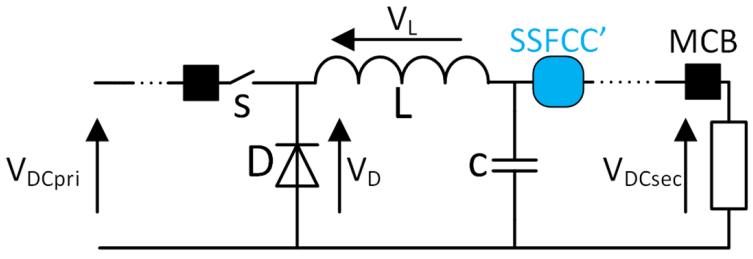

Figure 7.18: Typical configuration of a buck converter.

longer protection time-window can restore the use of time-based overcurrent coordination and enable the use of economic mechanical-circuit breakers. This solution requires no communication and uses significantly less high-speed devices, which will not only dramatically reduce the expense of the protection scheme but also improve its reliability by widening the decision-making time-window. Additionally, the MLE protection scheme provides flexibility in network extension. The original protection layout needs no reprogramming when a new feeder is installed. Though the operating time is longer, the energy dissipation will not dramatically rise because of the use of current limitation.

More generally, this MLE protection scheme has shown that there is a timely opportunity to study the metrological limitations more thoroughly as DC microgrid research matures, and ensure innovations in this field are accessible to new microgrid scheme planners. In particular, the author believes that further specific research into moderate-speed DC protection schemes could enable more rapid uptake of widespread large-scale civil DC microgrid applications.

Chapter 8

Conclusion

With the development of power electronic technology, DC networks have been increasingly used in the power system. In recent years, HVDC technology has developed rapidly and many HVDC power transmission projects have been widely applied in practice. Extended to the low-voltage area, due to the multiple advantages of DC in connecting renewable energy resources and energy storage devices, LVDC distribution network has the potential to promote the next generation of the power distribution system and it has become a new research hotspot. However, new technical standards must be established before widely applying the LVDC network. One of the main challenges is to design the specialised protection system. However, due to the different fault characteristics of DC system, the traditional AC protection methods can no longer be used in DC networks. Dealing with LVDC network protection, Fletcher [25] has taken the lead in analysing the fault characteristics of LVDC system and proposed theoretical basis of LVDC protection. Based on the previous work, this thesis has taken the actual working conditions into account and proposed the potential protection implementation challenges of the existing protection schemes. This thesis has proposed corresponding solutions to address implementation challenges. The work presented in this thesis is divided into two parts. The first part (Chapter 1-3) has reviewed the basic structure, operation principle and the state-of-the-art protection schemes in LVDC networks. At the end of the first part (Section 3.4 and 3.5), the author has discussed the research gaps and identified the remaining technical challenges about the existing LVDC pro-

tection schemes. The second part of the thesis includes Chapter 4-7. In Chapter 4, an LVDC model has been established to investigate the fault behaviours in complex networks. The conclusion can be drawn is that the fault current before the peak value, where the protection device must operate, is mainly caused by the capacitor discharge of the converter. The three main contributions of this thesis are delivered in Chapter 5-7.

On the basis of the relevant research in recent years, more consideration is given to the practicability of DC protection schemes in the real-world implementation. Since a DC fault usually induces a very high current magnitude in a very short time, it is generally believed that DC protection devices must operate fast to prevent the occurrence of excessive fault current. However, high-speed protection schemes must be supported by advanced on-line measurement devices. Specifically, high-speed differential protection requires very precise time synchronisation, otherwise, a very small time synchronisation error may cause protection mal-operation when external faults occur. The author has proposed a "multi-sample differential (MSD) protection scheme" to address this issue, which improves the protection stability of external faults whilst maintaining the protection sensitivity when faults occur inside the protected zone.

Additionally, the measurement of rate-of-change of current, which is commonly used in high-speed distance protection, is susceptible to noise. Even a tiny noise may lead to poor measurement accuracy causing protection failure. The author has presented two approaches to reduce the impact of noise. One is selecting an appropriate step-time according to the noise intensity for derivative computation, the other is applying a low-pass filter with an appropriate cut-off frequency according to the circuit characteristics. Whilst if a very high noise exists in the current measurement, both methods should be considered in a joint to restrain the influence of noise in $\mathrm{d}i/\mathrm{d}t$ measurement. Finally, considering the inherent high cost of using a large number of high-speed devices, high-speed protection schemes may not be suitable for low-power DC distribution networks, where installation costs are a key design factor. A feasible strategy is to use high-speed fault current limiters (FCL) at the power sources to limit the rise of fault current, whilst the downstream complex network employs the tradition mechani-

cal circuit breaker (MCB) to isolate the fault in a relaxed time-window. Accordingly, the author has proposed a "modulated low fault-energy (MLE) protection scheme", which realises non-communication protection coordination based on the FCL + MCB structure. The MLE protection scheme imitates the conventional IDMT overcurrent protection which has been widely applied in traditional AC power grid for decades with good reliability. The author believes that the FCL + MCB based moderate-speed protection is more immune to environmental interference and can significantly reduce the cost, so it has more practical application value for DC distribution networks.

In general, the main difficulty of DC protection is to compromise between the high-speed protection requirements and protection reliability. The fast capacitor discharging speed requires the protection device to detect and isolate the fault current quickly. High-speed protection schemes, such as communication-based differential protection, can detect and cut off faults in several milliseconds. However, high-speed protection relays may be vulnerable to even very short-term environmental interference. Advanced hardware may be employed to realise both of high-speed and good reliability, but it is necessary to avoid excessive cost caused by large-scale use. The author believes that the scheme entirely based on high-speed hardware is not conducive to the reliability and economy of the protection system, and the excessive dependence on the communication system makes these worse. It is recommended that the design of DC protection scheme should not only pursue high operation speed but also consider the reliability of long-term use and the cost. By limiting fault energy in some way, a longer allowed time-window for clearing the faults may be achievable without damaging network devices. Compared with the high-speed protection schemes, energy-limitation schemes may improve the reliability of protection while reducing the cost, which has more potential for large-scale application in practice.

8.1 Review of Chapters and Contributions

- Chapter 1 has briefly introduced the prospects of DC microgrid in modern power system and its advantages in integrating the growing renewable elements. How-

ever, before realising large-scale deployment of DC microgrid, it is necessary to establish a comprehensive electrical protection system. Although many effective protection schemes have been proposed in the literature, few of them have considered the implementation challenges in practice. As the motivation of this research, this thesis will shed light on the implementation challenges of DC protection schemes and propose the corresponding solutions.

- Chapter 2 has outlined the fundamentals of the LVDC network, including the network topology, voltage-level and operating modes. Also, this chapter has overviewed the commonly used renewable elements, such as PV, wind turbine, ESS and EV. These devices must be connected through corresponding power electronic converters to control power transfer, and the LVDC network must adopt appropriate control strategy to balance the power of each component and maintain normal voltage.

- Chapter 3 has reviewed DC fault characteristics, available protection hardware, and the state-of-the-art DC protection schemes, including high-speed overcurrent, differential and distance protection. According to the requirements of these protection methods, the chapter has also proposed the implementation challenges of the DC protection schemes in practice.

- Chapter 4 has demonstrated the model of each component with the corresponding mathematical principles, including the AC source, DC loads, PV generators and ESSs. A DC microgrid model has eventually been built by combining the components with appropriate converters.

- Chapter 5 has proposed a "multi-sample differential (MSD) protection scheme" to address the issue that a short time synchronisation error (TSE) may cause protection instability in the conventional high-speed DC differential protection. The MSD protection scheme considers multiple current measurement samples, to ensure the protection stability when a fault probably occurs outside the protected zone, but remain sensitive when a fault occurs inside the zone. The effectiveness has been proved with both software simulation and hardware experiment results.

- Chapter 6 has proposed two methods for optimising the accuracy of the rate-of-change of current ($\mathrm{d}i/\mathrm{d}t$) measurement. The $\mathrm{d}i/\mathrm{d}t$ measurement is necessarily used for DC fault distance detection, however, the measurement of $\mathrm{d}i/\mathrm{d}t$ is very sensitive to even small noise which may cause a protection failure. One method is selecting an optimised sampling frequency which can be derived from the noise level. The other method is applying a low-pass filter with appropriate cut-off frequency. The performances of optimisation have been demonstrated with simulation results.

- Chapter 7 has proposed a "modulated low fault-energy (MLE) protection scheme" to achieve moderate-speed protection coordination in DC networks. Since the high-speed DC protection schemes require many advanced devices, hence these may not be suitable for widely-used in low-power LVDC networks. Inspired by the IDMT graded overcurrent protection for the AC grid, MLE will realise protection coordination in different operating time based on current and voltage measurements with a lower cost. This method employs an "FCL + MCBs" structure, which allows a longer operating time for selecting the fault location. Each relay operates only based on the local measurement and no communication is required. From both simulation and experiment results, the relays at different positions trip in graded operating times.

8.2 Key Areas of Future Work

A number of areas of future work have been identified which have the potential to boost the realisation of reliable wide-area LVDC network protection. These are discussed in the following sections.

8.2.1 Real-World Performance Evaluation of the Protection Schemes with Practical Demonstration Projects

So far, the LVDC network has not been widely used in reality. Due to the lack of long-term verification in real-world projects, this thesis has only analysed the potential implementation challenges of the protection schemes from the theoretical level. In Chapter 5, the proposed MSD protection scheme is verified based on an artificial communication delay using FPGA, and in Chapter 6, the improvement of $\mathrm{d}i/\mathrm{d}t$ measurement is demonstrated based on an added white noise. By producing these virtual interferences, the proposed protection schemes have been validated to improve the performance and maintain protection reliability. However, the prototype hardware of the protection schemes must be manufactured and further verified in the real on-site LVDC projects, so as to ensure that these methods can remain robust before their live implementation in a complex real environment. At present, some LVDC demonstration projects are being invested and constructed around the world, which may allow conducting the on-site test in the future. The following work will move to discover and resolve the issues along with the actual applications, including verifying whether the mentioned issues exist in practice; validating whether the proposed method can effectively mitigate the issues; and revealing more implementation issues during long-term practical application.

8.2.2 Exploration of More Reliable Moderate-Speed Protection Schemes

A novel moderate-speed has been proposed in Chapter 7 using a modulated fault current to restrain the fault current within a non-destructive level. The moderate-speed protection strategies have greater advantages than the high-speed strategies for LVDC networks, because this sort of methods can dramatically reduce the cost and decrease of risk of protection mal-operation. The author believes the moderate-speed protection is more likely to become the major protection strategy in the future. However, the proposed MLE protection scheme is the first method in this kind. There potentially exists better moderate-speed protection schemes. For example, the modulation of fault

current may have adverse impacts on the stability of the LVDC network. If the FCL can limit the fault current into a steady-state for achieving downstream protection coordination, the LVDC network may be less affected by the protection operation. Based on the idea of using a mix of circuit breaking technologies, future research should consider actual hardware limitations to develop the most adaptable DC protection schemes. After long-term practical verification, the scheme with the best performance will be selected.

8.2.3 Development of DC Parallel and Serial Arc Fault Protection Strategies

This thesis mainly focuses on the short circuit fault protection. However, DC arc faults can also cause a significant hazard for the security of the LVDC power system. DC arc faults can be divided into the type of series fault and parallel fault. A parallel arc fault occurs between two poles. Compared with short-circuit fault, the parallel arc fault usually leads to a small current between poles. The series arc fault occurs on a single pole. The poor connection of the line may result in a series arc fault, leading to a higher line impedance. Arc faults may only cause small changes in current and voltage, which is accordingly challenging to detect. However, the failure of arc fault protection may result in long-term partial heat accumulation leading to a severe fire hazard. A potential solution of arc fault protection is to analyse the unique waveform characteristics of arc faults, so as to distinguish the difference between arc faults and normal load changes. The author will also investigate arc fault protection in future research and eventually design a comprehensive protection system for future LVDC distribution networks.

Bibliography

[1] H. Lund and B. Mathiesen, "Energy system analysis of 100% renewable energy systems - The case of Denmark in years 2030 and 2050," *Energy*, vol. 34, no. 5, pp. 524-531, 2009.

[2] UK Government, "National renewable energy action plan - Article 3 of the renewable energy directive 2009/28/EC," United Kingdom, 2009.

[3] UK Government, "UK plan for tackling roadside nitrogen dioxide concentrations - An overview," *Environment Food & Rural Affairs*, United Kingdom, 2017.

[4] International Energy Agency, "China 13th Renewable Energy Development Five Year Plan (2016-2020) [Online]," Available: http://www.nea.gov.cn/2016-12/19/c_135916140.htm, [Accessed: 02.08.19].

[5] D. Green, "Centralised to decentralised energy: What does it mean? [Online]," Available: https://reneweconomy.com.au/centralised-decentralised-energy-mean-34072, [Accessed: 05.08.19].

[6] SUNPOWER, "Home Solar System [Online]," Available: https://us.sunpower.com/homeowners/equinox-home-solar-systems, [Accessed: 08.08.19].

[7] TESLA, "Solar Roof [Online]," Available: https://www.tesla.com/en_GB/solarroof?redirect=no, [Accessed: 10.08.19].

[8] BBC News, "Electric carmaker Tesla to build factory in Shanghai [Online]," Available: https://www.bbc.co.uk/news/business-44789823, [Accessed: 10.08.19].

[9] T. Dragičević, X. Lu, J. C. Vasquez, and J. M. Guerrero, "DC Microgrids—Part II: A Review of Power Architectures, Applications, and Standardization Issues," *IEEE Transactions on Power Electronics*, vol. 31, pp. 3528-3549, 2016.

[10] A. Dyśko, D. Tzelepis, and C. Booth, "Assessment of Risks Resulting from the Adjustment of ROCOF Based Loss of Mains Protection Settings - Phase II," Department of Electronic and Electrical Engineering, University of Strathclyde, Glasgow, 2015.

[11] A. Ulbig, T. Borsche, and G. Andersson, "Impact of Low Rotational Inertia on Power System Stability and Operation," presented at *the IFAC World Congress*, Cape Town, 2014.

[12] Eirgrid and Soni Company, "RoCoF modification proposal – TSOs' recommendations," Northern Ireland, 2012.

[13] F. Glinka, R. Bertram, T. Wippenbeck, P. Erlinghagen, and A. Schnettler, "Protection of today's and future low voltage grids with high DG penetration: Laboratory and simulative analysis of blinding of protection with inverters," in *13th International Conference on Development in Power System Protection 2016 (DPSP)*, 2016, pp. 1-6.

[14] F. Coffele, C. Booth, A. Dysko, and G. Burt, "Quantitative analysis of network protection blinding for systems incorporating distributed generation," in *IET Generation, Transmission & Distribution*, vol. 6, pp. 1218-1224, 2012.

[15] N. Phannil, C. Jettanasen, and A. Ngaopitakkul, "Power quality analysis of grid connected solar power inverter," in *2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017 - ECCE Asia)*, pp. 1508-1513, 2017.

[16] Z. Jing, "The damage and restraining measures of harmonics in power systems," in *2011 2nd International Conference on Artificial Intelligence*, Management Science and Electronic Commerce (AIMSEC), pp. 736-738, 2011.

[17] F. Li, R. Li, and F. Zhou, "Monitoring and energy management of the microgrid," in *Microgrid Technology and Engineering Application*, pp. 91-113, 2016.

[18] Berkeley Lab - Grid Integration Group, "About Microgrids [Online]," Available: https://building-microgrid.lbl.gov/about-microgrids, [Accessed: 12.08.19].

[19] J. John, M. Francis, L. Ju, and J. Jin-Woo, "AC-microgrids versus DC-microgrids with distributed energy resources: A review," in *Renewable and Sustainable Energy Reviews*, vol. 24, pp. 387-405, 2013.

[20] Engineering and Technology History, "Milestones: Pearl Street Station [Online]," Available: http://ethw.org/Milestones:Pearl_Street_Station,_1882, [Accessed: 01.08.19].

[21] A. Rizzato Lede, *et al.*, "Microgrid architectures for distributed generation: A brief review," in *IEEE PES Innovative Smart Grid Technologies Conf.*, Washington US, pp. 1-6, 2017.

[22] W. Long and S. Nilsson, "HVDC transmission: yesterday and today," *IEEE Power and Energy Magazine*, vol. 5, no. 2, pp. 22-31, 2007.

[23] N. Mohan, T. Undeland, and W. Robbins, "Line-frequency phase-controlled rectifiers and inverters: line-frequency ac - controlled dc," in *Power Electronics: Converters, Applications, and Design*, 3rd ed, USA: John Wiley & Sons, inc., pp. 103-111, 2002.

[24] E. Rodriguez-Diaz, F. Chen, J. Vasquez, J. Guerrero, R. Burgos, and D. Boroyevich, "Voltage-Level Selection of Future Two-Level LVdc Distribution Grids: A Compromise Between Grid Compatibility, Safety, and Efficiency," *IEEE Electrification Magazine*, vol. 4, pp. 20-28, 2016.

[25] S. Fletcher, "Protection of Physically Compact Multi-terminal DC Power Systems," *PhD Thesis*, Electronic and Electrical, University of Strathclyde, Glasgow, UK, 2013.

[26] J. Yang, J. Fletcher, and J. Reilly, "Short-Circuit and Ground Fault Analyses and Location in VSC-Based DC Network Cables," *IEEE Transactions on Industrial Electronics*, vol. 59, pp. 3827-3837, 2012.

[27] D. Salomonsson, L. Soder, and A. Sannino, "Protection of Low-Voltage DC Microgrids," *IEEE Transactions on Power Delivery*, vol. 24, pp. 1045-1053, 2009.

[28] J. Bialasiewicz, "Renewable Energy Systems With Photovoltaic Power Generators: Operation and Modeling," *IEEE Transactions on Industrial Electronics*, vol. 55, pp. 2752-2758, 2008.

[29] A. Naiem, Y. Hegazy, A. Abdelaziz, and M. Elsharkawy, "A Classification Technique for Recloser-Fuse Coordination in Distribution Systems With Distributed Generation," *IEEE Transactions on Power Delivery*, vol. 27, pp. 176-185, 2012.

[30] P. Cairoli, R. Rodrigues, and H. Zheng, "Fault current limiting power converters for protection of DC microgrids," in *SoutheastCon 2017*, 2017, pp. 1-7.

[31] X. Chen and J. Jin, "Energy Efficiency Analysis and Energy Management of a Superconducting LVDC Network," *IEEE Transactions on Applied Superconductivity*, vol. 26, pp. 1-5, 2016.

[32] L. Qi, J. Pan, X. Huang, and X. Feng, "Solid-state fault current limiting for DC distribution protection," in *2017 IEEE Electric Ship Technologies Symposium (ESTS)*, Arlington US, pp. 187-191, 2017.

[33] M. Monadi, C. Gavriluta, A. Luna, J. I. Candela, and P. Rodriguez, "Centralized Protection Strategy for Medium Voltage DC Microgrids," *IEEE Transactions on Power Delivery*, vol. 32, pp. 430-440, 2017.

[34] P. Nuutinen, *et al.*, "LVDC rules – technical specifications for public LVDC distribution network," *CIRED - Open Access Proceedings Journal*, vol. 2017, no. 1, pp. 293-296, 2017.

[35] M. Wadi, *et al.*, "Smart hybrid wind-solar street lighting system fuzzy based approach: Case study Istanbul-Turkey," in *6th International Istanbul Smart Grids and Cities Congress and Fair (ICSG)*, Istanbul Turkey, pp. 71-75, 2018.

[36] S. Georges and F. Slaoui, "Case Study of Hybrid Wind-Solar Power Systems for Street Lighting," in *21st International Conference on Systems Engineering*, pp. 82-85, 2011.

[37] S. Bora and P. Pol, "Development of solar street lamp with energy management algorithm for ensuring lighting throughout a complete night in all climatic conditions," in *2016 International Conference on Inventive Computation Technologies (ICICT)*, vol. 2, pp. 1-5, Tamilnadu India, 2016

[38] H. Chiu, *et al.*, "Design and Implementation of a Photovoltaic High-Intensity-Discharge Street Lighting System," *IEEE Transactions on Power Electronics*, vol. 26, no. 12, pp. 3464-3471, 2011.

[39] MathWorks (2019), "Implement generic battery model - Simulink," Available: https://www.mathworks.com/help/physmod/sps/powersys/ref/battery.html, [Accessed: 03.09.19].

[40] T. Dragicevic, "Hierarchical control of a direct current microgrid with energy storage systems in a distributed topology," *PhD Thesis*, Faculty Elect. Eng. Comput., University of Zagreb, Zagreb Croatia, 2013.

[41] G. Lacey, G. Putrus, and E. Bentley, "Smart EV charging schedules: supporting the grid and protecting battery life," *IET Electrical Systems in Transportation*, vol. 7, no. 1, pp. 84-91, 2017.

[42] R. Balog and P. Krein, "Bus Selection in Multibus DC Microgrids," *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 860-867, 2011.

[43] T. Dragicevic, *et al.*, "Advanced LVDC Electrical Power Architectures and Microgrids: A step toward a new generation of power distribution networks," *IEEE Electrification Magazine*, vol. 2, no. 1, pp. 54-65, 2014.

[44] Q. Shafiee, *et al.*, "Hierarchical Control for Multiple DC-Microgrids Clusters," *IEEE Transactions on Energy Conversion*, vol. 29, no. 4, pp. 922-933, 2014.

[45] Q. Shafiee, *et al.*, "Modeling, stability analysis and active stabilization of multiple DC-microgrid clusters," in *2014 IEEE International Energy Conference (ENERGYCON)*, Croatia, pp. 1284-1290, 2014.

[46] L. Meng, *et al.*, "Review on Control of DC Microgrids and Multiple Microgrid Clusters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 3, pp. 928-948, 2017.

[47] S. Moayedi and A. Davoudi, "Distributed Tertiary Control of DC Microgrid Clusters," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1717-1733, 2016.

[48] C. Jin, *et al.*, "Implementation of Hierarchical Control in DC Microgrids," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 8, pp. 4032-4042, 2014.

[49] J. Park, *et al.*, "DC Ring-Bus Microgrid Fault Protection and Identification of Fault Location," *IEEE Transactions on Power Delivery*, vol. 28, no. 4, pp. 2574-2584, 2013.

[50] R. Mohanty and A. Pradhan, "Protection of Smart DC Microgrid With Ring Configuration Using Parameter Estimation Approach," *IEEE Transactions on Smart Grid*, vol. 9, no. 6, pp. 6328-6337, 2018.

[51] U. Orji, *et al.*, "Adaptive Zonal Protection for Ring Microgrids," *IEEE Transactions on Smart Grid*, vol. 8, no. 4, pp. 1843-1851, 2017.

[52] N. Hatziargyriou, *et al.*, "Microgrids - an overview of ongoing research, development, and demonstration projects," *IEEE Power and Energy Magazine*, vol. 5, no. 4, pp. 78-94, 2007.

[53] X. Liu, P. Wang, and P. Loh, "A Hybrid AC/DC Microgrid and Its Coordination Control," *IEEE Transactions on Smart Grid*, vol. 2, no. 2, pp. 278-286, 2011.

[54] M. Nasir, *et al.*, "Solar PV-Based Scalable DC Microgrid for Rural Electrification in Developing Regions," *IEEE Transactions on Sustainable Energy*, vol. 9, no. 1, pp. 390-399, 2018.

[55] SUNPOWER, "MAXEON GEN II SOLAR CELLS [Online]," Available: https://us.sunpower.com/solar-resources/sunpower%C2%AE-maxeon%E2%84%A2-gen-ii-solar-cells/, [Accessed: 10.09.19].

[56] TESLA, "Model S - Premium Electric Sedan [Online]," Available: https://www.tesla.com/sites/default/files/tesla-model-s.pdf, [Accessed: 12.09.19].

[57] J. Unwin, "The top 10 countries in the world by wind energy capacity [Online]," Available: https://www.power-technology.com/features/wind-energy-by-country/, [Accessed: 15.09.19].

[58] Power Technology, "Top 10 biggest wind farms [Online]," Available: https://www.power-technology.com/features/feature-biggest-wind-farms-in-the-world-texas/, [Accessed: 20.09.19].

[59] L. Saihi and A. Boutera, "Robust control of a variable-speed wind turbine with fixed pitch angle and strategy MPPT control associated on a PMSG," in *8th International Conference on Modelling, Identification and Control (ICMIC)*, Algeria, pp. 326-331, 2016.

[60] G. Rajani, "Emerging trends in Uninterrupted Power Supplies: Patents view," in *2016 Biennial International Conference on Power and Energy Systems: Towards Sustainable Energy (PESTSE)*, India, pp. 1-5, 2016.

[61] S. D'Arco, J. Suul, and O. Fosso, "A Virtual Synchronous Machine implementation for distributed control of power converters in SmartGrids," Electric Power Systems Research, vol. 122, pp. 180-197, 2015.

[62] J. Li, B. Chen, J. Zhou, and Y. Mo, "The optimal planning of wind power capacity and energy storage capacity based on the bilinear interpolation theory," in *Smart Power Distribution Systems*, Academic Press, pp. 411-445, 2019.

[63] Server Room Environments, "Why UPS Systems Use Lead Acid Batteries [Online]," Available: https://www.serverroomenvironments.co.uk/blog/why-ups-systems-use-lead-acid-batteries, [Accessed: 25.09.19].

[64] K. Ogura and M. Kolhe, "Battery technologies for electric vehicles," in *Electric Vehicles: Prospects and Challenges*, Elsevier, pp. 139-167, 2017.

[65] A. Fathima and K. Palanisamy, "Renewable systems and energy storages for hybrid systems," in *Hybrid-Renewable Energy Systems in Microgrids*, Woodhead Publishing, pp. 147-164, 2018.

[66] IN COMPLIANCE, "The Future of Battery Technologies: A General Overview & Focus on Lithium Ion [Online]," Available: https://incompliancemag.com/the-future-of-battery-technologies-a-general-overview-a-focus-on-lithium-ion/, [Accessed: 27.09.19].

[67] IEA, "Global EV Outlook 2019 - Scaling up the transition to electric mobility [Online]," Available: https://www.iea.org/publications/reports/globalevoutlook2019/, [Accessed: 27.09.19].

[68] TESLA, "Tesla Supercharger [Online]," Available: https://www.tesla.com/en_GB/supercharger?redirect=no, [Accessed: 28.09.19].

[69] BMW, "Product - BMW i WALLBOX CONNECT [Online]," Available: https://www.shopbmwusa.com/Product/6536/BMW-I-WALLBOX-CONNECT/, [Accessed: 28.09.19].

[70] GTM Creative Strategies, "Why Electrified Transportation Needs Microgrids - Microgrids provide EV charging flexibility in terms of power and cost savings [Online]," Available: https://www.greentechmedia.com/articles/read/why-electrified-transportation-needs-microgrids, [Accessed: 29.09.19].

[71] T. Gnann, A. Klingler, and M. Kühnbach, "The load shift potential of plug-in electric vehicles with different amounts of charging infrastructure," *Journal of Power Sources*, vol. 390, pp. 20-29, 2018/06/30/ 2018.

[72] BBC Autos, "Questioning electric vehicles' green cred [Online]," Available: http://www.bbc.com/autos/story/20160316-questioning-electric-vehicles-green-cred, [Accessed: 30.09.19].

[73] Y. Siwakoti, M. Forouzesh, and N. Pham, "Power Electronics Converters — An Overview," in *Control of Power Electronic Converters and Systems*, Academic Press, pp. 3-29, 2018.

[74] D. Tiku, "dc Power Transmission: Mercury-Arc to Thyristor HVdc Valves [History]," *IEEE Power and Energy Magazine*, vol. 12, no. 2, pp. 76-96, 2014.

[75] ABB, "From mercury arc to hybrid breaker - 100 years in power electronics [Online]," Available: https://library.e.abb.com/public/369669d5dd6e8e6ec1257ba500293166/70-78%202m315_EN_72dpi.pdf, [Accessed: 04.10.19].

[76] ABB, "The Gotland HVDC link - The world's first commercial HVDC transmission system, the Gotland HVDC link built in 1954, has over time been replaced with a 260 MW bipole transmission system [Online]," Available: https://new.abb.com/systems/hvdc/references/the-gotland-hvdc-link, [Accessed: 06.10.19].

[77] IEEE Transmission and Distribution Committee, "HVDC PROJECTS LISTING [Online]," Available: http://www.ece.uidaho.edu/hvdcfacts/Projects/HVDCProjectsListingDec2006.pdf, [Accessed: 08.10.19].

[78] Z. Ye, "Modeling and control of parallel three-phase PWM converters," *PhD Thesis*, Electr. Comput. Eng. Dept., Virginia Polytechnic Institute, Blacksburg, VA, USA, 2000.

[79] P. C. Loh, *et al.*, "Autonomous Operation of Hybrid Microgrid With AC and DC Subgrids," *IEEE Transactions on Power Electronics*, vol. 28, no. 5, pp. 2214-2223, 2013.

[80] X. She, A. Huang, and R. Burgos, "Review of Solid-State Transformer Technologies and Their Application in Power Distribution Systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 3, pp. 186-198, 2013.

[81] Y. Du, *et al.*, "Review of non-isolated bi-directional DC-DC converters for plug-in hybrid electric vehicle charge station application at municipal parking decks," in *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, California USA, pp. 1145-1151, 2010.

[82] D. Dong, *et al.*, "Grid-Interface Bidirectional Converter for Residential DC Distribution Systems — Part 1: High-Density Two-Stage Topology," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1655-1666, 2013.

[83] D. Dong, *et al.*, "Grid-Interface Bidirectional Converter for Residential DC Distribution Systems — Part 2: AC and DC Interface Design With Passive Components Minimization," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1667-1679, 2013.

[84] Z. Ding, *et al.*, "A Novel Soft-Switching Multiport Bidirectional DC–DC Converter for Hybrid Energy Storage System," *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 1595-1609, 2014.

[85] Z. Zhang, *et al.*, "Analysis and Design of a Bidirectional Isolated DC–DC Converter for Fuel Cells and Supercapacitors Hybrid System," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 848-859, 2012.

[86] M. Ryu, *et al.*, "Test bed implementation of 380V DC distribution system using isolated bidirectional power converters," in *2013 IEEE Energy Conversion Congress and Exposition*, Colorado, pp. 2948-2954, 2013.

[87] P. Kundur, "Power System Stablity and Control (Power System Engineering Series)," Toronto: McGraw-Hill inc., p. 1176, 1994.

[88] A. Mullane, G. Bryans, and M. Malley, "Kinetic energy and frequency response comparison for renewable generation systems," in *2005 International Conference on Future Power Systems*, Netherlands, pp. 6, 2005.

[89] J. Guerrero, *et al.*, "Advanced Control Architectures for Intelligent Microgrids — Part I: Decentralized and Hierarchical Control," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 4, pp. 1254-1262, 2013.

[90] M. Rana and M. Abido, "Energy management in DC microgrid with energy storage and model predictive controlled AC–DC converter," *IET Generation, Transmission & Distribution*, vol. 11, no. 15, pp. 3694-3702, 2017.

[91] M. Singaravel and S. Daniel, "MPPT With Single DC–DC Converter and Inverter for Grid-Connected Hybrid Wind-Driven PMSG–PV System," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 8, pp. 4849-4857, 2015.

[92] N. Eghtedarpour and E. Farjah, "Distributed charge/discharge control of energy storages in a renewable-energy-based DC micro-grid," *IET Renewable Power Generation*, vol. 8, no. 1, pp. 45-57, 2012.

[93] National Grid, "Frequency Changes during Large Disturbances and their Impact on the Total System [Online]," Available: https://www.nationalgrid.com/sites/default/files/documents/16943-Industry%20Consultation.pdf, [Accessed: 15.10.19].

[94] L. Gao, *et al.*, "A DC Microgrid Coordinated Control Strategy Based on Integrator Current-Sharing," *Energies*, vol. 10, no. 8, 2017.

[95] R. Ferreira, *et al.*, "Analysis of voltage droop control method for dc microgrids with Simulink: Modelling and simulation," in *10th IEEE/IAS International Conference on Industry Applications*, US, pp. 1-6, 2012.

[96] M. Tawfeeq. (2005), "Power system Protection - part 5 Overcurrent Protective Relays," Available: https://www.philadelphia.edu.jo/academics/mlazim/uploads /Power%20System%20protection%20-%20Part%2005.pdf, [Accessed: 20.10.19].

[97] Schneider Electric, "RM22TR33 three-phase voltage control relay 380 - product datasheet [Online]," Available: https://docs-emea.rs-online.com/webdocs/1591/0900766b81591879.pdf, [Accessed: 21.10.19].

[98] M. Bamber, *et al.*, "Current and Voltage Transformers," in *Network protection and automation guide: protective relays, measurement and control*, ALSTOM, pp. 87-108, 2011.

[99] Infineon, "Current Sensing Using Linear Hall Sensors - Application Note [Online]," Available: https://www.infineon.com/dgdl/Current_Sensing_Rev.1.1.pdf?fileId=db3a304332d040720132d939503e5f17, [Accessed: 22.10.19].

[100] LEM, "Current Transducer-HAS 50...600-S and Voltage Transducer-LV 25-P [Online]," Available: https://www.lem.com/sites/default/files/products_datasheets/has_50_600-p_e.pdf, [Accessed: 23.10.19].

[101] TAMURE-EUROPE, "HALL EFFECT CURRENT SENSORS [Online]," Available: http://www.tamura-europe.co.uk/sites/pro/hal.html, [Accessed: 23.10.19].

[102] Honeywell, "Current Sensors Line Guide [Online]," Available: https://sensing.honeywell.com/honeywell-sensing-current-sensors-line-guide-005895-1-en.pdf, [Accessed: 24.10.19].

[103] LEM, "Frequently Asked Questions [Online]," Available: https://www.lem.com/en/faqs, [Accessed: 24.10.19].

[104] H. Brändle, "ABB FOCS Fiber-Optic Current Sensor [Online]," Available: https://www.ieee.ch/assets/Uploads/pes/downloads/0506/052kbohnertopticalsensors.pdf, [Accessed: 25.10.19].

[105] ABB, "FOCS – Fiber-Optic Current Sensor [Online]," [Accessed: 26.10.19].

[106] LEM, "Split coil Rogowski coil - datasheet [Online]," Available: https://www.lem.com/sites/default/files/products_datasheets/art-b22-dxxxxx_series.pdf, [Accessed: 26.10.19].

[107] K. Brydak and A. Szlachta, "Measuring methods of welding process parameters," *Measurement Automation Monitoring*, vol. 62, pp. 26, 2016.

[108] Semikron, "Power MOSFET Modules – Semitrans TM M1 SKM 111AR Datasheet [Online]," Available: http://www.gdrectifiers.co.uk/uploads/SEMIKRON_DataSheet_SKM_111_AR_.pdf, [Accessed: 27.10.19].

[109] STMicroelectronics, "AN4544 Application note - IGBT datasheet tutorial [Online]," Available: https://www.st.com/resource/en/application_note/dm00122161-igbt-datasheet-tutorial-stmicroelectronics.pdf, [Accessed: 27.10.19].

[110] X. Song, C. Peng, and A. Huang, "A Medium-Voltage Hybrid DC Circuit Breaker, Part I: Solid-State Main Breaker Based on 15 kV SiC Emitter Turn-OFF Thyristor," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 1, pp. 278-288, 2017.

[111] National Instruments, "Intelligent Real-Time Embedded Controller for CompactRIO on FPGA Chassis and I/O modules." Available:ni.com/en-gb/shop/compactrio.html, [Accessed: 28.10.19].

[112] NUMATO LAB, "FPGA Vs ASIC: Differences Between Them And Which One To Use? [Online]," Available: https://numato.com/blog/differences-between-fpga-and-asics/#what-is-asic, [Accessed: 01.11.19].

[113] M. Baran and N. Mahajan, "Overcurrent Protection on Voltage-Source-Converter-Based Multiterminal DC Distribution Systems," *IEEE Transactions on Power Delivery*, vol. 22, no. 1, pp. 406-412, 2007.

[114] M. Bamber, *et al.*, *et al.*, "Overcurrent protection for phase and earth fault," in Network protection and automation guide: protective relays, measurement and control, Alstom Grid, 2011.

[115] S. Fletcher, *et al.*, "High-Speed Differential Protection for Smart DC Distribution Systems," *IEEE Transactions on Smart Grid*, vol. 5, no. 5, pp. 2610-2617, 2014.

[116] M. Monadi, *et al.*, "A communication-assisted protection scheme for direct-current distribution networks," *Energy*, vol. 109, pp. 578-591, 2016.

[117] A. Emhemed and G. Burt, "An Advanced Protection Scheme for Enabling an LVDC Last Mile Distribution Network," *IEEE Transactions on Smart Grid*, vol. 5, no. 5, pp. 2602-2609, 2014.

[118] S. Fletcher, *et al.*, "Fault detection and location in DC systems from initial $\mathrm{d}i/\mathrm{d}t$ measurement," presented at *the Euro Tech Con Conference*, Manchester, UK, 2012.

[119] X. Feng, L. Qi, and J. Pan, "A Novel Fault Location Method and Algorithm for DC Distribution Protection," *IEEE Transactions on Industry Applications*, vol. 53, no. 3, pp. 1834-1840, 2017.

[120] A. Meghwani, S. Srivastava, and S. Chakrabarti, "A Non-unit Protection Scheme for DC Microgrid Based on Local Measurements," *IEEE Transactions on Power Delivery*, vol. 32, no. 1, pp. 172-181, 2017.

[121] H. Chen, "Research on the control strategy of VSC based HVDC system supplying passive network," in *2009 IEEE Power & Energy Society General Meeting*, Alberta Canada, pp. 1-4, 2009.

[122] C. Li, "DC Microgrid Demo [Online]," Available: https://www.mathworks.com/matlabcentral/fileexchange/69223-dc-microgrid-demo, [Accessed: 04.11.19].

[123] W. Tasi-Fu and C. Yu-Kai, "Modeling PWM DC/DC converters out of basic converter units," *IEEE Transactions on Power Electronics*, vol. 13, no. 5, pp. 870-881, 1998.

[124] C. Li, "DC-DC Step-Down (Buck) Converter with Close-Loop Power Ctrl [Online]," Available: https://ww2.mathworks.cn/matlabcentral/fileexchange/70538-dc-dc-step-down-buck-converter-with-close-loop-power-ctrl?s_tid=prof_contriblnk, [Accessed: 07.11.19].

[125] B. Zhao, *et al.*, "Overview of Dual-Active-Bridge Isolated Bidirectional DC–DC Converter for High-Frequency-Link Power-Conversion System," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4091-4106, 2014.

[126] MathWorks, "Implement PV array modules [Online]," Available: https://ww2.mathworks.cn/help/physmod/sps/powersys/ref/pvarray.html, [Accessed: 09.11.19].

[127] R. Li and L. Xu, "Review of DC fault protection for HVDC grids," *Wiley Interdisciplinary Reviews: Energy and Environment*, vol. 7, no. 2, p. e278, 2018.

[128] N. Villamagna and P. A. Crossley, "A Symmetrical Component-Based GPS Signal Failure-Detection Algorithm for use in Feeder Current Differential Protection," *IEEE Transactions on Power Delivery*, vol. 23, no. 4, pp. 1821-1828, 2008.

[129] L. Zhan, *et al.*, "Utilization of Chip-Scale Atomic Clock for Synchrophasor Measurements," *IEEE Transactions on Power Delivery*, vol. 31, no. 5, pp. 2299-2300, 2016.

[130] IEEE Standard for N times 64 kbps Optical Fiber Interfaces between Teleprotection and Multiplexer Equipment, 2017.

[131] Use of IEC 61850 to transmit synchrophasor information according to IEEE C37.118, 2012.

[132] IEEE Standard for Synchrophasor Data Transfer for Power Systems, 2011.

[133] Network Time Protocol, 2015.

[134] Precision Time Protocol, 2008.

[135] D. Tzelepis, *et al.*, "Centralised busbar differential and wavelet-based line protection system for multi-terminal direct current grids, with practical IEC-61869-compliant measurements," *IET Generation, Transmission & Distribution*, vol. 12, no. 14, pp. 3578-3586, 2018.

[136] V. D. Andrade and E. Sorrentino, "Typical expected values of the fault resistance in power systems," in *2010 IEEE/PES Transmission and Distribution Conference and Exposition: Latin America (T&D-LA)*, pp. 602-609, 2010.

[137] J. Won, *et al.*, "Dual-Phase Tapped-Delay-Line Time-to-Digital Converter With On-the-Fly Calibration Implemented in 40 nm FPGA," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 10, no. 1, pp. 231-242, 2016.

[138] K. Parnell and R. Bryner, "Comparing and contrasting FPGA and microprocessor system design and development [Online]," Available: https://pdfs.semanticscholar.org/3822/8702298b6210c829c1bc34288b289bbf005f.pdf, [Accessed: 15.11.19].

[139] Vision, "Maintenance-Free Rechargeable Sealed Lead Acid Battery Datasheet [Online]," Available: https://www.vision-batt.eu/sites/default/files/public/docs/products/manuals/CP1280H.pdf, [Accessed: 15.11.19].

[140] Velleman, "Adjustable DC power supply – PS3020, [Online]," Available: www.esr.co.uk/manuals/461-555.pdf, [Accessed: 17.11.19].

[141] TDK, "Aluminum electrolytic capacitor, [Online]," Available: www.mouser.co.uk/datasheet/2/400/B41456_B41458-1219979.pdf, [Accessed: 17.11.19].

[142] M. Farhadi and O. Mohammed, "A New Protection Scheme for Multi-Bus DC Power Systems Using an Event Classification Approach," *IEEE Transactions on Industry Applications*, vol. 52, no. 4, pp. 2834-2842, 2016.

[143] A. Meghwani, S. Srivastava, and S. Chakrabarti, "A new protection scheme for DC microgrid using line current derivative," in*2015 IEEE Power & Energy Society General Meeting*, Colorado US, pp. 1-5, 2015.

[144] P. Rakhra, "On the Protection of Compact DC Power Systems with High-Power Energy Storage," *PhD Thesis*, Electronic and Electrical Engineering, University of Strathclyde, 2017.