University of Strathclyde
Electronic and Electrical Engineering
Department

Parallel Connected Inverter Operation in an Islanded Microgrid

by

Mohd Azrik Bin Roslan
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This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

Signed: Mohd. Azrik Date: 08 July 2013

Dedication

To my mother, my father, my wife and Nurul Iman

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Abstract

This thesis focuses on improving power sharing and ac distribution system power losses for parallel connected inverters in an islanded microgrid. The effect of line impedance on power flow in ac system is presented. A new circulating current definition for multiple parallel connected inverters connected to the same load bus is proposed. An improved instantaneous average current sharing (IACS) scheme with two additional gain schedulers is proposed to improve conventional IACS controller performance under line impedance mismatch. A generalized model of single-phase parallel connected inverters with the improved IACS scheme is derived. This model is used for voltage and current controller design. A new power sharing scheme utilizing a central controller for parallel connected inverters in an islanded microgrid is presented. This scheme is optimized after incorporating a power ratio calculation. Case studies of a rural islanded microgrid involving three DGs with eight distributed loads demonstrate the power sharing scheme's capability to reduce distribution power losses and improve voltage regulation.

List of Symbols

a_1 a_2	Gain step (Gain scheduler 1 and 2)
c_1 c_2	Threshold for acceptable current difference (Gain scheduler 1,2) (A)
C	Capacitance (F)
C_f	Output filter capacitance (F)
D	PWM duty cycle
D_{jl}	Distance between the j^{th} inverter and the l^{th} load (m)
$DRat_{jl}$	Power ratio based on distance between each inverter and load
E	Inverter output voltage amplitude (V)
E_o	Rated inverter output voltage amplitude (V)
ΔE	Maximum allowable output voltage amplitude deviation (V)
$\overline{E}_k$	Output voltage of k^{th} inverter (V)
ΔE_{xj}, ΔE_{yj}, ΔE_{zj}	Adjustment amplitude for the j^{th} inverter (V)
f	System fundamental frequency (Hz)
f_{sw}	Switching frequency (Hz)
f_{comm}	Communication frequency (Hz)
G_j	Closed loop voltage gain of j^{th} inverter
H_j	Outer current loop controller of j^{th} inverter
i_o	Output current (A)
i^*	Reference current (A)
i_N	Output current of N^{th} inverter (A)
i_{dN}	Current difference of N^{th} inverter (A)
$\overline{I}_k$	Output current of k^{th} inverter (A)
$\overline{I}_{avg}$	Average output current (A)
$\overline{I}_{Hk}$	Circulating current seen by k^{th} inverter (A)
K_1 K_2	Gain scheduler 1, 2
K_f	Gain of the voltage feed-forward loop
K_c	Gain of the current feedback loop
K_P	Proportional gain of voltage controller
K_{Res}	Resonant gain of voltage controller

K_{PH}	Proportional gain of current sharing controller
K_{ResH}	Resonant gain of current sharing controller
L	Inductance (H)
L_f	Output filter inductance (H)
L_{intj}	Interfacing inductance of j^{th} inverter (H)
$LPRat_l$	l^{th} load active power ratio
$LQRat_l$	l^{th} load reactive power ratio
m	Frequency droop coefficient
n	Voltage droop coefficient
N	Number of parallel connected inverters
N_L	Number of loops for voltage synchronization
P	Active power (W)
$P_{\max}$	Maximum active power (W)
P_j	Output active power of j^{th} inverter (W)
P_j^o	Rated active power of the j^{th} inverter (W)
P_j^*	Active power reference of j^{th} inverter (W)
$P_{\Delta j}$	Active power difference of j^{th} inverter (W)
P_{aj} P_{bj} P_{cj}	Active power limits of the j^{th} inverter (W)
P_{L_l}	Active power consumes by l^{th} load (W)
r_{Pj} r_{Qj}	Active and reactives power ratio of j^{th} inverter
r_{PT}	Active power total ratio
r_{QT}	Reactive power total ratio
R	Resistance (Ω)
R_f	Output filter resistance (Ω)
S_{base}	Base apparent power (VA)
T	Sampling period (s)
T_a, T_b, T_c, T_d	Power adjustment period (s)
T_r	Max time for power adjustment (s)
Q	Reactive power (VAr)
$Q_{\max}$	Maximum reactive power (VAr)
Q_j	Output reactive power of j^{th} inverter (VAr)

Q_j^o	Rated reactive power of the j^{th} inverter (VAr)
Q_j^*	Reactive power reference of j^{th} inverter (VAr)
$Q_{\Delta j}$	Reactive power difference of j^{th} inverter (VAr)
Q_{aj}, Q_{bj}, Q_{cj}	Reactive power limits of the j^{th} inverter (VAr)
Q_{L_l}	Reactive power consumes by l^{th} load (VAr)
v_i^*, V^*	Reference voltage (V)
V	Load bus voltage (V)
V_{dc}	Dc voltage (V)
V_{base}	Base voltage (V)
V_{pcc}	Point of common coupling voltage (V)
V_{diff}	Voltage difference (V)
ω_o	Rated frequency (rad/s)
ω_c	Cut off frequency of proportional-resonant controller (rad/s)
$\Delta\omega$	Maximum allowable output voltage frequency deviation (rad/s)
X	Reactance (Ω)
Z	Magnitude of system impedance
Z_j	Output impedance of j^{th} inverter (Ω)
Z_{lj}	Line impedance of j^{th} inverter (Ω)
$\bar{Z}_k$	System impedance of k^{th} inverter (Ω)
Z_L	Load impedance (Ω)
Z_{linej}	Line impedance of j^{th} inverter (Ω)
α , ϕ , δ	Power angle (^{o})
$\Delta\alpha_{xj}$, $\Delta\alpha_{yj}$, $\Delta\alpha_{zj}$	Adjustment angles for the j^{th} inverter (^{o})
θ	Phase of system impedance (^{o})

List of Abbreviations

ac	Alternating Current
ADC	Analogue to Digital Converter
CAN	Communication Area Network
CHP	Combined Heat and Power
dc	Direct Current
DG	Distributed Generation
DSP	Digital Signal Processor
IACS	Instantaneous Average Current Sharing
IGBT	Insulated Gate Bipolar Transistor
IP	Internet Protocol
PCC	Point of Common Coupling
PI	Proportional-Integral
PR	Proportional-Resonant
PSO	Particle Swarm Optimization
PV	Photovoltaic
PWM	Pulse Width Modulation
RVG	Reference Voltage Generator
SCU	Synchronization Control Unit
SPWM	Sinusoidal Pulse Width Modulation
TCP	Transmission Control Protocol
THD	Total Harmonics Distortion
UK	United Kingdom
UPS	Uninterruptible Power Supplies
VSI	Voltage Source Inverter
3C	Circular Chain Control

Preface

Distributed generation (DG) technology has been developing fast in many countries due to the availability of different energy resources such as photovoltaic panels, fuel cells, and wind turbines. DG is usually managed in a more decentralized way through the concept of a microgrid. Microgrid technology is still new and developing so offers many research possibilities. The goal of this thesis is to develop a control technique to improve the power sharing, reduce the distribution power losses, and improve load voltage regulation in a DG based islanded microgrid. This thesis comprises of seven chapters:

Chapter one provides DG background, development, technologies, advantages and challenges. Then the microgrid concept is introduced followed by the problem statements and research objectives.

Chapter two presents a brief explanation on the inverter configuration and a detailed survey of parallel connected inverter control for island mode operation. Droop control and active load sharing control with their derivatives are presented.

Chapter three investigates ac power flow analysis for inverters under the effect of inductive, resistive and complex line impedance. Then a new circulating current definition for multiple parallel connected inverters connected to the same load bus is proposed.

Chapter four develops an advanced instantaneous average current sharing (IACS) scheme to improve the conventional IACS controller which performs poorly under line impedance mismatch. Two gain schedulers are added to the conventional IACS controller. A generalized model of a single-phase parallel connected inverter system is derived and used for voltage and current controller design and the parameter selection process.

Chapter five presents a new power sharing scheme for parallel connected inverters in an islanded microgrid. The technique requires low-bandwidth communication between the inverters and the central controller for active and reactive power information exchange. The proposed power sharing scheme outperforms

conventional droop control as it has a faster dynamic response, better sharing of reactive power between inverters that have different line impedances, and has the ability to set the active and reactive power ratio for each inverter.

In Chapter six, the proposed power sharing scheme in Chapter five is optimized by modifying the power ratio calculation. A case study of a rural islanded microgrid that consists of 3 DGs and 8 loads (group of houses) is presented. The distance between each DG to each load and the ratio of power consumed by each load to the total load are taken into consideration for power ratio calculation in the central controller. As a result, the optimized power sharing scheme is able to reduce the distribution power losses and improve load voltage regulation.

Finally, Chapter seven concludes the thesis, presents the author's contribution and suggests possible future research.

Chapter 1

Introduction

Electricity services have been predominantly served by the centralized power system that consists of generation, transmission and distribution systems. However in recent years, the concept of distributed generation has attracted huge interest amongst energy policy makers, electric power system planners, operators, and developers [1.1]. There are several reasons for this interest. First, due to the global warming, many governments decided to increase the use of renewable energy to reduce the green-house gas emission. Secondly, overall energy efficiency can be increased by using the cogeneration or combined heat and power (CHP) scheme. In addition, on-site power generation may provide higher power reliability and security for industries that require uninterrupted service [1.2].

1.1 Distributed generation

Distributed generation (DG) sometimes called embedded generation generally refers to the generation of electricity at a smaller scale and can be stand alone to supply local loads or connected to distribution network for both supplying local loads and exporting excess energy. It is mostly connected to the low or medium voltage grid but a few large DGs can be connected to the bus bars of the high voltage grid as in Figure 1.1. DG power capacity can range from a few kW to several hundreds of MW [1.2].

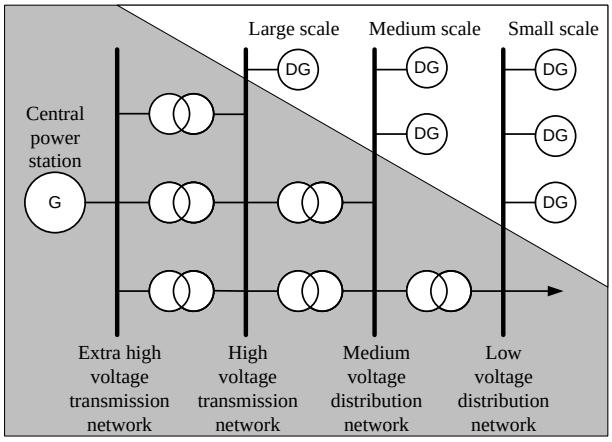


Figure 1.1 Connection of DG to existing transmission and distribution networks.

1.1.1 Background and development of DG

Previously, when the electricity coverage and demand were low, electricity supply system generators were built close to the load they were connected and only a simple connection was used for the load connection. This distributed approach was revised when the demand for electricity increased and electricity became a commercial alternative for the old energy systems such as hydraulics, direct heating, and steam. The centralized approach proved to be economically feasible and replaced the old distributed generation system [1.3].

In United Kingdom (UK), the strive for cheaper electricity in the 1920s and 1930s after the First World War lead to the creation of the National Grid in 1935. A 132 kV grid was built and completed the year after. There are 7 grid areas for the UK with the control centres located at Newcastle, Leeds, Manchester, Birmingham, Bristol, London, and Glasgow. All these grid areas were coupled together unofficially in 1937 and was proven to be productive, offering many benefits (e.g., sharing peak load coverage and backup power). This integrated electricity grid system has enhanced the overall security of the electricity supply as well as reduced the cost of generating electricity [1.4].

After the Second World War, the demand for electricity increased and the existing grids were not sufficient so the 275kV and 400kV super grids were built in the 1950s and 60s to support the ever increasing demand. Then, until the 1990s, the number of large power stations increased and most were built at remote locations or near the fuel sources. This centralized approach, although offering several disadvantages (e.g., transmission and distribution costs, energy efficiency), was preferred because these disadvantages outweighed the huge economies gained by building larger power plants.

The privatisation of the electrical utilities announced in 1988 and implemented in 1990, introduced newcomers to the generation industry, sparking competition among energy companies [1.5]. They realised opportunities in smaller scale DGs due to the following developments: First, the change in policy allowing gas to be used as a fuel for power generation and the availability of cheap gas from the North Sea introduced the use of Combined Cycle Gas Turbines which shifts the trend towards generation using natural gas. Second, the financial incentives introduced by the government to

encourage the development of renewable generation, and finally there was growing interest in the area of cogeneration.

Nowadays, advancements in designs and component materials related to DG such as photovoltaic panels, micro-turbines, digital control, remote monitoring equipment etc., have increased the range of applications and opportunities for modern DG. These advance technologies together with restructuring of wholesale and retail markets for electric power also opened the possibility to have energy system that give more freedom for customers to manage their own power to meet their own needs [1.6].

1.1.2 Type of DG

There are now many DG technologies available. Some are already established and tested but others are new and under development. DG technologies include photovoltaic, wind power, fuel cells, bio fuels, hydropower and cogeneration.

Briefly the concept, advantages, challenges, applications and examples of the mentioned DG technologies are listed in Table 1.1.

1.1.3 DG advantages

DG technology in general promises several advantages and some are now briefly discussed.

a) Increased electric system reliability

Electric system reliability is a measure of the system's ability to meet the electricity needs of customers. A traditional approach of achieving a reliable system is to have enough redundancy to ensure continuous operation when failures occur to the transmission line or the main generators. DG can supplement this by supporting local voltage level, supplying power during peak periods, and avoiding power outages that can occur due to excessive load demand [1.6]. Additionally, DG can indirectly reduce stress on grid components by preventing them from operating near their rating, hence reducing equipment failure and power outage frequency [1.7].

b) Power quality improvement

Customers, especially business operations, are concerned about power quality because it can damage the electronic components in equipment and appliances. Some power quality problems originate from utility distribution systems but most are often local problems. The best way to deal with them is through a local solution using local sources of active and reactive powers [1.8]. DG can be used to address this issue by providing voltage regulation support, harmonic control, continuous power for sensitive loads, and power factor correction [1.9].

c) Reduction of peak power requirement

The addition of DG to the grid network reduces the peak power requirement. This affects capital investment as investment decisions on new plant and equipment in the power industry usually depends on the peak power requirement. This reduction indirectly reduces the costs of electricity because acquisition of power from the most expensive power plants can be minimized. It also minimizes maintenance costs by reducing the wear and tear of electrical delivery equipment [1.6].

d) Reduce transmission and distribution losses

Transmission and distribution losses are a major disadvantage of a centralized power structure. DG is normally located at the customer site so there will only be small transmission and distribution losses. The location, DG rating, and operating power factor should be taken into consideration to achieve optimum distribution loss reduction [1.10].

e) Environmental friendly

Global warming has raised awareness worldwide about the importance of cleaner energy. Environmental concerns are the main motivating factors for the increased DG usage in Europe. DG technologies primarily use renewable energy (e.g., wind, solar, hydro, etc.) which significantly reduces greenhouse gas emissions [1.11]. It also promotes the efficient use of energy for electricity and heat production (e.g., CHP).

Table 1.1 DG technologies

Technology	Concept	Advantages	Challenges	Application	Example
Photovoltaic (PV) Ref: [1.12-14]	Direct conversion of solar radiation to electricity using photoelectric materials	• No pollution • Ideal for remote application • No moving parts • Low operating cost	• Low efficiency (12-20 %) • High capital cost • Intermittent output	Off-grid application	Powering remote village
				Grid connection	Import & export power to utility grid
				Building integrated PV	Roofing, wall and glazing system
				Hybrid power system	Combination of PV, wind, diesel generator and batteries
Wind Power Ref: [1.15-17]	Conversion of wind energy to mechanical energy	• Small footprint • No greenhouse pollution • Ideal for remote application	• Wind capacity variation • Noise pollution • Visual impact • Wildlife impact	Stand-alone device	Water pumping or battery charging in rural area
				Grid connection	Wind farm
				Hybrid power system	Small turbines connected with diesel generators, batteries and PV system
Fuel Cell Ref: [1.18-20]	Device that allows hydrogen and oxygen to be combined to produce electricity (reverse electrolysis process)	• High efficiency conversion • Quite operation • High power density	• High cost	Grid connection	Ensuring continuity of supply in the event of grid failure
				Transportation	Zero emission vehicle
Biofuel Ref: [1.21, 22]	Plant matter and its derivative are used as solid fuel or converted into liquid or gaseous forms for the production of electricity, heat, chemicals or fuels	• Low emission level • Cheaper than fossil fuel	• Environmental impact in the process of making biofuels	Electricity generation	Small size electrical power stations (<30MW)
Hydropower Ref: [1.23-25]	Convert kinetic energy of water to electricity	• High efficiency • Source freely available • Low cost per kilowatt	• The impact on environment • Limited site	Electricity generation	Small hydroelectric power plant
CHP Ref: [1.26-28]	System that generate electricity and heat in a single process	• High fuel conversion efficiencies (around 60% - 80%)	• High capital and maintenance cost	Electricity generation	CHP Plant

1.1.4 DG challenges

Although there are advantages of DG, there are also some disadvantages that need to be taken into consideration, such as high capital cost, controller complexity, power quality issues, protection, and safety concern.

a) High capital cost

One of the key issues that holds back DG mass expansion is high capital cost. For the projected period 2008 to 2035, most DG technologies other than hydroelectricity cannot economically compete with traditional fossil fuels (natural gas and coal) except in a few regions. However, some DG technologies such as solar power can be economical where electricity prices are relatively high or when there is government incentive. In most cases, the primary economic motivation for the construction of DG facilities always comes from government policies or incentives [1.29]. Table 1.2 compares power plant capital cost among several power plants technologies. The capital cost includes the civil and structural costs, mechanical equipment supply and installation, electrical and instrumentation control, project indirect costs and owners costs. From this table, in general, the capital cost to build renewable energy plants is higher than that for natural gas plant. However there has been a huge reduction in capital cost for onshore wind and solar PV plants. In the near future they can possibly match the price for natural gas plant.

Table 1.2 Power plant capital cost estimation [1.30]

Power plant technologies	**2012 Price ($/kW)**	**2010 Price ($/kW)**	**Difference (%)**
Coal (Dual Unit APCCCS*)	4,724	4,760	-1
Natural Gas (ACT**)	676	691	-2
Nuclear	5,530	5,546	0
Fuel Cells	7,108	7,105	0
Biomass (Combined Cycle)	8,180	8,205	0
Onshore Wind	2,213	2,534	-13
Offshore Wind	6,230	6,211	0
Solar Thermal	5,067	4,877	4
Solar PV (150 MW)	3,873	4,943	-22
Geothermal-Dual Flash	6,243	5,798	8
Municipal Solid Waste	8,312	8,557	-3
Conventional Hydroelectric	2,936	3,197	-8

*APCCCS - Advanced pulverized coal with carbon capture and sequestration
**ACT - Advanced Combustion Turbine

b) Control complexity

With the use of power electronics as an interfacing unit to the grid, controller implementation can be complex especially when coordination is required among parallel connected DGs. As coordination and control of DG are relatively new areas, there is no established standard and a lack of technical experience in addressing operational issues involving a large number of plug-and-play micro sources [1.31].

c) Power quality

Without a proper control of DG connected to grid, power quality might be affected. In terms of voltage level, connecting a huge number of DGs to a distribution network can force the voltage level to exceed the voltage level threshold. This can occur if the DG capacity exceeds the required load while the upstream voltage at the substation is held near the maximum allowable level. DG with some fluctuation in output power (e.g., wind turbine due to mechanical fluctuation) combined with insufficient energy storage devices to smooth this out, can cause power system flicker [1.32]. DG can also affect the system frequency if poorly controlled. This will put a burden on the grid operator to maintain the system frequency [1.33].

d) Protection

With the increased number of DG, it is possible for power to flow in bi-directionally, hence new protection schemes are needed to facilitate this issue. Some of the required protection that should be considered are [1.34]:

- DG should be disconnected from the utility grid when no longer operating in parallel
- Protection of the utility grid from damage caused by DG plants and vice versa.
- To prevent unnecessary trips, all protective relays should be coordinated.

e) Safety

Connecting DG to a distribution network introduces a source of energy at a point where previously there may not have been a source. When a fault occurs on the distribution network and the DG operators fails to detect and disconnect the DG from the main grid, a safety risk is created to the maintenance personnel who undertake repair work. [1.35].

1.2 Microgrid

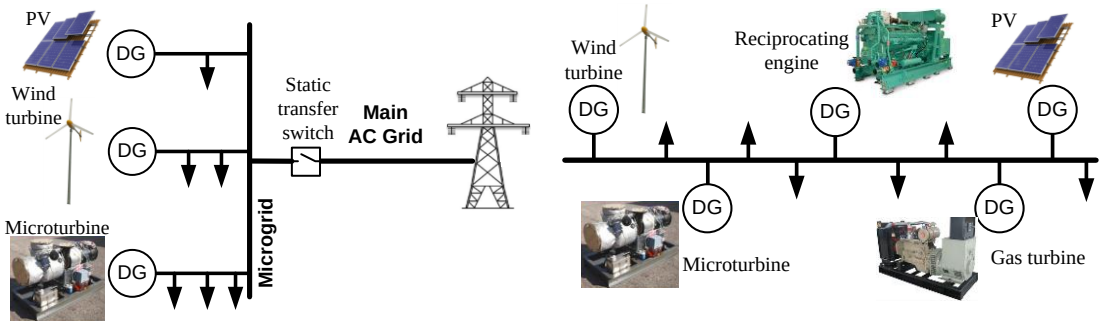
Microgrid is defined as a system that has at least one DG, energy storage devices and associated loads [1.36]. The individual DG equipped with a power electronic interface and controller is collectively called DG unit. Microgrid technology can offer improved service reliability, better economics, and reduced dependency on the local utility [1.37]. It can be classified into two categories, namely a grid connected microgrid and an isolated microgrid.

1.2.1 Grid connected microgrid

This type of microgrid is usually connected to the main grid (grid connected mode) through a static transfer switch as shown in Figure 1.2 (a). However under certain circumstances such as fault or disturbance occurrences in the main grid, it can be disconnected and operate in island mode. This disconnection stage is usually called the islanding process. Each mode has different control objectives. In the grid connected mode, each DG in the microgrid does not have to regulate the voltage of the system as this is done by the stiffer mains grid. In this mode, the DG has to inject appropriate currents and acts as sources of active and reactive powers. Within this mode, with a proper control, DG can provide ancillary services to the main power system, improve voltage and power quality supplied to local customers, and sustaining stable operation of the power system [1.2]. In contrast, in island mode, DGs are responsible for regulating the voltage and frequency in the microgrid and supply power to meet the local loads requirements with acceptable power quality.

1.2.2 Isolated microgrid

An isolated microgrid (also known as a remote microgrid) can be defined as a downsize version of a large scale utility grid. The typical isolated microgrid is shown in Figure 1.2 (b). DG in this microgrid has to regulate the voltage amplitude and frequency of the system and all load power demands have to be supplied by the DG. This standalone microgrid is suitable for supplying power to rural areas where power demand is relatively low and it is not cost effective to install transmission lines and supply the power from the main grid [1.38].



(a) (b)

Figure 1.2 Microgrid: (a) grid connected microgrid and (b) isolated microgrid.

1.3 Problem statement

The concept of DG has emerged as an alternative to conventional power systems due to the availability and technological advancement of different kinds of energy resources such as photovoltaic panels, fuel cells, and wind turbines [1.39]. With the advantages of this generation concept, it has become a regular choice for electric utility planners when catering for ever increasing load demands and for providing customers with a reliable power. DG is usually managed in a more decentralized way through the concept of a microgrid [1.36].

In microgrid control, system line impedance, whether inductive, resistive or a combination of both, plays an important role in determining the control approach since it affects the system power flow. Normally power flow analysis is based on inductive or resistive line impedance but few researchers consider power flow analysis with a complex line impedance. Control parameters are usually tuned for a specific microgrid configuration and line impedance condition. However it is more convenient to have robust control that can adapt to changes in line impedance and system parameters.

Most researches in the low voltage microgrid control area focus on improving the power quality (voltage and frequency regulation, harmonics, etc.) and power sharing. There is no interest in the power loss aspect as this is usually not significant and can be neglected. However with increasing DG power capacity and for applications such as rural isolated microgrids, where houses are located several miles from DG sources, power loss can be a significant problem. So it is interesting to explore the possibility of adapting a strategy in a microgrid control system that achieves good power sharing performance as well as minimizing the power loss.

1.4 Research objectives

In this research, power sharing aspects of parallel inverter operation in an island microgrid is investigated and the main research objectives are:

- To study the impact of line impedance on power sharing;
- To investigate the circulating current phenomenon in parallel inverter connection;
- To propose a control technique to improve power sharing performance; and
- To find an optimized power sharing ratio among parallel inverters to minimize transmission losses and improve load voltage regulation in rural islanded microgrid applications.

1.5 Scope of the research

In this research, the following assumptions are used:

- Stiff dc link
- Conventional two-level inverter topology
- Power device switching loss is neglected
- For three phase system, the loads are balanced.

1.6 Scope of thesis

The thesis is organized in 7 chapters

- Chapter 2 presents single and three phase inverter topologies. It also covers a detail literature review of existing control techniques proposed by researchers for standalone parallel connected inverters. The control techniques can be classified into two main categories: droop control and active load sharing.
- In Chapter 3, ac power flow analyses of an inverter system connected to a common ac bus through resistive, inductive and complex line impedances are investigated. For each line impedance case, the effect of the inverter's output voltage power angle and amplitude on active and reactive power flow are investigated. In the second part of the chapter, the circulating current phenomenon in a parallel inverter system is investigated.
- In Chapter 4 an improved instantaneous average current sharing controller is proposed for a single phase system. The gain scheduling technique is adapted in the proposed scheme.
- Chapter 5 presents a new control scheme that permits arbitrary power sharing between parallel connected inverters in a microgrid operating in island mode. The scheme processes the active and reactive output power information from all the inverters in a central controller that calculates the set-points for each inverter, based on the desired ratios of their output powers.
- In Chapter 6, the power sharing scheme proposed in Chapter 5 is expanded by adding a power ratio calculation that optimizes inverter operation of distributed generation in a rural isolated microgrid. Parallel connected inverters operation with the calculated power ratio ensures minimum transmission loss in an islanded microgrid.
- Chapter 7 presents the general conclusions and some recommendations for future research.

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Chapter 2

Inverter Configurations and Control Techniques

This chapter presents some inverter connected configurations and a detailed survey of various control techniques used for inverter parallel connection in a microgrid. For the inverter configuration, single and three phase inverter configurations are presented and their features are discussed. For the control techniques, a survey of different control techniques with and without a communication link and their advantages and disadvantages are discussed.

2.1 Inverter configurations

Inverter is a power switching device to convert a dc input voltage/current to an ac output voltage/current. The ac output voltage amplitude, phase and frequency can be fixed or variable [2.1].

2.1.1 Single-phase inverters

A typical single phase H-bridge voltage source inverter (VSI) is shown in Figure 2.1. It consists of four power semiconductor devices (with fast recovery diodes). With proper switching, $+V_{dc}$ and $-V_{dc}$ can be applied across the output terminals. This inverter configuration is suitable for uninterruptible power supply (UPS), static VAR compensator, active filter, and as an interface for small DG (solar panels, fuel cells, wind turbines, etc).

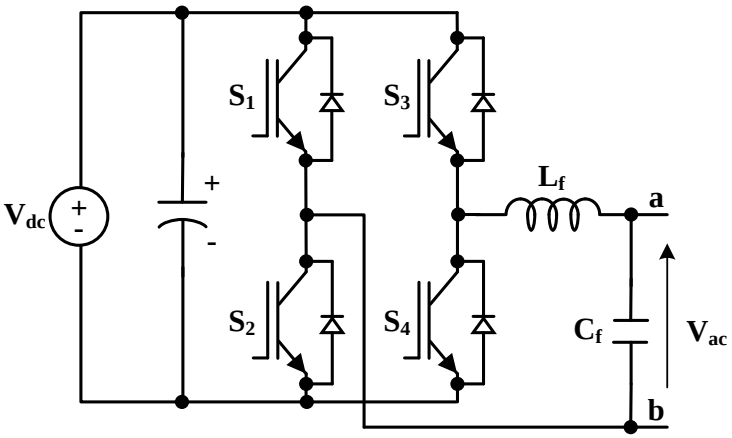


Figure 2.1 Single phase H-bridge inverter.

2.1.2 Three-phase inverters

A three phase VSI can be classified by the number of output terminals. Common three-phase inverter configurations used are as follows.

a) Three-phase three-wire configuration

The three-phase three-wire arrangement shown in Figure 2.2 (a) is the classical three-phase inverter configuration. It is suitable for applications such as adjustable speed drive, UPS and flexible alternating current transmission system (FACTS). For power system supply application such as on a low voltage distribution network that normally consists of single-phase loads, a neutral wire is required. In this case a Δ/Y transformer can be used. The transformer leakage inductance can function as filter inductance. The use of a transformer gives advantages in term of isolation from the main grid and the ability to block any dc component. However it is heavy, bulky and costly.

b) Three-phase four-wire – split dc configuration

The three-phase four-wire with a split dc source configuration [2.2-4] is shown in Figure 2.2 (b). The dc link capacitor is split into two capacitors and no inductor (for filtering) is needed in the neutral line as there is no neutral switching action. With this configuration, each phase can be controlled separately thus making current control easy. However there are two issues with this configuration, namely, first, unbalanced voltage of the two dc bus capacitors and second, voltage ripple due to currents flowing in the neutral line. Mid-point control schemes have been proposed in [2.4] to solve the first problem by adding a half-bridge chopper with PI or hysteresis current control to feed current to the mid-point of the split dc-bus. The second problem can be solved by using large capacitors but this is expensive.

c) Three-phase four-wire – four-legged inverter configuration

The four-leg inverter configuration is shown in Figure 2.2 (c). It utilizes two extra switches to accommodate the fourth wire. Three-dimensional space vector modulation [2.5, 6] and modified hysteresis current control [2.7] among others can be used to control this inverter configuration.

The addition of the two switches doubles the number of practical switching states (compared to normal space vector modulation) and increases current control complexity. This configuration also possess an electromagnetic compatibility problem as switching of the fourth wire produces voltage ripple across any parasitic capacitance, causing a common mode current [2.8]. The detail performance comparison of split dc capacitor and four-legged inverter configurations is presented in [2.9].

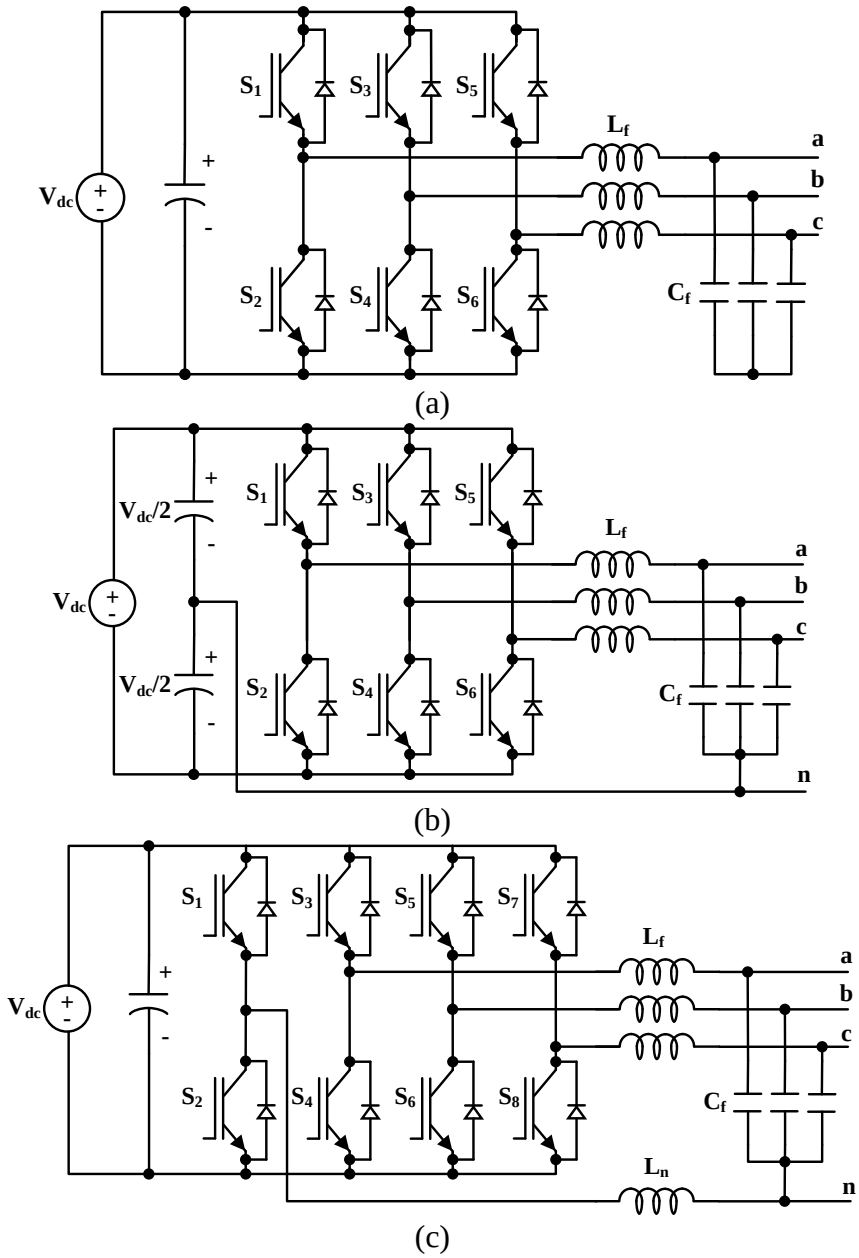


Figure 2.2 Three-phase inverter configurations: (a) three-phase three-wire, (b) three-phase four-wire split dc and (c) three-phase four-wire four-legged inverter.

2.2 Parallel connected inverter control for island mode operation

In island mode microgrid operation, the inverter main objectives are to regulate the microgrid voltage (amplitude and frequency) and supply the required current needed by arbitrarily varying loads. Another important control aspect is to ensure that the loads are shared properly between inverters while minimizing any circulating current in the system. In general, the control techniques for parallel operation of inverters can be divided into two categories: i) droop control techniques and ii) active load sharing techniques.

2.2.1 Droop control

A well-established control method is frequency and voltage droop [2.10, 11]. This technique tries to mimic the parallel operation of a large scale power system that droops the frequency of the ac generator when its output power increases. By using an inverter, the frequency and amplitude of the output voltage can be controlled independently. To achieve the required power sharing, the droop technique makes tight adjustments over the inverter output voltage frequency and amplitude, as a power-dependent function, to compensate for active and reactive power imbalance. Many researchers have focused on improving the droop control method for DG applications. They proposed modified droop [2.12-19], adaptive droop [2.20-25], combined droop [2.26-28], networked droop [2.29, 30] and hierarchical droop [2.31-34] control schemes. The droop techniques are summarized in Table 2.1, Table 2.2 and Table 2.3.

a) Conventional droop

Conventional droop control [2.10, 11] is deduced from the assumption of a purely inductive line impedance, *X*. The equivalent per-phase model of an inverter connected to point of common coupling (PCC) bus is shown in Figure 2.3 (a) while the phasor diagram is shown in Figure 2.3 (b). In an inductive system, the per-phase active and reactive powers (*P* and *Q*) injected to the PCC bus from the inverter are:

$$P = \frac{EV\sin\alpha}{X} \qquad Q = \frac{EV\cos\alpha - V^2}{X} \tag{2.1}$$

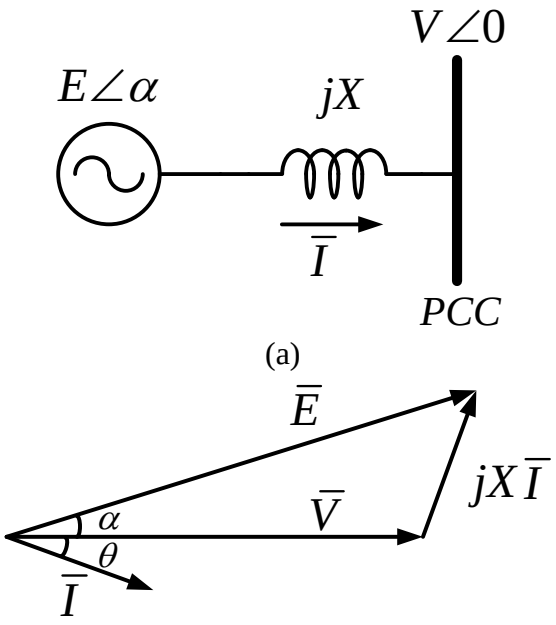


Figure 2.3 Inverter connected to PCC bus: (a) Equivalent per-phase model and (b) phasor diagram.

Based on (2.1), and with the assumption that the power angle α is very small (sin $\alpha \approx \alpha$ and cos α=1) active power injected from the inverter to the PCC bus is mainly influenced by α. On the other hand, the reactive power is mostly affected by the amplitude difference (*E*-*V*). The inverter output voltage phase can be changed indirectly by changing the output voltage frequency. Consequently, the frequency droop and output voltage droop can be used to control the inverter output power. The conventional droop control scheme block diagram is shown in Figure 2.4 (a). Figure 2.4 parts (b) and (c) show the *P*-ω droop and *Q*-*E* droop characteristics of two inverters with different power rating respectively. The droop characteristic for each inverter can be expressed as

$$\omega_i = \omega_o - m_i P_i \tag{2.2}$$

$$E_i = E_o - n_i Q_i \tag{2.3}$$

where P_i, Q_i, m_i and n_i are the actual active power output, actual reactive power output, frequency droop coefficient and voltage droop coefficient of i^{th} inverter respectively. ω_o and E_o are the rated frequency and rated voltage amplitude respectively.

The frequency and voltage droop coefficient are:

$$m_i = \frac{\Delta\omega}{P_{i\max}} \tag{2.4}$$

$$n_i = \frac{\Delta E}{Q_{i\max}} \tag{2.5}$$

where $P_{i\max}$, $Q_{i\max}$ are the maximum active and reactive powers that can be supplied by the i^{th} inverter and $\Delta\omega$ and ΔE are the maximum allowable output voltage frequency and amplitude deviation respectively.

It can be seen from Figure 2.4 parts (b) and (c) that, during steady state, which is the point when $\omega_1=\omega_2$ and $E_1=E_2$, inverter 1 supplies P_1 and Q_1 while inverter 2 supplies P_2 and Q_2. When the droop coefficients are increased, good power sharing can be achieved but at the expense of poor voltage regulation. So during the design process, a trade-off occurs when selecting a droop coefficient value.

The main advantage of the droop technique is no communication among parallel connected inverters is required thereby making it highly modular and reliable. However, there are several disadvantages of the conventional droop technique, such as:

- Load dependent frequency and amplitude deviations that induce poor performance in load voltage regulation
- Impedance mismatch will affect *P* and *Q* sharing
- Poor transient and hot swap performance

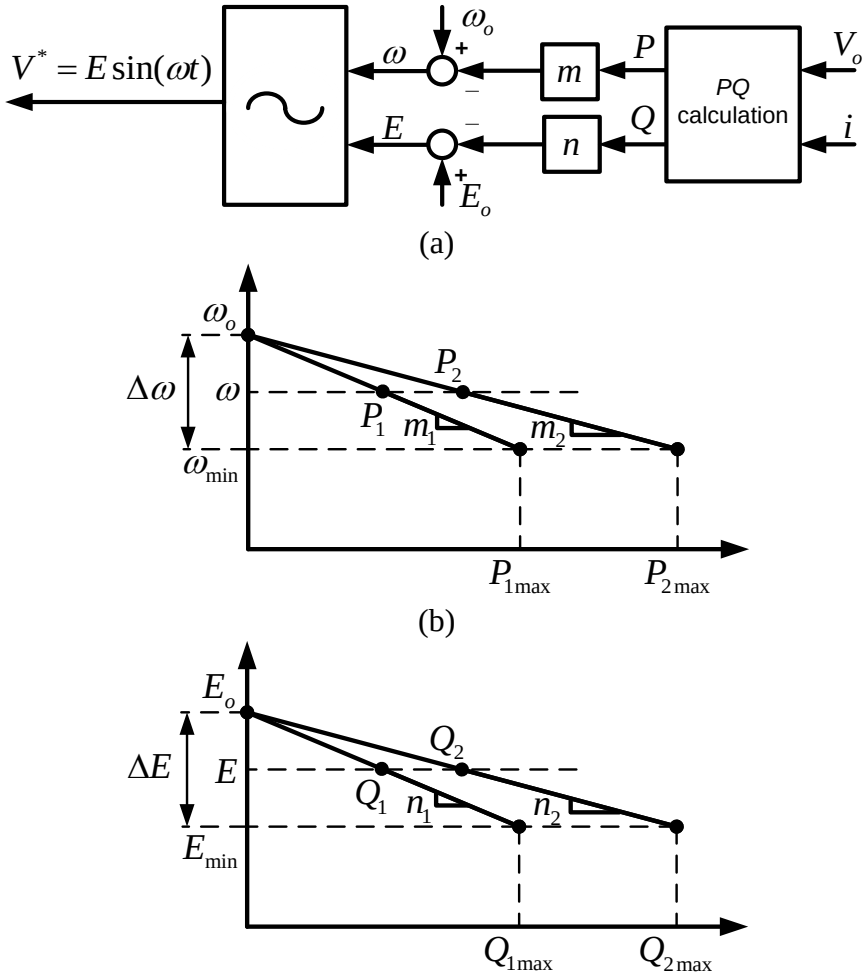


Figure 2.4 Conventional droop control scheme: (a) block diagram, (b) *P*-ω droop and (c) *Q*-*E* droop.

b) Modified droop

In order to enhance the dynamic performance of parallel connected inverters in DG systems, the authors in [2.12] proposed modified droop control by adding a supplemental transient droop characteristic to the conventional static droop approach. This technique is able to achieve good transient performance. However it is difficult to select a suitable coefficient for the derivative term in the supplemental droop equation. Droop control for resistive line impedance that uses *P*-*E* and *Q*-ω droops is presented in [2.13]. Angle droop instead of frequency droop was used in [2.14, 15]. This technique has better frequency regulation than the conventional droop technique. In [2.16], a modification of the droop equation and the addition of virtual

complex impedance to consider the effect of complex line impedance, has been presented. This technique achieves good current sharing and minimizes fundamental and harmonic circulating currents but *Q* sharing was not presented. Droop control with a derivative controller has been used [2.17]. It enhances power loop dynamics but simulation and experimentation do not consider transient cases. The authors in [2.18] proposed a modified droop equation by subtracting the rms of the measured voltage from the voltage set point. This technique compensates voltage drop due to the load and the droop effect. In [2.19], *Q* versus time rate of change of *V* droop with a voltage restoration function is proposed. It improves voltage amplitude regulation and *Q* sharing. Block diagrams for some modified droop controllers are shown in Figure 2.5.

c) Adaptive droop

Several authors have proposed droop techniques with droop parameters that can be changed adaptively with operating conditions. In [2.20], the authors presented a static droop characteristic with an adaptive transient droop function that ensures active damping of power oscillations at different operating conditions. However, it was not verified experimentally. An impedance voltage drop estimation function with online reactive power offset estimation has been proposed in [2.21] which yield good *P* and *Q* sharing. But this strategy is complicated and sensitive to parameter tolerance. The authors in [2.22] proposed an algorithm to modify the droop constant based on the operating conditions. This technique is able to improve active power sharing but reactive power sharing performance was not presented. In [2.23], control parameters are adjusted to compromise between reactive power sharing and voltage regulation at the load buses. The optimal droop constants were predetermined by solving a system specific optimization problem. The same optimization based technique is presented in [2.24]. It selects optimized droop coefficients that are derived from the analysis of a small signal model. This technique yields stable microgrid operation but *P* and *Q* sharing performance is not presented. In [2.25], bifurcation theory is used in scheduling the droop parameters to improve voltage and frequency regulation. It produces stable operation in some cases but no hardware verification was presented.

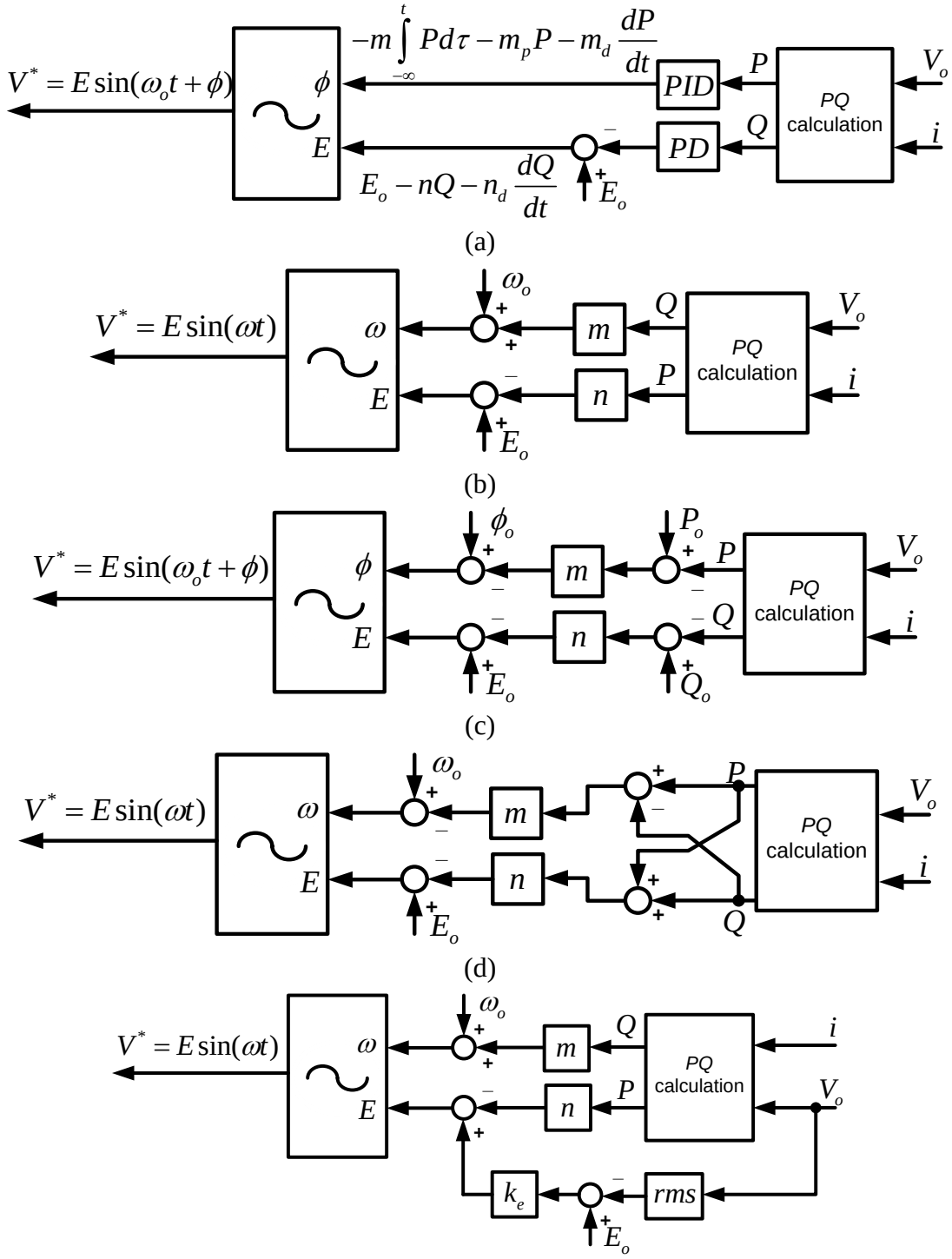


Figure 2.5 Modified droop control: (a) supplemental transient droop [2.12], (b) droop for resistive line impedance [2.13], (c) angle droop [2.14, 15], (d) complex line impedance droop [2.16], and (e) robust droop [2.18].

d) Combined droop

Several authors have proposed a combination of droop techniques with other techniques to improve performance. The authors in [2.26] combined the droop method and an average power control method. This technique requires low bandwidth communications but is able to improve the load sharing capability. In [2.27], particle swarm optimization (PSO) was used to optimize the droop constant and a robust controller with a double-layer PSO algorithm has been proposed for output voltage control. This technique yields good *P* and *Q* sharing but no hardware implementation was presented. The droop technique has been combined with an unbalance compensator in [2.28]. It produces good voltage unbalance compensation and compensation effort is properly shared between DGs but its implementation is complex.

e) Networked droop

Some droop techniques use network communication to share information among parallel connected inverters to improve the performance of conventional droop control. In [2.29], the authors proposed an improved angle droop technique that uses web-based low bandwidth communications (shown in Figure 2.6 (a)) to share power angle information between all inverters in the microgrid. The power angle information from other inverters is used in making adjustments to each inverter's droop equation. This technique achieves good *P* sharing but *Q* sharing performance was not presented. The authors in [2.30] proposed the addition of a weighted power function with networked data, to conventional droop (shown in Figure 2.6 (b)) to improve power sharing. The first inverter sends its active and reactive powers to a slave inverter through a communication area network (CAN) bus. The second inverter processes this power information together with its own active and reactive powers to get weighted powers before being used by the droop controller. The authors claimed that this technique has superior load sharing performance compared to a droop-only method but no *P* or *Q* plots were presented as verification.

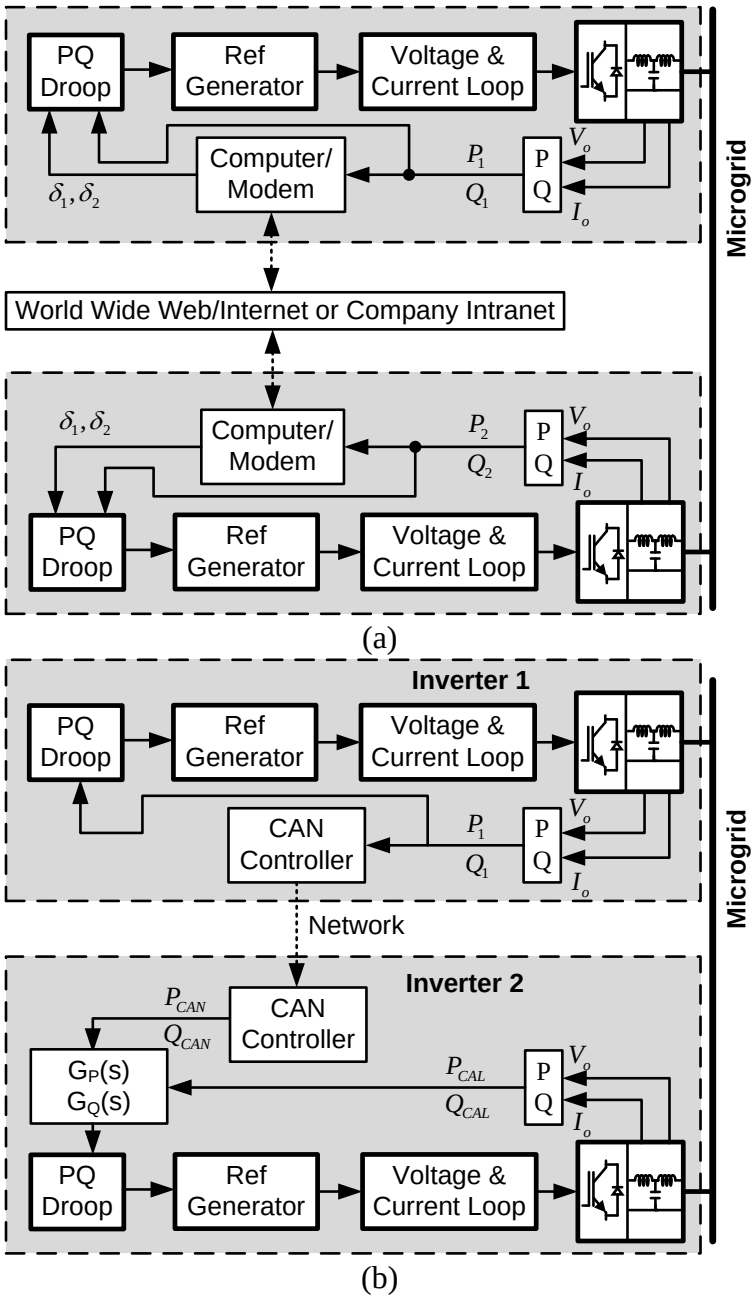
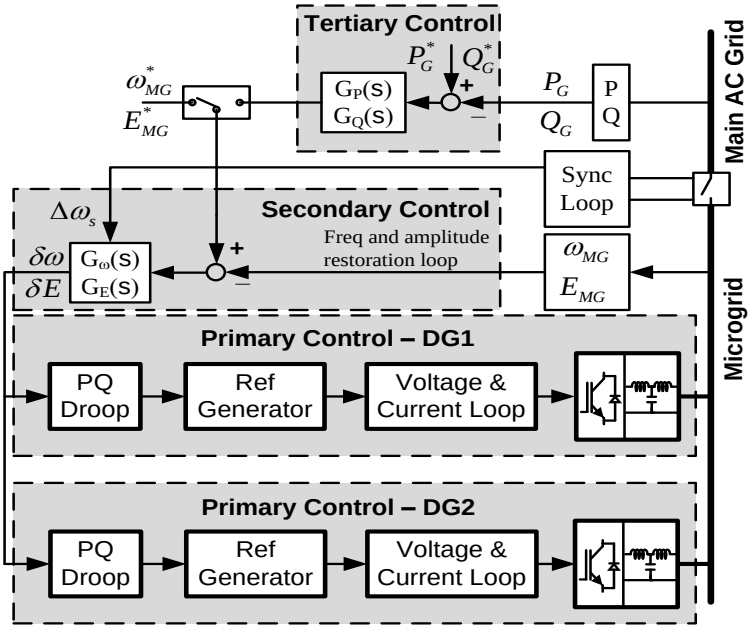


Figure 2.6 Networked droop (a) web based networked droop [2.29] and (b) weighted power function with networked data [2.30].

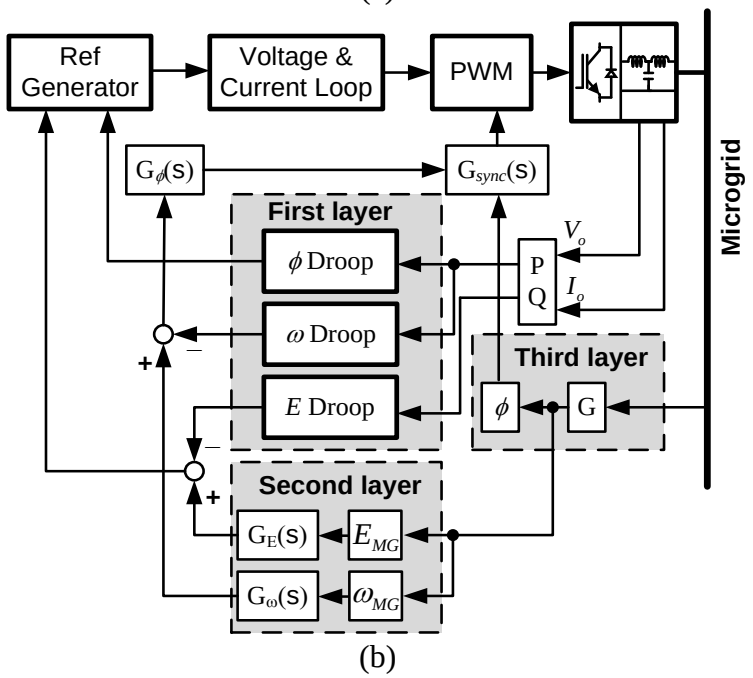
f) Hierarchical droop

Droop techniques with hierarchical control have been proposed by several authors to improve power sharing and voltage regulation of the conventional droop technique. Local output voltage with power droop control is usually implemented as the first layer. In [2.31], secondary and tertiary controls were introduced to bring the deviated

voltage and frequency back to rated values and control the power flow respectively. This technique can be used both in ac and dc microgrids and produces good power sharing and voltage regulation. Communication is required between each inverter and the secondary controller. A block diagram for this controller is shown in Figure 2.7 (a).



(a)



(b)

Figure 2.7 Hierarchical droop (a) hierarchical control presented in [2.31] and (b) three layer control technique [2.32].

Three layer control is also proposed in [2.32]. Droop control is used in the first layer and a voltage deviation compensation function is used by second layer. Third layer is quasi-synchronization which ensures the inverter's voltage angle is close to that at the PCC. This technique requires measurement of the microgrid voltage for the second and third layers. It produces good *P* sharing with improved voltage regulation. However *Q* sharing performance was not presented. A block diagram for this controller is shown in Figure 2.7 (b). In [2.33], secondary control was applied to manage compensation of load bus voltage unbalance and harmonics, by sending proper control signals to the primary level. It enhances voltage quality and improves load sharing performance however it is not verified experimentally. Two layer control is been presented in [2.34]. Secondary control restores the frequency and amplitude deviations produced by the primary control (droop control). Low bandwidth communication is required between the secondary controller and each inverter. This technique achieves good power sharing performance with improved voltage amplitude and frequency regulation.

2.2.2 Active load sharing techniques

To achieve proper current sharing and voltage regulation in a parallel inverter connected system, some information is shared between the parallel connected inverters. The second kind of control scheme, collectively named active load sharing scheme, utilizes communication among parallel inverter modules [2.35]. These schemes employ different mechanisms to share information among the inverters. The reported active load sharing techniques can be classified as: master slave control [2.36-43], circular chain control [2.44, 45], centralized control [2.46], average current sharing control [2.47-52], and average power sharing control [2.53]. Most of these control techniques are used in UPS application but some can be applied to DG applications. The characteristics, advantages and disadvantages of these control techniques are summarized in Table 2.4 and Table 2.5.

a) Master slave control [2.36-39, 41-43]

In master slave control (shown in Figure 2.8), the master inverter regulates the voltage and frequency and other inverters become slaves. In other words, the master module acts as a voltage source while the slaves operate as current sources. In general, this control technique achieves good current sharing and stability. There are some variants to this control technique, which depend on the selection of the master module. In a dedicated scheme, one fixed module is selected as the master unit. There is also a rotating scheme in which the master is arbitrary chosen. In another variant, the module that produces maximum rms current is selected as the master module [2.35].

In [2.36], the reference current for slave inverter was source from the power distribution centre while in [2.37], output current from the master module was used as reference current for the slave module. The authors in [2.38] introduced a phase control algorithm into the conventional master slave technique to enable precise current sharing even if the modules have different ratings. *P* and *Q* share buses that are driven by the inverter that has the highest output power (master inverter), was proposed in [2.39]. In this approach, slave inverters calculate the difference between their output power and the power in the shared buses and make adjustments in the output voltage frequency and amplitude. Another variant of the master control strategy is current limitation control [2.40]. In this technique, there is a master module that controls the load voltage and the slave modules only supply and share the load current with the master module. A slave module receives a reference current command from the previous module which has limited amplitude, resulting in non-sinusoidal output current from each inverter.

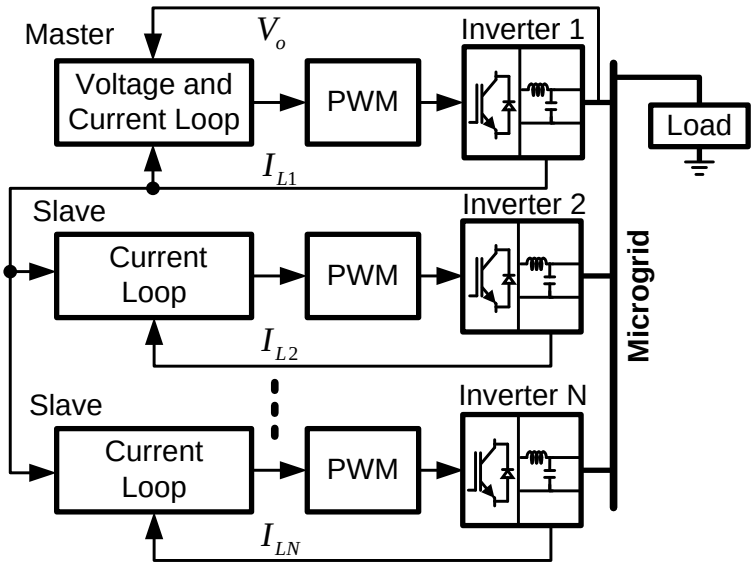


Figure 2.8 Master slave control technique.

b) Circular chain control (3C) [2.44, 45]

In the 3C technique (shown in Figure 2.9) [2.44, 45], successive inverter modules track the current of the previous inverter to achieve equal current distribution. The first module tracks the last to form a circular chain connection. Each inverter regulates its output voltage based on the common reference voltage. However a problem occurs when there is a damaged or failed inverter in the loop. If this is not detected and isolated quickly, it will impact the performance of the overall system and in the worst case, can cause total system failure. Two lines are usually used for communication to achieve bidirectional communication and to increase reliability.

c) Centralized control [2.46]

In this technique (shown in Figure 2.10), the central controller regulates the load voltage in an outer loop and sends reference current to each inverter. The reference current is determined by adding the output of voltage controller and the average load current (total load current divide by number of inverters). The current controller in each inverter processes the difference between the reference current and its output current. This control technique produces excellent current sharing but lacks reliability and redundancy. The need to measure load current renders this control unsuitable for system with distributed loads.

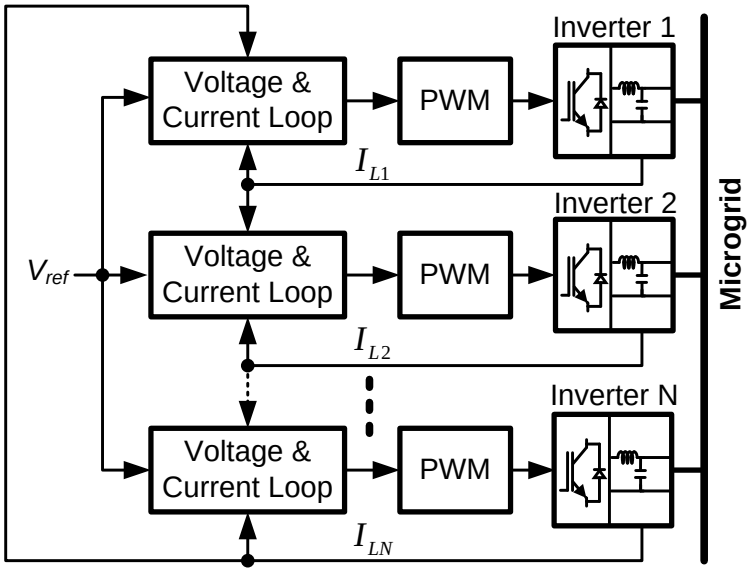


Figure 2.9 3C control technique.

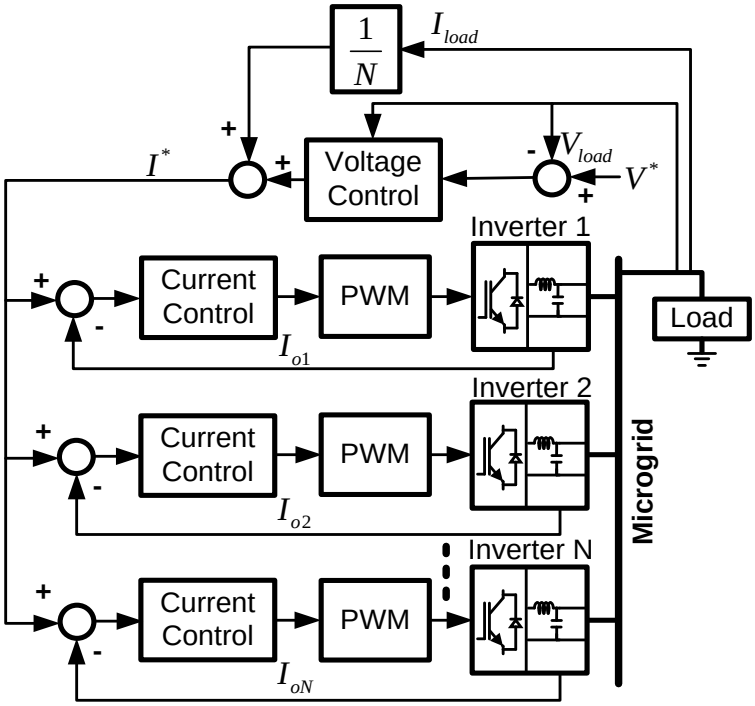


Figure 2.10 Centralized control technique.

d) Average current sharing control [2.47-52]

This control technique uses the same concept that is applied to parallel connected dc/dc converters. A common current bus with the system average current information, is used. The average current is computed by connecting this current bus to the current sensor of each inverter through a resistor. The central controller can also be used to calculate the average current values before transmitting to each inverter. The average

current is used as reference for each inverter and the current control can be implemented either within the inner or outer current loops. In this technique, all the inverters in the microgrid take part in the voltage, frequency, as well as the current regulation, demonstrating the democratic nature of this controller. The control diagram is shown in Figure 2.11.

Instantaneous output voltage control with current deviation and current deviation cancellation control utilizing a current share bus, were introduced in [2.47]. Robust voltage and current controllers were used in [2.48] to improve voltage regulation and current sharing performance. In [2.49], average current sharing was realized through three shared buses (inverter reference, sensed load current, and feedback voltage) interconnecting all the paralleled modules. It produces a fast dynamic response but with the addition of an extra communication bus. A multi-inverter system with an instantaneous average current sharing scheme was modelled in [2.50] by introducing a disturbance source to represent all the sources that may cause current imbalance.

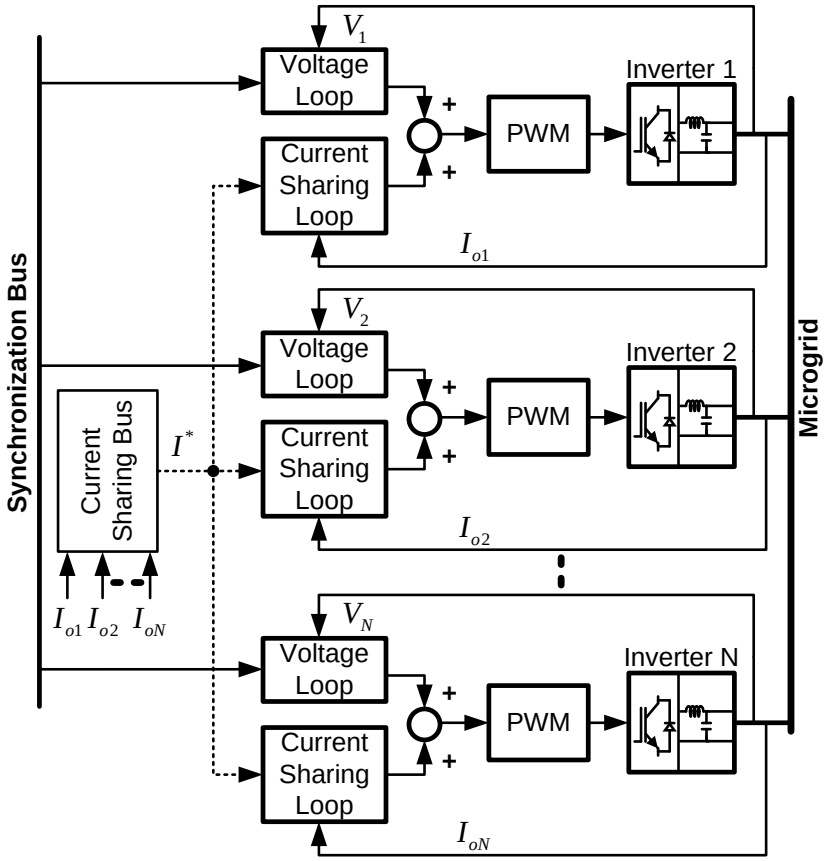


Figure 2.11 Average current sharing control technique.

In [2.51], a sinusoidal reference voltage was digitally generated through a synchronous square-wave signal shared among all the modules in parallel operation. Current sharing control was realized in an analogue manner by means of applying its circulating current to adjust its reference voltage. The authors in [2.52] introduced a compensation strategy to conventional average current sharing, by feeding back the reference current of each inverter. This approach improves the weighted current distribution among inverters and all inverters share the load based on their rating.

e) Average power sharing control [2.53]

This technique is similar to average current sharing but in this technique, the averaged *P* information is used instead of current. Hence only low bandwidth communication is required compared to high bandwidth communication used in average current sharing. Each inverter unit controls their output *P* sharing using an active power regulator and *Q* sharing is achieved through phase locked loop control. This technique achieves good power sharing performance but is only suitable for a balanced system.

Table 2.1 Conventional and modified droop techniques

Control techniques	Concept	Advantages	Disadvantages	Ref	Year
Conventional droop	• *P*-ω and *Q*-*E* droop	• No communication • High modularity • Good reliability	• Load dependent frequency and amplitude deviations that induce poor performance in load voltage regulation • Impedance mismatch will affect P and Q sharing • Only based on predominantly inductive line impedance. • Poor transient and hot swap performance	[2.10]	1988
				[2.11]	1993
Modified droop	• Power derivative integral term is introduced to the conventional droop equation to improve the transient response	• Fast transient response	• Difficult to select the suitable coefficients for derivative term that ensures stable operation	[2.12]	2004
	• Droop control for resistive output impedance	• Good active power sharing performance	• *Q* sharing is not presented	[2.13]	2007
	• Angle droop	• Good frequency regulation	• *Q* sharing is not presented	[2.14]	2009
	• Angle droop • A supplementary loop is proposed around the conventional droop control of each DG converter to stabilize the system and ensure satisfactory load sharing	• Stabilizes the operation for the droop control that have high gain	• Only cater for a specified range of operation	[2.15]	2010
	• Modification of droop equation and addition of virtual complex impedance to consider the effect of complex line impedance.	• Good current sharing • Minimizes fundamental and harmonic circulating currents	• *Q* sharing is not presented	[2.16]	2010
	• Droop control with derivative controller is used	• Enhance power loop dynamics	• Simulation and experiment do not cover transient cases	[2.17]	2011
	• Droop equation is modified by deducting rms of measured voltage value to the voltage set point	• Able to compensate voltage drop due to load and droop effect	• Poor *Q* sharing performance	[2.18]	2013
	• Q vs time rate of change of V droop with voltage restoration function	• Improved reactive power sharing	• Difficult to determine restoration gain to achieve stable operation	[2.19]	2013

Table 2.2 Adaptive and combined droop techniques

Control techniques	Concept	Advantages	Disadvantages	Ref	Year
Adaptive droop	• Combine static droop characteristics with an adaptive transient droop function	• Active damping of power oscillations	• Authors did not present experimental validation of this technique	[2.20]	2008
	• Introduces the impedance voltage drops estimation function and employs online reactive power offset estimation	• Good *P* and *Q* sharing	• This strategy is complicated and sensitive to parameter tolerance	[2.21]	2009
	• Algorithm to modify droop constant based on operating condition.	• Improve active power sharing performance	• *Q* sharing performance is not presented • Improvement is not significant	[2.22]	2010
	• Adaptive voltage droop scheme • Droop parameters are determined by two methods, i) trade-off between *Q* sharing and voltage regulation and ii) solving optimization problems	• Improve decoupling between *P* and *Q* • Improve *Q* sharing under several line impedance conditions	• Complicated • Can only cater for a specified range of operation	[2.23]	2010
	• Selection of droop parameters from set of optimized droop coefficients that are determined based on the analysis of small signal model	• Stable microgrid operation under several operational conditions	• Only for limited case (not robust) • *P* and *Q* sharing performance are not presented	[2.24]	2008
	• Bifurcation theory is used in scheduling the droop parameters to improve voltage and frequency regulation	• Stable operation under certain cases	• Limited cases presented • Complicated	[2.25]	2010
Combined droop	• Combined droop method and average power control method that require a low bandwidth communication	• Improved load sharing capability	• Need communication	[2.26]	2004
	• Particle swarm optimization is used to optimize the droop constant. *L1* robust control theory with the double-layer PSO algorithm has been proposed for output voltage control.	• Good active and reactive power sharing	• Complicated	[2.27]	2010
	• Unbalance compensator is added	• Good compensation of voltage unbalance • Compensation effort is properly shared between DGs	• Complicated	[2.28]	2013

Table 2.3 Networked and hierarchical droop techniques

Control techniques	Concept	Advantages	Disadvantages	Ref	Year
Networked droop	• Improved droop technique that uses web-based low bandwidth communication	• Good active power sharing	• Require communication • *Q* sharing performance is not presented	[2.29]	2010
	• Weighting power function is added to conventional droop to improve power sharing	• Improve load sharing error	• Require communication • Performance under impedance mismatch is unknown • *P* and *Q* sharing performance are not analysed properly.	[2.30]	2012
Hierarchical droop	• Secondary control and tertiary control are introduced to bring the deviated voltage and frequency back to the rated values and control the power flow respectively.	• Good power sharing and voltage regulation • Standardized for ac and dc microgrid	• Need communication • *Q* sharing performance is unknown	[2.31]	2011
	• Multilayer droop control • 1st layer – introduce power proportional term to conventional droop • 2nd layer – compensate voltage deviation • 3rd layer – quasi-synchronization to ensure the angle of inverter is close to PCC	• Good *P* sharing • Improve voltage regulation	• *Q* sharing performance is unknown	[2.32]	2012
	• Secondary control is applied to manage the compensation of sensitive load bus voltage unbalance and harmonics by sending proper control signals to the primary level	• Enhance voltage quality • Improve load sharing performance	• Need communication	[2.33]	2012
	• Secondary control restores the frequency and amplitude deviations produced by the primary control.	• Good power sharing • Improved voltage amplitude and frequency regulation	• Need communication	[2.34]	2013

Table 2.4 3C, centralized and master slave control techniques

Control techniques	Concept	Advantages	Disadvantages	Ref	Year
Master slave	• Master module acts as a voltage source inverter while the slaves operate as a current source inverters • Reference current for slave inverter is given by power distribution centre.	• Good current sharing capability and stability	• Total system failure can occur if communication fail	[2.36]	1995
	• Output current from master module is used as reference current for slave module. • All inverters can be selected as master module and the selection of master module is made through via a single common status line	• Good current sharing capability and stability • Automatic selection of master module in case 1 inverter fails.	• Only suitable for inverters that have equal parameters	[2.37]	1998
	• Phase control algorithm is introduce to conventional master slave technique to enable precise current sharing even if the modules have different rating	• Load current can still be supplied from slave inverter even if the master inverter fails.	• Linear load only results are not presented so current sharing performance cannot be verified	[2.38]	2004
	• Employ *P* and *Q* share buses that is driven by the inverter that have the highest output power (master inverter). • Slave inverters calculate the difference between their output power and power in the share buses and make adjustment in the output voltage frequency and amplitude	• Fast dynamic response and precise load sharing	• PI controller in power loops may cause instability to the overall system.	[2.39]	2004
	• There is a master module that controls the load voltage and the slave modules will only supply the load current. A slave module will receive reference current command from the previous module which has limited amplitude.	• Stable voltage regulation	• Total system failure can occur if communication fail • Output current is not sinusoidal	[2.40]	2004
	• Central command generates references for different DGs based on sensed voltage and current at different nodes	• Current is shared based on rating • Fast transient dynamics • Improve power quality	• Power sharing ratio is changing with load	[2.41]	2012
	• New communication platform for master slave architecture utilizing the communicating function of DSP and human machine interface on main devices	• Improved energy management system	• Increase in complexity	[2.42]	2012
	• Master slave method without any communication link between DGs and loads. • Current at PCC of each inverter is sensed, transformed to dq frame, applied appropriate gain and reverted back to abc frame to become a reference current for that particular inverter.	• No communication among inverters • Current is shared based on rating	• Power sharing ratio is changing with load	[2.43]	2012
3C	• Circular chain connection is used to connect all modules and each module has an inner current loop control to track the inductor current of its previous module	• Good current sharing performance	• Total system failure can occur if communication fail	[2.44]	2000
				[2.45]	2007
Centralized	• Central controller regulates the load voltage using outer loop and sends current reference to each inverter. Reference current is determined by dividing the total load with number of parallel inverters	• Good current sharing performance	• Only suitable for inverter and load that are located nearby.	[2.46]	2003

Table 2.5 Average current sharing and average power sharing control techniques

Control techniques	Concept	Advantages	Disadvantages	Ref	Year
Average current sharing	• Instantaneous output voltage control with the current deviation and current deviation cancellation control utilizing the current share bus circuit.	• Good current sharing performance	• Total system failure can occur if communication fail	[2.47]	1998
	• averaged current-sharing control with robust voltage and current controllers	• Fast dynamic response • Equal current distribution		[2.48]	2001
	• Average current method is realized through 3 share buses (inverter reference, sensed load current and feedback voltage) interconnecting all the paralleled modules without extra control modules.	• Fast dynamic response and equal load current sharing	• Too many share buses • Total system failure can occur if communication fail	[2.49]	2002
	• Multi-inverter system with instantaneous average-current-sharing scheme is modelled by introducing a disturbance source to represent all the sources that may cause current unbalances	• Good theoretical prediction of real system	• Current dynamic is relatively slow because its bandwidth is limited by the voltage loop	[2.50]	2003
	• Sinusoidal reference voltage is generated in digital manner through a sharing synchronous square-wave signal among all the modules in parallel operation. • Current sharing control is realized in analog manner by means of applying its circulating current to adjust its reference voltage	• Good current sharing	• Transient performance is not presented.	[2.51]	2004
	• A compensation strategy is added to conventional average current sharing • Reference current of each inverter is fed back as a compensation signal to improve weighting current distribution	• All inverters share the linear or nonlinear load based on their rating	• Total system failure can occur if communication fail	[2.52]	2005
Average Power Sharing	• Active power bus is used instead of instantaneous current bus.	• Good power sharing performance	• Only good for balanced system • Total system failure can occur if communication fail	[2.53]	2003

2.3 Summary

In this chapter, single and three phase inverter configurations have been presented. Their characteristics, applications, advantages and disadvantages were briefly discussed. The second part of the chapter reviewed control of parallel connected inverters used in islanded microgrid. The control techniques are divided into two categories: i) droop and ii) active load sharing control. Based on research trends, most researchers favour and focuses on droop control techniques as they have advantages in terms of flexibility due to lack of communication among parallel inverters. However, due to advancements in the communications infrastructure, there is also potential for some active load sharing techniques to be expanded and improved. Considering this fact, and having advantages in term of producing good voltage regulation and current sharing performance, average current sharing is selected to be improved in a single phase microgrid application (chapter 4). For three phase microgrid application for a larger system, where DGs are located far from each other, average current sharing is not suitable as it requires high bandwidth communication. So an average power sharing technique is more suitable and has been selected to be used in three phase microgrid in chapters 5 and 6.

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Chapter 3

AC Power Flow Analysis and Circulating Current among Parallel Connected Inverters

In this chapter, ac power flow analysis of an inverter based system connected to a common ac bus through purely resistive, inductive or complex line impedances is investigated. For each line impedance case, the effect of an inverter's output voltage power angle and amplitude on the active and reactive power flow are studied. Several active and reactive powers plots are generated to visualize the impact of line impedance on the power flow in an AC system. In the second part of the chapter, the circulating current phenomenon in a parallel connected inverter system is analysed. Circulating currents for multiple parallel connected inverters are defined and simulations allow investigation of circulating current due to voltage phase, amplitude and frequency imbalance.

3.1 AC power flow analysis, accounting for the effects of line impedance

Line impedance is an important factor when implementing a control technique for an inverter for microgrid operation, whether it is operating in grid connected or island mode. At high and medium voltage levels, line impedance is highly inductive but at a lower voltage level, line impedance is considered approximately resistive but sometimes can be complex [3.1]. Line impedance determines the inverter control strategy as the active and reactive powers flow depend on this parameter [3.2].

The equivalent per-phase model of an inverter connected to PCC bus is shown in Figure 3.1. Complex power injected by an inverter to the PCC bus is given by

$$S = P + jQ \tag{3.1}$$

where P is the active power and Q is the reactive power, defined as

$$P = \frac{EV}{Z}\cos(\theta - \alpha) - \frac{V^2}{Z}\cos\theta \qquad Q = \frac{EV}{Z}\sin(\theta - \alpha) - \frac{V^2}{Z}\sin\theta \tag{3.2}$$

where E is the inverter output voltage amplitude measured at the filtered bus, V is the point of common coupling bus voltage amplitude, and α is the power angle. Z and θ are the magnitude and phase of the overall system impedance respectively, which consist of resistance and inductive reactance, R and $j\omega L$.

3.1.1 Purely inductive line impedance

For an inductive line impedance system, which is normally associated with medium and high power lines or a low voltage line with relatively large output inductance, it can be assumed that the line resistance is negligible (Z=X and θ = 90^o) and the equations in (3.2) reduced to:

$$P = \frac{EV\sin\alpha}{X} \qquad Q = \frac{EV\cos\alpha - V^2}{X} \tag{3.3}$$

Based on (3.3), and with the assumption that the power angle α is very small ($\sin\alpha \approx \alpha$ and $\cos\alpha$=1) active power and reactive power injected to the PCC bus is mainly influenced by α and amplitude difference (E-V) respectively.

Figure 3.2 shows the active and reactive power plots for different voltage levels with purely inductive line impedance (R=0 Ω and X=0.3 Ω). Active and reactive power plots when E = V and α is varied are shown in Figure 3.2 parts (a), (b) and (c) while the plots when α is fixed at 0 and E is varied, are shown in Figure 3.2 parts (d), (e) and (f). From Figure 3.2 (a), inverter active power output increases as α increases and vice versa. Figure 3.2 (b) shows that at α = 0, reactive power is 0 and when α becomes more +ve or –ve, the reactive power from the inverter decreases. The rate of active and reactive power change increase when the voltage level increases. Both the active and reactive power plots are combined and shown in Figure 3.2 (c). From this figure, with purely inductive line impedance, the variation of α has more effect on the active power than the reactive power.

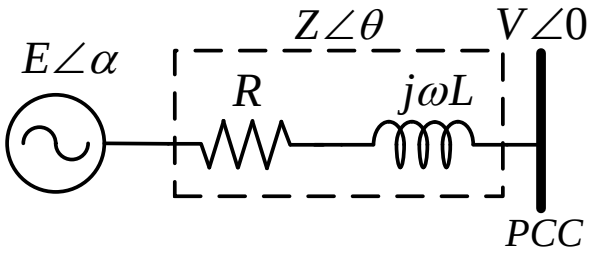


Figure 3.1 Equivalent per-phase model of an inverter connected to PCC bus

Figure 3.2 (d) shows when α is fixed at 0, changing E will not affect the active power. In Figure 3.2 (e), reactive power coming from the inverter increases as E increases and vice versa. Figure 3.2 (f) compares both active and reactive power plots with varying E, on the same plot.

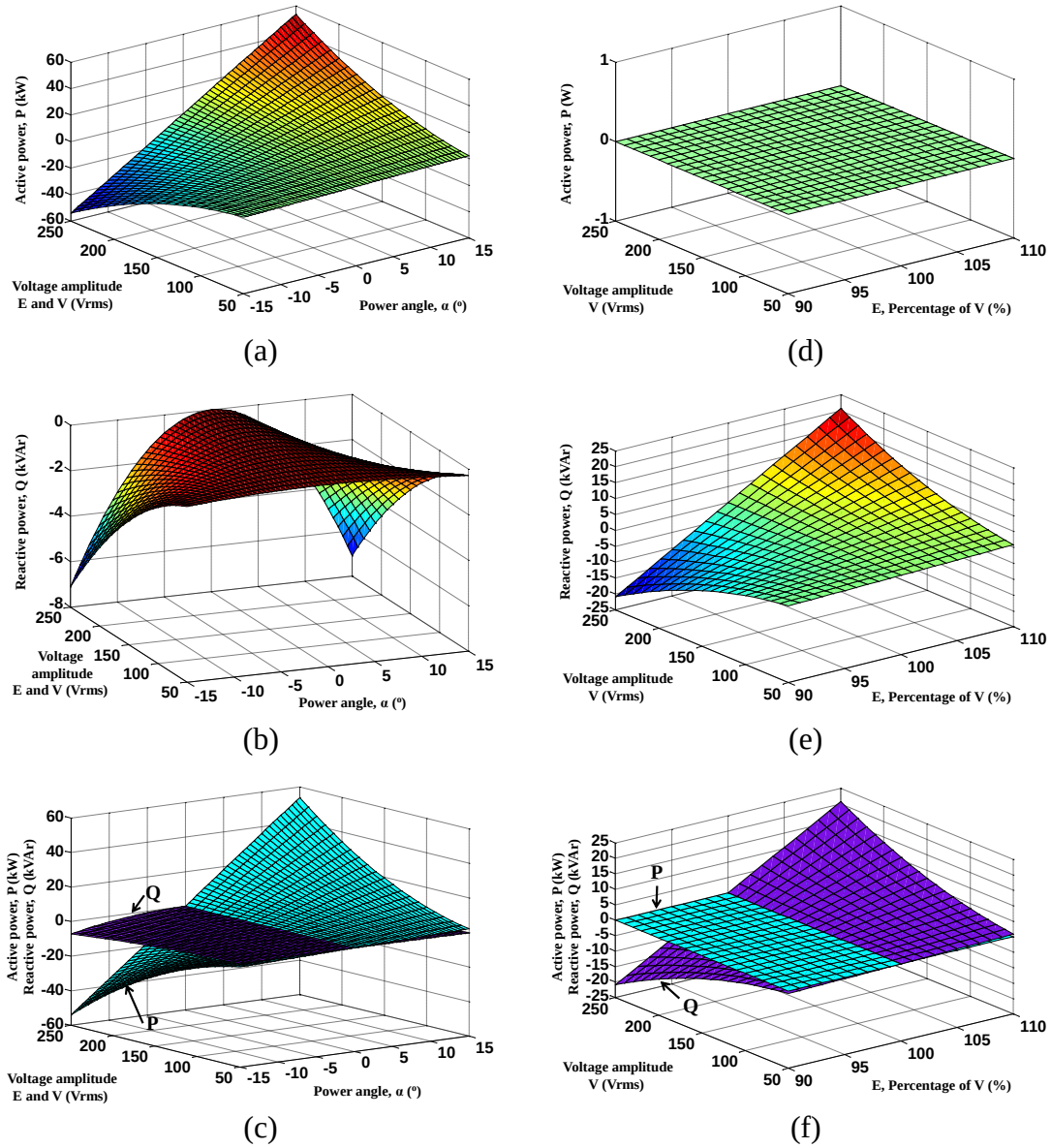
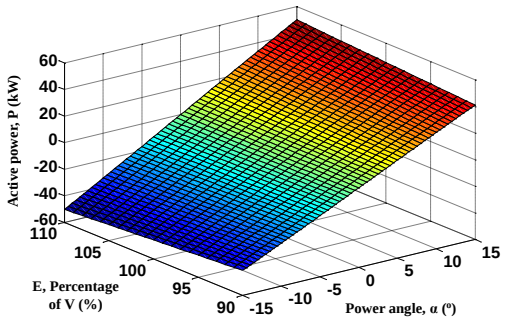
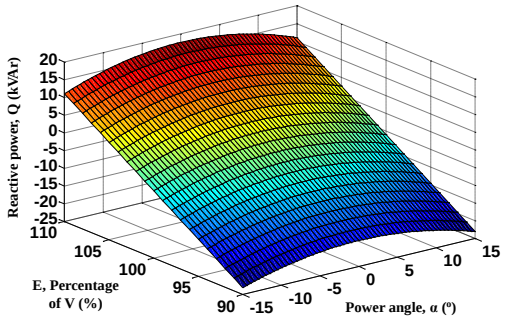


Figure 3.2 *P* and *Q* plots for different voltage levels under purely inductive line impedance (R=0 Ω and X=0.3 Ω): (a) *P* with fixed *E* and varying α; (b) *Q* with fixed *E* and varying α; (c) *P* and *Q* with fixed *E* and varying α; (d) *P* with $\alpha=0$ and varying *E*; (e) *Q* with $\alpha=0$ and varying *E* and (f) *P* and *Q* with $\alpha=0$ and varying *E*.

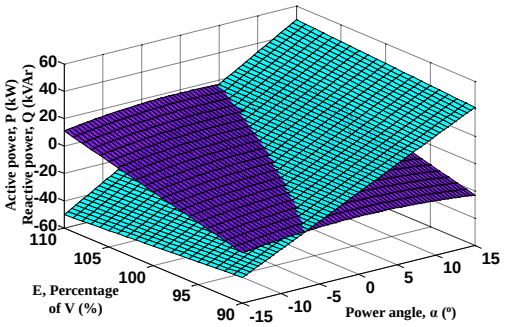
Figure 3.3 shows the active and reactive power plots with a purely inductive line impedance and V=230V with varying E and α. For all value of E, the active power increases as α increases and vice versa, as shown in Figure 3.3 (a). In Figure 3.3 (b), for all values of E, the reactive power follows a bell shaped curve as α increases from -15º to 15º and the magnitude of the reactive power increases as E increases. For comparison, both plots are combined in Figure 3.3 (c).



(a)



(b)



(c)

Figure 3.3 P and Q plots under purely inductive line impedance (R=0 Ω and X=0.3 Ω) and V=230V with varying E and α: (a) P (b) Q; and (c) P and Q.

3.1.2 Purely resistive line impedance

For a resistive system, which is common in low voltage power cables, the inductive reactance is negligible compared to resistance (hence, $Z=R$ and $\theta = 0^o$) and the equations in (3.2) become:

$$P = \frac{EV\cos(\alpha) - V^2}{R} \qquad Q = \frac{-EV\sin\alpha}{R} \tag{3.4}$$

From (3.4) and with very small α, the active and reactive powers are mostly affected by amplitude difference (E-V) and α respectively, which are the reverse for inductive dominated systems. Figure 3.4 shows the active and reactive powers plots for different voltage levels for purely resistive line impedance (R=0.3 Ω and X=0 Ω). Active and reactive power plots when $E = V$ and α is varied are shown in Figure 3.4 parts (a), (b) and (c) while the plots when α is fixed at 0 and E is varied are shown in Figure 3.4 parts (d), (e) and (f).

Figure 3.4 (a) shows that when α=0, active power is 0 but as α becomes more +ve or –ve, the active power from the inverter decreases. From Figure 3.4 (b), reactive power decreases as α increases and vice versa. The rate of active and reactive power changes increases when the voltage level increases. Both the active and reactive power plots are combined in Figure 3.4 (c), for comparison. From this figure, for a purely resistive line impedance, the variation of α affects the reactive power more than the active power. Figure 3.4 (d) shows when α is fixed at 0, active power increases as E increases and vice versa. From Figure 3.4 (e), changing E will not affect the reactive power. Figure 3.4 (f) compares both active and reactive powers with varying E, on the same plot.

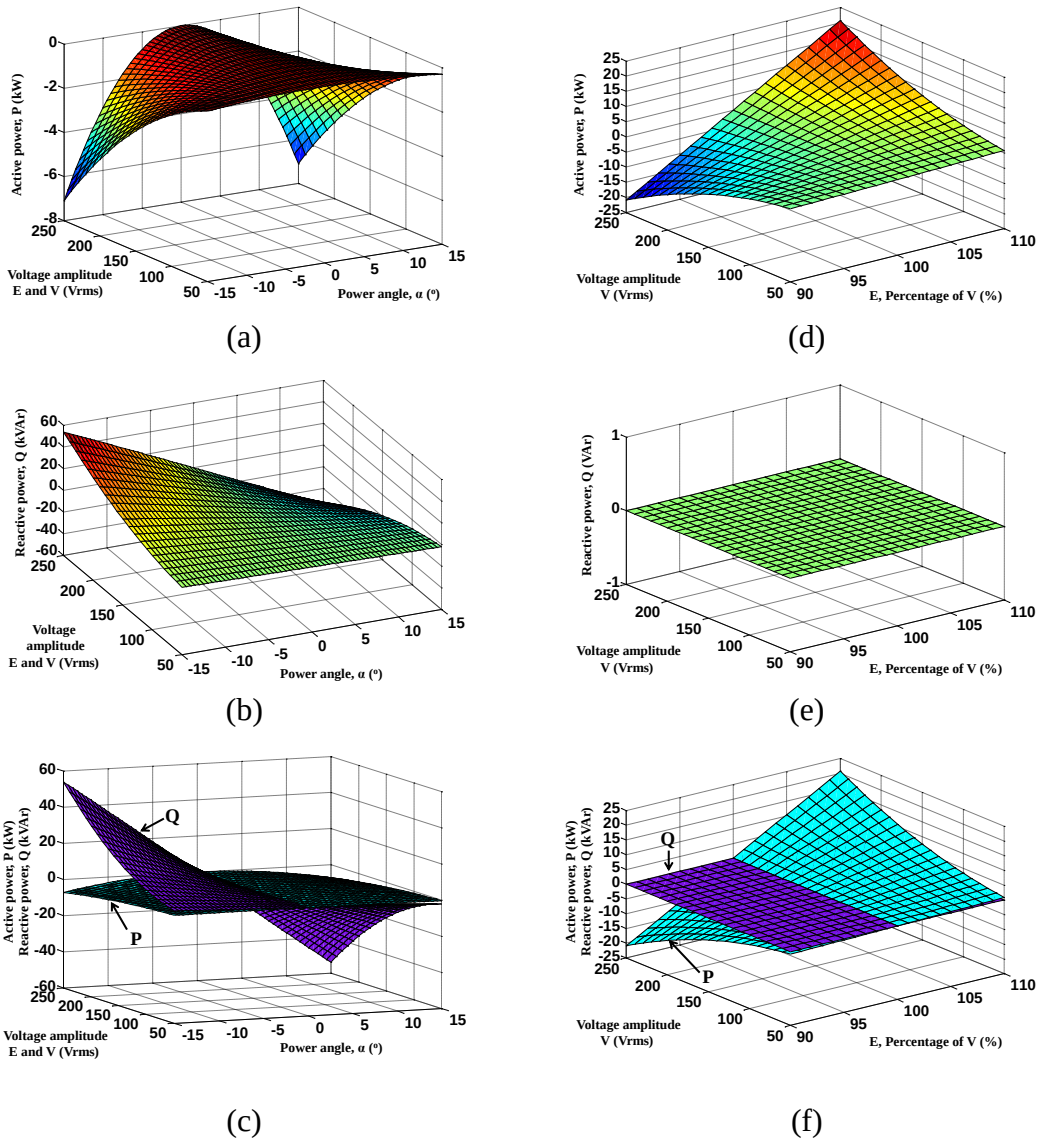
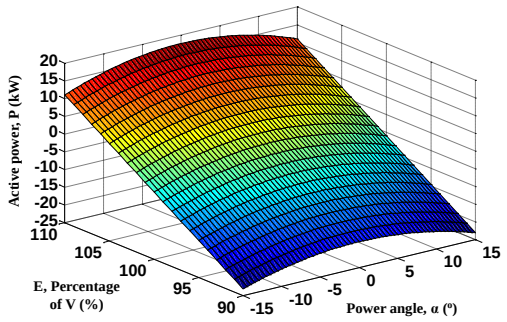
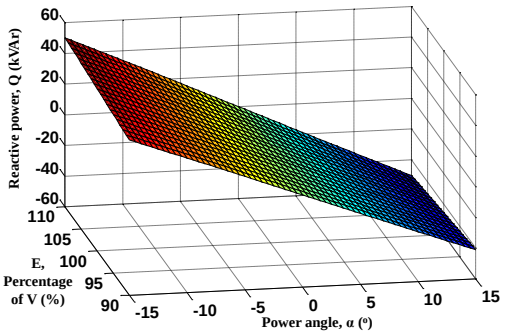


Figure 3.4 *P* and *Q* plots for different voltage levels under purely resistive line impedance (R=0.3 Ω and X=0 Ω): (a) *P* with fixed *E* and varying α; (b) *Q* with fixed *E* and varying α; (c) *P* and *Q* with fixed *E* and varying α; (d) *P* with $\alpha=0$ and varying *E*; (e) *Q* with $\alpha=0$ and varying *E* and (f) *P* and *Q* with $\alpha=0$ and varying *E*.

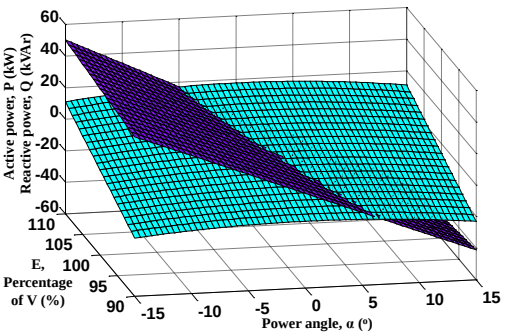
Active and reactive power plots with purely resistive line impedance (R=0.3 Ω and X=0 Ω) and V=230 V with varying E and α are shown in Figure 3.5. In Figure 3.5 (a), for all values of E, the active power follows a bell shaped curve as α increases from -15º to 15º and the magnitude of active power increases as E increases. Figure 3.5 (b) shows that for all E, the reactive power decreases as α increases and vice versa.



(a)



(b)



(c)

Figure 3.5 P and Q plots under purely resistive line impedance (R=0.3 Ω and X=0 Ω) and V=230V with varying E and α: (a) P, (b) Q, and (c) P and Q.

3.1.3 Complex line impedance

Most impedance analyses are usually done by assuming either pure inductance or pure resistance. However, in many real world applications, the line impedance is complex. In this case, the active and reactive power flows comply with equation (3.2). Complex impedance can be divided into three categories:

(i) $X = R$;

(ii) $X/R > 1$; and

(iii) $R/X > 1$.

Figure 3.6 shows the active and reactive power plots for different X/R ratio (Z is fixed at 0.3 Ω). Power plots when E is fixed at 230 V and α is varied are shown in Figure 3.6 parts (a), (b) and (c) while the plots when α is fixed at 0 and E is varied are shown in Figure 3.6 parts (d), (e) and (f). Figure 3.6 (a) shows for $X/R \geq 1$, active power increases as α increases and vice versa. In Figure 3.6 (b), for X/R=1 to X/R=3.8, reactive power decreases as α increases and vice versa. As the line impedance becomes more inductive, the reactive power plot becomes more like a bell shape. Both active and reactive power plots are compared in Figure 3.6 (c).

When α is fixed and E is varied, the active power increases as E increases and vice versa however the gradient of active power change decreases as the line impedance become more inductive, as shown in Figure 3.6 (d). Figure 3.6 (e) shows for $X/R \geq 1$, reactive power increases as E increases and vice versa. Both active and reactive power plots are compared in Figure 3.6 (f).

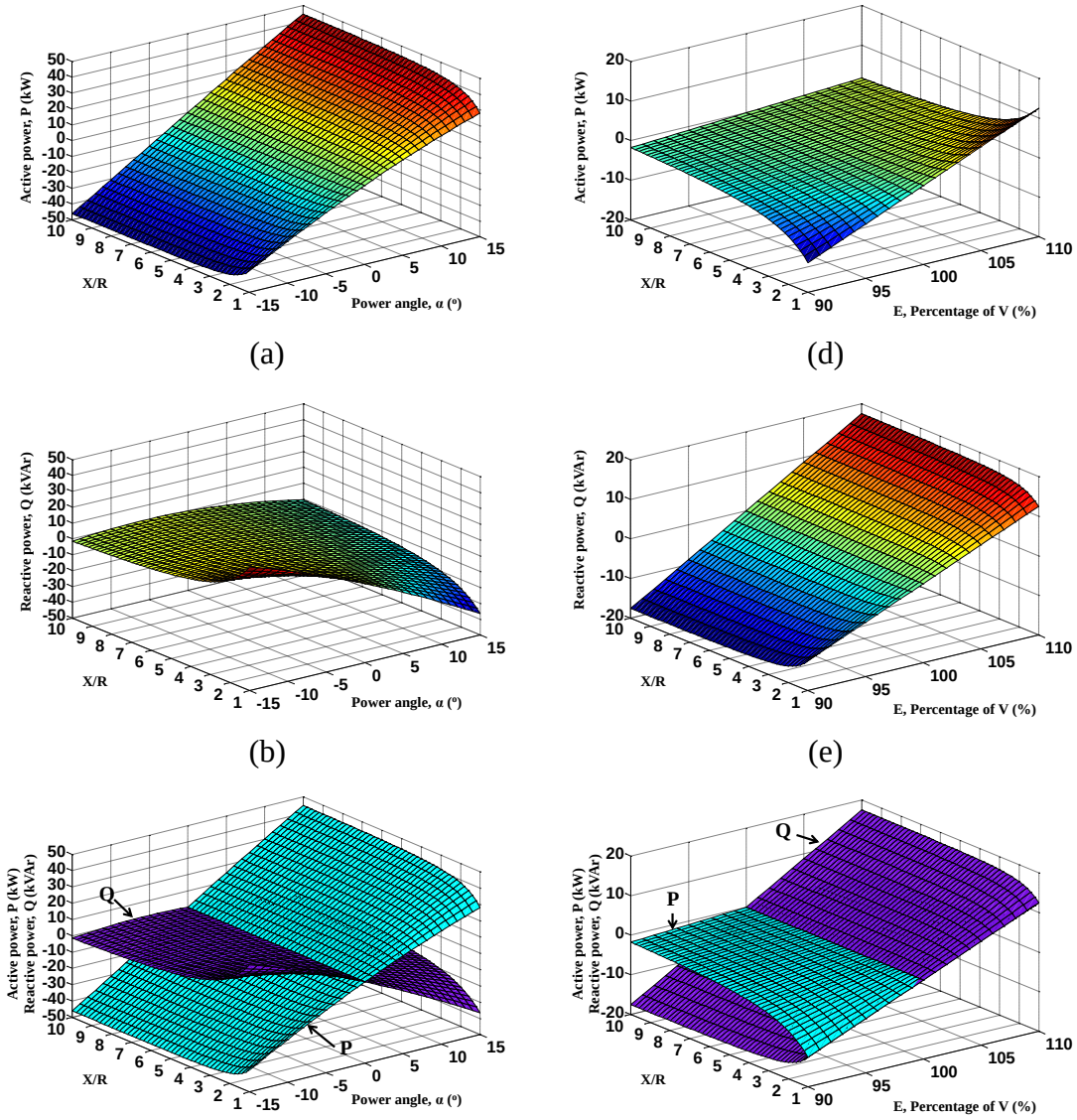


Figure 3.6 *P* and *Q* plots for different *X/R* ratio with *Z*=0.3 Ω and *V*=230 V: (a) *P* with fixed *E* and varying *α*; (b) *Q* with fixed *E* and varying *α*; (c) *P* and *Q* with fixed *E* and varying *α*; (d) *P* with *α=0* and varying *E*; (e) *Q* with *α=0* and varying *E* and (f) *P* and *Q* with *α=0* and varying *E*.

Active and reactive power plots for different *R/X* ratio (*Z* is fixed at 0.3 Ω) are shown in Figure 3.7. The power plots when *E* is fixed at 230 V and *α* is varied are shown in Figure 3.7 parts (a), (b) and (c) while the plots when *α* is fixed at 0 and *E* is varied are shown in Figure 3.7 parts (d), (e) and (f). Figure 3.7 (a) shows that for *X/R*=1 to *X/R*=3.8, active power increases as *α* increases and vice versa. As the line impedance becomes more resistive, the reactive power plot becomes more like a bell shape. In general, for $R/X \geq 1$, reactive power decreases as *α* increases and vice versa as shown

in Figure 3.7 (b). Both active and reactive power plots are compared in Figure 3.7 (c). When α is fixed and E is varied, the active power increases as E increases and vice versa and this applies when $R/X \geq 1$ as shown in Figure 3.7 (d). Figure 3.7 (e) shows that the reactive power increases as E increases and vice versa however the gradient of reactive power change decreases as the line impedance become more resistive. Both active and reactive power plots are compared in Figure 3.7 (f).

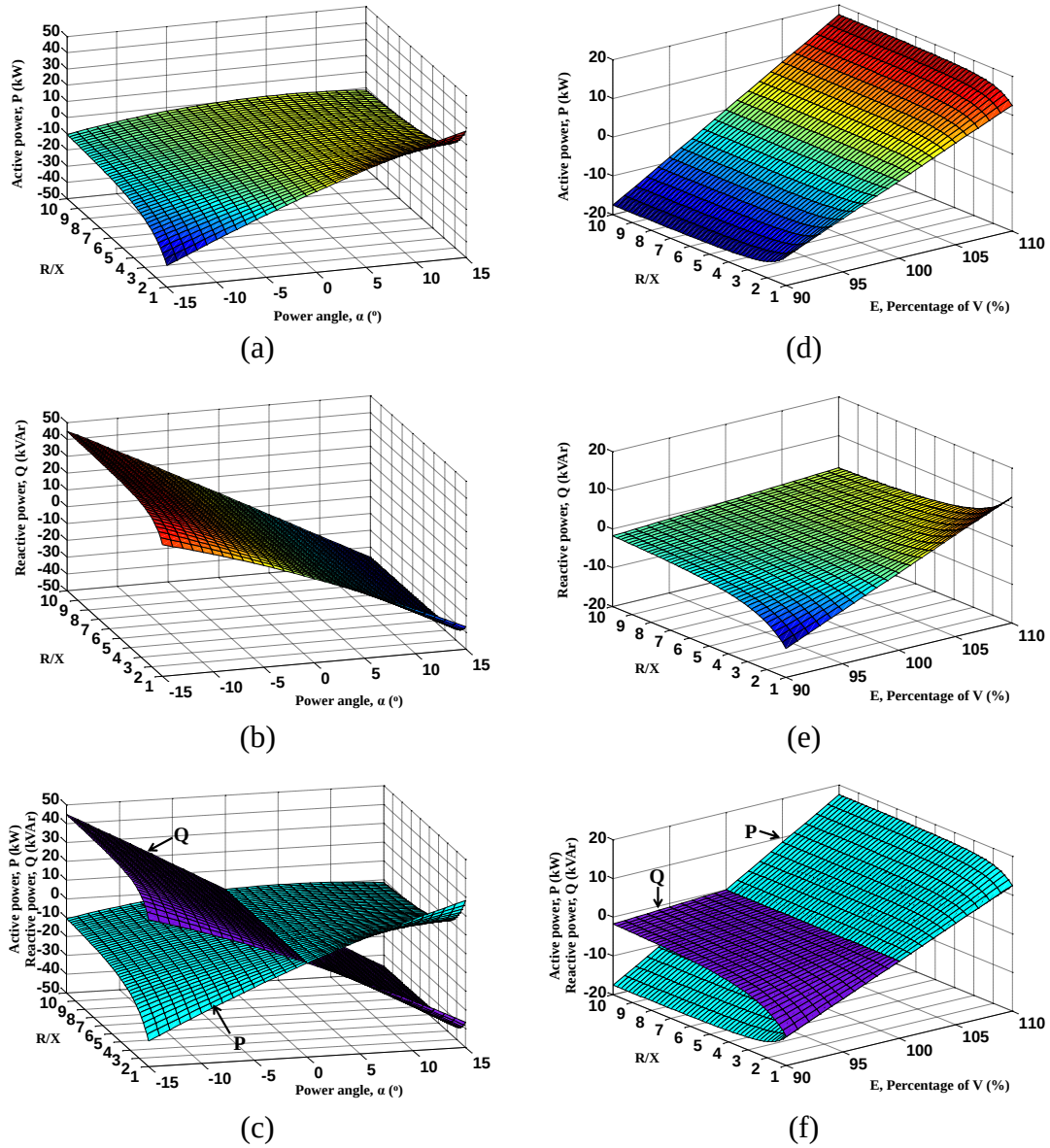


Figure 3.7 P and Q plots for different R/X ratio with Z=0.3 Ω and V=230 V: (a) P with fixed E and varying α; (b) Q with fixed E and varying α; (c) P and Q with fixed E and varying α; (d) P with $\alpha=0$ and varying E; (e) Q with $\alpha=0$ and varying E and (f) P and Q with $\alpha=0$ and varying E.

3.1.4 Effects of line impedance: Summary

In this section, the effects of different line impedance characteristic to the power flow in ac system are investigated. Under purely inductive line impedance, active power and reactive power injected to the PCC bus is mainly influenced by α and amplitude difference (E-V), respectively. These conditions are true when α is relatively small (-15^{o} to 15^{o}).

For purely resistive line impedance, the opposite conclusion from the purely inductive line impedance can be observed. In this condition, the amplitude difference (E-V) gives bigger impact on the active power flow while changes in α (small angle) affect more on reactive power flow.

For complex line impedance, three conditions can exist: i) $X = R$; ii) $X/R > 1$ and iii) $R/X > 1$. When E=V=230 V, for $X/R \geq 1$, active power increases as α increases and vice versa while for $X/R = 1$ to $X/R = 3.8$, reactive power decreases as α increases and vice versa. As the line impedance becomes more inductive, the reactive power plot becomes more like a bell shape. When $\alpha = 0$, for $X/R \geq 1$, the active power increases as E increases and vice versa however the gradient of active power change decreases as the line impedance become more inductive. On the other hand, with the same condition, the reactive power increases as E increases and vice versa.

When E=V=230 V, for R/X=1 to R/X=3.8, active power increases as α increases and vice versa. As the line impedance becomes more resistive, the reactive power plot becomes more like a bell shape. On the other hand, for $R/X \geq 1$, reactive power decreases as α increases and vice versa. When $\alpha = 0$, for $R/X \geq 1$, the active and reactive power increases as E increases and vice versa. However the gradient of reactive power change decreases as the line impedance become more resistive.

3.2 Circulating current in parallel inverters

Circulating current is an important aspect that should be taken into account when dealing with parallel inverters in a microgrid. Previous literature has discussed circulating current in parallel connected inverter applications [3.3-9]. Ideally, it is desired that each parallel connected inverter have an output voltage that has the same phase, amplitude and frequency, however in real life operation this is difficult to achieve because each component has its own inaccuracy. In general, there will be a circulating current flowing in the parallel system if there is voltage mismatch of inverter output voltages in term of amplitude, phase or frequency [3.3]. In [3.4], the authors added another factor, namely modulation. They proved that without uniform modulation, the circulating current still occurs even though all the parallel connected inverters have the same modulating signals. In [3.5], the authors discussed the circulating current by representing the two paralleled inverters with two parallel connected dual buck converters that share a same DC link. Based on the circulating current analysis, the authors proposed a controller that can change the switching pattern when the circulating current exceeds certain limits in order to reduce the circulating current. Circulating current for a 3-phase grid connected parallel inverters system has been discussed in [3.6]. The authors proposed a circulating current definition for each individual phase. The active and reactive components of circulating currents were defined in [3.7, 8]. The authors in both cases used the circulating current analysis to properly design the output impedance of their systems. In [3.9], circulating current was defined as the negative of difference between average current in the system and the output current of an inverter. All this literature discussed circulating current for two parallel connected inverters system. No literature so far has discussed circulating current in a parallel connected inverters system that contains more than two inverters. It is interesting to know the definition and characteristics of circulating current in this kind of system. These aspects are covered in this section.

3.2.1 Circulating current in two parallel connected inverters system

Figure 3.8 shows the equivalent circuit of two parallel connected inverters supplying a load through system impedances. $\bar{I}_1$ and $\bar{I}_2$ are the output currents of inverter 1 and inverter 2 respectively and they are defined as:

$$\bar{I}_1 = \frac{\bar{E}_1 - \bar{V}_o}{\bar{Z}_1} = \frac{\bar{U}_{\Delta 1}}{\bar{Z}_1} \tag{3.5}$$

$$\bar{I}_2 = \frac{\bar{E}_2 - \bar{V}_o}{\bar{Z}_2} = \frac{\bar{U}_{\Delta 2}}{\bar{Z}_2} \tag{3.6}$$

where $\bar{E}_1$, $\bar{E}_2$, $\bar{V}_o$, $\bar{Z}_1$ and $\bar{Z}_2$ are the output voltage of first inverter, output voltage of second inverter, load voltage, system impedance of first inverter and system impedance of second inverter, respectively. The load voltage can be derived using the Millman's theorem:

$$\bar{V}_o = \frac{\frac{\bar{E}_1}{\bar{Z}_1} + \frac{\bar{E}_2}{\bar{Z}_2}}{\frac{1}{\bar{Z}_1} + \frac{1}{\bar{Z}_2} + \frac{1}{\bar{Z}_o}} = \frac{\bar{Z}_o\left(\bar{E}_1\bar{Z}_2 + \bar{E}_2\bar{Z}_1\right)}{\bar{Z}_1\bar{Z}_2 + \bar{Z}_2\bar{Z}_o + \bar{Z}_1\bar{Z}_o} \tag{3.7}$$

where $\bar{Z}_o$ is the load impedance. By common definition, circulating current in this system is given by [3.3, 4]

$$\bar{I}_H = \frac{\bar{I}_1 - \bar{I}_2}{2} \tag{3.8}$$

However, it can be argued that the calculation can be done in the opposite way, that is:

$$\bar{I}_H = \frac{\bar{I}_2 - \bar{I}_1}{2} \tag{3.9}$$

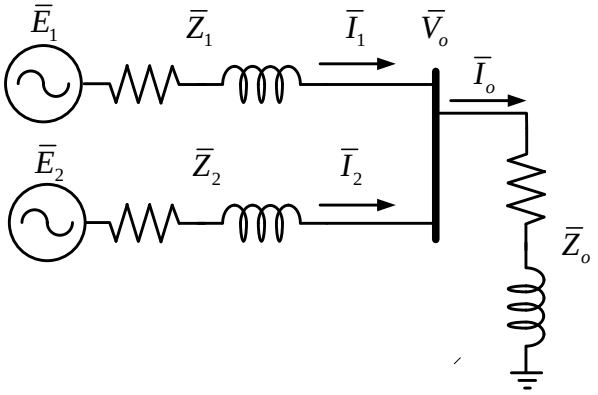


Figure 3.8 Two parallel inverters system.

So in this case, the circulating current can be defined based on which inverter the circulating current is seen from. The circulating current seen by inverter 1 and 2 are given by (3.10) and (3.11) respectively.

$$\bar{I}_{H1} = \frac{\bar{I}_1 - \bar{I}_2}{2} \tag{3.10}$$

$$\bar{I}_{H2} = \frac{\bar{I}_2 - \bar{I}_1}{2} \tag{3.11}$$

Substituting (3.5) and (3.6) into (3.10) and (3.11) results in

$$\bar{I}_{H1} = \frac{\bar{U}_{\Delta 1} Z_2 - \bar{U}_{\Delta 2} Z_1}{2 Z_1 Z_2} \tag{3.12}$$

$$\bar{I}_{H2} = \frac{\bar{U}_{\Delta 2} Z_1 - \bar{U}_{\Delta 1} Z_2}{2 Z_1 Z_2} \tag{3.13}$$

The average output current from the two inverters is:

$$\bar{I}_{avg} = \frac{\bar{I}_1 + \bar{I}_2}{2} \tag{3.14}$$

It can be shown that the different between each inverter output current and the average current is the same as the circulating current seen by each inverter [3.9].

$$\bar{I}_1 - \bar{I}_{avg} = \frac{2\bar{I}_1 - \bar{I}_2 - \bar{I}_1}{2} = \frac{\bar{I}_1 - \bar{I}_2}{2} = \bar{I}_{H1} \tag{3.15}$$

$$\bar{I}_2 - \bar{I}_{avg} = \frac{2\bar{I}_2 - \bar{I}_1 - \bar{I}_2}{2} = \frac{\bar{I}_2 - \bar{I}_1}{2} = \bar{I}_{H2} \tag{3.16}$$

3.2.2 Circulating current in an *N* parallel inverters system

Figure 3.9 shows the equivalent circuit of *N* parallel inverters supplying a load through system impedances. Current from each inverter is:

$$\bar{I}_k = \frac{\bar{E}_k - \bar{V}_o}{\bar{Z}_k} = \frac{\bar{U}_{\Delta k}}{\bar{Z}_k} \quad (k = 1, 2, ..., N) \tag{3.17}$$

where $\bar{I}_k$, $\bar{E}_k$ and $\bar{Z}_k$ are output current, output voltage and system impedance of the k^{th} inverter respectively. As with the two inverter system, the generalized equation for load voltage, $\bar{V}_o$, is derived using the Millman's theorem and given by (3.18).

$$\bar{V}_o = \frac{\frac{\bar{E}_1}{\bar{Z}_1} + \frac{\bar{E}_2}{\bar{Z}_2} + ... + \frac{\bar{E}_N}{\bar{Z}_N}}{\frac{1}{\bar{Z}_1} + \frac{1}{\bar{Z}_2} + ... + \frac{1}{\bar{Z}_N} + \frac{1}{\bar{Z}_o}} = \frac{\sum_{j=1}^{N}\left(\frac{\bar{E}_j}{\bar{Z}_j}\right)}{\frac{1}{\bar{Z}_o} + \sum_{j=1}^{N}\left(\frac{1}{\bar{Z}_j}\right)} \tag{3.18}$$

The average output current is given by:

$$\bar{I}_{avg} = \frac{\sum_{j=1}^{N} \bar{I}_j}{N} \tag{3.19}$$

The circulating current seen by each inverter is defined as the different between its output current and the average current.

$$\bar{I}_{Hk} = \bar{I}_k - \bar{I}_{avg} = \frac{N\bar{I}_k - \sum_{j=1}^{N} \bar{I}_j}{N} \quad (k = 1, 2, ..., N) \tag{3.20}$$

where $\bar{I}_{Hk}$ is the circulating current seen by the k^{th} inverter. Substituting (3.17) into (3.20) results in

$$\bar{I}_{Hk} = \frac{N\bar{U}_{\Delta k}\prod_{\substack{j=1 \\ j\neq k}}^{N} \bar{Z}_j - \sum_{j=1}^{N}\left(\bar{U}_{\Delta j}\prod_{\substack{i=1 \\ i\neq j}}^{N} \bar{Z}_i\right)}{N\prod_{j=1}^{N} \bar{Z}_j} \quad (k = 1, 2, ..., N) \tag{3.21}$$

Equation (3.21) is a novel equation definition for the circulating current seen by the k^{th} inverter.

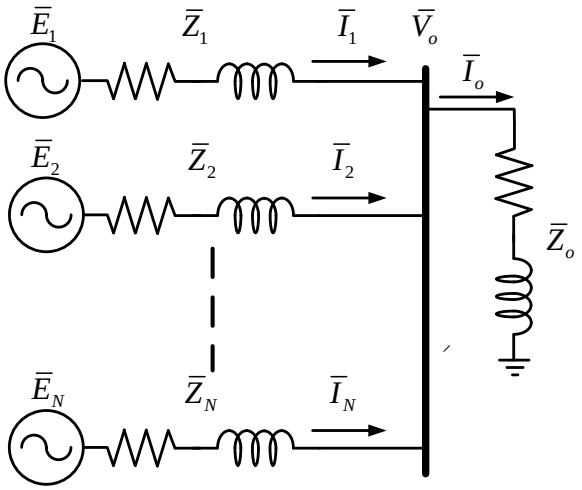


Figure 3.9 *N* parallel inverters system.

3.2.3 Simulation setup: Circulating current in three parallel connected inverters system

Several MATLAB/Simulink simulations have been conducted to investigate the circulating current in a three parallel inverters system. To simplify the simulation, three voltage sources ($\bar{E}_1$, $\bar{E}_2$ and $\bar{E}_3$) are used to represent the output voltage of three inverters (after LC filtering). All the three voltage sources are connected to a load ($\bar{Z}_o$) through their respective line impedances ($\bar{Z}_1$, $\bar{Z}_2$ and $\bar{Z}_3$). The system configuration is shown in Figure 3.10. The active and reactive powers calculation blocks are used to calculate the output power (P_1, Q_1, P_2, Q_2, P_3, Q_3), power absorbed by line impedance (P_{D1}, Q_{D1}, P_{D2}, Q_{D2}, P_{D3}, Q_{D3}), circulating power (P_{H1}, Q_{H1}, P_{H2}, Q_{H2}, P_{H3}, Q_{H3}), power absorbed by line impedance due to circulating current (P_{DH1}, Q_{DH1}, P_{DH2}, Q_{DH2}, P_{DH3}, Q_{DH3}), and load power (P_o, Q_o). I_{H1}, I_{H2} and I_{H3} shown in Figure 3.10 are the circulating currents seen by voltage sources 1, 2 and 3 respectively and these currents are calculated using equation (3.20). There are 9 simulations, divided into five parts. All are simulated for 0.1s and the output current from all voltage sources, circulating currents, load current, and average current are plotted for each simulation. The system parameters used for each test are listed in Table 3.1. The power rating of one inverter (all the three inverters have the same power rating) is selected for the S_{base} value. Highlighted boxes in the table contain the parameters that are different from the control parameters (Test 1).

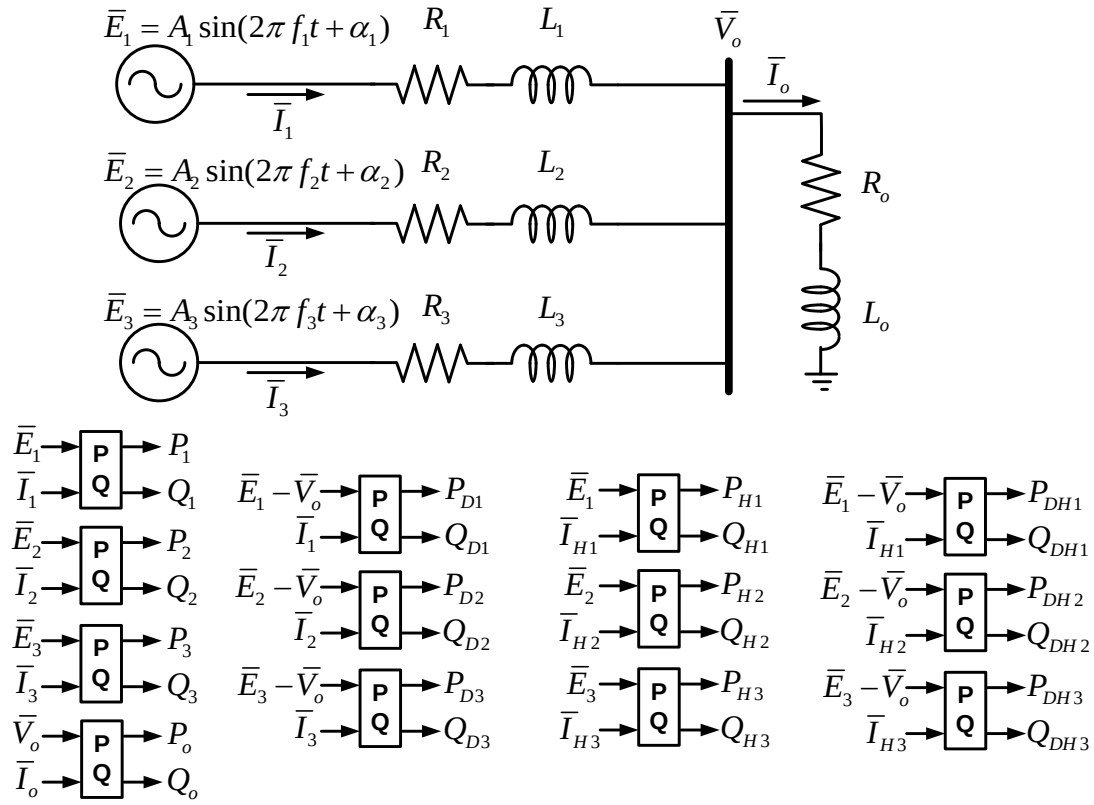


Figure 3.10 Circulating current simulation for three parallel connected voltage sources.

a) Part I: Ideal condition (Test 1)

In this part, the ideal condition of parallel operation is simulated. The system parameters in column Test 1 (Table 3.1) are used. The voltage sources and line impedances for the three parallel voltage sources are identical. All of them are connected to the *RL* load.

b) Part II: Circulating current due to phase difference (Test 2, 3, 4 and 5)

Simulations in this part are intended to show the circulating current occurrence in a parallel system due to phase differences among voltage sources. In Test 2, the load is the same as Test 1. Partial loading is used for Test 3 and the load is disconnected for Test 4. Tests 3 and 4 are intended to show the effect of load on circulating current. In Test 5, the same load as Test 1 is used but the line impedances from voltage sources 1 and 3 are changed to see the effect of line impedance on circulating current.

c) Part III: Circulating current due to amplitude difference (Tests 6 and 7)

In this part, the effect of voltage amplitude difference of parallel connected voltage sources on the circulating current is investigated. For Test 6, the amplitude of the first and third voltage sources are changed while the other parameters are the same as Test 1. Test 7 is the same as Test 6 but with the load disconnected from the system.

d) Part IV: Circulating current due to frequency difference (Test 8 and 9)

Investigation on the effect of voltage frequency difference of parallel connected voltage sources on the circulating current is performed. For Test 8, the frequency of the second and third voltage sources are changed while other parameters are the same as Test 1. Test 9 is the same as Test 8 but with the load disconnected from the system.

Table 3.1 System Parameters

		Test 1	Test 2	Test 3	Test 4	Test 5	Test 6	Test 7	Test 8	Test 9
V_{base} (V)		230								
S_{base} (VA)		3000								
E_1	A_1 (pu)	1	1	1	1	1	1	1	1	1
	α_1 (^{o})	0	0	0	0	0	0	0	0	0
	f_1 (Hz)	50	50	50	50	50	50	50	50	50
E_2	A_2 (pu)	1	1	1	1	1	1.022	1.022	1	1
	α_2 (^{o})	0	1.5	1.5	1.5	1.5	0	0	0	0
	f_2 (Hz)	50	50	50	50	50	50	50	50.02	50.02
E_3	A_3 (pu)	1	1	1	1	1	0.983	0.983	1	1
	α_3 (^{o})	0	-0.8	-0.8	-0.8	-0.8	0	0	0	0
	f_3 (Hz)	50	50	50	50	50	50	50	49.96	49.96
Z_1	R_1 (pu)	0.028	0.028	0.028	0.028	0.017	0.028	0.028	0.028	0.028
	X_1 (pu)	0.036	0.036	0.036	0.036	0.027	0.036	0.036	0.036	0.036
Z_2	R_2 (pu)	0.028	0.028	0.028	0.028	0.028	0.028	0.028	0.028	0.028
	X_2 (pu)	0.036	0.036	0.036	0.036	0.036	0.036	0.036	0.036	0.036
Z_3	R_3 (pu)	0.028	0.028	0.028	0.028	0.045	0.028	0.028	0.028	0.028
	X_3 (pu)	0.036	0.036	0.036	0.036	0.045	0.036	0.036	0.036	0.036
Z_o	R_o (pu)	0.284	0.284	0.567	∞	0.284	0.284	∞	0.284	∞
	X_o (pu)	0.089	0.089	0.178	∞	0.089	0.089	∞	0.089	∞

3.2.4 Simulation results: Circulating current in 3 parallel connected inverters

In this subsection, the simulation results of the circulating current in a 3 parallel inverters system are presented. Power and current measurements from each test are also presented in Table 3.2 and Table 3.3 respectively.

a) Part I: Ideal condition (Test 1)

Simulation results for Part A are shown in Figure 3.11. When the system parameters are the same for the three voltage sources, each source supplies the same current to the load. The average current will be the same as the output current from each source so there is no circulating current. This is expected as there will be no voltage difference among the voltage sources so the current from all voltage sources will only flow to the load.

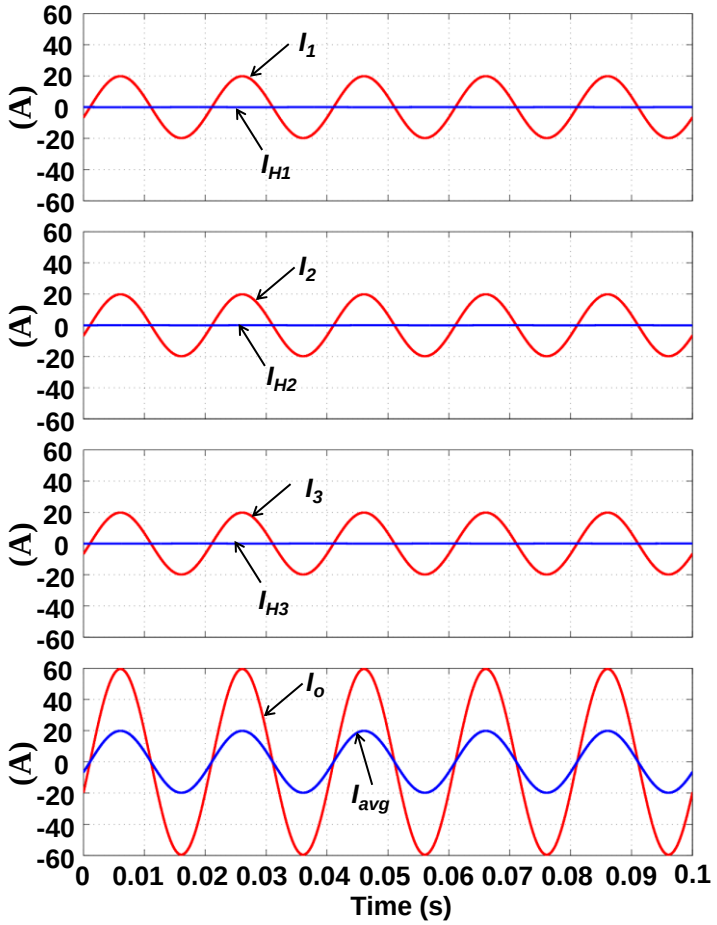


Figure 3.11 Simulation results for Test 1.

Table 3.2 shows that all the voltage sources equally shared the active and reactive powers (1.017pu and 0.35pu each) required by the load. Due to the non-existence of circulating current, there is no circulating power and no power is absorbed by line impedance due to circulating current. The sum of powers absorbed by line impedance and load power is equal to the sum of output powers. From Table 3.3, the sum of output current is equal to the load current which means currents from voltage sources only feed the load.

Table 3.2 Simulation results – power measurements

		Test 1	Test 2	Test 3	Test 4	Test 5	Test 6	Test 7	Test 8	Test 9
E_1	P_1 (pu)	1.017	0.950	0.454	-0.068	1.217	0.999	-0.020	1.079	0.063
	P_{D1} (pu)	0.033	0.030	0.007	0.0002	0.033	0.031	0.00003	0.036	0.0002
	P_{H1} (pu)	0	-0.068	-0.068	-0.068	0.195	-0.020	-0.020	0.063	0.063
	P_{DH1} (pu)	0	-0.004	-0.002	0.0002	0.0006	-0.0001	0.00003	0.004	0.0002
	Q_1 (pu)	0.350	0.404	0.228	0.058	0.676	0.326	-0.025	0.305	-0.049
	Q_{D1} (pu)	0.041	0.038	0.009	0.0003	0.052	0.039	0.00004	0.045	0.0002
	Q_{H1} (pu)	0	0.058	0.058	0.058	0.330	-0.025	-0.025	-0.049	-0.049
	Q_{DH1} (pu)	0	0.0009	0.0006	0.0003	0.017	-0.002	0.00004	-0.0001	0.0002
E_2	P_2 (pu)	1.017	1.394	0.903	0.385	1.335	1.324	0.283	1.261	0.249
	P_{D2} (pu)	0.033	0.055	0.023	0.007	0.051	0.061	0.006	0.046	0.003
	P_{H2} (pu)	0	0.385	0.385	0.385	0.323	0.283	0.283	0.249	0.249
	P_{DH2} (pu)	0	0.030	0.019	0.007	0.028	0.008	0.006	0.019	0.003
	Q_2 (pu)	0.350	0.077	-0.112	-0.296	0.050	0.715	0.356	0.165	-0.200
	Q_{D2} (pu)	0.041	0.069	0.029	0.008	0.064	0.077	0.007	0.058	0.004
	Q_{H2} (pu)	0	-0.296	-0.296	-0.296	-0.323	0.356	0.356	-0.200	-0.200
	Q_{DH2} (pu)	0	0.006	0.007	0.008	0.002	0.029	0.007	0.002	0.004
E_3	P_3 (pu)	1.017	0.717	0.219	-0.306	0.516	0.748	-0.253	0.719	-0.305
	P_{D3} (pu)	0.033	0.024	0.006	0.004	0.017	0.016	0.005	0.025	0.005
	P_{H3} (pu)	0	-0.306	-0.306	-0.306	-0.510	-0.253	-0.253	-0.305	-0.305
	P_{DH3} (pu)	0	-0.015	-0.005	0.004	-0.020	0.003	0.005	-0.015	0.005
	Q_3 (pu)	0.350	0.584	0.414	0.252	0.340	0.027	-0.318	0.590	0.259
	Q_{D3} (pu)	0.041	0.030	0.008	0.006	0.017	0.021	0.006	0.030	0.006
	Q_{H3} (pu)	0	0.252	0.252	0.252	0.008	-0.318	-0.318	0.259	0.259
	Q_{DH3} (pu)	0	0.008	0.006	0.006	-0.004	-0.014	0.006	0.008	0.006
$E_1+E_2+E_3$	P_{sum} (pu)	3.051	3.061	1.575	0.011	3.068	3.070	0.011	3.058	0.008
	P_{Dsum} (pu)	0.098	0.110	0.037	0.011	0.101	0.109	0.011	0.106	0.008
	P_{Hsum} (pu)	0	0.011	0.011	0.011	0.009	0.011	0.011	0.008	0.008
	P_{DHsum} (pu)	0	0.011	0.011	0.011	0.009	0.011	0.011	0.008	0.008
	Q_{sum} (pu)	1.051	1.065	0.530	0.014	1.065	1.067	0.013	1.061	0.010
	Q_{Dsum} (pu)	0.124	0.138	0.046	0.014	0.132	0.137	0.013	0.134	0.010
	Q_{Hsum} (pu)	0	0.014	0.014	0.014	0.015	0.013	0.013	0.010	0.010
	Q_{DHsum} (pu)	0	0.014	0.014	0.014	0.015	0.013	0.013	0.010	0.010
Load	P_o (pu)	2.952	2.951	1.538	0	2.967	2.961	0	2.952	0
	Q_o (pu)	0.928	0.927	0.483	0	0.932	0.930	0	0.927	0

Table 3.3 Simulation results – current measurements

	Test 1	Test 2	Test 3	Test 4	Test 5	Test 6	Test 7	Test 8	Test 9
I_1 rms (A)	1.076	1.033	0.508	0.089	1.392	1.050	0.032	1.121	0.080
I_2 rms (A)	1.076	1.396	0.910	0.485	1.336	1.473	0.446	1.272	0.320
I_3 rms (A)	1.076	0.925	0.468	0.396	0.618	0.761	0.414	0.930	0.400
$I_1+I_2+I_3$ rms (A)	3.227	3.353	1.886	0.971	3.346	3.284	0.891	3.323	0.800
I_o rms (A)	3.227	3.226	1.647	0	3.235	3.231	0	3.227	0
$I_1+I_2+I_3-I_o$ rms (A)	0	0.127	0.239	0.971	0.111	0.053	0.891	0.096	0.800

b) Part II: Circulating current due to phase difference (Test 2, 3 , 4 and 5)

Simulations in Part II are intended to show the effect of voltage phase difference among parallel voltage sources on the circulating current. The simulation results for Test 2, 3, 4 and 5 are shown in Figure 3.12 parts (a), (b), (c) and (d) respectively. Circulating currents exist when there are voltage differences among parallel voltage sources and these currents are the same for all the three tests even though the loading condition is different in each test. In Test 2, partial loading is used so it can be seen that the output current from each voltage source is reduced but the circulating current remains the same. When the load is disconnected from the system in Test 4, the output currents become the same as the circulating currents. From these results, it can be concluded that the circulating current is independent of the load condition and when there is no load, the output current of each voltage source is the circulating current seen by each voltage source. In Test 5, with the same loading condition as Test 2 but with changes in line impedances for voltage sources 1 and 3, different circulating currents can be observed as shown in Figure 3.12 (d). This is expected because when the line impedances from voltage sources 1 and 3 are reduced and increased respectively, more current comes from voltage source 1 and less current comes from voltage source 3. These in turn affect the circulating currents in the system. So it can be concluded that circulating currents in a parallel system are affected by the system line impedances.

In terms of power flow in the system (refer Table 3.2), for tests 2, 3 and 4, the circulating power from each voltage source is the same for all the three tests. Also the output power at a no load condition (Test 4) is the same as the circulating power. For the three tests, the sum of circulating powers is the same as sum of power

absorbed by line impedances due to circulating current (P_{Hsum}= P_{DHsum} = 0.011pu and Q_{Hsum}= Q_{DHsum}= 0.014pu).

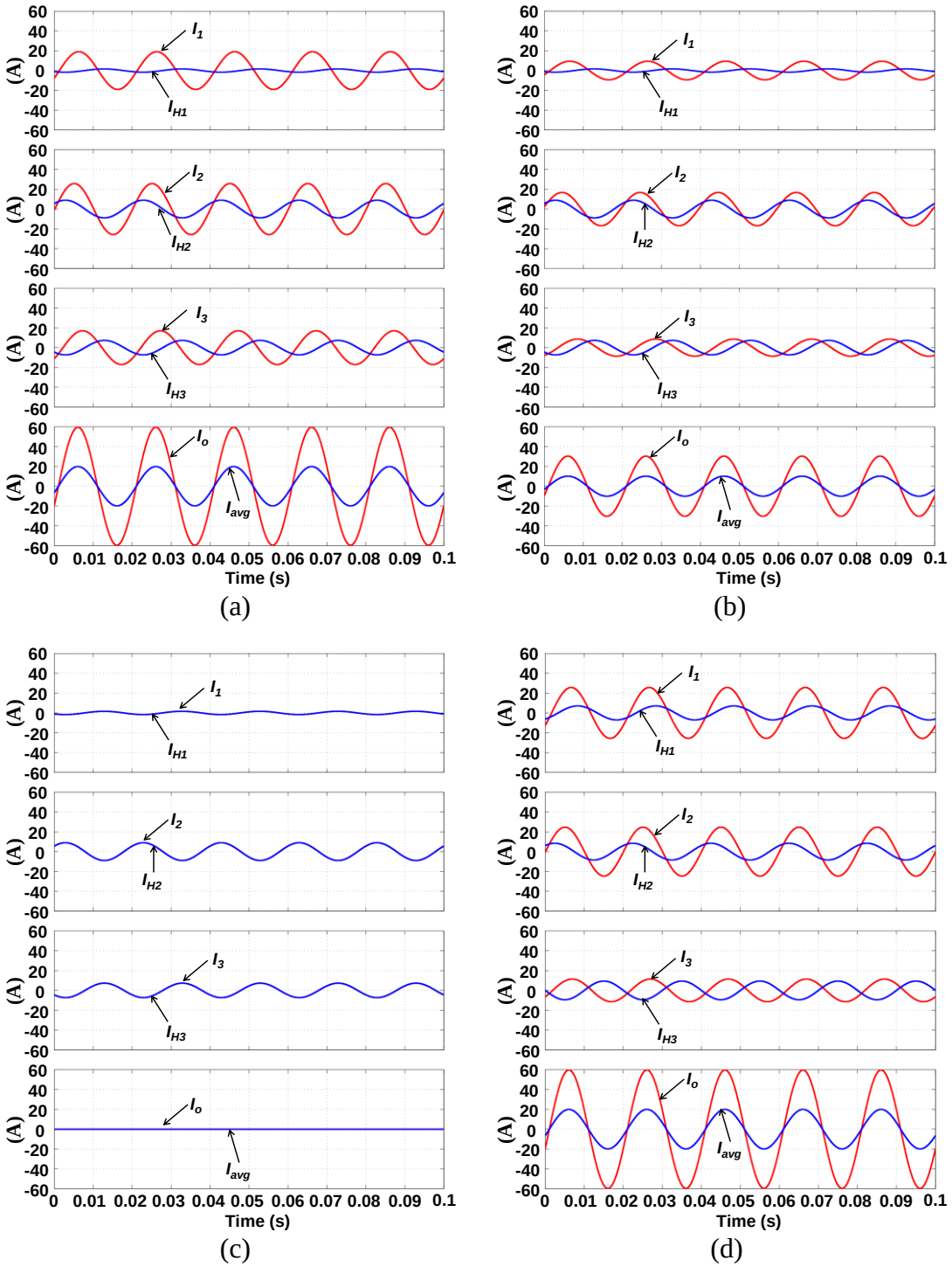


Figure 3.12 Simulation results for Part II. (a) Test 2; (b) Test 3; (c) Test 4; and (d) Test 5.

In Test 2, the output powers from all voltage sources are all positive but with different magnitude. This indicates that there are no net active or reactive power exchanges among inverters. For this case, the only negative impact of circulating current in the system is the extra active and reactive power losses (0.011pu and 0.014pu respectively) in the line impedances due to unequal current from each voltage source. From Table 3.3, there is 0.127pu difference between total output current and load current. This is the circulating currents that causes the system extra power losses.

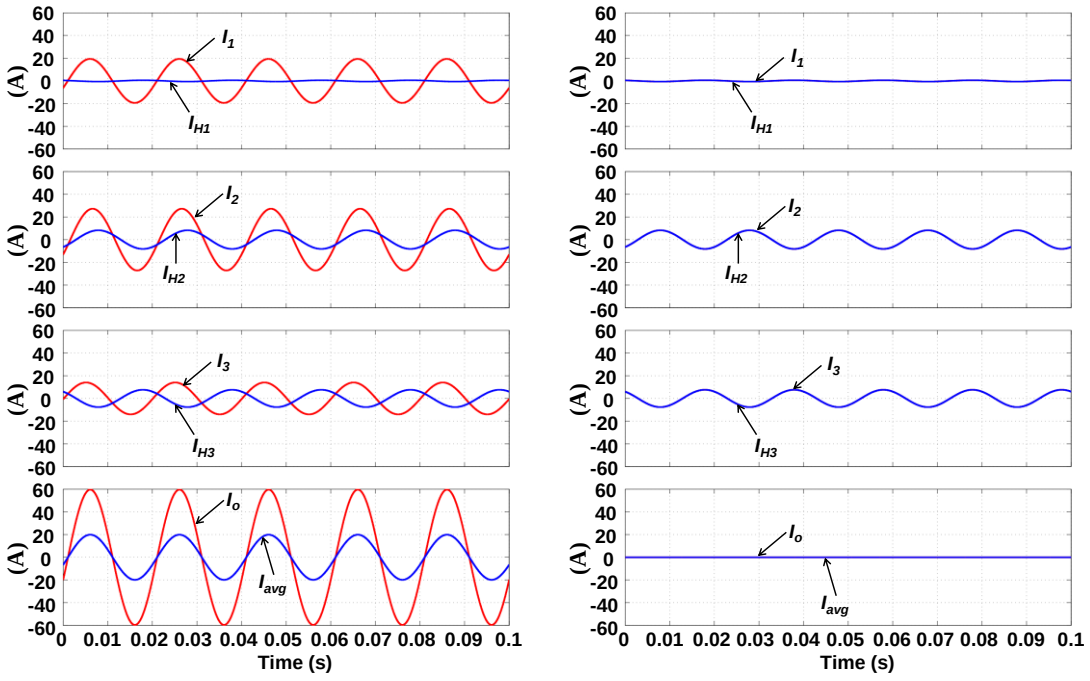
In Test 3, when the load is changed to partial loading, the second voltage source absorbs 0.112pu active power which means there is net reactive power exchange from other voltage sources to this voltage source. In real world inverter application, this can make the DC link voltage increase and affects the overall control and stability of inverters. For this test, there is a difference of 0.239pu between total output current and load current as shown in Table 3.3.

When the load is completely disconnected in Test 4, the first voltage source absorbs 0.068pu of active power and supplies 0.058pu of reactive power, the second voltage source supplies 0.385pu of active power and absorbs 0.296pu of reactive power, and third voltage source absorbs 0.306pu of active power and supplies 0.252pu of reactive power. All of these powers are the results of 0.971pu of current difference between the sum of the output currents and the load current shown in Table 3.3. Furthermore there are 0.011pu and 0.014pu losses of active and reactive power respectively in the line impedance due to the circulating currents.

For Test 5, when compared to Test 2, when the line impedances are changed, the output power from each voltage source is also changed. This power change is expected as the current from each voltage source is also changing with line impedance. In this particular case, there is no net power flow among inverters but P_{DHsum} decreases from 0.011pu to 0.009pu while Q_{DHsum} increases from 0.014pu to 0.015pu.

c) Part III: Circulating current due to amplitude difference (Test 6 and 7)

In this part, the effect of voltage amplitude difference among parallel voltage sources on the circulating current is investigated. The simulation results for tests 6 and 7 are shown in Figure 3.13 parts (a) and (b) respectively. In Test 6, circulating currents exist when there is amplitude difference among parallel connected voltage sources. As in part II, the circulating currents remain the same even when the load is disconnected from the system as shown in Test 7. Referring to Table 3.2, in Test 6, there is no net power exchange among voltage sources as all produce positive active and reactive output power. However due to the circulating current, there are extra power losses in the line (P_{DHsum} = 0.011pu and Q_{DHsum}= 0.013pu). In Test 7, under a no load condition, the first voltage source absorbs 0.02pu and 0.025pu of active and reactive power respectively. The second voltage source supplies 0.283pu and 0.356pu of active and reactive power while voltage source 3 absorbs 0.253pu and 0.318pu of active and reactive power. Due to these power flows, there will be 0.011pu and 0.013pu loss of active and reactive power respectively in the line impedances. From Table 3.3, in Test 7, the excessive current is about 0.891pu.

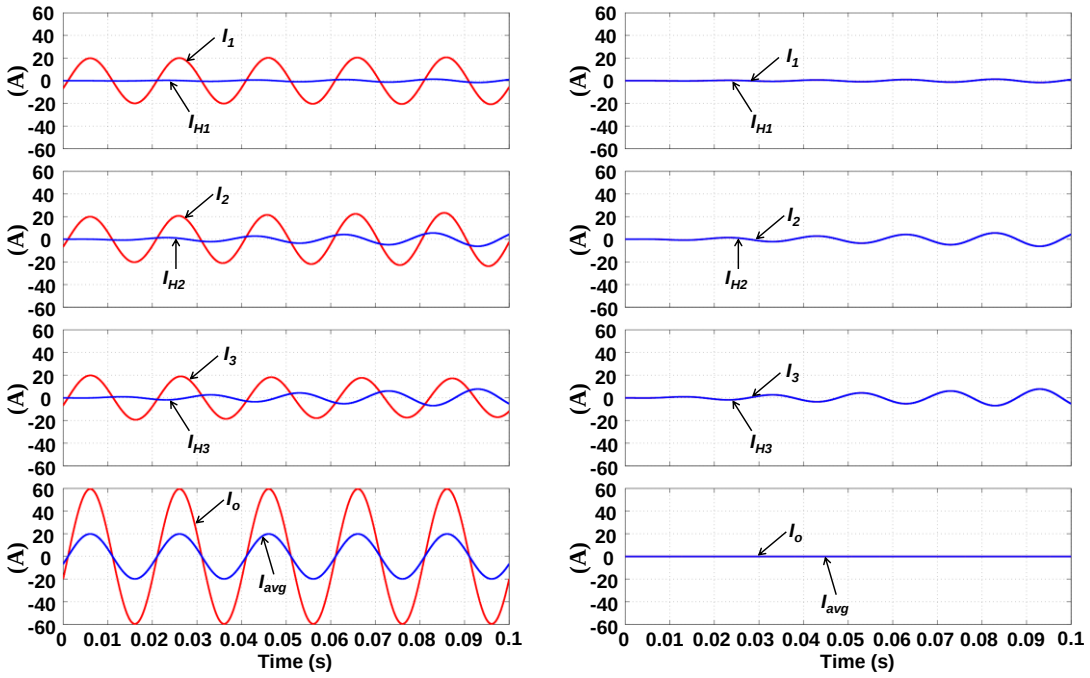


(a) (b)

Figure 3.13 Simulation results for Part III. (a) Test 6 (b) Test 7.

d) Part IV: Circulating current due to frequency difference (Tests 8 and 9)

Simulations in Part IV are intended to show the effect of voltage frequency difference among parallel voltage sources on the circulating current. The simulation results for tests 8 and 9 are shown in Figure 3.14 parts (a) and (b) respectively. The circulating currents exist in a system when frequencies of parallel connected voltage sources differ from each other. As expected, the circulating currents remain the same even when the load is disconnected as shown in Figure 3.14 (b). In terms of power flow, for Test 8, there is no net power flow among voltage sources (each voltage source outputs positive active and reactive powers) but the circulating currents produce extra power losses in the line impedances. In Test 9, the first voltage source supplies 0.063pu of active power and absorbs 0.049pu of reactive power and second voltage source supplies 0.249pu of active power and absorbs 0.2pu of reactive power. Voltage source 3 absorbs 0.305pu of active power and supplies 0.259pu of reactive power. Due to these power flows, there will be 0.008pu and 0.01pu losses of active and reactive powers respectively in the line impedances.



(a) (b)

Figure 3.14 Simulation results for Part IV. (a) Test 8 (b) Test 9.

3.3 Summary

In this chapter, ac power flow analysis for inverters under the effect of inductive, resistive and complex line impedance has been investigated. Several active and reactive power plots were obtained to visualize the impact of voltage power angle and amplitude on active and reactive power flowing in an ac system at different voltage levels.

In the second part of the chapter, circulating current was defined for a multiple parallel connected inverters connected to the same load bus. Several simulations were performed to visualize the circulating currents phenomenon due to the phase, amplitude and frequency differences among parallel connected inverters. Several conclusions can be made based on these simulations:

- Circulating current occurs when there are difference in output voltage amplitude, phase and frequency of parallel connected inverters.
- Circulating current is a current superimposed on normal power currents and is used as a tool to describe imbalance between inverters.
- Circulating current exists regardless of the load.
- At low loading or a no load condition, circulating current can cause power exchange among parallel connected inverters. This can affect the overall control and even damage the inverter. At high loading conditions, usually there will be no net power flow among inverters. In this case, the circulating current determines the power sharing ratio of parallel connected inverters. However this normally produces extra power losses in line impedances.
- In a real world situation, when the rating of an inverter is different, $S_1 = 2S_2$, then it is common to supply the load based on this ratio. In this case the current from inverter 1 will be double that of inverter 2. So provided there is no net active or reactive power flowing between inverters, the only negative impact is the extra line impedance losses.

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Chapter 4

Improved Instantaneous Average Current Sharing (IACS) Control

In this chapter, an improved IACS controller is proposed for a single phase system. A gain scheduling technique is adapted in the proposed technique. The objective is to improve the performance of the conventional IACS controller in term of current and power sharing between inverters under difference line impedance conditions. A generalized model of a single-phase parallel connected inverter system is derived. The model incorporates details of the control loops that use a proportional-resonant controller but not the switching action. The voltage and current controller design and parameter selection process are discussed. The simulation and experimental results will show that adaptive gain scheduling manages to improve the performance of the conventional IACS controller.

4.1 Background

From Chapter 2, in all active load sharing schemes, the output currents of parallel connected inverters are regulated at each switching cycle. These schemes have good performance, both in current sharing and voltage regulation, but do not incorporate the effects of line impedance. In an actual distributed system, the line impedance of one unit can be significantly different from the impedance of another unit.

As presented in section 3.1, load sharing is affected by line impedance variation. More important, the *X/R* ratio of line impedance affects the stability margin of a microgrid [4.1, 2]. If the system is informed of the line impedance then its effect can be compensated. Without this information, the controller is unable to compensate the voltage drop and power loss due to the line impedance. Few researchers have considered the effect of line impedance in the design of the control scheme [4.3-5]. In [4.3], the author proposed a combined droop method and power adjusting mechanism. A small ac voltage signal is injected into the system as a control signal. The quantity to be shared controls the frequency of this control signal. As far as an instantaneous current sharing control scheme is concerned, only [4.6] discussed the effect of line impedance on controller performance.

4.2 Parallel connected inverter system configuration

This section discusses the single inverter construction and parallel inverter configuration with IACS control used in this chapter.

4.2.1 Single inverter construction

A typical inverter consists of a dc power source, a bridge type inverter and an LC filter as shown in Figure 4.1. Assuming an ideal source from the DG side, the dc bus dynamics can be neglected. The inverter converts the dc input to an ac output based on the modulation signal from the SPWM modulator. L_f, R_f and C_f represent the inductance, resistance, and capacitance of the output filter, respectively. The line impedance between the inverter and the load network is the equivalent impedance due to the connecting lines or cables. This line impedance can be inductive or resistive. The load can be resistive, inductive, or capacitive; linear or nonlinear.

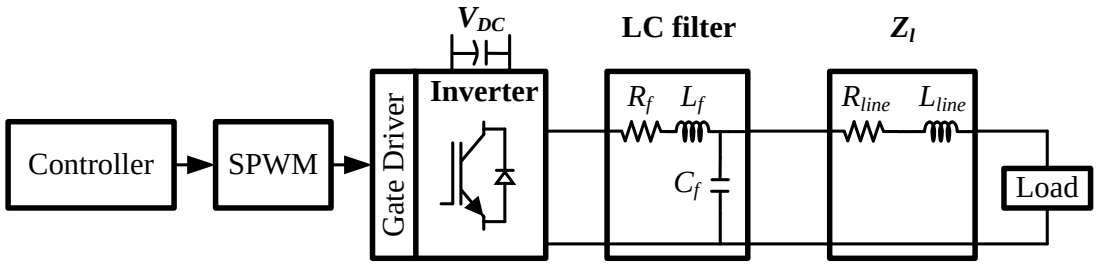


Figure 4.1 Block diagram of an inverter.

4.2.2 Multiple parallel connected inverter system

Figure 4.2 shows an instantaneous average current sharing scheme for a multiple parallel connected inverter system. Each inverter in the system receives a pre-synchronized reference voltage and delivers its own measured output current value to the current sharing bus from which the reference current is generated. This reference current becomes the reference for the outer current sharing loop of each inverter. The error between this reference and the output current of an individual inverter is fed to the current controller and the high gain of this controller provides an adequate corrective signal that is added to the modulating signal. In other words, the current sharing controller tries to increase the current if its output current is less than the reference current and decreases the current when the output current is more than the reference by adjusting the inverter output voltage.

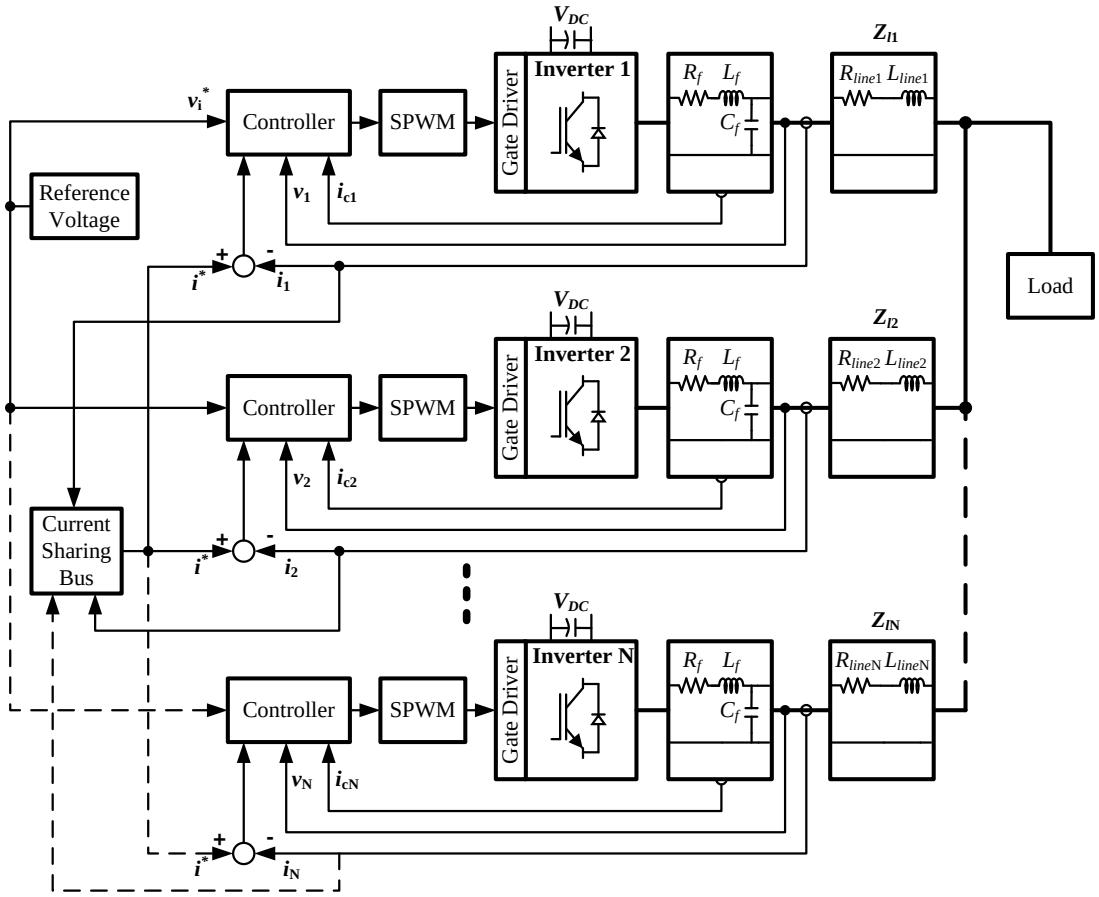


Figure 4.2 Instantaneous average current sharing scheme for a multiple inverter system.

4.3 IACS controller

A conventional IACS controller in general has good voltage regulation and current sharing performance. However, it can be improved to be adaptive to line impedance variations during operation. An improved IACS controller embedded with two gain schedulers is presented in this section.

4.3.1 Conventional IACS controller

Figure 4.3 shows the conventional IACS controller. Each inverter has three feedback control loops and one feed-forward control loop. The three feedback control loops are: i) inner current, ii) voltage control, and iii) outer current sharing. The inner current feedback loop and voltage feedback loop can provide good overall performance for both steady state and transient responses as shown in [4.7], for a single inverter system. For the inner current loop, the capacitor current is selected as

the controlled variable, which provides fast dynamic response for the overall system, reduces the controller sensitivity to the parameter variations, and makes the controller more robust. In [4.6], a traditional PI controller is used to regulate the output voltage and voltage feed-forward is added to provide high tracking accuracy of the reference.

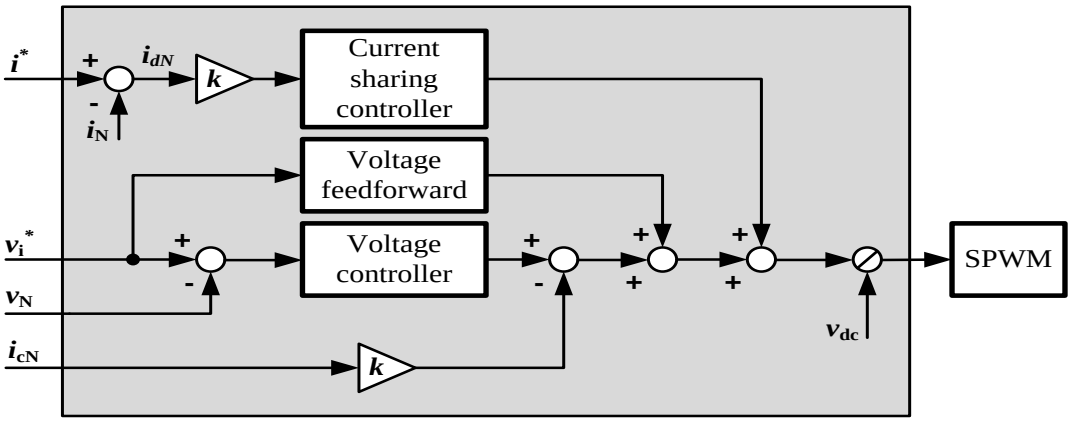


Figure 4.3 Conventional IACS controller.

4.3.2 Proposed IACS controller

The conventional IACS controller gives good system performance with equal or nearly equal line impedances. However when the line impedance between the inverters and load is not the same for each connection or the line impedance changes during operation, the sharing performance deteriorates.

To improve this controller, some changes have been made. For voltage regulation, a PR controller is used due to its superior performance in terms of low steady-state error, good dynamic response, and reduced steady-state deviations of frequency and amplitude. This controller achieves a very high gain around the resonance frequency, thus being capable to eliminate the steady-state error between the controlled signal and its reference at the resonance frequency. To add adaptive capability to the controller, gain scheduling techniques are considered. The gain scheduling principle is shown in Figure 4.4, which consists of a predefined range of gain value θ_i, the system auxiliary measurements, and logic for detecting the operating point and varying the gain value. In each parallel connected inverter cases, the auxiliary measurement is the difference between the reference current and the inverter current. With this approach, line impedance variation, which affects the current output of the inverter, is compensated by the gain variation. The advantage of gain scheduling

is that the controller gains respond at the same rate as the auxiliary measurements respond to parameter changes. Frequent and rapid changes of the controller gains, however, may lead to instability. Unpredictable changes in the plant dynamics may lead to performance deterioration or even to failure [4.8].

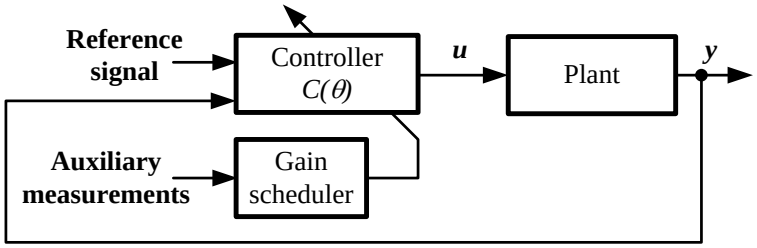


Figure 4.4 Gain scheduling principle.

Two gain schedulers are added to the conventional IACS controller as shown in Figure 4.5. Gain scheduler 1 changes the gain of the controlled signal (before the modulator) based on the current difference i_{dN}. This impacts on the modulation index of the PWM modulator. For the inverter with an output current lower than the reference current, this gain increases the magnitude of the controlled signal hence increases the modulation index. This makes the inverter deliver more current. For the other case, where inverter output current is higher than the reference current, the gain decreases the modulation index, forcing the inverter to deliver less current.

Gain scheduler 1 is set as follows:

$$\begin{aligned} &K_1(k+1) = K_1(k) + x \\ &x = 0 \qquad\quad if\ \ c_1 \le i_{dN} \le -c_1 \\ &x = -a_1 \qquad if\ i_{dN} > c_1 \\ &x = a_1 \qquad\ \ if\ i_{dN} < -c_1 \end{aligned} \tag{4.1}$$

where K_1 is the controller gain, c_1 is the threshold for acceptable current difference, and a_1 is the gain step. K_1 is set in such that it will not make the peak controlled signal to exceed the v_{dc} value. This is done to make sure the modulation index does not exceed 1.

Gain Scheduler 1 alone cannot ensure minimal current difference among parallel connected inverters. It only minimizes the difference by adjusting the modulation index of the controlled signal. To further reduce the current difference, hence

improve current sharing, Gain Scheduler 2 is used. This gain scheduler functions as follows:

$$\begin{aligned} &K_2(k+1) = K_2(k) + x \\ &x = 0 \qquad\quad if\ \ c_2 \le i_{dN} \le -c_2 \\ &x = -a_2 \qquad if\ i_{dN} > c_2 \\ &x = a_2 \qquad\quad if\ i_{dN} < -c_2 \end{aligned} \tag{4.2}$$

where K_2 is the controller gain, c_2 is the threshold for acceptable current difference, and a_2 is the gain step. From simulations, by increasing the gain of the current difference i_{dN}, the inverter current output also increases and vice versa. However the sensitivity of this gain to inverter current is not as great as that of Gain Scheduler 1. Simply, Gain Scheduler 1 acts as a course tuner and Gain Scheduler 2 acts as a fine-tuner. The sharing performance is improved by combining the two gain schedulers.

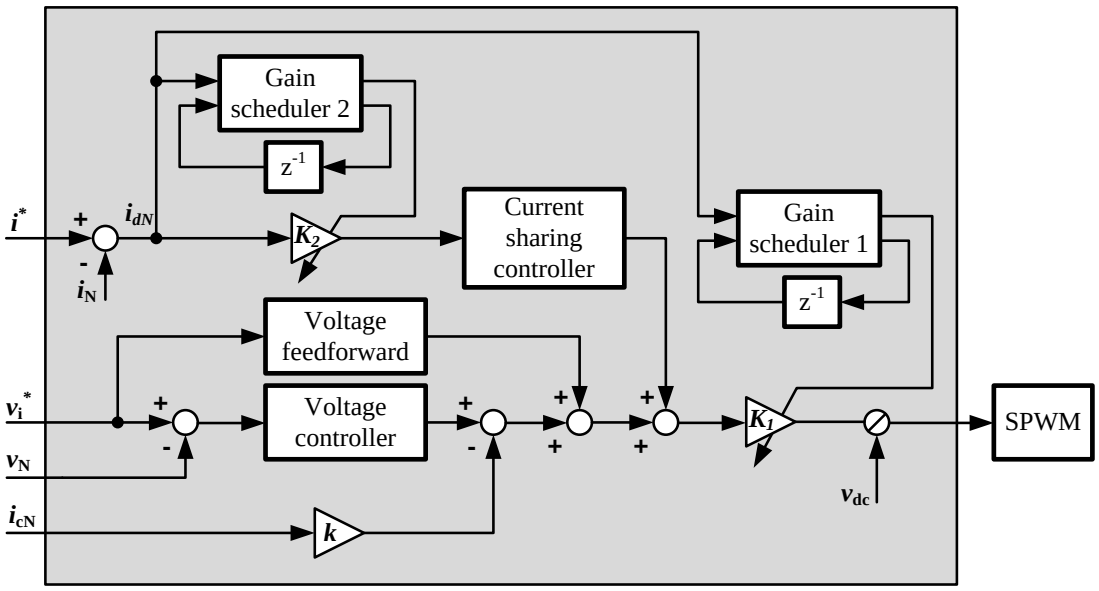


Figure 4.5 Proposed improved IACS controller.

4.4 Generalized model of parallel multi inverter system

An inverter with the instantaneous average current sharing scheme is modelled in Figure 4.6. It consists of a simple linear inverter model (dot shaded area) with two feedback loops and one feed-forward controller loop. This model has two inputs which are input voltage (v_i^*) and output current (i_o) and one output which is the output voltage of the inverter (v_o). L_f, C_f and R_f represent the filter inductance,

capacitance and resistance respectively. G_v represents the PR voltage controller of the voltage feedback loop, K_f is the gain of the voltage feed-forward loop, and K_c is the gain of the current feedback loop. In this model it is assumed that the inverter has unity gain. That is, the modulation index of the SPWM modulator is assumed to be 1. The equation for G_v is given in (4.3).

$$G_v = K_P + \frac{K_{\mathrm{Res}}(s + w_c)}{s^2 + 2w_c s + w_c^{\,2} + w_o^{\,2}} \tag{4.3}$$

where K_P, K_{Res} and w_c are the proportional gain, resonant gain, and cut off frequency of the PR controller respectively, and w_o is the system fundamental system. Equation (4.3) introduces a finite gain to avoid stability problems associated with an infinite gain of the ideal PR controller. Furthermore, by properly setting w_c value, the controller bandwidth can be widened. This helps reducing sensitivity towards frequency variation (e.g. droop technique) [4.9]. The closed-loop voltage gain G can be derived from Figure 4.6 by setting i_o to 0 and the model can be simplified to (4.4). By setting v_i^* to 0, the model can be simplified to (4.5), to find the output impedance of the inverter.

$$G = \frac{K_1(G_v + K_f)}{C_f L_f s^2 + \left(C_f R_f + C_f K_c\right)s + K_1 G_v + 1} \tag{4.4}$$

$$Z = \frac{L_f s + R_f}{L_f C_f s^2 + \left(R_f C_f + K_1 K_c C_f\right)s + K_1 G_v + 1} \tag{4.5}$$

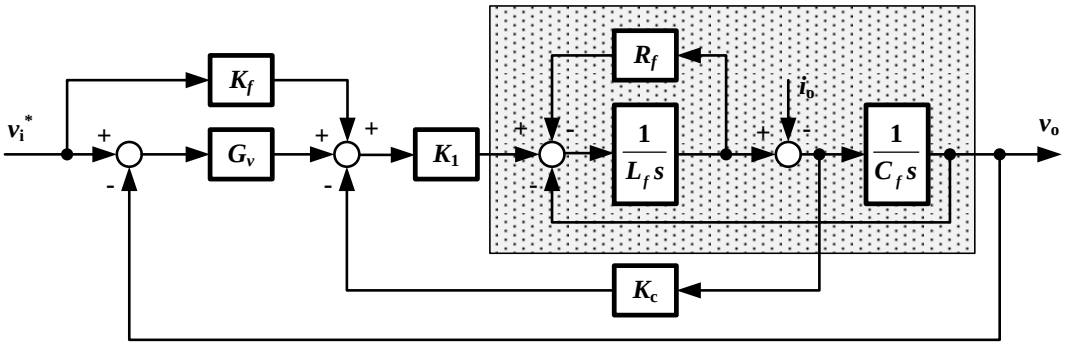


Figure 4.6 Inverter model with instantaneous current sharing scheme.

By replacing G_v in (4.4) and (4.5) with (4.3), the following equations are obtained

$$G = \frac{g_{n2}s^2 + g_{n1}s + g_{n0}}{g_{d4}s^4 + g_{d3}s^3 + g_{d2}s^2 + g_{d1}s + g_{d0}} \tag{4.6}$$

$$g_{n2} = K_1(K_P + K_f)\ ;\ g_{n1} = K_1(2K_P w_c + K_{\mathrm{Res}} + 2K_f w_c)\ ;$$
$$g_{n0} = K_1\left(K_P({w_c}^2 + {w_o}^2) + K_f({w_c}^2 + {w_o}^2) + K_{\mathrm{Res}} w_c\right);$$
$$g_{d4} = C_f L_f\ ;\ g_{d3} = 2w_c C_f L_f + C_f R_f + C_f K_c\ ;$$
$$g_{d2} = C_f L_f({w_c}^2 + {w_o}^2) + 2w_c(C_f R_f + C_f K_c) + K_1 K_P + 1$$
$$g_{d1} = (C_f R_f + C_f K_c)({w_c}^2 + {w_o}^2) + 2K_1 K_P w_c + K_1 K_{\mathrm{Res}} + 2w_c$$
$$g_{d0} = K_1 K_P({w_c}^2 + {w_o}^2) + K_1 K_{\mathrm{Res}} w_c + {w_c}^2 + {w_o}^2$$

$$Z = \frac{z_{n3}s^3 + z_{n2}s^2 + z_{n1}s + z_{n0}}{z_{d4}s^4 + z_{d3}s^3 + z_{d2}s^2 + z_{d1}s + z_{d0}} \tag{4.7}$$

$$z_{n3} = L_f\ ;\ z_{n2} = 2L_f w_c + R_f\ ;\ z_{n1} = L_f({w_c}^2 + {w_o}^2) + 2R_f w_c\ ;$$
$$z_{n0} = R_f({w_c}^2 + {w_o}^2)\ ;\ z_{d4} = L_f C_f$$
$$z_{d3} = 2C_f L_f w_c + C_f R_f + K_1 K_c C_f$$
$$z_{d2} = C_f L_f\left({w_c}^2 + {w_o}^2\right) + 2w_c\left(C_f R_f + K_1 K_c C_f\right) + K_1 K_P + 1$$
$$z_{d1} = \left(C_f R_f + K_1 K_c C_f\right)\left({w_c}^2 + {w_o}^2\right) + K_1(2K_P w_c + K_{\mathrm{Res}}) + 2w_c$$
$$z_{d0} = K_1 K_P({w_c}^2 + {w_o}^2) + K_1 K_{\mathrm{Res}} w_c + {w_c}^2 + {w_o}^2$$

The parallel multi inverter system model is shown in Figure 4.7. In this model, each inverter is treated as a voltage source connected in series with line impedance. All parameter variations including the closed loop voltage gain (G_j), the output impedance of the inverter (Z_j), and line impedance (Z_{lj}), are taken into consideration. In this model, an outer current loop controller, H, is also included for all the inverters. Z_L represents the load impedance and v_o is the load voltage. The reference voltage v^*_i and reference current i^* are same for all inverters.

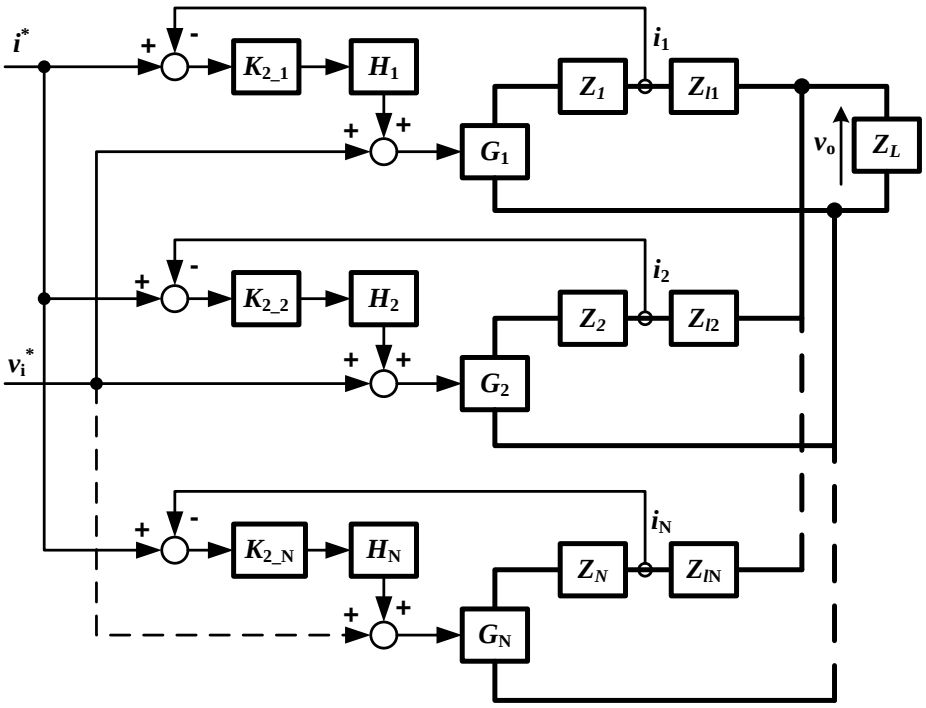


Figure 4.7 The model of the parallel multi inverter system

The system is then described as

$$v^*_{i1} = v^*_{i2} = v^*_{iN} = v^*_i \tag{4.8}$$

$$i^* = \frac{\sum_{j=1}^{N} i_j}{N} \tag{4.9}$$

$$v_o = \left(i_1 + i_2 + \ldots + i_N\right) Z_L \tag{4.10}$$

$$\sum_{j=1}^{N}\left(G_j v^*_i + G_j K_{2\_j} H_j \left[i^* - i_j\right]\right) - N v_o = \sum_{j=1}^{N} i_j \left(Z_j + Z_{lj}\right) \tag{4.11}$$

Replacing i^* in (4.11) with (4.9) and solving for v_o, the output voltage characteristic of the parallel multi inverter system is obtained

$$v_o = \frac{\sum_{j=1}^{N} i_j \left(Z_j + Z_{lj}\right) - \sum_{j=1}^{N}\left(G_j v^*_i\right) + \sum_{j=1}^{N} G_j K_{2\_j} H_j i_j}{\left(\sum_{j=1}^{N} G_j K_{2\_j} H_j \frac{1}{N Z_L} - N\right)} \tag{4.12}$$

To obtain the current sharing characteristic for each inverter, equations (4.9) and (4.12) are inserted into equation (4.11). For clarity, the symbol *'k'* is used to represent the k^{th} inverter.

For the k^{th} inverter, the output current is

$$i_k = \frac{\begin{array}{c}\left(\sum_{j=1}^{N} G_j K_{2\_j} H_j \frac{1}{NZ_L} - N\right)\left(NG_k v^*_i + G_k K_{2\_k} H_k \sum_{\substack{j=1 \\ j\neq k}}^{N} i_j\right) \\ -N\left(\sum_{\substack{j=1 \\ j\neq k}}^{N} i_j \left(Z_j + Z_{lj}\right) - \sum_{j=1}^{N}\left(G_j v^*_i\right) + \sum_{\substack{j=1 \\ j\neq k}}^{N} G_j K_{2\_j} H_j i_j\right)\end{array}}{\begin{array}{l}\left(\sum_{j=1}^{N} G_j K_{2\_j} H_j \frac{1}{NZ_L} - N\right)\left[N\left(Z_k + Z_{lk}\right) - G_k K_{2\_k} H_k \left(1-N\right)\right] \\ +N\left(Z_k + Z_{lk}\right) + NG_k K_{2\_k} H_k\end{array}} \tag{4.13}$$

In this chapter, in which the effect of line impedances is studied, all the parallel connected inverters are assumed to be the same and only the line impedances differ. That is, it is assumed that

$$G_1 = G_2 = G_N = G \tag{4.14}$$

$$Z_1 = Z_2 = Z_N = Z \tag{4.15}$$

$$H_1 = H_2 = H_N = H \tag{4.16}$$

Using this assumption, (4.12) and (4.13) reduces to

$$v_o = \frac{Gv^*_i - \frac{1}{N}\sum_{j=1}^{N} i_j Z_{lj}}{\left(1 + \frac{Z}{NZ_L}\right)} \tag{4.17}$$

$$i_k = \frac{N\left(1 + \frac{Z}{NZ_L}\right)Gv^*_i + \left(1 + \frac{Z}{NZ_L}\right)GK_2 H \sum_{\substack{j=1 \\ j\neq k}}^{N} i_j - NGv^*_i + \sum_{\substack{j=1 \\ j\neq k}}^{N} i_j Z_{lj}}{\left(1 + \left(1 + \frac{Z}{NZ_L}\right)GK_2 H(N-1) - Z_{lk}\right)} \tag{4.18}$$

4.5 Stability and harmonic impedance analysis of parallel multi inverter system

In this section, control system dynamics and stability of the voltage and current control loop are investigated by using the root locus and Bode plot methods.

4.5.1 Stability analysis of the voltage control loop without gain schedulers

From (4.17), the stability of the output voltage only depends on the denominator in which the characteristic equation is

$$1+\frac{Z}{NZ_L}=0 \tag{4.19}$$

From this characteristic equation, the effect of the proportional and resonant gains of the voltage controller (K_P and K_{Res}) on voltage regulation stability are investigated. By replacing Z in (4.19) with (4.7) and separating the factors K_P and K_{Res}, the characteristic equations to find the root locus of K_P and K_{Res}, become (4.20) and (4.21) respectively.

$$1+\frac{K_P\left[n_{kp2}s^2+n_{kp1}s+n_{kp0}\right]}{d_{kp4}s^4+d_{kp3}s^3+d_{kp2}s^2+d_{kp1}s+d_{kp0}}=0 \tag{4.20}$$

$$n_{kp2}=NZ_LK_1\ ;\ n_{kp1}=NZ_LK_1 2w_c\ ;\ n_{kp0}=NZ_LK_1(w_c{}^2+w_o{}^2)\ ;$$

$$d_{kp4}=NZ_LL_fC_f\ ;\ d_{kp3}=NZ_L\left(2w_cL_fC_f+R_fC_f+K_1K_cC_f\right)+L_f$$

$$d_{kp2}=NZ_L\left[L_fC_f(w_c{}^2+w_o{}^2)+2w_cR_fC_f+2w_cK_1K_cC_f+1\right]+2L_fw_c+R_f$$

$$d_{kp1}=NZ_L\left[R_fC_f(w_c{}^2+w_o{}^2)+2w_c+K_1K_cC_f(w_c{}^2+w_o{}^2)+K_1K_{\mathrm{Res}}\right]$$
$$+L_f(w_c{}^2+w_o{}^2)+2R_fw_c\ ;$$

$$d_{kp0}=NZ_L\left(w_c{}^2+w_o{}^2+K_1K_{\mathrm{Res}}w_c\right)+R_f(w_c{}^2+w_o{}^2)$$

$$1+\frac{K_{\mathrm{Res}}\left[n_{kr1}s+n_{kr0}\right]}{d_{kr4}s^4+d_{kr3}s^3+d_{kr2}s^2+d_{kr1}s+d_{kr0}}=0 \tag{4.21}$$

$$n_{kr1}=NZ_LK_1\ ;\ n_{kr0}=NZ_LK_1w_c\ ;d_{kr4}=NZ_LL_fC_f$$

$$d_{kr3}=NZ_L\left(2w_cL_fC_f+R_fC_f+K_1K_cC_f\right)+L_f$$

$$d_{kr2}=NZ_L\left[L_fC_f(w_c{}^2+w_o{}^2)+2w_cR_fC_f+2w_cK_1K_cC_f+K_1K_P+1\right]+2L_fw_c+R_f$$

$$d_{kr1}=NZ_L\left[R_fC_f(w_c{}^2+w_o{}^2)+K_1K_cC_f(w_c{}^2+w_o{}^2)+2K_1K_Pw_c+2w_c\right]$$
$$+L_f(w_c{}^2+w_o{}^2)+2R_fw_c$$

$$d_{kr0}=NZ_L\left[\left(w_c{}^2+w_o{}^2\right)+K_1K_P(w_c{}^2+w_o{}^2)\right]+R_f(w_c{}^2+w_o{}^2)$$

where K_1 is the gain for gain scheduler 1, K_P, K_{Res} and w_c are the proportional gain, resonant gain, and cut off frequency of the PR voltage controller respectively and w_o is the system fundamental frequency. Using equations (4.20) and (4.21), the system values in Table 4.1 and K_1 set to 1, the root locus is plotted at difference K_{Res} values in Figure 4.8. As all parallel connected inverters are assumed identical, the root locus will be the same no matter how many inverters are connected to the system. The system is generally stable because all the poles are located on the left half plane of the imaginary axis. From the plot, when K_P is increased, the system becomes more oscillatory, and the system is most stable when K_{Res} is small. Figure 4.9 shows the root locus plot for (4.21) at different K_P values. The system becomes less stable as K_{Res} increases and should not exceed 46600 to ensure that the system is maintained in the stable region.

Table 4.1 Parameter list

Description	**Value**
Filter Inductance (L_f)	1 mH
Filter Resistance (R_f)	0.2 Ω
Filter Capacitance (C_f)	20 μF
Feed-forward Gain (K_f)	1
Capacitor Current Gain (K_c)	5
Nominal Frequency (w_o)	314.15 rad/s
Cutoff Frequency (w_c)	94.24 rad/s
Number of Parallel Connected Inverter (N)	2
Load Impedance (Z_L)	10 Ω

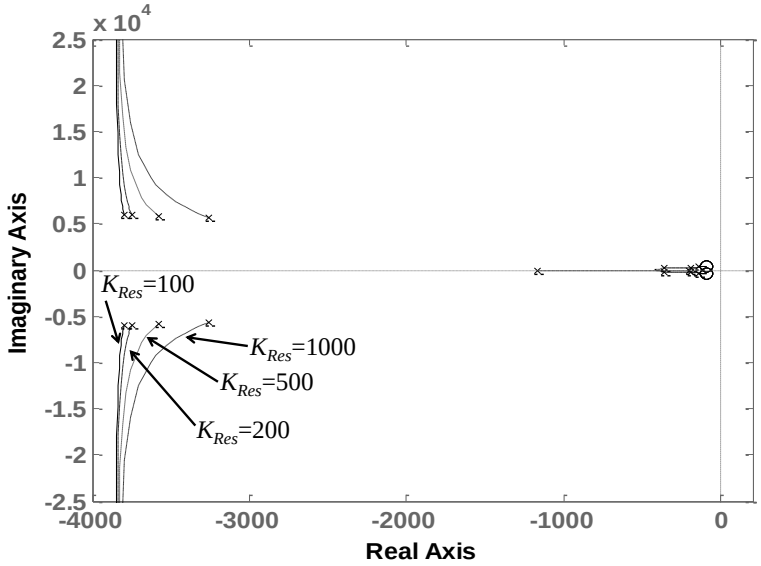


Figure 4.8 Root locus of (4.20) at different value of K_{Res}.

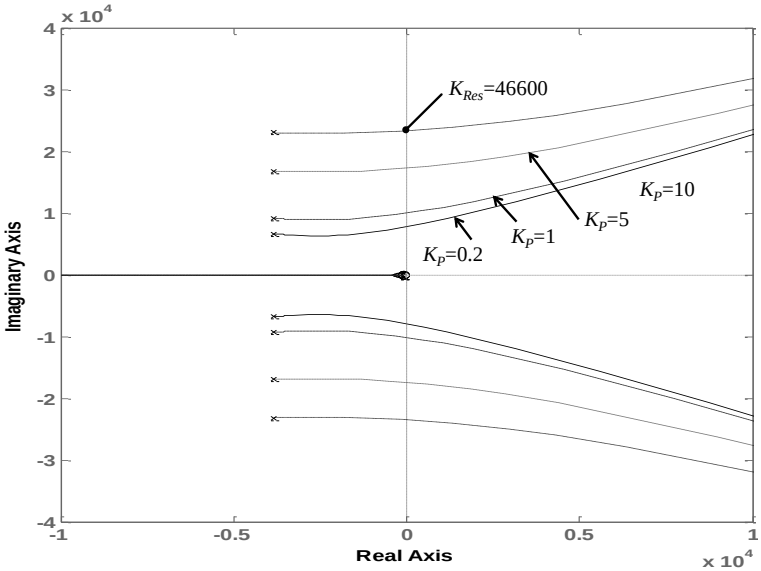


Figure 4.9 Root locus of equation (4.21) at different K_P.

4.5.2 Harmonic impedance

The performance of a control system also depends on harmonic impedance. In the ideal case, the harmonic impedance should be zero in order to minimize the harmonic voltage distortion from the inverter when the load causes distortion [4.10]. Figure 4.10 shows Bode plots for the system output impedance at different K_P values when K_{Res} is 100. From the plot, a larger K_P gives a lower overall harmonic impedance and the peak response occurs at a higher frequency. The phase margins when K_P is 10, 5, 1 and 0.2 are -96.5^o at 1480 Hz, -96.15^o at 863 Hz, -86.6^o at 313 Hz and -71.1^o at 217 Hz, respectively. All cases indicate stable operation.

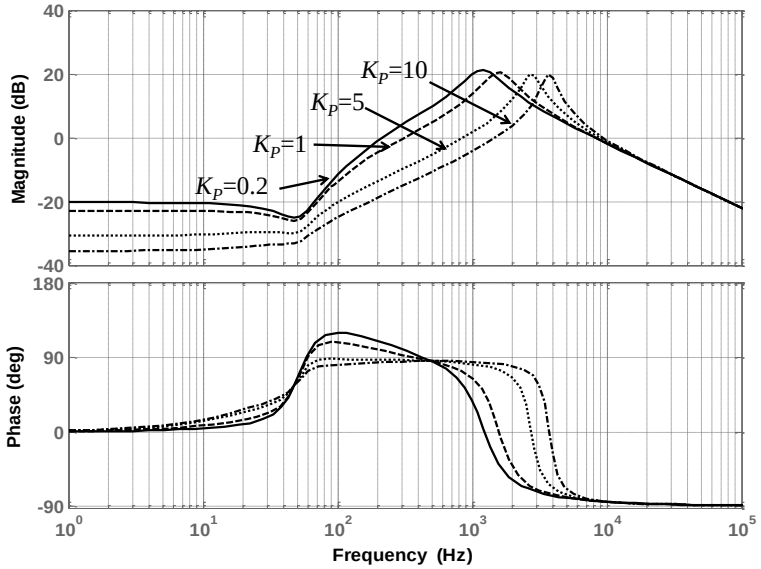


Figure 4.10 Bode plot of output impedance (Z) for K_{Res}=100.

K_P and K_{Res} are selected based on the previous root locus and Bode plots to ensure a stable system and at the same time give low overall harmonic impedance. Lower K_P ensures better system stability but produces higher harmonic impedance. A higher K_P gives lower harmonic impedance but makes the system more oscillatory. So there is a trade-off between the two factors. The values of 5 and 100 have been selected for K_P and K_{Res} respectively.

4.5.3 Stability analysis of current sharing loop without gain schedulers

From (4.18), the stability of the output current of k^{th} inverter depends on the denominator, for which the characteristic equation is given by

$$1+\left(1+\frac{Z}{NZ_L}\right)GK_2H(N-1)-Z_{lk}=0 \tag{4.22}$$

H, as mentioned, is the outer current sharing loop controller. It utilizes a proportional resonance controller, given by (4.23)

$$H=K_{PH}+\frac{K_{ResH}(s+w_c)}{s^2+2w_cs+w_c^{\,2}+w_o^{\,2}} \tag{4.23}$$

where K_{PH} is the proportional gain and K_{ResH} is the resonant gain of the controller.

The effects of these parameters value on the stability of the output current are investigated. Replacing H in (4.22) with (4.23) and rearranging the equation to factor K_{PH} and K_{ResH}, the characteristic equations to find the root locus for K_{PH} and K_{ResH} are (4.24) and (4.25) respectively.

$$1+\frac{K_{PH}\begin{pmatrix}P_{n8}s^8+P_{n7}s^7+P_{n6}s^6+P_{n5}s^5\\+P_{n4}s^4+P_{n3}s^3+P_{n2}s^2+P_{n1}s+P_{n0}\end{pmatrix}}{\begin{matrix}P_{d10}s^{10}+P_{d9}s^9+P_{d8}s^8+P_{d7}s^7+P_{d6}s^6\\+P_{d5}s^5+P_{d4}s^4+P_{d3}s^3+P_{d2}s^2+P_{d1}s+P_{d0}\end{matrix}}=0 \tag{4.24}$$

$$1+\frac{K_{\mathrm{Re}sH}\begin{pmatrix}R_{n7}s^7+R_{n6}s^6+R_{n5}s^5+R_{n4}s^4\\+R_{n3}s^3+R_{n2}s^2+R_{n1}s+R_{n0}\end{pmatrix}}{\begin{matrix}R_{d10}s^{10}+R_{d9}s^9+R_{d8}s^8+R_{d7}s^7+R_{d6}s^6\\+R_{d5}s^5+R_{d4}s^4+R_{d3}s^3+R_{d2}s^2+R_{d1}s+R_{d0}\end{matrix}}=0 \tag{4.25}$$

Detailed equation components for both equations are shown in Appendix B.5.1. Using (4.24), the root locus for K_{PH} plotted for difference K_{ResH} is shown in Figure 4.11, while the root locus for K_{ResH} at difference K_{PH} is plotted using (4.25) and is shown in Figure 4.12. For both plots, values from Table 4.1 are used, K_P is 5, K_{Res} is 100 and K_1 and K_2 are 1. Both root loci indicate that the system is stable because all the poles are located on the left half plane of the imaginary axis. From these plots, increasing K_{PH} makes the system more oscillatory while increasing K_{ResH} makes the system more unstable. The system will become unstable when K_{ResH} exceeds 28,400.

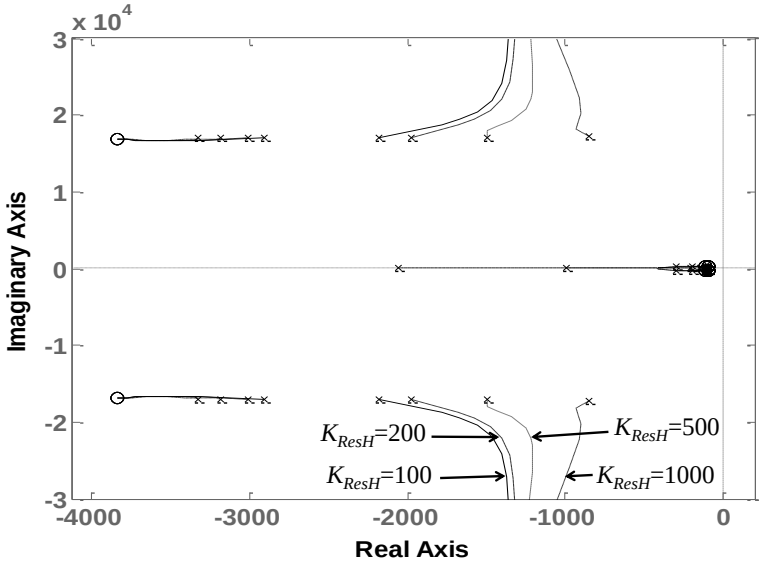


Figure 4.11 Root locus of (4.24) at different values of K_{ResH} . $K_1$and K_2 are 1.

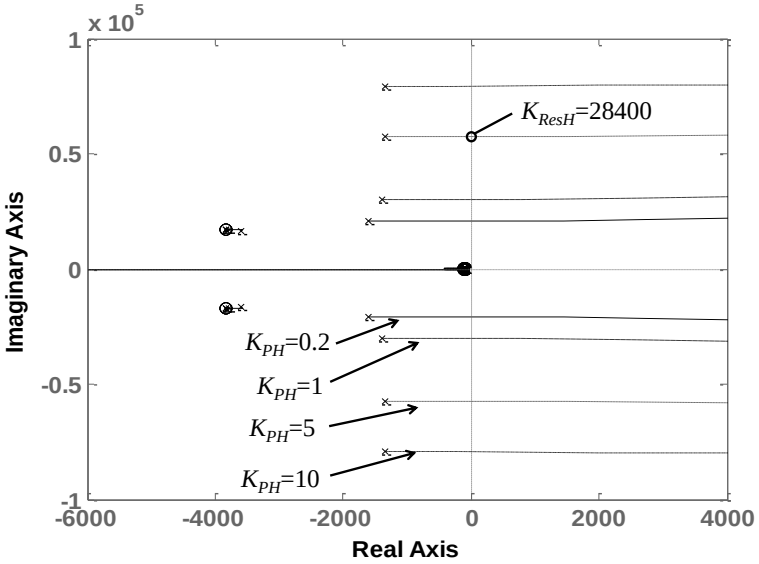


Figure 4.12 Root locus of (4.25) at different value of K_{PH}. $K_1$and K_2 are set to 1.

Bode plots of (4.22) in Figure 4.13 shows the system frequency response at difference values of K_{ResH} when K_{PH} is 0.2. The fundamental frequency gain increases when K_{ResH} is increased. The fundamental frequency gain should be high enough so that the current sharing controller produces a signal to make the inverter output the appropriate current. Based on these considerations, K_{PH} is chosen as 0.2 and K_{ResH} is set to 1000.

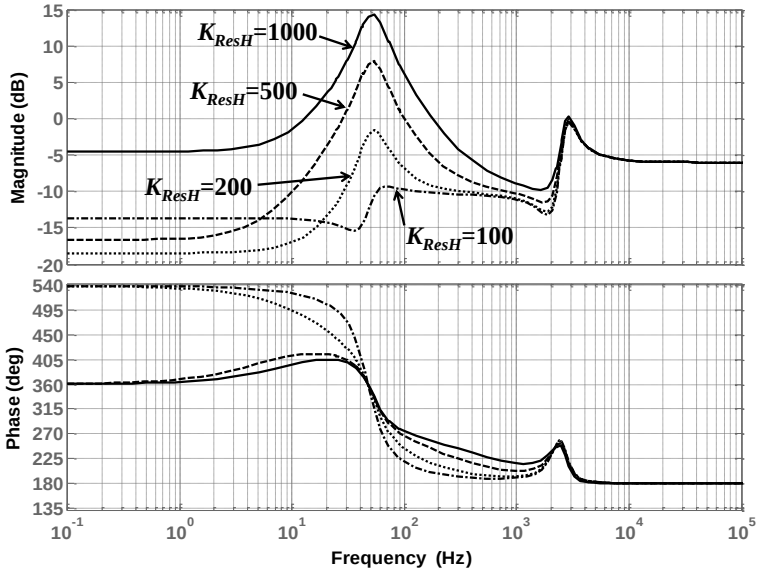


Figure 4.13 Bode plots of $\left[\left(1+\frac{Z}{NZ_L}\right)GH(N-1)-Z_{lk}\right]$ with Z_{lk}=0.5Ω.

4.5.4 Stability analysis of controller with gain schedulers

Adding gain schedulers affects the stability of the system. The gain scheduler technique can be considered as a collection of linear controllers to control a nonlinear system [4.11], so the root locus method can be used to determine the stability of the system. From (4.17), the voltage stability is only affected by K_1 and not K_2. However as explain in section 4.3.2, Gain Scheduler 1 limits the value of K_1 so that it does not make the controlled signal peak amplitude exceeds the DC-link voltage value. By having this limitation, the modulation index will not exceed 1 thereby prevent the system from becoming unstable. This can be proved by investigating the root locus of K_1. By replacing Z in (4.19) with (4.7) and rearrange the equation to factor out K_1, the characteristic equation to find the root locus for K_1becomes

$$1+\frac{K_1\left[n_{k3}s^3+n_{k2}s^2+n_{k1}s+n_{k0}\right]}{d_{k4}s^4+d_{k3}s^3+d_{k2}s^2+d_{k1}s+d_{k0}}=0 \tag{4.26}$$

$$n_{k3}=NZ_LK_cC_f\ ;n_{k2}=NZ_L\left(2w_cK_cC_f+K_P\right);$$
$$n_{k1}=NZ_L\left[K_cC_f(w_c^{\,2}+w_o^{\,2})+2K_Pw_c+K_{\mathrm{Res}}\right];$$
$$n_{k0}=NZ_L\left[K_P(w_c^{\,2}+w_o^{\,2})+K_{\mathrm{Res}}w_c\right];d_{k4}=NZ_LL_fC_f\ ;$$
$$d_{k3}=NZ_L\left(2w_cL_fC_f+R_fC_f\right)+L_f\ ;$$
$$d_{k2}=NZ_L\left(L_fC_f(w_c^{\,2}+w_o^{\,2})+2w_cR_fC_f+1\right)+2L_fw_c+R_f\ ;$$
$$d_{k1}=NZ_L\left(R_fC_f(w_c^{\,2}+w_o^{\,2})+2w_c\right)+L_f(w_c^{\,2}+w_o^{\,2})+2R_fw_c\ ;$$
$$d_{k0}=NZ_L\left(w_c^{\,2}+w_o^{\,2}\right)+R_f(w_c^{\,2}+w_o^{\,2})$$

Using equation (4.26) and the system values from Table 4.1 and Table 4.2, the root locus of K_1 when it is increases from 0 to 2 is plotted and shown in Figure 4.14. From this figure, the voltage is stable for all value of K_1.

As previously stated, current stability is based on the characteristic equation given in (4.22). From this equation, the values of K_1 and K_2 impact the current stability. To investigate the effect of K_2 on the current sharing loop stability, (4.22) is rearrange to factor out K_2 and the characteristic equation becomes (4.27).

$$1+\frac{K_2\begin{pmatrix}T_{n8}s^8+T_{n7}s^7+T_{n6}s^6+T_{n5}s^5\\+T_{n4}s^4+T_{n3}s^3+T_{n2}s^2+T_{n1}s+T_{n0}\end{pmatrix}}{\begin{matrix}T_{d10}s^{10}+T_{d9}s^9+T_{d8}s^8+T_{d7}s^7+T_{d6}s^6\\+T_{d5}s^5+T_{d4}s^4+T_{d3}s^3+T_{d2}s^2+T_{d1}s+T_{d0}\end{matrix}}=0 \tag{4.27}$$

Detail equation (4.27) components are presented in Appendix B.5.2. Using this equation and parameter values from Table 4.1 and Table 4.2, the root locus of K_2 at different K_1 is shown in Figure 4.15. This figure indicates the acceptable range of K_2 that can be applied by gain scheduler 2 to the system so that the system stays in a stable region. Higher values of K_1 makes the output current more oscillatory while higher K_2 make the system more unstable, tending to oscillate. Also lower K_1 reduces the acceptable range of K_2. So in the design stage, the range of K_2 should be selected based on the root locus of K_2 when K_1 is minimum.

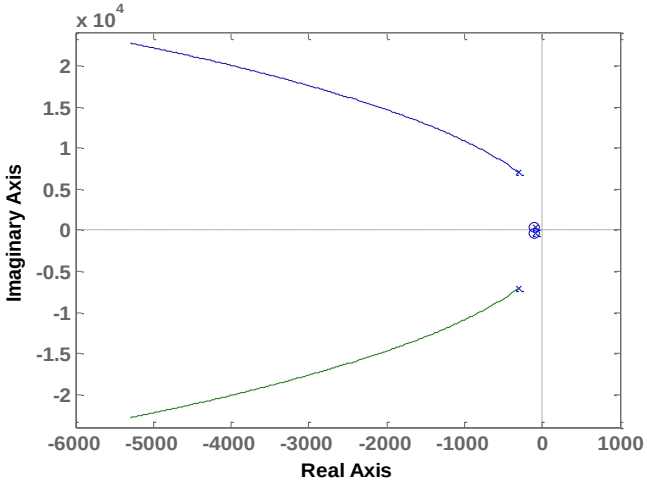


Figure 4.14 Root locus plot of (4.26).

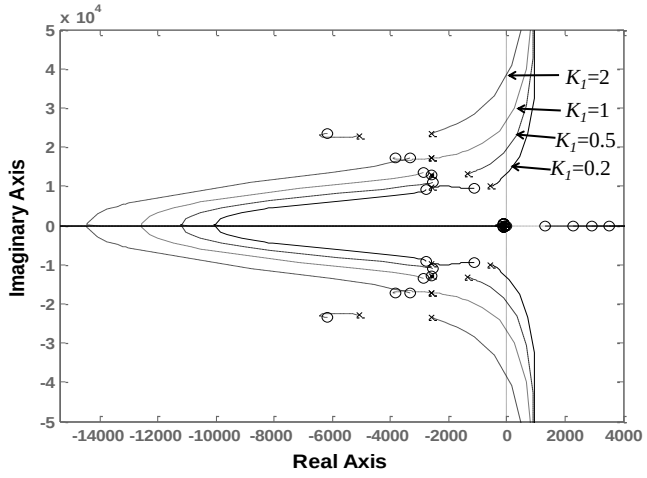


Figure 4.15 Root locus plot of (4.27) using parameter in Table 4.1.

4.6 Simulation results

Several Matlab/Simulink simulations have been conducted to investigate the performance of conventional IACS (PI control without gain schedulers) and improved IACS (PR control with gain schedulers) when varying the line impedance between the inverters and the load. The system configuration is as in figure 4.2 (but for two parallel connected inverters). The communication delay is represented by adding 1 sample delay. System parameters are shown in Table 4.1 and Table 4.2. The simulations are divided into two parts. In the first part, the performance of controller under inductive line impedance is investigated and the second part covers resistive line impedance.

4.6.1 Part 1 (Inductive line impedance)

The line impedance for both inverters is given in Table 4.3. The line inductance of inverter 2, L_{Line2}, is reduced from 5mH to 0 in 0.5mH steps. These simulations are conducted for 4 load conditions, as given in Table 4.4. The simulations are for both controller cases; i) conventional IACS and ii) improved IACS.

Table 4.2 System parameters

Description	Value
DC Link Voltage (V_{DC})	400 V
Reference Voltage (v_i^*)	240 Vrms
Switching Frequency	4.2 kHz
Conventional - Proportional Gain (k_p)	4.5
Conventional - Integral Gain (k_i)	2780
Conventional Current Controller Transfer Function (H_c)	$\frac{40\left(1.6\times10^{-4}s+1\right)}{\left(1\times10^{-3}s+1\right)\left(1\times10^{-5}s+1\right)}$
Voltage Controller Proportional Gain (K_P)	5
Voltage Controller Resonant Gain (K_{Res})	100
Current Controller Proportional Gain (K_{PH})	0.2
Current Controller Resonant Gain (K_{ResH})	1000

Table 4.3 Simulation Part 1 - line impedance value

Description	Value
Inverter 1 Line Resistance (R_{Line1})	0.01 Ω
Inverter 2 Line Resistance (R_{Line2})	0.01 Ω
Inverter 1 Line Inductance (L_{Line1})	5 mH
Inverter 2 Line Inductance (L_{Line2})	5 mH

Table 4.4 Load condition for simulation Part 1 and Part 2

Load Condition	Active Power (W)	Reactive Power (VAr)
1	4000	1600
2	3000	1200
3	2000	800
4	1000	400

Part 1 simulation results for conventional and improved IACS controllers are shown in the parts of Figure 4.16. For the conventional IACS controller, when the line inductance L_{Line2} decreases and the load is increased, the circulating current, the active power difference, and reactive power difference increase linearly. The improved IACS controller reduces the circulating current by 88%. Active power difference is also reduced by 97%, and reactive power difference is improved by 45%. These results indicate that the controller adaptive mechanism is able to improve inverter sharing performance.

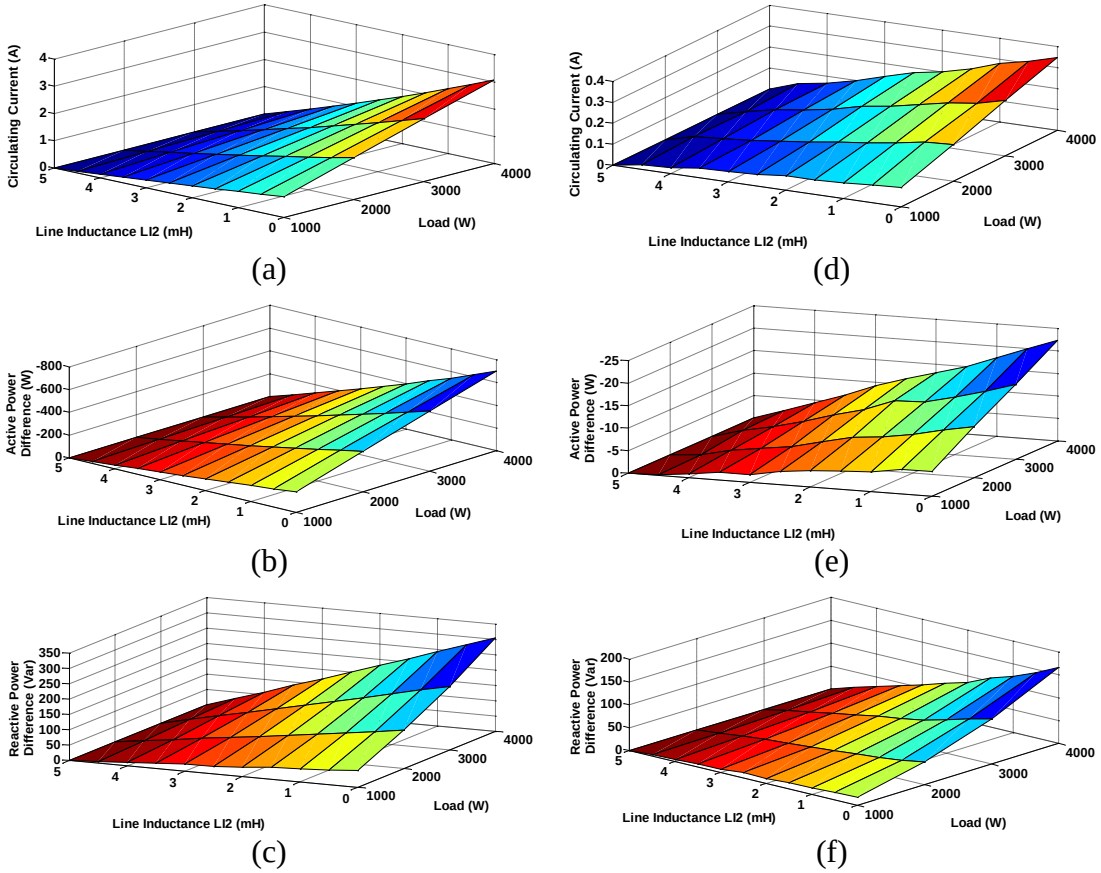


Figure 4.16 Part 1 simulation results under inductive line impedance condition: (a) to (c) conventional IACS; and (d) to (f) improved IACS.

4.6.2 Part 2 (Resistive line impedance)

In the second part, the line impedance for both inverters is as given in Table 4.5. Then the line resistance of inverter 2, R_{Line2}, is reduced from 0.8Ω to 0Ω in 0.08Ω steps. The load conditions and controllers used are the same as in Part 1.

Table 4.5 Simulation part 2 - line impedance value

Description	Value
Inverter 1 Line Resistance (R_{Line1})	0.8 Ω
Inverter 2 Line Resistance (R_{Line2})	0.8 Ω
Inverter 1 Line Inductance (L_{Line1})	0.5 mH
Inverter 2 Line Inductance (L_{Line2})	0.5 mH

The part 2 simulation results, using conventional IACS and improved IACS controllers, are shown in Figure 4.17. With resistive line impedances, the conventional IACS controller system produces a similar pattern as part 1, of circulating current, active power difference, and reactive power difference, when the line resistance, R_{Line2} and the load change as shown in Figure 4.17 parts (a) to (c). From Figure 4.17 parts (d) to (e), the improved IACS controller reduces the circulating current by more than 90%, reduce the active power difference by nearly 83%, and improves the reactive power difference by more than 96%.

Figure 4.18 shows inverter 1 and inverter 2 waveforms for the simulations in part 2 using the conventional IACS controller, while Figure 4.19 shows the waveforms when the improved IACS is used. From these figures, the current and power sharing have improved when using the proposed controller.

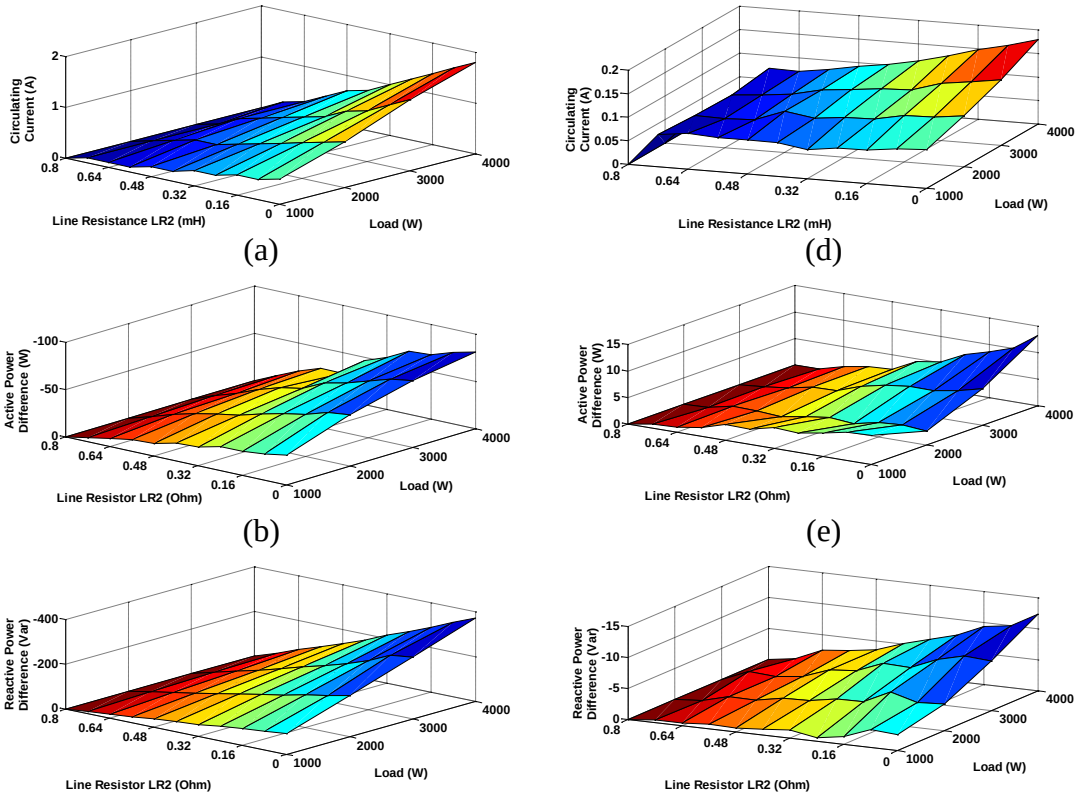


Figure 4.17 Part 2 simulation results under resistive line impedance condition: (a) to (c) conventional IACS; and (d) to(f) improved IACS.

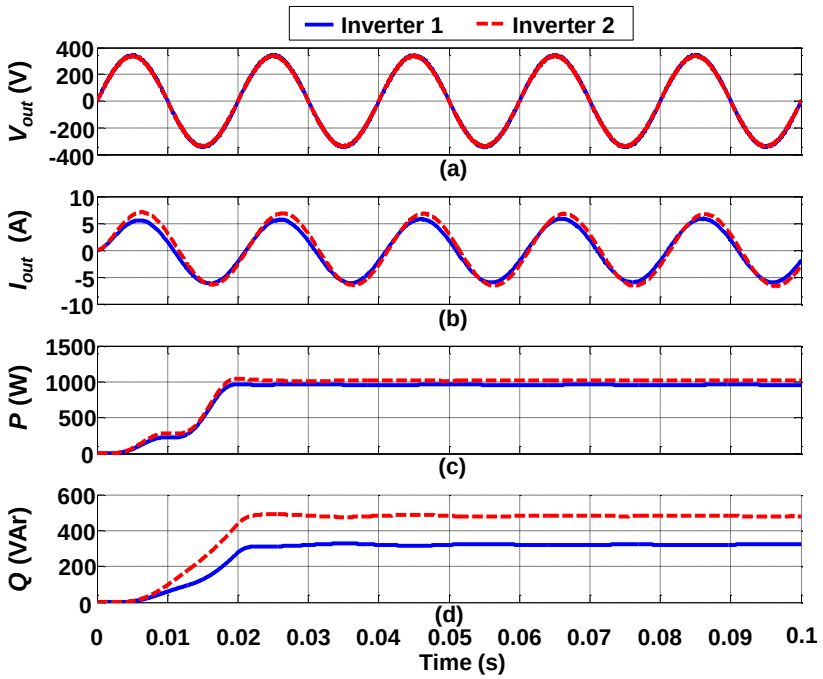


Figure 4.18 Simulation waveforms of inverter 1 and inverter 2 (part 2) using conventional IACS controller when R_{Line2} is 0.08 Ω and load is 2000W 800VAr: (a) inverter voltage; (b) inverter current; (c) active power; and (d) reactive power.

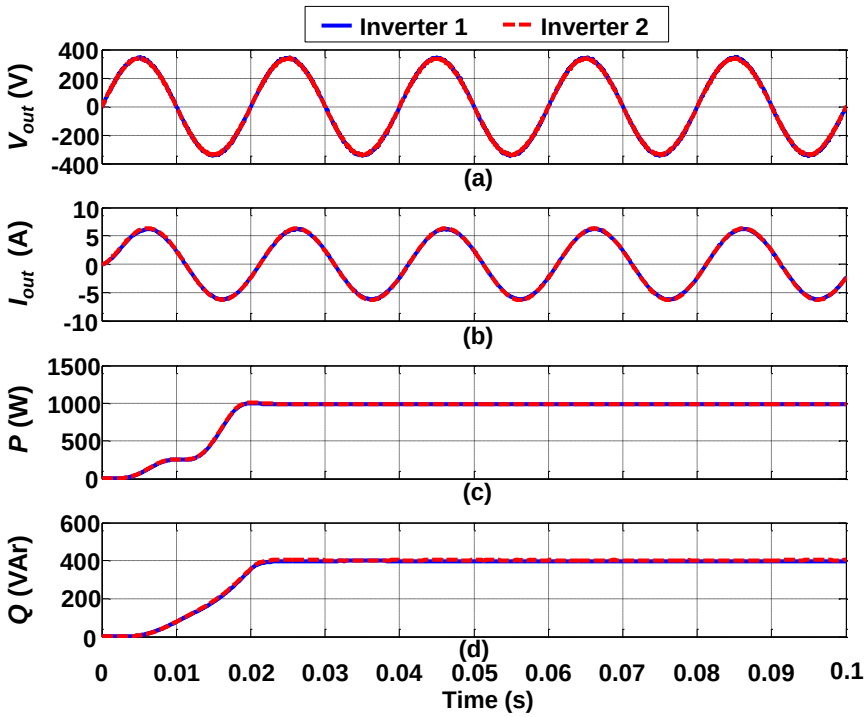


Figure 4.19 Simulation waveforms of inverter 1 and inverter 2 (part 2) using improved IACS controller when R_{Line2} is set at 0.08 Ω and load is 2000 W 800 VAr: (a) inverter voltage, (b) inverter current, (c) active power, and (d) reactive power.

4.7 Experimental results

A microgrid consisting of two single phase IGBT inverters and a local load is built to confirm the effectiveness of the proposed improved IACS controller. The hardware arrangement is shown in Figure 4.20. Each inverter is controlled by an Infineon TriCore™ TC1796B DSP. The switching frequency for both inverters is 4.2 kHz. The LC output filter and other system parameters are listed in Table 4.6.

IACS control is implemented by having a third DSP receive the output current information from both inverters and then calculate the average current before sending it back to each inverter. This signal is then converted back to analogue by a DAC circuit. Experiments are conducted for both conventional and improved IACS controllers.

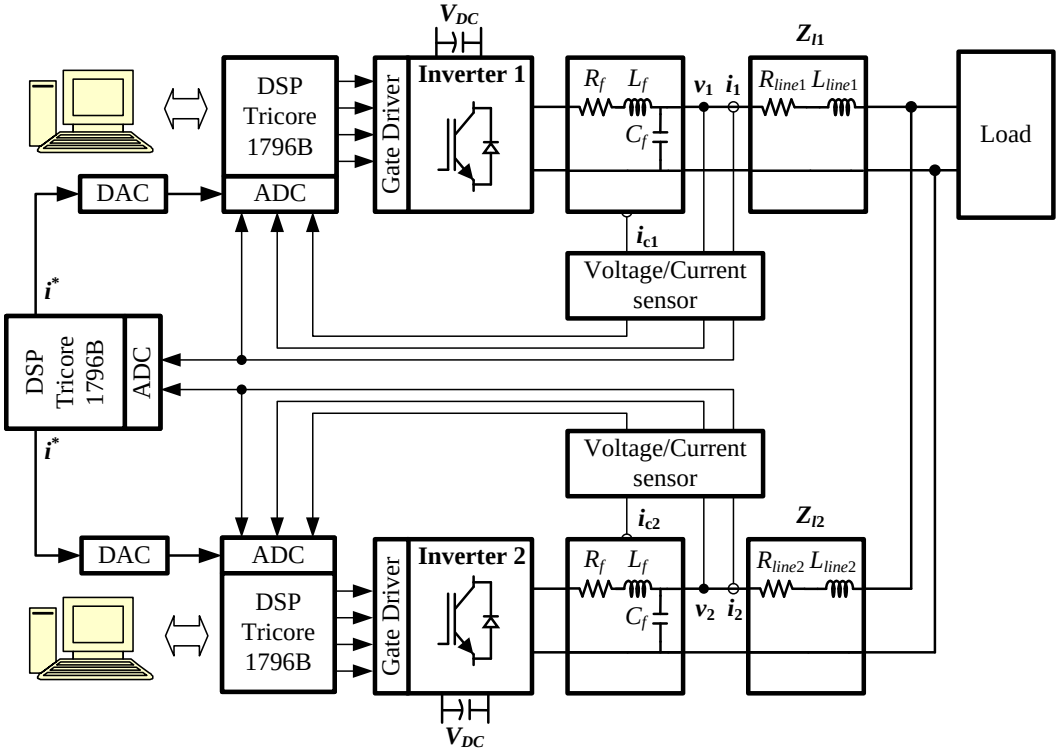
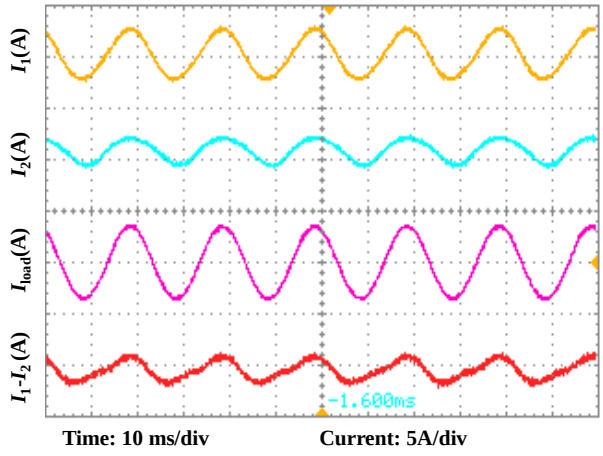


Figure 4.20 Hardware arrangement.

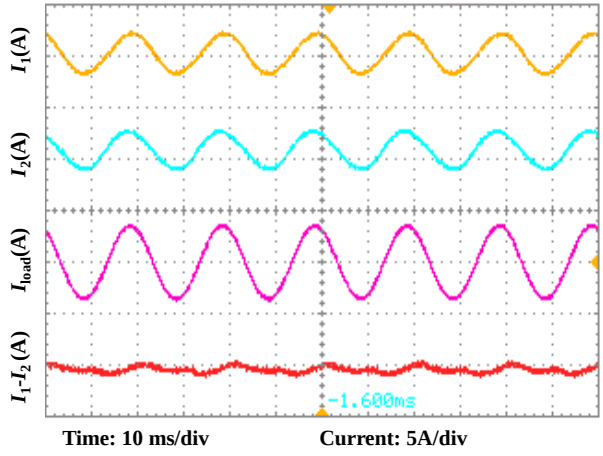
Table 4.6 Parameters for hardware implementation

Description	**Value**
DC Voltage (V_{DC})	200 V
Output Voltage	110 Vrms
Switching Frequency	4.2 kHz
Filter Inductance (L_f)	1 mH
Filter Resistance (R_f)	0.2 Ω
Filter Capacitance (C_f)	20 μF
Inverter 1 Line Impedance (Z_{l1})	3.5 mH
Inverter 2 Line Impedance (Z_{l2})	5 mH
Load	0.5kW

The results for the conventional IACS controller are shown in Figure 4.21 (a) while Figure 4.21 (b) shows the results for the improved IACS controller. From the results, the conventional IACS is unable to compensate the difference of line impedance among the inverters while the improved IACS controller is able to reduce the current difference from 0.97 A to 0.3 A through its adaptive action. The output voltage of each inverter and the load voltage are shown in Figure 4.22. Inverter 1 and inverter 2 output voltage total harmonic distortion (THD) are measured at 1.8% and 1.9% respectively.



(a)



(b)

Figure 4.21 Inverter 1 output current, inverter 2 output current, load current and current difference: a) conventional IACS and b) improved IACS.

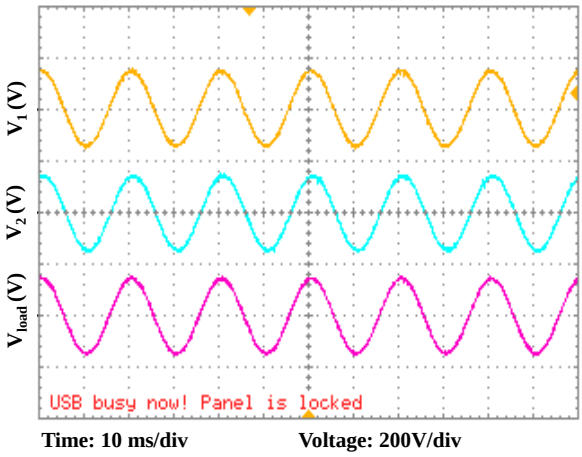


Figure 4.22 Inverter 1 output voltage, inverter 2 output voltage, and load voltage.

4.8 Summary

An improved instantaneous average current sharing control scheme has been proposed that improves the conventional IACS controller which performs poorly under impedance mismatching. PR controller is used (instead of PI control) for voltage regulation and two gain schedulers have been included into the conventional IACS controller. This first gain scheduler changes the modulation index of the modulating signal while the second gain scheduler modifies the current error signal. However it's worth mentioning that the use of PR controller (that increases the order of the system from third order to fourth order) and the addition of two gain schedulers increase the complexity of the overall system. Simulations and experiments substantiate the enhanced performance over the conventional IACS controller when controlling parallel connected inverters under different line impedance conditions.

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Chapter 5

Power Sharing Scheme of Parallel Connected Inverters for an Islanded Microgrid

This chapter presents a new control scheme that permits arbitrary power sharing between parallel connected inverters in a microgrid operating in island mode. The scheme processes active and reactive output power information from all inverters to a central controller which calculates the set-points for each inverter, based on the desired ratios of their output powers. This necessitates adjustment of the inverters' terminal voltages (phase and magnitude) relative to the voltage at the common ac bus. The proposed power-sharing scheme is validated using MATLAB/Simulink simulation and experimental results from three parallel connected inverters with a number of passive loads.

5.1 Background

The proposed IACS control technique presented in Chapter 4 requires high bandwidth communication among parallel connected inverters for average current information sharing. Although it has good current sharing performance, it is more suitable for a DG system that has inverters located in close proximity [5.1]. For a larger DG system, this control approach is difficult to implement. To avoid communications, droop control techniques are commonly used. However, as mentioned in section 2.2.1, the conventional droop technique suffers from problems such as inherent trade-off between voltage regulation and load sharing, poor performance under impedance mismatch, etc. Some proposed improvements to droop control, such as networked droop and hierarchical droop techniques, utilize low bandwidth communications to compensate the mentioned drawbacks. This implies that communication is necessary in order to achieve excellent voltage control and power sharing.

In this chapter, a new control scheme based on an average power sharing technique is presented. It uses low bandwidth communication between an inverter and the central controller for active and reactive power sharing. It can be an alternative to a modified

droop based technique due to its features and advantages, as will be covered in this chapter.

5.2 Circuit configuration

The parallel connected inverter configuration used is shown in Figure 5.1. Each inverter module consists of a three-phase inverter, which is controlled using SPWM; an output power filter; a contactor; two voltage transducers; and an interfacing inductor. The first voltage transducer is after the output power filter, and is followed by a contactor. This transducer measures the inverter's output voltage when it is connected to the microgrid. The second voltage transducer is after the contactor, enabling the inverter to measure the point of common coupling voltage (V_{pcc}) prior and during the synchronization stage. This measured voltage is sent to the reference voltage generator (RVG) to adjust the reference voltage (V^*) so that it is synchronized to V_{pcc}. When an inverter is connected to the microgrid, RVG will provide the reference voltage for the controller. Each inverter output voltage is regulated by a proportional integral (PI) controller in the *d-q* synchronous reference frame, as shown in Figure 5.2. Parameter selection for a PI controller is presented in Appendix C.

The interfacing inductor limits inrush current during inverter synchronization to the ac bus. This inductor dominates the overall line impedance, hence the system becomes inductive. The central controller receives active and reactive power information from each inverter and calculates the active and reactive power references for each inverter. These power references are sent to RVG for phase and amplitude adjustments. Low bandwidth communication is used to share the power information between the inverters. Communication details are considered in sections 5.4.3 and 5.4.4.

The use of a contactor and two voltage transducers enables the inverter to operate in 4 different modes.

- *Mode 1*
  - Contactor is opened.
  - Inverter is not connected to the microgrid.
  - Inverter is not generating voltage.

- *Mode 2*
  - Contactor is opened.
  - Inverter is not connected to the microgrid.
  - Inverter is not generating voltage.
  - Inverter measures V_{pcc}, which is the microgrid network voltage, through the transducer placed after the contactor. This information is used for voltage synchronization.
- *Mode 3*
  - Contactor is opened.
  - Inverter is not connected to microgrid.
  - Inverter is generating voltage.
  - Voltage transducer before the contactor is used to measure the output voltage and inverter builds up voltage in a closed loop mode.
- *Mode 4*
  - Contactor is closed.
  - Inverter is connected to the microgrid.
  - Inverter is generating voltage.
  - Inverter supplies power to the microgrid.

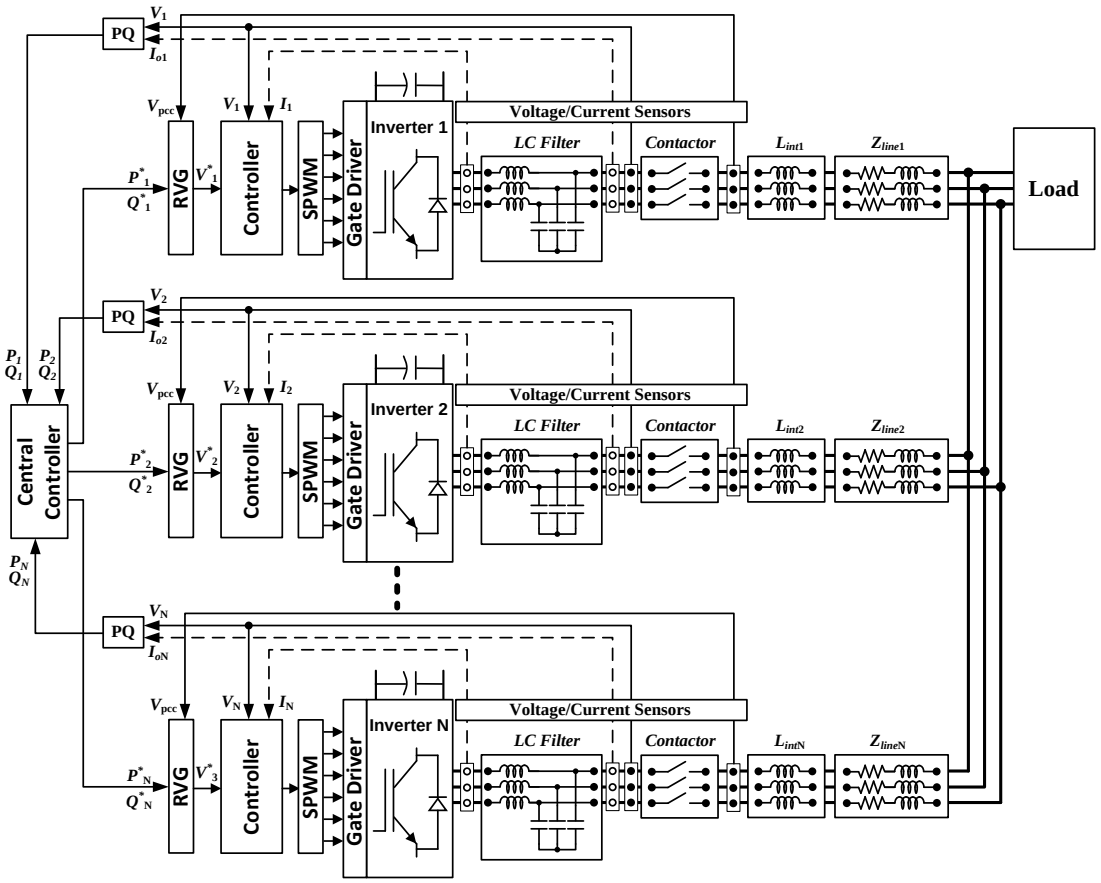


Figure 5.1 Parallel inverter configuration.

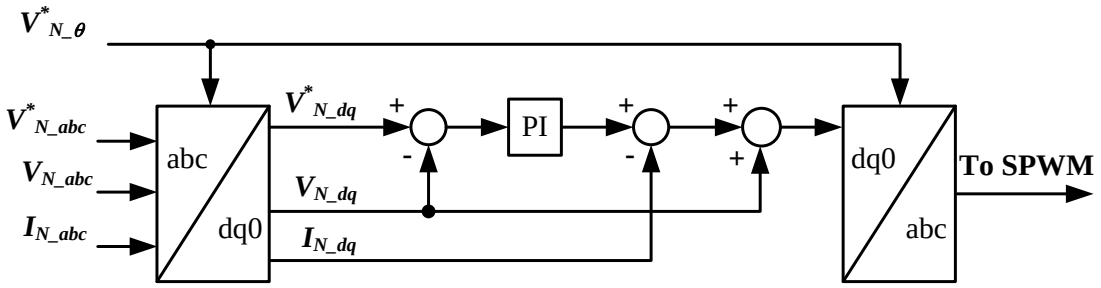


Figure 5.2 Controller for each inverter.

5.3 Synchronization of parallel inverter

Synchronization with minimum error in the phase and magnitude of the connecting inverter compared to those in operation is important for a proper transition from single inverter operation to parallel operation. Improper synchronization creates large inrush current at the moment of connection to the AC bus. Several approaches have been proposed to obtain proper voltage synchronization [5.2-7]. In [5.2], the authors utilized a synchronization control unit (SCU) that uses a microcontroller to generate a synchronous signal and sends it to each parallel connected inverter in every line

cycle. This approach depends on the SCU and synchronization is affected if the SCU fails.

In [5.4-6], a synchronization bus that contains the wired-AND results of a square wave generated by each module, was used. The synchronization signal is then sent to each module for V^* synchronization. There is also precondition controlling of the frequency of the synchronization signal for stabilizing it to the fundamental frequency. In [5.7], the authors proposed a synchronization bus that contains the average value of V^* from all modules. Each inverter sends a V^* signal to the bus through an averaging circuit. The average signal is then sent back to each module and the zero crossing instant of this signal is used to adjust V^* generation. However, such approaches [5.4-7] suffer from complexity and dependent on the communication bandwidth of the synchronization bus. They also lack reliability as the overall system could collapse if a bus fault occurs. A phase locked loop (PLL) approach was adopted in [5.3]. A PLL is an approach which enables one signal to track the phase of another. It allows an output signal to synchronize with a reference input signal in phase and frequency [5.8]. However, there are drawbacks in terms of implementation complexity and it is inherently noise sensitive. Furthermore, loss of synchronization can occur during distorted or unbalanced voltages.

In the next section, the proposed voltage synchronization scheme based on a zero crossing detection technique is presented.

5.3.1 Voltage synchronized, zero crossing detection based scheme

In this approach, zero crossing detection is used to synchronize the connecting inverter's reference voltage frequency and phase to the voltage at the point of common coupling (V_{pcc}). The synchronization flow chart is shown in Figure 5.3. Before the synchronization process starts, ac voltage must be established on the microgrid network. The first inverter, in Mode 4, establishes the microgrid voltage and frequency using an internally generated reference voltage V^* defined as follows:

$$V^*(k) = E\sin\alpha(k) \tag{5.1}$$

$$\begin{aligned} &\alpha(k) = \alpha(k-1) + 360\cdot f\cdot T(k) \\ &if\ \{\alpha(k) \geq 360\} \\ &\alpha(k) = \alpha(k) - 360 \end{aligned} \tag{5.2}$$

$$T(k) = 1/\ f_{sw} \tag{5.3}$$

where E is the preset amplitude, $\alpha(k)$ is the angle, f is the system fundamental frequency, $T(k)$ is the sampling period, and f_{sw} is the switching (sampling) frequency. During synchronization of subsequent inverters, each connecting inverter measures its V_{pcc} and sends this information to its RVG.

If the voltage is already established on the microgrid, the inverter starts the synchronization process from Mode 2. The connecting inverter generates the V^*. The inverter then detects the zero crossing of V_{pcc}. This is the point when V_{pcc} changes from –ve to +ve. Details on the proposed zero crossing technique are covered in section 5.3.2. At this point, the inverter resets $\alpha(k)$ to 0 to ensure that V^* is in phase with V_{pcc}. Then V^* and V_{pcc} waveforms will be as in Figure 5.4 (a). For the ideal case where there is no clock cycle difference among DSPs, this will be the end of the synchronization process. The inverter can be changed to Mode 3, generate voltage and ready to be connected to the microgrid. However, this is usually not the case. The clock cycle difference makes the frequency of V^* differ slightly from V_{pcc}. If the V^* frequency is slightly lower, the V^* waveform moves to the right of the V_{pcc} waveform as shown in Figure 5.4 (b). If the V^* frequency is higher, its waveform moves to the left of the V_{pcc} waveform, as shown in Figure 5.4 (c).

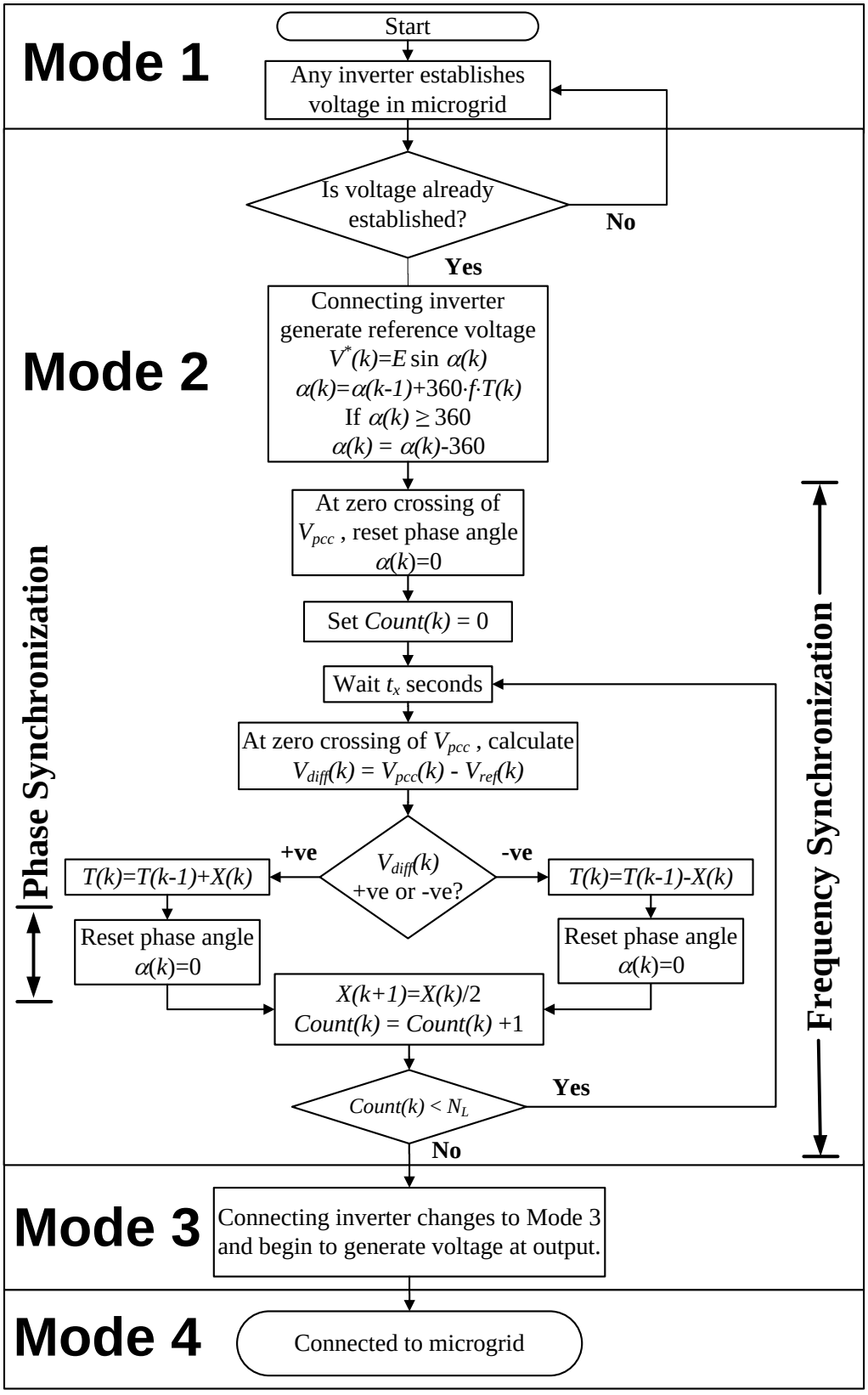


Figure 5.3 Synchronization flow chart.

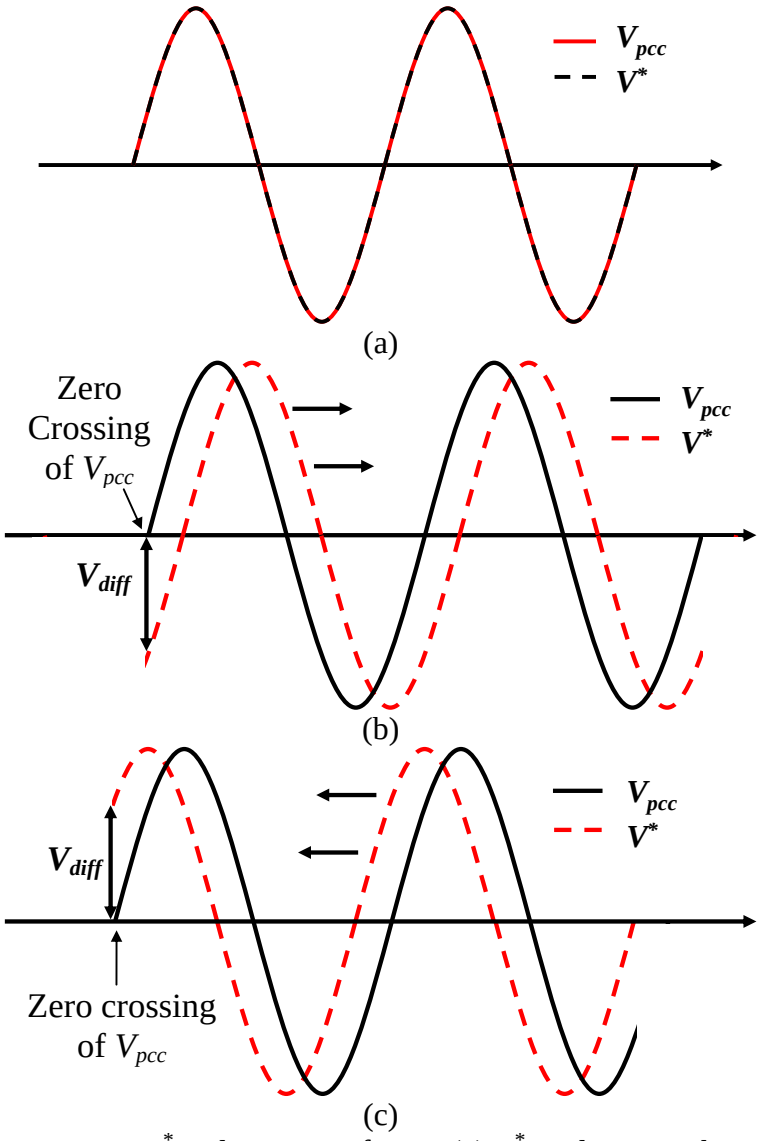


Figure 5.4 V^* and V_{pcc} waveforms. (a) V^* and V_{pcc} in phase with each other. (b) V^* has a lower frequency than V_{pcc}. (c) V^* has a higher frequency than V_{pcc}.

From these observations, some corrective action should be taken. Frequency synchronization can be achieved using Reset-Wait-Measure-Change procedural loops. After generating V^* and setting $\alpha(k)$ to 0, *Count(k)* is set to 0. This is a counter for the frequency synchronization loops. The system then waits for t_x seconds, which is the time to observe the behavior of V^* and then measure the voltage difference $V_{diff}(k)$.

$V_{diff}(k)$ is defined as:

$$V_{diff}(k) = V_{pcc}(k) - V^*(k) \tag{5.4}$$

There are 3 possible values for $V_{diff}(k)$. The value is 0 if the frequency of V^* and V_{pcc} is the same. If V^* frequency is lower than V_{pcc}, $V_{diff}(k)$ will be +ve and if the V^* frequency is higher than V_{pcc}, $V_{diff}(k)$ will be –ve as shown in Figure 5.4 parts (b) and (c) respectively. For a +ve value of $V_{diff}(k)$, the switching period $T(k)$ is increased to increase V^* frequency while for a –ve $V_{diff}(k)$, the switching period $T(k)$ is decreased to decrease V^* frequency as shown in the following equations.

$$\begin{aligned} &if\ V_{diff} > 0 \qquad T(k) = T(k-1) + X(k) \\ &if\ V_{diff} < 0 \qquad T(k) = T(k-1) - X(k) \end{aligned} \tag{5.5}$$

where $X(k)$ is the offset value. The initial value of $X(k)$ is chosen large enough to change the polarity of V_{diff} at the second loop cycle and the value of a thousandth of $T(k)$ is an appropriate selection for $X(k)$. $\alpha(k)$ is then reset back to 0 to ensure V^* is in phase again with V_{pcc}. The process continues, calculating the next cycle value of $X(k)$, namely

$$X(k+1) = \frac{1}{2} X(k) \tag{5.6}$$

The next cycle value of $X(k)$ is set to be half the present value so that the value converges after several loops. $Count(k)$ is then incremented:

$$Count(k) = Count(k) + 1 \tag{5.7}$$

The DSP checks whether $Count(k)$ is smaller or equal to the specified number of loops required, N_L. The frequency synchronization looping repeats if $Count(k)$ has not reach N_L and proceeds to the next stage when N_L is reached. Normally the value of N_L is selected to be more than 10 to get satisfactory results. This is because after 10 iterations, $X(k)$ converges to 0.1% of its initial value.

After the synchronization process, the inverter moves to Mode 3 in which it generates a voltage based on the new synchronized V^*. The inverter is now ready to be connected to the microgrid.

5.3.2 Zero crossing detection

The zero crossing detection method used is based on measurement of the voltage and locating the zero crossing of the instantaneous voltage which is the instant when the voltage changes from –ve to +ve as shown in Figure 5.4 (b).

Due to the use of switching devices, noise problems are unavoidable. Noise will affect the accuracy of zero crossing detection [5.9]. To solve the noise issue, an author has proposed a neural network structure and a logic circuit which produces the time elapsed from the previously detected zero-crossing instant as a feedback signal to the network [5.10]. Although this method gives competitive performance, it is complex and difficult to implement practically [5.11].

Using an averaged instantaneous voltage can give a good approximation of the real instantaneous value. Several instantaneous voltage samples are measured during one switching cycle and then averaged to get the average value. The average instantaneous voltage is given by

$$V(k) = \frac{V(k_1) + V(k_2) + ... + V(k_n)}{n} \tag{5.8}$$

where $V(k_n)$ is the n^{th} instant of the instantaneous voltage and n is the total measured instants. The more measurements, the better the approximation. However, the control bandwidth of the controller should be taken into consideration. More measurements consume control bandwidth. Zero crossing detection is based on this averaged instantaneous voltage value.

To detect the voltage zero crossing, the previous cycle value $V(k\text{-}1)$ is required. The controller then starts to locate the zero crossing by searching for the following conditions:

$$V(k-1) < 0V \quad AND \quad V(k) = 0V \tag{5.9}$$

However, in practice, it is difficult to meet ideal conditions. It is not possible to get an exact 0 value for $V(k)$. A more attainable condition can be used:

$$V(k-1) < 0V \quad AND \quad V(k) > 0V \quad AND \quad V(k) < 0.1\,V \tag{5.10}$$

This condition specifies that *V(k-1)* should be –ve while *V(k)* should fall within the range 0 to 0.1. This is a close enough approximation to a zero value. The controller may need a number of cycles to locate a *V(k)* value that meets these conditions. However, for a fast DSP this detection process may take a few milliseconds.

Another important issue to be considered is system power quality disturbance. A small disturbance deteriorates the position of zero crossing and estimation accuracy. To work around this, a voltage checking algorithm is included to check the consistency of the zero crossing during the synchronization phase. A counter C_{check} is used to ensure that after the system locates the first zero crossing, the next zero crossing detection should only occur when C_{check} equals C_{zero} which is given by:

$$C_{zero} = \frac{f_{sw}}{f} \tag{5.11}$$

where f_{sw} is the sampling frequency and f is the system fundamental frequency. The counter C_{check} is reset to zero every time the system locates the zero crossing. When the system detects that there is no consistency in the measurements, the voltage is assumed have disturbances and waits until stable measurements occurs, to proceed with the synchronization.

5.4 Proposed power sharing technique

This section discusses the proposed power sharing technique, central controller, reference voltage adjustment, and communications.

5.4.1 Central controller

The main function of the central controller is to process the output active and reactive power information from each inverter and then generate active and reactive power references for each unit. A central controller approach offers the advantage of being able to share the total active and reactive powers between the inverters by an arbitrary ratio that can be specified. The power reference calculation only includes power information from microgrid connected inverters, excluding any information from inverters intentionally disconnected from the microgrid or when there is a communication problem with a particular inverter. This is achieved by implementing the communication strategy covered in section 5.4.4. Assuming N inverters connected to the microgrid, the total ratio for active power and reactive powers are defined as follows:

$$r_{PT} = \sum_{j=1}^{N} r_{Pj} \qquad r_{QT} = \sum_{j=1}^{N} r_{Qj} \tag{5.12}$$

where r_{Pj} and r_{Qj} are the active and reactive power ratios set for the j^{th} inverter respectively. The active and reactive power references for the j^{th} inverter are:

$$P_j^*(k) = \frac{r_{Pj}}{r_{PT}} \sum_{h=1}^{N} P_h(k-1) \qquad Q_j^*(k) = \frac{r_{Qj}}{r_{QT}} \sum_{h=1}^{N} Q_h(k-1) \tag{5.13}$$

where P_h and Q_h are the output active and reactive powers from the h^{th} inverter respectively.

5.4.2 Reference voltage adjustment

When the RVG of an inverter receives the power references from the central controller, it calculates the active and reactive power differences. The active and reactive power differences of the j^{th} inverter are:

$$P_{\Delta j}(k) = P_j^*(k) - P_j(k-1) \qquad Q_{\Delta j}(k) = Q_j^*(k) - Q_j(k-1) \tag{5.14}$$

From these power differences, the RVG adjusts the reference voltage in order to force the inverter active and reactive output powers to follow their references. The voltage adjustment is divided into two stages, viz., phase adjustment and amplitude adjustment. As stated, the system impedance is assumed to be dominated by inductive reactance, so the active power can be adjusted by varying the reference voltage phase at the filter bus relative to that of the common ac bus. On the other hand, the reactive power is changed by adjusting the amplitude of the reference voltage. There is no change in the frequency of the reference voltage. A more detail description is presented in the following subsections.

a) Phase adjustment

The RVG monitors $P_{\Delta j}$ and adjusts its power angle α_j based on the following conditions:

$$\begin{aligned}
&if\,(P_{\Delta j} > P_{aj}) && \alpha_j(k) = \alpha_j(k-1) + \Delta\alpha_{xj} \\
&if\,(P_{bj} < P_{\Delta j} \le P_{aj}) && \alpha_j(k) = \alpha_j(k-1) + \Delta\alpha_{yj} \\
&if\,(P_{cj} < P_{\Delta j} \le P_{bj}) && \alpha_j(k) = \alpha_j(k-1) + \Delta\alpha_{zj} \\
&if\,(-P_{cj} < P_{\Delta j} \le P_{cj}) && \alpha_j(k) = \alpha_j(k-1) + 0 \\
&if\,(-P_{bj} < P_{\Delta j} \le -P_{cj}) && \alpha_j(k) = \alpha_j(k-1) - \Delta\alpha_{zj} \\
&if\,(-P_{aj} < P_{\Delta j} \le -P_{bj}) && \alpha_j(k) = \alpha_j(k-1) - \Delta\alpha_{yj} \\
&f\,(P_{\Delta j} \le -P_{aj}) && \alpha_j(k) = \alpha_j(k-1) - \Delta\alpha_{xj}
\end{aligned} \tag{5.15}$$

where P_{aj}, P_{bj} and P_{cj} are the active power limits of the j^{th} inverter and $\Delta\alpha_{xj}$, $\Delta\alpha_{yj}$ and $\Delta\alpha_{zj}$ are the adjustment angles for the j^{th} inverter, at every sampling time. The active power limits are defined as:

$$P_{aj} = \tfrac{1}{20} P_j^0 \qquad P_{bj} = \tfrac{1}{40} P_j^0 \qquad P_{cj} = \tfrac{1}{100} P_j^0 \tag{5.16}$$

where P_j^0 is rated active power of the j^{th} inverter. These active power limits are selected to ensure power adjustments are done in steps. The given P_{cj} value ensures no power fluctuation occurs at the end of the power transient.

Figure 5.5 (a) shows the timing diagrams used to assist in deriving expression for the adjustment angles for the proposed power sharing. ΔP_{xj}, ΔP_{yj} and ΔP_{zj} are the changes in the j^{th} inverter active power output as a result of different angle adjustments, T_d is power adjustment period, and T_r is the maximum time needed to

change the inverter output power from an initial operating condition to the desired new operating point. Selection of the T_r value impacts performance and stability. Time domain stability analysis is conducted for several T_r values and the results are presented in Appendix C.5. T_r can be divided into three regions with different output power adjustment levels, defined as follows:

$$T_a = \tfrac{2}{3} T_r \qquad T_b = T_c = \tfrac{1}{6} T_r \tag{5.17}$$

T_a occupies two third of T_r because large power adjustments take place during this period, while T_b and T_c, each take 1/6 of T_r because only small power adjustments are needed during these period. These values can give faster power adjustment during the initial transient and slower response at the end.

Assuming an inverter is just connected to the microgrid and required to output its rated active power, and the voltage magnitude at the filter bus and common ac bus remain constant within each sampling period, the following proportional expressions are obtained:

$$\frac{\Delta P_{xj}}{T_d} = \frac{P_j^0 - P_{aj}}{T_a} \qquad \frac{\Delta P_{yj}}{T_d} = \frac{P_{aj} - P_{bj}}{T_b} \qquad \frac{\Delta P_{zj}}{T_d} = \frac{P_{bj} - P_{cj}}{T_c} \tag{5.18}$$

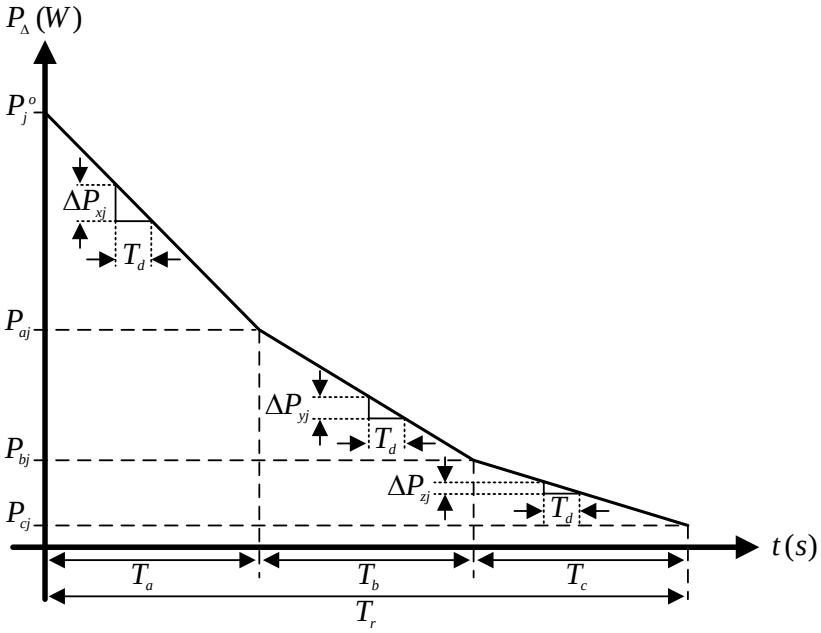
The active power injected by an inverter into the common ac bus for the inductive system given in (3.3) is rearranged as follows (assuming $E \approx V$) to obtain an expression for the adjustment angle:

$$\alpha = \sin^{-1}\left[\frac{PX}{V^2}\right] \tag{5.19}$$

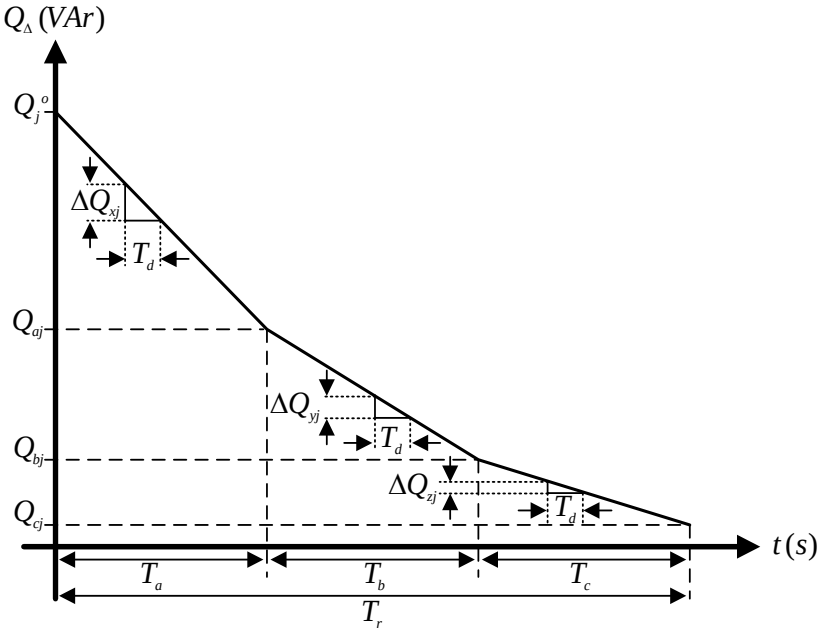
From this equation, the following expressions for adjustment angles can be obtained by replacing ΔP_x, ΔP_y and ΔP_z from (5.18), respectively, into the P term in (5.19).

$$\begin{aligned}
\Delta\alpha_{xj} &= \sin^{-1}\left[\frac{T_d}{T_a}\frac{\left(P_j^{\,0} - P_{aj}\right)X_j}{V^2}\right] \\
\Delta\alpha_{yj} &= \sin^{-1}\left[\frac{T_d}{T_b}\frac{\left(P_{aj} - P_{bj}\right)X_j}{V^2}\right] \\
\Delta\alpha_{zj} &= \sin^{-1}\left[\frac{T_d}{T_c}\frac{\left(P_{bj} - P_{cj}\right)X_j}{V^2}\right]
\end{aligned} \tag{5.20}$$

Adding or subtracting an adjustment value $\Delta\alpha_{xj}$ to the angle α_j produces rapid change in active power from the j^{th} inverter, while adjustment values $\Delta\alpha_{yj}$ and $\Delta\alpha_{zj}$ produce relatively slower changes in active power. When $|P_{\Delta j}|$ is between P_{bj} and P_{cj}, even slower adjustment is needed to avoid active power output fluctuation around the set point.



(a)



(b)

Figure 5.5 Time diagrams for the voltage adjustment parameters: a) phase adjustment and b) amplitude adjustment.

b) Amplitude adjustment

The RVG also monitors $Q_{\Delta j}$ and adjusts the reference voltage amplitude simultaneously as the load angle adjustment in the previous step. Adjustments to the reference voltage amplitude are based on the following conditions:

$$\begin{aligned}
&if\,(Q_{\Delta j} > Q_{aj}) && E_j(k) = E_j(k-1) + \Delta E_{xj} \\
&if\,(Q_{bj} < Q_{\Delta j} \le Q_{aj}) && E_j(k) = E_j(k-1) + \Delta E_{yj} \\
&if\,(Q_{cj} < Q_{\Delta j} \le Q_{bj}) && E_j(k) = E_j(k-1) + \Delta E_{zj} \\
&if\,(-Q_{cj} < Q_{\Delta j} \le Q_{cj}) && E_j(k) = E_j(k-1) + 0 \\
&if\,(-Q_{bj} < Q_{\Delta j} \le -Q_{cj}) && E_j(k) = E_j(k-1) - \Delta E_{zj} \\
&if\,(-Q_{aj} < Q_{\Delta j} \le -Q_{bj}) && E_j(k) = E_j(k-1) - \Delta E_{yj} \\
&f\,(Q_{\Delta j} \le -Q_{aj}) && E_j(k) = E_j(k-1) - \Delta E_{xj}
\end{aligned} \tag{5.21}$$

where Q_{aj}, Q_{bj} and Q_{cj} are the active power limits of the j^{th} inverter and ΔE_{xj}, ΔE_{yj} and ΔE_{zj} are the amplitude adjustments for the j^{th} inverter at every sampling time. The active power limits are defined as:

$$Q_{aj} = \tfrac{1}{20} Q_j^0 \qquad Q_{bj} = \tfrac{1}{40} Q_j^0 \qquad Q_{cj} = \tfrac{1}{100} Q_j^0 \tag{5.22}$$

where Q_j^0 is rated reactive power of the j^{th} inverter. The reasons for selecting these parameters are the same as those in the previous subsection (5.4.2 a).

The time diagram to assist in derivation of the expression for the amplitude adjustments is shown in Figure 5.5 (b). ΔQ_{xj}, ΔQ_{yj} and ΔQ_{zj} are the changes in the j^{th} inverter reactive power output as a result of different amplitude adjustments.

Assuming an inverter is just connected to the microgrid and required to output its rated reactive power, the following proportional expression are obtained:

$$\frac{\Delta Q_{xj}}{T_d} = \frac{Q_j^0 - Q_{aj}}{T_a} \qquad \frac{\Delta Q_{yj}}{T_d} = \frac{Q_{aj} - Q_{bj}}{T_b} \qquad \frac{\Delta Q_{zj}}{T_d} = \frac{Q_{bj} - Q_{cj}}{T_c} \tag{5.23}$$

The reactive power injected by an inverter into the common ac bus given in (3.4) is rearranged as follows (with the assumption that $\alpha \approx 0$) to obtain the expression for the amplitude adjustments:

$$E - V = Q\frac{X}{V} = \Delta E \tag{5.24}$$

From this equation, the following expressions for amplitude adjustments can be obtained by replacing ΔQ_x, ΔQ_y and ΔQ_z from (5.23), respectively, into the Q term in (5.24).

$$\begin{aligned}\Delta E_{xj} &= \left(Q_j^{\,0} - Q_{aj}\right)\frac{T_d}{T_a}\frac{X_j}{V}\\ \Delta E_{yj} &= \left(Q_{aj} - Q_{bj}\right)\frac{T_d}{T_b}\frac{X_j}{V}\\ \Delta E_{zj} &= \left(Q_{bj} - Q_{cj}\right)\frac{T_d}{T_c}\frac{X_j}{V}\end{aligned} \tag{5.25}$$

The summarized reference voltage adjustment steps performed by the RVG are shown in Figure 5.6.

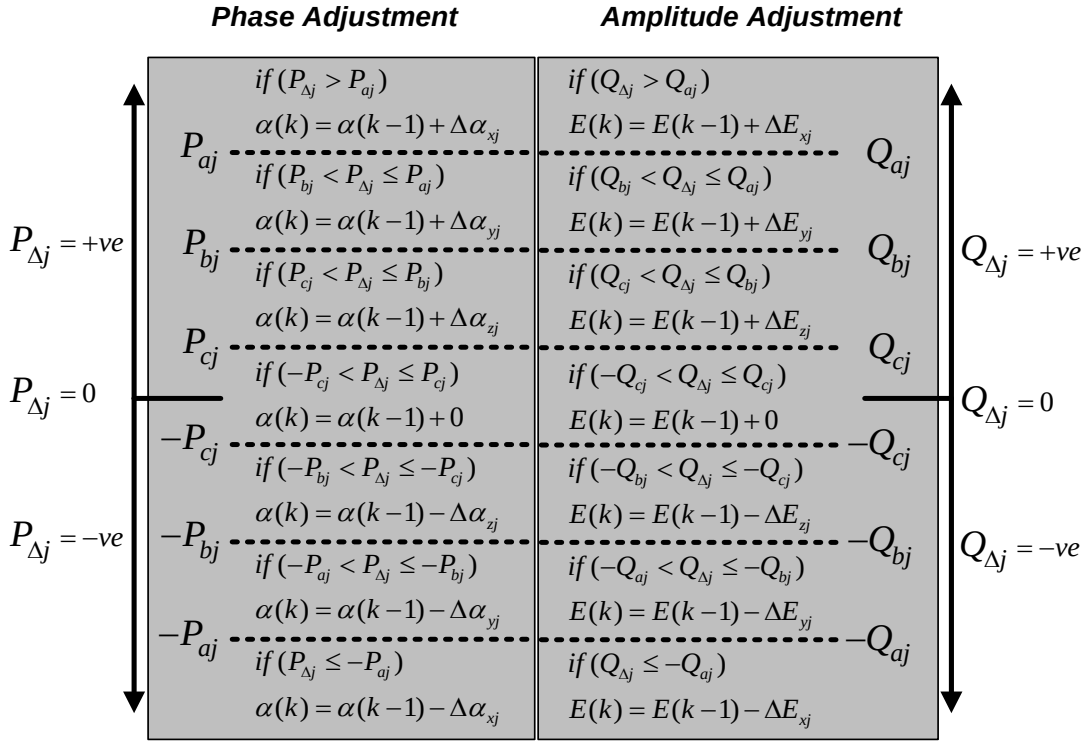


Figure 5.6 Illustration of the steps needed for simultaneous adjustment of the phase and amplitude of the inverter reference voltage.

5.4.3 Communication structure

The control technique requires low-bandwidth communication for active and reactive power information exchange between each inverter and the central controller. The communication type may vary depending on inverter unit location and the available communication structure. For example, in rural areas, company intranet and a dedicated website can be used for communication as proposed in [5.12]. If the inverters are located in the same building but separated distant from each other, the local area network communication can be used [5.13].

The experimentation in this chapter uses communication based on PWM signals outputted by each DSP and converted to dc at the target destination using low pass filters. The PWM frequency used is 10 kHz, which is higher than the inverter control switching frequency (4.2kHz). This frequency is adopted so that small filters can be used to filter the PWM carrier signal from the dc component.

5.4.4 Communication strategy

When considering any control strategy that uses communication, it is important to ensure that the system does not collapse during a communication failure. In the proposed power sharing technique, the following communication strategy is used to ensure that the system continues to operate safely even when there is a communication failure between the inverters and the central controller. The flow chart and PWM signals diagram for the proposed communication strategy are shown in Figure 5.7 parts (a) and (b) respectively.

a) Communication from inverter to central controller

The communication strategy is implemented such that duty cycles of 0.8 and 0.1 are used to modulate rated and minimum power (active and reactive power) respectively. A duty cycle of 0 is used to send information that the inverter is not connected to the microgrid.

b) Communication from the central controller to the inverter

A duty cycle of 0.8 is used to modulate maximum active and reactive power references and duty cycle of 0.1 is used to modulate the minimum active and reactive

power references. When the central controller detects that an inverter is not connected to microgrid (due to intentional disconnection or communication loss), it sends information with a duty cycle of 0 to that particular inverter.

c) Communication failure

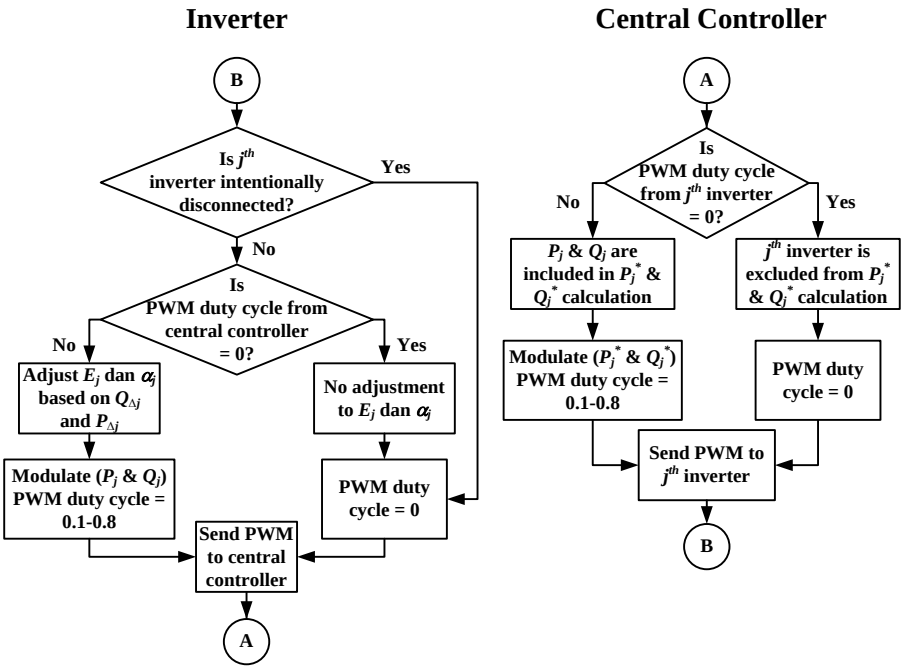
This communication failure can be classified into two cases; loss of communication from inverter to central controller and/or loss of communication from central controller to an inverter.

In the first case, the central controller receives the same information as with the condition when an inverter is sending information with a duty cycle of 0. It assumes that the particular inverter is not connected to the microgrid and excludes it from calculation of the power references. The central controller sends information to that particular inverter with a duty cycle of 0.

For the second case, the inverter receives the same information for the condition when the central controller is sending information with a duty cycle of 0. For both cases, the inverter detects that there is a communication issue because it is still supplying power to the microgrid and expects valid power references.

When this occurs, the RVG of the particular inverter stops making any reference voltage (phase and amplitude) changes and power continues to be supplied to the microgrid based on the recent state of its output voltage. At the same time, it should send its power information with a duty cycle of 0 to the central controller to avoid its power being calculated in the power references calculation. The last step is crucial for the second case because if the inverter continues sending its actual power information to the central controller, this will results in the wrong power references been sent to the other inverters.

At this stage, the inverter is programmed to send its actual power information to the central controller every 0.1s to check whether the communication problem still exists or not. If it still does not receive a proper power reference from the central controller, it will resend the power information with a duty cycle of 0. These steps are repeated until the communication issues are resolved.



(a)

Information	PWM Signals		
	Origin	Destination (before low-pass filter)	
		Normal	Communication loss
From inverter P_j or Q_j (min)	D = 0.1, $1/f_{comm}$	D = 0.1, $1/f_{comm}$	D = 0, $1/f_{comm}$
From central controller P^*_j or Q^*_j (min)	D = 0.1, $1/f_{comm}$	D = 0.1, $1/f_{comm}$	D = 0, $1/f_{comm}$
From inverter P_j or Q_j (max)	D = 0.8, $1/f_{comm}$	D = 0.8, $1/f_{comm}$	D = 0, $1/f_{comm}$
From central controller P^*_j or Q^*_j (max)	D = 0.8, $1/f_{comm}$	D = 0.8, $1/f_{comm}$	D = 0, $1/f_{comm}$
Intentional disconnection	D = 0, $1/f_{comm}$	D = 0, $1/f_{comm}$	D = 0, $1/f_{comm}$

(b)

Figure 5.7 Communication strategy between inverter and central controller: (a) flow chart and (b) PWM signals.

5.5 Simulation results

This section presents Matlab/Simulink simulations to validate the performance of the proposed power-sharing scheme. The microgrid shown in Figure 5.1 comprises three parallel inverters and loads, with parameters listed in Table 5.1. The robustness of the proposed controller to impedance mismatch is investigated by using different interfacing inductance on all inverters.

Table 5.1 System parameters

Description		**Symbol**	**Value**
DC link voltage		V_{DC}	150 V
Reference voltage		V^*	60 V (peak)
Switching frequency		f_{sw}	4.2 kHz
System frequency		f	50 Hz
Communication frequency		f_{comm}	10 kHz
Proportional gain		K_p	2
Integral gain		K_i	800
Initial switching period		$T(0)$	$1/f_{sw}$ s
Initial offset value		$X(0)$	$T(0)$/1000 s
Waiting time		t_x	5 s
Counter limit		N_L	12
Power adjustment period		T_d	5 ms
Max power adjustment time		T_r	600 ms
Filter inductance (all)		L_f	2 mH
Filter capacitance (all)		C_f	30 μF
Interfacing inductance 1		L_{int1}	5 mH
Interfacing inductance 2		L_{int2}	3.75 mH
Interfacing inductance 3		L_{int3}	6.2 mH
Line impedance 1		Z_{line1}	0.3 Ω
Line impedance 2		Z_{line2}	0.2 Ω
Line impedance 3		Z_{line3}	0.4 Ω
Load 1 (R load)			440 W
Load 2 (R load)			880 W
Load 3 (RL load)			440W/ 60VAr
Load 4 (RL load)			760W / 215VAr
Nonlinear Load			180 W
Inverter 1 Rating			0.5 kW
Inverter 2 Rating			0.5 kW
Inverter 3 Rating			0.8 kW
Part I	P ratio	$R_{P1} : R_{P2} : R_{P3}$	1:1:1
	Q ratio	$R_{Q1} : R_{Q2} : R_{Q3}$	1:1:1
Part II, III and IV	P ratio	$R_{P1} : R_{P2} : R_{P3}$	1:2:4
	Q ratio	$R_{Q1} : R_{Q2} : R_{Q3}$	1:1:1
Part V	P ratio	$R_{P1} : R_{P2} : R_{P3}$	5:5:8
	Q ratio	$R_{Q1} : R_{Q2} : R_{Q3}$	5:5:8
Part VI	P ratio	$R_{P1} : R_{P2} : R_{P3}$	1:1:1 → 1:2:4 →1:1:1
	Q ratio	$R_{Q1} : R_{Q2} : R_{Q3}$	1:1:1 → 1:2:4 →1:1:1
Part I – *P-α* droop coefficient		m	0.001 rad/(W.s)
Part I – *Q-E* droop coefficient		n	0.001 (V/VAr)

The simulation results are divided into six parts. Part I compares the dynamic performance of the proposed power-sharing scheme with conventional droop control under similar operating conditions. Part II presents the scheme performance with different power ratios assigned to each inverter. In part III, the simulation results are for communication loss from inverter 1 to the central controller while part IV presents simulation results when there is communication loss from the central controller to inverter 2. The proposed scheme, with power ratios set based on the rating of inverters, are presented in part V. Part VI presents the proposed scheme performance when power ratios are changed during inverter operation.

5.5.1 Simulation Part I – Proposed scheme versus conventional droop

Initially, only inverter 1 supplies load 1. At time t = 0.1s, a second inverter is connected to the microgrid followed by the third inverter at t = 0.4s. Load 1 is disconnected at t=1.0s, reconnected back to the microgrid at t = 1.2s, and at t = 1.6s, additional load (load 2) is added to load 1. In this part, the proposed technique (with a sharing ratio of 1:1:1 is set, active and reactive power) is compared to the conventional droop technique. Figure 5.8 presents simulation comparison results. Figure 5.8 (a) shows the current contributions of the three inverters and the total load current waveform using the proposed power-sharing scheme, while the current waveforms obtained using conventional droop control are presented in Figure 5.8 (b). These results show that both control schemes are able to share the total load between the three inverters but with different dynamic responses.

Figure 5.8 parts (c) and (d) show the active and reactive power output of the three inverters, and the total load active and reactive powers using the proposed power sharing technique and conventional droop control respectively. The proposed power-sharing scheme has a faster dynamic response than conventional droop control, as the former takes less than 100ms to equally share the active and reactive powers between the three inverters. Also the proposed scheme exhibits lower circulating currents between the inverters than with conventional droop control as seen in Figure 5.8 parts (a) and (b) from t = 1.0s to t = 1.2s. When the second load is connected at t=1.6s, good transient and steady state performances are observed. Figure 5.8 (d) shows that conventional droop control has a slower dynamic response and takes

longer for the inverters to achieve equal active power sharing, while it is unable to achieve equal reactive power sharing. This is because conventional droop control is sensitive to impedance mismatch.

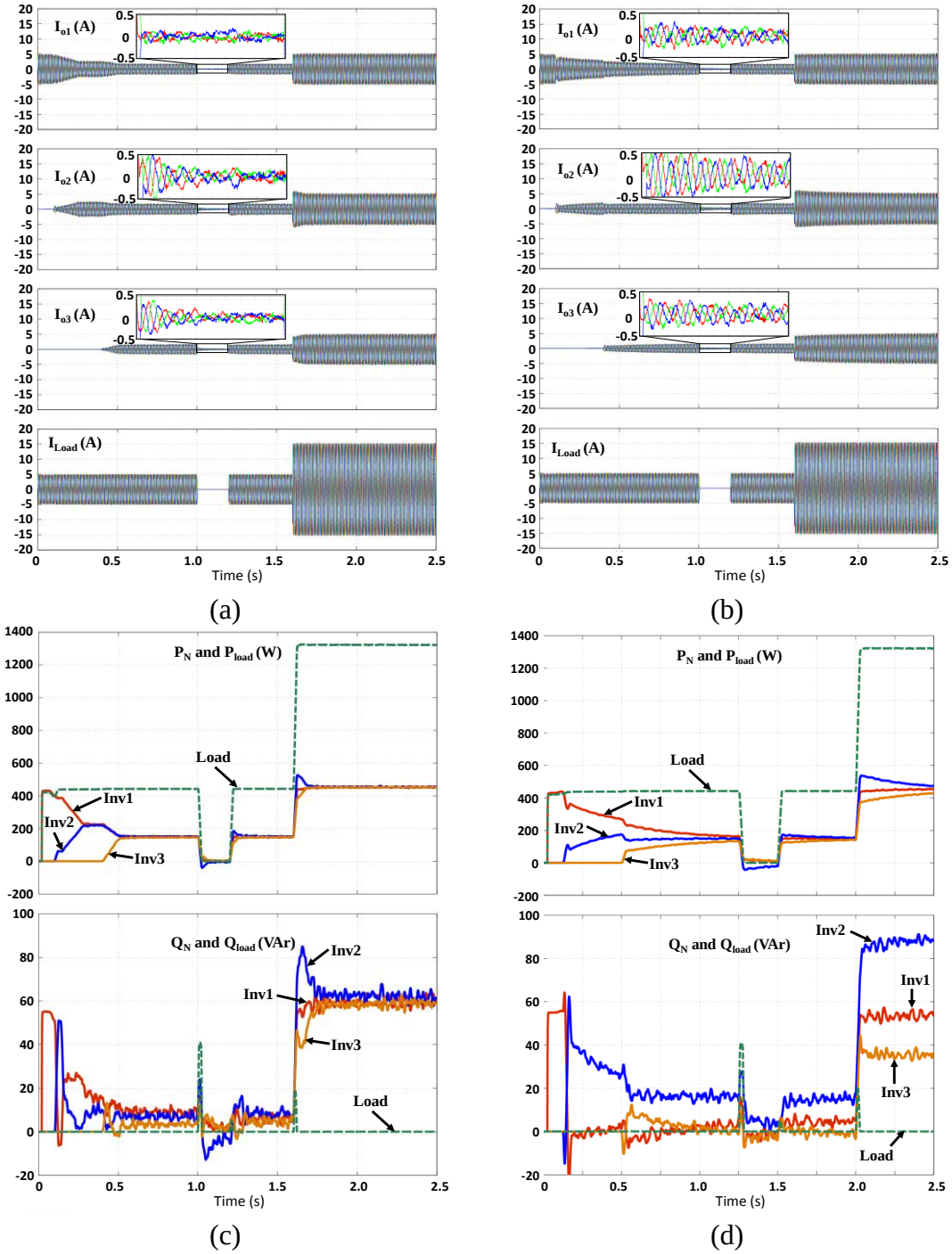
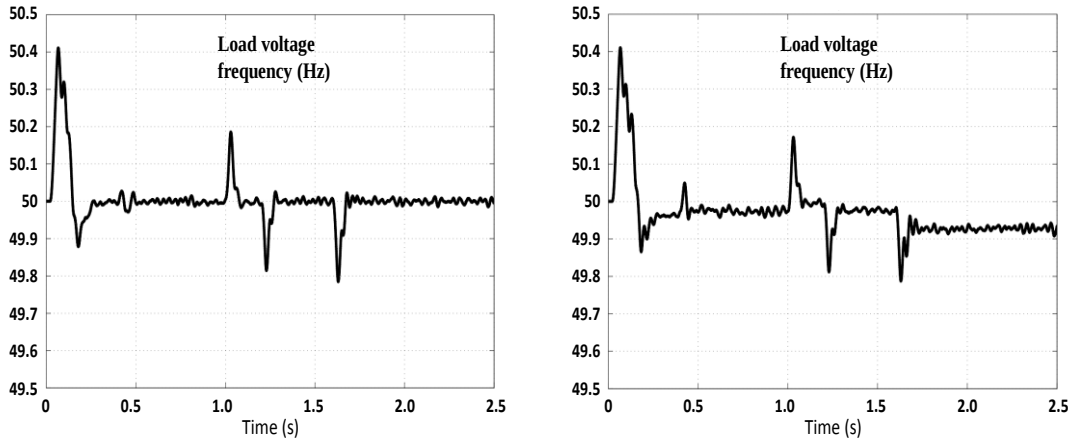


Figure 5.8 Part I simulation results : a) output current and load current using proposed technique, b) output current and load current using conventional droop technique, c) inverters and load *P* and *Q* using proposed technique, and d) inverters and load *P* and *Q* using conventional droop technique.

Figure 5.9 parts (a) and (b) show the output voltage frequency when using the proposed technique and droop technique respectively. From these figures, the proposed technique has better frequency regulation as no adjustment is made to the frequency of output voltage of each inverter.

5.5.2 Simulation Part II – *R* Load – R_{P1}:R_{P2}:R_{P3} = 1:2:4 R_{Q1}:R_{Q2}:R_{Q3} = 1:1:1

At first, only inverter 1 supplies load 1. At time t = 0.1s, a second inverter is connected to the microgrid followed by the third inverter at t = 0.4s. Load 1 is disconnected at t = 1.0s, reconnected to the microgrid at t = 1.2s, and at t = 1.6s, additional load (load 2) is added to load 1. In this part the active and reactive power sharing ratios are set to 1:2:4 and 1:1:1 respectively. Figure 5.10 (a) shows output current of the three inverters and total load current waveforms, when the three inverters share active and reactive power in the specified ratios. Figure 5.10 (b) displays active and reactive power outputs and load active and reactive power. The proposed power sharing is able to force the inverters' active and reactive output powers to follow the ratios set by the central controller, within less than 5 cycles (100ms). When additional load is introduced at t = 1.6s, all inverters still satisfy the required power ratios set by the central controller. The active power difference, P_{Δ}, and phase adjustment, $\Delta\alpha$, are shown in Figure 5.10 (c) while reactive power difference, Q_{Δ}, and voltage amplitude of each inverter, E, are shown in Figure 5.10 (d). These two figures show how the adjustment is made to the output voltage phase and amplitude to achieve the required power sharing.



(a) (b)

Figure 5.9 Comparison of load voltage amplitude and frequency. (a) proposed controller and (b) conventional droop control.

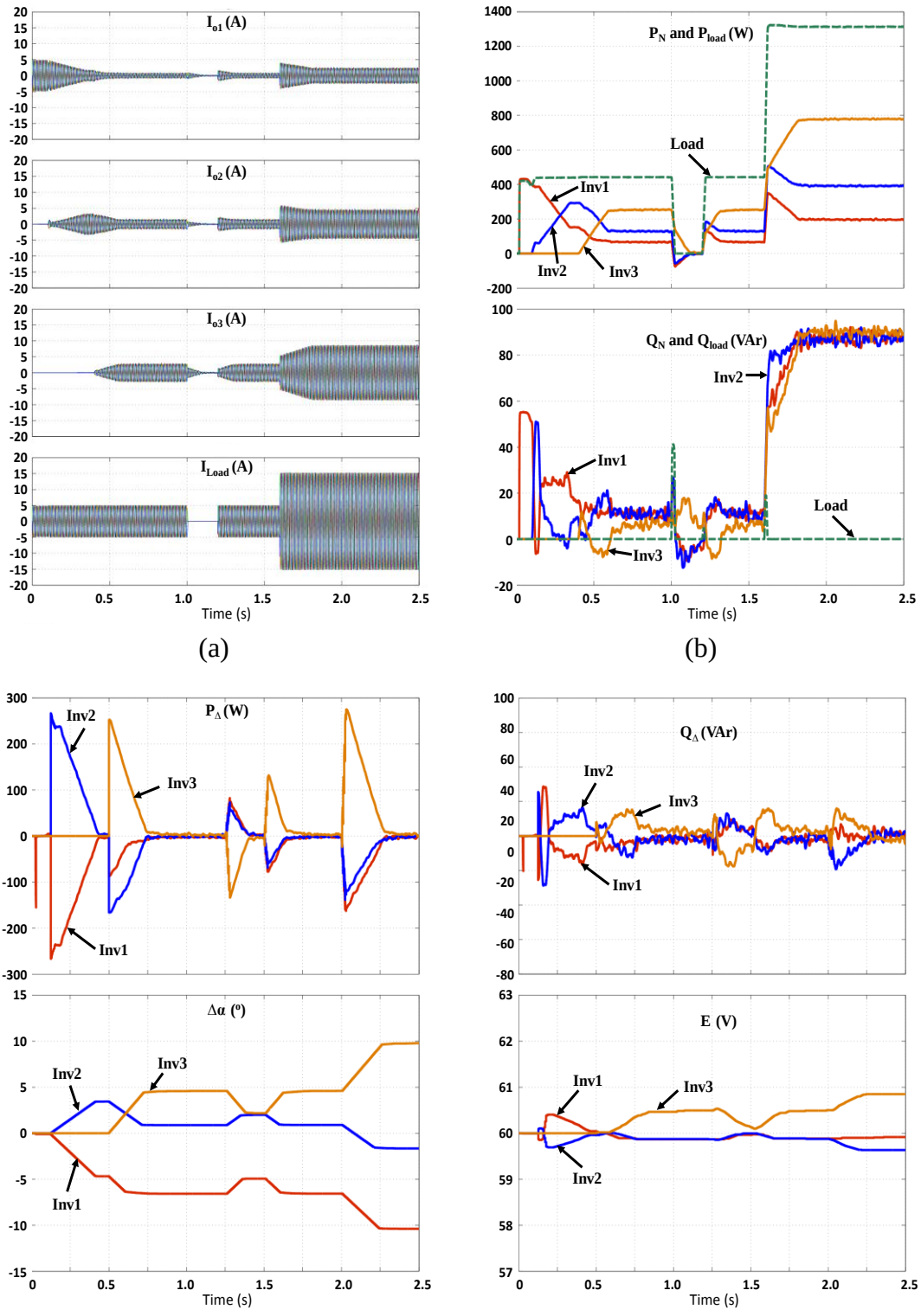


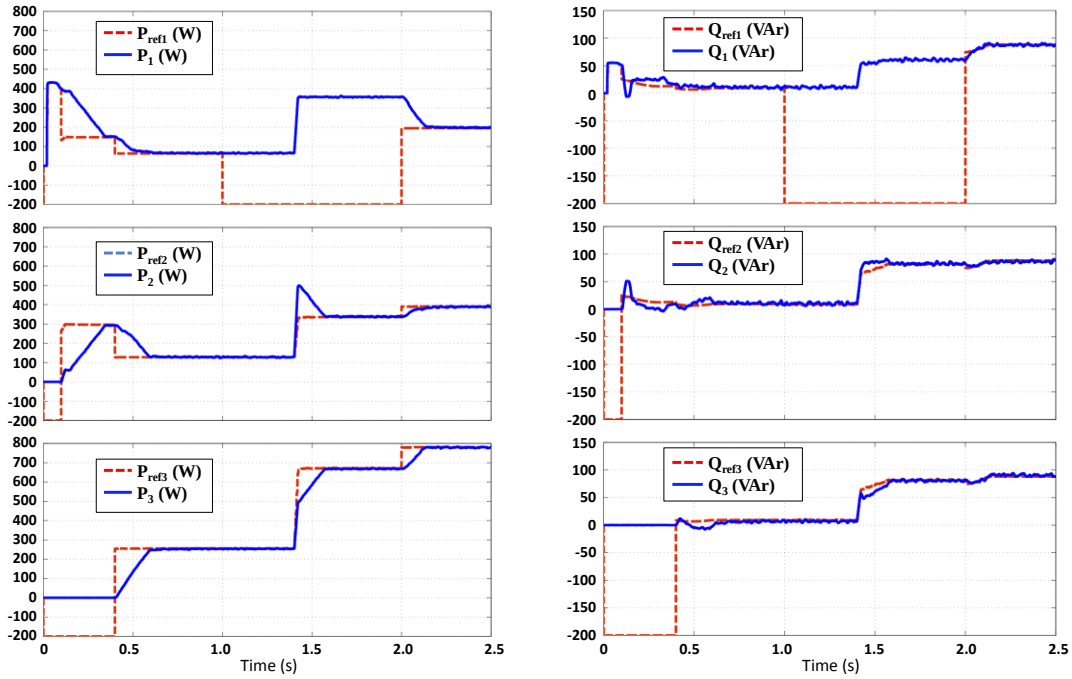
Figure 5.10 Simulation results for Part II: (a) output current and load current, (b) inverter *P* and *Q* and load *P* and *Q* using proposed technique, (c) *P*Δ - Δ*α* and (d) *Q*Δ - *E* (peak).

5.5.3 Simulation Part III – Communication loss

This part presents simulation results when communication is lost between inverter 1 and the central controller. Initially, only load 1 is connected to inverter 1. At time t = 0.1s, a second inverter is connected to the microgrid followed by the third inverter at t = 0.4s. Load 2 is added to load 1 at t = 1.4s and communication loss occurs between t = 1.0s to t = 2.0s.

All three inverters are set to share active and reactive powers in the ratios 1:2:4 and 1:1:1 respectively. In both parts III and IV, for simplicity, -200 (W or VAr) is used to represent PWM communications with a duty cycle of 0 and the value received by an inverter or the central controller when there is communication loss (see section 5.4.4). Figure 5.11 parts (a) and (b) show power references and output power (active and reactive) for the three inverters. Prior to t = 1.0s, all inverters are able to share the active and reactive power based on the specified ratios. When there is loss of communication between inverter 1 and the central controller (at t = 1.0s), the central controller assumes that inverter 1 is not connected to microgrid and excludes it from the power reference calculations. It then sends -200W and -200VAr power references to inverter 1. When inverter 1 receives this command, it will not change its reference voltage and supplies the load based on its recent voltage state.

Without any change in the load condition, inverter 1 supplies the same power as before the communication loss. When the load changes at t = 1.4s, the amount of power delivered from inverter 1 cannot be controlled but the power from inverters 2 and 3 can still be controlled to follow the specified ratio ($P_3 = 2P_2$). When the communication is back to normal at t = 2.0s, the central controller receives proper power information from inverter 1 and includes it in the reference power calculation. It then sends new power references to all inverters, which are then able to accurately follow their power references.



(a) (b)

Figure 5.11 Simulation results for Part III – Lost of communication from inverter 1 to central controller: (a) active power references and inverters output active power and (b) reactive power references and inverters output reactive power.

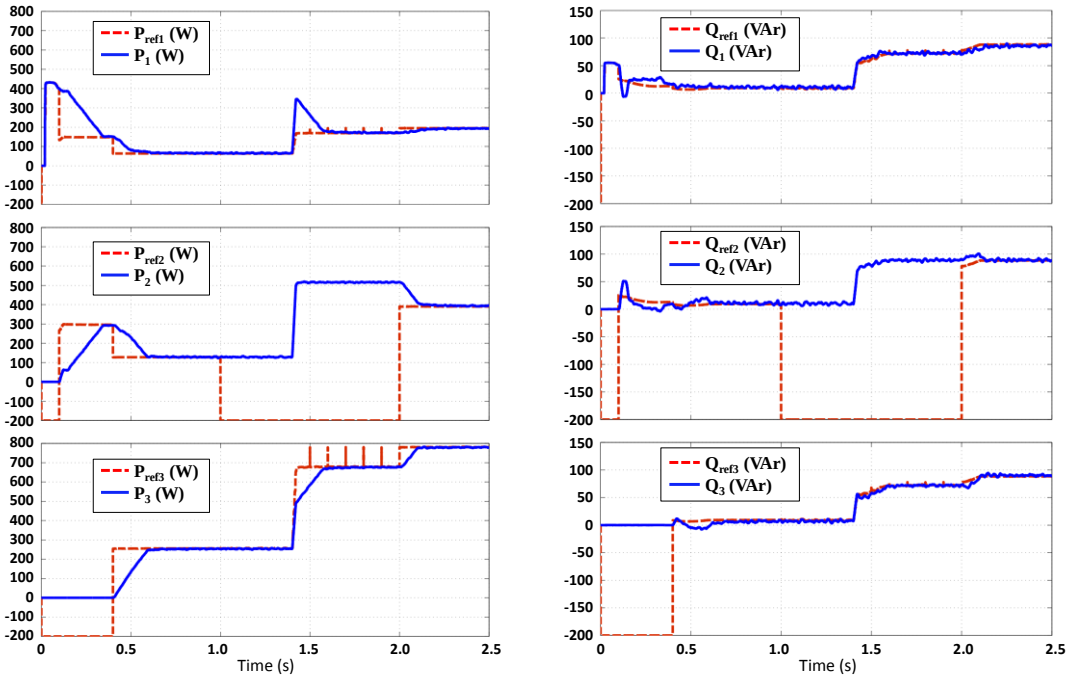
5.5.4 Simulation Part IV – Communication loss

This part presents simulation when communication is lost from the central controller to inverter 2. At first, only inverter 1 supplies load 1. At time t = 0.1s, a second inverter is connected to the microgrid followed by the third inverter at t = 0.4s. Load 2 is added to load 1 at t = 1.4s and communication loss occurs between t = 1.0s to t = 2.0s. The three inverters are set to share active and reactive powers in the ratios 1:2:4 and 1:1:1 respectively. Power references and output power (active and reactive) for the three inverters are shown in Figure 5.12 (a) and (b). All the inverters are able to achieve the specified power ratios prior to t = 1.0s. When the communication loss occurs at t = 1.0s, inverter 2 receives -200W and -200VAr as its active and reactive power references respectively. It detects that there is a communication issue as it is still supplying power to microgrid and expecting a proper power reference from the central controller. It stops any changes to its reference voltage and supplies the microgrid based on its recent voltage state. In order to avoid its power being calculated in the power reference calculation, it sends -200 (W and VAr) to the central controller. When load 2 is added to load 1 at t = 1.4s, the output power from

inverter 2 cannot be controlled to follow the specified ratio but the other two inverters maintain their ratio ($P_3 = 4P_1$).

Some spikes on the active power reference of inverters 1 and 3 can be observed between t = 1.5s to t = 2.0s. This occurs because every 0.1s, inverter 2 sends its actual power information to the central controller to check whether the communication issue has been resolved or not. At this moment, the central controller includes inverter 2 power information in the calculation of the power references thus producing the spikes. If inverter 2 does not receive the proper power references after sending its actual power, it will resend -200 (W and VAr) to the central controller.

When communication from the central controller to inverter 2 is back to normal at t = 2.0s, inverter 2 power information is included in the power reference calculation. It receives proper power references from the central controller and all three inverters are able to track their power references.



(a) (b)

Figure 5.12 Simulation results for Part IV – Lost of communication from central controller to inverter 2: (a) active power references and inverters output active power and (b) reactive power references and inverters output reactive power.

5.5.5 Simulation Part V – *RL* Load – R_{P1}:R_{P2}:R_{P3} = R_{Q1}:R_{Q2}:R_{Q3} = 5:5:8

In this part, active and reactive power is shared based on the rating of each inverter (R_{P1}:R_{P2}:R_{P3} = R_{Q1}:R_{Q2}:R_{Q3} = 5:5:8) and passive RL loads are used. At first, only inverter 1 supplies load 3. At time t = 0.1s, a second inverter is connected to the microgrid followed by the third inverter at t = 0.4s. Load 1 is disconnected at t = 1.0s, reconnected back to the microgrid at t = 1.2s, and at t = 1.6s, additional load (load 4) is added to load 3. Figure 5.13 (a) shows output current of the three inverters and total load current waveforms while Figure 5.13 (b) displays active and reactive power outputs and load active and reactive power. From these figures, all inverters are able to share the active and reactive power based on the specified ratio. P_Δ - $\Delta\alpha$ and Q_Δ - E plots are shown in Figure 5.13 parts (c) and (d) respectively. These two figures show how the adjustments are made to the output voltage phase and amplitude to achieve the required power sharing.

5.5.6 Simulation Part VI – Changing ratio (1:1:1 → 1:2:4 → 1:1:1)

In this part, prior to t = 0.5s, all the three inverters are connected to the microgrid and supplying load 3 with active and reactive power ratios set to 1:1:1. At t = 1.0s, active and the reactive power ratios are changed to 1:2:4 and then reverted to 1:1:1 at t = 2.0s. Figure 5.14 (a) shows output current of the three inverters and total load current waveforms. Smooth output current transitions can be observed in this figure. Active and reactive output power and load active and reactive power are shown in Figure 5.14 (b) and both active and reactive powers follow the specified power ratio. P_Δ - $\Delta\alpha$ and Q_Δ - E plots are shown in Figure 5.14 parts (c) and (d) respectively.

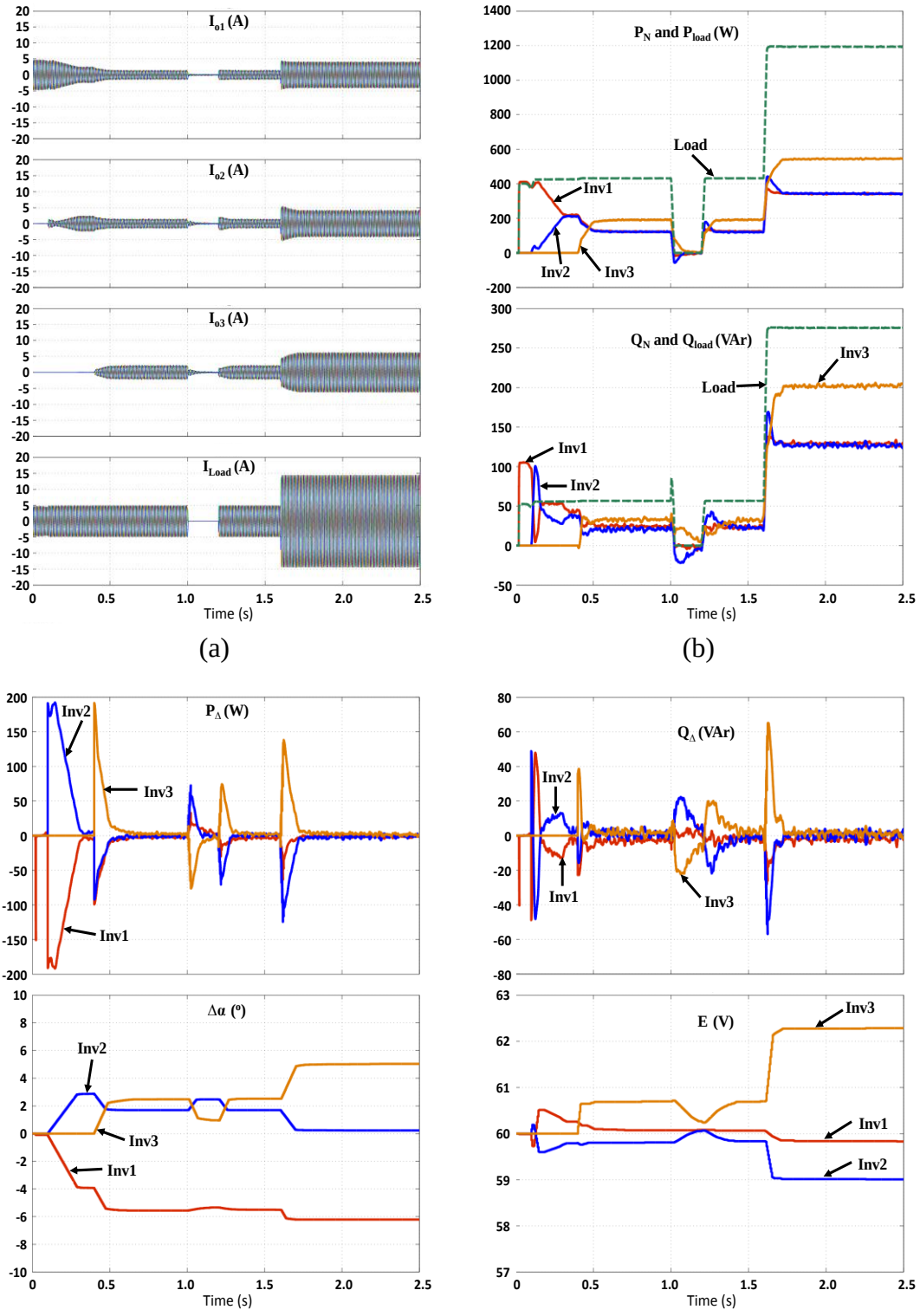


Figure 5.13 Simulation results for Part V: : (a) output and load current; (b) output and load *P* and *Q*; (c) P_Δ - $\Delta\alpha$; and (d) Q_Δ - ΔE.

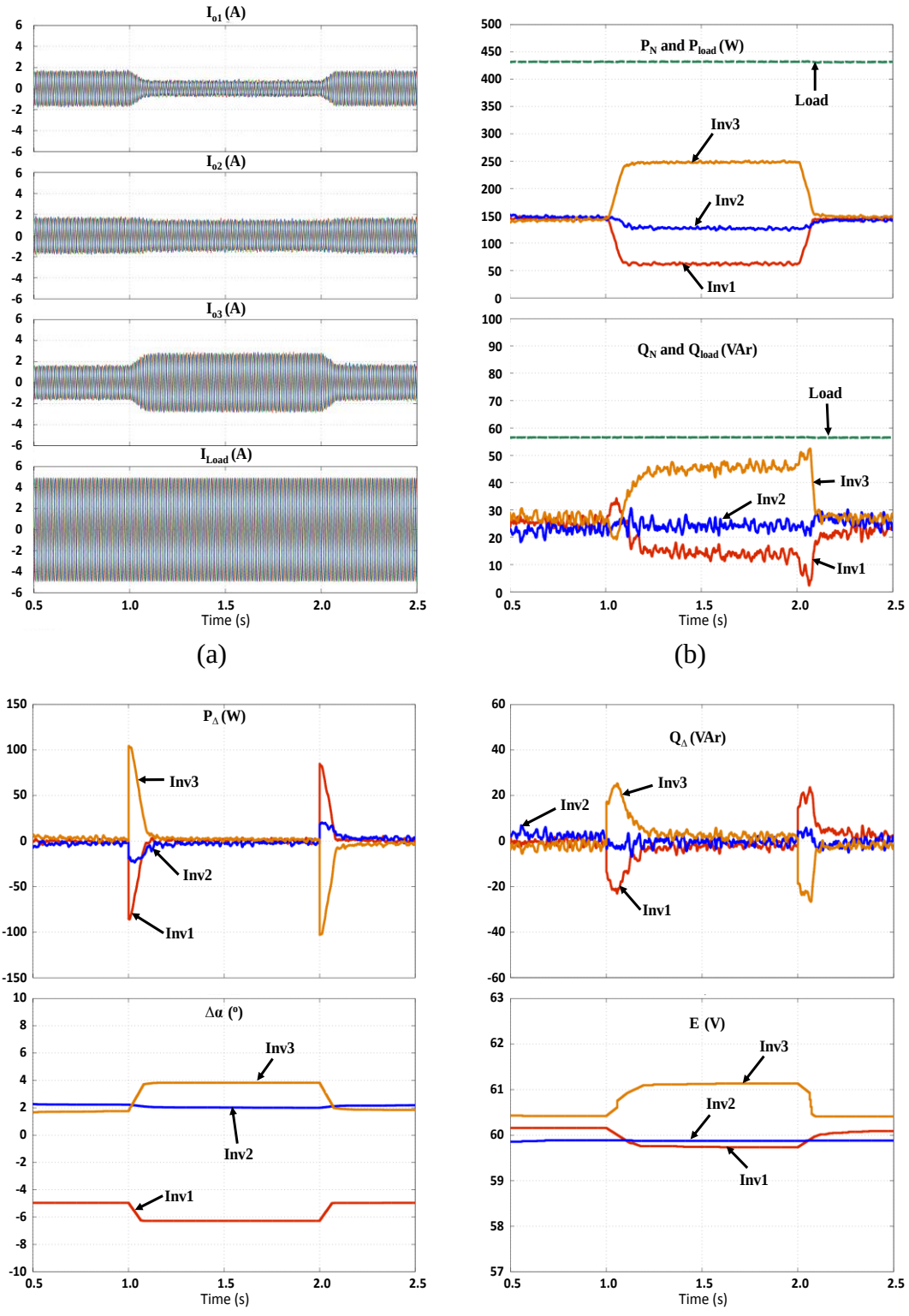


Figure 5.14 Changing ratio (1:1:1 - 1:2:4 – 1:1:1) : (a) Output and load current; (b) Output and load *P* and *Q*; (c) P_Δ - $\Delta\alpha$; and (d) Q_Δ - ΔE.

5.6 Experimental results

The scaled microgrid consists of three inverters and number of local loads, used to validate the practicality of the proposed power-sharing scheme. Figure 5.15 shows the hardware arrangement. Each inverter is controlled by an Infineon TriCore™ TC1796B and the same DSP is used for the central controller. The communication is implemented using PWM channels at the source and low-pass filters at the destinations, for reasons previously explained. The test rig parameters are the same as in the simulation section and the experimental results are organized in the same order as the simulations. An additional case demonstrates the performance of the proposed power-sharing scheme with a nonlinear load.

5.6.1 Experiment Part I – *R* Load – R_{P1}:R_{P2}:R_{P3} = 1:1:1 R_{Q1}:R_{Q2}:R_{Q3} = 1:1:1

Figure 5.16 shows the experimental results for different operating conditions when the three parallel inverters equally share the active power and reactive powers needed by the load (1:1:1). Initially, only inverter 1 supplies load 1. Figure 5.16 (a) shows the system transient response when inverter 2 is introduced onto the microgrid, while Figure 5.16 (b) shows experimental waveforms that illustrate system steady state and transient response when inverter 3 is connected.

Power sharing between the inverters is achieved without any inrush current or significant transients, due to the adopted synchronization method and proposed power-sharing scheme. Figure 5.16 (c) depicts the system response during sudden disconnection of the main load. Figure 5.16 (d) shows that the circulating currents between inverters, when the main load is disconnected, are small (around 300mA p-p). Waveforms showing system response when load 2 is added to load 1 are presented in Figure 5.16 (e). Results illustrating the applicability of the proposed power-sharing scheme with a nonlinear load, are displayed in Figure 5.16 (f), where a three-phase uncontrolled diode bridge rectifier feeding a resistive load is introduced onto the main ac bus from a no load condition. The proposed power sharing is able to cope with a nonlinear load that injects significant current harmonics.

The output voltage of the three inverters and load voltage when the inverters are connected to the microgrid are shown in Figure 5.17. This figure shows that all inverters are smoothly synchronized and the measured total harmonic distortion of the load voltage is less than 2.5 %.

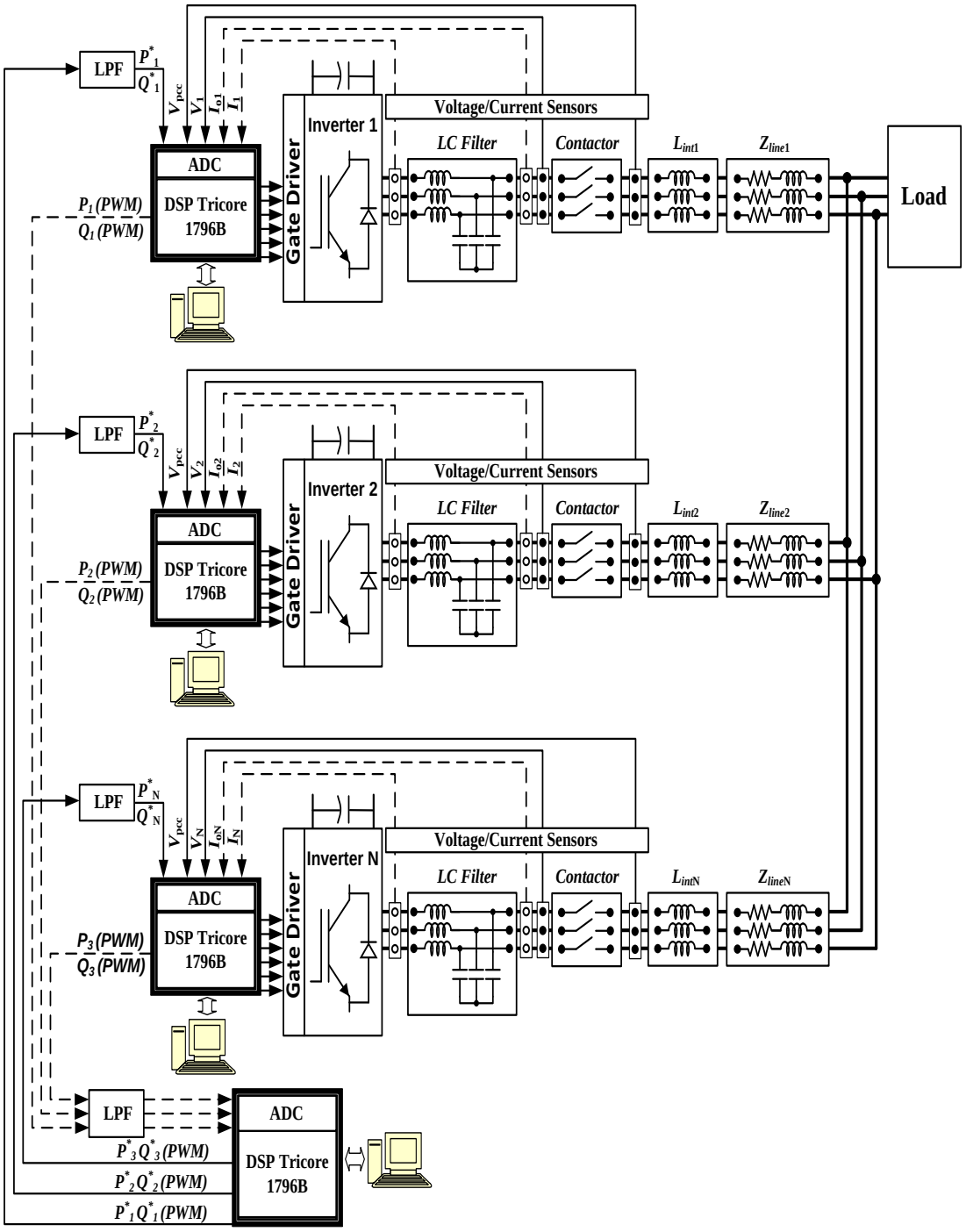


Figure 5.15 Hardware arrangement.

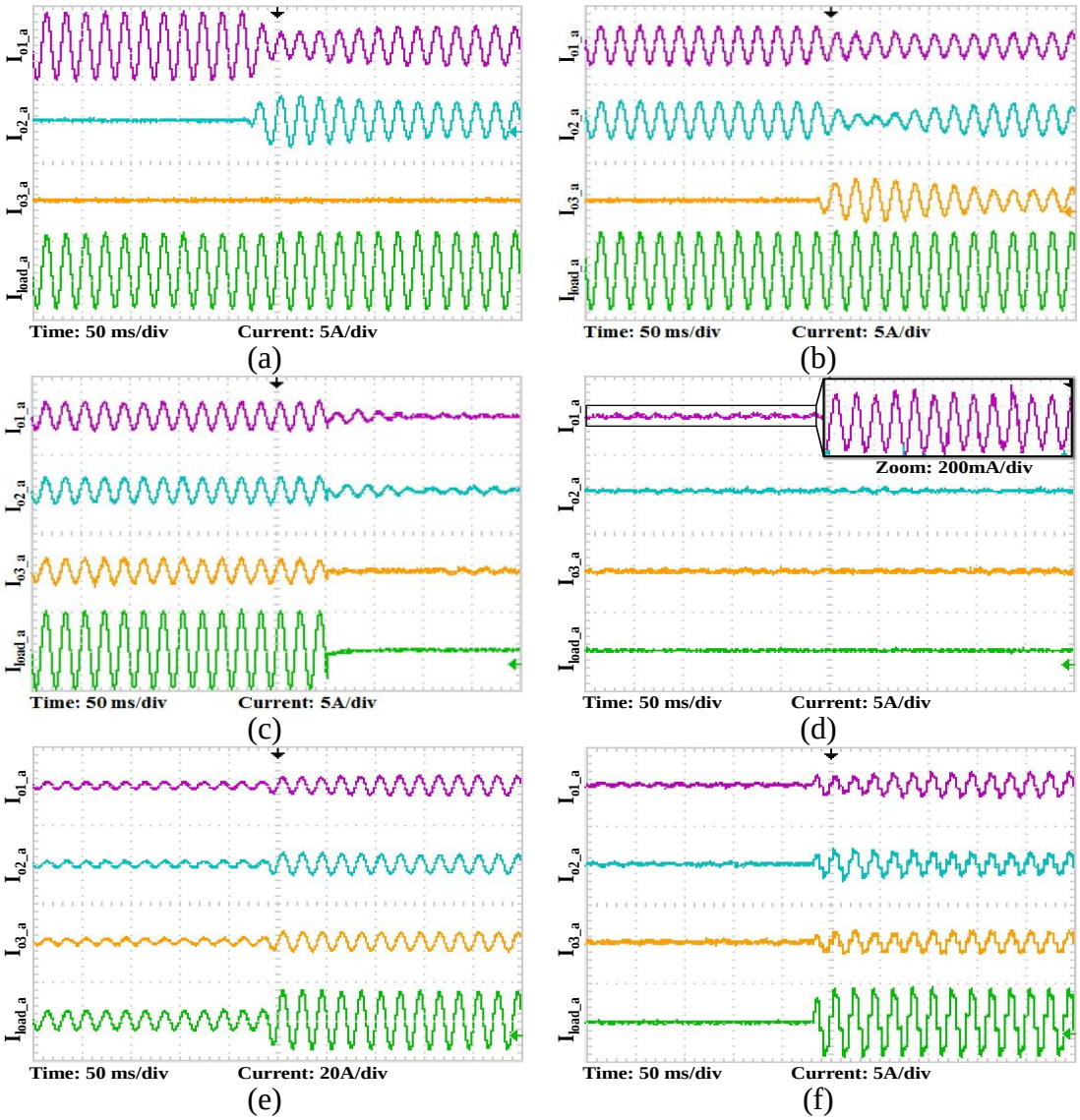


Figure 5.16 Current waveforms under different operational conditions with 1:1:1 power ratio: (a) inverter 2 is connected to microgrid ; (b) inverter 3 is connected to microgrid; (c) half load to no load; (d) circulating current under no load condition; (e) half load to full load; and (f) no load to rectifier type load

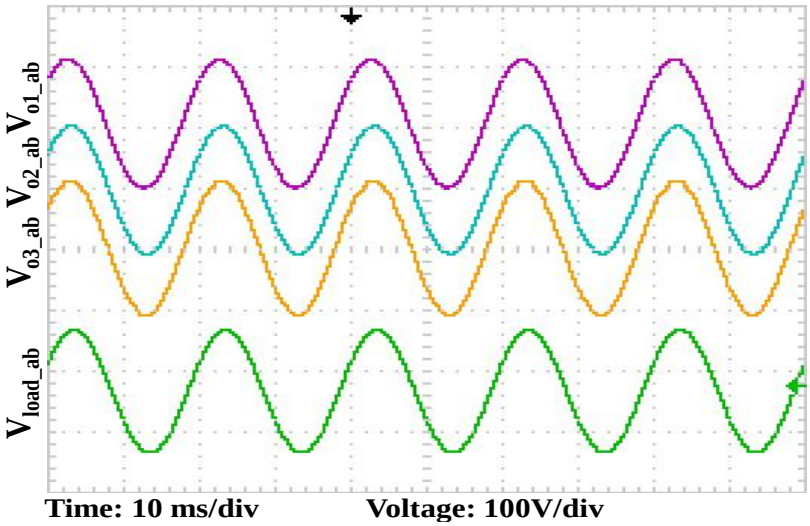


Figure 5.17 Output voltage of three inverters and load voltage when all the inverters are connected to the microgrid and supplying both load 1 and load 2.

5.6.2 Experiment Part II – *R* Load – R_{P1}:R_{P2}:R_{P3} = 1:2:4 R_{Q1}:R_{Q2}:R_{Q3} = 1:1:1

The active power and reactive power ratios are set to 1:2:4 and 1:1:1 respectively. This means $P_1 = \frac{1}{7}P_L$, $P_2 = \frac{2}{7}P_L$ and $P_3 = \frac{4}{7}P_L$, $Q_1 = Q_2 = Q_3 = \frac{1}{3}Q_L$, where P_L and Q_L are the total load active and reactive powers, and P_j and Q_j where j=1 to 3 represent active and reactive power outputs of inverters 1, 2 and 3. The experimental results under different operational conditions are shown in Figure 5.18. Initially, only inverter 1 supplies load 1. In Figure 5.18 (a), the transient performance when inverter 2 is connected to the microgrid is shown. This result shows smooth transient performance and after 350 ms, both inverters are able to achieve the specified power ratio. The same good transient performances are observed when inverter 3 is connected to the microgrid, as shown in Figure 5.18 (b). The steady-state performance of the three inverters supplying load 1 and transient performance when the load is disconnected are shown in Figure 5.18 (c). In Figure 5.18 (d), the circulating currents among the parallel inverters are shown and are small in magnitude. The transient performance when load 2 is added to load 1 is shown in Figure 5.18 (e) where the specified ratios are achieved. Finally, Figure 5.18 (f) shows that the controller is able to achieve the same good performance with a nonlinear type load.

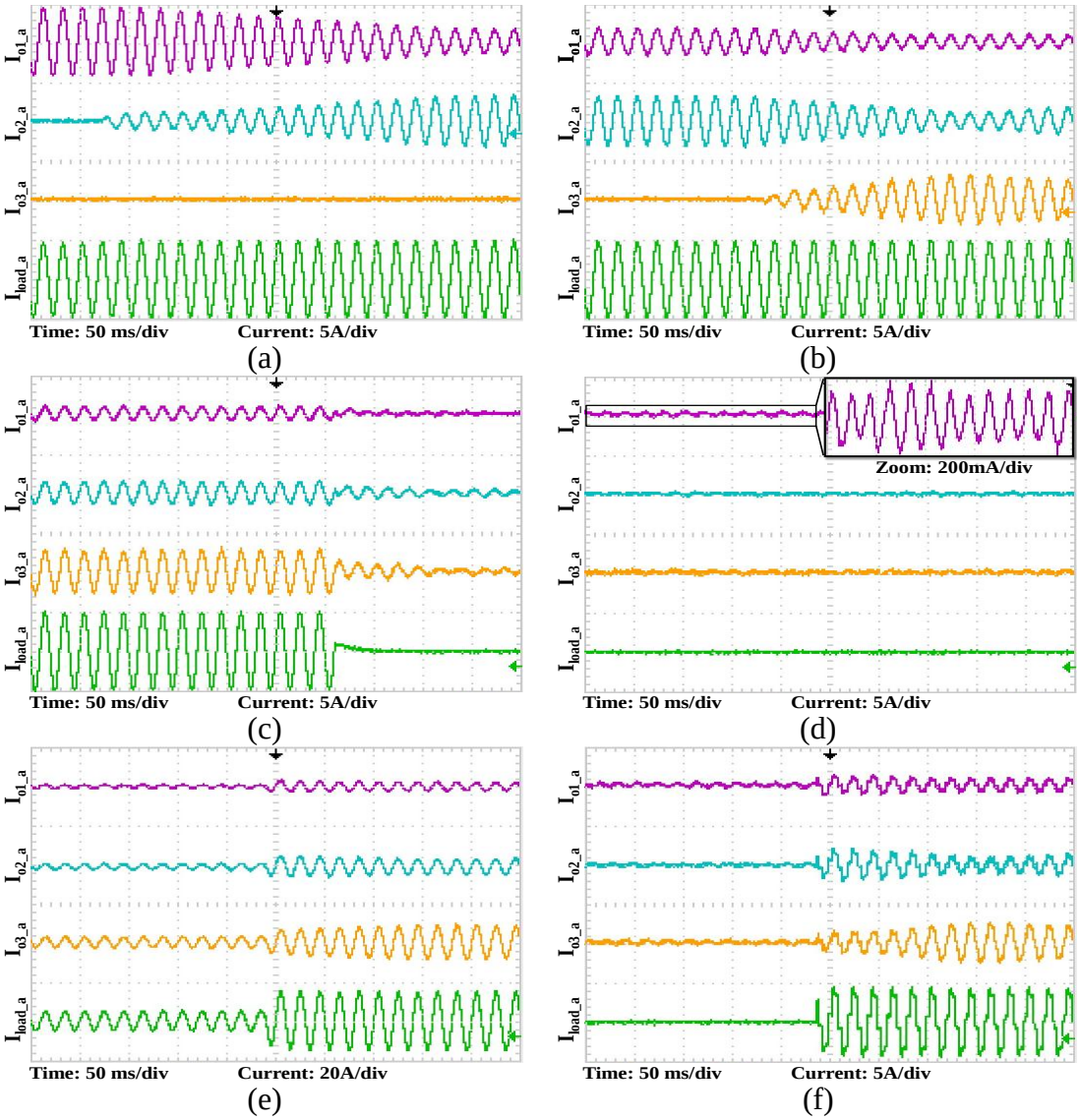


Figure 5.18 Current waveforms under different operational conditions with the active power and reactive power ratio set to 1:2:4 and 1:1:1 respectively. (a) inverter 2 is connected to microgrid ; (b) inverter 3 is connected to microgrid; (c) half load to no load; (d) circulating current under no load condition; (e) half load to full load; and (f) no load to rectifier type load

5.6.3 Experiment Part III – Changing ratio (1:1:1 → 1:2:4 → 1:1:1)

In this part, initially, all three inverters are connected to the microgrid and supplying load 1 with active and reactive power ratios of 1:1:1. Transient performance when the power ratios are changed to 1:2:4 is shown in Figure 5.19 (a). This figure shows that the output currents of the three inverters follow their specified power ratio component. In Figure 5.19 (b), the transient performance when the power ratios revert to 1:1:1 is shown. From these two figures, the controller is able to achieve the required power sharing even if the ratios are changing during operation.

5.6.4 Experiment Part IV – Disconnection of inverters during operation

In this part, the hot swap capability of the proposed controller is demonstrated. Initially, all three inverters are connected to the microgrid and supply load 1. Figure 5.20 (a) is the transient performance when inverter 2 is disconnected while supplying load 1 with a power ratio of 1:1:1. When inverter 2 is disconnected, current from inverters 1 and 3 increases and is equally shared. Transient performances when inverter 2 is disconnected, inverter 1 is disconnected and inverter 3 is disconnected, while all the three inverters are supplying load 1 with power ratio set to 1:2:4 are shown in Figure 5.20 parts (b), (c) and (d) respectively. From these results, the remaining inverters are able to share load current based on the specified ratio.

The simulation and experimental results indicate the superiority of the proposed technique in terms of power sharing compared to the conventional droop technique. Additionally, the ability to set the required power ratio gives extra flexibility on power management. Table 5.2 compares the proposed power sharing technique to conventional droop control.

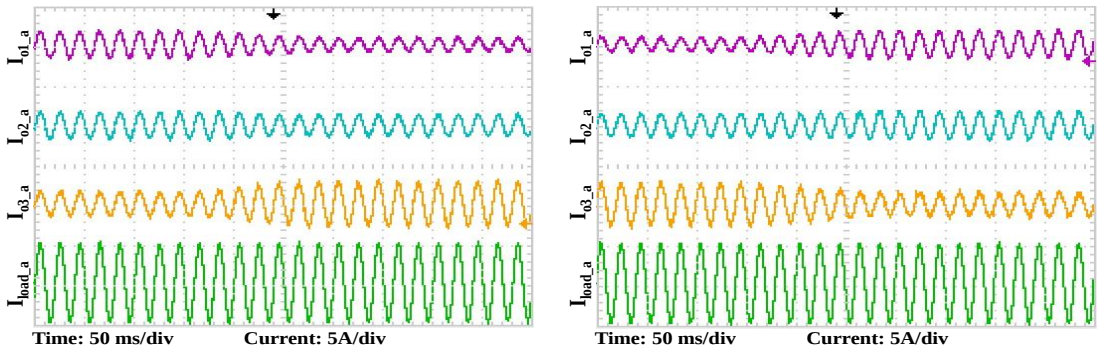


Figure 5.19 Changing active power ratio:
(a) From 1:1:1 to 1:2:4 and (b) from 1:2:4 to 1:1:1.

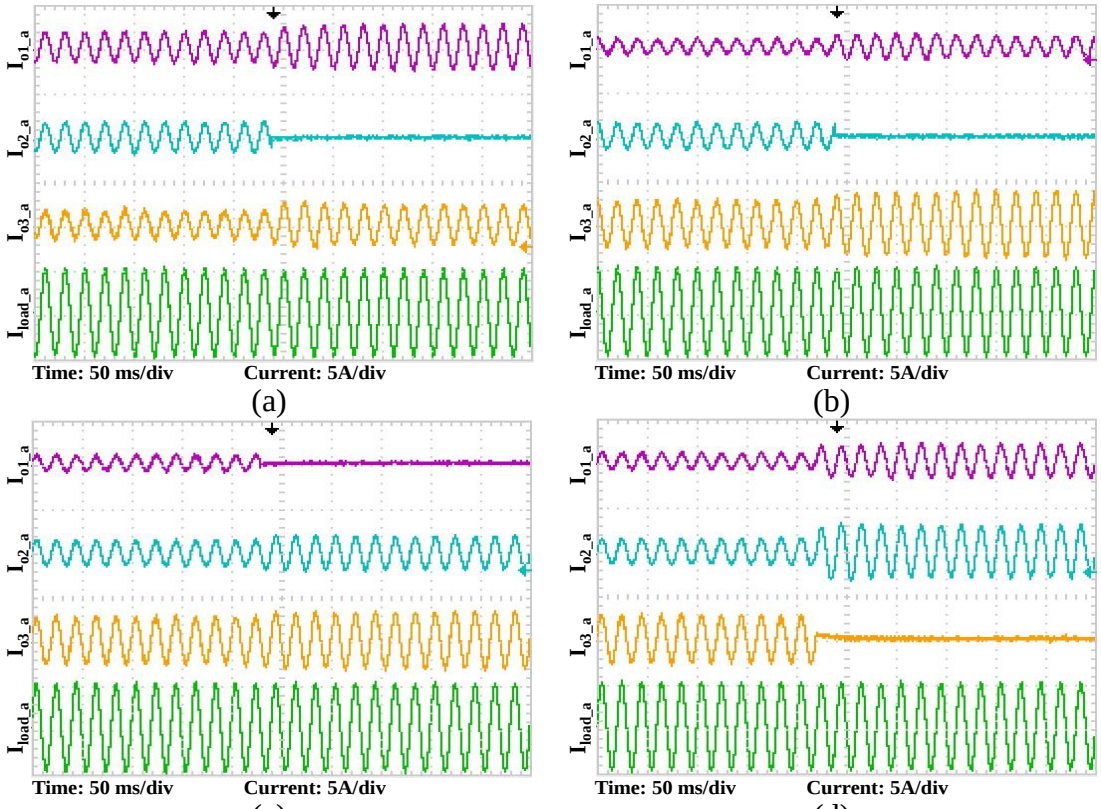


Figure 5.20 Hot swap capability – Disconnection : (a) inverter 2 is disconnected (Ratio - 1:1:1); (b) inverter 2 is disconnected (ratio - 1:2:4); (c) inverter 1 is disconnected (ratio - 1:2:4); and (d) Inverter 3 is disconnected (ratio - 1:2:4)

Table 5.2 Comparison between the proposed power sharing technique and conventional droop control, under impedance mismatch conditions.

Control technique	Conventional droop	Proposed technique
Approach	• P-ω and Q-V droop	• Each inverter sends output P and Q to a central controller • Central controller calculate the reference P and Q for each inverter • Inverter adjusts phase and amplitude to achieve required P and Q.
Communications	• No	• Yes
Active power sharing performance (refer to Part I simulation results)	• Achieves active power sharing with slow transient response (0.8s)	• Achieves active power sharing with fast response (0.2s)
Reactive power sharing	• Not able to achieve reactive power sharing under line impedance mismatch conditions	• Able to achieve reactive power sharing regardless of line impedance conditions.
Voltage frequency variation	• There will be a trade-off between active power sharing and frequency regulation	• Frequency is fixed as the adjustment is only applied to the angle of reference voltage.
Voltage amplitude regulation	• There is a trade-off between reactive power sharing and amplitude regulation.	• Amplitude varied based on the reactive power sharing requirement.
Other advantages	• Easy to implement	• Ability to share active and reactive power based on specified ratio. • No system failure even if there is communication loss. • Communication between inverters and central controller can be used for optimization of available power (economic dispatch).

5.7 Summary

In this chapter, a new power sharing scheme for parallel connected inverters in an islanded microgrid has been proposed. The technique requires low-bandwidth communication between inverters and the central controller to exchange inverter active and reactive power output information. Simulation and practical implementation results demonstrated that the proposed power sharing technique operates under impedance mismatch, load step, a nonlinear load condition, and demonstrated hot swap capability. The proposed power sharing outperforms conventional droop control as it has a faster dynamic response, better frequency regulation, better sharing of reactive power between inverters that have different line impedances, and has the ability to set the active and reactive power ratio for each

inverter. The technique can also operate for a microgrid with distributed loads. The ability to set specific active and reactive power ratios gives flexibility to the utility owner to manage the available power in an efficient and effective manner.

However, this control scheme does increase control complexity as it requires communication between each inverter and central controller. Although it has been shown that communication failure will only affect the power sharing accuracy, the total system failure can possibly occur if the central controller itself failed.

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Chapter 6

Optimized Operation of Inverter Based Distributed Generation in a Rural Islanded Microgrid

In this chapter, the proposed power sharing scheme in the Chapter 5 is extended by adding a power ratio calculation that can optimize the operation of inverter based distributed generation units in a rural islanded microgrid. Parallel connected inverter operation with the calculated power ratio ensures minimum distributed power losses in an islanded microgrid. The proposed optimized power sharing scheme is validated using MATLAB/Simulink simulation results of three three-phase parallel inverters in a rural islanded microgrid. Furthermore, experimental results from a prototype of two three-phase parallel inverters connected to three passive loads are also presented.

6.1 Background

Distribution power losses contribute the highest percentage of the overall power losses in an electric power system. In average, the distribution power losses around the world from 2006 to 2010 averaged 9.01% as shown in Table 6.1. As mentioned in section 1.1.3, one DG advantage is that it is able to reduce transmission and distribution power losses as it is located near the customer site [6.1]. DG location and rating need to be properly considered during the planning stage to achieve minimum distribution power losses [6.2]. Apart from these considerations, the power losses can be further minimized during operation by using a proper control scheme.

In this chapter, a rural islanded microgrid is studied. In this type of microgrid, the loads (usually houses) are located several miles away from the DG sources so distribution power losses are significant. In normal practice, DGs connected to this microgrid share the loads based on their rating. However, in this chapter, it can be proved that, using the proposed power sharing technique from Chapter 5 with properly calculated power sharing ratios, distribution power losses can be significantly reduced under several loading conditions. Furthermore this optimized power sharing scheme also improves voltage regulation.

Table 6.1 World electricity generation and distribution power losses [6.3]

Year	2006	2007	2008	2009	2010
Net Generation (billion kWh)	18005	18842	19157	19071	20225
Distribution power losses (billion kWh)	1629	1707	1731	1734	1784
Distribution power losses (%)	9.05	9.06	9.04	9.09	8.82

6.2 System under study

This section discusses the rural islanded microgrid under study including the DG and load configuration as well as system communication requirements.

6.2.1 Rural islanded microgrid

A rural islanded microgrid system as shown in Figure 6.1 is considered. In this typical rural village arrangement, groups of houses are located distant from each other. There are three inverter based DGs supplying 8 loads where each consists of a group of houses. The distance between each load/DG bus is denoted by D1 to D10. It is assumed in this study that the same low voltage power cables are used throughout the system.

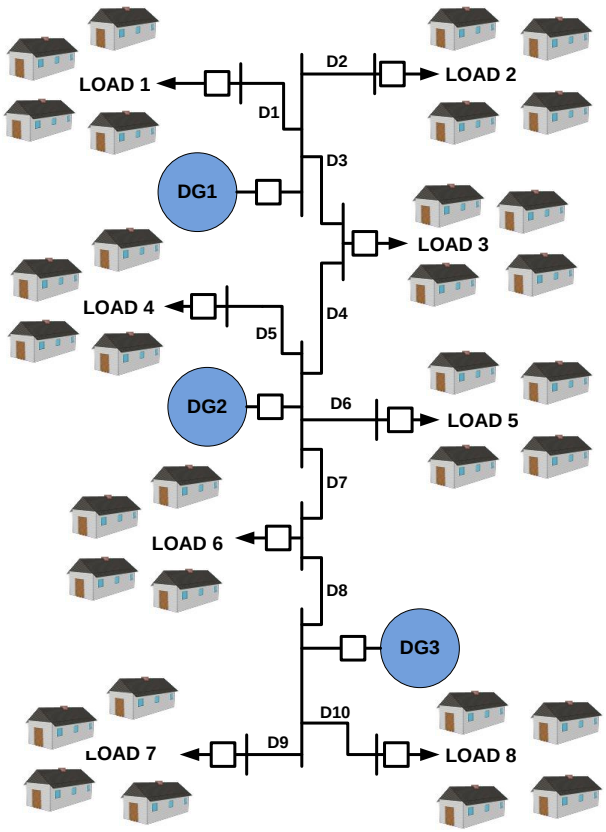


Figure 6.1 Rural islanded microgrid.

6.2.2 DG configuration

The inverter based DG configuration used in this study is shown in Figure 6.2 (a). Each DG module is assumed to have a fixed DC link voltage and consists of a three-phase inverter, which is controlled using sinusoidal pulse width modulation (SPWM); a reference voltage generator (RVG); a controller; an output power filter; and an interfacing inductor. Each inverter output voltage is regulated by a proportional integral (PI) controller in the *d-q* synchronous reference frame. Output active and reactive power calculations are based on voltage and current measurement after the interfacing inductor. This output power information is sent to the central controller through a wireless communication interface. Active and reactive power references from the central controller are received through the same wireless interface. This power references are used in RVG as parameters to make adjustment to the reference voltage.

6.2.3 Load configuration

Each load in this study is a group of houses as shown in Figure 6.2 (b). Considering that houses in a particular group are closely located, only one smart meter is installed at each group and not at every house. This smart meter measures the active and reactive powers consumed by the load and sends these wirelessly to the central controller.

6.2.4 Communication with the central controller

In the proposed control scheme, a central controller is used to generate active and reactive power references for each DG unit. It receives active and reactive output power information from each DG unit and active and reactive power consumed by each load. For this reason, a low-bandwidth communication is required for information exchange between each DG/load and the central controller.

Some researchers have discussed the use of communications in power system applications [6.4-8]. The communication type may vary depending on inverter unit location and available communication structure. For example, if the inverters are located in the same building but separate distantly from each other, the local area network communication can be used [6.4]. In rural areas, company intranet and

dedicated website can be used for communication as proposed in [6.5]. In [6.7], the authors discussed in detail the use of Distributed Network Protocol 3.0 over TCP/IP (DNP3 over TCP/IP) in a smart grid demonstration, the Future Renewable Electric Energy Delivery and Management (FREEDM) systems. The authors in [6.8] discuss the use of a new wireless communication platform power system application that utilizes an IP digit spread spectrum wireless network combined with a 3G wireless public network. They claim that this platform is low cost but can achieve high transmission rate.

In this study a wireless communication is used for information exchange between DGs/loads and the central controller. The wireless communication system for DGs, loads and the central controller are show in Figure 6.2 parts (a), (b) and (c) respectively. When implementing any control strategy that uses communication, it is important to ensure that the system does not collapse during a communication failure. It has been showed in Chapter 5 that, with a communication failure between DGs and the central controller, the overall system will not collapse. During the communication failure, only power sharing performance is affected.

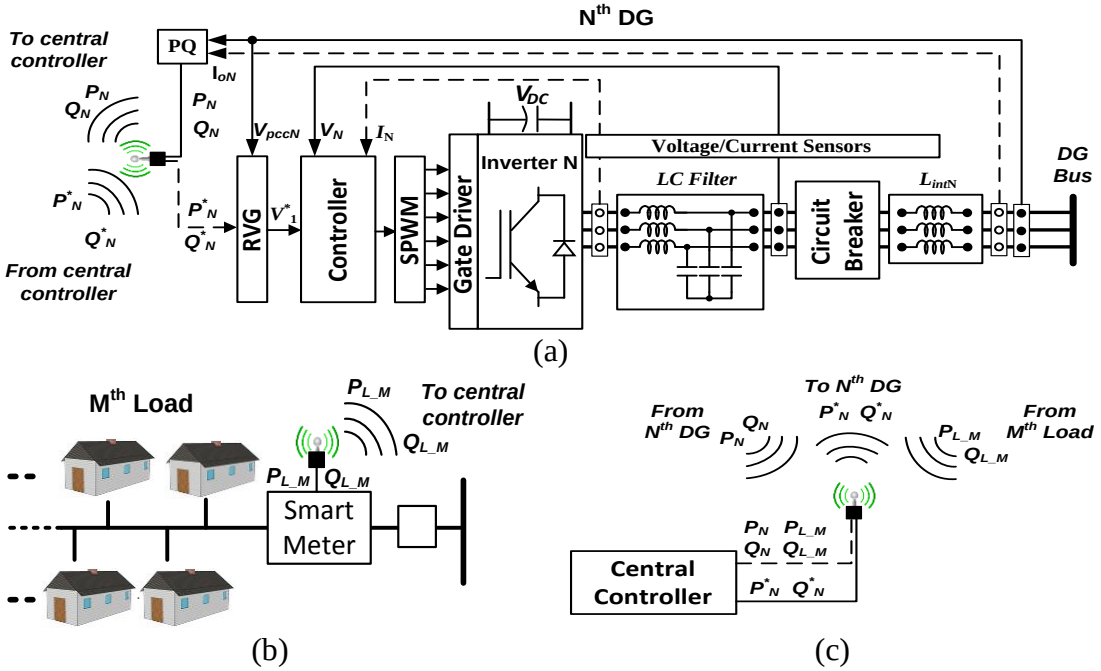


Figure 6.2 Islanded microgrid configuration and wireless communication interface: (a) DG , (b) load, and (c) central controller.

6.3 Power ratio calculation in the central controller

As discussed in section 5.4.1, the main function of the central controller is to process the output active and reactive power information from each inverter and then generate active and reactive power references for each unit. In order to calculate the correct power ratio to minimize power losses in the distribution line, the central controller has to know additional information such as i) the power consumed by each load and ii) distance between each DG and each load. Without knowing the power consumed by each load, it is impossible to determine the power losses in the line. To minimize the power losses in a distribution line, current required by each load should be supplied based on admittance from each DG to that particular load. However in this study, it is assumed that the same low voltage power cables (same impedance per unit distance) are used throughout the microgrid system. In this case, only the distance information is needed by the central controller. From this distance information, the admittance information can be determined from the inverse of the distance.

Assuming N inverters and M loads are connected to the microgrid, the power ratio based on distance between each inverter and load is given by

$$DRat_{jl} = \frac{D_{jl}^{-1}}{\sum_{h=1}^{N} D_{hl}^{-1}} \tag{6.1}$$

where D_{jl} is the distance between the j^{th} inverter and the l^{th} load while D_{hl} is the distance between the h^{th} inverter and the l^{th} load. The load active and reactive power ratios are given by (6.2) and (6.3) respectively

$$LPRat_{l} = \frac{P_{L\_l}}{\sum_{i=1}^{M} P_{L\_i}} \tag{6.2}$$

$$LQRat_{l} = \frac{Q_{L\_l}}{\sum_{i=1}^{M} Q_{L\_i}} \tag{6.3}$$

where P_{L_l} and Q_{L_l} are active and reactive power consumed by the l^{th} load while P_{L_i} and Q_{L_i} are active and reactive power consumed by the i^{th} load.

The active and reactive power ratios assigned to each inverter are:

$$r_{Pj} = \sum_{l=1}^{M} \left(LPRat_l \times DRat_{jl} \right) \tag{6.4}$$

$$r_{Qj} = \sum_{l=1}^{M} \left(LQRat_l \times DRat_{jl} \right) \tag{6.5}$$

Total active and reactive power ratios are given by:

$$r_{PT} = \sum_{j=1}^{N} r_{Pj} \tag{6.6}$$

$$r_{QT} = \sum_{j=1}^{N} r_{Qj} \tag{6.7}$$

The active and reactive power references for the j^{th} inverter are defined as follows:

$$P_j^*(k) = \frac{r_{Pj}}{r_{PT}} \sum_{h=1}^{N} P_h(k-1) \tag{6.8}$$

$$Q_j^*(k) = \frac{r_{Qj}}{r_{QT}} \sum_{h=1}^{N} Q_h(k-1) \tag{6.9}$$

where P_h and Q_h are the output active and reactive powers from the h^{th} inverter respectively.

6.4 Simulations results

This section presents Matlab/Simulink simulations that are divided into two parts. Simulation in the first part shows the proposed scheme performance with different line impedance X/R ratios. In the second part, the optimized power-sharing scheme simulation results are presented.

6.4.1 Part 1 : Performance under difference line impedance *X/R* ratio

As presented in the Chapter 5, the proposed power adjustment algorithm is deduced assuming inductive line impedance where active and reactive powers are affected by output voltage power angle and amplitude respectively. However in a low voltage application, line impedance is predominantly resistive. So it is interesting to see how the proposed scheme performs under different line impedance *X/R* ratios. Figure 6.3 shows the microgrid configuration used for simulation in Part 1. Two DGs are connected to a common load through an interfacing inductor and line impedance.

The interfacing inductor and line impedance are identical for both DGs. The system parameters are listed in Table 6.2. The line impedance is fixed at 0.6283 Ω (with variation in *X/R* ratio). The nominal output voltages of both DGs are 230 V (rms) and they are set to share the active and reactive powers in the ratio DG1:DG2 = 1:2.

The performance of proposed scheme for different line impedance *X/R* ratios is shown in Figure 6.4. Transient response when the line impedance *X/R* ratio is 10 is shown in Figure 6.4 (a). This figure shows a smooth transient response for both DGs in achieving the required power demand. This is expected in the highly inductive line impedance case, as the output voltage angle and amplitude adjustment only affect the active and reactive powers respectively. When the line impedance *X/R* ratio is changed to 2, slight changes to the transient response and DGs output voltage amplitude and angle are observed in Figure 6.4 (b). Small fluctuation can be observed in active and reactive power transients when the line impedance *X/R* ratio is 1 as shown in Figure 6.4 (c). In the previous two cases, changing output voltage angle and amplitude starts to affect both active and reactive powers. Figure 6.4 parts (d) to (f) show that when the line impedance become more resistive (*X/R* < 0.5), the fluctuation in active and reactive power transients becomes larger and it takes longer for both DGs to achieve the required power demand. These occurs because of the resistive line impedance, where angle and amplitude adjustments have more effect on reactive and active powers respectively (which is the opposite to inductive line impedance). However, in this simulation, the availability of interfacing inductances contribute to the inductive element of the overall system impedance thus enabling both DGs to still achieve the required power demand with the existing control scheme.

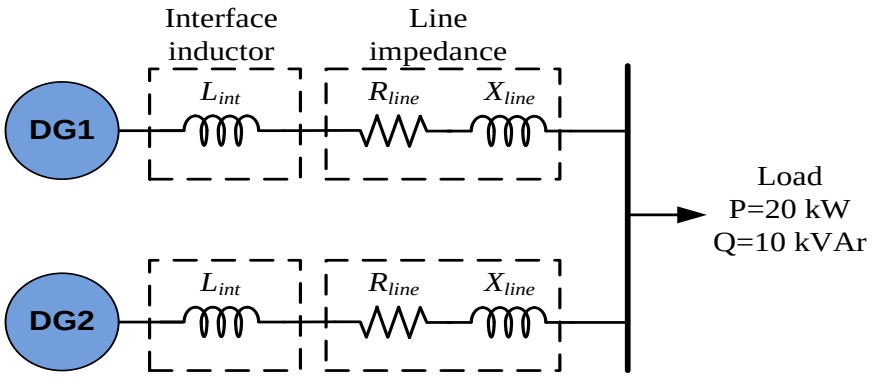
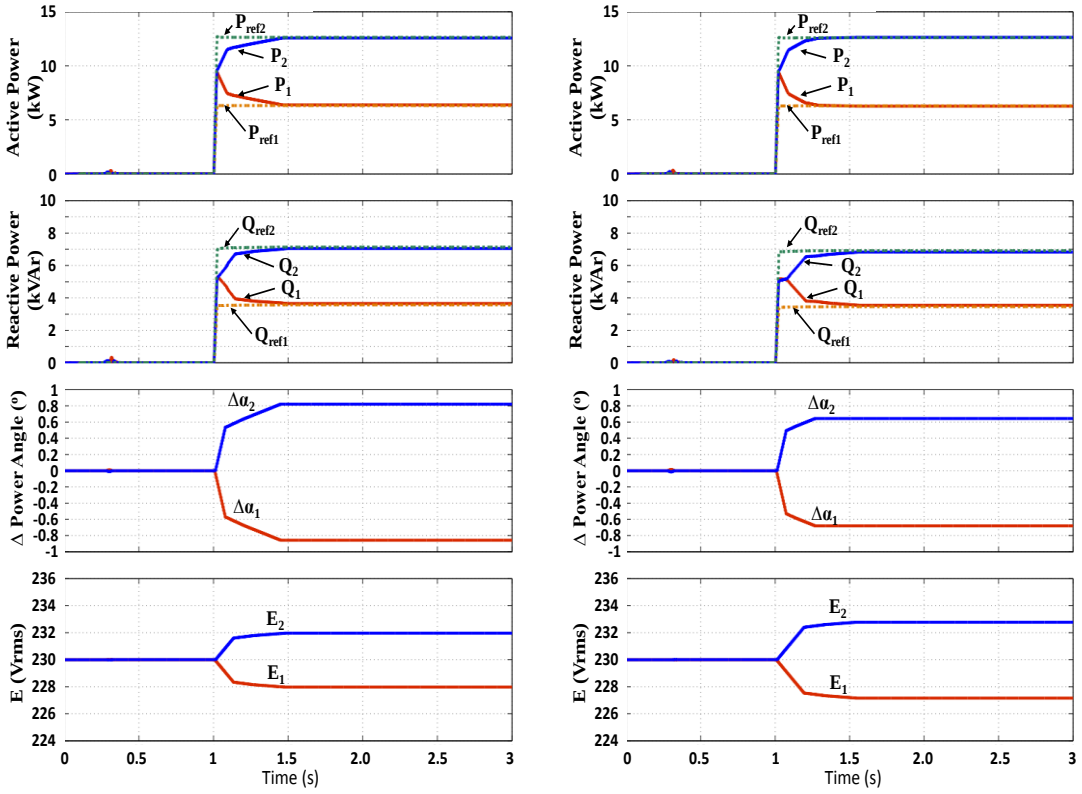
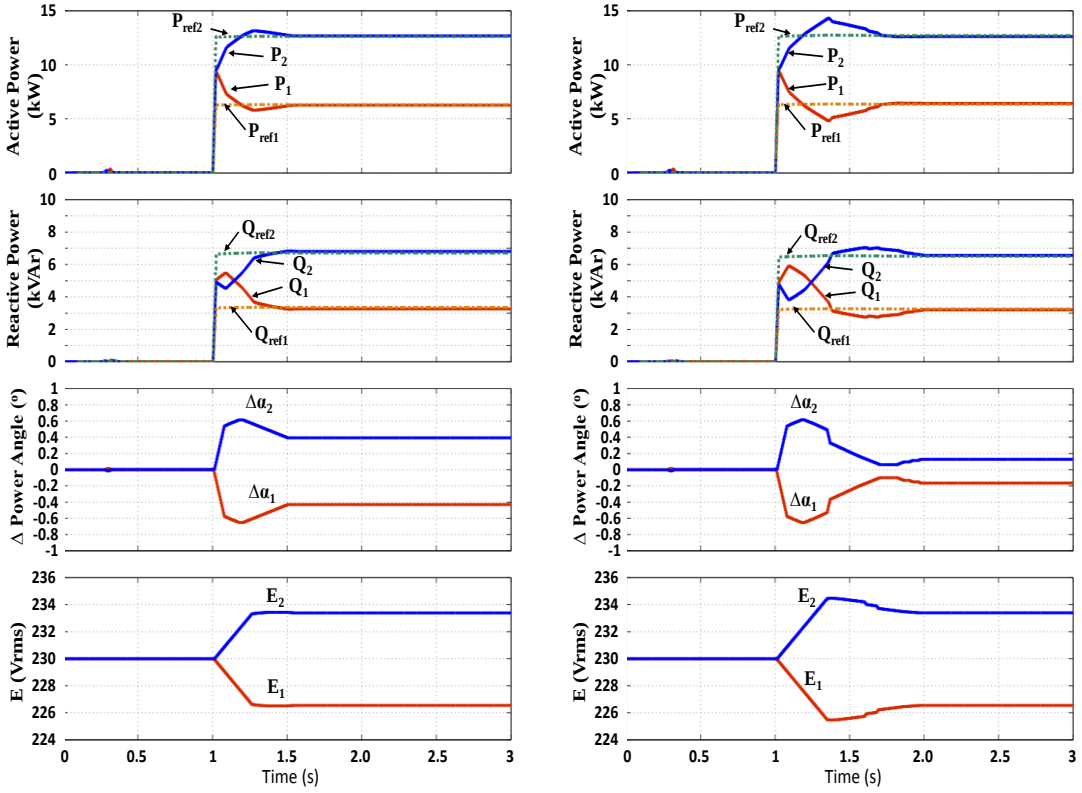


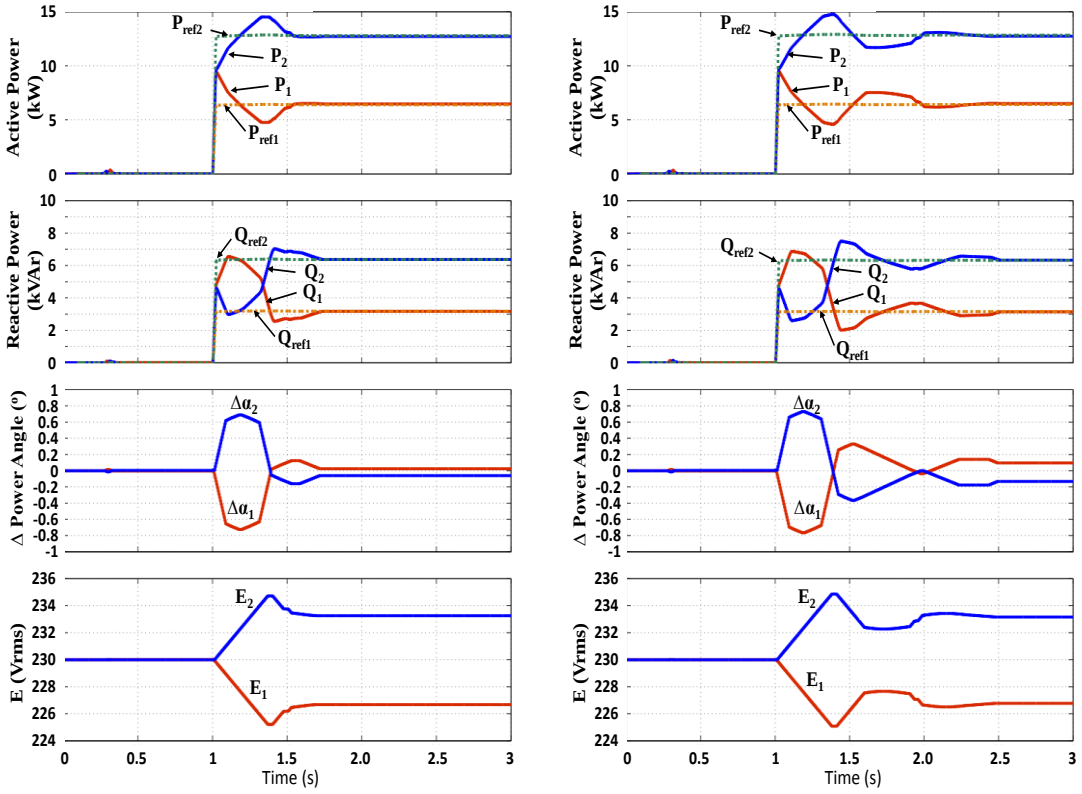
Figure 6.3 Simulation Part 1 microgrid configuration


Active Power (kW)
Reactive Power (kVAr)
Δ Power Angle (°)
E (Vrms)
Time (s)
P_{ref2}
P_2
P_1
P_{ref1}
Q_{ref2}
Q_2
Q_1
Q_{ref1}
$\Delta\alpha_2$
$\Delta\alpha_1$
E_2
E_1

(a) (b)


Active Power (kW)
Reactive Power (kVAr)
Δ Power Angle (°)
E (Vrms)
Time (s)
P_{ref2}
P_2
P_1
P_{ref1}
Q_{ref2}
Q_2
Q_1
Q_{ref1}
$\Delta\alpha_2$
$\Delta\alpha_1$
E_2
E_1

(c) (d)



(e) (f)

Figure 6.4 Proposed scheme performance for different *X/R* ratio of line impedance with $Z = 0.6283\ \Omega$: (a) *X/R* = 10, (b) *X/R* = 2, (c) *X/R* = 1, (d) *X/R* = 0.5, (e) *X/R* = 0.2, and (f) *X/R* = 0.1

Table 6.2 System parameters

Description	Symbol	Value
DC link voltage	V_{DC}	850 V
Switching frequency	f_{sw}	4.2 kHz
System frequency	f	50 Hz
Power adjustment period	T_d	5 ms
Max power adjustment time	T_r	600 ms
Filter inductance (all)	L_f	2 mH
Filter capacitance (all)	C_f	30 μF
Interfacing inductance (all)	L_{int1}	0.5 mH

6.4.2 Part 2 : Optimized power sharing scheme

This section presents Matlab/Simulink simulations to validate the performance of the proposed optimized power-sharing scheme. The rural islanded microgrid shown in Figure 6.1 that comprises of three DGs and eight loads is used. The system parameters are listed in Table 6.2 and Table 6.3. The DG nominal voltage amplitude is set higher than the microgrid base voltage to accommodate the voltage drop due to the interfacing inductance and line impedances. DG output voltage upper and lower limits are ±5% of the DG nominal voltage to avoid the load voltage going beyond a ±10% voltage variation limit. Distances between buses and their corresponding line resistance and reactance are shown in Table 6.4. The values used for line resistance and reactance are based on the assumption that single core XLPE/PVC low voltage power cable (70 mm^2) is used for the whole microgrid. This particular cable has AC resistance and reactance of 0.342 Ω/km and 0.0858 Ω/km respectively at 50 Hz. In Table 6.5, the number of houses in each load and active and reactive power consumption by each load during full loading and quarter loading, are shown. The active and reactive power consumptions during full loading are set by assuming each house in that load consume 5000 W and 3750 VAr (0.8 pf) at the same time.

Table 6.3 System parameters (Simulation part 2)

Description	Symbol	Value
DG nominal voltage	V	240 V (rms)
DG voltage upper limit	V_{HI}	252 V (rms)
DG voltage lower limit	V_{LO}	228 V (rms)
Microgrid base voltage	V_B	230 V (rms)
Microgrid base apparent power	S_B	200 kVA
DG 1 Rating		150 kW
DG 2 Rating		200 kW
DG 3 Rating		150 kW

Table 6.4 Distance between buses and corresponding line resistance and reactance.

	Distance (m)	**R (Ω)**	**X (Ω)**
D1	550	0.188	0.047
D2	500	0.171	0.043
D3	700	0.239	0.060
D4	650	0.222	0.056
D5	450	0.154	0.039
D6	400	0.137	0.034
D7	600	0.205	0.051
D8	750	0.257	0.064
D9	300	0.103	0.026
D10	350	0.120	0.030

Table 6.5 Loads Active and reactive power consumption

Load	**No of houses**	**Full loading**		**Quarter loading**	
		P (W)	**Q (VAr)**	**P (W)**	**Q (VAr)**
Load 1	9	45000	33750	11250	8438
Load 2	13	65000	48750	16250	12188
Load 3	8	40000	30000	10000	7500
Load 4	14	70000	52500	17500	13125
Load 5	6	30000	22500	7500	5625
Load 6	9	45000	33750	11250	8438
Load 7	12	60000	45000	15000	11250
Load 8	9	45000	33750	11250	8438

Simulations are separated into three cases that have different loading configurations. In all cases, the proposed scheme is compared to the conventional technique. In the conventional scheme, the active and reactive powers are shared among DGs based on the power rating of each DGs (DG1:DG2:DG3 = 3:4:3).

a) Case 1 (Loading concentrated near DG1)

All three DGs are connected to the microgrid and all loads operate at a quarter loading condition. While the system is in steady state, loads 1, 2 and 3 are increased to full loading at t=4s. The simulation results are shown in Figure 6.5. In this simulation, high power is demanded by the loads near DG 1. Using the proposed scheme, most of the power demands are supplied from DG 1, followed by DG 2 and DG 3 as shown in Figure 6.5 (a). For the conventional scheme, the active power demands are shared by DGs based on their rating as shown in Figure 6.5 (b). Due to

the limitation set for voltage amplitude variation, the reactive power sharing based on DG power rating cannot be achieved, resulting in DG 1 supplying more reactive power while DG 3 absorbs reactive power. The active and reactive power losses in the line for both the proposed and conventional schemes are shown in Figure 6.5 parts (c) and (d) respectively. These results show that the proposed scheme is able to reduce the active and reactive power losses by 11550 W and 3024 VAr (0.058 pu and 0.015 pu) respectively. These represent improvements of 56.4% and 34.2% in active and reactive power losses respectively.

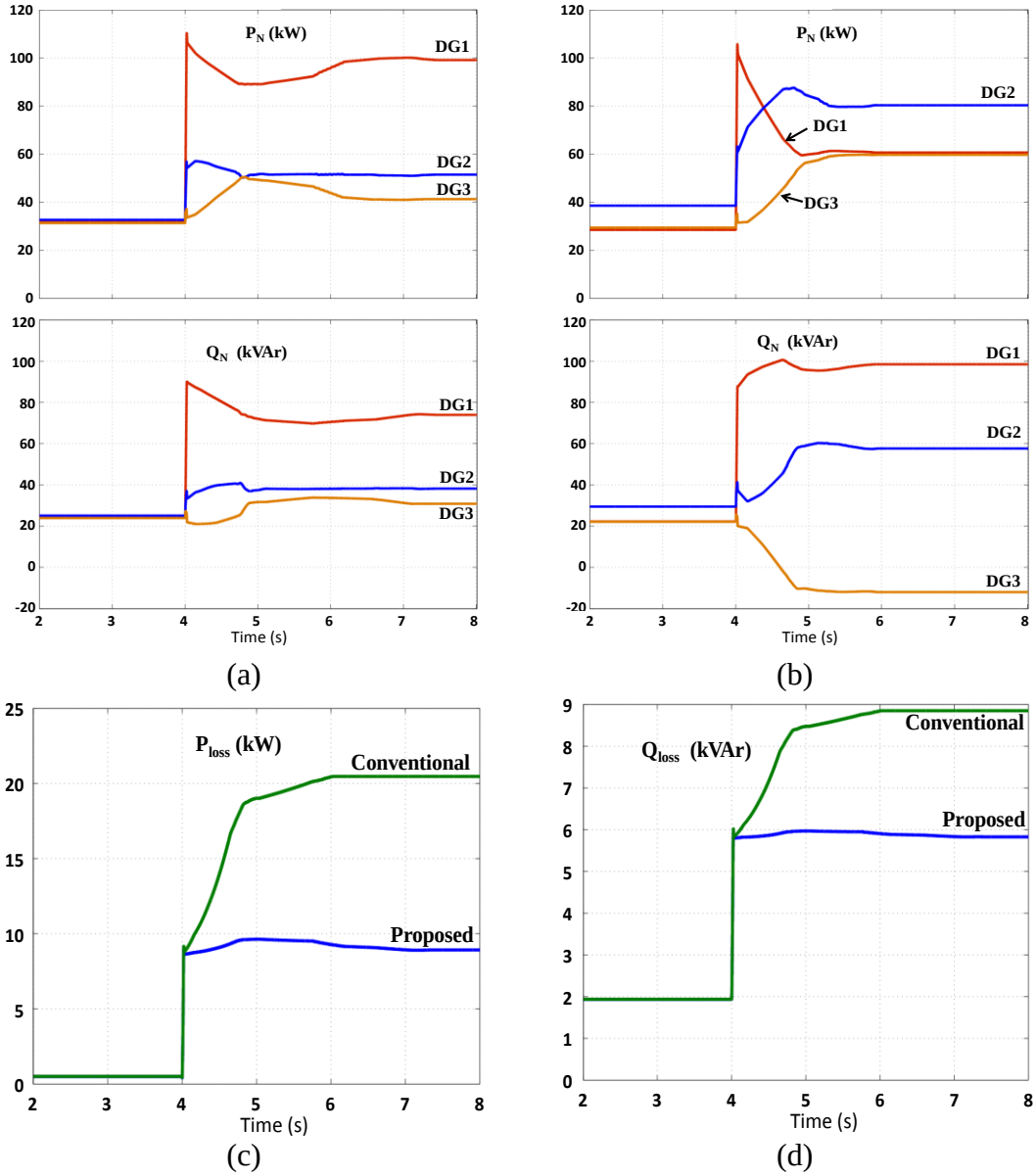


Figure 6.5 Simulation results for Case 1: (a) DGs output *P* and *Q* using proposed scheme (b) DGs output *P* and *Q* using conventional power sharing, (c) active power losses, and (d) reactive power losses

DG output voltage and load voltage regulation results for the proposed and conventional schemes are shown in Figure 6.6 parts (a) and (b) respectively. Using the proposed scheme, the DG output voltage deviation from the set point (240 V) is minimized. At steady state, the output voltages of DG 1, DG 2 and DG 3 are 234.7 V, 240.1 V and 246.5 V respectively. All loads voltages at steady state are within ±10% of the system voltage (207 V to 253 V). The lowest load voltage is measured at Load 2 (211.5 V) while the highest is at Load 8 (241.6 V).

For the conventional scheme, from Figure 6.6 (b), in steady state, DG 1, DG 2 and DG 3 output voltages are 228 V, 245.6 V and 252 V respectively. Due to the low output voltage at DG 1, Load 1 and Load 2 which are located near this DG suffer from low voltage (206.3 V and 202.8 V respectively), outside the -10% limit. At the high side, due to the high voltage at DG 3, Load 7 and Load 8, those are located near this DG, have high voltage (249.9 V and 250.2 V respectively) which near the +10% mark.

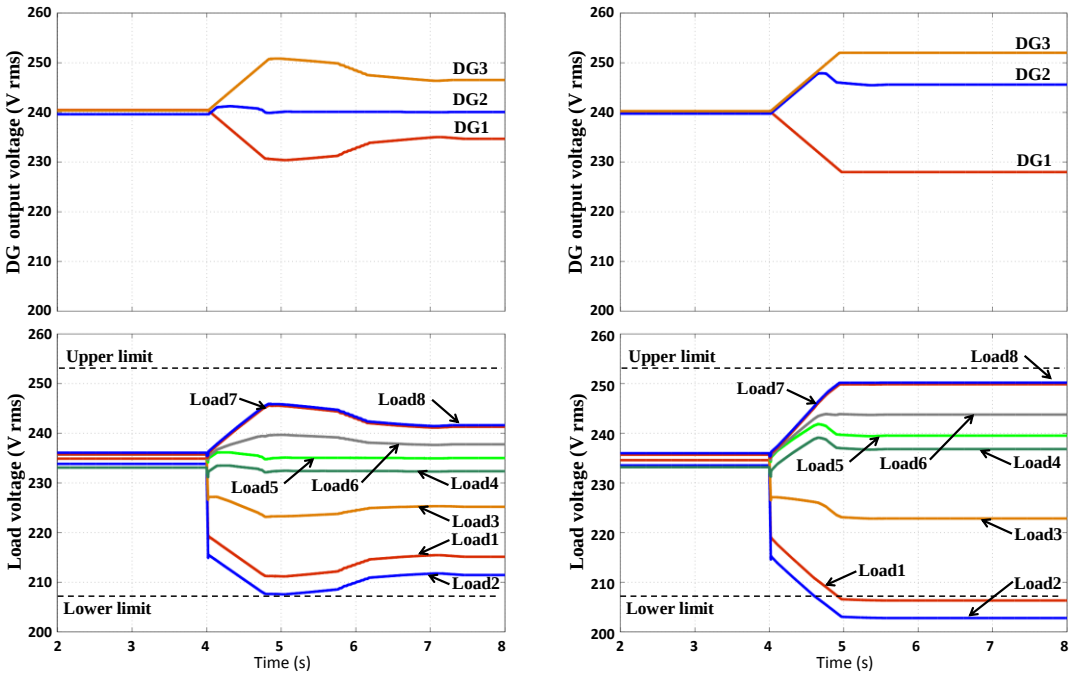


Figure 6.6 DG output voltage and load voltage regulation for Case 1: (a) proposed and (b) conventional technique.

b) Case 2 (Load concentration near DG3)

In this case, the initial condition is the same as case 1 but after t=4s, loads 6, 7 and 8 are increased to full load. With the proposed scheme, the central controller detects the loading condition and identifies that most of power demand should be supplied from DG 3 as it is nearest the loads, as shown in Figure 6.7 (a). The DG output active and reactive powers using the conventional scheme are shown in Figure 6.7 (b). The result shows that the output active power ratio follows the rating of DGs. However due to the limitation set on voltage amplitude variation, DG 1 and DG 3 are unable to correct their reactive power because their output voltage amplitude reaches the upper and lower limit respectively. Hence, reactive power sharing based on DG power rating cannot be achieved. Figure 6.7 parts (c) and (d) show active and reactive power losses for the proposed and conventional schemes respectively. The results show that using proposed scheme, 10190 W and 2684 VAr (0.051 pu and 0.013 pu) of active and reactive powers can be saved. These indicate improvements of 61.6% and 33.9% in active and reactive power losses respectively.

Figure 6.8 parts (a) and (b) show DG output voltage and load voltage regulation for the proposed and conventional schemes respectively. For the proposed scheme, DG 1, DG 2 and DG 3 output voltage at steady state are 247 V, 240.4 V and 234 V respectively. Among the loads, Load 1 has the highest voltage (240.7 V) while load 7 has the lowest (217.9 V). These are well within the specified limits.

Figure 6.8 (b) shows that when using the conventional scheme, the DG output voltages at steady state are 252 V, 244.9 V and 228 V for DG 1, DG 2 and DG 3 respectively. Load 1 has the highest voltage at 248.8 V while Load 7 has the lowest voltage (209.4 V), nearly reaching the 207 V limit.

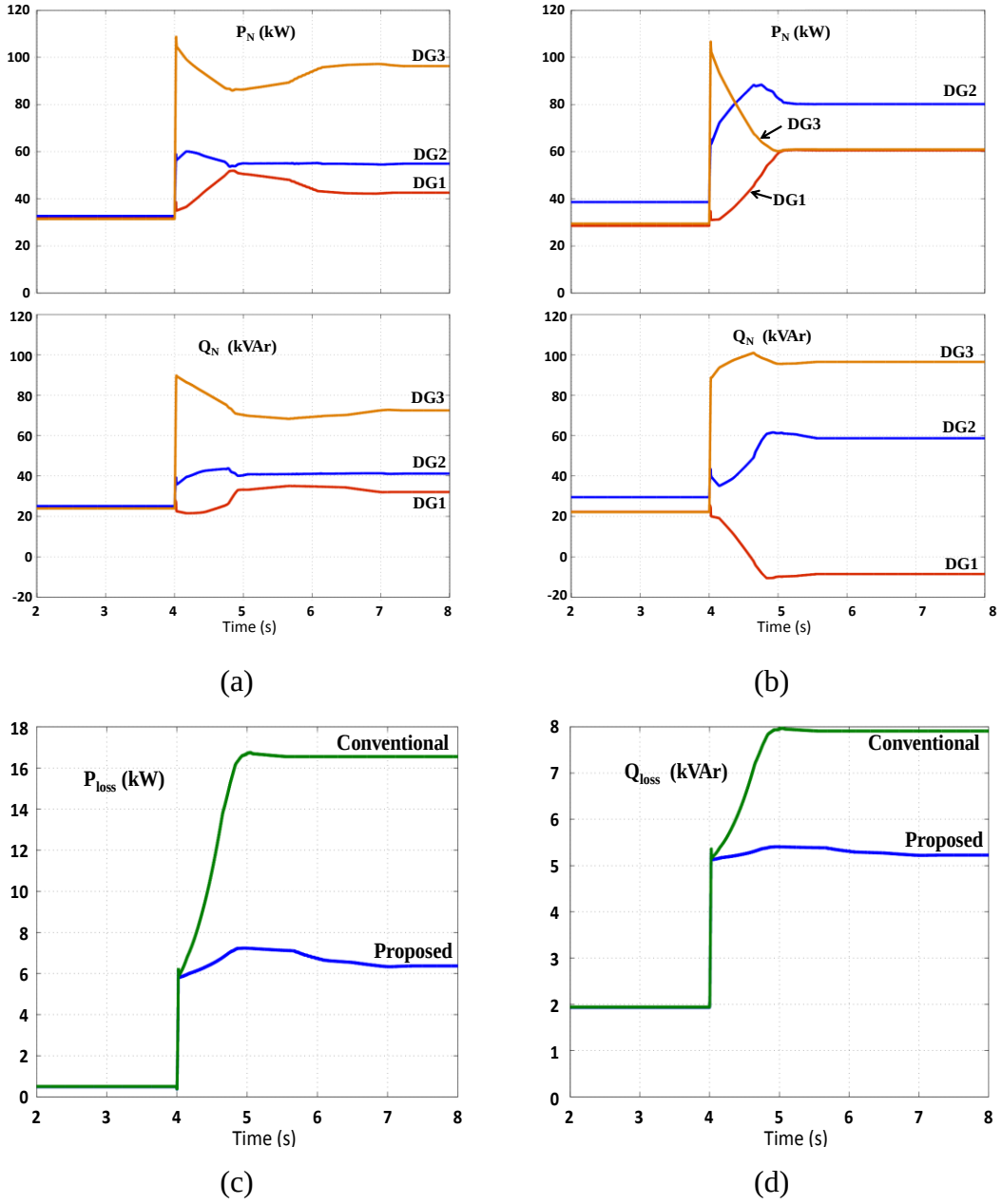
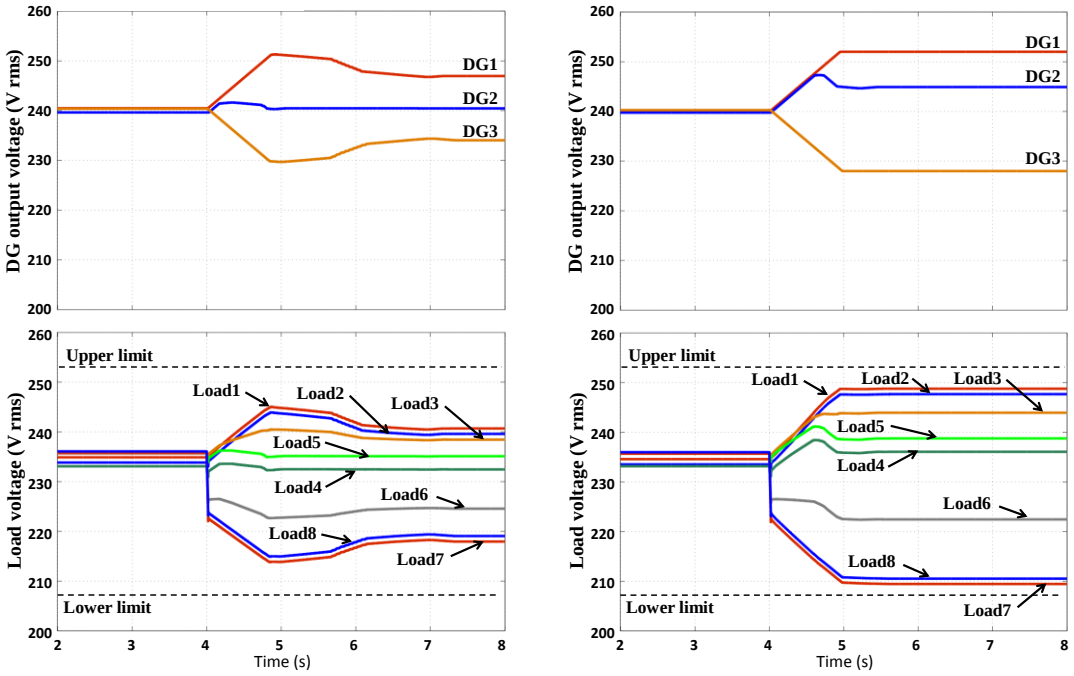


Figure 6.7 Simulation results for case 2: (a) DGs output *P* and *Q* using proposed scheme (b) DGs output *P* and *Q* using conventional power sharing, (c) active power losses, and (d) reactive power losses.

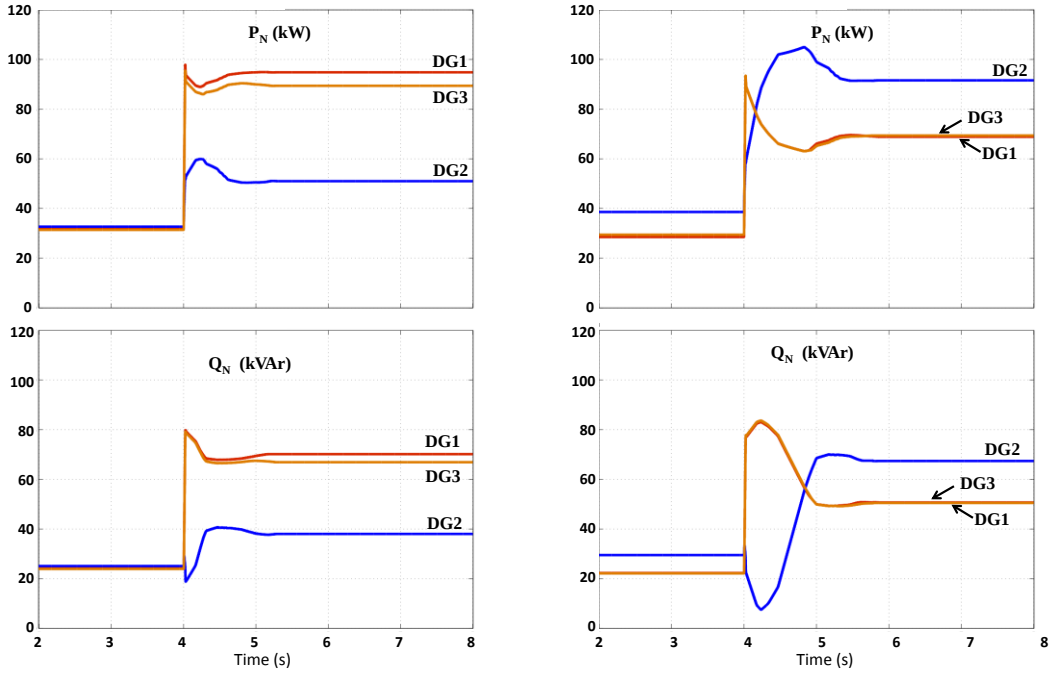


(a) (b)

Figure 6.8 DG output voltage and load voltage regulation for Case 2: (a) proposed and (b) conventional

c) Case 3 (Loading concentration near DG1 and DG3)

All three DGs are connected to the microgrid and all loads are operating at quarter loading. While the system is in steady state, loads 1, 2, 7 and 8 are increased to full load at *t*=4s. This case represents loading concentration near DG 1 and DG 3. Using the proposed scheme, most of the power demands are supplied from DG 1 and DG 3 and less power from DG 2 as it is located farthest from the loads as shown in Figure 6.9 (a). The power sharing based on individual inverter rating (conventional power sharing) is shown in Figure 6.9 (b). The active and reactive power losses in the line for both the proposed and conventional schemes are shown in Figure 6.9 parts (c) and (d) respectively. The proposed scheme reduces the active and reactive power losses by 4624 W and 1050 VAr (0.023 pu and 0.005 pu) respectively. The active and reactive power losses are improved by 28.9 % and 12.6 % respectively.



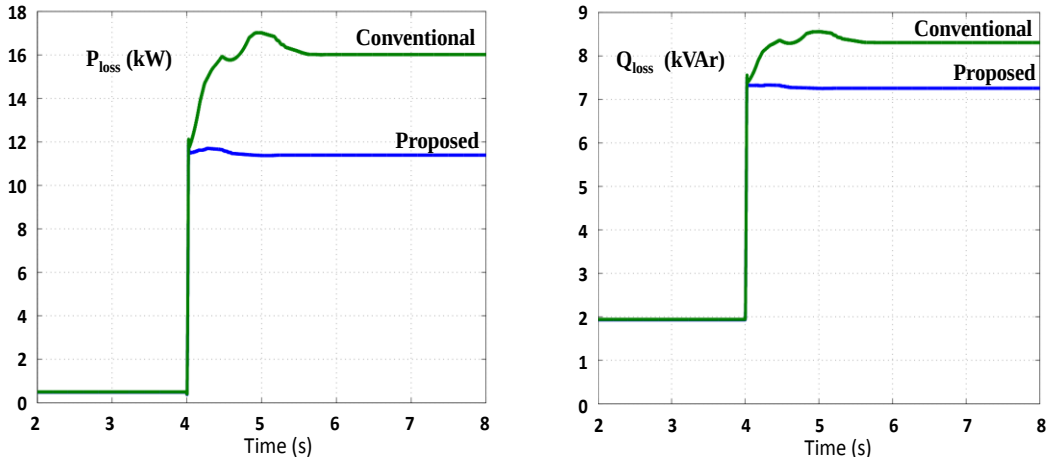


Figure 6.9 Simulation results for case 3: (a) DGs output *P* and *Q* using proposed scheme (b) DGs output *P* and *Q* using conventional power sharing, (c) active power losses, and (d) reactive power losses.

DGs output voltage and loads voltage regulations for the proposed and conventional schemes are shown in Figure 6.10 parts (a) and (b) respectively. Using the proposed scheme, at steady state, the output voltages of DG 1, DG 2, and DG 3 are 238.9 V, 241.2 V and 237.1 V respectively. All load voltages at steady state are well within the limits. The lowest load voltage is Load 2 (215.8 V) while the highest is at Load 5 (236.1 V).

Using the conventional scheme, in Figure 6.10 (b), at steady state, DG 1, DG 2 and DG 3 output voltages are 230.6 V, 247.2 V and 230.8 V respectively. Load 2 has the lowest voltage among the loads at 209.2 V which almost reaches the 207 V lower limit. At the extreme, Load 5 has the highest voltage at 240.3 V. From these results, it is clear that the proposed scheme not only produces lower active and reactive power losses but also achieves better load voltage regulation.

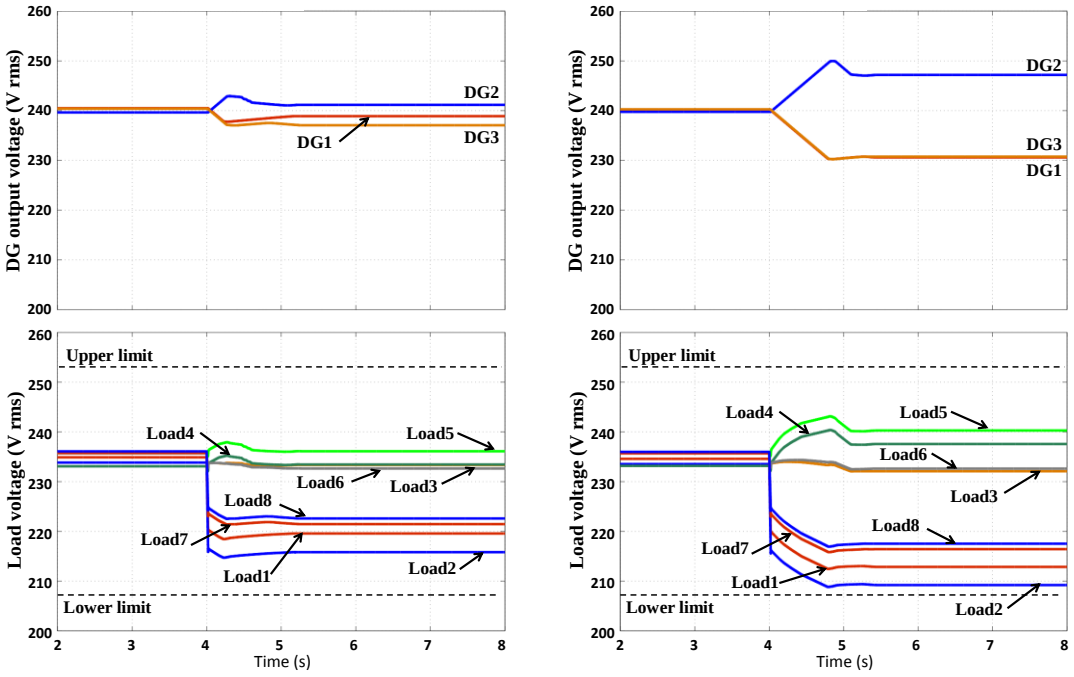


Figure 6.10 DG output voltage and load voltage regulation for Case 3: (a) proposed and (b) conventional.

6.5 Experimental results

A low scale microgrid prototype of two inverters and three loads is used to validate the practicality of the proposed optimized power-sharing scheme. The hardware arrangement is shown in Figure 6.11. Each inverter is controlled by an Infineon TriCore™ TC1796B and the same DSP type is used for the central controller. From Figure 6.11, inverter 1's interfacing inductor is connected to load 1 through Z_{line1}. Load 1 is connected to load 2 through Z_{line2}, while load 2 bus is connected to load 3 through Z_{line4}. Finally, load 3 bus is connected to inverter 2's interfacing inductor through Z_{line3}. Wire coils are used to emulate the line impedances. Each coil has resistance and reactance values around 0.3 Ω and 0.063 Ω respectively (the values are near identical for all coils so it can be assumed that the number of coils indirectly represents distance). The communication between an inverter and the central controller is implemented using PWM channels at the source and low-pass filters at the destinations. Voltage and current for each load are measured and directly feed to the central controller for the load power consumption measurements. The test rig parameters are shown in Table 6.6.

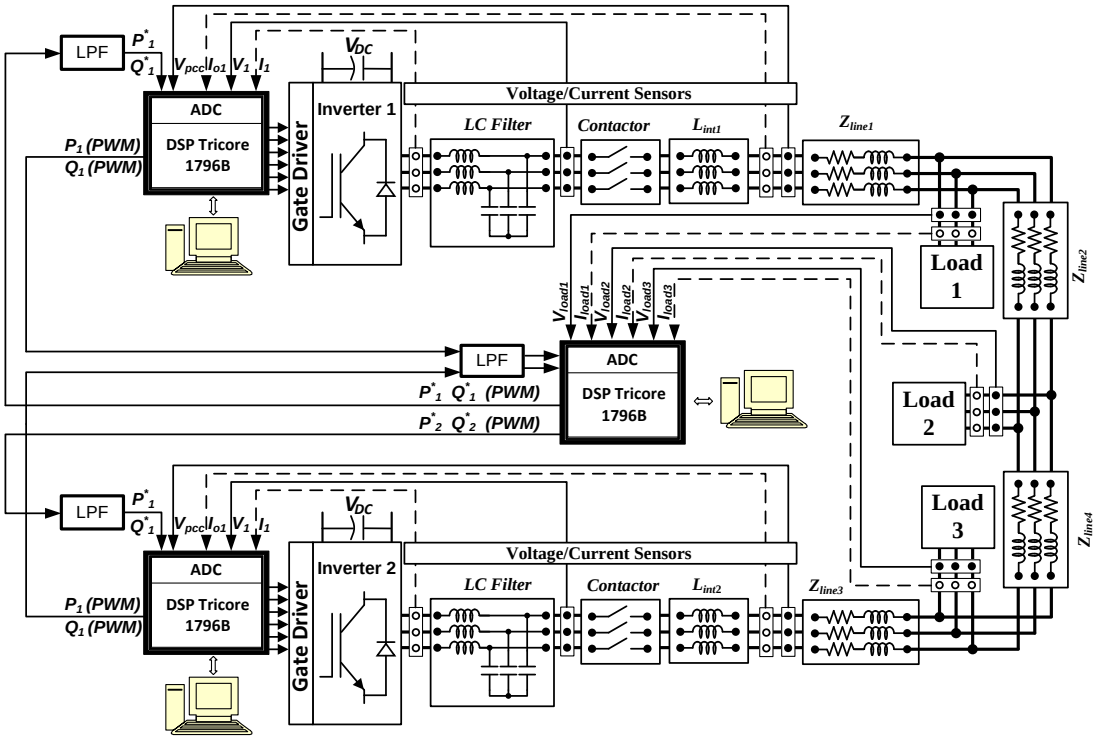


Figure 6.11 Hardware arrangement

Table 6.6 Hardware implementation - system parameters

Description	**Symbol**	**Value**
DC link voltage	V_{DC}	150 V
Reference voltage	V_{ref}	60 V (peak)
Switching frequency	f_{sw}	4.2 kHz
System frequency	f	50 Hz
Communication frequency	f_{comm}	10 kHz
Power adjustment period	T_d	5 ms
Max power adjustment time	T_r	300 ms
Filter inductance (all)	L_f	2 mH
Filter capacitance (all)	C_f	30 μF
Interfacing inductance 1	L_{int1}	5 mH
Interfacing inductance 2	L_{int2}	6.2 mH
Line impedance 1	Z_{line1}	0.31 Ω
Line impedance 2	Z_{line2}	0.31 Ω
Line impedance 3	Z_{line3}	0.31 Ω
Line impedance 4	Z_{line4}	0.62 Ω
Inverter 1 Rating		0.5 kW
Inverter 2 Rating		0.5 kW

Experimental results are divided into 6 tests that show different cases of changing load conditions. The loading conditions of each test are shown in Table 6.7. In each test, two different power ratio settings are used. The first is the proposed scheme which calculates the power ratios based on the distance between each inverter to each load and the ratio of each load power to the overall loads. The second scheme is the conventional scheme where power sharing is based on the power rating of each inverter. As the power ratings for both inverters are the same, they should equally share. The experimental results (power measurements) for all the 6 tests are shown in Table 6.7. The output current waveforms for Test 1, 2 and 3 are shown in Figure 6.12 while output current waveforms for Test 4, 5 and 6 are shown Figure 6.13.

6.5.1 Test 1 : No load → load 1

In this test, as load 1 is located nearer to inverter 1, most of the power should come from that inverter. From Table 6.7, with the proposed scheme, calculated power ratios for inverters 1 and 2 are 0.8 and 0.2 respectively. Figure 6.12 (a) shows that output current from inverter 1 is around 4 times that from inverter 2 and Figure 6.12 (b) shows equal current sharing between both inverters. Power losses in the line for the proposed and conventional schemes are 8.2 W and 20.5 W respectively. These results show that the proposed scheme is able to reduce the active power loss by 60%.

6.5.2 Test 2 : No load → load 3

When load 3 is connected to the microgrid, the opposite to the previous test can be seen. More current comes from inverter 2 as it is located nearer to this inverter compared to inverter 1. Figure 6.12 (c) shows that output current from inverter 2 is around 4 times that from inverter 1 and Figure 6.12 (d) shows equal current sharing between both inverters. Power losses in the line for the proposed and conventional schemes are 5.7 W and 13.7 W respectively (a 58.4% reduction in power loss).

6.5.3 Test 3 : No load → load 2

Load 2 is separated from inverter 1 and inverter 2 through 0.62 Ω and 0.93 Ω of line impedances respectively. To minimize line power loss, more current should be provided by inverter 1. In this case, the calculated power ratio using the proposed schemes is R_{P1}:R_{P2}=0.6:0.4. Figure 6.12 parts (e) and (f) show output current for the proposed and conventional schemes respectively. In term of power loss, the proposed and conventional schemes suffer 15.5 W and 22.7 W of active power losses respectively (a 31.7% reduction in power loss).

Table 6.7 Hardware implementation results

Test	**Test 1**		**Test 2**		**Test 3**		**Test 4**		**Test 5**		**Test 6**	
Load Conditions	No load → Load 1		No load → Load 3		No load → Load 2		Load 3 → Load 1+3		Load 2+3 → Load 1+2+3		Load 1+2+3 → Load 1+2	
Ratio Type *	C	P	C	P	C	P	C	P	C	P	C	P
Inverter 1 active power ratio, R_{P1}	0.5	0.8	0.5	0.2	0.5	0.6	0.5	0.485	0.5	0.521	0.5	0.698
Inverter 2 active power ratio, R_{P2}	0.5	0.2	0.5	0.8	0.5	0.4	0.5	0.515	0.5	0.479	0.5	0.302
Inverter 1 active power reference, P^*_1 (W)	108.9	168.5	115.9	44.9	112.2	130.5	220.5	207.4	323.8	334.6	218.5	297.0
Inverter 2 active power reference, P^*_2 (W)	108.9	39.7	115.9	179.6	112.2	87.0	220.5	220.6	323.8	307.4	218.5	128.3
Inverter 1 active power output, P_1 (W)	109.4	162.7	112.0	47.9	111.2	130.3	222.9	215.1	323.5	334.6	220.3	296.5
Inverter 2 active power output, P_2 (W)	108.5	41.7	119.8	176.6	113.3	87.2	218.1	223.8	324.0	307.4	216.7	128.9
Active power output sum (P_1+P_2), P_{SUM} (W)	217.9	204.4	231.7	224.5	224.5	217.6	441.0	439.0	647.6	642.0	437.0	425.3
Load 1 active power, PL_1 (W)	197.4	196.2	0.0	0.0	0.0	0.0	192.7	193.9	189.0	189.9	191.3	190.8
Load 2 active power, PL_2 (W)	0.0	0.0	0.0	0.0	201.7	202.0	0.0	0.0	193.2	194.3	197.4	197.3
Load 3 active power, PL_3 (W)	0.0	0.0	218.0	218.8	0.0	0.0	214.1	214.9	211.3	212.5	0.0	0.0
Load active power sum ($PL_1+PL_2+PL_3$), PL_{SUM} (W)	197.4	196.2	218.0	218.8	201.7	202.0	406.7	408.8	593.6	596.7	388.7	388.1
Power loss **($P_{SUM} - PL_{SUM}$), P_{loss} (W)**	20.5	8.2	13.7	5.7	22.7	15.5	34.3	30.2	54.0	45.3	48.3	37.2

*** C = Conventional P = Proposed**

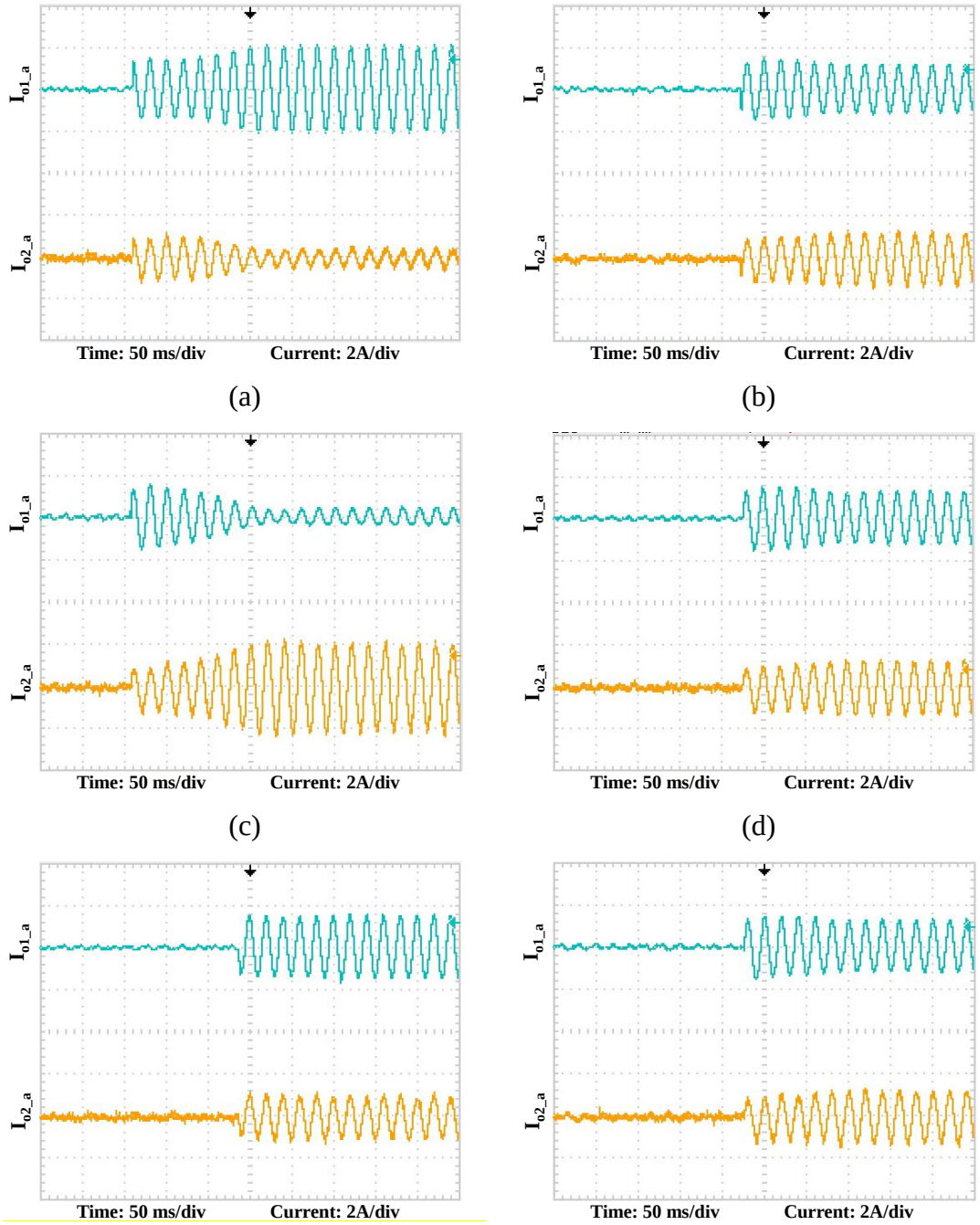


Figure 6.12 Experimental results output current waveforms : (a) Test 1 – proposed ; (b) Test 1 – conventional; (c) Test 2 – proposed; (d) Test 2 – conventional; (e) Test 3 – proposed, and (f) Test 3 – conventional.

6.5.4 Test 4 : Load 3 → load 1+3

In this test, initially only load 3 is connected to the microgrid, and, when using the proposed scheme, the calculated power ratio is R_{P1}:R_{P2}=0.2:0.8. When load 1 is connected, the power ratio changes to R_{P1}:R_{P2}=0.48:0.51. This change is shown by the output current waveform in Figure 6.13 (a). Figure 6.13 (b) shows that using the conventional scheme, the output currents of both inverters 1 and 2 are almost the same before and after the connection of load 1. The power losses after load 1 connection are 30.2 W and 34.3 W for the proposed and conventional schemes respectively (a 12% reduction in power loss)

6.5.5 Test 5 : Load 2+3 → load 1+2+3

Loads 2 and 3 are initially connected to the microgrid and the calculated power ratio is R_{P1}:R_{P2}=0.39:0.61. When load 1 is connected, the power ratio changes to R_{P1}:R_{P2}=0.52:0.48. This power ratio changes are indirectly shown by the inverters output current in Figure 6.13 (c). Using the conventional scheme, power demands are shared equally between both inverters and their output currents are shown in Figure 6.13 (d). The power losses after the connection of load 1 are 45.3 W and 54 W for the proposed and conventional schemes respectively (a 16.1% reduction in power loss).

6.5.6 Test 6 : Load 1+2+3 → load 1+2

Load 1, 2 and 3 are initially connected to the microgrid and based on previous test, the calculated power ratio is R_{P1}:R_{P2}=0.52:0.48. When load 3 is disconnected, the power ratio changes to R_{P1}:R_{P2}=0.7:0.3. This change can be indirectly seen by the output current waveform in Figure 6.13 (e). Figure 6.13 (f) shows that using the conventional scheme, the output current of both inverters 1 and 2 are almost equal before and after the disconnection of load 3. Power losses in the line for the proposed and conventional schemes are 37.2 W and 48.3 W (a 23% reduction in power loss).

Figure 6.13. Experimental results output current waveforms: (a) Test 4 – proposed; (b) Test 4 – conventional; (c) Test 5 – proposed; (d) Test 5 – conventional; (e) Test 6 – proposed, and (f) Test 6 – conventional.

6.6 Summary

In this chapter, an extension of the proposed power sharing technique from the previous chapter has been presented. In this proposed scheme, the power ratio assigned to each DG is calculated based on two parameters: i) distance between each DG to each load and ii) ratio of power consumed by each load to the overall loading. A case study of a rural islanded microgrid that consist of 3 DGs and 8 loads (groups of houses) has been presented and simulation results show that the proposed power sharing scheme is able to reduce the active and reactive power losses in the distribution line. For the first case, when loads are concentrated near DG1, the proposed power sharing scheme reduces the active and reactive power losses by 56.4% and 34.2% respectively. 61.6% and 33.9% improvement in active and reactive power losses can be observed in the second case when loads are concentrated near DG3. For the final case when loads are concentrated near DG1 and DG3, active and reactive power losses are improved by 28.9% and 12.6% respectively. Furthermore, the proposed scheme produces better load voltage regulation than the conventional scheme. A scaled down microgrid consisting of two inverters and three loads is used to validate the practicality of the proposed optimized power-sharing scheme. All the 6 tests show that the proposed scheme is able to reduce active power loss and the improvement varies from 12% to 60% depending on the load conditions.

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Chapter 7

Conclusion

7.1 General conclusion

In recent years, distributed generation (DG) has gain popularity as an alternative to the conventional power system. The first chapter of the thesis discussed DG background, development, technologies, advantages and challenges. DGs are usually managed in a more decentralized way through the concept of a microgrid. This thesis focuses on improving the power sharing among parallel connected DGs and reducing the distribution power losses in an islanded microgrid.

From chapter two, it can be concluded that the control techniques for an islanded microgrid are currently dominated by droop based techniques. This is because they have advantages in terms of flexibility due to lack of communication among parallel connected inverters. However due to communication advancements some active load sharing techniques can be developed as alternatives to droop based techniques. In chapter three, ac power flow analysis for inverters under the effect of inductive, resistive and complex line impedance was investigated. Some figures have been utilized in order to visualize the impact of voltage power angle and amplitude on active and reactive power flow in an ac system at different voltage levels. Also, a new circulating current definition for multiple parallel connected inverters connected to the same load bus has been proposed.

In chapter four, to improve the conventional IACS controller which performs poorly under line impedance mismatching, an improved IACS controller with two additional gain schedulers was proposed. One gain scheduler changes the modulation index of the modulating signal while the other modifies the current error signal. The superiority of the proposed IACS controller, compared to the conventional controller, has been verified by simulations and hardware experimentation.

A new power sharing scheme for parallel connected inverters in an islanded microgrid was proposed in chapter five. The technique requires low-bandwidth communication between inverters and the central controller for active and reactive power information exchange. The performance of the proposed power sharing

scheme was compared to the conventional droop technique in simulation. The proposed power sharing method outperforms conventional droop control as it has a faster dynamic response, better sharing of reactive power between inverters that have different line impedances, and has the ability to set the active and reactive power ratio for each inverter. The ability to set specific active and reactive power ratios gives flexibility to the utility owner to manage the available power in an efficient and effective manner.

In chapter six, an optimized power sharing scheme was proposed. The distance between each DG to each load and the ratio of power consumed by each load to the total load are taken into consideration for power ratio calculation in the central controller. A case study of a rural islanded microgrid that consists of 3 DGs and 8 loads (group of houses) has been presented. Simulation results show that the proposed power sharing scheme reduces the active and reactive power losses in the distribution line and has better load voltage regulation that the conventional scheme. A scaled microgrid consisting of two inverters and three loads was used to validate the practicality of the proposed optimized power-sharing scheme.

7.2 Author's contribution

The research undertaken in this thesis focuses on improving parallel connected DG power sharing with line impedance mismatch. The thesis contribution is summarized as follows:

- Detailed ac power flow analysis of an inverter based system connected to a common bus through purely resistive, inductive or complex line impedances has been presented. For each line impedance case, the effect of an inverter's output voltage power angle and amplitude on the active and reactive power flow have been studied.
- New generalized circulating current definition for multiple parallel connected inverters connected to the same load bus has been proposed and verified with simulation.
- An improved instantaneous average current sharing (IACS) scheme was proposed. Embedded two gain schedulers into the conventional IACS scheme

enhances its performance when controlling parallel connected inverters with different line impedances.

- A generalized model of single-phase parallel connected inverters using the improved IACS scheme was derived and used for voltage and current controller design and the parameter selection process.
- A new power sharing scheme for parallel connected inverters in an islanded microgrid has been proposed.
- An optimized power sharing scheme incorporates power ratio calculation based on two parameters: i) distance between each DG to each load and ii) ratio of power consumed by each load to the overall total load. This scheme reduces distribution power losses and improves load voltage regulation.

7.3 Suggestion for future research

Potential areas for further research include:

- In chapter 3, circulating current in multiple parallel connected inverters connected to the same load bus is defined. This definition can be further generalized for multiple parallel connected inverters with several distributed loads.
- The proposed gain scheduler can be implemented into a different controller scheme (droop, master slave … etc.).
- The proposed power sharing scheme can be further improved by having an advance adaptive function that can adaptively modify the amount of angle and amplitude adjustment based on the active and reactive power differences.
- Studying the implementation of the proposed power sharing scheme under unbalanced load conditions.
- Investigation of the proposed power sharing scheme in the grid connected mode.
- The optimized power sharing scheme presented in chapter 6 can be further improved by incorporating a load voltage restoration function. By having this feature, the central controller can command the parallel connected DGs to increase or decrease their output voltages to ensure all loads are operated closest to their rated voltage.

Appendix A

Test Rig Structure

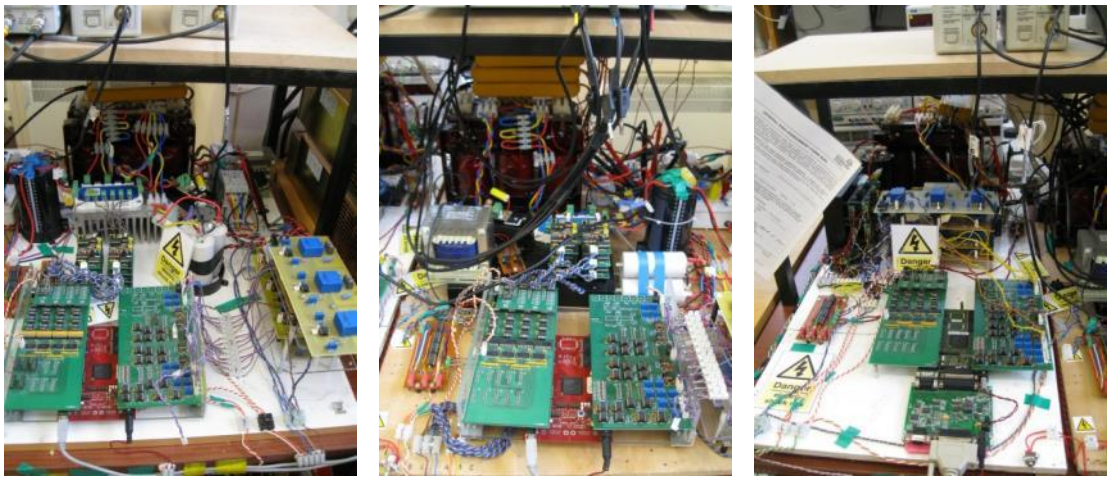
Details about inverter elements, line impedance, loads, measuring equipment and simulation software are introduced here.

A.1 Inverter elements

The picture of the test rig is shown in Figure A.1. It consists of 3 sets of three phase voltage source inverters and several sets of loads. All the three inverter sets are shown in Figure A.2. Each inverter set comprises the following components:

- DSP: Infineon *TriCore* 1796B
- DSP interfacing circuit
- DC power supplies.
- IGBT module
- DC link capacitors
- LC filter
- Gate drive circuits
- Current and voltage transducers
- Interfacing inductor
- Line impedance

Figure A.1 Full test rig



(a) (b) (c)

Figure A.2 Inverter sets. (a) Inverter 1, (b) Inverter 2 and (c) Inverter 3

A.1.1 Digital signal processor (DSP)

The main purpose of the DSP is to perform the control algorithm based on the measured signals it received and then generate the switching pattern to drive the inverter switches. The measured signals are the digitized analogue signals that it received from the current and voltage transducers. The Infineon 32-bit TriCore 1796B DSP used in this project is shown in Figure A.3 and is used for all the three inverter sets.

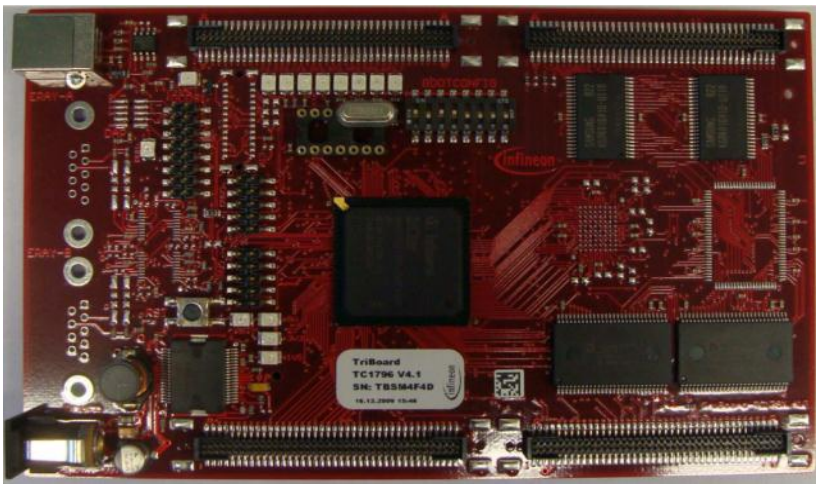


Figure A.3 Infineon 32-bit TriCore 1796B DSP

Some of its features are listed below:

- High performance 32-bit super-scalar *TriCore*™ V1.3 CPU with 4 stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision floating point unit (FPU)
  - 150 MHz at full automotive temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
- Multiple on-chip memories
  - 2 Mbyte embedded program flash with ECC
  - 128 Kbyte data flash
  - 192 Kbyte on chip SRAM
  - 16 Kbyte instruction cache

- 16-channel DMA controller
- 32-bit External Bus Interface Unit (EBU)
- Sophisticated interrupt system with 2x255 hardware priority arbitration levels serviced by CPU and PCP2
- High performing triple bus structure
- Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC)
  - Two High-Speed Synchronous Serial Channels (SSC)
  - One Multi CAN Module with four CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer
  - Two General Purpose Timer Array Modules (GPTA) with additional Local Timer Cell Array (LTCA2)
  - Two 16-channel Analog-to-Digital Converter units (ADC) with selectable 8-bit, 10-bit, or 12-bit resolution
  - One 4-channel Fast Analog-to-Digital Converter unit (FADC) with concatenated comb filters for hardware data reduction: supporting 10-bit resolution, min. conversion time of 280ns
- 44 analog input lines for ADC and FADC
- 123 digital general purpose I/O lines, 4 input lines
- Digital I/O ports with 3.3 V capability
- Dedicated Emulation Device chip for multi-core debugging, tracing, and calibration via USB V1.1 interface available (TC1796ED)
- Clock Generation Unit with PLL
- Core supply voltage of 1.5 V
- I/O voltage of 3.3 V
- Full automotive temperature range: -40° to +125°C

A.1.2 DSP interfacing circuits

In order to protect the DSP and electrically isolate it from the external circuits, two interfacing circuit boards are used. The first is used to isolate the ADC channels of the DSP from the transducers circuits and the second isolates the DSP's output ports from the gate drive circuits. Both interfacing circuits are shown in Figure A.4. The green board on the left is the one used to isolate the ADC channels and the one on the right is used to isolate the output ports. Their schematic diagrams are shown in Figure A.5 and Figure A.6 respectively.

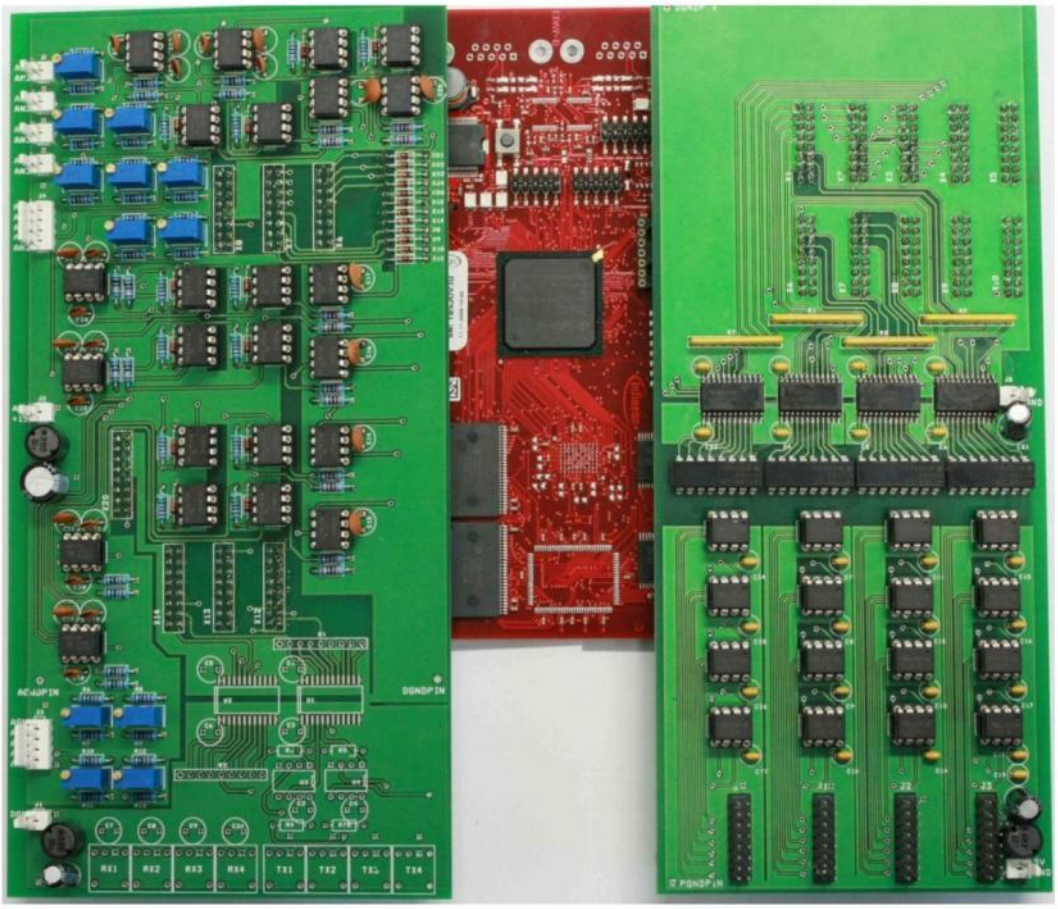


Figure A.4 DSP interfacing circuits

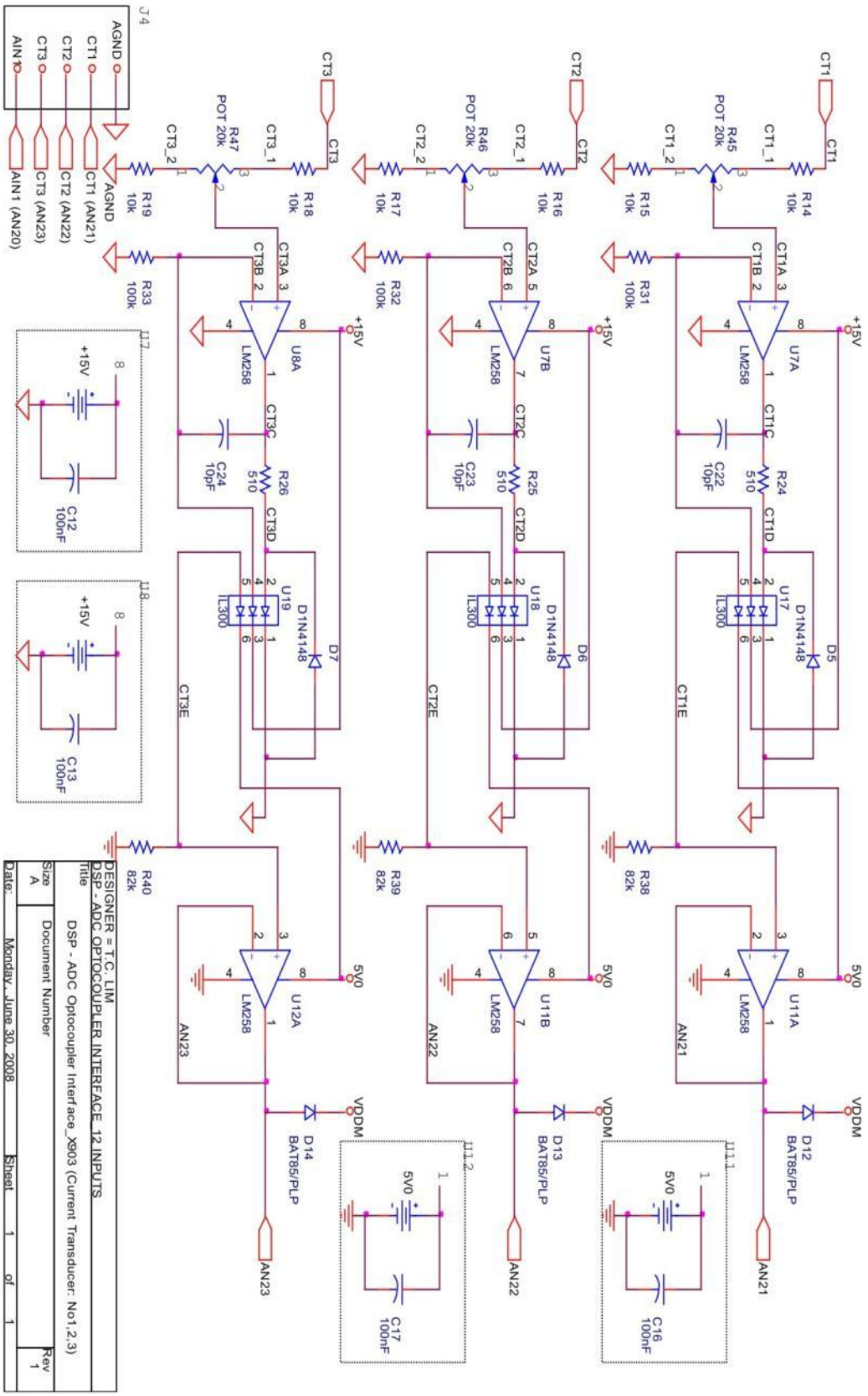
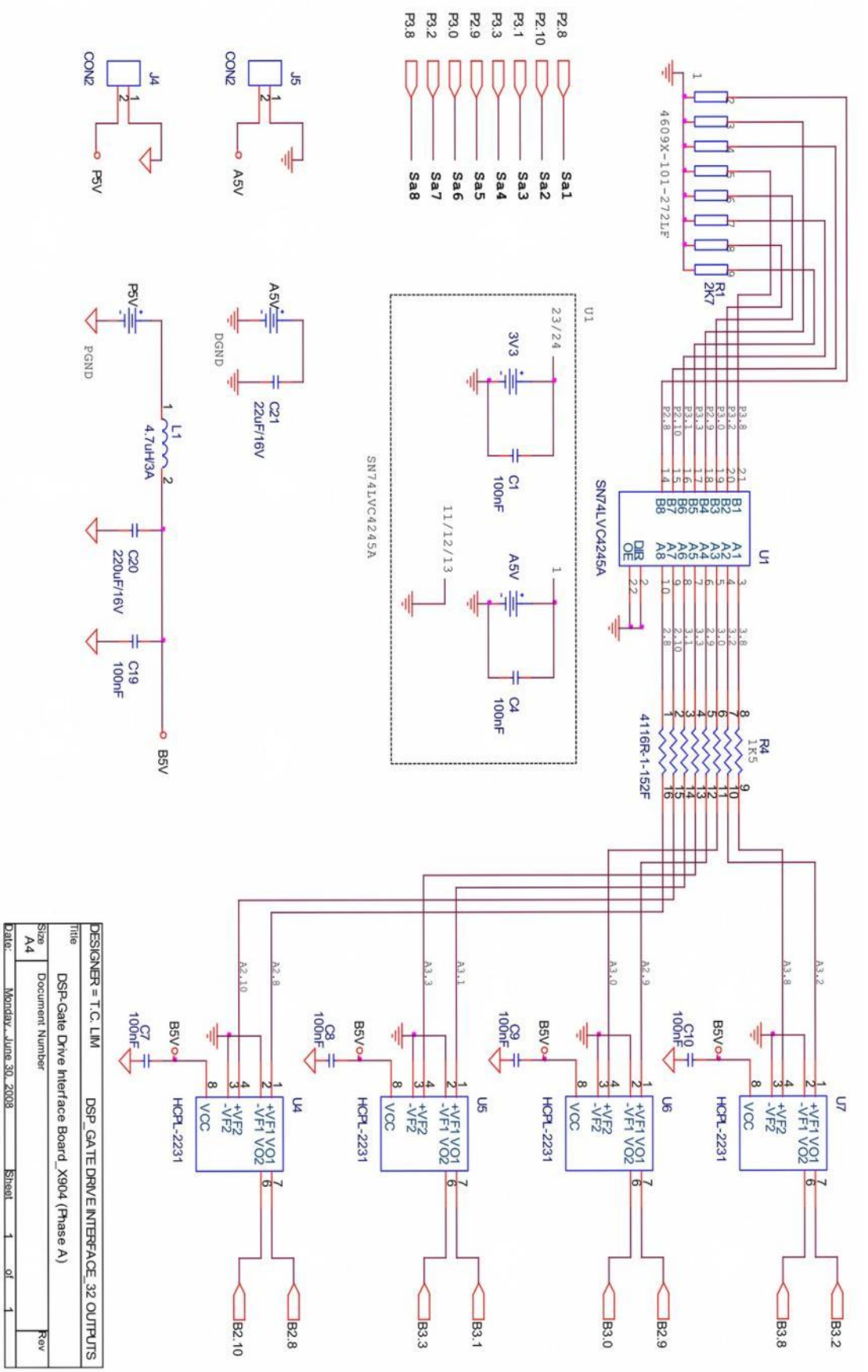


Figure A.5 DSP interfacing circuit for ADC channels


DESIGNER = T.C. LIM
DSP_GATE DRIVE INTERFACE_32 OUTPUTS
Title
DSP-Gate Drive Interface Board_X904 (Phase A)
Size
A4
Document Number
Rev
Date:
Monday, June 30, 2008
Sheet
1
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1
SN74LVC4245A
4609X-101-272LF
4116R-1-152F
HCPL-2231
P2.8
P2.10
P3.1
P3.3
P3.2
P3.0
P2.9
P3.8
Sa1
Sa2
Sa3
Sa4
Sa5
Sa6
Sa7
Sa8
B2.8
B2.10
B3.1
B3.3
B2.9
B3.0
B3.2
B3.8
B5V
A5V
3V3
P5V
PGND
DGND
CON2
4.7uH3A
22uF/16V
220uF/16V
100nF

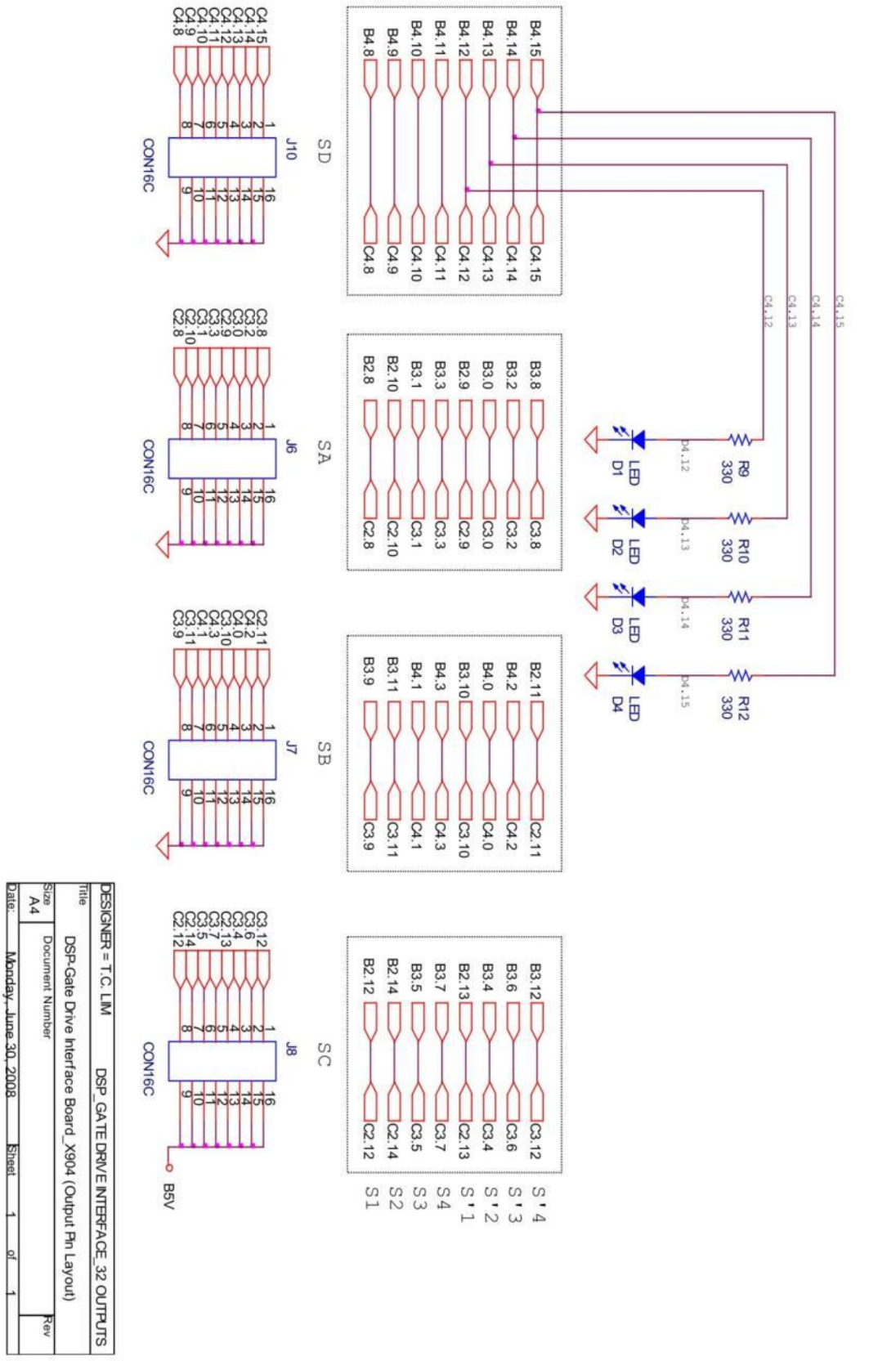


Figure A.6 DSP interfacing circuit for output ports

A.1.3 DC power supply

To supply the required dc voltage to the dc terminal of inverter, high voltage dc power supply is used for each inverter. The power supplies used are listed below and their photograph is shown in Figure A.7.

- Inverter 1 – XANTREX XFR
    - Max voltage : 300 V
    - Max current : 9 A
    - Max power : 2.7 kW
- Inverter 2 – ARGANTIX KDC
    - Max voltage : 600 V
    - Max current : 25 A
    - Max power : 15 kW
- Inverter 3 – ARGANTIX XDS
    - Rated voltage : 600 V
    - Rated current : 25 A

Figure A.7 Dc power supplies

A.1.4 IGBT Module

Infineon BSM100GD120DN2 IGBT power module is used for each inverter set. There are 6 IGBT switches packed in this module. It includes fast free-wheel diodes connected across each switch. The IGBT module datasheet and photo are shown in Figure A.8 and Figure A.9 respectively.

BSM 100 GD 120 DN2 eupec

Maximum Ratings

Parameter	Symbol	Values	Unit
Collector-emitter voltage	V_{CE}	1200	V
Collector-gate voltage R_{GE} = 20 kΩ	V_{CGR}	1200	
Gate-emitter voltage	V_{GE}	± 20	
DC collector current T_C = 25 °C T_C = 80 °C	I_C	 150 100	A
Pulsed collector current, t_p = 1 ms T_C = 25 °C T_C = 80 °C	I_{Cpuls}	 300 200	
Power dissipation per IGBT T_C = 25 °C	P_{tot}	 680	W
Chip temperature	T_j	+ 150	°C
Storage temperature	T_{stg}	-40 ... + 125	
Thermal resistance, chip case	R_{thJC}	≤ 0.182	K/W
Diode thermal resistance, chip case	R_{thJCD}	≤ 0.36	
Insulation test voltage, t = 1min.	V_{is}	2500	Vac
Creepage distance	-	16	mm
Clearance	-	11	
DIN humidity category, DIN 40 040	-	F	sec
IEC climatic category, DIN IEC 68-1	-	40 / 125 / 56	

Switching Characteristics, Inductive Load at T_j = 125 °C

Turn-on delay time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 100 A R_{Gon} = 6.8 Ω	$t_{d(on)}$	 -	 160	 320	ns
Rise time V_{CC} = 600 V, V_{GE} = 15 V, I_C = 100 A R_{Gon} = 6.8 Ω	t_r	 -	 80	 160	
Turn-off delay time V_{CC} = 600 V, V_{GE} = -15 V, I_C = 100 A R_{Goff} = 6.8 Ω	$t_{d(off)}$	 -	 400	 520	
Fall time V_{CC} = 600 V, V_{GE} = -15 V, I_C = 100 A R_{Goff} = 6.8 Ω	t_f	 -	 70	 100	

Free-Wheel Diode

Diode forward voltage I_F = 100 A, V_{GE} = 0 V, T_j = 25 °C I_F = 100 A, V_{GE} = 0 V, T_j = 125 °C	V_F	 - -	 2.3 1.8	 2.8 -	V
Reverse recovery time I_F = 100 A, V_R = -600 V, V_{GE} = 0 V di_F/dt = -800 A/µs, T_j = 125 °C	t_{rr}	 -	 0.3	 -	µs
Reverse recovery charge I_F = 100 A, V_R = -600 V, V_{GE} = 0 V di_F/dt = -800 A/µs T_j = 25 °C T_j = 125 °C	Q_{rr}	 - -	 4 11	 - -	µC

Figure A.8 Infineon BSM100GD120DN2 datasheet

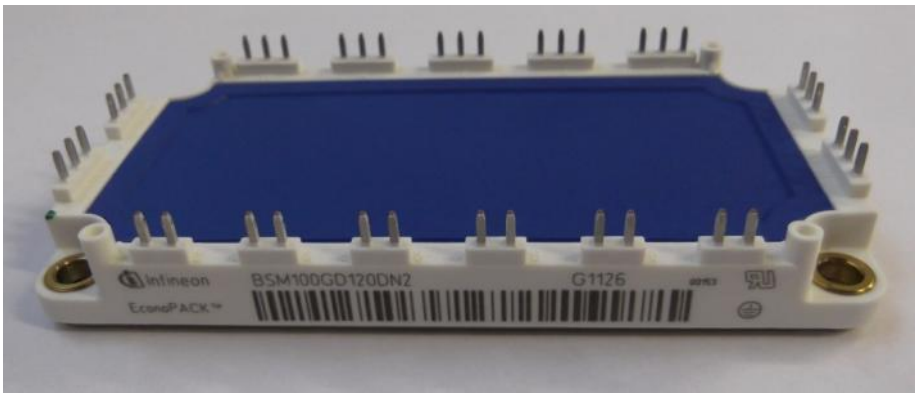


Figure A.9 Infineon BSM100GD120DN2 photo

A.1.5 DC link capacitors

To ensure a stable DC link voltage, 600V/2200μF electrolytic, high ripple current capacitors from Panasonic is used for each inverter set. This capacitor is shown in Figure A.10.

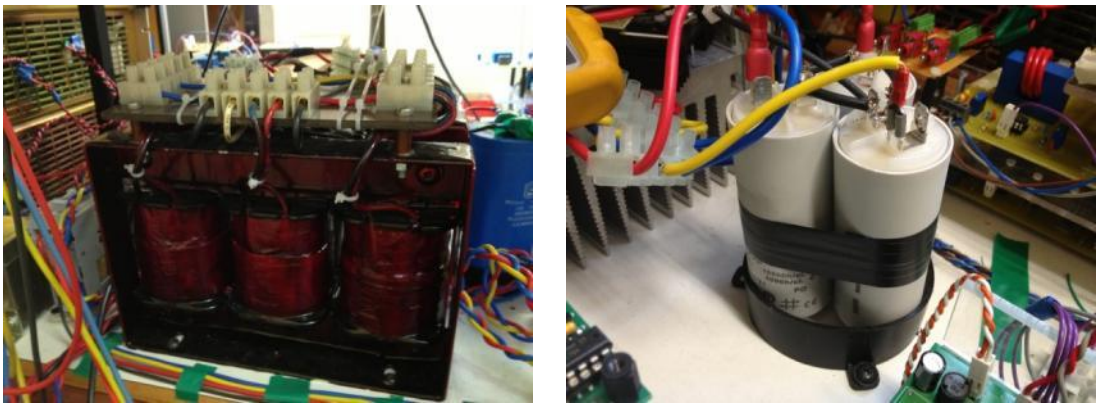
A.1.6 LC filter

To filter the output voltage of the inverter, a three-phase inductor and three single phase capacitors are used. The inductors have values of 2.0 mH and a 20 A current rating. This allows current ripple through the inductor within the standard specific limits. High frequency ac capacitors of 30 μF are used with a 440 V ac rated voltage. The LC-filter used is shown in Figure A.11 parts (a) and (b).

A.1.7 Gate drive circuit

The function of gate drive circuit is to supply sufficient gate drive voltage and current for the semiconductor switching devices. Isolation between the DSP common ground and the inverter switches common point is implemented using optocouplers. Figure A.12 shows the gate drive circuit photo and Figure A.13 shows the circuit schematic.

Figure A.10 DC link capacitor



(a) (b)

Figure A.11 LC filter: (a) Three-phase inductor and (b) three single phase capacitors

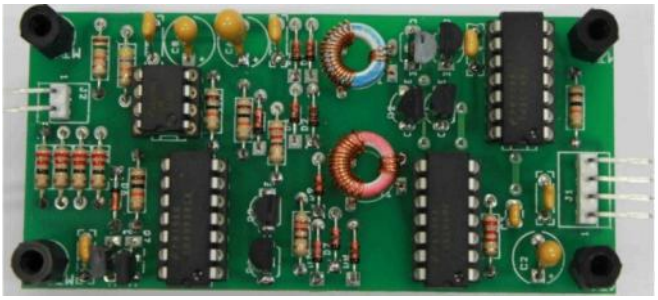


Figure A.12 Gate drive circuit photo

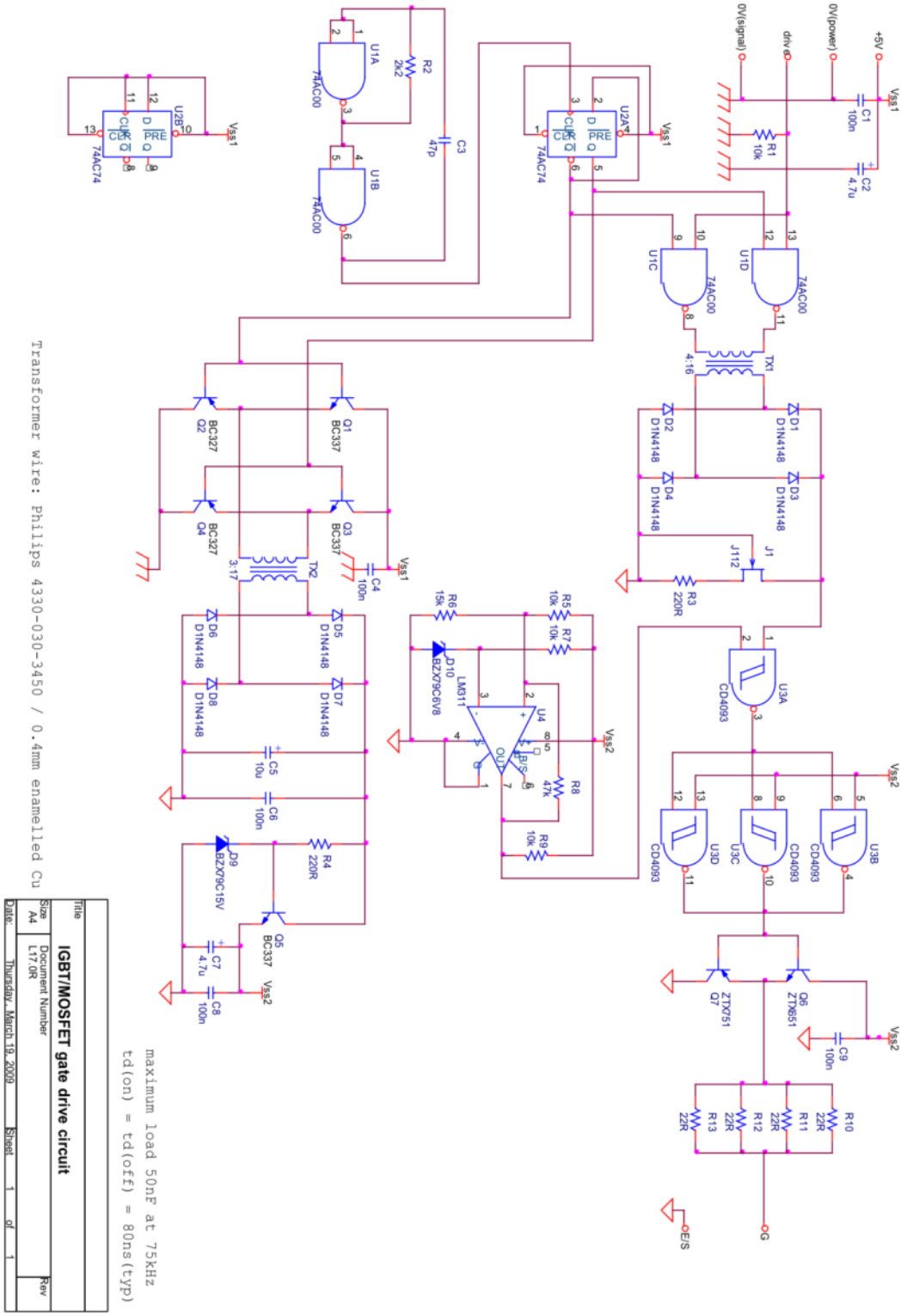


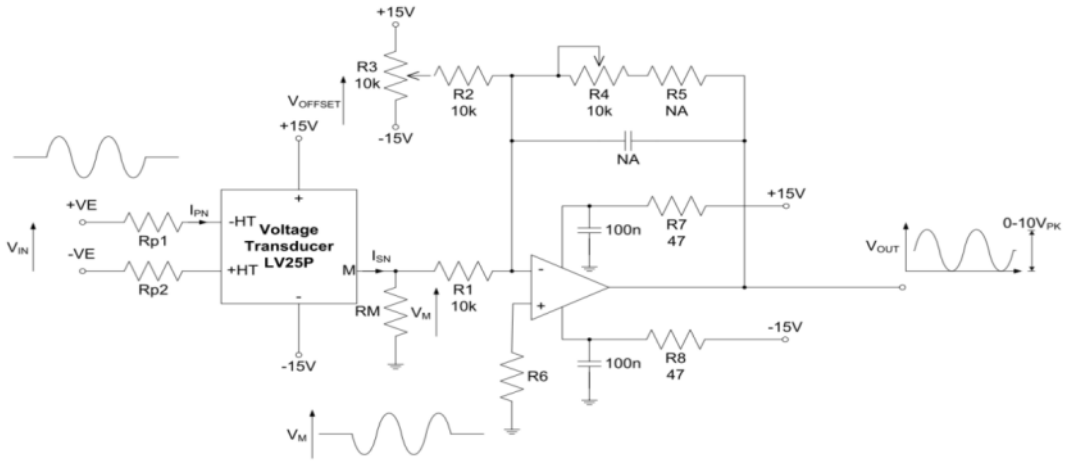
Figure A.13 Gate drive circuit schematic

A.1.8 Voltage and current sensing circuit

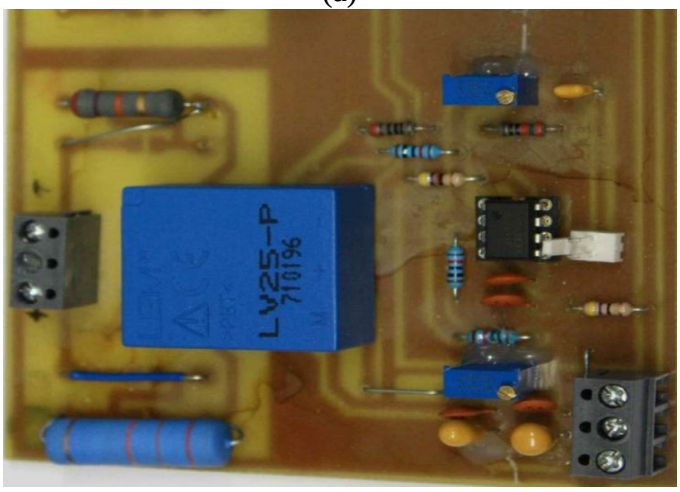
In the hardware implementation, voltage and current measurements are required as feedback signals for the controller. Voltage and current sensing circuits are used.

a) Voltage sensing circuit

The schematic and photo of the voltage sensing circuit are shown in Figure A.14 parts (a) and (b) respectively. LEM LV25-P voltage transducer is used in the voltage sensing circuit. It uses the Hall-effect to measure ac and dc voltages and has a galvanic isolation between the primary (high voltage) and the secondary circuit (electronic circuit). The datasheet for this voltage transducer is shown in Figure A.15. In order to get an appropriate voltage to feed the DSP, a signal conditioning circuit is incorporated in the voltage sensing circuit.



(a)



(b)

Figure A.14 Voltage sensing circuit : (a) Schematic and (b) photo

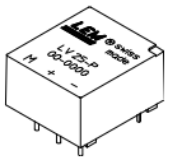
LEM

Voltage Transducer LV 25-P

I_{PN} = 10 mA
V_{PN} = 10..500 V

For the electronic measurement of voltages : DC, AC, pulsed..., with a galvanic isolation between the primary circuit (high voltage) and the secondary circuit (electronic circuit).

16084



Electrical data

I_{PN}	Primary nominal current rms		10		mA
I_{PM}	Primary current, measuring range		0 .. ± 14		mA
R_M	Measuring resistance		$R_{M\,min}$	$R_{M\,max}$	
	with ± 12 V	@ ± 10 mA $_{max}$	30	190	Ω
		@ ± 14 mA $_{max}$	30	100	Ω
	with ± 15 V	@ ± 10 mA $_{max}$	100	350	Ω
		@ ± 14 mA $_{max}$	100	190	Ω
I_{SN}	Secondary nominal current rms		25		mA
K_N	Conversion ratio		2500 : 1000		
V_C	Supply voltage (± 5 %)		± 12 .. 15		V
I_C	Current consumption		10 (@ ± 15 V) + I_S		mA

Accuracy - Dynamic performance data

X_G	Overall Accuracy @ I_{PN}, T_A = 25°C	@ ± 12 .. 15 V	± 0.9		%
		@ ± 15 V (± 5 %)	± 0.8		%
ε_L	Linearity error		< 0.2		%
			Typ	Max	
I_O	Offset current @ I_P = 0, T_A = 25°C			± 0.15	mA
I_{OT}	Temperature variation of I_O	0°C .. + 25°C	± 0.06	± 0.25	mA
		+ 25°C .. + 70°C	± 0.10	± 0.35	mA
t_r	Response time [1] to 90 % of I_{PN} step		40		µs

General data

T_A	Ambient operating temperature	0 .. + 70	°C
T_S	Ambient storage temperature	- 25 .. + 85	°C
R_P	Primary coil resistance @ T_A = 70°C	250	Ω
R_S	Secondary coil resistance @ T_A = 70°C	110	Ω
m	Mass	22	g
	Standards	EN 50178: 1997	

Note: [1] R_1 = 25 kΩ (L/R constant, produced by the resistance and inductance of the primary circuit).

Features

- Closed loop (compensated) voltage transducer using the Hall effect
- Isolated plastic case recognized according to UL 94-V0.

Principle of use

- For voltage measurements, a current proportional to the measured voltage must be passed through an external resistor R_1 which is selected by the user and installed in series with the primary circuit of the transducer.

Advantages

- Excellent accuracy
- Very good linearity
- Low thermal drift
- Low response time
- High bandwidth
- High immunity to external interference
- Low disturbance in common mode.

Applications

- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Power supplies for welding applications.

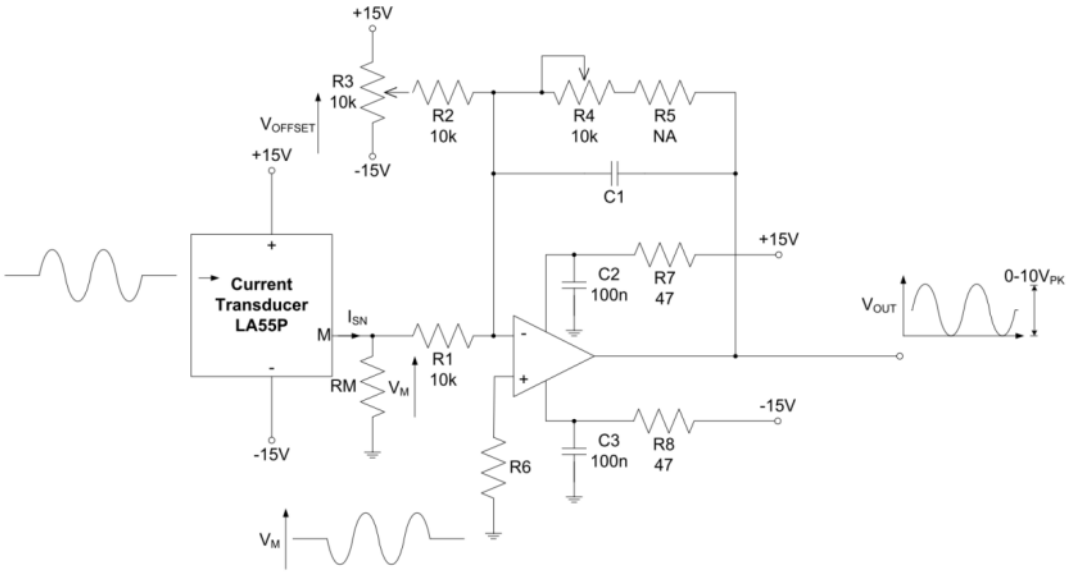
Application domain

- Industrial.

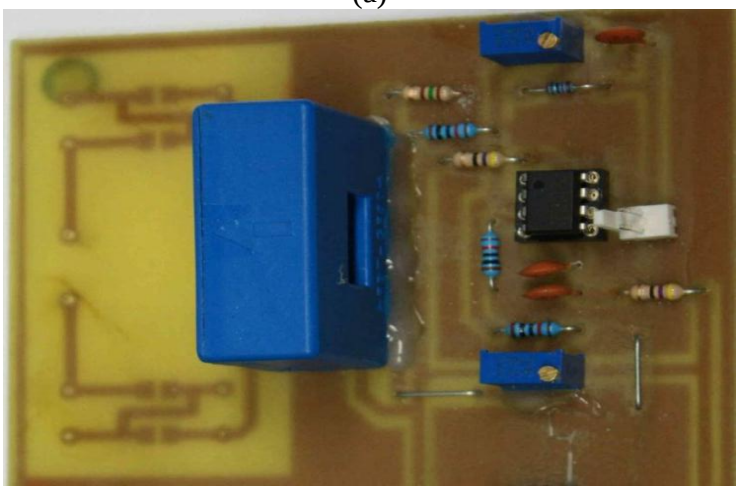
Figure A.15 LEM LV 25-P voltage transducer datasheet

b) Current sensing circuit

Figure A.16 parts (a) and (b) show the schematic and photo of the current sensing circuit. In this circuit, LEM LA 55-P current transducer is used to electronically measure the ac and dc currents. Figure A.17 shows the datasheet of this current transducer. Like the voltage sensing circuit, a signal conditioning circuit is incorporated in the circuit sensing circuit to ensure an appropriate voltage is fed to the DSP.



(a)



(b)

Figure A.16 Current sensing circuit : (a) Schematic and (b) photo

Current Transducer LA 55-P

I_{PN} = 50 A

For the electronic measurement of currents : DC, AC, pulsed..., with a galvanic isolation between the primary circuit (high power) and the secondary circuit (electronic circuit).

Electrical data

				T_A = 70°C		T_A = 85°C		
				$R_{M\,min}$	$R_{M\,max}$	$R_{M\,min}$	$R_{M\,max}$	
I_{PN}	Primary nominal r.m.s. current			50				A
I_P	Primary current, measuring range			0 .. ± 70				A
R_M	Measuring resistance @							
	with ± 12 V	@ ± 50 A_{max}		10	100	60	95	Ω
		@ ± 70 A_{max}		10	50	60 [1]	60 [1]	Ω
	with ± 15 V	@ ± 50 A_{max}		50	160	135	155	Ω
		@ ± 70 A_{max}		50	90	135 [2]	135 [2]	Ω
I_{SN}	Secondary nominal r.m.s. current			50				mA
K_N	Conversion ratio			1 : 1000				
V_C	Supply voltage (± 5 %)			± 12 .. 15				V
I_C	Current consumption			10 (@ ± 15 V) + I_S				mA
V_d	R.m.s. voltage for AC isolation test, 50 Hz, 1 mn			2.5				kV

Accuracy - Dynamic performance data

				Typ	Max	
X	Accuracy @ I_{PN}, T_A = 25°C	@ ± 15 V (± 5 %)			± 0.65	%
		@ ± 12 .. 15 V (± 5 %)			± 0.90	%
ε_L	Linearity				< 0.15	%
I_O	Offset current @ I_P = 0, T_A = 25°C				± 0.2	mA
I_{OM}	Residual current [3] @ I_P = 0, after an overload of 3 x I_{PN}				± 0.3	mA
I_{OT}	Thermal drift of I_O	0°C .. + 70°C		± 0.1	± 0.5	mA
		- 25°C .. + 85°C		± 0.1	± 0.6	mA
t_{ra}	Reaction time @ 10 % of $I_{P\,max}$				< 500	ns
t_r	Response time @ 90 % of $I_{P\,max}$				< 1	µs
di/dt	di/dt accurately followed				> 200	A/µs
f	Frequency bandwidth (- 1 dB)				DC .. 200	kHz

General data

T_A	Ambient operating temperature		- 25 .. + 85	°C
T_S	Ambient storage temperature		- 40 .. + 90	°C
R_S	Secondary coil resistance @	T_A = 70°C	80	Ω
		T_A = 85°C	85	Ω
m	Mass		18	g
	Standards [4]		EN 50178	

Notes : [1] Measuring range limited to ± 60 A_{max}
[2] Measuring range limited to ± 55 A_{max}
[3] Result of the coercive field of the magnetic circuit
[4] A list of corresponding tests is available

Features

- Closed loop (compensated) current transducer using the Hall effect
- Printed circuit board mounting
- Insulated plastic case recognized according to UL 94-V0.

Advantages

- Excellent accuracy
- Very good linearity
- Low temperature drift
- Optimized response time
- Wide frequency bandwidth
- No insertion losses
- High immunity to external interference
- Current overload capability.

Applications

- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Switched Mode Power Supplies (SMPS)
- Power supplies for welding applications.

980706/8

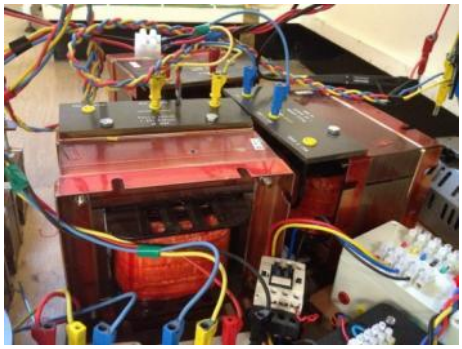
LEM Components www.lem.com

Figure A.17 LEM LA 55-P current transducer datasheet

A.1.9 Interfacing inductor

In order to avoid large inrush current during inverter synchronization to the ac bus and during transient, interfacing inductor is used for each inverter. Three single phase inductor are used for each inverter. The interface inductor used for inverter 1, 2 and 3 are listed below and they are shown in Figure A.18 below.

- Inverter 1 interfacing inductor (L_{int1}) – 5 mH
- Inverter 2 interfacing inductor (L_{int2}) – 3.75 mH
- Inverter 3 interfacing inductor (L_{int3}) – 6.2 mH



(a)

(b)

(c)

Figure A.18 Interfacing inductor : (a) L_{int1},(b) L_{int2} and (c) L_{int3}

A.2 Line impedances

Wire coils shown in Figure A.19 are used to represent the line impedances. Each coil has resistance and reactance value around 0.3 Ω and 0.063 Ω respectively.

Figure A.19 Wire coils to represent line impedance

A.3 Loads

In order to test the effectiveness of the proposed controller, the DG prototype needs to be tested with linear and nonlinear loads.

A.3.1 Linear loads

Balanced linear load in the laboratory is designed by using several resistor banks with various resistance values. They are shown in Figure A.20. All loads can be step changed to provide transient testing by using a contactor.

A.3.2 Nonlinear load

Balanced nonlinear load is made of a three-phase rectifier bridge, and load resistor, as shown in Figure A.21

(a)

(b)

Figure A.20 Linear load

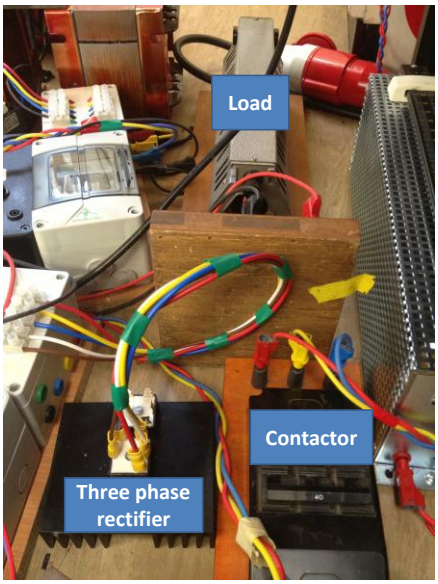


Figure A.21 Nonlinear load

A.4 Measuring instruments

For hardware implementation, digital oscilloscopes are used for signal visualization. In order to get the appropriate signals to feed the oscilloscope, current and voltage probes are used. For power quality measurement, three phase power analyzer is used.

A.4.1 Digital storage oscilloscope (DSO)

DSO is a type of electronic test instrument that allows observation of constantly varying signal voltages, usually as a two-dimensional graph of one or more electrical potential differences using the vertical or y-axis, plotted as a function of time (horizontal or x-axis). Many signals can be converted to voltages and displayed this way. Signals are often periodic and repeat constantly so that multiple samples of a signal which is actually varying with time are displayed as a steady picture. Many oscilloscopes (storage oscilloscopes) can also capture non-repeating waveforms for a specified time and show a steady display of the captured segment. The following two DSOs are used in the test rig. Their pictures are shown in Figure A.22.

a) Tektronix TDS 2024

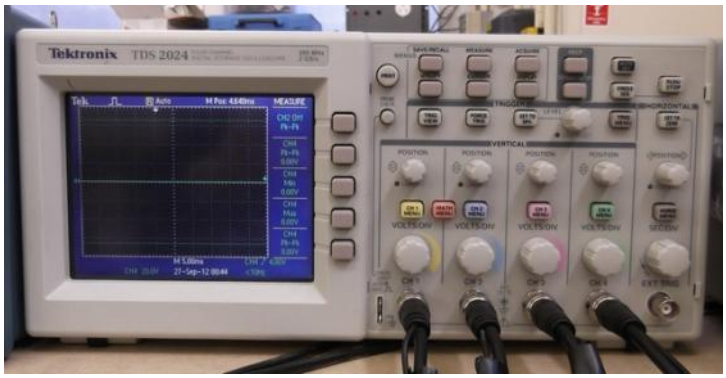
This is a DSO manufactured by Tektronix and has the following features:

- Channel : 4 channels
- Bandwidth : 200 MHz
- Sample rate : 2.0 GS/s
- Display : colour

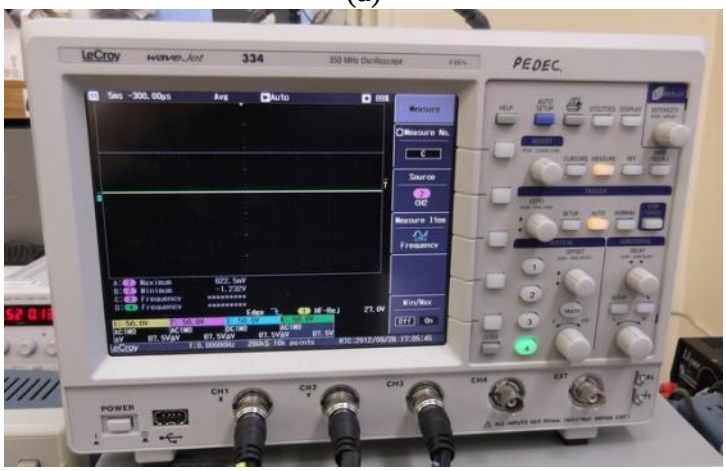
b) Le CroyWavejet 334

This Le Croy oscilloscope has the following features:

- Channel : 4 channels
- Bandwidth : 350 MHz
- Sample rate : 2.0 GS/s
- Display : colour



(a)



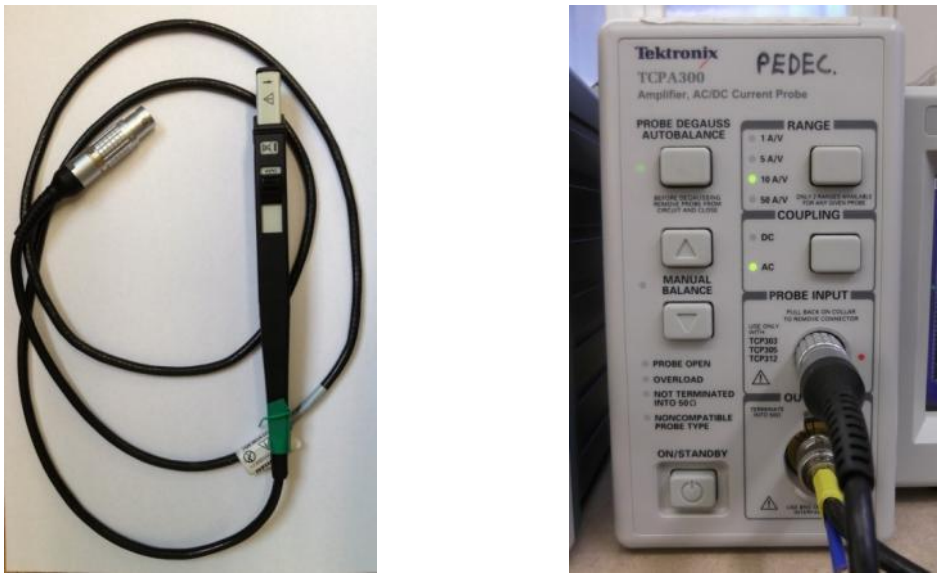
(b)

Figure A.22 Digital storage oscilloscope:
(a) Tektronix TDS 2024 and (b) Le CroyWavejet 334

A.4.2 Current probe

Tektronix TCP305A current probe together with TCPA300 amplifier shown in Figure A.23 are used for current measurement. Some of the features of this AC/DC current measurement system are listed below:

- Bandwidth : DC – 50 MHz signal
- Max DC current : 50 A
- Max RMS current : 35.4 A
- Automatic scaling
- AC/DC input coupling
- Split-core construction allows easy circuit connection



(a) (b)

Figure A.23 Tektronix AC/DC current measurement system:
(a) TCP305A current probe and (b) TCPA300 amplifier

A.4.3 Voltage probe

Voltage probe extends the measurement capability of oscilloscopes to display and measure in-circuit waveforms that are referenced to high common mode voltages. TESTEC TT-SI 9001 differential probe (shown in Figure A.24) is used for voltage measurement. Differential probes are like two probes in one. Instead of measuring a test point in relation to a ground point (like single-ended active probes), differential probes measure the difference in voltage of a test point in relation to another test point. This voltage probe has the following specification:

- Bandwidth: DC to 25MHz
- Attenuation Ratio: 1:10 / 1:100
- Accuracy: +/-2%
- Rise Time: 14ns
- Input Impedance: 4MΩ // 5,5pF each side to ground

A.4.4 Three phase power analyzer

For real time power measurement (including power quality measurement), Voltech PM300 three phase power analyzer is used. The equipment is shown in Figure A.25. Some of its features are as follows:

- Measure Watts, Volts, Amps, VA, VAr, PF, cos phi, Vrms, Vpeak, voltage crest factor, Arms, A peak, Amps crest factor, frequency
- THD, voltage, current and power harmonics
- Programmable for watt-hour, ampere-hour and other integrator measurements
- Available with IEEE488 or RS323 communications interfaces installed

Figure A.24 TESTEC TT – SI 9001 differential probe

Figure A.25 PM300 three phase power analyzer

A.5 Simulation and experimental software

Simulation software is used in this thesis to test the designed controllers and algorithms before the hardware implementation. MATLAB/SIMULINK is used for all simulations. In hardware implementation, Digital Application Virtual Engineering (DAVE) and TASKING TriCore VX are used.

A.5.1 MATLAB/SIMULINK

MATLAB® is a high-level language and interactive environment for numerical computation, visualization, and programming developed by MathWorks. MATLAB allows matrix manipulations, plotting of functions and data, implementation of algorithms, creation of user interfaces, and interfacing with programs written in other languages, including C, C++, Java, and FORTRAN. SIMULINK on the other hand is an additional package for MATLAB. It is a data flow graphical programming language tool for modelling, simulating and analyzing multi-domain dynamic systems. Its primary interface is a graphical block diagramming tool and a customizable set of block libraries. It offers tight integration with the rest of the MATLAB environment and can either drive MATLAB or be scripted from it. Simulink is widely used in control theory and digital signal processing for multi-domain simulation and Model-Based Design.The following MATLAB and SIMULINK versions are used for simulations in this thesis.

- MATLAB R2011b (version 7.13.0.564) (64 bit)
- SIMULINK (version 7.8)

A.5.2 DAVE

DAVE (version 2) software is low level code generation software developed by Infineon Technologies to support their microcontroller application. This software provides intelligent wizards, which help users to configure the chip to work the way they need it and automatically generate C-code with appropriate driver functions for all of the on-chip peripherals and interrupt controls. The generated code can be automatically imported in compiler tools from Altium, HighTec, Keil and DAVE™ Bench.

A.5.3 TASKING TriCore VX

TASKING TriCore VX is a development toolset developed by Altium that support the TriCore architecture from Infineon Technologies. TASKING (version 2.2 r3) used for this thesis consists of dedicated C/C++ compilers and assemblers, a multi-core linker/locator and debugger. Using this software, the proposed control is coded in C language, compiled and uploaded to the TriCore microcontroller through USB cable.

Appendix B

Equation Derivations for Chapter 4

B.1 Parallel multi inverter system

An inverter with the instantaneous average current sharing scheme is modelled in Figure B.1. This model has two inputs which are input voltage (v_i^*) and output current (i_o) and one output which is the output voltage of the inverter (v_o). L_f, C_f and R_f represent the filter inductance, capacitance and resistance respectively. G_v represents the PR voltage controller of the voltage feedback loop, K_f is the gain of the voltage feed-forward loop, and K_c is the gain of the current feedback loop. In this model it is assumed that the inverter has unity gain. That is, the modulation index of the SPWM modulator is assumed to be 1. The equation for G_v is given by (B.1).

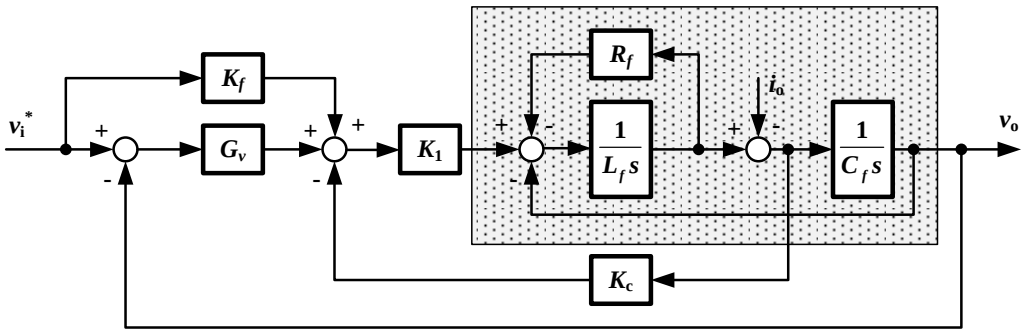


Figure B.1 Inverter model with instantaneous current sharing scheme

$$G_v = \frac{K_P s^2 + (2K_P w_c + K_{Res})s + K_P(w_c^2 + w_o^2) + K_{Res} w_c}{s^2 + 2w_c s + w_c^2 + w_o^2} \quad \text{(B.1)}$$

B.1.1 Closed loop voltage gain (*G*)

The closed-loop voltage gain G can be derived from Figure B.1 by setting i_o to be 0 and the model can be simplified to:

$$G = \frac{K_1(G_v + K_f)}{C_f L_f s^2 + \left(C_f R_f + C_f K_c\right)s + K_1 G_v + 1} \tag{B.2}$$

By replacing G_v in (B.2) with (B.1) the following full derivation can be obtained and closed loop voltage gain becomes (B.3)

$$G = \frac{K_1\left(\frac{K_P s^2 + (2K_P w_c + K_{\text{Res}})s + K_P(w_c{}^2 + w_o{}^2) + K_{\text{Res}} w_c}{s^2 + 2w_c s + w_c{}^2 + w_o{}^2} + K_f\right)}{C_f L_f s^2 + \left(C_f R_f + C_f K_c\right)s} + K_1\left(\frac{K_P s^2 + (2K_P w_c + K_{\text{Res}})s + K_P(w_c{}^2 + w_o{}^2) + K_{\text{Res}} w_c}{s^2 + 2w_c s + w_c{}^2 + w_o{}^2}\right) + 1$$

$$G = \frac{K_1\left[\begin{array}{c}\frac{K_P s^2 + (2K_P w_c + K_{\text{Res}})s + K_P(w_c{}^2 + w_o{}^2) + K_{\text{Res}} w_c}{s^2 + 2w_c s + w_c{}^2 + w_o{}^2} \\ + \frac{K_f\left(s^2 + 2w_c s + w_c{}^2 + w_o{}^2\right)}{s^2 + 2w_c s + w_c{}^2 + w_o{}^2}\end{array}\right]}{\frac{\left(C_f L_f s^2 + \left(C_f R_f + C_f K_c\right)s\right)\left(s^2 + 2w_c s + w_c{}^2 + w_o{}^2\right)}{s^2 + 2w_c s + w_c{}^2 + w_o{}^2} + K_1\left(\frac{K_P s^2 + (2K_P w_c + K_{\text{Res}})s + K_P(w_c{}^2 + w_o{}^2) + K_{\text{Res}} w_c}{s^2 + 2w_c s + w_c{}^2 + w_o{}^2}\right) + \frac{s^2 + 2w_c s + w_c{}^2 + w_o{}^2}{s^2 + 2w_c s + w_c{}^2 + w_o{}^2}}$$

$$G = \frac{K_1\left[\begin{array}{l}K_P s^2 + (2K_P w_c + K_{\text{Res}})s + K_P(w_c{}^2 + w_o{}^2) \\ + K_{\text{Res}} w_c + K_f s^2 + 2K_f w_c s + K_f\left(w_c{}^2 + w_o{}^2\right)\end{array}\right]}{\begin{array}{c}C_f L_f s^4 + 2w_c C_f L_f s^3 + C_f L_f\left(w_c{}^2 + w_o{}^2\right)s^2 + \left(C_f R_f + C_f K_c\right)s^3 \\ + 2w_c\left(C_f R_f + C_f K_c\right)s^2 + \left(C_f R_f + C_f K_c\right)\left(w_c{}^2 + w_o{}^2\right)s \\ + K_1\left[K_P s^2 + (2K_P w_c + K_{\text{Res}})s + K_P(w_c{}^2 + w_o{}^2) + K_{\text{Res}} w_c\right] + s^2 + 2w_c s + w_c{}^2 + w_o{}^2\end{array}}$$

$$G = \frac{\begin{array}{c} K_1\left(K_P + K_f\right)s^2 + K_1(2K_P w_c + K_{\text{Res}} + 2K_f w_c)s \\ +K_1\left[K_P(w_c{}^2 + w_o{}^2) + K_f\left(w_c{}^2 + w_o{}^2\right) + K_{\text{Res}} w_c\right] \end{array}}{\begin{array}{c} C_f L_f s^4 + \left(2w_c C_f L_f + C_f R_f + C_f K_c\right)s^3 \\ +\left[C_f L_f\left(w_c{}^2 + w_o{}^2\right) + 2w_c\left(C_f R_f + C_f K_c\right) + K_1 K_P + 1\right]s^2 \\ +\left[\left(C_f R_f + C_f K_c\right)\left(w_c{}^2 + w_o{}^2\right) + 2K_1 K_P w_c + K_1 K_{\text{Res}} + 2w_c\right]s \\ +K_1 K_P(w_c{}^2 + w_o{}^2) + K_1 K_{\text{Res}} w_c + w_c{}^2 + w_o{}^2 \end{array}}$$

$$G = \frac{g_{n2}s^2 + g_{n1}s + g_{n0}}{g_{d4}s^4 + g_{d3}s^3 + g_{d2}s^2 + g_{d1}s + g_{d0}} \tag{B.3}$$

$$\begin{aligned}
g_{n2} &= K_1(K_P + K_f) \\
g_{n1} &= K_1(2K_P w_c + K_{\text{Res}} + 2K_f w_c) \\
g_{n0} &= K_1\left(K_P(w_c{}^2 + w_o{}^2) + K_f(w_c{}^2 + w_o{}^2) + K_{\text{Res}} w_c\right) \\
g_{d4} &= C_f L_f \\
g_{d3} &= 2w_c C_f L_f + C_f R_f + C_f K_c \\
g_{d2} &= C_f L_f(w_c{}^2 + w_o{}^2) + 2w_c(C_f R_f + C_f K_c) + K_1 K_P + 1 \\
g_{d1} &= (C_f R_f + C_f K_c)(w_c{}^2 + w_o{}^2) + 2K_1 K_P w_c + K_1 K_{\text{Res}} + 2w_c \\
g_{d0} &= K_1 K_P(w_c{}^2 + w_o{}^2) + K_1 K_{\text{Res}} w_c + w_c{}^2 + w_o{}^2
\end{aligned}$$

B.1.2 Output Impedance (*Z*)

By setting $v_i{}^*$ to 0, the model in Figure B.1 can be simplified to (B.4), to find the output impedance of the inverter.

$$Z = \frac{L_f s + R_f}{C_f L_f s^2 + \left(C_f R_f + K_1 K_c C_f\right)s + K_1 G_v + 1} \tag{B.4}$$

By replacing G_v in (B.4) with (B.1) the following full derivation can be obtained and output impedance becomes (B.5)

$$Z = \frac{L_f s + R_f}{\begin{array}{c} C_f L_f s^2 + \left(C_f R_f + K_1 K_c C_f\right)s \\ +K_1\left[\dfrac{K_P s^2 + (2K_P w_c + K_{\text{Res}})s + K_P(w_c{}^2 + w_o{}^2) + K_{\text{Res}} w_c}{s^2 + 2w_c s + w_c{}^2 + w_o{}^2}\right] + 1 \end{array}}$$

$$Z=\frac{\begin{array}{c}L_f s+R_f\end{array}}{\begin{array}{c}C_f L_f s^2\left(s^2+2w_c s+w_c{}^2+w_o{}^2\right)+\left(C_f R_f+K_1K_cC_f\right)s\left(s^2+2w_c s+w_c{}^2+w_o{}^2\right)\\+\left[K_1K_P s^2+K_1(2K_P w_c+K_{\text{Res}})s+K_1K_P(w_c{}^2+w_o{}^2)+K_1K_{\text{Res}}w_c\right]\\+s^2+2w_c s+w_c{}^2+w_o{}^2\end{array}}$$

$$Z=\frac{\begin{array}{c}\left(L_f s+R_f\right)\left(s^2+2w_c s+w_c{}^2+w_o{}^2\right)\end{array}}{\begin{array}{c}C_f L_f s^2\left(s^2+2w_c s+w_c{}^2+w_o{}^2\right)+\left(C_f R_f+K_1K_cC_f\right)s\left(s^2+2w_c s+w_c{}^2+w_o{}^2\right)\\+\left[K_1K_P s^2+K_1(2K_P w_c+K_{\text{Res}})s+K_1K_P(w_c{}^2+w_o{}^2)+K_1K_{\text{Res}}w_c\right]\\+s^2+2w_c s+w_c{}^2+w_o{}^2\end{array}}$$

$$Z=\frac{\begin{array}{c}L_f s^3+2L_f w_c s^2+L_f\left(w_c{}^2+w_o{}^2\right)s+R_f s^2+2R_f w_c s+R_f\left(w_c{}^2+w_o{}^2\right)\end{array}}{\begin{array}{c}C_f L_f s^4+2C_f L_f w_c s^3+C_f L_f\left(w_c{}^2+w_o{}^2\right)s^2+\left(C_f R_f+K_1K_cC_f\right)s^3\\+2w_c\left(C_f R_f+K_1K_cC_f\right)s^2+\left(C_f R_f+K_1K_cC_f\right)\left(w_c{}^2+w_o{}^2\right)s+K_1K_P s^2\\+K_1(2K_P w_c+K_{\text{Res}})s+K_1K_P(w_c{}^2+w_o{}^2)+K_1K_{\text{Res}}w_c+s^2+2w_c s+w_c{}^2+w_o{}^2\end{array}}$$

$$Z=\frac{\begin{array}{c}L_f s^3+\left(2L_f w_c+R_f\right)s^2+\left[L_f\left(w_c{}^2+w_o{}^2\right)+2R_f w_c\right]s+R_f\left(w_c{}^2+w_o{}^2\right)\end{array}}{\begin{array}{c}C_f L_f s^4+\left(2C_f L_f w_c+C_f R_f+K_1K_cC_f\right)s^3\\+\left[C_f L_f\left(w_c{}^2+w_o{}^2\right)+2w_c\left(C_f R_f+K_1K_cC_f\right)+K_1K_P+1\right]s^2\\+\left[\left(C_f R_f+K_1K_cC_f\right)\left(w_c{}^2+w_o{}^2\right)+K_1(2K_P w_c+K_{\text{Res}})+2w_c\right]s\\+K_1K_P(w_c{}^2+w_o{}^2)+K_1K_{\text{Res}}w_c+w_c{}^2+w_o{}^2\end{array}}$$

$$Z=\frac{z_{n3}s^3+z_{n2}s^2+z_{n1}s+z_{n0}}{z_{d4}s^4+z_{d3}s^3+z_{d2}s^2+z_{d1}s+z_{d0}} \tag{B.5}$$

$$z_{n3}=L_f\ ;\ z_{n2}=2L_f w_c+R_f\ ;\ z_{n1}=L_f(w_c{}^2+w_o{}^2)+2R_f w_c\ ;$$
$$z_{n0}=R_f(w_c{}^2+w_o{}^2)\ ;\ z_{d4}=L_f C_f$$
$$z_{d3}=2C_f L_f w_c+C_f R_f+K_1K_cC_f$$
$$z_{d2}=C_f L_f\left(w_c{}^2+w_o{}^2\right)+2w_c\left(C_f R_f+K_1K_cC_f\right)+K_1K_P+1$$
$$z_{d1}=\left(C_f R_f+K_1K_cC_f\right)\left(w_c{}^2+w_o{}^2\right)+K_1(2K_P w_c+K_{\text{Res}})+2w_c$$
$$z_{d0}=K_1K_P(w_c{}^2+w_o{}^2)+K_1K_{\text{Res}}w_c+w_c{}^2+w_o{}^2$$

B.2 Parallel system output voltage

The model of a parallel multi inverter system is shown in Figure B.2. In this model, each inverter is treated as a voltage source connected in series with line impedance. All parameter variations including the closed loop voltage gain (G_i), the output impedance of the inverter (Z_i), and line impedance (Z_{li}), are taken into consideration. In this model, the outer current loop controller, H, is also included for all the inverters. Z_L represents the load impedance and v_o is the load voltage. The reference voltage v^*_i and reference current i^* are same for all inverters.

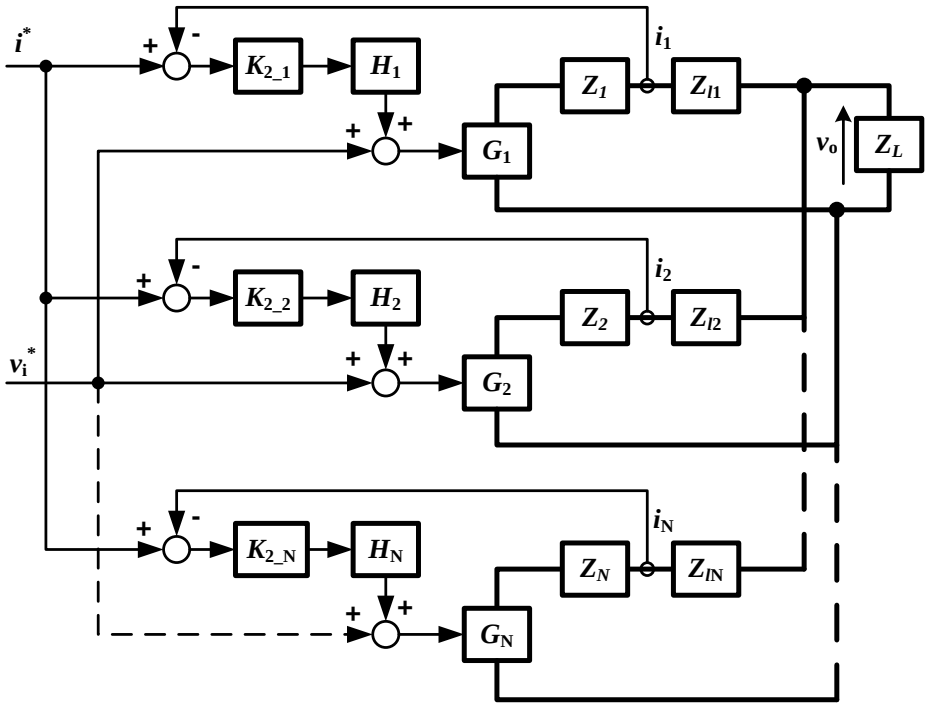


Figure B.2 The model of the parallel multi inverter system

The system is then describable as

$$v^*_{i1} = v^*_{i2} = v^*_{iN} = v^*_i \tag{B.6}$$

$$i^* = \frac{\sum_{j=1}^{N} i_j}{N} \tag{B.7}$$

$$\sum_{j=1}^{N} i_j = i_1 + i_2 + \ldots + i_N = \frac{v_o}{Z_L} \tag{B.8}$$

$$\begin{aligned} G_1\left[v^*_i+\left(i^*-i_1\right)K_{2\_1}H_1\right]-v_o &= i_1\left(Z_1+Z_{l1}\right)\\ G_2\left[v^*_i+\left(i^*-i_2\right)K_{2\_2}H_2\right]-v_o &= i_2\left(Z_2+Z_{l2}\right)\\ G_N\left[v^*_i+\left(i^*-i_N\right)K_{2\_N}H_N\right]-v_o &= i_N\left(Z_N+Z_{lN}\right) \end{aligned} \tag{B.9}$$

By combining all equations in (B.9), the following is obtained

$$\sum_{j=1}^{N}\left(G_j v^*_i+G_j K_{2\_j}H_j\left[i^*-i_j\right]\right)-Nv_o=\sum_{j=1}^{N}i_j\left(Z_j+Z_{lj}\right) \tag{B.10}$$

By substituting (B.6), (B.7) and (B.8) into (B.10) and solving for V_o , generalized output voltage equation for parallel inverter system (B.11), can be obtained

$$\sum_{j=1}^{N}\left(G_j v^*_i+G_j K_{2\_j}H_j\left(\frac{\sum_{j=1}^{N}i_j}{N}-i_j\right)\right)-Nv_o=\sum_{j=1}^{N}i_j\left(Z_j+Z_{lj}\right)$$

$$\sum_{j=1}^{N}\left(G_j v^*_i\right)+\sum_{j=1}^{N}\left(G_j K_{2\_j}H_j\left(\frac{v_o}{NZ_L}-i_j\right)\right)-Nv_o=\sum_{j=1}^{N}i_j\left(Z_j+Z_{lj}\right)$$

$$\sum_{j=1}^{N}G_j K_{2\_j}H_j\frac{v_o}{NZ_L}-\sum_{j=1}^{N}G_j K_{2\_j}H_j i_j-Nv_o=\sum_{j=1}^{N}i_j\left(Z_j+Z_{lj}\right)-\sum_{j=1}^{N}\left(G_j v^*_i\right)$$

$$v_o\left(\sum_{j=1}^{N}G_j K_{2\_j}H_j\frac{1}{NZ_L}-N\right)=\sum_{j=1}^{N}i_j\left(Z_j+Z_{lj}\right)-\sum_{j=1}^{N}\left(G_j v^*_i\right)+\sum_{j=1}^{N}G_j K_{2\_j}H_j i_j$$

$$v_o=\frac{\sum_{j=1}^{N}i_j\left(Z_j+Z_{lj}\right)-\sum_{j=1}^{N}\left(G_j v^*_i\right)+\sum_{j=1}^{N}G_j K_{2\_j}H_j i_j}{\left(\sum_{j=1}^{N}G_j K_{2\_j}H_j\frac{1}{NZ_L}-N\right)} \tag{B.11}$$

When the following are assumed, equation (B.10) can be simplified to (B.13)

$$\begin{aligned} G_1=G_2=G_N=G\\ Z_1=Z_2=Z_N=Z\\ H_1=H_2=H_N=H\\ K_{2\_1}=K_{2\_2}=K_{2\_N}=K_2 \end{aligned} \tag{B.12}$$

$$\sum_{j=1}^{N}\left(Gv^*_i + G_j K_{2\_j} H_j \left[i^* - i_j\right]\right) - Nv_o = \sum_{j=1}^{N} i_j \left(Z_j + Z_{lj}\right)$$

$$NGv^*_i + GK_2 H\left(Ni^* - \sum_{j=1}^{N} i_j\right) - Nv_o = Z\sum_{j=1}^{N} i_j + \sum_{j=1}^{N} i_j Z_{lj}$$

$$NGv^*_i + GK_2 H\left(N\frac{\sum_{j=1}^{N} i_j}{N} - \sum_{j=1}^{N} i_j\right) - Nv_o = Z\frac{v_o}{Z_L} + \sum_{j=1}^{N} i_j Z_{lj}$$

$$NGv^*_i - Nv_o = Z\frac{v_o}{Z_L} + \sum_{j=1}^{N} i_j Z_{lj}$$

$$v_o\frac{Z}{Z_L} + Nv_o = NGv^*_i - \sum_{j=1}^{N} i_j Z_{lj}$$

$$v_o\left(N + \frac{Z}{Z_L}\right) = NGv^*_i - \sum_{j=1}^{N} i_j Z_{lj}$$

$$v_o = \frac{NGv^*_i - \sum_{j=1}^{N} i_j Z_{lj}}{N + \frac{Z}{Z_L}}$$

$$v_o = \frac{Gv^*_i - \frac{1}{N}\sum_{j=1}^{N} i_j Z_{lj}}{1 + \frac{Z}{NZ_L}} \qquad \text{(B.13)}$$

B.3 Parallel system output current

From (B.9), it is known that the system equation for k^{th} inverter is given by

$$G_k\left[v^*_i+\left(i^*-i_k\right)K_{2\_k}H_k\right]-v_o=i_k\left(Z_k+Z_{lk}\right) \tag{B.14}$$

Replacing i^* and v_o in (B.14) with (B.7) and (B.11) respectively, the generalized equation for output current is derived as follows to achieve (B.15)

$$G_k\left[v^*_i+\left(\frac{\sum_{j=1}^{N}i_j}{N}-i_k\right)K_{2\_k}H_k\right]-v_o=i_k\left(Z_k+Z_{lk}\right)$$

$$NG_kv^*_i+G_kK_{2\_k}H_k\left(\sum_{\substack{j=1\\j\neq k}}^{N}i_j+i_k-Ni_k\right)-Nv_o=Ni_k\left(Z_k+Z_{lk}\right)$$

$$NG_kv^*_i+G_kK_{2\_k}H_k\sum_{\substack{j=1\\j\neq k}}^{N}i_j+G_kK_{2\_k}H_ki_k\left(1-N\right)-Nv_o=Ni_k\left(Z_k+Z_{lk}\right)$$

$$NG_kv^*_i+G_kK_{2\_k}H_k\sum_{\substack{j=1\\j\neq k}}^{N}i_j-N\left(\frac{\sum_{j=1}^{N}i_j\left(Z_j+Z_{lj}\right)-\sum_{j=1}^{N}\left(G_jv^*_i\right)+\sum_{j=1}^{N}G_jK_{2\_j}H_ji_j}{\left(\sum_{j=1}^{N}G_jK_{2\_j}H_j\frac{1}{NZ_L}-N\right)}\right)$$
$$=Ni_k\left(Z_k+Z_{lk}\right)-G_kK_{2\_k}H_ki_k\left(1-N\right)$$

$$NG_kv^*_i+G_kK_{2\_k}H_k\sum_{\substack{j=1\\j\neq k}}^{N}i_j-N\left(\frac{\begin{array}{c}\sum_{\substack{j=1\\j\neq k}}^{N}i_j\left(Z_j+Z_{lj}\right)+i_k\left(Z_k+Z_{lk}\right)-\sum_{j=1}^{N}\left(G_jv^*_i\right)\\+\sum_{\substack{j=1\\j\neq k}}^{N}G_jK_{2\_j}H_ji_j+G_kK_{2\_k}H_ki_k\end{array}}{\left(\sum_{j=1}^{N}G_jK_{2\_j}H_j\frac{1}{NZ_L}-N\right)}\right)$$
$$=Ni_k\left(Z_k+Z_{lk}\right)-G_kK_{2\_k}H_ki_k\left(1-N\right)$$

$$NG_k v^*_i + G_k K_{2\_k} H_k \sum_{\substack{j=1 \\ j\neq k}}^{N} i_j - N\left(\frac{\sum_{\substack{j=1 \\ j\neq k}}^{N} i_j \left(Z_j + Z_{lj}\right) - \sum_{j=1}^{N}\left(G_j v^*_i\right) + \sum_{\substack{j=1 \\ j\neq k}}^{N} G_j K_{2\_j} H_j i_j}{\left(\sum_{j=1}^{N} G_j K_{2\_j} H_j \frac{1}{NZ_L} - N\right)}\right)$$

$$= Ni_k\left(Z_k + Z_{lk}\right) - G_k K_{2\_k} H_k i_k \left(1-N\right) + \frac{Ni_k\left(Z_k + Z_{lk}\right) + NG_k K_{2\_k} H_k i_k}{\left(\sum_{j=1}^{N} G_j K_{2\_j} H_j \frac{1}{NZ_L} - N\right)}$$

$$W = \left(\sum_{j=1}^{N} G_j K_{2\_j} H_j \frac{1}{NZ_L} - N\right)$$

$$NWG_k v^*_i + WG_k K_{2\_k} H_k \sum_{\substack{j=1 \\ j\neq k}}^{N} i_j - N\left(\sum_{\substack{j=1 \\ j\neq k}}^{N} i_j \left(Z_j + Z_{lj}\right) - \sum_{j=1}^{N}\left(G_j v^*_i\right) + \sum_{\substack{j=1 \\ j\neq k}}^{N} G_j K_{2\_j} H_j i_j\right)$$

$$= NWi_k\left(Z_k + Z_{lk}\right) - WG_k K_{2\_k} H_k i_k \left(1-N\right) + Ni_k\left(Z_k + Z_{lk}\right) + NG_k K_{2\_k} H_k i_k$$

$$i_k\left[NW\left(Z_k + Z_{lk}\right) - WG_k K_{2\_k} H_k \left(1-N\right) + N\left(Z_k + Z_{lk}\right) + NG_k K_{2\_k} H_k\right]$$

$$= W\left(NG_k v^*_i + G_k K_{2\_k} H_k \sum_{\substack{j=1 \\ j\neq k}}^{N} i_j\right) - N\left(\sum_{\substack{j=1 \\ j\neq k}}^{N} i_j \left(Z_j + Z_{lj}\right) - \sum_{j=1}^{N}\left(G_j v^*_i\right) + \sum_{\substack{j=1 \\ j\neq k}}^{N} G_j K_{2\_j} H_j i_j\right)$$

$$i_k = \frac{W\left(NG_k v^*_i + G_k K_{2\_k} H_k \sum_{\substack{j=1 \\ j\neq k}}^{N} i_j\right) - N\left(\sum_{\substack{j=1 \\ j\neq k}}^{N} i_j \left(Z_j + Z_{lj}\right) - \sum_{j=1}^{N}\left(G_j v^*_i\right) + \sum_{\substack{j=1 \\ j\neq k}}^{N} G_j K_{2\_j} H_j i_j\right)}{W\left[N\left(Z_k + Z_{lk}\right) - G_k K_{2\_k} H_k \left(1-N\right)\right] + N\left(Z_k + Z_{lk}\right) + NG_k K_{2\_k} H_k}$$

$$i_k = \frac{\begin{array}{c}\left(\sum_{j=1}^{N} G_j K_{2\_j} H_j \frac{1}{NZ_L} - N\right)\left(NG_k v^*_i + G_k K_{2\_k} H_k \sum_{\substack{j=1 \\ j\neq k}}^{N} i_j\right) \\ -N\left(\sum_{\substack{j=1 \\ j\neq k}}^{N} i_j \left(Z_j + Z_{lj}\right) - \sum_{j=1}^{N}\left(G_j v^*_i\right) + \sum_{\substack{j=1 \\ j\neq k}}^{N} G_j K_{2\_j} H_j i_j\right)\end{array}}{\begin{array}{c}\left(\sum_{j=1}^{N} G_j K_{2\_j} H_j \frac{1}{NZ_L} - N\right)\left[N\left(Z_k + Z_{lk}\right) - G_k K_{2\_k} H_k \left(1-N\right)\right] \\ +N\left(Z_k + Z_{lk}\right) + NG_k K_{2\_k} H_k\end{array}} \qquad \text{(B.15)}$$

When equations (B.12) are assumed, equation (B.14) can be simplified to (B.16)

$$i_k = \frac{G\left[v^*_i + \left(i^* - i_k\right)K_2H\right] - v_o}{\left(Z + Z_{lk}\right)}$$

$$i_k = \frac{G\left[v^*_i + \left(\dfrac{\sum_{j=1}^{N} i_j}{N} - i_k\right)K_2H\right] - \left(\dfrac{Gv^*_i - \dfrac{1}{N}\sum_{j=1}^{N} i_j Z_{lj}}{1 + \dfrac{Z}{NZ_L}}\right)}{\left(Z + Z_{lk}\right)}$$

$$\text{Let } 1 + \frac{Z}{NZ_L} = X$$

$$i_k = \frac{G\left[v^*_i + \left(\dfrac{\sum_{j=1}^{N} i_j}{N} - i_k\right)K_2H\right] - \left(\dfrac{Gv^*_i - \dfrac{1}{N}\sum_{j=1}^{N} i_j Z_{lj}}{X}\right)}{\left(Z + Z_{lk}\right)}$$

$$i_k = \frac{XG\left[v^*_i + \left(\frac{1}{N}\sum_{j=1}^{N} i_j - i_k\right)K_2H\right] - \left(Gv^*_i - \frac{1}{N}\sum_{j=1}^{N} i_j Z_{lj}\right)}{X\left(Z + Z_{lk}\right)}$$

$$i_k = \frac{XGv^*_i + XGK_2H\left(\frac{1}{N}\sum_{j=1}^{N} i_j - i_k\right) - Gv^*_i + \frac{1}{N}\sum_{j=1}^{N} i_j Z_{lj}}{X\left(Z + Z_{lk}\right)}$$

$$i_k = \frac{NXGv^*_i + XGK_2H\left(\sum_{\substack{j=1 \\ j\neq k}}^{N} i_j + i_k\left(1 - N\right)\right) - NGv^*_i + \sum_{\substack{j=1 \\ j\neq k}}^{N} i_j Z_{lj} + i_k Z_{lk}}{NX\left(Z + Z_{lk}\right)}$$

$$i_k + XGHi_k(1-N) - i_k Z_{lk} = NXGv^*_i + XGH\sum_{\substack{j=1 \\ j\neq k}}^{N} i_j - NGv^*_i + \sum_{\substack{j=1 \\ j\neq k}}^{N} i_j Z_{lj}$$

$$i_k = \frac{N\left(1+\frac{Z}{NZ_L}\right)Gv^*_i + \left(1+\frac{Z}{NZ_L}\right)GK_2H\sum_{\substack{j=1 \\ j\neq k}}^{N} i_j - NGv^*_i + \sum_{\substack{j=1 \\ j\neq k}}^{N} i_j Z_{lj}}{1+\left(1+\frac{Z}{NZ_L}\right)GK_2H(1-N) - Z_{lk}} \qquad \text{(B.16)}$$

B.4 Voltage Stability

The stability of the output voltage only depends on the denominator of (B.13) in which the characteristic equation is given by

$$1+\frac{Z}{NZ_L}=0 \tag{B.17}$$

B.4.1 Root locus equation for K_p

Replacing Z in (B.17) with (B.5), the following equation can be obtained.

$$\begin{aligned}1+\frac{L_f s^3+(2L_f w_c+R_f)s^2+\left[L_f(w_c{}^2+w_o{}^2)+2R_f w_c\right]s+R_f(w_c{}^2+w_o{}^2)}{NZ_L L_f C_f s^4+\left[NZ_L 2w_c L_f C_f+NZ_L R_f C_f+NZ_L K_1 K_c C_f\right]s^3}=0\\ +\left[\begin{matrix}NZ_L L_f C_f(w_c{}^2+w_o{}^2)+NZ_L 2w_c R_f C_f\\ +NZ_L+NZ_L 2w_c K_1 K_c C_f+NZ_L K_1 K_P\end{matrix}\right]s^2\\ +\left[\begin{matrix}NZ_L R_f C_f(w_c{}^2+w_o{}^2)+NZ_L 2w_c\\ +NZ_L(w_c{}^2+w_o{}^2)K_1 K_c C_f+NZ_L K_1(2K_P w_c+K_{\mathrm{Res}})\end{matrix}\right]s\\ +NZ_L\left(w_c{}^2+w_o{}^2\right)+NZ_L K_1 K_P(w_c{}^2+w_o{}^2)+NZ_L K_1 K_{\mathrm{Res}} w_c\end{aligned} \tag{B.18}$$

By factoring out K_P, the following is obtained

$$\begin{aligned}1+\frac{L_f s^3+(2L_f w_c+R_f)s^2+\left[L_f(w_c{}^2+w_o{}^2)+2R_f w_c\right]s+R_f(w_c{}^2+w_o{}^2)}{K_P\left[NZ_L K_1 s^2+NZ_L K_1 2w_c s+NZ_L K_1(w_c{}^2+w_o{}^2)\right]+NZ_L L_f C_f s^4}=0\\ +\left[NZ_L 2w_c L_f C_f+NZ_L R_f C_f+NZ_L K_1 K_c C_f\right]s^3\\ +\left[NZ_L L_f C_f(w_c{}^2+w_o{}^2)+NZ_L 2w_c R_f C_f+NZ_L+NZ_L 2w_c K_1 K_c C_f\right]s^2\\ +\left[\begin{matrix}NZ_L R_f C_f(w_c{}^2+w_o{}^2)+NZ_L 2w_c\\ +NZ_L(w_c{}^2+w_o{}^2)K_1 K_c C_f+NZ_L K_1 K_{\mathrm{Res}}\end{matrix}\right]s\\ +NZ_L\left(w_c{}^2+w_o{}^2\right)+NZ_L K_1 K_{\mathrm{Res}} w_c\end{aligned} \tag{B.19}$$

Equation (B.19) is then rearranged as follows to get the characteristic equations to find the root locus of K_P

$$1+\frac{A}{BK_P+C}=0$$
$$BK_P+A+C=0$$
$$\frac{A+C}{A+C}+\frac{BK_P}{A+C}=0$$
$$1+\frac{BK_P}{A+C}=0$$

$$1+\frac{K_P\left[NZ_LK_1s^2+NZ_LK_1 2w_c s+NZ_LK_1(w_c{}^2+w_o{}^2)\right]}{NZ_LL_fC_fs^4+\left[NZ_L 2w_cL_fC_f+NZ_LR_fC_f+NZ_LK_1K_cC_f+L_f\right]s^3}=0$$
$$+\left[\begin{array}{c}NZ_LL_fC_f(w_c{}^2+w_o{}^2)+NZ_L 2w_cR_fC_f+NZ_L\\+NZ_L 2w_cK_1K_cC_f+2L_fw_c+R_f\end{array}\right]s^2$$
$$+\left[\begin{array}{c}NZ_LR_fC_f(w_c{}^2+w_o{}^2)+NZ_L 2w_c+NZ_L(w_c{}^2+w_o{}^2)K_1K_cC_f\\+NZ_LK_1K_{\mathrm{Res}}+L_f(w_c{}^2+w_o{}^2)+2R_fw_c\end{array}\right]s$$
$$+NZ_L\left(w_c{}^2+w_o{}^2\right)+NZ_LK_1K_{\mathrm{Res}}w_c+R_f(w_c{}^2+w_o{}^2)$$

$$1+\frac{K_P\left[n_{kp2}s^2+n_{kp1}s+n_{kp0}\right]}{d_{kp4}s^4+d_{kp3}s^3+d_{kp2}s^2+d_{kp1}s+d_{kp0}}=0 \qquad \text{(B.20)}$$

$n_{kp2}=NZ_LK_1$; $n_{kp1}=NZ_LK_1 2w_c$; $n_{kp0}=NZ_LK_1(w_c{}^2+w_o{}^2)$;

$d_{kp4}=NZ_LL_fC_f$; $d_{kp3}=NZ_L\left(2w_cL_fC_f+R_fC_f+K_1K_cC_f\right)+L_f$

$d_{kp2}=NZ_L\left[L_fC_f(w_c{}^2+w_o{}^2)+2w_cR_fC_f+2w_cK_1K_cC_f+1\right]+2L_fw_c+R_f$

$d_{kp1}=NZ_L\left[R_fC_f(w_c{}^2+w_o{}^2)+2w_c+K_1K_cC_f(w_c{}^2+w_o{}^2)+K_1K_{\mathrm{Res}}\right]$
$\quad+L_f(w_c{}^2+w_o{}^2)+2R_fw_c$;

$d_{kp0}=NZ_L\left(w_c{}^2+w_o{}^2+K_1K_{\mathrm{Res}}w_c\right)+R_f(w_c{}^2+w_o{}^2)$

B.4.2 Root locus equation for K_{Res}

To investigate the stability of voltage regulation due to resonant gain of the voltage controller K_{Res}, equation (B.18) is rearranged by factoring out K_{Res} term.

$$\begin{aligned}1+\frac{L_f s^3+(2L_f w_c+R_f)s^2+\left[L_f(w_c{}^2+w_o{}^2)+2R_f w_c\right]s+R_f(w_c{}^2+w_o{}^2)}{K_{\mathrm{Res}}\left[NZ_L K_1 s+NZ_L K_1 w_c\right]+NZ_L L_f C_f s^4}=0\\ +\left[NZ_L 2w_c L_f C_f+NZ_L R_f C_f+NZ_L K_1 K_c C_f\right]s^3\\ +\begin{bmatrix}NZ_L L_f C_f(w_c{}^2+w_o{}^2)+NZ_L 2w_c R_f C_f+NZ_L\\ +NZ_L 2w_c K_1 K_c C_f+NZ_L K_1 K_P\end{bmatrix}s^2\\ +\begin{bmatrix}NZ_L R_f C_f(w_c{}^2+w_o{}^2)+NZ_L 2w_c\\ +NZ_L(w_c{}^2+w_o{}^2)K_1 K_c C_f+NZ_L K_1 2K_P w_c\end{bmatrix}s\\ +NZ_L\left(w_c{}^2+w_o{}^2\right)+NZ_L K_1 K_P(w_c{}^2+w_o{}^2)\end{aligned} \tag{B.21}$$

Equation (B.21) is then rearranged as follows to get the characteristic equations to find the root locus of K_{Res}

$$1+\frac{A}{BK_{\mathrm{Res}}+C}=0$$
$$BK_{\mathrm{Res}}+A+C=0$$
$$\frac{A+C}{A+C}+\frac{BK_{\mathrm{Res}}}{A+C}=0$$
$$1+\frac{BK_{\mathrm{Res}}}{A+C}=0$$

$$\begin{aligned}1+\frac{K_{\mathrm{Res}}\left(NZ_L K_1 s+NZ_L K_1 w_c\right)}{NZ_L L_f C_f s^4+\left[NZ_L 2w_c L_f C_f+NZ_L R_f C_f+NZ_L K_1 K_c C_f+L_f\right]s^3}\\ +\begin{bmatrix}NZ_L L_f C_f(w_c{}^2+w_o{}^2)+NZ_L 2w_c R_f C_f+NZ_L\\ +NZ_L 2w_c K_1 K_c C_f+NZ_L K_1 K_P+2L_f w_c+R_f\end{bmatrix}s^2\\ +\begin{bmatrix}NZ_L R_f C_f(w_c{}^2+w_o{}^2)+NZ_L 2w_c+NZ_L(w_c{}^2+w_o{}^2)K_1 K_c C_f\\ +NZ_L K_1 2K_P w_c+L_f(w_c{}^2+w_o{}^2)+2R_f w_c\end{bmatrix}s\\ +R_f(w_c{}^2+w_o{}^2)+NZ_L\left(w_c{}^2+w_o{}^2\right)+NZ_L K_1 K_P(w_c{}^2+w_o{}^2)\end{aligned}$$

$$1+\frac{K_{\text{Res}}\left[n_{kr1}s+n_{kr0}\right]}{d_{kr4}s^4+d_{kr3}s^3+d_{kr2}s^2+d_{kr1}s+d_{kr0}}=0 \tag{B.22}$$

$$n_{kr1}=NZ_LK_1\ ;\ n_{kr0}=NZ_LK_1w_c\ ;d_{kr4}=NZ_LL_fC_f$$

$$d_{kr3}=NZ_L\left(2w_cL_fC_f+R_fC_f+K_1K_cC_f\right)+L_f$$

$$d_{kr2}=NZ_L\left[L_fC_f(w_c^{\,2}+w_o^{\,2})+2w_cR_fC_f+2w_cK_1K_cC_f+K_1K_P+1\right]+2L_fw_c+R_f$$

$$d_{kr1}=NZ_L\left[R_fC_f(w_c^{\,2}+w_o^{\,2})+K_1K_cC_f(w_c^{\,2}+w_o^{\,2})+2K_1K_Pw_c+2w_c\right]$$
$$+L_f(w_c^{\,2}+w_o^{\,2})+2R_fw_c$$

$$d_{kr0}=NZ_L\left[\left(w_c^{\,2}+w_o^{\,2}\right)+K_1K_P(w_c^{\,2}+w_o^{\,2})\right]+R_f(w_c^{\,2}+w_o^{\,2})$$

B.4.3 Root locus equation for K_1

To investigate the stability of voltage regulation due gain scheduler 1 gain, K_1, equation (B.18) is rearranged by factoring out K_1 term.

$$1+\frac{L_fs^3+(2L_fw_c+R_f)s^2+\left[L_f(w_c^{\,2}+w_o^{\,2})+2R_fw_c\right]s+R_f(w_c^{\,2}+w_o^{\,2})}{\begin{array}{c}K_1\left[\begin{array}{c}NZ_LK_1K_cC_fs^3+\left(NZ_L2w_cK_cC_f+NZ_LK_P\right)s^2\\+\left[NZ_L(w_c^{\,2}+w_o^{\,2})K_cC_f+NZ_L(2K_Pw_c+K_{\text{Res}})\right]s\\+NZ_LK_P(w_c^{\,2}+w_o^{\,2})+NZ_LK_{\text{Res}}w_c\end{array}\right]\\+NZ_LL_fC_fs^4+\left[NZ_L2w_cL_fC_f+NZ_LR_fC_f\right]s^3\\+\left[NZ_LL_fC_f(w_c^{\,2}+w_o^{\,2})+NZ_L2w_cR_fC_f+NZ_L\right]s^2\\+\left[NZ_LR_fC_f(w_c^{\,2}+w_o^{\,2})+NZ_L2w_c\right]s\\+NZ_L\left(w_c^{\,2}+w_o^{\,2}\right)\end{array}}=0 \tag{B.23}$$

Equation (B.23) is then rearranged as follows to get the characteristic equations to find the root locus of K_1

$$1+\frac{A}{BK_1+C}=0$$

$$BK_1+A+C=0$$

$$\frac{A+C}{A+C}+\frac{BK_1}{A+C}=0$$

$$1+\frac{BK_1}{A+C}=0$$

$$1+\frac{K_1\begin{bmatrix} NZ_L K_1 K_c C_f s^3+\left(NZ_L 2w_c K_c C_f + NZ_L K_P\right)s^2 \\ +\left[NZ_L(w_c{}^2+w_o{}^2)K_c C_f + NZ_L(2K_P w_c + K_{\text{Res}})\right]s \\ +NZ_L K_P(w_c{}^2+w_o{}^2)+NZ_L K_{\text{Res}} w_c \end{bmatrix}}{\begin{matrix} L_f s^3+(2L_f w_c+R_f)s^2+\left[L_f(w_c{}^2+w_o{}^2)+2R_f w_c\right]s+R_f(w_c{}^2+w_o{}^2) \\ +NZ_L L_f C_f s^4+\left[NZ_L 2w_c L_f C_f + NZ_L R_f C_f\right]s^3 \\ +\left[NZ_L L_f C_f(w_c{}^2+w_o{}^2)+NZ_L 2w_c R_f C_f + NZ_L\right]s^2 \\ +\left[NZ_L R_f C_f(w_c{}^2+w_o{}^2)+NZ_L 2w_c\right]s+NZ_L\left(w_c{}^2+w_o{}^2\right) \end{matrix}}=0$$

$$1+\frac{K_1\begin{bmatrix} NZ_L K_c C_f s^3+NZ_L\left(2w_c K_c C_f + K_P\right)s^2 \\ +NZ_L\left[K_c C_f(w_c{}^2+w_o{}^2)+2K_P w_c + K_{\text{Res}}\right]s \\ +NZ_L\left[K_P(w_c{}^2+w_o{}^2)+K_{\text{Res}} w_c\right] \end{bmatrix}}{\begin{matrix} NZ_L L_f C_f s^4+\left[NZ_L\left(2w_c L_f C_f + R_f C_f\right)+L_f\right]s^3 \\ +\left[NZ_L\left(L_f C_f(w_c{}^2+w_o{}^2)+2w_c R_f C_f+1\right)+2L_f w_c + R_f\right]s^2 \\ +\left[NZ_L\left(R_f C_f(w_c{}^2+w_o{}^2)+2w_c\right)+L_f(w_c{}^2+w_o{}^2)+2R_f w_c\right]s \\ +NZ_L\left(w_c{}^2+w_o{}^2\right)+R_f(w_c{}^2+w_o{}^2) \end{matrix}}=0$$

$$1+\frac{K_1\left[n_{k3}s^3+n_{k2}s^2+n_{k1}s+n_{k0}\right]}{d_{k4}s^4+d_{k3}s^3+d_{k2}s^2+d_{k1}s+d_{k0}}=0 \qquad \text{(B.24)}$$

$n_{k3}=NZ_L K_c C_f$; $n_{k2}=NZ_L\left(2w_c K_c C_f + K_P\right)$;

$n_{k1}=NZ_L\left[K_c C_f(w_c{}^2+w_o{}^2)+2K_P w_c + K_{\text{Res}}\right]$;

$n_{k0}=NZ_L\left[K_P(w_c{}^2+w_o{}^2)+K_{\text{Res}} w_c\right]$; $d_{k4}=NZ_L L_f C_f$;

$d_{k3}=NZ_L\left(2w_c L_f C_f + R_f C_f\right)+L_f$;

$d_{k2}=NZ_L\left(L_f C_f(w_c{}^2+w_o{}^2)+2w_c R_f C_f+1\right)+2L_f w_c + R_f$;

$d_{k1}=NZ_L\left(R_f C_f(w_c{}^2+w_o{}^2)+2w_c\right)+L_f(w_c{}^2+w_o{}^2)+2R_f w_c$;

$d_{k0}=NZ_L\left(w_c{}^2+w_o{}^2\right)+R_f(w_c{}^2+w_o{}^2)$

B.5 Current Stability

The stability of the output current only depends on the denominator of (B.16) in which the characteristic equation is given by

$$1+\left(1+\frac{Z}{NZ_L}\right)GK_2H(1-N)-Z_{lk}=0 \tag{B.25}$$

B.5.1 Root locus equation for K_{Ph} and K_{ResH}

H as mentioned is the outer current sharing loop controller. It utilizes a proportional resonance controller, given by

$$H=K_{PH}+\frac{K_{\mathrm{Res}H}(s+w_c)}{s^2+2w_cs+{w_c}^2+{w_o}^2} \tag{B.26}$$

where K_{PH} is the proportional gain and K_{ResH} is the resonant gain of the controller. The effects of these parameters value on the stability of the output current are investigated. Replacing G, Z and H in (B.25) with (B.3), (B.5) and (B.26) respectively and rearranging the equation to factor out K_{PH} and K_{ResH}, the characteristic equations to find the root locus for K_{PH} and K_{ResH} become (B.27) and (B.28). Detail equation components are given in (B.30), (B.31), (B.32) and (B.33)

$$1+\frac{K_{PH}\left(\begin{array}{l}P_{n8}s^8+P_{n7}s^7+P_{n6}s^6+P_{n5}s^5\\+P_{n4}s^4+P_{n3}s^3+P_{n2}s^2+P_{n1}s+P_{n0}\end{array}\right)}{\begin{array}{l}P_{d10}s^{10}+P_{d9}s^9+P_{d8}s^8+P_{d7}s^7+P_{d6}s^6\\+P_{d5}s^5+P_{d4}s^4+P_{d3}s^3+P_{d2}s^2+P_{d1}s+P_{d0}\end{array}}=0 \tag{B.27}$$

$$P_{n8}=K_2YL_{n6};P_{n7}=K_2Y\left(L_{n5}+2L_{n6}w_c\right);P_{n6}=K_2Y\left(L_{n4}+2L_{n5}w_c+L_{n6}w_x\right);$$
$$P_{n5}=K_2Y\left(L_{n3}+2L_{n4}w_c+L_{n5}w_x\right);P_{n4}=K_2Y\left(L_{n2}+2L_{n3}w_c+L_{n4}w_x\right);$$
$$P_{n3}=K_2Y\left(L_{n1}+2L_{n2}w_c+L_{n3}w_x\right);P_{n2}=K_2Y\left(L_{n0}+2L_{n1}w_c+L_{n2}w_x\right);$$
$$P_{n1}=K_2Y\left(2L_{n0}w_c+L_{n1}w_x\right);P_{n0}=K_2YL_{n0}w_x\ ;\ P_{d10}=XL_{d8};\ P_{d9}=X\left(L_{d7}+2L_{d8}w_c\right);$$
$$P_{d8}=X\left(L_{d6}+2L_{d7}w_c+L_{d8}w_x\right);\ P_{d7}=X\left(L_{d5}+2L_{d6}w_c+L_{d7}w_x\right)+K_2K_{\mathrm{Res}H}YL_{n6};$$
$$P_{d6}=X\left(L_{d4}+2L_{d5}w_c+L_{d6}w_x\right)+K_2K_{\mathrm{Res}H}Y\left(L_{n5}+L_{n6}w_c\right);$$
$$P_{d5}=X\left(L_{d3}+2L_{d4}w_c+L_{d5}w_x\right)+K_2K_{\mathrm{Res}H}Y\left(L_{n4}+L_{n5}w_c\right);$$
$$P_{d4}=X\left(L_{d2}+2L_{d3}w_c+L_{d4}w_x\right)+K_2K_{\mathrm{Res}H}Y\left(L_{n3}+L_{n4}w_c\right);$$
$$P_{d3}=X\left(L_{d1}+2L_{d2}w_c+L_{d3}w_x\right)+K_2K_{\mathrm{Res}H}Y\left(L_{n2}+L_{n3}w_c\right);$$
$$P_{d2}=X\left(L_{d0}+2L_{d1}w_c+L_{d2}w_x\right)+K_2K_{\mathrm{Res}H}Y\left(L_{n1}+L_{n2}w_c\right);$$
$$P_{d1}=X\left(2L_{d0}w_c+L_{d1}w_x\right)+K_2K_{\mathrm{Res}H}Y\left(L_{n0}+L_{n1}w_c\right);\ P_{d0}=XL_{d0}w_x+K_2K_{\mathrm{Res}H}YL_{n0}w_c$$

$$1+\frac{K_{\mathrm{Re}sH}\left(\begin{array}{l}R_{n7}s^7+R_{n6}s^6+R_{n5}s^5+R_{n4}s^4\\+R_{n3}s^3+R_{n2}s^2+R_{n1}s+R_{n0}\end{array}\right)}{\begin{array}{l}R_{d10}s^{10}+R_{d9}s^9+R_{d8}s^8+R_{d7}s^7+R_{d6}s^6\\+R_{d5}s^5+R_{d4}s^4+R_{d3}s^3+R_{d2}s^2+R_{d1}s+R_{d0}\end{array}}=0 \qquad \text{(B.28)}$$

$R_{n7}=K_2YL_{n6}$; $R_{n6}=K_2Y\left(L_{n5}+L_{n6}w_c\right)$; $R_{n5}=K_2Y\left(L_{n4}+L_{n5}w_c\right)$;

$R_{n4}=K_2Y\left(L_{n3}+L_{n4}w_c\right)$; $R_{n3}=K_2Y\left(L_{n2}+L_{n3}w_c\right)$; $R_{n2}=K_2Y\left(L_{n1}+L_{n2}w_c\right)$;

$R_{n1}=K_2Y\left(L_{n0}+L_{n1}w_c\right)$; $R_{n0}=K_2YL_{n0}w_c$; $R_{d10}=XL_{d8}$; $R_{d9}=X\left(L_{d7}+2L_{d8}w_c\right)$;

$R_{d8}=X\left(L_{d6}+2L_{d7}w_c+L_{d8}w_x\right)+K_2K_{PH}YL_{n6}$;

$R_{d7}=X\left(L_{d5}+2L_{d6}w_c+L_{d7}w_x\right)+K_2K_{PH}Y\left(L_{n5}+2L_{n6}w_c\right)$;

$R_{d6}=X\left(L_{d4}+2L_{d5}w_c+L_{d6}w_x\right)+K_2K_{PH}Y\left(L_{n4}+2L_{n5}w_c+L_{n6}w_x\right)$;

$R_{d5}=X\left(L_{d3}+2L_{d4}w_c+L_{d5}w_x\right)+K_2K_{PH}Y\left(L_{n3}+2L_{n4}w_c+L_{n5}w_x\right)$;

$R_{d4}=X\left(L_{d2}+2L_{d3}w_c+L_{d4}w_x\right)+K_2K_{PH}Y\left(L_{n2}+2L_{n3}w_c+L_{n4}w_x\right)$;

$R_{d3}=X\left(L_{d1}+2L_{d2}w_c+L_{d3}w_x\right)+K_2K_{PH}Y\left(L_{n1}+2L_{n2}w_c+L_{n3}w_x\right)$;

$R_{d2}=X\left(L_{d0}+2L_{d1}w_c+L_{d2}w_x\right)+K_2K_{PH}Y\left(L_{n0}+2L_{n1}w_c+L_{n2}w_x\right)$;

$R_{d1}=X\left(2L_{d0}w_c+L_{d1}w_x\right)+K_2K_{PH}Y\left(2L_{n0}w_c+L_{n1}w_x\right)$;

$R_{d0}=XL_{d0}w_x+K_2K_{PH}YL_{n0}w_x$

B.5.2 Root locus equation for K_2

K_2 is the gain of gain scheduler 2. The effect of this parameter value on the stability of the output current is investigated. Replacing *G*, *Z* and *H* in (B.25) with (B.3), (B.5) and (B.26) respectively and rearranging the equation to factor out K_2, the characteristic equations to find the root locus for K_2 becomes (B.29). Detail equation components are given in (B.30), (B.31), (B.32) and (B.33)

$$1+\frac{K_2\begin{pmatrix} T_{n8}s^8+T_{n7}s^7+T_{n6}s^6+T_{n5}s^5 \\ +T_{n4}s^4+T_{n3}s^3+T_{n2}s^2+T_{n1}s+T_{n0}\end{pmatrix}}{\begin{matrix}T_{d10}s^{10}+T_{d9}s^9+T_{d8}s^8+T_{d7}s^7+T_{d6}s^6 \\ +T_{d5}s^5+T_{d4}s^4+T_{d3}s^3+T_{d2}s^2+T_{d1}s+T_{d0}\end{matrix}}=0 \tag{B.29}$$

$$T_{n8}=K_{PH}YL_{n6};$$
$$T_{n7}=K_{PH}Y\left(L_{n5}+2L_{n6}w_c\right)+K_{ResH}YL_{n6};$$
$$T_{n6}=K_{PH}Y\left(L_{n4}+2L_{n5}w_c+L_{n6}w_x\right)+K_{ResH}Y\left(L_{n5}+L_{n6}w_c\right);$$
$$T_{n5}=K_{PH}Y\left(L_{n3}+2L_{n4}w_c+L_{n5}w_x\right)+K_{ResH}Y\left(L_{n4}+L_{n5}w_c\right);$$
$$T_{n4}=K_{PH}Y\left(L_{n2}+2L_{n3}w_c+L_{n4}w_x\right)+K_{ResH}Y\left(L_{n3}+L_{n4}w_c\right);$$
$$T_{n3}=K_{PH}Y\left(L_{n1}+2L_{n2}w_c+L_{n3}w_x\right)+K_{ResH}Y\left(L_{n2}+L_{n3}w_c\right);$$
$$T_{n2}=K_{PH}Y\left(L_{n0}+2L_{n1}w_c+L_{n2}w_x\right)+K_{ResH}Y\left(L_{n1}+L_{n2}w_c\right);$$
$$T_{n1}=K_{PH}Y\left(2L_{n0}w_c+L_{n1}w_x\right)+K_{ResH}Y\left(L_{n0}+L_{n1}w_c\right);$$
$$T_{n0}=K_{PH}YL_{n0}w_x+K_{ResH}YL_{n0}w_c;$$
$$T_{d10}=XL_{d8};$$
$$T_{d9}=X\left(L_{d7}+2L_{d8}w_c\right);$$
$$T_{d8}=X\left(L_{d6}+2L_{d7}w_c+L_{d8}w_x\right);$$
$$T_{d7}=X\left(L_{d5}+2L_{d6}w_c+L_{d7}w_x\right);$$
$$T_{d6}=X\left(L_{d4}+2L_{d5}w_c+L_{d6}w_x\right);$$
$$T_{d5}=X\left(L_{d3}+2L_{d4}w_c+L_{d5}w_x\right);$$
$$T_{d4}=X\left(L_{d2}+2L_{d3}w_c+L_{d4}w_x\right);$$
$$T_{d3}=X\left(L_{d1}+2L_{d2}w_c+L_{d3}w_x\right);$$
$$T_{d2}=X\left(L_{d0}+2L_{d1}w_c+L_{d2}w_x\right);$$
$$T_{d1}=X\left(2L_{d0}w_c+L_{d1}w_x\right);$$
$$T_{d0}=XL_{d0}w_x;$$

$$
\begin{aligned}
&L_{n6} = Vg_{n2}z_{d4}; L_{n5} = V\left(g_{n1}z_{d4} + g_{n2}z_{d3}\right) + g_{n2}z_{n3};\\
&L_{n4} = V\left(g_{n0}z_{d4} + g_{n1}z_{d3} + g_{n2}z_{d2}\right) + g_{n1}z_{n3} + g_{n2}z_{n2};\\
&L_{n3} = V\left(g_{n0}z_{d3} + g_{n1}z_{d2} + g_{n2}z_{d1}\right) + g_{n0}z_{n3} + g_{n1}z_{n2} + g_{n2}z_{n1};\\
&L_{n2} = V\left(g_{n0}z_{d2} + g_{n1}z_{d1} + g_{n2}z_{d0}\right) + g_{n0}z_{n2} + g_{n1}z_{n1} + g_{n2}z_{n0};\\
&L_{n1} = V\left(g_{n0}z_{d1} + g_{n1}z_{d0}\right) + g_{n0}z_{n1} + g_{n1}z_{n0};\\
&L_{n0} = Vg_{n0}z_{d0} + g_{n0}z_{n0}\ ; L_{d8} = Vg_{d4}z_{d4};\\
&L_{d7} = V\left(g_{d3}z_{d4} + g_{d4}z_{d3}\right);\ L_{d6} = V\left(g_{d2}z_{d4} + g_{d3}z_{d3} + g_{d4}z_{d2}\right);\\
&L_{d5} = V\left(g_{d1}z_{d4} + g_{d2}z_{d3} + g_{d3}z_{d2} + g_{d4}z_{d1}\right);\\
&L_{d4} = V\left(g_{d0}z_{d4} + g_{d1}z_{d3} + g_{d2}z_{d2} + g_{d3}z_{d1} + g_{d4}z_{d0}\right);\\
&L_{d3} = V\left(g_{d0}z_{d3} + g_{d1}z_{d2} + g_{d2}z_{d1} + g_{d3}z_{d0}\right);\\
&L_{d2} = V\left(g_{d0}z_{d2} + g_{d1}z_{d1} + g_{d2}z_{d0}\right);\ L_{d1} = V\left(g_{d0}z_{d1} + g_{d1}z_{d0}\right);\\
&L_{d0} = Vg_{d0}z_{d0};
\end{aligned}
\tag{B.30}
$$

$$
X = 1 - Z_{lk}\ ; Y = N - 1\ ;\ w_x = w_c^{\,2} + w_o^{\,2}\ ;\ V = NZ_L; \tag{B.31}
$$

$$
\begin{aligned}
g_{n2} &= K_1(K_P + K_f)\\
g_{n1} &= K_1(2K_P w_c + K_{\mathrm{Res}} + 2K_f w_c)\\
g_{n0} &= K_1\left(K_P(w_c^{\,2} + w_o^{\,2}) + K_f(w_c^{\,2} + w_o^{\,2}) + K_{\mathrm{Res}}w_c\right)\\
g_{d4} &= C_f L_f\\
g_{d3} &= 2w_c C_f L_f + C_f R_f + C_f K_c\\
g_{d2} &= C_f L_f(w_c^{\,2} + w_o^{\,2}) + 2w_c(C_f R_f + C_f K_c) + K_1 K_P + 1\\
g_{d1} &= (C_f R_f + C_f K_c)(w_c^{\,2} + w_o^{\,2}) + 2K_1 K_P w_c + K_1 K_{\mathrm{Res}} + 2w_c\\
g_{d0} &= K_1 K_P(w_c^{\,2} + w_o^{\,2}) + K_1 K_{\mathrm{Res}} w_c + w_c^{\,2} + w_o^{\,2}
\end{aligned}
\tag{B.32}
$$

$$
\begin{aligned}
&z_{n3} = L_f\ ;\ z_{n2} = 2L_f w_c + R_f\ ;\ z_{n1} = L_f(w_c^{\,2} + w_o^{\,2}) + 2R_f w_c\ ;\\
&z_{n0} = R_f(w_c^{\,2} + w_o^{\,2})\ ;\ z_{d4} = L_f C_f\\
&z_{d3} = 2C_f L_f w_c + C_f R_f + K_1 K_c C_f\\
&z_{d2} = C_f L_f\left(w_c^{\,2} + w_o^{\,2}\right) + 2w_c\left(C_f R_f + K_1 K_c C_f\right) + K_1 K_P + 1\\
&z_{d1} = \left(C_f R_f + K_1 K_c C_f\right)\left(w_c^{\,2} + w_o^{\,2}\right) + K_1(2K_P w_c + K_{\mathrm{Res}}) + 2w_c\\
&z_{d0} = K_1 K_P(w_c^{\,2} + w_o^{\,2}) + K_1 K_{\mathrm{Res}} w_c + w_c^{\,2} + w_o^{\,2}
\end{aligned}
\tag{B.33}
$$

Appendix C

Chapter 5 Stability Analysis

C.1 Parallel connected inverter system

An inverter model used in chapter 5 is shown in Figure C.1. This model has two inputs which are input voltage (v_i^*) and output current (i_o) and one output which is the output voltage of the inverter (v_o). Detail parameters of each block are given below:

$$G_1 = \frac{K_p s + K_i}{s}$$
$$G_2 = \frac{1}{L_f s} \qquad \text{(C.1)}$$
$$G_3 = \frac{1}{C_f s}$$

K_p and K_i represent PI controller proportional and integral gain of voltage feedback loop, K_c is the gain for current loop and K is the modulation gain of the inverter. L_f and C_f represent the filter inductance and capacitance respectively.

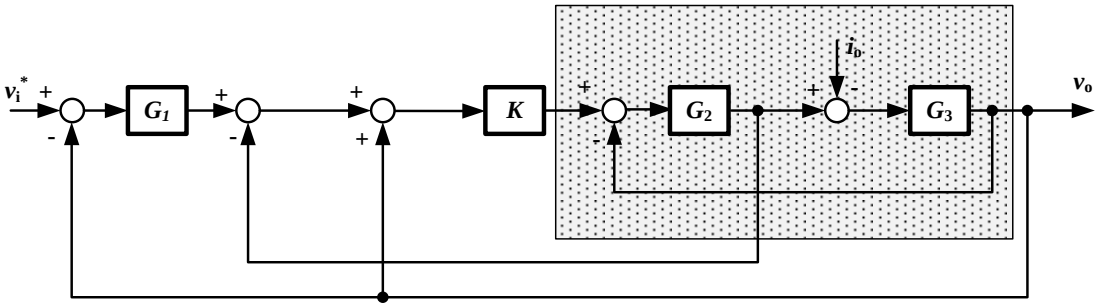


Figure C.1 Inverter model

C.1.1 Closed loop voltage gain (*G*)

The closed-loop voltage gain *G* can be derived from Figure C.1 by setting i_o to 0 and the model can be simplified to:

$$\frac{v_o}{v_i^*} = G = \frac{KG_1G_2G_3}{1+G_2G_3-KG_2G_3+KG_2+KG_1G_2G_3} \tag{C.2}$$

Substituting G_1, G_2, G_3 and G_4 in (C.2) with (C.1), *G* becomes (C.3).

$$G = \frac{K\left(\frac{K_ps+K_i}{s}\right)\frac{1}{L_fs}\frac{1}{C_fs}}{1+\frac{1}{L_fs}\frac{1}{C_fs}-K\frac{1}{L_fs}\frac{1}{C_fs}+K\frac{1}{L_fs}+K\left(\frac{K_ps+K_i}{s}\right)\frac{1}{L_fs}\frac{1}{C_fs}}$$

$$G = \frac{\frac{K\left(K_ps+K_i\right)}{L_fC_fs^3}}{\frac{L_fC_fs^3+s-Ks+KC_fs^2+K\left(K_ps+K_i\right)}{L_fC_fs^3}}$$

$$G = \frac{K\left(K_ps+K_i\right)}{L_fC_fs^3+s-Ks+KC_fs^2+K\left(K_ps+K_i\right)}$$

$$G = \frac{KK_ps+KK_i}{L_fC_fs^3+KC_fs^2+\left(KK_p-K+1\right)s+KK_i} \tag{C.3}$$

C.1.2 Output Impedance (*Z*)

By setting v_i^* to 0, the model in Figure C.1 can be simplified, to find the output impedance of the inverter.

$$-\frac{v_o}{i_o} = Z = \frac{G_3+KG_2G_3}{1+KG_2+KG_1G_2G_3-KG_2G_3+G_2G_3} \tag{C.4}$$

Substituting G_1, G_2, G_3 and G_4 in (C.2) with (C.1), *Z* becomes (C.5)

$$Z = \frac{\frac{1}{C_fs}+K\frac{1}{L_fs}\frac{1}{C_fs}}{1+K\frac{1}{L_fs}+K\left(\frac{K_ps+K_i}{s}\right)\frac{1}{L_fs}\frac{1}{C_fs}-K\frac{1}{L_fs}\frac{1}{C_fs}+\frac{1}{L_fs}\frac{1}{C_fs}}$$

$$Z = \frac{\frac{L_f s^2 + Ks}{C_f L_f s^3}}{\frac{C_f L_f s^3 + KC_f s^2 + K\left(K_p s + K_i\right) - Ks + s}{C_f L_f s^3}}$$

$$Z = \frac{L_f s^2 + Ks}{C_f L_f s^3 + KC_f s^2 + K\left(K_p s + K_i\right) - Ks + s}$$

$$Z = \frac{L_f s^2 + Ks}{C_f L_f s^3 + KC_f s^2 + \left(KK_p - K + 1\right)s + KK_i} \tag{C.5}$$

C.2 Parallel system output voltage

The model of a parallel multi inverter system is shown in Figure C.2. In this model, each inverter is treated as a voltage source connected in series with output impedance and line impedance. All parameter variations including the closed loop voltage gain (G_i), output impedance of the inverter (Z_i), and line impedance (Z_{li}), are taken into consideration. Z_L represents the load impedance and v_o is the output voltage.

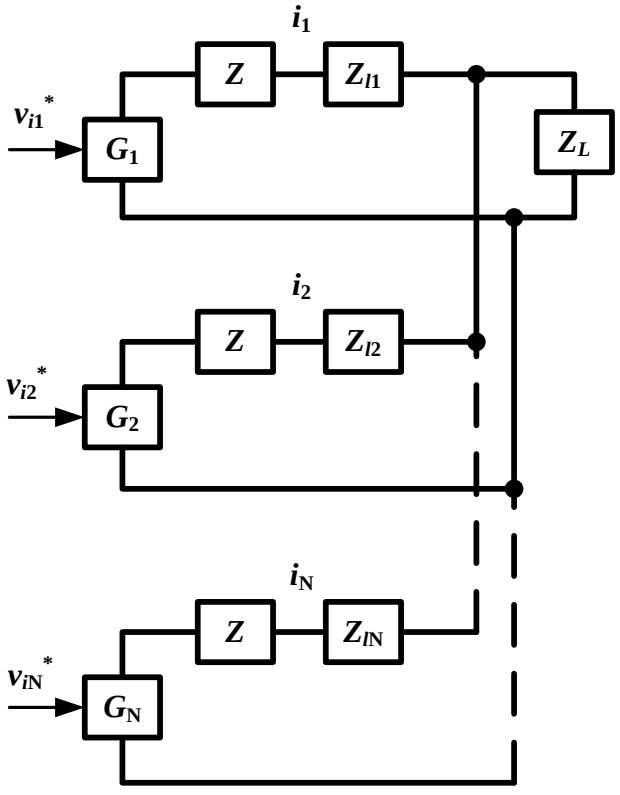


Figure C.2 The model of the parallel multi inverter system

The parallel system can be described as:

$$\sum_{j=1}^{n} i_j = i_1 + i_2 + \ldots + i_n = \frac{v_o}{Z_L} \tag{C.6}$$

$$\begin{aligned} G_1 v^*_{i1} - v_o &= i_1 \left(Z_1 + Z_{l1} \right) \\ G_2 v^*_{i2} - v_o &= i_2 \left(Z_2 + Z_{l2} \right) \\ G_N v^*_{iN} - v_o &= i_N \left(Z_N + Z_{lN} \right) \end{aligned} \tag{C.7}$$

In this model, all the parallel connected inverters are assumed to be the same, where

$$\begin{aligned} G_1 = G_2 = G_N = G \\ Z_1 = Z_2 = Z_N = Z \end{aligned} \tag{C.8}$$

By adding the equations in (C.7) and using the assumption in (C.8), the following is obtained

$$G \sum_{j=1}^{N} v^*_{ij} - N v_o = Z \sum_{j=1}^{N} i_j + \sum_{j=1}^{N} i_j Z_{lj} \tag{C.9}$$

By substituting (C.6) into (C.9) and solving for V_o , a generalized output voltage equation for parallel inverter system (C.10) can be obtained

$$G \sum_{j=1}^{N} v^*_{ij} - N v_o = Z \frac{v_o}{Z_L} + \sum_{j=1}^{N} i_j Z_{lj}$$

$$Z \frac{v_o}{Z_L} + N v_o = G \sum_{j=1}^{N} v^*_{ij} - \sum_{j=1}^{N} i_j Z_{lj}$$

$$v_o \left(\frac{Z}{Z_L} + N \right) = G \sum_{j=1}^{N} v^*_{ij} - \sum_{j=1}^{N} i_j Z_{lj}$$

$$v_o = \frac{\frac{1}{N} G \sum_{j=1}^{N} v^*_{ij} - \frac{1}{N} \sum_{j=1}^{N} i_j Z_{lj}}{1 + \frac{Z}{N Z_L}} \tag{C.10}$$

C.3 Voltage Stability

The stability of the output voltage only depends on the denominator of (C.10) in which the characteristic equation is

$$1+\frac{Z}{NZ_L}=0 \tag{C.11}$$

C.3.1 Root locus equation for K_p

Replacing Z in (C.11) with (C.5), the following equation is obtained.

$$1+\frac{L_f s^2+Ks}{NZ_L\left[C_f L_f s^3+KC_f s^2+\left(KK_p-K+1\right)s+KK_i\right]}=0 \tag{C.12}$$

Equation (C.12) is then rearranged as (C.13) to get the characteristic equations to find the root locus of K_P

$$1+\frac{L_f s^2+Ks}{K_p\left(NZ_L Ks\right)+NZ_L C_f L_f s^3+NZ_L KC_f s^2+\left(NZ_L-NZ_L K\right)s+NZ_L KK_i}=0$$

$$A=L_f s^2+Ks$$
$$B=NZ_L Ks$$
$$C=NZ_L C_f L_f s^3+NZ_L KC_f s^2+\left(NZ_L-NZ_L K\right)s+NZ_L KK_i$$

$$1+\frac{A}{K_p\left(B\right)+C}=0$$
$$K_p\left(B\right)+A+C=0$$
$$\frac{K_p\left(B\right)}{A+C}+\frac{A+C}{A+C}=0$$
$$1+K_p\frac{B}{A+C}=0$$

$$1+K_p\frac{NZ_L Ks}{NZ_L C_f L_f s^3+\left(NZ_L KC_f+L_f\right)s^2+\left(K+NZ_L-NZ_L K\right)s+NZ_L KK_i}=0 \tag{C.13}$$

C.3.2 Root locus equation for K_i

To investigate the stability of the voltage regulation due to the integral gain of the voltage controller K_i, equation (C.12) is rearranged by factoring out the K_i term to get (C.14).

$$1+\frac{L_f s^2+Ks}{K_i\left(NZ_L K\right)+NZ_L C_f L_f s^3+NZ_L K C_f s^2+\left(NZ_L K K_p+NZ_L-NZ_L K\right)s}=0$$

$$A=L_f s^2+Ks$$
$$B=NZ_L K$$
$$C=NZ_L C_f L_f s^3+NZ_L K C_f s^2+\left(NZ_L K K_p+NZ_L-NZ_L K\right)s$$

$$1+\frac{A}{K_i\left(B\right)+C}=0$$
$$K_i\left(B\right)+A+C=0$$
$$\frac{K_i\left(B\right)}{A+C}+\frac{A+C}{A+C}=0$$
$$1+K_i\frac{B}{A+C}=0$$

$$1+K_i\frac{NZ_L K}{NZ_L C_f L_f s^3+\left(NZ_L K C_f+L_f\right)s^2+\left(NZ_L K K_p+K+NZ_L-NZ_L K\right)s}=0 \qquad \text{(C.14)}$$

C.4 Stability analysis of the voltage control loop

In this section, voltage control loop stability is investigated for different values of K_p and K_i by plotting the root locus of these parameters.

C.4.1 Voltage control loop stability due to K_p

Using equations (C.13) and the system values in Table C.1, the root locus of K_p at difference K_i values are plotted in Figure C.3. From the plot, in general when K_p is increased, the system becomes more stable but as the gain gets higher, the system becomes more oscillatory. For K_i values of 100, 200, 400, 800 and 1400, K_p should be more than 0.043, 0.113, 0.256, 0.538 and 0.966 respectively for the system to be stable.

Table C.1 Parameter list

Description	Value
Filter Inductance (L_f)	2 mH
Filter Capacitance (C_f)	30 μF
Modulation Gain (K)	1
Number of Parallel Connected Inverter (N)	3
Load Impedance (Z_L)	12 Ω

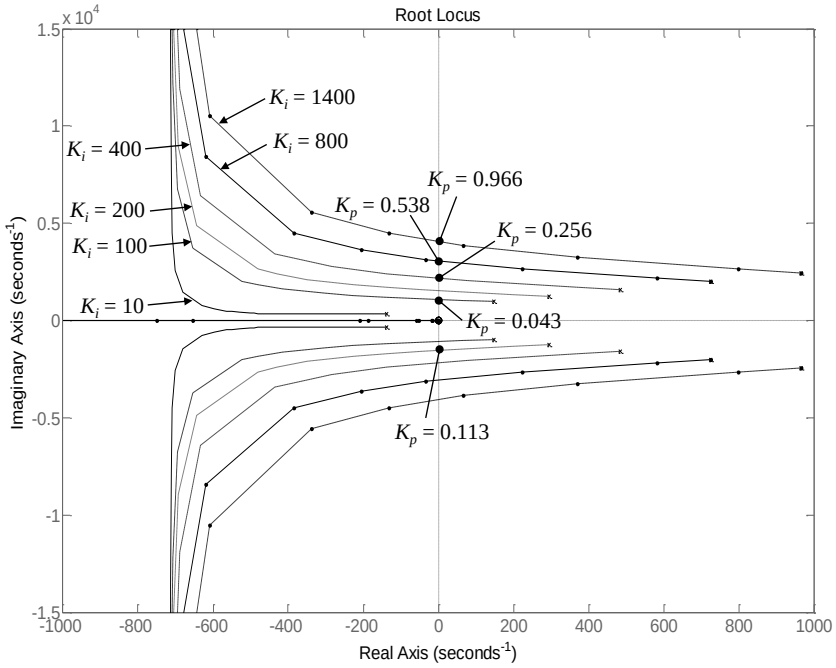


Figure C.3 Root locus of K_p at difference K_i values

C.4.2 Voltage control loop stability due to K_i

To investigate the stability of the voltage control loop due to K_i, equation (C.14) and the system values in Table C.1 are used to plot the root locus of K_i at different K_p values. The root locus plot is shown in Figure C.4. The system becomes less stable as K_i increases. For K_p values of 0.1, 0.2, 0.5, 1, 2 and 4, K_i should not exceed 182, 326, 754, 1470, 2890 and 5760 respectively for the system to remain stable.

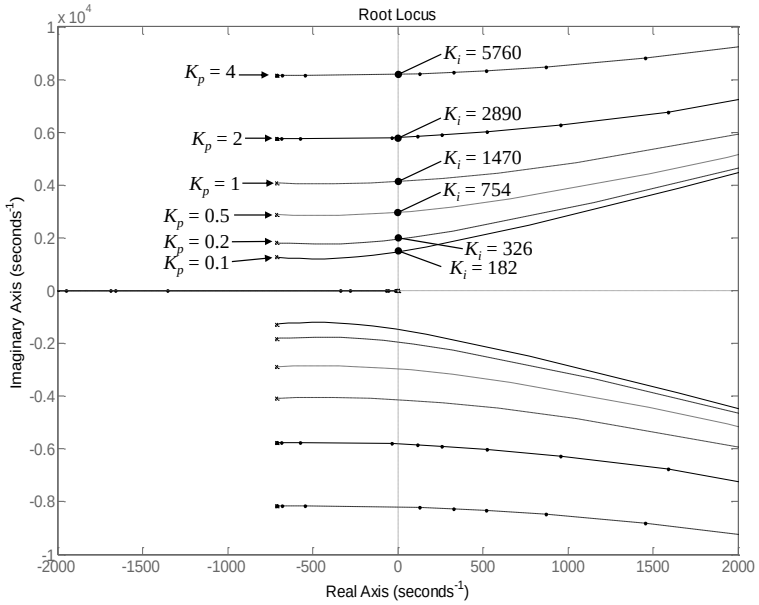


Figure C.4 Root locus of K_i at difference K_p values

C.4.3 Frequency response

In this section, frequency response of closed loop voltage gain (G), and harmonic impedance are investigated. Figure C.5 shows the system frequency response at difference values of K_p when K_i is 800. From the plot, all K_p values produce unity gain with no phase deviation for frequencies less than 150 Hz. Higher K_p values results in higher controller bandwidth.

Figure C.6 shows the Bode plots for the system output impedance at different K_i values when K_P is 2. From the plot, a larger K_i gives lower overall harmonic impedance and the peak response occurs at a higher frequency. The proposed power sharing scheme is derived based on an inductive output impedance, so from the plot a K_i value of 800 makes the output impedance inductive for a wider frequency range.

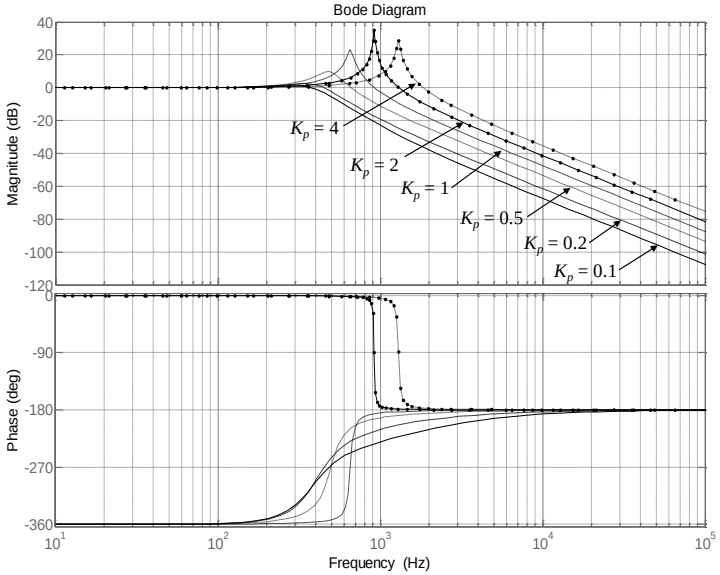


Figure C.5 Bode plot of G at different K_p values

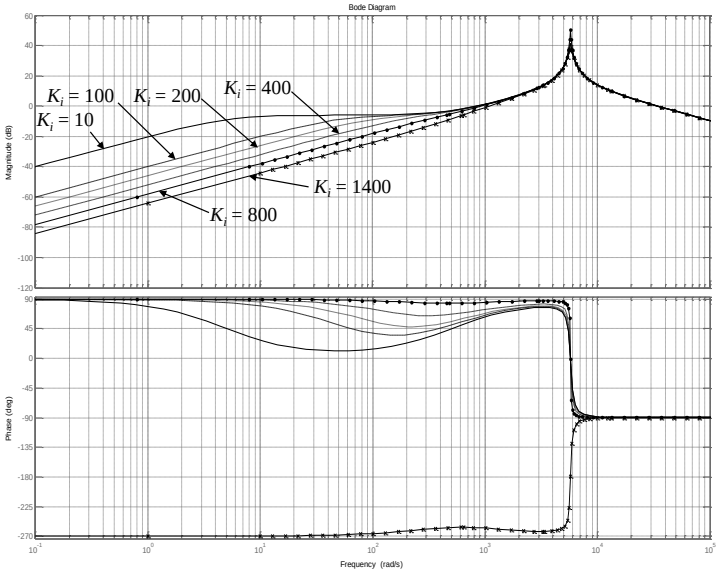


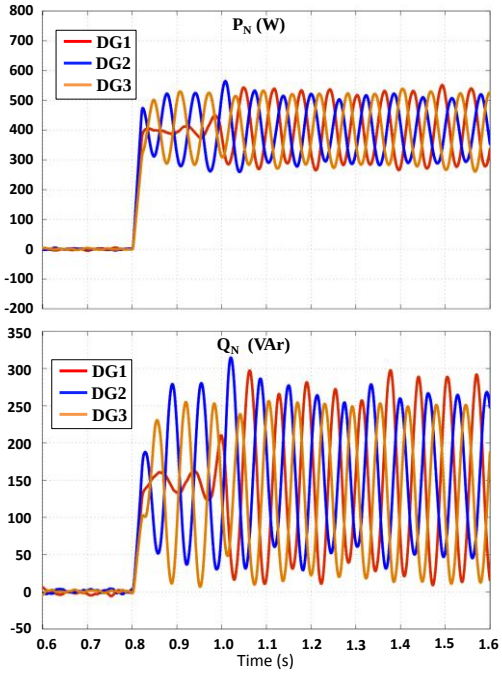
Figure C.6 Bode plot of Z at different K_i values

C.4.4 K_p and K_i selection

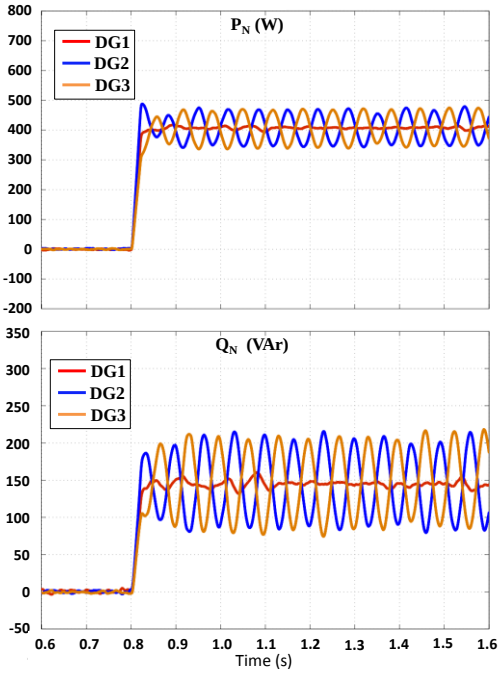
K_p and K_i are selected based on the previous root locus and Bode plots to ensure a stable system and at the same time give low overall harmonic impedance. A K_i value of 800 produces inductive output impedance and lower harmonic impedance so it is the preferred choice for K_i. From Figure C.3, for a K_i of 800, K_p should be more than 0.538 for the system to become stable. A higher K_p results in higher bandwidth but makes the system oscillatory. So there is a trade-off between the two factors. A value of 2 is finally selected for K_p as it gives reasonable bandwidth (1.4 kHz) with modest system oscillation.

C.5 Stability analysis for max power adjustment time (T_r)

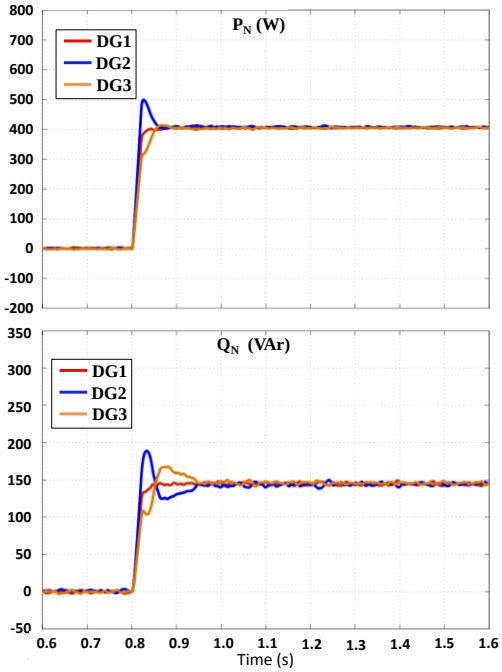
T_r is the maximum time needed to change the inverter output power from an initial operating condition to the desired new operating point in the proposed power sharing scheme. From equations (5.20) and (5.25), the adjustment angle and amplitude depend on this parameter value. To investigate the effect of this parameter value on the stability of the system, load step simulations for different T_r values are conducted using the simulation setup from Chapter 5. Initially, inverters 1, 2 and 3 are connected to the microgrid without supplying any load. At time t=0.8s, Loads 3 and 4 are connected to the microgrid. Figure C.7 shows the simulation results for different T_r values. For a small T_r value, the adjustment angle and amplitude become large thus resulting in significant adjustment in active and reactive powers and vice versa. For T_r = 0.1s, the load step makes the system unstable as shown in Figure C.7 (a). This is because, due to large adjustment to the power angle and amplitude, the active and reactive power differences ($P_{\Delta j}$ and $Q_{\Delta j}$) cannot settle between ± P_{cj} and ±Q_{cj} respectively (refer to Figure 5.6). Figure C.7 (b) shows that the system becomes less unstable when T_r is increased to 0.2s. Figure C.7 parts (c), (d) and (e) show that the system is generally stable but has an under-damped response for reactive power. When T_r = 0.6s, the active and reactive powers produce critically-damped responses as shown in Figure C.7 (f). As the T_r value increases, the system start to produce an over-damped responses for active and reactive powers as shown in Figure C.7 parts (g) and (h). From these observations, 0.6s is selected for T_r.


P_N (W)
DG1
DG2
DG3
Q_N (VAr)
DG1
DG2
DG3
Time (s)

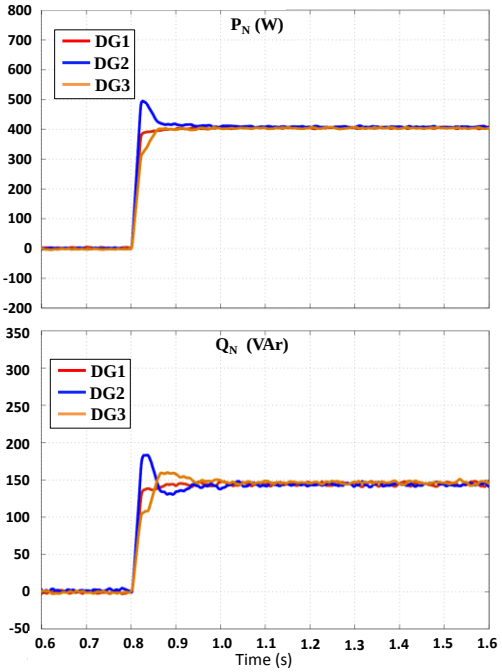
(a)


P_N (W)
DG1
DG2
DG3
Q_N (VAr)
DG1
DG2
DG3
Time (s)

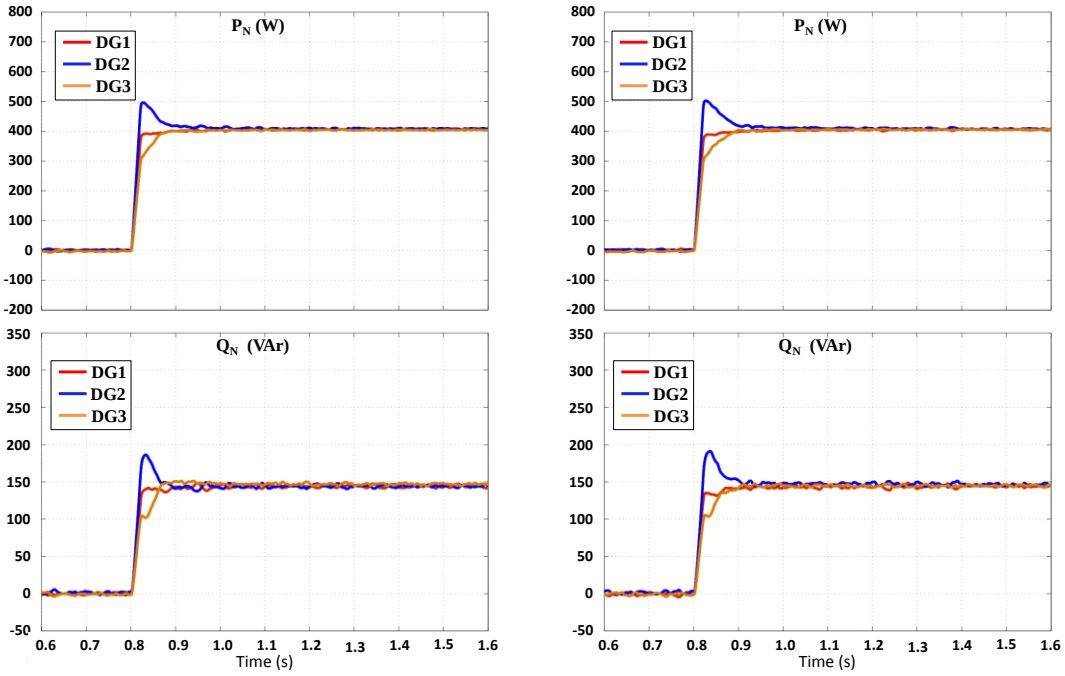
(b)


P_N (W)
DG1
DG2
DG3
Q_N (VAr)
DG1
DG2
DG3
Time (s)

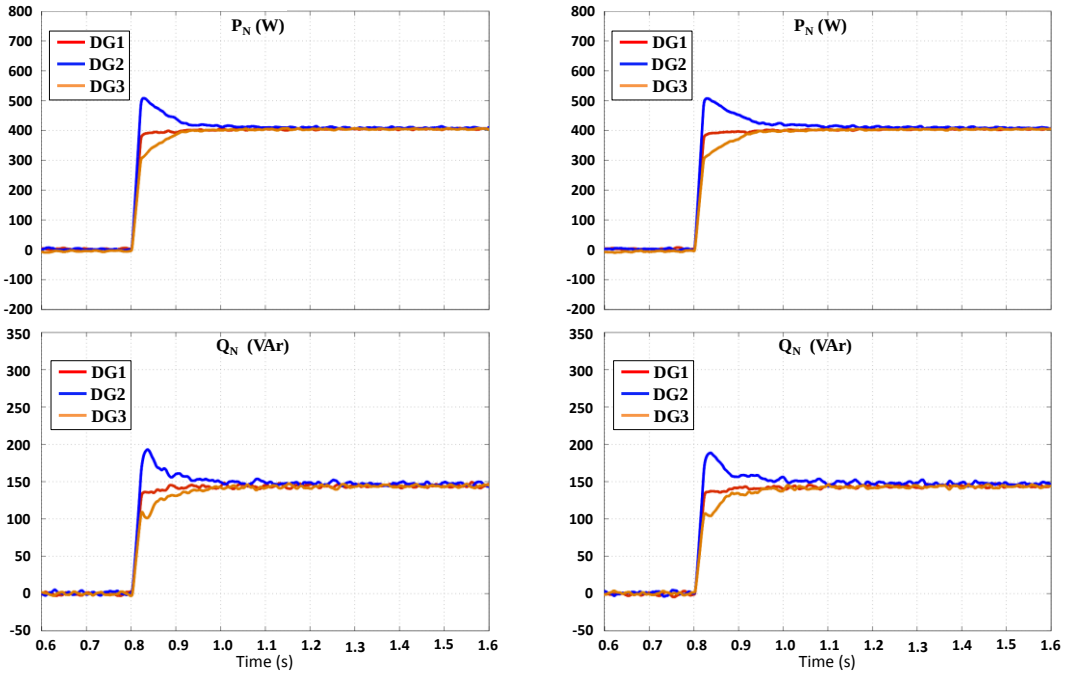
(c)


P_N (W)
DG1
DG2
DG3
Q_N (VAr)
DG1
DG2
DG3
Time (s)

(d)



(e) (f)



(g) (h)

Figure C.7 Load step simulation results for different value of T_r: (a) T_r =0.1s, (b) T_r =0.2s, (c) T_r =0.3s, (d) T_r =0.4s, (e) T_r =0.5s, (f) T_r =0.6s, (g) T_r =0.8s and (h) T_r =1s

Appendix D

Sample DSP Codes for Experimental Implementation

C code for selected control algorithms proposed in this thesis are presented here; namely, DSP main program (variables definition), ADC conversion, digital filter, reference voltage generation, central controller(P Ref Calculation), power sharing, voltage controller, current sharing and SPWM. For the sake of simplicity and clarity of code presented, introductory portions of the code with DSP register configurations are omitted. Only variable declarations and the control algorithm code implemented are included here.

D.1 DSP Main Program – Variables definition

```
#include "MAIN.h"
#include "stdio.h"
#include "math.h"

//Constant
float pi=22.0/7.0;int Zcheck=84;

//System Initialization
float Tz=2381;                  //switching period multiplier
float Half_Tz=1190;             //Half of the switching period
float VDC=150.0;                //DC Voltage (Volts)
float freq=50.0;                //frequency of the system
float delay=7;                  //delay to slowly increase the amplitude of Vref
float timer1=30;                //time to close contactor...
float ff=0.0002381136216;       //initial timing to adjust the frequency
float fff=0.0000001;            //compensation to adjust ff
float Imax=20.0;                //Maximum output current value
float MAG=60.0;                 //46.0 is max for 100VDC
float freq2;                    //frequency after droop
float Xalfa=0;
float dm=0.0001;                //droop coefficient

//Special Operation
int contactor_only=0;           //if 0 --> normal operation if 1 --> contactor only operation

//Normal Operation
int bypass_ph_reset=0;          //initial phase resetif 0 -->dont bypass if 1 --> bypass
int bypass_freq_sync=1;         //freq sync if 0 -->dont bypass if 1 --> bypass
int bypass_v_check=1;           //voltage noise checkif 0 -->dont bypass if 1 --> bypass
//Modulation Type
int modulation=1;               //if 0 -->Spave Vector PWM              if 1 --> Sinusoidal PWM
//Controller Setting
int loops=0;                    //if 0 --> open loop        if 1 --> closed loop
int ctrl_frame=0;               //if 0 -->dq frame          if 1 --> abc frame
int CTRL=0;//(abc only)         //if 0 --> old controller  if 1 --> new controller
int c_outer_loops=0;            //if 0 --> without outer current loop if 1 --> with
int Virtual_Impedance=0;        //if 0 --> without virtual impedance if 1 --> with
int fdroop=0;                   //if 0 --> without frequency droop          if 1 --> with
int V_measure=0;                //if 0 --> L2L measurement          if 1 --> phase measurement
int AMP=0;                      //if 0 --> Amp slowly increase (black start)   if 1 --> ramp
int P_Sharing=1;                //if 0 --> Power sharing  OFF if 1 --> Power sharing  ON
```

```
float Gain_P=1;                 //Proportional gain
float Gain_I2=150.0;            //Integral gain
float Gain_I;
float KI=1.0;                   //Current loop gain
float KC=3.0;                   //Capacitor Current loop gain
float KM=1.0;                   //modulation gain 0.9455
float KV=2.0;                   //Voltage drop due to virtual impedance gain

//Gate Signal Parameter/////////////////////////////////////////////////////////////////
Unsigned int a1=0,B1=0,c1=0,d1=0,e1=0,F1=0,G1=0,H1=0,I1=0;
unsigned int J1=0,K1=0,L1=0,P1=0,P2=0,Q1=0,Q2=0,R1=0,R2=0,S1=0,S2=0;
//Digital Filter Parameter//////////////////////////////////////////////////////////////
float B,A,Vgo=0,Vgmo=0,Igo=0,Igmo=0;
float P1fm=0,P1fo=0,P1fmo=0,Q1fm=0,Q1fo=0,Q1fmo=0;    //LPF level 1 - For Pout
float P2fm=0,P2fo=0,P2fmo=0,Q2fm=0,Q2fo=0,Q2fmo=0;    //LPF level 2 - For Pout
float P3fm=0,P3fo=0,P3fmo=0,Q3fm=0,Q3fo=0,Q3fmo=0;    //LPF level 3 - For Pout
float PX1fm=0,PX1fo=0,PX1fmo=0;                       //LPF level 1 - For Pinv 2
float PX2fm=0,PX2fo=0,PX2fmo=0;                       //LPF 1 - For Pinv 3
float Pld1_1fm=0,Pld1_1fo=0,Pld1_1fmo=0;              //LPF 1 - For Load1 Power
float Pld1_2fm=0,Pld1_2fo=0,Pld1_2fmo=0;              //LPF 2 - For Load1 Power
float Pld1_3fm=0,Pld1_3fo=0,Pld1_3fmo=0;              //LPF 3 - For Load1 Power
float Pld2_1fm=0,Pld2_1fo=0,Pld2_1fmo=0;              //LPF 1 - For Load2 Power
float Pld2_2fm=0,Pld2_2fo=0,Pld2_2fmo=0;              //LPF 2 - For Load2 Power
float Pld2_3fm=0,Pld2_3fo=0,Pld2_3fmo=0;              //LPF 3 - For Load2 Power
float Pld3_1fm=0,Pld3_1fo=0,Pld3_1fmo=0;              //LPF level 1 - For Load3 Power
float Pld3_2fm=0,Pld3_2fo=0,Pld3_2fmo=0;              //LPF level 2 - For Load3 Power
float Pld3_3fm=0,Pld3_3fo=0,Pld3_3fmo=0;              //LPF level 3 - For Load3 Power

//ADC VARIABLES/////////////////////////////////////////////////////////////////////
int Ch4_res,Ch5_res,Ch6_res,Ch7_res,Ch8_res,Ch9_res,Ch10_res; //Channel Resolution
int Ch11_res,Ch12_res,Ch13_res,Ch14_res,Ch15_res;             //Channel Resolution
int k=0; unsigned intGPint_A;

//System Variables
float V_Out_ab1[5],V_Out_bc1[5],V_Out_ca1[5],V_Out_ab,V_Out_bc,V_Out_ca;//Vout
float V_Out_ab_filtered,V_Out_bc_filtered,V_Out_ca_filtered;          //Vout Filtered
float I_Out_a1[5],I_Out_b1[5],I_Out_a,I_Out_b,I_Out_c;               //Iout
float I_Out_a_filtered,I_Out_b_filtered,I_Out_c_filtered;            //Iout Filtered
float I_C_a1[5],I_C_b1[5],I_C_a,I_C_b,I_C_c;                        //Ic
float I_L_a1[5],I_L_b1[5],I_L_a,I_L_b,I_L_c;                        //IL
float I_Other_a1[5],I_Other_b1[5],I_Other_a,I_Other_b,I_Other_c  ;  //Iother
float V_Out_a,V_Out_b,V_Out_c,V_Out_a_Unfiltered;                    //Vout (phase)
float sysmode=0;                                                     //System Mode
float angle;                    //Angle of output voltage for D-Q Transformation
float angle2;                   //Angle of output current for D-Q Transformation
float V_Out_alpha,V_Out_beta;   //Output voltage alpha beta (D-Q Transformation)
float I_Out_alpha,I_Out_beta;   //Output current alpha beta (D-Q Transformation)
float V_Out_mag1,V_Out_mag;     //Output voltage magnitude
float  I_Out_mag1,I_Out_mag;    //Output current magnitude
float P_Average,Q_Average;      //Average Active and Reactive Power
float Vdiff;                    //V_Out_a-V_Ref_a;
float VGdiff;                   //V_Out_a-V_Out_a_Unfiltered;
float alfa=0;                   //Reference Voltage phase angle
float add;                      //Increment in alfa
floatV_Ref_a,V_Ref_b,V_Ref_c;   //Reference Voltage
float V_Ref_mag,V_Ref_mag2=0;   //Gain of Reference Voltage
float Mod_a,Mod_b,Mod_c,Mod_d,Mod_q; //Modulating Signal
float V_Ref_d,V_Ref_q,V_Ref_0;  //D-Q variable of Reference Voltage
```

```
float V_Out_d,V_Out_q,V_Out_0;          //D-Q variable of Output Voltage
float I_Out_d,I_Out_q,I_Out_0;          //D-Q variable of Output Current
float I_C_d,I_C_q,I_C_0;                //D-Q variable of Capacitor Current
float I_L_d,I_L_q,I_L_0;                //D-Q variable of Inductor Current
int     Inverter_Status=0;              //If 1 inverter is ready (max peak)

//////////Control Variables/////////////////////////////////////////////////////////
float VMa,VMb,VMc,VXa,VXb,VXc,VXao=0,VXbo=0,VXco=0,VMao=0,VMbo=0,VMco=0
float VMd,VMq,VM0,VXd,VXq,VX0,VXdo=0,VXqo=0,VX0o=0,VMdo=0,VMqo=0,VM0o=0;
float IAavg,IBavg,ICavg;            //Current average (I_Out_a+I_Other_a)/2;  (same for phase b and c)
float IAdiff,IBdiff;                //IAdiff=IAavg-I_Out_a;  (same for phase b)
float Ictra,Ictrb;
float IAdiffabs,IBdiffabs;          //Absolute current error  IAdiffabs=fabs(IAavg)-fabs(I_Out_a);
float Icheck,mode,mode2;            //check whether the inverter 1 is supplying current or not
float Xfa[3],Xfb[3],Yfa[3],Yfb[3];  //Delay value
float gain=5;                       //Gain for Outer current loop

//Virtual Impedance
float R_Virt=0;                     //Resistance for virtual impedance (Ohm)
float L_Virt=0.005;                 //Inductance for virtual impedance (Henry)
float AlphaX,BetaX,AngleX,MagX,AngleX2,MagX2,X1,X2,V_A,V_B,V_C;
//Space Vector Modulation SVM Parameter//////////
float T11,T12,T10,theta,Valpha,Vbeta,Vm;
unsigned int T1,T2,T0,Tx,i=0,Error=0,n,D=10;//SPWM
unsigned intPha,Phb,Phc,Phd,Ph,Qh;//Synchronizing Variable//////////////////////////////
float log0=0,log1=0,check,check2,maxy=1,Vagreal,maxx[10];

//DATA LOGGING VARIABLE/////////////////////////////////////////////////////
float M_V_Out_ab[500], M_V_Out_bc[500], M_V_Out_ca[500];
float M_V_Out_a[500], M_V_Out_b[500], M_V_Out_c[500];
float M_I_Out_a[500],M_I_Out_b[500],M_I_Out_c[500];
float M_I_C_a[500],M_I_C_b[500],M_I_C_c[500];
float M_Mod_a[500],M_Mod_b[500],M_Mod_c[500];
float M_1[500],M_2[500],M_3[500],M_4[500],M_5[500],M_6[500],M_7[500],M_8[500],M_9[500];

//Communication Variables
float Pmod1=0,Pmod2=0;float comm1=0,comm2=0;
//Input Variables
int Xpin;           //Check whether contactor 2 is opened or closed

//Power Sharing Variables for all inverters
float chk_p1=30.0,chk_p2=20.0,chk_p3=10.0;      //Band for power adjustment(for 125 - 150 V DC)
float adj1=0.1,adj2=0.01,adj3=0.001,adj4=0;     //Adjustment value to alfa (for 125 - 150 V DC)
float PRef,Pdiff,P_limit=-800.0, alfa_change=0;
int CHK,Central_stat;

//Power Sharing Variables for inverter 1 only
float P_Inv1,P_Inv2,P_Inv3,P_SUM;
float Inv1_stat=0,Inv2_stat=0,Inv3_stat=0;
float Ratio=0,Ratio_Inv1=1,Ratio_Inv2=1,Ratio_Inv3=1;
float PRef1,PRef2,PRef3;
float G_Inv2_Ld[3],G_Inv3_Ld[3];
float P_Ld[3],D_ratio2[3],D_ratio3[3],Ld_rat[3];
float PLD1,PLD2,PLD3,Ploss;
//Loop integer
int m=0,n1=1199,n2=0,n3=0,n4=0,j1=0,j2=0,j3=0,j4=0,count=0,count1=0,onn=0;
```

D.2 ADC conversion

```
k=0;
while(k<5)
{ADC0_vStartSingleAutoscan();
GPint_A=0;
Ch4_res=(ADC0_CHSTAT4) & 0x00000fff;Ch5_res=(ADC0_CHSTAT5) & 0x00000fff;
Ch6_res=(ADC0_CHSTAT6) & 0x00000fff;Ch7_res=(ADC0_CHSTAT7) & 0x00000fff;
Ch8_res=(ADC0_CHSTAT8) & 0x00000fff;Ch9_res=(ADC0_CHSTAT9) & 0x00000fff;
Ch10_res=(ADC0_CHSTAT10) & 0x00000fff;Ch11_res=(ADC0_CHSTAT11) & 0x00000fff;
Ch12_res=(ADC0_CHSTAT12) & 0x00000fff;Ch13_res=(ADC0_CHSTAT13) & 0x00000fff;
Ch14_res=(ADC0_CHSTAT14) & 0x00000fff;Ch15_res=(ADC0_CHSTAT15) & 0x00000fff;

//output line to line voltage
V_Out_ab1[k]=(Ch12_res*3.0/4095.0-1.2766678)*375.4285714285714;
V_Out_bc1[k]=(Ch13_res*3.0/4095.0-1.28767)*373.2954545454545;

//Inductor current
I_L_a1[k]=-(Ch5_res*3.0/4095.0-1.225)*9.72972972972973;
I_L_b1[k]=-(Ch6_res*3.0/4095.0-1.3485)*9.473684210526316;

//Output current
I_Out_a1[k]=-(Ch8_res*3.0/4095.0-1.473)*8.726114649681529;
I_Out_b1[k]=-(Ch9_res*3.0/4095.0-1.373)*8.823529411764706;

//Active Power from other inverter
I_Other_a1[k]=(Ch14_res*3.0/4095.0-0.4778)*2144.54214025305;
I_Other_b1[k]=(Ch11_res*3.0/4095.0-0.5255)*1942.50194250194;
k++;}

//Find average value
V_Out_ab=(V_Out_ab1[0]+V_Out_ab1[1]+V_Out_ab1[2]+V_Out_ab1[3]+V_Out_ab1[4])/5.0;
V_Out_bc=(V_Out_bc1[0]+V_Out_bc1[1]+V_Out_bc1[2]+V_Out_bc1[3]+V_Out_bc1[4])/5.0;
I_C_a=(I_C_a1[0]+I_C_a1[1]+I_C_a1[2]+I_C_a1[3]+I_C_a1[4])/5.0;
I_C_b=(I_C_b1[0]+I_C_b1[1]+I_C_b1[2]+I_C_b1[3]+I_C_b1[4])/5.0;
I_Out_a=(I_Out_a1[0]+I_Out_a1[1]+I_Out_a1[2]+I_Out_a1[3]+I_Out_a1[4])/5.0;
I_Out_b=(I_Out_b1[0]+I_Out_b1[1]+I_Out_b1[2]+I_Out_b1[3]+I_Out_b1[4])/5.0;
I_Other_a=(I_Other_a1[0]+I_Other_a1[1]+I_Other_a1[2]+I_Other_a1[3]+I_Other_a1[4])/5.0;
I_Other_b=(I_Other_b1[0]+I_Other_b1[1]+I_Other_b1[2]+I_Other_b1[3]+I_Other_b1[4])/5.0;
I_L_a=(I_L_a1[0]+I_L_a1[1]+I_L_a1[2]+I_L_a1[3]+I_L_a1[4])/5.0;
I_L_b=(I_L_b1[0]+I_L_b1[1]+I_L_b1[2]+I_L_b1[3]+I_L_b1[4])/5.0;

//phase C equations
V_Out_ca=-V_Out_ab-V_Out_bc;I_Out_c=-I_Out_a-I_Out_b;I_L_c=-I_L_a-I_L_b;
I_C_a=I_L_a-I_Out_a;I_C_b=I_L_b-I_Out_b;I_C_c=I_L_c-I_Out_c;
```

D.3 Digital filter

```
V_Out_alpha=(0.333333333)*(2*V_Out_ab-V_Out_bc-V_Out_ca);
V_Out_beta=(0.57735026918)*(V_Out_bc-V_Out_ca);
I_Out_alpha=(0.333333333)*(2*I_Out_a-I_Out_b-I_Out_c);
I_Out_beta=(0.57735026918)*(I_Out_b-I_Out_c);

V_Out_mag1=sqrt(V_Out_alpha*V_Out_alpha+V_Out_beta*V_Out_beta);
angle=atan2(V_Out_beta,V_Out_alpha);
I_Out_mag1=sqrt(I_Out_alpha*I_Out_alpha+I_Out_beta*I_Out_beta);
angle2=atan2(I_Out_beta,I_Out_alpha);
```

```
B=exp(-ff*2.0*pi*15.0);
A=1.0-B;

V_Out_mag=+B*Vgo+A*Vgmo;
Vgo=V_Out_mag; Vgmo=V_Out_mag1;
I_Out_mag=+B*Igo+A*Igmo;
Igo=I_Out_mag; Igmo=I_Out_mag1;
```

D.4 Reference voltage generation

```
///////Amplitude Detection////////////////////////////////////
if (n1==1199)
{ //Loop-001-S
P3_OUT_P4=0;P3_OUT_P6=1;
if (n3<1000)
{ //Loop-002-S Detecting the voltage at point of common coupling (PCC)
Vagreal=V_Out_ab_filtered;
if (maxx[n4]<Vagreal){maxx[n4]=Vagreal;}
else{maxx[n4]=maxx[n4];}
n3++;} //Loop-002-E
else{Vagreal=0;n3=0;n4++;}
if (n4==10)
{maxy=(maxx[0]+maxx[1]+maxx[2]+maxx[3]+maxx[4]+maxx[5]+maxx[6]+maxx[7]+maxx[8]
+maxx[9])/10.0;
n1++;
if (maxy>20){sysmode=1;}
else{sysmode=0;}
if (sysmode==0)
{n1=1202;}
}
}//Loop-001-E

else if (n1==1200)          //phase reset
{P3_OUT_P4=0;P3_OUT_P6=1;
if (bypass_ph_reset==1)
{n1++;}
j2++;

//Zero Crossing detection
log0=V_Out_a_Unfiltered;
if (bypass_v_check==1)
{j2=Zcheck;j4=1;}
if (log0>0 && log0<0.1 && log1<0 && j2>=(Zcheck-5) && j2<=(Zcheck+5))
{
j4++;
if (j4==2)
{alfa=Xalfa-add;check=check+1;n1++;log1=0;log0=0;j1=j2;}
}

if (log0>0 && log0<0.1 && log1<0)
{ j1=j2;j2=0;}
log1=log0;
}
```

```
//frequency synchronization
else if (n1==1201)
{ //Loop-006-S
P3_OUT_P4=0;
P3_OUT_P6=1;
if (bypass_freq_sync==1)
{n1++;}
//Zero Crossing detection
count1++;log0=V_Out_a_Unfiltered;
if (log0>=0 && log0<0.3 && log1<0)
{if (count==500) count=0;
Vdiff=V_Out_a_Unfiltered-V_Ref_a;
M_3[count]=Vdiff;
log1=0;log0=0;alfa=0;count++;n1++;
}
log1=log0;
} //Loop-006-E
else if (n1==1202) //close the contactor
{
if (sysmode==0)
{P3_OUT_P4=1;P3_OUT_P6=1;}
else{P3_OUT_P4=1;P3_OUT_P6=0;}
n1++;
V_Ref_mag2=0;
} //Loop-013-E

alfa=alfa+add;
///////Reset the alfa if it is more than 360 degree/////////
if (alfa>=360)
{alfa=alfa-360;}

////////////Ampitude of the reference voltage////////////////
if (sysmode==0)
{V_Ref_mag=MAG;}
else
{V_Ref_mag=MAG;}
if (n1<=1202)
{V_Ref_mag2=V_Ref_mag;}
else
{ //Loop-014-S       //add delay to slowly increase the amplitude
if (V_Ref_mag2<V_Ref_mag)
{V_Ref_mag2=V_Ref_mag2+(V_Ref_mag)/(4200*delay);}
else
{V_Ref_mag2=V_Ref_mag;Inverter_Status=1;P4_OUT_P2=1;}
} //Loop-014-E
////////Reference Voltage equation////////////
if (AMP==0)
{//Black start
V_Ref_a=(V_Ref_mag2)*sin(alfa*pi/180);
V_Ref_b=(V_Ref_mag2)*sin(alfa*pi/180-2*pi/3);
V_Ref_c=(V_Ref_mag2)*sin(alfa*pi/180+2*pi/3);
}
else
{//Full Amplitude
V_Ref_a=(MAG)*sin(alfa*pi/180);
V_Ref_b=(MAG)*sin(alfa*pi/180-2*pi/3);
V_Ref_c=(MAG)*sin(alfa*pi/180+2*pi/3);
}
```

D.5 Central Controller - P Ref Calculation

```
Central_stat=1;
Xpin=(IO_ubReadPin(IO_P8_5)||IO_ubReadPin(IO_P8_7));//Checking contactor B stat
G_Inv2_Ld[0]=1;G_Inv2_Ld[1]=0.5;G_Inv2_Ld[2]=0.25;G_Inv3_Ld[0]=0.25;G_Inv3_Ld[1]=0.3333;
G_Inv3_Ld[2]=1;P_Ld[0]=Pld1_3fo*3;P_Ld[1]=Pld2_3fo*3;P_Ld[2]=Pld3_3fo*3;
if (P_Ld[0]<=10)
{P_Ld[0]=1.0;}
if (P_Ld[1]<=10)
{P_Ld[1]=1.0;}
if (P_Ld[2]<=10)
{P_Ld[2]=1.0;}

D_ratio2[0]=G_Inv2_Ld[0]/(G_Inv2_Ld[0]+G_Inv3_Ld[0]);
D_ratio2[1]=G_Inv2_Ld[1]/(G_Inv2_Ld[1]+G_Inv3_Ld[1]);
D_ratio2[2]=G_Inv2_Ld[2]/(G_Inv2_Ld[2]+G_Inv3_Ld[2]);
D_ratio3[0]=G_Inv3_Ld[0]/(G_Inv2_Ld[0]+G_Inv3_Ld[0]);
D_ratio3[1]=G_Inv3_Ld[1]/(G_Inv2_Ld[1]+G_Inv3_Ld[1]);
D_ratio3[2]=G_Inv3_Ld[2]/(G_Inv2_Ld[2]+G_Inv3_Ld[2]);
Ld_rat[0]=P_Ld[0]/(P_Ld[0]+P_Ld[1]+P_Ld[2]);
Ld_rat[1]=P_Ld[1]/(P_Ld[0]+P_Ld[1]+P_Ld[2]);
Ld_rat[2]=P_Ld[2]/(P_Ld[0]+P_Ld[1]+P_Ld[2]);
Ratio_Inv2=D_ratio2[0]*Ld_rat[0]+D_ratio2[1]*Ld_rat[1]+D_ratio2[2]*Ld_rat[2];
Ratio_Inv3=D_ratio3[0]*Ld_rat[0]+D_ratio3[1]*Ld_rat[1]+D_ratio3[2]*Ld_rat[2];

if (IO_ubReadPin(IO_P8_3)==1)
{Ratio_Inv1=1;Ratio_Inv2=1;Ratio_Inv3=1;}
else
{Ratio_Inv1=1;}
if (Xpin==0 || Inverter_Status==0 )
{P_Inv1=-960.0;}
else
{P_Inv1=P3fo;}
P_Inv2=PX1fo;              //Active Power from Inverter 2
P_Inv3=PX2fo;              //Active Power from Inverter 3
Ratio=0;
P_SUM=0;
if (P_Inv1 >P_limit)
{Inv1_stat=1;P3_OUT_P0=1;P_SUM=P_SUM+P_Inv1;Ratio=Ratio+Ratio_Inv1;}
else{Inv1_stat=0;P3_OUT_P0=0;}
if (P_Inv2 >P_limit)
{Inv2_stat=1;P3_OUT_P2=1;P_SUM=P_SUM+P_Inv2;Ratio=Ratio+Ratio_Inv2;}
else{Inv2_stat=0;P3_OUT_P2=0;}
if (P_Inv3 >P_limit)
{Inv3_stat=1;P3_OUT_P8=1;P_SUM=P_SUM+P_Inv3;Ratio=Ratio+Ratio_Inv3;}
else{Inv3_stat=0;P3_OUT_P8=0;}
if (Inv1_stat==1)
{PRef1=Ratio_Inv1/Ratio*P_SUM;}
else{PRef1=0;}
if (Inv2_stat==1)
{PRef2=Ratio_Inv2/Ratio*P_SUM;}
else{PRef2=0;}
if (Inv3_stat==1)
{PRef3=Ratio_Inv3/Ratio*P_SUM;}
else{PRef3=0;}

Ploss=P_SUM-(P_Ld[0]+P_Ld[1]+P_Ld[2]);
```

D.6 Power sharing

```
if (P_Sharing==1 &&Inverter_Status==1 &&Xpin==1 &&Central_stat==1)
{
P2_OUT_P11=1;
PRef=PRef1;                 //For inverter 1 only
//PRef=PX1fo;               //For inverter 2 and inverter 3
Pdiff=PRef-P3fo;
if (alfa>40 &&alfa<50)
{CHK=0;}
if (alfa>130 &&alfa<140)
{CHK=0;}
if (alfa>220 &&alfa<230)
{CHK=0;}
if (alfa>220 &&alfa<230)
{CHK=0;}
if (alfa>310 &&alfa<320)
{CHK=0;}

if ((alfa>=30&&alfa<(30+add))||(alfa>=120&&alfa<(120+add))||(alfa>=210&&alfa<(210+add))
||(alfa>=300&&alfa<(300+add))&&(CHK==0))
{
if(Pdiff<=(-chk_p1)){alfa=alfa-adj1;alfa_change=alfa_change-adj1;CHK=1;}
if(Pdiff>(-chk_p1)&&Pdiff<=(-chk_p2))
{alfa=alfa-adj2;alfa_change=alfa_change-adj2;CHK=1;}
if(Pdiff>(-chk_p2)&&Pdiff<=(-chk_p3))
{alfa=alfa-adj3;alfa_change=alfa_change-adj3;CHK=1;}
if(Pdiff>(-chk_p3)&&Pdiff<=(chk_p3))
{alfa=alfa+adj4;alfa_change=alfa_change+adj4;CHK=1;}
if(Pdiff>(chk_p3)&&Pdiff<=(chk_p2))
{alfa=alfa+adj3;alfa_change=alfa_change+adj3;CHK=1;}
if(Pdiff>(chk_p2)&&Pdiff<=(chk_p1))
{alfa=alfa+adj2;alfa_change=alfa_change+adj2;CHK=1;}

if(Pdiff>(chk_p1))
{alfa=alfa+adj1;alfa_change=alfa_change+adj1;CHK=1;}
}
}
else
{P2_OUT_P11=0;}
```

D.7 Voltage controller

```
VXa=V_Ref_a-V_Out_a;
VXb=V_Ref_b-V_Out_b;
VXc=V_Ref_c-V_Out_c;

if (Gain_I<Gain_I2)
{Gain_I=Gain_I+(Gain_I2)/(4200*5);}
else
{Gain_I=Gain_I2;}

VMa=VMao+(ff/2.0)*(VXao+VXa)*Gain_I;VMb=VMbo+(ff/2.0)*(VXbo+VXb)*Gain_I;
VMao=VMa;VXao=VXa;VMbo=VMb;VXbo=VXb;
```

```
if (CTRL==0)
{//Controller (without IL)
Mod_a=VMa+Gain_P*VXa-I_C_a+V_Out_a;
Mod_b=VMb+Gain_P*VXb-I_C_b+V_Out_b;
Mod_c=-Mod_a-Mod_b;}
else
{//Controller (with IL)
Mod_a=((VMa+Gain_P*VXa-I_L_a)*KI-(I_C_a*KC)+V_Out_a)*KM;
Mod_b=((VMb+Gain_P*VXb-I_L_b)*KI-(I_C_b*KC)+V_Out_b)*KM;
Mod_c=-Mod_a-Mod_b;}

//Voltage control in dq frame
VXd=V_Ref_d-V_Out_d; VXq=V_Ref_q-V_Out_q;
VMd=VMdo+(ff/2.0)*(VXdo+VXd)*Gain_I;VMq=VMqo+(ff/2.0)*(VXqo+VXq)*Gain_I;
VMdo=VMd;VXdo=VXd;VMqo=VMq;VXqo=VXq;
if (CTRL==0)
{Mod_d=VMd+Gain_P*VXd-1.0*I_Out_d+V_Out_d;Mod_q=VMq+Gain_P*VXq-
1.0*I_Out_q+V_Out_q;}
else
{Mod_d=((VMd+Gain_P*VXd-I_L_d)*KI-(I_C_d*KC)+V_Out_d)*KM;
Mod_q=((VMq+Gain_P*VXq-I_L_q)*KI-(I_C_q*KC)+V_Out_q)*KM;}

if (ctrl_frame==0)
{Mod_a=Mod_d*sin(alfa*pi/180.0)+Mod_q*cos(alfa*pi/180.0);
Mod_b=Mod_d*sin(alfa*pi/180.0-2.0*pi/3.0)+Mod_q*cos(alfa*pi/180.0-2.0*pi/3.0);
Mod_c=Mod_d*sin(alfa*pi/180+2*pi/3)+Mod_q*cos(alfa*pi/180+2*pi/3);}
```

D.8 Current sharing

```
//check whether the inverter 1 is supplying current or not
if (n2<1200)
{
if (Icheck<I_Out_a)
{Icheck=I_Out_a;}
else{Icheck=Icheck;}
n2++;
}
else{if (Icheck>0.3){mode=1;}
else{mode=0;}
Icheck=0;
n2=0;}
//Find average current
IAavg=(I_Out_a+I_Other_a)/2.0;IBavg=(I_Out_b+I_Other_b)/2.0;

//Current error
IAdiff=IAavg-I_Out_a;IBdiff=IBavg-I_Out_b;

//Absolute current error
IAdiffabs=fabs(IAavg)-fabs(I_Out_a);IBdiffabs=fabs(IBavg)-fabs(I_Out_b);

Xfa[2]=Xfa[1];Xfa[1]=Xfa[0];Xfa[0]=gain*IAdiff;
Xfb[2]=Xfb[1];Xfb[1]=Xfb[0];Xfb[0]=gain*IBdiff;
Ictra=0.3313*Xfa[1]-0.1194*Xfa[2]+0.7881*Yfa[1]+3.598e-11*Yfa[2];
Ictrb=0.3313*Xfb[1]-0.1194*Xfb[2]+0.7881*Yfb[1]+3.598e-11*Yfb[2];
Yfa[2]=Yfa[1];Yfa[1]=Yfa[0];Yfa[0]=Ictra;
Yfb[2]=Yfb[1];Yfb[1]=Yfb[0];Yfb[0]=Ictrb;
```

```
//Close Loop with current sharing loop
if (c_outer_loops==0)
{Mod_a=Mod_a;
Mod_b=Mod_b;
Mod_c=-Mod_a-Mod_b;}
else
{Mod_a=Mod_a+Yfa[0];
Mod_b=Mod_b+Yfb[0];
Mod_c=-Mod_a-Mod_b;}
```

D.9 SPWM

```
Pha=(int)((Half_Tz-D)*(1+(Mod_a/VDC*2))/2);
Phb=(int)((Half_Tz-D)*(1+(Mod_b/VDC*2))/2);
Phc=(int)((Half_Tz-D)*(1+(Mod_c/VDC*2))/2);
Phd=(int)((Half_Tz-D)*(1+(0/VDC*2))/2);
a1=Half_Tz-Pha;B1=Half_Tz+Pha;c1=Half_Tz-Phb;d1=Half_Tz+Phb;
e1=Half_Tz-Phc;F1=Half_Tz+Phc;R1=Half_Tz-Phd;R2=Half_Tz+Phd;
G1=Half_Tz-Pha-D;H1=Half_Tz+Pha+D;I1=Half_Tz-Phb-D;J1=Half_Tz+Phb+D;
K1=Half_Tz-Phc-D;L1=Half_Tz+Phc+D;S1=Half_Tz-Phd-D;S2=Half_Tz+Phd+D;
```

Appendix E

List of Tables and Figures

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Chapter 3 AC Power Flow Analysis and Circulating Current among Parallel Connected Inverters

Chapter 4 Improved Instantaneous Average Current Sharing (IACS) Control

Chapter 6 Optimized Operation of Inverter Based Distributed Generation in Rural Islanded Microgrid

Appendix F

Summary of Relevant Published Research by the Author

[1] A. M. Roslan, K. H. Ahmed, S. J. Finney, and B. W. Williams, " Improved instantaneous average current sharing control scheme for inverter parallel operation in microgrid," in *Microgeneration and Related Technologies (MICRoGEN'II), 2011 2nd International Conference on*, 2011.

Abstract

An improved instantaneous average current sharing control scheme for parallel connected inverters taking into account the effect of line impedance is presented. The system presented here consists of two single phase inverters connected in parallel. This control technique requires interconnections among inverters for information sharing. The improvement is based on the adaptive gain scheduling technique that varies the controller's parameters. The simulation results show that the adaptive gain scheduling approaches introduced improves the performance of conventional controller in term of current and power sharing between inverters under difference line impedance condition.

[2] A. M. Roslan, K. H. Ahmed, S. J. Finney, and B. W. Williams, "Improved Instantaneous Average Current-Sharing Control Scheme for Parallel-Connected Inverter Considering Line Impedance Impact in Microgrid Networks," *Power Electronics, IEEE Transactions on*, vol. 26, pp. 702-716, 2011.

Abstract

A new control scheme for parallel-connected inverters taking into account the effect of line impedance is presented. The system presented here consists of two single-phase inverters connected in parallel. The control technique is based on instantaneous average current-sharing control that requires interconnections among

inverters for information sharing. A generalized model of a single-phase parallel-connected inverter system is derived. The model incorporates the detail of the control loops that use a proportional-resonant controller, but not the switching action. The voltage- and current-controller design and parameters selection process are discussed. Adaptive gain scheduling is introduced to the controller to improve the current and power sharing for a condition, where the line impedance is different among the inverters. The simulation results show that the adaptive gain-scheduling approaches introduced improve the performance of conventional controller in terms of current and power sharing between inverters under difference line impedance condition. The experiments validate the proposed system performance.

[3] M. Azrik, K. H. Ahmed, S. J. Finney, and B. W. Williams, "Voltage synchronization scheme based on zero crossing detection for parallel connected inverters in AC microgrids," in *Industrial Electronics (ISIE), 2012 IEEE International Symposium on*, 2012, pp. 588-593.

Abstract

A new voltage synchronization scheme is proposed for parallel connected inverters in AC microgrids. Instead of using the same reference voltage for all inverters, this scheme directly synchronizes the reference voltage of a connecting inverter to the point of common coupling voltage. Two contactors are used with each inverter module to enable the inverter to operate in 4 different modes. Voltage synchronization using this scheme requires no control interconnection among parallel connected inverters. Experimental results validate the practicality of the proposed synchronization schemes.