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Design and Implementation of Wireless Data Acquisition System for Measurements in High Voltage Substations

by

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Declaration

I, Yu Wang, hereby declare that this work has not been submitted for any other degree at this university or any other institution and that, except where reference is made to the work of other authors, the material presented is original.

Copyright statement

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Abstract

This thesis reports a R&D project of development and implementation of "Wireless Digital EMI measurement System". This system is developed to replace presently-used "Fibre Analogue EMI Measurement System" and acquire the fast transient EMI signal in substations.

This system is a typical "distributed field data acquisition system". The front-ends of this system are several "Remote Acquisition Units" (RAU). The background (or back-end) of this system is a PC. A point-to-multipoint wireless local area network is used to connect RAUs and PC.

The RAU is placed in substations with a sensor together and controlled by a remote PC. The RAU performs 80MSPS sampling rate, has 512kB memory and trigger capability. It captures the fast transient EMI signal, stores the data in its memory and sends the data to remote PC. Because general purpose acquisition products (such as DSO) are not suitable for this application, the RAU had to be implemented through a board-level design, i.e. using components and custom designed PCBs to build the RAU. In this board-level design, ADC, memory and a CPLD were employed to build the high-speed acquisition circuit, a micro-controller was applied for control and communication functions.

The wireless communication network is a bi-directional network, which transmits the data from RAUs to PC and vice versa. This communication network is based on Bluetooth wireless modems.

The PC is the background of this system, which provides a Man-Machine Interface to users. The application software is written in Assembly language.

The "Wireless Digital EMI measurement system" has been fully tested in the laboratory and some measurements were made in a substation. The tests and measurements showed that the system can significantly increase the efficiency of EMI measurement in substations or of emissions from large systems. Furthermore the acquisition circuit in this system can be produced as an individual product for other diverse applications. Intellectual Protection is being sought in the latter case.

CONTENTS

Abbreviations and Acronyms

AC:	Alternating Current
A/D:	Analogue to Digital, or Analogue to Digital Converter
ADC:	Analogue to Digital Converter
AIS:	Air Insulated Substation
ALE:	Address Latch Enable
AM:	Amplitude Modulation
ARQ:	Automatic Repeat Request
ASCII:	American Standard Code for Information Interchange
ASIC:	Application Specific Integrated Circuit
AT:	American Telecommunication
BGA:	Ball Grade Array
BNC:	A kind of connector for coaxial cable
CLK:	Clock
CT:	Current Transformer
CQDDR:	Channel Quality Driven Data Rate
CPLD:	Complex Programmable Logic Device
CTS:	Clear To Send
CMOS:	Complementary Metal-Oxide Semiconductor
DC:	Direct Current
DSO:	Digital Storage Oscilloscope
E-Field:	Electronic Field
ECL:	Emitter Coupling Logic
ETSI:	Europe Telecommunication Standard Institute
EIA:	Electronic Industry Association
EMC:	Electromagnetic Compatibility
EMI:	Electromagnetic Interference
ERC:	Europe Radio Committee
ESD:	Electrostatic Discharge
FCC:	Federal Communication Commission
FCC:	Forward Correction Code
FCE:	Forward Correction Encoding
FM:	Frequency Modulation

FPGA:	Field Programmable Gate Array
GAL:	Gate Array Logic
GIS:	Gas Insulated Substation
GSM:	Globe Service of Mobile
GUI:	Graphic User Interface
H-Field:	Magnetic Field
I/O:	Input/Output port
ISM:	Industry, Science and Medicine
IEC:	International Electronic Communication
IEEE:	Institute of Electronic and Electrical Engineer
ISA:	Industrial Standard Association
LAN:	Local Area Network
MCU:	Micro Controller Unit
OE:	Output Enable
PAL:	Programmable Array Logic
PCB:	Printed Circuit Board
PCI:	Peripheral Components Interconnection
PLD:	Programmable Logic Device
PM:	Phase Modulation
RAM:	Random Access Memory
RAU:	Remote Acquisition Unit
RD:	Read
RF:	Radio Frequency
RS-232:	An EIA standard for series data communication, based on unbalance signal transmission.
RS-422:	An EIA standard for series data communication, based on differential signal transmission.
RTS:	Request To Send
SPS:	Samples Per Second
SMA:	Surface Mounted Assembly
SRAM:	Static RAM
SST:	Spread Spectrum Technology
TQFP:	Thin Plastic Quad Flat Package
TTL:	Transistor-Transistor Logic

UART:	Universal Asynchronous Receiver and Transmitter
VLDS:	Very Low Voltage Deferential Signalling
VT:	Voltage Transformer
VQFP:	Very fine Quad Flat Package
WLAN:	Wireless Local Area Network
WR:	Write

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Chapter 1 Introduction

This Ph.D project is a "Research and Development" (R&D) work to design and implement a prototype "Wireless Digital Measurement System". This system is a typical "Distributed Field Data Acquisition System", which is used for the EMI measurement in substations replacing presently-used "Fibre Analogue Measurement System".

This thesis addresses four issues:

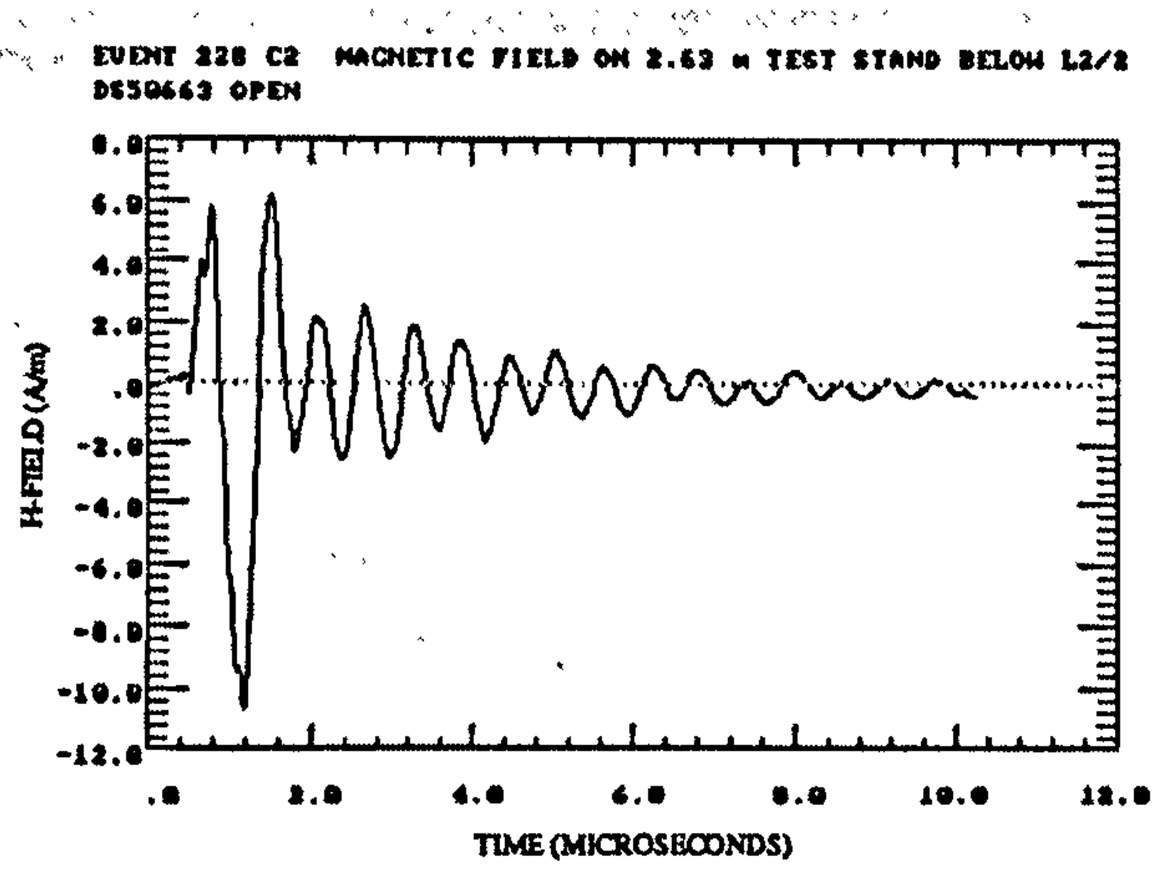
1) Briefly introduces EMI measurement in substation. Explain the application of the newly-developed measurement system.
2) Reports the research and development work on the newly-developed system.
3) Studies the principles of this system and give the details of the design.
4) Gives a reference to users who will use this new system and designers who will upgrade the new system in the future.

Among them, (2) and (3) are the main goals of this thesis and form the bulk of the thesis.

1.1 The proposal of this project

EMI stands for Electro-Magnetic Interference. In substations, EMI arises from any electrical current or voltage discontinuity, such as switching operations in switchyard [1]. In substations, when the switches, such as circuit breakers or disconnectors, are opening or closing, they cause significant electrical discharges and electrical emissions. For the switches in substation, which usually interrupt huge current, the electrical emissions are considerable. These emissions will cause EMI signals, which can interfere with electronic equipment over the air or through cables. EMI measurement in a substation is conducted to record the EMI signals and characterize the EMI immunity level of that substation.

The high frequency EMI signal is a transient signal. Depending on the duration of the discharge, the radiated EMI signal usually lasts several milliseconds to one second.



Magnetic Field at h = 2.63 m above Ground under Outer Phase

Fig. 1.1: Radiated EMI signal in an air-insulated switchyard

The interval of switching events in a switchyard is usually tens of minutes to several days. The EMI signals, according to their medias, are classified into Radiated EMI and Conducted EMI. Fig.1.1 shows a typical example of the radiated magnetic-field (H-field) EMI signals recorded in a switchyard [2].

Nowadays, the radiated EMI measurement campaigns in substations (such as in the UK) are typically based on high frequency three-axis electric (E) and magnetic (H) field sensors linked via optical fibres to large memory digital recording scopes [3].

Fig.1.2 shows the typical fibre-based radiated EMI measurement system.

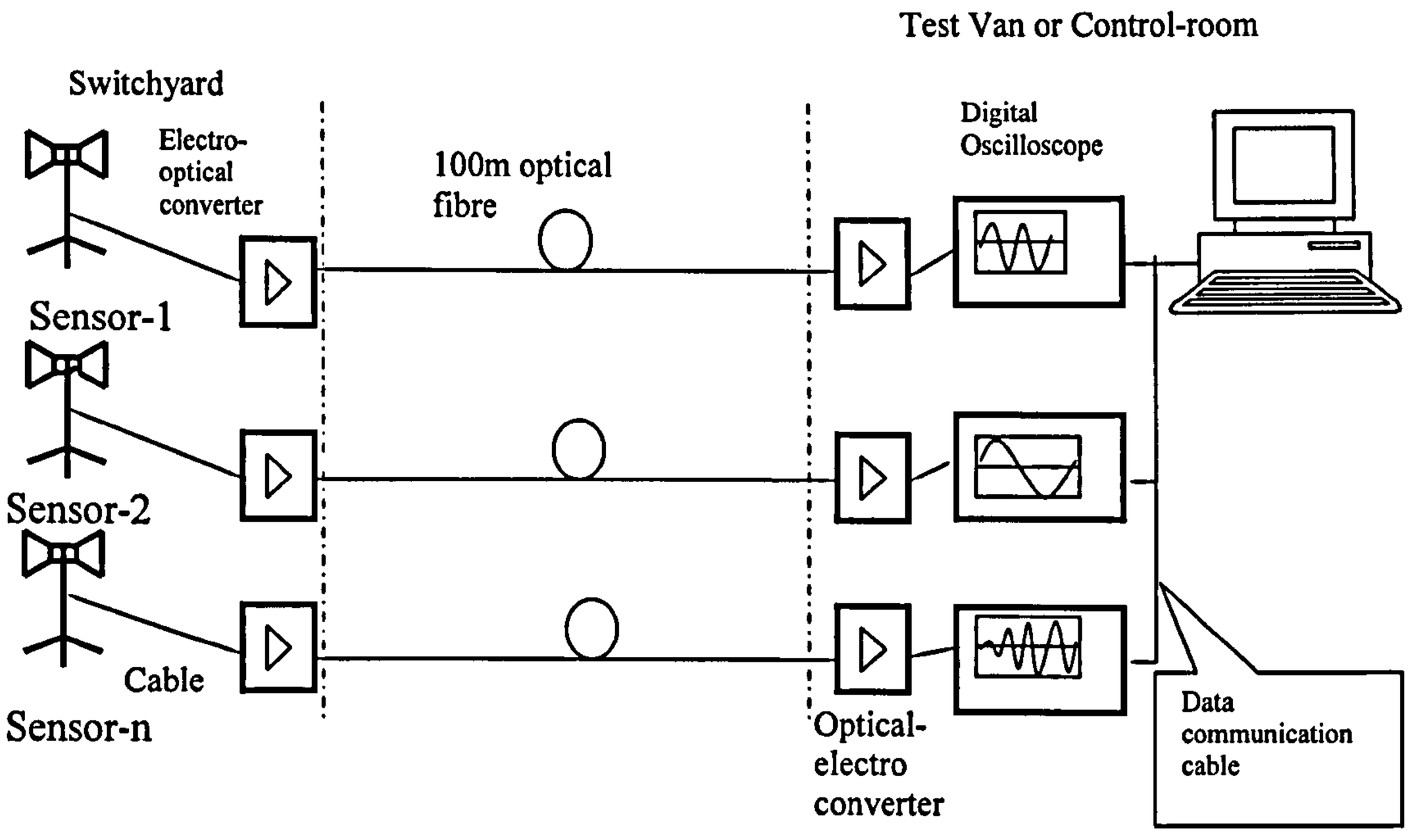


Fig. 1.2: Typical present radiated EMI measurement system in substation

Sensors 1~ n are placed in the switchyard, PC and DSOs are placed in test bench (Test Van or Control Room). They are linked with 100 meters optical fibre.

The brief operating mechanism is summarised as below:

In this measurement system, the analogue electrical signals output from the sensors are converted into optical signal by electro-optical converters. The optical signals are transmitted over 100 meters optical fibre to the test-van or relay room. The optical signals are re-converted into electrical signals at the other end, and the electrical signals are then input to digital oscilloscopes. The digital oscilloscopes work on a single-trigger mode[1] to capture the transient EMI signal. Once a switching action happens, the EMI signal triggers all the oscilloscopes. They will record the EMI signals in their local memories. The recorded data, which contain the information of the waveform of the EMI signal, can then be downloaded to a computer through

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[1] In single-trigger mode, when the acquisition starts and the trigger condition becomes true, the waveform is updated once only and the acquisition stops. The waveform will be kept in the screen and memory of the oscilloscope, until the triggered situation is released and new acquisition is enabled [106].

GPIB cables or other links. These data are the raw output of the measurement. The data then can be displayed and analysed on or off the measurement site using other software, such as FFT (Fast Fourier Transform) processing software. For the details of the operation mechanism of this system, please see [1, 4].

In the field of the switchyard, where sensors are placed, the EMC environment is extremely harsh. Measurement equipments, such as PC and DSO, cannot work well there. The test equipment has to be housed within a shielded test-van or control room, which are situated away from the source and may be separated from sensors for tens of meters. Since analogue signals must be transmitted in real time, the transmission of the EMI signal cannot avoid the moment when EMI signal happens. If a long cable were applied to transmit the analogue EMI signal from sensor to oscilloscope, the cable could couple significant EMI signal and add the interference to the pure EMI signal, i.e. sensors output. Thus, optical fibre is chosen as the medium to transmit the analogue signal. This removes the risk of corruption of the signal being transmitted [4]. Fig1.3, Fig.1.4 and Fig1.5 give a real example of this fiber-based measurement system.

Fig. 1.3 shows 4 sensors placed in a switchyard. The nearest one with a tripod is the high-frequency H-field sensor. The two with red pedestals are high-frequency E-field sensors and the dish-shaped one in the background is the low-frequency E-field sensor.

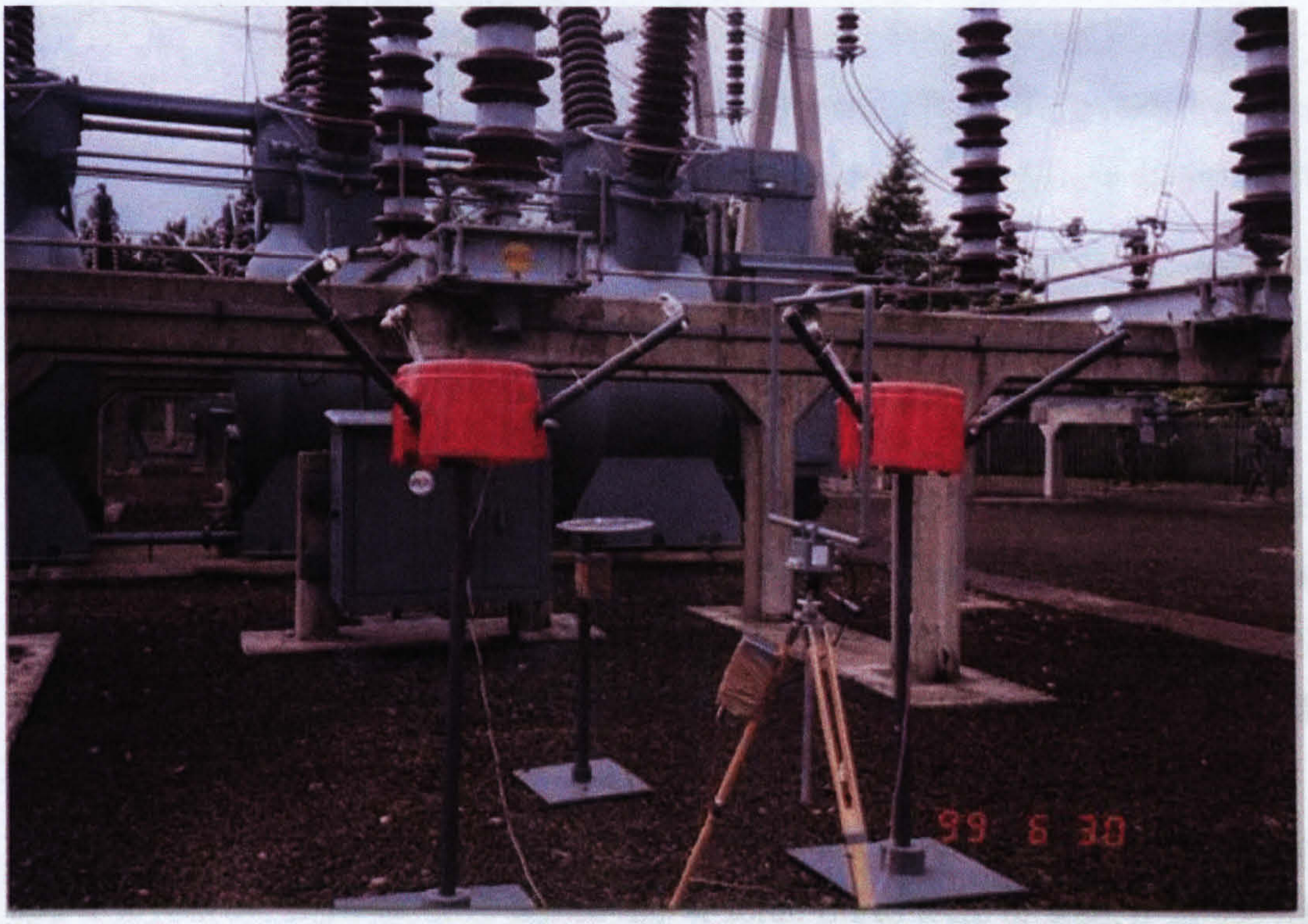

Fig. 1.3: 4 Sensors in the field of switch-yard

Fig.1.4 shows the test-van stopped away from the source. It obtains AC 240V power supply from a petrol generator.

Fig. 1.4: Test-van in a substation

Fig. 1.5: Inside of the test van

Fig.1.5 shows the measurement equipment inside the test-van. There are several DSOs and some optical-electrical converters in the picture.

This system has been used for years. As it uses optical fibre to transmit analogue signal, it is named as "Fibre Analogue Measurement System". The downside of this system is that optical fibres are difficult to lay out and easily broken. Since the EMI measurement system is temporarily installed in the substation only when the measurement is being carried out, there are no permanent stands or trenches to accommodate the fibre in substations. Each time, before measurements were taken, operators had to spend a day to layout the fibre network and set up. If some fibres were broken, it would take further time to replace them. Thus, to solve this "fibre" problem, a new system was proposed. That is "Wireless linked Measurement System", which uses wireless to link the sensors and the PC, giving operators the most flexibility. Fig.1.6 shows the configuration of this wireless system.

1.2 The digital wireless solution

The EMI signal to be transmitted has up to 10MHz frequency components. It is well known that to transmit an analogue signal, the RF carrier should have much wider bandwidth. Obviously, it is impossible to apply a dedicated wide RF bandwidth for this engineering. Thus, this wireless link has to be built in a "license-free" band. In the "license-free" band, there isn't any existing wireless product with such wide bandwidth. Also wireless transmission is more susceptive to the EMI compared with a cable. Therefore, wireless channels cannot carry the real-time analogue signal and so a digital transmission solution is considered. The EMI signal is a transient signal, which usually has just several milliseconds duration and only arises from the switching operation. The interval of switching actions in a switchyard is usually several days in normal situation and tens of minutes during maintenance work or measurement work. In other words, during the interval, only several milliseconds

signal needs to be transmitted from the front-end to PC over the wireless channel. A digital system can achieve this transmission with a narrow bandwidth carrier but takes a long time as outlined below.

This solution uses a Remote Acquisition Unit (RAU) in the front end (close to sensors) to digitise the analogue signal and capture the significant transient EMI signal, record it in its memory. The recorded data can then be transmitted to PC over the wireless link at anytime.

In substations, apart from the moment of switching action, the EMI environment is fairly quiet and suitable for wireless data communication. Unlike the analogue signal, the digital signal need not be transmitted at real-time. Because the digital EMI signal has been captured and stored in the memory, the data can be transmitted at any time and the transmission can be at a slow rate, which requires a narrow bandwidth of the carrier. That is to say, by the advantage of digital technology, the wireless data communication can take longer time and narrower bandwidth to transmit an analogue signal having shorter period and wider bandwidth. Furthermore, modern wireless data communication technology can employ data protection strategy, such as FCC (Forward Correction Code) and ARQ (Automatic Repeat Request). This ensures the integration and correctness of the communicated data. Fig.1.6 shows the block diagram of the Wireless Digital Measurement System.

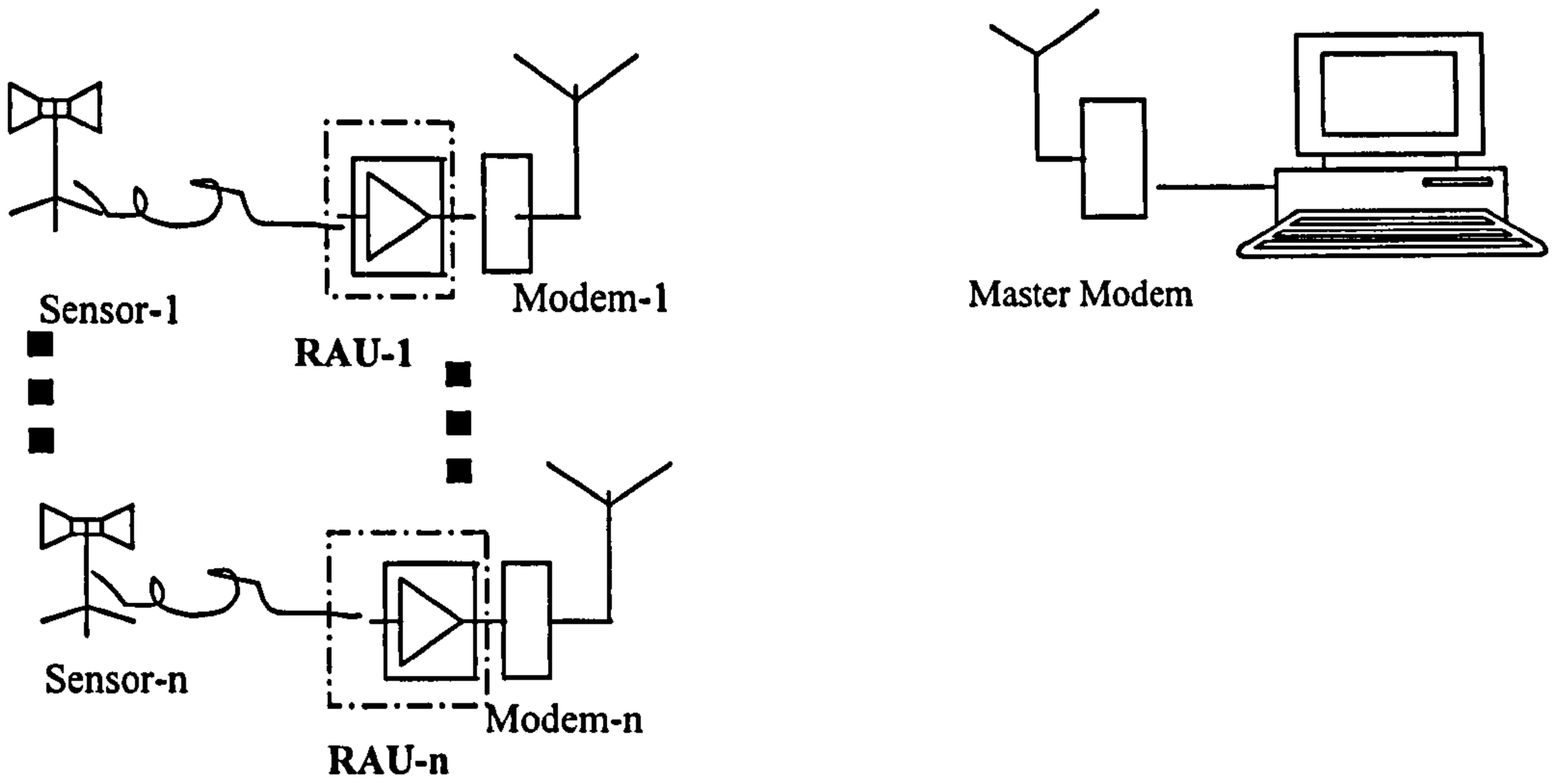

Fig. 1.6: Block diagram of wireless digital measurement system

In Fig.1.6, RAU (Remote Acquisition Unit) is placed in the front end near the sensor to capture the EMI signal. It is controlled by PC from a remote place over a point-to-multipoint wireless network.

Because the newly-developed measurement system uses a wireless channel to transmit a digital signal, it is named as "Wireless Digital Measurement System" or "Wireless Data Acquisition System". Comparing with the currently-used Fibre Analogue Measurement System, shown in Fig.1.2, it can be seen that, in wireless digital measurement system, DSOs have been removed. The acquisition functions of DSO are fulfilled by RAU and the display and control function of DSO are fulfilled by PC. Operators can use the PC to control RAUs and download data from them just like controlling a remote DSO. For this reason, RAU can be regarded as a "wireless oscilloscope".

In this system, RAU is designed to acquire the signal and communicate with the PC through the wireless network. To realise the communication function, RAU needs an intelligent unit, such as computer or an embedded CPU. To acquire the signal, RAU needs an acquisition unit. Obviously, RAU should consist of two parts—

communication unit and acquisition unit. Based on this structure, there are three RAU solutions that can be considered:

1) DSO solution: This design uses a DSO and a PC with the DSO's application software building the RAU. By implementing the DSO's application software and a PC-to-PC wireless communication network, the local PC (at RAU) can obtain the data of the measured signal and send the data to remote PC (at test-van or control room).

2) Industrial PC solution: It uses an industrial PC with an acquisition card building the RAU to acquire the signal and communicate with remote PC.

3) Board-level solution: Using a custom acquisition circuit and embedded CPU with custom software to obtain the data and communicate with remote PC.

DSO solution and industrial PC solution would make the RAU physically bulky and costly (This project addresses a cost-effective solution). They also need a large power supply, which is not suitable for a battery-based device (There is not always available power supply in switchyard). Thus, DSO and industrial computer are not suitable for the RAU in this system. RAU design took the "Board-level" solution. Board-level solution means using custom PCBs and general components to build the RAU. It reduces the cost, physical size and power supply, but makes the development complicated. However, this is the best choice for this project.

In the RAU, a custom acquisition circuit is responsible for data acquisition function and an embedded CPU is responsible for the communication function. There are two acquisition modes for this custom acquisition circuit design—software mode and hardware mode. Software mode is using a CPU to input data from an ADC (Analogue to Digital Converter) directly and store the data into its memory. This CPU also implements the trigger function. Obviously, all of this process is implemented by a program and its speed is limited. Software mode has a simple circuit but can achieve a lower sampling rate than hardware mode. Practically, software mode cannot achieve a sampling speed more than 20MSPS. In this system, the desired sampling rate is 80MSPS. It has to be implemented by hardware mode. Hardware mode is using logic circuits to manage the conversion and storage processing, as well as the trigger function. Based on the components available

commercially, hardware mode can achieve the sampling speed as high as several giga samples per second. Most fast acquisition devices use hardware mode, such as DSO and computer based acquisition cards. According to the requirements of the project, the RAU is built by a board-level design using a hardware mode. This design achieve 80MSPS sampling rate with 512K memory size. The downside of hardware mode is the complexity of its circuit configuration. Fig.1.7 shows the assembled RAU. In chapter 3, Fig. 3-1 shows the configuration of the RAU.

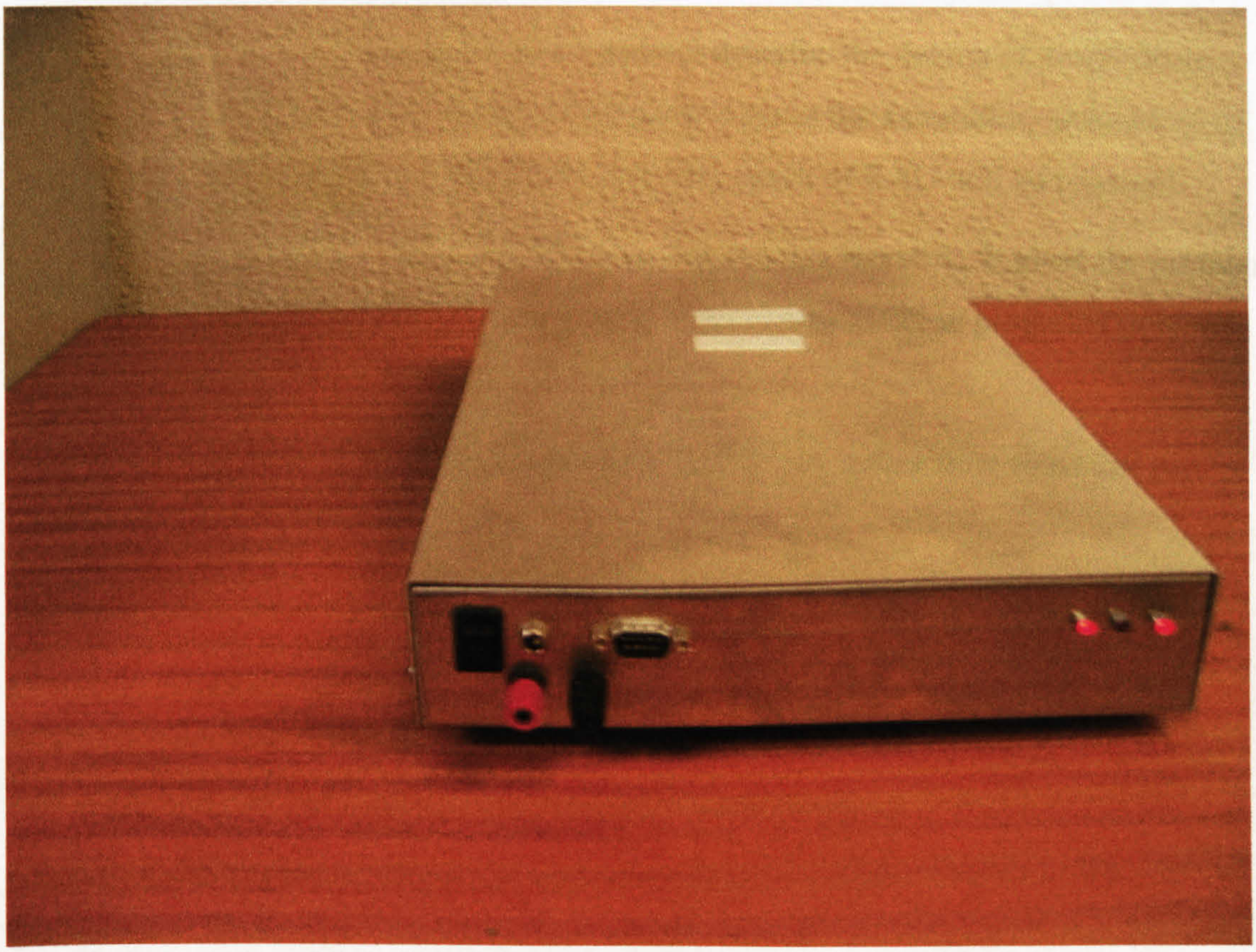

Fig. 1.7: Picture the of RAU

1.3 Overview of this thesis

This thesis is organised along the sequence of the development work.

Chapter 2 is devoted to a literature review. The materials to be reviewed in this chapter are in three aspects. First of all, as background to the application of the Wireless Digital Measurement System, the EMI measurement campaign in

substations is introduced. Secondly, the existing data acquisition equipment is reviewed, which have a similar function to RAU. Finally, some key techniques to be taken in this project are reviewed, such as CPLD technique and Bluetooth technique. Additionally, the solution of this project is explained.

Chapter 3 presents the system design. The structure of the whole system is given as well as the arrangement of research and development works. Also the principle and the functional design of the acquisition part are descript in Chapter 3.

Chapter 4 describes RAU. Section 4.1 and 4.2 describe the details of Acquisition Board and CPU Board. Section 4.3 of chapter 4 gives the assembling instruction of the RAU box. In section 4.4 the commissioning result of RAU will be reported.

Chapter 5 describes the Wireless Data Communication Network. It gives the protocol of this communication network and explains the communication programs in both the RAU side and the PC side.

Chapter 6 describes the control software in the PC side with a flow chart and its explanations.

Chapter 7 reports the test results of the newly-developed system. These tests were made in the laboratory and at substation.

At the end of the thesis, Chapter 8 concludes this project and gives some recommendations for future development.

1.4 Summary of this project

The development in this project includes high-speed digital and analogue circuit design, software and hardware design for a microprocessor, logic design for PLD, software design for PC and design of a communication system.

According to Joseph A. Schumpeter, the Austrian-American economist, innovation is a new combination of existing elements and conditions of production [6]. Another economist Ian. M. Rose has pointed out that since the 1930's, more R&D practices are aimed at innovations but not inventions [7]. As with most R&D practices in the electronics field, this project creates a new product by novel combination of existing

technologies and components. Therefore, it can be regarded as an innovation, which is an original work and produced two new products:

1) The Wireless EMI Measurement System that can be applied in EMI measurement in substations replacing presently-used Fibre Analogue system and solve the "fibre problem".

2) The Acquisition Board in RAU has an interface compatible with most 8-bit embedded CPU (Intel style bus or Motolora style bus). It can be an individual product used for embedded design to acquire fast transient signals especially when DSO or PC-based acquisition cards are not applicable. This feature will be presented in later chapters.

Chapter 2 Literature review

This chapter is dedicated to the literature review. Firstly, as application background of this project, the EMI measurement campaigns in substations are reviewed. Next, as design reference, some data acquisition equipments are reviewed. Finally, some technology and components to be employed in this design are examined.

2.1 Introduction to substation engineering and the EMI measurement in substations

2.1.1 An introduction to the electrical supply system

An electric power system, or as it is sometimes called today, an electric energy system is the name given to the group of power stations, transformers, switchgear and other components interconnected by overhead lines and underground cables. In Britain, the generation and transmission of electricity is the responsibility of many utilities. All the utilities work closely together and the whole transmission system is interconnected and synchronized [8]. The electric power network consists of power stations, transmission lines and substations.

The network connecting power stations and primary substations is known as supergrid. It was built to carry large quantity of power across the country on 400kV or 275kV overhead lines. In the UK, the electricity is transmitted in 3-phases at 50Hz.

Primary substations take the power from 400kV or 275kV overhead lines and transmit the power to other secondary substations or distribution substations with lower voltage such as 132kV, 33kV or 11kV. Distribution substations deliver electricity to consumers with single-phase 240V at 50Hz.

2.1.2 Substations and emissions in substation

The substation is built for the transmission and distribution of the electricity as well as for the control and protection functions. Substations usually consist of busbars, transformers, switchgear, and a low voltage control and protection system. Transformers, busbars and switchgear are located in the switchyard and most (but not

all) control equipment is housed in a control room away from the switchyard to avoid EMI.

For protection, if a component, whether a transformer, terminal network or a section of transmission line, develops a fault, it is important that the faulty component be isolated from the other components as rapidly as possible. Switchgears are used to isolate the faulty components. There are 3 different types of switchgear: Breaker, Fuse and Isolator (Disconnector) [8]. For example, to protect the power system from a fault on the overhead line, the power network is divided into a large number of zones. One zone, for example, could be a length of overhead line between two substations. At each end of this overhead line, each phase of the lines is monitored by a current transformer (CT), which is designed to sense the amount of current through the overhead line. If a fault occurs in this section, such as overhead line short circuit to ground, the output of the CT is larger than normal. In each end of the line, the abnormal CT output trips the relays, which in turn trip the circuit breakers, so that the faulty line is isolated from the rest of the system. In a similar way, other components can be protected. This protection system also employs automatic re-closing strategy, i.e., the protection system re-closes the breakers a while after they have been opened. If the fault is still present, breakers will open again. After several attempts, the breakers will permanently open and this section of the overhead line is dead, until operators confirm that the fault has been removed and breakers are then closed [9].

Switchgear in substations automatically reacts to fault events. Also, during maintenance works, or installation works, operators use switchgear to isolate a certain part of the network.

When the breaker is opened, it interrupts the network currents. The network reacts to the current interruption by transient oscillations, which give rise to a so-called transient recovery voltage (TRV), across the two contactors of the breaker and forms the arc. Fig.2.1 shows the model circuit for TRV. Ug is the voltage between two lines and L is the distributed inductance in the network, R and C are the distributed resistance and capacitance.

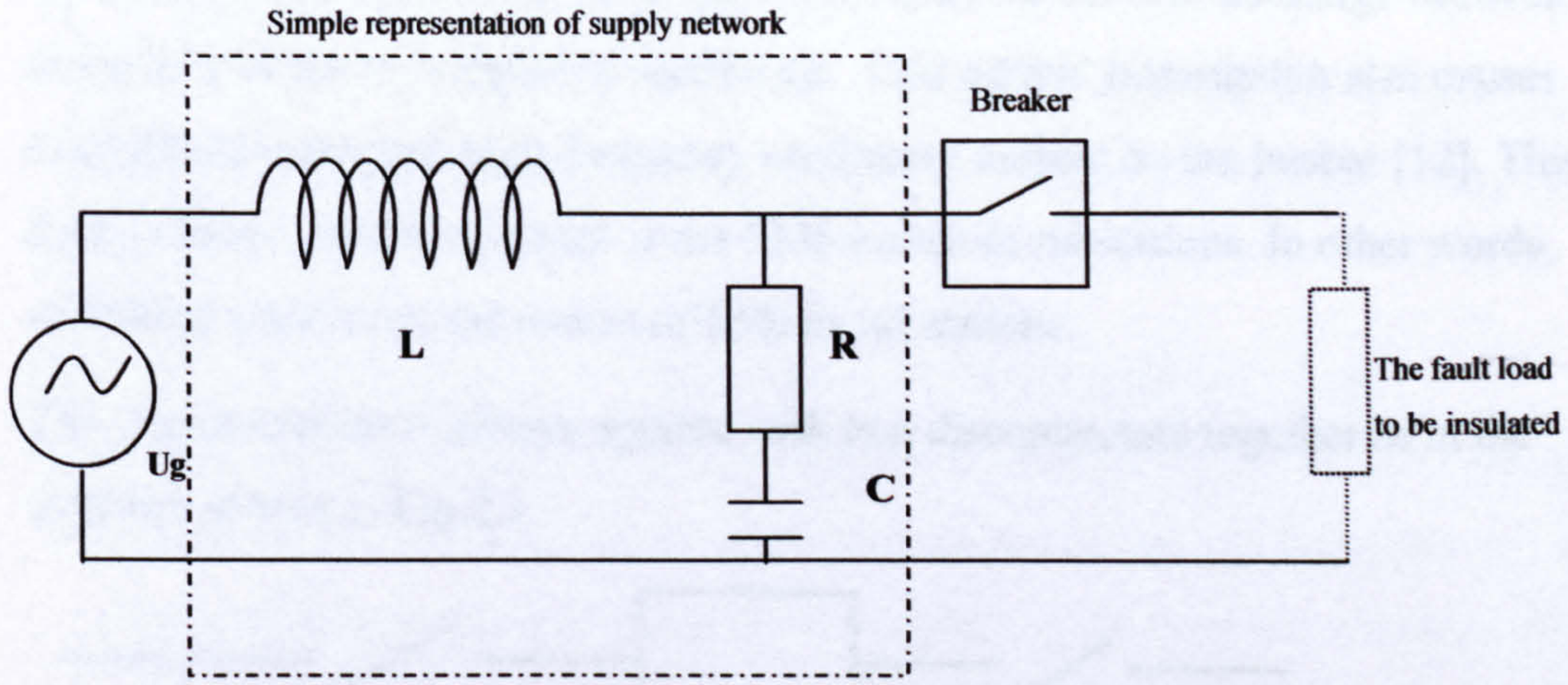

Fig. 2.1: Simplest model circuit for TRV evaluation

Switchgear uses 3 different methods for insulation or arc extinction: oil-insulated switchgear uses oil to protect contactors; air-insulated switchgear uses air to blow the arc; gas-insulated switchgear uses gas (SF6) to blow the arc [10]. The substation, which employs air-insulated switchgear, is called an air-insulated substation (AIS) and the substation employing gas-insulated switchgear is accordingly called gas insulated substation (GIS). Fig.2.2 shows a gas-insulated switchgear.

Fig. 2.2: Installation view of the gas insulated switchgears in a GIS

Due to the huge current the switchgear interrupts, the electric discharge between contactors of the switchgear is significant. This current interruption also causes considerable transient high frequency oscillatory current on the busbar [12]. This forms electric emission, which is the EMI source in substations. In other words, switching actions are the reason of EMI in substations.

The circuit breaker is always applied with two disconnectors together as in the structure shown in Fig.2.3.

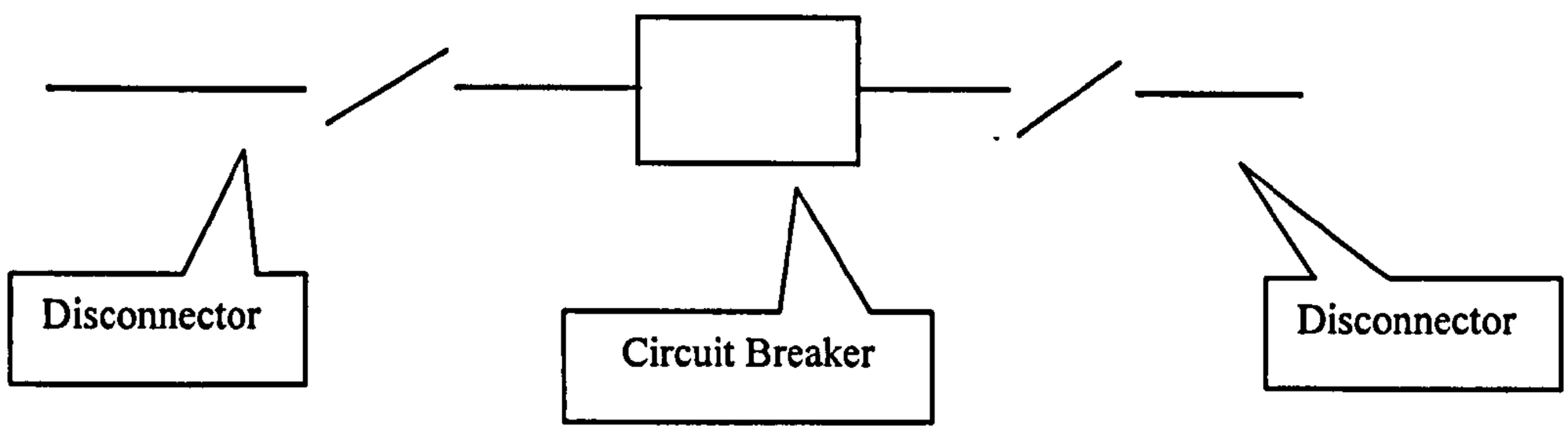

Fig. 2.3: Layout of Circuit Breaker and Disconnector

Where disconnectors are located on both sides of a circuit breaker, they are designed to provide more spacing between the live line and the dead line. Because the circuit beaker is designed to quickly close or open, its two contactors cannot move a long distance, and the space between two the contactors may not be adequate which makes leak occasionally from the live line across the contactors to the dead line. Therefore, the disconnector is applied to provide further interval. It usually opens in 1~5 seconds when the circuit is dead and closes before the circuit breakers is to be closed. Due to the remaining electric charge on the dead line, when disconnectors are opened, they also create electric emission and oscillatory transient current in the busbars or wires, which also cause EMI in substations.

Circuit breakers and disconnectors are the major EMI sources in substations. Accordingly, there are four types of EMI signals to be measured in substations: EMI made by opening of a circuit breaker; EMI made by closing of a circuit breaker; EMI made by opening of a disconnector; EMI made by closing of a disconnector. These EMI signals interfere with electric devices through radiation and conduction.

2.1.3 Emissions measurement in substations

The EMI measurement is done to characterize the EMI environment in substations. The data can be used to evaluate if the equipment to be installed in the substation have adequate EMI immunity.

Especially in recent years, more and more new control, protection and communication technologies have been applied in substations. Some examples are protection equipment based on microprocessor technologies, replacing power line carriers (analogue based technology) with wireless communication or optical fibre systems (digital based technology) etc. To successfully introduce and operate newer microprocessor-based technologies in the harsh EMI environment of HV substations, they must be immune to such interference, which needs to be very well characterised.

Normally, depending on their location, equipments used in a substation is typically required to comply with levels 2 to 4 of the most often used generic immunity specifications (UNIPEDE Norm Spec 230.05 or IEC 61000-6-5). For some new technology equipment that are distributed closer to EMI sources in the switchyard, their EMI requirements need to be carefully evaluated, particularly on the basis of the true characteristics of the environment [3]. There are six basic standards covering transient immunity tests: IEC 61000-4-2 (electrostatic discharges - ESD), 61000-4-4 (fast transients), 61000-4-5 (surges), 61000-4-9 (pulse magnetic field), 61000-4-10 (damped oscillatory magnetic field), and 61000-4-12 (oscillatory waves).

According to a survey on recent EMI measurement reports [13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 12, 23, 24, 24a, 25, 26], the Working Group 36.04 (EMC general aspects) has made the conclusion that the highest frequency generated in AIS substation is 10MHz and 140MHz in GIS substation [3].

For GIS substations, to measure the signal up to 140MHz signals with adequate precision, the analogue bandwidth of DSO should be more than 200MHz and the sampling rate should be more than 500MSPS (the relationship between bandwidth and sampling rate will be discussed later in chapter 4). If building an acquisition circuit with this performance, the components (ADC, logic circuit and memory) should have 1GHz working speed. Such a design cannot be achieved by TTL(Transistor-Transistor Logic) or CMOS (Complementary Metal-Oxide

Semiconductor) circuits so other higher speed components and interfaces, such as VLDS or ECL circuit should be required. That would increase the development difficulty and require expensive components and facilities, such as FPGA with VLDS interfaces and latest FPGA development kit. The fund and time period allocated for this project could not support such a development. Therefore, the prototype design employs TTL/CMOS technology and addresses the EMI measurement in AIS substations, where the upper frequency is 10MHz. On the other hand, the frequency of 140MHz in GIS was measured close to the source. Away from the source, the voltage/current would have undergone significant attenuation and hence, for the purpose of the radiated emission, a similar bandwidth is sufficient for GIS [12]. To provide a suitable bandwidth, the acquisition device in the Wireless Digital Measurement System is chosen to have 20MHz bandwidth. For such analogue bandwidth, the sampling rate should be at least 50MSPS (Minimum 2.5 times of the signal bandwidth that allows filter take 5MHz bandwidth for "roll down"). The final result is 80MSPS, which approaches the limitation of a TTL circuit.

2.1.4 Emissions measurement equipments

Depending on the structure of the substation, types of switchgear and different operational currents and voltages, the EMI signals have different frequencies, periods, amplitudes, and shapes. Therefore, the measurement should take place under different conditions. The EMI measurements according to their types are divided into conducted measurement and radiated measurement. Conducted EMI measurements using current transformer (CT) and voltage transformer (VT) sense the EMI signal on the transmission lines in the control room or switchyard. Radiated measurements using antenna sense the EMI signal at different places in the switchyard. The EMI measurements according to the EMI characteristics are divided into 4 types: 50Hz magnetic field (50Hz H-field), 50Hz electric field (50Hz E-field), high frequency magnetic field (High frequency H-field) and high frequency electric field (High frequency E-field). Different measurements apply different sensors. For example, a HI-3604 ELF Survey Meter can be used for low-frequency E-field low-frequency H-field measurement, a SU2 electric sensor can be used for high frequency E-field, and ARAPLA-2051B can be used for high frequency H-field [27, 28, 29].

A block diagram of fibre-based radiated EMI measurement system has been given in Fig.1.2, while Fig.2.4 shows the details of each channel of that system [31, 32]:

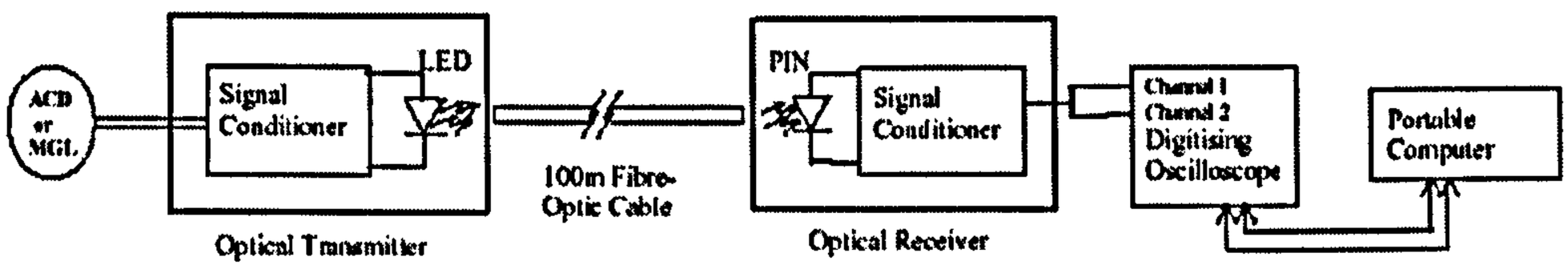

Fig. 2.4: Block diagram of radiated transient measurement system

ACD (Asymptotic Conical Dipole) or MGL (Multigap Loop) is the high frequency sensor, which senses the strength of electric field or magnetic field respectively. These sensors have high frequency response and their voltage output presents the frequency information and amplitude information of the fields. In the system, operators use digital storage oscilloscopes to record the waveform of the output signal from sensors. These Oscilloscopes are set to single trigger mode to capture the transient EMI signal during the switching operations. The recorded data can then be analyzed on or off the site to evaluate the EMI distributions in the time, space and frequency domains.

2.2 Review of data acquisition technology

2.2.1 Feasibility of a digital measurement system

The aim of this project is to design and produce a Wireless Measurement System for EMI measurement to replace current fibre systems. As explained before, the signal at the front end should be captured and converted into digital form, consequently, the acquisition device at the front end should have the functions of DSO. This signal acquisition device or, as described in many similar projects [33], digital front-end is the key point of this new system.

In fact, such a digital front-end has been considered since early 1997, when the EMC group in Strathclyde University was developing an EMI measurement system. At that time, since the digital equipment would be complex and physically bulky, they

had to abandon the digital solution and instead chose the "Fibre Analogue" solution. The problem of the digital acquisition unit had been reported in [1].

The obstacles for building a digital system in 1997 were:

1) If they employed existing digital equipment, such as PC-based acquisition cards, the whole system would be bulky and susceptive to EMI.
2) If they developed their own circuit, the development work would be difficult and would take a long time (They had just 1year to develop that measurement system).

In 2002, when this project commenced, the situation had changed.

1) Thanks to the rapid development of digital ICs in recent years, especially PLD technology and their derived products, developing a high-speed, large-scale digital circuit becomes easier than before.
2) As a Ph.D project, the expected time allowed a designer to accomplish the development of the digital system, overcoming the significant challenges presented.

2.2.2 Necessity to develop a custom acquisition circuit

As mentioned before, this digital wireless system is designed to replace a DSO and fibre link in current measurement systems. Obviously, the acquisition unit at the front end fulfills the functions of a DSO to record the waveform of fast transient signals.

For a CPU-based system, there are two ways to acquire a signal: Software mode and hardware mode. These two modes have been briefly explained before in chapter 1. Software acquisition mode uses ADC to feed data to the CPU directly. Since the acquiring process is controlled by software, which is a sequential operation, the sampling speed is limited. Even with fastest DSP, the single channel acquisition speed cannot exceed 20MSPS. Hardware acquisition mode builds a hardware acquisition circuit with ADC, memory, and other logic circuits. Using this method, the converted data can be buffered into a memory at a high speed and the CPU can

read the data from memory at low speed non-simultaneously. The hardware mode can achieve a sampling speed much higher than the software mode. The fast transient signal here refers to a signal with such a high frequency that software mode acquisition techniques cannot deal with.

There are two kinds of universal devices performing the hardware mode acquisitions—DSO and PC-based acquisition card.

Oscilloscopes were originally designed to display repetitive signals. Many years before the digital oscilloscope was invented, to observe a transient signal had been a problem for engineers, since analogue oscilloscopes can neither stop the signal nor store the signal. Philips Corp. developed a camera-oscilloscope to deal with a transient signal, which applies a camera cooperating with the trigger function of the oscilloscope to take a picture of the display of the oscilloscope. Fig.2.5 shows the photograph of this product.

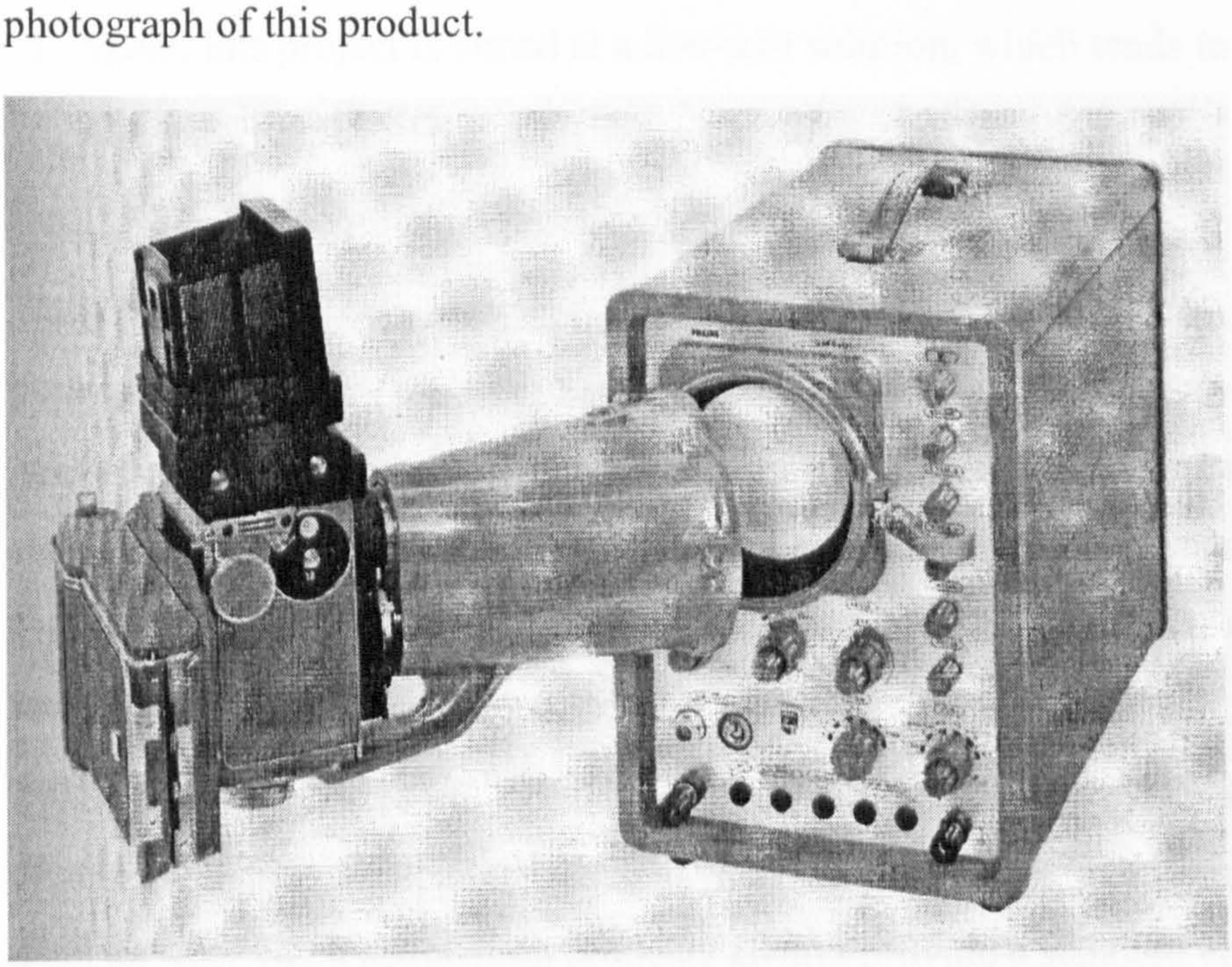

Fig. 2.5: Philips single-picture recording system equipment "PM9300" Camera-Oscilloscope [32]

Now it is easier since digital technique is applied in oscilloscope. Digital Oscilloscope can store a transient signal in memory by either automatic "trigger" action or manual "stop", then the captured transient signal can be displayed the transient signal for as long as operators want.

A DSO is applied to record the transient EMI signals in an existing EMI measurement system. However, in this project, DSO cannot be used at front-end for the reasons of:

1) The front-end is expected to be a small and simple device, which should use an embedded CPU to obtain the data and encode them for wireless communication. However DSO manufactures don't provide users the interface to an embedded CPU. DSO just provides user with two interfaces: one is keyboard and display; the other is the application software in a PC. Users' embedded CPU cannot obtain data from both the display or PC software. That is to say, DSO is not suitable for an embedded application.

2) DSO is not suitable to be placed in the front-end in switchyards due to EMC problems.

3) Again, this project is aimed at a low-cost solution, which tends to favour a system without DSO.

Next, PC-based acquisition products are examined:

Since PC's have become increasingly popular, huge numbers of Virtual DSO and PC-based acquisition products have been developed. PC-based DSO uses an add-in card or a stand-alone acquisition unit to acquire the measured signal and use a PC system to display waveform and implement keyboard functions. Such PC-based systems have the functions of DSO and also provide integrated man-machine interface to the user.

There are thousands of PC-based acquisition products, which are designed for many diverse industrial applications, such as imaging acquisition, radar system, laser detector, etc. Such acquisition products always provide a standard computer interface, such as PCI, ISA PXI, USB etc, which are attached to a computer (PC, PowerPC or so). They also provide users with a device driver program or integrated application software, which needs a general Operation System (OS) such as Window, Unix or similar. Thus, these acquisition products usually need to be installed in a computer system. An embedded CPU cannot obtain data from the acquisition card directly.

If an industrial computer had been used in the switchyard, it could provide a solution using a computer with acquisition card and a wireless communication modem to build a digital front-end. However, this solution was rejected when it was discussed in the EMI group, since a PC or industrial computer has a complex construction, which may cause EMC problem. Also, the computer, even a signal-board computer would impose a power consumption that is not suitable for battery-powered equipment (power supply product in switchyard may not be conveniently located). Again, the hardware and software of the computer system would increase the cost compared to using a single-chip embedded CPU.

Thus, the universal acquisition instruments, i.e. DSO and PC-based acquisition card, have been rejected in this project. The next paragraph discusses the feasibility of utilizing other specific equipment.

There is much electrical equipment designed to deal with fast transient signals, especially in the applications of radar systems, ultrasonic images, CT images and in some automatic control systems. Most of this equipment employs computer-based data acquisition products to acquire the fast transient signal. However, there are still few equipment that use monolithic embedded CPU instead of a computer for the requirement of small size or low-cost. For such equipment, designers have to make their own acquisition circuits. However those designs are not available to be used for this project due to following 2 reasons:

1) As a part of certain equipment, the acquisition circuits are usually not supplied as products. Designers rarely publish the details of their acquisition circuits.

2) All the custom acquisition circuits in the equipment are designed for some specific purposes. They always have their specific performances or functions. It is not possible to find a proper acquisition design from them that is suitable for this type of EMI measurement system. For example, a digital distributed video monitoring network may have their own acquisition circuits in the front-end following the outputs of video cameras. That acquisition circuit doesn't need an adjustable triggered function, which is essential to EMI measurement system [33].

Therefore a custom design of the acquisition unit is necessary, which is a board level design, i.e. using general components and building a custom PCB circuit.

2.3 The techniques and components for the wireless data acquisition system

2.3.1 Review of wireless "Data Logger"

This wireless digital EMI measurement system has the common construction of so-called "distributed field data collection (or acquisition) systems". Such kind systems acquire signals at several front-ends and transmit the collected data to a remote background, usually a PC. There are many "distributed field data collection system" products that exist in the market and are known as "data loggers". However, such data loggers are not applicable for the "EMI measurement system" as they only provide slow sampling rates, which match the communication speed. Since the data logger samples the signal, converts the signal and sends the data to PC simultaneously, the sampling rate of the data logger never exceeds the communication speed. In other words, a data logger acquires a slow real-time signal, whereas the "EMI measurement system" acquires a fast transient signal. For example, HOTEK Technologies Ltd. Has a series of wireless data logger products with adjustable sampling rate from10 samples per second to 1 sample per hour. Fig.2.6 shows the example of a temperature monitoring system using their products [39]. Because such products are designed for real-time acquisition, most of them haven't enough memory to buffer the converted data in front-ends. Even though some of these products have small memory, it is designed for temporary buffering of the data in case the communication is interrupted for a short period. For example, Fluke's wireless logger 2625/WL can be configured to "interval scan mode" and buffer 16K data. However, the maximum rate of this data logger is only 11kSPS, which cannot be used for the measurement of

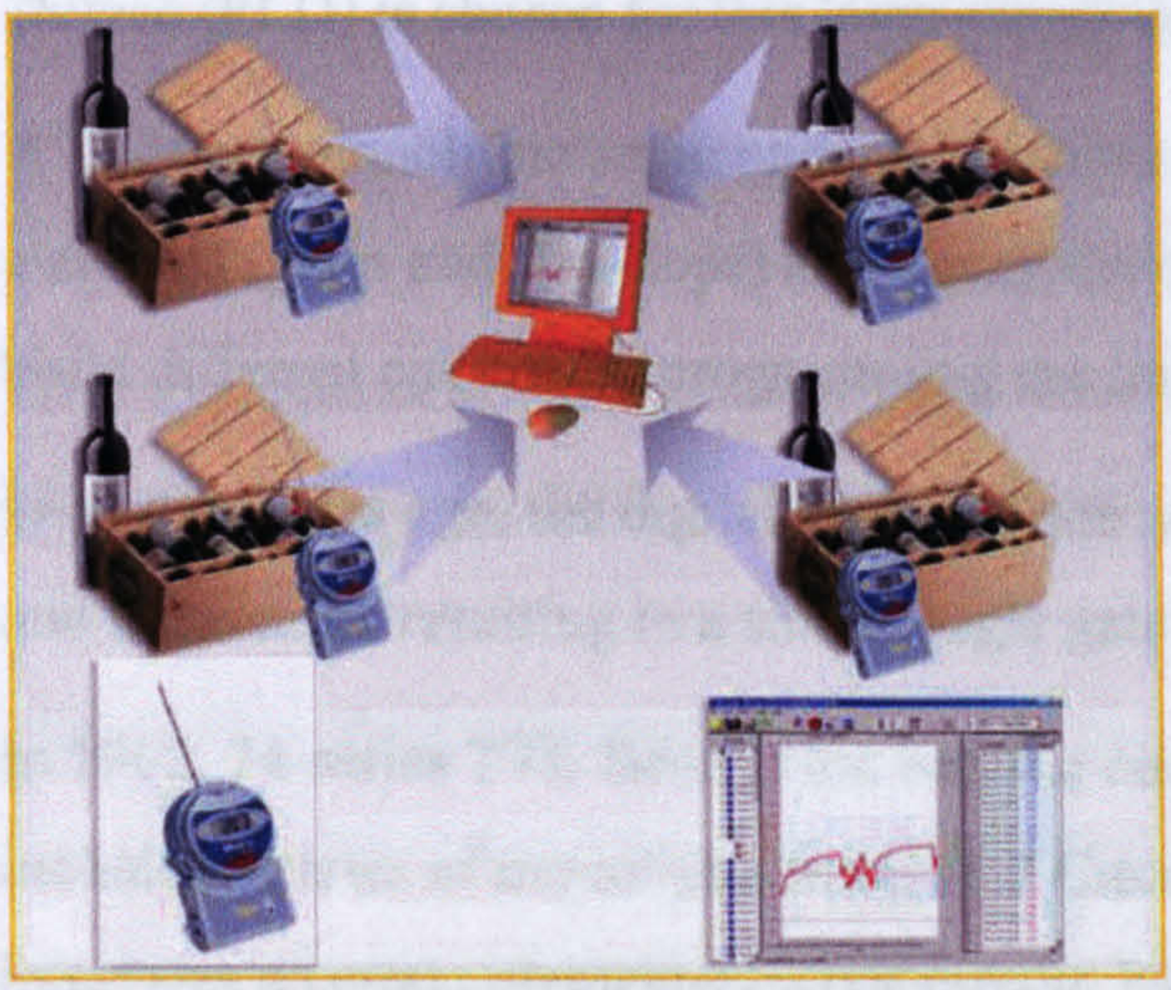

Fig. 2.6: Temperature monitoring System with HOTEK data loggers

the fast transient signal in this project [40]. In addition to the above, no data logger has a trigger capability.

2.3.2 PLD and its application in large scale logic circuit

In order to realise its correct function, the acquisition circuit should consist of 3 elements: an ADC, a memory and a logic circuit. ADC and memory can be simply chosen from the products available in the market. But building the logic circuit is the key part of this design.

Examining the required functions of the acquisition unit, it is clear that the logic circuit in this part is complex and working at a high-speed. It should manage the storage process, realise trigger functions and build an interface to embedded CPU. This needs a huge amount of logic resource (Gates, registers and interconnections). Also, within every conversion cycle, the logic circuit should finish all the actions of generating a memory address, taking the converted bytes from ADC, writing the data to memory. This requires the logic circuit working at a speed higher than the ADC conversion. Considering the circuit scale and working speed, a Programmable Logic Device (PLD) is chosen for this logic circuit design.

A PLD is a monolithic semiconductor circuit containing a large number of logic elements (gates and flip-flops) and interconnection wires, which allows the user to build different circuits by programming the interconnection matrix of the PLD.

Over 4 decades ago, the digital logic circuits were built entirely by discrete resistors and transistors, resulting in a simple logic gate being fairly bulky.

In 1962, 74-series TTL family first became commercially available. The 74-family includes a series of monolithic Integrated Circuits (IC) and every chip in them integrates a certain elementary logic circuit. Users can connect different 74-series ICs together to build their complex logic circuits. By the early '80s, a veritable alphabet soup of logic family variants were released—TTL, S, LS, F, ALS, CD4000, HC, HCT, AC, ACT, FCT, LVT, AHCT. Also different packages and speed-grades products were provided. Today, over 500,000 unique 7400 devices can be chosen to suit different applications [34].

However, to build a complex logic circuit using 7400 products, designers still need to make large PCBs to contain a mass of interconnection wires and plenty of 7400 devices. Although Application Specific Integrated Circuit (ASIC) can synthesize a large circuit within a single chip, it doesn't suit small quantity production or prototype systems. PLD products thereafter were invented in the middle of 1980's, for the original purpose of reducing the numbers of 7400 devices in some logic designs. Early PLD products are PAL (Programmable Array Logic) and GAL (Gate Array Logic), which usually have 10~20 configurable flip-flops and many gates within a single chip. After that, some larger PLD devices were released with more usable logic units in one chip. These large scale PLDs are called CPLD (Complex Programmable Logic Device), which usually have 30~300 macro-cells, each macro-cell has 1 or 2 configurable flip-flops, several product terms and a configurable input/output port. Another kind of PLD is FPGA. In1985, Xilinx pioneered FPGA (Field Programmable Gate Array) technology, which based on so-called lookup-table technology uses RAM (Random Access Memory) to implement logic functions. FPGA provides much more logic resources and higher speed than CPLD but needs to be re-configured every time it is powered up. Additionally, FPGA always have a high price and need expensive development facilities. Thus, unless FPGA is necessary, users usually select CPLD to build logic circuits.

PLD products have rapidly developed in recent years, and the performances of the PLD, either CPLD or FPGA, have improved significantly. Latest CPLD may have more than 300 macro-cells and recent large FPGA may have millions of equivalent logic gates [35, 36, 37, 38].

Nowadays, PLD is widely applied in digital circuits. Compared with discrete logic devices, PLD is more preferred for complex digital design as it has the following advantages:

1) PLD can significantly reduce the PCB size as well as the number of components by building a complex circuit inside a single chip.

2) PLD can achieve higher speed. As most interconnection wires are built in the PLD, the "transmission line delay" is reduced to a minimum.

3) PLD provides most flexibility to users. For prototype designs, designers can modify their logic designs by simply changing the program codes and re-configuring the PLDs without remaking new PCBs.

In this project, the acquisition unit employs CPLD to implement the logic circuit.

2.3.3 Features of wireless modems

The general way to build a wireless link between two CPUs is using wireless modems. Usually, in such wireless communication systems, wireless modems implement the protocols in lower layers, such as addressing and data protection, whereas host machines implement the protocol in the application layer. In this EMI measurement system, host machines[2] (the unit where the original data is generated or received) are the embedded CPUs in front-ends and the PC in the background. The following paragraphs discuss the features of wireless products and how to select the wireless modem for this EMI measurement system.

Dependent on the media, wireless data communication products can be divided into RF, Infrared, laser or other wireless modes. Infrared or other modes are not suitable for this project. In this thesis, "wireless" always refers to the RF mode.

The modulation modes of RF communication device can be divided into AM (Amplitude Modulation), FM (Frequency Modulation), PM (phase modulation), etc. As FM mode usually provides better interference immunity for digital communication, most digital wireless modems employ FM technology [41].

Every RF transmission device transmits signals by emitting an electromagnetic wave at a certain frequency with a limited bandwidth. In an adjacent place, if a different wireless communication device emits RF signals in the same frequency band, they may interfere with each other. To avoid such frequency collisions, some standards were established. These standards divided the RF spectrum (from 9KHz to 30GHz) into numerous channels (frequency bands) and allocated them for different

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[2] In a modems linked network, the machine, where a modem obtains non- modulated data from or sends demodulated data to is the host machine for that modem. E.g. in the dial-up network, the PC is the host machine for its attached modem.

applications or reserved them for future uses. These standards also limit the emission power of wireless products. For example in the UK, a GSM system takes the band from 935.2MHz – 939.6MHz and 947.4 MHz- 954.8MHz. The frequency band from 86.9MHz ~93.5MHz is allocated to BBC Radio 2,3,4 (For more detail, please refer to http://www.ofcom.org.uk). These standards were made by organizations known as "wireless communication administrators". The "international Frequency Registration Board" is responsible for allocating the part of frequency spectrum, which is used for global applications. Different countries or different regions have their own "wireless communication administrators" responsible for allocating the frequency spectrum to applications in the local region, as well as supervising wireless device manufacturers. For example, in America, all the wireless products should be compliant with the standards of FCC (Federal Communication Commission). In the UK, wireless products are compliant with the standards made by ETSI (Europe Telecommunication Standard Institute) and ERC (Europe Radio Committee). Wireless standards in different counties or different regions may be slightly different [42, 43, 44].

Most available radio frequency resource has been allocated to public services, such as TV broadcast, navigation systems, the public mobile phone network and security and military networks. For private wireless communication, the wireless device can operate in certain so-called "license-free" frequency-bands. Operators can use these frequency bands for their own miscellaneous applications without applying for a frequency access license from their local administrators. Most industrial automatic control engineering uses "License free" products to build their own wireless local area network (WLAN). Likewise, in this project, designers will use "license-free" wireless modem building a LAN.

Popular "license free" wireless modems in the UK market mainly operate in 4 "license-free" bands: 458MHz (457.5~458.5), 433MHz (433.05~433.79), 868MHz (867~870), 2.4GHz (2400MHz~2483.5MHz). 458MHz is a Telemetric band, 433MHz is SRD (Short Range Device) / ISM (Industrial Scientific and Medical) band, 868MHz and 2.4G are ISM bands [45].

Examining these products, it has been found that 2.4 G modem products usually have higher communication speed, since they use wider bandwidth. Therefore, 2.4 G products are preferred for the application of the EMI measurement system.

Another reason to choose 2.4 G products is that they always implement "Spread Spectrum technology" (SST). SST was developed by the military, since it allows many wireless devices to share an enlarged frequency band. SST also improves the EMI immunity of wireless communication [46]. It is therefore important for the EMI measurement system.

There are 3 major open protocols that are implemented for 2.4 G modem products—HomeRF, Bluetooth and IEEE 802.11(Wi-Fi). HomeRF products have limited range (50 metres), which is not suitable for this measurement system. Compared with Bluetooth, the advantage of Wi-Fi is fast speed. The downside of Wi-Fi is it needs more complex configuration and it is more susceptible to interference [47]

The communication speed required for this EMI measurement system is not very crucial, Bluetooth modem is preferred for this project. Using Bluetooth product also brings an additional benefit. Since it would be the first time that a Bluetooth product was used in EMI measurement in switchyards, the experience can be a reference for other EMI measurement projects potentially using Bluethooth device within switchyards.

Apart from the 3 open protocols, some 2.4 G data modem implement manufacturers' private protocols. These products have different performances, such as range, speed, to fit different applications. Because these products are usually designed for industrial applications, they always have adequate EMI immunity. The only downside of such products is that they usually cost more than Bluetooth wireless modems. However, this kind of wireless modem is also a good choice to build the wireless data communication network in this EMI measurement system.

All the wireless modems, that were deemed to be suitable for this project, are listed in chapter 5, where the selection of an appropriate modem is considered.

Chapter 3 System design and the solution for Acquisition

This chapter presents the system design. System design is aimed at finding a solution at the system level to fulfil the functions. It also divides the whole system into several parts to determine the functions of every part and clear the relationships between each part. In other words, system design determines the structure of the whole system and the interfaces between every subsystem.

3.1 Functional design of the system

This system is a field data collection system based on a wireless network. This system has 3 main functions:

1) Capture and record the transient EMI signal, which comes from different sensors. The desired sampling rate is 50MSPS or higher, which is capable of acquiring the EMI signal with maximum 20MHz frequency.
2) Transmit the recorded data to a remote PC through a wireless network
3) Control the acquisition process and collect the recorded data from the PC.

Thus, the whole system can be divided into 3 parts as shown in Fig.1.6: Firstly, the Remote Acquisition Unite (RAU), which is located in switchyard, takes the role of a DSO in the Fibre Analogue Measurement System. Secondly, Wireless Data Communication Network, which should be a bi-directional Point-to-Multipoint network that transmits control commands from the PC to RAUs and data from RAUs to the PC. Finally, the PC-based control platform, which is an application program to provide an operating environment to users.

3.2 RAU and its interface to communication network

The RAU is designed to capture the EMI signal as a DSO. As mentioned in chapter 2, the sampling rate of the RAU should be more than 50MSPS. The design of RAU is thereafter aimed at 50MSPS and as high as possible (Actually 80MSPS). The memory size of the RAU determines the length of signal that can be recorded. Experience at Strathclyde indicates that 5ms is adequate. Thus the RAU has 512k Bytes memory. The input of the RAU is the analogue signal output from the sensor.

RAU uses an A/D converter to digitise the analogue signal and uses a memory to buffer the data. Once the measured signal meets the trigger condition, the RAU will stop the buffering operation. At that moment, the data kept in the memory is the information of the signal around the trigger point. An embedded CPU can then read the data from the memory and send them to a remote PC over the wireless communication network. A Complex Programmable Logic Device (CPLD) is used in this design for logic functions. The CPU needs an interface to the wireless communication network to exchange data. Most applicable modems, which are designed for such applications, have RS-232 or other serial port to the host machine. To adapt to more wireless modems, the RAU provides RS-232, RS-422 and TTL serial ports. These ports are driven by a Universal Asynchronous Receiver and Transmitter (UART) of the embedded CPU. Fig.3.1 shows the block diagram of the RAU. The details of the RAU design will be described in next chapter.

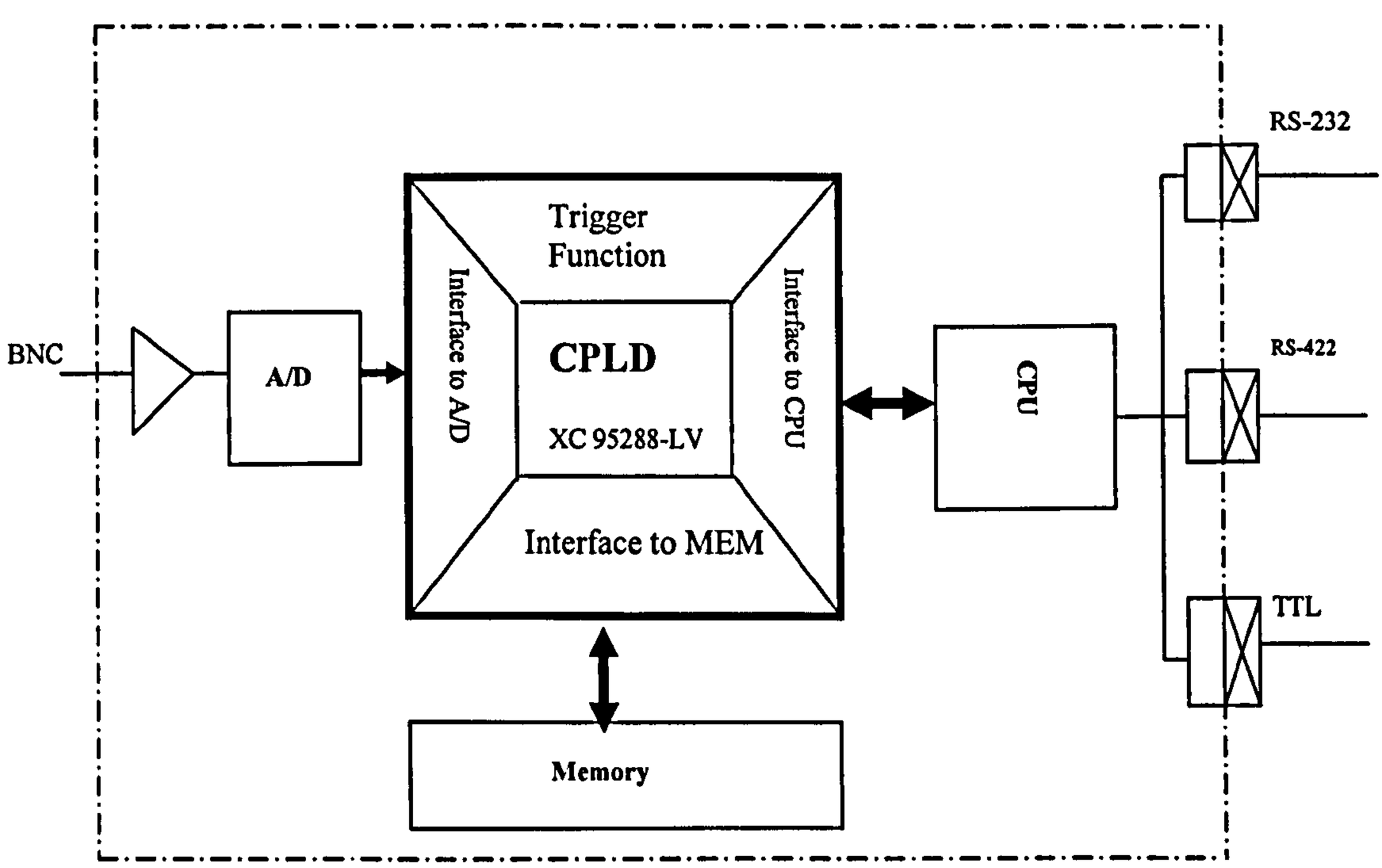


Fig. 3.1: Block diagram of RAU

A visual impression of the completed unit is shown in Fig.4.52 and repeated here in Fig.3.2 for ease of reference.

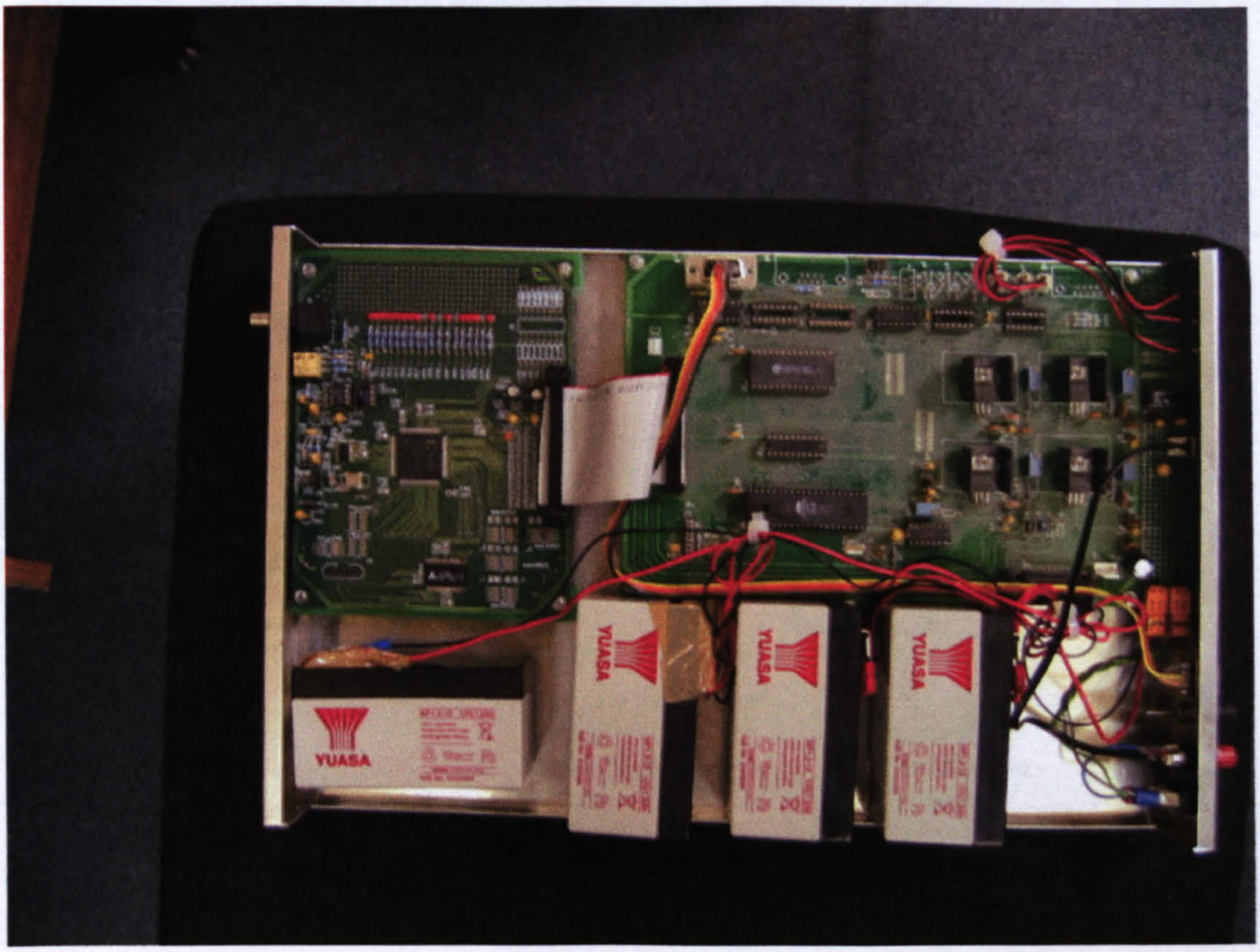


Fig. 3.2: Inside of the RAU

3.3 Wireless communication network

This wireless data communication network must have a bi-directional point-to-multipoint topology. RAUs in this network are slave-machines and the PC is the master-machine[1]. The wireless modem should be responsible to transmit data between PC and RAUs. Since in the PC and the RAU, the software cannot implement much low-level communication protocols, which are usually complicated, the modems should implement a complete communication protocol and provide easy interfaces to their host machines (RAUs and PC) to build a wireless network. For example, in some so-called "Transparent Link", two modems can make a modem-pair as shown in Fig.3.3. In that pair, modem can take original data from its host

[1] If a communication network has one and only has one node can exchange data with all other nodes in the network simultaneously or non-simultaneously, this network is defined as point-to-multipoint network. The node can exchange data to multi nodes is called master-node and the others are slave-nodes [107].

machine, then encodes, modulates, and sends the data to the remote opposite modem. The opposite modem receives, demodulates and decodes the wireless data, then sends the original data to its host. Thus, for the host-machines in both sides, the wireless link acts as a transparent link or "wireless cable" [5].

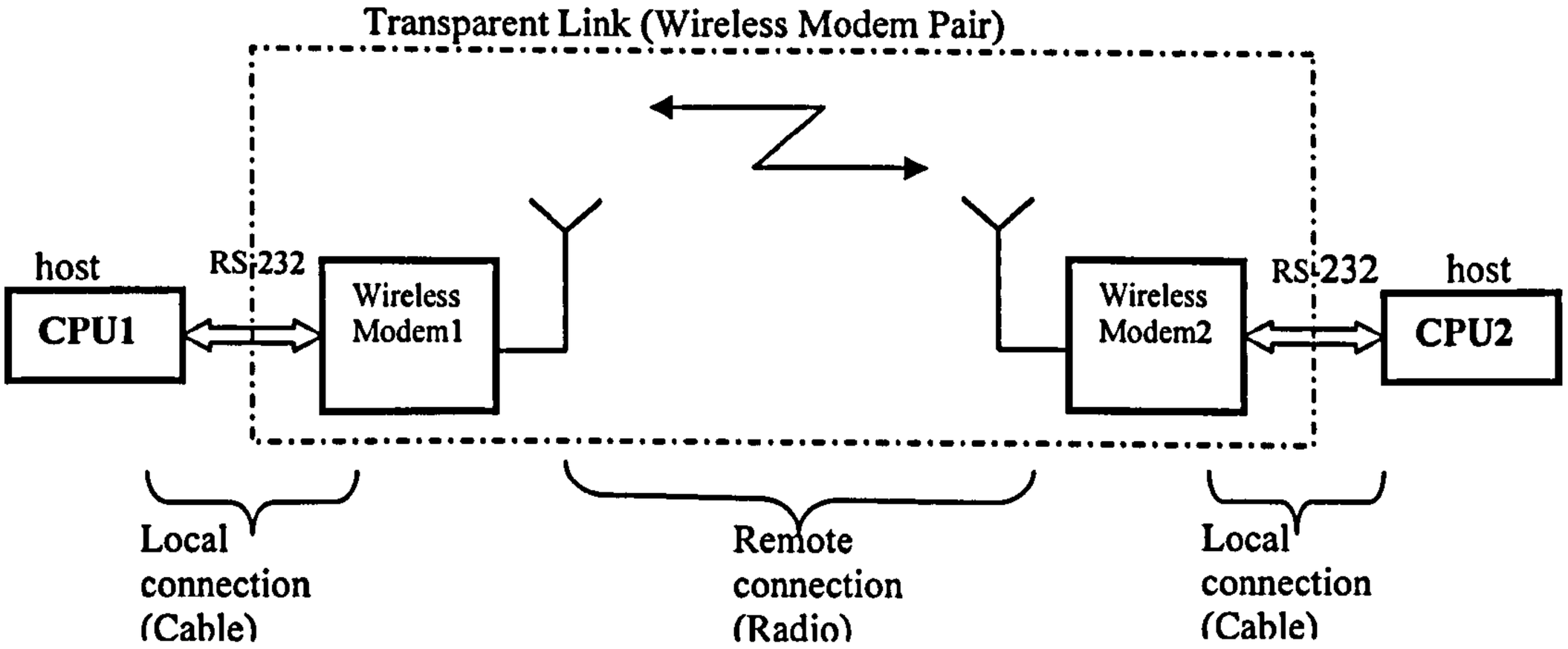


Fig. 3.3: Wireless pair (point-to-point)

The data sent to the modem will be replicated on the other side without any extra information. Thus, for the PC and embedded CPU, they only need to build a communication interface between the application software and the lower network service. Therefore in this communication system, host machines only realize the functions of application layer and modems realize other lower layers functions. There are plenty of wireless products have such a "Transparent Link" feature, most of them connect to the host machine with a serial port, such as RS-232 port RS-422 or TTL UART port. The final choice should refer to their actual performance. Before the final selection is made, the RAU reserves 3 types of serial ports (RS-232, RS-422 and TTL) to adapt more products. The detailed design of this network is described in chapter 5

3.4 PC-based control platform

The PC-based control platform is an application software, which provides a man-machine interface to operators. Using this interface, operators can set-up the parameters of RAUs, such as trigger-level, trigger-delay, pre-trigger, sampling rate

etc. This software also displays the states of RAUs. Once a RAU is triggered, the operator can download the data from the remote RAU. These data are the raw product of the measurement, which can then be displayed and analysed in other DSP (Digital Signal Processing) software, such as FFT (Fast Fourier Transform) processing software.

The control-platform also controls the data communication network.

3.5 Research and development of configured system

Fig.3.4 shows the flow diagram of the research and development of this system.

After the system is designed, every part can then be developed separately. The development work of the RAU includes hardware and software design, which took more time to develop than other two parts. The RAU is also the most complex and difficult part in this project. Consequentially, the bulk of the thesis was devoted to the RAU description.

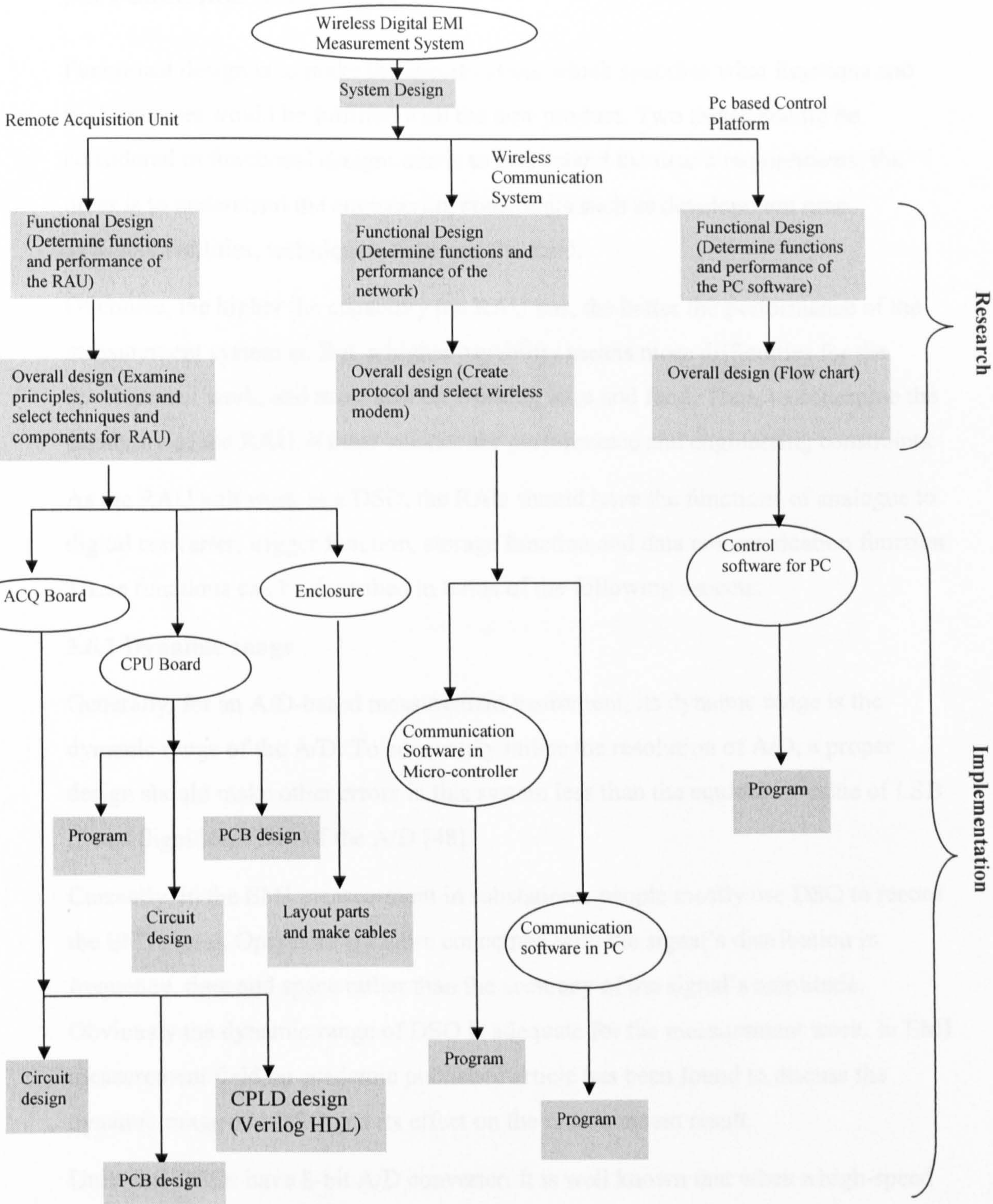


Fig. 3.4: Research and development work in this project

3.6 Functional design of RAU

Functional design is to make the specification, which specifies what functions and performances would be fulfilled with the new product. Two things should be considered in functional design: one is to understand the user's requirements; the other is to understand the engineering constraints such as development time, available facilities, techniques, team and the fund.

Of course, the higher the capability the RAU has, the better the performance of the measurement system is. But, a higher capability means more difficulties for the development work, and more cost on working time and fund. Thus, to determine the capability of the RAU, it must balance the performance and engineering constraints.

As the RAU will work as a DSO, the RAU should have the functions of analogue to digital converter, trigger function, storage function and data communication function. These functions can be described in terms of the following aspects:

3.6.1 Dynamic range

Generally, for an A/D-based measurement instrument, its dynamic range is the dynamic range of the A/D. To adequately utilise the resolution of A/D, a proper design should make other errors in this system less than the equivalent value of LSB (Least Significant Bit) of the A/D [48].

Currently, in the EMI measurement in substations, people mostly use DSO to record the EMI signal. Operators are more concerned with the signal's distribution in frequency, time and space rather than the accuracy of the signal's amplitude. Obviously the dynamic range of DSO is adequate for the measurement work. In EMI measurement field no academic published article has been found to discuss the dynamic range of a DSO and its effect on the measurement result.

Universal DSOs have 8-bit A/D converter. It is well known that when a high-speed A/D works in its full speed, its resolution will become worse. For 8-bit A/D, it will generally drop down to 7-bits or 7.5 bits, which can provide 40-50 dB dynamic range. Therefore, following DSOs, RAU employs an 8-bit A/D to obtain 40dB-50dB dynamic range.

The accuracy/error here refers only to the static signal. The dynamic signal will be discussed later.

3.6.2 Bandwidth and sampling rate:

The bandwidth quoted for an oscilloscope often refers to the frequency at which the amplitude has fallen by 3dB [49]. The bandwidth quoted for RAU has the same meaning. It must cover the whole bandwidth of the signal to be measured. As has been pointed out before, the measurement system is designed for the transient measurement in high voltage substations, and in most high voltage substation the dominant EMI frequency is 3MHz and the highest frequency is about 10MHz [3].

In a bandwidth limited measurement system, dynamic signal is always attenuated. Such bandwidth limitation introduces measurment error for high frequency signals, called "rising time error". DSO designers used to estimate the "rising time error" by following table" [50]

Table 3.1: Rising time error versus bandwidth

Rising time error	DSO bandwidth	
	for Gaussian response	for Flat response
20%	1.3 times of signal bandwidth	1 time of signal bandwidth
10%	1.5 times of signal bandwidth	1.2 times of signal bandwidth
3%	1.9 times signal bandwidthe	1.4 times of signal bandwidth

In Table 3.1 Gaussian response and flat response are used to describe the gain-frequency characteristic of the analogue channel. If the gain-frequency response graphic has a sharpen "roll-off", it is call "Flat response" otherwise it is called "Gaussian response"

Assuming the response of the analogue channel in RAU will be a Gaussian system, pursuing a good accuracy, the bandwidth of RAU should be more than 19MHz (1.9 times the signal bandwidth). For convenience of calculation, 20MHz is chosen for the bandwidth of RAU.

Theoretically, for a sampling measurement device, to recover the signal containing 20MHz frequency component, it must have at least 40MHz sampling rate (Nyquist sampling principle). However, practically for a measurement equipment, e.g. DSOs, it usually has the sampling rate of 2.5 to 4 times of the bandwidth for anti-alias purpose. This anti-alias design will be discussed in section 4.1. Thus RAU is designed to have more than 50MHz sampling rate and actual implementation will pursue the sampling rate as high as possible (Actual sampling rate is 80MHz).

Furthermore, the sampling rate of RAU should be adjustable for the purpose of recording a signal with a lower frequency over a long time, like changing the time base of an oscilloscope. According to the measurement request, RAU has eight shifts: 80MSPS, 40MSPS, 20MSPS, 10MSPS, 5MSPS, 2.5MSPS, 1.25MSPS and 625kSPS. Also, for the commissioning work, it designed to have a real time data acquisition mode, which can realise 40kSPS (Depends on the wireless transmission speed) real time data acquisition.

3.6.3 Memory size

For a DSO, when it records a signal, one sampling point takes a byte (8 bits) of memory (every sampling point in DSO is represented by a 8-bit digital code). The memory size limits the length of the signal that can be recorded.

In substations, short transient EMI signals usually have several micro seconds to several milliseconds duration, long EMI signals may have 1 second duration, which is made up of several short duration EMI pulses.

The memories in DSOs are usually limited, so which not be able to record a long signal at its full sampling speed. Practically, for long duration EMI signals, it is a common practice to use a low sampling speed to record the whole shape of the signal, find the interesting area of the signal and position the area, then record the details of that area at a high sampling rate using trigger-delay function in the next electrical emission event (a EMI signal caused by a certain switching action makes the same waveform under the same condition). Thus, with the trigger-delay function of DSO, operators can measure features of interest within a long signal using small memory. Fig.3.5. illustrates this application.

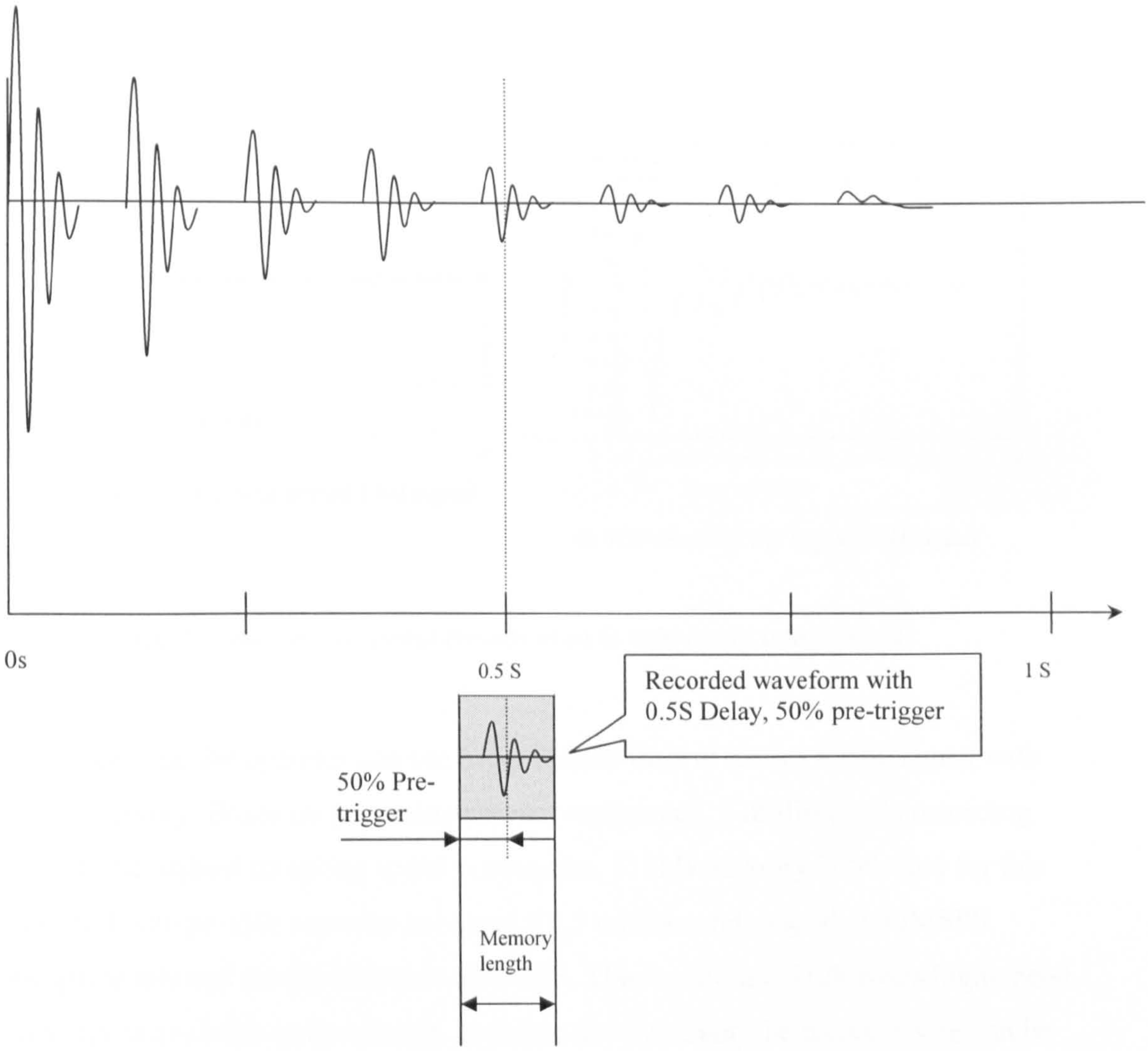
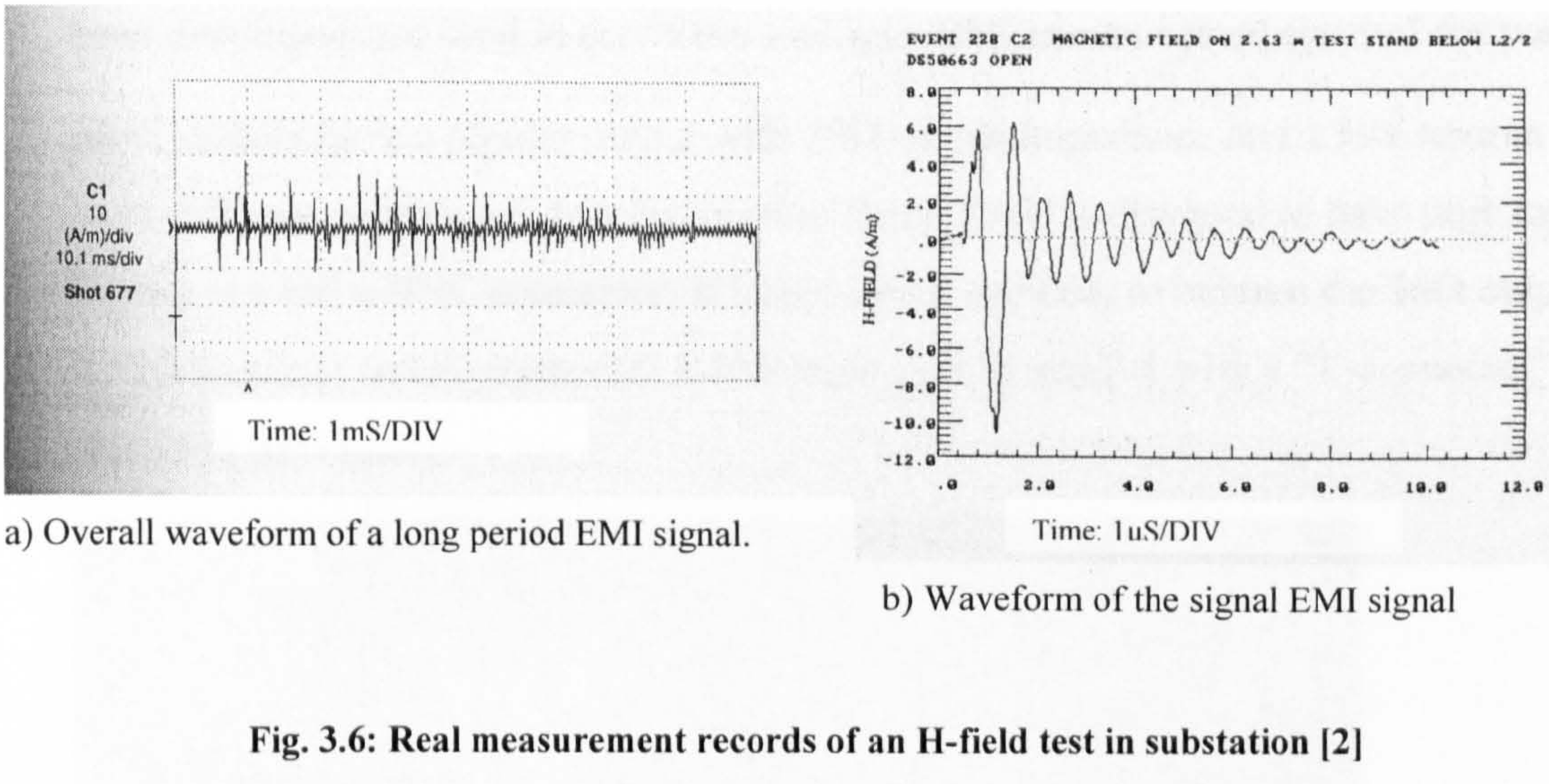


Fig. 3.5: Using Trigger-Delay Function to Measure features within a long-period signal

Fig.3.6 shows the real measurement record in a substation. Fig. 3.6 (a) is the waveform of the whole signal (Magnetic field), which has 100ms length and consists of several so-called micro-pulses. Fig. 3.6 (b) is the waveform of a micro-pulse, which has 12 microseconds length [51].



a) Overall waveform of a long period EMI signal.

b) Waveform of the signal EMI signal

Fig. 3.6: Real measurement records of an H-field test in substation [2]

It is clear that the operator can use trigger-delay time to record a long signal with small memory. Based on past measurement experience, 5 milliseconds recording time at the highest sampling speed is adequate. 512kB memory is selected for this design. It can provide capacity to record a 6.5 milliseconds signal at 80MSPS sampling rate and nearly 800ms at 625kSPS. The monolithic 512k bytes high-speed memory is available in the market. In future development, the memory size can be expanded by using a larger chip or more chips.

3.6.4 Input range and input impedance

The full-scale input range of RAU will be 2Volt, from –1V to +1V. In the measurement work, most sensor output signals are bipolar signal within this range. If the output of a sensor exceeds this range, an attenuator will be applied. If the output is too small to take the whole dynamic range, in this case, the measurement resolution will be reduced, an external adjustable amplifier can be used to amplify the measured signal to a adequate level. Although an adjustable pre-amplifier is a common design and can be easily merged with the RAU circuit together on a single board, however, the first version design still leaves the adjustable pre-amplifier outside of the RAU to simplify the prototype.

The prototype RAU will have a fixed input range of –1 V to +1 V. An external adjustable signal conditioning unit can be applied to adapt the measured signal to be suitable for the input range of the RAU. Such stand-alone adjustable amplifiers has been developed and used in the "fibre analogue EMI measurement system" for years.

Most sensors have a bipolar output with 50Ω output impedance and a few sensors have different impedance, to adapter all of them, RAU is designed to have high input impedance and a BNC connector. If long cable is applied, to balance the 50Ω output, a 50Ω terminal can be connected to the input port in parallel with a "T-connecter" as shown in the Fig.3.7.

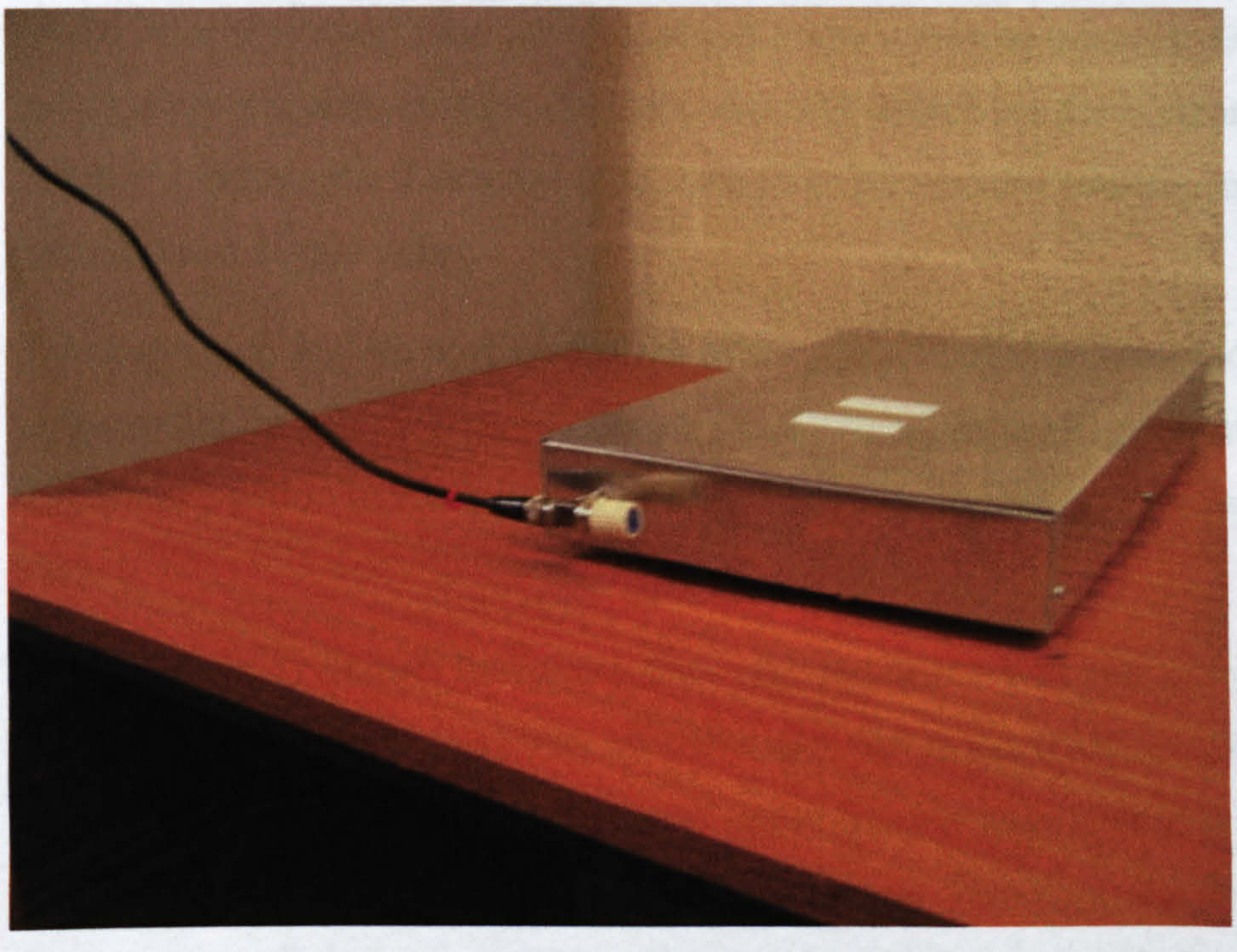


Fig. 3.7: Connection of signal cable, 50Ω terminator and RAU

Adaptors can be used to adapt some sensors output different from bipolar or BNC, such as SMA to BNC adaptor or Differential to bipolar adaptor.

3.6.5 Trigger function

In the single trigger mode of a DSO, once the DSO is triggered, it will stop sampling and hold the signals on the screen and record them in the memory.

In EMI measurements, operators always use the signal level to distinguish the EMI signal, other modes, such as TTL trigger or video trigger, are not necessary. Also,

since the electro-magnetic signals from sensors are always bipolar, the negative trigger-level is not necessary either. Therefore, the RAU has the following voltage trigger mode: when the input signal is greater than the trigger-level, the RAU will be triggered. The trigger-level can be set-up within a range from 0 to +1V with 20mV resolution.

Detailed explanation of the trigger function is presented in section 4.1 and appendix F (Wireless Digital Data Acquisition System User Manual, Page 11)

The trigger function also includes "horizontal control". The horizontal control of the oscilloscope decides which part of the measured signal should be captured on the screen or memory and takes which position of the screen or memory. Different oscilloscope manufactures use different term and definitions for horizontal control. The RAU follows the Tektronix style, using two parameters: pre-trigger (or trigger position) and trigger delay.

The pre-trigger decides how much time of the signal should be recorded before the trigger-point. In other words, pre-trigger is used to adjust the trigger-point's horizontal position in the screen or memory. The adjustment range is from 0% to 99%.

The trigger-delay defines how much time after the primary-trigger-point, where the signal meets the trigger condition, should elapse before the RAU responds to the trigger action. In EMI measurement, the trigger delay is usually used in the situation where the point to be measured is behind a primary-trigger-point over the whole memory range. Subsection 3.6.3 has illustrated such application (Refer to Fig. 3.5). For typical EMI measurements, the 5 seconds maximum delay time is adequate.

In RAU a 19-bit counter, which is clocked by the sampling clock, will be used to generate up to 6.5 seconds delay at 80MSPS.

3.6.6 Power supply

As there is no conveniently available power supply in the switchyard, the RAU has to use a battery as the power source. Previous experience on EMI measurements have shown that most measurement work can be finished within 1 or 2 hours after all

the equipments has been installed. 4 hours battery duration should be adequate for most of the measurement work.

This battery or battery group will be placed inside the screened enclosure with the other RAU circuits together.

3.6.7 Communication interface

The RAU is connected to a wireless modem and communicate with the PC through the wireless modem. After examining the available wireless products in the market, several models, which have acceptable performances and reasonable prices, were selected. All of them have a serial port (RS-232, RS-422 or TTL) to exchange data with the host. More details of these wireless products are listed in chapter 5—"The wireless data communication network".

The development schedule for the whole measurement system is to make the RAU first, then connecting the RAU and PC with an RS-232 cable. With the cable link, the commission and debugging work of the RAU can be done. After the RAU is ready, the cable link can be replaced with a wireless link.

As the final wireless product to be used for this project had not been finally selected when the prototype RAU was being designed, the prototype RAU has to reserve three serial ports for different wireless modems: RS-232, RS-422 and TTL.

Obviously, apart from the serial port, the communication interface also needs some software functions, such as data encoding and decoding, which need an intelligent component. Thus, an embedded CPU is included in the RAU design.

3.6.8 Enclosure

Considering the electromagnetic environment in the substation, all the parts of RAU have to be well screened. The RAU will have a metal enclosure to contain the circuits and support them. The panel will have a switch and some indicators, as well as all the connectors.

3.6.9 Specification

In summary, the profile of the RAU can be listed below, it is also the specification of the RAU.

1) 8-Bit A/D and 1/128 resolution, 40dB or above dynamic range (full-scale).

2) Up to 80MSPS sampling rate, 8 selectable shifts.

3) 20MHz bandwidth.

4) 2 Volt fixed input range (+1V to –1V).

5) A BNC connector with high input impedance.

6) 512k bytes memory.

7) Adjustable pre-trigger and 0-6 seconds trigger-delay range.

8) Inside rechargeable battery(s) lasting 4 hours or more.

9) An embedded CPU carrying out control and communication functions.

10) RS-232, RS-422, TTL serial ports for connection to wireless transceiver.

11) Metal enclosure providing adequate EMI immunity.

Fig.3.8 shows the structure of RAU.

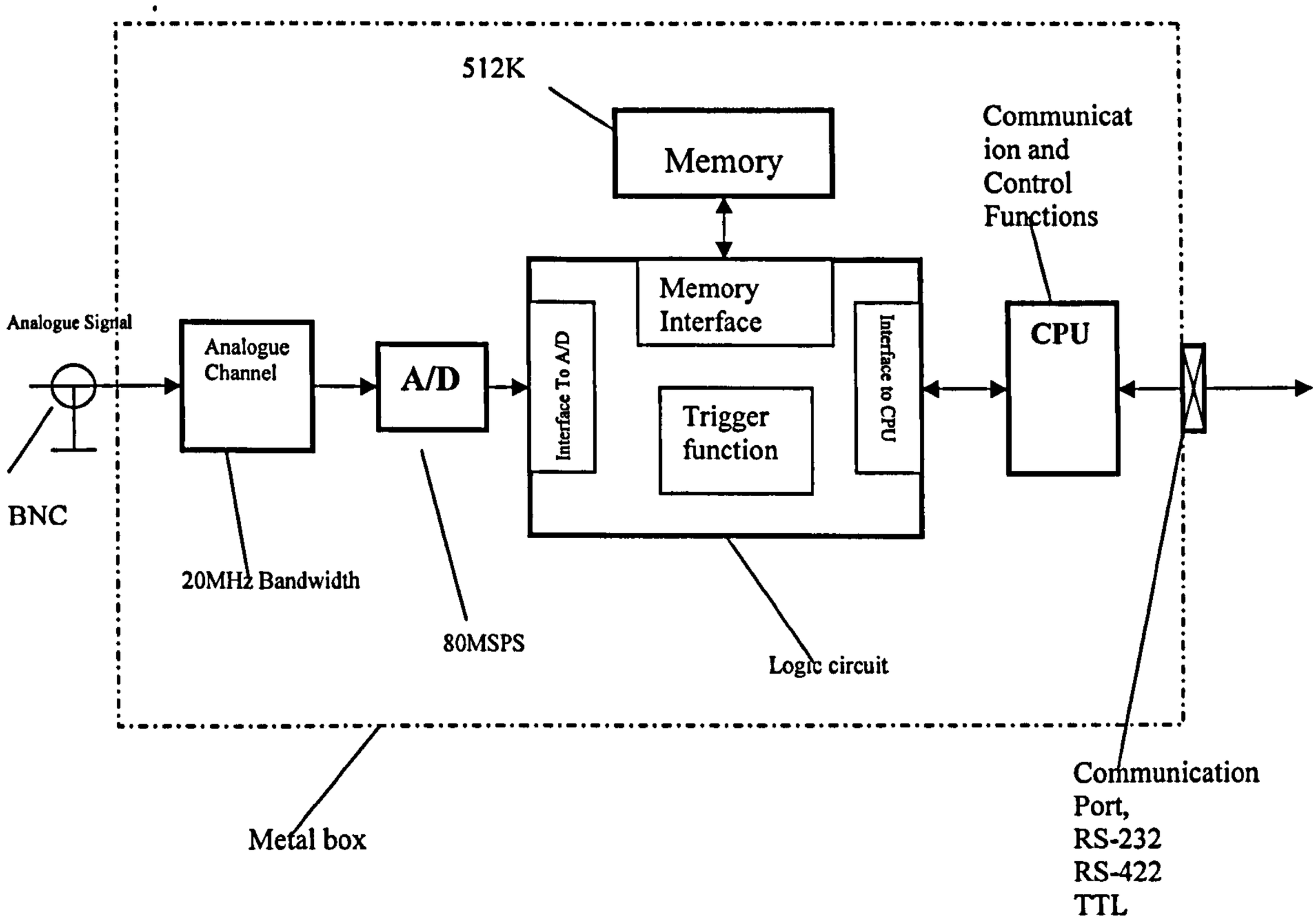


Fig. 3.8: Functional profile of RAU

This section (3.6) gave a functional design for the RAU. Section 3.7 will present the technical solution and give a pre-design of RAU.

3.7 Overall design of RAU- principles and techniques

The overall design stage for an electronic product is the stage after functional design and before the detail design. It provides the technical solution and the development solution. Generally, a technical solution selects proper techniques, examines the principles, selects suitable components, builds a structure of the system and verifies the whole structure. The development solution divides a complex system into several parts, defines the interface between them and arranges the development team or working schedule for them. In this section, the overall design of the RAU will fulfil

all the general tasks and as prototype design, it also needs a reserve design margin for future updates.

The RAU is like a DSO working at a single-trigger mode, therefore the DSO design can be referred for the RAU design. However, the references are very limited because DSO' manufacturers, unlike television manufacturers, who provide circuits to users, do not release their designs. Only the basic principles of DSO can be found in a few books. It was therefore necessary to achieve the target functions based on available techniques and components.

The block diagram of the RAU is given in Fig. 3.18. Summarising the overall design, the profile of the RAU has been formed as follows:

The analogue signal is input to the RAU and is digitised by A/D converter ADC08100, the digital data is then buffered in a 512KB SRAM ALL7C34096, which works in a cycle mode to make a FIFO. When the analogue signal is greater than the trigger-level, an original trigger signal is generated, starting a logic-delay timer. After a certain delay time, the final trigger signal is asserted. This final trigger signal will stop writing new data to SRAM. After that, a micro-controller AT89c52 can read out the 512 kilo bytes data from SRAM. The data can then be sent to a remote PC. The logic functions are implemented by a CPLD component XC95288XL. RAU consists of a 4-layer PCB containing high-speed circuits and a double side PCB containing other low-speed circuits. The two PCBs are connected by a 40-core flat cable. All the RAU parts are enclosed within a metal box.

3.7.1 Sampling and storing principle for RAU

A digital storage oscilloscope is also known as a sampling oscilloscope. In contrast, traditional oscilloscopes are known as real-time oscilloscopes. It implies that DSO is based on a sampling action. The sampling process for a DSO is that, at every certain time interval, it samples and holds an analogue signal point, digitises it to an 8-bit code, and records these codes into a memory. Fig.3.9 illustrates the sampling process:

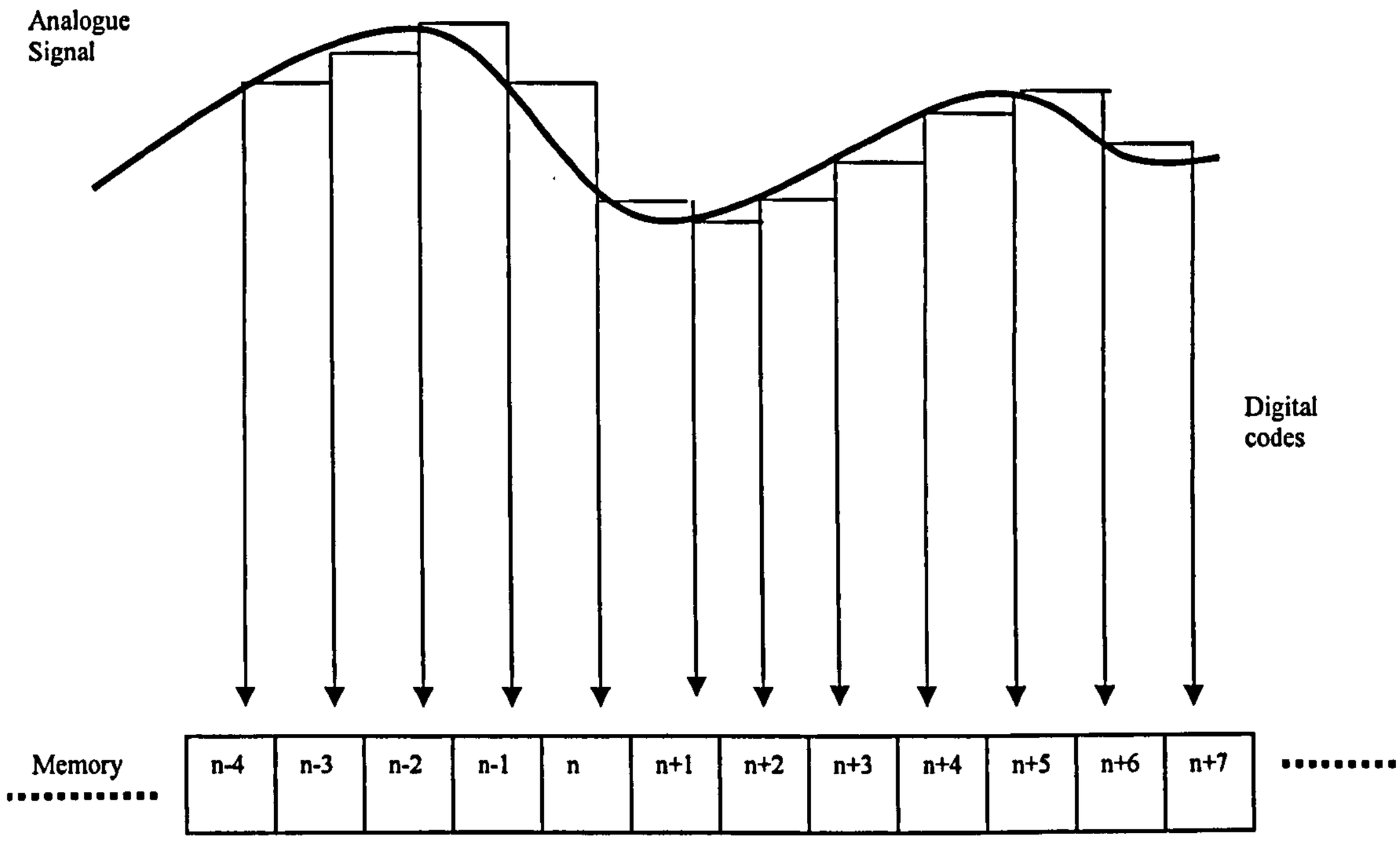


Fig. 3.9: Process of sampling and storing waveform

In the Fig.3.9, the horizontal axis represents time. The codes of sampled points are stored in the memory units from address "n-4" to "n+7". If the sampling frequency is greater than the Nyquist frequency for the analogue signal, the data stored in memory can then be recovered as the original waveform [53]. The reason digital oscilloscopes store measured signals but do not display them directly has been specified in chapter 2 and, for convenience, it is briefly repeated here:

A storage oscilloscope can hold a transient signal in memory by either pressing the "stop" button in auto-trigger mode or setting-up a proper trigger condition in single-

trigger mode. After that, the captured signal can be displayed as long as the operators require. In contrast, real-time oscilloscopes can only display a repetitive signal.

It is clear that the storage mechanism is used to hold a transient signal. DSOs use trigger function to recognise the transient signal, e.g. by setting up a proper trigger level the DSO can recognise a transient signal with significant amplitude. However, transient signals are usually unforeseen, so when the DSO recognised the transient signal and start to record it, it has past. So, logically, the record action (sampling and storage) must start before the transient event happens and must be on-going when the transient event happens. Since nobody can exactly predict when the unforeseen event will be happening, to measure an unforeseen transient signal, the DSO may have to start recording a long time in advance. On the other hand, the memory size is limited, so the DSO records the almost endless signal period with a limited memory using "Roll Mode".

"Roll mode" has been explained by Ian Hickman in his book " Oscilloscope". Fig.3.10 shows a block diagram of the original DSO [50].

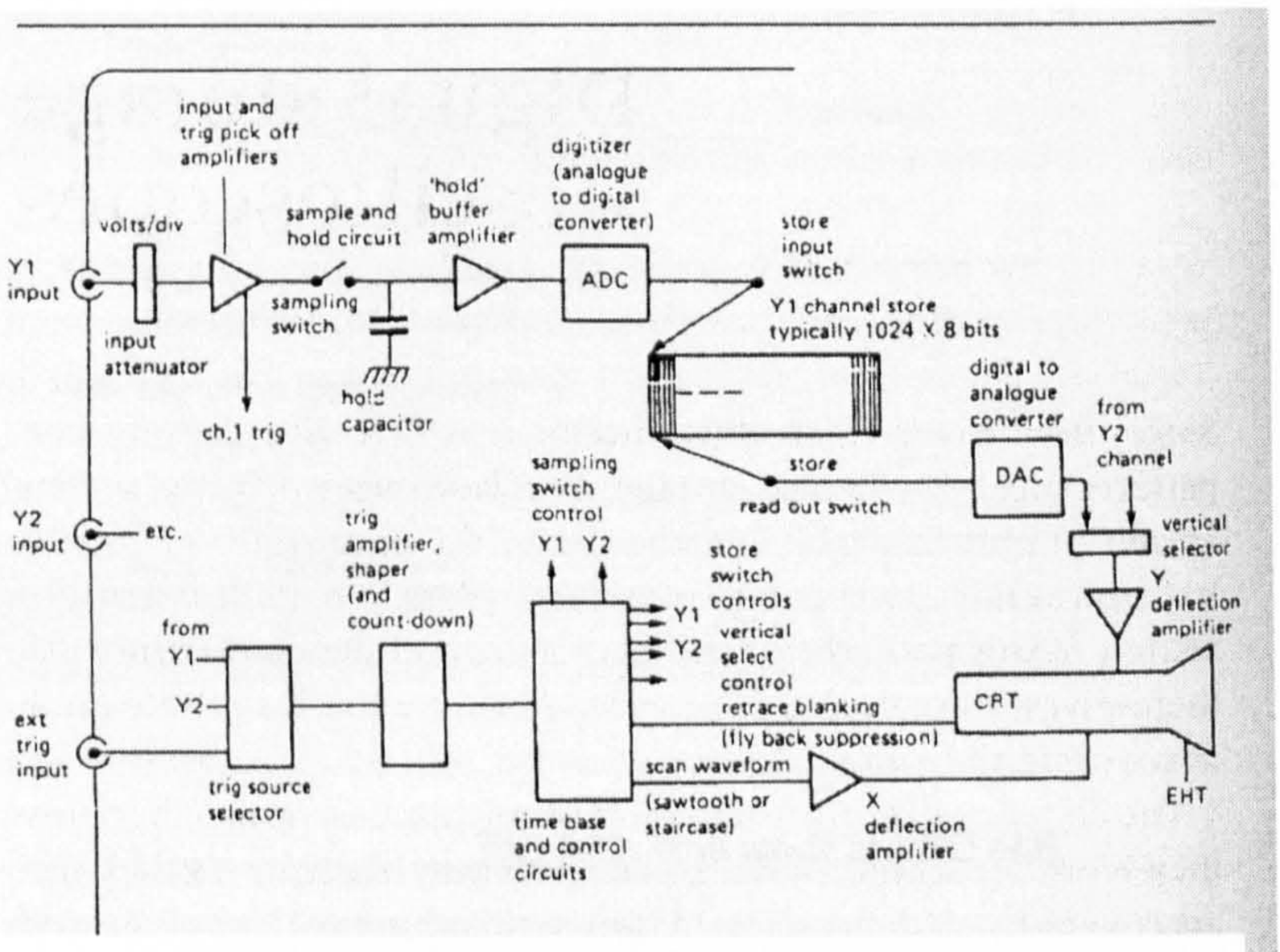


Fig. 3.10: Simplified outline block diagram of typical DSO [49]

According to Ian Hickman, "roll mode" makes DSO different from conventional oscilloscopes. To explain the "roll mode", he gave an example of a DSO with 1024 bytes memory, which can buffer 1024 sample points as shown in Fig.3.11. The process of the roll mode is described as follows: When sampling starts, the samples will be stored into the memory from position 0 to position1023. After 1024 samples the memory is full and a new sample will take position 0 and rewrite the memory. The memory is thus cyclic. It is like a loop of recording tape, earlier information is replaced continuously by the later [50].

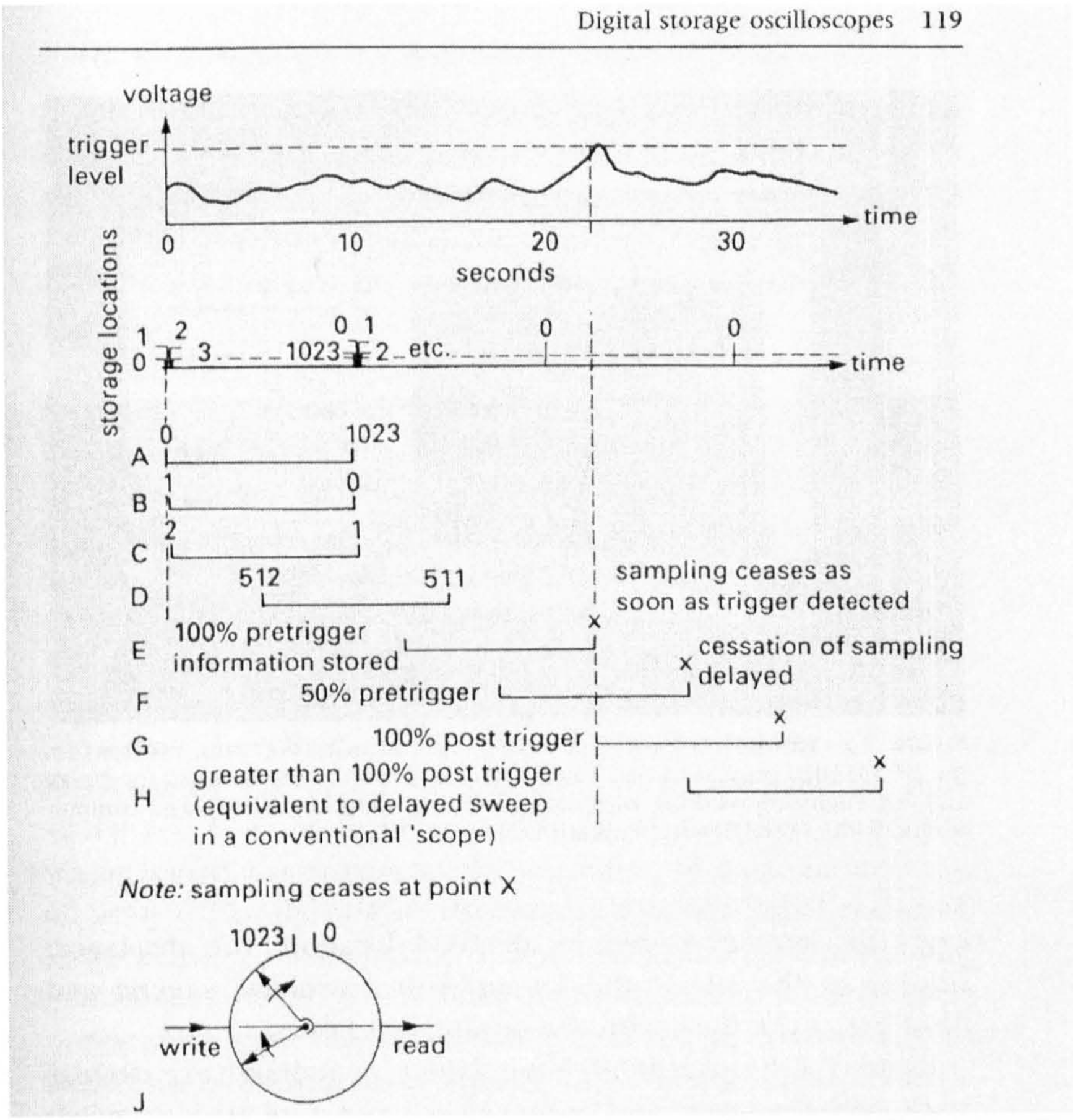


Fig. 3.11: Roll mode in DSO [49]

In single-trigger mode, once a DSO is triggered, after a certain delay time, it stops the writing operation. At this moment, the memory holds the signal around the trigger point. The delay time determines how much of the memory records the signal after the trigger point. The rest of the memory records the signal before the trigger

point, i.e. pre-trigger in Fig.3.11. The data can then be read out from the memory for displaying or downloading.

The RAU also employs "Roll Mode". As shown in Fig.3.12, A 512K memory with an increasing counter is used to build a FIFO (First-In-First-Out) buffer. When A/D completes a new sampling, the byte (8-bit code) from A/D is stored in the memory and the oldest (512,000 samples ago) byte in the memory will be discarded (covered by new byte). Since the 19-bit increasing counter runs circularly, the 512k (2^{19}) memory buffers the data circularly.

The timing sequence diagram of the sampling and storing process is shown in Fig.3.13 (time-delay information is not included).

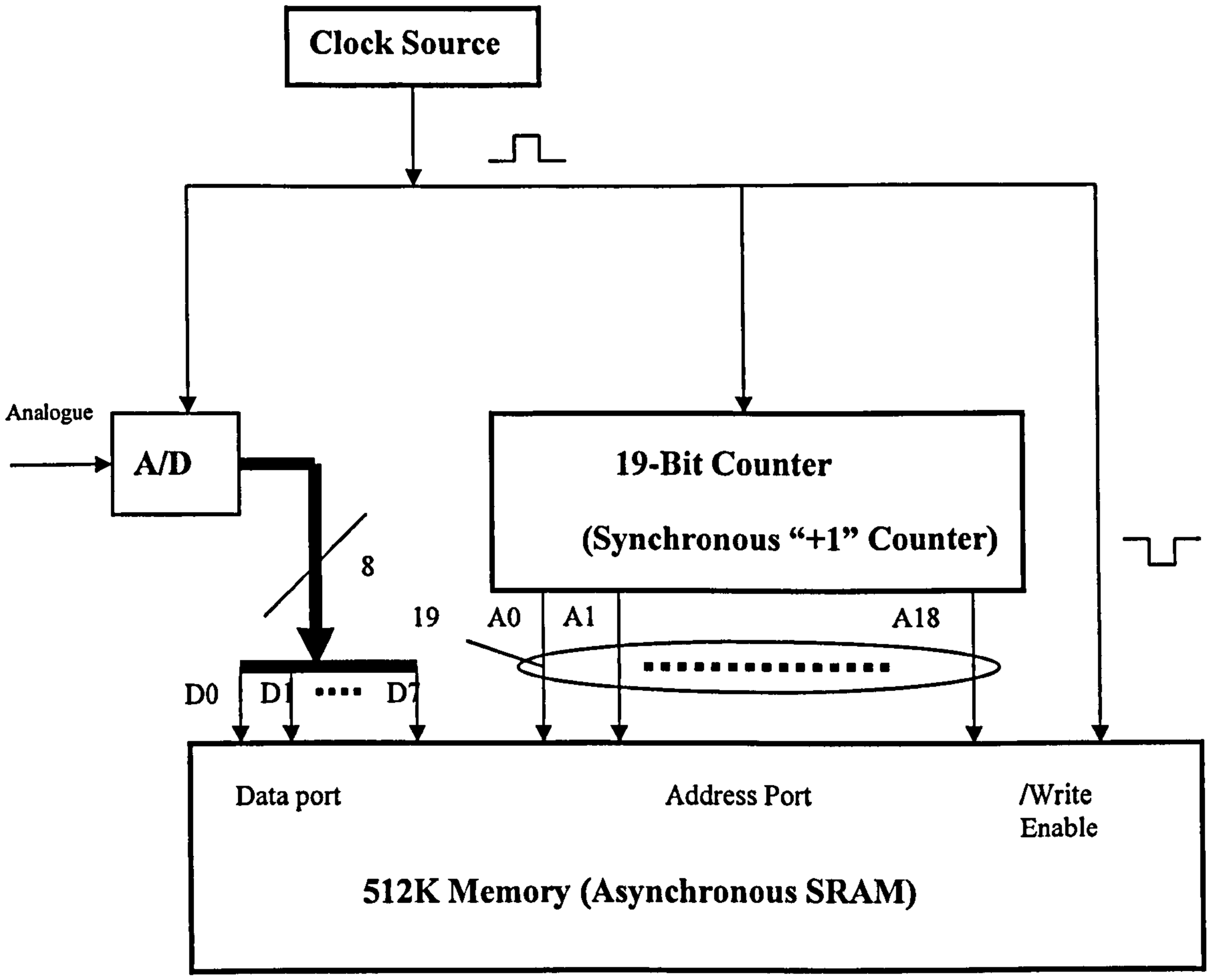


Fig. 3.12: Simplified sampling and storing logic

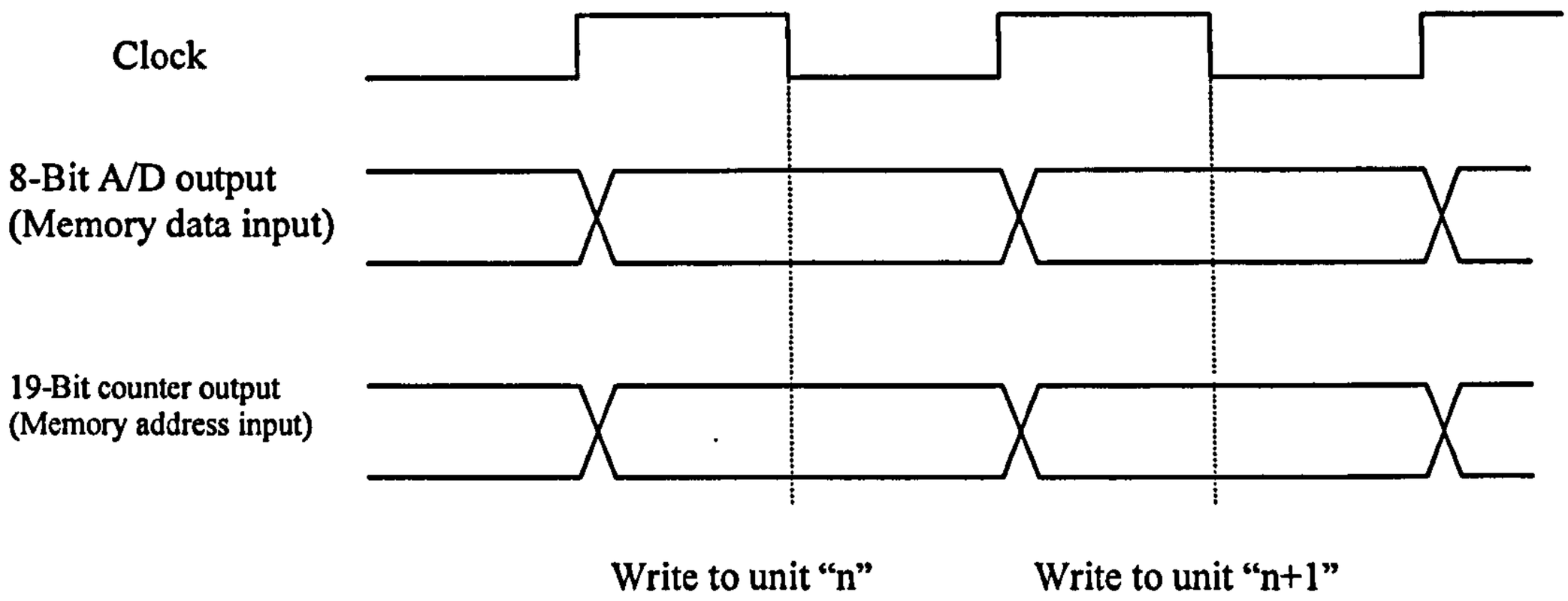


Fig. 3.13: Timing of sampling and storing process

Where the clock source is a square oscillator, it provides a "converting clock" to the A/D, as well as a "counting pulse" to the 19-bit counter and "writing pulse to 512k memory.

The A/D starts sampling at the positive edge of the clock, the counter also increases at the positive edge. Before the negative edge of the clock, the output of the A/D and the output of the counter have been established. The negative edge then writes data from the A/D into the memory unit. The 8-bit output of the A/D is the "data" input of memory, the output of the 19-bit counter is the "address" input of 512k memory and the clock pulse is the "write" pulse (low active) of the memory. This operation is repeated in every clock period. The new data is thus stored in a new address. The address is increased in "1" from 0 to 514,288 (512k) circularly.

By this way, the RAU continuously writes the data into the memory circularly and the memory always contains the latest 512kB information of the input signal. This process is shown in Fig.3.14. Assuming the A/D sampling rate is 80MSPS and memory size is 512kB (1kB=1024 bytes), thus, after the initial 6.5ms (power up), the memory is full. Then, it always contains the last 6.5ms (512k/80MSPS) signal.

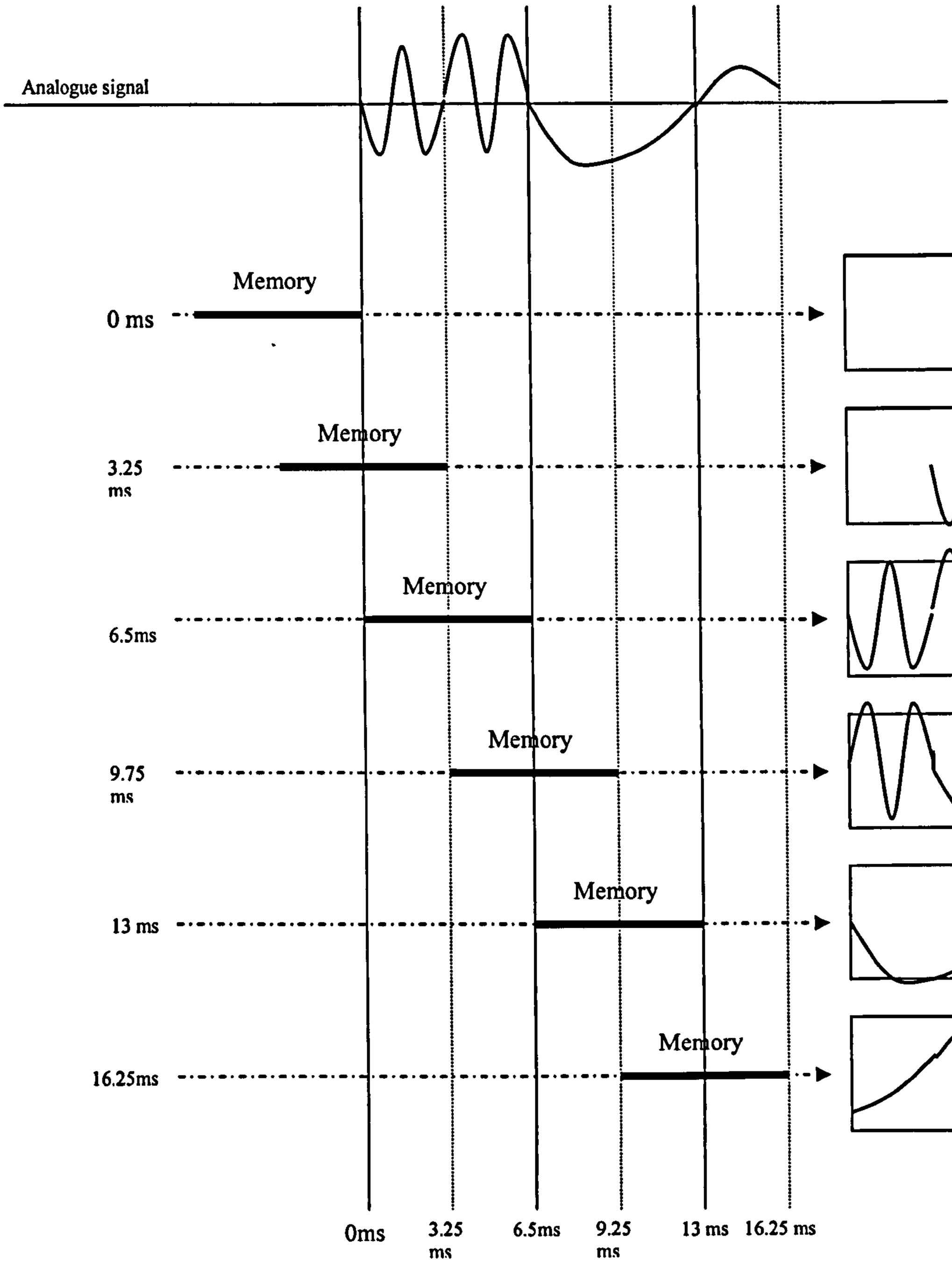


Fig. 3.14: Process of storing operation (FIFO)

In the top of Fig.3.14, the measured signal is represented with the time on the horizontal axis and amplitude on the vertical axis. Six situations are listed there, which represent the positions of the memory at different moments. The windows in the right side show the waveforms recorded in the memory at those moments. In the figure, it can be seen that the memory is always filled with the latest 6.5 milliseconds signal. At moment 0, the memory is empty; at 6.5ms; it contains the waveform from 0 to 6.5ms; at 13.5ms, it records the signal from 6.5ms to 13ms and so on until the storage is stopped. When the memory stops storing new data, the memory will keep the information of the last 6.5ms signal before the stop point.

The question of when the storing action should be stopped and how to stop it are now considered.

3.7.2 The trigger principle of RAU

Obviously, the "stop" action can capture a signal in roll mode. DSO users can use trigger condition to recognise the signal to be captured. E.g., in EMI measurements, the transient EMI pulse always has significant amplitude. If the operator has set-up a proper trigger level for the DSO, the EMI signal will trigger the DSO and be recorded. The signal point at which the trigger condition is met, is defined as the trigger-point. If the storing operation is stopped at the moment of trigger-point, the memory will contain the waveform before trigger-point. E.g. in RAU, the whole memory will record 6.5ms signal at 80MSPS, as shown in (a) of Fig. 3.16. However, sometimes, operators want to observe not only the waveform before the trigger point but also the waveform after it. In that case, the stop action should be delayed after the trigger point. E.g., in RAU if the delay time is 3.25ms (50% of whole recording time), the memory will record 3.25ms waveform before trigger point and 3.25ms waveform after trigger point, as shown in (b) of Fig.4.16. Furthermore, if the desired signal is behind the trigger point for a long time, as shown in (d) of Fig.3.16, the RAU will provide a longer delay time to capture it. As has been discussed in the functional design, the delay time of the RAU can be set-up up to a maximum of 1024 times of the whole memory, that is roughly 6.5 seconds at 80MSPS, The principle of the trigger function can be implemented in the RAU by the logic diagram shown in Fig.3.15.

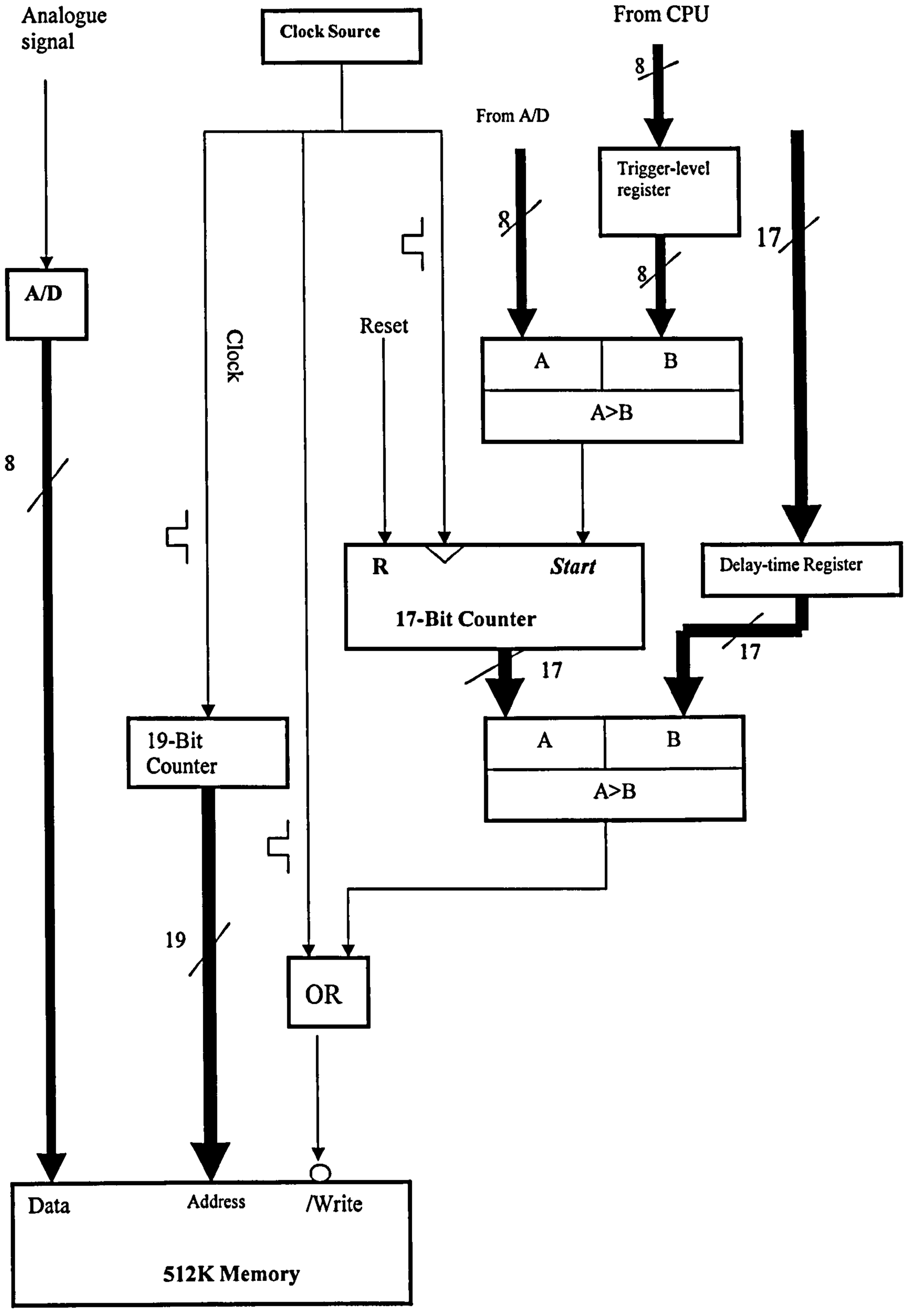


Fig. 3.15: Simplified trigger logic

In Fig.3.15, the number marked on the bus (thick black line) means the number signal lines in the bus.

A comparator is applied to compare the trigger level with the measured signal. Once the measured signal exceeds the trigger-level, the comparator will generate a logic signal, which is defined as the original-trigger-signal. The original-trigger-signal starts a 17-bit timer to calculate the delay time. Once the delay time has elapsed, the logic circuit will generate a logic signal to stop writing to memory. This signal is the defined as the final-trigger-signal in this thesis. The timer is achieved by a digital comparator, which compares a 17-bit counter and a 17-bit delay-time-register. The 17-bit counter is clocked by a sampling clock and started by the original-trigger-signal. The delay-time register is pre-loaded with the value of the delay time, which is represented in the pulse number of the sampling clock. The original-trigger-signal starts the 17-bit counter. This counter then counts the sampling clock. Once the counter output is equal to the value set-up in the delay-time-register, the comparator will output a logic signal (final-trigger-signal). The delay time is set-up by the users at the PC and transmitted to RAU. The embedded CPU will then write it into the delay-time-register.

The "Delay-time" is used for horizontal control. It is defined as the time between trigger-point and the moment to stop storing. However, the conception of "delay time" is used for the machine and implemented by the circuit. Since most users are familiar to using a DSO, the RAU will provide a control environment with a PC, which follows the DSO style.

Different DSO manufacturers use different terms and definitions for horizontal control. The RAU follows the Tektronix style giving the operator two variables for horizontal control: "pre-trigger" and "trigger-delay".

"Pre-trigger" means the duration before the trigger-point at which the DSO starts to record the signal. "Pre-trigger" is defined as a percentage of the memory or screen. That means in the whole memory or screen, which portion is used to record the signal before the trigger-point. Of course, the remaining memory or screen is used to record the signal after the trigger-point. The remaining portion is called "post-trigger", it equals "100% - (pre-trigger)". It can be seen that, this percentage determines at which position the trigger-point should be in the entire memory or

screen. Because of this, "pre-trigger" is some times in the user manual is also called the "trigger position".

The "Trigger-delay" is defined as the time after the trigger-point, at which the DSO reacts to the trigger event. That is to say, "trigger-delay" defines another point, which is behind the trigger-point in "trigger-delay" time. This point will be recorded in the memory or screen and take the position, which the "pre-trigger" determines. In normal measurement, the "trigger-delay" is usually set-up to "0". It is only used to measure the signal behind a trigger-point in long duration [54].

Following the Tektronix style, in this wireless EMI measurement the PC provides a control environment for users to determine the "pre-trigger" and "trigger-delay" for horizontal control. Unlike the users point of view, the circuit of the RAU implements "delay time" for horizontal control. The difference between them is that the machine always acquires the signal and stops acquiring in a "delay-time", whereas the user let the machine start acquiring before "trigger-point" in "pre-trigger" time.

To prevent confusion in defining the term of "trigger-delay" and "delay-time", in the rest of this thesis "delay-time" is named as "logic-delay-time" or "Logic-delay", it is not used for the user but only used for the machine.

The three terms "pre-trigger", "trigger-delay" and "logic-delay-time" have different meanings. Fig.3.16 explains their relationship:

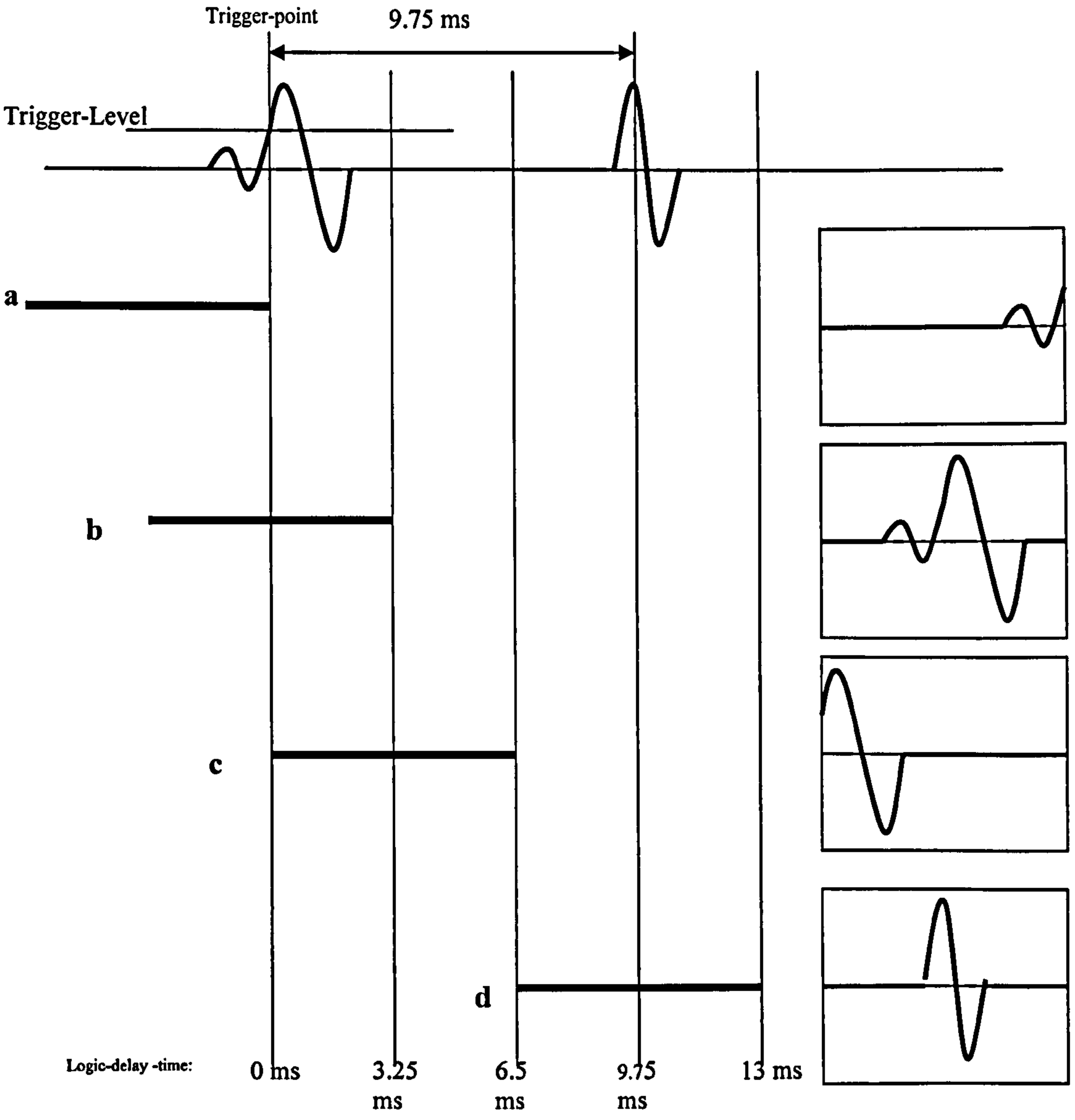


Fig. 3.16: Different delay time capture different signal wavefrom

a) stop storing as soon as the RAU is triggered, i.e. 0ms logic-delay-time. It records the 6.5 ms signal before trigger point, i.e. 100% pre-trigger and 0 trigger-delay

b) stop storing in 3.25 ms after trigger point, i.e. 3.25 ms logic-delay-time. It records 3.25ms signal before the trigger point and 3.25 ms signal after the trigger point implements 50% pre-trigger and 0 trigger-delay.

c) stop storing in 6.5 ms after trigger-point, i.e. 6.5 ms logic-delay-time. It record 6.25 ms signal after the trigger point, i.e. 0% pre-trigger and 0 trigger-delay

d) if the desired measurement event is not around the trigger point but behind it 9.75 ms and the user wants to record the event in the middle of the memory. The circuit stops storing in 13ms after trigger-point (9.75 plus 3.25), i.e. 13ms logic-delay-time. It records 3.25 ms signal before that event and 3.25 ms after that, i.e. 50% pre-trigger and 9.75 ms trigger-delay.

As shown in the 3.16 it is clear that logic-delay-time has the following relationship with other two horizontal control parameters.

$$Logic\_Delay\_Time = (100\% - pre\_triiger) \bullet T + trigger\_delay \qquad \textbf{(Equation 3.1)}$$

Where Logic-Delay-Time is presented in the time dimension. T is the time taken to fill the whole memory with sampled data at a certain sampling rate, e.g. the memory size of the RAU is 512 kB, when the sampling rate is 80MSPS, T is around 6.5ms.

Equation 3.1 can also presented by memory size without considering the sampling rate:

$$Logic\_trigger\_Delay = 100\% - pre\_trigger + trigger\_delay \qquad \textbf{(Equation 3.2)}$$

All the parameters in Equation 3.2 are presented as a percentage of the whole memory.

Since the minimum adjustable delay time step is 1% of the whole memory and the largest logic-delay-time is 1024 times of the whole memory length, the whole adjustable range has 102400 (1024*100) steps, which can be covered by 2^{17}. Therefore, as shown in Fig.3.15, a 17-bit counter is applied to calculate the delay-time.

The operator inputs the "pre-trigger" and "trigger-delay" to the PC. These parameters will be translated to logic-delay-time by the embedded CPU and written to the logic-delay-time-register.

3.7.3 Embedded CPU and acquisition control

In the RAU, the embedded CPU is incorporated to receive the control command from the PC and to control the acquisition. It also needs to read data from the acquisition circuit and send them to the PC. The control codes that come from the PC are trigger level, trigger delay, sampling rate, reset, etc. Therefore, a logic circuit should have some registers to contain these codes. These registers make a control code array. The embedded CPU can write control codes to the registers by a "write" operation. The next example shows the control process for the PC to set-up the RAU's trigger-level to 0.5V.

The full scale of A/D is 2 Volt (from -1V to +1V), which is represented by the digital code from "0" to "255", 0.5 volt accordingly equals digital code of 192 (decimal) or 11000000(binary). The PC sends the command to the embedded CPU: "set trigger level to 11000000B" (this data transmission process will be explained later in chapter 5). The embedded CPU then writes the binary code "11000000" (0.5V) to the register in the logic circuit. This register is one input to an 8-bit comparator. Another input to the comparator comes from the A/D. Therefore, when the A/D output is greater than 11000000B, i.e. the input analogue signal is over 0.5V, the comparator will assert the original-trigger-signal.

3.7.4 Outline of the RAU

Apart from the above, the RAU also needs a power supply, communication unit and other functions. The block diagram of the whole RAU is shown in Fig.3.17.

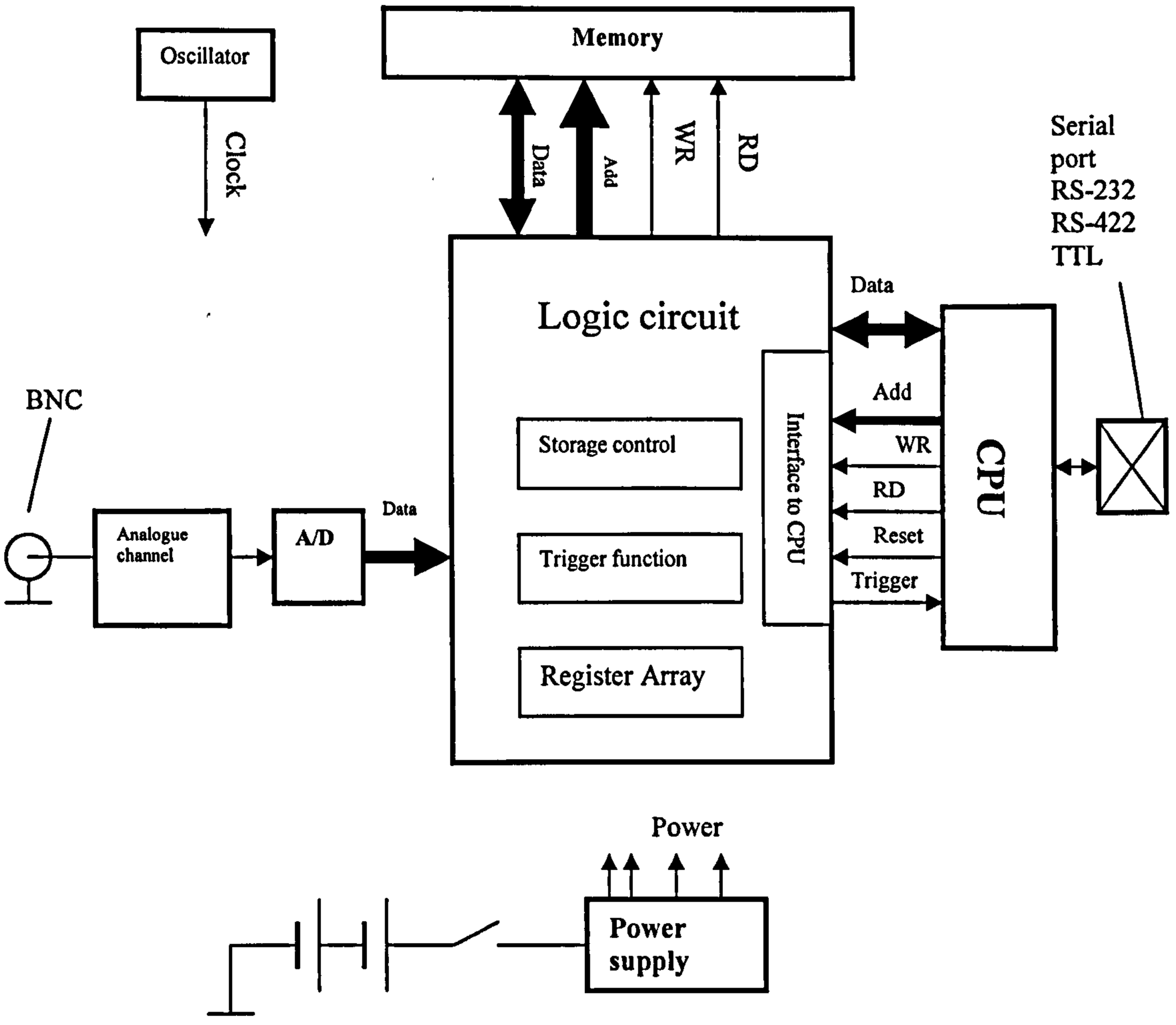


Fig. 3.17: Outline of RAU

3.7.5. Components selection

Most general digital ICs have a TTL/CMOS interface. Hence, as long as the speed is adequate, designers would prefer TTL/CMOS components for prototype design. In this design of RAU, although the logic circuit should be working at a high frequency (switching mode), which almost approaches the limitation of the components having a TTL or CMOS interface, the speed still can be achieved by TTL/CMOS

components. Therefore, in the RAU, the digital components are all TTL/CMOS compatible.

For the overall design of the RAU, only the key components, which control the whole system, are selected and discussed in this section. Other associated common components will be mentioned in the detailed design.

3.7.5.1 A/D converter

As has been specified in 3.6, the RAU has 8-bit resolution and at least 50MSPS sampling rate. International Semiconductors products ADC08100 has been found to meet these requirements. ADC08100 is a low-power, 8-bit, monolithic analogue-to-digital converter with an on-chip track-and-hold circuit. Being optimised for low cost, low power, small size and ease of use, this product operates at conversion rates of 20 MSPS to100 MSPS with outstanding dynamic performance over its full operating range while consuming just 1.3mW per MHz [55]. Another important feature of this converter is that it has a TTL/CMOS compatible data interface.

3.7.5.2 Embedded CPU: AT89c52

The embedded CPU should have 8-bit byte-width or more, medium speed, extendable external bus and on-chip UART (Universal Asynchronous Receiver and Transmitter). Atmel's product AT89C52 has been found suitable for this specification.

AT89C52 is one of Atmel's micro-controller (MCU), which belongs to Intel 8051 series based on MCS51 architecture. The 8051 family is one of the most popular micro-controller products [56]

The Atmel AT89C52 is a powerful microcomputer, which provides a highly-flexible and cost-effective solution to many embedded control applications [57]. Also, AT89C52 provides a full duplex UART. The data rate of this UART can be configured up to 115200bps. This data speed is suitable for most wireless modems, and might be selected for this project.

3.7.5.3 Memory—512kB SRAM: ALL7C34096

The memory of RAU should have 512 kilo bytes capacity, 8-bit word-width, a "TTL/CMOS compatible" interface and high speed. To simplify the peripherals of

this memory, an asynchronous static RAM (random access memory) has been chosen. ALL7C34096 from Alliance has been found suitable for this application, which is 4Mbit (512k * 8) asynchronous SRAM (Static RAM) and 12 nanoseconds full-access time (80MSPS). Furthermore, in this product series, Alliance also provides -10ns and -8ns module with the same package and pin-out, thus, the prototype RAU has the capability of increased speed by using faster SRAM without changing the PCB and other components [58].

3.7.5.4 Logic circuit: the application of CPLD (Complex Programmable Logic Device)

The logic functions in the RAU have been described earlier in section 3.6 and illustrated in Fig.3.15 and Fig.3.12 (storage control, trigger control, interfaces etc). It would be too complex to be built by using discrete logic devices such as 54/74 series. Therefore, CPLD components will be used to build this logic circuit. Contemporary CPLD integrates a large amount of logic resource within the single chip (gates, flip-flops and programmable interconnection lines). Users can build any logic design with a CPLD by planning its internal interconnections [36, 59]. The advantage of CPLD has been presented in chapter 2. For further understanding of PLD, readers can read related books [37].

To select a PLD device, the following conditions must be considered: 1.Logic design resource, 2. TTL/CMOS interface and I/O pins, 3. Working speed.

As an estimate, the logic design requires a total of about 150 registers or flip-flops. If using Xilinx CPLD, it needs about 150 macro-cells (one macro-cell contains one programmable register). For safety, 50 macro-cells were allocated as a design margin. Thus the CPLD should have more than 200 macro-cells. Xilinx CPLD XC95288 series has 288 macro-cells, abundant interconnections and gates, which meets the design requirement on logic resource.

The I/O pins of this CPLD need to connect to both 5V and 3.3V interfaces, since the SRAM and A/D converter have 3.3V COMS I/O and the micro-controller here has a 5V I/O. XC95288 series has several operation voltage modules. '95288' module has 5V operation voltage, 95288XL has 3.3 V operation voltage and 95288VL has 2.5V operation voltage, among which, only 3.3V (95288XL) module can be compatible

with both 3.3V and 5V peripherals.XC95288 series has a different footprint from 44-pin to 286-pin with VQFP(Very fine Quad Flat Package), TQFP(Thin Plastic Quad Flat Package) or BGA (Ball Grid Array) packages. The logic circuit in the RAU needs about 80 -100 I/Os (Input/Output pins), hence, the module with144-pins is selected. Considering that the prototype PCB will be soldered manually, TQFP package is selected (other kind of packages are difficult for manual soldering [60, 61, 62].

XC95288XL is available in different speeds: -6ns, -8ns, -10ns, -12ns, -15ns. These numbers stand for the pin-to-pin delay of the CPLD. For example, for -6ns device, an asynchronous signal (only implements combination logic) takes 6ns delay time from an input pin to an output pin. Xilinx also uses index "fsys" to describe the how fast the device implement sequential logic operation. A -6ns product has 200MHz fsys. -6ns product is the fastest CPLD that can be found in Xilinx CPLD products when the author started this project. Thus XC95288XL-6ns-144TQFP was chosen for this design. A software emulation showed that, XC95188XL-6ns-144TQFP achieves 83.2MHz operation speed when it implements the acquisition circuit logic design. The software simulator is provided by CPLD manufacture. It simulates the implement of user's design in PC and simulates the operations. This simulation can approximately calculate the circuit operational speed. For details information please refer to [72].

3.7.5.5 Power supply—Adjustable regulators LM371

As has been mentioned before, the RAU is a battery-powered equipment.

A Yuasa 12V maintenance-free rechargeable sealed lead acid battery has been selected as the power source in the RAU, since this kind of battery and associated charger are common products.

Within the RAU, the circuits need four kinds of DC power supply:

1) +5V DC for micro-controller AT89C52 and the positive power source of Op-Amp. (200mA to 300mA)

2) –5V DC for negative source of Op-Amp. (less than 15mA)

3) 3.3V DC for CPLD, A/D converter, SRAM, etc. (300mA to 500mA)

4) An adjustable DC power supply should be reserved for an unforeseen usage.

5) The RAU also provides the power supply to the wireless modem. This power requirement is different on different modems. (The development work of RAU is undertaken before wireless communication)

It is clear that, the power supply will transform 12V DC to +5V, -5V, 3.3V and an adjustable DC. Two kinds of components can be applied for this purpose. One is switched mode DC/DC converter (or regulator) and another is linear regulator. A linear power supply can provide the current with smaller ripple and less noise, but the conversion efficiency is lower than switch mode power supply. It is well known that, for a prototype design, the power supply needs a big margin in both quality and capacity. In the RAU, a linear regulator is selected for its lower ripple output and better noise-rejection [63]. Although the quality of a switch power supply may be adequate, a linear regulator is safer for a prototype design.

The National Semiconductors product LM317 was selected as power supply components in RAU to generate all the positive voltages. It is a 3-terminal adjustable regulator with 1 Amp maximum output current and a wide adjustable output range. This component gives the circuit design enough margin and flexibility. Furthermore, comparing with other voltage-fixed regulator, LM317 has better anti-noise performance [64, 65]. The negative 5 volt will be generated by +5V using a Voltage inverter.

3.7.6. Circuits arrangement

Properly dividing a complex system into several parts can ease the difficulty of development and reduce the risk of a whole system failing due to a single fault.

In the RAU, apart from connectors, switches and batteries, other components must be placed on PCB(s). PCBs are used to support the components and lay out the connecting tracks between components [66].

Reviewing the description of the RAU, it can be seen that the components of logic circuits (CPLD), A/D converter and memory have a high-density pin-out and work at a high-speed, whereas the micro-controller, power supply and communication

components have lesser density pin-out and work at low-speed. To carry the dense tracks and high-speed signals requires multi-layer PCBs. For the low-density circuit and the low speed signal, a double sides PCB is adequate. Thus, the circuit of the RAU is divided into two boards. One board includes an A/D converter, logic circuit and memory. This board implements the functions of acquisition and here after, it is named as the "Acquisition Board". Another board includes micro-controller, power supply and communication ports. Since the main function of this part is implemented by the AT89c52 (the embedded CPU) and its software, here after, this board is called the "CPU Board".

Xilinx CPLD 95288 is suggested to use a 4-layers PCB to carry it [67]. Therefore, the Acquisition Board is designed to be a 4-layer PCB. The CPU Board will be a double side PCB.

Such a division also makes the interface between the two parts to be simplest.

Fig.3.18 shows the interconnection between Acquisition Board and CPU Board and whole RAU's structure.

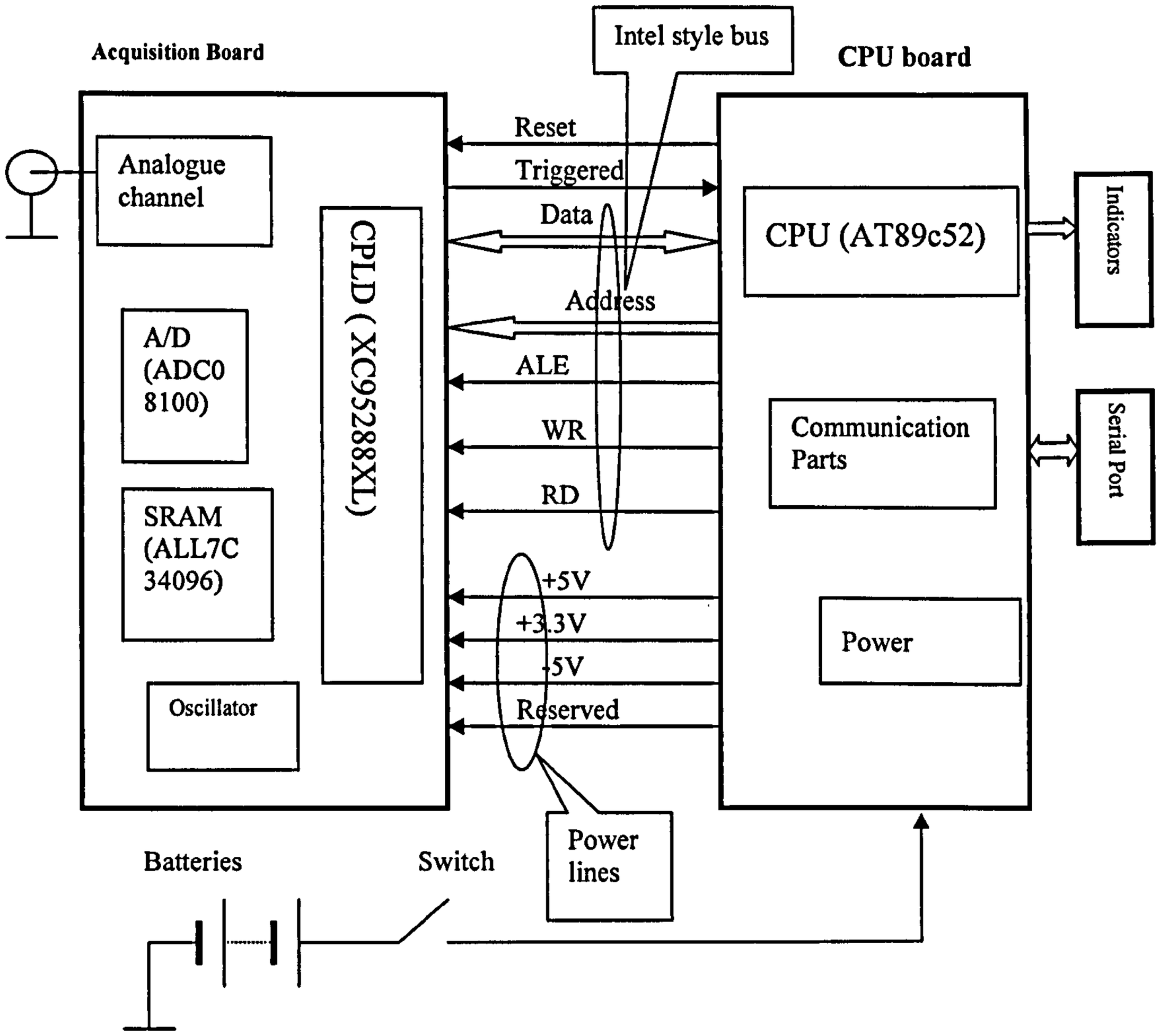


Fig. 3.18: Interconnection between CPU board and Acquisition Board and the structure of whole RAU

Explanation of the signals:

Reset signal (TTL signal, high level active, from CPU Board to Acquisition Board): it initiates the logic circuit, releases previous triggered state and restarts a new measurement.

Triggered signal (TTL signal, high level active, from Acquisition Board to CPU Board): it informs micro-controller about the triggered state of acquisition.

Power lines: (power supply, from CPU board to Acquisition Board) they provide the power supplies of +5V, -5V, +3.3V and an adjustable power supply (reserved for spare use)

Intel-Style Bus: It is a standard bus, designed to link the peripherals to the Intel-style CPU directly. It also can be adapted to a Motorola-style CPU by simply adding a logic circuit [68]. Through this bus, a micro-controller (Intel-Style CPU) exchanges data with the Acquisition Board, such as to write data to or read data from an external memory. This Intel-style bus consists of a data bus (8 lines), an address bus (4 lines) and a control bus (WR, RD and ALE).

Further explanations about the Intel-Style Bus and the reading/writing operation of the micro-controller are presented in the book [69].

The interconnection between the CPU Board and the Acquisition Board can be implemented with a 40-core flat parallel cable with 40-pin plugs on each side. Accordingly, 40-pin sockets are placed on both CPU Board and Acquisition Board.

Table 4.2 lists the details of the cable. Every signal takes a single line and every power supply takes adjacent two lines. All the power lines are separated by ground lines.

Note:

1) Cable: 40-core "1.27 mm Pitch Standard Ribbon Cable".

2) Cable length: 3 cm.

3) Sockets: 40-pin IDC cable mounting plug.

Table 3.2: Table of Cable 40-Core Flat Cable in RAU

Side A (CPU Board), 40-Pin plug		Side B (Acquisition Board), 40-Pin plug	
Core Number	Signal name	Core Number	Signal name
1	D0	1	D0
2	D1	2	D1
3	D2	3	D2
4	D3	4	D3
5	D4	5	D4
6	D5	6	D5
7	D6	7	D6
8	D7	8	D7
9	A0	9	A0
10	A1	10	A1
11	A2	11	A2
12	A3	12	A3
13	INT0	13	TRIGGERED
14	T1	14	(SPARE)
15	(SPARE)	15	(SPARE)
16	ETRIG	16	ETRIG
17	A15	17	A15
18	ALE	18	ALE
19	WR	19	WR
20	RD	20	RD
21	RESET	21	RESET
22	P1.3	22	P1.3
23	P1.4	23	P1.4
24	P1.5	24	REFRESH
25	VCC	25	VCC
26	VCC	26	VCC
27	GND	27	GND
28	GND	28	GND
29	+3.3	29	+3.3
30	+3.3	30	+3.3
31	GND	31	GND
32	GND	32	GND
33	-5V	33	-5V
34	-5V	34	-5V
35	GND	35	GND
36	GND	36	GND
37	RESERVED	37	RESERVED
38	RESERVED	38	RESERVED
39	GND	39	GND
40	GND	40	GND

Chapter 4 RAU (Remote Acquisition circuit)

This chapter will present the details of the RAU. As described before, RAU consists of Acquisition Board, CPU board. Section 4.1 presents the Acquisition Board. Section 4.2 presents the CPU board. In section 4.3, the assembly of RAU is given.

4.1 Acquisition Board

As its name implies, the Acquisition Board is designed to carry out the functions of data acquisition. The block diagram is given Fig.4.1. For schematic design sheet, refer to appendix A.

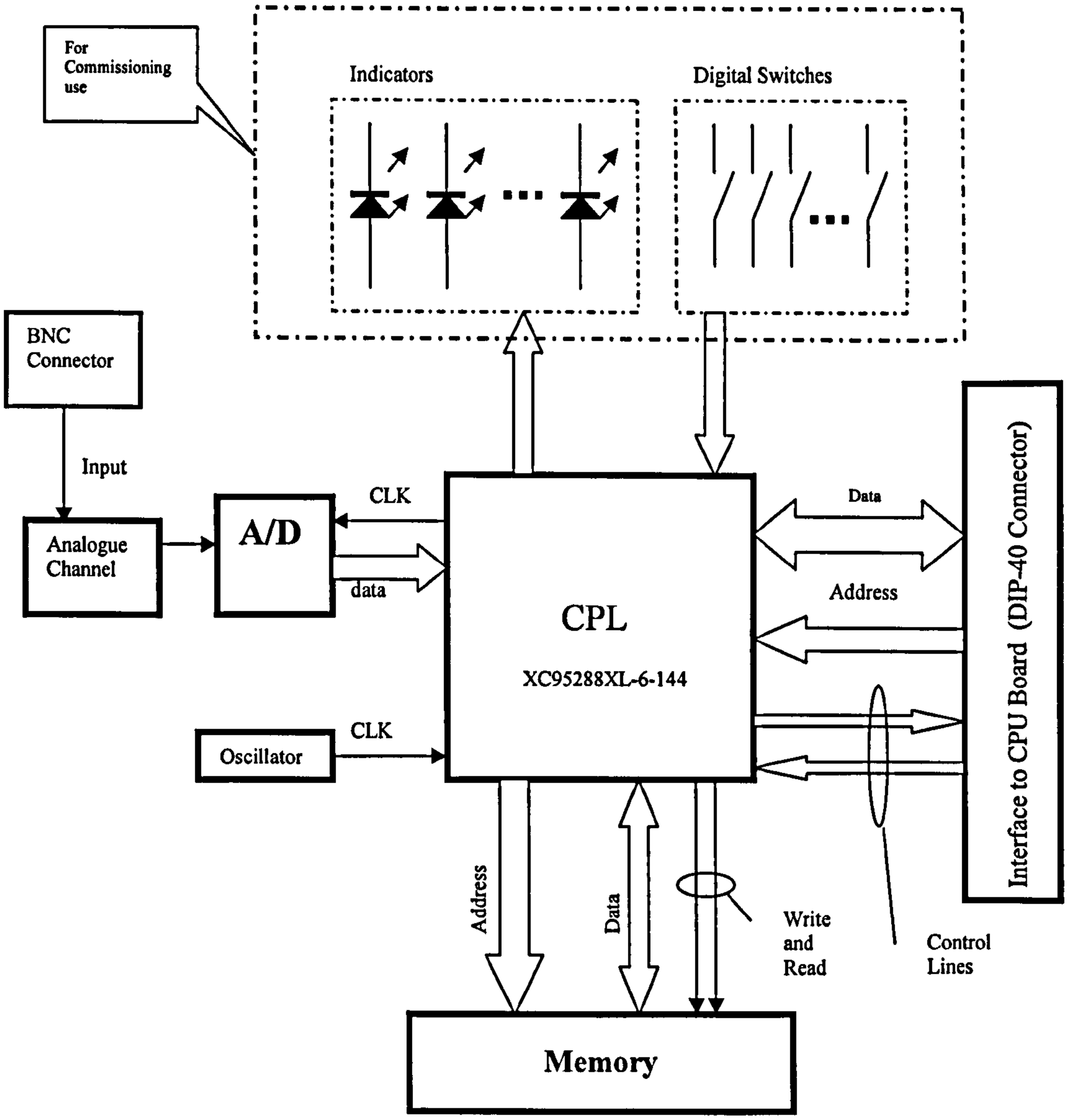


Fig. 4.1: Detailed diagram of the Acquisition Board

This circuit consists of several parts: Memory, Connector to CPU Board, Commissioning Part, ADC, Analogue Channel, CPLD, oscillator and other components.

Most of the logic circuitries are in the CPLD. The logic circuit in the CPLD is divided into several parts: "Interface to Memory (SRAM)", "Interface to CPU", "Trigger Function" and "Commissioning and Debugging Circuit". They will be separately presented in this section.

4.1.1 A/D converter and related circuitry

Fig.4.2 shows the configuration of the ADC circuit and its peripherals.

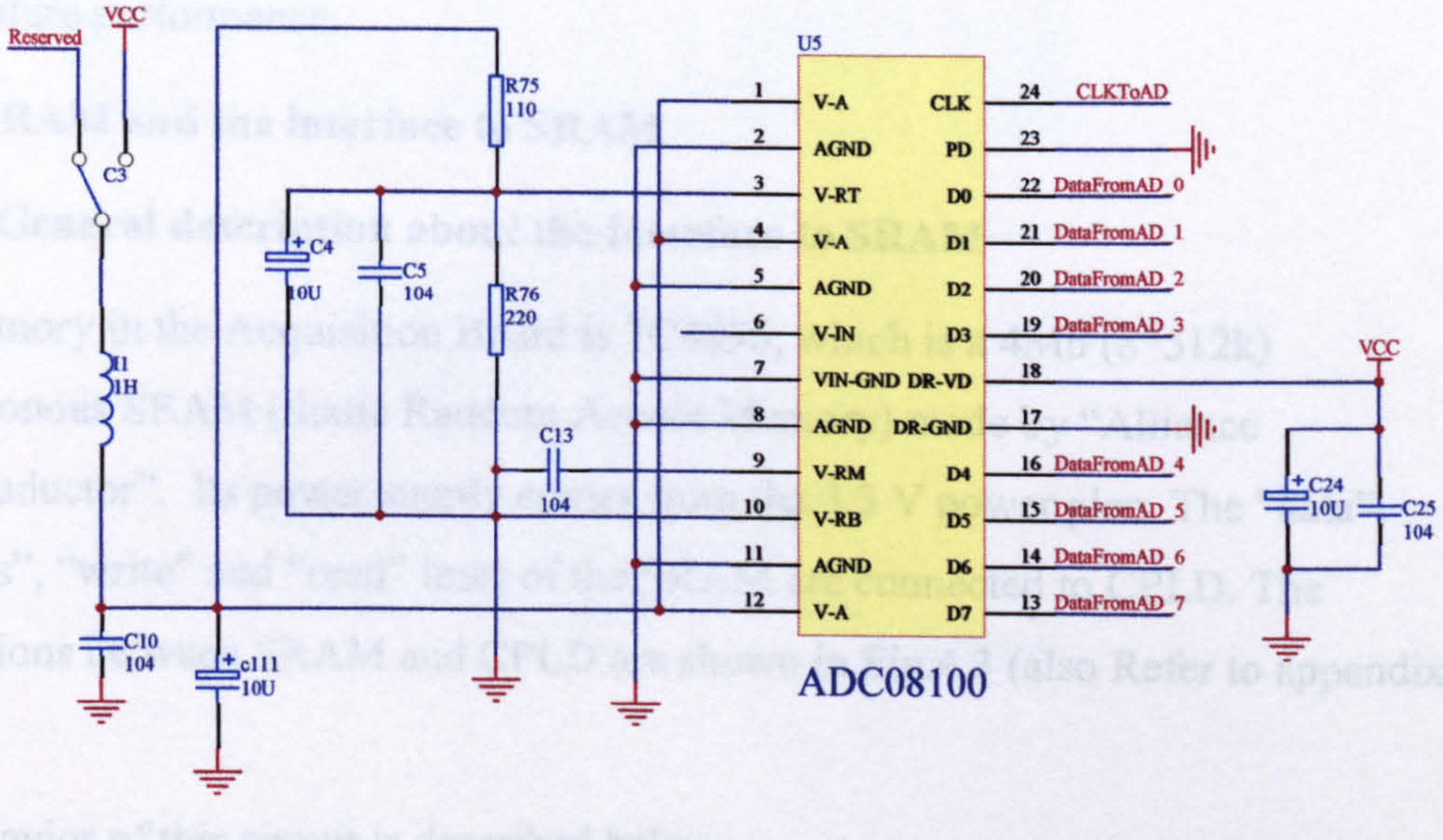


Fig. 4.2: A/D converter and peripherals

The A/D converter ADC08100 is designed to convert an analogue signal to 8-bit digital code. The "original clock" from the oscillator goes through the CPLD to drive the A/D converter. For every clock period, it completes a process of sampling, converting and data output. Through the output pins D0-D7, the 8-bit data are sent to the CPLD and then buffered into SRAM. V-RT input pin is the high side of the reference ladder. This design configures the A/D converter with 2 volt input range. This analogue range takes the digital code range from 0 to 255. There are 3 Analogue Power pins (V-A) in the converter. They input a power supply for the analogue part of this chip, whereas V-D is the power supply input pin for digital part of this chip. Both of these power supplies are drawn from 3.3V Vcc on this board and filtered. Furthermore, the two power supplies are separated by a choke. However, since all the digital components in this board are using this 3.3V power supply, these components may introduce interference to the power rail. In case the 3.3V power supply has worse quality for the analogue part, a separate power supply has been reserved for the analogue part of the ADC as shown in the figure ("Reserved" and

the Switch). The ADC configuration and its related circuits exactly follow the application example in the data sheet of ADC08100 [55].

The resistors in this circuit are chosen from metal film resistors for better temperature performance.

4.1.2. SRAM and the interface to SRAM

4.1.2.1 General description about the interface to SRAM

The memory in the Acquisition Board is 7C4096, which is a 4Mb (8*512k) asynchronous SRAM (Static Random Access Memory) made by "Alliance Semiconductor". Its power supply comes from the 3.3 V power plan. The "data", "address", "write" and "read" lines of the SRAM are connected to CPLD. The connections between SRAM and CPLD are shown in Fig.4.3 (also Refer to appendix A).

The behavior of this circuit is described below:

Once the circuit is powered-up, the ADC starts to convert the analogue measured signal into digital codes under the 80MHz conversion clock. The ADC's data is input to CPLD and from there, they are written to SRAM at a specified speed (1/2, 1/4, 1/8, … or 1/64 of original frequency). The SRAM is circularly used and always contains the latest 512k bytes data of the measured signal. Once the RAU is triggered, the CPLD stops writing data to SRAM and stops increasing the address for SRAM. When the operators on the PC side knows that the RAU has been triggered, they can download data from the SRAM. The operator sends the read command to the AT89c52, then, AT89c52 starts to read 8000H port. Every time the AT89c52 reads the 8000H port, the CPLD transmits a byte from the SRAM to AT89c52 and increases the address counter letting the address point to next unit of SRAM. By this method, repeating 512k times reading 8000H, AT89c52 can read out all the data stored in SRAM.

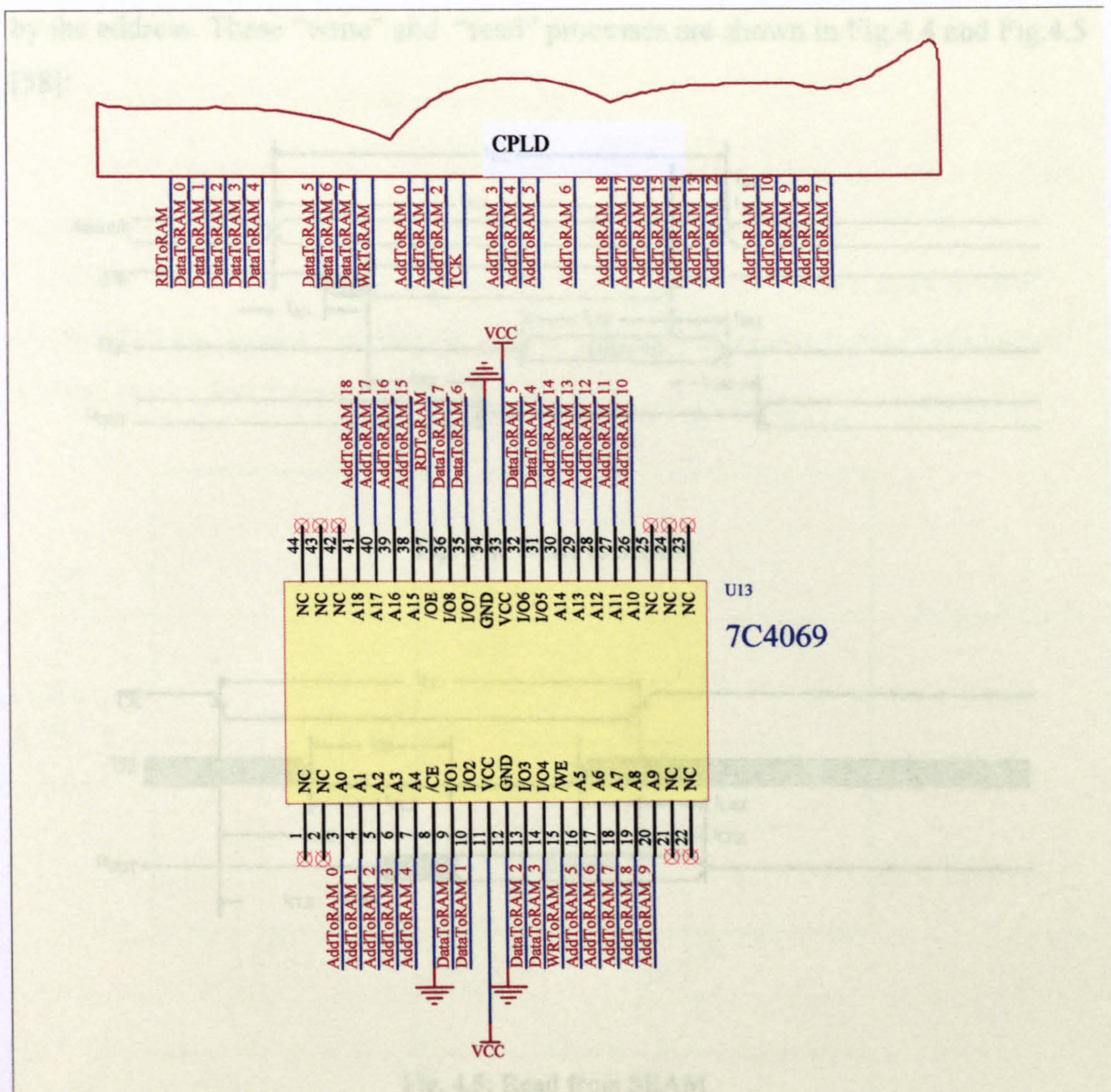


Fig. 4.3: Connections between SRAM and CPLD

Generally, to read from and write to this asynchronous SRAM, the host (CPLD in this design) should output RD (Read), WR (Write) and 19-bit address signals to SRAM. For read operation, the host outputs 19-bit "address" signal to the "address" pins of SRAM, the low "RD" signal to "OE" (Output Enable) pin of SRAM, then, the "data" port of SRAM will output the 8-bit data, which is stored in the memory unit specified by the address, and the host can then input the 8-bit data. For write operation, the host outputs low "WR" to "WE" pin of SRAM, outputs the address and data to SRAM, and the data port of SRAM inputs the data. At the end of the low-level period of WR signal, the data is stored in the memory unit, which is specified

by the address. These "write" and "read" processes are shown in Fig.4.4 and Fig.4.5 [58]:

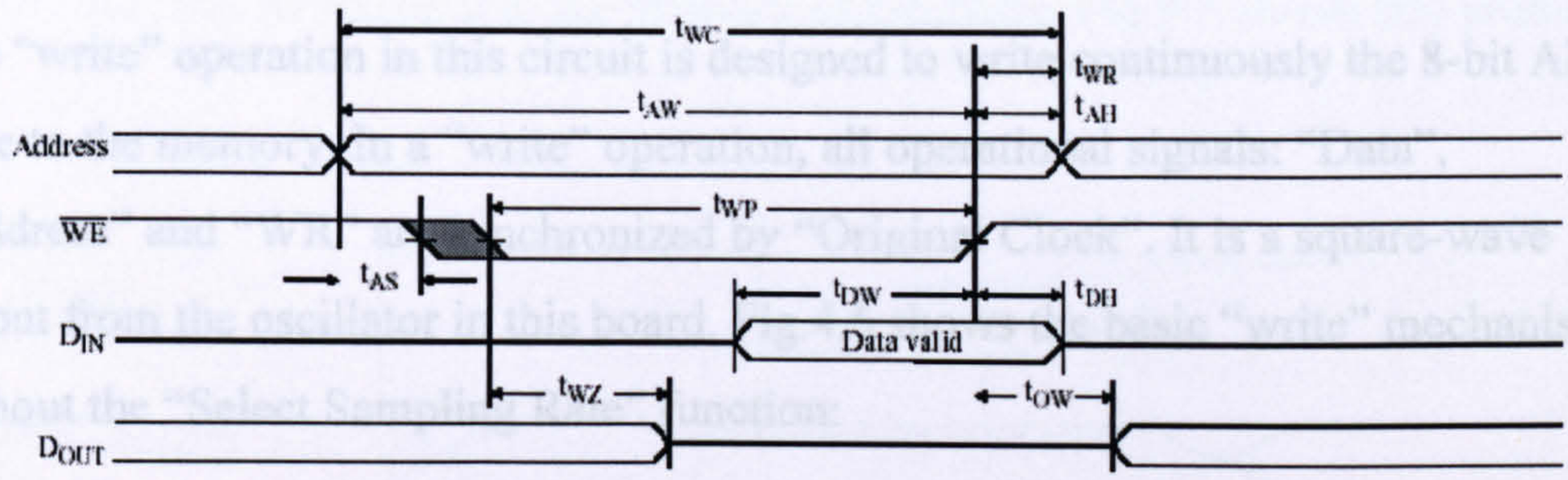


Fig. 4.4: Write to SRAM

Fig. 4.5: Read from SRAM

In adopting the above timing-sequence, the CPLD should be configured accordingly to build the "Interface to SRAM":

The 19 output lines of the CPLD are connected to19-bit "Address" input ports of the SRAM. The 19-bit address comes from a 19-bit synchronous counter built-in the CPLD. The CPLD also provides "WR" and "RD" pulses to the SRAM with two output lines. The CPLD uses 8 lines to connect the data port of SRAM. These 8 lines are configured as a bi-directional port. When a "write" operation takes place, the data port of CPLD is in "input" state and the data port of the SRAM in "output" state. When a "read" operation takes place, the data port of the CPLD is in "output" state and the data port of the SRAM in "input" state.

4.1.2.2 Basic "write" operation to SRAM

The "write" operation in this circuit is designed to write continuously the 8-bit ADC code to the memory. In a "write" operation, all operational signals: "Data", "Address" and "WR" are synchronized by "Original Clock". It is a square-wave output from the oscillator in this board. Fig.4.6 shows the basic "write" mechanism without the "Select Sampling Rate" function:

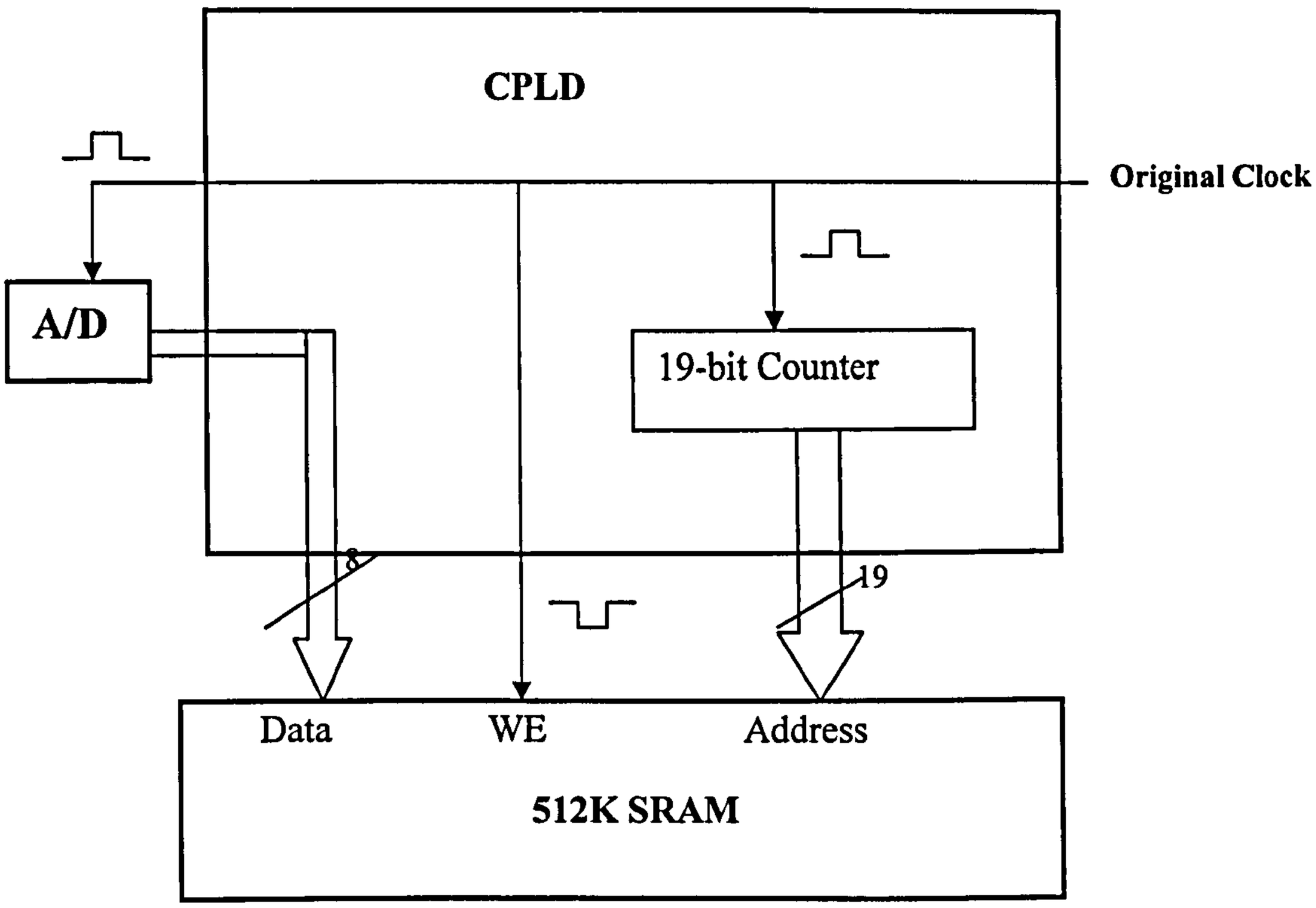


Fig. 4.6: Basic "Write" mechanism

Where the "Address" is the output of a19-bit increasing counter counting the "original clock"; "WE" is the "original clock" itself; "Data" signal comes from the ADC driven by the "original clock", and the paths through the CPLD.

After the rising edge of the "original clock", ADC starts a new conversion and a 19-bit counter increases. Before the positive period ends, the "Data" and the "Address" are ready. At the following falling edge, the "Data" is written to the memory unit

specified by "Address". Repeating this process, the next clock will start a new conversion and write a new 8-bit "Data" into the next memory address. Thus, the ADC's data can be stored into the memory sequentially. Fig.4.7 shows this process.

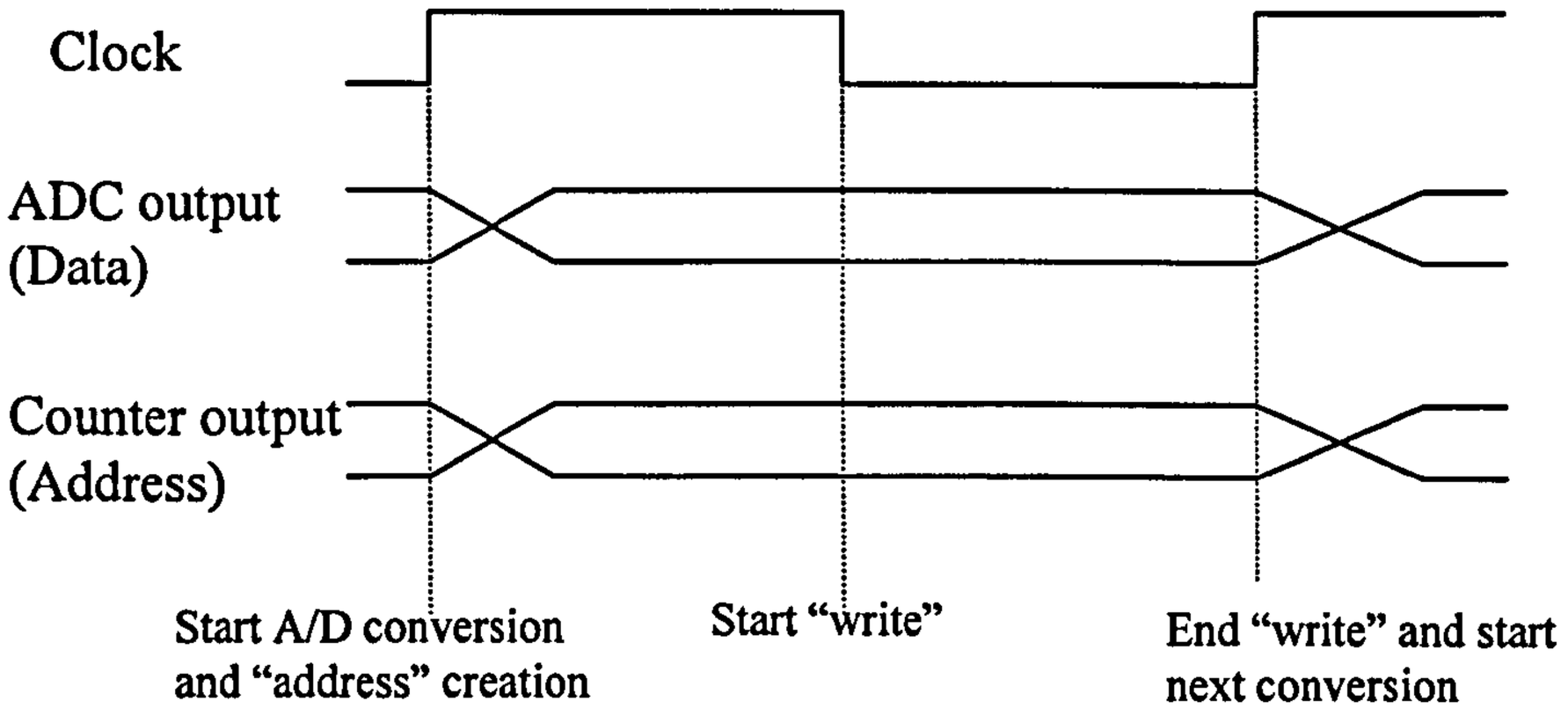


Fig. 4.7: Timing sequence of the "write" operation

Of course, there are some time-delays in this process. For a convenient description, this section only discusses the logic process and the time delay will be discussed later in section 4.1.3. Fig.4.7 just shows the logic timing sequence and the time delay does not included in this figure. The crosses in "data" and "address" signal just represent the transition of signal's state. The shape of the cross does not represent any time delay information.

4.1.2.3 Adjustable frequency for "write" operation

The above design is a basic structure. In the final design, the RAU should have an adjustable sampling rate from 1MSPS to 80MSPS. The simplest way for "Adjustable Sampling Rate" function is to use a changeable oscillator. However, the effective conversion rate of ADC08100 is only 20MHz to 100MHz, so it cannot be adjusted over a wide range. Therefore, adjusting the sampling rate of the RAU can only change the storage rate. That is, keeping A/D conversion in a fixed frequency (80MHz) and adjusting the frequency of "address" generator from 1.25MHz to 80MHz. Fig.4.8 shows this mechanism:

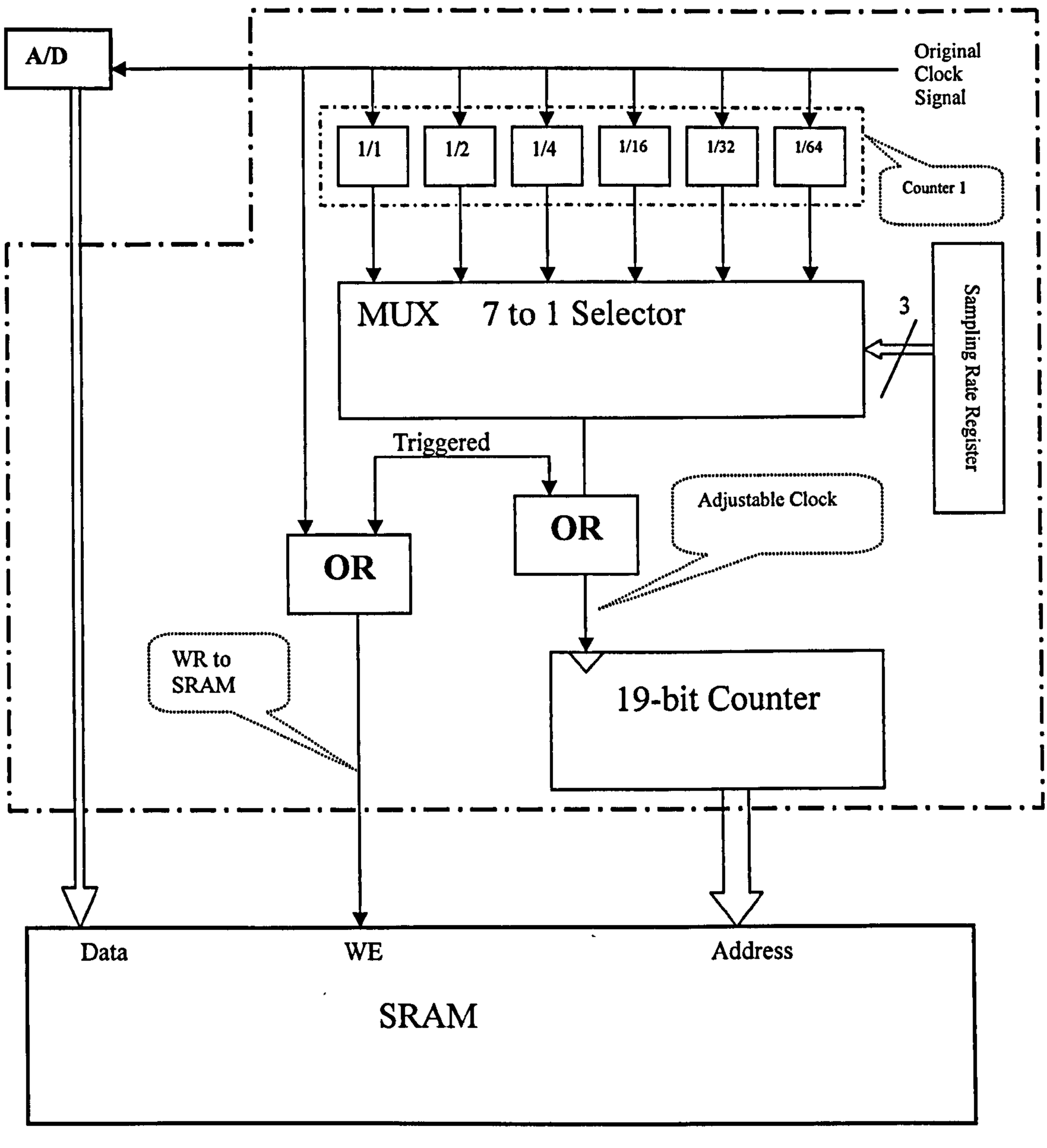


Fig. 4.8: "Write" mechanism

In Fig.4.22, the clock for19-bit counter comes from the "Adjustable Clock" instead of the "original clock". By "counter 1", the "original clock" is divided into 7 different clocks with 1/1, 1/2, 1/3 … 1/64 of the original frequency.These 7 different clocks input to the "multiplexor", which is a "7-to-1 selector" controlled by the selection factor stored in a 3-bit register –the "Sampling Rate Register". This register is controlled by a remote PC. (The process of setting-up this register will be discussed in a later section). The truth table of the "7-to-1 Selector" is listed below:

Table 4.1: Truth table of the multiplexor

Frequency	80MHz	40MHz	20MHz	10MHz	5MHz	2.5MHz	1.25MHz
Selection Code	000	001	010	011	100	101	110

As an example, when the "010" is written to the "sampling rate register", 20MHz is selected as the counting pulse for 19-bit counter. The conversion speed of the ADC is still 80MSPS, and a "write" operation also takes place at the same speed. But, the address is change to 20M times per second, i.e., for every 4 times conversions, only one byte is written to the memory. Apart from the stored byte, the other 3 conversion results are discarded.

Furthermore, the sampling action should be stopped when the RAU is triggered. Therefore, the address counting pulse and "WR" pulse are blocked by a "triggered" signal as shown in Fig. 4.8.

The description of this design (Frequency Divider and Multiplexor) in Verilog_HDL language is listed below:

In the Verilog-HDL design, the "original clock" is named as "CLK", the frequency divider is named as counter1. The 7 inputs of the MUX (multiplexor) are Counter[0], Counter[1]…Counter[5] and CLK. The selection code is defined as SpeedSelection. And the output of the MUX is defined as AdjustableCLK. For further information, refer to appendix E.

```
always @ (posedge Reset or posedge CLK)
begin
        if (Reset)
                Counter1=6'b0;
        else
                Counter1=Counter1+1'b1;
end

assign
AdjustableCLK=(Counter1[5]&SpeedSelection[2]&SpeedSelection[1]&SpeedSelection[0])|
(Counter1[4]&SpeedSelection[2]&SpeedSelection[1]&~SpeedSelection[0])|
(Counter1[3]&SpeedSelection[2]&~SpeedSelection[1]&SpeedSelection[0])|
(Counter1[2]&SpeedSelection[2]&~SpeedSelection[1]&~SpeedSelection[0])|
(Counter1[1]&~SpeedSelection[2]&SpeedSelection[1]&SpeedSelection[0])|
(Counter1[0]&~SpeedSelection[2]&SpeedSelection[1]&~SpeedSelection[0])|
(CLK&~SpeedSelection[2]&~SpeedSelection[1]&SpeedSelection[0]);
```

4.1.2.4 "Read" operation to SRAM

The "write SRAM" mechanism has been discussed. Next, the "read" mechanism will be presented.

As has been described in section 3.7, when the trigger condition is met, the "write" action will be stopped and the latest 512K bytes data are kept in the SRAM. Thus, the micro-controller can read out the 512K data and send them to a remote PC. To allow the micro-controller to read the data from the SRAM, the CPLD interface to the SRAM is built with the "read" mechanism.

The read operation for the micro-controller AT89c52 is to implement a so-called "external device read" instruction "MOVX A, @DPTR", which means to move the data in the external address, pointed by the DPTR, into the accumulator of the micro-controller. Fig.4.93 shows the process of the "Read" instruction [57].

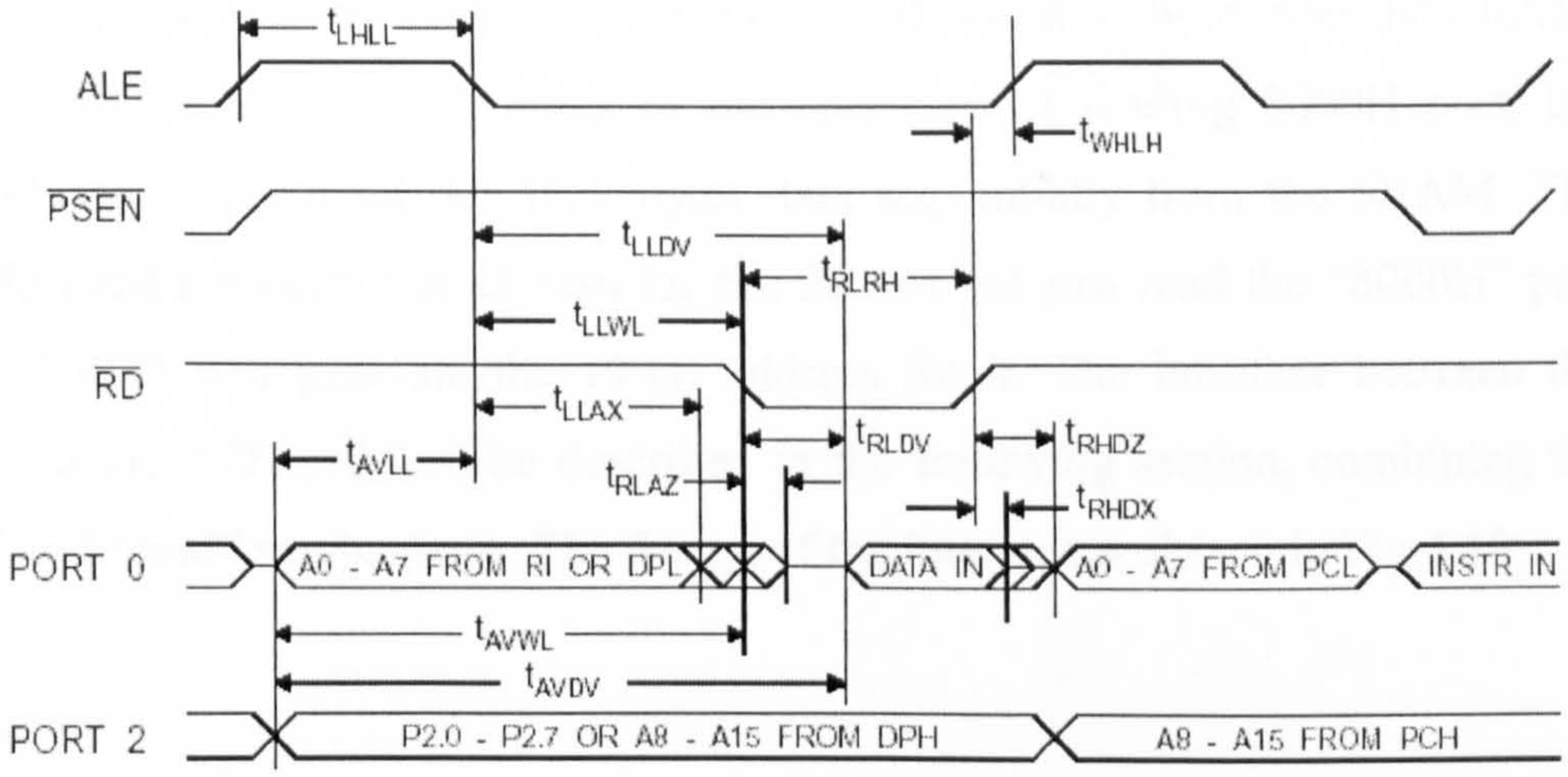


Fig. 4.9: External memory read cycle of AT89c52

Two cycles are required for this instruction. In the first cycle, a 16-bit address is generated (port0 and port 2) and in the second cycle, the AT89c52 output "read" pulse from "RD" line and inputs the data from the data lines (port0 is a multi-purpose port for both low 8-bit address and data) [70]. According to this read mechanism, the CPLD provides a readable port to the AT89c52 and configures it with address 8000H (in hex, i.e. 10000000 in binary). This port is like an external memory unit for AT89c52.

In the RAU design, there are two address encoding systems. One is used for the CPLD to point the unit in the SRAM in the Acquisition Board. This address has 19-bit width and is generated by the CPLD. Another is used for the AT89c52 to read external memory, which has a 16-bit width and generated by the AT89c52. In the thesis, when the "address" is being discussed, if the address is operated by the AT89c52, it means the 16-bit address; if the address is operated by CPLD, it means the 19-bit address. Also, the "Data" bus for the AT89c52 is different from the "Data" bus for the SRAM.

When the AT89c52 reads the 8000H port, the CPLD opens the data route from the AT89c52 to the SRAM and let the AT89c51 read out 1 byte (8 bits) from the SRAM. At the end of the read action, the CPLD increases the "19-bit address counter" by "1".

Thus, in the next reading action, the AT89c52 will read next byte from the SRAM. By this way, repeating 512k times of the operation of reading 8000H port, the AT89c52 can read out all the 512k bytes data sequentially from the SRAM. The AT89c52 need not point the address for the SRAM but just read the "8000H" port and the CPLD will generate the 19-bit address for it. The interface between the CPLD and the AT89c52 will be described in the following section, combining the "write" and "read" mechanisms. The design of the interface is shown in Fig.4.10:

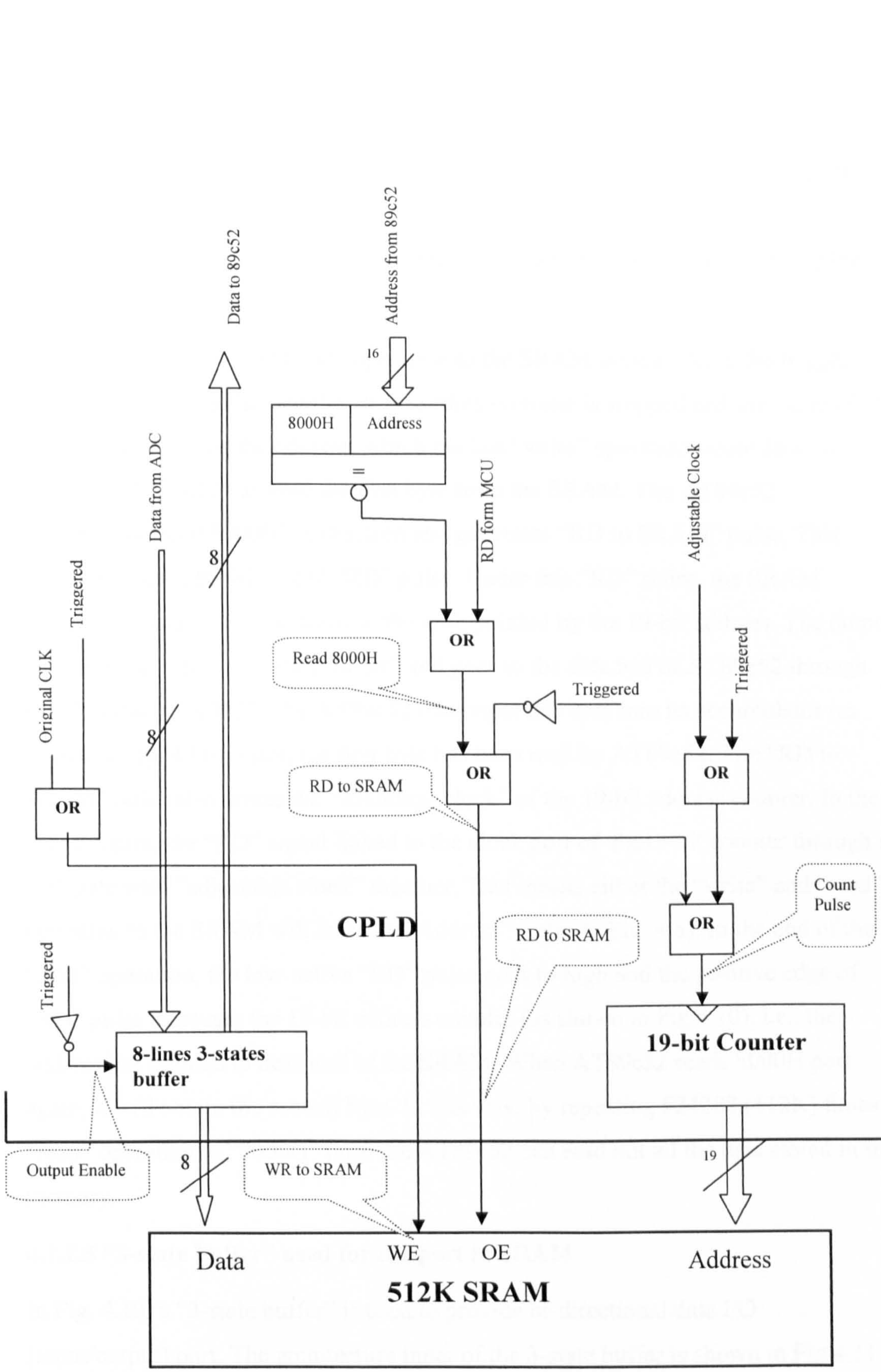


Fig. 4.10: "Read" mechanism for SRAM

When the AT89c52 reads 8000H, it generates the signal of "Read 8000H", which is a

low-active pulse (will be explained in section "The interface to CPU"). This pulse "OR" the inverted "triggered" signal and then outputs " RD to the SRAM" signal. "RD to SRAM" is connected to the "OE" line of the SRAM. Here, the "OR" operation is designed to prevent an unintended "read" SRAM operation during the acquiring period.

Thus, the process of the "Read" operation to the SRAM is clear. After the trigger event, the "write" pulse and the 19-bit address counter is stopped and the value of the 19-bit counter keeps the address, which the last "write" operation wrote data to. Then, the AT89c52 can read the first byte from the SRAM. The AT89c52 implements "read 8000H" instruction and generates "RD to SRAM" pulse. This pulse gives the SRAM a valid "RD" pulse. Under this "RD" pulse, the SRAM outputs the data, which is stored in the unit, pointed by the 19-bit address. The output data enters an "8-line, 3-state buffer" and goes to the data bus of AT89c52 through the "Interface to CPU". The AT89c52 then input this data into its accumulator (as shown in Fig. 4.10). Thus, the first byte has been read by AT89c52. The "RD to SRAM" pulse also drives the "counting- clock" of the 19-bit address counter. In the above figure, the "RD" signal linked to the clock port of the19-bit counter through a "or" gate with "adjustable clock" together. That means either the "write" and "read" operation to the SRAM will increase "Address" (refer to Fig. 4.8). In the end of the "read" operation, the low-active "RD" pulse goes to high and the positive edge of "RD" pulse increases the 19-bit address counter (as shown in Fig.4.10), i.e., the address has pointed to next unit of the SRAM. When AT89c52 reads 8000H port again, it will obtain the second byte. In this way, by repeating 524288 (512K) times "read" operation to "8000H" port, the AT89c52 can read out all the data stored in the memory.

4.1.2.5 "3-state buffer" used for the port to SRAM

In Fig. 4.10, a "3-state buffer" is used to provide bi-directional data I/O (input/output) port. The architecture inner of the 3-state buffer is shown in Fig.4.11.

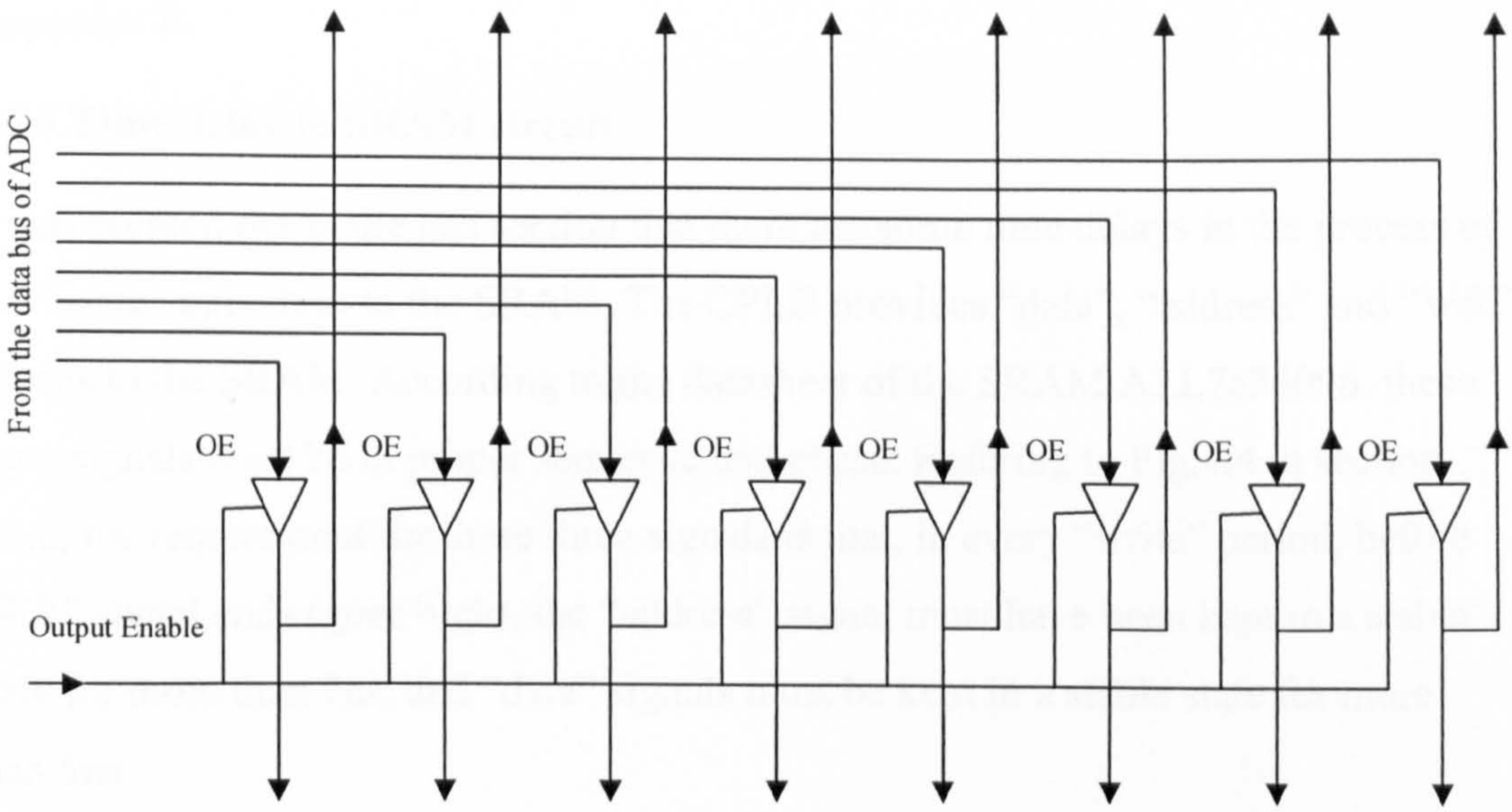


Fig. 4.11: Architecture of the "3-state bus buffer"

The "3-state bus buffer" consists of 8 3-state gates. Every 3-state gate has 4 lines: input line, output line, feedback line and "OE" control line. In Fig.4.11, 8 input lines link the 8-bit data bus of the ADC respectively, the output lines are linked to the 8-bit "Data" bus of the SRAM, feedback lines linked to the 8-bit "Data" bus in the "Interface to the AT89c52" (refer to section 4.1.4). All the OE (output enable) lines are linked together to the inverted "Triggered" signal (shown in Fig. 4.10). When the RAU is not triggered, the OE is high, the 3-state buffer transmits the signal from the ADC to the SRAM. When the RAU is triggered, OE is low and the output of the 3-state gate presents high impedance, thus, the ADC and SRAM are isolated and the signals are transmitted from the SRAM to the "interface to CPU" through the feedback lines when the AT89c52 reads "8000H". For details of the structure of 3-state gate, refer to [71]

CPLD XC95288XL provides a configurable 3-state output port for every I/O pin. It can be used to build the 3-state bus buffer [72].

Up to now, the memory and its related circuit have been presented. For the whole Verilog-HDL description of the design of the "Interface to SRAM", refer to Appendix E.

4.1.3 Time delay in SRAM circuit

It was pointed out in the last section that there are some time delays in the process of the "write" operation to the SRAM. The CPLD provides "data", "address" and "WR" signals to the SRAM. According to the datasheet of the SRAM ALL7c34096, these three signals must be in proper sequence and phase. Refering to Fig.4.4 in section 4.1.2, the requirement for these three signals is that, in every "write" period, before "WR" signal ends (goes high), the "address" signal must have been kept in a stable state for more than 7ns, and "data" signals must be kept in a stable state for more than 5ns.

In logic design, all the three signals "data", "WR" and " Address" are synchronised by the same clock source (original clock). Without delays, these three signals are designed to feed to SRAM in the correct time sequence. However, in actual circuits, since these three signals pass through different routes before they arrive to the SRAM, the different routes produce different delays and these three signals cannot arrive at the SRAM's input pins simultaneously. Because the "write" operation is at a fairly high speed (80MHz) and the "write" operation period is fairly short (12.5 ns). These different delays are significant to make the time sequences and phases relationship deviate from what the logical design had expected. Therefore, the delays in this circuit have to be examined.

For convenient calculation, all the time delays for "data", "address" and "WR" signals refer to the same point-the rising edge of the "original clock". For example, the delay of "data" signal is defined as the time between the moment when the original clock starts a new period (rising edge) and the moment when the "data" signal arrives at the SRAM's input pins. The next paragraphs will discuss the delays of "data", "address" and "WR" signal.

Firstly, the time-delay for "data" signal is examined. It consists of 3 end-to-end routes as shown in Fig4.12.

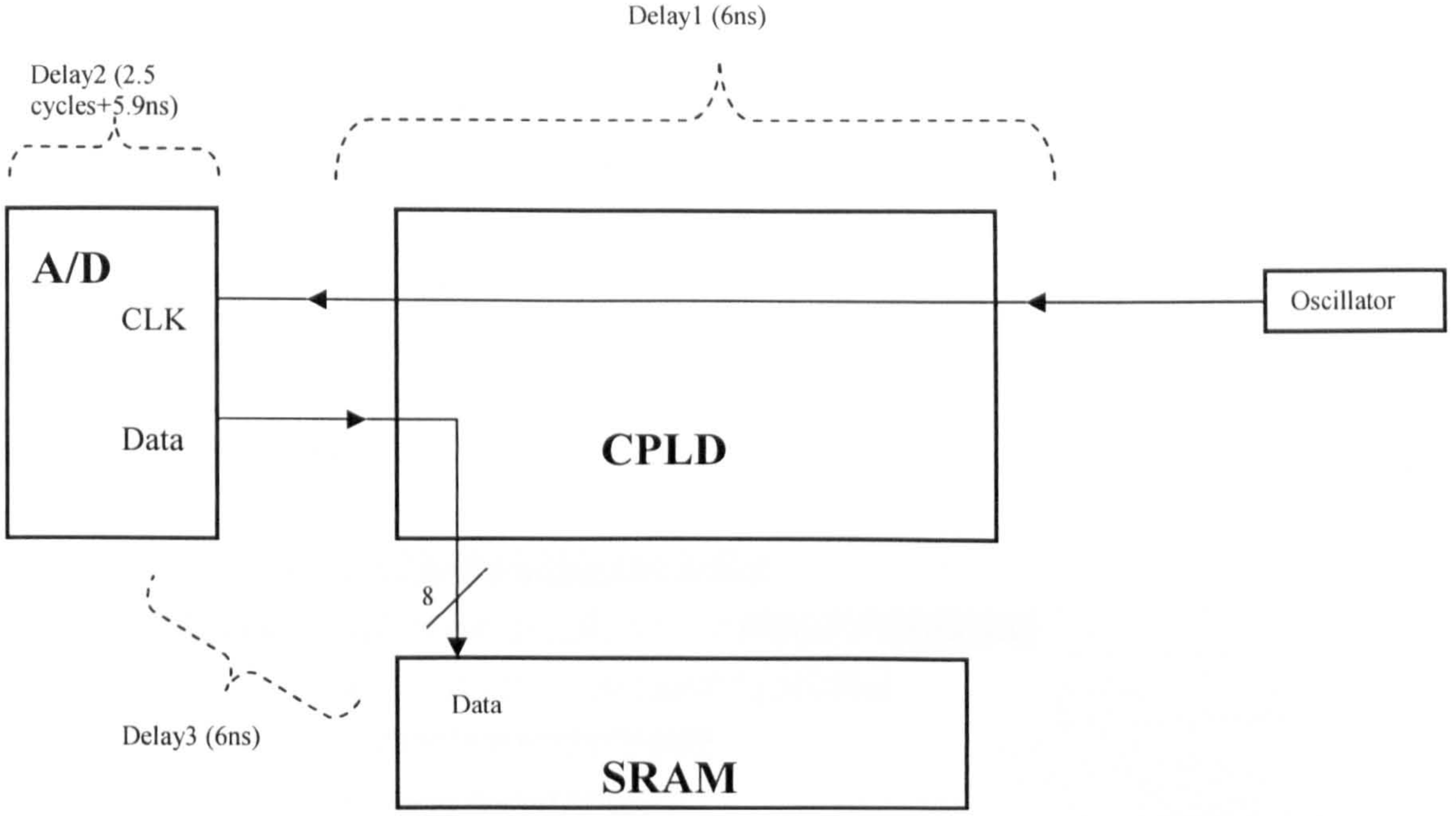


Fig. 4.12: Delay components of "data" signal

The original clock paths through the CPLD and enters the ADC. This clock starts a new conversion in the ADC, which then outputs the 8-bit "data" signal to the CPLD. Through the CPLD, the "data" signal enters the SRAM. There are 3 delays during this process:

1) Delay 1: The time between the original clock inputs to the CPLD and the same signal outputs from the CPLD. It is a so-called "Propagation delay". According to the datasheet of XC95288xl-6, this delay is 6 ns [60]. "Xilinx PDL Development Software Kit" also provides the delay calculation tool-"Timing Analyser". Applying the "Timing Analyser", measuring the delay between the input pin of the "original clock" and the pin, at which the clock is output to ADC, the result can be obtained as below. For the operation and explanation of this "Timing Analyser", refer to the user manual of the Xilinx software kit "ISE" [73]

Detailed Path Analysis Report

Design: acq7

Device: XC95288XL-6-TQ144

Speed File: Version 3.0

Program: Timing Report Generator: version F.26

Date: Fri Nov 12 17:24:39 2004

Timing Analysis Options:

From: CLK

To: CLKToAD

Output will be sorted by increasing path delays.

Logical Path	*Delay Type*	*Delay*	*Cumulative*
	**********		
	* *Pad to Pad (tPD)* *		
	**********		
From: CLK	-	*: 0.0ns*	*(0.0ns)*
Thru: CLK_IBUF	*tIN*	*: 2.2ns*	*(2.2ns)*
Thru: CLK_IBUF$BUF0	*tLOGI + tPDI*	*: 1.4ns*	*(3.6ns)*
To: CLKToAD	*tOUT*	*: 2.4ns*	*(6.0ns)*

Where tIN is the delay in the input pin buffer of the CPLD. tOUT is the delay caused by output pin buffer in the CPLD. Other delays listed in the report are caused by internal routes in the CPLD. The report shows the total delay of this route is 6ns. For detail explanations about these terms and the method for calculation, refer to [74, 60, 35].

2) Delay 2: The time delay caused by the ADC. This delay time includes two parts: "Output Delay" and "Pipeline Delay". According to the datasheet of the ADC 08100 [55]. "Output Delay" is the time after the rising edge of the clock and before the updated data are present at the output pins. It is typically 5.9 ns. "Pipeline Delay" is defined as the time between the initiation of the conversion and the data presented in the output driver stage of the ADC. It is 2.5 clock cycles. In the ADC, data lags are the Pipeline Delay plus Output Delay as shown in Fig.4.13.

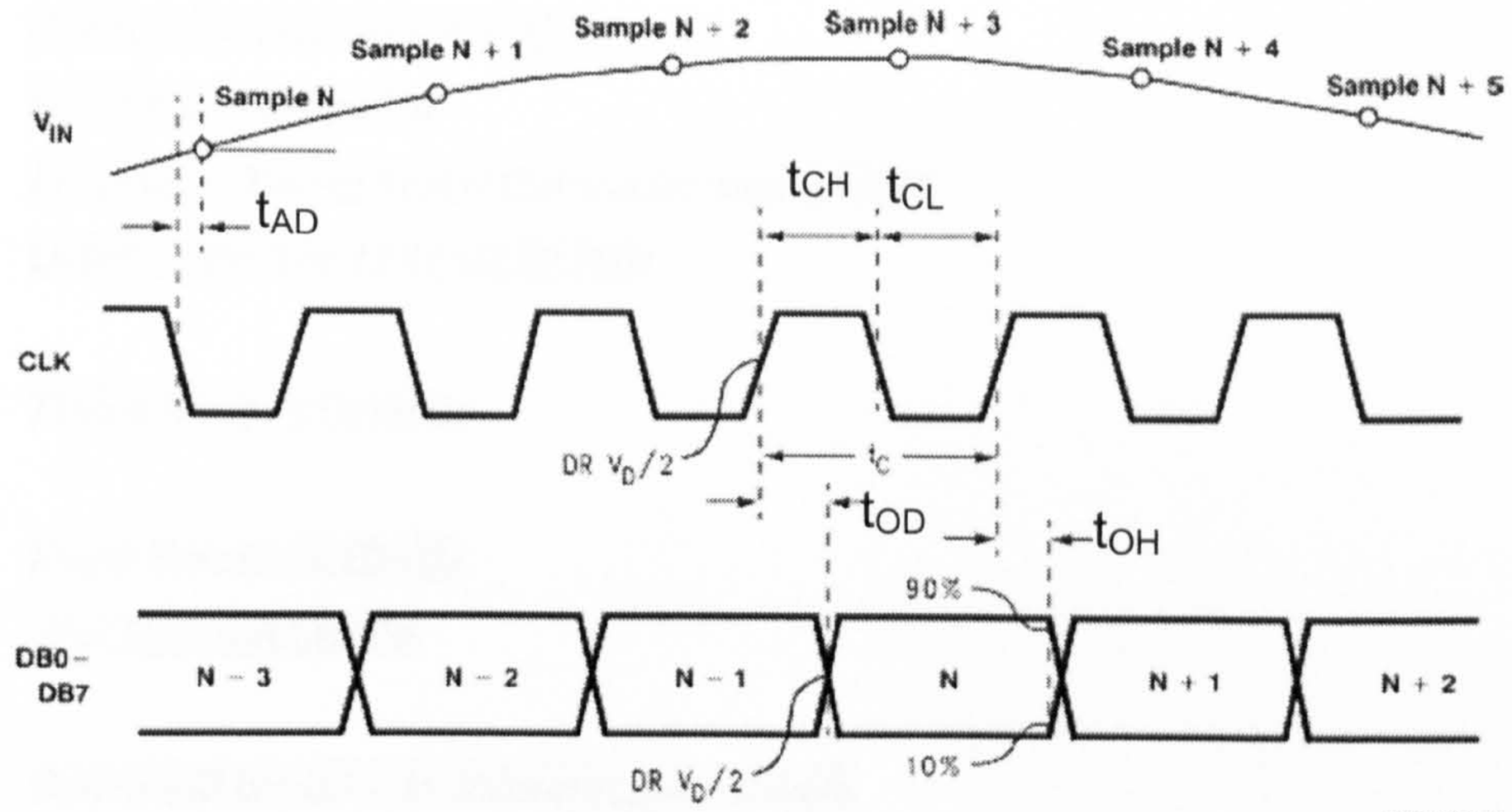


Fig. 4.13: Data delay of the ADC08100

Where Vin is the input analogue signal. In every falling edge of the clock, the ADC samples a signal point and starts to convert it. After 2.5 cycles, the converted data are ready in the output stage and at the next rising edge of the clock the data will be output. The output delay is marked in Fig.4.13 as "t_{OD}". The rising edge also ends the output of the last data. The delay time after rising edge before the last data is invalid is "hold time". It is 4.8ns for ADC08100 and marked as "t_{OH}" in the figure. The pipeline delay need not to be considered here, since it does not affect the "write" operation to the SRAM, either by changing the sequence or by changing the phase. Only "Output Delay" and "Output Hold" are considered.

3) Delay 3: The CPLD "propagation delay" for "data" signal, as delay 1, it is 6ns. The software tool "Timing Analyser" gave the following report:

Detailed Path Analysis Report

Design: acq7

Device: XC95288XL-6-TQ144

Speed File: Version 3.0

Program: Timing Report Generator: version F.26

Date: Fri Nov 12 11:03:39 2004

Timing Analysis Options:

From: DataFromAD<0>

To: DataToRAM<0>

Output will be sorted by increasing path delays.

Logical Path	*Delay Type*	*Delay*	*Cumulative*
---	---	---	---

****

* *Pad to Pad (tPD)* *

****

From: DataFromAD<0> -		*0.0ns*	*(0.0ns)*
Thru: DataFromAD_0_IBUF	*tIN*	*2.2ns*	*(2.2ns)*
Thru: DataFromAD_0_IBUF$BUF1	*tLOGI + tPDI*	*1.4ns*	*(3.6ns)*
To: DataToRAM<0>	*tOUT*	*2.4ns*	*(6.0ns)*

The total delay time for "data" signal is the sum of above three sections: 6+5.9+6= 17.9ns, and the valid duration of "data" signal in every period is 12.5-5.9+4.8=11.4ns (as shown in Fig. 4-13, $t_C - t_{OD} + t_{OH}$).

Secondly, the time-delay for the "WR" signal is examined. The route of this signal from "original clock" to "WR" is shown in Fig.4.14:

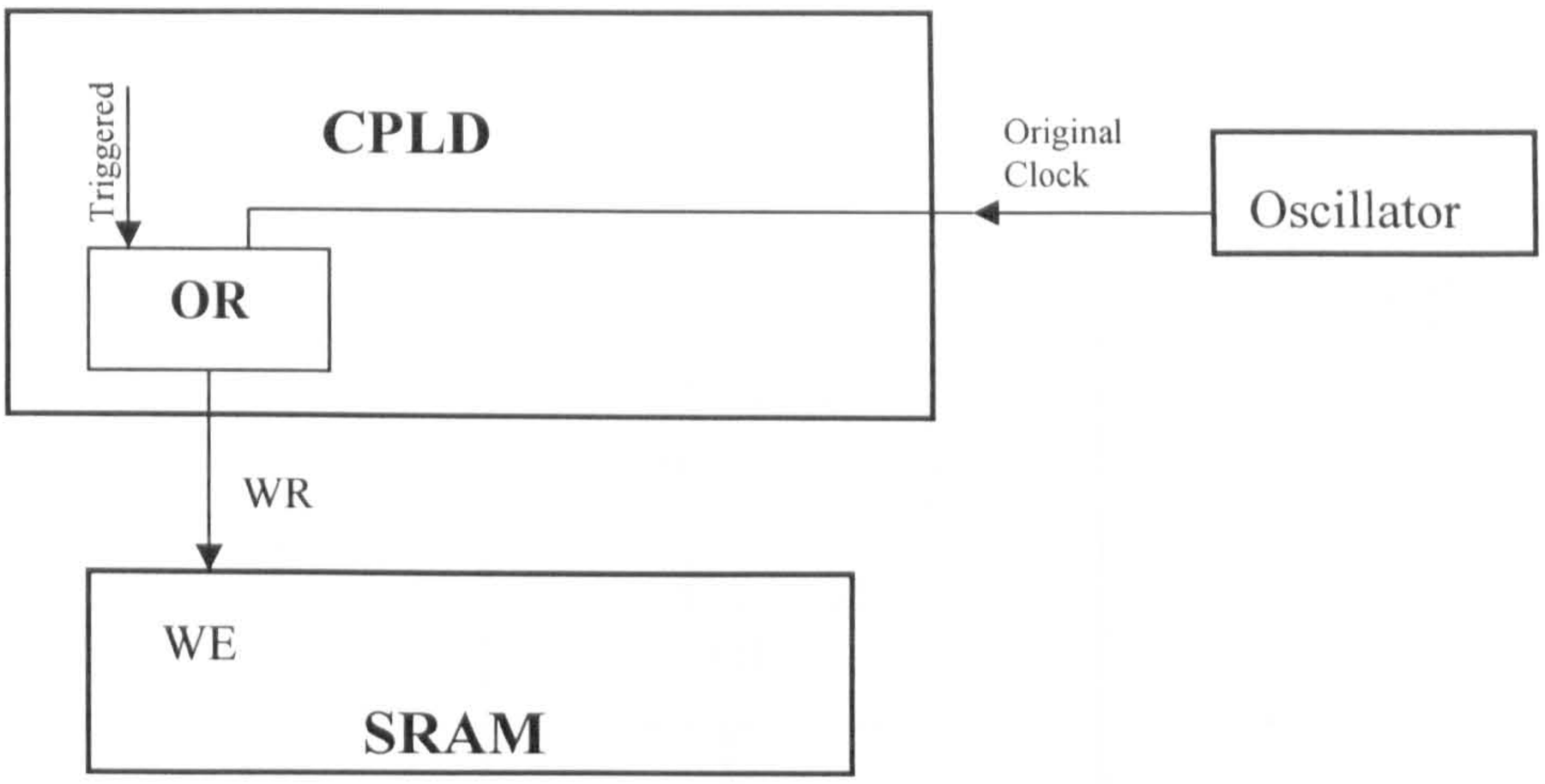


Fig. 4.14: Delay of the "WR" signal

As the "Timing Analyser" reported, the delay is 6ns as a standard "product term propagation delay"

It may be observed that compared with "delay 1" and "delay 3" in "data" signal, there is an extra "OR" gate in the route of the "WR" signal. However, the time delays for both of them are the same because it is the mechanism used by CPLD to implement combinational logic. When a signal is transmitted from one pin to another pin though the CPLD, it always passes a "product term" inside of the CPLD. The "product term" naturally contains an "OR" gate. Whether the transmitted signal take an "OR" operation or not, the "OR" gate cannot be omitted. If the signal takes the "OR" operation, it passes through the "OR" gate with another certain signal; If the signal does not need to be "OR", it passes through the "OR" gate with logic "0" (link to ground).

Finally, the delay for the "address" signal is examined. The route of this signal is shown in Fig.4.15:

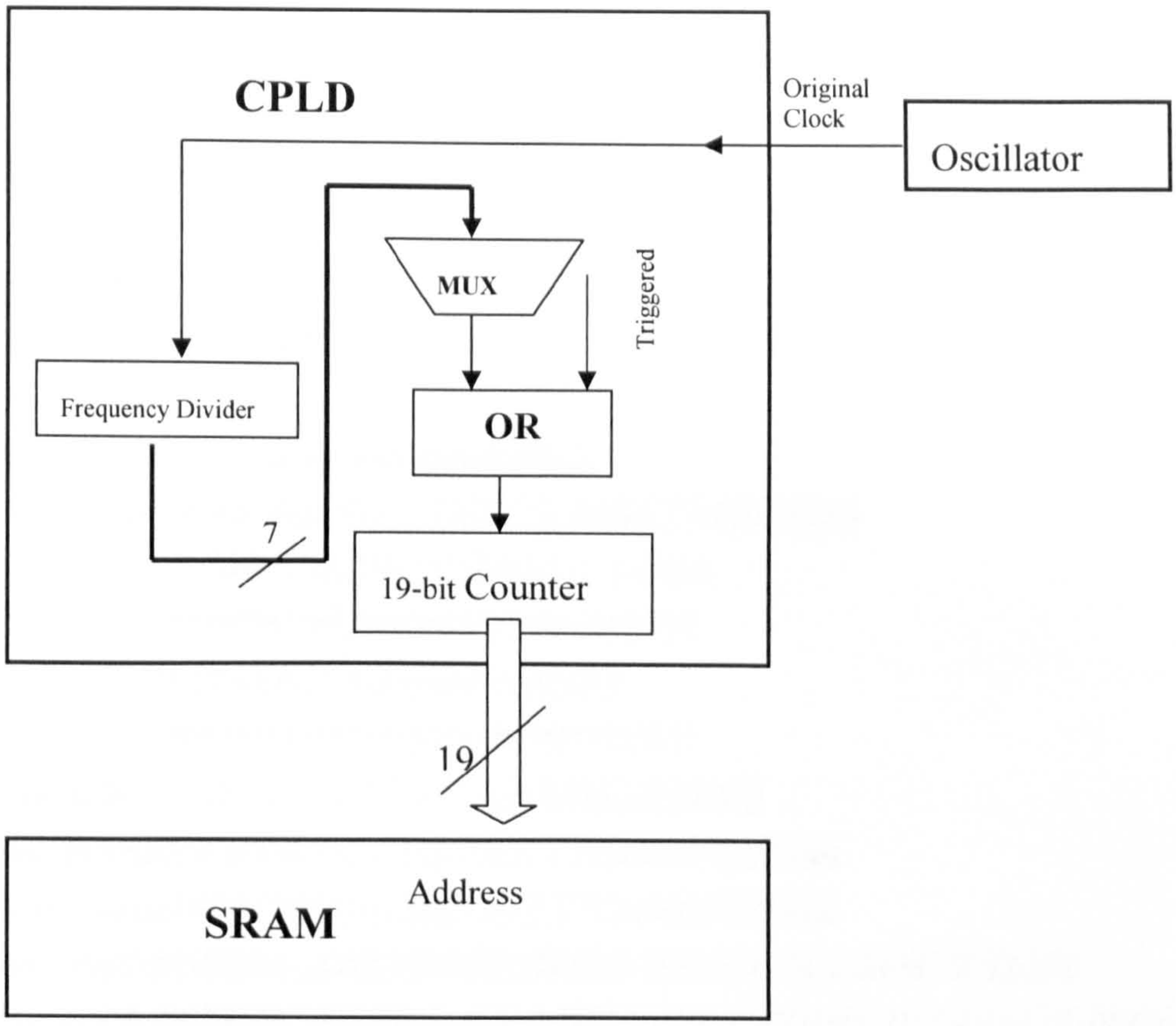


Fig. 4.15: Delay of "address" signal

As presented in the last section, the original clock is divided by a frequency divider to generate seven square-wave signals with seven different frequencies. The seven signals enter a 7-1 multiplexor and one of them is selected as the clock pulse for the 19-bit counter. Then, the clock pulse drives the 19-bit counter to generate a 19-bit "address" and output the "address" to the SRAM. The "Timing Analyser" reported the delay of "address" signal during above routes is 15.6ns, as shown below.

Detailed Path Analysis Report

Design: acq7

Device: XC95288XL-6-TQ144

Speed File: Version 3.0

Program: Timing Report Generator: version F.26

Date: Fri Nov 12 10:59:24 2004

Timing Analysis Options:

From: CLK
To: AddressToRAM<18>

Output will be sorted by increasing path delays.

Logical Path	*Delay Type*	*Delay*	*Cumulative*
	**********		
	* Clock Pad to Output Pad (tCO) *		
	**********		
From: CLK	-	*: 0.0ns*	*(0.0ns)*
Thru: FCLKIO_0 tGCK		*: 1.2ns*	*(1.2ns)*
Thru: Counter1<1> tCOI		*: 0.2ns*	*(1.4ns)*
Thru: $OpTx$INV$100__$INT.UIM tF + tLOGI + tPTA + tPDI		*: 3.8ns*	*(5.2ns)*
Thru: $OpTx$INV$100__$INT.UIM tF + tPTCK + tCOI + tCOI + tPDI		*: 4.2ns*	*(9.4ns)*
Thru: acq5RAMInterface_Address<18>$Q tF + tPTCK + tCOI		*: 3.8ns*	*(13.2ns)*
To: AddressToRAM<18> tOUT		*: 2.4ns*	*(15.6ns)*

The result is based on the longest route through the frequency divider. If the sampling selection is 80MHz speed, i.e. 1/1 of the "original clock", the route will not include a "frequency divider". It makes the delay 0.8ns less. Therefore, the time delay for the "address" signal is from 14.8 ns to 15.6 ns.

Thus, the delay time for "data", "WR", and "address" are respectively 17.9ns, 6ns and 14.8-15.6ns.

Furthermore, the "data" signal pass through more traces on board than other two signals, that is the traces between CPLD and A/D. The distance of the track is 50mm (return journey). According to the experiential formula, for the FR4 multi-layer PCB, the delay time in the trace is 7ps/mm [75, 67]. Adding this signal delay, the delay time for "data" becomes about 18.3ns. These delay times are all relative to the point

of rising edge of original clock. The phase relationship of these three signals is illustrated in the Fig.4.16

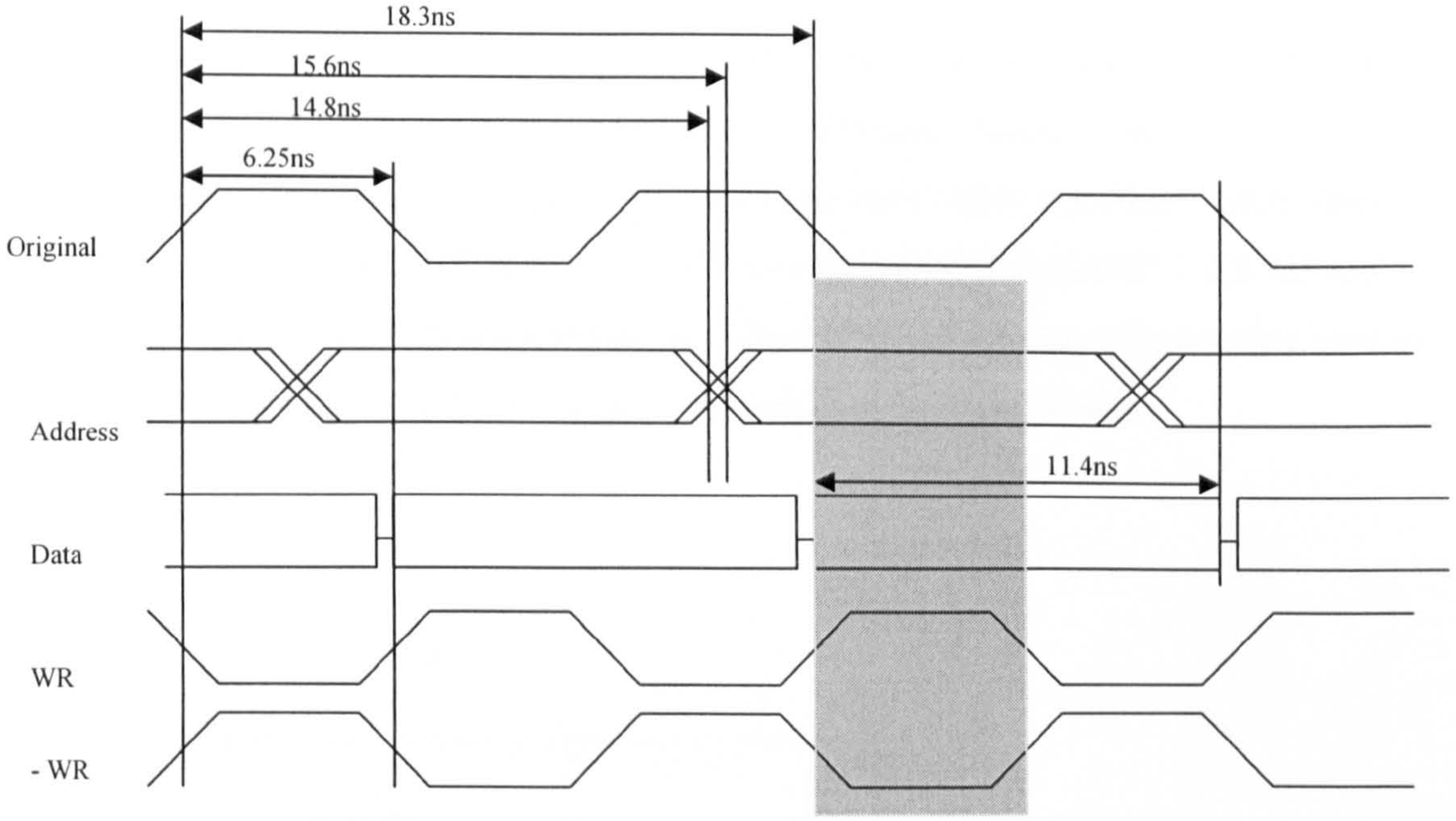


Fig. 4.16: Timing diagram of the "write operation" with delay

The clock period is 12.5ns (80MHz square wave) and according to the requirement of the SRAM (ALL7c34096), to write data correctly to the memory unit in the "write" period ("WR" signal is low), the "address" signal and "data signal" should be kept in a stable state for more than 5ns before "WR" goes high. It can be seen that the "WR" pulse cannot take a proper stable "address" and "data" signal, but the inverted "WR" can (shadowed area). In the whole "write" period, "address" and "data" stay in a stable state with big margins. Since the logic design did not consider the delay time, the final practical design of this circuit should be modified. It uses an inverted "original clock" to generate the "WR". The modified "WR" signal is reversed to the previous "WR" and makes the same delay as the previous "WR" signal.

Of course, the above analysis on signal delay is theoretical and using typical data. The real delay is obtained from real circuit tests. But, if the theoretical analysis were not true, it would be too late to find the problem when the PCB had been made. Therefore, in the design stage, some delay time adjustment mechanisms are reserved. This adjustment can be done by adding extra gates in the route of these signals. These gates are usually some inverters or delay lines outside of the CPLD. Different delay is typically 5-60ns per pair depending on the logic family. Thus, in the pin configuration of the CPLD, some I/Os have been reserved to introduce some inner medium signals outside of the CPLD. These pins are "WRToRAM" 1,2,3,4,5 and "TimeControl" 1,2 (refer to appendix A). Fig.4.17 gives an example showing how to change the delay time of "WR" signal by using external components.

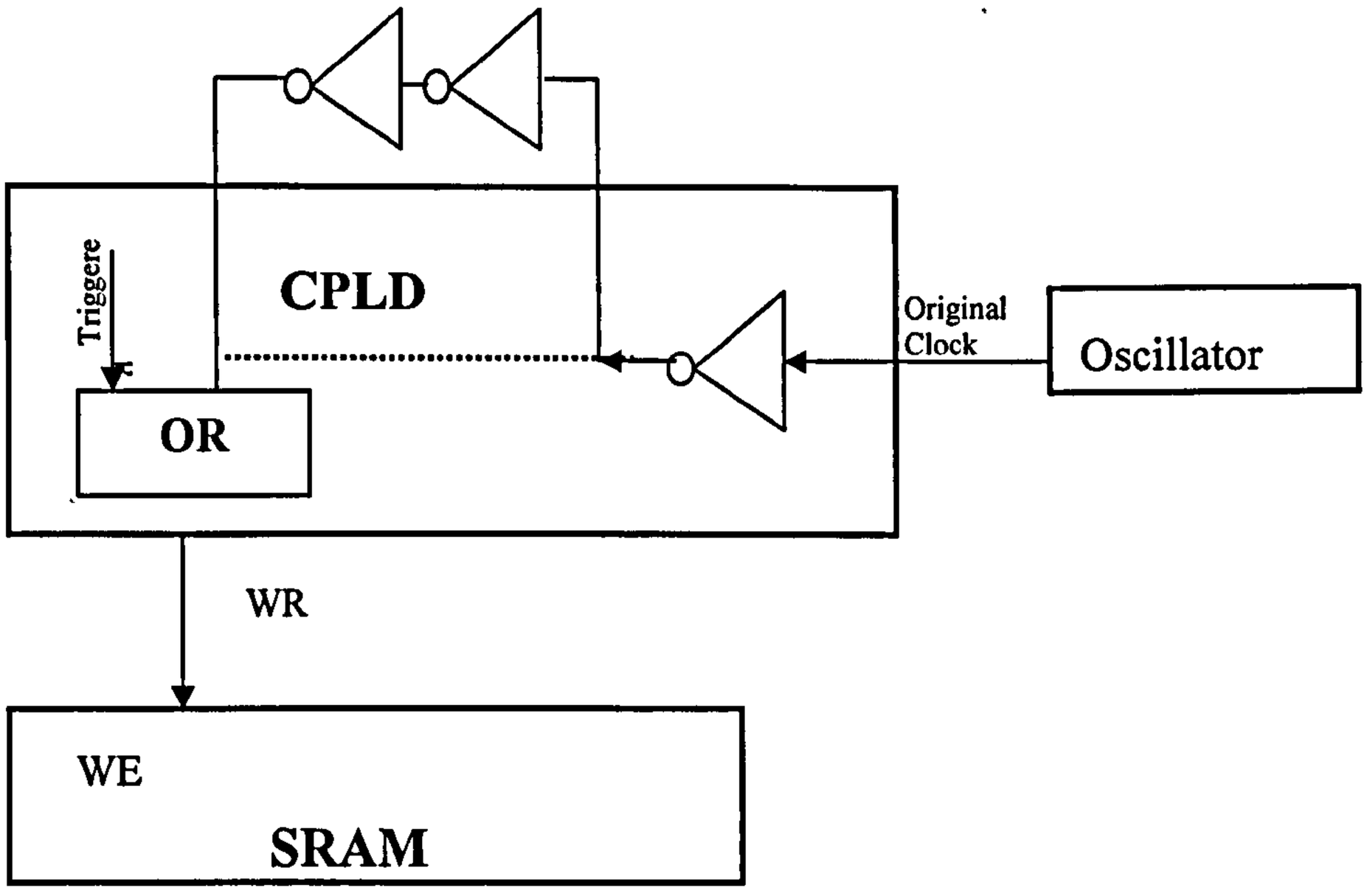


Fig. 4.17: Example of change delay time

In Fig.4.17, the dashed line is the designed route without adjustable delay. To add extra delay to this signal, in the midway, the signal is led outside of the CPLD and passes though two inverters (or a delay line) then re-enters the CPLD. By this way, the whole delay time of "WR" signal can be increased by the latency time of two

inverters. Furthermore, to finely adjust the additional delay time, a potentiometer can by applied. Such delay adjustment circuits are often used in Analogue Device's demo board for their ADC products. Fig.4.18 shows a part of the demo board for AD9012 (60M, 8bit ADC). In this circuit, ADC, Data- Latch and Memory are using the same clock source, but with a different delay for proper timing sequences. A pair of inverters is used to add extra delay time. Between two inverters, a potentiometer cooperates with the distributed capacitance in its traces and pads to build an RC network for adjustment of the delay time [76].

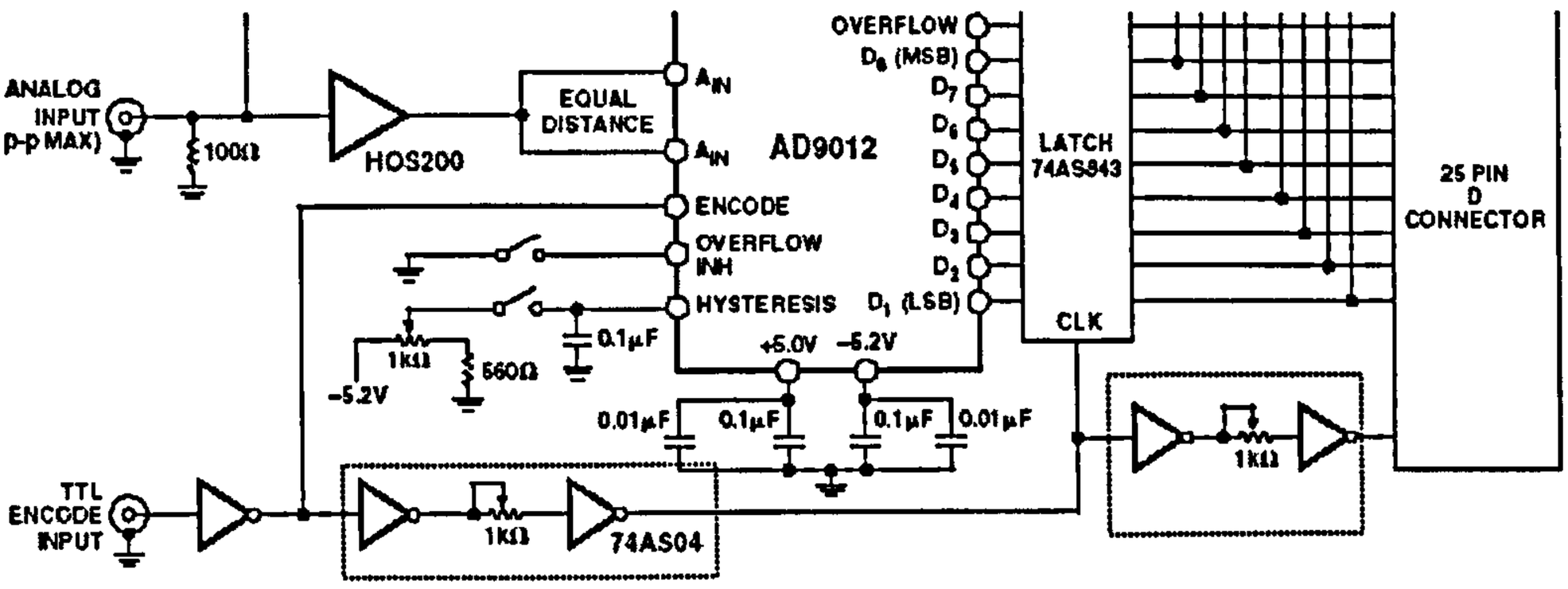


Fig. 4.18: Adjustable delay mechanism in the demo board of AD9012

The design of RAU takes the delay adjustment mechanism as shown in the demo-board of ADC9012. However, since the theoretical analysis has shown that without further adjustment, the timing sequence should meet the requirement of "write" operation, there is a little chance of needing the delay adjustment. Therefore, the schematic design did not implement the delay adjustment mechanism but in PCB design, allowance was made for the addition of this circuit should it be required.

4.1.4 Interface to CPU

In the Acquisition Board, the interface to CPU includes two parts: the electrical connection and the logical function.

MCU (Micro Controller Unit, i.e. AT89c52 in this design) is electrically connected to the CPLD through a 40-core flat cable. The connections are shown in Fig.4.19.

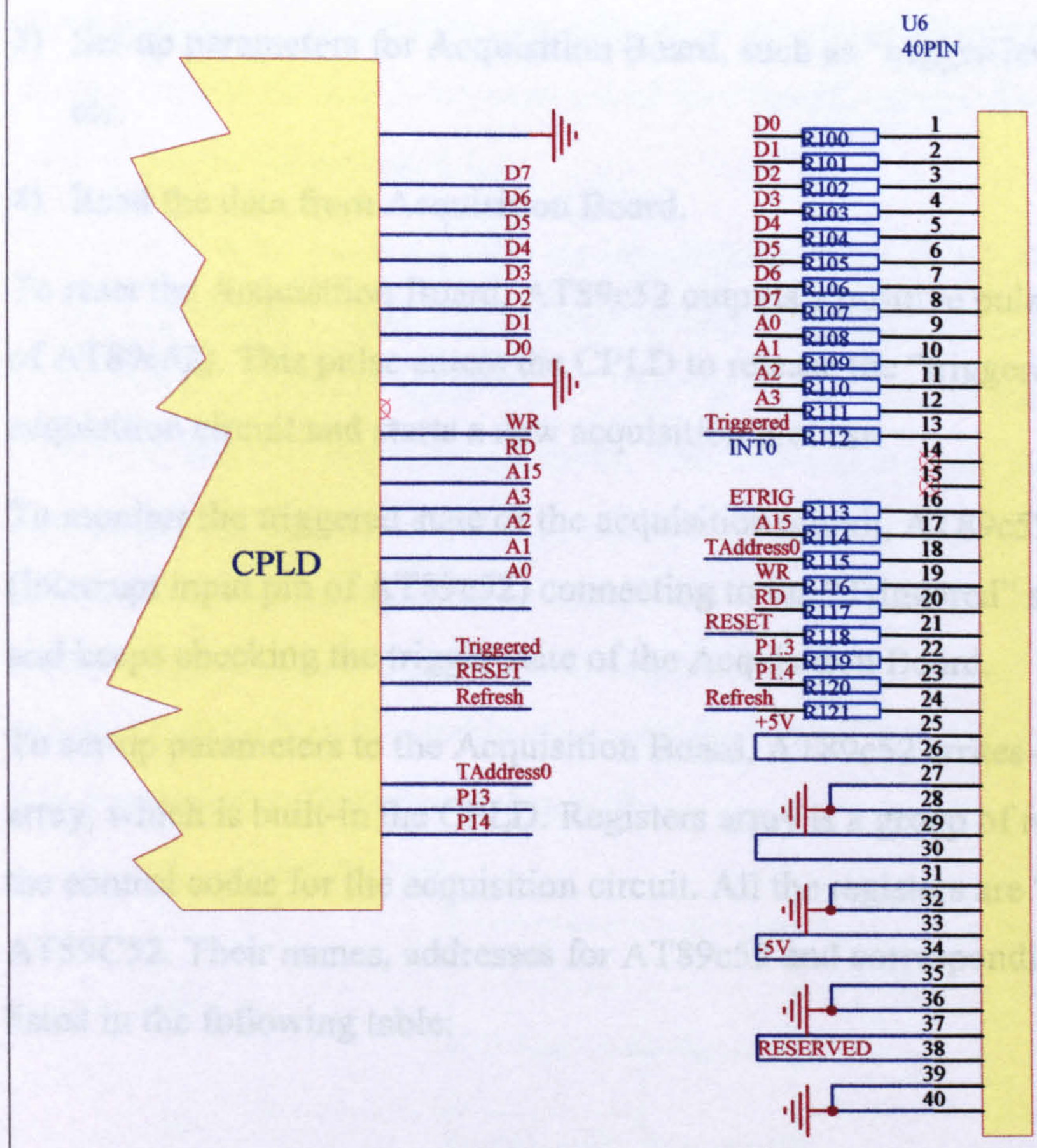


Fig. 4.19: Connections between CPLD and the socket of 40- core cable

In the right hand of Fig.4.19, there is a socket to host the 40-core cable linked to CPU board. Through the cable, data bus (D0—D7) is connected to the data bus of AT89c52 (D0—D7 of AT89c52); Address bus (A15, A3, A2, A1, A0) is connected to the relative address bus opposite and the other signal in the CPLD are connected to the corresponding signals on the CPU Board. (Refer to appendix C, and Table 4.2 in section 3.7). The electrical characteristics of this interface will be discussed later in this section. Next, the logic design of this interface is presented.

The logic function of the "Interface to CPU" is built in the CPLD. The Interface is designed to exchange data and commands with the AT89c52. All operations via this interface are listed below:

1) Reset Acquisition Circuit.

2) Monitor the state of Acquisition Circuit.

3) Set-up parameters for Acquisition Board, such as "trigger-level", "trigger-delay" etc.

4) Read the data from Acquisition Board.

To reset the Acquisition Board, AT89c52 outputs a positive pulse from "P1.3" (Pin 4 of AT89c52). This pulse enters the CPLD to release the "triggered" state of acquisition circuit and starts a new acquisition process.

To monitor the triggered state of the acquisition circuit, AT89c52 uses "p3.0" (Interrupt input pin of AT89c52) connecting to the "Triggered" signal on the CPLD and keeps checking the trigger state of the Acquisition Board.

To set-up parameters to the Acquisition Board, AT89c52 writes data into a registers array, which is built-in the CPLD. Registers array is a group of registers containing the control codes for the acquisition circuit. All the registers are "write-only" for AT89C52. Their names, addresses for AT89c52 and corresponding explanation are listed in the following table:

Table 4.2: Details of the registers array

Names of Registers	Address for AT89c52	Explanation
TriggerLevel	8000H(Hex)	7 bit data, resolution= $\frac{2V}{2^7} \approx 0.02V$
TriggerPosition	8001H	7 bit date, bit 0 to bit7 of Logic-Delay-Time, resolution= $\frac{MemoryLength}{2^7}$
TriggerDelayL	8002H	8 bit data, bit 8 to bit15 of Logic-Delay-Time
TriggerDelayH	8003H	2 bit data, bit 16 to bit17 of Logic-Delay-Time
Status of RAU	8004H	8 bit code, Reserved
Speed selection	8005H	3 bit data, see table 4.3 for the explanation

AT89c52 takes commands from a remote PC and writes the parameters into the above registers. These parameters will act on the acquisition circuit. In this way the PC can control the RAU. An example of how the PC selects the sampling speed has been illustrated in section 4.1.2.

For the AT89c52, these registers are like different units in an external device and the "write" operation to them can be done by implementing a so-called "external write instruction"—"MOVX @DPTR,A". "DPTR" is the indirect address register in AT89c52, and "A" is the Accumulator. This instruction sends the 8-bit data in the accumulator to the external device, which is pointed by "DPTR". When AT89c52 writes data to the external unit, it outputs 16-bit address and 8-bit data from the Address Bus and Data Bus, and then outputs a negative "Write" pulse. The address and data will be kept in a stable state until the "write" pulse is ended. The process of this instruction is illustrated in Fig.4.20.

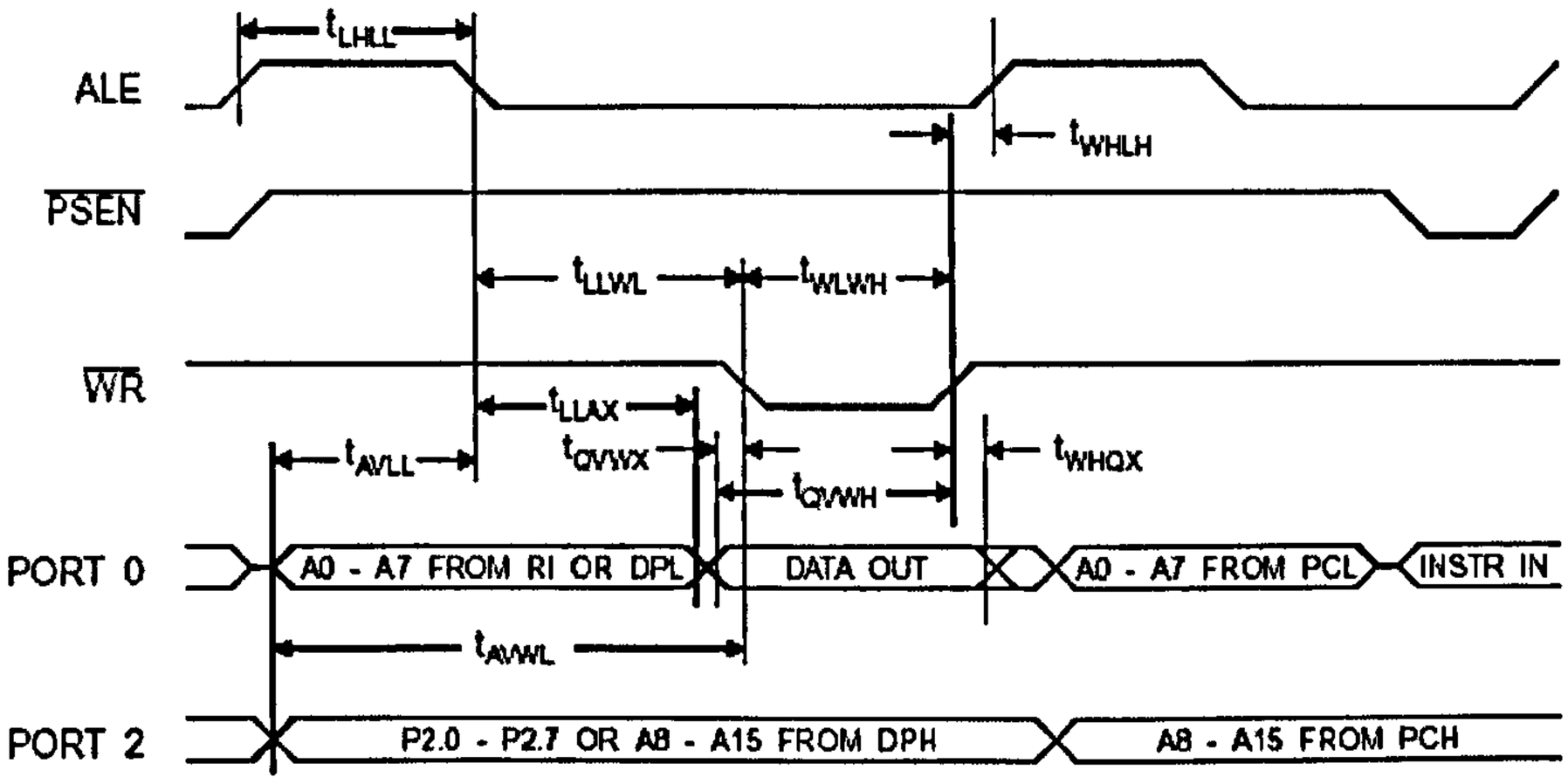


Fig. 4.20: External device "Write" circle of AT89C52

To match this operation of AT89c52, the CPLD builds the interface as shown in Fig.4.21.

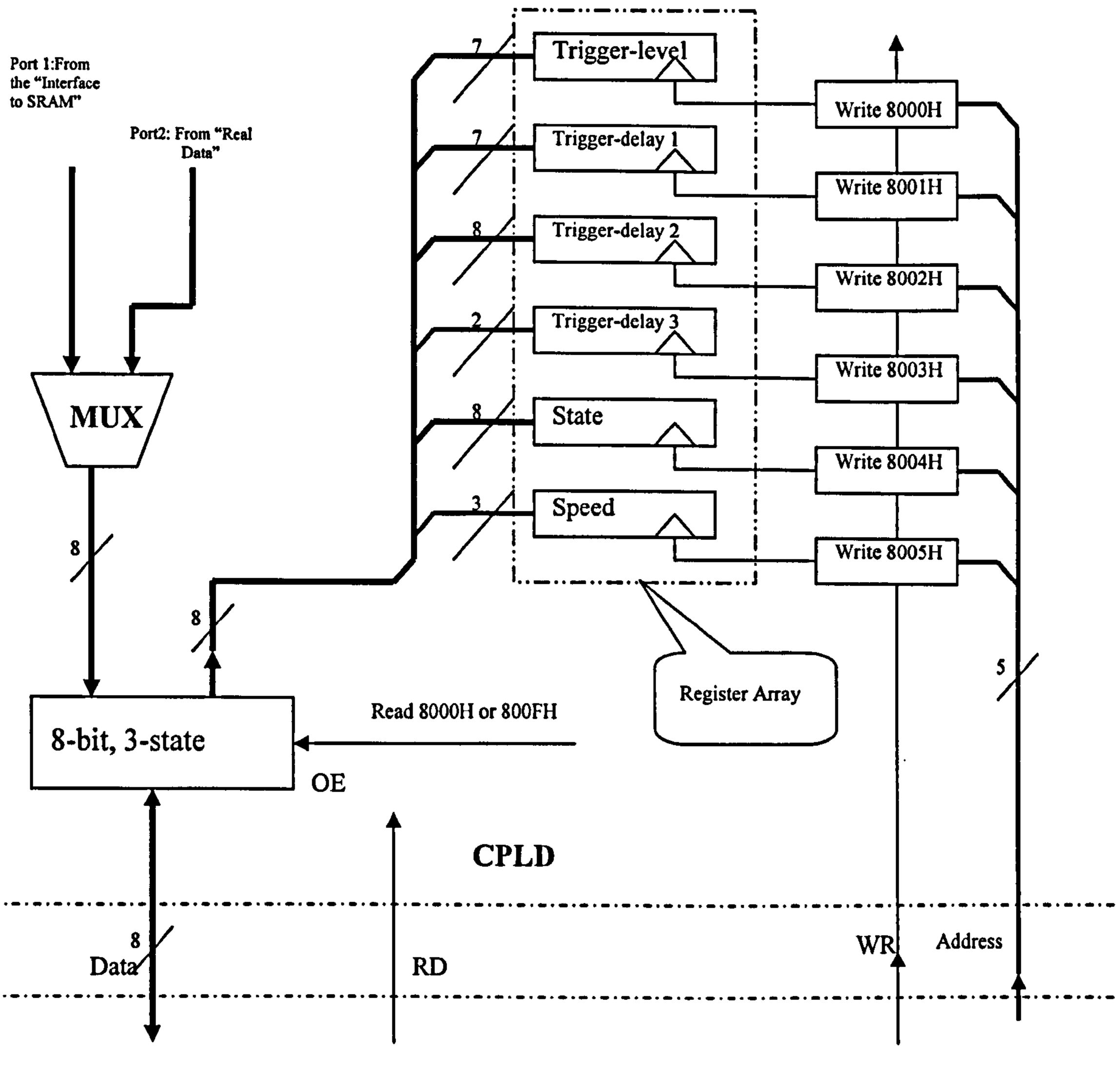


Fig. 4.21: Structure of the "Interface to MCU"

In the left hand of Fig.4.21, there is the "8-bit, 3-state buffer". When AT89c52 reads data from the CPLD, it outputs; when AT89c52 writes data to the CPLD, it inputs. As shown in Fig.4.21, the 5 registers build-up the "Register Array". All registers

input data from data bus, when the AT89c52 writes data into a certain register, the 5-bit "address" of the target register will appear in the Address Bus, while the active "WR" is given. Consequently, the decoder "Write ****H", shown in the right side of the figure, will assert a high level signal, which latches the present data into the register.

These registers are made up by several D-flip-flops. As an example, the structure of the 7-bit "Trigger-level" register is shown in Fig.4.22

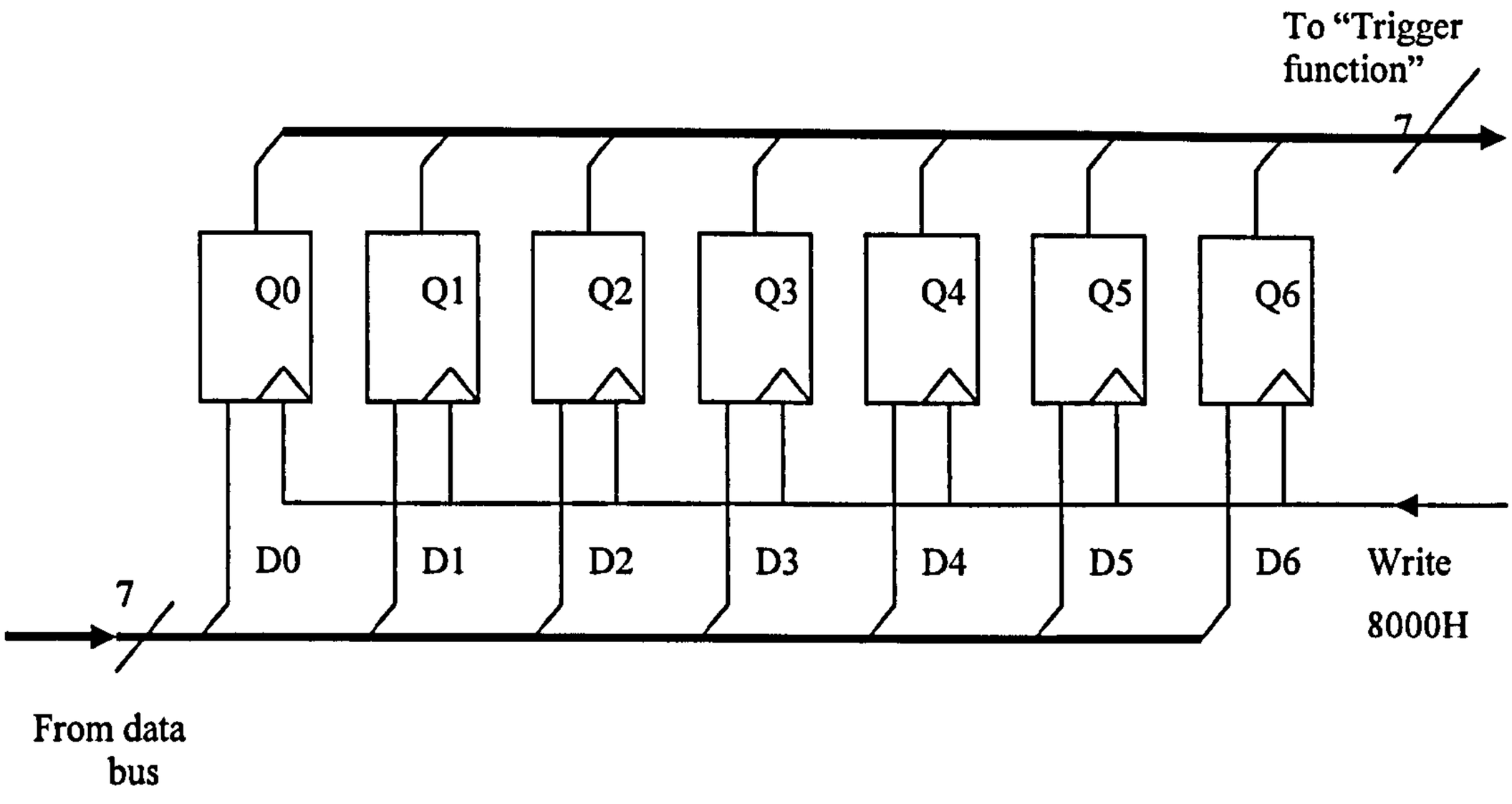


Fig. 4.22: Structure of "Trigger-level" register

This register consists of 7 pieces of D-flip-flops. The "D" inputs of the flip-flop 1, 2, 3, … 7 come from the responding bits of Data Bus. And the "Q" outputs are linked to the "Trigger function circuit". All clock ports of these flip-flops in this register are configured as "Latching at falling edge". All of them are controlled by "Write 8000H" decoder. Thus, when the "Write 8000H" decoder outputs a positive signal, the falling edge of that signal will latch the present data in this register.

As shown in Fig. 4.23, "Write 8000H" decoder consists of an address decoder (comparator) and an "AND" gate. When the address equals 8000H, and active "WR" is given, the positive "Write 8000H" signal will be asserted. Other decoders have the same structure.

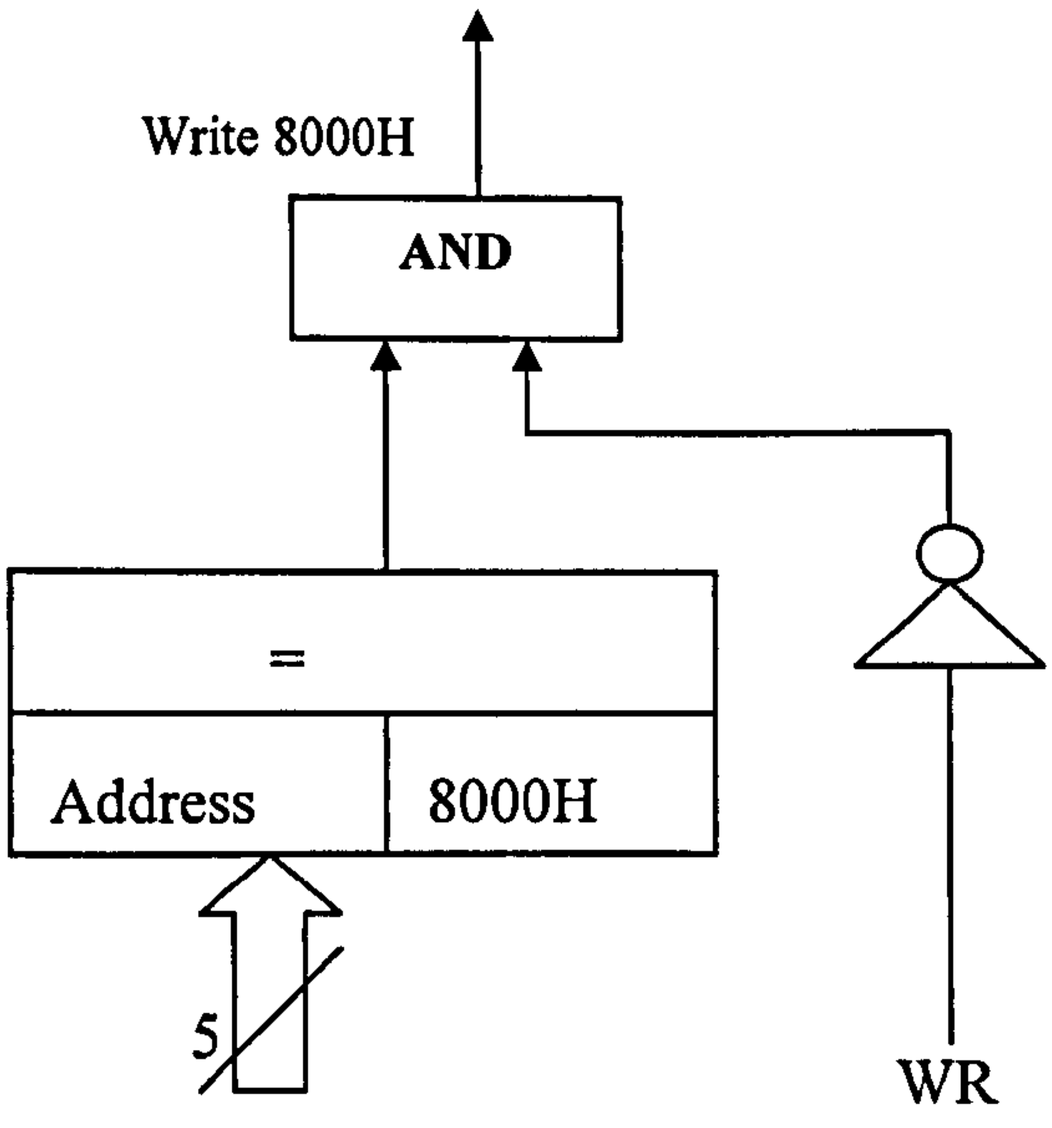


Fig. 4.23: Decoder of "Write 8000H"

It should be noted, that decoders just use 5 lines of all the 16 lines of address bus (A15, A3, A2, A1 and A0), i.e. the rest of the address bits are ignored. Therefore, 8000H is just a nominal address for the "Trigger-level" register, and many different addresses also point to the same register, e.g. 9000H also points to 8000H. However, since a 5 lines address can distribute 32 addresses, which are adequate to distinguish all the units in the CPLD, "Interface to CPU" just takes 5 address lines to build the circuit.

The above description explained how the AT89c52 "write" data to the CPLD with the built-in "Interface to CPU". Next, the "read" process will be explained.

AT89c52 reads two kinds of data from the CPLD: one is the data from the SRAM and another is so-called "Real data".

The definition of "Real Data" can now be explained. The "Read Data" comes from the ADC directly. Opposite the buffered data in the SRAM, and since the data is the output of the ADC in real-time, it is named as "Real Data".

For reading SRAM, as has been presented in earlier sections, when the AT89c52 reads 8000H by implementing "MOVX A,@DPTR", the data will be transmitted from SRAM to "Interface to CPU". This data arrives at "Port 1"of the "Interface to CPU" as show in Fig.4.21.

For reading "Real Data", AT89c52 implements a read instruction from the "800F" address. It makes the 8-bit "Real Data" register to transmit a byte to "Port 2" in the part of the "Interface to CPU".

Port 1 and Port 2 are two input ports of a multiplexor as shown in Fig.4.21. When the AT89c52 reads 8000H, it links Port 1 to the data bus of AT89c52. When the AT89c52 reads 800FH, it links Port 2 to the data bus. Thus the AT89c52 is able to read data from SRAM by reading 8000H and read "Real Data" by reading 800FH (See Fig. 4.21).

No matter if the RAU is triggered or not, operators can read the "Real Data" at any time. To read the "Real Data", the AT89c52 gives a latch pulse "Refresh Buffer" to the "Read Data" register, the rising edge of the pulse latches a byte output from ADC, and then the AT89c52 reads it by implementing a "MOVX A,@DPTR" instruction (Read 800FH) and sends it to the remote PC immediately. In this manner, the real-time signal can be displayed on the PC. This function is just for debugging and commissioning use. The "Real Data" register is built-in to the CPLD as shown in Fig.4.24:

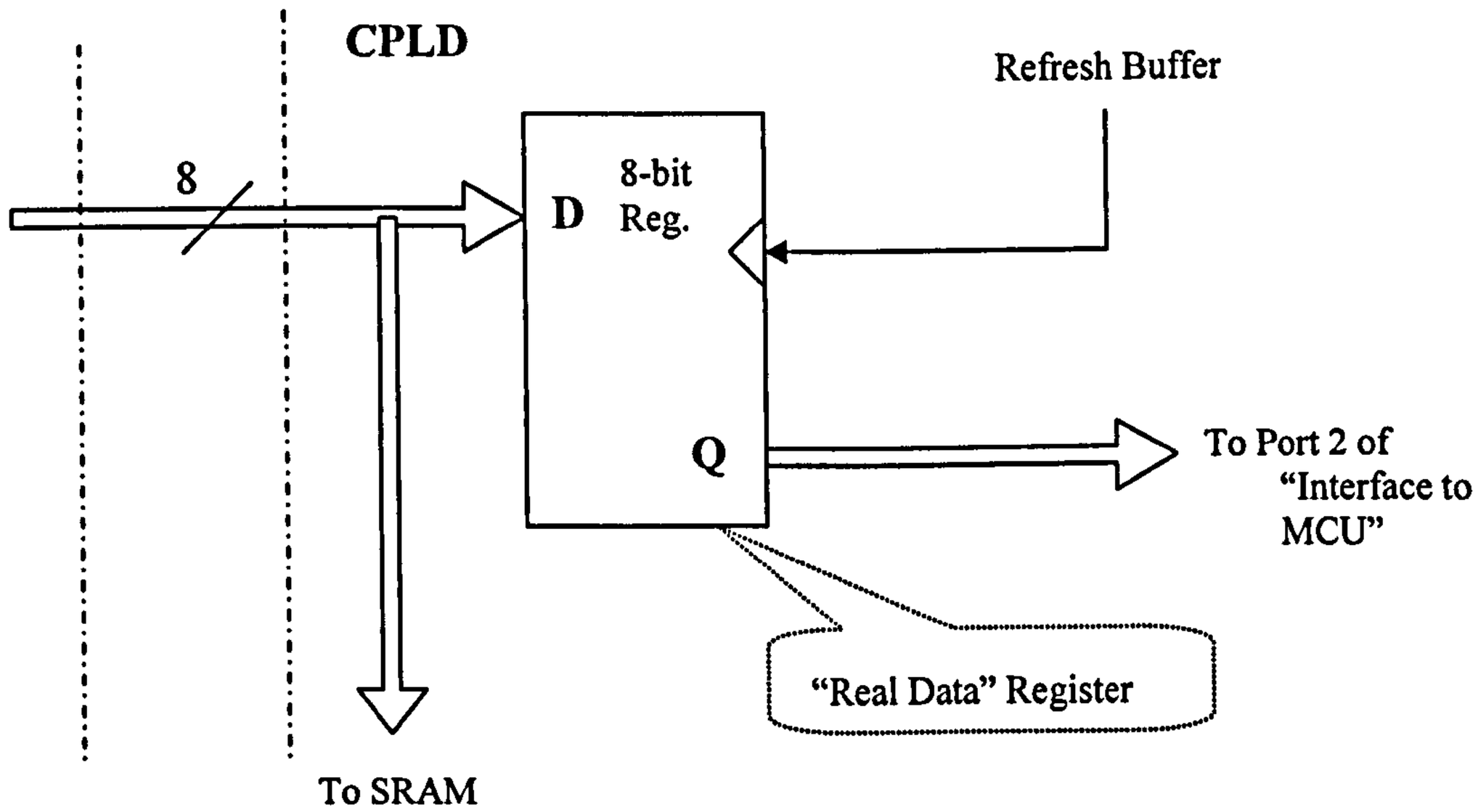


Fig. 4.24: Logic diagram of " Real Data" register

The register is formed by 8 D-Flip-flops as the other registers above. The inputs of these flip-flops come from the ADC. Its 8-bit outputs linked to "Port 2". AT89c52 does not input data from the ADC directly but through a latch (register), because the "read" period of the AT89c52 is 1 microsecond. During this period, the input data in the Data Bus of AT89c52 should be kept in a stable state, but without latching, the data output of the ADC would be dynamic (changed 80M times per second).

By repeating the action of giving a "Refresh Buffer" pulse and "Reading 800FH", AT89c52 can continuously read the real-time output of the ADC and continuously sends them to a PC. Therefore, a PC can display a real-time signal graphically. Obviously, this function is useless for practical EMC measurement, because without trigger function, the signal cannot be synchronized, and the sampling rate is too low to capture a transient signal (200kSPS roughly). But it gives a designer a direct way to observe the input signal and analyse the working state of the circuit. It is useful for debugging and commissioning work. For example, when a sine wave signal is input to the RAU, the "Real Data" can be displayed in a PC as shown in Fig.4.25.

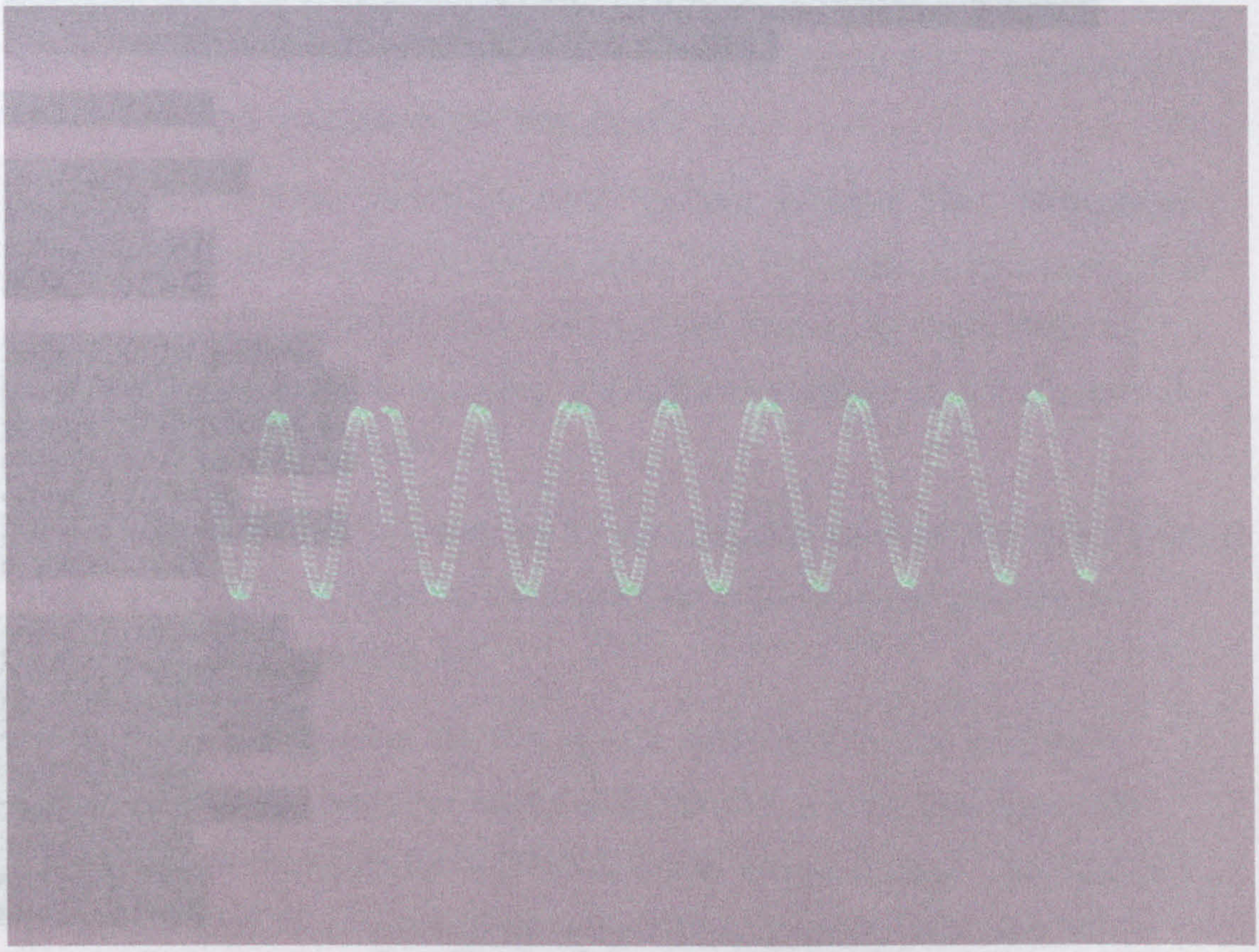


Fig. 4.25: Waveform of the "Real Data"

Every times the AT89c52 reads 128 bytes data from A/D, i.e. 128 sampling points, and send them to PC for display. As every screen can display 628 points in horizontal, the graphic shows 5 discontinuous sections. Also, as the reflection on the screen, the graphic shows a shadow closed to original image.

Thus, apart from the functions required by design specification, there is also a "Real Data" function used by designer for commissioning work. In "Real Data" mode, RAU acquires signal and send the data to PC in a real time. The sampling speed of the "Real Time" acquisition mode depends on the wireless data communication speed, as the data transmission takes most time in this process. In this application, with Bluetooth modem, the sampling speed is 40kSPS. Please note, this "Real Data" mode is not provided to users of this measurement system but only used for debugging work of the RAU.

The Verilog-HDL description of this "Interface to CPU" in the CPLD is listed below (refer to appendix E):

```
module registers(Data,Address,wr,rd,TriggerLevel,TriggerPosition,TriggerDelayL,
                                                    TriggerDelayH,Status,SpeedSelection,Port1,
                                                    Port2,ReadRAM);

inout [7:0] Data;

input [4:0] Address;
input wr,rd;
input [7:0]Port1;
input [7:0]Port2;

output [6:0] TriggerLevel;
output [6:0] TriggerPosition;
output [7:0] TriggerDelayL;
output [1:0] TriggerDelayH;
output [7:0] Status;
output [2:0] SpeedSelection;
output ReadRAM;

reg [6:0] TriggerLevel;
reg [6:0] TriggerPosition;
reg [7:0] TriggerDelayL;
reg [1:0] TriggerDelayH;
reg [7:0] Status;
reg [2:0] SpeedSelection;
wire [7:0] Port;
wire [7:0] Port1;
wire [7:0] Port2;

wire [7:0] Data;
```

```
always @ (negedge wr)

                begin
                        case (Address)
                                5'b 10000: TriggerLevel=Data[6:0];
                                5'b 10001: TriggerPosition=Data[6:0];
                                5'b 10010: TriggerDelayL=Data;
                            5'b 10011: TriggerDelayH=Data[1:0];
                                5'b 10100: Status=Data;
        5'b 10101: SpeedSelection=Data[2:0];
//                                      5'b 10110: Atenuation=Data[2:0];
                        endcase

end

assign Port[7:0]=(Address==5'b11111)? Port1[7:0]:Port2[7:0];

assign ReadRAM=!((Address==5'b11111)&!rd);

assign Data[7:0]=(Address[4]&!rd)? Port[7:0]:8'bz;

endmodule
```

In this file, "Data" is the data from and to the AT89c52; "wr" and "rd" is the "WR" and "RD" signal from the AT89c52; the registers have the definitions as shown in table 4.4; "ReadRAM" is the signal, generated in this "Interface to CPU" and to be sent to "Interface to SRAM" as described in previous section; Port 1 is the access to SRAM and Port 2 is the access to "Real Data".

The logic design of the "Interface to CPU" has been presented. Next, the electrical connection will be discussed. As shown in Fig 4.33, the connection between CPLD and the AT89c52 includes the traces on board and wires of the cable. Since the CPLD and the AT89c52 are operating with different voltages, the I/O tolerance of both sides must be considered.

In the interface of the CPLD, there are 11 input connections (WR, RD, P13, P14 etc). 2 output connections (Triggered, Taddress0) and 8 bi-directional connections (D0~D7) (Refer to Appendix A).

As specified in the datasheet, the I/Os on each XC9500XL device are fully 5V tolerant, even though the power supply of XC9500XL is 3.3V. This allows 5V CMOS signal to connect to the XC9500XL inputs without damage. Thus, the 11 input pins of CPLD can be connected to the AT89c52 directly. But other I/O (Input/Output) pins and output pins have problems on driving a 5V CMOS device,

such as AT89c52.The reason is that the logic-high threshold for 5V CMOS is 3.5V, whereas the logic-high output of XC9500XL family device is 2.4V-3.3V, which can be seen in Table 4.5 [77]:

Table 4.3: Logic threshold for different logic families

Items	V_{OL} (Max)	V_{OH} (Min)	V_{IL} (Max)	V_{IH} (Min)	V_{CC}	GND
5V CMOS	0.5V	4.44V	0.8V	3.5V	5V	0V
5V TTL	0.4V	2.4V	0.8V	2.0V	5V	0V
3.3VCMOS	0.4V	2.4V	0.8V	2.0V	3.3V	0V

There are two solutions for this problem. One is applying a "level-translator", which is designed to match different voltages, such as TI's 74ALVC4245 and Maxim's MAX3002 (Bi-directional) [78]. Another solution is attaching pull-up resistors in the input side of the 5V CMOS device. This is an experimental solution for Altera's 3.3V CPLD driving 5V CMOS device. This method was well known by most CPLD application engineers, even before it was officially suggested by Altera. But, up to now, Xilinx has not encouraged their users to use such pull-up resistors in their official documentation.

In the PCB design, at the bi-directional ports and the input ports of AT89c52, the positions of the pull-up resistors have been reserved. The locations for bi-directional 3.3V –5V translator MAX3002 have also been reserved [78]. The final circuit did not use either translator or pull-up resistors. It was found that XC9500XL family devices can drive Atmel's MCU AT89c52 directly.

Another potential electrical problem for the connection between the CPLD and the AT89c52 is "Ringing" or "Overshoot/Undershoot". The reason for this problem is the ground plans for the AT89c52 and the CPLD are on separate boards. Even

though the two ground planes are linked by a number of wires, they may have slightly different level for a dynamic signal. To prevent "Overshoot/Undershoot", it is suggested to reserve a series resistance location for the value between 20Ω and 50 Ωon the connection traces [60, 79]. Therefore, several resistors are attached to the transmission lines in series (R100~R121, in Fig. 4-19). These resistors can also prevent to CPLD from the "surge" damage. In this design, the 5v power supply for the AT89c52 and the 3.3 V power supply for CPLD cannot set-up at an exactly simultaneous time. "Surge" may be present at the moment when the AT89c52's output signal arrived at the input pins of the CPLD before the CPLD is powered. 50~1000 Ω series resistor is suggested to reduce such "Surge" current [80].

4.1.5 Trigger functions

As a fundamental function of the RAU, the principle and structure of the Trigger function has been described in section 2 of this chapter (overall design of RAU). This section details the logic design and its implementation.

The trigger function includes two parts: trigger recognizing circuit and trigger delay circuit. In the RAU, the trigger recognizing circuit is a comparator to compare the level of measured signal and the set-up trigger-level. It can be built by either an analogue comparator or digital comparator. The analogue comparator has the advantage of high response speed. However, it needs an analogue comparator circuit and DAC (Digital to Analogue Converter) circuit. That means it would cost more components and the PCB area. Whereas the digital comparator can be built within the CPLD, it neither adds any hardware nor increases the PCB size. After examining the digital comparator using Xilinx simulation tool "Time Analyser", it was found that its speed is adequate. Therefore, the digital comparator was chosen. The logic design of this comparator is shown below in Fig.4.26:

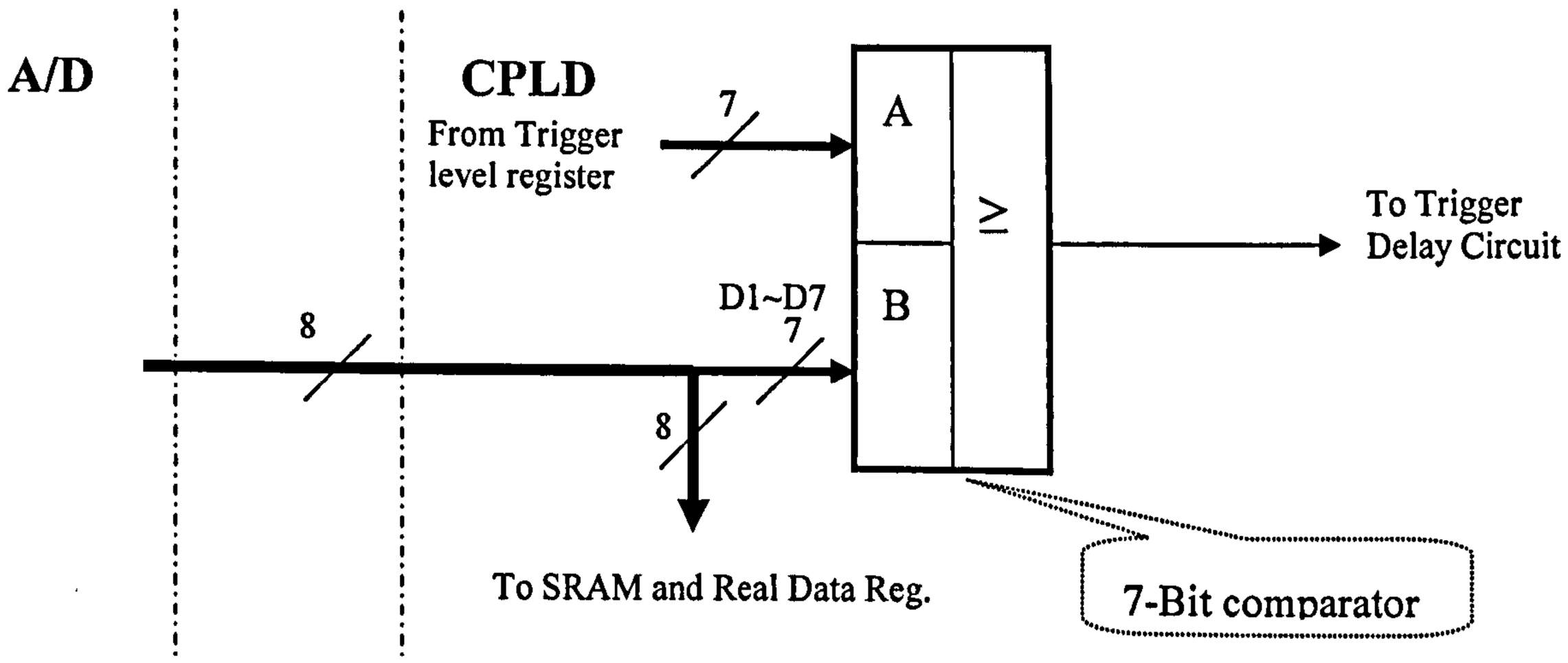


Fig. 4.26: Logic diagram of comparator

In the circuit, the ADC sends 8-bit data to the CPLD. The highest 7 bits input to B port of the Comparator (7-bit precision has been adequate for the measurement). The 7-bit data are compared with the data in A port, which is the value stored in the "Trigger-level register". Once the ADC's output is greater or equal the trigger-level, the Comparator outputs a logic "1" (high level signal) to the trigger-delay circuit. This signal is defined as the "original-trigger-signal" in this thesis and named as "trigger 1" in the Verilog-HDL file.

The trigger-delay function, as described earlier, is to adjust the position of the trigger point along the recorded area. It applies a counter to implement a Logic-Delay for this adjustment. Logic-Delay is the sum of the "pre-trigger" and "delay time", which is set-up at the PC and sent to the RAU. The adjustment resolution is 1% of the whole memory. The memory has 512k units, which takes 512k "Address Counting" clocks. 1% of the memory is roughly 5k units, which takes 5k "Address Counting" clocks. That means every 5000 "Address Counting" clocks generate a "Logic-Delay" clock. It has roughly $\frac{1}{2^{12}}$ frequency of the "Address Counting" clock. Thus, this design takes 12^{th} bit (Q-11) of the 19-bit address counter as the counted clock for this "Logic-Delay" counter and names it as "CLK_11". Fig.4.27 shows the logic circuit of the trigger-delay function.

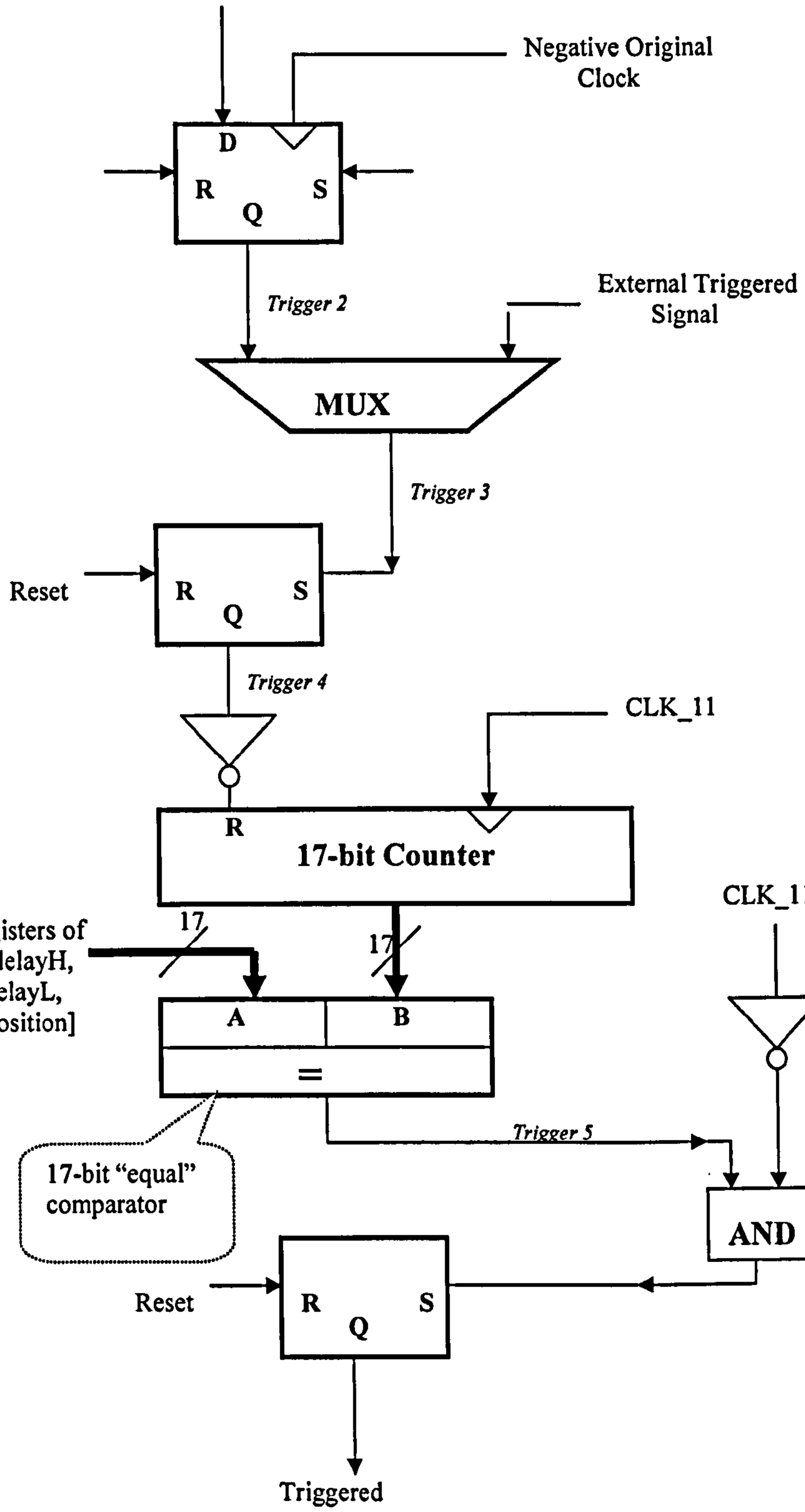


Fig. 4.27: Logic circuit of the trigger-delay function

The output signal of the "trigger-level" comparator is "trigger 1". It is latched by negative "original clock" in a D-Flip-flop at every second half-period of the original clock. This flip-flop is used to remove the unstable comparing result due to the data switching of ADC at the beginning of every conversion period. After this, "trigger 2" enters a multiplexer, which selects the trigger source (External trigger function is not applied in the real product, but reserved in this design). After the multiplexer, the trigger signal (trigger 3) drives the "set" pin of an RS-Flip-flop. Once the "original-trigger-signal" outputs a high pulse, the RS-Flip-flop will be set and will keep the output to logic "high" until it is released by the "Reset" signal. The output of the RS-Flip-flop becomes "trigger 4" and is connected to the "reset" port of a 17-bit counter through an inverter. Thus, once the "trigger 4" is set to logic "high". The "17-bit counter" will start to count the CLK_11. The output of the counter is linked to a 17-bit comparator and compared with the number stored in the registers of "Trigger-delay H", "Trigger-delay L" and " Trigger-position", which are respectively storing the high 2 bits, medium 8 bits and low 7 bits of the trigger-delay value. When the counted clock number equals the value in the registers, i.e. the set-up delay time has elapsed. The 17-bit Comparator outputs "equal" signal "trigger 5". Since the "equal" signal is a transient signal, it should be latched. Thereby, "trigger 5" is linked to "set" port of a RS-Flip-flop and sets it to logic "1". Once the triggered signal is set, it will keep the state until the "Reset" signal comes. "Reset" signal comes from P13 of the AT89c52. It can release the triggered state and start a new acquisition. The whole process of the trigger circuit can be summarized as described below:

Once the measured signal exceeds the trigger-level, it will start the timer (17-bit counter and 17-bit comparator). After a certain delay time, the timer gives the final triggered signal.

4.1.6 Contingencies for debugging

Due to the complexity of the Acquisition Circuit, test points should be made to observe the signals at various points in the circuit. Especially, for the CPLD, since most logic circuitries are built inside of the chip, it is always helpful to arrange some pins to bring the inner signal outside. Furthermore, for the small package of CPLD and the tiny spaces between their pins, these pins should be extended away from the chip for more spaces to accept the probes of oscilloscope or other test equipment. 26 pins in the CPLD have been arranged for this purpose. They are labelled with TAddress1 ~ Taddress18 and Tdata0 ~ Tdata7 in Schematic Circuit Sheet (Appendix A) . TAddress1~18 are arranged to output the signals from CPLD. Each output pin is led to a through hole, the size of which can hold a probe. For a convenient observation, each pin is also attached to an LED (Light-Emitting Diode) as shown in Fig.4.28.

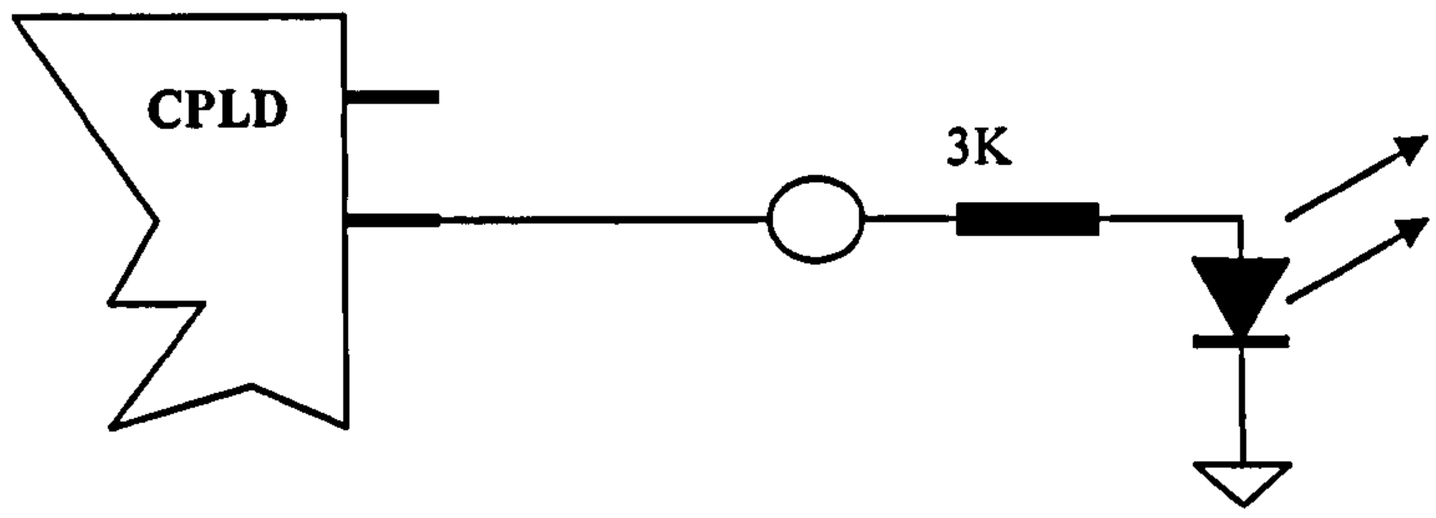


Fig. 4.28: Configuration of the output test pin of CPLD

Tdata0 ~ Tdata7 pins are arranged to input a signal from some digital switches on the PCB. Fig.4.29 shows the connection of an "input test pin".

All these test circuit are located on the top side of the board as shown in Appendix C.

With the interconnection links within the CPLD, any inner route can be temporarily diverted to the "output test pins" and the signal can be display or measured. For example, when

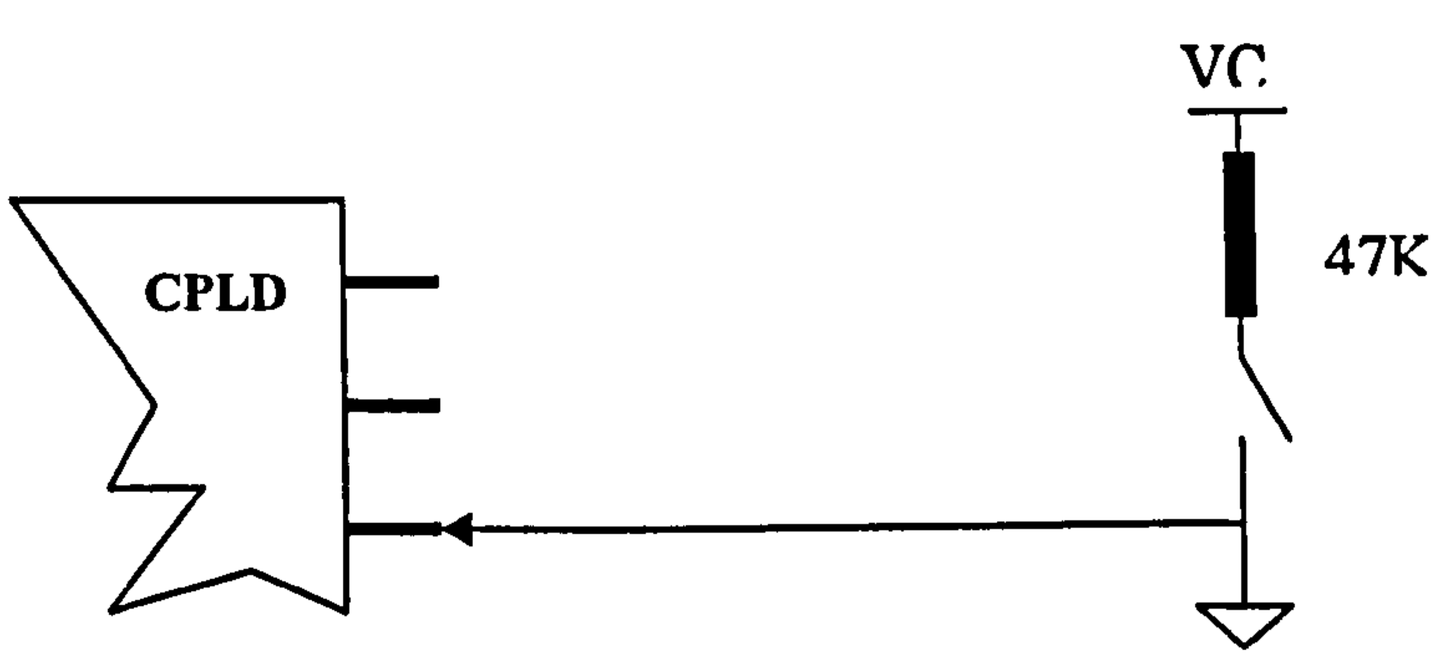


Fig. 4.29: Structure of the input test pin

debugging the "Trigger function circuit", introducing the intermediate signals, such as "trigger 2", "trigger 3", "trigger 4" or the "17-bit delay timing counter", the working state of the trigger circuit can be observed. In this manner, the circuit can be checked step by step. The "test input pins" (TData0 ~ TData7) can give a temporary input to every circuit inside the CPLD. For example, before the trigger function is accomplished, the test input pin can give a simulated "triggered" signal to "The interface to SRAM" for commissioning.

Also, for debugging and commissioning purposes, in this Acquisition Board, some ground points are placed in 4 corners, which is used for attaching "Ground clips".

In summing-up all the circuits of "Interface to ADC", "Interface to SRAM", "Interface to CPU", "Registers Array" and "Trigger Function", the whole design of the logic circuit in CPLD has been completed. The final Verilog-HDL description is listed in appendix E.

4.1.7 Analogue channel

In the Acquisition Board, the circuit after the BNC connector and before the A/D converter is "Forward Analogue Channel" or simply "analogue channel". This analogue channel achieves three functions:

1. Impedance match: It give a high input impedance to the sensor and give a low output impedance to the A/D converter

2. Amplitude match (+1V offset): Sensors output a bipolar signal with 2V peak-to-peak amplitude from –1V to + 1V, whereas the A/D converter has 0-2V full scale. That means, in the A/D converter, 0V to 2V analogue signal takes 0 to 255 digital codes. Thus 1 volt offset must be added in the original signal before it is input to the A/D converter. Thus, –1V to +1V analogue signal from the sensor will be converted to digital 0-255.

3. Bandwidth limitation: According to the functional design specifications, the analogue channel should ensure 20MHz pass bandwidth and cut off all frequency components above 40 MHz (Nyquist frequency of this acquisition system).

The analogue channel can be described using Fig.4.30:

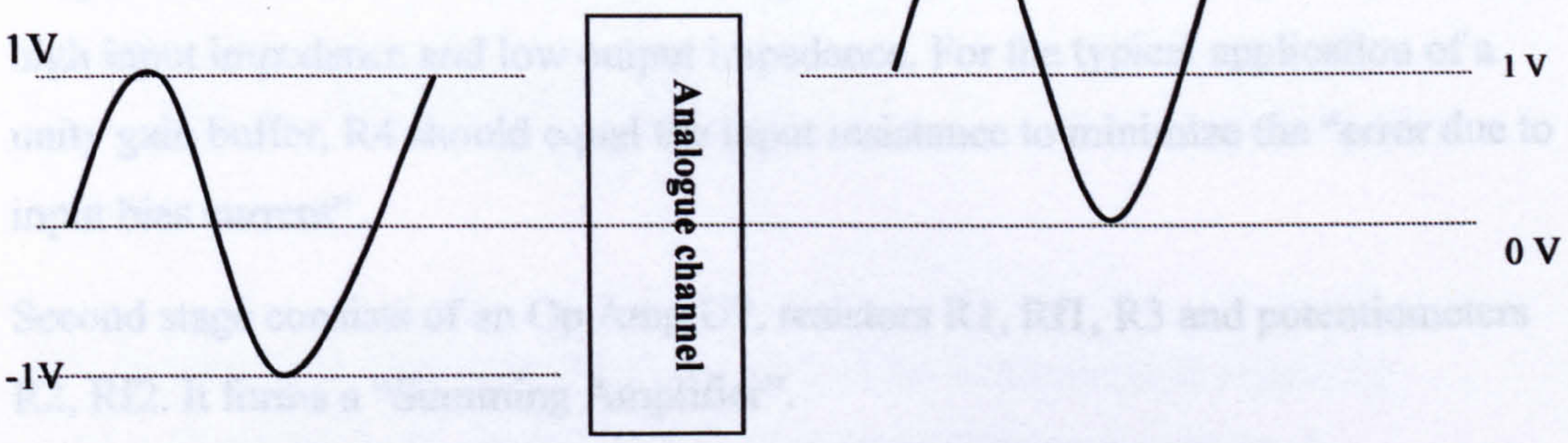


Fig. 4.30: Relationship between input and output of the analogue channel

4.1.7.1 Circuit design of the analogue channel

The analogue channel is made up of two amplifier stages as shown in Fig.4.31

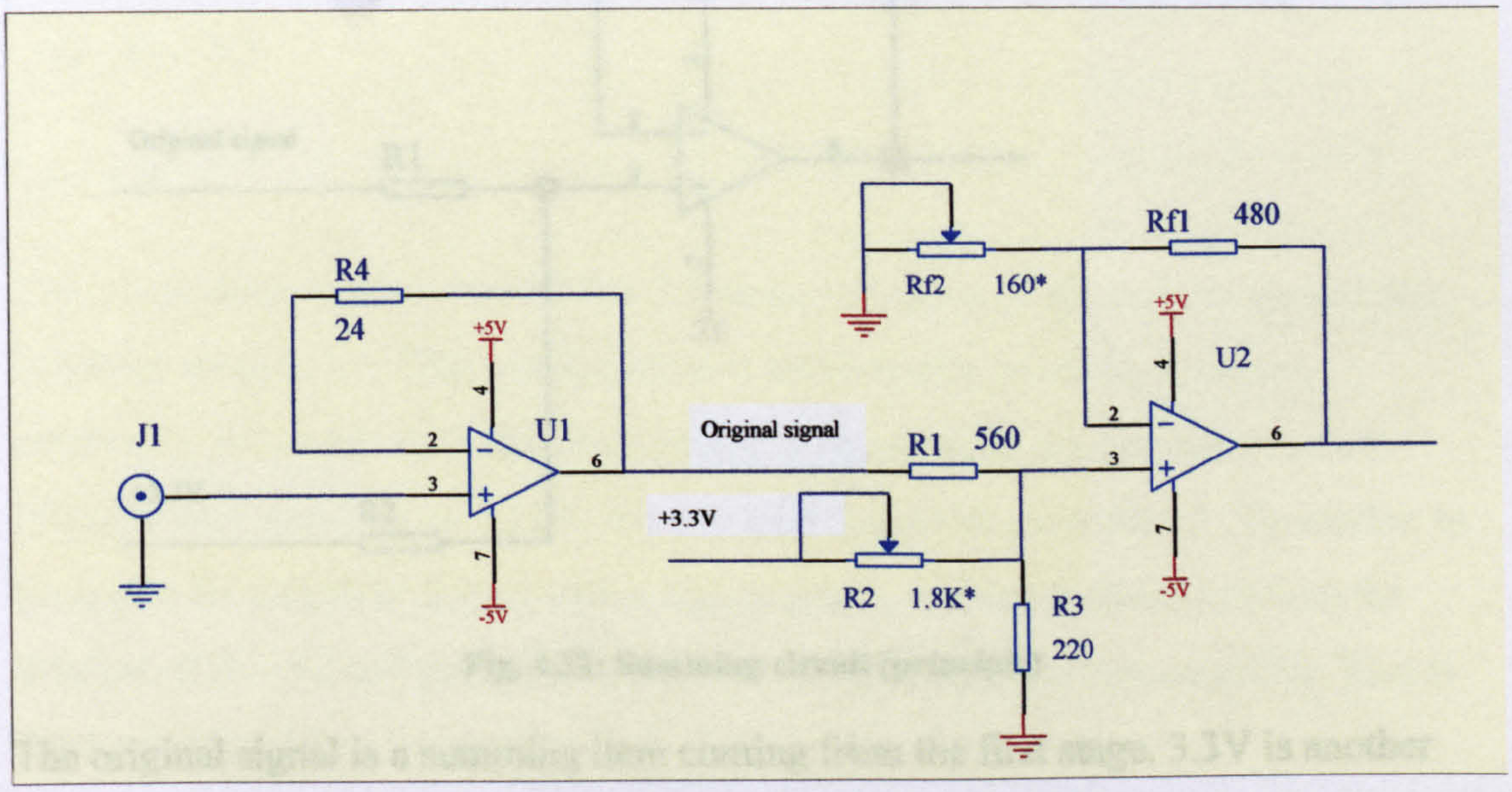


Fig. 4.31: Two stages of the analogue channel

The Operational Amplifier LM7171 has been found suitable for this design. It has 200MHz unity-gain bandwidth $\pm 5V$ operational power supply [81].

The first stage is a unity gain buffer, which is made up by an Op Amp (Operational Amplifier) U1 and a resistor R4. It is designed to buffer the input signal by making a high input impedance and low output impedance. For the typical application of a unity gain buffer, R4 should equal the input resistance to minimize the "error due to input bias current".

Second stage consists of an Op Amp U2, resistors R1, Rf1, R3 and potentiometers R2, Rf2. It forms a "Summing Amplifier".

As has been pointed out before, the analogue channel should give 1volt offset to the original signal. Theoretically, this can be done by a typical two items summing amplifier as shown in Fig.4.32:

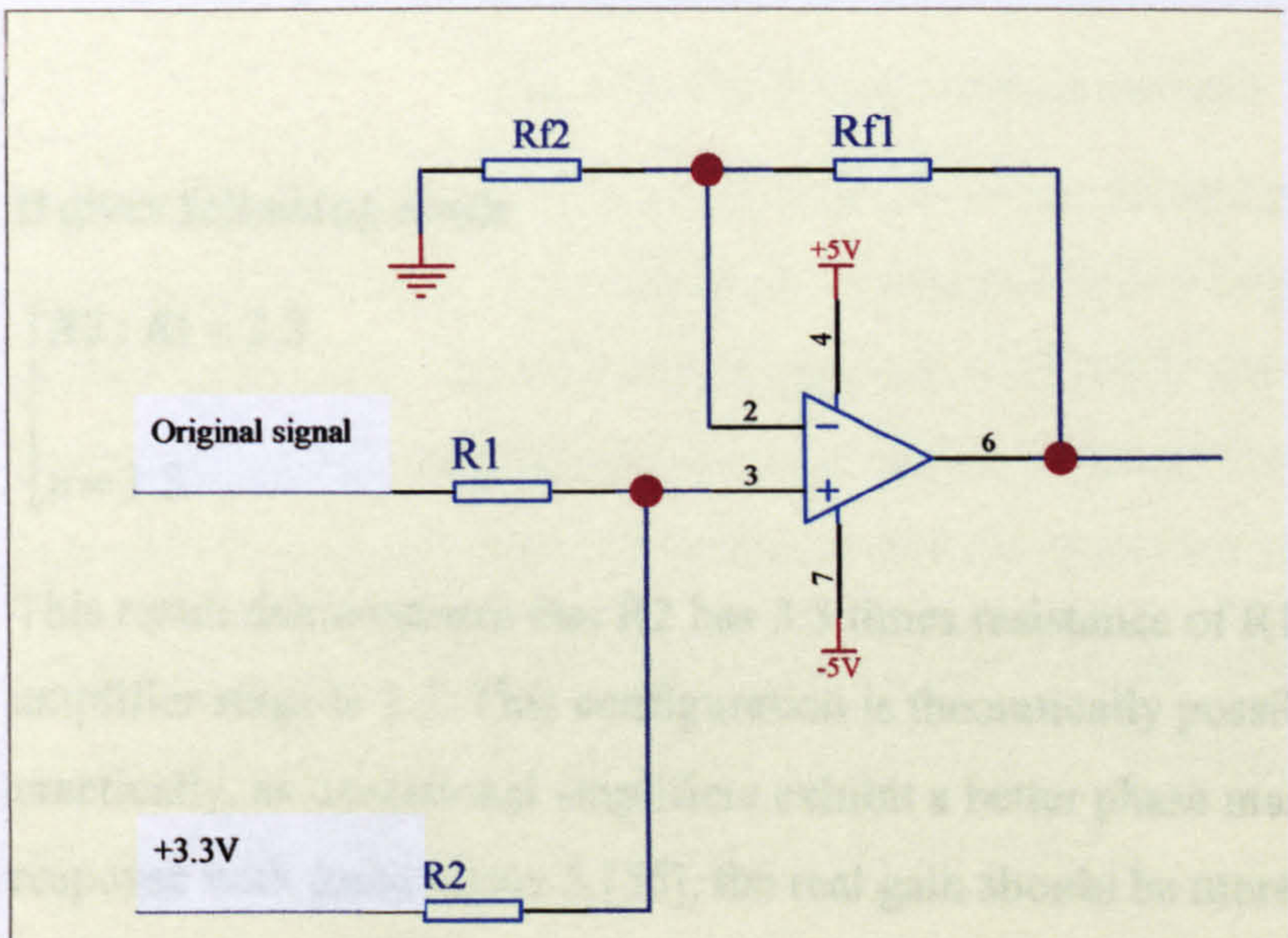


Fig. 4.32: Summing circuit (principle)

The original signal is a summing item coming from the first stage. 3.3V is another summing item coming from the power plane of this board. The two signals are added and amplified by the amplifier U2 and output from pin 6 of the Op Amp. The summing result is given by Equation (4.1):

$$Vout = \frac{R2 \bullet Voriginal + R1 \bullet 3.3V}{R1 + R2} \bullet (\frac{Rf1}{Rf2} + 1) \qquad \textbf{(Equation 4.1)}$$

Let *Rf1/Rf2* +1 = *n*, i.e. the close-loop gain of the Op Amp, Equation (4.1) becomes

$$Vout = \frac{R2 \bullet Voriginal + R1 \bullet 3.3V}{R1 + R2} \bullet n \qquad \textbf{(Equation 4.2)}$$

This summing amplifier should give 1 volt offset to the original signal, i.e. $Vout = Voriginal + 1V$. Based on this, Equation (4.3) can be obtained:

$$\begin{cases} R2/(R1+R2) \bullet n = 1 \\ \\ 3.3 \bullet R1/(R1+R2) \bullet n = 1 \end{cases} \qquad \textbf{(Equation 4.3)}$$

It gives following result:

$$\begin{cases} R2 : R1 = 3.3 \\ \\ n = 1.3 \end{cases}$$

This result demonstrates that R2 has 3.3 times resistance of R1 and the gain of this amplifier stage is 1.3. This configuration is theoretically possible, however, practically, as operational amplifiers exhibit a better phase margin and transient response with gains above 3 [55], the real gain should be more than 3. Thereafter, to configure the amplifier circuit with a higher gain, a resistor is added between the junction of R1, R2 and ground to attenuate the input signal of this amplifier. That is shown in Fig.4.33.

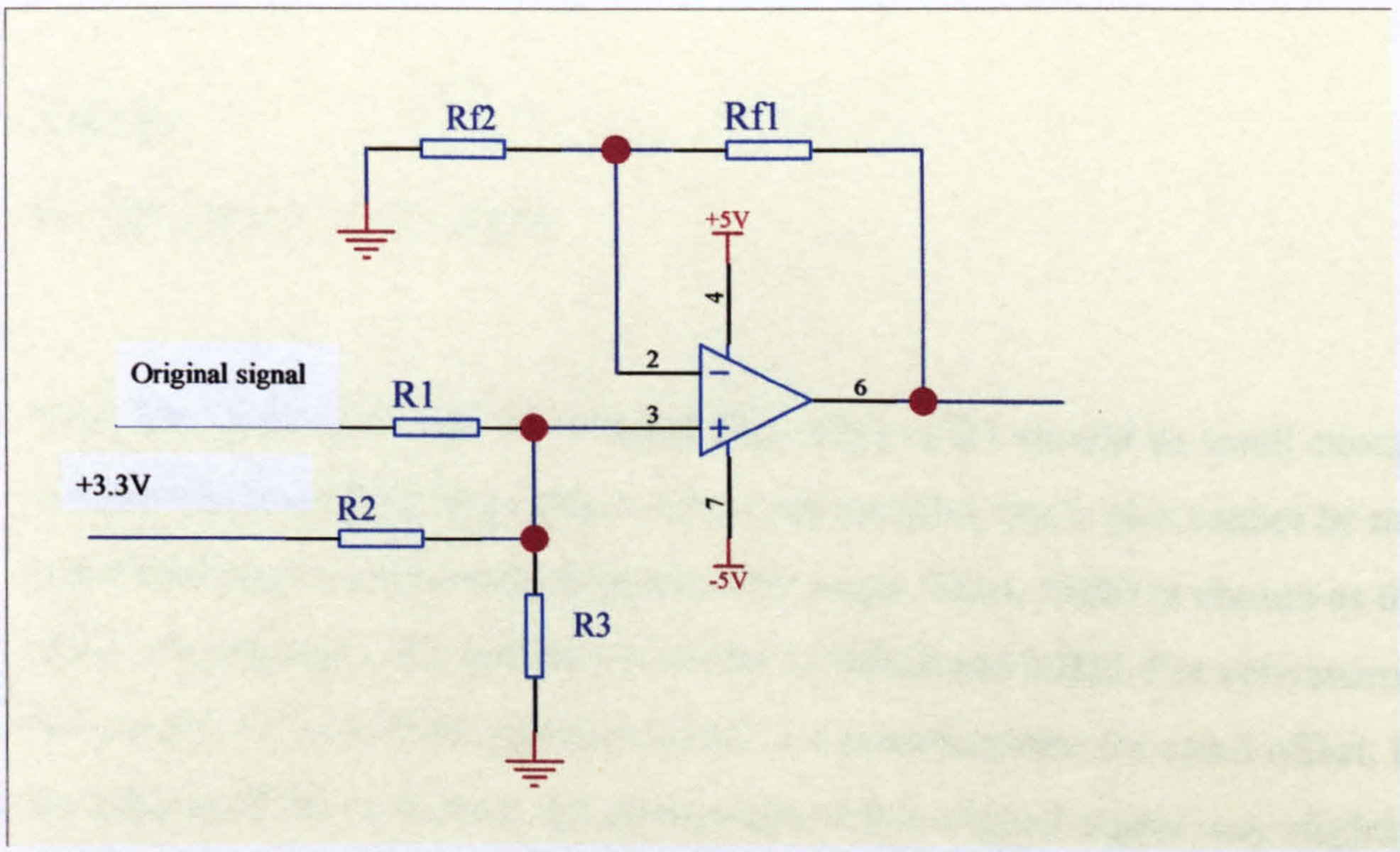


Fig. 4.33: Three-terms summing amplifier

In Fig.4.33, R3 is placed between the junction of R1, R2 and ground to attenuate the input signal, so that the Op Amp can be configured with a larger gain. Considering that the open-loop bandwidth of this amplifier is 200MHz and the close-loop bandwidth goes down when the closed-loop gain is rising. The gain here cannot exceed 5. Here set the gain to 4, which makes the close-loop bandwidth 50MHz.

Fig.4.33 can also be regarded as three-terms summing amplifier. The added items are the original signal, 3.3 volt and 0 volt. According to "Superposition Theorem" the output of this stage can be calculated by equation 4.4:

$$Vout = n \bullet (Voriginal \bullet \frac{R2 // R3}{R1 + (R2 // R3)} + 3.3 \bullet \frac{R1 // R3}{R2 + (R1 // R3)} + 0 \bullet \frac{R1 // R2}{R3 + (R1 // R2)})$$

(Equation 4.4)

Replacing "n" with "4" and "Vout" with "Voriginal +1", the following result is obtained:

$$\begin{cases} \dfrac{R2R3}{R1R2 + R1R3 + R2R3} = 1/4 \\ \dfrac{R1R3}{R1R2 + R1R3 + R2R3} \bullet 3.3 = 1/4 \end{cases}$$

It gives:

R1 : R2 : R3=1 : 3.30 : 0.371

Now, the value of R1 can be selected. The value of R1 should be small enough that oscillations caused by large phase delays are avoided, but it also cannot be too small and draws large current from first amplifier stage. Thus, 560Ω is chosen as the value of R1. Accordingly, R2 and R3 should be 1.848kΩ and 208Ω. For convenience, practically, R3 is a 220Ω register and R2 is a potentiometer for exact offset. Due to the change of the resistance, the attenuation of the original signal may slightly deviate from 1/4. Therefore, the gain of this amplifier cannot be exactly 4 and a potentiometer Rf2 is applied for exact adjustment.

In this summing amplifier, the gain of this operation amplifier is roughly 4, which equals 1+(Rf1:Rf2). To reduce the error due to base input current, the combination of the parallel resistance of Rf1, Rf2 should be equal to the parallel resistance of R1, R2 and R3, i.e. Rf1//Rf2=R1//R2//R3.

The above two conditions can give the equation 4.5 to resolve Rf1, Rf2:

$$\begin{cases} 1+\dfrac{Rf1}{Rf2}=4 \\ Rf1 // Rf2 = R1 // Rf2 // Rf3 \end{cases} \qquad \textbf{(Equation 4.5)}$$

Rf1= 480Ω and Rf2=160Ω approximately.

Thus, the second stage of an analogue channel is built as shown in Fig.4.34.

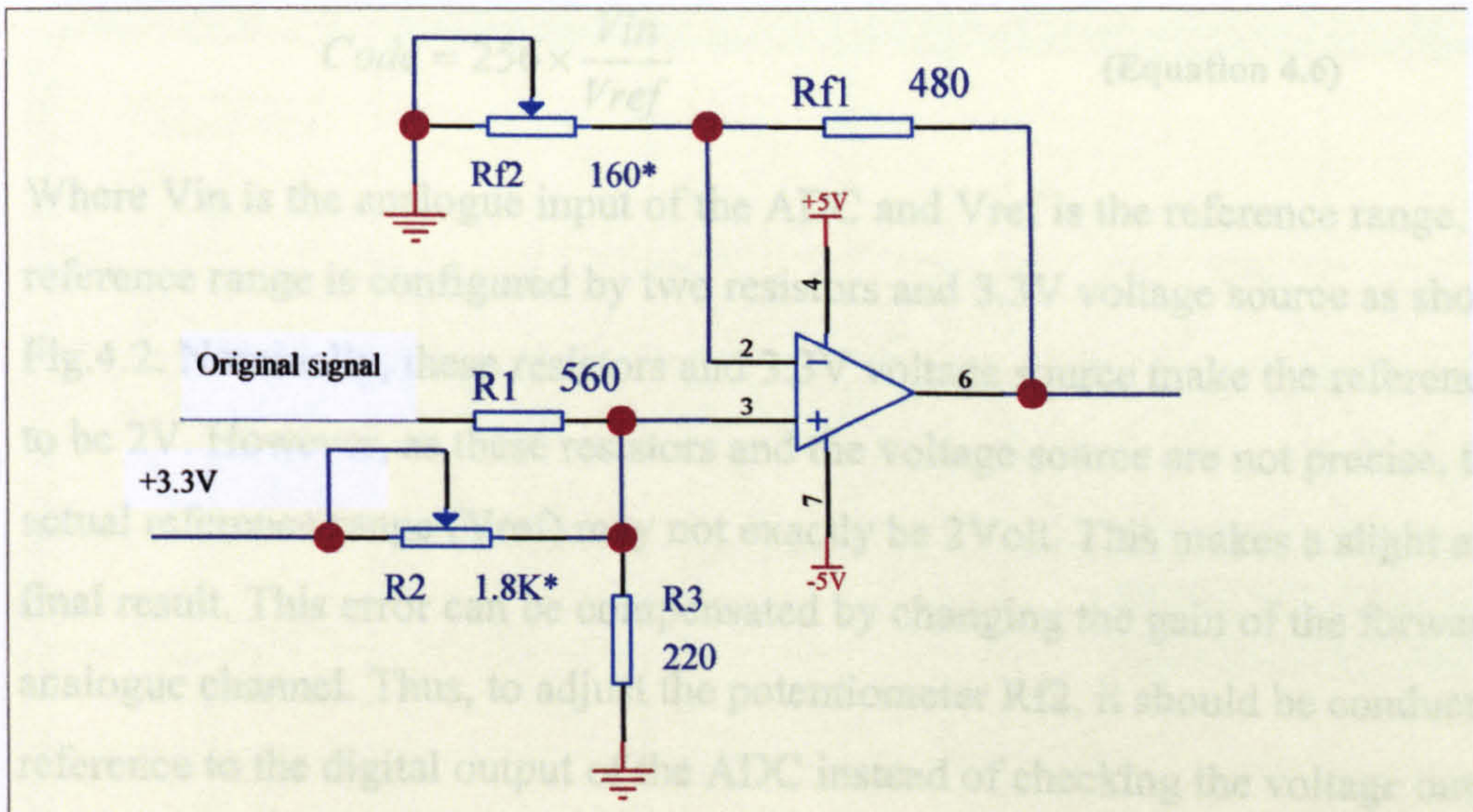


Fig. 4.34: Second stage of the analogue channel

4.1.7.2 Calibration of the analogue channel

There are two potentiometers in the analogue channel: R2 and Rf2. R2 is used to give an exact 1V offset to the original input signal and Rf2 is to adjust the gain (nominal 4). They are adjusted by the following steps:

(1) Adjustment of R2: Giving a –1V DC at the input port of the Acquisition Board, measuring the voltage at the junction of R1, R2 and R3 (or Pin 3 of U2), adjust R2 letting the voltage on this point to be zero, at which, the second stage gain has to effect.

(2) Adjustment of Rf2: Although R1, R2 and R3 are designed to give 1/4 attenuation to the original signal, the real resistors, for the precision reasons, cannot make the exactly 1/4 attenuation. Thus the gain, given by Rf1 and Rf2, should be accordingly different from 4. The adjustment can be done by giving 0 volt DC at the input of the Acquisition Board (short the input to ground), and turning the potentiometer Rf2, letting the output of the amplifier attain 1V.

Furthermore, practical calibration should consider the error of the input range of the A/D converter. For the ADC08100, the input signal of the ADC will be converted to digital code according to Equation (4.6).

$$Code = 256 \times \frac{Vin}{Vref} \qquad \textbf{(Equation 4.6)}$$

Where Vin is the analogue input of the ADC and Vref is the reference range. The reference range is configured by two resistors and 3.3V voltage source as shown in Fig.4.2. Nominally, these resistors and 3.3V voltage source make the reference range to be 2V. However, as these resistors and the voltage source are not precise, the actual reference range (Vref) may not exactly be 2Volt. This makes a slight error in final result. This error can be compensated by changing the gain of the forward analogue channel. Thus, to adjust the potentiometer Rf2, it should be conducted with reference to the digital output of the ADC instead of checking the voltage output of the second amplifier, i.e. giving 0V input and turning the potentiometer of Rf2 to give an ADC output of "10000000" in binary.

The ADC's output has been exported to drive 8 LEDs. Thus, the calibration can be done by simply watching the LEDs and turning the potentiometer.

Table 4.4 shows the real test records after calibration. The test result shows that the analogue channel and the ADC have accurate precision and linear characteristic within the input range between –1V to +1V.

Table 4.4: Digital outputs and their corresponding analogue inputs

Analogue Input (Volt)	-1.00	-0.80	-0.60	-0.40	-0.20	0.00	0.20	0.40	0.60	0.80	1.00
Digital Output (Hex)	0H	1AH	33H	4DH	66H	80H	9AH	0B3H	0CDH	0E6h	0FFH

Fig.4.35 records the analogue channel's response to a 1MHz sine wave. Channel 2 (upper waveform) is the output of the analogue channel and channel 1 is the input signal of the analogue channel. It shows that the analogue channel gives 1V offset and "1" gain to the original signal.

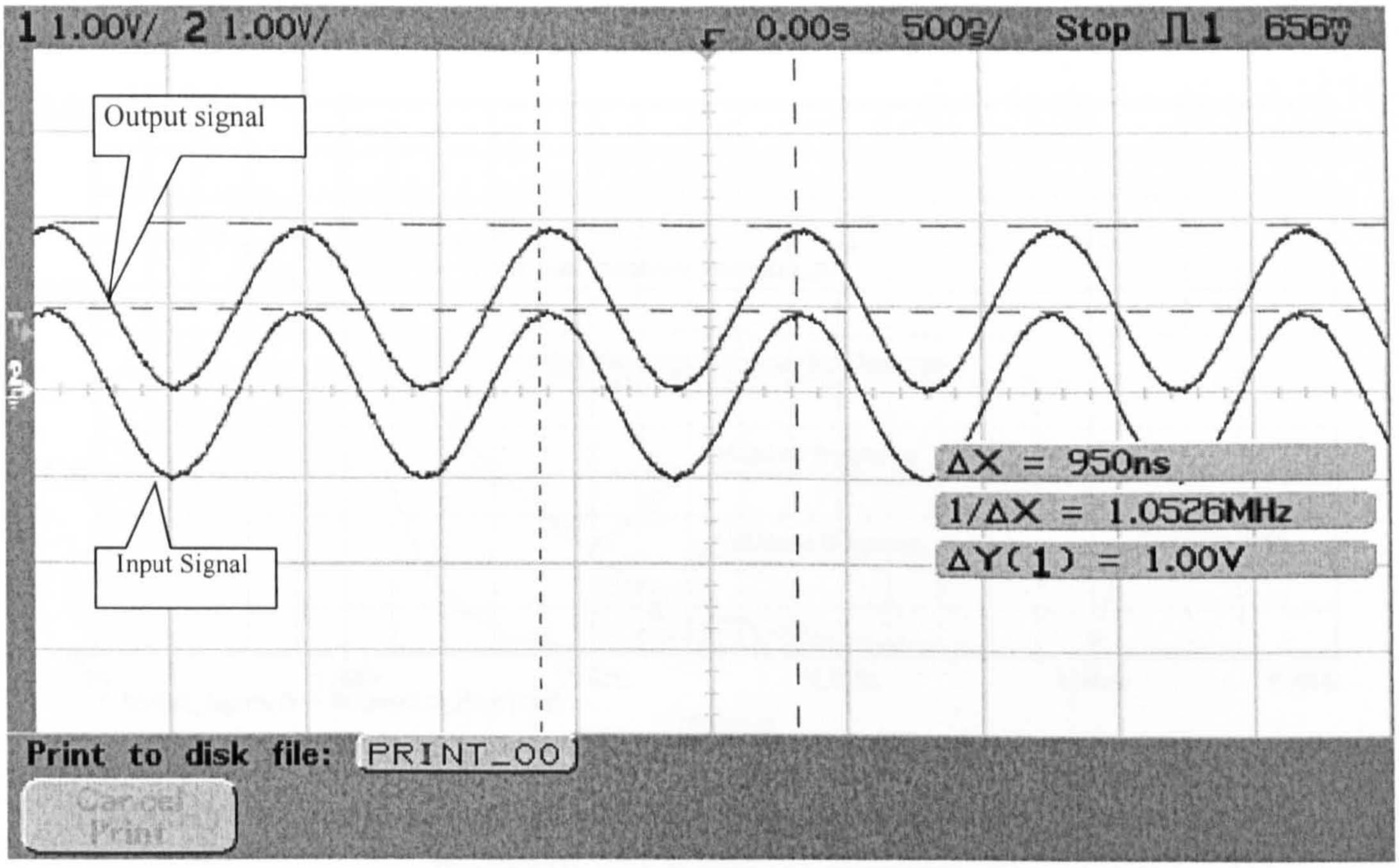


Fig. 4.35: Input and output waveforms of the analogue channel (1MHz sine wave)

4.1.7.3 Bandwidth limitation of the analogue channel

For any sampling measurement equipment, the alias problem must be considered. In a sampling system, if the measured signal has frequency components higher than half the sampling frequency, the higher frequency signal components will fold back to appear as a lower frequency content. In measurement systems, this phenomenon is called "aliasing" or "frequency aliasing". The method to remove "aliasing" for the measurement system is called "anti-aliasing". The common "anti-aliasing" method is filtering the higher frequency at the input port of the sampling system. DSOs always have such filters.

For a digital oscilloscope to measure a signal accurately, the signal must not have significant frequency content above the Nyquist frequency, which is half the sampling frequency. Any frequency above the Nyquist frequency folds back into the frequency-domain region below the Nyquist frequency [50].

An example of anti-aliasing is illustrated for a 1GHz bandwidth, 4GSPS DSO's analogue channel, as shown in Fig.4.36.

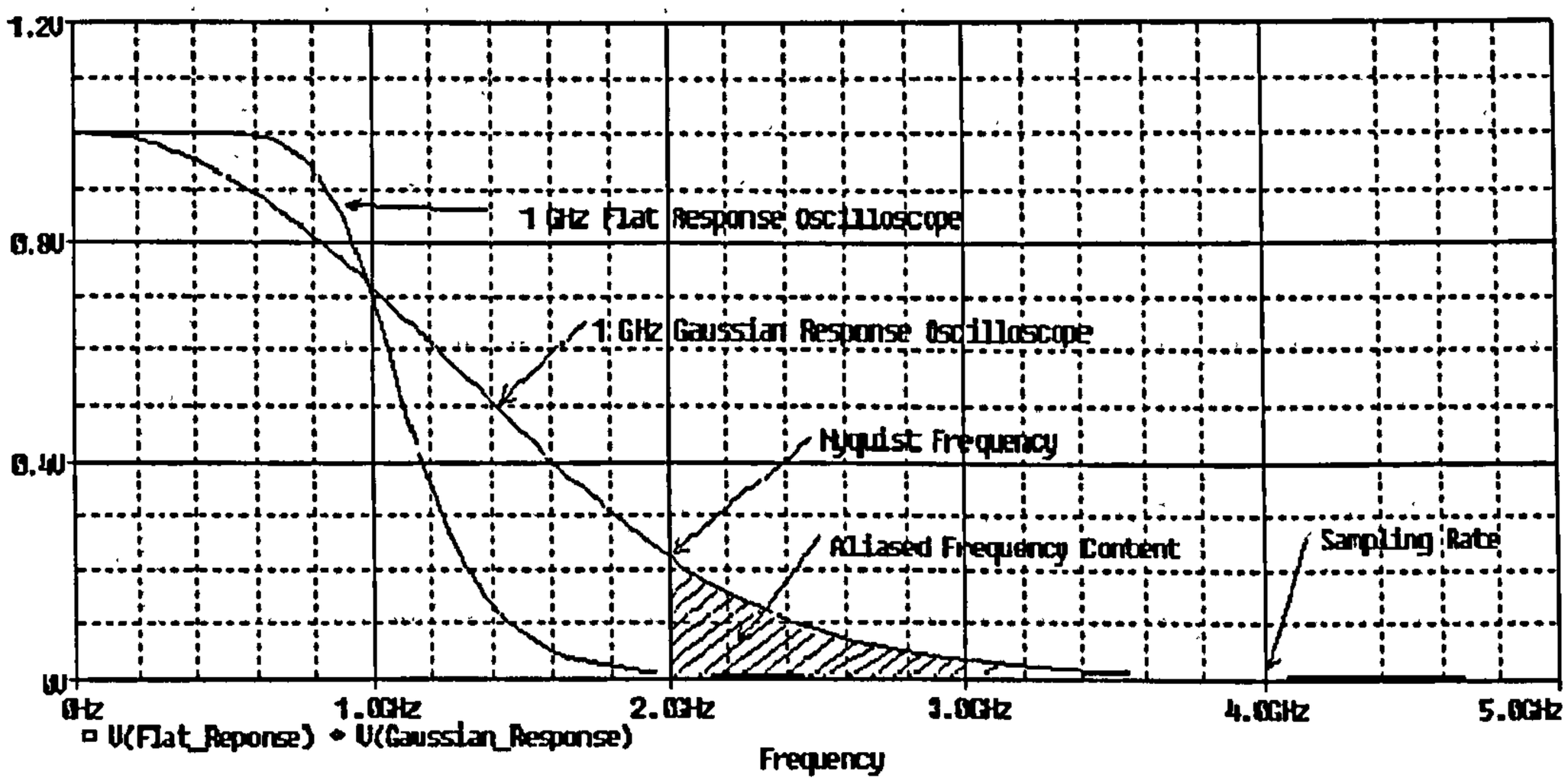


Fig. 4.36: Two kind of frequency responses of the analogue channel of DSO with 1GHz Bandwidth and 4GSPS sampling rate

It can be seen that oscilloscopes filter the signal components higher than the Nyquist frequency.

In the EMI measurement project, most sensors have filters to cut-off the high frequency content for anti-aliasing. However, as a general sampling equipment, the RAU should also have the anti-alias filter. The RAU has 20MHz bandwidth and 80MHz sampling rate. Therefore, the analogue channel should have 20MHz bandwidth and attenuate the frequency contents above 40MHz (Nyquist frequency). This can be simply done by adding a capacitor to build an RC filter in the analogue channel as shown in Fig.4.37.

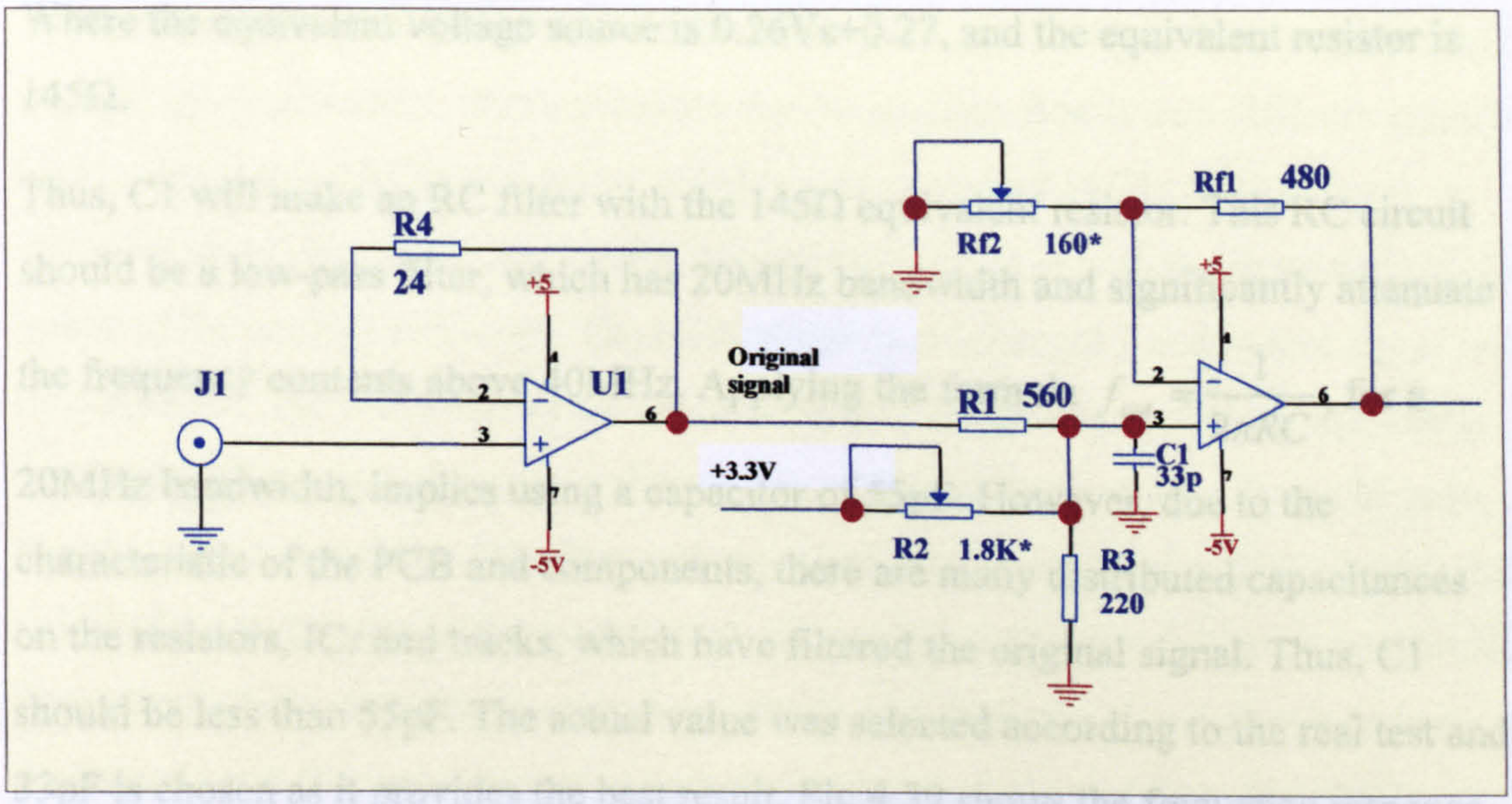


Fig. 4.37: Final design of the analogue channel

In Fig.4.37, C1 is added to form a RC filter with forward resistors network(R1, R2 and R3). According to Thevenin's theorem, for C1, its forward network is a two terminals network, which can be simplified with a voltage source and a series resistor as shown in Fig.4.38.

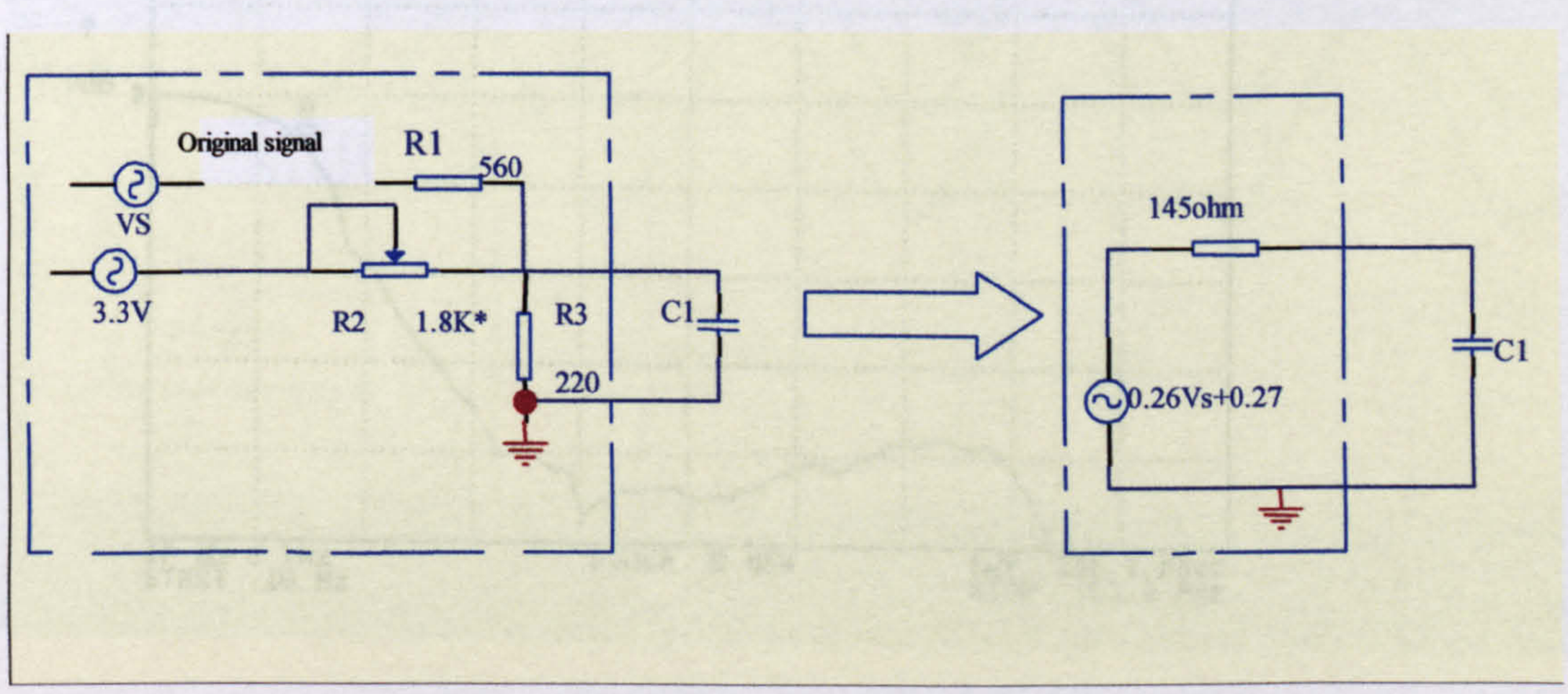


Fig. 4.38: Resistors network before C1 and its equivalent circuit

Where the equivalent voltage source is 0.26Vs+0.27, and the equivalent resistor is 145Ω.

Thus, C1 will make an RC filter with the 145Ω equivalent resistor. This RC circuit should be a low-pass filter, which has 20MHz bandwidth and significantly attenuate the frequency contents above 40MHz. Applying the formula $f_{cut} = \frac{1}{2\pi RC}$, for a 20MHz bandwidth, implies using a capacitor of 55pF. However, due to the characteristic of the PCB and components, there are many distributed capacitances on the resistors, ICs and tracks, which have filtered the original signal. Thus, C1 should be less than 55pF. The actual value was selected according to the real test and 33pF is chosen as it provides the best result. Fig.4.39 shows the frequency response of this analogue channel. This chart is made by an HP network analyzer. It can be seen that the analogue channel has 20MHz bandwidth and the frequency contents above 40MHz have been significantly attenuated.

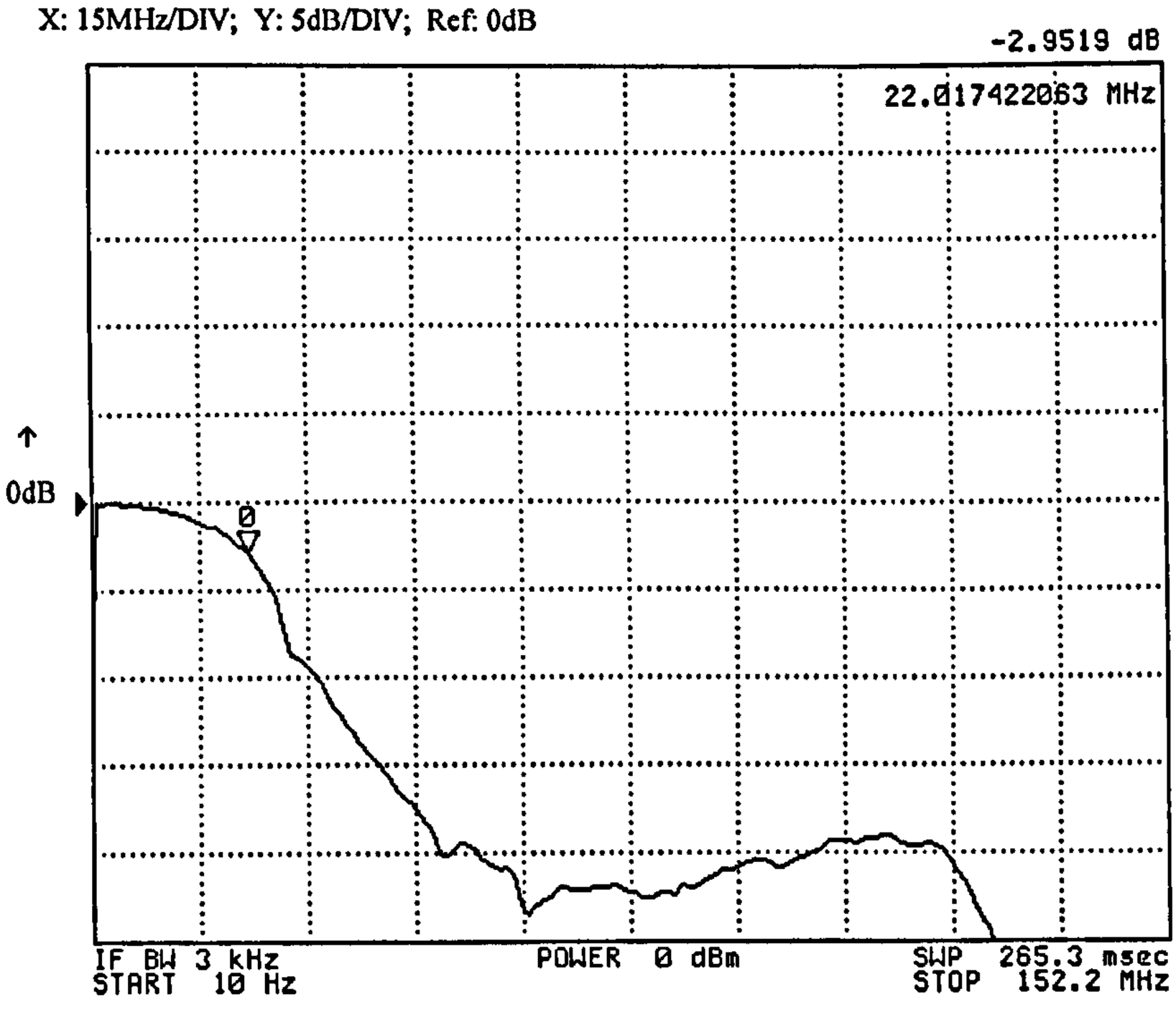


Fig. 4.39: Frequency response of the analogue channel

Fig.4.40 to Fig.4.43 show the test results of the analogue channel. This test was done using a signal generator, which provides the Acquisition Board with different signals (1kHz sine wave, 1MHz sine wave, 20MHz sine wave and 1MHz square wave). A 100MHz bandwidth DSO was used to measure the signal at both the input and output points of the analogue channel. The input signal is on channel 1 and output signal is on channel 2. The result shows the characteristic of the analogue channel accurately correspond to the gain-frequency chart in Fig. 4.39 and design target. It can be seen that the output signal has 1V offset and represents the input signal and along with the rising of the frequency of the input signal, the analogue channel shows the bandwidth limitation, which attenuate the signal amplitude and delay the signal phase. In low frequency band the output signal has no attenuation and phase delay. At 20MHz frequency, the amplitude of the output signal is attenuated to 70% of the original signal and its phase was delayed in 45°. For a square wave, the analogue change make 15ns rising time delay and 15ns falling time delay.

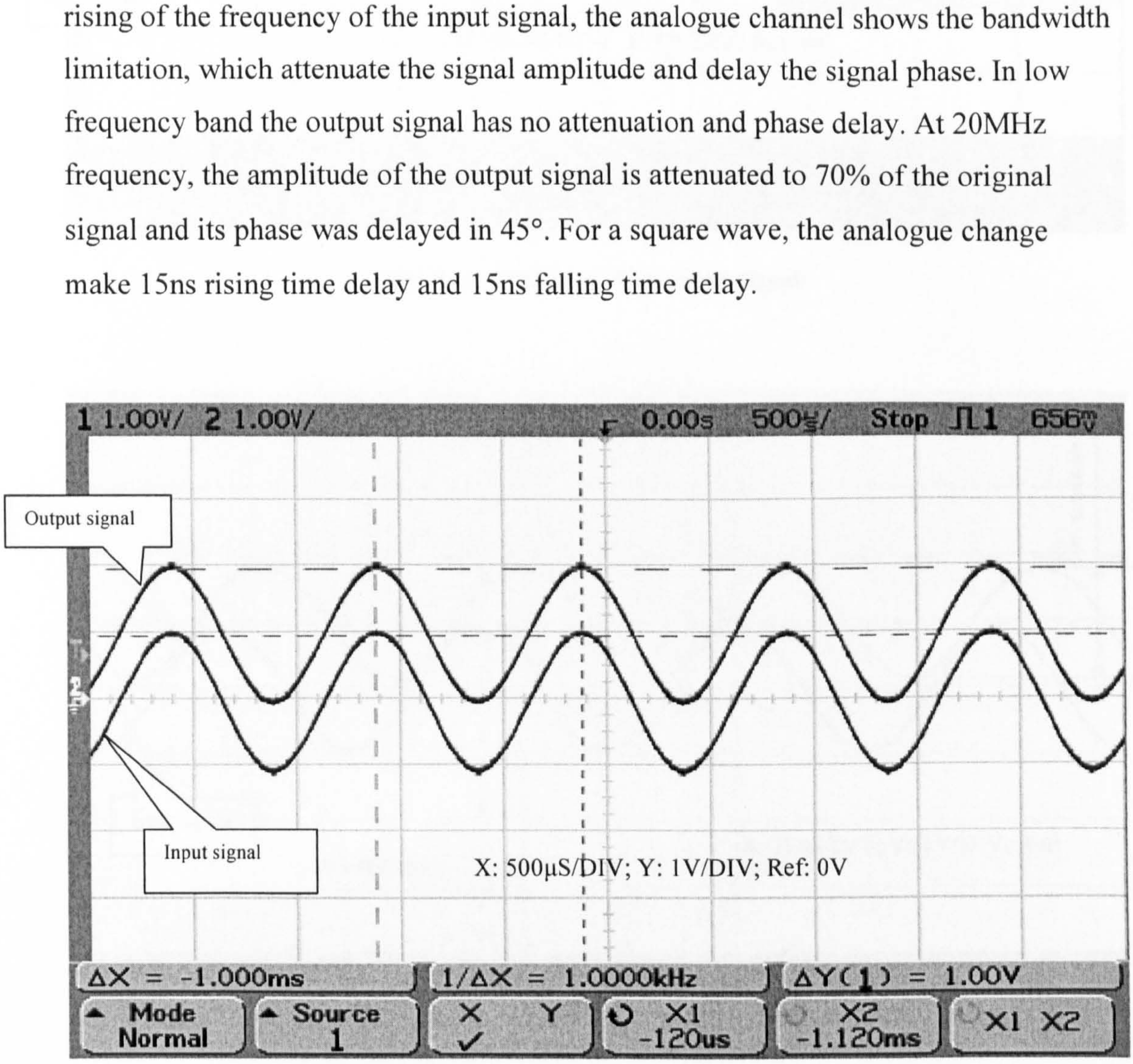


Fig. 4.40: 1kHz sine wave input signal

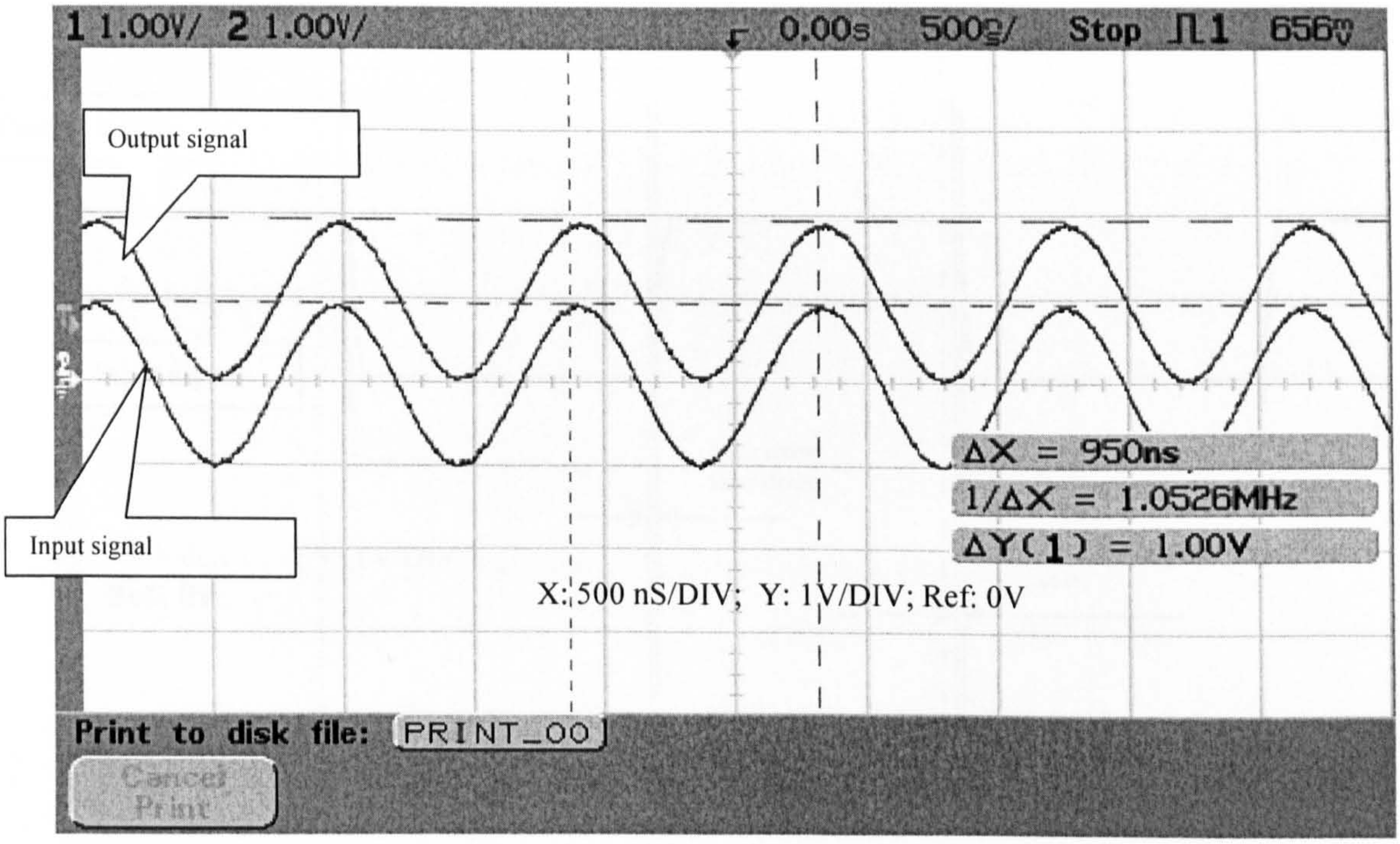


Fig. 4.41: 1MHz sine wave input signal

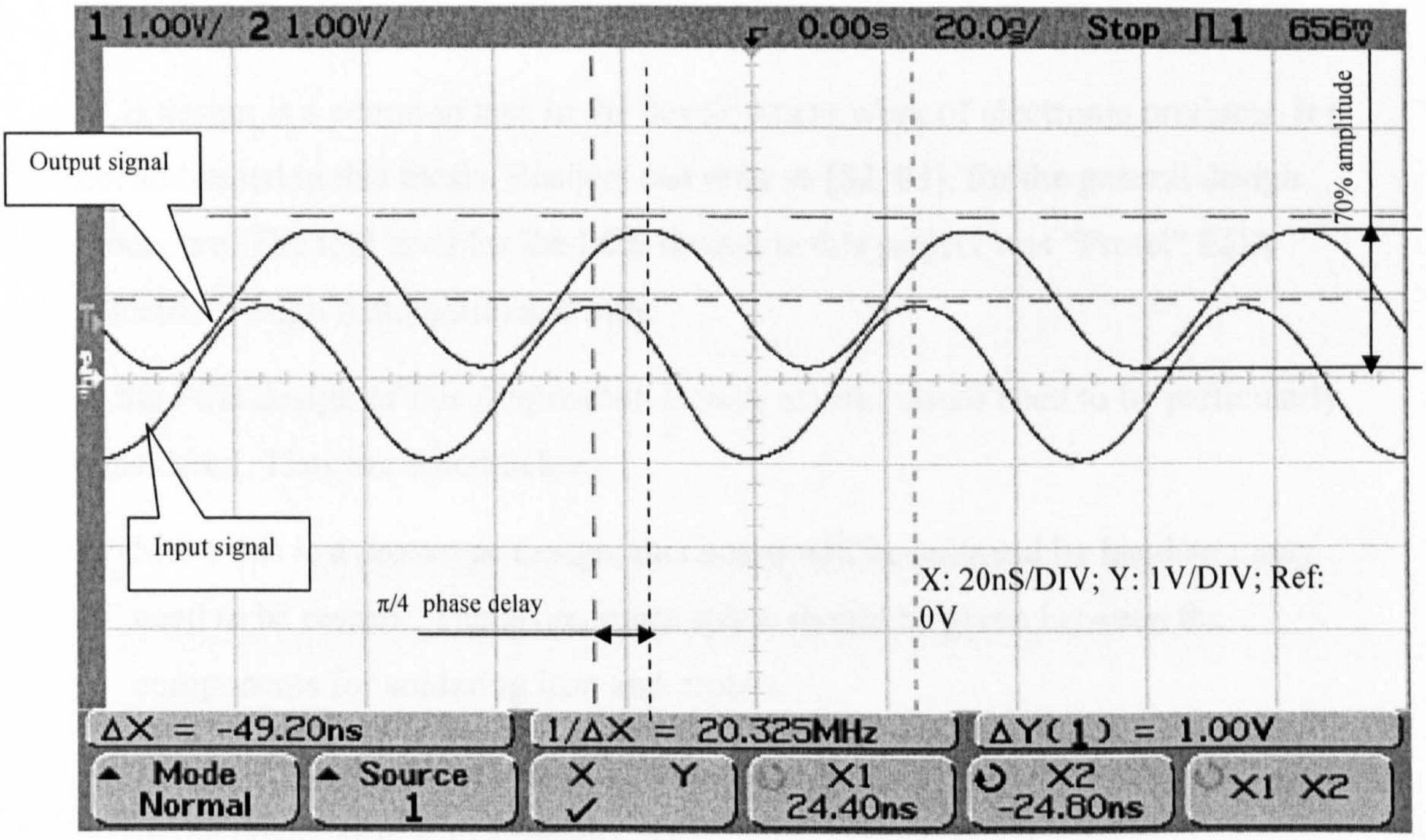


Fig. 4.42: 20MHz sine wave input signal

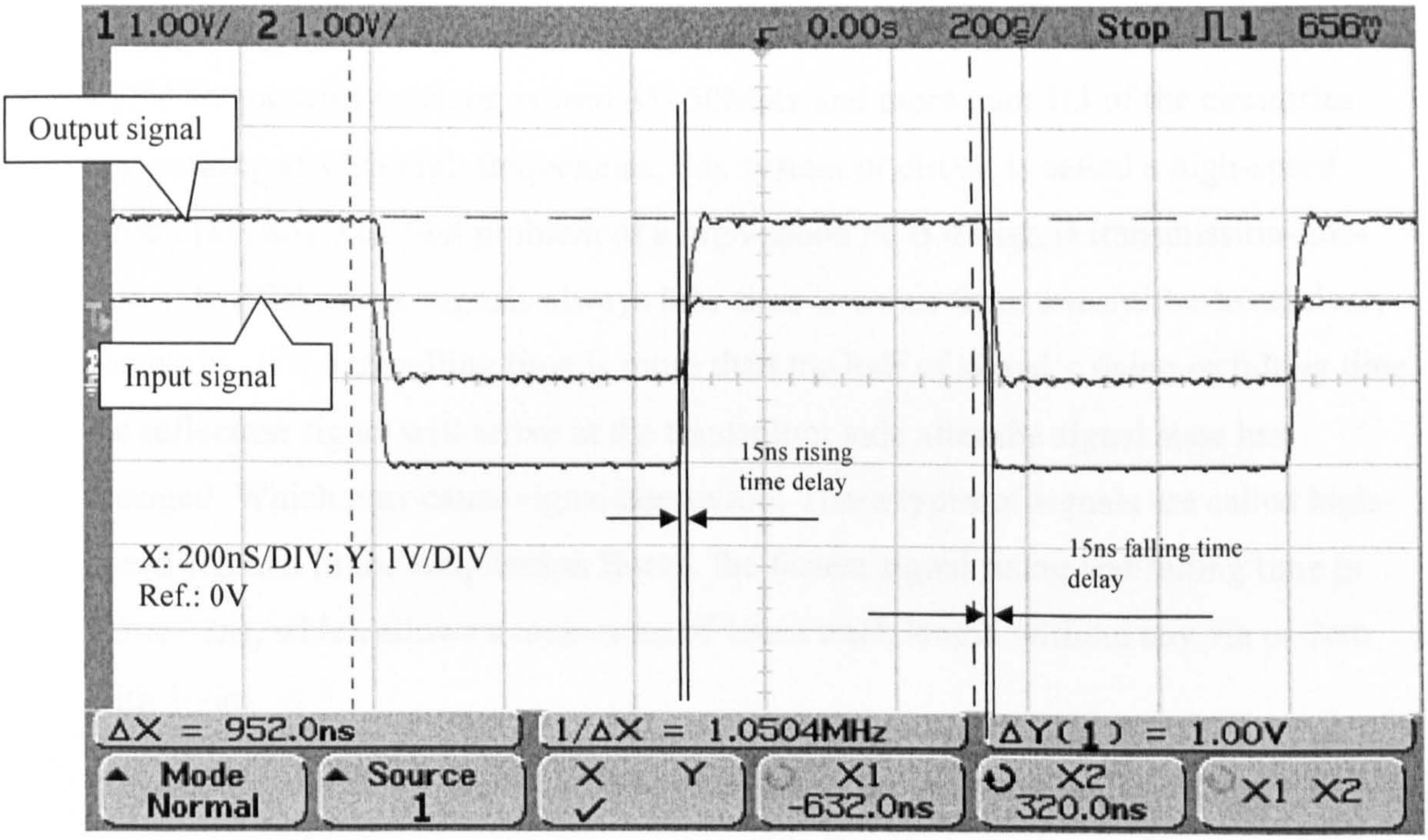


Fig. 4.43: 1MHz square wave input signal

4.1.8 PCB considerations

PCB design is a common task in the development work of electronic products. It is not addressed in this thesis. Readers can refer to [82, 83], for the general design procedure. The tool used for the PCB design in this project was "Protel" EDA (Electric Design Automatic) software.

In the PCB design of this Acquisition Board, several issues need to be particularly considered. They are listed below:

1) Since this is a prototype design, this board will be soldered by hand and may need to be rework. Therefore, more space should be given between the components for soldering iron and probes.

2) For possible unforeseen modification, a via (through hole) array has been placed in the board. (Refer to appendix B)

3) As it is a high-speed circuit, the integrity of signals and EMI should be considered as detailed below:

A well accepted definition of a high-speed circuit is that, for a digital system, the signal frequencies reach or exceed 45~50MHz and more than 1/3 of the circuitries are working at such high frequencies, this system or circuit is called a high-speed circuit [84, 85]. The first problem of a high-speed PCB design is transmission-line-effect. In PCB traces, signals always take time to travel from transmitter to receiver. Generally, if the travelling time is more than the half of signal's rising or falling time, the reflection signal will arrive at the transmitter side after the signal state has changed. Which may cause signal aberration. These types of signals are called high-speed signals. In the Acquisition Board, the fastest signal rising and falling time is 1.5ns~ 2ns, which allows a maximum of 10cm track length without any via or 7cm with 1 via.

Fortunately, due to the small size and few vias of the Acquisition Board, there aren't any tracks with a long length. The modern CPLD technique allows designers the ability to reduce the PCB size. Therefore, reflection problems are not critical in this PCB. However, other problems of high-speed circuits may still exist, such as "ring"(or Overshoot/Undershoot), "Ground Bounce", "Signal Coupling" (or Cross Talk), "EMI" etc requiring careful PCB design.

Obeying the general PCB design rules always helps the integrity of signals and the EMC environment. These general rules are listed below and have been implemented in the Acquisition Board.

1) Marximise the ground plan.
2) Using thicker tracks to carrying large currents.
3) Using low frequency decoupling capacitors at the power entry site and high frequency decoupling capacitors at power pins of the components. Always locate them close to the power and ground plane.
4) Separate the analogue circuit and digital circuits in two parts and split ground plane into analogue piece and digital piece.
5) Minimize the length of tracks.
6) Try to reduce vias.
7) Avoid right-angle tracks.

8) Optimise component layout and physical connection topology.

Furthermore there are some special rules for high speed PCB design. As Xilinx suggested for the PCB design with their product XC9500xl family, a "check list" has been made for the signal integrity and EMI [67]. The items and their implementations are in the table 4.7:

Table 4.5: Check list for the high speed PCB design

Problems	Solutions and Implementations
Overshoot/Undershoot	Insert series resistors in the lines between CPLD and AT89c52
Ground Bounce	Dedicated and integrated Ground Plane
Reflection	Not critical
Cross Talk	Enlarge the spaces of the parallel traces once they leave the components for a distance
EMI	Not critical. Closed ground loop and dedicated ground plane.

Fig.4.44 and Fig.4.45 show the unpopulated and assembled Acquisition Board respectively.

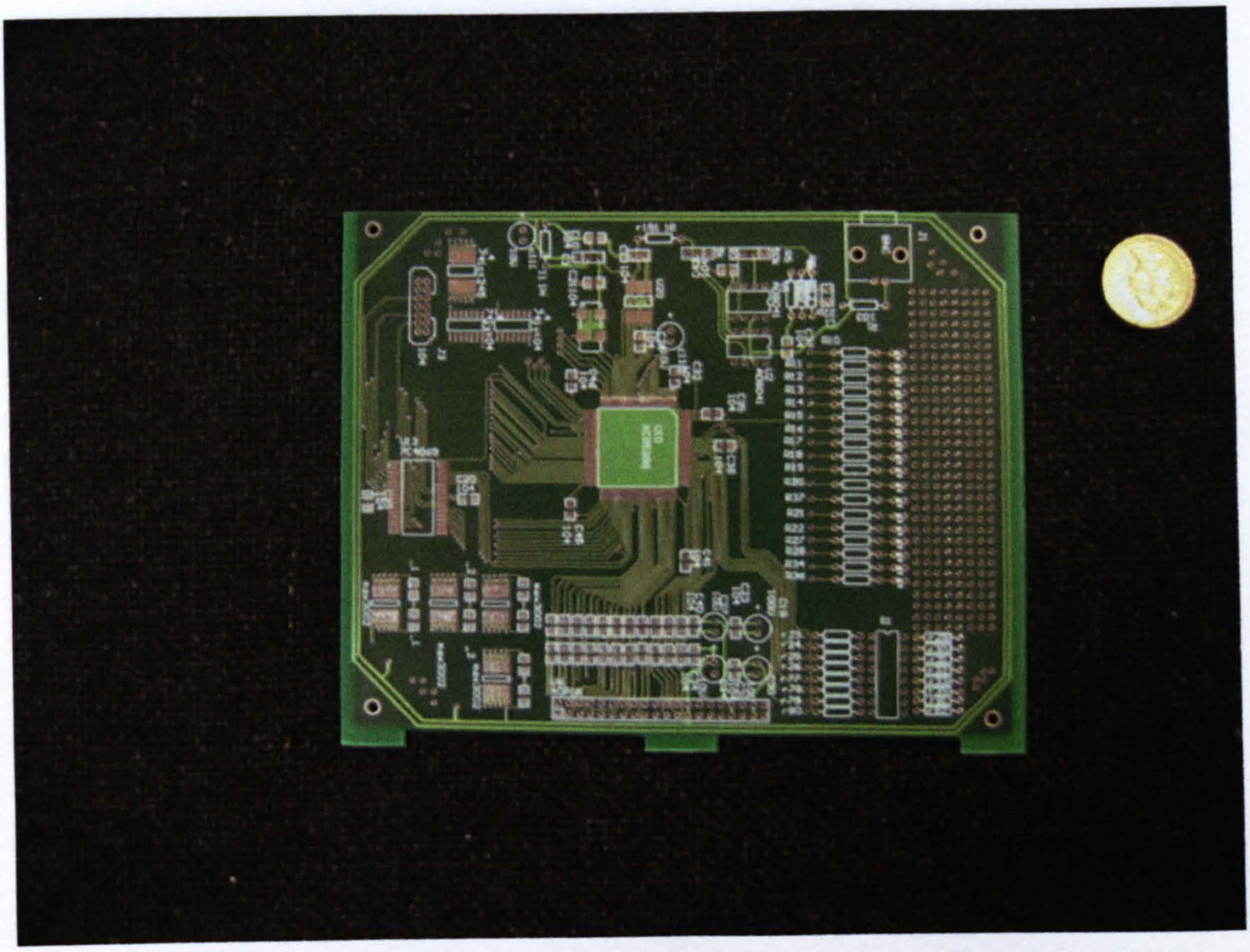


Fig. 4.44: Unpopulated Acquisition Board

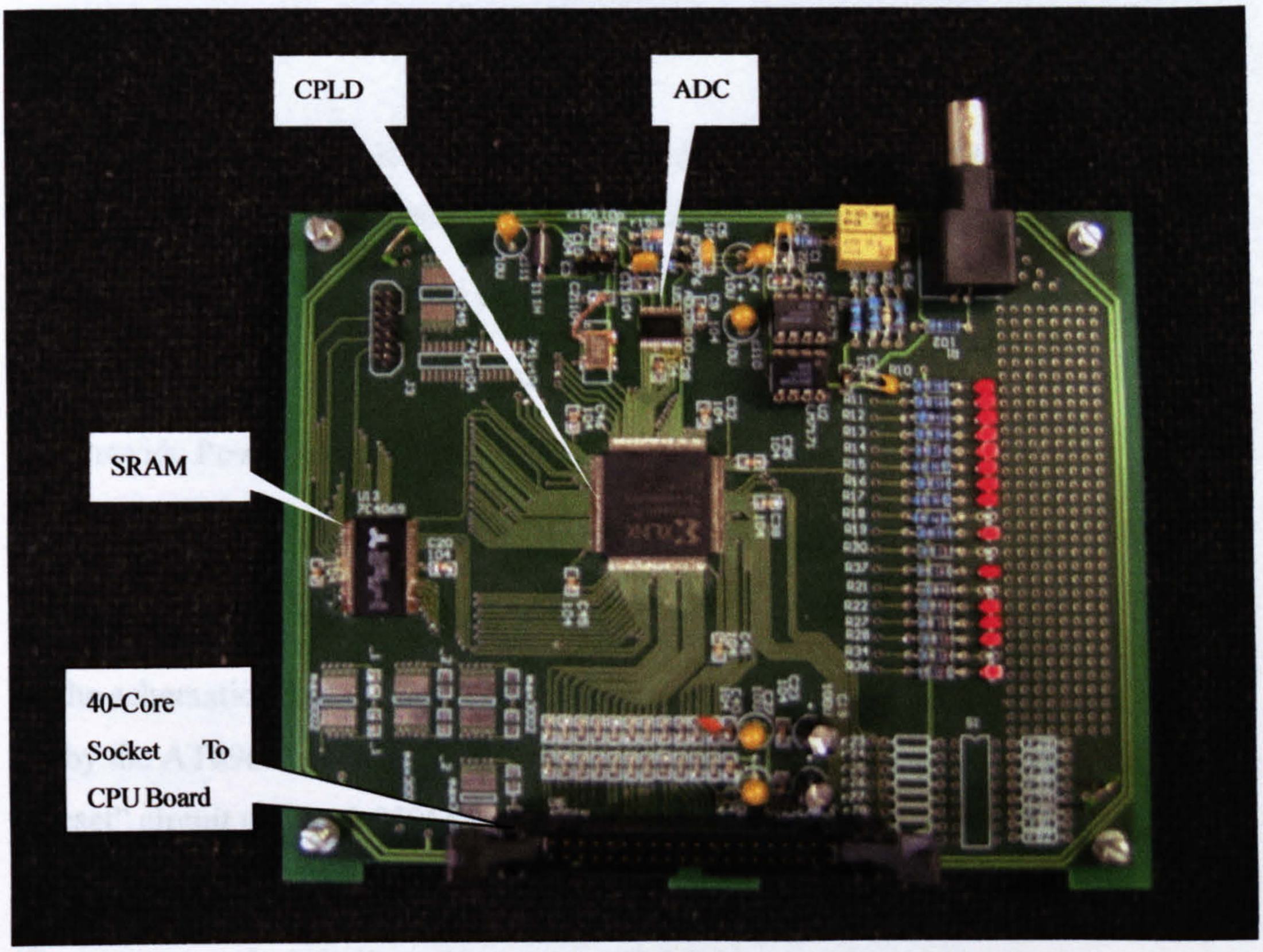


Fig. 4.45: Populated Acquisition Board

4.2 CPU Board

The CPU board consists of the MCU (AT89c52) system, power supply and communication ports. As introduced before, it accomplishes 3 functions.

1) Exchange data with remote PC through wireless network;
2) Implement PC's commands and control the Acquisition Board;
3) Provide Power supply to the RAU.

The design of this system includes hardware design and software design

4.2.1 Hardware design of the CPU Board

In the schematic sheet of the CPU board (Appendix C), the AT89c52 system is built-up by the AT89c52 (U1), a 64kB memory 62256 (U4), address latch 74LS373 (U3), "Reset" circuit and a 11.059MHz crystal. It is a typical application for MCS-51 family micro-controller, for detailed explanation please refer to related books [69].

The power supply is built-up by 4 chips of LM371- the adjustable voltage regulator (U5, U6, U7, U8). Among them, U7, U5 are connected in series, U7 converts 12V to 8V and output 8V DC to U5, U5 converts 8V to 5V. U8, U6 are connected in series, U8 converts 12V DC to 7.5 V and provides 7.5V DC to U6, U6 converts 7.5V DC to 3.3V. (Refer to appendix C and appendix D). Such a series configuration is designed to improve the conversion efficiency, as the optimized input-output voltage difference for LM371 is 3.0V~4.5V.

7.5 V is also provided to Bluetooth Modem. In the schematic sheet, MAX889 (U11) had been designed to generate –5V DC. Due to the high temperature of that component, it was replaced by an inverted voltage converter ADM660 [86]. (Refer to Appendix G)

J7 is the 40-pin socket used to house the 40-core flat cable connecting the CPU Board and Acquisition Board. J1 is a 16-pin power socket used to input several power supplies outside of the board. J8 is the input port of the external trigger source (Not in use). J9 is the 12V power source input pin.

When the CPU Board was designed, the wireless modem was not chosen yet. Therefore, in the circuit design, several modems' interfaces are reserved: RS-232, RS-422 and TTL. In the schematic sheet, Sockets J2, J3, J4 are respectively used for RS-232 Port, RS-422 Port and a dedicated connector to Nortic's wireless transceiver-nRF403 [87, 88]. The AT89c52 uses RXD (Receive Data) and TXD (Transmit Data) pins to exchange data with the above serial ports. These two pins are linked to the RS-232 socket through MAX232 (RS-232 line driver and receiver) [89]; to RS-422 socket through MC3486 (RS-422 line receiver) [90] and MC3487 (RS-422 line driver) [91];to the Nortic Wireless Modem Socket through MAX3391 (3.3V/5V Level Translator, as this Nortic product can only accept 3.3V signals) [92]. In the final circuit, since the final selected wireless modem has a RS-232 port, the other two links have been removed in the PCB assembling (Refer to Appendix G: "Technique Specification": "Assembling and Soldering notices"). Also, the wireless modem applies hardware flow control by using RTS (Request To Send) and CTS (Clear To Send) as "handshake" signals. Thus the AT89c52 uses two I/O pins P16 and P17 for the RTS and CTS signal. In serial data communication, on the receiver side, when the data receiving buffer is about full (75% generally), it sets RTS to "high" to inform the opposite transmitter to stop sending. After the data have been taken away from the buffer by the processor and the buffer is almost empty (25% generally), the receiver restores the RTS to "low". Every time, the transmitter wants to send data, it always checks CTS, which is linked to the RTS of the receiver, and sends data when CTS is low. For details of the "Flow Control" in RS-232 communication, refer to [93]

Thus, the AT89c52 uses P16 and P17 for these "Flow control" signals. P16's output signal through MAX232 becomes RTS. CTS signal though MAX232 goes to P17.

4.2.2 Software of AT89c52

4.2.2.1 Functions of the software in AT89c52:

1) Receive the commands from PC (Receive data from UART)
2) Interact with Acquisition Board according to the commands
3) Send required data to PC

4.2.2.2 Brief introduction on the format of Communication Data Packets

This content will be detailed in the next chapter, "data communication network". To help in understanding the software, here, the format of the Communication Data Packet is given in advance:

1) Data Packet from PC to RAU (16 Bytes):

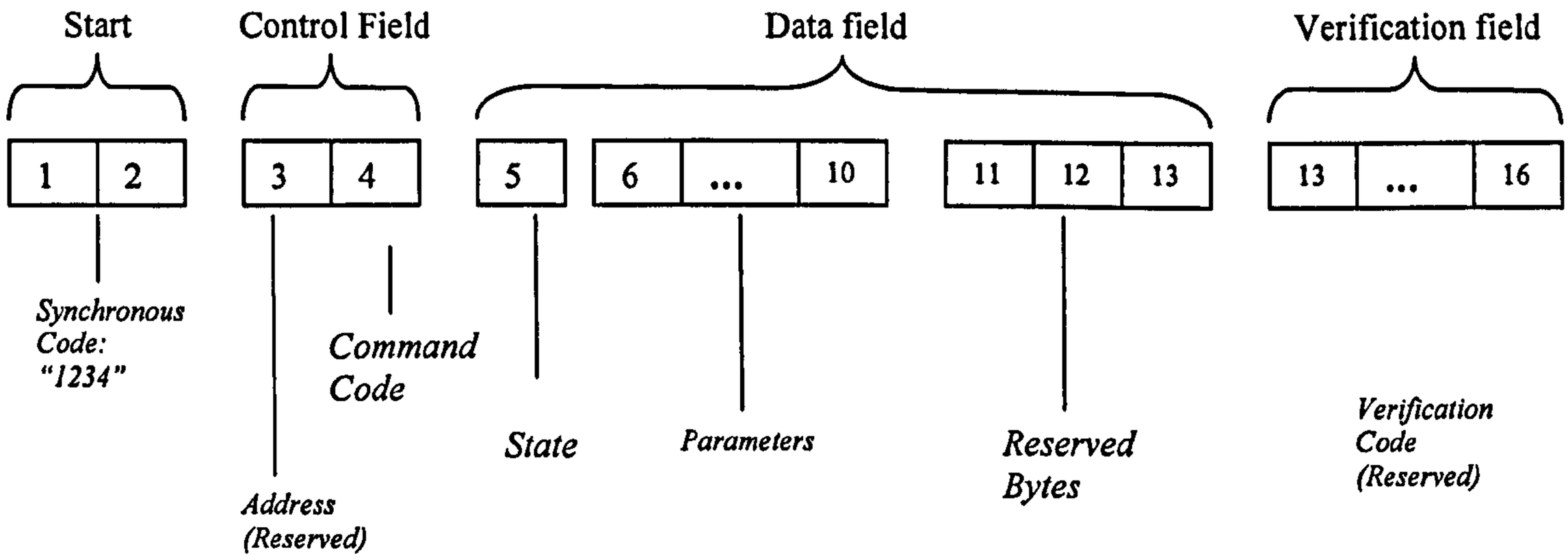


Fig. 4.46: Data Packet from PC to RAU

Every time the PC sends a command to the RAU, it sends a packet as above in Fig.4.46. This packet starts with 2 byte of synchronous code "1234". Address and Command Code take the following two bytes (Control Field). Following Control field, data field has 9 bytes, including 1 byte of "State" 5 bytes of "Parameters" and 3 bytes reserved for future use. Parameters include "Trigger-Level", "Trigger-Delay" etc. At the end of the packet, 4bytes verification codes are reserved.

After receiving a data packet, the RAU will execute different actions according to different "Command Codes" as listed in Table 4.6

Table 4.6: Explanation of "Command Code"

Command Code	Actions to be done
0DH	Set-up parameters to Acquisition Board
0EH	Reset Acquisition Board
00H	Read "Real- Data"
04H	Read Parameters
08H	Download Captured Data (Stored in SRAM)

To implement the command of "Set-up" and "Reset", the AT89c52 need not send any data back to PC. For the other three commands, the AT89c52 needs to send the required data to PC. The data format from RAU to PC is illustrated in Fig.4.47:

2) Data Packet from RAU to PC:

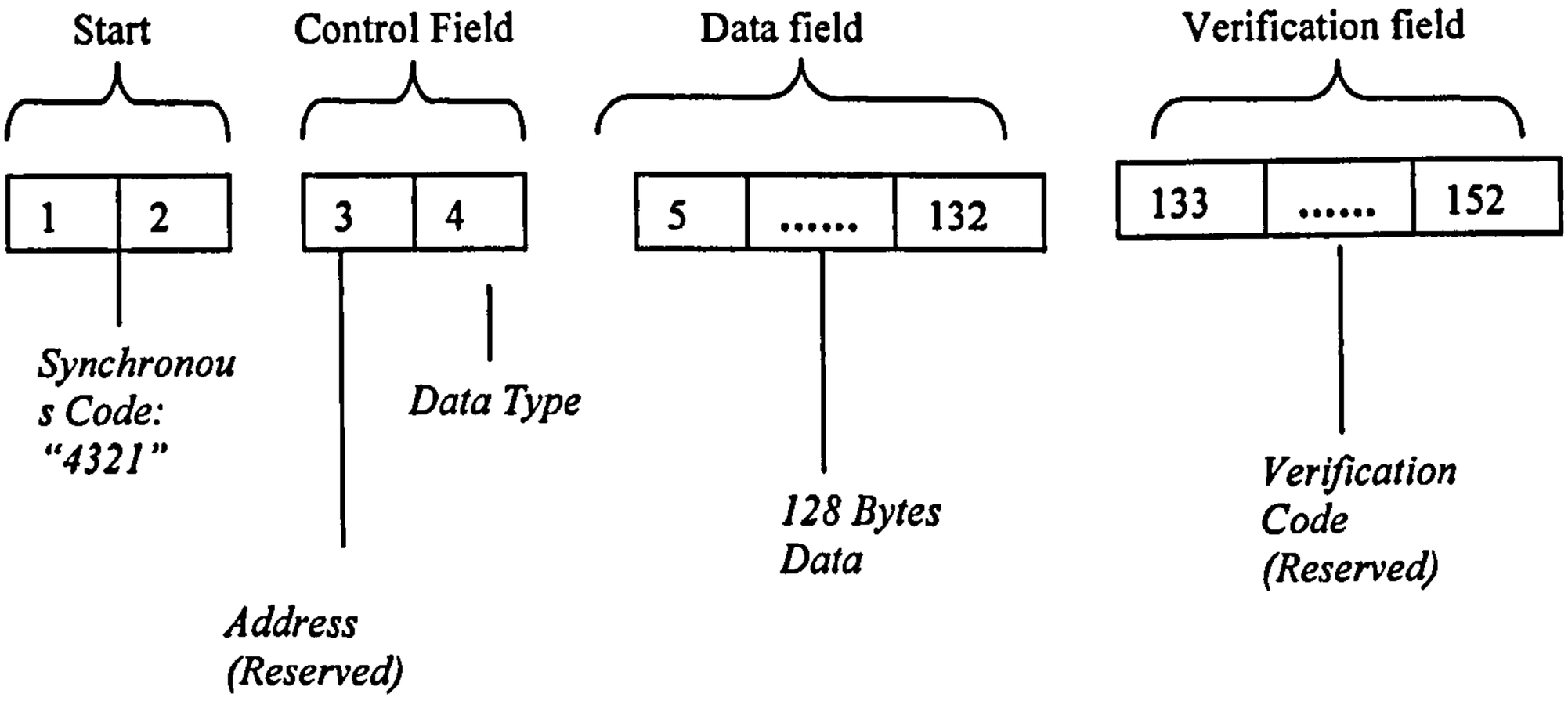


Fig. 4.47: Data Packet from RAU to PC

The data packet sent to the PC starts with "4321" and contains 128 byte data. Depending on what kind of data the PC requested, the data is obtained from different places: If the PC is reading "Real Data" the data comes from the "Real Data

Register". If the PC is downloading the captured 512k data, the data come from SRAM. If PC is reading parameters, the data come from "parameters registers". Once PC requests such a data set, the data packet will be sent to the PC continuously until it sends another command to stop it.

4.2.2.3 The resource distribution of the AT89c52 system

In this design, AT89c52 has 16 I/O lines (P10 to P17 and P30 to P37), 128 Bytes internal memory, 16-bit external address, which can map 64kB external memory or I/O port. These resources are distributed Table 4.7:

Table 4.7: "Resources allocation of the AT89c52"

I/O or Memory	*Usage*
P13 (Out)	*"Reset Acquisition" Pulse*
P15 (Out)	*"Refresh" Pulse*
P16 (Out)	*RTS*
P17 (In)	*CTS*
P30 (In)	*Triggered*
P32 (Out)	*Power Indicator*
25H~32H (Internal Memory)	*Receiving Data Buffer Area*
34H~45H (Internal Memory)	*Verification Data Area (Reserved)*
7100H~71FFH (External Memory)	*Sending Data Buffer Area*
8000H~8007H (External I/O, Write-Only))	*Write-able registers in CPLD, as listed in Table 4.2*
8000H (External I/O, Read-Only)	*Read-able port for "Captured Data" (In SRAM on Acquisition Board)*
800FH (External I/O, Read-Only)	*Read-able port for "Real-Data"*

4.2.2.4 Flowchart of the software of AT89c52 and its explanation

The AT89c52 receives serial data from the modem by interrupt mode. The diagrams in Fig.4.48 and Fig.4.49 show the main routine flowchart and interrupt service flowchart. Every time the AT89c52 receives a byte in UART (Serial Port), it enters the interrupt routine. When AT89c52 finds the two bytes of synchronous code ("12H", "34"H), it will store the following 14 bytes of data into the "Received Data Buffer" and inform the main routine by asserting the "New Message" mark. Then, it searches for the next synchronous code.

In the main routine, at the beginning of every nest, the main program checks "The new Message" mark. If a new packet is received, the program will check the packet and implement the command contained in the data packet. The commands the PC send are "Set-up Parameters", "Reset Acquisition", "Read Parameters", "Read Real-Data", and "Download the captured data in SRAM". Among them, "Set-up" and "Reset" commands are expected to be implemented only once. The commands "Read parameters", "Read Real-Data" and "Download" are expected to be repeated until the PC sends another command to stop them. Therefore, as shown in the flowchart, after implementing "Set-up" or "Reset" commands, program changes "Command Code" to "0FFH". It is a "Null Operation Command Code" in this program. It stops such a command taking place again in the next nest. The initial value of the "Command Code" is "0FFH"

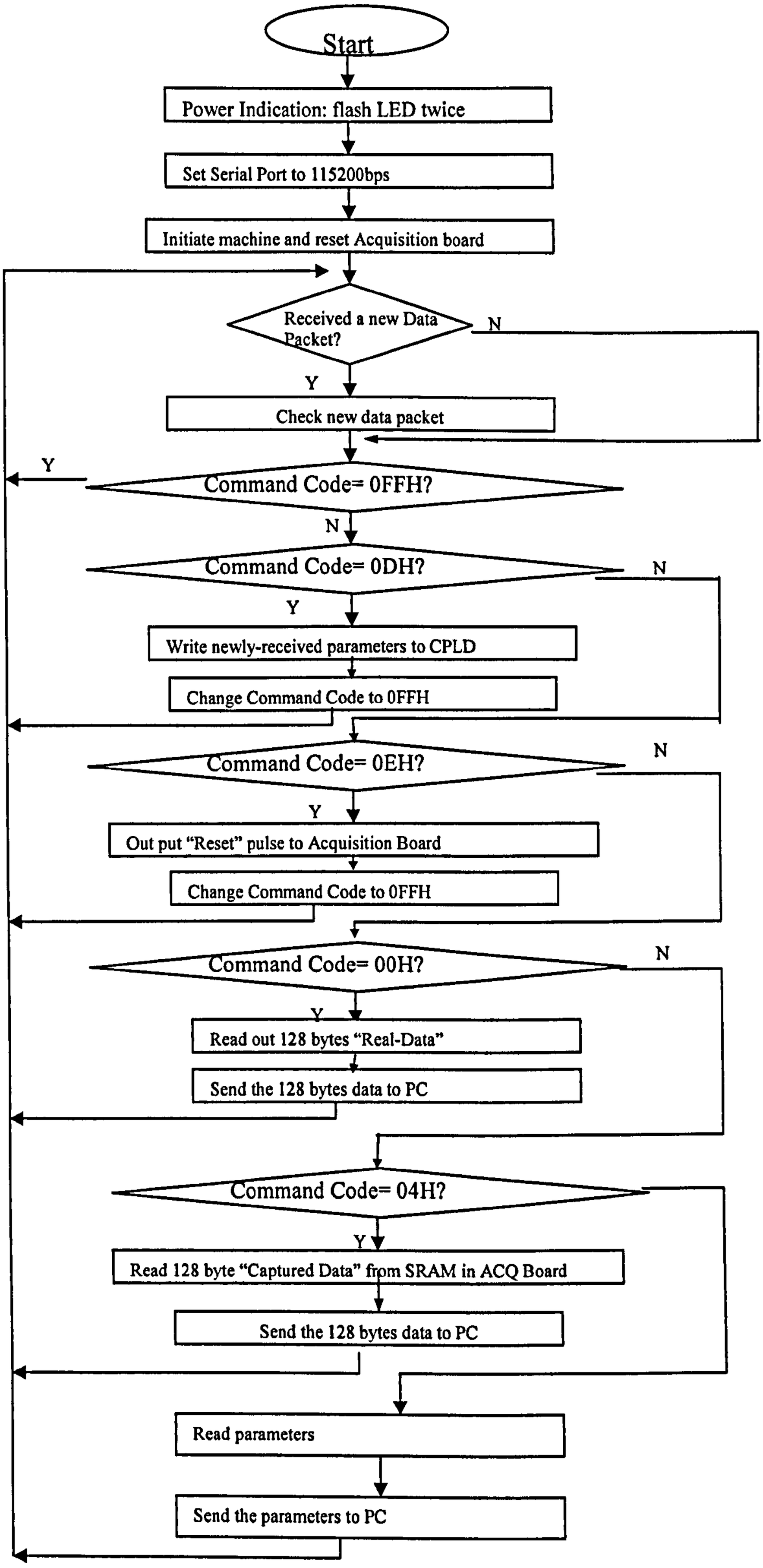


Fig. 4.48: Flowchart of Main Routine in AT89c52

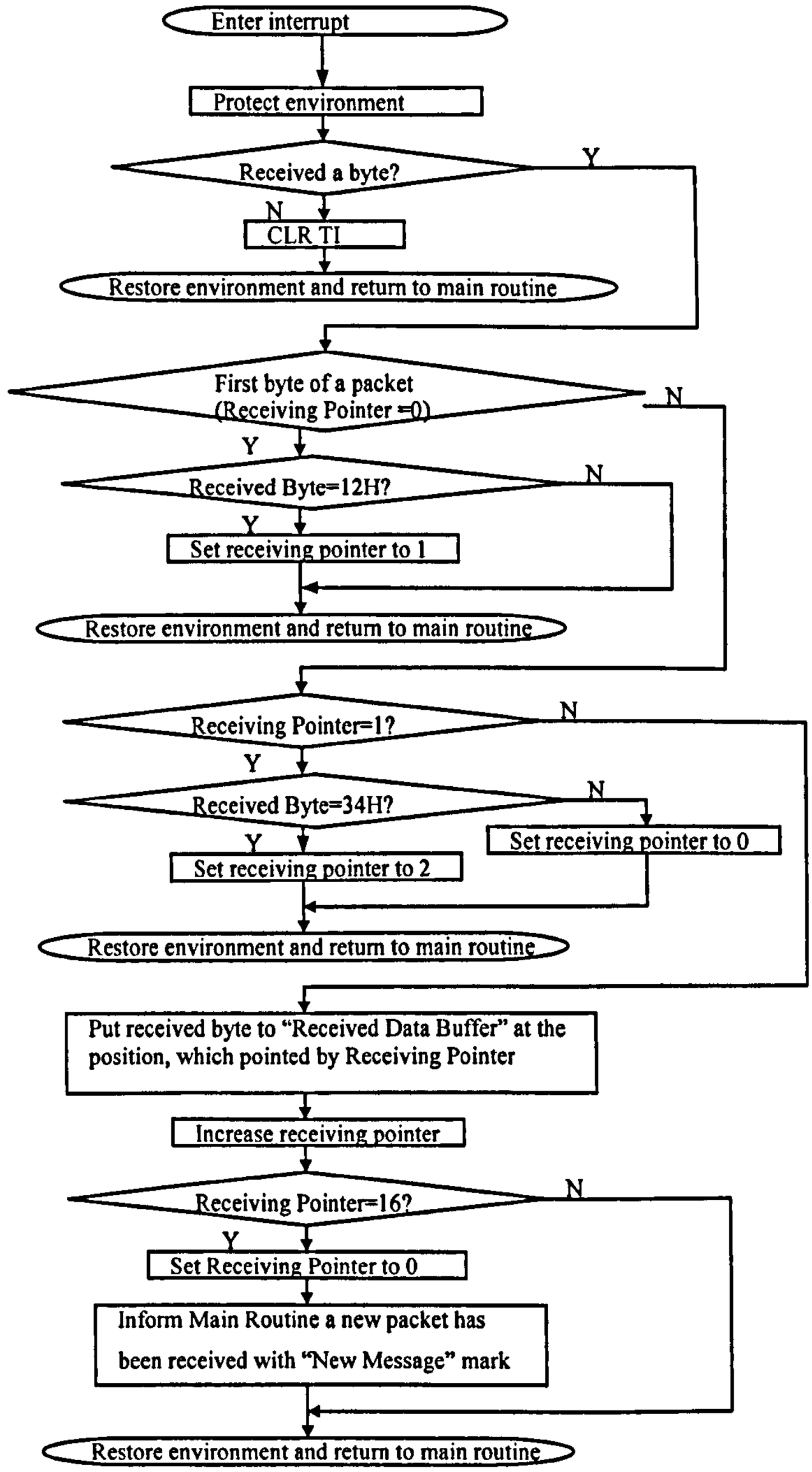


Fig. 4.49: Flowchart of the serial port interrupt service routine in AT89c52

4.2.3 PCB consideration for CPU Board

The PCB design for the CPU Board is a typical design of a double sided PCB. Only a few things need to be particularly specified here:

1) Adequate space should be made for the Heat Sinks of power components LM371.

2) As a prototype design, a "pads and through holes array" should be reserved for unforeseen modification.

3) As has been presented earlier in section 4.1, the locations of some Voltage Level Translators should be reserved.

Fig.4.50 shows the assembled CPU board.

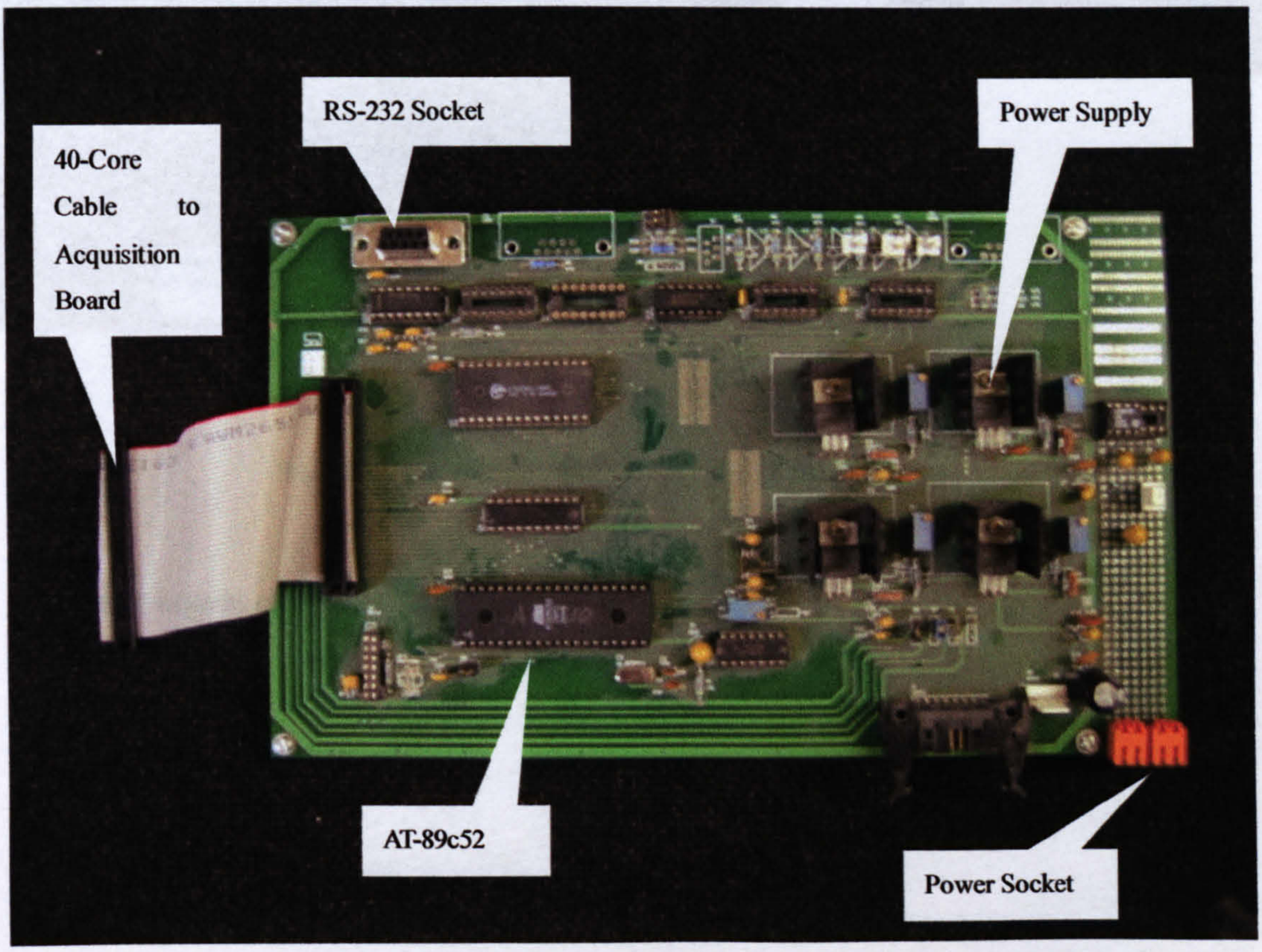


Fig. 4.50: Assembled CPU Board

4.3 Assembly of the RAU

As mentioned before, the RAU consists of an Acquisition Board and a CPU Board. These two boards are enclosed in a metal box, which is designed to support these boards and protect them from radiated EMI.

In Fig.4.51, the front panel has a BNC socket (Right picture in Fig.4.51) and the Rear Panel (Left picture in Fig.4.51) has the LED indicators, Switch, Charger terminal, RS-232 port to Modem and the power socket to modem.

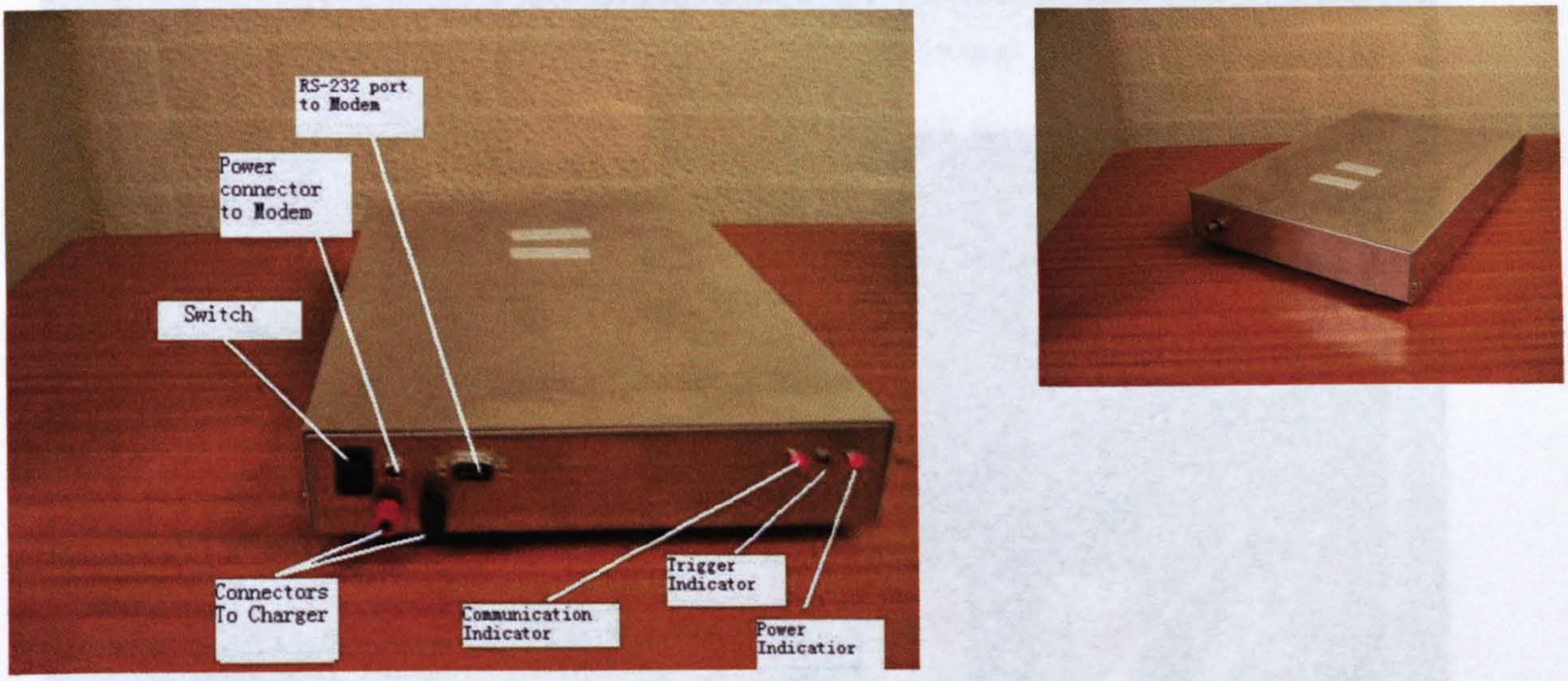


Fig. 4.51: Front and rear connectors of the RAU

The inner layout of the RAU is shown in the Fig.4.52.

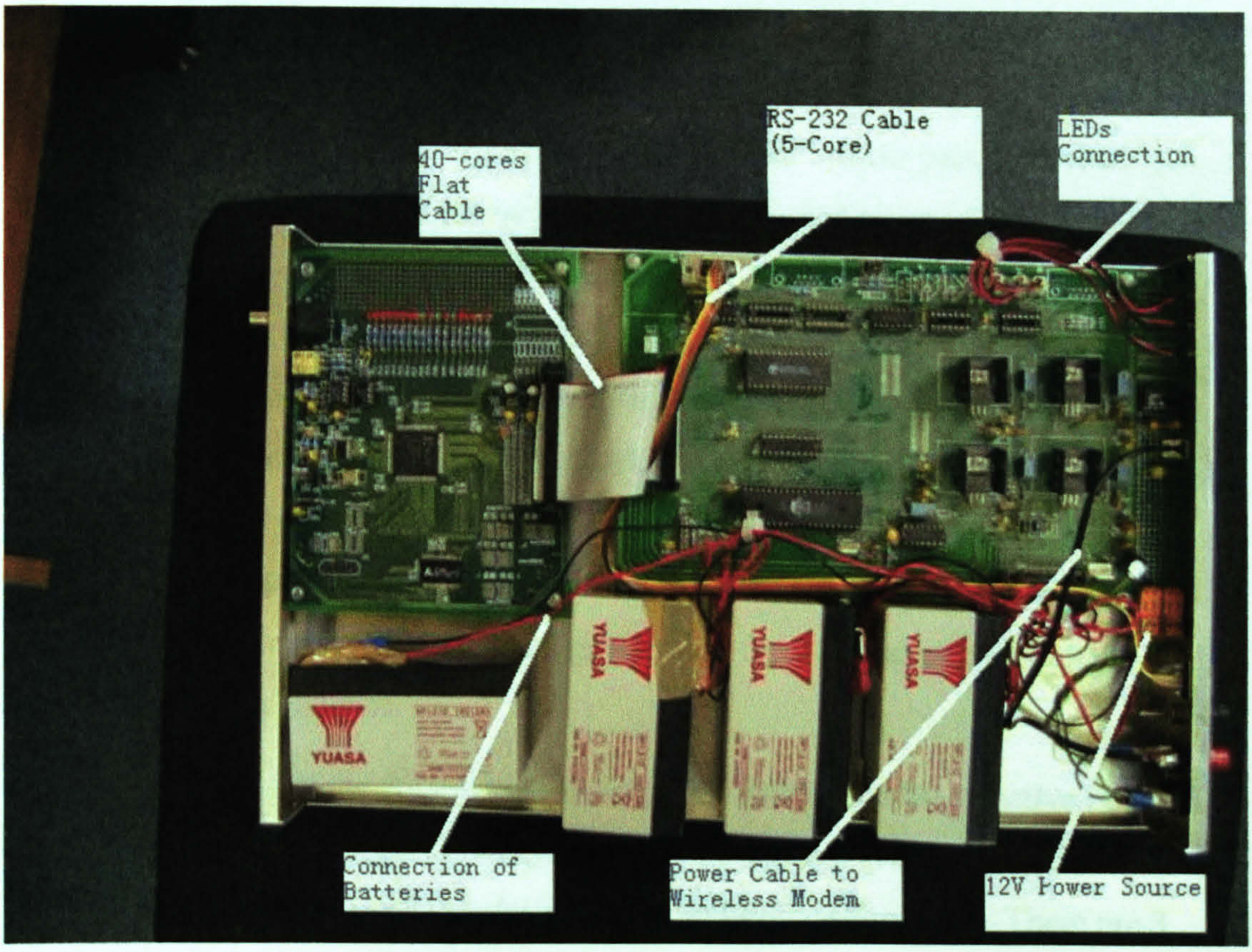


Fig. 4.52: Inner layout of the RAU

In Fig.4.52, An Acquisition Board on the left, a CPU board on the right and batteries at the bottom. They are fixed by using the assembling holes on the box. A 40-Core cable links the Acquisition Board and the CPU board. A 5-cores RS-232 cable connects the serial port socket (9-Pin

Fig. 4.53: Control of the 12V Power Source

D-Type Socket) on the CPU board and the same socket on the rear panel. Three 2-wire cables connect the LED sockets on the PCB and the LEDs on the panel. The 7.5 V power supply are linked to the 3.5mm "Jack Socket" on the panel and feeds power to the wireless modem. Batteries are connected in parallel to provide a 12V power source. The positive pole of the 12V Batteries through a SPDT (Single-Pole Double-through) switch, connected to either the power source connector on the CPU board or the positive connector of the battery charger. The connection of the 12V power source is shown in Fig.4.53. When the RAU is switched on, the positive pole of the batteries is linked to the 12V connector on the CPU Board. When the RAU is switched off, the positive pole of the battery is linked to Charger connector on the panel. This design protects the charging operation from taking place when the RAU has not been switched off.

The ground planes of the Acquisition Board, CPU Board and the negative pole of batteries are connected together to system ground. System ground should be connected to the metal enclosure for the best shielding performance. There are 3 main topologies to connect system ground to a shielding enclosure: Single Point Connection, Double Point Connection and Multipoint Connection. A debate about the advantages of these topologies has existed for many years. This thesis does not address this question. In real engineering, most designers select the connection topologies according to the practical result. In this project, after comparing the test results of different topologies, Single Point Connection was found to perform the best and the connection point is at the wireless modem power socket on the rear panel. The method of the test is giving a DC input to RAU, checking the ripple of the output by watching the real-data and recorded data. The EMC (Electro-Magnetic Compatibility) of this metal enclosure cannot be exactly calculated. The practical method is to select one box temporarily, and test the circuits with the box in real environment or the environment having the same EMI level. If there is not any EMC problem, the box can be chosen. The EMC tests of the whole system will be presented in a later chapter.

4.4 Examples of the RAU captured signal

This is the last section of this chapter, but before ending it some test results are given to help understanding the operator process of the RAU.

The test used a signal generator to give the RAU a signal with a certain waveform and trigger for the RAU, The data from the RAU is downloaded and displayed in "Dadisp©"— a "Waveform-Viewer" software made by Dadisp Corp. (US). The data, as described before, are byte sequences and every byte represents a sampling point. "Dadisp" locates these bytes on an X-Y coordinate, in which, Y-axis (vertical-axis) presents the value of the byte i.e. the amplitude of the sampling point and X (Horizontal axis) presents the sequence of the byte i.e. the time information of the sampling point. After positioning all the sampling points, Dadisp links all the points by straight lines. The range of Y-axis is from 0 to 256, which corresponds to signal level form –1V to +1V. The range of X-axis is from 0 to 524288 i.e. 512k sampling points. For the huge range of X-axis, just a small section of whole signals can be illustrated here.

As the Dadisp software links dots by straight lines, some waveforms shown here may not be perfect, especially for the high-speed signals. For example, at 80MHz sampling rate, if the measured signal has 20MHz frequency, every period will be sampled 4 times, i.e. 4 dots form a sine curve as show in Fig.4.56. However, it will not affect the test result. If a sine interpolator (based on sinc function) was used to reconstruct the signal, it would look much better. Fig.4.54 shows different recovered results of using "Straight Line" interpolator and using "Sine" interpolator in a DSO.

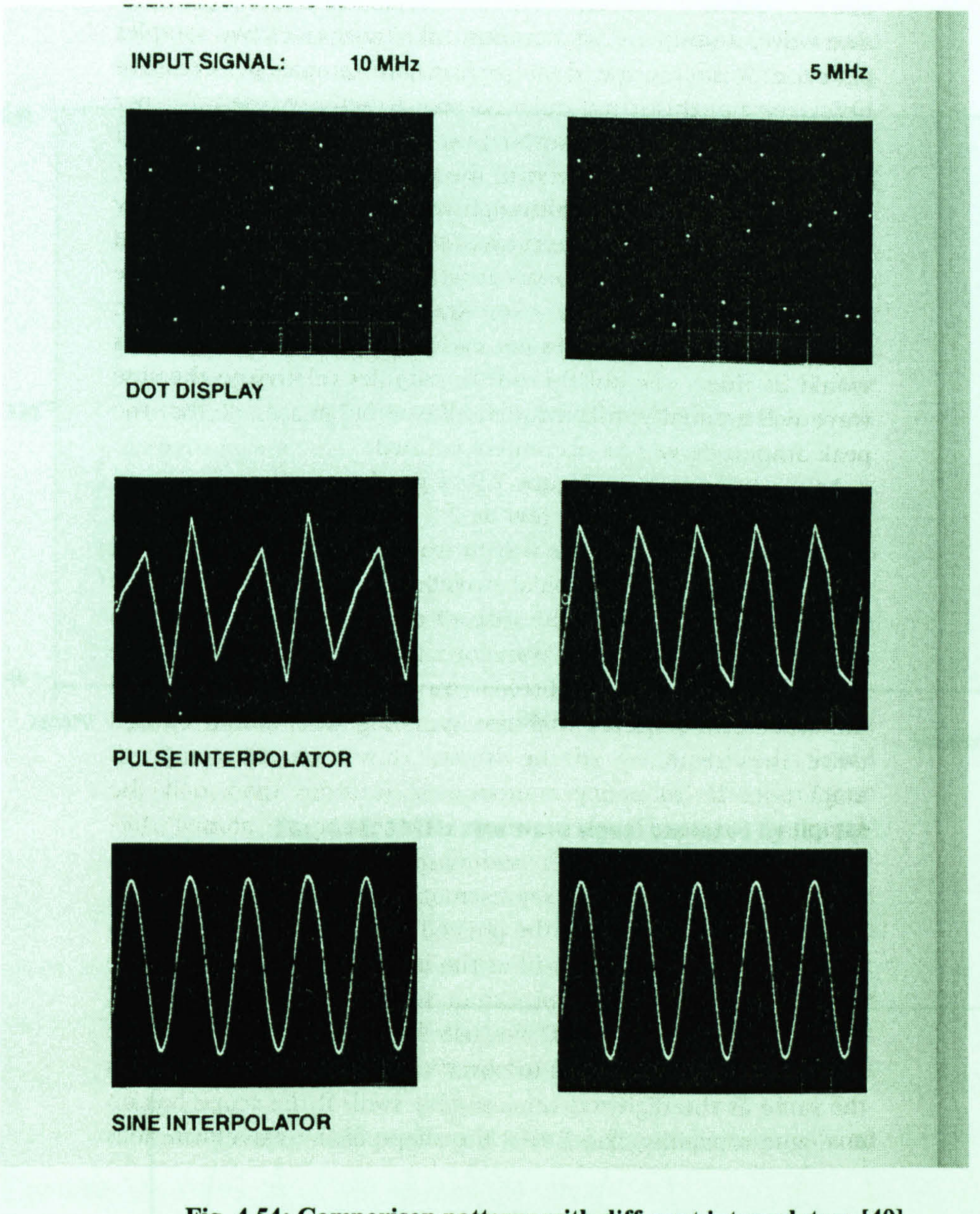


Fig. 4.54: Comparison patterns with different interpolators [49]

The Dadisp software does not have the function of "Sine Interpolator". Fig.4.55, Fig.4.56 and Fig.4.57 show the signals recorded by the RAU and displayed by Dadisp:

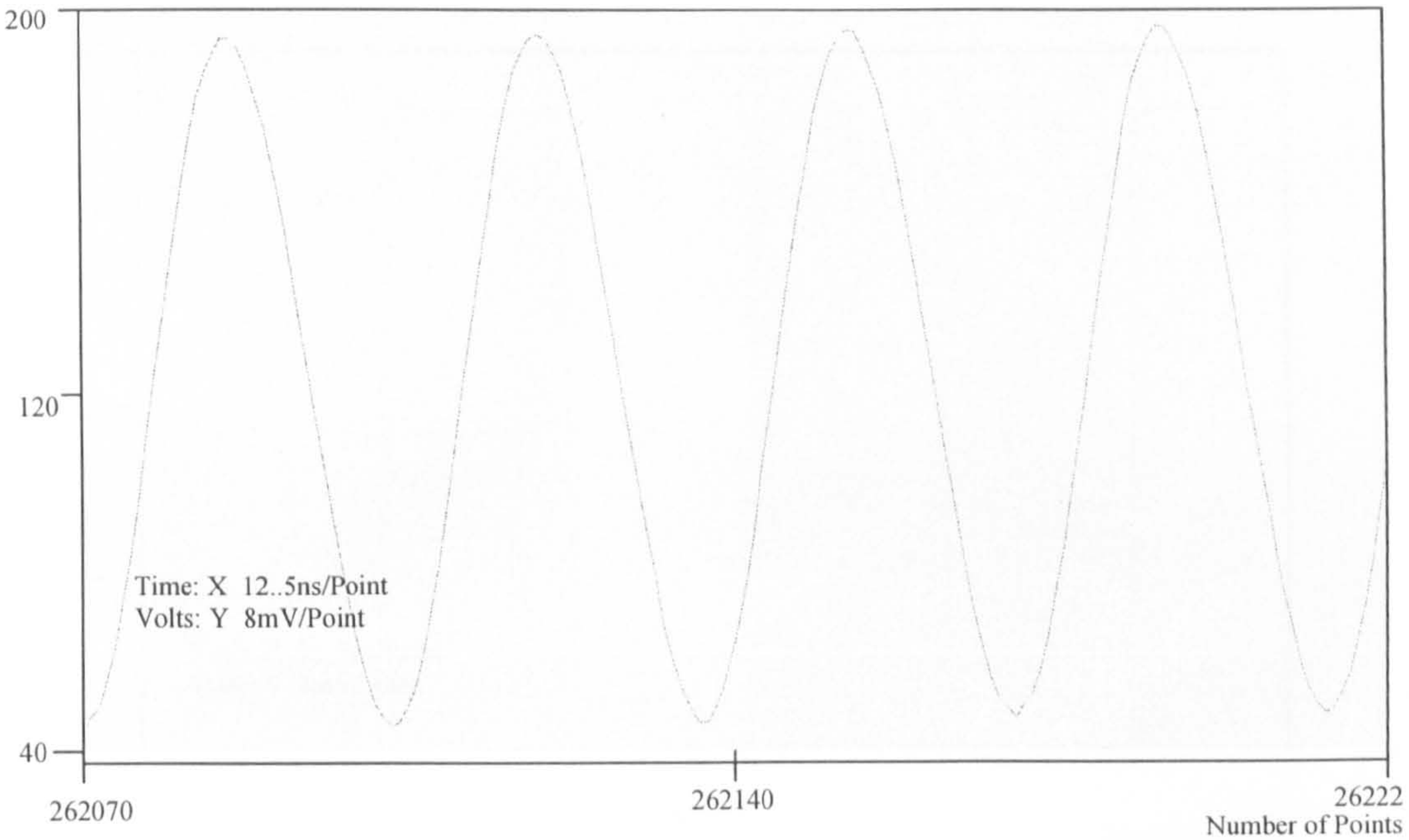


Fig. 4.55: 2MHz sine wave signal captured by the RAU

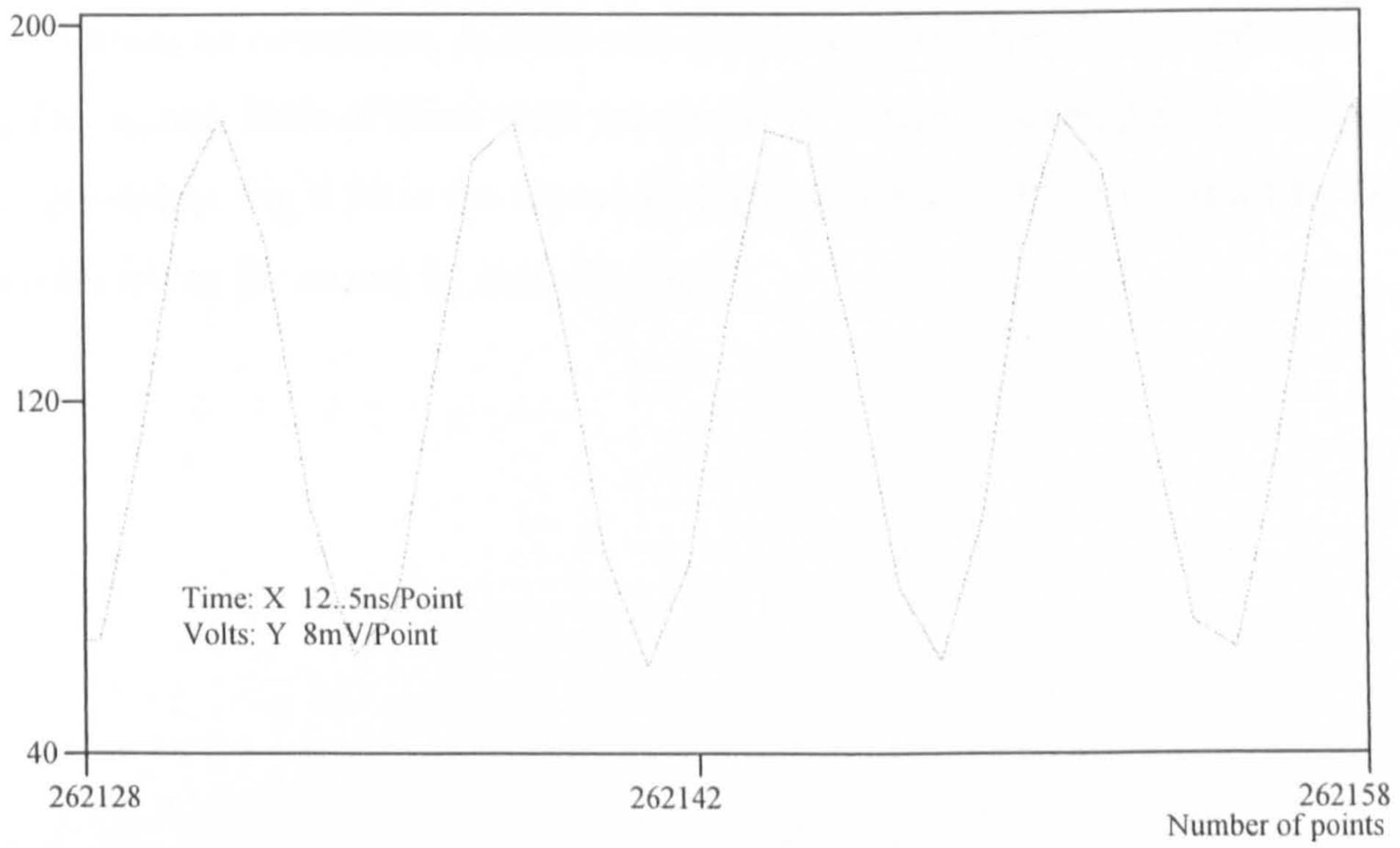


Fig. 4.56: 20MHz sine wave recorded by the RAU

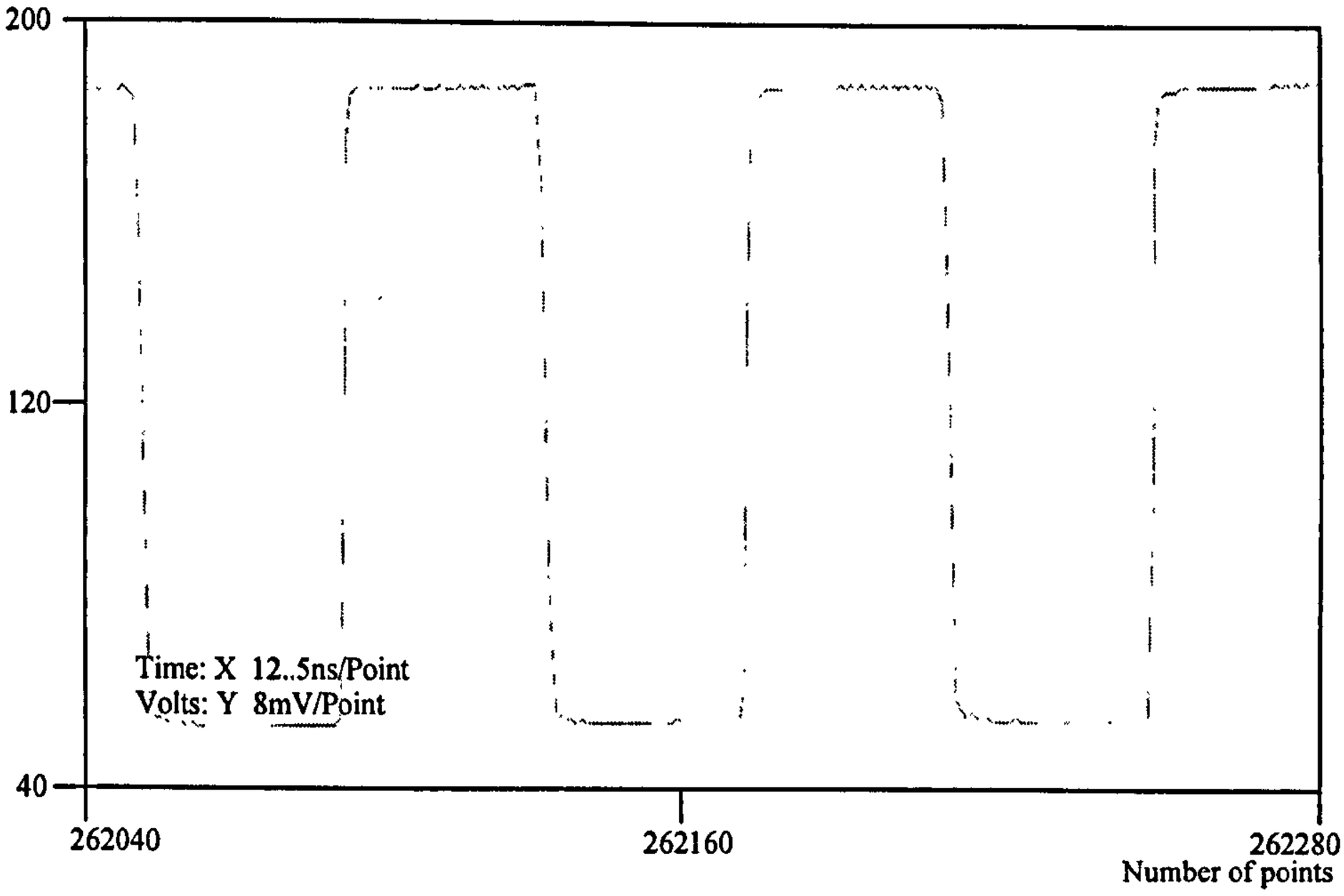


Fig. 4.57: 1MHz square wave recorded by the RAU

Fig.4.58 and Fig.4.59 show the records of a transient signal caused by the switching-on action of the signal generator. At the moment of being powered-up, the signal generator outputs an overshoot. A DSO was also linked with the RAU together to measure this signal. Both of them were set-up to 0.5V trigger-level, 50% pre-trigger and 0 trigger-delay. Fig.4.58 is the record by RAU and Fig.4.59 is the record by DSO. These results are as far as can be seen the same.

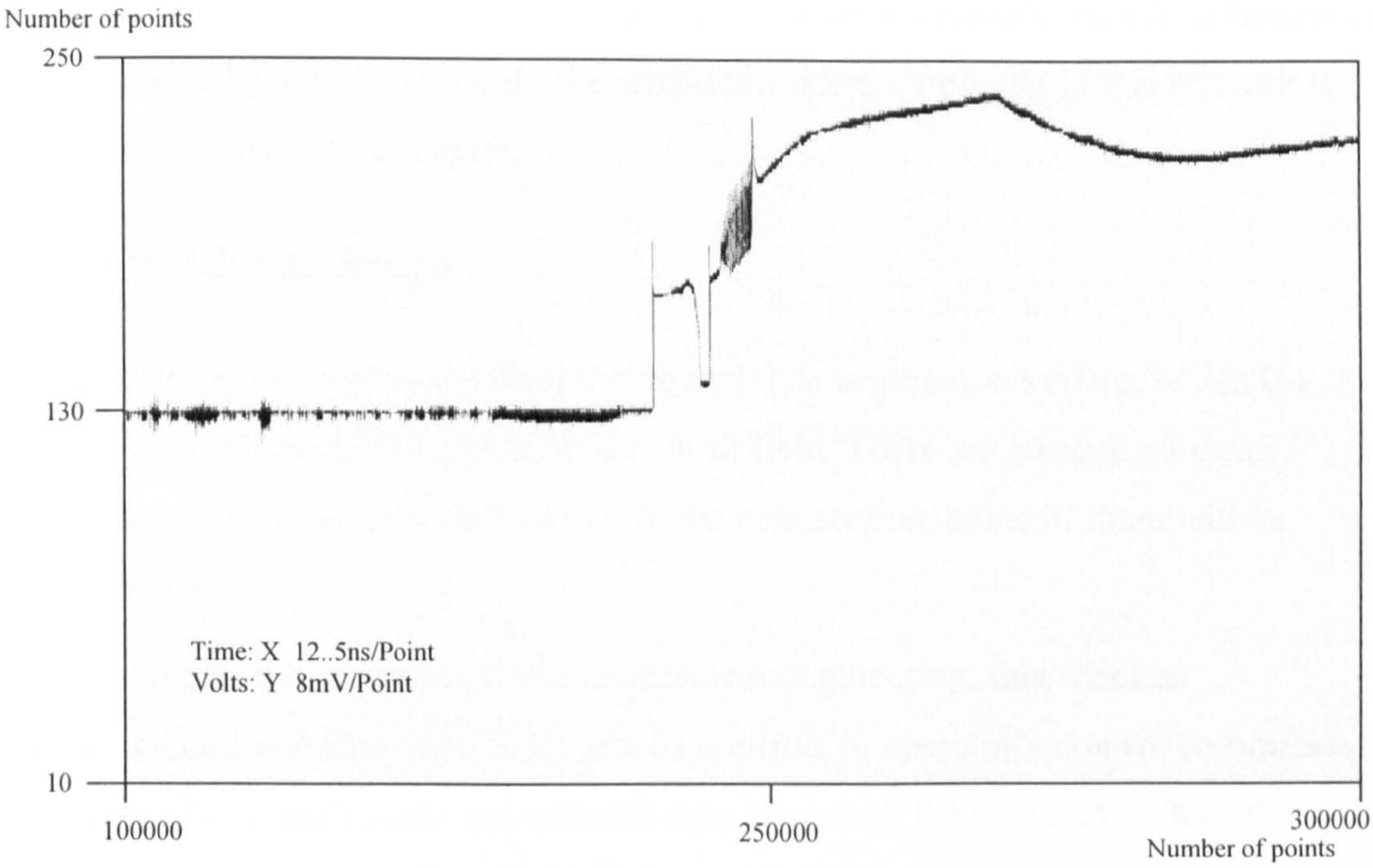


Fig. 4.58: Switching-on Pulse from signal generator recorded by the RAU

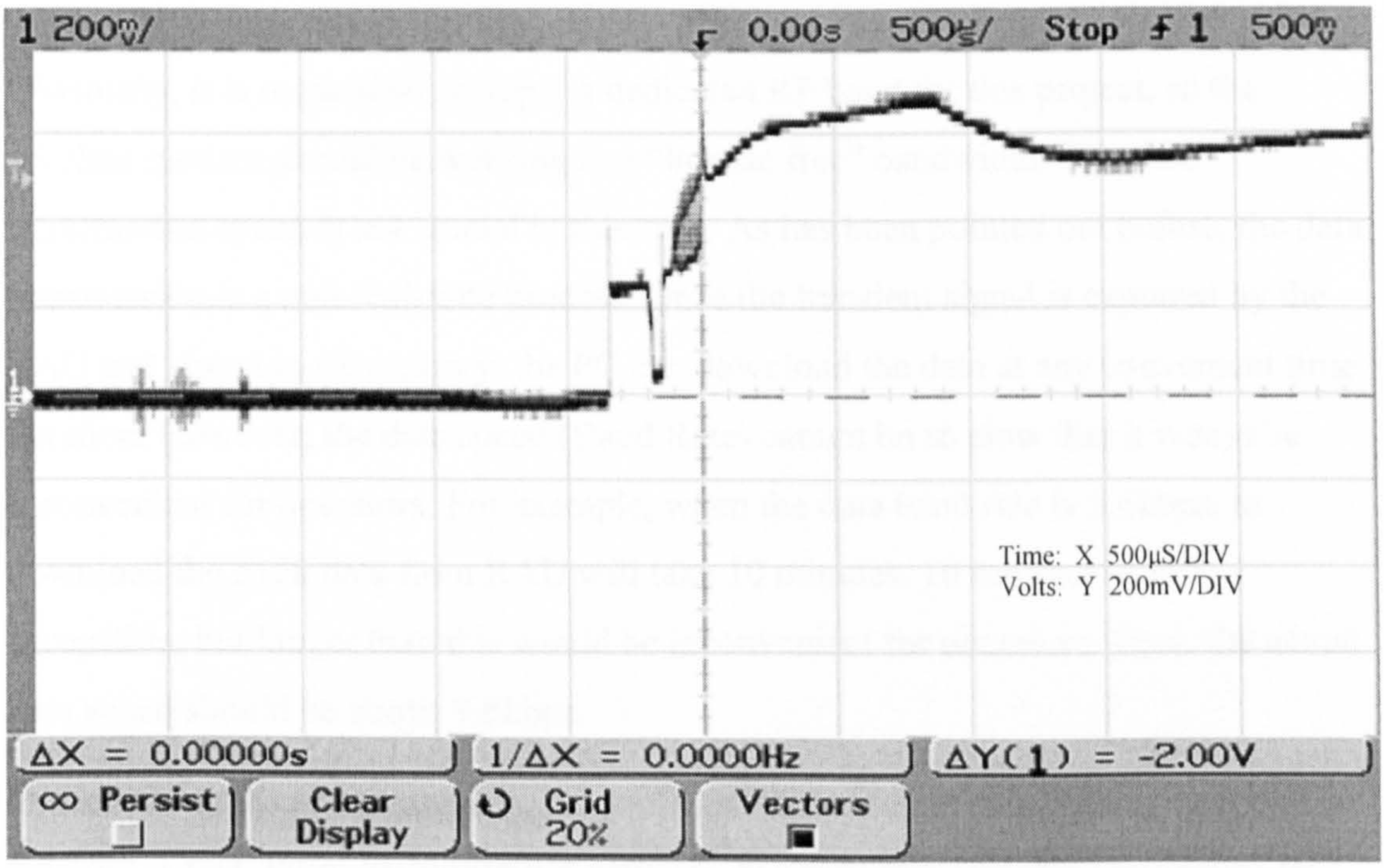


Fig. 4.59: Switching-on Pulse from signal generator recorded by the DSO

Chapter 5 The Wireless Data Communication Network

This chapter presents the wireless data communication network, including functions, structure and a simple protocol. The wireless modem employed in this network is also introduced in this chapter.

5.1 Functional design

This wireless network is a typical distributed data acquisition system, which is a common application in the industrial control field. There are various wireless modems suitable for this application. In the next section, some of them will be introduced.

According to the requirement of measurement engineering, this wireless communication system should be able to transmit an operator's control commands from the PC to each RAU and transmit data from each RAU to a PC. Thus, this network should be a bi-directional, Point-to-Multipoint network. The communication range should be larger than 50 metres to meet most measurement circumstances. Of course, a wider wireless range would be better, but a wireless modem with longer transmission distance always has a higher price and has greater power consumption. Obviously, it is impossible to apply a dedicated RF band for this project, so the wireless modem should be working in a "license free" bandwidth. The data transmission speed is not crucial in this case. As has been pointed out before, the data transmission is a non-real-time process. Once the transient signal is captured by the RAU and stored in its memory, the PC can download the data at any convenient time duration. However, the data speed (Baud Rate) cannot be so slow that it would be inconvenient for operators. For example, when the data baud rate is 9.6kbps, to download the 512k data from RAU will take 10 minutes. 10 minutes is still acceptable, but longer than this would be inconvenient for operators. Thus, the actual data speed should be above 9.6kbps.

Summarizing the above analysis, the profile of this wireless data communication network is that, Point-to-Multipoint network, bi-directional, working in license-free RF band, more than 50 meters transmission range, and more than 9.6kbps actual speed.

5.2 Modem selection

As mentioned earlier in chapter 2, the wireless modem should have standard interfaces to the host machine and provide strong data protection. To select the modem, the data rate, communication range, noise immunity and the price of the products need to be considered. Due to low cost preference, the price of the modem should not exceed 300 pounds. However, it does not mean that the high price product need not be examined here. Because future applications, some engineering applications may need a better performance and be regardless of price. For example, a "long range" wireless modem always has a high price, which is not taken by this prototype system but can be recommended for a long distance application in the future. Thus all available products have been examined. The short list is given in Table 5.1. (All the listed products use frequency modulation).

Table 5.1: Short list of the wireless modem

Model	BlueWave Industrial RS232 Cable	RM96XX Radio Modem	HPS-120	X8200 Radio Modem	232C-868 FRI	ADAM-4550	SRM 6100/ 6000	SST-2450
Frequency	2.4G Bluetooth	400-480M	2.4G Bluetooth	460-470M	868MHz	2.4G	2.4G/ 900M	2.4G
Supplying	UK supplier, In stock	UK supplier, In stock	UK supplier, In stock	UK supplier, In stock	UK supplier, In stock	UK supplier, In stock	US supplier, In stock	UK supplier, 4-8 weeks
Manufacture	Wireless Future, UK	Wireless Data, UK	HandyWave, Korea	Warwick Ltd., UK	RF Solution, UK	Advantech	DataLink, US	ICPDas,
Data Speed (bps)	115200/ 1M	19200/ 16K	115200/ 1M	115200/ 20K	38.4K/ 20K	115200/ 1M	115200/ 1M	19200/ 1M
Range	100m	10km	100m/ 500m with extension	1km	600m	150m/ 20km with extension	24km	300m
Network	Polling	Point-to-multipoint	Polling	Point-to-Multipoint	Point-to-Multipoint	Multipoint (Peer to peer)	Multipoint (Peer-to-peer)	Multipoint (Peer to peer)
Error Control	FEC and ARQ	FEC and ARQ	FEC and ARQ	ARQ	ARQ	ARQ	FEC and ARQ	ARQ
Industrial Design	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes
Power Supply	150mA @ 3.5~9V	500mA@12V	110mA@ 5~12V	350mA@ 10~26V	33mA@ 12V	500mA@ 10~30V	650mA @ 12V	200mA@ 12V
Interface to Host	RS-232	RS-232, TTL and RS-422	RS-232	RS-232 and TTL	RS-232	RS-232 and RS-422	RS-232 and RS-422	RS-232
Price (Pounds)	170	500	110	400	100	570	1200	224
Note							Recomm-ended by an expert	Recomm-ended by an expert
Advantage	High-speed, good price, Bluetooth	Wide range, Multiple frequency channel	Low cost, high speed, Bluetooth	Wide range.	Low cost	High speed.	Long range	Medium range
Disadvantage	Short range	High price, low speed	Short range, no metal box	High price, low speed	Low speed	High price	High price, needs an European license	Not in stock

The information was provided by manufacturers in 2003 and was checked with their technical support staff in that year. The products may have been updated since then. For details of these products, please refer to [94, 95, 96, 97, 98, 99, 100].

In the "Data Speed" row, there are two numbers for every product. The first number corresponds to the "Through out" data rate, at which the host machine exchange data with modem. Second number corresponds to "Over-air" speed, at which, the modulated bit stream is transmitted by a carrier wave. The real data speed, at which the data are exchanged between two host machines, is called "Actual Data Rate". Most manufacturers do not specify this parameter. It depends on the bandwidth of the carrier wave, the encoding efficiency and the error rate in different application circumstances. For example, an error code may cause a repeat transmission and decrease the Actual Data Rate. Generally, the "Actual Data Rate" can achieve 30%~ 70% of the "Over-air" speed.

In the "Range" row, all the listed the numbers refer to the emission radius of the modems in an open-air space. In a substation, since there is a fence around the Switchyard, the actual distance may be reduced.

In the "Network" row, "Polling" means that modems can just build a Point-to-Point connection simultaneously, but they can achieve point-to-multipoint network by a polling mode. In this configuration, the master host machine connects each remote modem in turn.

In "Disadvantage" row, the product SRM6100/6000 is said to need a European License. The US manufacturer was applying for the license for European markets at the end of 2003 and was informed that their products would be approved by the end of 2004. Without the license problem, the product can be a good choice for a long distance application in the future.

In the above short list, SST-245, X24-109pk, SRM6100, X8200, HSP-120 and "Bluewave Industrial 232 Cable" are working at a 2.4 GHz frequency band. All of them apply "Frequency Hopping Spread Spectrum" technology, which provides better "Noise Immunity". In particular, Bluetooth products implement a new technology of "CQDDR", which further strengthens noise immunity. Therefore, Bluetooth products are preferred for this project. Another benefit of using a Bluetooth product is that this would be the first time a Bluetooth product was used for EMI measurement in a substation. This experience can be reference for other power engineering application that may use Bluetooth technology.

A GSM (Global Service of Mobile) wireless modem had also been considered [101]. That modem has a RS-232 interface to connect with the host machine and transfer data files over the GSM network at 9.6kbps baud rate. The advantage of this is that an operator can control the acquisition units everywhere. The disadvantage is the extra cost for SMS (Short Messaging Service) to send a big data file.

In comparing all the products in the short list, the "Bluewave Industrial 232 Cable" was chosen. Fig.5.1 shows the picture of the wireless modem.

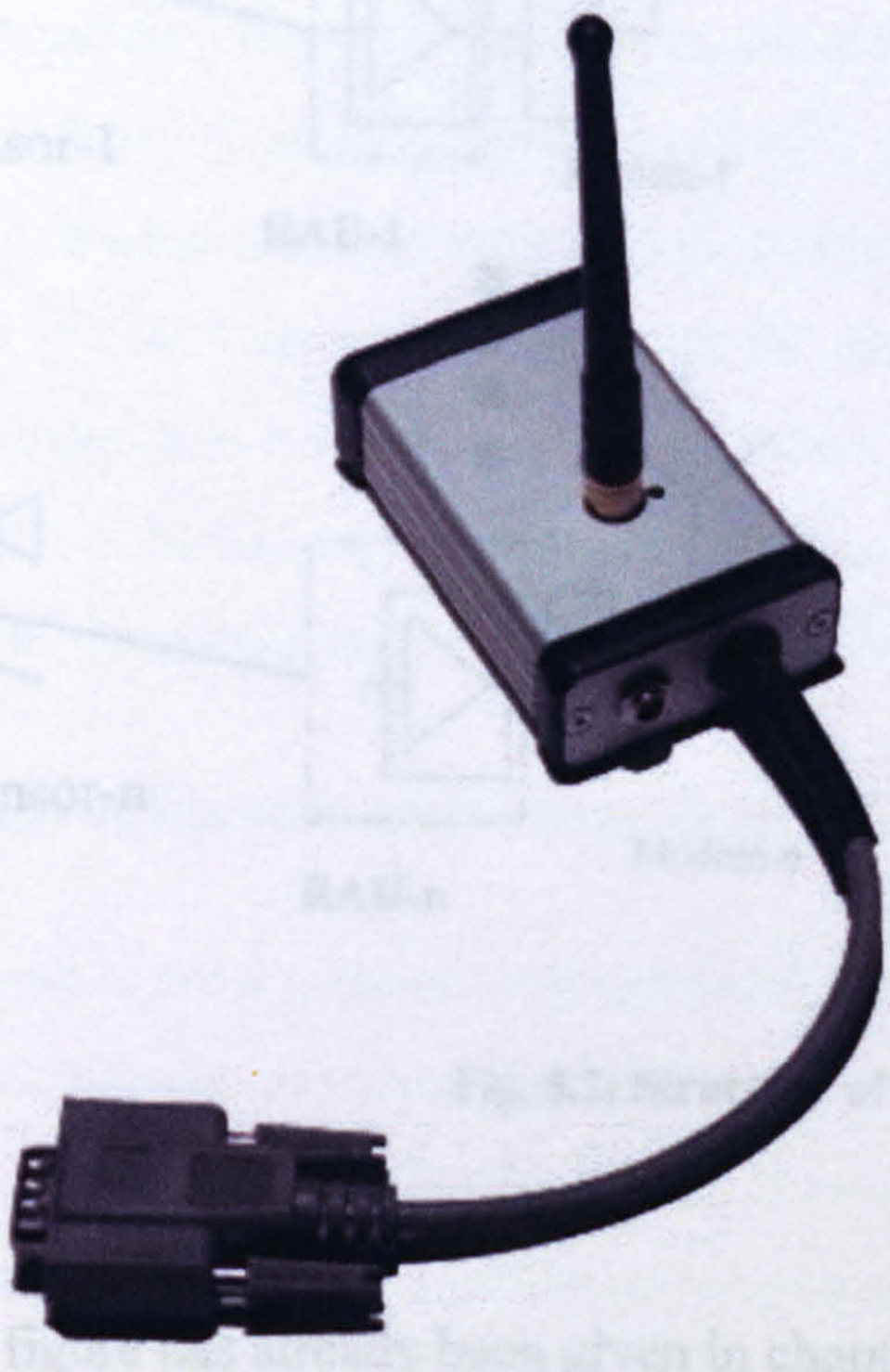


Fig. 5.1: Picture of the modem "Wireless RS-232 Cable"

The process of selection of the wireless modem is choosing one from the shortlist according to the datasheet and then testing it in the real application field. If the first selected modem is not satisfactory, analyse the problem and try another modem. Fortunately, in the real application, first selected "Bluewave Industrial 232 Cable" was satisfactory.

5.3 Network structure and communication process

The Bluewave Industrial RS232 Cable is the wireless modem product of Wireless Future Company. It fully conforms to Bluetooth class1 V1.1., has a 100m wireless

range and a SPP (Serial Port Protocol) profile. It can be connected to the host machine with a RS-232 port. With this modem, the point-to multipoint network is built as shown in Fig.5.2:

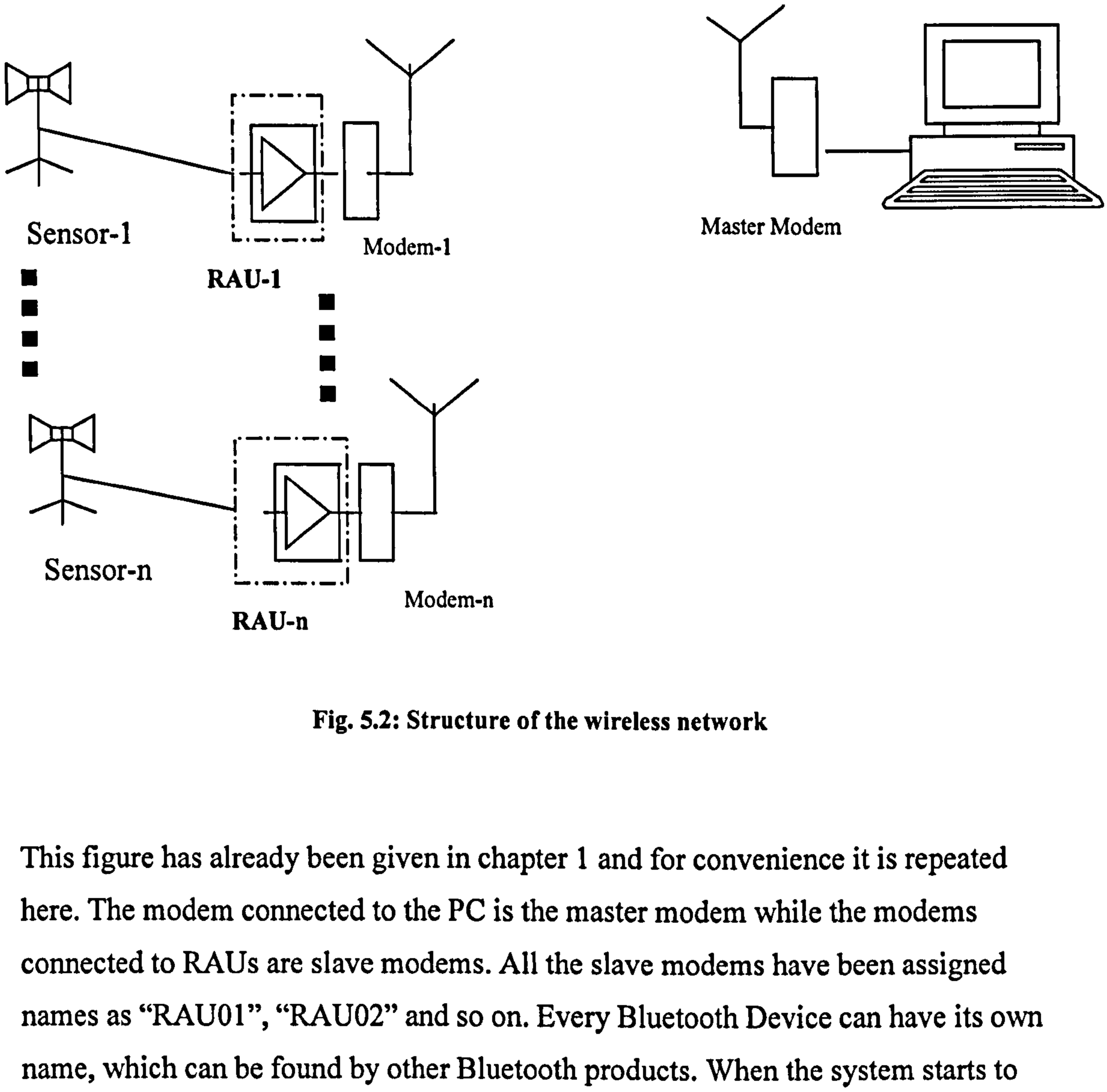


Fig. 5.2: Structure of the wireless network

This figure has already been given in chapter 1 and for convenience it is repeated here. The modem connected to the PC is the master modem while the modems connected to RAUs are slave modems. All the slave modems have been assigned names as "RAU01", "RAU02" and so on. Every Bluetooth Device can have its own name, which can be found by other Bluetooth products. When the system starts to work, the PC sends three '+' to its modem. The three ASCII codes "+" are separated by 100ms. On receiving them, modem turns to Command Mode. In "Command mode" the PC can control a modem with AT commands set. Initially, PC send "AT+BWI " to modem to perform a Bluetooth inquiry. Implementing this inquiry, the modem will search for other Bluetooth devices within an effective range, then returns a "Device List" to the PC, which contains the names and addresses of all the

Bluetooth devices that have been found. If an RAU with its attached modem has been powered-up, it will be displayed in the devices list. The operator can then establish a connection between the PC and one of the RAUs by using "AT+BWC" command plus the address code of the target modem (Every Bluetooth device has a global unique address code). Once the connection is established, the PC sends "AT+BWE" command to its modem letting it exit "Command Mode" and return to "Data Mode". In "Data Mode", any data sent from the PC to its modem will be sent to the opposite wireless modem and reproduced at the RS-232 port of the opposite host machine, and vice versa. Thus, the wireless connection can be regarded as a virtual RS-232 cable link between the PC and RAU. After the PC has finished the data exchange with the target RAU, it enters "Command Mode" again by sending three '+'. In "Command Mode", the PC disconnects the current connection and establishes a new connection with another remote RAU, then exchanges data with that RAU. In this way, the master machine can alternate the connection with all the remote slave machines and build a point to multipoint network.

5.4 Data format and other definitions of the communication network

As there is not a generate communication protocol can be used in this case, a simple data communication protocol has been create for this data communication between RAU and PC. It includes the format of two data packets and other definitions implemented in this communication system. The data communication system had been designed to adapt general license-free wireless modems with serial ports. Although in the final design, a Bluetooth product was chosen, the communication principle also aims to suit other general products. Therefore, the data format of this communication system has a general structure for serial communication. It is easy to modify it to adapt to most general wireless modem having a serial port.

The data format here defines the bit sequence of the data frames transmitted between the PC and the RAUs. This format also defines the method of how to exchange data between the PC and the RAUs. The set of these definitions can be seen as a communication protocol, since wireless modems have implemented their protocols to achieve the data communication functions. In this case, the designer does not need to be concerned with details of how the data are transmitted over the wireless channel,

and need only consider the data access method at the level of source machine and the destination machine. If the whole system is thought of as a data communication network, then the PC and the RAUs implement the protocol of the application layer and the wireless modems implement the protocol of other lower layers i.e. physical layer, data link and network layer. It should be clarified, here, that the application layer does not mean the application software in the PC and RAU, but is the interface between the application software and the network service [102]

There are numbers of wireless modems in the market designed to replace cable link and provide a so-called "Transparent Link". In fact, before selecting the wireless modem, the network was built using RS-422 cable, and the data format was made based on the cable linked serial data communication.

Generally, in serial data communications, for synchronization, the data is transmitted in packets, which start with synchronous bits. A typical serial data packet includes 4 elements: Synchronous code, Control field, Data field (or load) and Verification Field [103]

The synchronous code in the data packet from the PC to the RAU is "1234"Hex (2 bytes) and "4321" Hex in the data packet from the RAU to a PC. The control field usually includes address, data type etc. In this design, since the Bluetooth modem make point-to-point connections, an address code is unnecessary. However, for future applications with a true point-to-multipoint connection, the address code may be needed, thus, one byte is reserved in the data frame for address information.

In the data packet from the PC to the RAU, the control field contains an address byte and a "Command" byte. The data field contains the operate parameters, which the command requires. All the commands and its combined data are listed in Table 5.2:

Table 5.2: Data to be sent from PC to RAU

Commands	Combined data
Set-up parameters	Trigger-level, Trigger-delay, Trigger-source, Sampling rate, states
Reset	Null
Download "Captured Data"	Null
Read "Real Data"	Null
Read "Parameters"	Null

All the commands are represented by 1 byte command code encoded as below:

Set-up parameters: 0DH

Reset: 0EH

Download “Captured Data”: 08H

Read “Real Data”: 00H

Read “Parameters”:04H

Although the data combined with commands have different lengths (“Set-up” requires 6 bytes data and the others require zero), the data packet still has a fixed length instead of a variable length to simplify the communication operation. It can be seen that there are a maximum of 6 bytes to be transmitted in a signal packet. However, for future applications, the data packet reserves some vacancies. For example, if the next version of this system adds a function of controllable input amplification, the amplification code will take a byte.

Therefore, the data packet includes 2 bytes of synchronous code, 2 bytes in the control field (Address and Command), 8 bytes in data field (6 bytes parameter and 2 bytes reserved) and a verification field. In data communications, the data frame usually has a verification field to protect the information in this data frame. Using these codes, the receiver can check every received packet and implement FEC or ARQ to correct the errors. In this communication system, wireless modems apply a data protection strategy and ensure the correction and integrity of data communication over the air. If the wireless modems have provided enough protection, it is not necessary to employ data protection methods again in the application layer. However, in the case that future applications use other types of modems, which might not provide adequate data protection, the application layer can employ its data verification strategy to complement. Thus the 4 bytes have been reserved for the verification code.

In actual practice, the communication system exhibits perfect data integrity and correctness, no error has been found during the communication process under the EMI conditions in a switchyard and laboratory, which will be presented in Chapter 7. Thereby, the verification process in this application does not take place and is just

reserved for future application.The format of the data packet transmitted from PC to RAU has been illustrated in Fig. 4.46.

The command code in the Fig.4.46 has been listed in Table 4.6. The parameters (only valid with the "Set-up parameter" command) are listed below:

Byte 5: states (Reserved)

Byte 6: Trigger-level

Byte 7: low byte of logic-delay-time

Byte 8: Middle byte of the logic-delay-time

Byte 9: High byte of the logic-delay-time

Byte 10: Sampling speed selection code

Similar to the data format of the packet from the PC to the RAU, the packet from RAU to PC also consists of four parts: Synchronous code, Control field, Data field and Verification field. All the data sent from RAU to PC are encoded with a fixed length packet. The synchronous code in this packet is "4321" H. The control field include a reserved address byte and a byte specifying the data type in its packet.

There are 3 types of data to be sent from the RAU to the PC: Real Data, Parameters and Captured data. The data type indication numbers for them are 40H, 41H, 42H respectively.

Data field contains the 3 types of data: Parameters, Real-data and Captured-data. Captured-data has 512k in length, while the other two kinds of data have endless length, that means once the RAU starts to send Parameters or Real-data, until other commands stops it, the data will be send to the PC continuously. In other hand, the length of the data field in this packet cannot be endless. So, for convenience of processing and considering future verification functions, the data length is assigned to 128 bytes. Thus the format of the data packet from RAU to PC is formed as shown in Fig.4.47.

For the "Real data" and "Captured data" packet, in data field, all the 128 bytes are filled with requested data. For the "Parameter" data packet, only the 1st to 6th bytes in

the data field are required and the other locations are unused. The 6 bytes are listed below:

Byte 1: states

Byte 2: Trigger-level

Byte 3: low byte of logic-delay-time

Byte 4: Middle byte of the logic-delay-time

Byte 5: High byte of the logic-delay-time

Byte 6: Sampling speed selection code

The formats of byte 2 ~ byte7 have been given in section 4.1.4, Table 4.2.

Byte 1 is the "State" byte. Bit 7 of this byte indicates the "Triggered" state of the RAU, "1" means RAU has been triggered. The other 7 bits of this byte (Bit 0 ~ Bit 6) are reserved to "0".

The proceeding text has presented the protocol of this network in the application layer. The protocol is implemented by software in both the PC and RAU. The details of the software in the RAU have been described in Chapter 4 and the PC software will be described in Chapter 7. A brief description of the communication is given here.

When the PC starts the control program, the operator selects a RAU to communicate with. The PC turns its Bluetooth modem to command mode, establishes a connection to the specified RAU. After the connection has been established, it returns to the data mode. When the operator sets-up all the parameters for the RAU, the PC will send out a packet containing "Set-up Parameters" command and the corresponding parameters after. Receiving this packet, the RAU writes all the parameters to the respective registers. When the operator sends a "Reset" command, the RAU releases an original "Triggered" state and starts to capture the transient signal. When an operator send "Read Real-Data" command, the RAU will continuously send back the data packets containing Real-Data. On receiving the "Real-Data" the PC displays them in a waveform. If the operator sends a "Read parameters" command to the RAU, it will send back a "Parameter" packet, which receives and displays on the

screen. When an operator sends "Read captured data" command to the RAU, the RAU will send 512k "captured data" back to the PC, which receives the data and saves them on the disk. When operators want to change object from one RAU to another one, they can exit the control environment with the present RAU and input other RAU's name in DOS command line. The PC will disconnect the current wireless connection and establish another connection to the specified RAU.

In this communication system, the actual data transmission rate is 41kbps. The modem inputs data from the RAU at 115.2kbps,which is faster than the modem's actual speed. As a result, the modem uses an RTS signal to stop the RAU sending data when the data buffer is full. (For the functions of RTS signal, refer to section 4.4.1). Actual observations show that when the communication is on going, the RTS signal is a square wave with about 50% duty cycle and 1 second period. The RTS signal is also used to drive the communication indicator on the panel of the RAU. When the communication is on going, the LED flashes.

It can be seen that RAU has two data acquisition modes: buffered data mode and real time acquisition mode. Buffered data mode digitises and stores the signal with a high sampling rate. Every times when the trigger condition is met, the buffered 512K bytes can be read and transmitted from RAU to PC. As actual transmission speed of the wireless communication network is 40Ksps, to download the 512K acquired data, PC needs 130 seconds. When the PC is downloading the buffered data from RAU, RAU cannot acquire other signal. Thus, the minimum interval between two acquisition actions or two download actions is 130 seconds. Of course, the mnimum interval time can be different depending on different wireless modems.

Real time acquisition mode reads the data from A/D directly and sends the data to PC with out buffering, thus, the sampling speed depends on the data communication speed between PC and RAU. In this case the sampling speed is 40kSPS. Please note, this real time acquisition mode is not designed for measurement but only used for designer in commissioning work.

Chapter 6 Software design for PC-based control platform

This chapter describes the application software on the PC-side. The software provides users with a control platform to control remote RAUs and collect data from them.

This application software was intended to be a Graphic User Interface (GUI) working under Windows Operating System (Windows OS) and written by a C++ programmer. However, with the funding restriction, the application software programmer was not available when the system was being developed. The author had to create a temporary application to suit. This temporary application software was written using assembly language and has full functions of the control platform but with a text-interface under DOS environment. Currently, the graphic C++ program is being developed.

This DOS version program is a temporary version and will ultimately be replaced by the graphic version. Considering this fact, this chapter merely presents the principle of the PC software and briefly introduce the process.

For exact details of this software please refer to "The source code of the PC-software" in design files (Due to space limitation the hardcopy of the source code of this program was not included in this thesis)

6.1 Functions of the program for PC

This program is designed to allow an operator to do the following 6 operations.

1) Establishing a wireless connection with a specified RAU
2) Setting-up operational parameters for an RAU
3) Resetting the RAU
4) Monitoring the RAU operating state (watching parameters and triggered state)
5) Watching the "Real Data" to monitor the input signal
6) Downloading the "Captured Data" and storing them into the specified file

To establish a wireless connection, the PC first turns its master Bluetooth modem into "Command" mode and sends AT command "Disconnect" to the master modem over the RS-232 cable, letting it disconnect the wireless link with remote slave Bluetooth modem. Next, PC sends AT command "Connect to XXXXXXXXXXXX" to master modem letting it establish a connection to the address XXXXXXXXXXXX. "XXXXXXXXXXXX" is a 12 Hex-bit address code. Every Bluetooth device has such a 12-bit unique address. For example, in this system, the slave modem "RAU01" is addressed with "00:a0:96:1d:cd:56" and RAU02 is addressed with "00:02:78:02:d6:d2".

To set-up operational parameters to the RAU, users can press the "S" key at any time, the PC will display the "Set-up" menu as shown in Fig.6.1 to input all the parameters.

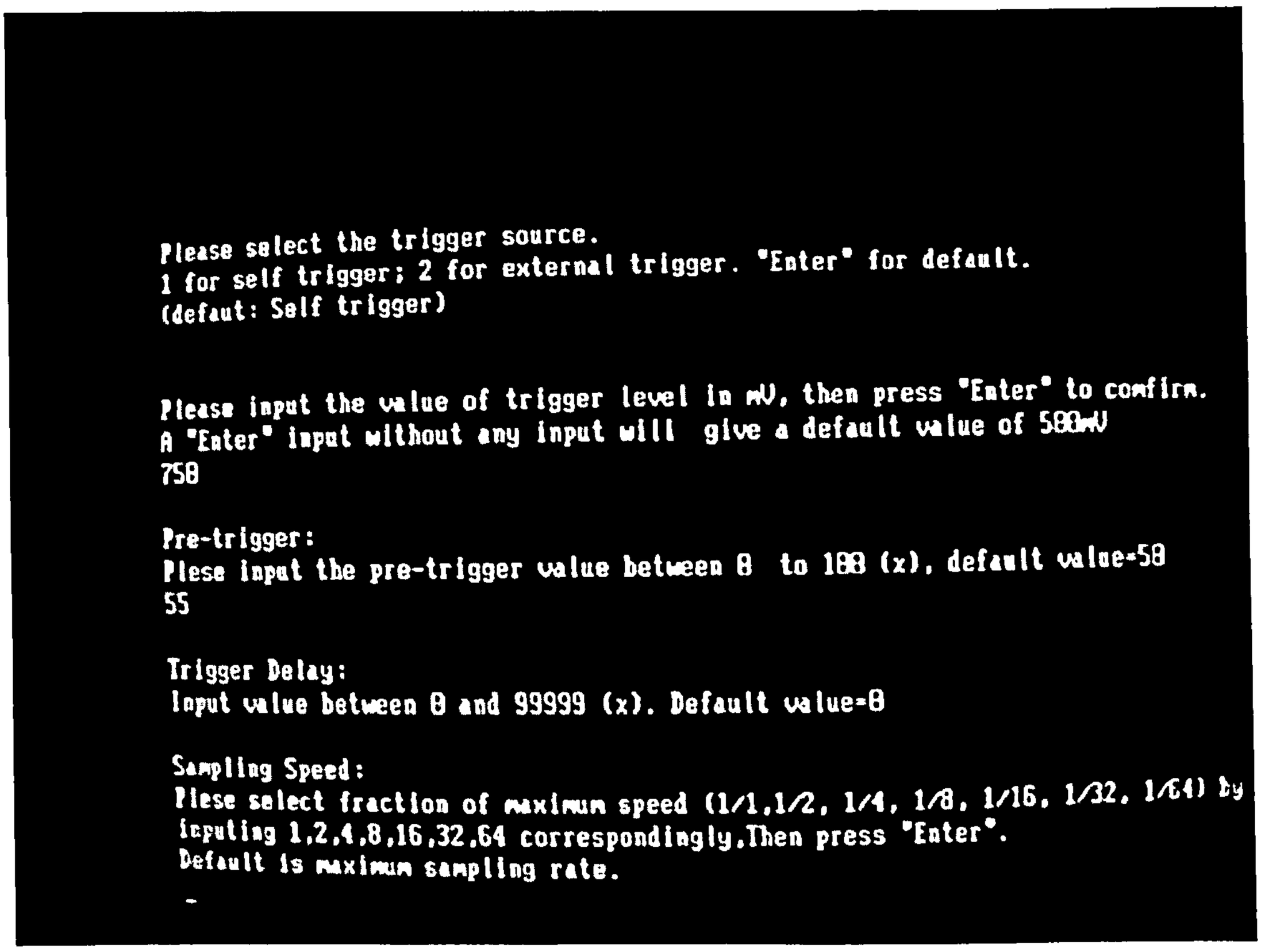


Fig. 6.1: "Set-up" menu in PC

Fig.6.1 illustrates the set-up operation to configure the RAU to "Self trigger", "750 mV trigger-level", "55% pre-trigger", "0 trigger-delay" and "full-speed sampling rate".

After the user inputs all the parameters, the program will encode them to a data packet with "set-up" property as shown in Fig.4.46, then sends this packet to the RAU. On receiving the packet, the RAU will configure the Acquisition Board according to these parameters, after which the PC will display the menu as shown in Fig.6.2:

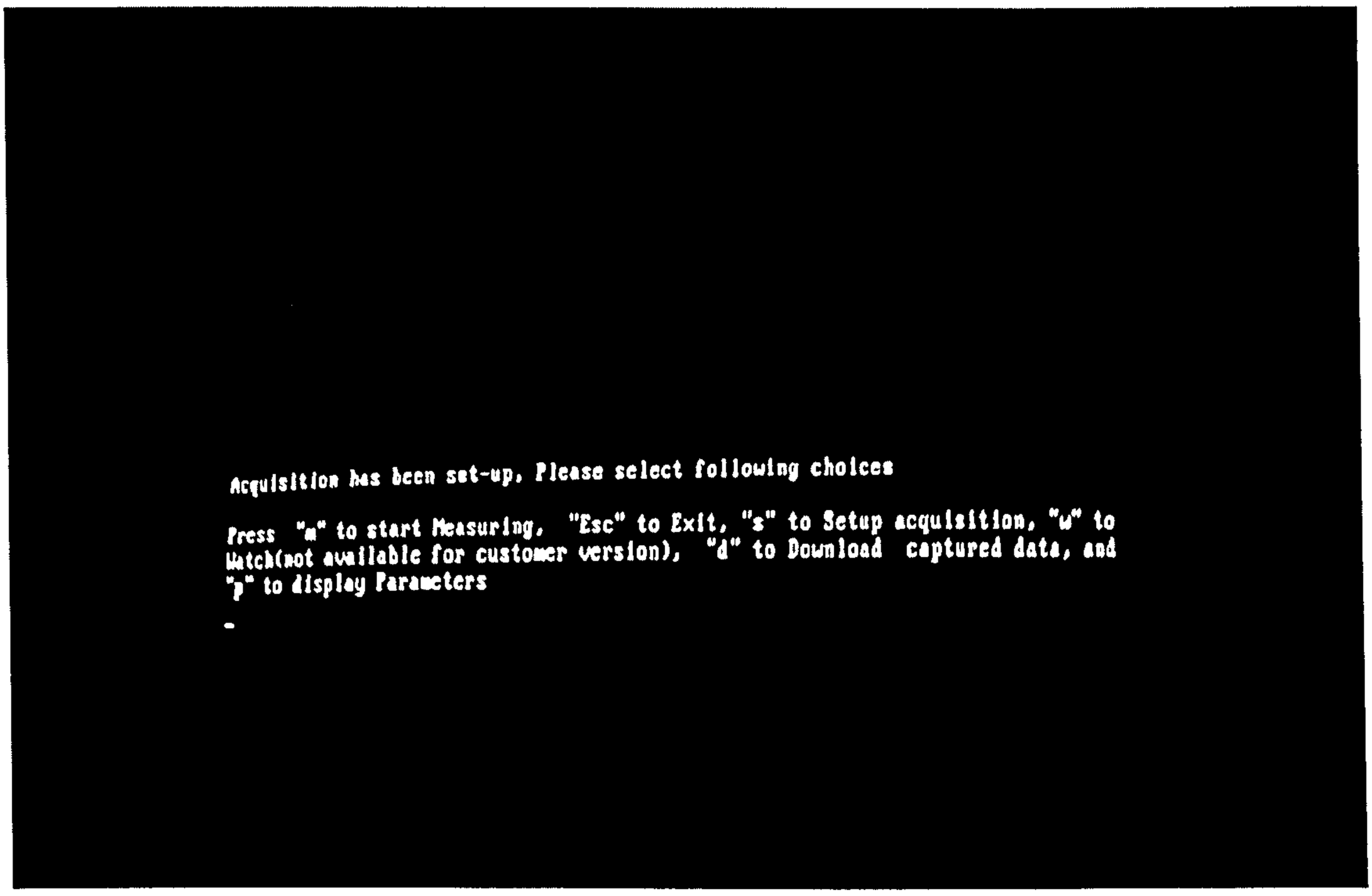


Fig. 6.2: Display after "Set-up"

To reset the RAU, the user can press "M" key (stands for "Measurement starts") at any time and the PC will send a packet to the RAU with a "Reset" command as shown in Fig.4.46. After that, the PC will display as shown in Fig.6.3.

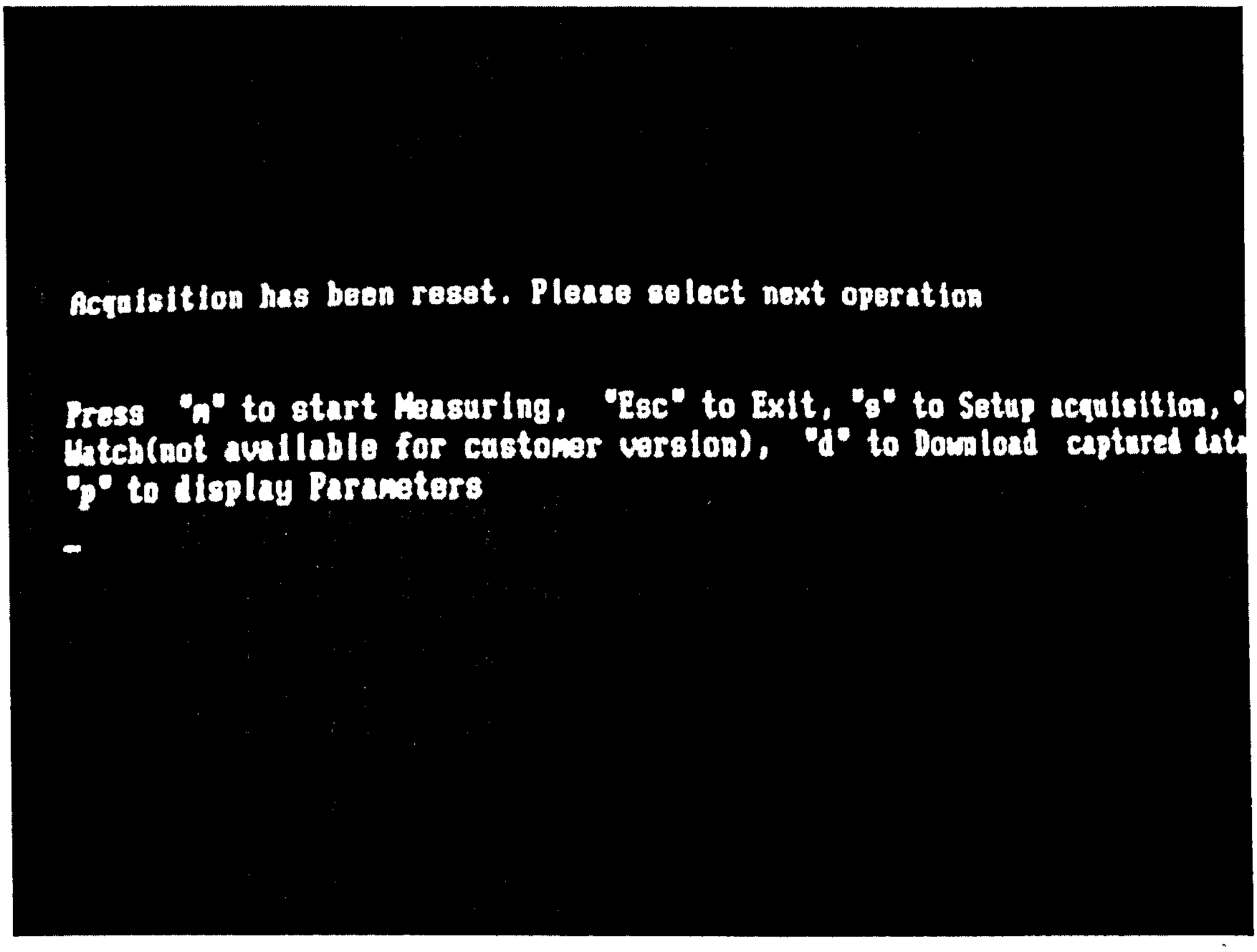


Fig. 6.3: Display after "Reset"

To monitor the state of the RAU, the user can press "P" (stands for "Parameters display") and the PC will send a packet to RAU with a "Read parameters" command. On receiving this packet, the RAU will continuously send data packets to the PC with the states information. The PC keeps receiving these data packets and continuously updates the display. Fig.6.4 shows the display of this operation.

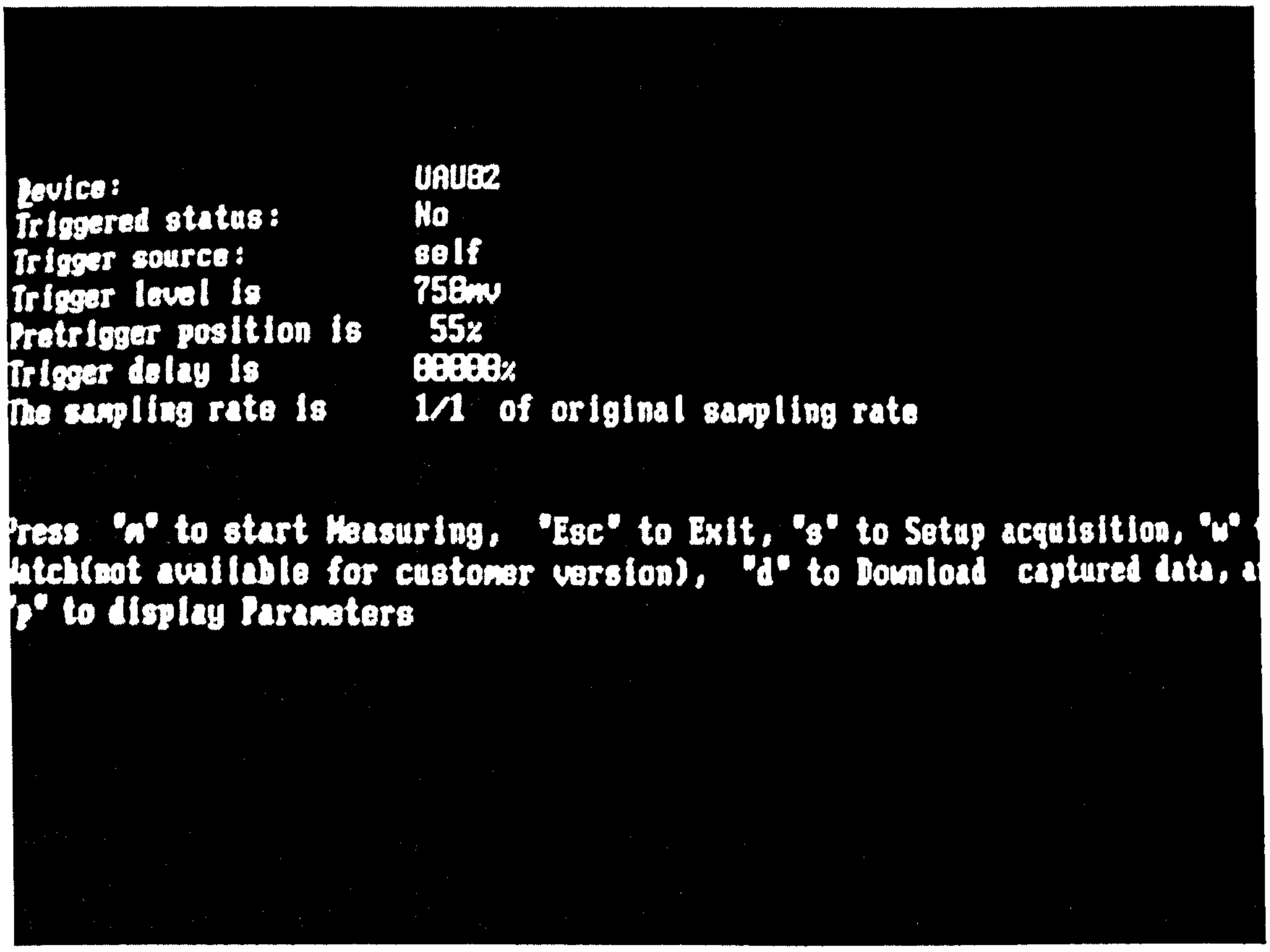


Fig. 6.4: Display of RAU's states

By watching the above display, the user can monitor the trigger status of the RAU. Once it has been triggered, the "trigger status" will be changed to "Yes".

To read "Real Data", the user can press the "W" key (Stands for "Watch signal"), and the PC will send a data packet to the RAU with a "Read Real Data" command. After receiving this command, the RAU sends "Real Data" to the PC continuously. The PC will keep displaying the received "Real Data" in a waveform as shown in Fig.4.25

Once the RAU is triggered, the user can download the captured data from the RAU. For this operation, the user can press "D" (stands for "Download"). The PC sends the command to the RAU asking it to send back the 512k of captured data. The PC also

gives a prompt to the user for the file name, in which the downloaded data will be stored. During the period of downloading, the program displays the process in percentage. Fig.6.5 illustrates the process of the data being saved to the file "Example.DAT".

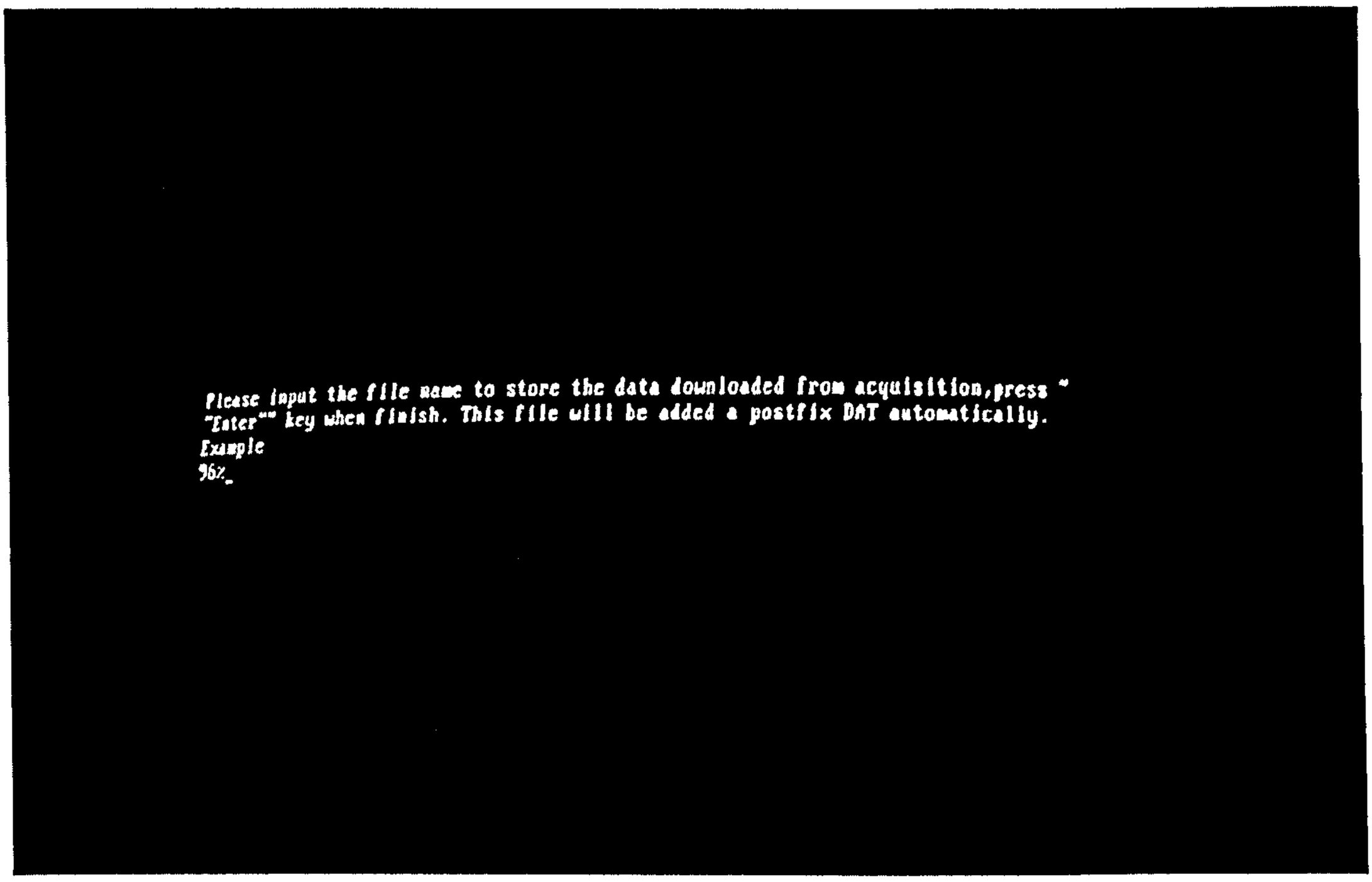


Fig. 6.5: Display during download

When the 512k data have been totally downloaded, the program will prompt the user to select next operation as shown in Fig.6.6.

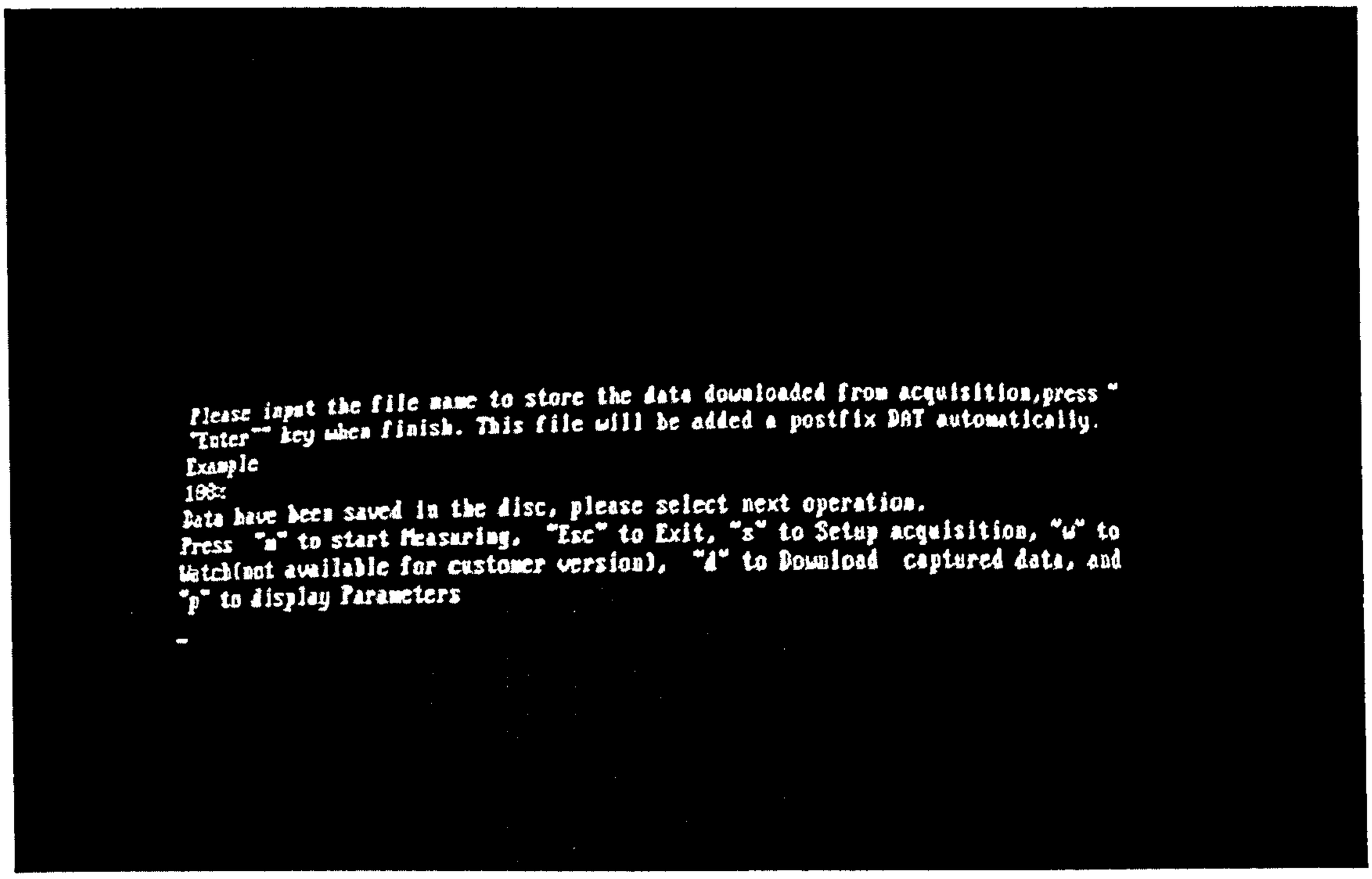


Fig. 6.6: Display after download

6.2 Flow chart of the PC software and the explanations for it

The main program continuously checks the "keyboard" in every loop. This allows the user to be able to input a command at any time. In every loop of the main routine, the PC runs in a certain operation mode. There are 6 different operation modes in this program:

1) Watching Mode (display the Real Data)
2) Download mode
3) Set-up mode
4) Monitor mode (display the RAU's parameters)
5) Reset mode
6) Idle mode (no action taken)

The initial operational mode is idle mode. When the user presses a different key, the program will switch to the respective mode, e.g. "S" key turns the program into "Set-up" mode, "D" key to "Download mode" and so on. Different operational modes cause the program to run along different routes in the main loop as shown in Fig.6.8. Apart from "Idle mode", there are 5 operational modes to be processed in this main routine, and the program treats them in different ways. "Set-up" and "Reset" operations should be implemented just once after the appropriate key input, thus at the end of these operations the program switches the operational mode to "Idle", in order to avoid implement these operations again in the next loop. For "Real Data" and "Monitor" modes, the program should operate in a continuous loop until other input key is asserted. Thus, those modes can only be changed by "Key processing". For a "Download" operation, it should end when 512k bytes data have been stored in the disk. Thus, the program switches the "Download" mode to "Idle" mode automatically when 512k data are received. The flow chart of the main routine is shown Fig.6.7.

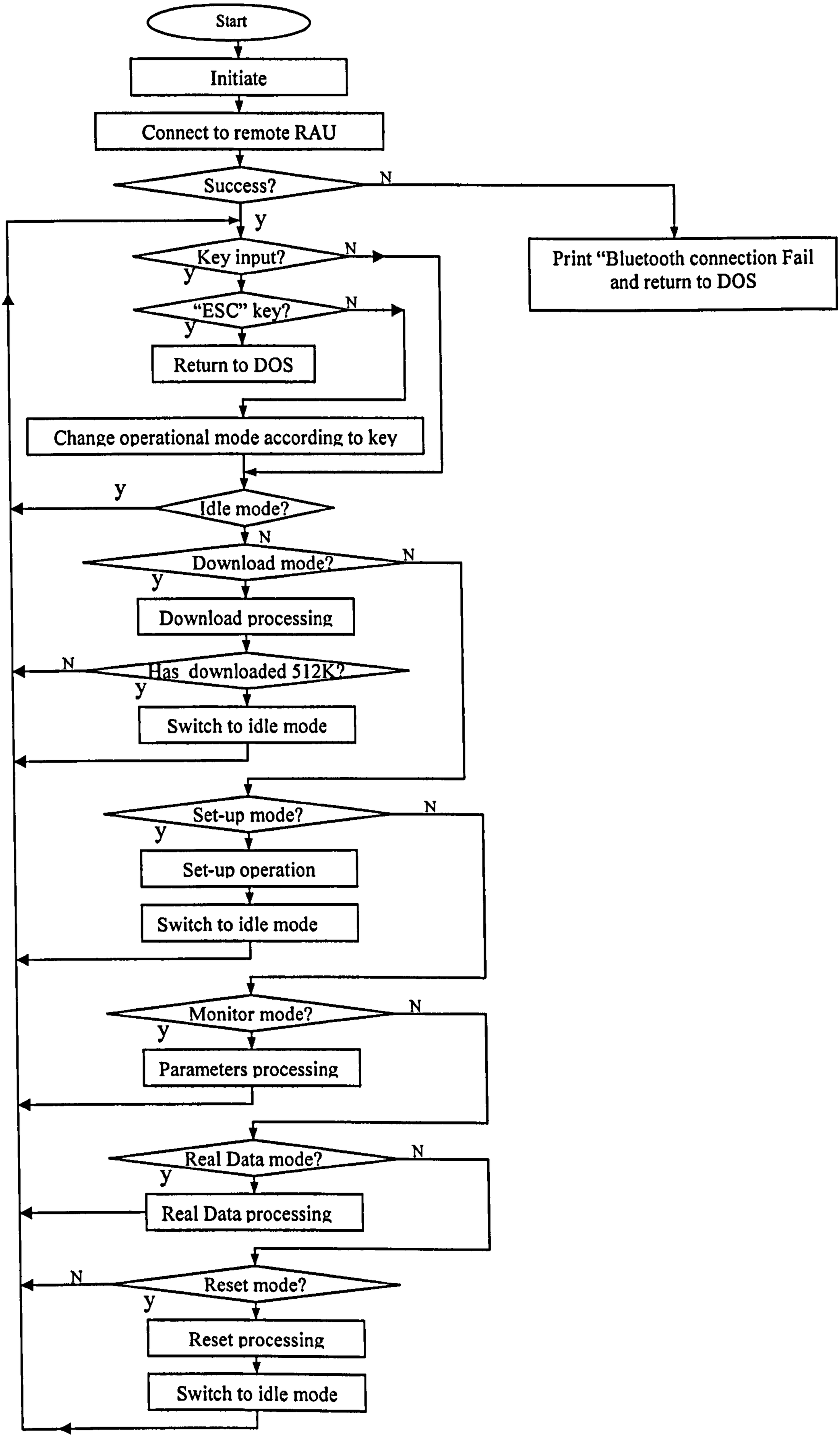


Fig. 6.7: Main routine flow chart

There are 5 processes in this program respectively for "Set-up", "Download", "Monitor", "Real Data" and "Reset" operations. In the "Set-up" operation, the program prompts the user to input all the parameters and then sends them to a remote RAU with a "Set-up" command. In "Reset" operation, the program sends a data packet to RAU with the "Reset" command.

The "Monitor", "Download" and "Real Data" operations are similar. Fig.6.8 shows the flow chart of "Real Data" processing as an example. All the three operations are based on the same method but the only difference between each these three operations is that for "Real Data" operation, the program displays the received data packets in a waveform, while for the "monitor" operation, the program displays the received data in text and for the "Download" operation, the program writes the received data packets to the designated file.

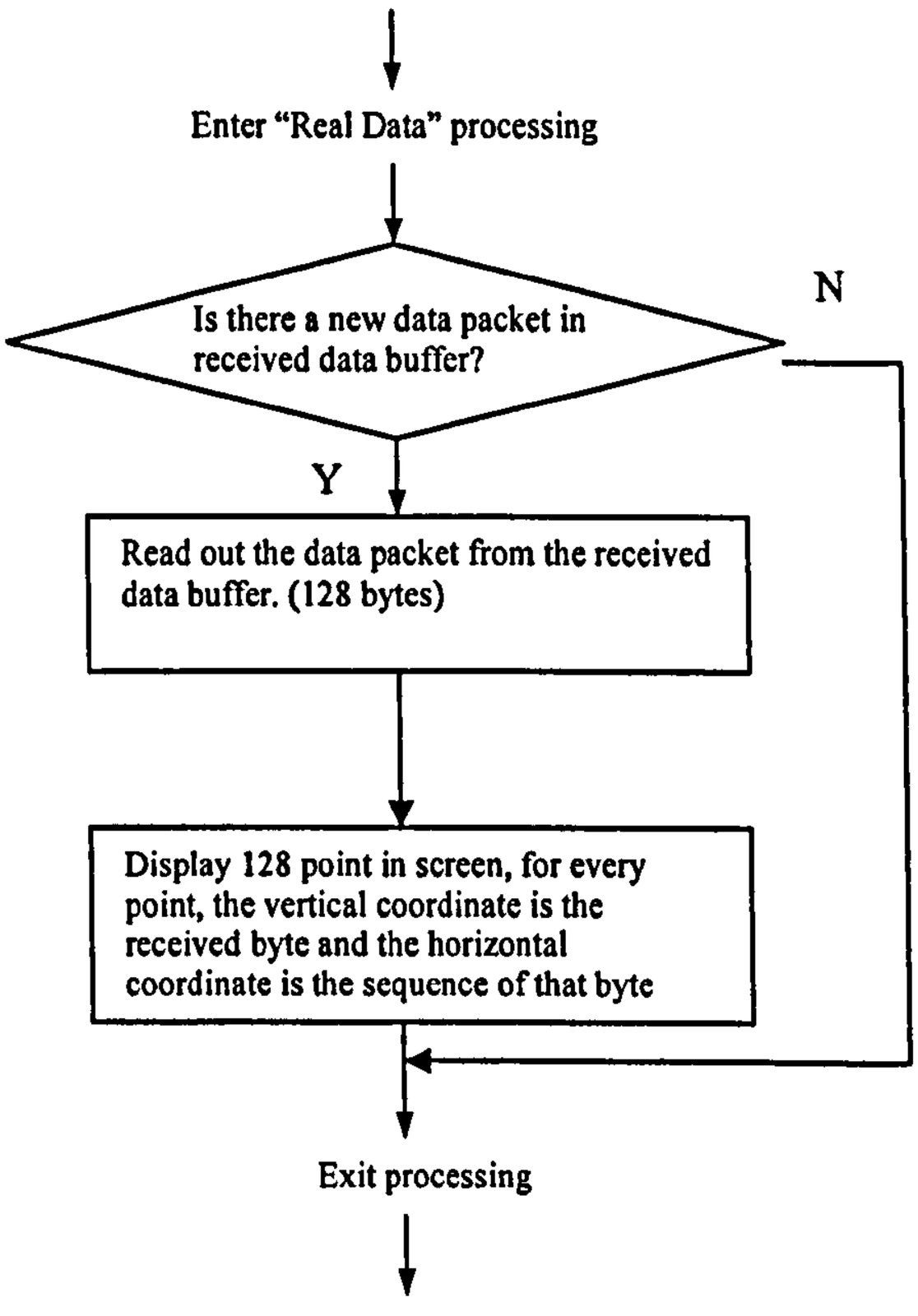


Fig. 6.8: Flow chart of "Real Data" processing

The "received data buffer" in the above flow chart is a 16k data area built-in to the "data paragraph" of the program. It is configured as a first-in-first-out buffer. Data receiving subroutine reads data from a serial port and writes the received data into this "received data buffer", while the processing routine reads the data from the buffer.

6.3 Supplementary explanation for serial data communication

In this program, the baud rate of the serial port of the PC is configured to 115200 bps. The receiving subroutine and sending subroutine execute the serial communication in this program. For a sending operation, the main routine writes the data into the sending buffer, the sending subroutine will encode them into a data packet and send them.

The receiving subroutine is an interruption service routine running in interruption mode. After receiving a data packet, it writes the received data into different data buffers according to the "data type" indication in that received data packet. There are 3 data buffers in this program: "Real Data" data buffer, "Download" data buffer and "Parameters" data buffer, every buffer has 16k size. These buffers are designed to avoid missing byte(s) when the CPU is running other tasks. Even if the main routine did not read out the data packet on time, the new received data can be buffered for a while and read out later. In fact, there are also another two buffers in the PC system, the receiving queue in hardware and the receiving buffer in Windows XP or Windows 2000 operation system. All of them are designed to guarantee the integrity of the data received at the serial port.

Although this program runs in a DOS environment, it does not run in real DOS environment but runs as a Virtual DOS machine, which is controlled by Windows 2000 or WindowXP

From Window 2000, the Windows Operation System does not allow users programs to control the hardware even in its DOS environment. All the write operations to the serial port do not really act on the hardware but are taken over by the Windows system. Similarly, the read operation on the serial port does not act on the real hardware but read from the mapped port built by the Windows system. This mapped

port is linked to a serial data buffer. When the user's program implements a reading operation from a serial port, it actually reads the data from that buffer.

Chapter 7 Results and discussions

Up to now, the whole "Wireless Digital EMI measurement System" has been presented. Each part of this system has been fully tested and some test results have been presented before in their related chapters. This chapter is dedicated to the test of the whole system and discussions of the test results.

Since this Wireless Digital EMI measurement system will be installed in a harsh EMI environment (the switchyard), the EMC test for this system is important. This chapter reports the system test under the EMI conditions in the laboratory and substation.

7.1 EMC test in laboratory

7.1.1 Facilities to emulate EMI environment in laboratories

In fact, all new equipment to be used in substations face such kinds of EMC problems. For such equipments it would be ideal to have a test under an equivalent EMI condition in the laboratory and evaluate its EMI immunity performance before it is actually installed in the substation. For this purpose, the EMC group at Strathclyde University has designed "Portable Electric and Magnetic Field" generators, which can roughly emulate the substations EMI environment in a laboratory. This allows us to evaluate the EMC characteristics of electric devices before they are installed in a substation [103].

There are two generators in this test system: an E-field (Electric field) generator and H-field (Magnetic field) generator. The E-field generator is designed to give a nominal output of 250kV/m (1 meter away from the generator), with a ringing frequency of 600kHz. The generator generates E-field every 100ms and every E-field pulse last 20 microseconds.

The H-field generator is designed to produce 50 A/m with a frequency range between 20MHz and 50MHz. This is also a pulsed output. The H-field output has 20 microseconds duration and 300 milliseconds interval.

These generators are designed to implement the EMI test standard of IEC 61000-4-10 [104]. This in-house system has been reported at various conferences [30, 31, 32]

Apart from the high-frequency E-field and H-field, 50Hz E-field and H-field are also part of the EMI in substations. 50Hz E-field is not crucial for most electric equipment. For a complete environmental emulation, a 50Hz H-field test was included. 50Hz H-field is generated by a cable loop laid on the floor, carrying 50Hz AC current. The equipment to be tested was placed in the middle of the cable loop. By changing the current magnitude through the cable, different H-field amplitudes can be generated there.

Fig.7.1 and Fig.7.2 show these generators and the EMI immunity test area.

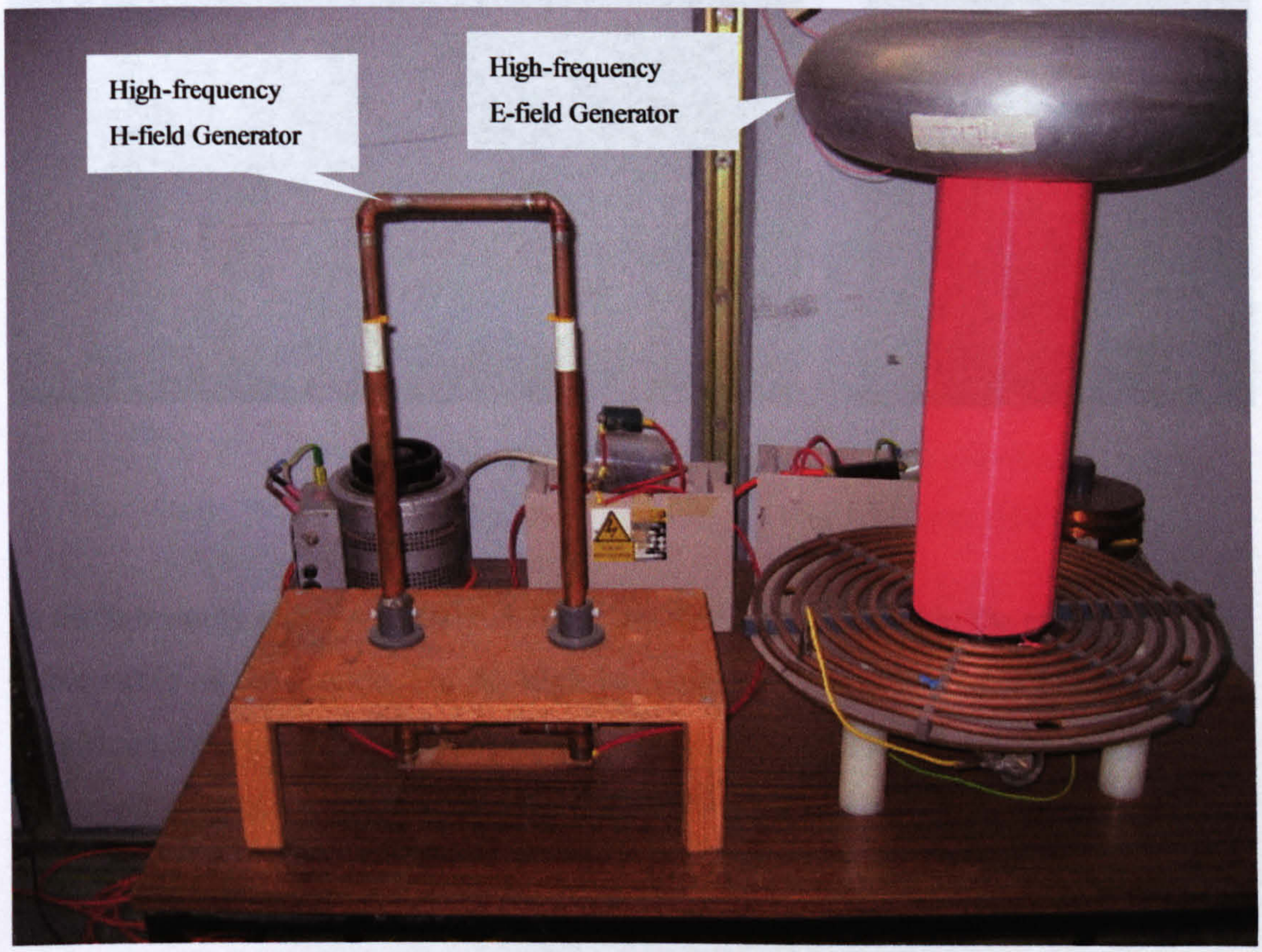


Fig. 7.1: High frequency H-field generator and high frequency E-field generator

In the left hand of the Fig.7.1, there is a H-field generator, which is built-up by a copper slider and LC circuit. In the right hand of the figure, there is an E-field generator, which is built-up by a Tesla coil and other components.

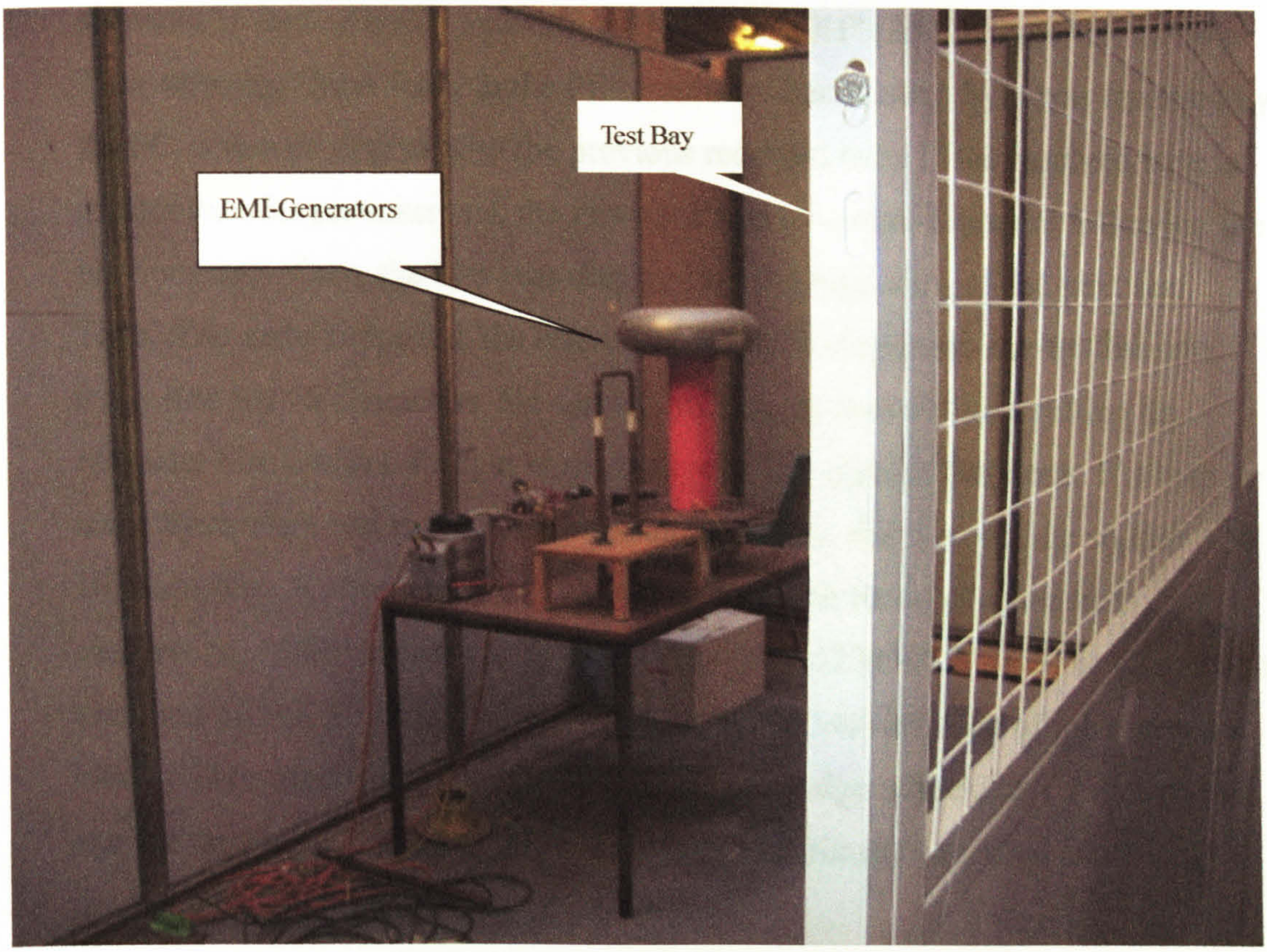


Fig. 7.2: Test set-up

In the immunity test, for a 50Hz H-field, the RAU was located in the centre of the cable circle on the ground. For the high frequency E-field and H-field tests, the RAU was located on a stand. By changing the distance between RAU and the generators, the amplitudes of the electromagnetic field around the RAU can be changed.

7.1.2 EMC test methodology in laboratory

EMI affects this wireless measurement system by radiated wave in two aspects: Interfering with the wireless communication and interfering with the RAU circuit. As both the wireless communication signal and radiated EMI signal are electromagnetic wave and transmitted in a same space, the wireless communication is more sensitive to a radiated signal. The EMI tests were, therefore arranged, as follow:

1) Communication test: Let the RAU send a certain data sequence to the PC under different EMI conditions. The PC verifies and displays these data in the PC. If any error is present, the PC will record that error and give an alarm. The data

sequence is formed by 10 bytes from "30H" to "39H" (ASCII code "0" to "9"). They were sent from RAU to the PC circularly. Each time a byte was received by the PC, it was compared with the previous received byte. If the received byte is greater than the previous one, the new-received byte was displayed following the previous one, if not, the byte was displayed at the beginning of the next line. Thus, if no error happened, the correct data will be displayed line-by-line and every line has 10 characters. On screen, the display looked like a rolling-up character block with a straight vertical edge on the right of the block. If a byte or some bytes were lost in the communication process, that line will be shorter than 10 characters. A wrong byte will also make that line break into two lines. For example, if "34H" is changed to "36H", the line "123456789" will be changed to two lines of "1236" and "56789". In that case, the vertical edge of the character block will be zigzagged. By simply watching the edge of the data block, people can see the error situation quickly. This is an experimental method and widely used in telecommunication engineering.

2) Circuit test 1: A zero input was given to RAU, the RAU should convert the analogue input signal into digital code "80H". Under different EMI conditions the output of the RAU was observed in the PC by displaying the "Real Data". Meanwhile, the program would check every received "Real Data". If it deviates from "80H", the process is stopped and the wrong data is recorded. A "Zero" input can be made by connecting the input port to "Ground" via a 50Ω terminator. In this case, any interference affecting the RAU circuit would be added to the "Zero" output.

3) Circuit test 2: Since in item 2, "Real Data" comes from the A/D directly, it does not check the memory circuit. In this item, the trigger-level is set to "0", letting RAU captured the input "zero" signal. Then, the PC downloads the data and checks them.

4) System test: Use a sensor to measure the EMI signal. The output of the sensor is connected to the RAU and DSO simultaneously. Compare the measurement results form the RAU and DSO. In this test, the RAU is placed near to the EMI

generators whereas DSO is placed outside of the screened test bay to avoid the EMI effects. Fig.7.3 illustrates the layout.

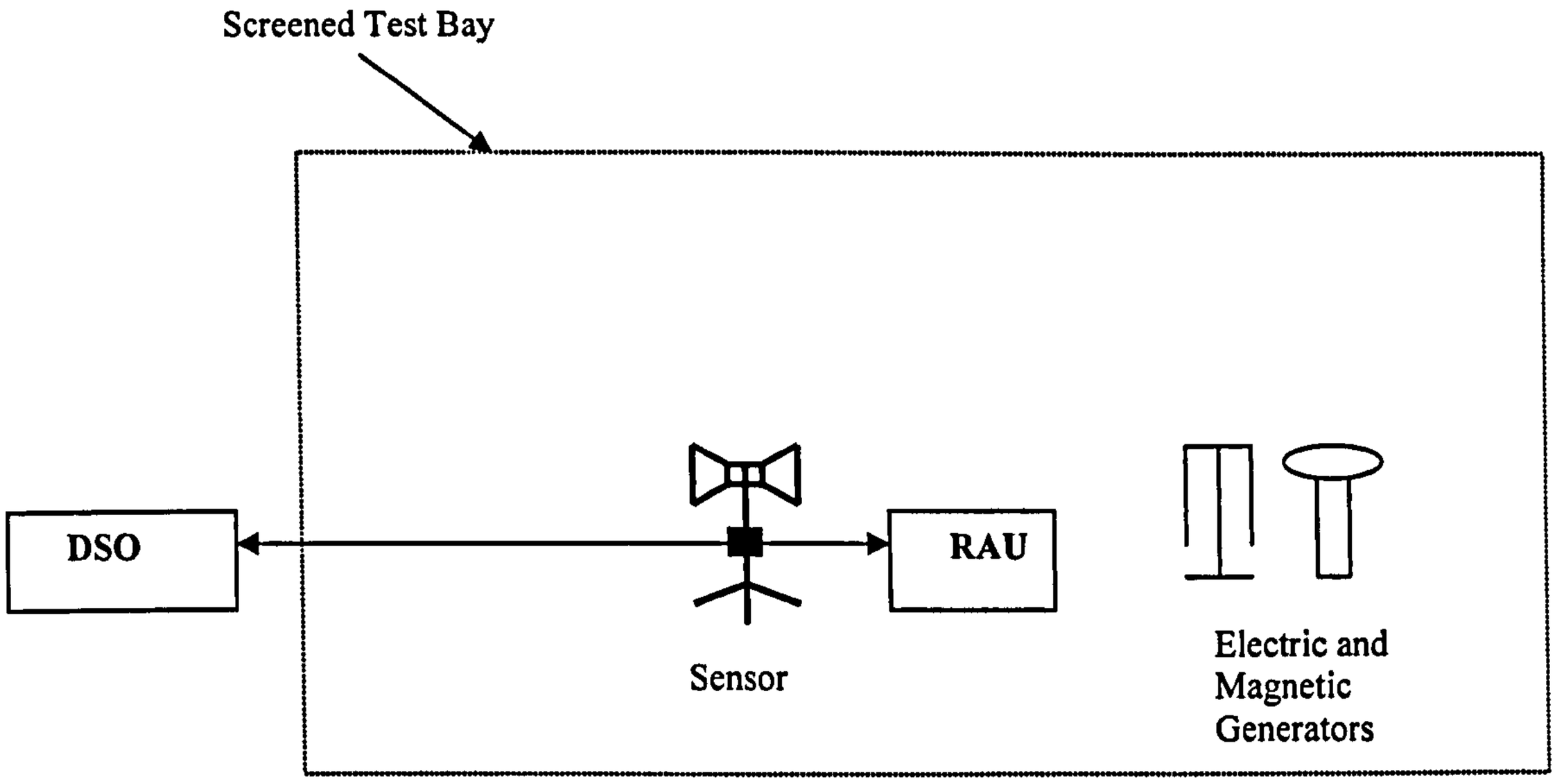


Fig. 7.3: EMI test in laboratory with a sensor

The next section gives the test results of above items with different EMI conditions.

7.1.3 The EMC test results in laboratory and the analysis

1) The test with 50Hz H-field

Table 7.1: Test result with 50Hz H-field

Items / Amplitude	Communication Test (3 times, 2 hours each time)	Circuit Test 1 Real Data (3 times, 1 hour each time)	Circuit Test 2 Download Data (5 times, each time 512 kB)
0 A/m (Ampere/Meter)	Correct (41.05kbps)	Correct	Correct
50 A/m	Correct (41.05kbps)	Correct	Correct
100 A/m	Correct (41.05kbps)	Correct	Correct
150A/m	Correct (38.91kbps)	Correct	Correct

The results in Table 7.1 reveal that up to 150A/m amplitude, the 50Hz H-field does not affect the integrity and correctness of the communicated data. The 50Hz H-field just changed the communication speed at 150A/m. As shown in Table 7.1, when the 50 Hz H-field increased to 150A/m, the actual data baud rate dropped to 38.91 kbps from 41.05 kbps. This can be explained as follows:

We assume that the 50Hz H-field acted on the RF channel and created error bits in the transmitted data. Bluetooth Devices can check this error by a verification code. When the receiver finds an error in the received packet, it will ask the transmitter to send that packet again. Bluetooth devices also implement CODDR (Channel Quality Driven Data Rate). If the error rate is so high that retransmission takes place too often, the transmitter will add FEC (Forward Error Correction) code in every packet. Both the repeat action and adding FEC code would slow the actual communication speed. That is to say, when the EMI environment becomes harsh, the actual data speed of the Bluetooth communication will be reduced, but the data correctness and integrity are guaranteed [105]. The data protection mechanism has been introduced earlier in chapter 2. It appears that, when the 50Hz H-field increased to 150A/m, the Bluetooth devices took more time to implement data protection protocol. However, this will not affect the data communication in this system. According to the previous experience of the stuff in EMC group, the maximum 50Hz H-field in substations is 100A/m.

2) The test with high frequency E-field

Table 7.2: EMC test with high-frequency E-field

Items / Amplitude	Communication Test (3 times, 2 hours every time)	Circuit Test 1 Real Data (3 times, 1 hours every time)	Circuit Test 2 Download Data (5 time, every time 512 kB)
0 V/m	Correct (41.05kbps)	Correct	Correct
60kV/m	Correct (41.05kbps)	Correct	Correct
250 kV/m	Correct (41.05kbps)	Correct	Correct

The above result revealed that the high frequency E-field interference does not destroy the data acquisition system, neither spoiling the data communication nor the electric circuit of the RAU. Even if the high frequency E-field may destroy some communicated bytes, the Bluetooth protection mechanism would operate with them, so the error was not presented in the test results.

3) Test with high frequency H-field interference

The H-field generator generates oscillatory high frequency H-field pulses with a 2 microseconds duration, 300ms interval and amplitude of up to 50A/m. Table 7.3 shows the test results:

Table 7.3: Test result with high frequency H-field interference

Items / Amplitude	Communication Test (3 times, 2 hours each time)	Real Data (3 times, 1 hour each time)	Download Data (5 times, each time 512 kB)
0 A/m	Correct (41.05kbps)	Correct	Correct
12.5 A/m	Correct (41.05kbps)	Correct	Correct
50 A/m	Correct (41.05kbps)	Correct	Correct

The test results show that the high-frequency H-field interference did not affect the data acquisition system. Although the high frequency H-field may interfere with the wireless transmission, the Bluetooth data protection mechanism can recover the spoiled data and ensure the integrity and correctness of that data, as had been presented previously.

4) The test with the sensor under the full EMI environment

This test is designed to acquire the signal from a high frequency H-field sensor using the RAU while high frequency E-field and H-field generators are working. The test

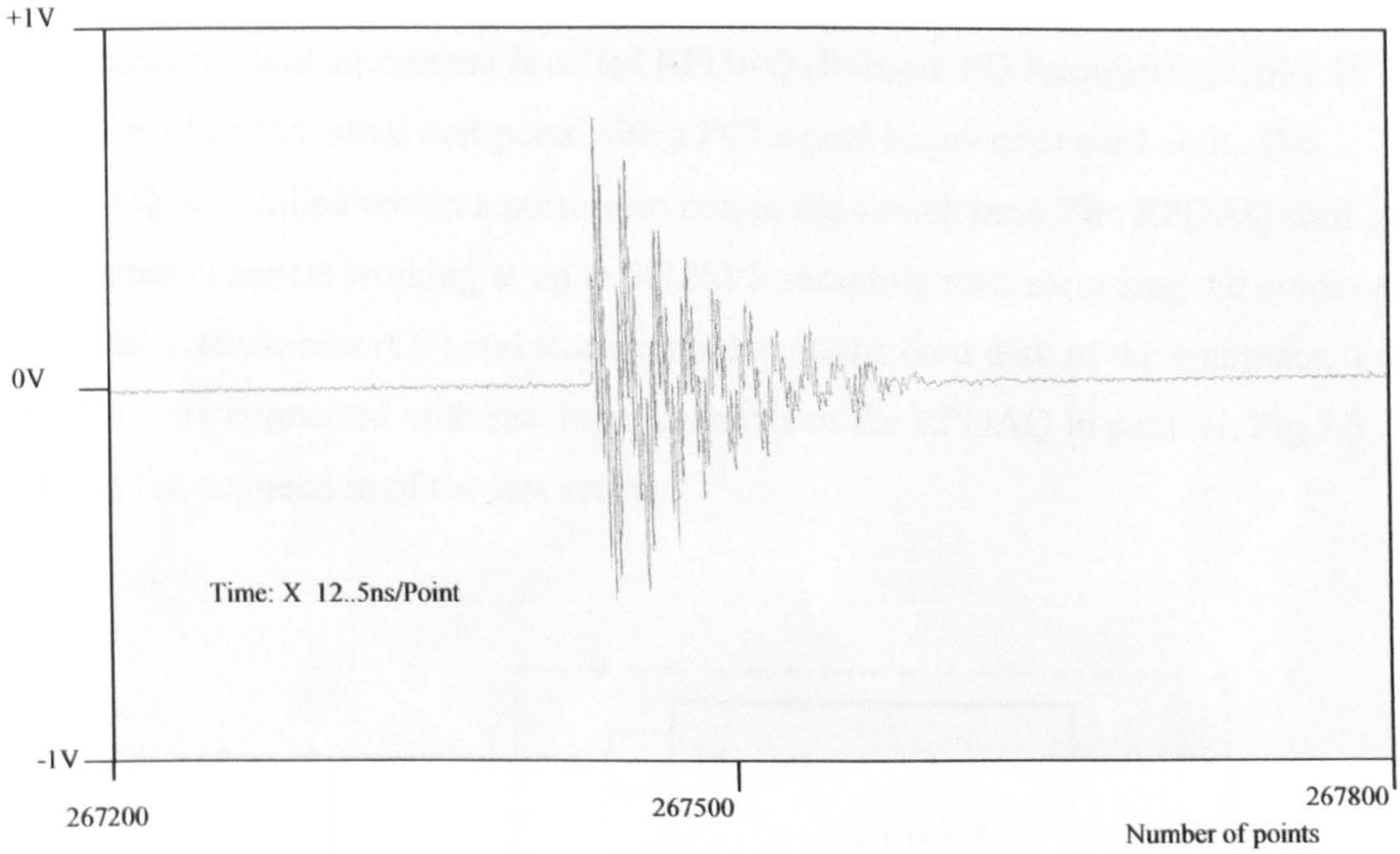


Fig. 7.4: Waveform of high-frequency H-field made by in-house generator

method has been described before in Fig.7.3. Fig.7.4 shows the test result, which is the waveform from the sensor and recorded by the RAU. It is exactly the same as the waveform recorded by the DSO.

7.2 Acquisition test and distance test in substation

The test in the substation was conducted for two purposes: testing the EMC immunity of the Wireless Digital EMI Measurement System in the environment of substation and testing the wireless communication range in the substation.

7.2.1 Measurement set-up

This site test was arranged in June, July and August of 2004 in Wishaw (Scotland) substation. Due to the radiated EMI, measurement was not available at that time, the test was arranged to make a conducted EMI measurement. At Wishaw substation a

measurement system to monitor a current transformer output has been permanently installed and is always available. Therefore, the wireless measurement system can work in parallel with the permanent measurement system and their measurement results can be compared.

The measurement equipment is called RPDAQ (Remote PD Acquisition Unit). It consists of an industrial computer with a PCI signal acquisition card on it. The RPDAQ is installed within a protection box in the switchyard. The RPDAQ card has two input channels working at up to 50MSPS sampling rate, recording the output of a Current Transformer (CT) and storing the data in the hard disk of the computer. Two RAUs were connected with two input channels of the RPDAQ in parallel. Fig.7.5 shows the connection of the test set-up.

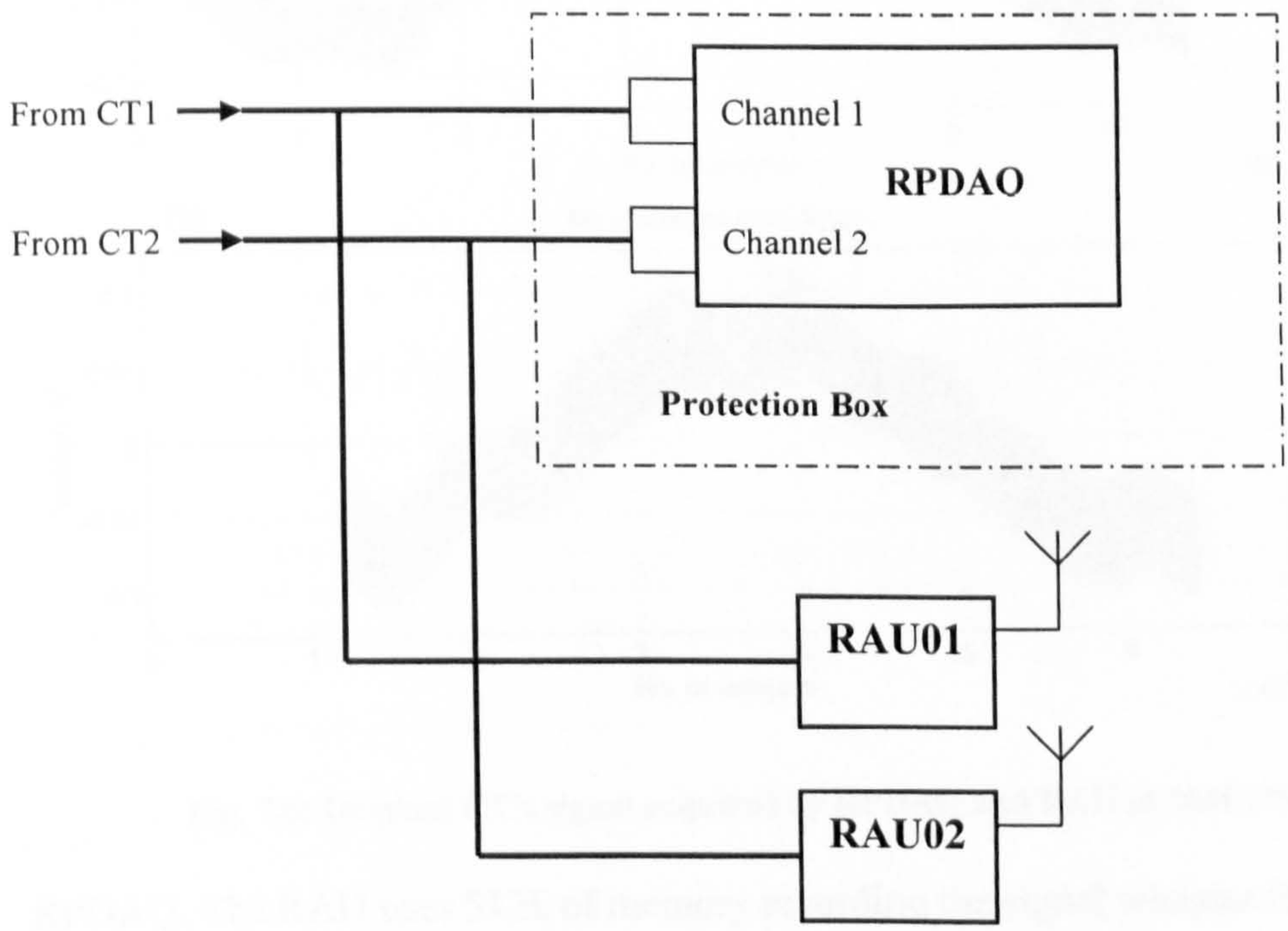


Fig. 7.5: Connection of the test set-up

In Fig.7.5, the output of the CT is a bi-polar voltage signal, which represents the current through the power transmission line. The RAUs and RPDAQ acquire the CT's signal simultaneously. The CT's output has a high frequency signal

superimposed on 50Hz. The signal of the CT is a repetitive signal. But unlike the transient signal, it cannot provide single synchronization to both RAU and RPDAQ. Hence, the RAU and RPDAQ may record a different period (20ms per period). However, since the current signal is repetitive, every period has a similar shape and the acquired results of RAU and RPDAQ should still be comparable. Of course, the details of the signal may be slightly different as shown in Fig.7.6.

Fig.7.6 shows the comparison between the waveforms acquired by the RAU and

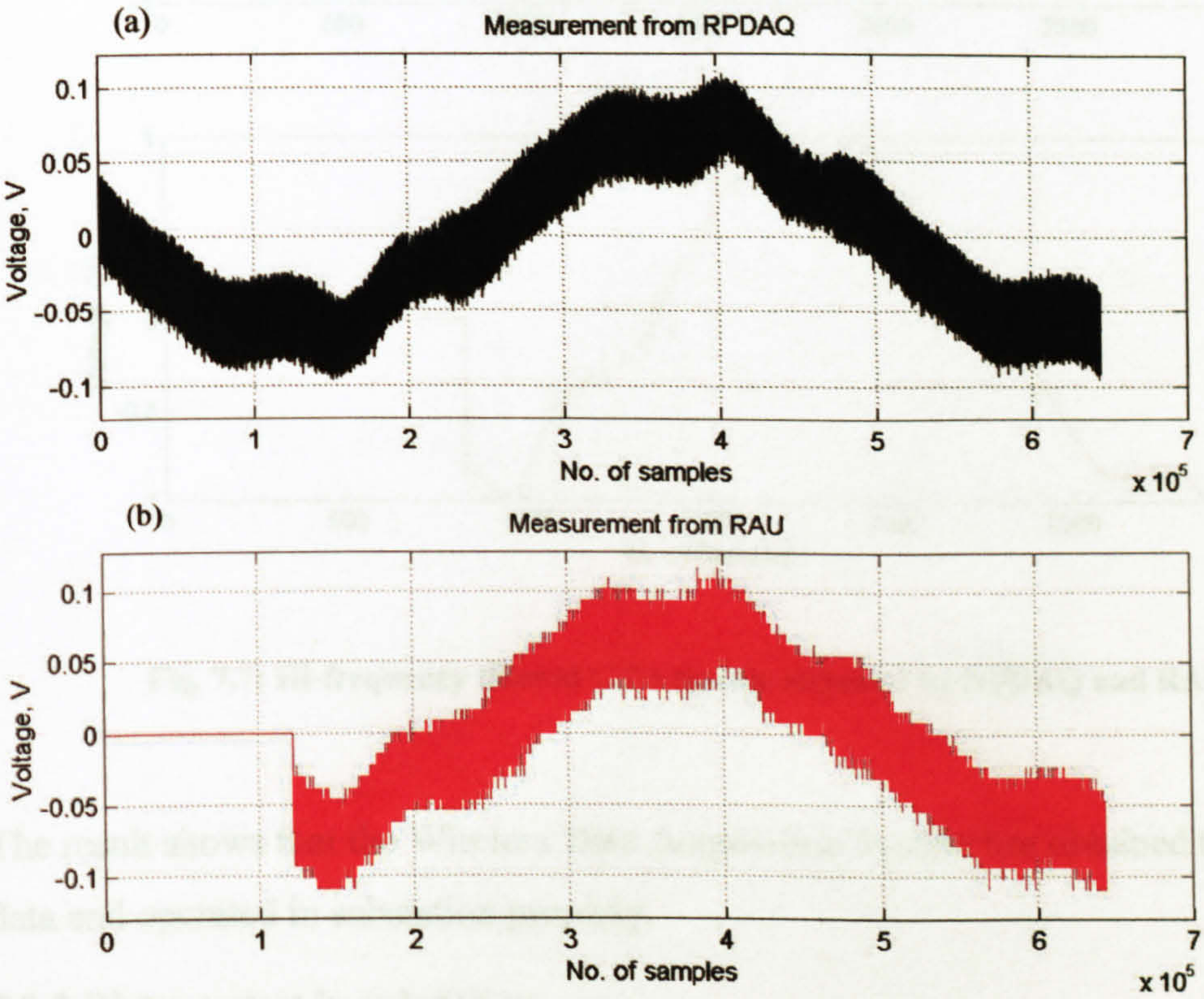


Fig. 7.6: Original CT's signal acquired by RPDAQ and RAU at 20MSPS

RPDAQ. The RAU uses 512k of memory recording the signal whereas the RPDAQ uses a hard disk. Consequently, the RAU's record is much shorter than the RPDAQ's. The CT's output signal consists of a low frequency signal and a high frequency signal. The low frequency signal has 300mV amplitude and is related to the 50Hz alternating power frequency voltage. The high frequency signal has a maximum of 50mV amplitude and is caused by different interferences on the transmission lines. The acquired original signal is given in Fig.7.6, which is a composite signal with the high frequency signal carried on the 50Hz signal. The high frequency filtered

waveforms are also given below in Fig.7.7, in which the high frequency components have been removed using MatLab.

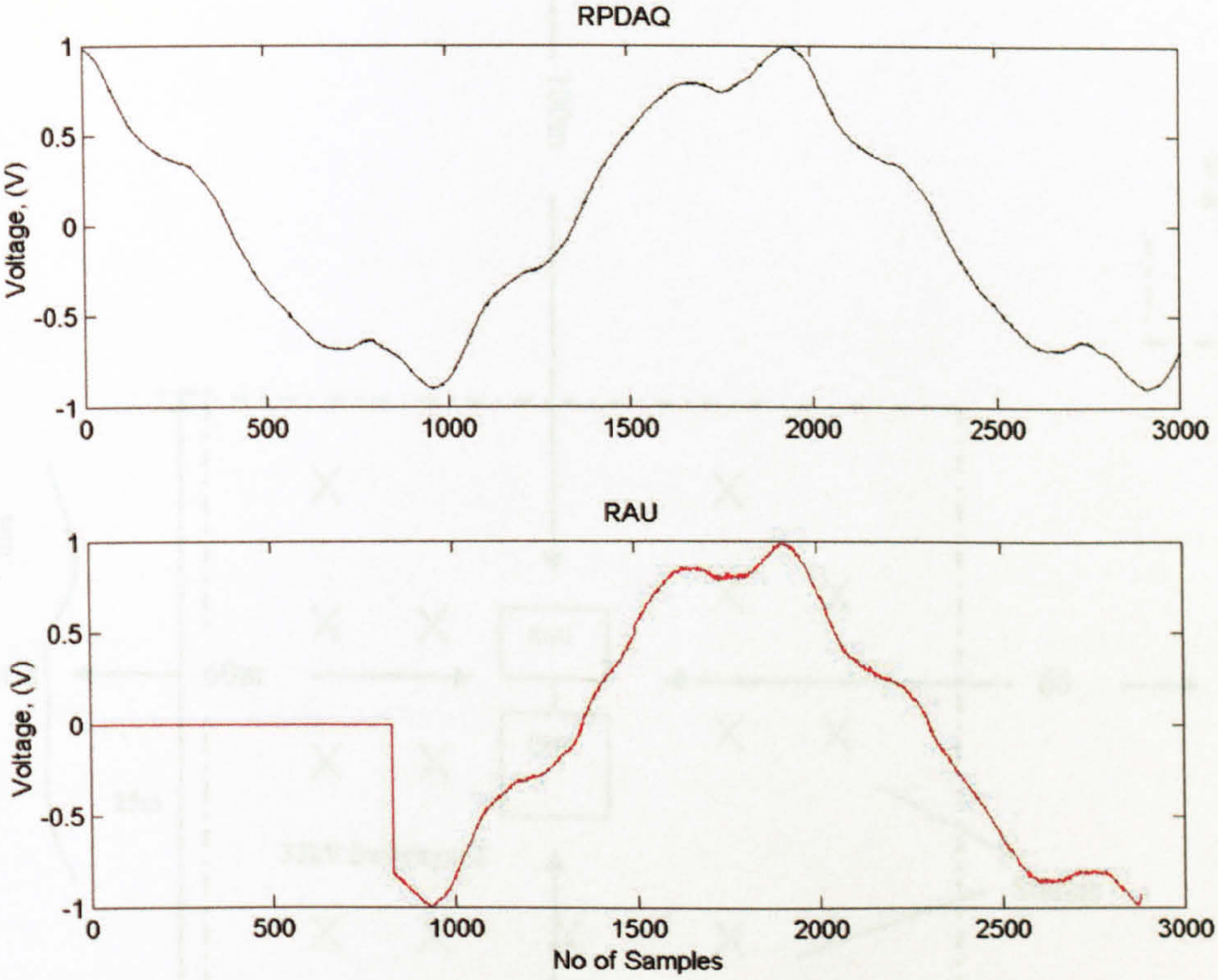


Fig. 7.7: Hi-frequency filtered CT's signals acquired by RPDAQ and RAU

The result shows that the Wireless Data Acquisition System has obtained the correct data and operated in substation properly.

7.2.2 Distance test in substation

In the distance test, a RAU was placed within the switchyard. The laptop and its attached master modem were moved away from RAUs until the wireless signal disappeared. The laptop and modem were moved back towards the RAU and stopped at the point when the wireless signal was just recovered. At that point, the data acquisition operations were repeated to see if the result was correct. If data communication had no problem at that point, the distance from this point to RAU is the farthest wireless communication distance in that direction. The test was repeated at four points (point 1~4 as shown in Fig.7.8) in four different directions. Fig.7.8 shows a schematic of the terrain of the test field.

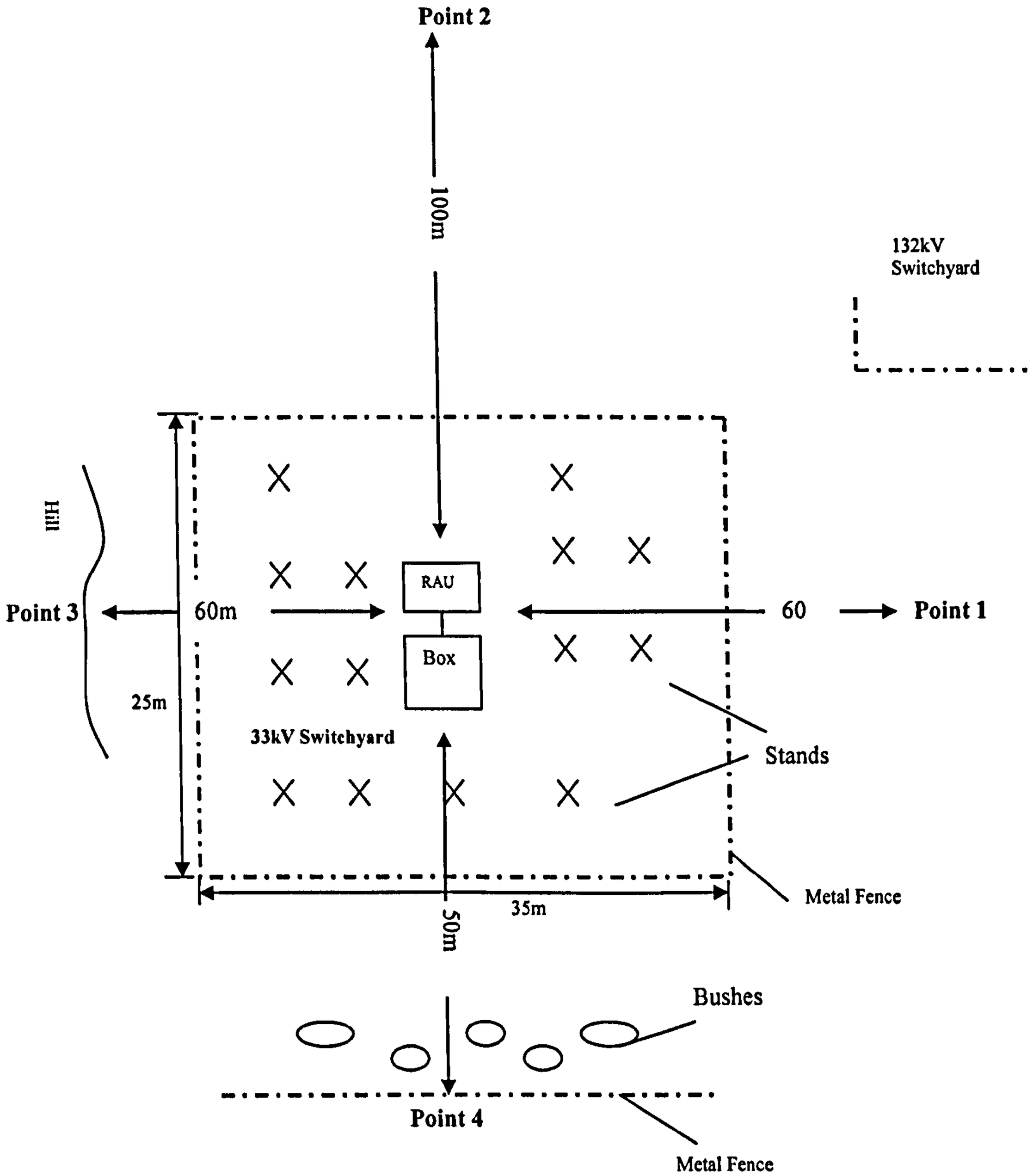


Fig. 7.8: Schematic for distance test in substation

The actual size of the switchyard is 35 meters long by 25 meters wide. The test reveals that without further obstacles outside the switchyard, the wireless communication range can reach at least 60 meters. Of course, different substations

have different layouts and the communication distance will be varied in different in each case. This test result can be used as a reference for future work.

Chapter 8 Conclusions and recommendations for future development

8.1 New features of this EMI measurement system: Wireless and Digital

This thesis described the design and implement action of a Wireless Linked Distributed Data Acquisition System for EMI measurement in substations. The system consists of 3 parts: RAU, Wireless Network and PC software.

The motivation for this project was to solve the "fibre" problem in the EMI measurement technology. As described before, the fibre link creates considerable difficulties for the EMI measurement in substations. Obviously a wireless solution can solve this problem and would be the most convenient. Replacing a physical link with a wireless link has become common in recent years and is normally easy to implement. However, in this case, it is impossible to simply replace the fibre with a wireless connection. The analogue signal transmitted by fibre has a wide bandwidth, which cannot be carried by an RF channel. Using an RF carrier to transmit a real time analogue signal would also be more sensitive to electro-magnetic interference. Fortunately, the measured signal is an intermittent transient signal and does not need to be transmitted in real time. This means that a digital system can deal with such a wireless transmission. In the front end, the transient signal is recognised and stored in the local memory and then transmitted to the remote PC. The transmission of the digital signal can be carried out at a slower speed, i.e. the digital system uses a narrow bandwidth RF channel and a long period to transmit a signal with wide bandwidth and short period. Modern wireless data communication technology also implements data protection strategy, which ensures the correctness and integrity of the communicated data even in a harsh EMI environment. The result of the project does not, therefore, simply replace fibre link with a wireless link, but also changes the analogue system to a digital system.

8.2 Development work

At the front end of this system, the RAU should have a data conversion function, a trigger function and a storage function as a digital oscilloscope does in the present Fibre Analogue EMI Measurement System. For this reason, in this project, the RAU is also termed as "Wireless Digital Oscilloscope". The RAU was the key device in this system and the development of the RAU was the most difficult work in the whole project, taking one and half years.

Compared with the development of the RAU, wireless communication network and PC software were easier. Roughly, in the whole development work, the RAU took 50% effort; PC-software took 15%; Communication Network took 15% and the system integration took the rest 20% as shown in Fig.8.1.

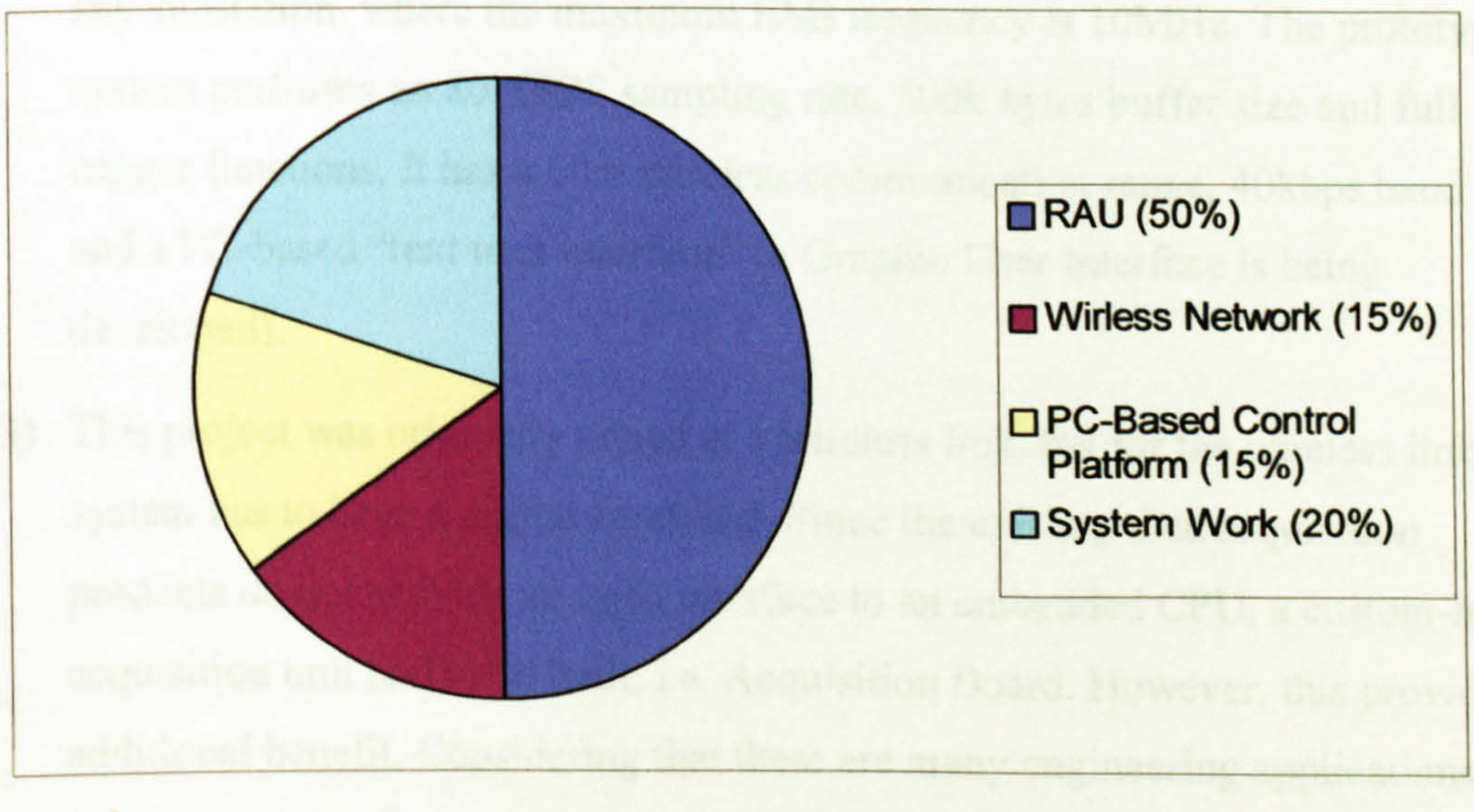


Fig. 8.1: Working load distribution of the whole project

In this project, the design combines both software and hardware, includes analogue and digital circuit designs. The system applies Embedded CPU, PLD and communication technologies. The development work has utilized several development tools: Protel PCB design Kit, Xilinx PLD development Kit, MCS-51 series micro-controller development Kit and IBM x86 assembly language development tool. It can be seen that this project is a complex, multidisciplinary project.

8.3 Achievements

In this project, a Wireless Digital EMI Measurement System has for the first time been created and used for EMI measurement in a substation. The main achievements obtained by the prototype system can be described in the following four points:

1) As a prototype design, this system is practical and verified the "Wireless and Digital" principles. It first realised a wireless link for the EMI measurement system in substations, which operators had been anticipating for many years. Based on the principles and structure of this prototype design, any future design can easily achieve better performances, such as a higher sampling rate, or larger memory size.

2) As actual equipment, the prototype system can be used for EMI measurements in any substation, where the maximum EMI frequency is 10MHz. The prototype system performs an 80MSPS sampling rate, 500k bytes buffer size and full trigger functions. It has a 60m wireless communication range, 40kbps baud rate and a PC-based "text user interface" (a Graphic User Interface is being developed).

3) This project was originally aimed at a wireless link, but for the wireless link, the system has to have a digital front-end. Since the existing data acquisition products do not provide an open interface to an embedded CPU, a custom-built acquisition unit had to be built, i.e. Acquisition Board. However, this provides an additional benefit. Considering that there are many engineering applications where acquiring fast transient signals with an embedded CPU is implemented, the Acquisition Board can be an independent product used for similar application. The design of acquisition board is applying an UK patent and will be synthesized into a single module. The application of this acquisition product will be presented in the later section on "Recommendations for future development".

4) During the project, Bluetooth Products have been introduced in substation engineering. This experience can be a reference for other similar applications, which intend to use Bluetooth products in substations.

As most R&D projects, this project achieves an innovation but not invention. Innovations do not create any new technology or material but they provide a new solution by a new combination of existing material and technologies.

8.4 Recommendations for future development

This project has developed a prototype "Wireless Digital EMI Measurement System". As a general prototype design, after a period of practical application, the prototype may need modification and an upgrade, i.e. further development. Such further developments usually modify a prototype design to have better performance and wider applications. Some recommendations for the development in the future are now outlined.

1) Power supply

As mentioned earlier in chapter 4, the RAU uses analogue power supply. An analogue power supply provides a high-quality power source, which is good for prototype design and commissioning work. However, an analogue-mode power supply always have lower conversion efficiency than a switched-mode power supply. In this battery-powered equipment, lower conversion efficiency means shorter battery duration. Thus, changing the analogue mode power supply to switched-mode will make the RAUs have a longer working duration with the same battery. The conversion efficiency of the power supply in this prototype design is less than 50%, whereas the switched-mode power supply can achieve 70-80%. The switch-mode power supply product should have 12V DC input and 5V, 3.3V –5V output, and such a module is a common product. However, comparing it with an analogue power supply, switched-mode power supplies always have bigger "ripple" noise. Also the switch-mode power supplies are more susceptible to interference. Thus the selected products should be carefully tested in the laboratory and the real environment. The prototype design has reserved a 16 pin plug and 4 way jumpers to change the on board power supply to an external one. Future development can take this plug connecting different switch-mode power supply products and test them in substations.

2) Second set of PCBs

In the prototype Acquisition Board and CPU board, commissioning circuits take more than half the PCB area. It is suggested that a second set of PCBs be produced, removing such commissioning circuits. Thus, the PCB size will be reduced. The prototype PCBs have some modifications, which are implemented by cutting some PCB traces and adding some jumper wires. In the second set of PCBs those modifications should be realized.

3) Consideration of lithium battery

For rechargeable-battery applications, lithium batteries are currently the best choice, if the price is irrelevant.

Lithium battery has larger capacity and less "memory effect", which allows users to recharge it at any convenient time.

4) Third set of PCBs

The design of the third set of PCBs may include the following 3 new functions:

a) Adjustable amplifier in forward channel

As mentioned before, this prototype RAU uses an external adjustable amplifier to adapt the measured signal to the input range. If possible, arranging an adjustable amplifier inside of RAU will give more convenience to operators.

b) Battery state monitor

Simply adding a small A/D converter will allow the operator to be able to monitor the charging status. This will allow the measurement operation to be more convenient.

c) Fixed power supply from 240V/AC

This wireless data acquisition system is being considered for installation in substations for a 24-hour monitoring network. In that application, RAU needs to add an AC 240V power adapter.

5) Better performance in the future

This system has 20MHz bandwidth and 80MSPS sampling rate. It can be used in situations where the upper limit of the EMI frequency is 20MHz. To measure a

signal with frequency component higher than 20MHz, the acquisition circuit should have wider bandwidth and higher sampling rate. That means the components in the RAU should be increased, i.e. the A/D conversion speed, digital signal processing speed and storage speed should be higher, which cannot be achieved by TTL interfaces and TTL logic circuits. If future systems are designed to measure higher frequency signals, the Acquisition Board is suggested to employ faster components, such as ECL (Emitter Coupled Logic) or LVDS (Low Voltage Differential Signaling). For example, a future design can employ a high-speed ADC replacing ADC08100, employ a FPGA with LVDS interface replacing CPLD, employ faster memory replacing the SRAM. Based on the available components nowadays, such a design could achieve up to 1GSPS sampling rate. However, the principles and the basic structure of the future Acquisition Board will be the same as the prototype design.

Any future development can also use larger memory to buffer more data and use a more powerful wireless modem for further communication distance or communication speed.

6) Acquisition Card

The Acquisition Board in the RAU has been designed to deal with a fast transient signal and provide an interface to the embedded CPU. In fact, in industrial areas, people often operate with similar fast transient signal. Although DSO or other PC-based acquisition devices can deal with fast transient signal, they are not always available for an embedded system.

In many projects, where there is a need to use a single chip micro-controller or microprocessor, designers used to design their own sampling circuit. Those circuits are usually designed for their specific applications and, therefore, cannot be used for other equipment. However, in this project the Acquisition Board has most of the general acquisition functions, since it was designed to replace the DSO in previous system and deals with miscellaneous signals. Also the Acquisition Board has the interface to MCS-51 series micro-controller, which is compatible with most popular micro-controller or processor. Therefore, the Acquisition Board can be used for acquiring fast transient signal in many embedded situations. Considering the

demands of this application, the EMC group has applied for a patent for the design of the Acquisition Board and is planning to put it into the market as an independent product. If so, the Acquisition Board will be synthesized into a single module. Furthermore, it could form a product series with different grades of sampling rate, memory size input channels etc to meet diverse applications demands. This work can be done in future development.

It can be expected that after further development, the Wireless Data Acquisition System will have better performance and wider application.

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Appendix A: Schematic sheet of Acquisition Board

ACQ

XC95288

U18

7C4069

U13

ADC08100

U5

OSCILLATOR_SMD

U9

Offset signal

+3.3V

R1 560

R2 160*

R3 220

R4 24

R5 480

R2 1.8K*

C1 33P

C2 15P

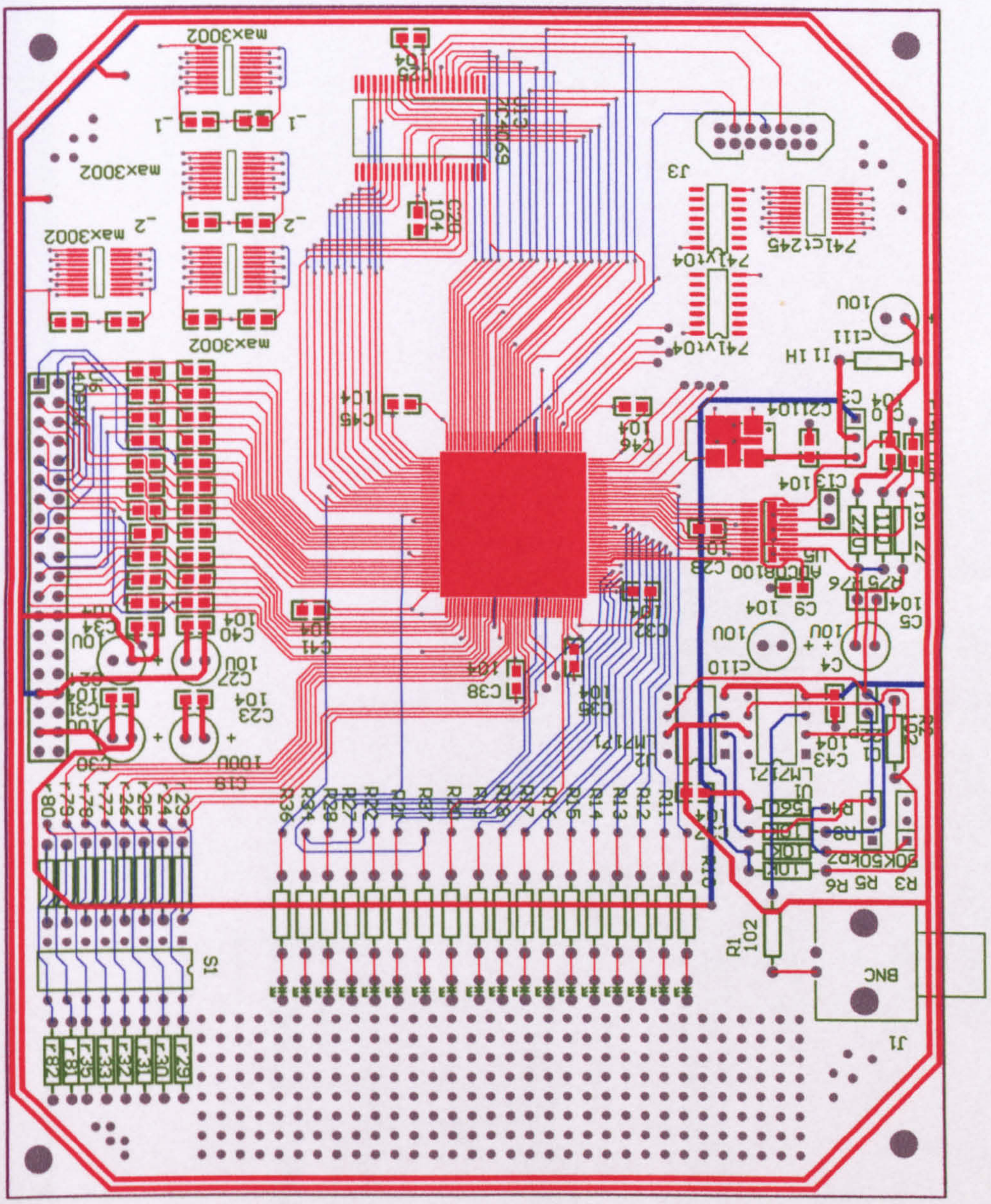
J1

U1

Appendix B: PCB sheet of Acquisition Board

(1:1)

Appendix C: Schematic sheet of CPU Board



Appendix C: Schematic sheet of CPU Board

ADC08100

XC95288

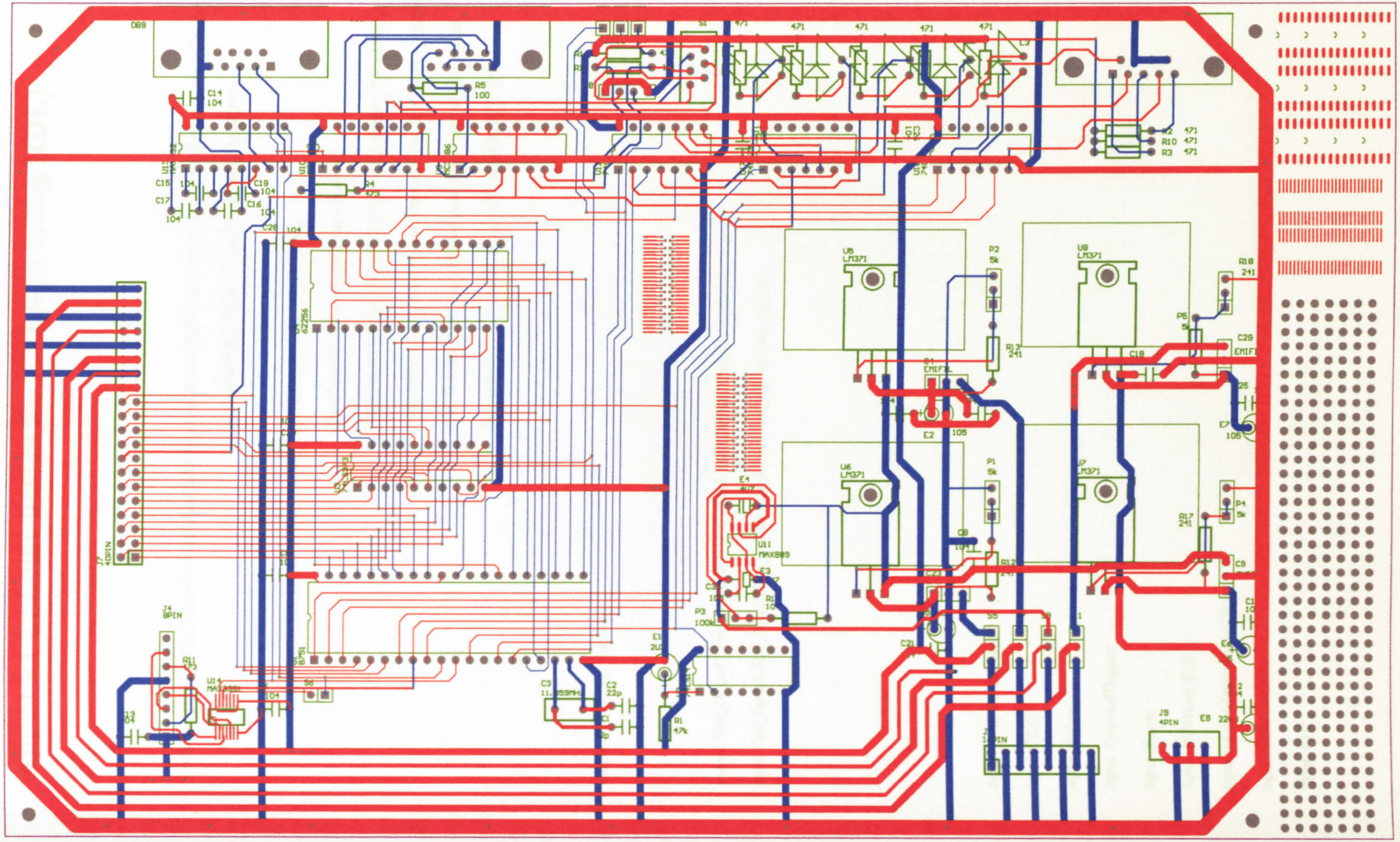
7C4069

OSCILLATOR_SMD

Title	ACQ		
Size	Number		Revision
C	1		1.1
Date	22 Feb 2005	Sheet of	
File	F:\acq1.DSN	Drawn By	Yu Weimin

Appendix D: PCB sheet of CPU Board

(1:1)


DB9
C14
104
R5
100
S1
471
471
471
471
471
R2 471
R10 471
R3 471
C15 104
C17 104
C19 104
C16 104
C26 104
U10
U11
U12
U13
U14
U15
U16
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U48
U49

Appendix E: Logic design for CPLD (Verilog HDL)

```
module acq7 ( CLKToAD,DataFromAD,DataToRAM,AddressToRAM,RDToRAM,WRToRAM,CLK,Refresh,ExternalTrigger,
                                                    Reset,WRFromCPU,RDFromCPU,AddressFromCPU,
DataWithCPU,P13,P14,P13Out,P14Out,Triggered,CLK1,CLK2,CLK3,CLK4,
                                                    TimeControl2,TimeControl3,TimeControl4,
                                                    WRToRAM1,WRToRAM2,WRToRAM3,WRToRAM4,WRToRAM5,
                                                    Test_Address,Test_Output1,Test_Output2,Test_Output3,Test_Output4,
                                                    Test_Output5,Test_Output6,Test_Input1,Test_Input2,Test_Input3,
                                                    Test_Input4,Test_Input5,Test_Input6/*,LatchData[7:2]*/);

output [18:0] Test_Address;


output Test_Output1,Test_Output2,Test_Output3,Test_Output4,Test_Output5,Test_Output6;
input Test_Input1,Test_Input2,Test_Input3,Test_Input4,Test_Input5,Test_Input6;


input [7:0] DataFromAD;
input CLK;
input Refresh;
input ExternalTrigger;
input Reset;
input WRFromCPU;
input [4:0]AddressFromCPU;
input RDFromCPU;
input P14;
```

```
input  P13;
input  TimeControl2;
input TimeControl3;
input TimeControl4;
input WRToRAM2,WRToRAM4;

output  [18:0] AddressToRAM;
output  RDToRAM;
output  WRToRAM;
output  Triggered;
output  P13Out;
output  P14Out;
output  CLKToAD;
output  CLK1,CLK2,CLK3,CLK4;

output  WRToRAM1,WRToRAM3,WRToRAM5;


inout   [7:0]DataToRAM;
inout   [7:0]DataWithCPU;


wire [7:0] DataToRAM;
wire [4:0]AddressFromCPU;
wire [7:0] DataFromAD;
//wire [7:2] LatchData;


wire ReadRAM;
wire Triggered;
wire [7:0]Port1;
wire [7:0]Port2;
wire [6:0]TriggerLevel;
wire [7:0]TriggerDelayL;
wire [1:0]TriggerDelayH;
wire [6:0]TriggerPosition;
wire [7:0]Status;
```

```
wire [2:0]SpeedSelection;

reg [5:0] Counter1;


always @ (posedge Reset or posedge CLK)
begin
        if (Reset)
                Counter1=6'b0;
        else
                Counter1=Counter1+1'b1;
end


assign Test_Address[16]=(Counter1[5]&SpeedSelection[2]&SpeedSelection[1]&SpeedSelection[0])|
(Counter1[4]&SpeedSelection[2]&SpeedSelection[1]&~SpeedSelection[0])|
(Counter1[3]&SpeedSelection[2]&~SpeedSelection[1]&SpeedSelection[0])|
(Counter1[2]&SpeedSelection[2]&~SpeedSelection[1]&~SpeedSelection[0])|
(Counter1[1]&~SpeedSelection[2]&SpeedSelection[1]&SpeedSelection[0])|
(Counter1[0]&~SpeedSelection[2]&SpeedSelection[1]&~SpeedSelection[0])|
(CLK&~SpeedSelection[2]&~SpeedSelection[1]&SpeedSelection[0]);


assign P13Out=!P13;
assign P14Out=!P14;


assign CLK1=!CLK;
assign CLK2=!TimeControl2;
assign CLK3=!TimeControl3;
```

```
assign CLK4=!TimeControl4;


assign WRToRAM1=!WRToRAM;

assign WRToRAM3=!WRToRAM2;

assign WRToRAM5=!WRToRAM4;


RAMInterface acq5RAMInterface

(.Port1(Port1),.DataFromAD(DataFromAD),.Port2(Port2),.DataToRAM(DataToRAM),

.ReadRAM(ReadRAM),.Address(AddressToRAM),.RD(RDToRAM),.WR(WRToRAM),.Triggered(Triggered),

.CLK(CLK),.Refresh(Refresh),.CLKToAD(CLKToAD),.CountPulse(Test_Output1),.Reset(P14),.AdjustableCLK(Test_Address[
16]));


registers acq5register (.Data(DataWithCPU),.Address(AddressFromCPU),.wr(WRFromCPU),.rd(RDFromCPU),

.TriggerLevel(TriggerLevel),.TriggerPosition(TriggerPosition),

.TriggerDelayL(TriggerDelayL),.TriggerDelayH(TriggerDelayH),.Status(Status),

.SpeedSelection(SpeedSelection),

.Port1(Port1),.Port2(Port2),.ReadRAM(ReadRAM));


trigger acq5trigger (.Data(DataFromAD),.CLK(CLK),.TriggerLevel(TriggerLevel),.Reset(P14),

.ExternalTriggerSelection(Status[1]),

.ExternalTrigger(ExternalTrigger),.CLK_11(AddressToRAM[11]),.TriggerPosition(TriggerPosition),

.TriggerDelayL(TriggerDelayL),.TriggerDelayH(TriggerDelayH),.Triggered(Triggered),

.Test_Output2(Test_Output2),.Test_Output3(Test_Output3),.Test_Output4(Test_Output4),

.LatchCLK(Counter1[1])/*,.LatchData(LatchData)*/);
```

```
assign Test_Address [17] = Test_Output2;

//assign Test_Address [16] = AdjustableCLK;

assign Test_Address [15] = SpeedSelection[2];

//assign Test_address [14] = Counter1[2];

assign Test_Address [14:9]=AddressToRAM[14:9];

assign Test_Address [0]=SpeedSelection[1];

assign Test_Address [18]=Triggered;

//assign Test_Address [8:3]=LatchData[7:2];

assign Test_Address [8:1]=DataFromAD [7:0];

assign Test_Output5=SpeedSelection[0];

assign Test_Output6=Test_Input6&Reset&Test_Input5;
```

```
endmodule

module registers(Data,Address,wr,rd,TriggerLevel,TriggerPosition,TriggerDelayL,
                                                    TriggerDelayH,Status,SpeedSelection,Port1,
                                                    Port2,ReadRAM);


inout [7:0] Data;


input [4:0] Address;
    input wr,rd;
    input [7:0]Port1;
    input [7:0]Port2;



output [6:0] TriggerLevel;
output [6:0] TriggerPosition;
output [7:0] TriggerDelayL;
output [1:0] TriggerDelayH;
```

```
output [7:0] Status;

output [2:0] SpeedSelection;

output ReadRAM;

reg [6:0] TriggerLevel;

reg [6:0] TriggerPosition;

reg [7:0] TriggerDelayL;

reg [1:0] TriggerDelayH;

reg [7:0] Status;

reg [2:0] SpeedSelection;

wire [7:0] Port;

wire [7:0] Port1;

wire [7:0] Port2;

wire [7:0] Data;

always @ (negedge wr)

                begin

                        case (Address)

                                5'b 10000: TriggerLevel=Data[6:0];

                                5'b 10001: TriggerPosition=Data[6:0];

                                5'b 10010: TriggerDelayL=Data;

                        5'b 10011: TriggerDelayH=Data[1:0];

                                5'b 10100: Status=Data;

        5'b 10101: SpeedSelection=Data[2:0];

//                              5'b 10110: Atenuation=Data[2:0];

                        endcase

end

assign Port[7:0]=(Address==5'b11111)? Port1[7:0]:Port2[7:0];
```

```
assign ReadRAM=!((Address==5'b11111)|!rd);

assign Data[7:0]=(Address[4]&!rd)? Port[7:0]:8'bz;

endmodule

module trigger(Data,CLK,TriggerLevel,Reset,ExternalTriggerSelection,Triggered,
                                        ExternalTrigger,CLK_11,TriggerPosition, TriggerDelayL,
        TriggerDelayH,Test_Output2,Test_Output3,Test_Output4,LatchCLK/*,LatchData*/);

input [7:0] Data;
input [6:0] TriggerLevel;
input CLK;
input Reset;
input CLK_11;
input [6:0]TriggerPosition;
input [7:0] TriggerDelayL;
input [1:0] TriggerDelayH;
input ExternalTriggerSelection;
input ExternalTrigger;
input LatchCLK;

output Triggered,Test_Output2,Test_Output3,Test_Output4;
//output LatchData;

//following outputs are for test the middle variables
/*output Trigger1,Trigger2,Trigger3,Trigger4;
output [16:0] Count2; */

wire Trigger1;
```

```
wire TimeLiitation;

reg Trigger2,Trigger4, Triggered;

reg [2:0] Count1;

reg [16:0]Count2;

reg [6:0] Count3;

reg [7:1] LatchData;

wire Trigger5;

wire Trigger3;



always @(posedge LatchCLK )

begin

                                LatchData[7:1]=Data[7:1];

end

assign Trigger1 = LatchData[7:1] >= TriggerLevel[6:0];



always @( negedge LatchCLK or posedge Reset)

begin

        if (Reset)

                Trigger2=1'b0;

        else

                Trigger2=Trigger1;

end


always @ (posedge LatchCLK or posedge Reset)

begin

        if (Reset)

                Count3=3'b0;

        else

                Count3= Count3+1'b1;

end
```

```
/*
assign
TimeLimitation=!Count3[6]&!Count3[5] &!Count3[4]&!Count3[3]&!Count3[2]&!Count3[1]&!Count3[0];

always @( negedge LatchCLK or posedge TimeLimitation)
begin
        if (TimeLimitation)
                Count1=3'b0;
        else
                if (Trigger2)
                Count1=Count1+1'b1;
end

*/

assign Trigger3=ExternalTriggerSelection? ExternalTrigger:Trigger2;//Count1[2];

always @(posedge Reset or posedge Trigger3)
begin
        if (Reset)

                Trigger4=1'b0;

        else
                        if (Trigger3)
                Trigger4=1'b1;
end
```

```
always @ (negedge Trigger4 or posedge CLK_11)
begin
        if (!Trigger4)
            Count2=17'b0;
        else
            Count2=Count2+1'b1;
end
assign Trigger5={TriggerDelayH,TriggerDelayL,TriggerPosition}/*17'b10000000001000000*/ == Count2;


always @ (posedge Reset or negedge CLK_11)
begin
        if (Reset)
            Triggered=0;
        else
            if(Trigger5)
                Triggered=1;
end

assign Test_Output2=Trigger1;
assign Test_Output3=Trigger2;
assign Test_Output4=Trigger1;

endmodule
```

Appendix F: Wireless Digital Data Acquisition System User Manual

1. Features and general description

Wireless Digital Data Acquisition System is field data collection equipment dedicated for EMI measurement in substations. It consists of several Remote Acquisition Units (RAUs), a point-to-multipoint wireless data communication network and a PC.

RAU can be connected with different type of sensors that are placed at different points to detect EMI signals caused by electrical emission in a substation. Usually, sensors are placed inside the switchyard of a substation.

A Control PC is placed in a control room or a test-van. It is connected with RAUs by a wireless data communication network.

When a switch action happens, it generates significant electrical emission resulting in Electro-Magnetic Interference that can be sensed by sensors in the substation. Users can capture the EMI signal by setting-up a proper trigger level on RAU. Once RAU is triggered, it will store the waveform of the EMI pulses and then send them to a remote PC through wireless data communication network. RAU has maximum sampling rate of 80 MSPS and adjustable rates of 40MSPS, 20MSPS, 10MSPS, 5MSPS, 2.5MSPS and 1.25MSPS. The RAU has a memory of 512K, which can record the signal's length of 6.4 ms at 80MSPS sampling rate and 0.5s at 1.25MSPS. RAU has a BNC socket to input signal. RAU has four rechargeable batteries to support itself.

The PC controls and monitors RAUs with application software.

The Wireless network is built by Bluetooth devices: Bluewave® data modem (made by WirelessFuture Ltd, UK) Please refer to the specification of this product. A master modem is linked to PC with RS-232 port and slave modems are linked to RAUs. This point-to-multipoint network can fulfill the requirement of multiple access by implementing a polling strategy. It has 100 meters range (open space) and 60-75 Kbps effective data rate.

Figure 1 shows the structure of the measurement system

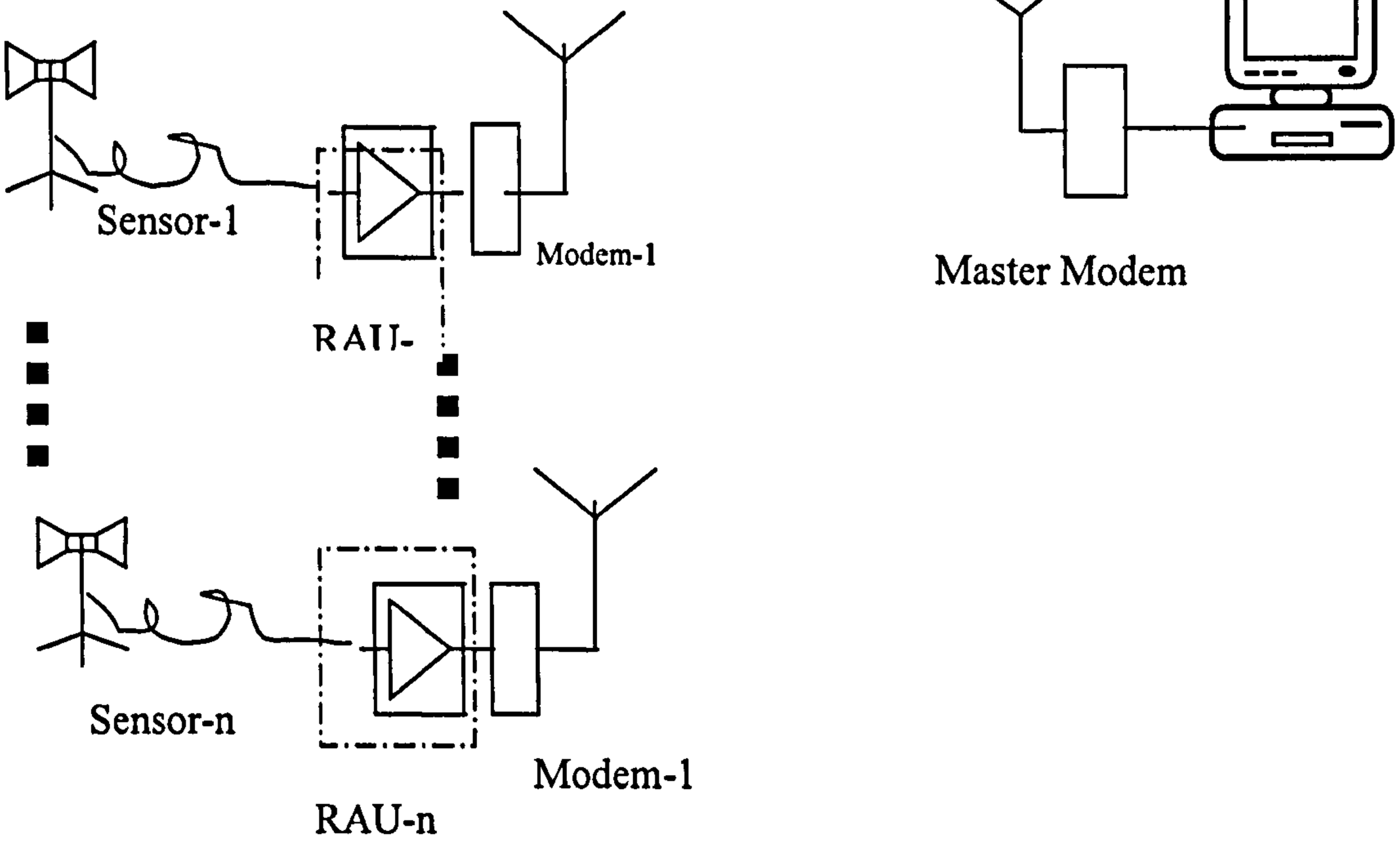


Figure 1: The structure of the system

This system provides convenience and mobility to the users. The functions of the system are like a wireless digital storage oscilloscope working in the single trigger mode. Users are suggested to review the features of digital oscilloscope and it's operations for a clearer understanding of this manual.

The prototype system has two RAUs and their attached modems.

2. List of the package

RAU	2
Slave Bluetooth Modem	2
2m Extension RS-232 Cable	2
USB power cable	1

12V battery charger	1
Floppy with an application software	1
PC or Laptop with Windows XP or Windows 2000 operation system	1
Power cable	2

Figure 2 shows the outline of RAU

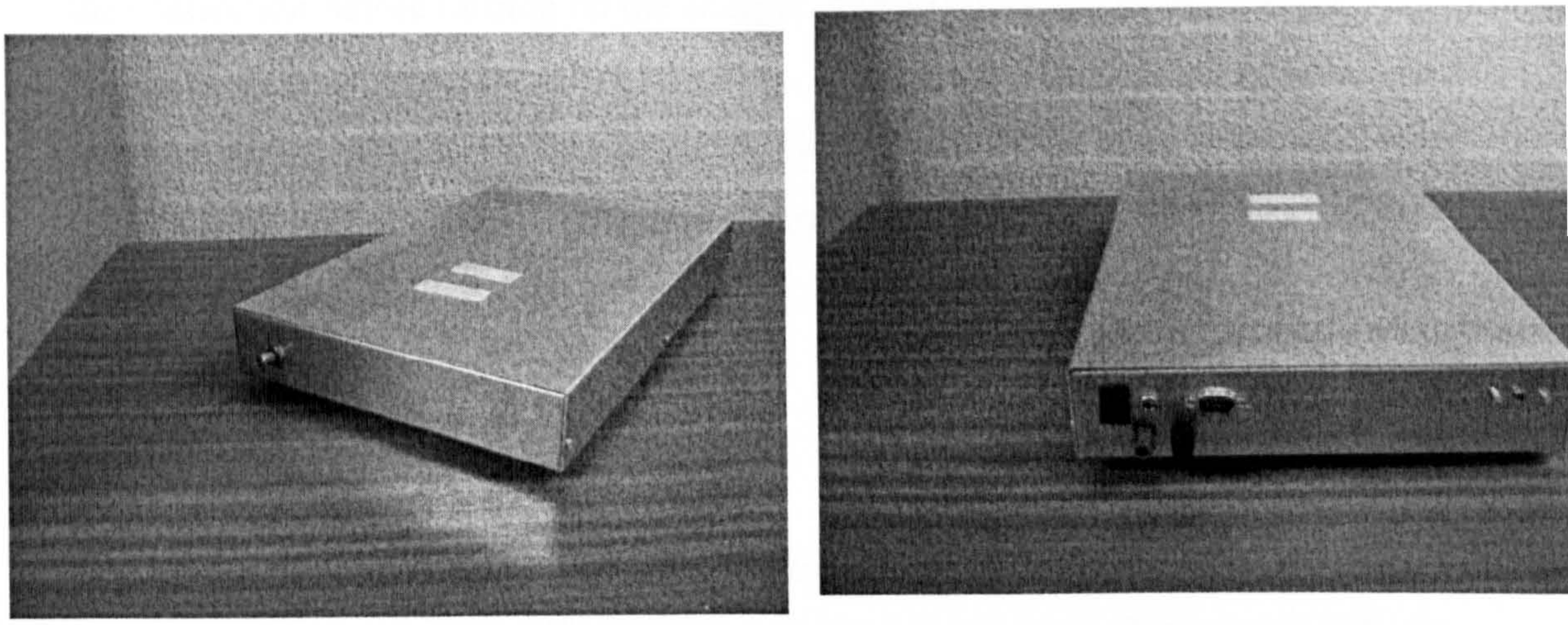


Figure 2: The outline of RAU

3. Installation

3.1 Checking Batteries

RAU is powered with four paralleled rechargeable batteries (12V 1.2 AH each). Full charged batteries group has 12.75 V output voltage and can last 4 hours when RAU

is working. The output voltage will drop down linearly with the decrease of the capacity. When the output voltage drops to 11.25 V, the batteries can't be used further and need to be recharged immediately.

Since most of the measurements take 1 to 2 hours, the RAU does not need to be charged every time before measurement. However, user must check the battery's voltage, calculate the remained capacity of the power and make sure it will be able to support next measurement work.

To check the output voltage of the batteries, turn off the RAU and measure the voltage between positive charge polar in the back panel (red pole) and the negative polar (black pole). Refer to Figure 1 for the position of these charge poles.

To charge the battery, turn off the RAU and use the positive clip (red one) of the charger to hold the positive red charge polar in RAU polar, use the negative clip to hold the negative charge polar in RAU. Then turn on the charger Please note check the connection before turning on the charger. The yellow LED of the charger indicates the charging is taking place going. When the charging processing is finished, the green LED of the charger will light. Please refer to the specification of this charger: Sealed Lead Acid Battery Charger, Made by R3 Technology Ltd, Aylesbury, Bucks, HP18 0XB, UK.

3.2 RAU connection

RAU has a BNC socket to input measured signals. User can use coaxial cable to connect RAU and sensors. If a sensor has an output connector different from RAU, an adaptor should be applied e.g. SMA to BNC adaptor can be used when the sensor has a SMA socket. In most situations, the sensor output the signal within the RAU input range –1V to +1V. If the output signal exceeds this range, an attenuator will be added to the route from sensor to RAU. If the output signal of a sensor is too small to take the whole dynamic range of RAU, then an external amplifier will help. RAU has a build-in input anti-alias filter for 80MSPS. If the sampling speed is less than this, it needs an external filter to cut-off the signal above Nyquist frequency. Most sensors

have such kind of filters, but not universal. In that case, operator should add an anti-alias filter. Figure 3,4,5,6 show above five connections:

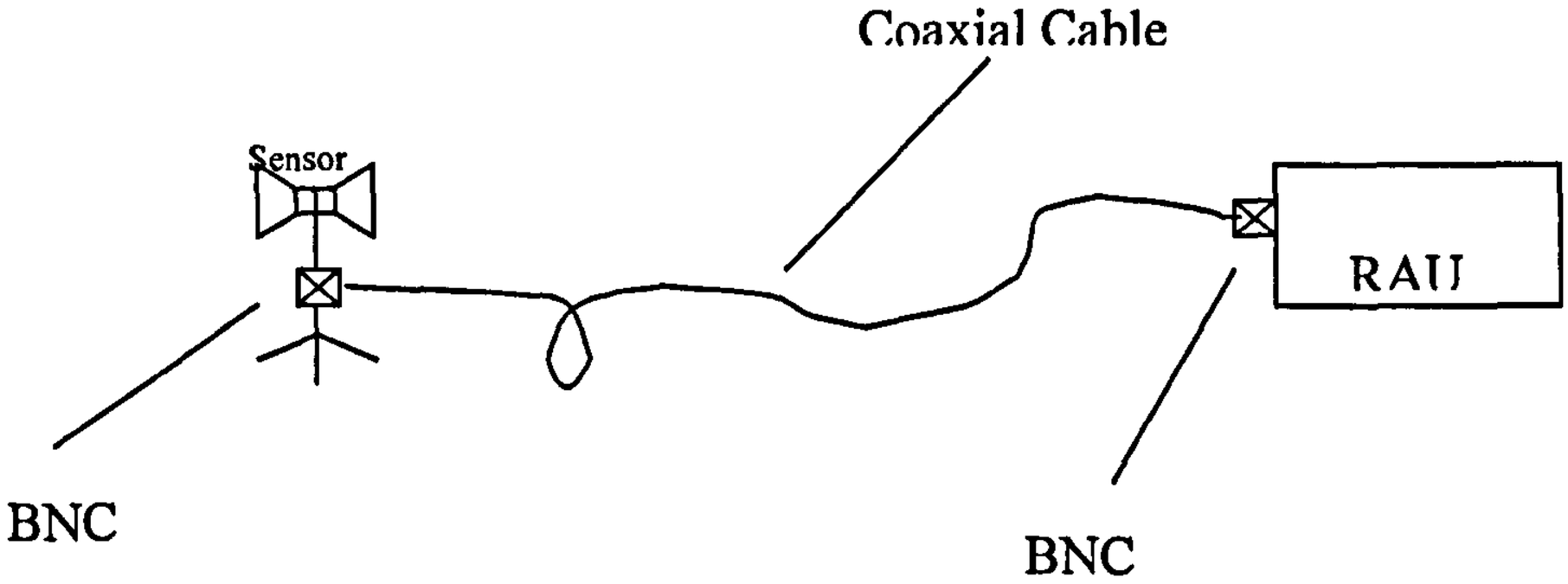


Figure 3: Normal connection of RAU

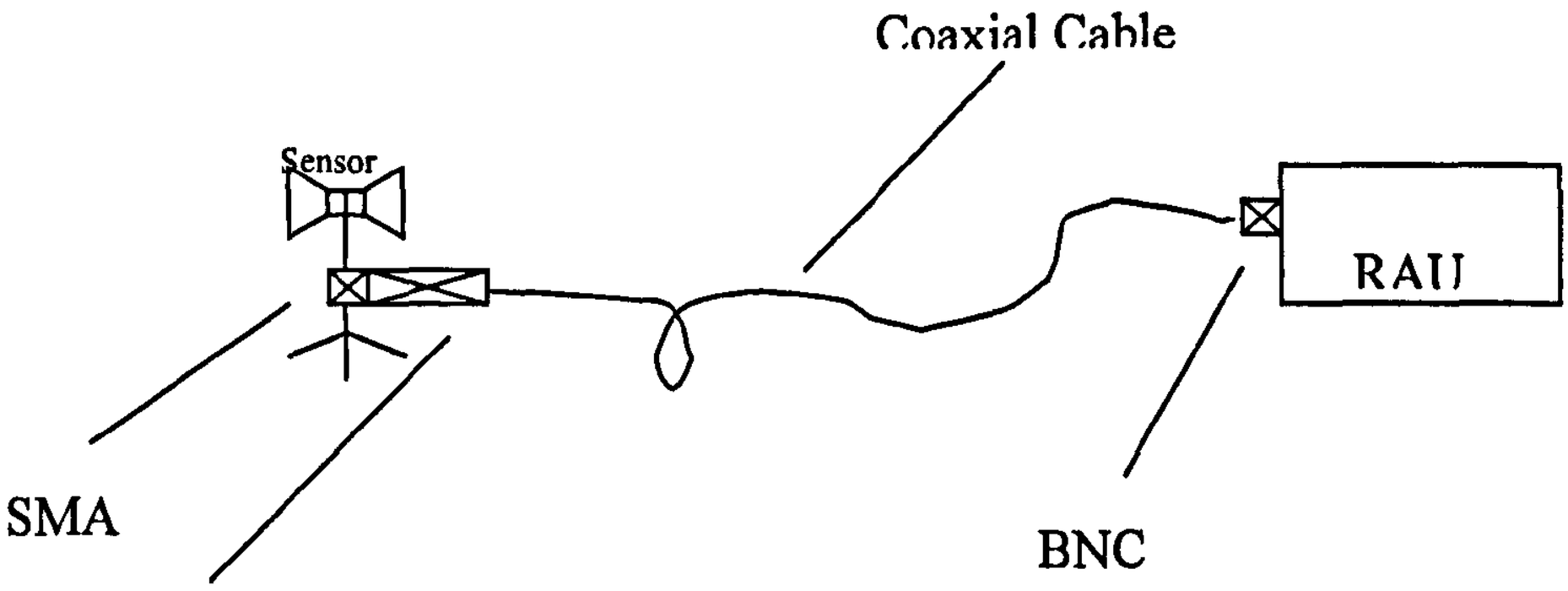
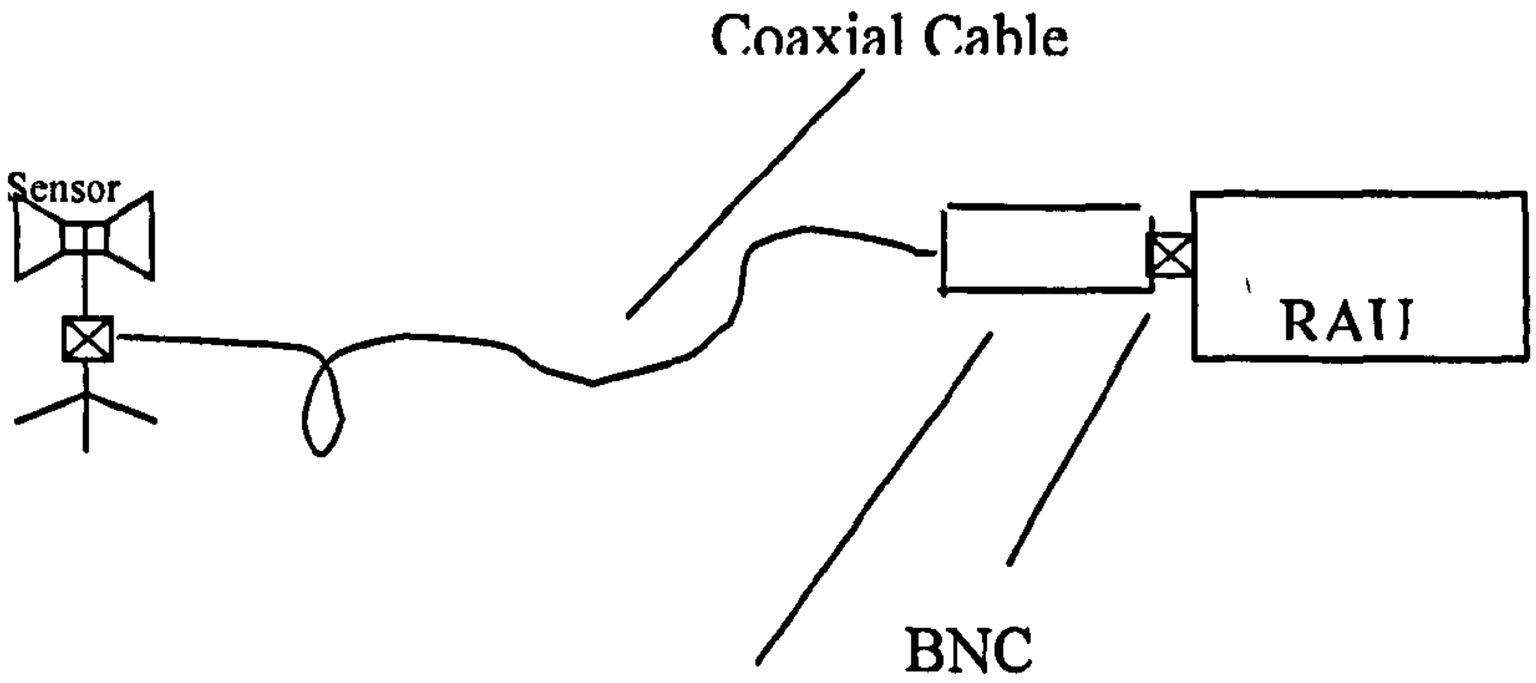


Figure 4: Need a connecter's adapter

SMA to BNC



Attenuation

Figure 5 Exceed input range

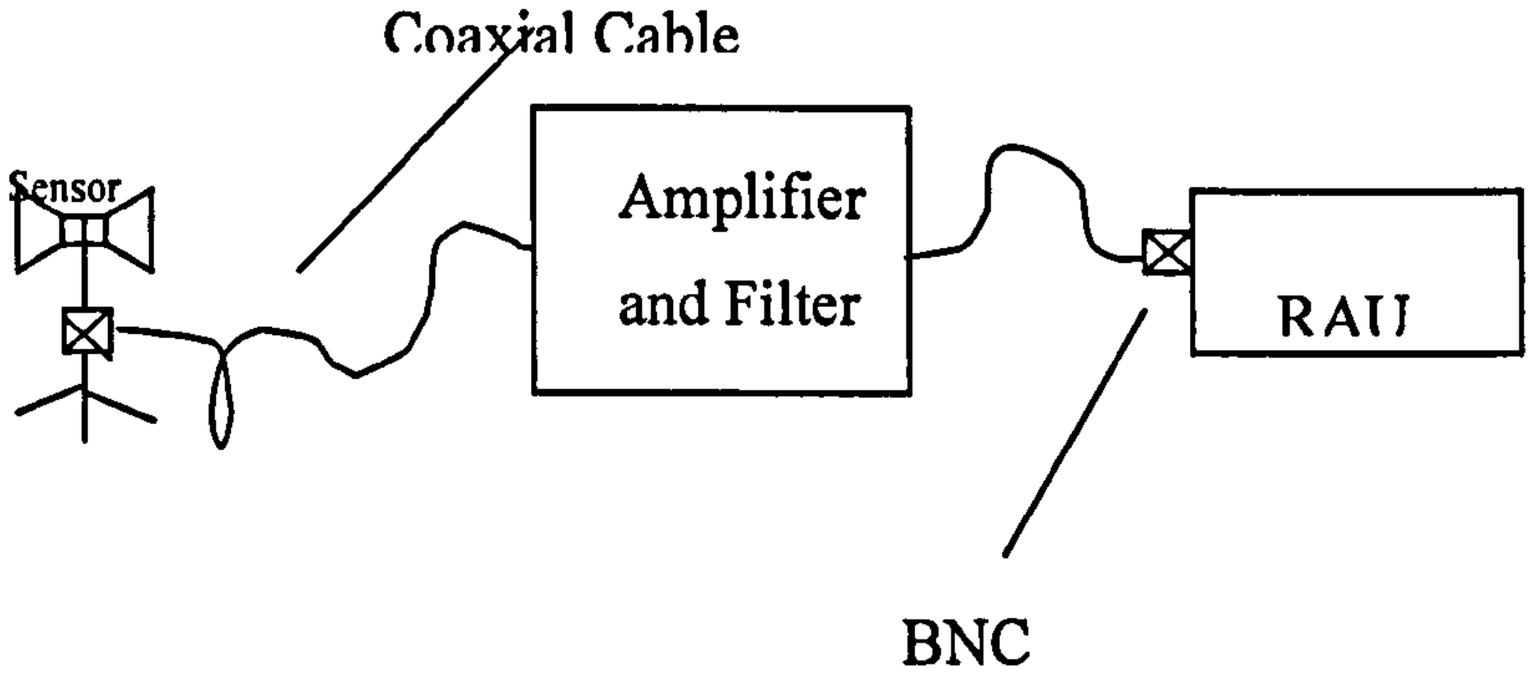


Figure 6 Signal is too small or has alias problem.

3.3 Software installation (DOS version)

Create a folder in PC or laptop. And copy two files RAU01 and RAU02. (RAUxx, if more RAU are included in that package).

After this, users can operate with certain RAU by keying-in its name (every RAU has its unique ID like RAU01, RAU02 and etc, which will appear as the Bluetooth Device Name)

3.4 Network Connection

Using power cable and RS-232 cable, user can connect a RAU to its attached Bluetooth Modems then repeat the work to connect all the pairs of RAU and Modem (e.g. the RAU labelled with RAU01 should connect to the modem labelled with RAU01 and so on).

Once the modem is powered (RAU provides 8V power supply to modem), the LED in top of the modem *will flash twice.*

Using USB power cable and RS-232 cable to connect the Bluetooth modem, labelled with Master. Once the master is powered, the LED will flash once.

Important: Do not power the modem until the RS-232 cable has been fixed.

4.Operations of the Software

4.1 Selecting an operation

After installation, once all the sensors and RAUs are ready in the site, turn on the RAU and run the application software in the PC or laptop (click the icon in that folder or input the executable file name with 'Enter' in DOS environment). Once the application program is launched, it will search the Bluetooth device, which the name of the program specifies and establish the connection with that Bluetooth device. If the connection has been made, the LED in master device will light. User will see the prompt lines in PC: Press 's' to Set-up; Press 'd' to download; Press 'Esc' to return to DOS; Press 'p' to display Parameters and Press 'm' to restart measurement. Above options can be selected at any time by pressing the short keys.

Following are the explanations of Download, Parameters Display, Start Measurement and Set-up:

Set-up: Set-up the operating parameters of RAU e.g. trigger level, trigger delay and etc.

Download: After RAU is triggered, user can download the data from RAU and save them in the local disk Download command will prompt user to input a file name to store the data.

Start Measurement: Start Measurement is the command to release previous triggered status and enable a new measurement. When RAU is triggered it keeps the captured data in the memory and stops accepting further signal, until "Start Measurement" command releases the triggered state. This feature is like the single trigger mode of a digital storage oscilloscope.

Display Parameters: This command will implement the monitoring menu. In that menu, all the RAU's parameters and status will be displayed and continuously updated.

Figure 7 and Figure 8 show the set-up menu and parameters menu.

```
Please select the trigger source.
1 for self trigger; 2 for external trigger. "Enter" for default.
(defaut: Self trigger)


Please input the value of trigger level in mV, then press "Enter" to confirm.
A "Enter" input without any input will  give a default value of 500mV
750

Pre-trigger:
Plese input the pre-trigger value between 0  to 100 (%), default value=50
55

Trigger Delay:
Input value between 0 and 99999 (x). Default value=0

Sampling Speed:
Plese select fraction of maximum speed (1/1,1/2, 1/4, 1/8, 1/16, 1/32, 1/64) by
inputing 1,2,4,8,16,32,64 correspondingly.Then press "Enter".
Default is maximum sampling rate.
-
```

Figure 7: the Set-up menu

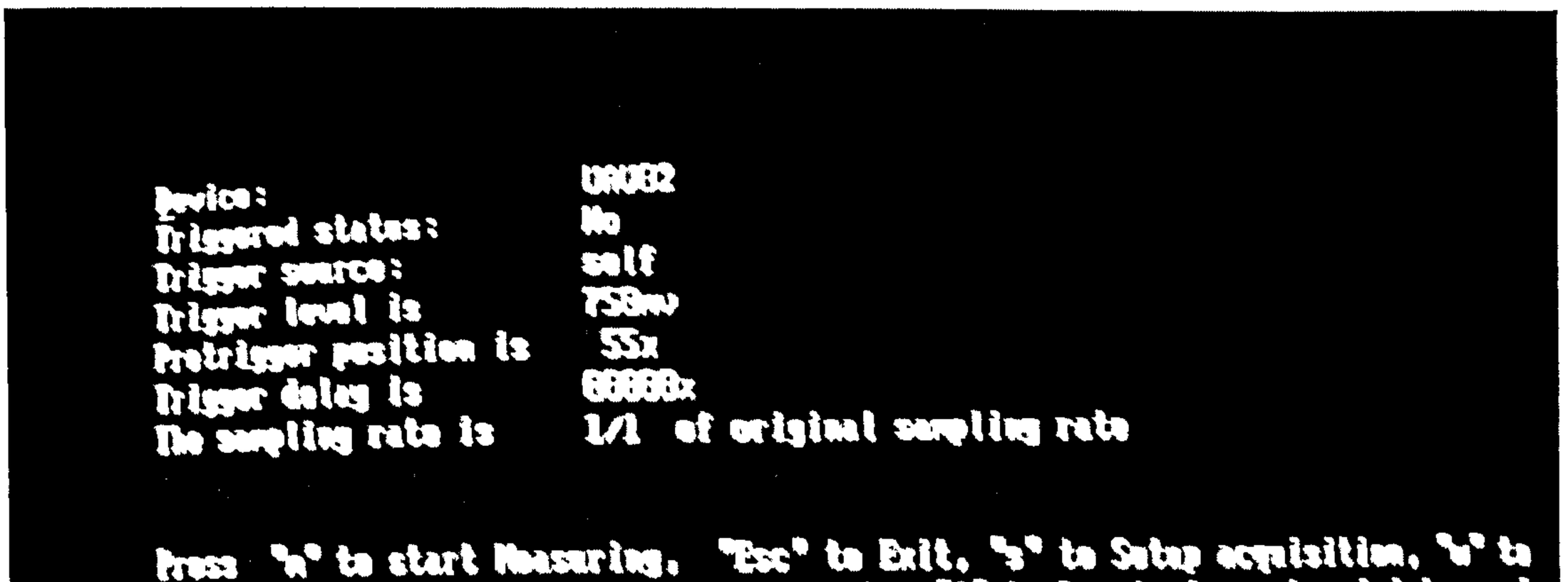


Figure 8: The parameters monitoring menu

4.2 How to set-up the RAU

(Please refer to the usage of single trigger mode of a digital oscilloscope when reading this subsection)

Enter 'Set-up' menu. Following the prompt lines user will be able to set-up trigger source, trigger level, trigger delay, trigger position and speed selection (time base). All the parameters have the same definitions as used in a digital storage oscilloscope. However, the following clarifications should be noted

Horizontal control of oscilloscope is to decide where a specified signal should appear in the horizontal position (time axis) of the screen or memory.

Different oscilloscope manufactures use different terms and definitions for horizontal control. This system follows Tektronix style and uses two parameters: trigger delay and pre-trigger (or trigger position).

Main-trigger-point is the moment when measured signal meets the trigger condition.

Trigger-delay defines the time intervalafter main-trigger-point before RAU responds to the trigger action. This moment is defined as Second-trigger-point.

Pre-trigger decides how much time before the second trigger point, when RAU starts recording.

Second-trigger-point is the specified point, which operators are interested in. When "Trigger delay" is '0'. The second-trigger-point is main-trigger-point itself. Figure 8 illustrates the situation when delay time is 0; pre-trigger (or trigger position) is 30%

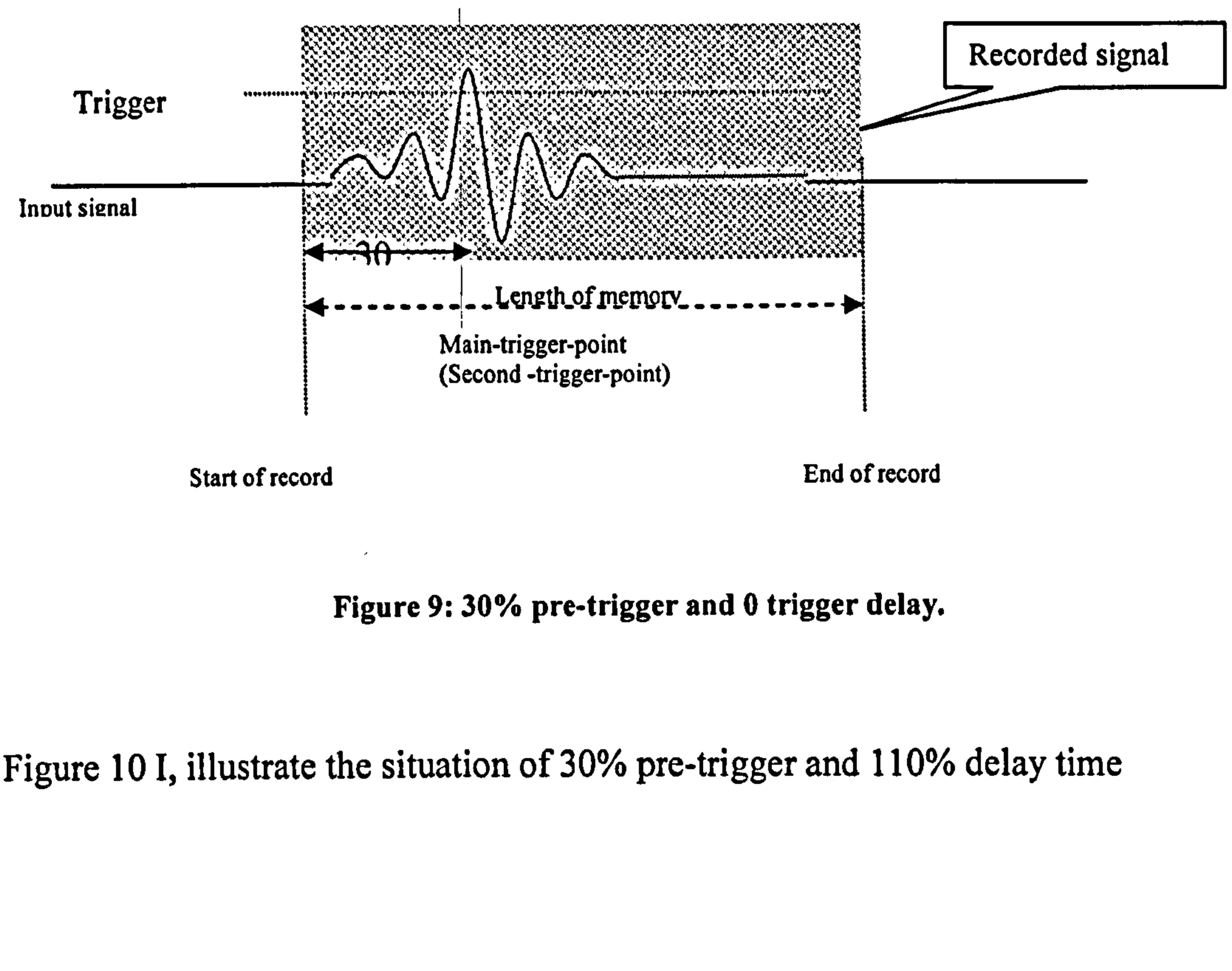


Figure 9: 30% pre-trigger and 0 trigger delay.

Figure 10 I, illustrate the situation of 30% pre-trigger and 110% delay time

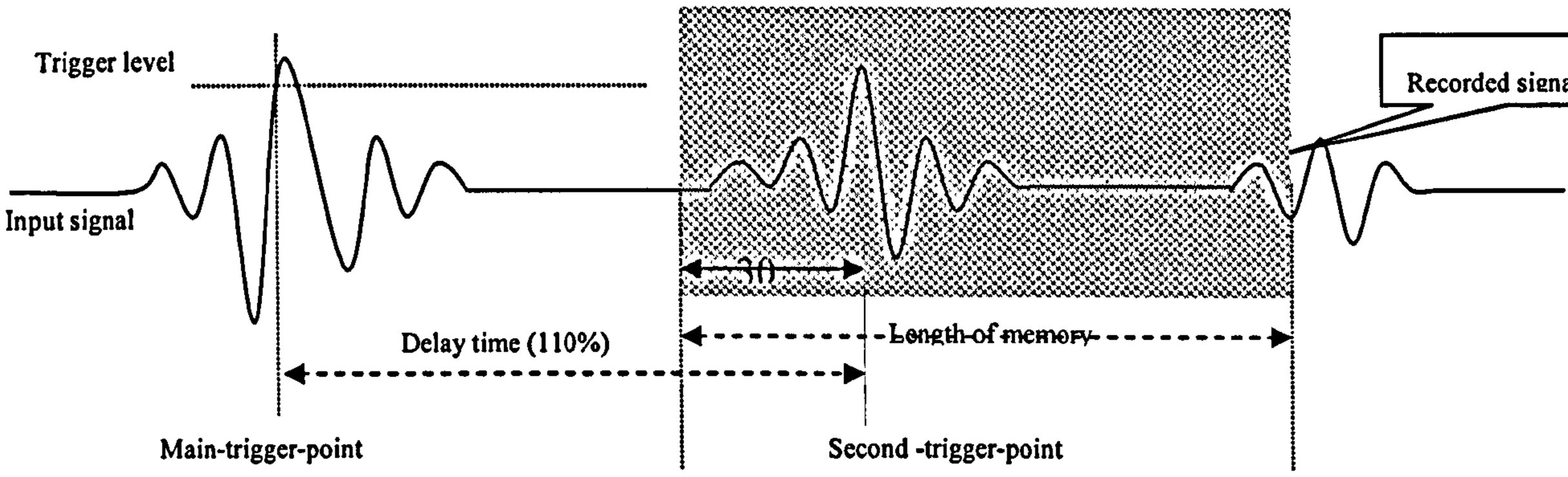


Figure 10: 30% pre-trigger and 110% trigger delay.

Here, pre-trigger (or trigger position) determines the position of the specified signal. Trigger delay should not always be used, unless the main trigger point is different from the point to be measured and the two are separated by a proportionally long time interval.

Next example explains when users need the function of trigger delay and how to use it:

In substations, a switching procedure may include several actions, which cause a series of electrical emissions. If the second emission pulses have similar amplitude with the first emission pulses, the two emission signals can't be distinguished by a proper trigger-level. And also, the second emission may separate from first one in 1 second. This time interval is too small for operators to clear first trigger and start a new measurement. Also, the memory of the RAU can't cover the whole 1 second signal period. In this case, operator can set-up the trigger delay to 1 second to measure the second emission.

Here, the system uses percentage to describe the pre-trigger and trigger delay time. Because the time of whole memory is different according to the different sampling rate, the delay time can be calculated by following formula:

$$T = X \bullet \frac{524288}{Sampling\_rate} \mu S$$

Where T is the delay time (unit: micro-second); X is the percentage; the unit of Sampling rate is SPS (samples per second).

It can be seen that RAU can provide 6.5 seconds delay at 80MSPS rate and 420S delay at 1.25MSPS.

Important: During the process of setting-up, if operator inputs a wrong value, they can't modify it using Backspace key or other keys. The only way to correct it is to finish current set-up operation and set-up again with the correct value.

5. General Measurement Process

A typical electrical emission measurement includes following steps:

1) Put all the sensors in the field of substation and connect RAUs to them. Connect Bluetooth wireless modems to the RAUs. Switch on the RAUs, the LED power indicators on RAU panel should flash once and then stably light.

2) Go to the control room or test-van, where PC or laptop is placed, link the master Bluetooth modem to the PC and switch on the PC and the LED on Bluetooth modem will flash once indicating that the modem has been powered. Run the application software, it will establish the wireless connection to the RAU that is specified by the program name. After the wireless connection is established, the LED on modem will be stably light and then the user can remotely operate the RAU.

3) Press 's' and set-up all the values; press 'm' to enable the new value and start the measurement. Press 'p' to check the status of the RAU; if everything is ok, press 'Esc' to leave this program and enter another RAU control program. Repeat such operation to every RAU in the field. When all of RAUs are ready, users can monitor any of them and wait for the switch action to happen.

4) When the switch action happens, all the RAUs will be triggered, provided the trigger levels have been set-up properly. User can then download the data by

pressing 'd'. The data will be saved in the local disk with a file name. Repeat the operation to every RAUs and obtain all the records.

5) Then user can go to every RAU's control menu and press 'm' to release previous triggered value and start a new measurement for next switching action. In addition, user can change the previous set-up value in that control menu if needed. The above measurement should be repeated until enough data is collected.

6) Switch off the RAU and PC. Analyse all data that has been collected with a waveform viewing software or other statistical software.

6. Important Notes

1) Full charged batteries in a RAU can last 4 hours, but depends on the quality of the batteries, which usually gets degraded after being charged several times. Never use the batteries when the output voltage is lower then 11.25 Volt

2) The measurement often takes place in a switchyard. Neither RAU nor Bluetooth modem are waterproof. As a result, never use them in rainy weather condition without cover. The cover or box used to shield the RAU or modem from water should not be made of metal, for it would shield the wireless signal as well.

3) After measurement or test, always check the RAUs and make sure they have been switched off. Otherwise the batteries would drain out.

4) Bluetooth modem manufactures have provided a stub antenna to every modem. However, user can replace it with other type of 2.4 G antenna with the same connector.

Appendix G: Technical Specification

1. System description

This Wireless Digital EMI Measurement System consists of Remote Acquisition Unit (RAU), Wireless Communication Network and PC-based Control Platform.

RAU is built-up by Acquisition Board, CPU board, and an Enclosure. Acquisition Board includes a CPLD, which implement a Verilog HDL design. CPU Board includes micro-controller, which implement a program.

Wireless Communication Network is built-up by several wireless modems and a simple protocol implemented by software on micro-controller and PC

PC-based Control Platform implements an application program as the background of this data acquisition system.

2. RAU

2.1 Acquisition Board

2.1.1 Circuit design of Acquisition Board

The circuit design was made by "Protel" ECAD software. The schematic design file can be found in the "Design files" CD, :\ACQ\ACQ.s01

The schematic sheet is shown in Appendix A

2.1.2 PCB design of Acquisition Board

The PCB design is made by "Protel" ECAD software. The PCBc design file can be found in the CD, :\ACQ\ACQ.PCB

The PCB sheet is shown in Appendix B

The 20 CAM Geber files are saved in the CD, :\ACQ\Gerber. These files are provided to PCB manufactures. Next are the explanations of them:

Gerber Files:

NS.GTL Top layer;

NS.GBL Bottom layer;

NS.GTO Top over layer;

NS.GP1 Internal plan 1;

NS.GP2 Internal plan 2;

NS.APR Apertures list;

NS.GBS Bottom solder mask;

NS.GTS Top layer solder mask;

NS.GTP Top Paste;

NS.GM1 Mechanical layer;

NS.GD1 Drill Drawing;

NS.GG1 Drill Guide;

NS.DRL NC Drill binary file;

NS.DRR NC Drill report file;

NS.TXT NC Drill ASCII file

2.1.3 Components list of Acquisition Board

Used	Part Type	Designator	Footprint	Description
1	1H	I1	axial0.4	Inductor
1	7C4069	U13	TSSOP-44	SRAM
3	10K	R6 R7 R8	AXIAL0.4	Resistor
6	10U	C4 C24 C27 C30 c110	Electro0.2	Electrolytic Capacitor
1	10p	c150	0805	Capacitor
16	11k	r23 r24 r25 r26 r29 r30 r31 r32 r33 r35 r77 r78 r79 r80 r81 r82	axial0.4	Resistor
1	22	r151	axial0.4	Resistor

1	22p	C1	rad0.1	Capacitor
1	40PIN	U6	IDC40	40P IDC Socket
2	50K	R3 R5	SIP3	Potentiometer
1	100U	C19	Electro0.2	Electrolytic Capacitor
2	102	R1 R2	AXIAL0.4	Resistor
18	103	R10 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R27 R28 R34 R36 R37	axial0.4	Resistor
1	104	J3	14wayPitch2mm	14P Connector
18	104	C9 C10 C20 C21 C23 C25 C28 C31 C32 C34 C35 C37 C38 C40 C41 C43 C45 C46	0805	Capacitor
2	104	C5 C13	RAD0.1	Capacitor
1	110	R75	AXIAL0.4	Resistor
22	220	R100 R101 R102 R103 R104 R105 R106 R107 R108 R109 R110 R111 R112 R113 R114 R115 R116 R117 R118 R119 R120 R121	0805	Capacitor
1	220	R76	AXIAL0.4	
1	560	R4	AXIAL0.4	
1	ADC08100	U5	TSSOP-24	NS ADC
1	BNC	J1	BNC-Socket	BNC Connector
18	LED	2 5 8 12 15 19 22 26 29 33 36 40 41 42 43 44	2-Pin 0.1In.	LED
2	LM7171	U1 U2	DIP8	Amplifier
1	OSCILLATOR	U9	4-Square- SMD	OSCILLATOR
1	XC95288	U10	TQFP-144	Xilinx CPLD

2.1.3 CPLD design

The source code of this design is listed in Appendix E

Design file is saved in the CD, \ACQ\CPLD\ACQ7.npl

2.1.4 Special notices for Acquisition Board

Notes:

1) All the electrolytic capacitors less than 10μF should be selected from Tantalum Series.
2) All the resisters should be chosen from Metal Film 1% series.
3) BNC socket should select a curved isolated one.
4) XC95288 select 6ns grade.
5) Soldering operations for each component are submitted to respective datasheets.
6) For further details of components selection and assembly, refer to the prototype board.

2.2 CPU Board

2.2.1 Circuit design of CPU Board

The schematic sheet is shown in Appendix C

The, schematic design file is saved in the CD. :\CPU\CPU.s01

2.2.2 PCB design of CPU Board

The PCB sheet is shown in Appendix D

The design file is saved in the CD. :\CPU\CPU.PCB

The Gerber files of this design are saved in the CD. :\CPU\Geber. Next are the explanations of them:

Top Overlay: Slave11.GTO

Top Layer: Slave11.GTL

Bottom Layer: Slave11.GBL

Mechanical Layer 1: Slave11 .GM1

Bottom Solder Mask: Slave11.GBS

Apertures list: Slave11.apt

NC Drill binary file: Slave11.DRL

NC Drill report file: Slave11.DRR

2.2.3 The components list of the CPU Board

Bill of Material for SLAVE.Bom

Used	Part Type	Designator	Footprint	Description
1	2U2	E1	ELECTRO0.1	Electrolytic Capacitor
1	4PIN	J8	SIP4	Jumper
1	4PIN	J9	SIP4/2.5MM	Jumper
2	4U7	E3 E4	ELECTRO0.2	Electrolytic Capacitor
4	5k	P1 P2 P4 P5	SIP3	Socket
1	8PIN	J4	SIP8	Socket
1	11.059M	C3	RAD0.2	Oscillator
1	16PIN	J1	IDC16	16Pin IDC Socket
2	22p	C1 C2	CAP0.2	Capacitor
1	40PIN	J7	IDC40	40 Pin IDC Socket
1	47k	R1	AXIAL0.4	Resistor
1	74LS14	U2	DIP14	IC
1	74LS74	U17	DIP14	IC
1	74LS373	U3	DIP20	IC
1	100	R5	AXIAL0.4	Resistor
1	100k	P3	SIP3	Potentiometer
1	101	R15	AXIAL0.4	Resistor
1	104	R14	AXIAL0.4	Resistor
20	104	C5 C6 C7 C8 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C25 C26 C28	CAP0.2	Capacitor
1	105	C36	CAP0.2	Capacitor
4	105	E2 E5 E6 E7	ELECTRO0.1	Electrolytic Capacitor
1	220U	E8	ELECTRO0.1	Electrolytic Capacitor
4	241	R12 R13 R17 R18	AXIAL0.4	Resistor
8	471	R2 R3 R6 R7 R8 R9 R10 R19	AXIAL0.4	Resistor
3	473	R4 R11 R16	AXIAL0.4	Resistor
2	7406	U12 U16	DIP14	IC
1	89c52	U1	DIP40	IC micro-controller

1	62256	U4	DIP28	IC SRAM
1	DB9	J5	DB9RA/F	9 pin D-type Socket
2	DB9	J2 J3	DB9RA/M	9 pin D-type Socket
4	EMIFIL	C4 C9 C23 C29	SIP3	EMI Filter
4	LM371	U5 U6 U7 U8	TO-220	IC Regulator
1	MAX232	U13	DIP16	IC
1	MAX889	U11	SOIC-8	IC
1	MAX3391	U14	TSSOP-14	IC
1	MC3486	U9	DIP16	IC
1	MC3487	U10	DIP16	IC

2.2.4 Software design of micro-controller 89c52

This design file (Source Code) and its explanations are saved in CD. :\CPU\acq10.asm

The definitions of the variables in this program is listed bellow:

```
ON_SENDING BIT 00H
NEW_MESSAGE BIT 01H

RESET_ACQ           BIT 93H
Refresh             BIT 95H
RTS_OUT             BIT 96H
CTS_IN              BIT 97H
TRIGGERED           BIT 0B2H; INT0
POWER_INDICATOR     BIT 0B4H; T0

COMMAND             BYTE 7FH
RECEIVED_POINT      BYTE 7EH
DATA_TYPE           BYTE 7DH
ADDRESS             BYTE 7CH
STORE_POINT_H       BYTE 7BH
STORE_POINT_L       BYTE 7AH

25H--32H ARE RECEIVED BUFFER
34H--45H ARE VERIFYING DATA BUFFER
SENDING BUFFER 7100H--71FFH
```

The flow chart of this program is shown bellow:

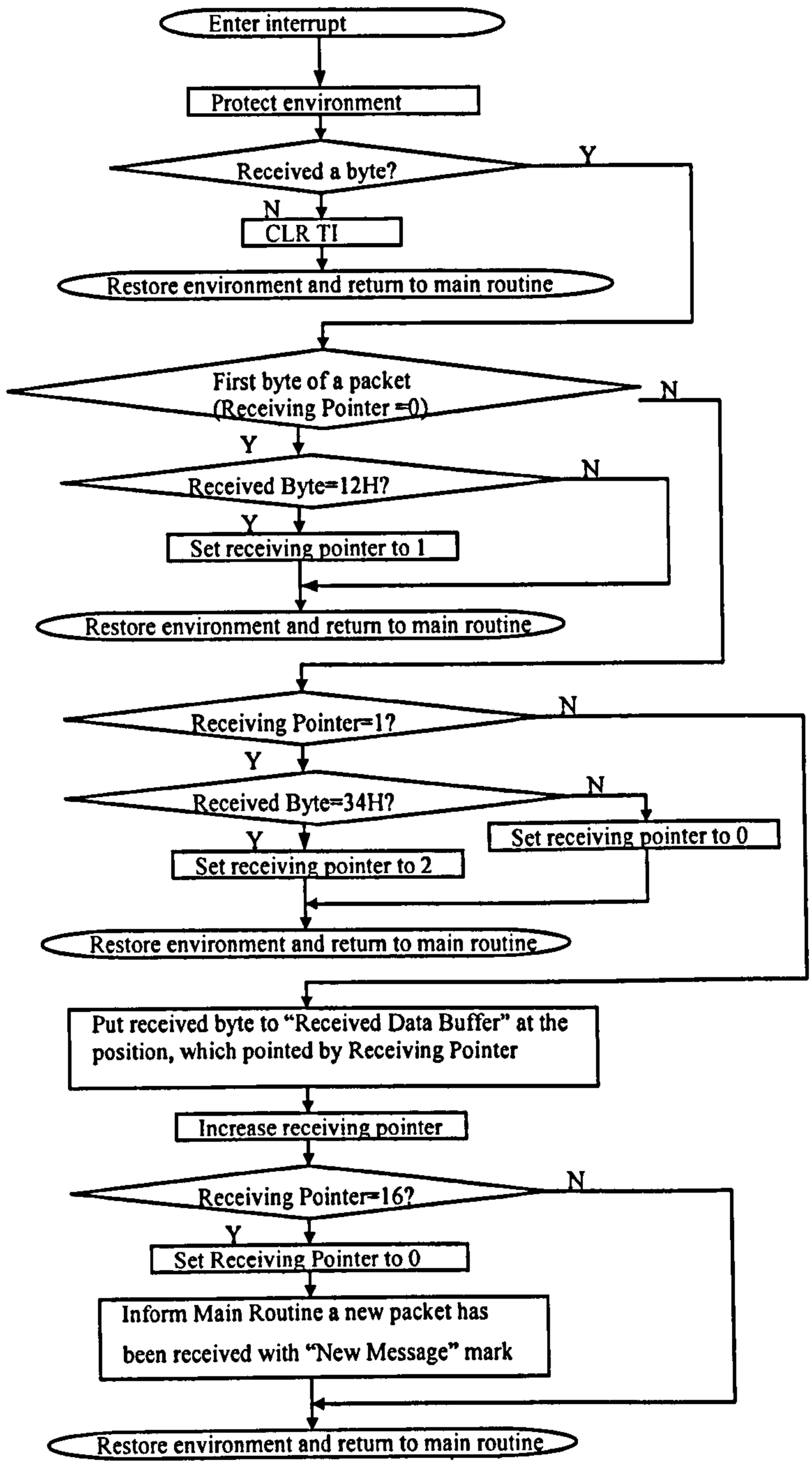


Figure 1: the flowchart for the MCU in RAU

2.2.5 Special notices for CPU Board

1) IC U9, U11, U10, U13, U14 are reserved for commissioning use. They were not assembled on the CPU Board

2) 4 Regulators LM317 need heat sinks with proper size taking the PCB space.

3) All the resistors should be selected from metal film 1% series

4) Soldering operations for each component are submitted to respective datasheets.

5) For further details of components selection and assembly, refer to the prototype board.

2.3 Enclosure

2.3.1 Layout of RAU Box

The supplier of this metal box is CPC Ltd., Store No. EN81256. It has 398mm length, 253mm wide and 50mm high. To house the circuit of the RAU, some holes should be made in front panel and rear panel. The next figure shows the rear panel of the RAU.

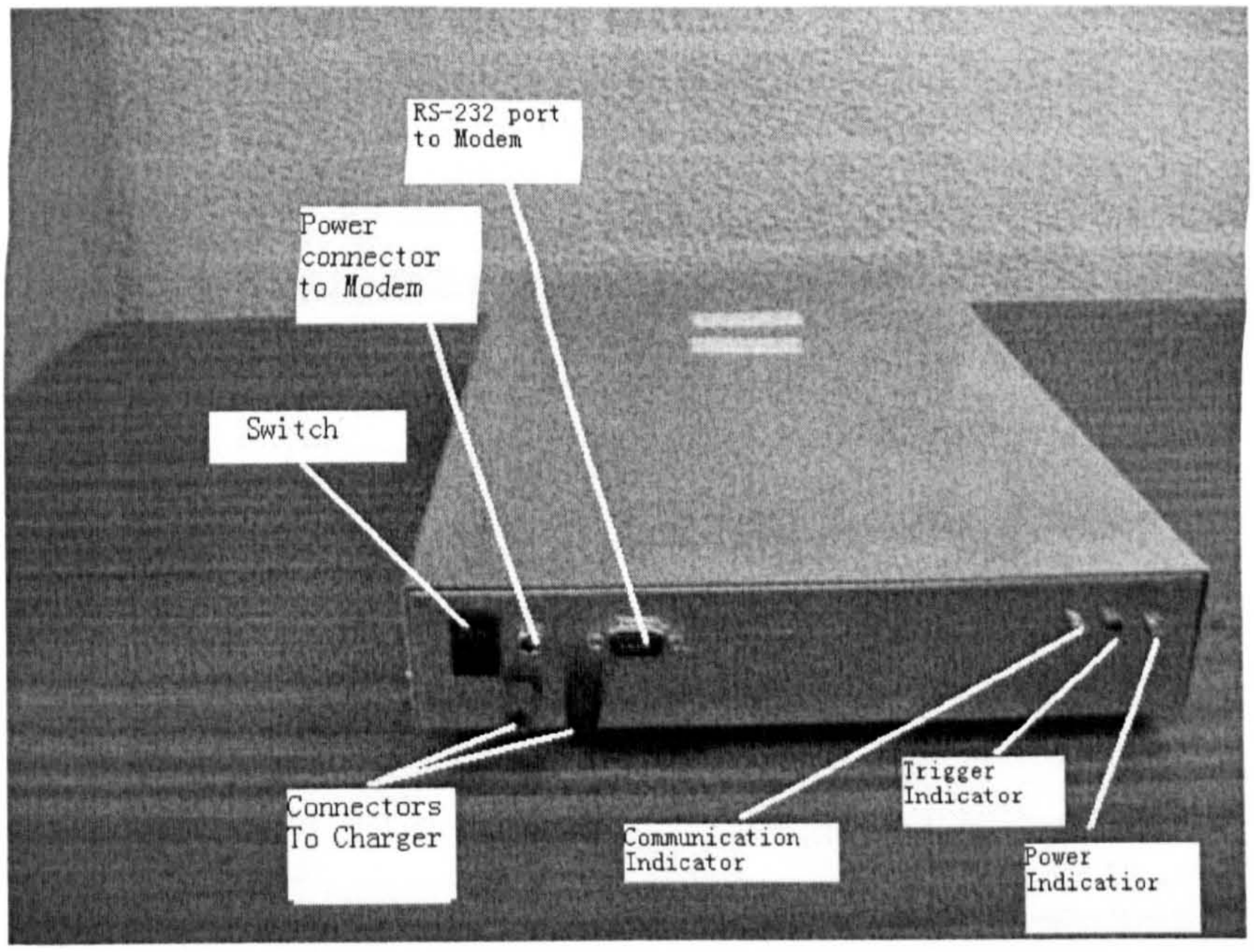


Figure 2: the rear panel of the RAU

Inside layout of the RAU is shown below:

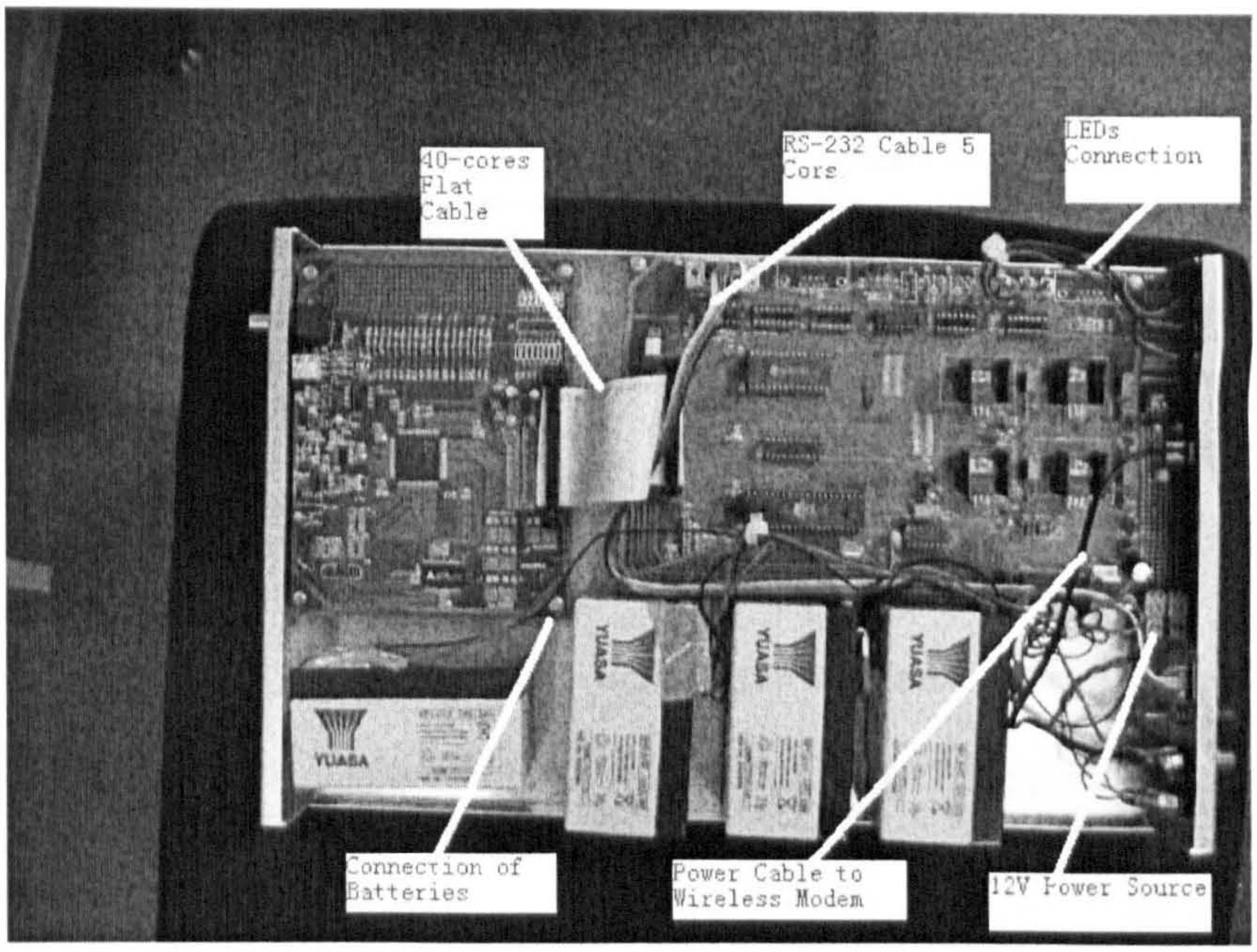


Figure 3: The inside layout of the RAU

There is a hole on front panel as shown below. The BNC socket on the Acquisition Board takes this hole with 12.5mm extension length.

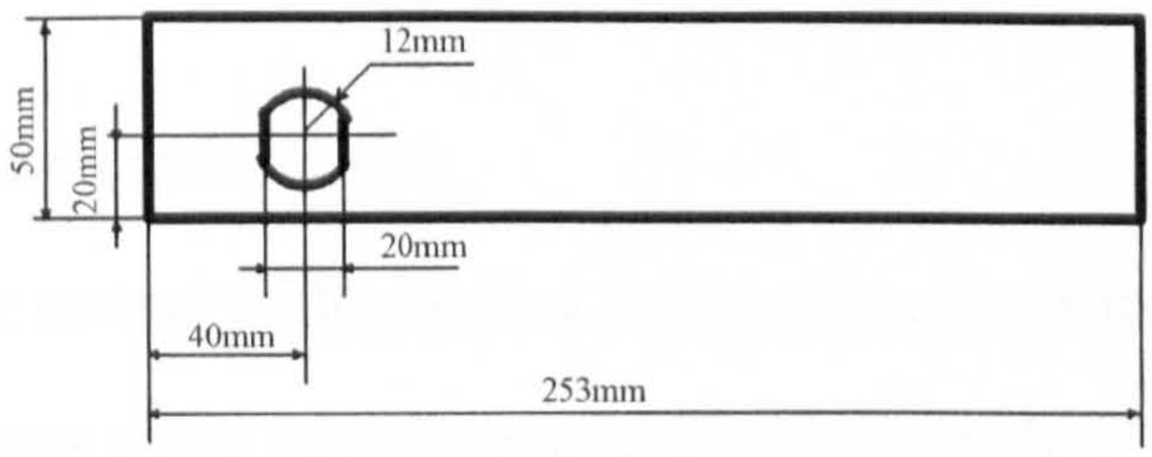


Figure 4: The drill guide diagram of the front panel of the RAU

There are 9 holes on the rear panel as shown below:

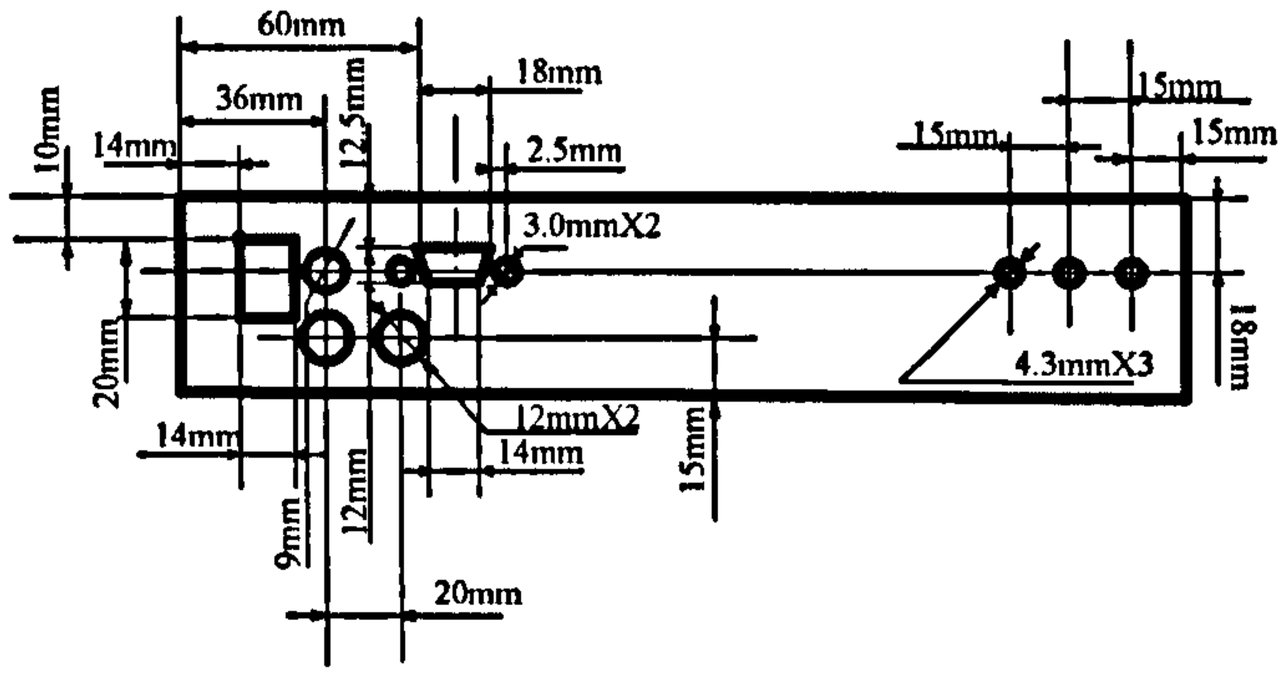


Figure 5: The drill guide diagram of the real panel of the RAU

Where three 3.0 mm holes in right hand hold three LEDs. (Supplied by CPC Plc. Order No. SC00473)

The trapezium hole with other two round holes on its both side are used for housing the DB-9 male plug.

9mm round hole in the left hand of the DB-9 plug houses the 3.5mm power socket, which is connected to wireless modem's power supply.

Two 12mm round holes is used to keep two poles, which are the connectors to a charger.

The rectangle hole in very right of the panel houses the power switch of the RAU.

2.3.2 Cable's specification

There are several cables applied for the connections inside of the RAU.

1) 40-cores cable, used for connection between the CPU board and the Acquisition Board. It is a 40-pin IDC plug to 40-pin IDC plug, 4.3 cm length, 40-cores flat cable. The signal definitions are listed below:

Table1: The signal list of 40-cares cable

Side A (CPU Board), 40-Pin plug		Side B (Acquisition Board), 40-Pin plug	
Core Number	Signal name	Core Number	Signal name
1	D0	1	D0
2	D1	2	D1
3	D2	3	D2
4	D3	4	D3
5	D4	5	D4
6	D5	6	D5

7	D6	7	D6
8	D7	8	D7
9	A0	9	A0
10	A1	10	A1
11	A2	11	A2
12	A3	12	A3
13	INT0	13	TRIGGERED
14	T1	14	(SPARE)
15	(SPARE)	15	(SPARE)
16	ETRIG	16	ETRIG
17	A15	17	A15
18	ALE	18	ALE
19	WR	19	WR
20	RD	20	RD
21	RESET	21	RESET
22	P1.3	22	P1.3
23	P1.4	23	P1.4
24	P1.5	24	REFRESH
25	VCC	25	VCC
26	VCC	26	VCC
27	GND	27	GND
28	GND	28	GND
29	+3.3	29	+3.3
30	+3.3	30	+3.3
31	GND	31	GND
32	GND	32	GND
33	-5V	33	-5V
34	-5V	34	-5V
35	GND	35	GND
36	GND	36	GND
37	RESERVED	37	RESERVED
38	RESERVED	38	RESERVED
39	GND	39	GND
40	GND	40	GND

2) 5 cores flat cable.

This cable links DB-9 socket on the panel and the DB-9 socket on the Acquisition Board. There are 5 signals are carried on this cable:

Table2: The signal list of 5-cores cable

Wire's colour and numbers	Signal' name
Black (1)	Signal ground
Brown (2)	TD
Red (3)	RD
Orange (4)	RTS
Yellow (5)	CTS

3) Two cores power cable for wireless modem.

This cable links the 8V power supply on CPU Board and 3.5mm Power socket on the panel. Black wire of this cable is ground line.

4) Two wires cable for LEDs

There are three of LED's cables linking the LEDs' sockets on CPU Board to the LED on the panel. The red wire is connected to the anode pole.

2.4 Special notices

1) PCBs are mounted in the box by screws. Each PCB has 4 mounting holes at its four corners. There are also 8 mounting hols on the bottom of the box. Screws take all these mounting holes to fix two PCB on the bottom of the box. Between PCB and the bottom, there are 8 spacers to isolate PCB and BOX.

2) The positions of the mounting holes on box are submitted to the real position of the PCB.

3) Four batteries are held on the bottom of the box by "hooks and loops fasteners".

4) For further details of the assembly of the RAU, refer to the prototype RAU.

2.5. Record of the rework modifications on PCBs.

1) In Acquisition Board, cut original connection between "Enable" pin of oscillator— U9:1 to GND. Connected U9:1 to VCC.

2) In CPU board, removed components MAX889 (U11) and its peripherals (E3, R14, P3, C36, E4). Used AD660 Building the power supply of –5V instead of MAX 889. For the details of the –5V power supply circuit, please refer to the datasheet of AD660 (From Analog Device Inc.).

3) In CPU board, added wires for RTS and CTS signals in RS-232 port: Added a wire connecting U13:13 to J2:8, added a wire connecting U13:14 to J2:7, added a wire connecting U13:12 to U1:8, added a wire connecting U13:11 to U1:7.

3. Communication network

3.1 Hardware configuration

The communication network is built-up with WirelessFutures™ products: Industrial 232-cable, which wireless modem based on Bluetooth technology. Slave modems are linked to RAU with RS-232 ports. Master modem is linked to PC with RS-232 Ports.

For the details of the wireless modem and its application, please refer to its datasheet.

3.2 software configuration

The software interface (the formats of data packets) between RAU and PC is show

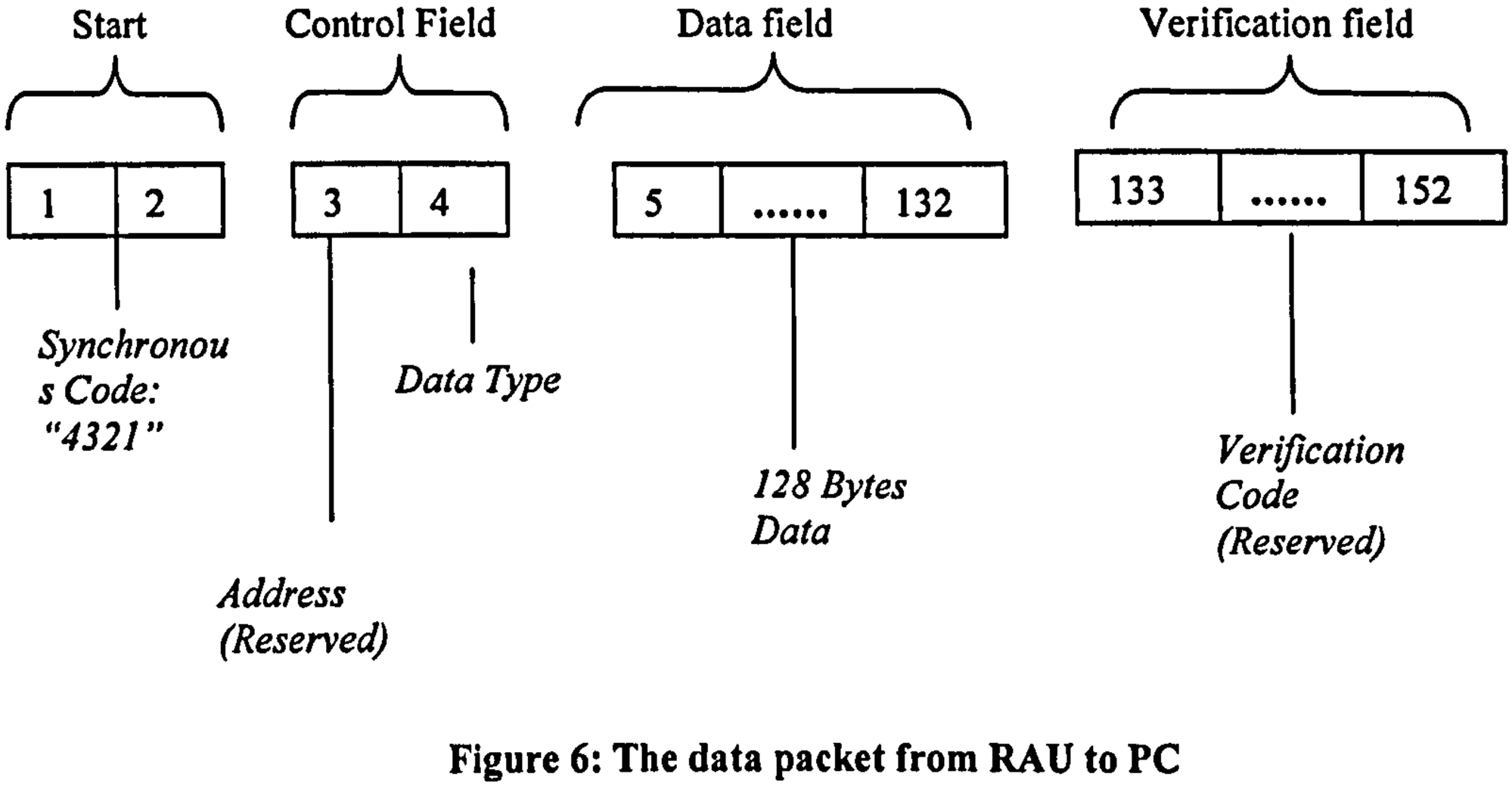


Figure 6: The data packet from RAU to PC

below:

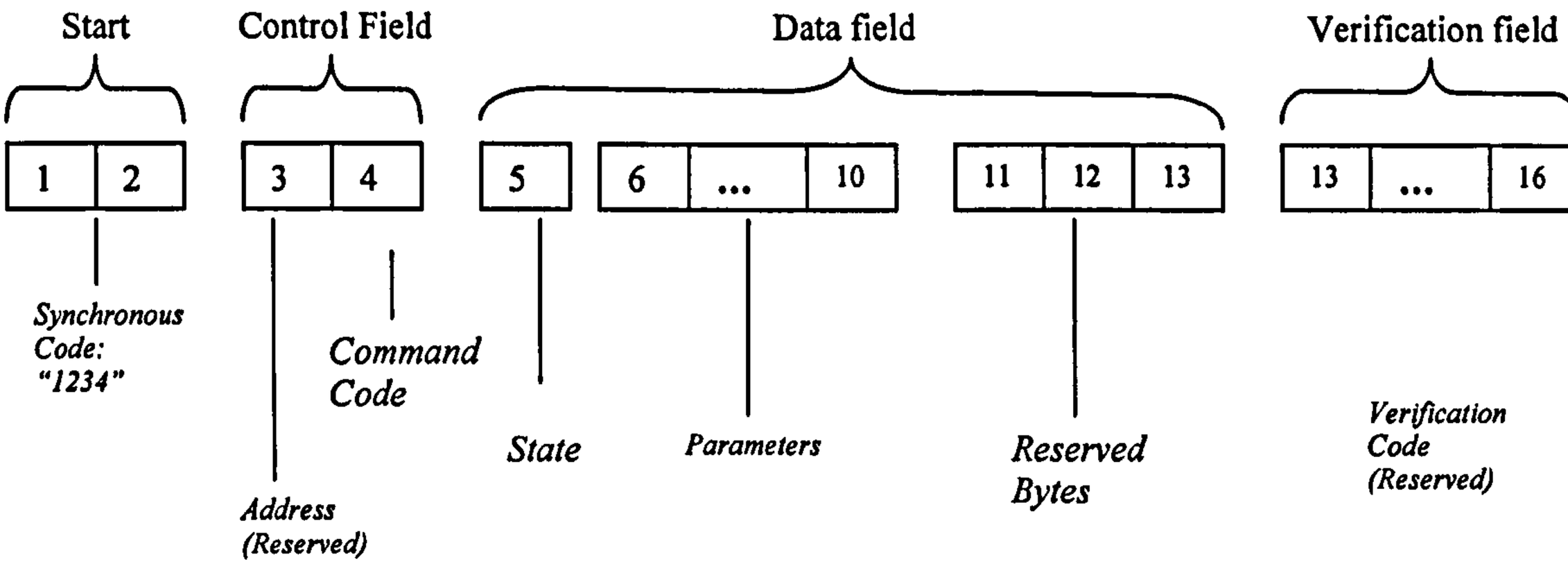


Figure 7: The data packet from PC to RAU

For the explanation of these data packets please refer to chapter 5 of the thesis "The wireless digital data acquisition system used for EMI measurement in substation"

4. PC software in this system

The source code of this program is written in Assembly language. This source code have been given in the CD at :\PC software\RAU01.asm and :\PC software\RAU02.asm. The executive programs are given in same folder named as RAU01.exe and RAU02.exe.

For the operation of this software, refer to "Wireless Digital EMI measurement system user manual"

RAU01.exe is used to operate RAU01 and RAU01.exe is used to operate RAU02.

To operate more RAUs, just change the Bluetooth address of the new modem, which new RAU connected to, in source code file of RAU01. (see the explanation in source code file).

The next is the flowchart of this program:

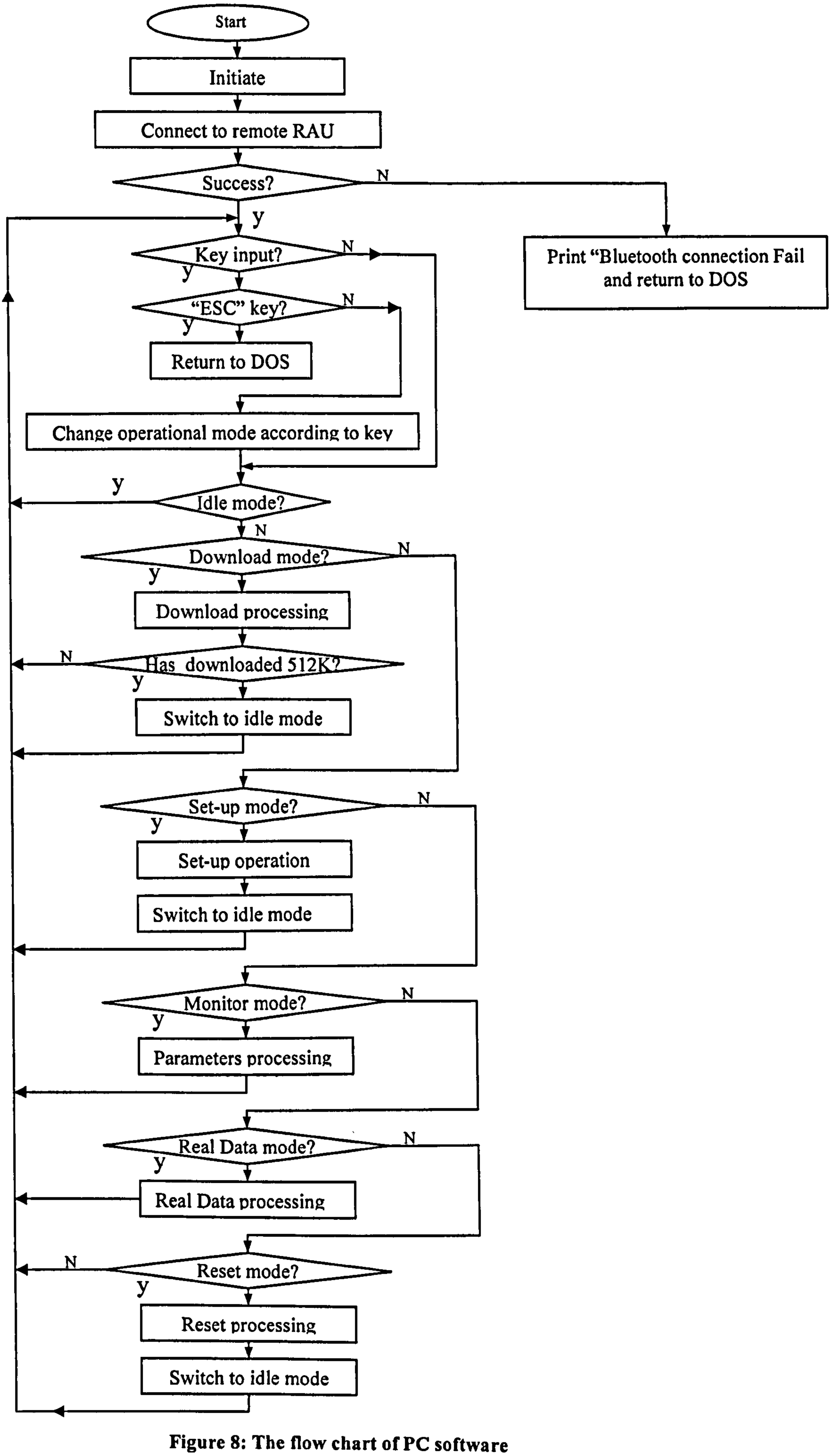


Figure 8: The flow chart of PC software

Appendix H: Publications

1) SIEW.W.H, WANG.Y, FAHEEM.M: "Digital Wireless Electromagnetic Interference (EMI) Data Acquisition System", Conf. IEEE, EMC 2005 Conference, Chicago, Aug. 8-12, 2005

2) SIEW.W.H, WANG.Y, FAHEEM.M: "Digital Wireless Electromagnetic Interference (EMI) Data Acquisition System", Conf., EMC Europe Workshop 2005, 19-21 Sep 2005, Rome, Italy

3) SIEW.W.H, WANG.Y, FAHEEM.M: "Digital Wireless Electromagnetic Interference (EMI) Data Acquisition System", British Electromagnetic Measurement Conf. 14-17 Nov, 2005, Teddington, UK

4) SIEW.W.H, WANG.Y, "The High-speed Acquisition Circuit and its Application in Embedded Design", "Journal of test and measurement", Sep, 2005, Taiyuan, China