University of Strathclyde
Department of Electronics and Electrical Engineering

Design, Analysis, and Modelling of Modular Medium-Voltage DC/DC Converter Based Systems

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This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

Signed: *Ahmed Aboushady* Date: 20 December 2012

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Abstract

This thesis investigates the design and analysis of modular medium-voltage dc/dc converter based systems. An emerging converter application is feeding offshore oil and gas production systems located in deep waters, on the sea bed, distant from the onshore terminal. The phase-controlled series-parallel resonant converter (SPRC) is selected as the dc/dc converter unit, for a 10kV dc transmission system. The converter has a high efficiency in addition to favourable soft switching characteristics offered by resonant converters which enable high frequency operation, hence designs with reduced footprints. The phase-controlled SPRC is studied in the steady-state and a new analysis is presented for the converter operational modes, voltage gain sensitivity, and analytically derived operational efficiency. The maximum efficiency criterion is used as the basis for selection of converter full load operational conditions. The detailed design of the output LC filter involves new mathematical expressions for interleaved multi-module operation. A novel large signal dynamic model is proposed for the phase-controlled SPRC with state feedback linearization. The model preserves converter large signal characteristics while providing a tool for faster simulation and simplified closed loop design and stability analysis. Using this model, a Kalman filter based estimator is proposed and applied for sensorless multi-loop output voltage control. The objective is to enhance the single-loop PI control dynamic response and closed loop stability with no additional sensors required for the inner loop state variables. Dynamic performance and robustness of the converter to operational circuit parameter variations are achieved with three new robust controllers; namely, Lyapunov, sliding mode, and predictive controllers. Finally, converter multi-module operation is studied, catering for voltage and current sharing of the subsea load-side step-down converter. To achieve a step-down voltage, the phase-controlled SPRC modules are connected in an input-series connection to share the medium level transmission voltage. Output-series and output-parallel connections are used to reach higher power levels. A new sensorless load voltage estimator is developed for converters remotely controlled. Matlab/Simulink simulations and experimental prototype results are used to substantiate all the proposed analysis techniques and control algorithms.

List of Symbols

C_o	Output filter capacitance (µF)
C_p	Resonant tank parallel capacitance (µF)
C_s	Resonant tank series capacitance (µF)
f	Inverter switching frequency (Hz)
f_0	Resonance frequency (Hz)
i_{Br}	Bridge rectifier input current (A)
i_{Brd} and i_{Brq}	*d*-axis and *q*-axis bridge rectifier input currents (A)
i_{Co}	Output filter capacitor current (A)
i_L	Resonant tank inductor current (A)
i_{Ld} and i_{Lq}	*d*-axis and *q*-axis resonant tank inductor current (A)
i_{Lo}	Output filter inductor current (A)
i_o	Output (load) current (A)
K_p, K_d and K_i	Proportional, Derivative and Integral PID controller parameters
L_c	Interconnecting cable inductance (mH)
L_l	Transformer leakage inductance referred to secondary (µH)
L_o	Output filter inductance (mH)
L_s	Resonant tank inductance (µH)
L_T	Total equivalent resonant inductance $L_T=L_l+L_s$ (µH)
M	Converter voltage gain (pu)
n	Transformer turns ratio (pu)
$P_{Cu\ filter}$	Output filter copper losses (W)
$P_{Cu\ tank}$	Resonant tank copper losses (W)
P_{Fe}	Transformer iron (core) losses (W)
P_o	Converter output power (W)
Q	Quality factor = Z_c/R_L (pu)
$\hat{Q}$	Quality factor corresponding to global efficiency maxima
R_{ac}	AC equivalent resistance of bridge rectifier=$(\pi^2/8)\times R_L$ (Ω)
r_c	Interconnecting cable resistance (Ω)
r_l	Parasitic resistance of transformer referred to secondary (Ω)
R_L	Load resistance (Ω)
r_{Lo}	Parasitic resistance of output filter inductor (Ω)

r_{Ls}	Parasitic resistance of resonant tank inductor (Ω)
r_T	Total equivalent resonant tank parasitic resistance $r_T=r_l+r_{Ls}$ (Ω)
v_{AB}	Inverter output voltage (V)
v_{AB1}	Fundamental inverter output voltage (V)
v_{AB}`	Inverter output voltage referred to secondary $=n\times v_{AB}$ (V)
v_{ABd}` and $v_{ABq}$`	*d*-axis and *q*-axis inverter output voltage referred to secondary (V)
v_{Br}	Bridge rectifier output voltage (V)
v_c	Control voltage signal (V)
v_{Cp}	Resonant tank parallel capacitor voltage (V)
v_{Cpd} and v_{Cpq}	*d*-axis and *q*-axis resonant tank parallel capacitor voltage (V)
v_{Cs}	Resonant tank series capacitor voltage (V)
v_{Csd} and v_{Csq}	*d*-axis and *q*-axis resonant tank series capacitor voltage (V)
v_{Lo}	Output filter inductor voltage (V)
v_o	Output (load) voltage (V)
v_o^*	Reference (desired) output voltage (V)
v_s	Input supply voltage (V)
T_s	Sampling period (μs)
Z_c	Resonant tank characteristic impedance $=\sqrt{L_T / C_s}$ (Ω)
ΔI_{Lo}	Output filter inductor ripple current (A)
ΔV_o	Output ripple voltage (V)
δ	Phase-shift control angle (°)
ω	Inverter switching angular frequency $=2\pi f$ (rad/s)
ω_0	Resonance angular frequency (rad/s)
ω_{pu}	Normalized frequency= ω/ω_0 (pu)
$\hat{\omega}_{pu}$	Normalized frequency corresponding to efficiency maxima (pu)

List of Abbreviations

ADC	Analogue to Digital Converter
CCC	Capacitor Commutated Converter
CLC	Central Limit Control
CSC	Current Source Converter
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
FEA	Finite Element Analysis
HVDC	High Voltage DC
IGBT	Insulated Gate Bipolar Transistor
IPOP	Input-Parallel Output-Parallel
IPOS	Input-Parallel Output-Series
ISOP	Input-Series Output-Parallel
ISOS	Input-Series Output-Series
IVS	Input Voltage Sharing
MFM	Multiple Frequency Modeling
MMC	Modular Multilevel Converter
OCS	Output Current Sharing
OVS	Output Voltage Sharing
PD	Proportional-plus-Derivative
PEBB	Power Electronic Building Block
PI	Proportional-plus-Integral
PLL	Phase Locked Loop
PRC	Parallel Resonant Converter
PWM	Pulse Width Modulation
SMC	Sliding Mode Controller
SPRC	Series-Parallel Resonant Converter
SRC	Series Resonant Converter
SVM	Space Vector Modulation
VSC	Voltage Source Converter
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Contents

Preface

A modular approach for connecting dc/dc converters is a technique proposed for constructing high power level converter architectures. The main advantages of a modular approach include, increased fault tolerance introduced by redundant modules, standardization of components leading to reduced manufacturing cost and time, power systems can be easily expanded, and higher power density of the overall system, especially with interleaving. System reliability is potentially improved due to redundancy but this must be traded off against the increased number of power electronic devices. Compared with direct series/parallel connection of power devices, modularity serves better when factors such as converter reconfiguration and power level scaling, as well as interleaving to reduce filter requirements, are considered. The main objective of this thesis is to design, analyse, model and control modular medium-power medium-voltage dc/dc converter based systems. A typical application considered for this modular approach is feeding subsea electrically actuated oil and gas production systems, from onshore terminals, but the proposed converter can be also applied to other applications. This thesis comprises seven chapters:

Chapter one provides an introductory overview of HVdc systems, in addition to a typical subsea project specification and requirements.

Chapter two presents a detailed review of existing high power dc/dc converter topologies in the literature and industry. According to the survey, the candidate topology for the subsea project is selected; namely the phase-controlled series-parallel resonant converter (SPRC). This will act as the main dc/dc converter building block.

Chapter three involves analysis of the phase-controlled series-parallel resonant converter steady-state characteristics. New relations and performance measures are derived. According to the steady-state measures, a new design procedure based on a maximum efficiency criterion is developed. This is used as basis for selection of the converter full load operational conditions. Circuit element design is also performed with emphasis on the nano-crystalline core transformer. The system design includes selection of resonant tank parameters in addition to the output LC filter design. New mathematical expressions are analytically derived for the output filter design with multi-module interleaved operation.

In **Chapter four** a novel large signal dynamic model for the phase-controlled SPRC is proposed. The model utilises a state feedback algorithm for linearization of converter non-linearity. The model preserves large signal converter dynamics, hence can be used for faster simulations in addition to simplified closed-loop design and stability analysis. Most importantly, the model can be used for online state variable estimation. The latter is used as basis for a new sensorless multi-loop PI output voltage controller to improve single-loop closed-loop stability and dynamics with no additional sensors.

Chapter five introduces three new robust controllers for output voltage control of the phase-controlled SPRC; namely, Lyapunov, sliding mode and predictive controllers. The proposed controllers increase converter robustness in response to external disturbances and circuit parameter variations which would typically occur in a hostile subsea environment. The proposed controllers also improve dynamic system behaviour.

C**hapter six** addresses multi-module operation of the phase-controlled SPRC with emphasis on voltage and current sharing. A novel control configuration for phase-controlled SPRC interleaved operation is proposed, common to both input series connection with both parallel and series output converter terminal connection. Load voltage is estimated to enable load voltage regulation without remote sensing. This is a potential advantage for the subsea project where manifolds are remotely located from the main subsea converter site. Also, the number of measurement sensors is reduced which reduces system complexity and eliminates noisy measurements resulting from long interconnecting signal cables.

Finally, in **Chapter seven** the author concludes the thesis, presenting the author's contribution, and suggestions for future research.

Dedication

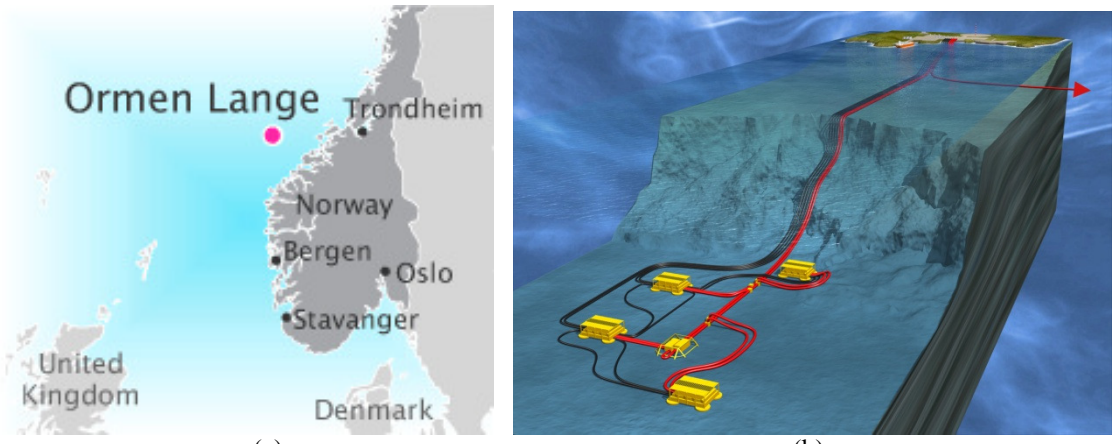
To the memory of my father…

To my mother and my fiancée…

Chapter 1

Introduction

As the search for oil moves into deeper waters and harsher environments, production is moving onto the seabed. Recently, there has been a significant trend in offshore oil and gas production, to eliminate offshore surface facilities and for the entire production system to be located on the seabed and connected back to an onshore terminal. The Ormen Lange field, shown in Fig. 1.1, is a good example of this approach, and is significant because it will supply 20% of the UK's gas consumption in coming years. The Ormen Lange field, 120 km from shore, came on-stream in September 2007, with peak production of 70 million cubic metres of gas and 50,000 barrels of condensate per day. Not a single installation is visible on the surface of the sea above Ormen Lange. All the installations are at sea depths of 800 to 1100 metres [1.1].



(a) (b)

Fig. 1.1: The Ormen Lange project: (a) location map [1.1] and (b) installations connected to a terminal back onshore at Norwegian mainland [1.2].

1.1 Subsea power distribution systems

Current requirements for electrical power for seabed oil installations call for relatively low power levels at relatively modest distances (10km) from surface power hubs. Pumps and compressors are all actuated by hydraulic fluid, so electric power necessary for valve on/off control is relatively low. For such systems, conventional ac power distribution systems are appropriate. The electrical requirements for the next generation of seabed installations pose significant technical issues. These issues are driven by a move to greater power transmission distance (step outs starting at 100km from the surface

power hub) and greater power requirements (10-15kW) due to the replacement of hydraulic-controlled pumps with pumps that are electrically driven [1.3].

The move to *All-Electric* subsea systems is likely to solve several problems in existing hydraulic-actuated systems. They can increase reliability, reduce maintenance arising from contamination of hydraulic fluid and umbilical blockages, permit condition monitoring, eliminate the need for hydraulic lines within the umbilical, reduce hydraulic fluid consumption thereby reducing costs, increase the speed of signal communication, and most importantly reduce the environmental risks from hydraulic fluid leaks.

1.2 DC versus AC for subsea transmission

In subsea power applications ac transmission faces problems due to the high capacitive charging currents drawn by long cables. This deteriorates the power factor and increases cable loss imposing a practical limit on the power that may be transferred. Given the same level of power transmitted as for ac cables, there are fewer physical restrictions limiting the transmission distance for HVDC submarine cables.

The use of dc power provides a solution to many problems associated with the next generation of subsea electrical power systems. The dc approach reduces reactive current, due to reduction of cable insulation capacitive ac effect, and reduces electrical cable loss due to absence of ac skin effect phenomenon. Moreover, compensation costs for dc lines are reduced as they do not require reactive power compensation. Some compensation may be necessary to allow for increased unloaded side voltage due to Frontier effect. There is considerable savings in installed cable costs. However, this is all achieved at the expense of increased use of solid-state energy conversion systems. Depending on the power level to be transmitted, savings can offset the higher converter station costs. In conventional power applications the economic break point for subsea HVDC versus HVAC is approximately 50km [1.4], [1.5] as shown in Fig. 1.2.

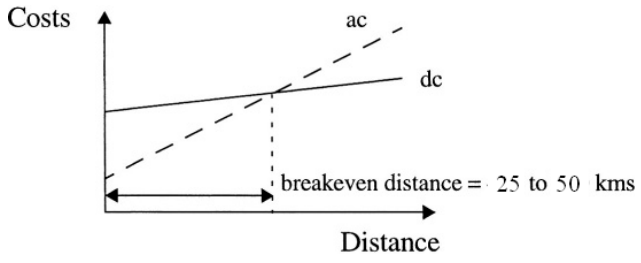


Fig. 1.2: Cost comparison for subsea cables operating with ac versus dc transmission.

1.3 High voltage direct current (HVDC) transmission

HVDC technology has characteristics which make it attractive for certain transmission applications. HVDC transmission is widely recognised as being advantageous for long-distance, bulk-power delivery, asynchronous interconnections and long submarine cable crossings [1.6]. Today there are many HVDC installations world-wide (in operation or planned for the near future) employing two distinct technologies; Conventional Line-commutated Current-Source converters (CSC) and Self-commutated Voltage-Source converters (VSC) [1.7].

1.3.1 HVDC power architectures

Two basic converter technologies are used in modern HVDC transmission systems:

(a) Conventional Current-Source Converter (CSC) HVDC

Conventional thyristor-based HVDC transmission represents a well-established technology used since the mid-1970s [1.4]. It represents a mature technology referred to as 'classic' HVDC. This approach employs back-to-back line-commutated thyristor converters as shown in

Fig. 1.3.

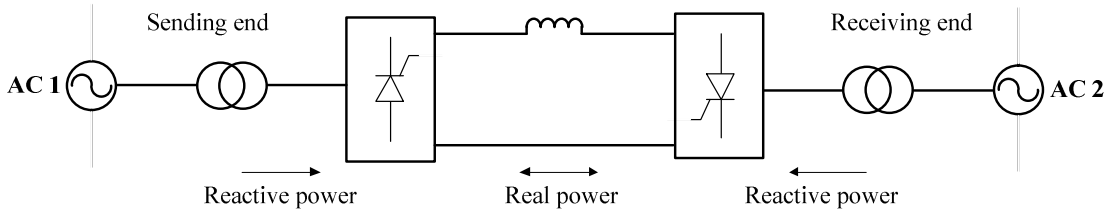


Fig. 1.3: HVDC system based on CSC technology with thyristors.

CSC-HVDC systems are installed at many different locations worldwide mainly for interconnecting two shore-based ac networks. This technology is, therefore, more suited for point-to-point transmission where the dc link connects to a stiff ac grid at either end. This technology is mainly established for bulk power transmission with one of the largest projects being the Itaipu system in Brazil at ±600kV, 6300 MW power level over 915km. The longest power transmission, 2,000km, in the world transmits ±800kV, 6,400 MW power from the Xiangjiaba hydropower plant to Shanghai in China [1.7], [1.8].

Numerous CSC-HVDC system configurations exist [1.7]:

(i) Back-to-Back CSC-HVDC System.

In this system, the two converter stations are located at the same site and there is no power transmission on a dc link over a long distance. A block diagram of a back-to-back CSC-HVDC system is shown in Fig. 1.4(a). It is used mainly for interconnecting ac systems with different frequencies (asynchronous interconnection).

(ii) Monopolar CSC-HVDC System.

In this configuration, two converters are used that are separated by a single pole line, and a positive or a negative dc voltage is used. Many HVDC subsea transmissions use a monopolar system with seawater acting as the return path. This configuration saves on the extra return cable which reduces cost, losses and maintenance requirements. However, it is not fault tolerant as only a single circuit exists for power transmission. Different monopolar schemes are shown in Fig. 1.4(b).

(iii)Bipolar CSC-HVDC System.

This is the most commonly used CSC-HVDC system configuration in applications where overhead lines are used to transmit power. The bipolar system is two monopolar systems. The advantage of such a system is that one pole can continue to transmit power when the other is out of service for whatever reason. In other words, each system can operate on its own as an independent system with the earth return. Due to poles operating at opposite polarities, the ground current is theoretically zero when both poles have equal currents. Various bipolar configurations used are illustrated in Fig. 1.4(c).

(iv) Multi-terminal CSC-HVDC System.

In this configuration, there are more than two sets of link connected converters. A multi-terminal CSC-HVDC system is shown in Fig. 1.4(d).

(b) Capacitor-Commutated Converter (CCC) HVDC

Converters with series capacitors connected between the converter valves and converter transformer were introduced in the late 1990's by ABB for weak-system applications, to provide commutation aid. This is a common problem for the line-commutated current source converters. Such a converter is referred to as capacitor-commutated converter (CCC) and is shown in Fig. 1.5.

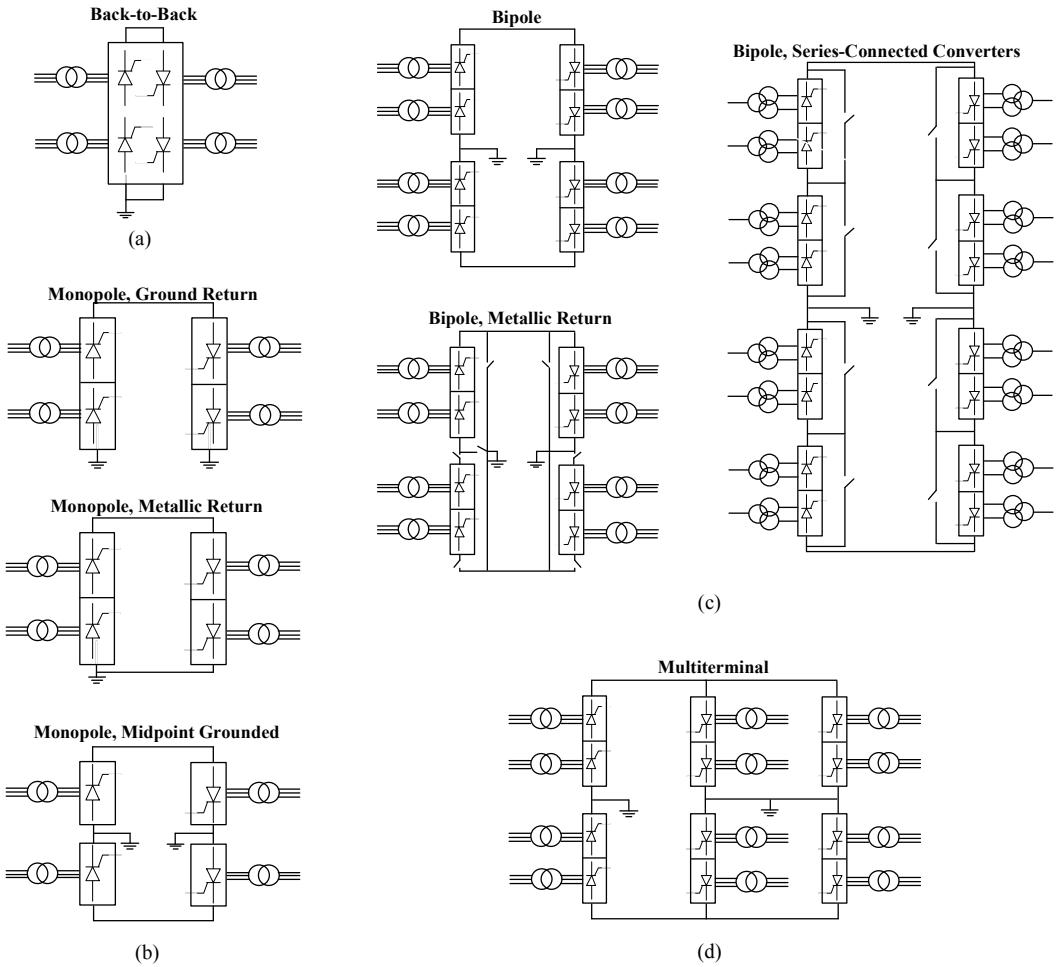


Fig. 1.4: CSC-HVDC system configurations and operating modes:
(a) back-to-back, (b) monopolar, (c) bipolar, and (d) multi-terminal.

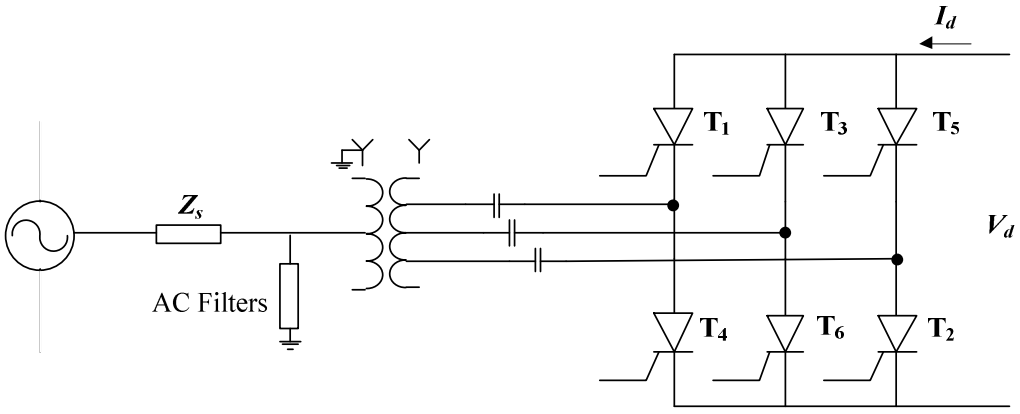


Fig. 1.5: Typical CCC configuration.

The line capacitor is in series with the leakage impedance of the transformer and the main valves. This has two-fold effects; the capacitor provides a forced commutation facility to the main valves and compensates for the leakage inductance (reactive power demand) of the converter transformer. The series capacitor provides some of the con-

verter reactive power compensation requirements automatically with load current and provides part of the commutation voltage, improving voltage stability.

Sizing of the commutation capacitor involves a compromise between conflicting requirements. Insufficient capacitance will cause a large over-voltage across the capacitor (and valves), and will not compensate sufficiently for the leakage inductance resulting in a lagging current drawn from the ac bus. Excessive capacitance will result in low over-voltages and will over-compensate for the demanded reactive power and may even draw a leading current from the ac system. In addition excessive capacitance has a cost penalty. Common design practise suggests that an economical capacitor size would be to cause, say, 10% over-voltage across the capacitor (and valves) as well as compensate for the reactive power demand to present unity power factor to the ac bus [1.4].

CCC converters are used in the 4 × 550 MW asynchronous Garabi tie between Brazil and Argentina and the 2 × 100 MW Rapid City tie between the eastern and western interconnected systems in the United States of America [1.4-6].

(c) Voltage-Source Converter (VSC) HVDC

Control limitations of conventional CSC-HVDC have led to the development of voltage source systems. Such CSC-HVDC limitations include:

- Commutation failures due to ac network disturbances;
- Coupled control of converter reactive and active power consumed or generated;
- Slow dynamic response due to converter operating at a multiple of line frequency;
- Inability to connect the CSC-HVDC system to a 'weak' ac network; and
- Need for bulky filters on ac and dc sides due to low operating frequency in addition to power factor correction capacitances on the ac side.

VSC-HVDC systems, also known as *Self-Commutated Converter Based Systems*, overcome the mentioned drawbacks by extending the principles of pulse width modulated (PWM) voltage source inverters to the 50kV-100kV range by utilizing modern semiconductor technologies, such as the Insulated-Gate Bipolar Transistor (IGBT). It is the continuous progress of high-voltage high-power fully-controlled semiconductors that has given rise to the VSC-HVDC technology. This technology is well-established for medium power transmission applications, with recent projects around 300-400 MW power levels. Fig. 1.6 shows a typical schematic of a VSC-HVDC system [1.7], [1.8].

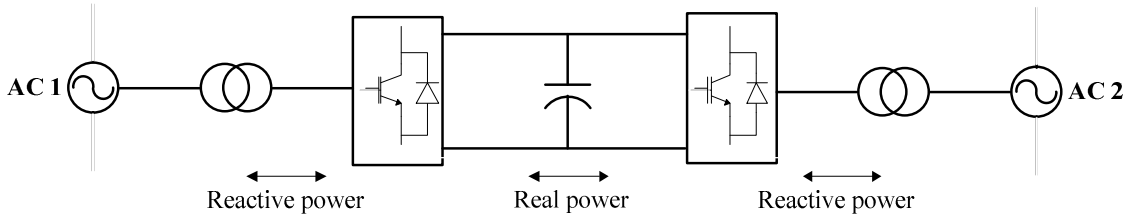


Fig. 1.6: HVDC system based on VSC technology using IGBTs.

VSC-HVDC systems represent recent developments in the area of dc power transmission technology [1.9]. Commercial experience with VSC-HVDC spreads over the last 15 years [1.10]. The breakthrough was made when the world's first VSC-based PWM-controlled HVDC system using IGBTs was installed in March 1997 (Hellsjön project, Sweden, 3 MW, 10 km distance, ±10 kV) [1.11]. The system is based on ABB's **'HVDC Light'** technology with series-connected IGBT converters. Subsequently, more VSC-HVDC systems have been installed worldwide [1.12-16], such as the "Troll A project" 2×41MW, ±60kV converter station installed in 2005 for Statoil, Norway 67 km offshore.

The simplest operational VSC topology is the conventional two-level three-phase converter. The converter is typically controlled with sinusoidal synchronous PWM, and the harmonics are associated with the switching frequency. The dc bus capacitor in Fig. 1.6 provides the required energy storage for power flow control and smooths out high frequency ripple. The VSC-HVDC system can also be built with other VSC topologies like multi-level converters. Numerous multi-level converter topologies are reported in the literature [1.17]. However, for HVDC applications there are two distinct topologies, namely, the neutral-point-clamped (NPC) converter [1.18] and the modular multi-level converter (MMC) [1.19, 20]. Techniques such as selective harmonic elimination (SHE) PWM and sinusoidal PWM for the control of these VSC topologies are presented in the literature.

Typically, it is desirable that a VSC generates PWM waveforms of higher frequency, compared to conventional thyristor-based systems. However, the operating frequency of these devices is also determined by the switching losses and the heat sink design, both of which are related to the throughput power. Switching losses, which are directly linked to high-frequency PWM operation, is a serious and challenging issue that needs to be addressed in VSC-based high-power applications. Other disadvantages of operat-

ing a VSC at high-frequency are electromagnetic compatibility/electromagnetic interference (EMC/EMI), transformer insulation stresses, and high frequency oscillations, which require additional filters [1.7].

Installed VSC-HVDC systems are limited to point-to-point application. Recent research has investigated the use of this technology for multi-terminal systems.

1.3.2 Challenges of subsea oil and gas HVDC transmission

There are a number of related areas in which dc transmission/distribution is established or receiving significant research effort. However the dominant issues for the subsea application may differ from those of related dc power systems. Such issues for subsea systems include:

- *Lifetime and reliability requirements.* Technology choices for subsea energy conversion systems may differ from those where access and maintainability issues are less significant. This, for instance, raises the trade-off issue between converter voltage rating and cable losses which may differ from surface systems.
- *Weight and volume constraints*. Systems must be designed that are compatible with subsea pressure housings and assembly systems. Power density requirement is likely to differ from that of surface systems.
- *Connections and terminations.* Operating voltage must be compatible with insulation levels practical for subsea electrical connectors and cables.
- *Power electronics losses and cooling.* Power semiconductor devices introduce conduction and switching losses which must be dissipated by the cooling system. The loss heat management systems must be compatible with subsea enclosures. Lifetime and reliability issues will limit the use of coolant pumps and agitator fans.

1.4 All-Electric subsea power distribution project

1.4.1 Outline and objectives

The project's objective is the analysis and design of a fully modular power distribution system architecture for subsea applications. Offshore nodes for oil and gas extraction are to be connected to a terminal onshore with an *All-Electric* actuation system for the subsea pumps and compressors. Fig. 1.7 shows the layout of the required system.

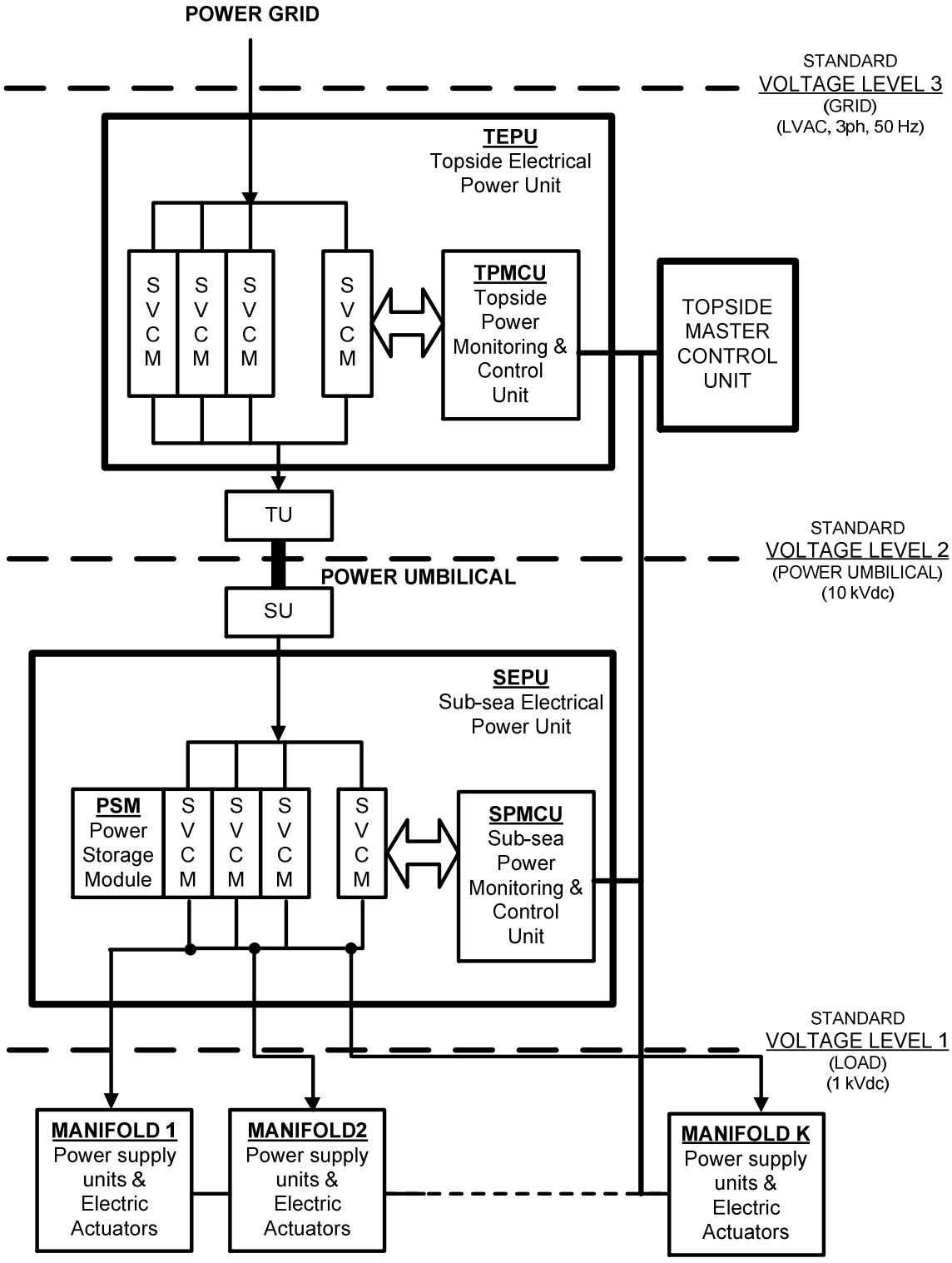


Fig. 1.7: Layout of the fully modular power distribution system architecture for subsea applications.

The topside electrical power unit (TEPU) comprises a number of standard voltage conversion modules (SVCMs) for the conversion of LVAC, three-phase 50 Hz grid power to a MV/HVDC level at the umbilical for subsea transmission. Typically, the design is

for a transmission voltage of 10 kVdc feeding loads totalling 10-15 kW. Power is transmitted subsea through the umbilical for step outs starting from 100 km where a subsea power station or subsea electrical power unit (SEPU) is situated. The purpose of the SEPU is to step down the MV/HVDC at the umbilical to load level voltage, typically 1 kVdc. It acts as the main co-ordinator to manifolds located in the surround.

Current commercially deployed HVDC systems (summarised in section 1.3.1) such as HVDC light could be sufficient to satisfy the project demands. However, with such relatively low power levels required (10-15 kW), medium-level transmission voltage (10 kVdc) and radial energy feed (that is, supply feeding loads with no inter-grid connection), the complex and costly HVDC light technology would be an excessive solution.

DC/DC converters are more compact and modular in design. They are being developed and applied in high-power applications, especially those associated with offshore renewables and subsea transmission where dc transmission is preferred. Not only do they offer a high power density technology solution, but also they act as dc transformers offering change of dc voltage/current levels at various transmission stages. This enables multi-terminal HVDC connections with different dc voltage levels as well as feeding different loads at different locations with different voltage/current requirements. Fig. 1.8 shows a single line diagram of the system with the proposed modular dc/dc converters.

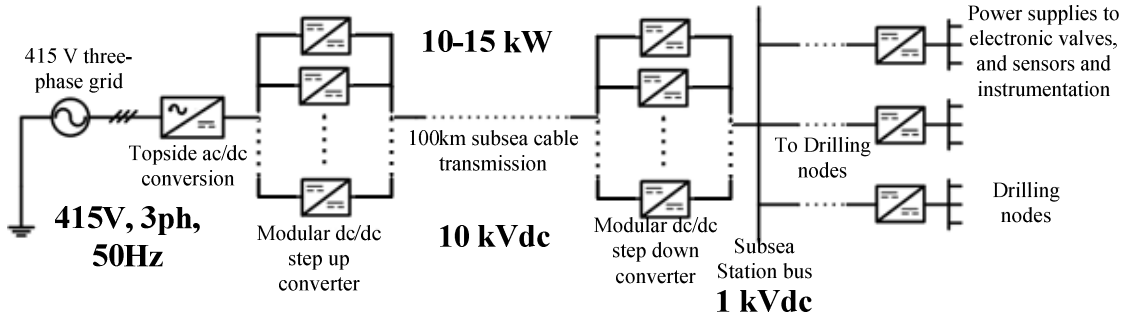


Fig. 1.8: Single line diagram of the subsea power distribution project with modular dc/dc converters.

Acting as the main building block for the subsea distribution system, the dc/dc converter modules are cascade-connected in series/parallel to reach the required voltage/power levels. For the on-shore electrical power unit, the dc/dc converters can be connected in an input-parallel output-series (IPOS) connection, to enable stepping up of the voltage to transmission level and to enable the required power level to be achieved through par-

allel connection at the input. Conversely, an input-series output-parallel (ISOP) connection is more suitable for the other end of the line where voltage is to be stepped down and the load currents to be shared between converter modules.

1.4.2 Features of the proposed architecture

The standard voltage conversion module (SVCM) for the topside and subsea electrical power units is fundamentally comprised of a dc/dc converter technology. This standard module will be the basic power electronic building block (PEBB) in a completely modular subsea power distribution system architecture [1.21]. The modular design has the following advantages over the existing hydraulic-actuated systems:

- High system efficiency;
- Relatively compact physical size (high power density);
- Cost-effective power umbilical;
- Longer step outs;
- High level of standardisation (ease of expansion and replacement);
- Feasible dynamic range windows for the input voltage;
- High flexibility and high level of power control; and
- Good fault tolerance, due to redundancy based on modularity.

The drawbacks of the proposed modular design are:

- High cost of power electronics;
- With increased number of electronic devices, modules and control signals, system complexity increases, hence reliability is reduced;
- Scarcity and complexity of connectivity solutions for subsea use;
- Relatively new and unproven design philosophy;
- Increased design complexity of proposed module;
- Significantly increased design effort;
- More difficult design optimisation; and
- Potentially not suitable for very high (multi-megawatt) power applications.

1.5 Scope of thesis

In the following chapters, the thesis continues as follows:

- Chapter two presents a detailed literature review of existing high power dc/dc converter topologies. According to the survey, the candidate topology for the subsea project is selected; namely the phase-controlled series-parallel resonant converter (SPRC) as the main dc/dc converter unit to be connected in different series/parallel connections to meet the required high power medium voltage project requirement.
- In chapter three, steady-state analysis of the phase-controlled series-parallel resonant converter is performed including presentation of new derived relations and performance measures. According to the steady-state measures, a detailed design procedure for circuit parameter values and optimum converter operating conditions is presented. The design includes analysis for single-module and multi-module operation issues. This includes the design of a high-frequency nano-crystalline core transformer, and output filter design using derived expressions for multi-module interleaved converter operation.
- In chapter four, the transient behaviour of the phase-controlled SPRC is studied. A novel linearization algorithm for the converter non-linear large signal model is derived using a state feedback technique. This enables linear control and stability analysis, closed-loop design, and most importantly enables the use of the model for online state variable estimation. The latter enables the derivation and implementation of a new sensorless multi-loop controller to improve the closed loop stability and dynamics compared with single-loop output voltage control.
- In chapter five, three new robust controllers are proposed for output voltage control of the phase-controlled SPRC. The controllers increase converter robustness in response to external disturbances and circuit parameter variation which would typically occur in the hostile subsea environment. The proposed controllers also improve dynamic system behaviour in contrast to conventional PI control.
- In chapter six, the multi-module operation of the phase-controlled SPRC is studied with the voltage and current sharing problem addressed. A novel load voltage estimation algorithm is proposed to enable load voltage regulation without remote sensing; a potential advantage for the subsea project where manifolds are remotely located from the main converter site. This reduces the number of measurement sensors required and eliminates noisy measurements resulting from long interconnecting signal cables.

- In chapter seven, the author gives the thesis conclusions, contributions, and suggestions for future research

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Chapter 2

High Power DC/DC Converters

In many industrial applications, it is required to convert a fixed-voltage dc source into a variable-voltage dc source [2.1]. A dc/dc converter converts directly from dc to dc and is therefore very commonly named as a *dc transformer* with the possibility of stepping up or down a dc voltage source. DC/DC converters are a common technology for renewable energy grid integration [2.2, 3], dc microgrids [2.4], HVDC applications [2.5], offshore oil/gas systems [2.6], and interfacing energy storage units with UPS systems [2.7]. Demand on high-power dc/dc converters became more popular due to increasing interest in dc transmission and distribution. This necessitates the interface of different dc voltage levels; hence the rapidly emerging high-power dc/dc converter technologies.

This chapter reviews the basic dc/dc converter configurations that are suitable candidates for high-power applications. In the first section, basic dc/dc converters are described from the perspective of the main specifications that characterize high-power operational and design requirements. In section two, series and parallel dc/dc converter connections are reviewed as a potential technique to attain high-power levels with a modular approach. In section three, existing high-power dc/dc converter technologies in the literature and for industrial implementation are reviewed. Finally in section four, in the light of the discussion in the three previous sections, a candidate topology for the *All-Electric* subsea project is defined with justification of the selection reasons.

2.1 Basic dc/dc converters

Basic dc/dc conversion is achieved using switched-mode PWM (hard switched), or resonant-mode (soft switched) converters, allowing control and regulation of the output voltage. In terms of the switching technique, dc/dc converters can be broadly classified as in Fig. 2.1. In industrial applications, dc/dc converters are often required to meet all or most of the following specifications [2.8]:

- Isolation between the source and the load;
- High-power density for size and weight reduction;
- Controlled power flow direction;

- High conversion efficiency; and
- Input and output waveforms with low total harmonic distortion for small filters.

Fig. 2.1 shows a general classification of dc/dc converters. The mentioned converter types have been well known for many years and have been thoroughly considered and analysed in the literature [2.9, 10]. The field of dc/dc converters has continuously been of interest to power electronics researchers. Their high efficiency and power density features made them attractive to many industries.

Fig. 2.2 illustrates the basic principle of a dc/dc converter in which the ac mains input is rectified, smoothed, and supplied to a high frequency transistor-based converter. The converter output is rectified and filtered to give the required dc output voltage. A high-frequency transformer is employed if an isolated output is required [2.10]. This functional block diagram is generalised for all types of dc/dc converters where the transistor-based converter may either be controlled with variable or fixed frequency PWM techniques. Design and operational characteristics for dc/dc converters in high-power applications are discussed in the following sub-sections.

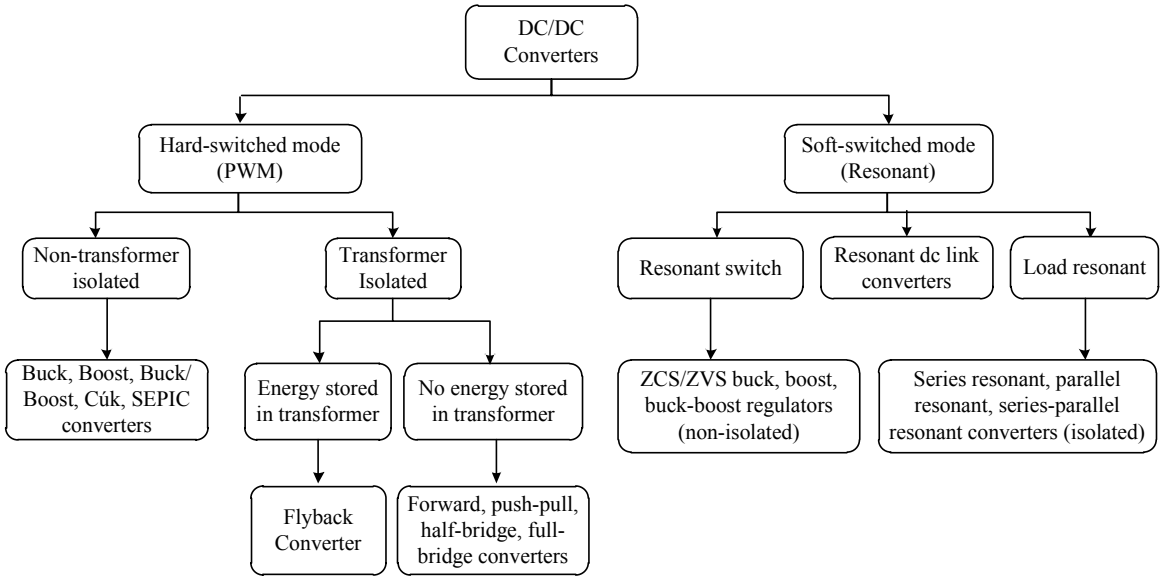


Fig. 2.1: General tree classification of dc/dc converters.

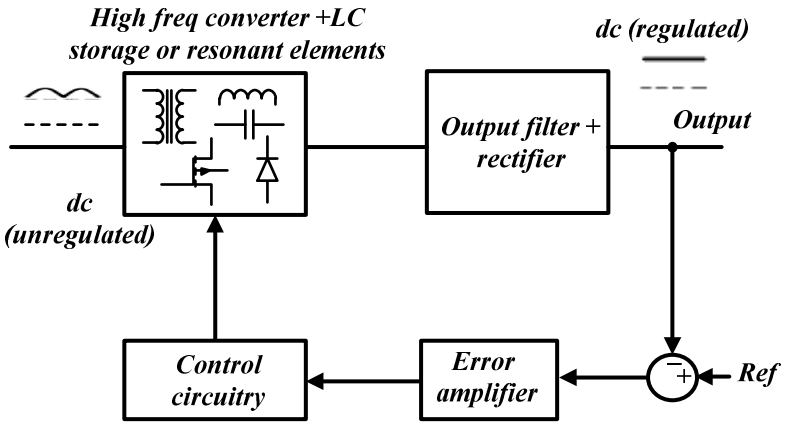


Fig. 2.2: Functional block diagram of dc/dc converters.

2.1.1 Transformer isolation

In many applications, it is desirable to incorporate a transformer into the switching converter to obtain electrical isolation between the converter input and output. For example, in off-line power supply applications, isolation is usually required by regulatory agencies. This isolation could be obtained by simply connecting a 50 or 60 Hz transformer at the power supply ac input terminals. Transformer size can be roughly approximated to vary inversely with frequency, hence incorporation of the transformer within the converter means it operates at the converter switching frequency (tens or hundreds of kilohertz) which leads to a significant reduction in transformer size. Also when a large step-up or step-down conversion ratio is required, the use of a transformer can allow better converter optimization. By proper choice of the transformer turns ratio, the voltage and current stresses imposed on the transistors and diodes can be minimized. This leads to better efficiency and lower cost. However, volt-second balance must be maintained on the transformer magnetizing inductance. Failure to achieve this results in transformer saturation and, usually, destruction of the converter. The means by which transformer volt-second balance is achieved is known as the *transformer reset* mechanism [2.11].

From Fig. 2.1, the half-bridge, full-bridge, forward and push-pull converters are commonly used isolated versions of the buck converter. The flyback converter is an isolated type of buck-boost converter. Isolated variants of the SEPIC and Cuk converters also exist in addition to transformer-isolated versions of resonant converters. These are mainly load-resonant converters where a transformer is placed in the intermediate ac resonant tank circuit.

2.1.2 Switching loss

Switching losses impose an upper limit on switching frequencies of practical converters. During the switching transients, the semiconductor switch voltage and current are simultaneously high. Consequently, the semiconductor switch experiences high instantaneous power loss. This can lead to significant average power loss, even though the switching transitions are short in duration. Switching loss causes converter efficiency reduction as the switching frequency increases.

Significant energy can be lost during the slow switching periods of minority-carrier semi-conductor devices such as BJTs, IGBTs, and thyristors. The diode reverse recovery process induces substantial additional energy loss in the transistor during the transistor turn-on transition. The energy stored in the semiconductor output capacitances is dissipated during the transistor turn-on transition. Energy stored in transformer leakage inductances and other stray inductances is usually dissipated by the transistor during the turn-off transition. The total switching power loss is equal to the sum of the aforementioned energy losses, multiplied by the switching frequency [2.11]. In this respect, soft switched converters offer an advantage over hard switched types. The former enables the use of LC elements operating above or below resonance to obtain zero-voltage (ZV) or zero-current (ZC) switching of transistors hence reducing switch turn-on or turn-off losses respectively. However, this is usually at the expense of marginal increase in conduction losses due to the additional circulating resonant currents. Fig. 2.3 shows a comparison of the switching losses magnitude between soft and hard switched dc/dc converters.

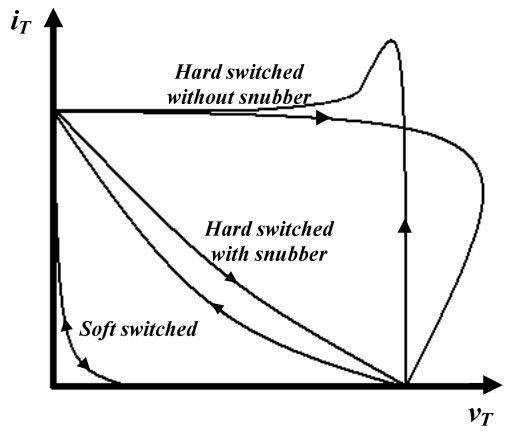


Fig. 2.3: Comparison of switching conditions in hard and soft switched transistors.

2.1.3 Power density

The size and weight of a dc/dc converter are directly related to those of its magnetic components (transformers and inductors), filters and other energy storage elements like capacitors. A high operating frequency generally means smaller size of magnetic, storage and filter elements. Due to their reduced switching losses, soft switching converters enable the increase in switching frequencies to levels higher than hard switched types and hereby enable realisation of such reduced footprint. However, the reduced component size is usually traded for a higher number of circuit elements.

2.1.4 Power flow direction

The conventional buck, boost and buck-boost converters are single quadrant converters. Most semiconductor elements only conduct unipolar current in the on state, and block unipolar voltage in the off state. This implies that, for proper functioning of the switch network, the source voltage, load voltage, and inductor current must all be positive. Consequently, the converters allow instantaneous power to flow in one direction only: source to load.

Bi-directional (regenerative) power flow can be obtained with a current-bidirectional two quadrant realization of the switch network. An example is illustrated in Fig. 2.4, in which a dc/dc converter interfaces batteries (low voltage side) to a higher voltage dc bus. The anti-parallel-connected transistors and diodes form current-bidirectional switches. Transistor Q_2 is driven with the complement of the Q_1 drive signal, such that Q_2 is off when Q_1 is on, and vice-versa. To charge the battery, the inductor current i_L is positive and flows through transistor Q_1 and diode D_2. To discharge the battery, the current reverses direction, and flows through transistor Q_2 and diode D_1. In both cases, the battery voltage is less than the main high voltage dc bus. The magnitude of the battery current can be controlled via adjustment of the duty cycle of Q_1 and Q_2 [2.11].

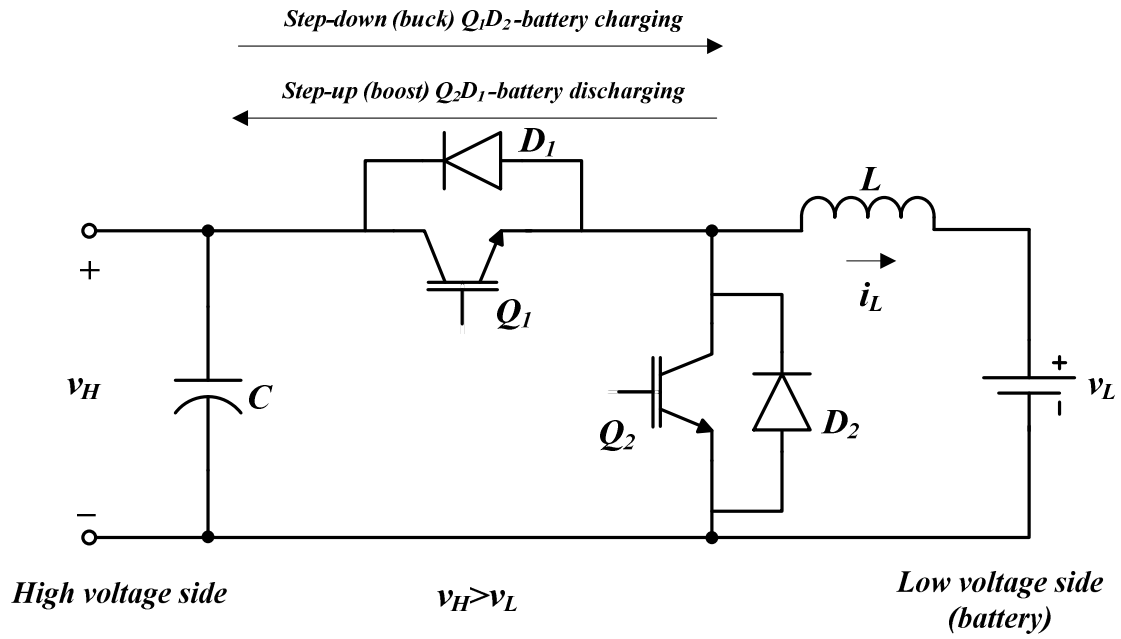


Fig. 2.4: A buck converter with two-quadrant bi-directional power flow.

2.1.5 Power capacity

For dc/dc converters to handle high-power levels, usually multi-switch converters (such as full-bridge types) are used rather than single-switch versions (such as buck or boost converters). It is impractical for a single switch configuration to handle megawatts or even hundreds of kilowatts. Moreover, multi-stage conversion (that is, converters with a dc/ac inversion stage then ac/dc rectification) enables the use of transformers, which not only provides galvanic isolation between the input and output but also can be adjusted to provide high voltage gains which optimize switch utilization. For instance, to achieve a step-down ratio of 10:1, the basic buck converter would need to operate with a 10% duty ratio. While if a full-bridge buck-derived converter is used with a step-down transformer of turns ratio 5:1, then the converter will operate with a 50% duty ratio which gives better switch utilisation (lower peak currents).

Another important factor that determines the power capacity of dc/dc converters is the efficiency limit. Converter losses should be minimized to enable high-power operation. Thus a highly efficient soft switching technique offers an attractive solution for high-power dc/dc converters. Therefore, it can be concluded that soft switching full bridge transformer isolated dc/dc converters offer a promising candidate technology for high-power dc/dc conversion.

In order to attain high-power operating levels with dc/dc converters as well as interfacing with different dc voltage levels, a potential technique is the series-parallel connection of dc/dc converters utilizing a modular approach. The next section reviews configurations and features of existing dc/dc converters connected in series-parallel to enable high-power capacities.

2.2 Series-parallel connection of dc/dc converters

Multi dc/dc converter modules connected in series-parallel have been the subject of vigorous previous research. In such an architecture, low-power, low-voltage (input and output) building block dc/dc converters are connected in any combination, series or parallel, both at the output as well as at the input sides, to realize any input-output specifications. The features of systems constructed from connecting multiple converter modules include:

- Ease of expansion of power system capability, by obtaining high-power dc/dc converters from low-power modules;
- Ease of thermal design as a result of each module handling only a part of the total power;
- Increased overall system reliability due to reduced thermal and electrical stresses on the power devices and components;
- Standardization of components leading to reduced manufacturing cost and time;
- Power system can be reconfigured to support varying input-output specifications;
- Improved system reliability due to N+1 redundancy; and
- High-power density converter designs, especially with interleaving.

Using series-parallel connection of dc/dc converters, four possible connections exist, namely, input-parallel output-parallel (IPOP), input-parallel output-series (IPOS), input-series output-parallel (ISOP), and input-series output-series (ISOS), as shown in Fig. 2.5. Each possible connection has its own specific features and applications [2.12, 13].

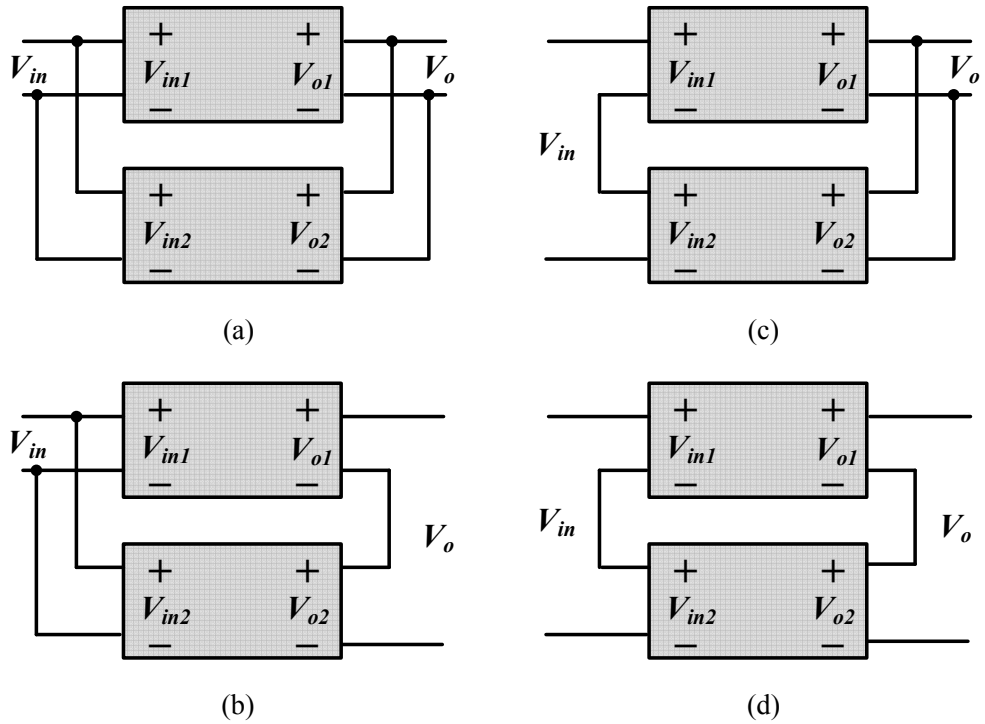


Fig. 2.5: Four possible input-output connections (a) IPOP, (b) IPOS (c) ISOP, and (d) ISOS.

2.2.1 Input-parallel, output-parallel (IPOP) connection

With the continued expansion of computer and telecommunication industries, distributed power systems consisting of paralleled modular converters delivering low output voltage and high output current are a popular practical configuration, where IPOP systems are among the most widely adopted [2.13, 14]. Non-isolated versions of buck or boost converters connected in parallel to obtain high-power-level power supplies were rigorously investigated [2.15-28]. IPOP connection of isolated power supplies (forward-type converters) have also been considered [2.29-31].

2.2.2 Input-parallel, output-series (IPOS) connection

IPOS connected dc/dc converters are common for low input voltage, high output voltage applications, hence are useful for voltage step up purposes. Examples of applications requiring high output voltages are X-ray equipment, photovoltaic systems, and electrostatic precipitators. A modular dc/dc converter employing IPOS connection with an isolated full-bridge-type connection, is presented in [2.32]. Standard dc/dc converters, with independent output voltage controllers, can be connected in series at the output achieving equal sharing of output voltage and input current. However, in order to obtain the advantages of modularity, such as redundancy, a common output voltage loop or an

output-voltage shared bus is required. A scheme based on a common output voltage loop and individual inner loops is discussed in [2.32]. An IPOS modular dc/dc converter with one common output LC filter has been presented in [2.33].

2.2.3 Input-series, output-parallel (ISOP) connection

A problem with input-parallel connections arises with high input supply voltages. Module input voltages are high meaning that possible series connection of switches is required to support the high input supply voltage. This is usually accompanied by the problem of static and dynamic voltage sharing. Also, conversion ratios for the individual modules will be high to obtain a low output voltage. In addition, with high input voltages, switching frequency is limited to reduce stresses and switching losses. For these reasons, it is essential to develop converters that can be connected in series at the input (Fig. 2.5(c) and (d)) with dynamic input-voltage sharing capability.

Apart from considerations of modularity, advantages of input-series connection include [2.12]:

- Enables the use of MOSFETs with low voltage rating, which are optimized for low on-state resistance, leading to higher efficiency;
- MOSFETs can be used instead of IGBTs for high input-voltage applications. Hence, switching frequency, and therefore, power density of such systems can be increased;
- No need for series connection of switches, since individual module input voltage is low, hence eliminating the problem of static and dynamic voltage sharing. Direct series connection of devices such as MOSFETs and IGBTs for high input voltage applications has been investigated [2.34]. However, the advantages of modularity, such as, scaling and reconfiguration are easily achieved with series connected converter modules, as opposed to series connected power devices;
- For high input-voltage applications, individual module conversion ratios are smaller than in input-parallel connections, hence smaller sized transformers are possible with a lower turns ratio and increased frequency of operation; and
- Possibility of interleaving to reduce filter ratings and improve transient performance.

ISOP systems are popular in applications where the input voltage is relatively high and the output voltage is relatively low, such as high-speed train systems [2.35], industrial drives [2.36], and undersea observatories [2.37]. The ISOP scheme was introduced only

at the concept level without detailed analysis in [2.32]. In [2.35], it has been implemented in a two-converter system with zero-voltage switching (ZVS) full-bridge converters employing charge control with input voltage feed forward. The control scheme accomplishes output current-sharing for output-parallel-connected modules as well as input voltage sharing for the input-series-connected modules for all operating conditions, including transients. Research activities by N. Mohan *et al*. involved modular schemes with input-series connections [2.12, 38-40]. In [2.38], a three-loop control scheme, including an input voltage loop, for ISOP connection, is presented. This is to ensure balanced sharing of the input voltage and output current among the converter modules. This design was improved [2.12] by a reference scheme where the input voltage of individual modules is the dynamic average of the total input voltage. This reference scheme minimizes interaction among the control loops. In [2.39], an ISOP scheme is proposed where the duty ratio to all converter modules is common. This scheme does not require a dedicated input-voltage or load-current-share controller. It utilises a common output voltage loop with an inner current loop from one converter only (dedicated master). It relies on the inherent self-correcting characteristics of the ISOP connection when the duty ratios of all converters are the same. However, the reliability and fault-tolerance of such a scheme are poor since the failure of the master converter results in failure of the overall system. Analysis, sensing and design methods along with experimental results for a fault-tolerant ISOP system using a common duty ratio scheme has been detailed in [2.40].

K. Siri *et al*. [2.41-44] have investigated methods for uniform input (or output) voltage distribution in ISOP (or IPOS) converters, utilising current-mode shared-bus commercial off-the-shelf (COTS) dc/dc converters. The authors propose unified approaches for uniform input (or output) voltage distribution. In addition the proposed controller produces system output voltage regulation and input current-limiting.

Ruan *et al*. [2.45] revealed the relation between the input-voltage sharing and output-current sharing of ISOP systems, and proposed an input voltage sharing control strategy which is independent of the output voltage regulation. L. Wand *et al*. [2.46] proposed an ISOP-connected modular dc/dc converter with interleaved (that is phase-shifted) equal duty cycle control. The main advantage of this technique is that it offers input voltage sharing with fewer sensors, hence reduced costs. Ripple in the input current and output

voltage are also reduced, therefore the input and output filter volumes are reduced leading to a higher power density. In [2.47], Kimball *et al*. proposed a sensorless current-mode approach for ISOP dc/dc converter topologies which results in a fast response to load steps, line disturbance rejection, accurate static and dynamic sharing, and high efficiency. A 20 kVA solid-state transformer was realised with ISOP connection of bidirectional phase-shifted dual-half-bridge converters [2.48].

2.2.4 Input-series, output-series (ISOS) connection

The main advantage of input-series connections is the suitability to high input voltages. If high output voltage is also needed then the individual converter modules have to be connected in series as well at the output [2.49]. In [2.50] an ISOS connected modular dc/dc converter scheme was proposed. A three-loop control scheme, similar to that introduced in [2.12] and [2.38], was proposed including a dedicated input voltage controller. This control scheme achieves equal sharing of the input as well as output voltages of the series-connected modules. The input voltage loop reference is the average of all the converter input voltages. Such a reference minimizes the interaction between the various control loops. Series connection of modular dc/dc converters has also found application in fuel cell systems. As in [2.51], a fuel cell, actively converting the supplied fuel to electricity, produces a typical output dc voltage of 0.6 V at full-load. Multiple cells are connected in series to obtain a high voltage. [2.52, 53] studied input and output voltage sharing issues in ISOS connected phase-shifted full-bridge converters. The former uses a common duty ratio scheme while the latter introduces duty cycle exchanging control to enhance voltage sharing.

Table 2.1 summarises the characteristics of the four possible input/output connections.

Connection	*Input voltage*	*Input current*	*Output voltage*	*Output current*
IPOP	low	high	low	high
IPOS	low	high	high	low
ISOP	high	low	low	high
ISOS	high	low	high	low

Table 2.1: A summary of the four possible input/output connection characteristics

2.3 Review of high-power dc/dc converters

Over the past ten years, high-power dc/dc converters became a candidate technology for HVDC systems, renewable energy integration, offshore oil/gas, industrial drives, and solid-state transformers. Fig. 2.6 shows a frequency versus power map of different high-power dc/dc converter research projects. According to existing technologies, high-power dc/dc converters can be considered to be in the 100kW-5MW power range.

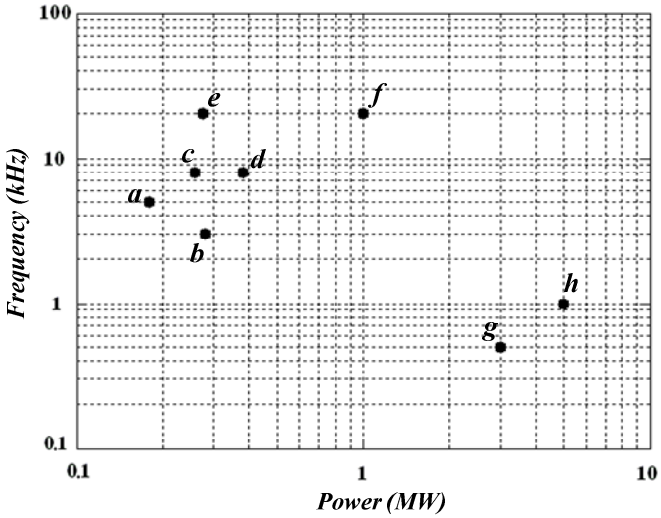


Fig. 2.6: Frequency vs. power map with different high-power dc/dc converter research efforts: (a) Alstom (15kV to 3.6kV) [2.54], (b) Uniflex (3.3kV to3.3kV) [2.55], (c) ABB (15kV to 2.8kV) [2.56], (d) Bombardier (15kV to 3.6kV) [2.57], (e) Freedm NCSU (24kV to 0.75kV) [2.58], (f) ETH Zurich (12kV to 1.2kV) [2.59], (g) KTH (33kV to 3kV) [2.60], and (h) E. ON RWTH (5kV to 5kV).

According to the need for galvanic isolation, high-power dc/dc converters can be classified into isolated and non-isolated types. The isolated types utilize transformers to realize voltage step up/down. For non-isolated converters, there are three methods to achieve voltage step up/down, namely magnetic, capacitive and magnetic/capacitive. Table 2.2 classifies various converters proposed in literature for use in different high-power dc/dc conversion applications. Table 2.3 presents a description, and the advantages and disadvantages of the high-power dc/dc converter topologies in Table 2.2 ordered with respect to their publication dates.

	Transformer isolated	***Non-transformer isolated***		
		Magnetic	***Capacitive***	***Magnetic and Capacitive***
Uni-directional power flow	[2.52, 53, 61-64]	[2.2, 65-67]	[2.68]	[2.69-71]
Bi-directional power flow	[2.48, 59, 61, 72-74]	-	[2.75]	[2.76]

Table 2.2: Classification of high-power dc/dc converters

Ref.	*Authors*	*Publication year*	*Dc/dc converter topology*	*Hard/Soft switched*	*Step up/down*	*Transformer isolated*	*Power flow direction*	*Power level*	*Advantages*	*Disadvantages*
[2.68]	G.G.Karady *et al.*	1991	Cockroft Walton voltage multiplier	Hard	Up	No	Uni-directional	100kW	- High efficiency - No magnetic components (light weight design is possible)	- High number of components (switches +caps) which reduces reliability - High switch current spikes - Poor voltage regulation
[2.69]	J.R. Cooper *et al.*	1991	Symmetric series connected resonance transformer	Hard	Up	No	Uni-directional	1MW	- High-power density - Has fault protection	-Uses high number of resonant elements to avoid use of high frequency transformer for step up. - Relatively low efficiency
[2.61]	R.Steigarwald *et al.*	1996	Full-bridge & diode rectifier	Hard	Down	Yes	Uni-directional	100kW	- Simple control - Constant frequency - No circulating current - Low ripple current in output cap (small size)	- High IGBT and rectifier stresses - High speed feedback diodes needed - Frequency limited (large transformer and output inductor)
			Phase-shifted full bridge and diode rectifier	Soft	Up/Down				- Simple control - Constant frequency - Resonant inductor built into transformer - High frequency operation possible, so reduced size and mass of magnetic elements	- Circulating current - Moderate IGBT and rectifier losses
			Variable frequency series-parallel resonant						- Sinusoidal currents - Soft switching, primary and secondary - Small output inductor - Low ripple current in output capacitor - Transformer leakage is no problem	- Variable frequency control hence difficult to control EMI, complex filtering and poor magnetic element utilization - Circulating current - Moderate IGBT losses - Low rectifier stresses - High voltage, high current resonant capacitors
			Auxiliary resonant commutated bridge		Down				- Low IGBT stresses - Constant frequency - No circulating current - Low ripple current in output capacitor	- Complex control - Auxiliary active devices needed - Output diodes hard switched - Two small resonant inductors
			Dual active bridge (DAB)		Up/Down		Bi-directional		- Constant frequency - No output filter inductor - Soft switching primary and secondary - Resonant inductance built into transformer - Controllable power flow direction	- Circulating current - Moderate IGBT stresses - Soft switching may be lost at light load - Eight active power switches - High ripple current in output capacitor - Relatively large transformer

Ref.	*Authors*	*Publication year*	*Dc/dc converter topology*	*Hard/Soft switched*	*Step up/down*	*Transformer isolated*	*Power flow direction*	*Power level*	*Advantages*	*Disadvantages*
[2.62]	R. Doncker *et al.*	2004	Three-phase series resonant converter	Soft	Down	Yes	Uni-directional	5kW	- High frequency (reduced component sizes). - Smaller output capacitance compared to single-phase version due to lower ripple in bridge output current	- Poor no load regulation - Higher number of resonant elements and switches compared to single-phase
[2.64]		2007						1MW	- Low conduction losses with GCTs - High efficiency	- Limited frequency due to use of GCTs. Magnetic elements not minimal in size.
[2.63]	L. Max *et al.*	2007	Full-bridge & diode rectifier (constant frequency control)	Hard	Down	Yes	Uni-directional	5MW	Same as [2.61] (Full-bridge and diode rectifier)	
			Full-bridge & diode rectifier (variable frequency control)	Soft					- IGBT zero turn on losses - Similar to phase-shifted bridge converter, soft switching obtained with minimal transformer built in leakage inductance.	- Large turn off snubbers necessary to reduce IGBT turn off losses. - variable frequency control means suboptimal transformer and filter design
[2.70]	D. Jovcic *et al.*	2009	Thyristor based resonant full-bridge & diode rectifier with rotating capacitor	Soft	Up	No	Uni-directional	5MW	- Very high gains achievable without use of transformer - Soft switching for all switches and diodes (eliminating switch turn off and diodes reverse recovery losses) - High efficiency - Not vulnerable to commutation failure	- Output voltage regulated by changing switching frequency (variable frequency control) - High switch stresses since voltage across them equal to output voltage - if IGBTs used (instead of thyristors), a series diode with same voltage rating has to be added which significantly increases conduction loss
[2.71]			Three-phase Thyristor-based resonant bridge & diode rectifier						Similar to single-phase version in [2.70] but: - Reduces peak input current, hence reducing losses and harmonics on the dc bus - During discontinuous mode, higher frequency operation possible. Hence, lower component sizing while still minimizing losses	- High number of resonant inductors and capacitors needed - Output filter inductor needed - At high input currents, slower switches must be used requiring large components - Efficiency reduced at high input currents
[2.76]			Dual thyristor resonant bridges sharing common ac capacitor		Up/Down		Bi-directional		- Two converter topologies: voltage polarity reversal suitable for interfacing current source converters; and current direction reversal suitable for connecting voltage-source converters. - Rapid response to power direction change - Good robustness to terminal voltage variations and faults	- Variable frequency control necessary. - Resonant capacitor will have 20-30% higher voltage than the high-voltage terminal. - Frequency of operation limited due to use of thyristors. Passive components large in size.

Ref.	*Authors*	*Publication year*	*Dc/dc converter topology*	*Hard/Soft switched*	*Step up/down*	*Transformer isolated*	*Power flow direction*	*Power level*	*Advantages*	*Disadvantages*
[2.59]	G.Ortiz *et al.*	2010	Dual active bridge with triangular modulation	Soft	Up/Down	Yes	Bi-directional	1MW	- ZCS on the high voltage side, hence reduced switching losses - High efficiency - Transformer leakage used for resonance	- Moderate IGBT stresses - Soft switching may be lost at light load - Large output capacitor needed (high ripple current)
			Constant frequency dual active bridge series resonant converter						- ZCS on the high voltage side, hence reduced switching losses - Transformer leakage part of resonant inductor - Relatively higher overall efficiency	- Resonant inductor and capacitor needed so larger converter - Poor no-load voltage regulation - Large output capacitor needed (high ripple current)
[2.75]	N.N.Lopatkin *et al.*	2010	Six-stage switched capacitor	Hard	Down	No	Bi-directional	3MW	- No magnetic devices; hence, overall size reduced. - High efficiency - Suitable for railway locomotive application	- Relatively high current switch spikes - Poor voltage regulation
[2.72]	M.Cacciato *et al.*	2010	Dual active bridge	Soft	Up/Down	Yes	Bi-directional	3kW	Same as [2.61] (Dual active bridge)	
[2.73]	H.Akagi *et al.*	2011	Modular system using dual active bridge modules	Soft	Up/Down	Yes	Bi-directional	0.5-1MW	Same as [2.61] (Dual active bridge)	
[2.74]	J.Shi *et al.*		Output paralleled dual active bridge in solid-state transfomer					20kW	- Possibility of power level expansion through parallel operation of bridges - Good fault tolerance due to modularity	Same as [2.61] (Dual active bridge)
[2.2]	N.Denniston *et al.*	2011	Multi-module cascade & series connections of boost, buck-boost & hybrid converters	Hard	Up	No	Uni-directional	1MW	- Simple module structure (single switch, single inductor, & transformerless) - High voltage gain through cascade or series connection - High efficiency - Compared to conventional HVDC, it has low device count, device rating & reliability	- Duty cycle is set to more than 0.9 to achieve high voltage gain. The switching frequency (1kHz) is relatively low to get enough turn-off time, resulting in large size of inductors and filter capacitors

Ref.	*Authors*	*Publication year*	*Dc/dc converter topology*	*Hard/Soft switched*	*Step up/down*	*Transformer isolated*	*Power flow direction*	*Power level*	*Advantages*	*Disadvantages*
[2.48]	H.Fan *et al.*	2011	ISOP connected phase-shift dual-half-bridge (DHB) in a solid-state transfomer	Soft	Up/down	Yes	Bi-directional	20 kW	- ZVS of all switching devices - High frequency switching also possible; hence high-power density modules - ISOP connection enhances system modularity and fault tolerance - Solves the problem of conventional dual active bridges losing soft switching at light loads. This is done using an adaptive inductor. - Adaptive inductor minimizes conduction losses at heavy load as well. - High efficiency over wide load range	Same as [2.61] (Dual active bridge)
[2.52]	Q.Lu *et al.*	2011	ISOS Phase-shifted full-bridge converters	Soft	Up	Yes	Uni-directional	9 kW	Same as [2.61] (Phase-shifted full-bridge) and: - Zero voltage, zero current switching of all switching devices - Uses low voltage rating switches for high-input high-output voltage applications	Same as [2.61] (Phase-shifted full-bridge)
[2.53]	D.Sha *et al.*	2012	ISOS Phase-shifted full-bridge converters					1.6 kW		

Table 2.3: Summary of high-power dc/dc converters in literature

Table 2.3 summarizes the features of several high-power dc/dc converters deployed commercially and in the literature. It can be concluded that key features for high-power requirements are transformer isolation, soft switching, and control simplicity. Accordingly, the suitability of the surveyed converters to specific applications can be determined. For instance, offshore wind farms require uni-directional power flow from the wind turbine to the load or grid. From table 2.3, a dc/dc converter that satisfies the aforementioned features and the uni-directional power flow requirement, is the phase-controlled series-parallel resonant converter. For applications requiring bi-directional power flow (such as solid-state transformers or reversible drives), the phase-controlled dual active half or full-bridge converters would serve best.

2.4 DC/DC converter topology selection for the All-Electric subsea project

The outline and specifications for the *All-Electric* subsea power distribution project were discussed in section 1.4.1. Since power flow is uni-directional from the onshore substation to subsea manifolds, from the discussion in the previous section, a suitable candidate dc/dc converter satisfying the design features is the phase-controlled series-parallel resonant converter. The converter implements soft switching, transformer-based galvanic isolation, offers high efficiency for a wide load range, and its control is not complex.

Considering the family of resonant soft switched converter possibilities, load resonant converters are more suitable than resonant-switch since the latter are generally single-switch converters and therefore not suitable for high-power operation. Also, transformer-based isolation is more applicable with load resonant converter types due to the existence of the intermediate ac conversion stage. The three main load resonant converters are the series resonant converter (SRC) [2.77-83], the parallel resonant converter (PRC) [2.84-86], and the series-parallel resonant converter (SPRC) [2.87-90]. The latter is selected since it combines the merits of SRC and PRC; eliminating their drawbacks. It can operate over both a large input voltage range and a large load range (no-load to full-load) while maintaining good efficiency. Table 2.4 gives a brief comparison of the main features of each resonant converter type to justify the selection of the SPRC.

Various techniques have been used to control the SPRC. These can be broadly classified into variable frequency [2.91-95] and fixed frequency approaches [2.96-98]. However,

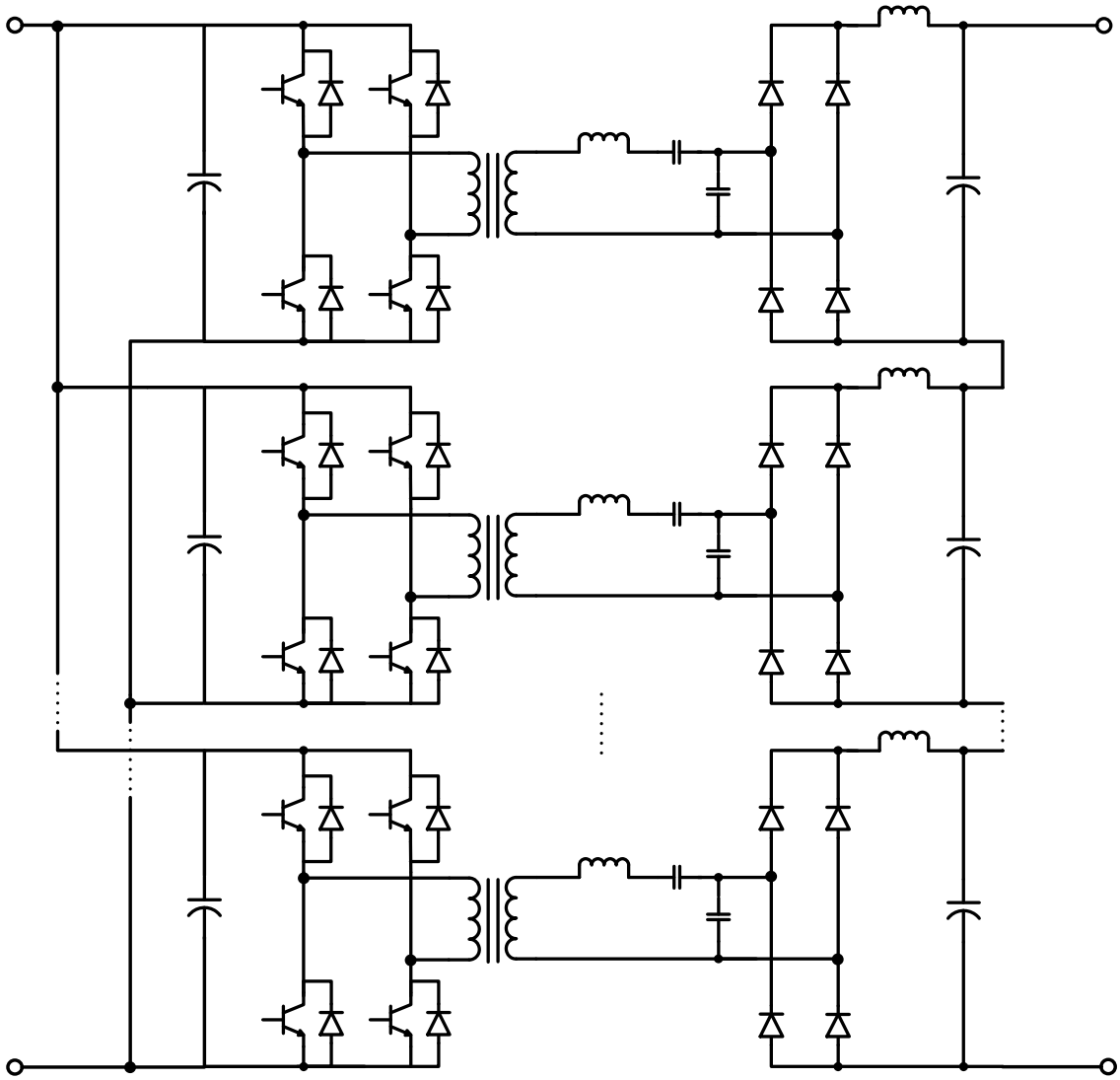
variable frequency techniques present practical problems, like a wide noise spectrum which makes it difficult to control EMI, more complex filtering and poor utilization of magnetic components. Also, the frequency control range is limited if zero voltage switching (ZVS) of the converter is to be achieved. Operation below resonance means ZVS is lost and the inverter switches operate with turn on losses. This necessitates the use of fast recovery anti-parallel diodes to avoid diode recovery shoot-through within the same inverter leg. Operation above resonance is preferred where the SPRC operates with a lagging power factor, hence ZVS. However, an increase in switching frequency above resonance results in a large non-linear reduction in converter voltage gain. Therefore, if frequency control is to be implemented, a narrow control frequency range above resonance is necessary to achieve both ZVS and an acceptable voltage gain. Fixed frequency control above resonance such as phase-shift control [2.96-100] overcomes problems of variable frequency control and offers good control on the output voltage via controlling the phase shift angle between the inverter legs; hence the effective inverter output voltage.

Characteristic	***Series (SRC)***	***Parallel (PRC)***	***Series-parallel (SPRC)***
Resonant frequency	constant	load-dependent	load-dependent
Open circuit output	no large currents	large current near resonance	large current near parallel branch resonance
Short circuit output	high current near resonance	protected by resonant inductor at all frequencies	high current near series branch resonance
Output voltage regulation	poor at no load and light loads	good light load regulation	good light load regulation
Zero voltage switching	yes, above resonance	yes, above resonance	yes, above resonance
Number of resonant tank elements	two	two	three
Light-load efficiency	good	poor	fair
Rectifier current/voltage driven	current	voltage	voltage
Output filter capacitor size	large	fair	fair

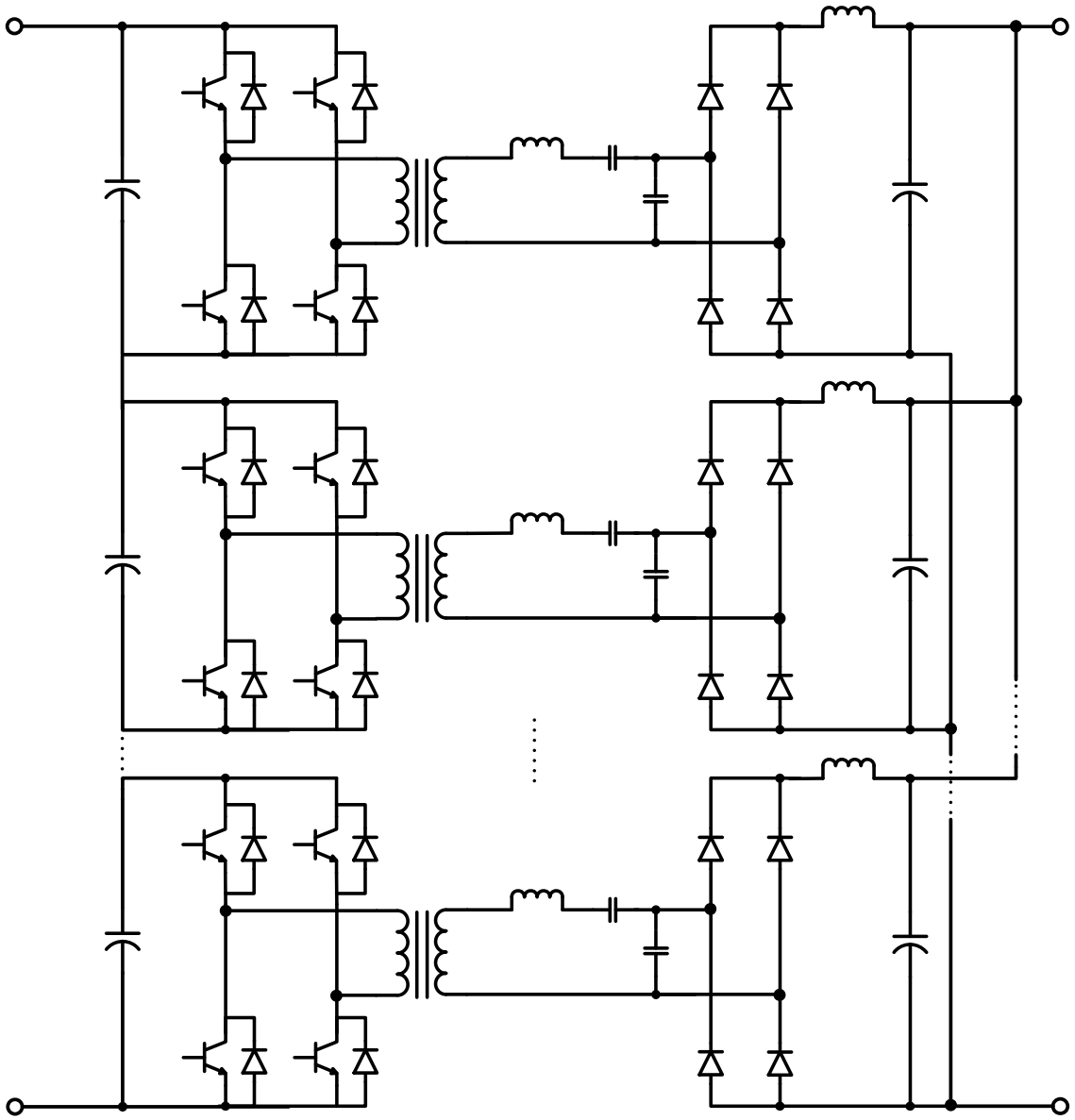
Table 2.4: Comparison of basic load resonant dc/dc converters

Phase control will, therefore, be implemented in this thesis as the main control technique for the series-parallel resonant converter. The main dc/dc SPRC converter building block, with series-parallel connections will enable handling of the high-power and

medium voltage requirements of the subsea project. Multi-module operation also provides features such as modularity, fault tolerance, and high-power density. IPOS and ISOP connections of SPRCs are suitable for the step up and down voltage requirements of the project. Fig. 2.7 shows the circuit diagrams for the IPOS and ISOP connected phase-controlled SPRC, being the selected converter topology for the project onshore step up and offshore step down substations, respectively.



(a)



(b)

Fig. 2.7: Phase-controlled SPRC selected for the *All-Electric* subsea project (a) IPOS connection for voltage step up substation, and (b) ISOP connection for voltage step down substation.

2.5 Summary

This chapter reviewed the basic requirements for industrial dc/dc converters; the most important being galvanic isolation between the source and load, high-power density, and high conversion efficiency. Multi-module series and parallel connections of dc/dc converters were reviewed with the main characteristics and applications of each presented. After surveying several high-power dc/dc converters deployed commercially and in the literature, ISOP/IPOS connection of phase-controlled SPRCs is selected as

the candidate dc/dc converter topology for the *All Electric* subsea project since it complies with the project requirements; especially high-power density, uni-directional power flow, transformer isolation, and high conversion efficiency due to its soft switching characteristics. Multi-module series-parallel SPRC connection enhances system modularity, fault tolerance, reduces manufacturing time and cost, and reduces component thermal and electrical stresses.

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Chapter 3

Steady-State Analysis and Design of the Phase-Controlled Series-Parallel Resonant Converter

In chapter two, the phase-controlled series-parallel resonant converter (SPRC) was selected as the candidate dc/dc converter building block for the *All-Electric* subsea project. This chapter focuses on the steady-state analysis and design of the converter giving further insight as well as new steady-state analysis and design methods, differing from the well-established material in the literature.

3.1 Background

The steady-state characteristics of the SPRC have been analysed extensively in the literature. Bhat [3.1] used a state space approach to find the steady-state solution numerically or in closed form. Verghese *et al.* [3.2] used sampled-data methods to obtain the transient and dynamic responses. Steigerwald [3.3] proposed complex analysis to enable comparison of resonant topologies. Kazimiercuk *et al.* [3.4] used Fourier series to analyse the resonant converter in the frequency domain. Batarseh *et al.* [3.5] used state-plane diagrams to obtain the steady-state and small-signal behaviour of resonant type converters. Witulski *et al.* [3.6] used lumped parameter equivalent circuits to obtain small-signal equivalent circuits.

Both variable and fixed frequency control of the SPRC have been studied thoroughly at steady-state. Variable frequency operated SPRCs includes topologies with half-bridge inverters [3.1, 7-9] and class D resonant inverters [3.4]. However, variable frequency operation presents practical problems, such as a wide noise spectrum which makes it difficult to control EMI, more complex filtering, and poor utilization of magnetic components. For this reason, fixed frequency operation such as phase-shift control of the SPRC overcomes problems of variable frequency control and offers good control of the output voltage.

Steady-state analysis and design of a fixed frequency PWM SPRC was studied by Bhat [3.10] based on complex ac circuit theory [3.3]. The converter voltage transfer function is presented analytically without further steady-state characteristics. Kazimierczuk *et al.*

[3.11, 12] introduced fixed frequency phase-controlled SPRCs using two paralleled class D or class E resonant inverters, with a common output rectifier. Detailed steady-state analytical and graphical studies of the proposed converters are carried out. However, a high number of resonant tank components are used compared to the basic SPRC. Jain [3.13-15] presents a phase-shift modulated double tuned SPRC to reduce the conduction and switching losses of the conventional SPRC and hence obtains better efficiency for wide input voltage and output load variations. However, more resonant components are used.

This chapter extends the work in [3.10] and presents new analysis and further insight into the basic phase-controlled SPRC. The analysis considers the effects of varying the phase angle, the output load and the switching frequency above resonance on converter operation. The following steady-state analysis is performed:

- Converter voltage transfer function;
- Detailed converter operation modes with mode boundaries graphically represented;
- Maximum power transfer to load;
- Converter voltage gain sensitivity to variations in operating frequency and load; and
- Converter efficiency including inverter, rectifier and passive element losses.

The remaining part of this chapter outlines the design criteria on which the circuit elements are selected to fulfil the requirements of the converter application in the proposed subsea project. The design process relies primarily on steady-state performance measures to ensure the best converter operating conditions. The design procedure starts with selection of the optimum resonant tank frequency and full-load Q factor which meet maximum converter efficiency. Detailed design and selection criteria of the resonant tank element values, the high-frequency nano-crystalline cored transformer, and the output filter are studied. A new analytical approach for the output filter design, with multi-module interleaved operation, is presented.

3.2 Steady-state analysis

Fig. 3.1(a) shows the circuit diagram for the phase-controlled SPRC, with the gating pattern for phase-shift control illustrated in Fig. 3.1(b). For analysis simplicity, the following assumptions are made:

- The resonant inductor current is sinusoidal due to the low-pass filter effect of the resonant tank when operating above resonance. This means that power from the inverter is transferred to the load solely at the fundamental frequency, hence representing v_{AB} with its fundamental component v_{AB1}.
- Output filter inductor L_o is large enough to minimize inductor current ripple.
- The effects of parasitic resistances, transformer magnetizing inductance, and inverter snubbers are neglected.
- Parallel resonant capacitance is equal to the series resonant capacitance (C_p=C_s). If C_p<C_s, the SPRC behaves more like an SRC with its poor light load output voltage regulation. If C_p>C_s, the SPRC behaves more like a PRC with its poor light load efficiency due to constant resonant tank current. The SPRC combines the merits of both the SRC and the PRC and eliminates their drawbacks. Therefore the analysis is carried out for C_p=C_s as an agreed compromise [3.3].

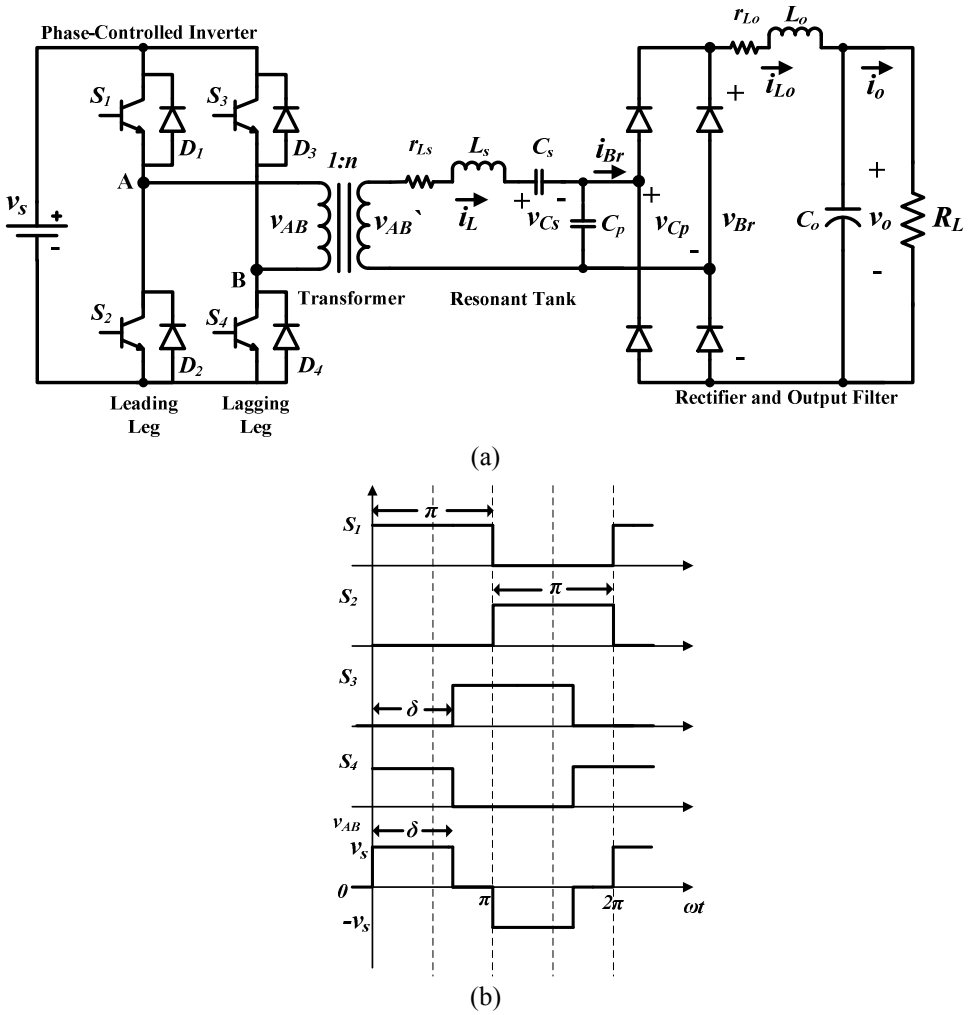


Fig. 3.1: Series-parallel resonant converter
(a) circuit diagram and (b) inverter gating pattern for phase-shift control

3.2.1 Voltage gain transfer function

Fig. 3.2 shows the ac equivalent circuit for the series-parallel resonant converter obtained from Fig. 3.1(a). The effect of the transformer magnetizing inductance is neglected and R_{ac} represents the ac equivalent resistance of the load and output rectifier as defined in [3.3].

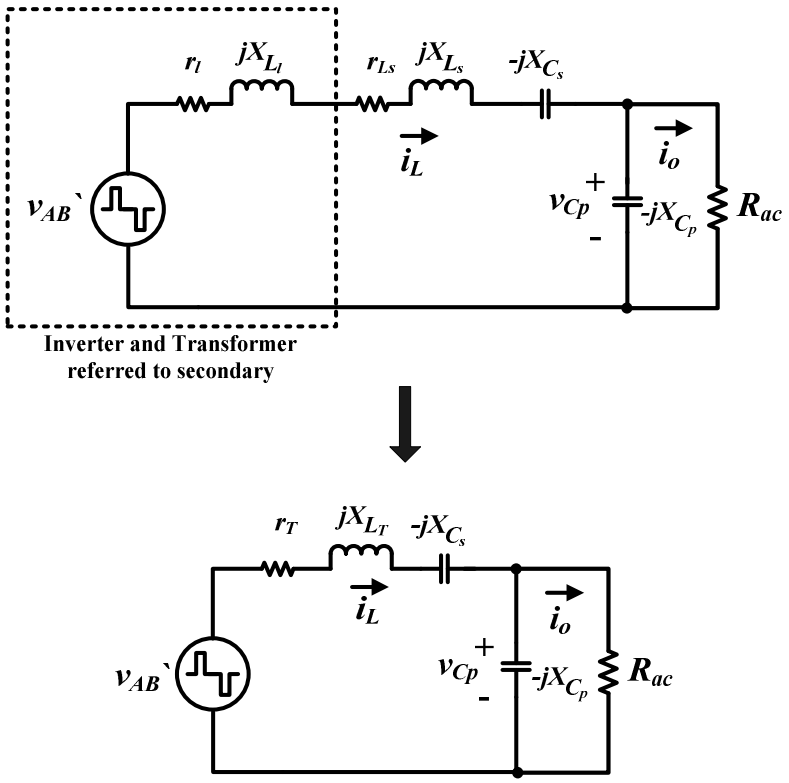


Fig. 3.2: AC equivalent circuit of the series-parallel resonant converter ($r_T=r_l+r_{Ls}$ and $X_{LT}=X_{Ll}+X_{Ls}$)

Neglecting parasitic resistances, an expression for voltage gain can be derived

$$\frac{|v_{C_{p1}}|}{|v_{AB_1}`|} = \frac{1}{\left|\left(1+\frac{X_{Cs}}{X_{Cp}}-\frac{X_{LT}}{X_{Cp}}\right)+j\left(\frac{X_{LT}}{R_{ac}}-\frac{X_{Cs}}{R_{ac}}\right)\right|} \tag{3.1}$$

where $v_{AB1}`$ and v_{Cp1} are the fundamental inverter output voltage referred to the transformer secondary and parallel capacitor voltage respectively. Using the Fourier transform, (3.1) can be represented as

$$\frac{\left(\frac{\pi}{2}V_o\right)}{\left(\frac{4nV_s}{\pi}\sin\frac{\delta}{2}\right)} = \frac{1}{\left|\left(1+\frac{X_{Cs}}{X_{Cp}}-\frac{X_{LT}}{X_{Cp}}\right)+j\left(\frac{X_{LT}}{R_{ac}}-\frac{X_{Cs}}{R_{ac}}\right)\right|} \tag{3.2}$$

Applying the definitions of R_{ac} ($(\pi^2/8)R_L$), Q ($Z_c/R_L=\sqrt{L_T/C_s}/R_L$) and ω_0 ($1/\sqrt{L_TC_s}$) from the List of Symbols, (3.2) can be expressed as

$$\frac{V_o}{V_s}=\frac{n\sin\frac{\delta}{2}}{\left|\frac{\pi^2}{8}\left(1+\frac{C_p}{C_s}-\omega^2L_TC_p\right)+jQ\left(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\right)\right|} \tag{3.3}$$

For C_p=C_s, the converter voltage gain transfer function M can be expressed as

$$M=\frac{V_o}{V_s}=\frac{n\sin\frac{\delta}{2}}{\left|\frac{\pi^2}{8}\left(2-\omega_{pu}{}^2\right)+jQ\left(\omega_{pu}-\frac{1}{\omega_{pu}}\right)\right|} \tag{3.4}$$

where ω_{pu}=ω/ω_0. Fig. 3.3 shows the converter voltage gain M plotted for ω_{pu}>1 (above resonance operation) and n=1 (transformer unity turns ratio). The converter can operate in step up and step down modes depending on the quality factor Q and the inverter switching frequency.

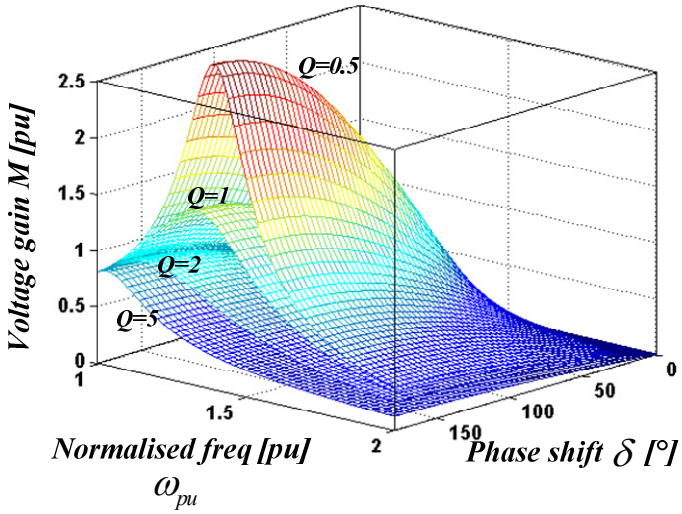


Fig. 3.3: Converter voltage gain M

Generally higher gains are obtained with light loads (low Q) with the resonant frequency boundary between an inductive and a capacitive resonant circuit shifting from ω_0 to $\omega_{02}=1/\sqrt{\frac{L_TC_pC_s}{C_p+C_s}}$ at no load; where ω_{02} is the resonance frequency at no load. This reduces to $\omega_{02}=\sqrt{2}\omega_0$ for C_p=C_s which is shown in Fig. 3.3 by the peak gain at Q=0.5 and ω_{pu} =1.414. The gain is reduced significantly for increased frequencies, reduced phase-shift, and for heavy loads with high Q factors.

3.2.2 Modes of operation and mode boundaries

Four modes of converter operation exist for the phase-controlled SPRC operating above resonance. These modes are summarised in Table 3.1 and depend on whether the resonant circuit is inductive or capacitive (according to loading factor Q and inverter frequency ω_{pu} above resonance) as well as the phase-shift angle δ. Some important parameters to define are:

- Input impedance of the resonant circuit (as shown in Fig. 3.4, neglecting r_T)

$$Z = \frac{R_{ac}{X_{C_p}}^2 + j\left[{R_{ac}}^2(X_{L_T} - X_{C_s} - X_{C_p}) + {X_{C_p}}^2(X_{L_T} - X_{C_s})\right]}{{R_{ac}}^2 + {X_{C_p}}^2} \tag{3.5}$$

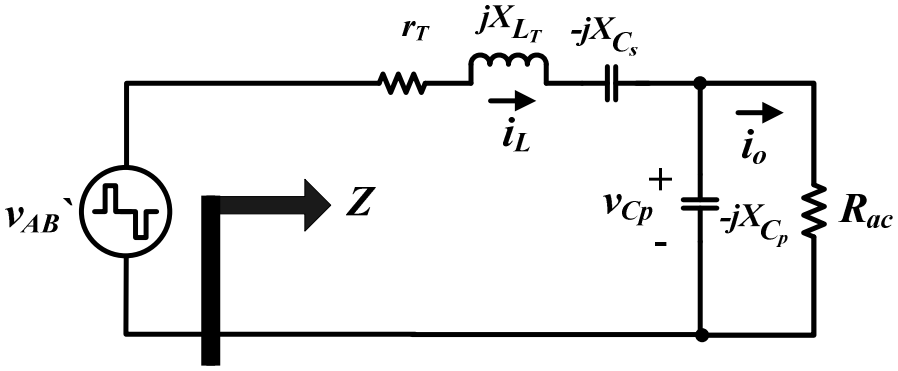


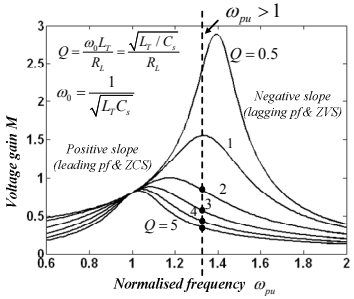
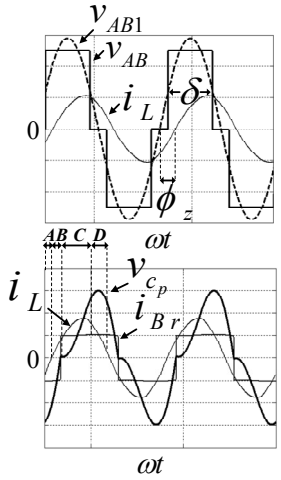
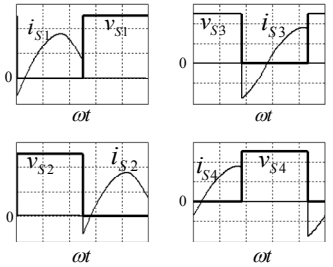
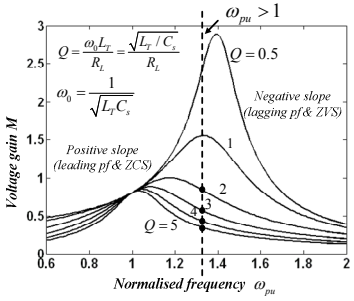
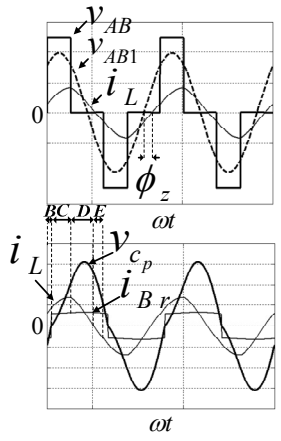
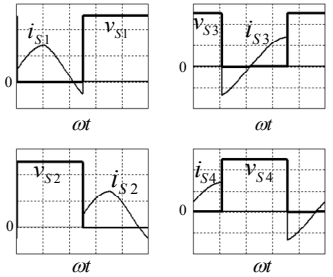
Fig. 3.4: Input impedance Z of resonant circuit

- Input impedance angle for C_p=C_s

$$\phi_z = \tan^{-1}\left[\frac{{\omega_{pu}}^4 + \left(\frac{64Q^2}{\pi^4} - 2\right){\omega_{pu}}^2 - \frac{64Q^2}{\pi^4}}{\frac{8Q}{\pi^2}\omega_{pu}}\right] \tag{3.6}$$

- Resonant circuit frequency for C_p=C_s (obtained from *Imag(Z)=0*)

$$\omega_{res(pu)} = \frac{\omega_{res}}{\omega_0} = \sqrt{\left(1 - \frac{32Q^2}{\pi^4}\right) + \sqrt{\left(1 - \frac{32Q^2}{\pi^4}\right)^2 + \frac{64Q^2}{\pi^4}}} \tag{3.7}$$

	Mode	Leading leg (S_1S_2)	Lagging leg (S_3S_4)	Location on frequency response plot	Voltage/Current waveforms		Energy recovery to supply	Conditions for mode operation
					Resonant tank	Converter switches		
Lagging inductor current	1	ZVS	ZVS				Yes	$\omega_{pu} > \omega_{res(pu)}$ and $\phi_z > \frac{\pi-\delta}{2}$
	2	ZCS	ZVS				No	$\omega_{pu} > \omega_{res(pu)}$ and $\phi_z < \frac{\pi-\delta}{2}$

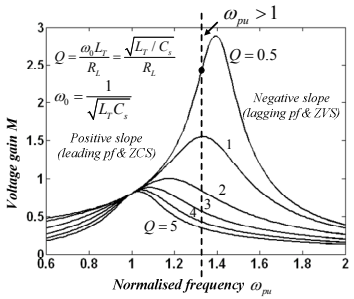
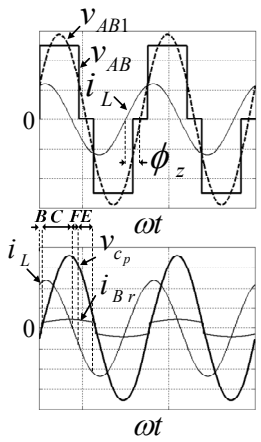
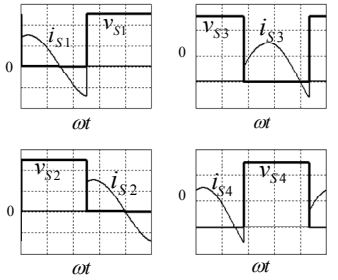
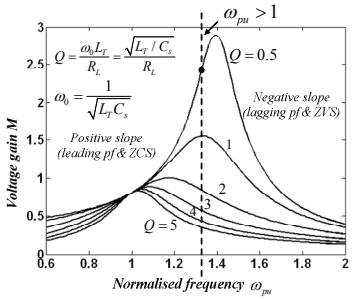
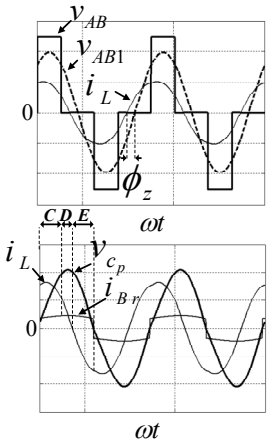
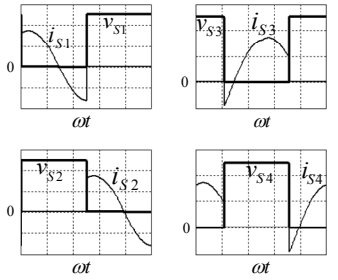
	Mode	Leading leg (S_1S_2)	Lagging leg (S_3S_4)	Location on frequency response plot	Voltage/Current waveforms: Resonant tank	Voltage/Current waveforms: Converter switches	Energy recovery to supply	Conditions for mode operation
Leading inductor current	3	ZCS	ZCS				Yes	$\omega_{pu} < \omega_{res(pu)}$ and $-\phi_z > \frac{\pi - \delta}{2}$
	4	ZCS	ZVS				No	$\omega_{pu} < \omega_{res(pu)}$ and $-\phi_z < \frac{\pi - \delta}{2}$

Table 3.1: Modes of operation of the phase-controlled SPRC operating above resonance

For mode comparisons, Fig. 3.5 shows the equivalent steady-state ac circuits for a positive half-cycle of the inverter output voltage v_{AB}. Negative half-cycle equivalent circuits are identical but with $-v_s$ and the complementary inverter switches conducting.

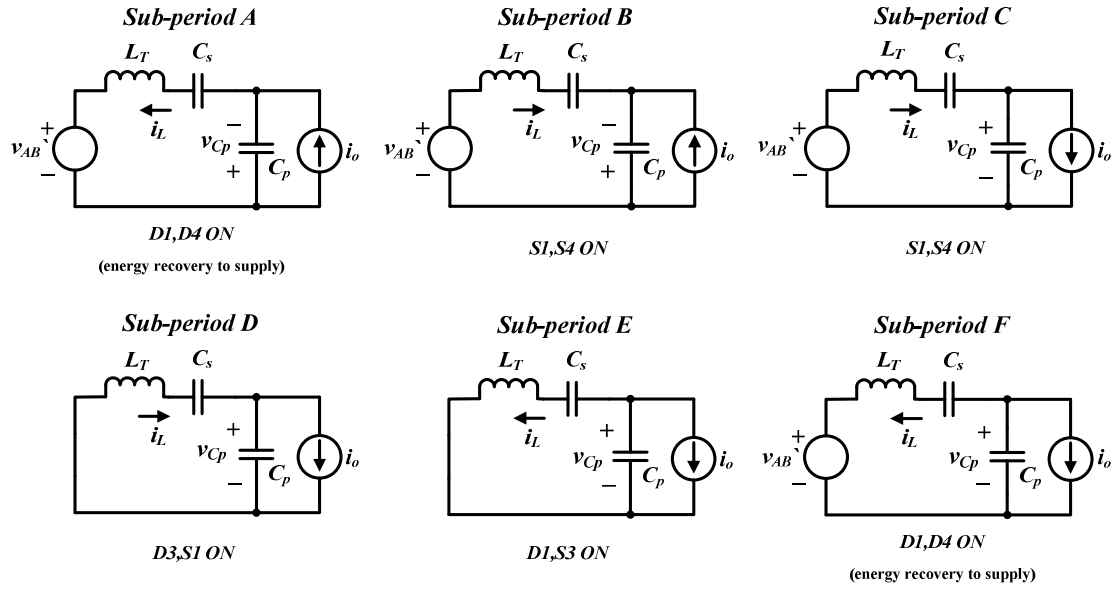


Fig. 3.5: Equivalent ac circuits for the positive half-cycle sub-periods

Mode operations are explained as follows:

- ***Mode 1:*** During sub-period *A*, resonant inductor current is negative; hence, resonant tank energy is fed back to the dc supply through diodes D_1, D_4. At the end of sub-period *A*, the resonant inductor current falls to zero and the powering stage starts with sub-periods *B* and *C* where energy is transferred from the source to the tank through switches S_1, S_4. During sub-period *B*, parallel capacitor C_p discharges until v_{Cp}=0. In sub-period *C*, $i_L > i_o$ and C_p charges up; hence the rapid rise in v_{Cp}. Correspondingly the inductor voltage decreases, allowing the inductor current to start decay. During sub-period *D*, the inverter upper half conducts (D_3 ,S_1). Energy in the resonant tank is dissipated in the zero voltage loop and no energy is returned to the dc supply.

  Converter switch voltage/current waveforms, verify zero-voltage turn on for all four switches in this mode of operation. The load current is carried by the switch antiparallel diode prior to switch operation hence the voltage across it is zero before conduction of the forward current. All four switches turn off whilst conducting current, but with inverter lagging leg switches turning off higher current. Switching stresses are therefore higher on the lagging leg compared to the leading leg.

This mode is characterised by the resonant inductor current i_L lagging the fundamental inverter output voltage v_{AB1} since $\omega_{pu} > \omega_{res(pu)}$ which means that the resonant tank is inductive and operation is on the negative slope of the frequency response plot. However, this mode is differentiated from mode 2 by the fact that i_L is also lagging the postive-going edge of the inverter output voltage waveform (v_{AB}), that is, $\phi_z < \frac{\pi - \delta}{2}$.

- ***Mode 2:*** As explained in mode 1 operation, mode 2 is characterised by a leading i_L waveform relative to the positive-going edge of v_{AB} while still lagging the fundamental v_{AB1} waveform. Operation is on the negative frequency response slope but zero voltage turn on is lost for the inverter leading leg switches only. Leading leg switches such as S_1 turn on with positive current and ZVS is lost. The negative turn off current in S_1 (through D_1, S_3, sub-period *E*) flows through S_2, S_3 at the start of the negative half-cycle powering stage. The reverse recovery time of D_1 must, therefore, be short to prevent overlapping conduction with S_2 in the same leg. This necessitates the use of fast recovery freewheel diodes for the leading leg switches in mode 2. No energy is recovered to the supply during this mode. Inverter lagging leg switches operate in a similar manner to mode 1 with zero voltage turn on.
- ***Mode 3:*** When operation is below resonance ($\omega_{pu} < \omega_{res(pu)}$), the resonant circuit becomes capacitive and i_L leads the fundamental inverter output voltage v_{AB1}. Similar to mode 1, energy is recovered to the supply through diodes D_1, D_4 (sub-period *F*) due to i_L leading the negative-going edge of inverter output voltage waveform v_{AB}. Operation is on the positive slope of the frequency response plot and all the inverter switches turn on positive current while turn off occurs at zero voltage. This necessitates the use of fast recovery diodes for all inverter switches (not only leading leg switches like in mode 2).
- ***Mode 4:*** Operation is below resonance ($\omega_{pu} < \omega_{res(pu)}$) but with i_L lagging the negative-going edge of v_{AB}. This means that no energy is recovered to the supply in this mode. Instead energy is dissipated in the zero-voltage loops of sub-periods *D* and *E*. Operation is on the positive slope of the frequency response plot but now with the inverter lagging leg switches switching on at zero-voltage. Only the leading leg switches turn on positive current, meaning that, similar to mode 2, fast recovery diodes are mandatory only for the leading leg switches.

Typically mode 1 is preferable due to the ZVS of both inverter legs. Switch turn on losses are eliminated and turn off losses can be mitigated by the use of lossless capacitive snubbers. Contrarily, operating below resonance (as in mode 3) results in transistor turn on switching losses and diode switching losses (fast recovery diodes are needed). Transistor turn off does occur in a lossless manner when operating below resonance. However, because turn off losses can be reduced using lossless snubbers when operating above resonance, this is not a major argument for operating below resonance.

Fig. 3.6 illustrates the mode boundary conditions defined by the last column of Table 3.1. Mode 1 operation is guaranteed for a wide load range for $\omega_{pu} > \sqrt{2}$ provided δ is not too low; otherwise mode 2 occurs. However, for $1 < \omega_{pu} < \sqrt{2}$ mode 1 occurs only for heavier loads. At lighter loads, mode 4 is preferred to mode 3 due to the lagging leg operating with ZVS. Therefore it can be concluded that operating at $\omega_{pu} > \sqrt{2}$ guarantees the preferred operation region (mode 1 for a wide load range or mode 2 in the worst case at excessively low δ). On the other hand, excessive increase in switching frequency leads to reduced converter voltage gain as illustrated in Fig. 3.3. The optimum choice of converter switching frequency is discussed in detail in section 3.3.1.

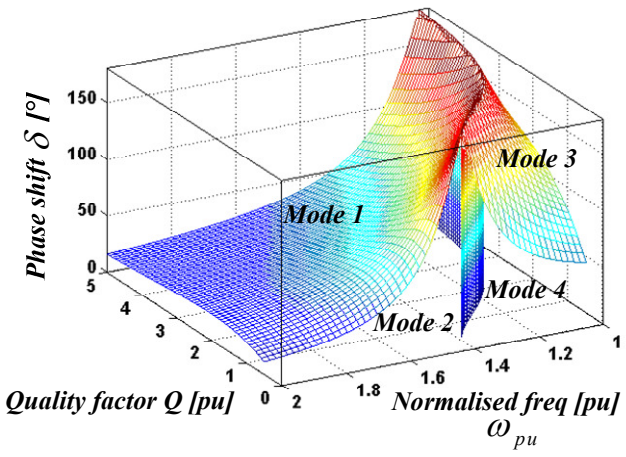


Fig. 3.6: Mode boundaries

3.2.3 Maximum power transfer

Maximum power transfer occurs when the load resistance matches the Thevenin equivalent impedance of the resonant tank. Hence, considering Fig. 3.2 and neglecting parasitic resistances, maximum power transfer can be obtained by

$$R_{ac} = \left| \frac{-jX_{C_p} \times j(X_{L_T} - X_{C_s})}{j(X_{L_T} - X_{C_s} - X_{C_p})} \right| \tag{3.8}$$

Equation (3.8) can be re-formulated using the definitions of R_{ac} $\left((\pi^2/8)R_L\right)$, $Q\left(\omega_0 L_T / R_L = Z_c / R_L\right)$ and ω_{pu} $\left(\omega/\omega_0\right)$.

$$Q = \frac{{\omega_{pu}}^2 - 2}{\frac{8}{\pi^2}\left(\omega_{pu} - \frac{1}{\omega_{pu}}\right)} \tag{3.9}$$

Per unit converter output power is plotted in Fig. 3.7. From (3.9), for every switching frequency there exists a value of Q where maximum power transfer occurs. At heavy loads (high Q), maximum power transfer occurs near ω_{pu}=1 where the circuit is purely resistive since the load effectively short circuits the parallel capacitor C_p, hence the circuit acts as a series resonant converter (SRC). As load gets lighter, resonance is asymptotic to ω_{pu}=1.414 where maximum power transfer occurs. For ω_{pu}>1.414, low Q is preferred for maximum power transfer since the circuit is analogous to a PRC. Maximum power transfer in (3.9) is seen to be independent of the phase angle δ. The higher the phase angle the higher is the converter output power.

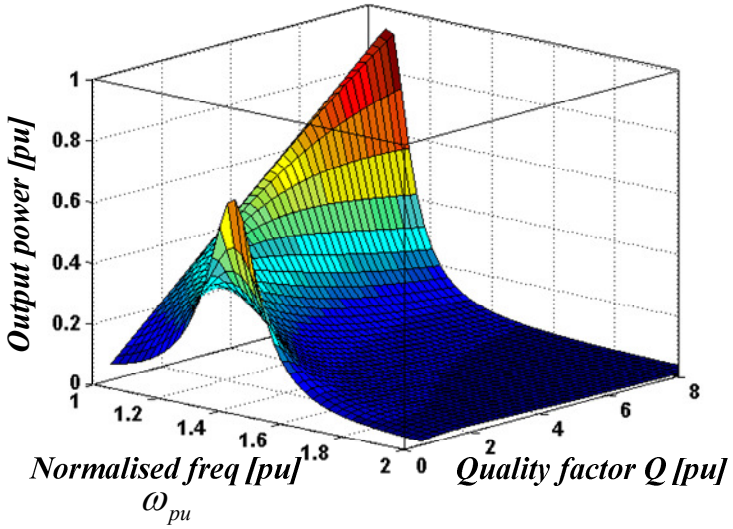


Fig. 3.7: Maximum power transfer

3.2.4 Voltage gain sensitivity

The sensitivity of the converter voltage gain to the change in operating frequency and load are both investigated in this section. Phase control of the SPRC is a fixed frequen-

cy control method. However, practical controller implementation results in an unavoidable small variation in switching frequency. The effects of this phenomenon in addition to effects of load variation on converter voltage gain will both be studied.

The Bode sensitivity of $Y(x_1,x_2,.....,x_n)$ with respect to x_1 is defined as (3.10) for small changes in x_1

$$S_{x_1}^{Y}=\frac{\partial Y/Y}{\partial x_1/x_1}=\frac{x_1}{Y}\frac{\partial Y}{\partial x_1} \tag{3.10}$$

In terms of magnitude, the converter voltage gain M in (3.4) can be re-written as

$$M=\frac{n\sin\frac{\delta}{2}}{\sqrt{\left(\frac{\pi^2}{8}\right)^2\left(2-\omega_{pu}{}^2\right)^2+Q^2\left(\omega_{pu}-\frac{1}{\omega_{pu}}\right)^2}} \tag{3.11}$$

The sensitivity of M to small changes in operating frequency ω_{pu} and load (represented by the quality factor Q) are defined in (3.12) and (3.13) respectively.

$$S_{\omega pu}^{M}=\frac{\omega_{pu}}{M}\frac{\partial M}{\partial \omega_{pu}}=\frac{-\frac{1}{2}\omega_{pu}\left(-\frac{\pi^4}{16}\omega_{pu}\left(2-\omega_{pu}{}^2\right)+2Q^2\left(\omega_{pu}-\frac{1}{\omega_{pu}}\right)\left(1+\frac{1}{\omega_{pu}{}^2}\right)\right)}{\left(\frac{\pi^2}{8}\right)^2\left(2-\omega_{pu}{}^2\right)^2+Q^2\left(\omega_{pu}-\frac{1}{\omega_{pu}}\right)^2} \tag{3.12}$$

$$S_{Q}^{M}=\frac{Q}{M}\frac{\partial M}{\partial Q}=\frac{-Q^2\left(\omega_{pu}-\frac{1}{\omega_{pu}}\right)^2}{\left(\frac{\pi^2}{8}\right)^2\left(2-\omega_{pu}{}^2\right)^2+Q^2\left(\omega_{pu}-\frac{1}{\omega_{pu}}\right)^2} \tag{3.13}$$

Since the feasible frequency control range for operation above resonance is $1<\omega_{pu}<\sqrt{2}$ (as discussed in section 3.2.2), examining the two extremes of ω_{pu} gives the limits of the sensitivity functions

$$S_{\omega pu}^{M}=\begin{cases}2\%, & \omega_{pu}=1\\ -3\%, & \omega_{pu}=\sqrt{2}\end{cases} \tag{3.14}$$

$$S_Q^M = \begin{cases} 0, & \omega_{pu} = 1 \\ -1\%, & \omega_{pu} = \sqrt{2} \end{cases} \tag{3.15}$$

From (3.14) and (3.15), it can be concluded that the converter voltage gain is less sensitive to operating frequency and load variations when operating at ω_{pu}=1. Converter gain is unaffected by load change when operating at ω_{pu}=1. This can be confirmed from Fig. 3.3 where at ω_{pu}=1, the converter gain is constant at M=0.8 for all Q. The converter becomes more sensitive as the operating frequency increases. The analysis shows that the converter is relatively insensitive to small variations in operating frequency and load.

3.2.5 Efficiency

In this section, the efficiency of the phase-controlled SPRC is studied in detail. The efficiency η is generally defined by (3.16).

$$\eta = \frac{\text{Output Power}}{\text{Input Power}} = \frac{\text{Output Power}}{\text{Output Power + Losses}} \tag{3.16}$$

Various losses exist for an SPRC, which are summarised in Fig. 3.8.

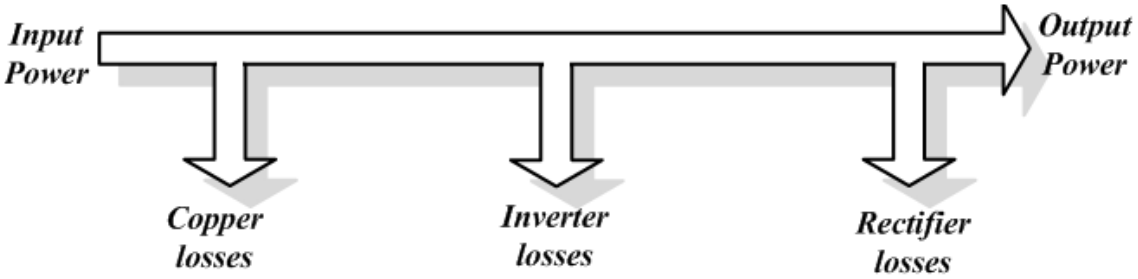


Fig. 3.8: Power flow diagram for a SPRC

In order to calculate the converter efficiency, expressions for output power and losses are derived and detailed in terms of the main parameters δ, Q and ω_{pu}. All power calculations are on a p.u. basis to generalise the derived expressions and avoid using specific circuit parameter values. It is assumed that all currents and voltages in the resonant tank are sinusoidal; hence power calculations are solely performed at fundamental frequency ω. The following base values are used for the p.u. calculations

$$
\begin{aligned}
V_{base} &= V_s \\
Z_{base} &= Z_c = \sqrt{L_T / C_s} \\
I_{base} &= V_{base} / Z_{base} = V_s / Z_c \\
P_{base} &= V_s^{\,2} / Z_c \\
\omega_{base} &= \omega_0
\end{aligned}
\tag{3.17}
$$

(a) Output power

Referring to Fig. 3.2, output power P_o can be calculated using

$$
P_o = \frac{\left|V_{Cprms}\right|^2}{R_{ac}} = \tfrac{1}{2}\frac{\left|V_{Cp\,peak}\right|^2}{R_{ac}} \tag{3.18}
$$

Applying the voltage divider rule as in (3.1) and (3.2), and taking the parasitic resistance r_T into account

$$
\left|V_{Cp\,peak}\right| = \frac{\frac{4nV_s}{\pi}\sin\tfrac{1}{2}\delta}{\left[\left(2-\omega_{pu}^{\,2}\right)+\frac{8r_TQ}{\pi^2Z_c}\right]+j\left[\frac{r_T\omega_{pu}}{Z_c}+\frac{8}{\pi^2}Q\left(\omega_{pu}-\frac{1}{\omega_{pu}}\right)\right]} \tag{3.19}
$$

Therefore, per unit output power can be expressed as

$$
P_o(pu) = \frac{n^2Q\sin^2\tfrac{1}{2}\delta}{\left[\frac{\pi^2}{8}\left(2-\omega_{pu}^{\,2}\right)+r_{T_{pu}}Q\right]^2+\left[\frac{\pi^2}{8}r_{T_{pu}}\omega_{pu}+Q\left(\omega_{pu}-\frac{1}{\omega_{pu}}\right)\right]^2} \tag{3.20}
$$

(b) Copper losses

These are associated with any losses in the copper wires or parasitic resistances of circuit elements. They are mainly divided into two sets for ease of calculation: resonant tank copper losses and output filter copper losses.

(i) Resonant tank copper losses

Resonant tank copper losses are associated with resonant inductor internal resistance and transformer winding resistances. These are combined in the total equivalent resistance $r_T=r_l+r_{Ls}$. Therefore, resonant tank copper losses can be defined as

$$P_{Cu_{tank}} = \left|I_{L_{rms}}\right|^2 r_T = ½\left|I_{L_{peak}}\right|^2 r_T \tag{3.21}$$

Considering Fig. 3.4 and the resonant tank input impedance Z in (3.5), but taking r_T into account

$$\left|I_{L_{peak}}\right| = \frac{\left|V_{AB_{peak}}\right|}{Z} = \frac{4nV_s}{\pi}\sin ½\delta \sqrt{\frac{\frac{\pi^4 Z_c^{\,2}}{64Q^2} + \frac{Z_c^{\,2}}{\omega_{pu}^{\,2}}}{\left[\frac{r_T\pi^2 Z_c}{8Q} + Z_c^{\,2}\left(1-\frac{1}{\omega_{pu}^{\,2}}\right)\right]^2 + \left[\frac{\pi^2 Z_c^{\,2}}{8Q\omega_{pu}}\left(\omega_{pu}^{\,2}-2\right) - \frac{r_T Z_c}{\omega_{pu}}\right]^2}} \tag{3.22}$$

Therefore, the per unit resonant tank copper losses can be expressed as

$$P_{Cu_{tank}}(pu) = \frac{r_{T_{pu}} n^2 \sin^2\frac{\delta}{2}\left(\frac{\pi^2}{8Q^2} + \frac{8}{\pi^2\omega_{pu}^{\,2}}\right)}{\left[\frac{r_{T_{pu}}\pi^2}{8Q} + \left(1-\frac{1}{\omega_{pu}^{\,2}}\right)\right]^2 + \left[\frac{\pi^2}{8Q\omega_{pu}}\left(\omega_{pu}^{\,2}-2\right) - \frac{r_{T_{pu}}}{\omega_{pu}}\right]^2} \tag{3.23}$$

(ii) Output filter copper loss

Output filter copper loss occurs in the output filter inductor internal resistance r_{Lo}. This can be defined as

$$P_{Cu_{filter}} = \left|I_o\right|^2 r_{Lo} \tag{3.24}$$

where

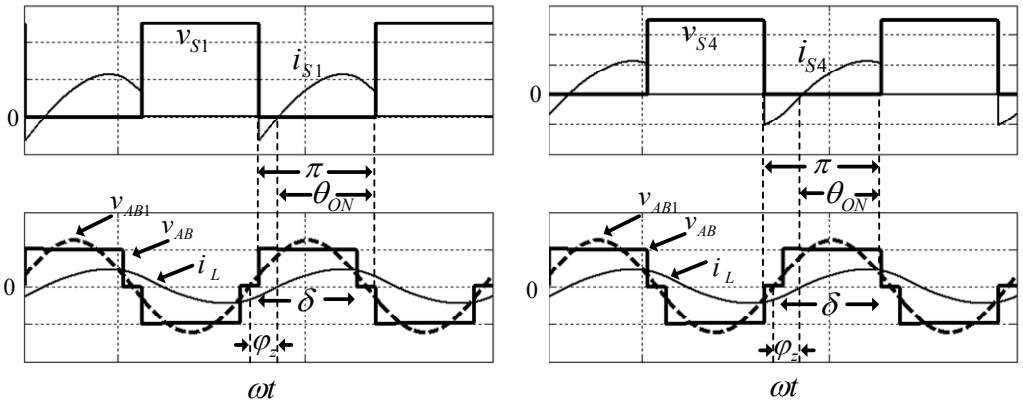
$$I_o = \frac{V_o}{R_L} = \frac{nV_s \sin ½\delta}{\sqrt{\left[\frac{\pi^2 Z_c}{8Q}\left(2-\omega_{pu}^{\,2}\right) + r_T\right]^2 + \left[\frac{\pi^2 r_T \omega_{pu}}{8Q} + Z_c\left(\omega_{pu} - \frac{1}{\omega_{pu}}\right)\right]^2}} \tag{3.25}$$

Therefore the per unit output filter copper loss can be expressed as

$$P_{Cu_{filter}}(pu) = \frac{n^2 r_{Lo_{pu}} \sin^2 ½\delta}{\left[\frac{\pi^2}{8Q}\left(2-\omega_{pu}^{\,2}\right) + r_{T_{pu}}\right]^2 + \left[\frac{\pi^2 r_{T_{pu}}\omega_{pu}}{8Q} + \left(\omega_{pu} - \frac{1}{\omega_{pu}}\right)\right]^2} \tag{3.26}$$

(c) Inverter losses

Inverter losses can be generally expressed as the summation of the conduction and switching losses in the inverter switches. In the case of ZVS and ZCS, turn on and turn off losses are eliminated respectively with the possibility of mitigating the contrary loss by the use of switching aid circuits. For instance, with ZVS, switch turn on losses are zero and turn off losses can be largely mitigated using lossless capacitive snubbers. For this reason, focus in this section is on the inverter conduction losses which comprise a high proportion of the total inverter losses. Fig. 3.9 shows typical switch voltage/current waveforms.



$$\theta_{ON(leading\ leg)} = \frac{3\pi - \delta}{2} - \phi_z \qquad \theta_{ON(lagging\ leg)} = \frac{\pi + \delta}{2} - \phi_z$$

(a) (b)

Fig. 3.9: Inverter switches voltage/current waveforms (a) S_1 (leading leg) and (b) S_4 (lagging leg).

Per switch conduction losses can be defined by

$$P_{cond(Inv)} = \frac{1}{T_s} \int_0^{T_{ON}} V_{ON} i \, dt \tag{3.27}$$

where T_s is the switching period, T_{ON} is the conduction time, and V_{ON} is the switch on-state voltage obtained from the device datasheet. Assuming sinusoidal steady-state resonant tank currents, as in Fig. 3.9, switch conduction losses are

$$P_{cond(Inv)} = \frac{V_{ON}}{2\pi}\int_0^{\theta_{ON}} nI_{L_{peak}} \sin\omega t \; d(\omega t)$$
$$= \frac{nV_{ON}I_{L_{peak}}}{2\pi}(1-\cos\theta_{ON}) \tag{3.28}$$

where θ_{ON} is the switch conduction angle and n is the transformer turns ratio. Therefore for two switches per inverter leg, the total conduction losses for the inverter are

$$P_{cond(Inv)}(pu) = \frac{n\left|V_{ON}\right|_{pu}\left|I_{L_{peak}}\right|_{pu}}{\pi}(2-\cos\theta_{ON(Leading\ leg)}-\cos\theta_{ON(Lagging\ leg)}) \tag{3.29}$$

where θ_{ON} is defined for the leading and lagging legs in Fig. 3.9, $|V_{ON}|_{pu}$ can be obtained by referring V_{ON} to V_{base} defined in (3.17), and similarly referring $\left|I_{L_{peak}}\right|_{pu}$ defined in (3.22) to I_{base}, yields

$$\left|I_{L_{peak}}\right|_{pu} = \frac{4n}{\pi}\sin\tfrac{1}{2}\delta\sqrt{\frac{\pi^4\omega_{pu}^2+64Q^2}{\left[r_{Tpu}\omega_{pu}\pi^2+\left(1-\frac{1}{\omega_{pu}^2}\right)\right]^2+\left[\pi^2\left(\omega_{pu}^2-2\right)-8Qr_{Tpu}\right]^2}} \tag{3.30}$$

(d) Rectifier losses

Similar to the inverter, rectifier losses can be divided into conduction and switching losses; the latter from reverse recovery. Since resonant converters employ high switching frequencies, fast recovery or zero recovery silicon carbide diodes should be used to minimise reverse recovery losses [3.16]. Switching losses will be neglected in the analysis and only conduction losses will be considered. Fig. 3.10 shows typical SPRC rectifier diode voltage/current waveforms.

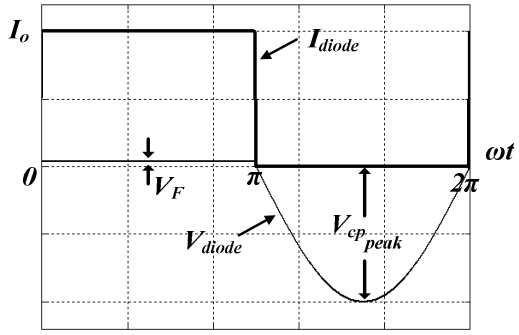


Fig. 3.10: SPRC rectifier diode voltage/current waveforms

Since the diode conducts load current for half the sinusoidal waveform period, diode conduction loss can be given by

$$P_{cond(\mathrm{Rec})} = \frac{1}{T_s}\int_0^{T_S/2} V_F I_o \, dt = ½ V_F I_o \tag{3.31}$$

where V_F is the forward voltage of the rectifier diode obtained from technical datasheet and I_o is the converter load current. Total rectifier losses can therefore be expressed by

$$P_{cond(\mathrm{Rec})} = 2V_F I_o = 2V_F \frac{V_o}{R_L} = \frac{2V_F}{R_L}.\frac{2}{\pi}\left|V_{c_{peak}}\right| \tag{3.32}$$

where $\left|V_{c_{peak}}\right|$ can be obtained from (3.19). This yields

$$P_{cond(\mathrm{Rec})} = \frac{2nV_F V_s \sin ½\delta}{\sqrt{\left[\frac{\pi^2 Z_c}{8Q}\left(2-\omega_{pu}{}^2\right)+r_T\right]^2+\left[\frac{\pi^2 r_T \omega_{pu}}{8Q}+Z_c\left(\omega_{pu}-\frac{1}{\omega_{pu}}\right)\right]^2}} \tag{3.33}$$

The per unit rectifier conduction losses can be therefore expressed as

$$P_{cond(\mathrm{Rec})}(pu) = \frac{2nV_{Fpu} \sin ½\delta}{\sqrt{\left[\frac{\pi^2}{8Q}\left(2-\omega_{pu}{}^2\right)+r_{Tpu}\right]^2+\left[\frac{\pi^2 r_{Tpu}\omega_{pu}}{8Q}+\left(\omega_{pu}-\frac{1}{\omega_{pu}}\right)\right]^2}} \tag{3.34}$$

Applying the efficiency equation (3.16), and using the per unit power equations derived, efficiency versus loading factor Q and normalised frequency ω_{pu} can be plotted. The efficiency of the phase-controlled SPRC is illustrated in Fig. 3.11. The values used for the plot are:

- A nominal 0.01 p.u. value is taken for all parasitic parameters

$$r_{T_{pu}} = r_{Lo_{pu}} = V_{F_{pu}} = V_{ON_{pu}} = 0.01 \text{ p.u.} \tag{3.35}$$

- Maximum phase-shift angle δ_{max}=180°
- Unity transformer turns ratio, n=1. This provides the worst case scenario for the step down transformer, since all losses are directly proportional to n or n^2.

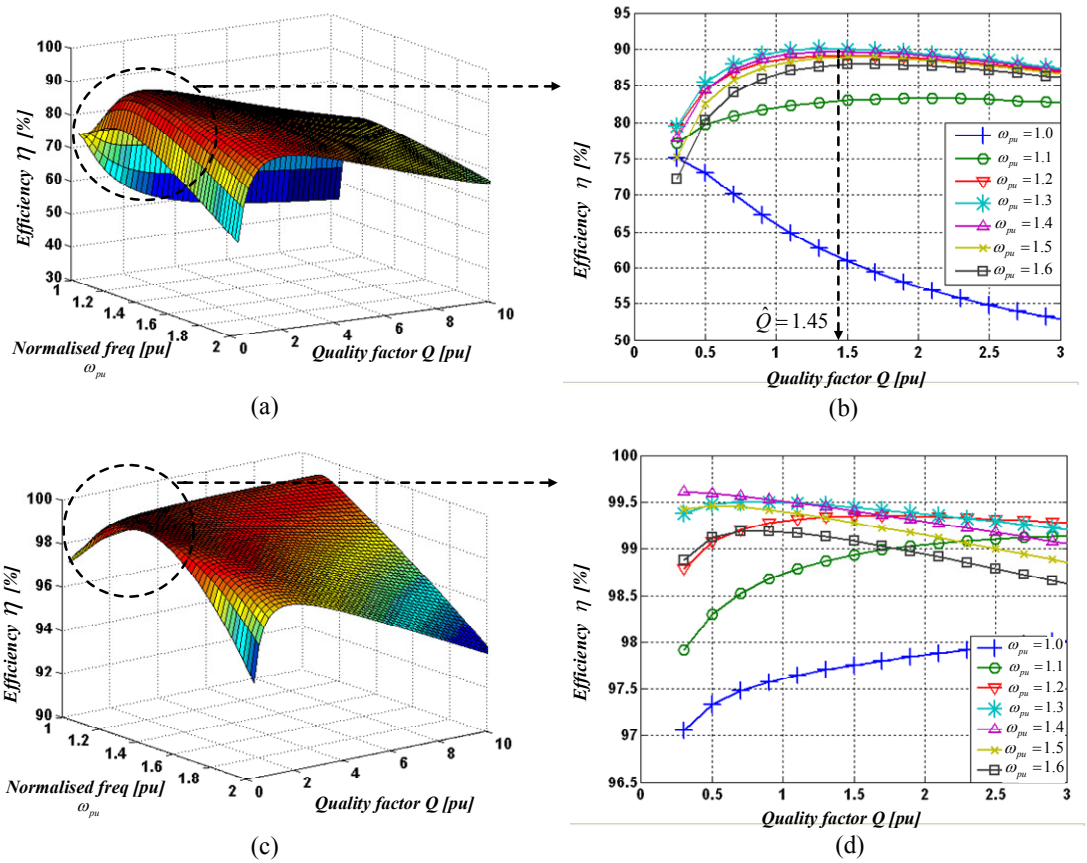


Fig. 3.11: Phase-controlled SPRC efficiency plots (a) 3D view (b) focus on global maximum at selected frequencies (c) 3D view of efficiency considering inverter & rectifier losses only (d) global maximum.

The following can be observed from Fig. 3.11:

- Fig. 3.11(a) shows that converter efficiency deteriorates with excessive loading (high Q) due to increased losses with increased load current.
- At high Q, efficiency is lowest at ω_{pu}=1 rather than at higher frequencies. This is because with high Q, the parallel resonant tank capacitor is effectively short circuited by the low output impedance and the SPRC acts as a series resonant converter (SRC). At ω_{pu}=1, the resonant tank impedance is purely resistive (equal to the parasitic resistances of the resonant tank elements only) causing maximum load current, hence maximum copper, inverter and rectifier losses.
- At low Q, the converter output is effectively open circuit and the SPRC behaviour is similar to that of a parallel resonant converter (PRC). This explains why at high frequencies (where the series L_T-C_s becomes more inductive) the converter behaves more like a PRC with the resonant tank and inverter current being relatively independent of load. This poor part-load efficiency problem is well known for PRCs.

- Efficiency is generally lower as frequency gets closer to ω_{pu}=1 and relatively higher as frequency increases. Higher operating frequency means higher inductive resonant tank impedance. This mitigates the load current, leading to reduced losses. Operating close to resonance causes high currents, hence reduced operating efficiency.
- Fig. 3.11(b) shows a more detailed view of the global maxima. Highest efficiency is approximately 90%, obtained with $\hat{\omega}_{pu} = 1.3$ and $\hat{Q} = 1.45$ (the ^ sign indicates global maxima). This fact will be used in designing the optimum operating conditions for the converter in section 3.3.
- Fig. 3.11 parts (c) and (d) show converter efficiency taking into account only inverter and rectifier losses. Efficiencies ranging from 97% to 99.5% are attained which shows that copper losses account for the majority of the converter losses. This establishes the fact that resonant converters do not suffer from high device losses even when operated at high switching frequencies. This makes them favourable when compared with conventional hard switching converters because higher switching frequencies enable the use of smaller magnetic component sizes.

3.3 Converter design procedure

The steady-state measures studied are used to design optimum operating conditions for the phase-controlled SPRC. First, the optimum resonant tank frequency and full-load Q factor are selected to achieve maximum converter efficiency. Derivation of resonant tank element values is then carried out followed by the high-frequency nano-crystalline transformer design. Finally, a detailed procedure for the output filter design is proposed based on new analytically derived equations for multi-module interleaved operation.

3.3.1 Operating inverter frequency

SPRC phase-control is a fixed frequency control technique. Selection of this fixed frequency affects several aspects of converter operation. Various operation ranges exist:

- ω_{pu}<1: This represents operation below resonance. This is not favourable as ZVS is lost and fast recovery anti-parallel diodes are required for the inverter.
- ω_{pu}=1: This represents the resonance frequency for the series L_T-C_s impedance. Operation at this frequency is not preferred although the converter becomes relatively insensitive to load variations (section 3.2.4). This is because at ω_{pu}=1, operation can be only in modes 3 and 4 where ZVS is partially or fully lost. This depends on Q as

shown in Fig. 3.6. Also, due to the high resonant tank currents at resonance, converter losses are high and efficiency is relatively low.

- $1< \omega_{pu}<\sqrt{2}$: This is the preferred region of frequency operation. A wide voltage gain M range is achievable, as shown in Fig. 3.3 and mode 1 operation is possible with full ZVS. Also, maximum converter efficiency is obtained in this range as shown in Fig. 3.11.
- $\omega_{pu}=\sqrt{2}$: This represents the resonance frequency for the series L_T-C_s-C_p impedance in the case of open-circuit output or light loading conditions. It is dangerous to operate at this frequency or close to it, as currents can be high enough to damage the converter and passive elements.
- $\omega_{pu}>\sqrt{2}$: Although in this frequency range the resonant tank impedance becomes highly inductive, meaning that ZVS is guaranteed (mode 1), converter gain is also mitigated and converter efficiency is reduced.

Therefore, it is evident that the most suitable frequency range is $1< \omega_{pu}<\sqrt{2}$. The selected frequency for maximum efficiency operation is $\hat{\omega}_{pu}=1.3$ as shown in Fig. 3.11.

3.3.2 Full-load *Q* factor

Q_{FL} represents the ratio between the resonant tank characteristic impedance and full-load output resistance. To operate at maximum converter efficiency, it is acceptable to assign $Q_{FL}=\hat{Q}=1.45$ as shown in Fig. 3.11.

3.3.3 Resonant tank elements value and ratings

As outlined in section 1.4, the *All-Electric* subsea project delivers power in the range of 10-15 kW. Typical transmission voltage is 10 kVdc, with a load-side voltage of 1 kVdc. The load-side step down converter, under consideration, comprises the modular architecture of the dc/dc phase-controlled SPRCs as discussed in section 2.4. Since the modular architecture will involve series-parallel connection of SPRCs, the above-mentioned ratings will be shared by the separate modules. Typical module ratings are:

- Power rating: 0.5-1 kW
- Module input voltage: 500 Vdc
- Module output voltage: 100 Vdc

- Module input current: 1-2 A
- Module output current: 5-10 A

Hence, the typical full-load output impedance R_{LFL} is 10-20 Ω. Using the selected Q_{FL}=1.45, and applying $Q_{FL}=Z_c/R_{LFL}$ then the characteristic impedance Z_c would be in the range of 14.5-29 Ω. The choice of Z_c and resonant frequency ω_0 will determine the values of resonant tank elements L_T and C_s.

The characteristic impedance typically affects converter voltage gain M as well as the ratio of the load to resonant tank currents. Examining these two factors aids in selecting an appropriate value for Z_c in the selected range. Re-formulating (3.4) and considering Fig. 3.4 while neglecting resonant tank parasitic resistance r_T , the following gains can be obtained as a function of Z_c

$$M=\frac{V_o}{V_s}=\frac{n\sin\tfrac{1}{2}\delta}{\sqrt{\left[\left(\frac{\pi^2}{8}\left(2-\omega_{pu}{}^2\right)\right)^2+\left(\frac{Z_c}{R_L}\left(\omega_{pu}-\frac{1}{\omega_{pu}}\right)\right)^2\right]}} \tag{3.36}$$

$$G=\frac{I_o}{I_L}=\frac{\pi\sqrt{2}}{4}\frac{1}{\sqrt{1+\left(\frac{\pi^2}{8}\frac{R_L\omega_{pu}}{Z_c}\right)^2}} \tag{3.37}$$

G is a ratio of output current to RMS resonant inductor current and is optimal as it approaches 1.11. At this value resonant tank current approaches the load current value. This means the resonant tank circulating current is not higher than the load current at light (part) loads, hence the converter part load efficiency is not poor. From (3.36) and (3.37), a high value of Z_c results in a current ratio G close to 1.11, however, converter voltage gain M is reduced and vice versa. Therefore Z_c is selected as an intermediate value in the range Z_c=14.5-29 Ω in order to compromise for both gains M and G.

Also, since $\hat{\omega}_{pu}=1.3$ has been selected and with an inverter switching frequency of f=40 kHz, the resonant tank natural frequency f_0 can be calculated as

$$f_0=\frac{1}{2\pi\sqrt{L_T C_S}}=\frac{f}{\hat{\omega}_{pu}}=30769\text{Hz} \tag{3.38}$$

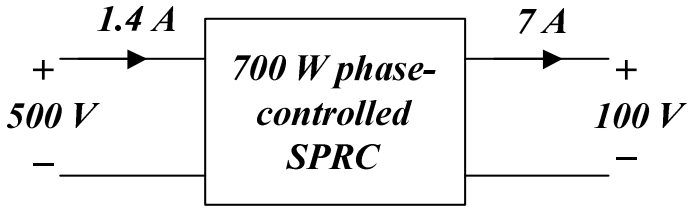
Applying (3.38) and using $Z_C = \sqrt{L_T / C_S}$, values for L_T and C_s can be obtained. Component ratings for the resonant tank inductor and capacitor can be obtained using (3.37) and (3.39). Table 3.2 summarises designed and calculated values for the subsea project.

$$V_{Cs} = I_L X_{Cs} = \frac{4}{\pi\sqrt{2}} \frac{Z_c}{\omega_{pu}} \sqrt{1 + \left(\frac{\pi^2}{8} \frac{R_L \omega_{pu}}{Z_c} \right)^2} I_o \tag{3.39}$$

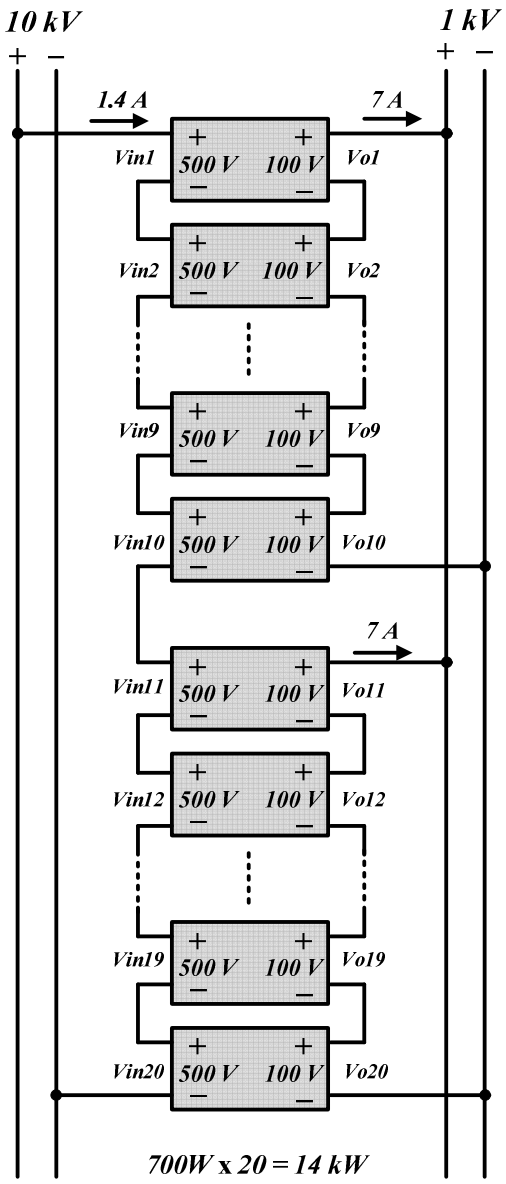
Parameter	*Definition*	*Value*	*Component rating*
Z_c	Characteristic impedance	20.7 Ω	-
Q_{FL}	Full-load Q factor	1.45	-
R_{LFL}	Full-load impedance	14.3 Ω	-
f	Inverter switching frequency	40 kHz	-
f_0	Resonant tank natural frequency	30.77 kHz	-
V_s	Input supply voltage	500 V	-
V_o	Output (load) voltage	100 V	-
I_{OFL}	Full-load output current	7 A	-
P_{FL}	Module full-load power rating	700 W	-
n	Transformer turns ratio	0.2	-
L_T	Total equivalent resonant inductance	107 µH	I_{LFL}=1.344I_{OFL}=9.41 A (RMS)
C_s	Series resonant capacitance	250 nF	V_{Cs}=21.4 I_{OFL}=150 V (RMS)
C_p	Parallel resonant capacitance	250 nF	V_{Cp}=V_oπ/2√2=111 V (RMS)

Table 3.2: Converter parameter values and ratings

Fig. 3.12(a) shows a schematic diagram of the proposed SPRC module, with full-load operating values. Fig. 3.12(b) shows how 20 such modules are connected in an input-series output-series/output-parallel (ISOS/OP) connection to obtain 10kVdc/1kVdc, 14 kW step down operation. This configuration is suitable for the load side subsea converter unit.



(a)



(b)

Fig. 3.12: (a) Proposed SPRC, full-load operating values (b) 20 modules connected in ISOS/OP to achieve the 14 kW, 10kVdc/1 kVdc step down load side converter

3.3.4 Nano-crystalline core transformer

(a) Transformer core model selection

This section gives a detailed design procedure for the nano-crystalline core transformer used in the phase-controlled SPRC. Nano-crystalline material is preferred for high-frequency operation due to its high core permeability, high magnetizing inductance and near square hysteresis loop [3.17]. Reduced transformer volume due to high-frequency operation supports the modularity of system design. As shown in Fig. 3.1, the transformer primary is connected to the inverter output so the input voltage to the transform-

er is a quasi-square wave signal. The secondary winding is connected to the resonant tank, hence the transformer rated secondary current is the rated resonant tank inductor current (9.41 A RMS) as calculated in Table 3.2. Fig. 3.13 shows a schematic with the transformer typical ratings. Table 3.3 summarises the notation used in the design process.

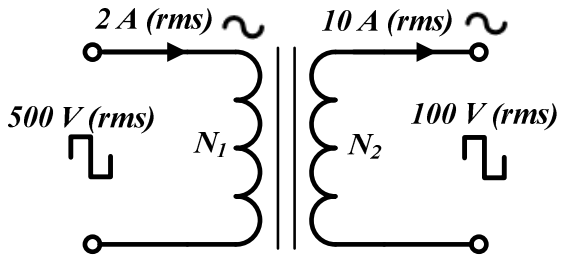


Fig. 3.13: Nano-crystalline core transformer full-load ratings

Parameter	*Definition*	
E_1	Primary winding emf	(V)
I_1	Primary current	(A)
I_2	Secondary current	(A)
N_1	Primary number of turns	
N_2	Secondary number of turns	
a_1	Primary copper wire cross-sectional area	(mm^2)
a_2	Secondary copper wire cross-sectional area	(mm^2)
J	Current density	(A/mm^2)
W_c	Total copper wire area in window	(mm^2)
k_u	Window utilization factor	
W_a	Window area	(mm^2)
A_c	Transformer core cross-sectional area	(mm^2)
f	Frequency of operation	(kHz)
B	Operating flux density	(T)
B_{sat}	Saturation flux density	(T)
μ_r	Relative permeability	
k	Form factor	

Table 3.3: Transformer design notations

The design process starts by assuming the number of primary turns

$$N_1 = 40 \text{ turns} \tag{3.40}$$

The secondary turns are

$$N_2 = \frac{V_2}{V_1} \times N_1 = \frac{100}{500} \times 40 = 8 \,\text{turns} \tag{3.41}$$

From the standard American Wire Gauge (AWG) copper wiring tables

$$J = 3 \text{ A/mm}^2 \tag{3.42}$$

$$a_1 = \frac{I_1}{J} = \frac{2}{3} = 0.67 \text{ mm}^2 \tag{3.43}$$

From AWG tables, the closest available conductor size is AWG#18 (cross-sectional area of 0.823 mm^2). However, the maximum frequency for 100% skin depth is 17 kHz. Since the operating frequency is f=40 kHz, conductors AWG#22 and higher can only be used. AWG#23 (cross-sectional area of 0.258 mm^2) is selected with 3 conductors connected in parallel. Therefore, actual primary winding copper cross-sectional area is

$$a_1 = 0.258 \times 3 = 0.774 \text{ mm}^2 \tag{3.44}$$

Similarly, for the secondary winding

$$a_2 = \frac{I_2}{J} = \frac{10}{3} = 3.33 \text{ mm}^2 \tag{3.45}$$

AWG#23 is selected with 13 conductors connected in parallel. The actual secondary winding copper cross-sectional area is

$$a_2 = 0.258 \times 13 = 3.354 \text{ mm}^2 \tag{3.46}$$

The total copper wire area in the window can be calculated as

$$W_c = N_1 a_1 + N_2 a_2 = 57.8 \text{ mm}^2 \tag{3.47}$$

Assuming a window utilization factor k_u=0.4, the window area must satisfy

$$W_a \geq \frac{W_c}{k_u} = \frac{57.8}{0.4} = 144.5 \text{ mm}^2 \tag{3.48}$$

The emf equation is used to calculate the transformer core cross-sectional area A_c:

$$E_1 = k f A_c B N_1 \tag{3.49}$$

where E_1=500V, k=4 (square wave), f=40 kHz, N_1=40 and B=0.8×B_{sat}=0.8×1.2=0.96 T.

$$A_c = 0.8138\ \text{cm}^2 \tag{3.50}$$

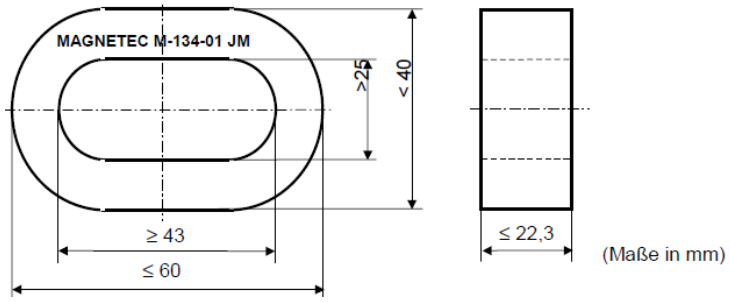
Using the design criteria in (3.48) and (3.50), the "*Magnetec GmbH M-134-01 JM*" transformer core is selected. The core data is [3.17]:

$$\begin{aligned} \mu_r &= 30000 \text{ at } 40\text{kHz} \\ A_c &= 0.8\ \text{cm}^2 \\ W_a &= 940.87\ \text{mm}^2 \end{aligned} \tag{3.51}$$

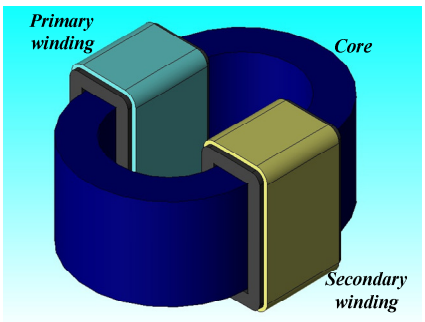
The actual operating values become

$$\begin{aligned} B &= 0.976\ \text{T} \\ k_u &= \frac{W_c}{W_a} = \frac{57.8}{940.87} = 0.0614 \text{ or } 6.14\% \end{aligned} \tag{3.52}$$

This window utilization factor allows space for the winding insulation. Fig. 3.14 shows core dimensions which verify its suitability for the modular converter design and shows a 3D view of the core drawn using the Finite Element Analysis (FEA) software JMAG-Designer.



(a)



(b)

Fig. 3.14: Core schematic (a) Dimensions (from Magnetec GmbH datasheet) and (b) 3D view.

(b) Leakage inductance calculation

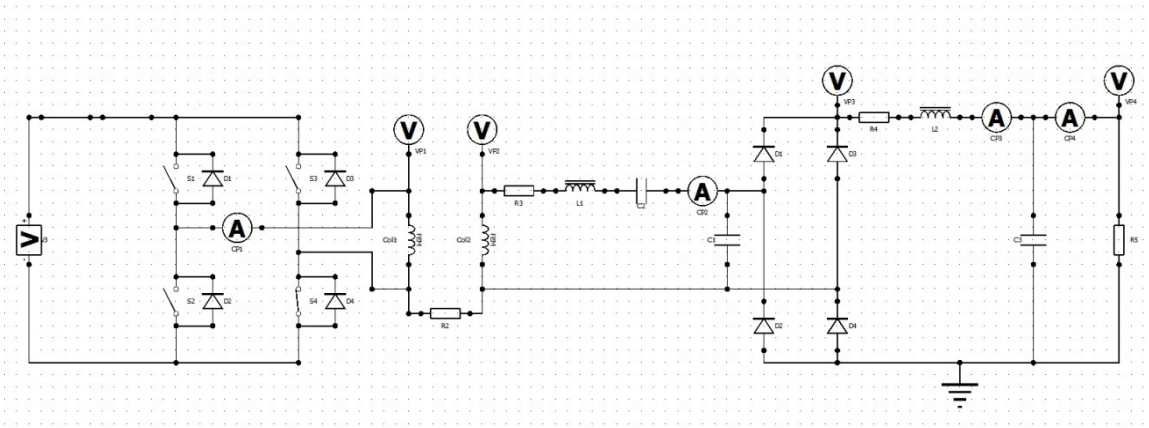
The leakage inductance L_l of the transformer is part of the design procedure outlined in section 3.3.3 and is incorporated in the value of the total resonant inductance L_T given by

$$L_T = L_S + L_l \tag{3.53}$$

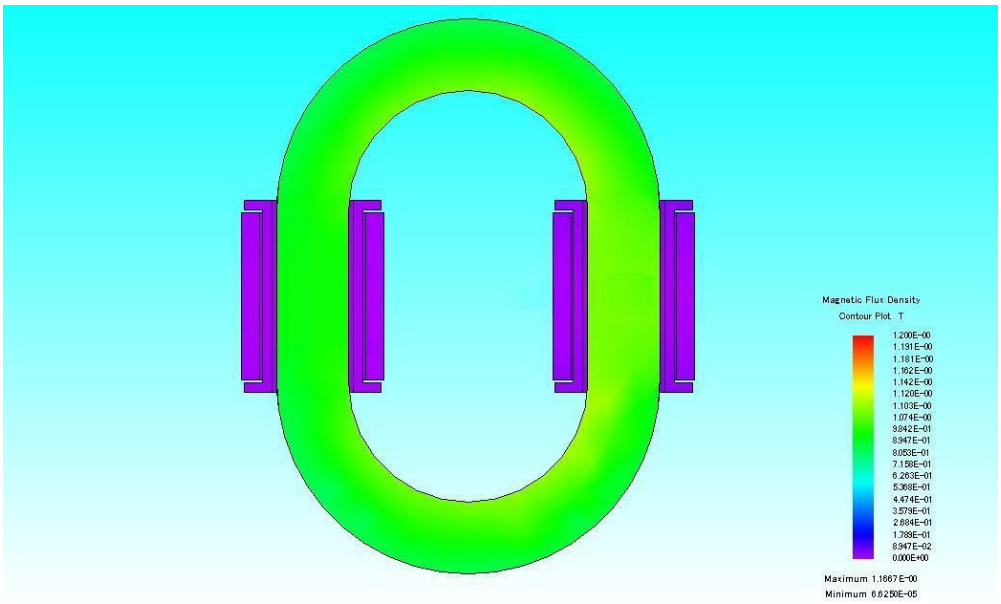
This enables calculation of the actual resonant inductance L_s to be added in the resonant tank in series with transformer secondary winding. This means that L_l has to be referred to the secondary side. This is performed in JMAG-Designer by performing a short-circuit test on the transformer designed. The primary winding is short circuited and a small voltage (just enough to reach rated transformer current) at the 40 kHz nominal operating frequency is applied to the secondary winding. Using the magnitudes and phase angles of the voltage and resulting current, values of the parasitic transformer resistance r_l and leakage inductance L_l are obtained referred to the secondary. The calculated values for the designed transformer are r_l=0.4Ω and L_l=7.4μH. Therefore, the value of L_s is

$$L_S = L_T - L_l = 107 - 7.4 = 99.6\mu H \tag{3.54}$$

In order to check the operating core flux density does not reach saturation and complies with the calculated value in (3.52), the phase-controlled SPRC is implemented using the JMAG-Designer circuit simulator tool and connected to the transformer operating at rated designed values. The system is simulated using FEA. Fig. 3.15(a) shows a schematic of the circuit simulator diagram and Fig. 3.15(b) shows the operating core flux density B which, at rated values, operates in vicinity of the calculated value in (3.52).



(a)



(b)

Fig. 3.15: (a) Converter circuit diagram using JMAG-Designer circuit simulator and (b) Maximum operating core flux density

(c) Core loss calculation

Transformer core losses are a function of the operating frequency and magnetic flux density. Assuming the operating flux density B is constant and near saturation ($B=0.8B_{sat}$ is commonly selected), a general expression for the core losses is

$$P_{Fe} = A\omega_{pu}{}^{K} \tag{3.55}$$

where A and K are proportionality constants determined by the transformer manufacturer. The "*Magnetec GmbH M-134-01 JM*" nano-crystalline core transformer implemented has a core power loss equation given by [3.17]

$$P_{Fe} = P_1 \times \left(\frac{F}{F_1}\right)^{x} \times \left(\frac{f}{f_1}\right)^{y} \times \left(\frac{B}{B_1}\right)^{z} \tag{3.56}$$

where the constants F_1, f_1 and B_1 are the initial form factor, frequency, and magnetic flux density, at which the power loss P_1 is calculated, while F, f, and B are the applied voltage form factor, frequency, and magnetic flux density respectively. Equation (3.56) can be re-formulated:

$$P_{Fe} = P_1 \times \left(\frac{F}{F_1}\right)^{x} \times \left(\frac{1}{f_1} \times \frac{\omega}{2\pi} \times \frac{\omega_0}{\omega_0}\right)^{y} \times \left(\frac{B}{B_1}\right)^{z} = \left[P_1 \times \left(\frac{F}{F_1}\right)^{x} \times \left(\frac{1}{f_1} \times \frac{\omega_0}{2\pi}\right)^{y} \times \left(\frac{B}{B_1}\right)^{z}\right] \omega_{pu}{}^{y} \tag{3.57}$$

Comparing (3.57) with (3.55) yields

$$A = P_1 \times \left(\frac{F}{F_1}\right)^x \times \left(\frac{1}{f_1} \times \frac{\omega_0}{2\pi}\right)^y \times \left(\frac{B}{B_1}\right)^z$$
$$K = y \tag{3.58}$$

The resonant tank frequency implemented is defined in Table 3.2 ($\omega_0/2\pi$=30769 Hz), the operating transformer flux density B=0.8B_{sat}=0.8×1.2=0.96T, and the operating form factor F=1 due to quasi square wave inverter output. The remaining constants are supplied by the manufacturer [3.17], P_1=60 W/Kg, m_{Fe}=83.1g, F_1=1.11, f_1=100 kHz, B_1=0.3 T, x=1.6, y=1.8 and z=2. Substituting these values into (3.58) yields

$$P_{Fe} = 5\omega_{pu}^{1.8} \quad \text{(W)} \tag{3.59}$$

Therefore, the transformer core losses at full-load are

$$P_{Fe} = 5(1.3)^{1.8} = 8\text{W} \tag{3.60}$$

To convert this to a per unit equivalent, P_{Fe} is referred to P_{base} defined in (3.17)

$$P_{Fe}(pu) = \frac{P_{Fe}}{P_{base}} = \frac{P_{Fe}Z_c}{V_s^2} = \frac{8 \times 20.7}{500^2} = 0.00066\text{pu} \tag{3.61}$$

Equation (3.61) shows that the transformer losses are negligible which verifies the low core loss characteristic of the nano-crystalline material although the operating frequency is high.

3.3.5 Output filter

The phase-controlled SPRC uses an LC output filter to attenuate the high-frequency ac components and to obtain a dc output voltage with minimum ripple. However, the output ripple content is a design trade-off with the size of the filter elements. This is an important issue if modularity and compact physical size are key design criteria.

In this section, novel analytical expressions relating ripple amplitude with LC filter element values for the phase-controlled SPRC are derived. The LC filter element values are dependent upon whether the converter operates in a single or a multi-module mode. In multi-module operation, interleaving the inverter control signals can lead to reduced

ripple, hence smaller filter elements will be required. The design procedure for each component follows.

(a) Single module converter operation

Fig. 3.16 shows the circuit diagram of the output filter with v_{Br} being the output bridge rectifier voltage, and typical waveforms for a sinusoidal voltage input to the rectifier. Undefined parameters are stated in Table 3.4.

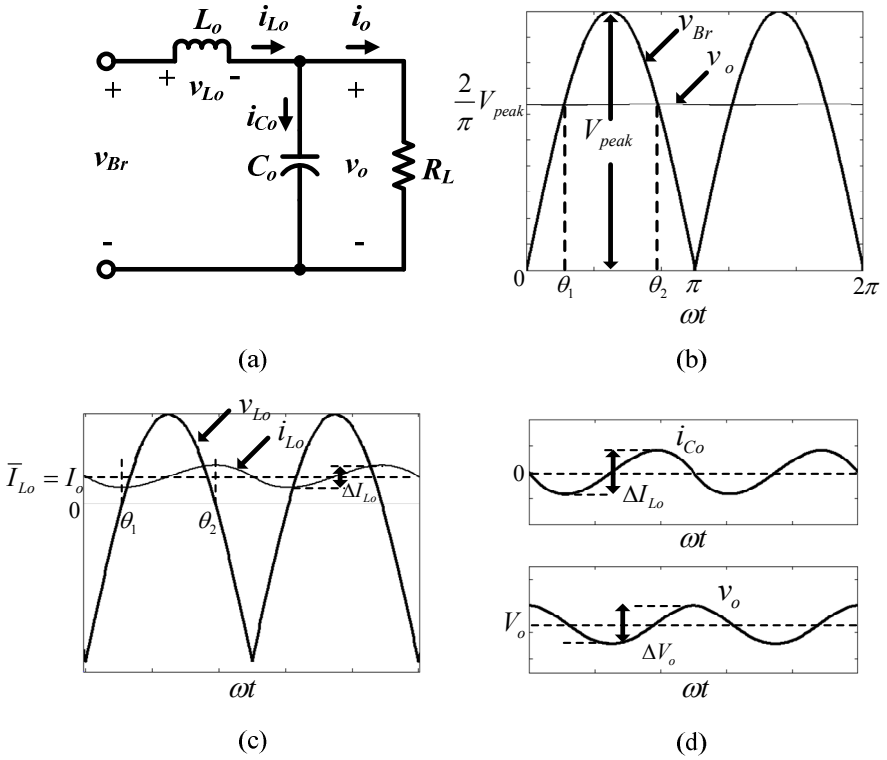


Fig. 3.16: SPRC output filter (a) circuit diagram, (b) bridge rectifier output voltage and converter output voltage, (c) inductor voltage and current and (d) capacitor voltage and current

Parameter	***Definition***	
V_{peak}	Peak bridge rectifier output voltage	(V)
θ_1	$\sin^{-1}\left(\frac{2}{\pi}\right) = 0.69$	(rad)
θ_2	$\pi - \sin^{-1}\left(\frac{2}{\pi}\right) = 2.45$	(rad)
ΔI_{Lo}	Ripple inductor current	(A)
ΔV_o	Ripple capacitor voltage	(V)
$\bar{I}_{Lo}$	Average inductor current	(A)
I_o	Average output load current	(A)
V_o	Average capacitor (load) voltage	(V)

Table 3.4: Output filter parameter definition

The maximum inductor current ripple ΔI_{Lo} can be obtained by integrating the *average positive* inductor voltage $\bar{V}_{Lo}^{+}$ over the period from θ_1 to θ_2

$$\Delta I_{Lo} = \frac{1}{\omega L_o}\int_{\theta_1}^{\theta_2} \bar{V}_{Lo}^{+}\, d\omega t = \frac{\bar{V}_{Lo}^{+}(\theta_2 - \theta_1)}{2\pi f L_o} \tag{3.62}$$

$$\begin{aligned}
\bar{V}_{Lo}^{+} &= \frac{1}{(\theta_2 - \theta_1)}\int_{\theta_1}^{\theta_2} v_{Lo}\, d\omega t \\
&= \frac{1}{(\theta_2 - \theta_1)}\int_{\theta_1}^{\theta_2} \left(V_{peak}\sin\omega t - V_o\right) d\omega t \\
&= \frac{V_o}{(\theta_2 - \theta_1)}\int_{\theta_1}^{\theta_2} \left(\frac{\pi}{2}\sin\omega t - 1\right) d\omega t \\
&= \frac{V_o}{(\theta_2 - \theta_1)}\left(\pi\cos\theta_1 - \theta_2 + \theta_1\right)
\end{aligned} \tag{3.63}$$

Substituting (3.63) into (3.62) yields

$$\Delta I_{Lo} = \frac{V_o\left(\pi\cos\theta_1 - \theta_2 + \theta_1\right)}{2\pi f L_o} = 0.105\frac{V_o}{f L_o} \tag{3.64}$$

For 0.5% ripple in the filter inductor current at the nominal operating converter values stated in Table 3.2, the value of L_o can be calculated

$$L_o = 0.105 \times \frac{V_o}{f\Delta I_{Lo}} = \frac{0.105 \times 100}{40000 \times 0.005 \times 7} = 7.5\text{mH} \tag{3.65}$$

Assuming the ripple capacitor current i_{Co} in Fig. 3.16(d) is sinusoidal:

$$\Delta V_o = \Delta I_{Lo} X_{Co} = \frac{\Delta I_{Lo}}{2\pi f C_o} \tag{3.66}$$

For 0.5% output voltage ripple at nominal converter ratings, C_o is

$$C_o = \frac{\Delta I_{Lo}}{2\pi f \Delta V_o} = \frac{0.005 \times 7}{2\pi \times 40000 \times 0.005 \times 100} = 278.5\text{nF} \tag{3.67}$$

(b) Multi-module converter operation (designed with interleaving)

When multiple output filters of the phase-controlled SPRC are connected in series/parallel, a technique known as *interleaving* is used so that current and voltage ripple of each converter do not reinforce, but instead tend to cancel. This technique results by phase shifting the switching instants of the converters over a switching period. By introducing a symmetrical phase-shift between the parallel/series converters, the output filter capacitor ripple is lowered due to ripple cancellation effects. As a result, the size of the output filter capacitance can be minimized [3.18, 19]. For the *All-Electric* subsea project, the phase-controlled SPRCs will be connected in ISOP and ISOS connections, as shown in Fig. 3.12(b), which means the output filter from one module is connected in series or parallel with other modules. Table 3.5 summarises possible configurations for *m*-connected modules. To preserve system modularity and to maintain system fault tolerant operation in case any module should fail, config#1 for both ISOP and ISOS will be implemented. For ISOP connection, interleaving reduces the total inductor ripple current, and the resulting ripple is further reduced by dividing it among the parallel output capacitors. Fig. 3.17 shows a reformulation of the config#1 circuit diagram and Fig. 3.18 gives typical results for interleaving two modules (*m*=2) with parallel output filters.

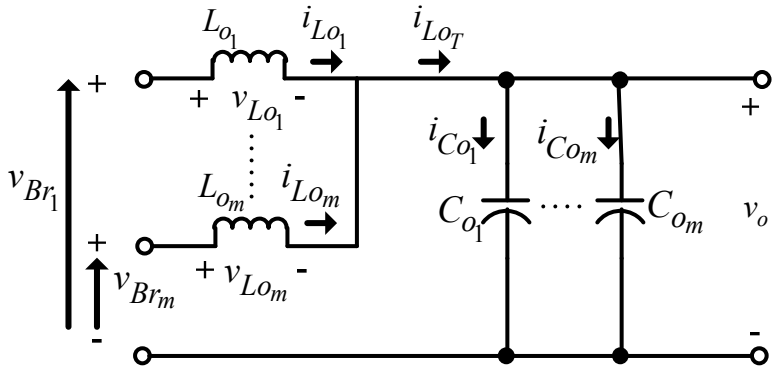


Fig. 3.17: Config#1 for ISOP connection

From Fig. 3.17:

$$i_{Lo_T} = \sum_{i=1}^{m} i_{Lo_i} \tag{3.68}$$

Assuming $L_{o_1} = L_{o_2} = ... = L_{o_m} = L_O$

$$i_{Lo_T} = \frac{1}{L_o} \int \sum_{i=1}^{m} v_{Lo_i}\, dt \tag{3.69}$$

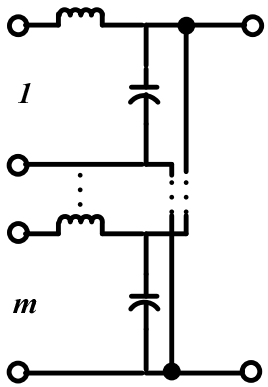
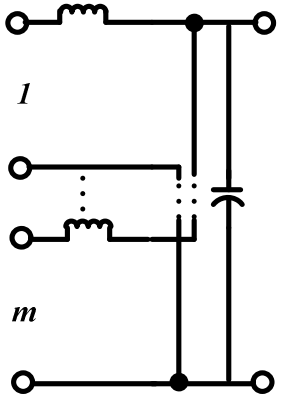
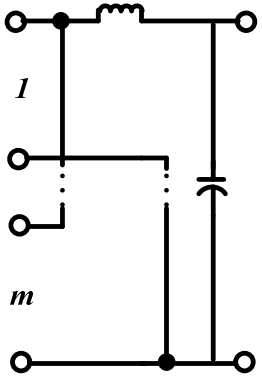
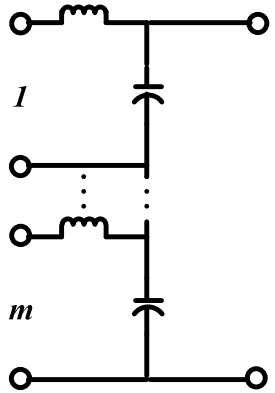
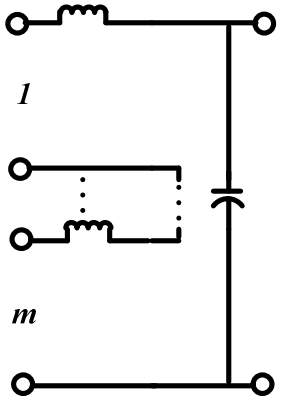
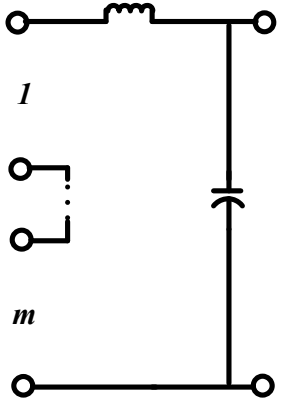
	Config#1	*Config#2*	*Config#3*	*Notes*
ISOP				• Config#1 preserves system modularity and system fault tolerant capability. Also, total inductor current ripple is divided among the parallel output capacitors, hence smaller ripple per capacitor. • In config#2, output capacitance needs to be *m* times the modular capacitance for the same output voltage ripple. Also, it has poor fault tolerance due to possibility of output capacitor failure. • In config#3, the inductor needs to be *m* times larger in current rating relative to the modular inductor. Also, config#3 has poor fault tolerance.
ISOS				• Config#1 preserves system modularity and system fault tolerant capability. The module capacitor has the full module inductor current ripple, so interleaving would only reduce total output voltage ripple but not individual capacitor ripple current. • In config#2 and config#3, ripple cancellation occurs when interleaving so the output capacitor has reduced ripple current. However, the output capacitor voltage rating is *m* times the modular capacitor voltage, i.e. it experiences the full output voltage. With both configurations, system modularity and fault tolerance are degraded due to the possibility of output capacitor failure.

Table 3.5: Possible connection configurations for *m* modules with ISOP and ISOS connections

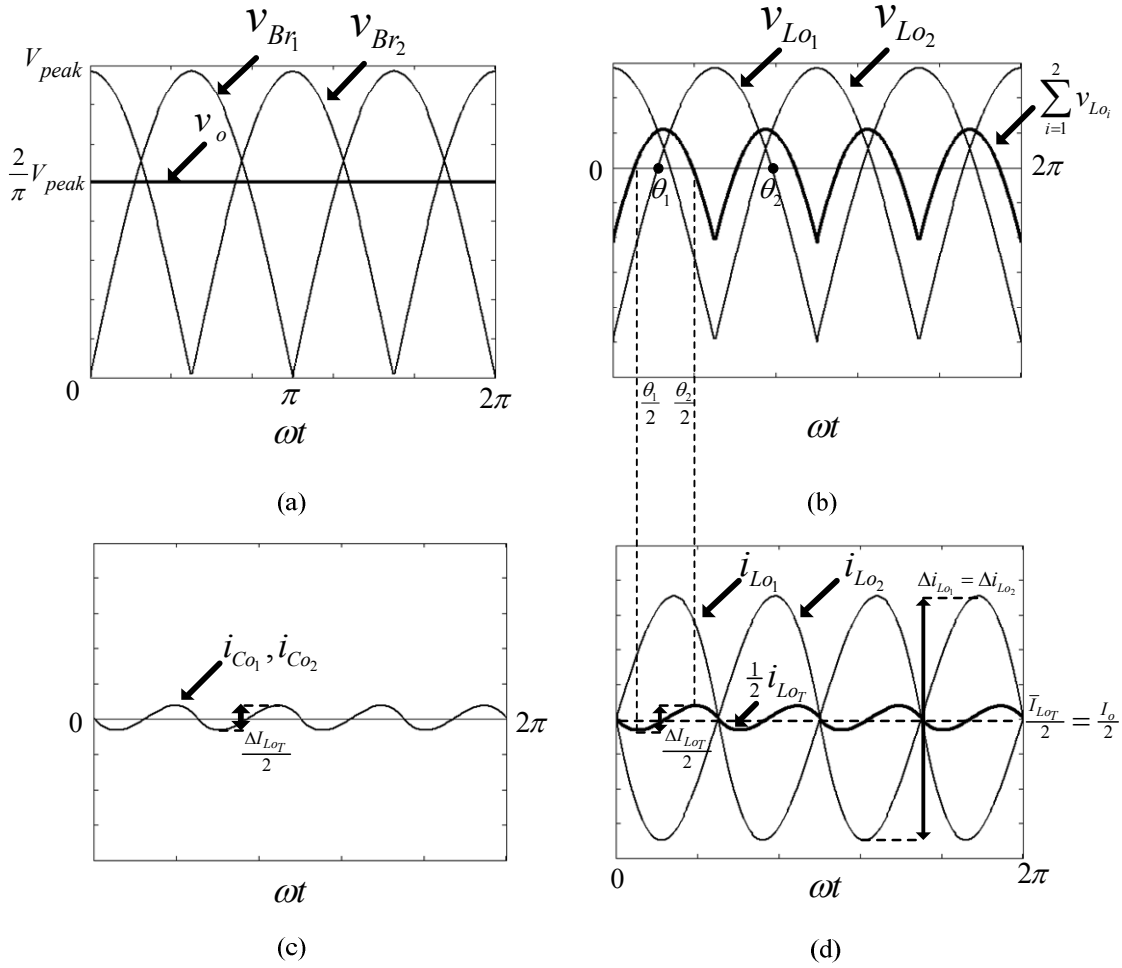


Fig. 3.18: Results for two interleaved SPRC output filters in ISOP connection (a) bridge rectifier output voltages and converter output voltage, (b) inductor voltages, (c) capacitor currents, (d) inductor currents

From the results in Fig. 3.18, $\sum_{i=1}^{m} v_{Lo_i}$ experiences *m* times the frequency of v_{Lo_i} due to interleaving the bridge rectifier outputs by π/m radians. The total inductor current ripple ΔI_{Lo_T} can be obtained by integrating the *average positive* aggregated inductor voltage over the period θ_1/m to θ_2/m as illustrated by Fig. 3.18(b) and (d).

$$\Delta I_{Lo_T} = \frac{1}{\omega L_o} \int_{\frac{\theta_1}{m}}^{\frac{\theta_2}{m}} \left(\overline{\sum_{i=1}^{m} v_{Lo_i}} \right)^{+} d\omega t = \frac{\left(\overline{\sum_{i=1}^{m} v_{Lo_i}} \right)^{+} \left(\frac{\theta_2}{m} - \frac{\theta_1}{m} \right)}{2\pi f L_o} \tag{3.70}$$

$$\left(\overline{\sum_{i=1}^{m} v_{Lo_i}}\right)^{+} = \frac{m}{\theta_2-\theta_1}\int_{\frac{\theta_1}{m}}^{\frac{\theta_2}{m}}\sum_{k=1}^{m}\left[V_{peak}\sin\left(\omega t+\frac{(k-1)\pi}{m}\right)-V_o\right]d\omega t$$

$$= \frac{mV_o}{\theta_2-\theta_1}\int_{\frac{\theta_1}{m}}^{\frac{\theta_2}{m}}\sum_{k=1}^{m}\left[\frac{\pi}{2}\sin\left(\omega t+\frac{(k-1)\pi}{m}\right)-1\right]d\omega t \tag{3.71}$$

Substituting (3.71) into (3.70) yields

$$\Delta I_{Lo_T} = \frac{V_o}{2\pi f L_o}\int_{\frac{\theta_1}{m}}^{\frac{\theta_2}{m}}\sum_{k=1}^{m}\left[\frac{\pi}{2}\sin\left(\omega t+\frac{(k-1)\pi}{m}\right)-1\right]d\omega t \tag{3.72}$$

Substituting into (3.72) for m=2 yields $\Delta I_{Lo_T} = \frac{0.021\times V_o}{fL_o}$ and for m=3, $\Delta I_{Lo_T} = \frac{0.009\times V_o}{fL_o}$ which are both lower than the ripple given by a single output filter (m=1) as calculated in (3.64). As the number of paralleled modules increases, total inductor current ripple decreases. In other words, for the same total current ripple as the single-module case, L_o can be reduced hence smaller in size. The value of L_o for all modules can be calculated from (3.72) according to the required total ripple current ΔI_{Lo_T}. From Fig. 3.17, the total ripple capacitor current is equivalent to ΔI_{Lo_T}. However, since m-module capacitors are connected in parallel, individual module capacitor current ripple is

$$\Delta I_{Co_i} = \frac{\Delta I_{Lo_T}}{m} \tag{3.73}$$

Hence, assuming sinusoidal ripple currents, the output voltage ripple is given by

$$\Delta V_o = \frac{\Delta I_{Co_i}}{2\pi f C_o} = \frac{\Delta I_{Lo_T}}{2\pi f m C_o} \tag{3.74}$$

This shows that output voltage ripple is m times smaller than the total inductor current ripple. The value of C_o for all modules can be calculated from (3.74) after the required output voltage ripple is specified.

For ISOS connection, config#1 in Table 3.5 shows that each module acts separately with module outputs being series-connected. This means that, even with interleaving

between modules, individual module capacitor ripple currents are equal to the module inductor current ripple. This is verified from Fig. 3.19(a) and (b) which illustrates typical results for interleaving two modules (m=2) with series output filters. Ripple cancellation effects only manifest in the aggregate load voltage and current as shown in Fig. 3.19(c). Hence, individual module inductance and capacitance values (L_o and C_o) for ISOS connected modules can be designed as in the single-module operation design procedure outlined by (3.62)-(3.67).

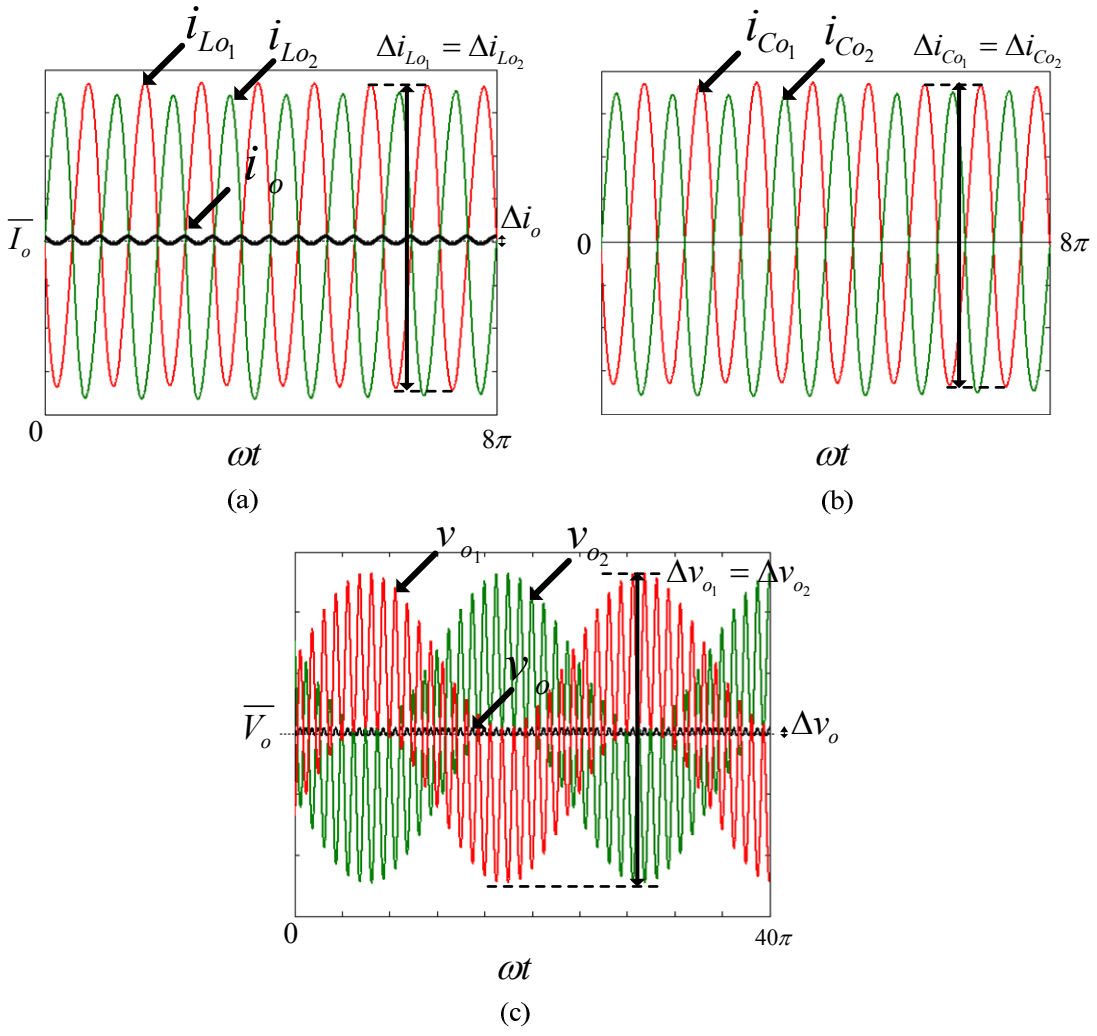
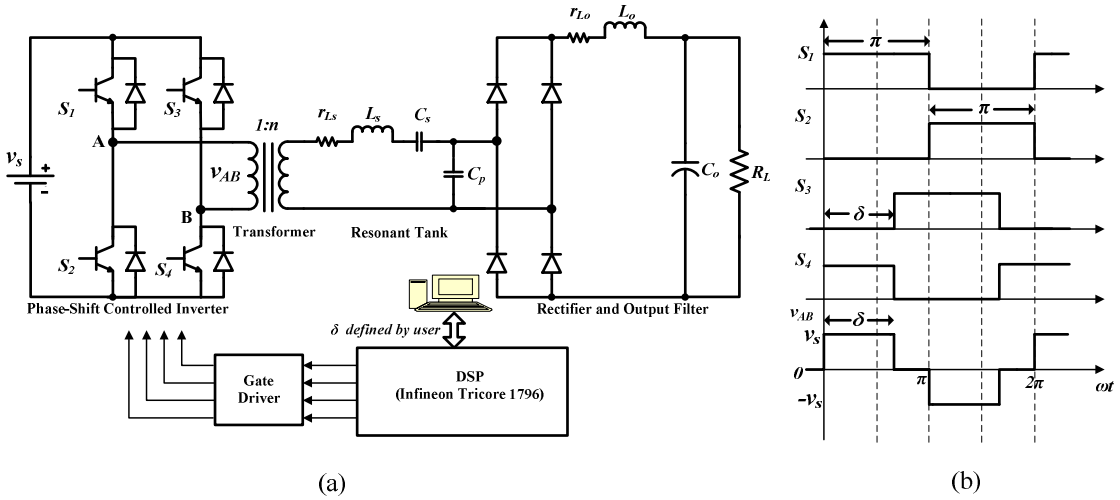


Fig. 3.19: Results for two interleaved SPRC output filters in ISOS connection (a) module inductor currents and output (load) current, (b) capacitor currents, (c) module output voltages and total load voltage.

3.4 Simulation and experimental prototype results

The 700W phase-controlled SPRC designed with the rated full-load values in Table 3.2 is scaled down to a 40W experimental laboratory prototype. The prototype converter circuit diagram is shown in Fig. 3.20. Element and operating values used are summa-

rised in Table 3.6. Optimum full-load designed conditions $\hat{Q}=1.45$ and $\hat{\omega}_{pu}=1.3$ (corresponding to maximum efficiency) are applied to the prototype converter.



(a) (b)

Fig. 3.20: Experimental prototype (a) circuit diagram and (b) inverter phase control gating pattern.

Parameter	***Definition***	***Value***
Z_c	Resonant tank characteristic impedance	20.7 Ω
Q_{FL}	Full-load Q factor	1.44
R_{LFL}	Full-load resistive load	14.4 Ω
f	Inverter switching frequency	40 kHz
L_s	Series resonant inductance	100.13 µH
L_l	Transformer leakage inductance (referred to secondary)	9.12 µH
L_T	Total equivalent resonant inductance (referred to secondary)	109.25 µH
C_s	Series resonant capacitance	255 nF
C_p	Parallel resonant capacitance	255 nF
f_0	Resonant tank natural frequency	30.154 kHz
ω_{pu}	Normalised frequency	40/30.154=1.327
L_o	Output filter inductance	12.5 mH
C_o	Output filter capacitance	120 µF
V_s	Input supply voltage	60 V
V_o	Output (load) voltage	24 V
I_{OFL}	Full-load output current	1.67 A
P_{FL}	Converter full-load power rating	40 W
n	Transformer turns ratio	0.5
δ_{FL}	Full-load inverter phase-shift angle (from equation 3.4)	90°

Table 3.6: Experimental prototype converter element and operating values

3.4.1 Full-load operation

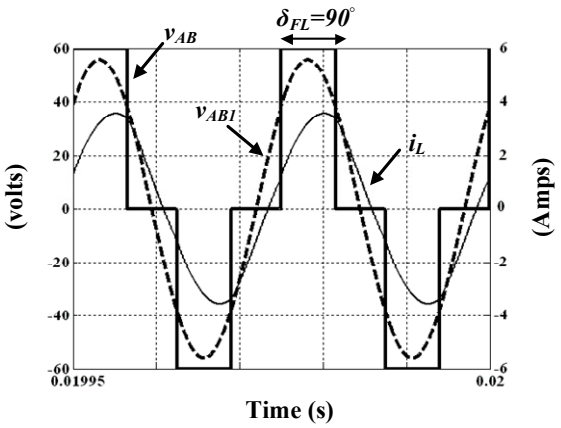
Fig. 3.21 shows full-load operation results for the 40W, 40 kHz phase-controlled SPRC prototype. The following can be concluded from the results:

- At full-load (δ_{FL}=90°, Q_{FL}=1.44 and ω_{pu}=1.327), the converter operates in mode 2. This is evident from Fig. 3.21(a) and (b) showing i_L lagging the fundamental inverter output voltage v_{AB1} (inductive resonant tank impedance) while leading the positive-going edge of v_{AB}. Operation in this mode is verified by Fig. 3.6 illustrating the mode boundaries which, at the full-load operating conditions, shows that the converter operates in mode 2. With this mode, the inverter leading leg loses ZVS while it is retained by the inverter lagging leg. Fast recovery anti-parallel diodes are necessary for the leading leg switches.
- Fig. 3.21(e) and (f) show that under the selected full-load conditions, output voltage V_o=24V, and the average inductor current $\bar{I}_{Lo}$=1.67A, which is equivalent to the output (load) current: the full-load output power equals 40W.
- Peak values for i_L, v_{Cs} and v_{Cp} can be verified as calculated in (3.37) and (3.39).

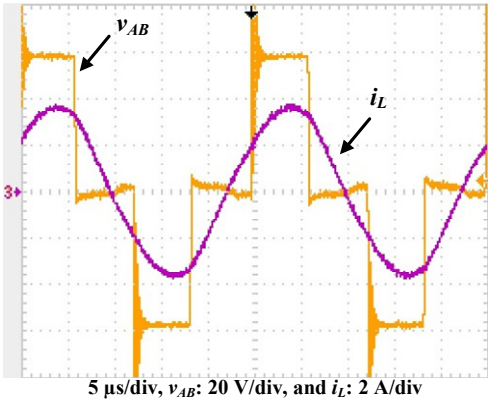
$$\begin{aligned} I_{L_{peak(FL)}} &= \frac{4}{\pi}\sqrt{1+\left(\frac{\pi^2}{8}\frac{R_L\omega_{pu}}{Z_c}\right)^2}\, I_{o(FL)} = \frac{4}{\pi}\sqrt{1+\left(\frac{\pi^2}{8}\frac{14.4\times 1.327}{20.7}\right)^2}\times 1.67 = 3.22\text{A} \\ V_{Cs_{peak(FL)}} &= \frac{Z_c}{\omega_{pu}} I_{L_{peak(FL)}} = \frac{20.7}{1.327}\times 3.22 = 50.27\text{V} \\ V_{Cp_{peak(FL)}} &= V_o \times \frac{\pi}{2} = 24\times\frac{\pi}{2} = 37.7\text{V} \end{aligned} \tag{3.75}$$

- The bridge rectifier input current i_{Br} shown in Fig. 3.21(c) and (d) is a square waveform of the output filter inductor current i_{Lo}. It is in phase with the parallel capacitor voltage v_{Cp} which drives the rectifier.
- Inductor voltage v_{Lo} shown in Fig. 3.21(g) and (h) is equal to $|v_{Cp}|-v_o$. The minimum value of v_{Lo} equals –24V (output voltage v_o).
- Capacitor ripple current Δi_{Co}, shown in Fig. 3.21(g) and (h), can be verified using (3.64)

$$\Delta I_{Co} = \Delta I_{Lo} = 0.105\frac{V_o}{fL_o} = \frac{0.105\times 24}{40000\times 12.5\times 10^{-3}} = 5\text{mA} \tag{3.76}$$

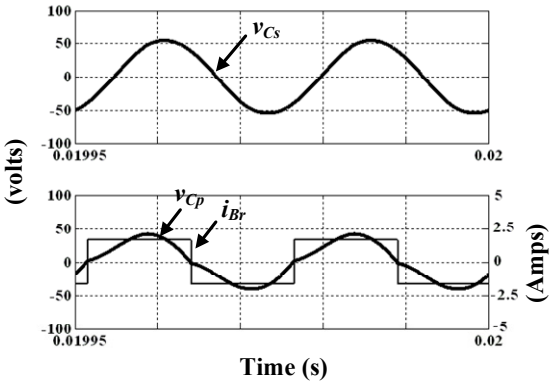


(a)



5 µs/div, v_{AB}: 20 V/div, and i_L: 2 A/div

(b)



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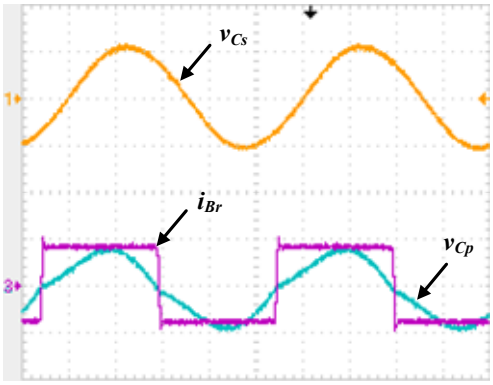
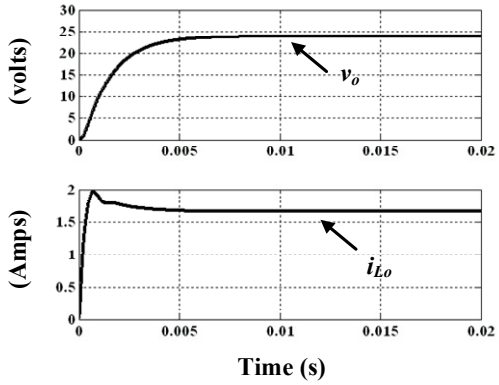
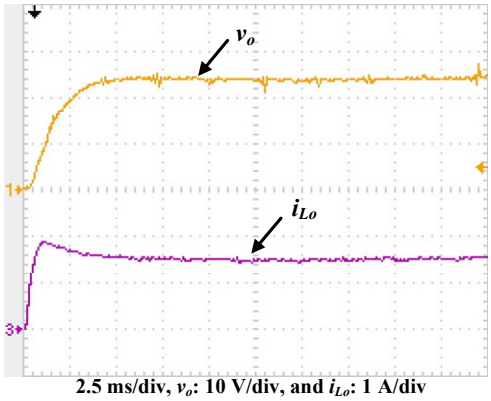


5 µs/div, v_{Cs}: 50 V/div, v_{Cp}: 50 V/div and i_{Br}: 2 A/div

(d)

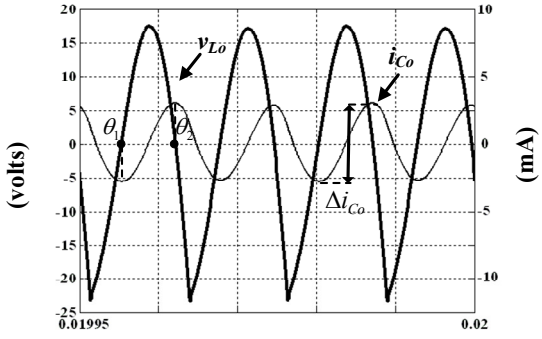


(e)

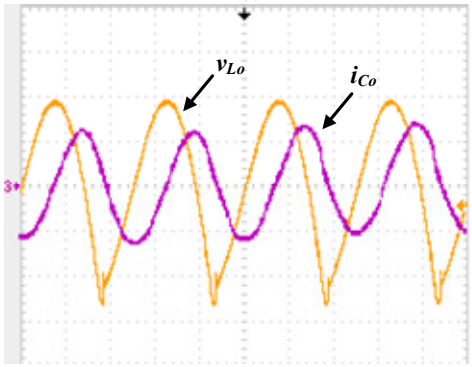


2.5 ms/div, v_o: 10 V/div, and i_{Lo}: 1 A/div

(f)



(g)



5 µs/div, v_{Lo}: 10 V/div, and i_{Co}: 2 mA/div

(h)

Fig. 3.21: Full-load operation results (a),(c),(e)&(g) Simulation, and (b),(d),(f)&(h) Experimental.

3.4.2 Half-load operation

Fig. 3.22 shows half-load operation results for the phase-controlled SPRC prototype. The following can be deduced from the results:

- At half-load conditions (δ_{HL}=48°, R_{LHL}=2R_{LFL}, Q_{HL}=0.5×Q_{FL}=0.72 and ω_{pu}=1.327), the converter operates in mode 4. This is seen in Fig. 3.22 (a) and (b), which shows i_L leading the fundamental inverter output voltage v_{AB1} (capacitive resonant tank impedance) while lagging the negative-going edge of v_{AB}. Operation in this mode is also verified by Fig. 3.6 illustrating the mode boundaries which, at the stated half-load operating conditions, shows that the converter operates in mode 4. With this mode, the inverter leading leg loses ZVS while it is retained by the inverter lagging leg. Fast recovery anti-parallel diodes are necessary for the leading leg switches.
- Fig. 3.22 (e) and (f) show that under half-load conditions, the output voltage V_o=24V and the average inductor current is $\bar{I}_{Lo}$=0.83A, which is equivalent to half the full-load output (load) current, while the output power is 20W.
- Similar to full-load operation, peak values for i_L, v_{Cs} and v_{Cp} at half-load are as calculated in (3.75).
- Capacitor ripple current Δi_{Co} is equal to the full-load case since the output voltage V_o of the converter is unchanged (V_o=24V).

Full- and half-load operation results have shown that the converter operates in modes 2 and 4 respectively. With the operating frequency being fixed for the phase control technique, it is the phase-shift angle δ and quality factor Q that both determine the operating mode as shown by the mode boundaries diagram in Fig. 3.6. Modes 1 and 3 operation are possible for the converter. At Q_{FL}=1.44, increasing the phase-shift angle δ beyond δ_{FL} allows mode 1 operation as shown in Fig. 3.23(a) and (b). Resonant tank current i_L lags the fundamental inverter voltage v_{AB1} and the positive-going edge of v_{AB} facilitates complete ZVS of all the inverter switches. By reducing converter loading (Q=0.36), the converter operates in mode 3, as shown in Fig. 3.23(c) and (d), where i_L leads both v_{AB1} and the negative-going edge of v_{AB}. ZVS is lost for all inverter switches.

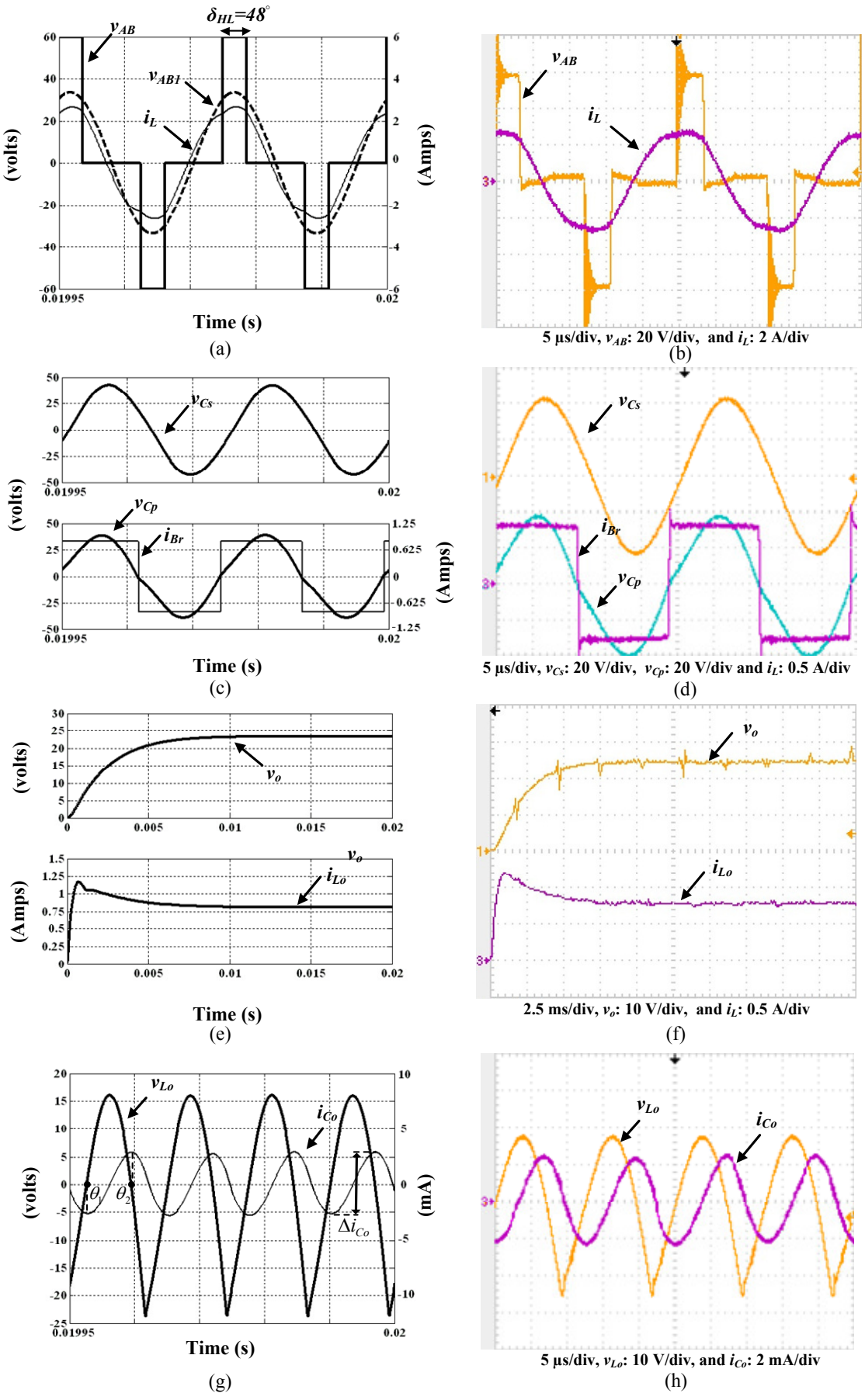


Fig. 3.22: Half-load operation results (a),(c),(e)&(g) Simulation, and (b),(d),(f)&(h) Experimental.

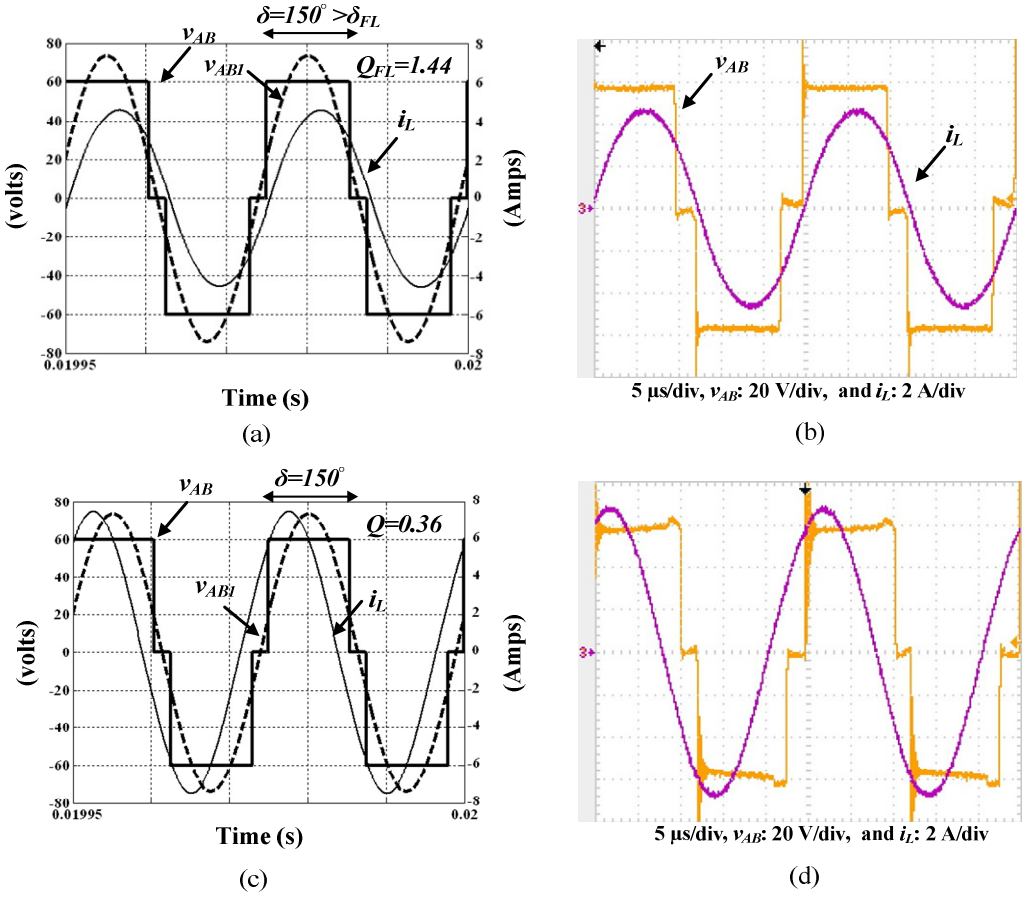


Fig. 3.23: Mode 1 and mode 3 operation results (a)&(c) Simulation, and (b)&(d) Experimental.

3.4.3 Operational efficiency

In order to assess converter operating efficiency as shown in Fig. 3.11, the prototype converter efficiency is measured and compared with the analytical (calculated) results obtained in section 3.2.5. Efficiency is obtained experimentally by measuring output power (from load voltage/current readings) and input power (from input supply readings). Fig. 3.24 shows the converter efficiency results obtained at the fixed operating normalised frequency ω_{pu}=1.327 while changing the loading (quality) factor Q. Experimental results verify that, at the selected operating frequency, maximum efficiency is obtainable at the full-load quality factor Q_{FL}=1.44. The experimental results are marginally lower than calculations which were based on a number of approximations that are potential causes of the resulting imprecision. Differences in results arise from:

- Difference between measured and actual circuit parameters. The latter may vary due to factors such as skin effect, temperature and magnetic core saturation;
- Interconnecting cable impedances are not taken into account with their associated extra copper losses;

- Waveforms in the analysis are assumed purely sinusoidal whereas in reality marginal distortion occurs due to square wave current from the bridge rectifier;
- Capacitor losses are not included in the analysis;
- Imperfect semiconductor drive waveforms are not included in the analysis;
- Imperfect semiconductor loss modelling; and
- The prototype operates at low power level where the operating voltages are low and currents are relatively high causing power losses to be comparable to input power level and hence reducing efficiency.

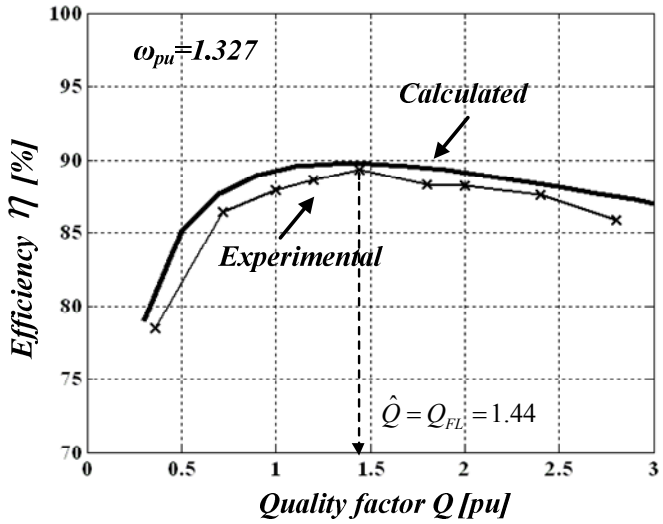


Fig. 3.24: Comparison between converter calculated and experimental efficiency results.

3.5 Summary

This chapter presented novel steady-state analysis to give insight into phase-controlled SPRC operation. Taking into account the three main converter control parameters (phase angle, frequency and load factor), detailed analysis was given of the converter voltage gain transfer function, converter operation modes together with analytical and illustrative derivations of mode boundaries and maximum power transfer criteria. In addition, converter voltage gain sensitivity to variation in operating frequency and load was studied. Detailed converter efficiency analysis was performed including all operational losses with analytical and graphical representations. A fully detailed design procedure was described for the selection of each converter circuit element in order to fulfil the requirements of the converter application in the subsea *All-Electric* project. The maximum efficiency point was used as the main criteria for selection of the full-load operating conditions. The design process included the selection of the resonant tank element values, nano-crystalline core transformer design and core selection, and

finally the output filter design depending on ripple current and voltage analysis in the case of single-module and multi-module converter operation with interleaving. Interleaving gives the advantage of output capacitor size reduction while compromising system modularity. This is because modules are not identically controlled (phase-displaced) and proper control coordination is needed to isolate faulty module and insert healthy module with the correct phase displacement. Finally, simulation and experimental results have verified converter operation and the design criteria derived.

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Chapter 4

Novel Large-Signal Converter Modelling using State Feedback Linearization

This chapter proposes a novel linearized large-signal state space model for the phase-controlled series-parallel resonant converter (SPRC). The proposed model implements state feedback linearization by using measurement of the output filter inductor current. The model combines multiple frequency and average state space modelling techniques to generate an aggregate model with dc state variables that are relatively easy to control and slower than the fast resonant tank dynamics. The main objective of the linearized model is to provide a linear representation of the converter behaviour under large-signal variation which is suitable for faster simulation and large-signal estimation/calculation of the converter state variables. The model also provides insight into converter dynamics as well as a simplified reduced order transfer function for PI closed-loop controller design. Experimental and simulation results from the switched converter are compared with the proposed state space model output to verify its accuracy and robustness. Finally, a novel sensorless multi-loop control scheme is proposed to enhance closed-loop stability and dynamics with a reduced number of measurement sensors. The scheme uses a Kalman filter-based estimator to estimate the inner loop control variable.

4.1 Background

Modelling of resonant converters is more complex than for PWM converters. In resonant converters, energy is transferred from input to output at the fundamental frequency whereas in conventional hard-switched converters, energy is transferred at dc. Therefore, in PWM converters, a small ripple assumption is valid meaning that state space averaging is suitable for modelling. In resonant converters, however, the switching frequency is comparable to the oscillatory frequency of the passive circuit, meaning that the small ripple assumption is invalid. Moreover, the non-linear coupling between resonant converter ac and dc state variables makes conventional state space averaging techniques inadequate for modelling.

Various transient models have been proposed in the literature for the SPRC. These are generally classified into small-signal or large-signal models. Small-signal models use

linearized large-signal state space models around an equilibrium point to enable stability analysis and closed-loop design [4.1]. The resulting closed-loop design, although eliminating error in the output voltage, results in satisfactory dynamic response only in a close neighbourhood to the steady-state operating point [4.2]. Beyond these limits, response is usually unsatisfactory. SPRC small-signal models include discrete time domain [4.3-5] and multiple frequency techniques [4.6-8]. A method based on discrete time domain modelling has been proposed for low order converters. The method becomes cumbersome with higher order converters. The multiple frequencies method transforms ac signals into dc signals at multiple frequencies, thereby providing a theoretically high accuracy model [4.9].

Although a small-signal model is sufficient for analysis and closed-loop design, it cannot be used to estimate converter state variables under large-signal variations, which are possible if the converter is operating with a wide range input voltage or variable load. With such variations, a large-signal converter model is needed. Such a model is useful for faster converter simulation, as well as large-signal estimation/calculation of converter ac and dc state variables, and hence can be used for converter sensorless control. However, since both resonant tank ac state variables and output filter dc state variables exist, combining their associated dynamic equations into one aggregate model is not possible in a linear manner, since the model includes non-linear mathematical relationships. The resulting large-signal model is non-linear. Several large-signal models based on a describing function method have been proposed for SPRC analysis [4.10, 11]. However, due to model non-linearity, non-linear controllers such as the sliding mode technique [4.12, 13] and robust optimal control [4.14] were designed for SPRC control.

With the necessity and utilization of a large-signal model clarified, the objective of this chapter is to linearize this model so that all converter state variables (ac and dc) are combined into one state space model. This model can then be used for faster simulation compared to the converter detailed switching model, and for state variable estimation/ calculation. In order to achieve this linearization objective, a state feedback scheme utilizing measurement of the dc output filter inductor current is implemented to overcome the non-linearity in the large-signal model. The model is first derived and is followed by in-depth analysis of the linearized system model. Accuracy, robustness, and validity of the proposed model are assessed by comparing experimental and simulation results from the switched phase-controlled SPRC. In the final section of this chapter, converter

multi-loop control is presented to enhance closed-loop stability and dynamic performance. Comparison is made between the most suitable states for feedback, according to a stability study. The state variable selected for the inner control loop is not directly measured but calculated using a Kalman filter-based estimator. This eliminates the sensor required to measure the inner loop control variable, hence sensorless multi-loop operation is achieved with no additional sensors, compared to conventional single-loop control.

4.2 Non-linear nature of dc/dc resonant converters

Fig. 4.1(a) shows the circuit diagram for a typical SPRC. The bridge rectifier, together with the output LC filter, act as a non-linear load to the resonant tank circuit. This non-linearity is clarified in Fig. 4.1(b). In addition, the model has a combination of ac and dc state variables which shows that converter large-signal behaviour cannot be modelled using such linear approaches as conventional average state space modelling.

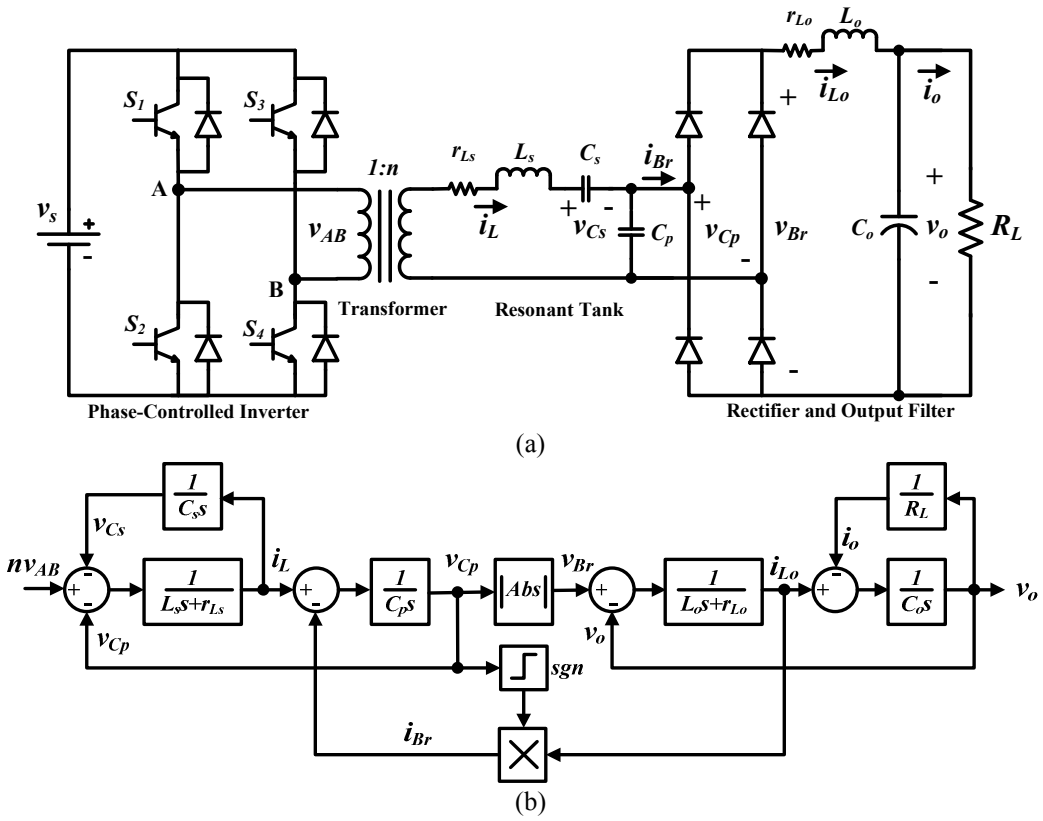


Fig. 4.1: (a) Circuit diagram for the SPRC and (b) non-linear model representation of the SPRC.

4.3 Proposed model for the dc/dc resonant converter

DC/DC resonant converters have two conversion stages; dc/ac (inversion) and ac/dc (rectification). Hence, two main sub-systems exist; the ac sub-system (resonant tank and transformer) and the dc sub-system (output filter), as illustrated in Fig. 4.2. Each sub-system has its own state variables, therefore both ac and dc state variables exist. In order to combine both types of signals into one model, it is essential to transform the ac state variables into equivalent dc quantities. This is achieved with the multiple frequency modelling (MFM) technique which converts ac state variables into *d-q* quantities (dc values with slow dynamics) using an arbitrary synchronous reference frame [4.9]. The resulting dc state variables from the resonant tank are combined with the naturally dc state variables of the output filter side (modelled with conventional average state space modelling) using a linearization scheme to overcome the non-linearity of the rectifier. The result is an aggregate large-signal linear model for the complete converter.

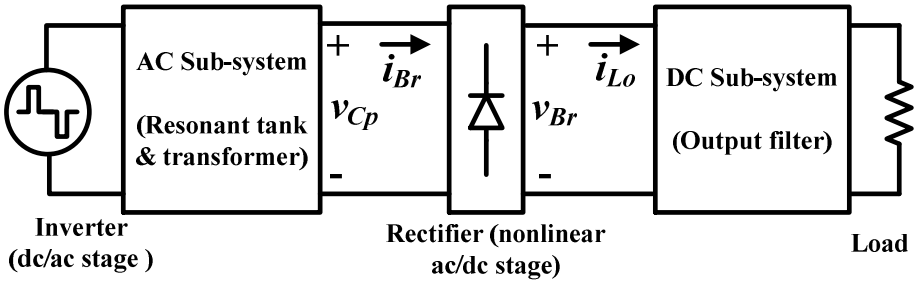


Fig. 4.2: Conversion stages and sub-systems in a typical resonant converter.

4.3.1 AC sub-system modelling

Fig. 4.3 shows the equivalent circuit diagrams for the ac sub-system of the SPRC. Three state variables exist: i_L, v_{Cs}, v_{Cp}. The voltage-current relations are described by

$$v_{AB}` = r_T i_L + L_T \frac{di_L}{dt} + v_{Cs} + v_{Cp} \tag{4.1}$$

$$i_L = C_s \frac{dv_{Cs}}{dt} \tag{4.2}$$

$$i_L - i_{Br} = C_p \frac{dv_{Cp}}{dt} \tag{4.3}$$

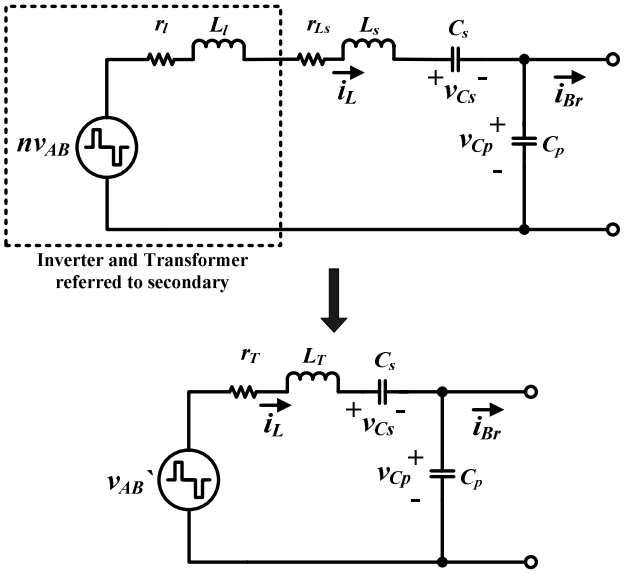


Fig. 4.3: Equivalent circuit diagrams for the ac sub-system.

The multiple frequency modelling approach [4.6, 7] for the SPRC, is utilized to model the resonant converter ac sub-system. Since the state variables have periodic characteristics, each state can be expressed by a Fourier series [4.8, 9]. Energy transfers from the input to the output mainly at the fundamental frequency, hence the dominant frequency for modelling and analysis of the ac sub-system state variables is assumed to be ω, the converter fundamental operating frequency. The state variables and input can be approximated as sinusoidal states with fundamental frequency ω as follows:

$$i_L = i_{Ld} \sin \omega t + i_{Lq} \cos \omega t \tag{4.4}$$

$$v_{Cs} = v_{Csd} \sin \omega t + v_{Csq} \cos \omega t \tag{4.5}$$

$$v_{Cp} = v_{Cpd} \sin \omega t + v_{Cpq} \cos \omega t \tag{4.6}$$

$$v_{AB}` = v_{ABd}` \sin \omega t + v_{ABq}` \cos \omega t \tag{4.7}$$

$$i_{Br} = i_{Brd} \sin \omega t + i_{Brq} \cos \omega t \tag{4.8}$$

where i_{Ld}, i_{Lq}, v_{Csd}, v_{Csq}, v_{Cpd} and v_{Cpq} are time-varying Fourier coefficients. The latter six Fourier coefficients, being time-dependent dc quantities, are considered as the new set of state variables. $v_{ABd}`$, $v_{ABq}`$, i_{Brd} and i_{Brq} are time-varying Fourier coefficients representing the new set of model inputs. Substituting (4.4)-(4.8) into (4.1)-(4.3) and equating sine and cosine coefficients, yields

$$v_{ABd}` = r_T i_{Ld} + L_T \frac{di_{Ld}}{dt} - L_T \omega i_{Lq} + v_{Csd} + v_{Cpd} \tag{4.9}$$

$$v_{ABq}` = r_T i_{Lq} + L_T \frac{di_{Lq}}{dt} + L_T \omega i_{Ld} + v_{Csq} + v_{Cpq} \tag{4.10}$$

$$i_{Ld} = C_s \frac{dv_{Csd}}{dt} - C_s \omega v_{Csq} \tag{4.11}$$

$$i_{Lq} = C_s \frac{dv_{Csq}}{dt} + C_s \omega v_{Csd} \tag{4.12}$$

$$i_{Ld} - i_{Brd} = C_p \frac{dv_{Cpd}}{dt} - C_p \omega v_{Cpq} \tag{4.13}$$

$$i_{Lq} - i_{Brq} = C_p \frac{dv_{Cpq}}{dt} + C_p \omega v_{Cpd} \tag{4.14}$$

Equations (4.9)-(4.14) in state space form

$$\dot{\vec{x}}_1(t) = A_1 \vec{x}_1(t) + B_1 \vec{u}(t) \tag{4.15}$$

where

$$\vec{x}_1(t) = [i_{Ld}\ i_{Lq}\ v_{Csd}\ v_{Csq}\ v_{Cpd}\ v_{Cpq}]^T \qquad \vec{u}_1(t) = [v_{ABd}`\ v_{ABq}`\ i_{Brd}\ i_{Brq}]^T$$

$$A_1 = \begin{bmatrix} -\frac{r_T}{L_T} & \omega & -\frac{1}{L_T} & 0 & -\frac{1}{L_T} & 0 \\ -\omega & -\frac{r_T}{L_T} & 0 & -\frac{1}{L_T} & 0 & -\frac{1}{L_T} \\ \frac{1}{C_s} & 0 & 0 & \omega & 0 & 0 \\ 0 & \frac{1}{C_s} & -\omega & 0 & 0 & 0 \\ \frac{1}{C_p} & 0 & 0 & 0 & 0 & \omega \\ 0 & \frac{1}{C_p} & 0 & 0 & -\omega & 0 \end{bmatrix} \qquad B_1 = \begin{bmatrix} \frac{1}{L_T} & 0 & 0 & 0 \\ 0 & \frac{1}{L_T} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C_p} & 0 \\ 0 & 0 & 0 & -\frac{1}{C_p} \end{bmatrix}$$

4.3.2 DC sub-system modelling

Fig. 4.4 shows the equivalent circuit diagram for the SPRC dc sub-system, where $\bar{v}_{Br}$ is the average of the rectifier output voltage v_{Br}. Energy is transferred at dc, so the dominant component for modelling and analysis is the dc (average) value. For

this reason, average state space modelling, with the small ripple assumption, is valid for modelling the dc sub-system.

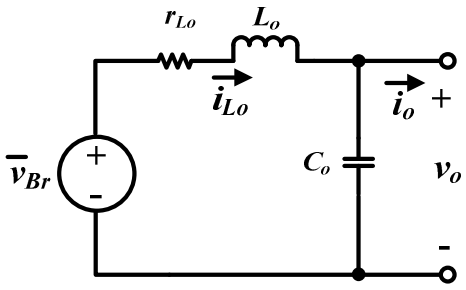


Fig. 4.4: Equivalent circuit diagram for the dc sub-system.

Two state variables exist, i_{Lo} and v_o, for which the voltage-current relationships are described by (4.16) and (4.17). The bar notation denoting the average value of the state variables will be neglected for standardization of the model.

$$\overline{v}_{Br} = r_{Lo} i_{Lo} + L_o \frac{di_{Lo}}{dt} + v_o \tag{4.16}$$

$$i_{Lo} - i_o = C_o \frac{dv_o}{dt} \tag{4.17}$$

Equations (4.16) and (4.17) can be represented in state space form

$$\dot{\vec{x}}_2(t) = A_2 \vec{x}_2(t) + B_2 \vec{u}(t) \tag{4.18}$$

where

$$\vec{x}_2(t) = [i_{Lo}\ v_o]^T \qquad \vec{u}_2(t) = [\overline{v}_{Br}\ i_o]^T \qquad A_2 = \begin{bmatrix} -\frac{r_{Lo}}{L_o} & -\frac{1}{L_o} \\ \frac{1}{C_o} & 0 \end{bmatrix} \qquad B_2 = \begin{bmatrix} \frac{1}{L_o} & 0 \\ 0 & -\frac{1}{C_o} \end{bmatrix}$$

4.3.3 Combined system non-linear model

Fig. 4.5 shows the non-linear model for the SPRC, combining the state space linear models of the ac and dc sub-systems. The voltage-current relationship between both sub-systems (separated by the bridge rectifier) is outlined by:

- The state variables of the ac sub-system are approximated as sinusoidal at the fundamental frequency, therefore

$$\overline{v}_{Br} = \frac{2}{\pi} v_{Br_{peak}} = \frac{2}{\pi} v_{Cp\,peak} = \frac{2}{\pi} \sqrt{v_{Cpd}^{\,2} + v_{Cpq}^{\,2}} \tag{4.19}$$

- Power balance theory: output power from the ac sub-system is equal to the input power to the dc sub-system (assuming lossless rectifier reverse recovery).

$$\frac{1}{2}\left(v_{Cpd} i_{Brd} + v_{Cpq} i_{Brq}\right) = \overline{v}_{Br} i_{Lo} \tag{4.20}$$

Substituting (4.19) into (4.20) yields

$$\frac{v_{Cpd}}{\sqrt{v_{Cpd}^{\,2} + v_{Cpq}^{\,2}}} i_{Brd} + \frac{v_{Cpq}}{\sqrt{v_{Cpd}^{\,2} + v_{Cpq}^{\,2}}} i_{Brq} = \frac{4}{\pi} i_{Lo} \tag{4.21}$$

As outlined by the analysis in [4.15], it can be also concluded that

$$i_{Br\,peak} = \frac{4}{\pi} i_{Lo} = \sqrt{i_{Brd}^{\,2} + i_{Brq}^{\,2}} \tag{4.22}$$

Equations (4.21) and (4.22) confirm the non-linear relationship between the ac and dc sub-systems of the series-parallel resonant converter. Hence the voltage-current relationship can be represented by

$$\begin{aligned} i_{Brd} &= f\left(i_{Lo}, v_{Cpd}, v_{Cpq}\right) \\ i_{Brq} &= f\left(i_{Lo}, v_{Cpd}, v_{Cpq}\right) \end{aligned} \tag{4.23}$$

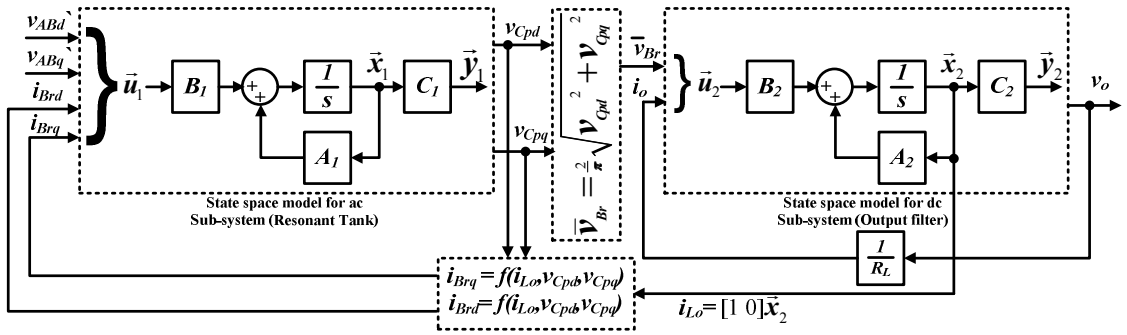


Fig. 4.5: Non-linear combined system model for the SPRC.

4.4 State feedback linearization

In this section, state feedback is used to linearize the relationship between the ac and dc sub-systems of the SPRC. The main objective of this linearization scheme is to formulate the necessary input voltages v_{ABd}` and $v_{ABq}$` to the resonant tank in Fig. 4.5 which force either ac sub-system output (v_{Cpd} or v_{Cpq}) to be zero. In this case, the mathematical square-root relationship representing the diode rectifier reduces to a simple gain and

both the ac and dc sub-systems are cascaded linear systems that can be combined into one aggregate linear model. In order to realize such linearization, feedback is needed of the output filter inductor current i_{Lo} as will be shown in the derivation. Steady-state ac analysis of the resonant tank is performed to calculate the required input voltages v_{ABd}` and $v_{ABq}$`.

4.4.1 Steady-state analysis of ac sub-system

Fig. 4.6 shows the steady-state phasor diagram for the ac sub-system (resonant tank), assuming sinusoidal state variables. The capital notation denotes steady-state values. Starting with v_{Cp} and i_{Br} and working backwards (as from Fig. 4.3), the inverter voltage v_{AB}` (referred to secondary) can be expressed as

$$\begin{aligned}
V_{ABd}` &= V_{Cp}\cos\theta_{V_{Cp}} + (V_L - V_{Cs})\cos(90+\theta_{I_L}) + V_{r_T}\cos\theta_{I_L} \\
&= V_{Cpd} + \left(\frac{1}{\omega C_s} - \omega L_T\right) I_L \sin\theta_{I_L} + r_T I_L \cos\theta_{I_L} \\
&= V_{Cpd} + \left(\frac{1}{\omega C_s} - \omega L_T\right)\left(I_{Brq} + I_{Cp}\cos\theta_{V_{Cp}}\right) + r_T\left(I_{Brd} + I_{Cp}\cos(90+\theta_{V_{Cp}})\right) \\
&= V_{Cpd} + \left(\frac{1}{\omega C_s} - \omega L_T\right)\left(I_{Brq} + V_{Cp}\omega C_p.\frac{V_{Cpd}}{V_{Cp}}\right) + r_T\left(I_{Brd} - V_{Cp}\omega C_p.\frac{V_{Cpq}}{V_{Cp}}\right) \\
&= V_{Cpd}\left(1 + \frac{C_p}{C_s} - \omega^2 L_T C_p\right) + V_{Cpq}\left(-r_T\omega C_p\right) + I_{Brd}\left(r_T\right) + I_{Brq}\left(\frac{1}{\omega C_s} - \omega L_T\right) \\
&= k_1 V_{Cpd} + k_2 V_{Cpq} + k_3 I_{Brd} + k_4 I_{Brq}
\end{aligned} \tag{4.24}$$

$$\begin{aligned}
V_{ABq}` &= V_{Cp}\sin\theta_{V_{Cp}} + (V_L - V_{Cs})\sin(90+\theta_{I_L}) + V_{r_T}\sin\theta_{I_L} \\
&= V_{Cpq} - \left(\frac{1}{\omega C_s} - \omega L_T\right) I_L \cos\theta_{I_L} + r_T I_L \sin\theta_{I_L} \\
&= V_{Cpq} - \left(\frac{1}{\omega C_s} - \omega L_T\right)\left(I_{Brd} + I_{Cp}\sin\theta_{V_{Cp}}\right) + r_T\left(I_{Brq} + I_{Cp}\sin(90+\theta_{V_{Cp}})\right) \\
&= V_{Cpd} - \left(\frac{1}{\omega C_s} - \omega L_T\right)\left(I_{Brd} - V_{Cp}\omega C_p.\frac{V_{Cpq}}{V_{Cp}}\right) + r_T\left(I_{Brq} + V_{Cp}\omega C_p.\frac{V_{Cpd}}{V_{Cp}}\right) \\
&= V_{Cpd}\left(r_T\omega C_p\right) + V_{Cpq}\left(1 + \frac{C_p}{C_s} - \omega^2 L_T C_p\right) + I_{Brd}\left(\omega L_T - \frac{1}{\omega C_s}\right) + I_{Brq}\left(r_T\right) \\
&= k_5 V_{Cpd} + k_6 V_{Cpq} + k_7 I_{Brd} + k_8 I_{Brq}
\end{aligned} \tag{4.25}$$

where

$$k_1 = k_6 = \left(1 + \frac{C_p}{C_s} - \omega^2 C_p L_T\right) \qquad k_2 = -k_5 = -r_T\omega C_p \qquad k_3 = k_8 = r_T \qquad k_4 = -k_7 = \left(\frac{1}{\omega C_s} - \omega L_T\right)$$

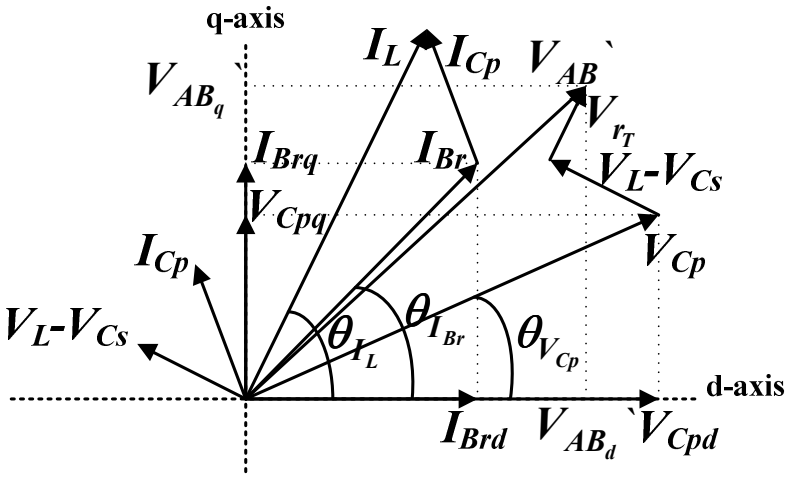


Fig. 4.6: Steady-state phasor diagram of the ac sub-system.

Expressions for the steady-state parallel capacitor voltage (V_{Cp}) can be obtained by solving (4.24) and (4.25) simultaneously, and re-arranging

$$V_{Cpd} = \frac{k_6}{k_1k_6 - k_2k_5} V_{ABd}` - \frac{k_2}{k_1k_6 - k_2k_5} V_{ABq}` + \frac{k_2k_7 - k_3k_6}{k_1k_6 - k_2k_5} I_{Brd} + \frac{k_2k_8 - k_4k_6}{k_1k_6 - k_2k_5} I_{Brq} \quad (4.26)$$

$$V_{Cpq} = -\frac{k_5}{k_1k_6 - k_2k_5} V_{ABd}` + \frac{k_1}{k_1k_6 - k_2k_5} V_{ABq}` + \frac{k_3k_5 - k_1k_7}{k_1k_6 - k_2k_5} I_{Brd} + \frac{k_4k_5 - k_1k_8}{k_1k_6 - k_2k_5} I_{Brq} \quad (4.27)$$

Therefore, steady-state values for the ac sub-system outputs (V_{Cpd} and V_{Cpq}) are obtained as a function of the inputs (V_{ABd}`, $V_{ABq}$`, I_{Brd} and I_{Brq}). This could be alternatively analyzed using state space equation (4.15) at steady-state

$$0 = A_1\vec{X}_1 + B_1\vec{U} \quad (4.28)$$

$$\vec{X}_1 = \begin{bmatrix} I_{Ld} & I_{Lq} & V_{Csd} & V_{Csq} & V_{Cpd} & V_{Cpq} \end{bmatrix}^T = -A_1^{-1}B_1 \begin{bmatrix} V_{ABd}` & V_{ABq}` & I_{Brd} & I_{Brq} \end{bmatrix}^T \quad (4.29)$$

4.4.2 State feedback scheme

As explained, the main objective of the linearization scheme is to calculate the necessary input voltages to the resonant tank v_{ABd}` and $v_{ABq}$` to force either outputs (v_{Cpd} or v_{Cpq}) to zero, in order to circumvent the square-root non-linearity. Which output is chosen to be zero is inconsequential to the modelling process as the objective is to control the converter output voltage. It is selected that v_{Cpq}=0. According to [4.15], the equivalent ac resistance at the rectifier input is given by

$$R_{ac} = \frac{V_{Cp}}{I_{Br}} = \frac{\pi^2}{8} R_L \quad (4.30)$$

This means that if v_{Cpq}=0, then i_{Brq}=0, due to the resistive relationship. According to (4.19)-(4.22), then $\overline{v}_{Br} = \frac{2}{\pi} v_{Cpd}$ and $i_{Brd} = \frac{4}{\pi} i_{Lo}$. Substituting V_{Cpq}=0 and I_{Brq}=0 into (4.26)-(4.27), and solving for V_{ABd}` and $V_{ABq}$` yields

$$V_{ABd}` = k_1 V_{Cpd} + k_3 I_{Brd} \tag{4.31}$$

$$V_{ABq}` = k_5 V_{Cpd} + k_7 I_{Brd} \tag{4.32}$$

Equations (4.31) and (4.32) show that the resonant circuit input voltage V_{AB}` is a function of $I_{Brd}$ (proportional to the load current) and $V_{Cpd}$ (proportional to the output voltage). $V_{AB}$` has to follow the relationship outlined by (4.31) and (4.32) in order to satisfy the main criteria for linearizing the converter model (I_{Brq}=0 and V_{Cpq}=0) and to ensure stable converter operation. The ac sub-system (resonant tank) is fed with

$$v_{ABd}` = k_1 v_c + k_3 i_{Brd} \tag{4.33}$$

$$v_{ABq}` = k_5 v_c + k_7 i_{Brd} \tag{4.34}$$

where v_c is a common control input for converter output voltage control. This scheme, therefore, uses a weighted state feedback approach with a measurement of the inductor current i_{Lo} to realize (4.33)-(4.34), necessary to linearize the resonant converter model. The scheme realization is illustrated in Fig. 4.7.

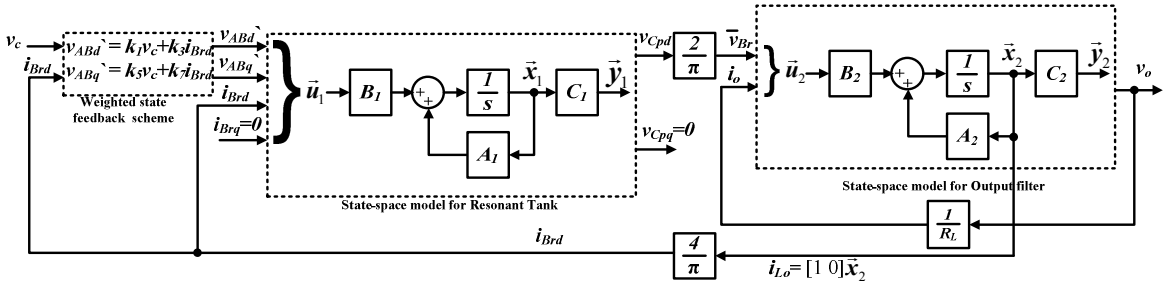


Fig. 4.7: Linearized model for the SPRC using weighted state feedback.

4.4.3 Aggregate linear model

An aggregate model for the resonant converter can be obtained by combining the two linear state space models (4.15) and (4.18) for the ac and dc sub-systems respectively. Taking (4.35) into account, yields the aggregate model (4.36):

$$\begin{aligned} \overline{v}_{Br} &= \frac{2}{\pi} v_{Cpd},\ i_{Brd} = \frac{4}{\pi} i_{Lo},\ i_{Brq} = 0 \\ v_{ABd}` &= k_1 v_c + \frac{4}{\pi} k_3 i_{Lo} \\ v_{ABq}` &= k_5 v_c + \frac{4}{\pi} k_7 i_{Lo} \end{aligned} \tag{4.35}$$

$$\begin{aligned} \dot{\vec{x}}(t) &= A\vec{x}(t) + B\vec{u}(t) \\ y(t) &= C\vec{x}(t) \end{aligned} \tag{4.36}$$

where

$$\vec{x}(t) = [i_{Ld}\ i_{Lq}\ v_{Csd}\ v_{Csq}\ v_{Cpd}\ v_{Cpq}\ i_{Lo}\ v_o]^T \qquad \vec{u}(t) = [v_c\ i_o]^T \qquad y(t) = v_o$$

$$A = \begin{bmatrix} -\frac{r_T}{L_T} & \omega & -\frac{1}{L_T} & 0 & -\frac{1}{L_T} & 0 & \frac{4k_3}{\pi L_T} & 0 \\ -\omega & -\frac{r_T}{L_T} & 0 & -\frac{1}{L_T} & 0 & -\frac{1}{L_T} & \frac{4k_7}{\pi L_T} & 0 \\ \frac{1}{C_s} & 0 & 0 & \omega & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_s} & -\omega & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C_p} & 0 & 0 & 0 & 0 & \omega & -\frac{4}{\pi C_p} & 0 \\ 0 & \frac{1}{C_p} & 0 & 0 & -\omega & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{2}{\pi L_o} & 0 & -\frac{r_{Lo}}{L_o} & -\frac{1}{L_o} \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{C_o} & 0 \end{bmatrix} \qquad B = \begin{bmatrix} \frac{k_1}{L_T} & 0 \\ \frac{k_5}{L_T} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & -\frac{1}{C_o} \end{bmatrix}$$

$$C = [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 1]$$

The aggregate linear model can also be represented using the transfer function technique

$$v_o(s) = \begin{bmatrix} G_1(s) & G_2(s) \end{bmatrix} \begin{bmatrix} v_c(s) \\ i_o(s) \end{bmatrix} \tag{4.37}$$

where

$G_1(s)$ is the control-to-output voltage transfer function, $G_1(s) = \left.\frac{v_o(s)}{v_c(s)}\right|_{i_o=0} = C(sI_{8\times 8} - A)^{-1} B_{i1}$

$G_2(s)$ is the output impedance, $G_2(s) = \left.\frac{v_o(s)}{i_o(s)}\right|_{v_c=0} = C(sI_{8\times8} - A)^{-1}B_{i2}$

B_{ik} denotes row i column k of matrix B.

4.5 Linearized converter model analysis

By considering the state space model (4.36), linearized system Eigen values can be obtained by studying the complex s-plane. System Eigen values are obtained by (4.38), summarized in Table 4.1, and plotted on the complex s-plane in Fig. 4.8.

$$\left|sI_{8\times8} - A\right| = 0 \tag{4.38}$$

Pole number	***Pole location in complex s-plane***	***Pole natural frequency ω_n***
$p_{1,2}$	$\pm j\omega$	ω
$p_{3,4}$	$s_{p3,4}$	$\omega_{n_{p3,4}}$
$p_{5,6}$	$s_{p5,6}$	$\omega_{n_{p5,6}}$
$p_{7,8}$	$-\frac{r_{Lo}}{2L_o} \pm j\sqrt{\frac{1}{L_oC_o} - \frac{r_{Lo}^{\ 2}}{4L_o^{\ 2}}}$	$\frac{1}{\sqrt{L_oC_o}}$

Table 4.1: Eigen values for the linearized resonant converter model

where

$$s_{p_{3,4}} = -\frac{r_T}{2L_T} \pm j\sqrt{\frac{-r_T^{\ 2}C_sC_p + 4L_TC_s + 4L_TC_p + 4L_T^{\ 2}C_sC_p\omega^2 + 4L_T\omega\sqrt{4L_TC_sC_p^{\ 2} + 4L_TC_pC_s^{\ 2} - r_T^{\ 2}C_s^{\ 2}C_p^{\ 2}}}{4L_T^{\ 2}C_sC_p}}$$

$$s_{p_{5,6}} = -\frac{r_T}{2L_T} \pm j\sqrt{\frac{-r_T^{\ 2}C_sC_p + 4L_TC_s + 4L_TC_p + 4L_T^{\ 2}C_sC_p\omega^2 - 4L_T\omega\sqrt{4L_TC_sC_p^{\ 2} + 4L_TC_pC_s^{\ 2} - r_T^{\ 2}C_s^{\ 2}C_p^{\ 2}}}{4L_T^{\ 2}C_sC_p}}$$

$$\omega_{n_{p3,4}} = \sqrt{\frac{C_s + C_p + 4L_TC_p + L_TC_sC_p\omega^2 + \omega\sqrt{4L_TC_sC_p^{\ 2} + 4L_TC_pC_s^{\ 2} - r_T^{\ 2}C_s^{\ 2}C_p^{\ 2}}}{L_TC_sC_p}}$$

$$\omega_{n_{p5,6}} = \sqrt{\frac{C_s + C_p + 4L_TC_p + L_TC_sC_p\omega^2 - \omega\sqrt{4L_TC_sC_p^{\ 2} + 4L_TC_pC_s^{\ 2} - r_T^{\ 2}C_s^{\ 2}C_p^{\ 2}}}{L_TC_sC_p}}$$

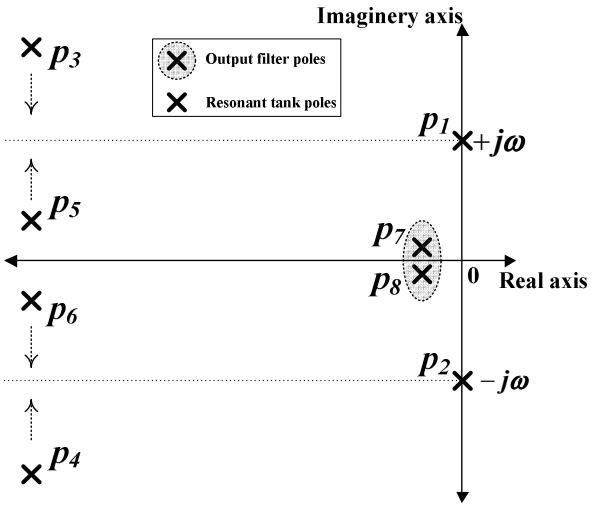


Fig. 4.8: Complex *s*-plane showing poles of the linearized resonant converter model.

4.5.1 Control-to-output voltage transfer function

By comparing the weighted state feedback scheme in (4.33)-(4.34) with (4.31)-(4.32), at steady-state v_{Cpd} is equal to the control input voltage v_c, that is, $V_{Cpd}= V_c$. Then by examining Fig. 4.7, the control-to-output voltage transfer function $G_1(s)$ is approximated by

$$G_1(s) = \frac{v_o(s)}{v_c(s)} \approx \frac{2}{\pi} \frac{v_o(s)}{\overline{v}_{Br}(s)} \tag{4.39}$$

This can be derived from state space equation (4.18) of the dc sub-system (output filter)

$$G_1(s) \approx \frac{2}{\pi} \frac{1}{L_o C_o s^2 + r_{Lo} C_o s + 1} \tag{4.40}$$

Such a simplified second order control-to-output voltage transfer function is not to replace the derived model (4.36) which provides detailed dynamics of the complete converter ac and dc state variables, but is useful for simplified closed-loop PI control as will be shown in section 4.5.2. The approximated transfer function (4.40) can be better understood by studying the exact transfer function $G_1(s)$ derived from (4.37)

$$G_1(s) = \frac{K \prod_{i=1}^{4} (s + z_i)}{\prod_{j=1}^{8} (s + p_j)} \tag{4.41}$$

where, K is a constant, p_1-p_8 are the poles of the control-to-output transfer function defined in Table 4.1 and z_1-z_4 are the zeros of the control-to-output transfer function and are defined by

$$z_{1,2} = \pm j\omega$$
$$z_{3,4} = -\frac{a_1}{2a_2} \pm j\sqrt{\frac{a_0}{a_2} - \frac{a_1^2}{4a_2^2}} \tag{4.42}$$

where

$$a_0 = \omega^4 L_T^2 C_s^2 C_p^2 + C_s^2 C_p^2 \omega^2 r_T^2 - 2\omega^2 C_s^2 C_p L_T - 2\omega^2 C_p^2 C_s L_T + C_s^2 + C_p^2 + 2C_s C_p$$
$$a_1 = C_s^2 C_p r_T + C_s C_p^2 r_T + \omega^2 C_s^2 C_p^2 r_T L_T$$
$$a_2 = C_s^2 C_p L_T + C_s C_p^2 L_T - \omega^2 C_s^2 C_p^2 L_T^2$$

The pole-zero map of the control-to-output transfer function is shown in Fig. 4.9. The effect of the marginally stable (un-damped) poles $p_{1,2}$ oscillating at ω is cancelled by the complex pair of zeros $z_{1,2}$ at the same location. The pole pair $p_{7,8}$ represents the output filter time constant which is much longer than that of the resonance circuit. Poles $p_{3,4}$ and $p_{5,6}$ of the resonant tank have large natural frequencies compared with the output filter. This can be verified from Table 4.1 ($\omega_{np7,8} >> \omega_{np3,4}$ and $\omega_{np7,8} >> \omega_{np5,6}$), since $L_o >> L_T$ and $C_o >> C_s$, C_p. For this reason, the dominant poles in the control-to-output voltage transfer function are $p_{7,8}$. Effects of $p_{3,4}$, $p_{5,6}$ and $z_{3,4}$ can be neglected due to their very fast dynamics. Equation (4.41) is reduced to the approximated version (4.40) where the output filter parameters only appear. In order to verify the validity of the approximated transfer function $G_1(s)$, Fig. 4.10 shows Bode plots and step response comparing the behaviour of the approximate and exact transfer functions.

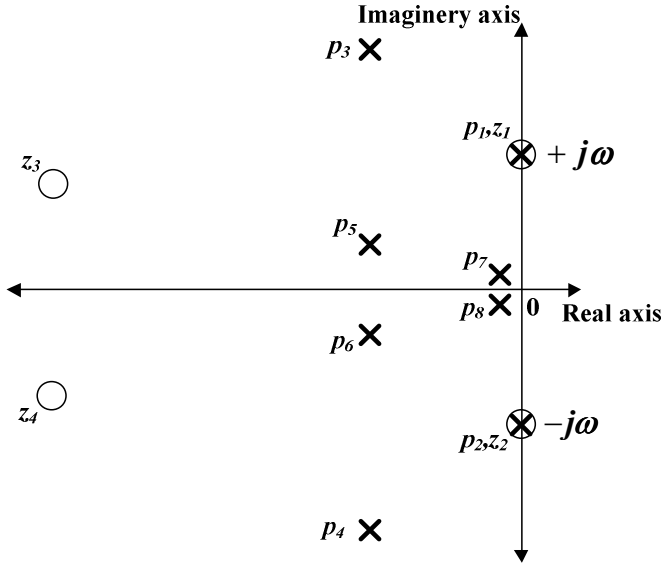
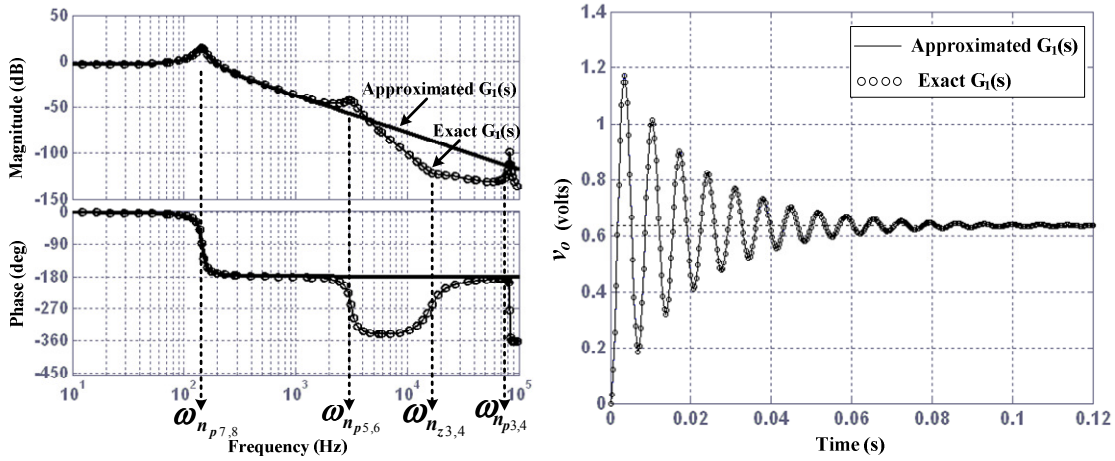


Fig. 4.9: Pole-zero map for actual control-to-output voltage transfer function $G_1(s)$ in complex s-plane.



(a) (b)

Fig. 4.10: Comparison between approximate and exact control-to-output voltage transfer function (a) Bode plot, and (b) step response.

Fig. 4.10(a) shows that the second order low pass filter response of the approximate transfer function mimics the exact control-to-output voltage transfer function. The higher frequency dynamics (caused by poles $p_{3,4}$ and $p_{5,6}$) are attenuated by the output filter. The step response in Fig. 4.10(b) further proves the analogy in behaviour of both the approximate and exact transfer functions. Such a reduced order transfer function is useful in simplifying the closed-loop design procedure. Pole-zero placement can be readily applied.

4.5.2 Closed-loop design

Since the dc/dc series-parallel resonant converter is used as a voltage source, the main objective is output voltage control. Hence, output voltage is used for feedback. All state variables are dc in the derived aggregate model, therefore PI control is applicable [4.16]. This means an infinite loop gain can be achieved by placing a pole at the origin, thereby eliminating steady-state error in the output voltage [4.17]. Fig. 4.11 shows the closed-loop structure to be used for PI control design. *C(s)* is PI control in a pole-zero form with k_i as the integral gain and k_p as the proportional gain.

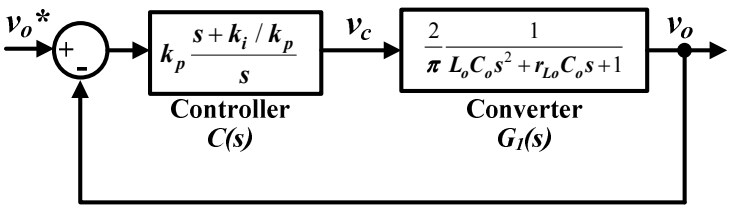
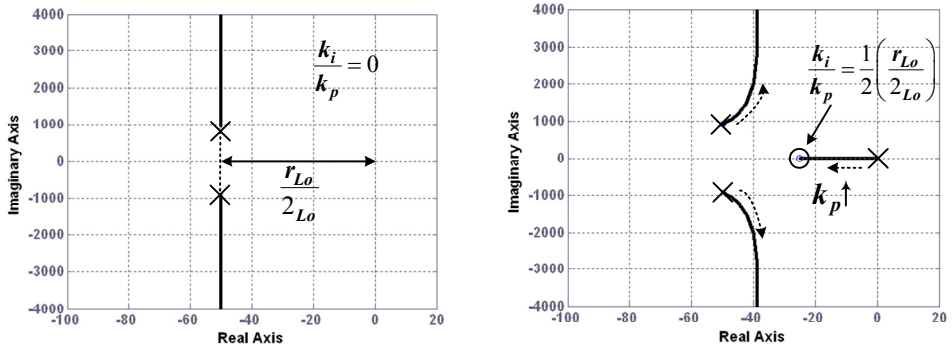


Fig. 4.11: Closed-loop structure for output voltage control.

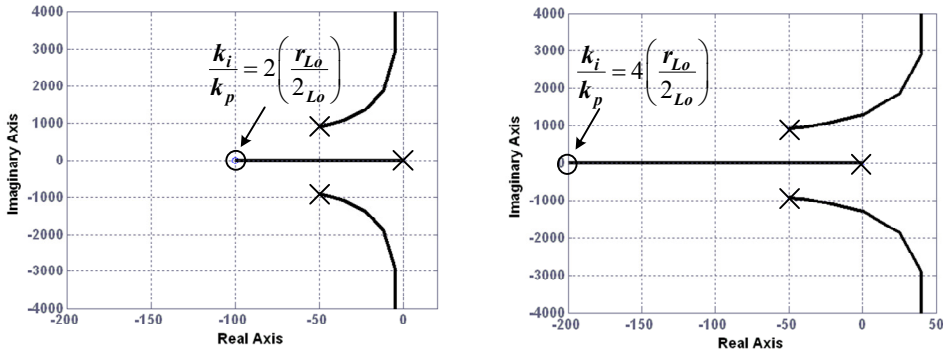
The closed-loop transfer function can be expressed as

$$\frac{V_O(s)}{V_O^*(s)} = \frac{\frac{2}{\pi}\left(k_p s + k_i\right)}{\left(L_O C_O\right)s^3 + \left(r_{LO} C_O\right)s^2 + \left(1 + \frac{2}{\pi}k_p\right)s + \frac{2}{\pi}k_i} \tag{4.43}$$

The location effect of the real left-hand plane zero k_i/k_p is studied in Fig. 4.12 to Fig. 4.14 to select its best location for the output response. The choice of k_p determines system overall stability. Fig. 4.12 shows root locus diagrams for different k_i/k_p. Since the zero of the PI controller is placed on the real-axis, it is moved in relation to the real part of the complex output filter pole-pair ($real(p_{7,8})=-r_{Lo}/2L_o$). The more k_i/k_p moves into the left hand plane, the more damped the closed-loop poles for a given k_p. For low values of k_i/k_p the closed-loop stability margin is higher, however, the system response is sluggish. Settling time cannot be reduced no matter how much k_p is increased. For this reason, high values of k_i/k_p are preferable for faster response though stability might be sacrificed due to a lower critical gain k_p for stability and lower phase margin. Fig. 4.13 shows the closed-loop step response. Results confirm the slower rise and settling times with mitigated oscillations for higher k_i/k_p. The step response is mainly over-damped since it is dominated by the low frequency real closed-loop pole. Its natural frequency is lower than that of the complex pole pair. This is clear from the under-damped step response in Fig. 4.13(a) where k_i/k_p=0. Fig. 4.14 shows the open-loop Bode plots with different controller zero locations. As described by the root locus analysis, stability margin (phase margin) is reduced as k_i/k_p is increased. Usually a phase margin of 45º to 60º is sufficient to ensure adequate closed-loop stability. High dc loop gain is ensured with the origin pole (integrator) which provides zero output voltage steady-state error; an essential characteristic for a voltage source.

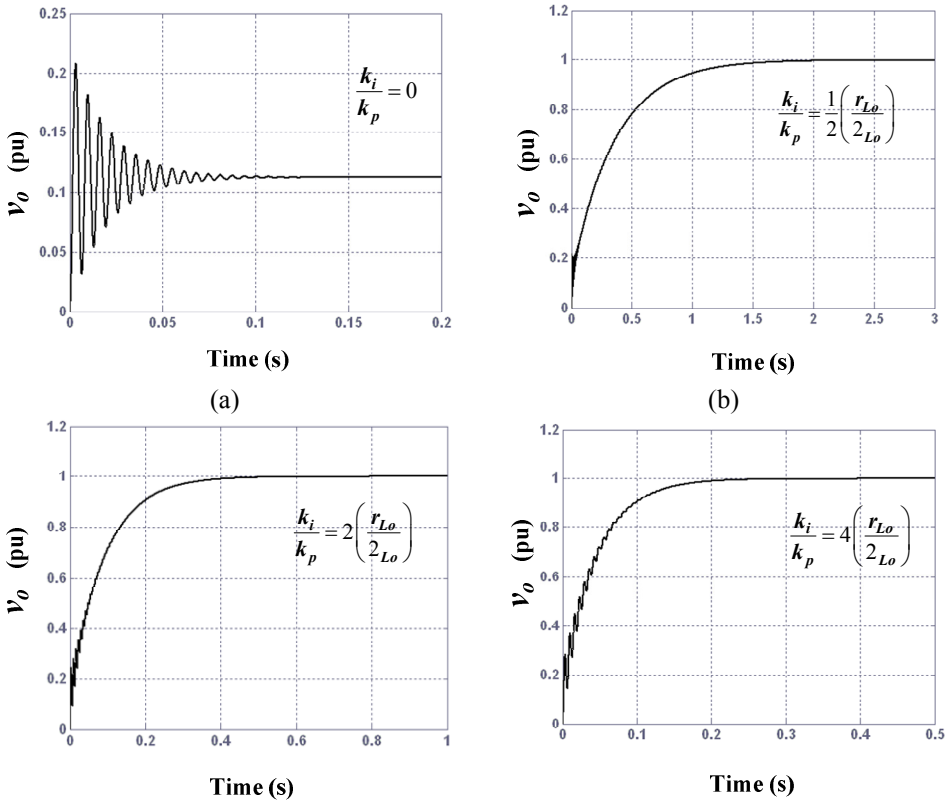


(a) (b)



(c) (d)

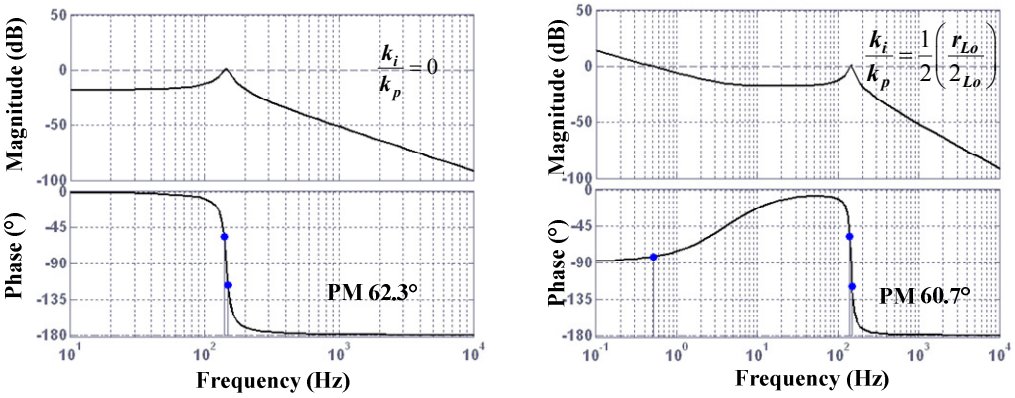
Fig. 4.12: Root loci for the open-loop transfer function $C(s)G_1(s)$



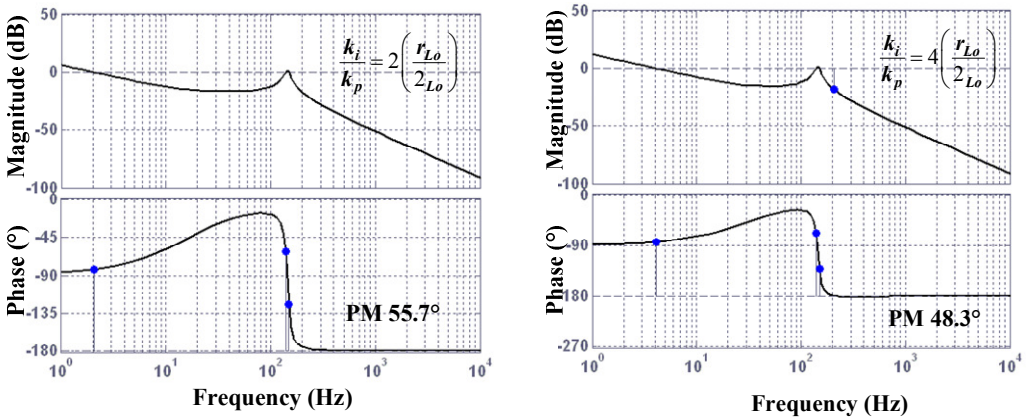
(a) (b)

(c) (d)

Fig. 4.13: Closed-loop step response for output voltage control loop



(a) (b)



(c) (d)

Fig. 4.14: Open-loop Bode plots

4.5.3 Output impedance

Similar to the previous analysis on the control-to-output voltage transfer function, the output impedance can be derived directly from the state space model of the dc sub-system in (4.18). This is due to $V_{Cpd}=V_c$ at steady-state. The output impedance transfer function $G_2(s)$ is

$$G_2(s)=\frac{v_o(s)}{i_o(s)}=-\frac{L_o s+r_{Lo}}{L_o C_o s^2+r_{Lo}C_o s+1} \tag{4.44}$$

The exact transfer function $G_2(s)$ can be derived from (4.37) and is expressed by

$$G_2(s)=-\frac{1}{C_o}\frac{\prod_{i=1}^{7}(s+z_i)}{\prod_{j=1}^{8}(s+p_j)} \tag{4.45}$$

where, p_1-p_8 are the poles defined in Table 4.1 and z_1-z_7 are the zeros of the output impedance and are defined by: $z_{1,2}= p_{1,2}$, $z_{3,4}= p_{3,4}$, $z_{5,6}= p_{5,6}$ and $z_7=r_{Lo}/L_o$. Therefore, $G_2(s)$ reduces to

$$G_2(s)=-\frac{1}{C_o}\frac{(s+z_7)}{(s+p_7)(s+p_8)}=-\frac{1}{C_o}\frac{\left(s+\frac{r_{Lo}}{L_o}\right)}{s^2+\frac{r_{Lo}}{L_o}s+\frac{1}{L_oC_o}} \tag{4.46}$$

The closed-loop output impedance can be studied by examining Fig. 4.15 and is expressed as

$$\frac{V_o(s)}{I_o(s)}=\frac{G_2(s)}{1+C(s)G_1(s)}=-\frac{s(L_o s+r_{Lo})}{L_oC_o s^3+r_{Lo}C_o s^2+(1+\frac{2}{\pi}k_p)s+\frac{2}{\pi}k_i} \tag{4.47}$$

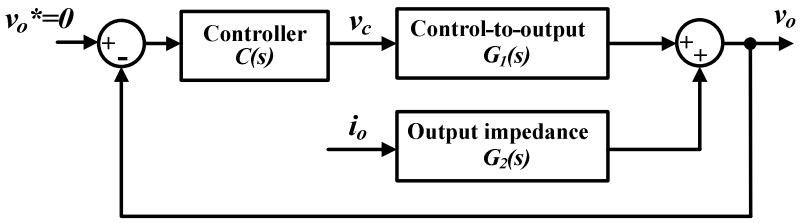
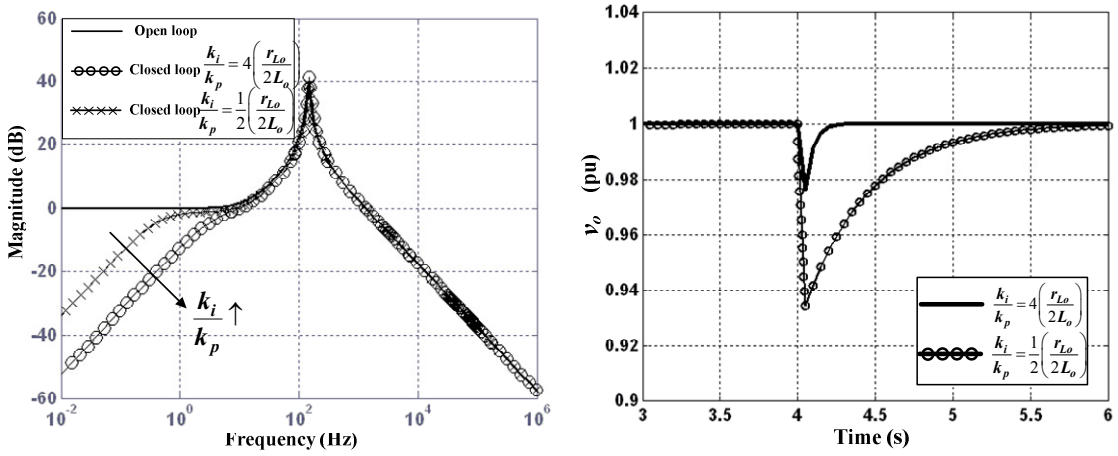


Fig. 4.15: Control structure to obtain the closed-loop output impedance

Fig. 4.16(a) shows Bode plots for the open- and closed-loop output impedances. Any high-frequency harmonic ripple in load current is attenuated by the converter output impedance. In dc/dc resonant converters, since the dominant frequency component of the load current is dc, open-loop output impedance will result in a constant voltage drop across r_{Lo}. This can be verified from the steady-state gain in (4.44). For the closed-loop case, attenuation of the dc load current is achieved by the controller integrator, appearing as an origin-zero in (4.47). Higher k_i/k_p leads to greater attenuation and the closed-loop system has better disturbance rejection and robustness against load variations. Fig. 4.16(b) shows the dynamic response of the closed-loop voltage control to a step load change for different k_i/k_p.



(a) (b)

Fig. 4.16: (a) Bode plots for open- and closed-loop converter output impedance, and (b) effect of changing k_i/k_p on closed-loop response to a step load change.

4.6 Simulation and experimental results

Fig. 4.17 illustrates the linearized SPRC closed-loop output voltage control, with the state feedback linearization scheme implemented.

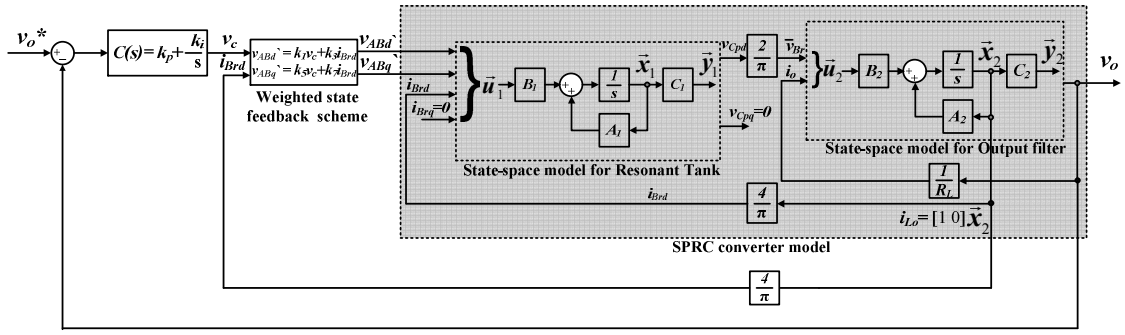
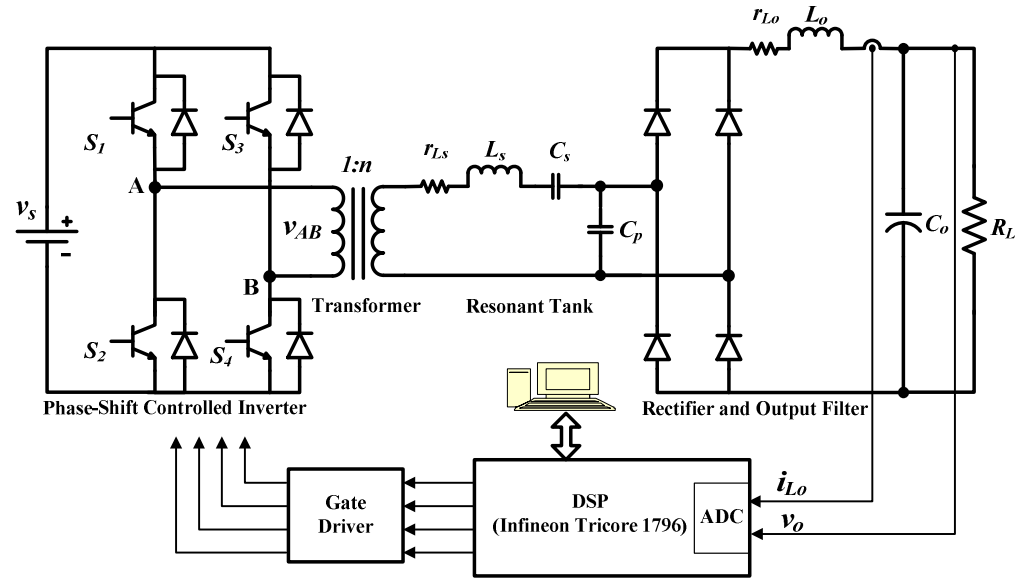


Fig. 4.17: Closed-loop SPRC output voltage control using the proposed linearization scheme.

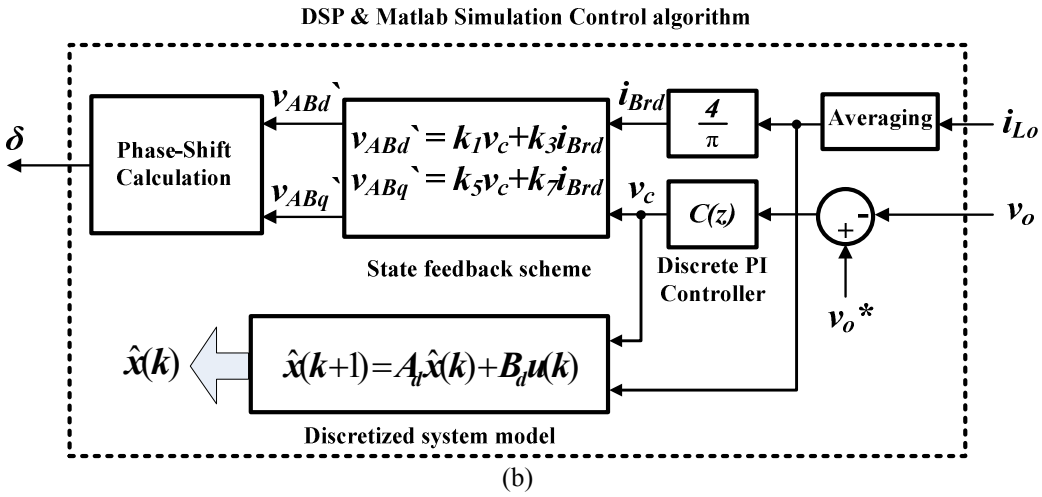
Closed-loop voltage control of the 40W, 40 kHz prototype phase-controlled SPRC is implemented experimentally and simulated in Matlab with a detailed switching model to verify the accuracy and robustness of the derived model in (4.37). Outputs from (4.37), which are the calculated/estimated state converter variables, are compared in Matlab with the detailed switching model of the converter and experimentally with actual converter measurements. Fig. 4.18 shows the control algorithm implementation both practically and in simulation and Table 4.2 summarizes the circuit and control parameter values.

Measurements of the actual SPRC output voltage v_o and output filter inductor current i_{Lo} are taken; the former to perform voltage control and the latter for state feedback linearization as shown in Fig. 4.18(a) and (b). Since i_{Lo} contains ripple due to the converter output filter, averaging is necessary since modelling of the dc sub-system (output filter) is based on an averaged state space technique. Since the linearization scheme uses v_{Cpq}=0 and i_{Brq}=0, the i_{Brd} necessary for the linearization scheme is obtained from $i_{Brd}=(4/\pi)i_{Lo}$. The PI controller output v_c and $i_{Brd}=(4/\pi)i_{Lo}$ are inputs to the linearization scheme which calculates the necessary outputs v_{ABd}` and $v_{ABq}$` that force v_{Cpq}=0. The scheme is weighted by constants k_1, k_3, k_5 and k_7 which are based on the converter circuit parameters as defined by (4.24)-(4.25).

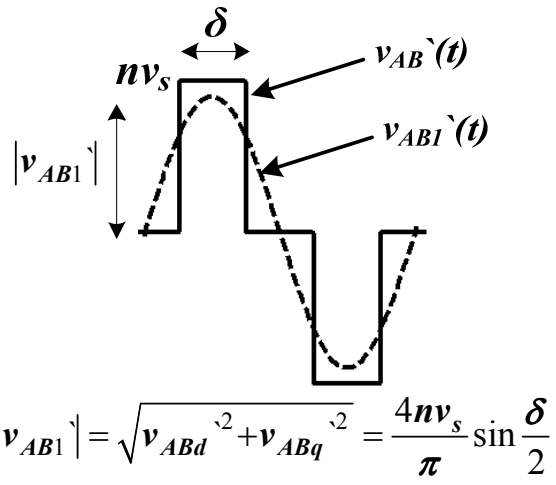
The phase shift angle δ between the inverter legs is then calculated by the algorithm in Fig. 4.18(c). With the state feedback outputs being v_{ABd}` and $v_{ABq}$` and knowing the supply voltage v_s and transformer turns ratio n, the phase shift angle can be calculated. All inverter switches are switched with a fixed 50% duty cycle; the only control variable being the phase shift angle between S_1 and S_3 as shown in Fig. 4.18(d). This controls the effective inverter output voltage duty cycle. The phase shift angle is updated every switching cycle (25 μs), viz., the inverter is switched at 40 kHz.



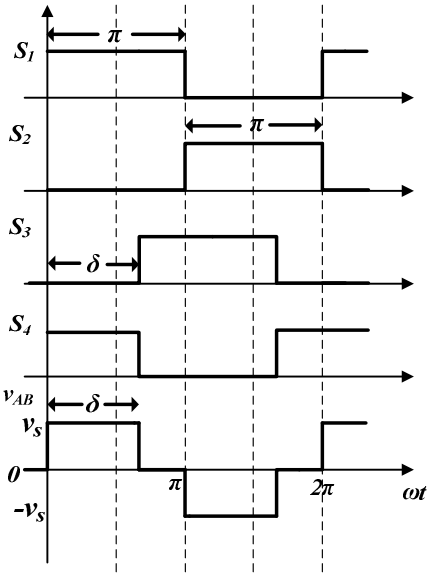
(a)



(b)



(c)



(d)

Fig. 4.18: Closed-loop control algorithm with state feedback, (a) circuit diagram, (b) control algorithm, (c) phase shift calculator, and (d) inverter phase control gating pattern.

Parameter	*Definition*	*Value*
Z_c	Resonant tank characteristic impedance	20.7 Ω
Q_{FL}	Full-load Q factor	1.44
R_{LFL}	Full-load resistive load	14.4 Ω
Q_{PL}	Part-load Q factor	0.511
R_{LPL}	Part-load resistive load	40.5 Ω
f	Inverter switching frequency	40 kHz
r_{Ls}	Parasitic resistance of resonant inductor	0.1916 Ω
L_s	Series resonant inductance	100.13 µH
r_l	Parasitic transformer resistance referred to secondary	0.6 Ω
L_l	Transformer leakage inductance (referred to secondary)	9.12 µH
r_T	Total parasitic resistance $r_T = r_{Ls} + r_l$	0.7916 Ω
L_T	Total equivalent resonant inductance (referred to secondary)	109.25 µH
C_s	Series resonant capacitance	255 nF
C_p	Parallel resonant capacitance	255 nF
r_{Lo}	Parasitic resistance of output filter inductor	0.5 Ω
L_o	Output filter inductance	12.5 mH
C_o	Output filter capacitance	120 µF
v_s	Input supply voltage	60 V
v_o^*	Reference output (load) voltage	24 V
P_{FL}	Converter full-load power rating	40 W
n	Transformer turns ratio	0.5
k_i/k_p	PI controller parameters $5\times(r_{Lo}/2L_o)$	100 Hz
k_p	Proportional gain	0.1
k_i	Integral gain	10

Table 4.2: Resonant Converter Parameters

In order to verify the linearized SPRC derived model, the state space equation defining the system in (4.36) is discretized to estimate the converter state variables experimentally and in the Matlab simulations. This allows the estimated results to be compared with measurements from the actual converter. The model is discretized with the main control algorithm interrupting at 25µs intervals, therefore, the sampling time used for discretization is T_s=25 µs. The discretized system is represented by

$$\hat{x}(k+1) = A_d\hat{x}(k) + B_d u(k) \tag{4.48}$$

where

$$A_d = e^{AT_s}$$

$$B_d = \int_0^{T_s} A(T_s - \tau)Bd\tau$$

$$\hat{x}(k) = [i_{Ld}\ i_{Lq}\ v_{Csd}\ v_{Csq}\ v_{Cpd}\ v_{Cpq}\ i_{Lo}\ v_o]^T$$

$$u(k) = [v_c\ i_o]^T$$

i_o is the output (load) current which can be approximated by the average inductor cur-

rent at steady-state. Fig. 4.19 shows the typical sampling diagram for the control algorithm implementation using an Infineon Tricore 1796 DSP with C-code execution times for the various control algorithm parts summarized in Table 4.3.

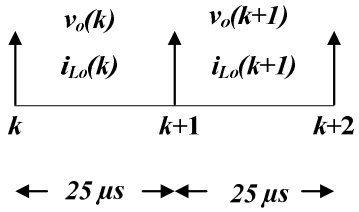


Fig. 4.19: Sampling diagram

Task	*Execution time (µs)*
Fast ADC measurement	1
PI control loop	3
State feedback scheme	4
Phase shift calculation	2
State variables calculation/estimation	13
Total	23

Table 4.3: DSP program execution time for the control algorithm

4.6.1 Model accuracy study

The response of the linearized large-signal model to large-signal variations is studied in order to assess its ability to track real converter behaviour. A step reference voltage from v_o^*=0 to v_o^*=24V is applied at t=0 and a step load change from Q_{PL}=0.511 to Q_{FL}=1.44 is applied at t=5.0s. Simulation and experimental results are shown in Fig. 4.20 and Fig. 4.21 respectively. The experimental results illustrate actual converter measurements compared with calculated state variables using the derived model. The derived model uses equivalent dc quantities for the ac state variables of the resonant tank (i_L, v_{Cs} and v_{Cp}). These quantities (i_{Ld}, i_{Lq}, v_{Csd}, v_{Csq}, v_{Cpd} and v_{Cpq}) do not physically exist, therefore, results compare the actual converter ac state variables measured with the corresponding peak value of the state variable calculated using the model. The peak values are calculated from the model using

$$\begin{aligned} i_L &= \sqrt{i_{Ld}^2 + i_{Lq}^2} \\ v_{Cs} &= \sqrt{v_{Csd}^2 + v_{Csq}^2} \\ v_{Cp} &= \sqrt{v_{Cpd}^2 + v_{Cpq}^2} \end{aligned} \tag{4.49}$$

For displaying on an oscilloscope, these estimated state variables are pulse width modulated and filtered to obtain their analogue peak values and are compared to the converter ac state variables measurements. Details of filter circuit used are given in Appendix A.

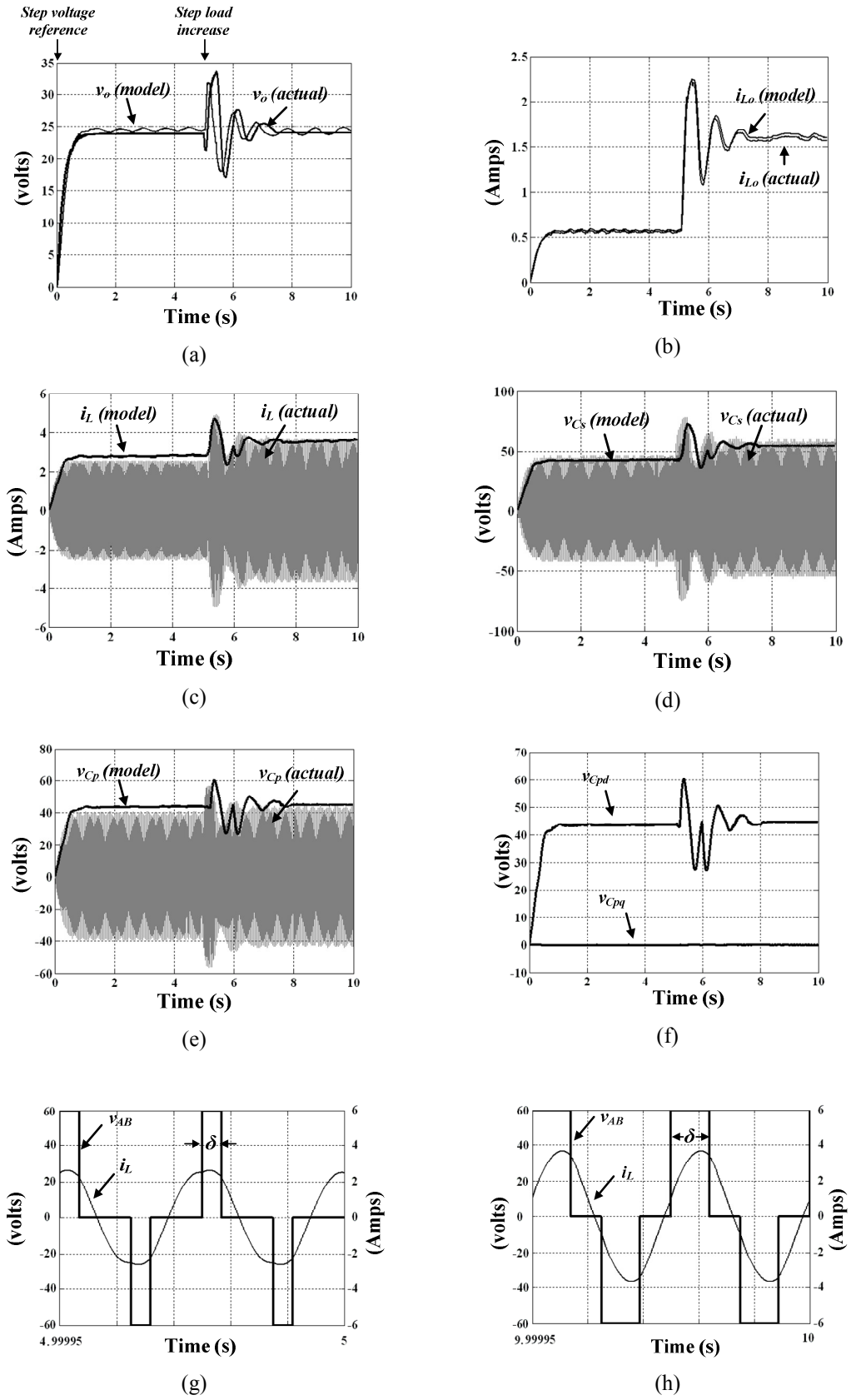
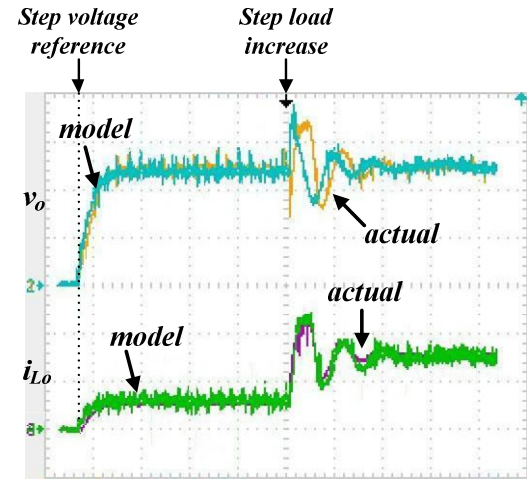
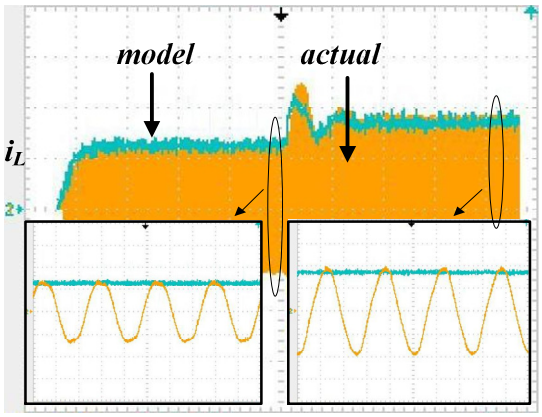


Fig. 4.20: Matlab simulations comparing actual switching and proposed large-signal model (full-load applied at t=5.0s), (a) output voltage, (b) output filter inductor current, (c) resonant inductor current, (d) series resonant capacitor voltage, (e) parallel resonant capacitor voltage, (f) dq equivalent resonant tank parallel capacitor voltages, (g) inverter output voltage at part-load, and (h) inverter output voltage at full-load.



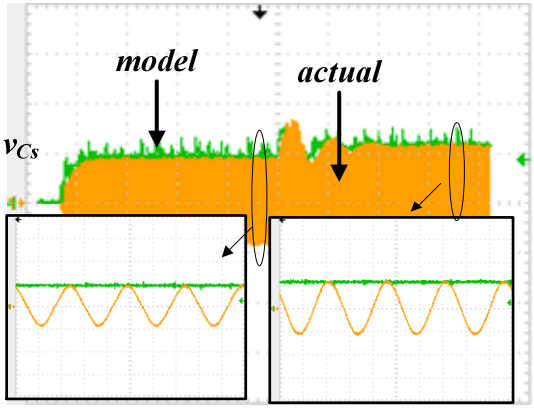
1 s/div, v_o: 10 V/div, and i_{Lo}: 1 A/div

(a)



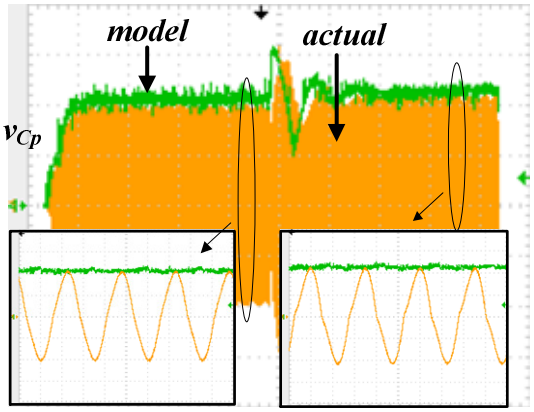
1 s/div, i_L: 2 A/div

(b)



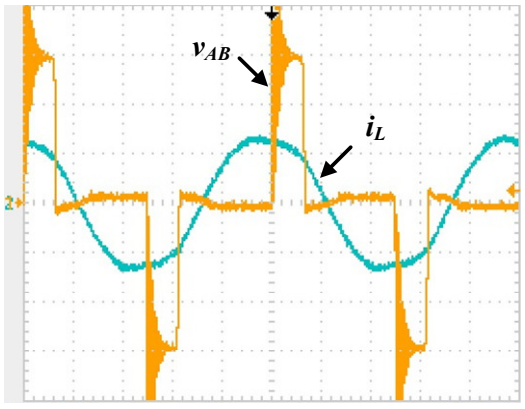
1 s/div, v_{Cs}: 50 V/div

(c)



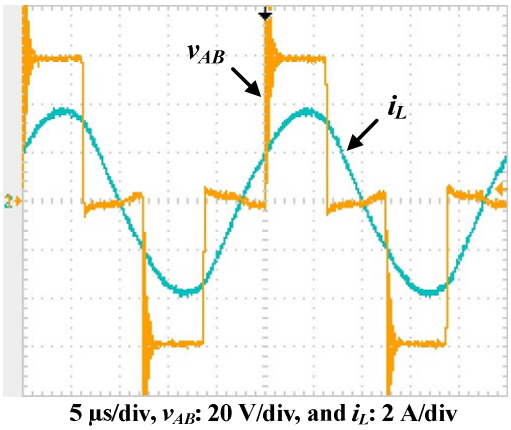
1 s/div, v_{Cp}: 20 V/div

(d)



5 µs/div, v_{AB}: 20 V/div, and i_L: 2 A/div

(e)



5 µs/div, v_{AB}: 20 V/div, and i_L: 2 A/div

(f)

Fig. 4.21: Experimental results comparing measurements from the actual converter and the proposed large-signal model, (a) output voltage and output filter inductor current, (b) resonant tank inductor current, (c) resonant tank series capacitor voltage, (d) resonant tank parallel capacitor voltage, (e) inverter output voltage at part-load (f) inverter output voltage at full-load.

With the application of two large-signal variations (step reference voltage at t=0 and step load at t=5.0s), the following can be deduced from Fig. 4.20 and Fig. 4.21:

- The negligible differences between actual converter measurements and calculated state variables from the derived model verify the accuracy of the measured circuit parameters which the model uses. Simulation and experimental results are similar with marginal differences due to the pure sinusoidal waveforms assumption in the model;

- Calculated state variables track peak voltages and currents of the measured state variables at steady-state. However, slight variations occur in the transient response at the application of the large-signal variations, especially in the voltage-based states v_o, v_{Cs} and v_{Cp} (Fig. 4.20(a), (d), (e) and Fig. 4.21(a), (c), (d) respectively). This is mainly due to the model neglecting the resonant tank and output filter capacitors' ESR in order to avoid further model complication. The inclusion of ESR in the model significantly increases number of terms while added precision in state variables is trivial. Transient response of the current-based states such as i_{Lo} and i_L (Fig. 4.20(b), (c) and Fig. 4.21(a), (b) respectively) mimic the actual converter measurements;

- Fig. 4.20(f) shows that the condition v_{Cpq}=0 outlined in (4.30)-(4.35) is maintained by the state feedback linearization scheme at all operating conditions, in addition to $v_{Cp(peak)} = v_{Cpd} \approx (\pi/2)v_o$. This verifies correct operation of the state feedback scheme;

- Fig. 4.20(g), (h) and Fig. 4.21(e), (f) show that after full-load application (Q_{FL}=1.44), the control loop increases the phase shift angle δ to produce more fundamental voltage output from the inverter. This is inevitable as the converter voltage gain is reduced, meaning more input voltage is required to maintain the required reference output voltage, v_o^*=24V;

- Natural increases occur in the values of i_{Lo} and i_L after increased loading at t=5.0s (see Fig. 4.20(b), (c) and Fig. 4.21(a), (b) respectively). This causes an increased voltage drop on v_{Cs}, whereas the increase in v_{Cp} is marginal. The latter can be explained by the fact that v_{Cp} controls v_o, so it is fairly constant with a slight increase to compensate for the increased voltage drop on the output filter inductor parasitic resistance after the application of full-load at t=5.0s; and

- The disturbance rejection capability of the PI controller can be improved to reduce the transient effect at the load transition instant. This can be achieved by increasing

the k_i/k_p ratio but lower k_p gain would need to be used to avoid closed-loop instability, which means a more sluggish response.

4.6.2 Model robustness study

Circuit parameters practically vary during operation. Resistive elements are affected by temperature while transformers and/or magnetic-core inductors are affected by core saturation. In order to assess the robustness of the derived model against such variations, a 10% increase in selected circuit parameters is applied to the actual switched converter model in simulation and compared with the unchanged parameter's large-signal model. Dominant circuit parameters that affect converter voltage gain are the resonant tank parasitic resistance r_T and equivalent inductance L_T which may be affected by changes in transformer leakage inductance. A 10% step increase in each parameter is applied to the converter operating at full-load to assess the model's response. The new parameter values applied are r_T= 0.87 Ω and L_T=120μH. Closed-loop results for each case are taken separately and illustrated in Fig. 4.22.

The effect of changing r_T is first studied. Fig. 4.22(a) and (b) show that the actual converter behaviour has negligible change at steady-state since the results for v_o and i_L are virtually unchanged after t=1.5s. The proposed model is capable of tracking the changed system parameter and estimates the state variables accurately. Fig. 4.22(c) confirms the minor effect on the converter due to changing r_T. This is shown by the analogy of the inverter output voltage v_{AB} and δ with the original case of converter operation with unchanged r_T (see Fig. 4.20(h)).

The effect of changing L_T is shown in Fig. 4.22(d)-(f). The increase in L_T causes an increase in the resonant tank characteristic impedance. This causes a sudden drop in the output voltage v_o, and the control loop functions immediately in an attempt to correct this voltage sag by increasing the inverter output voltage via an increase of δ as shown in Fig. 4.22(f), when compared with Fig. 4.20(h). The output voltage is restored to the reference value after approximately 1.5s due to the increased circuit time constant with increased L_T. However the large-signal model overestimates the output voltage by 5% due to the increased control input to the model. The resonant tank current i_L decreases slightly (as in Fig. 4.22(e)) and similarly the model overestimates i_L by 6%. It can be concluded that the model is relatively insensitive to changes in the resonant tank parasitic resistance r_T whereas changing L_T has more of an effect on the model's performance.

This is inevitable as the circuit resonant frequency changes and the entire dynamics of the converter are affected.

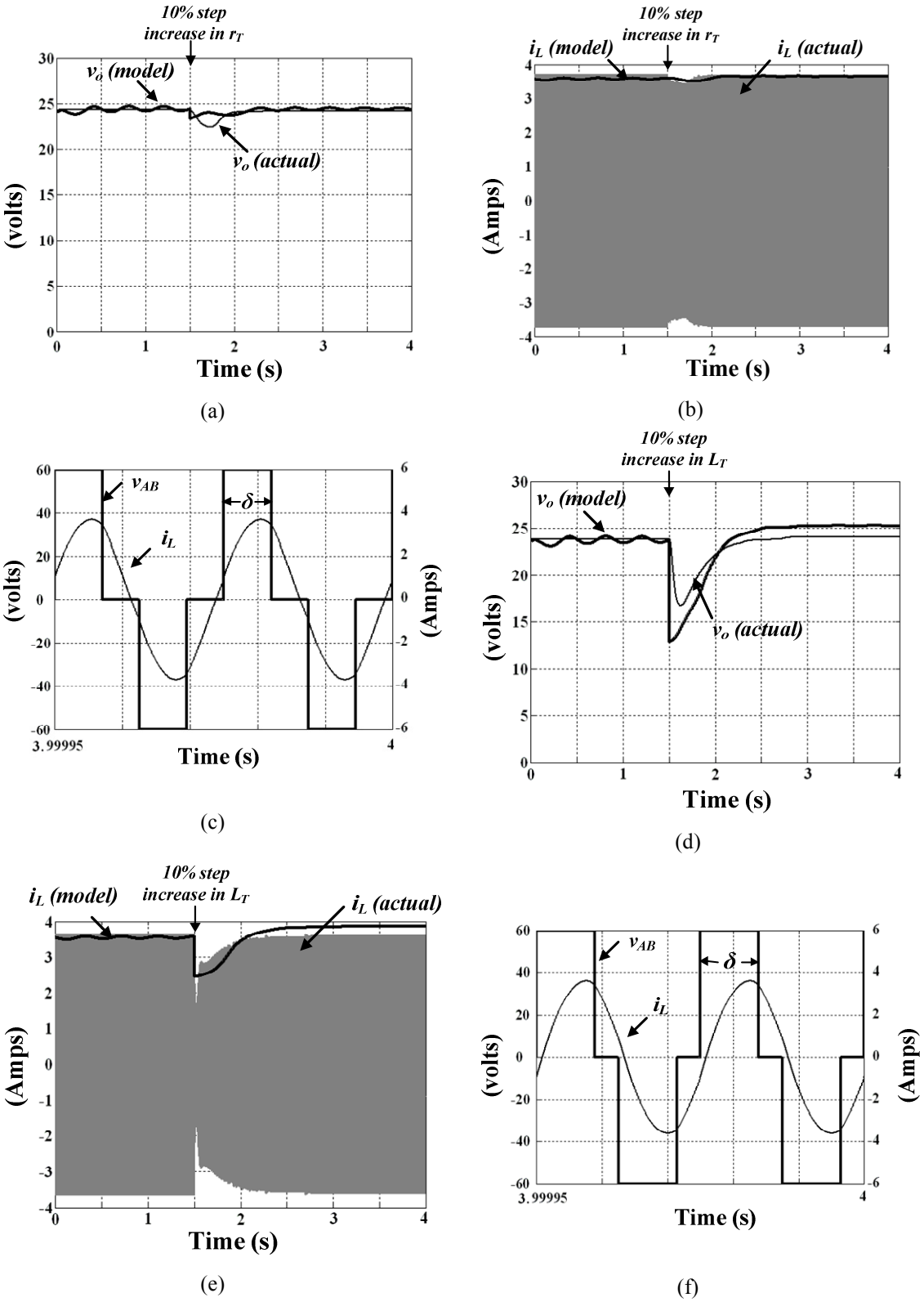


Fig. 4.22: Results for robustness analysis comparing the actual converter operating at Q_{FL} with the proposed model, in response to a +10% step change (at t=1.5s) in the value of: (a)-(c) r_T and (d)-(f) L_T.

4.6.3 Critical model evaluation

The original large-signal non-linear model is a relatively precise representation of the converter for the entire load operating range. However, its non-linearity limits the application of simple and well known linear analysis and control techniques. Small-signal models are an important linearization tool and have proven to be successful for control design and stability analysis of many systems. However the validity of the model remains limited to the close neighbourhood of the steady-state operating point and the model is not a true representative of large operational variations. From this perspective, the linearization scheme for the large-signal model was proposed to preserve the large-signal characteristics of the converter without linearizing around specific operating points. The methodology implemented for linearization can be viewed as an orientation of the ac subsystem *dq* state variables into an arbitrary reference frame to remove the main source of non-linearity; the mathematical square-root function.

The proposed model has shown to provide closely matching results with the actual converter switched model. However, at high converter loading (high Q factor), the harmonic content in the resonant tank increases and the sinusoidal nature approximation of the resonant tank state variables becomes less accurate. This is mainly because a high Q factor means low load impedance compared to the resonant tank characteristic impedance. Consequently, the ratio of the injected square wave current from the bridge rectifier to the resonant circuit current is high, hence introducing higher order harmonics. Distortion introduced at high Q causes the proposed linearized model to have a marginal error in the value of the calculated state variables. This can be improved by assuming that the resonant tank state variables are a harmonic series (instead of simply the fundamental component). However, this would result in n-times the existing number of resonant tank state variables, where n is the number of higher order harmonics included in the model. This makes the analysis more difficult, tedious and increases the computational burden on the DSP, and in return marginal improvement is achieved.

4.7 Sensorless multi-loop control

Multi-loop control schemes have been used to improve the stability and dynamic characteristics of power electronic converters [4.16, 18]. By increasing the closed-loop stability margin, loop gain can be increased to speed up system response and increase disturbance rejection capability [4.19, 20]. In this section, the single-loop output voltage PI

controller is extended to include an inner control loop to enhance closed-loop system performance. However, using the fast resonant tank state variables of the phase-controlled SPRC (i_L, v_{Cs} and v_{Cp}) for inner control loop realization presents a few practical challenges:

- The resonant tank state variables are approximately sinusoidal with a fundamental frequency equivalent to the switching (sampling) frequency at which the control is updated (phase angle δ). This is illustrated in Fig. 4.23.

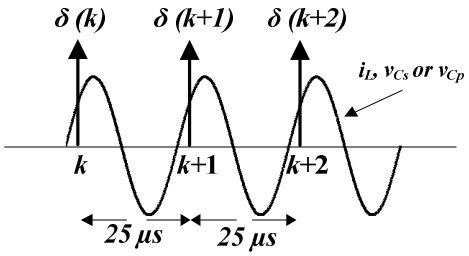


Fig. 4.23: Sampling diagram

  This is acceptable since the main converter control variable is the output voltage which is dc and slowly changing compared to the fast resonant tank dynamics. However, if the resonant tank state variable used for inner control loop is measured using a sensor and converted using the DSP analog-to-digital converter with the same sampling frequency as its fundamental frequency, one sample per period conversion results. Therefore, this cannot be used for control implementation. The use of higher sampling frequencies is unnecessary for the slow output voltage control and would also reduce the time available for DSP control algorithm execution.
- The resonant tank state variables are ac and the output voltage is dc. The latter is used for the outer loop, therefore, if a resonant tank state variable is used for the inner control loop, a phase-locked loop (PLL) is needed for conversion of the ac signals to dc. A PLL at such high fundamental frequency (f=40 kHz) becomes impractical because a higher sampling frequency is needed to increase its angle resolution.

Implementing the derived model with its associated linearization scheme solves both problems. This is because by using the model, the large-signal behaviour of all the state variables can be estimated, meaning that there is no need for measuring any state varia-

ble. Also the model converts all the fast resonant tank ac state variables to slowly changing dc equivalents, which excludes the need for a PLL for inner control loop realization. The use of the model enables the implementation of a sensorless multi-loop control scheme, hence reducing the number of required measurement sensors. Common problems associated with the use of sensors include [4.21]:

- Sensors raise the total cost of a control system
- Sensors and their associated wiring reduce the reliability of control systems
- Some signals are impractical to measure
- Sensors can induce significant errors such as stochastic noise, cyclical errors, and limited responsiveness.

In this section, a Kalman filter is used to estimate the required state variable for the inner control loop feedback. The Kalman filter is a least-square estimator set to minimize the estimated error covariance. State estimation is added to cater for system dynamics due to parameter variation. Its principal feature is the recursive processing of the noise measurement risk [4.22-25]. Only the estimated state from the previous time step and the present measurement are needed to compute the estimate for the present state [4.26]. The filter estimates the process state at a given time and then obtains feedback in the form of "noisy" measurements. As such, the Kalman filter has two stages:

- *Predict* (time update): responsible for projecting forward in time the current state estimate for the next time step; and
- *Correct* (measurement update): responsible for using an actual noisy measurement to obtain a more accurate prediction of the next time step state estimate.

In the Kalman filter algorithm, the discrete system and measurement equations can be expressed by

$$x(k+1) = A_d x(k) + B_d u(k) + w(k) \tag{4.50}$$

$$z(k) = Hx(k) + v(k) \tag{4.51}$$

where $w(k)$ and $v(k)$ are the process and measurement noise matrices respectively. Their covariance matrices $Q(k)$ and $R(k)$ can be expressed by

$$Q(k) = E\left[w(k)w(k)^T \right],\ R(k) = E\left[v(k)v(k)^T \right] \tag{4.52}$$

H in the measurement equation (4.51) relates the state vector to the measurement *z(k)*. An estimate error *e(k)* can be defined as

$$e(k) = x(k) - \hat{x}(k) \tag{4.53}$$

The estimate error covariance matrix is

$$P(k) = E\left[e(k)e(k)^T \right] \tag{4.54}$$

Fig. 4.24 shows the recursive Kalman filter algorithm with Kalman observer gain *L(k)* and Fig. 4.25 shows the proposed closed-loop sensorless multi-loop control scheme. Details of practical implementation of the Kalman filter algorithm are in Appendix C.

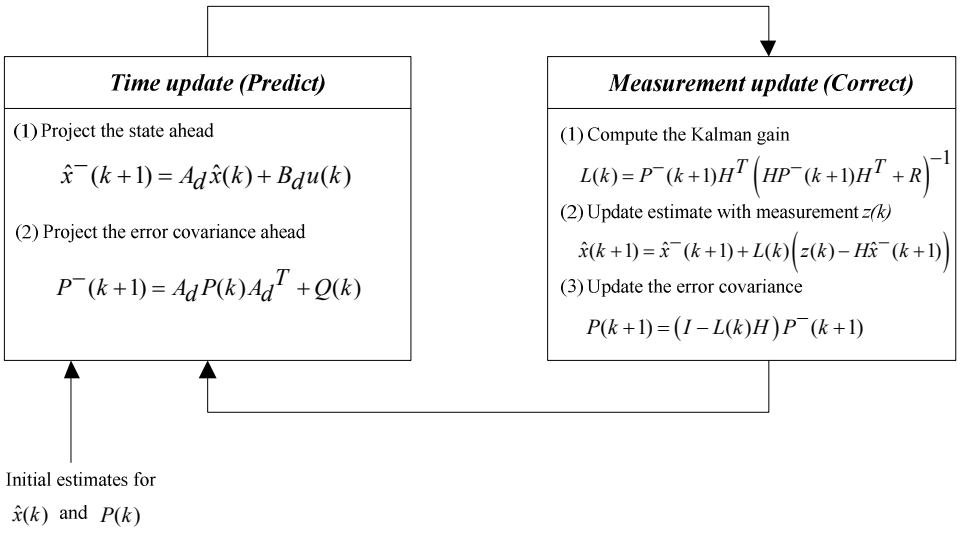
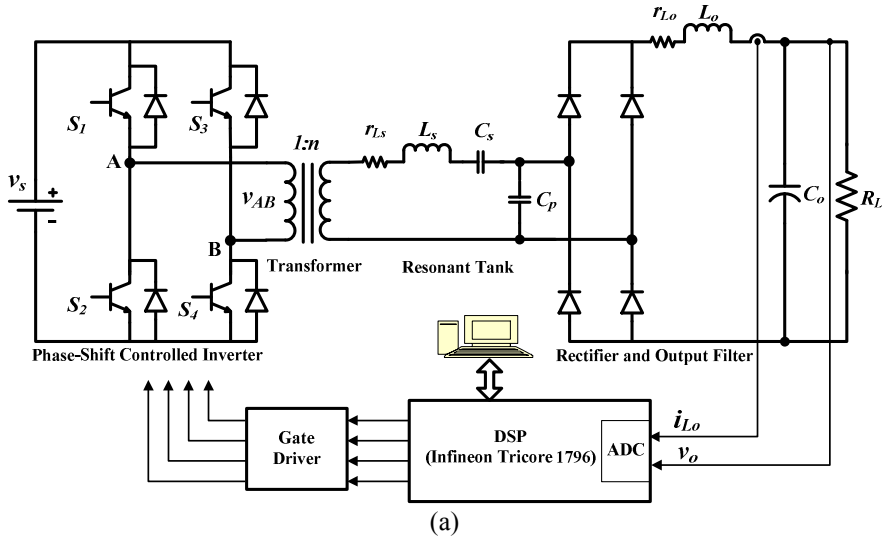


Fig. 4.24: Kalman filter recursive algorithm



(a)

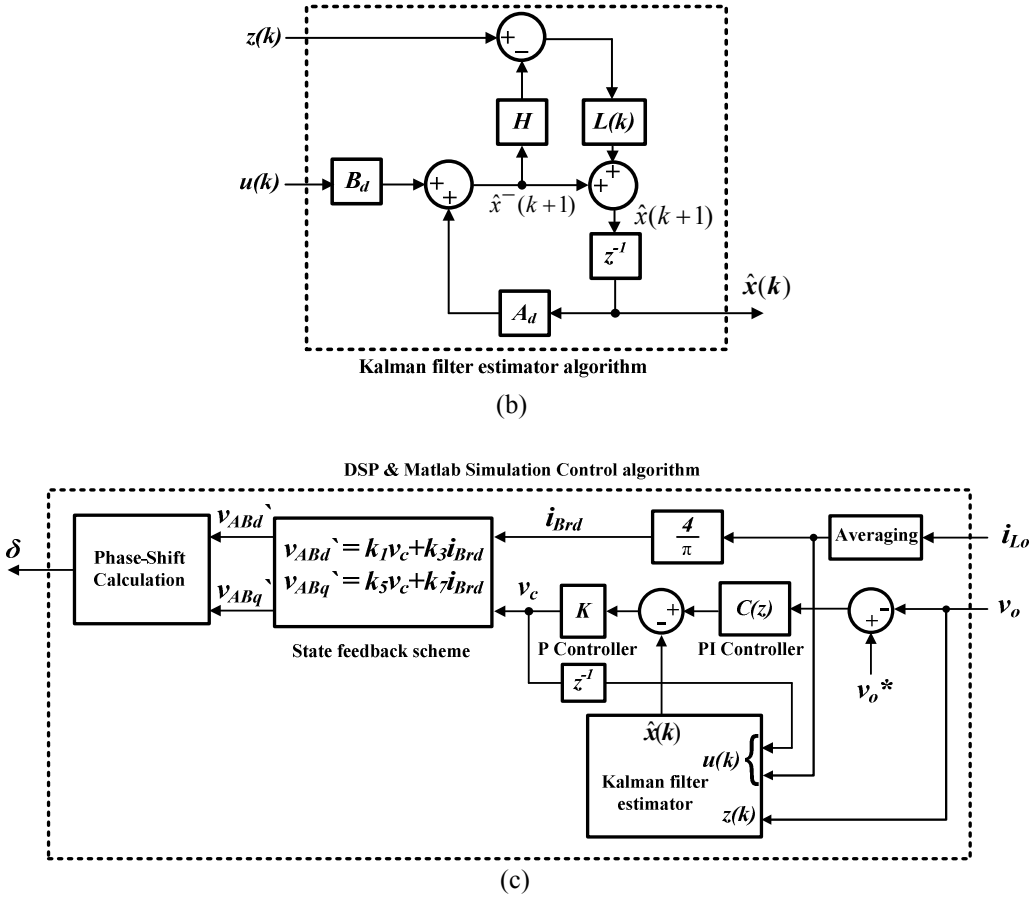


Fig. 4.25: Closed-loop sensorless multi-loop control scheme (a) Circuit diagram, (b) Kalman filter estimator, and (c) Control algorithm.

The selection of the state variable x for the inner control loop is made according to a stability study of the closed-loop system. The generalized transfer function block diagram for the multi-loop control system is illustrated in Fig. 4.26. The state variable x could be one of the following state variables: i_{Ld}, i_{Lq}, v_{Csd}, v_{Csq}, or v_{Cpd}. In order to obtain the necessary transfer functions for closed-loop behaviour study, the equivalent dq circuits of the linearized model (4.37) are derived, as shown in Fig. 4.27. The circuits simplify the representation of the system model, giving more insight into the state variable mathematical relations.

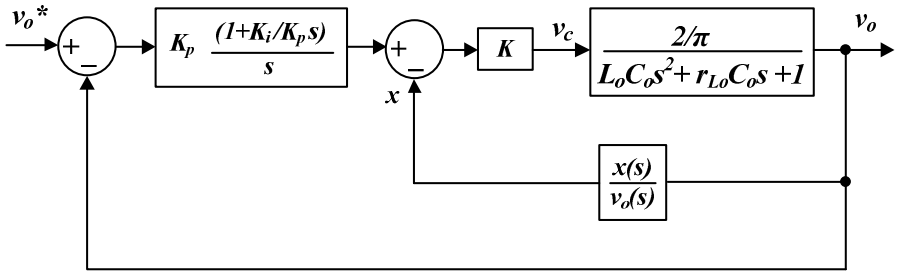


Fig. 4.26: Generalized transfer function block diagram for the multi-loop control system

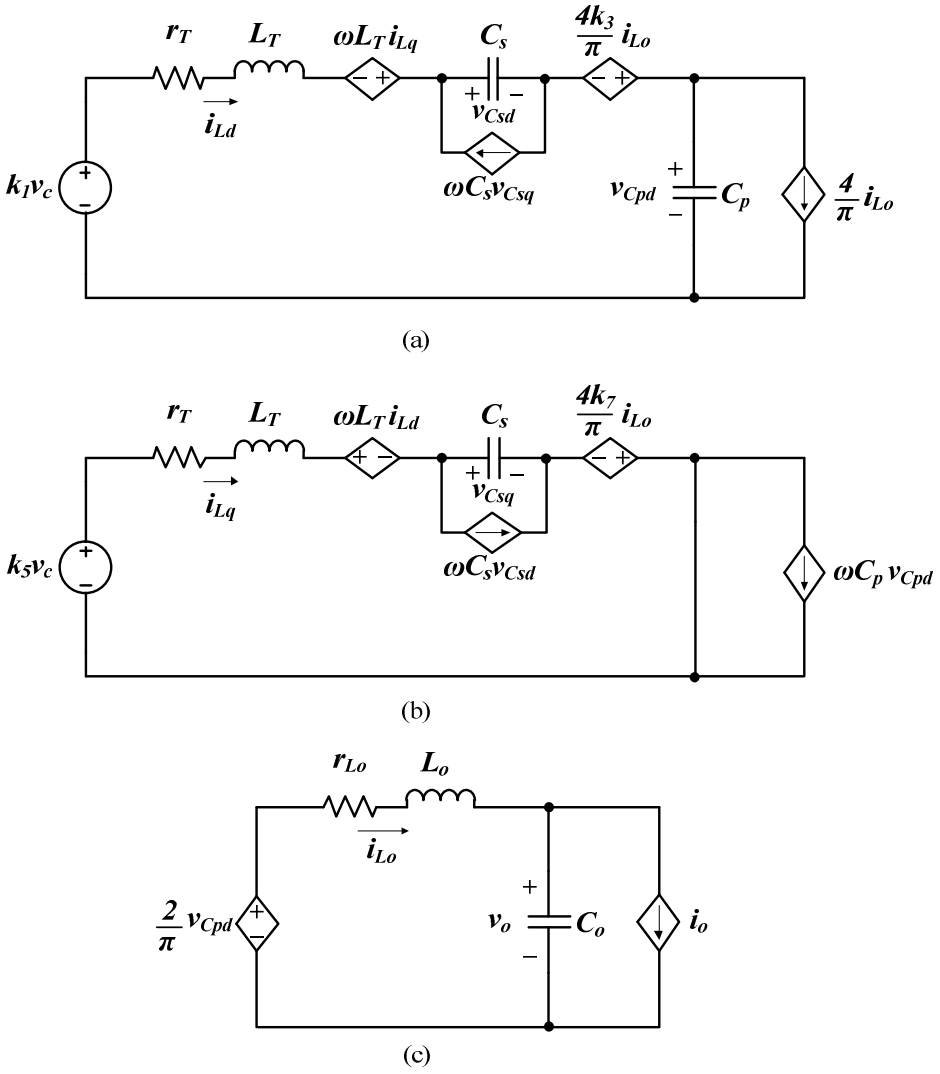


Fig. 4.27: Linearized model equivalent circuits (a) *d*-axis, (b) *q*-axis, and (c) output filter.

4.7.1 D-axis inductor current feedback, i_{Ld}

Inner control loop feedback using i_{Ld} can be realized by taking $x(s)=i_{Ld}(s)$ in Fig. 4.26. The transfer function $i_{Ld}(s)/v_o(s)$ can be obtained using the equivalent circuits in Fig. 4.27 with i_o=0. The transfer function $v_o(s)/v_c(s)$ is defined by (4.40). Therefore, the closed-loop transfer function can be expressed by

$$\frac{v_O(s)}{v_O^*(s)} = \frac{\frac{2}{\pi} KK_p \left(s + \frac{K_i}{K_p} \right)}{a_3 s^4 + a_2 s^3 + a_1 s^2 + \left(1 + \frac{2}{\pi} KK_p \right) s + \frac{2}{\pi} KK_i} \tag{4.55}$$

$a_3 = L_O C_O C_p K$, $a_2 = r_{Lo} C_O C_p K + L_O C_O$, $a_1 = KC_p + \frac{8C_o K}{\pi^2} + r_{Lo} C_O$.

4.7.2 Q-axis inductor current feedback, i_{Lq}

Taking $x(s)=i_{Lq}(s)$ and using the equivalent circuits with i_o=0, the closed-loop transfer function is

$$\frac{v_O(s)}{v_O^*(s)}=\frac{\frac{2}{\pi}KK_p\left(s+\frac{K_i}{K_p}\right)}{a_2s^3+a_1s^2+\left(a_0+\frac{2}{\pi}KK_p\right)s+\frac{2}{\pi}KK_i} \tag{4.56}$$

$a_2=L_oC_o\left(1+K\omega C_p\right)$, $a_1=r_{Lo}C_o\left(1+K\omega C_p\right)$, $a_0=1+K\omega C_p$.

4.7.3 D-axis series capacitor voltage feedback, v_{Csd}

Taking $x(s)=v_{Csd}(s)$ and using the equivalent circuits with i_o=0, the closed-loop transfer function can be expressed by

$$\frac{v_O(s)}{v_O^*(s)}=\frac{\frac{2}{\pi}KK_p\left(s+\frac{K_i}{K_p}\right)}{a_4s^5+a_3s^4+a_2s^3+a_1s^2+\left(a_0+\frac{2}{\pi}KK_p\right)s+\frac{2}{\pi}KK_i} \tag{4.57}$$

$a_4=-L_oC_oC_pL_TK$, $a_3=-r_{Lo}C_oC_pL_TK-L_oC_oC_pr_TK$,

$a_2=\frac{L_oC_oC_pK}{C_s}-r_{Lo}C_oC_pr_TK-L_TC_pK-\frac{8}{\pi^2}L_TC_oK+L_oC_o$, $a_1=\frac{r_{Lo}C_oC_pK}{C_s}-r_TC_pK+r_{Lo}C_o$,

$a_0=1+\frac{C_pK}{C_s}$

4.7.4 Q-axis series capacitor voltage feedback, v_{Csq}

Taking $x(s)=v_{Csq}(s)$ and using the equivalent circuits with i_o=0, the closed-loop transfer function is

$$\frac{v_O(s)}{v_O^*(s)}=\frac{\frac{2}{\pi}KK_p\left(s+\frac{K_i}{K_p}\right)}{a_3s^4+a_2s^3+a_1s^2+\left(1+\frac{2}{\pi}KK_p\right)s+\frac{2}{\pi}KK_i} \tag{4.58}$$

$a_3=-L_oC_oC_p\omega L_TK$, $a_2=-r_{Lo}C_oC_p\omega L_TK+L_oC_o$, $a_1=-2\omega L_TC_pK-\frac{8C_oK}{\pi^2\omega C_s}+r_{Lo}C_o$

4.7.5 D-axis parallel capacitor voltage feedback, v_{Cpd}

Taking $x(s)=v_{Cpd}(s)$ and using the equivalent circuits with i_o=0, the closed-loop transfer function can be expressed by

$$\frac{v_o(s)}{v_o^*(s)} = \frac{\frac{2}{\pi}KK_p\left(s+\frac{K_i}{K_p}\right)}{a_2s^3+a_1s^2+\left(a_0+\frac{2}{\pi}KK_p\right)s+\frac{2}{\pi}KK_i} \tag{4.59}$$

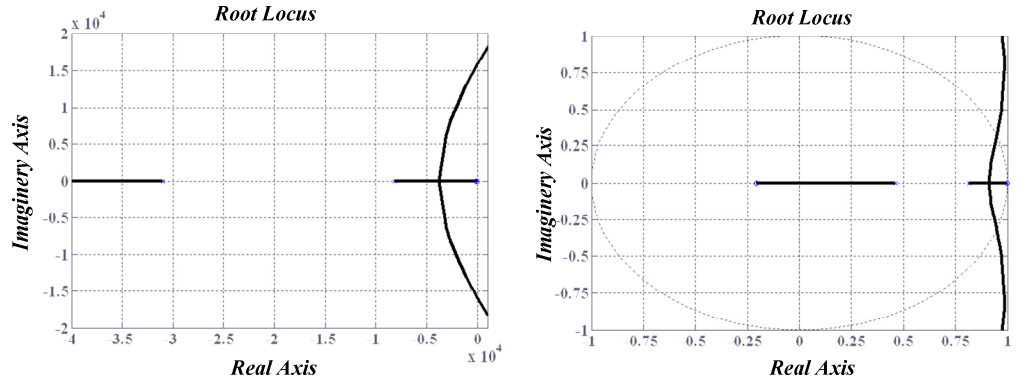
$$a_2 = L_oC_o(1+K)\,, \qquad a_1 = r_{Lo}C_o(1+K)\,, \qquad a_0 = (1+K)$$

4.7.6 Selection of inner control loop state variable

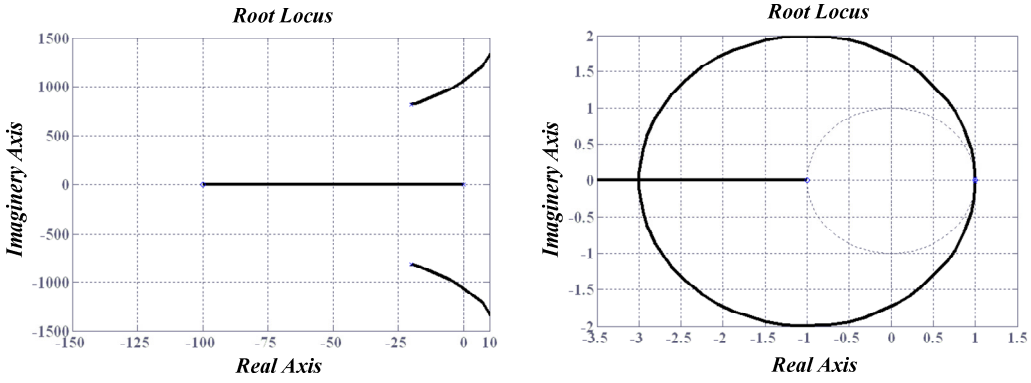
The state variable used for inner control loop realization is selected by studying the closed-loop system stability and closed-loop bandwidth. Selection will be made from i_{Ld}, i_{Lq}, v_{Csd}, v_{Csq}, or v_{Cpd}. The root locus technique is used for the stability study. The characteristic equations of the closed-loop transfer functions (4.55)-(4.59) are re-arranged to the form

$$1+K_pGH(s)=0 \tag{4.60}$$

GH(s) is the open-loop transfer function for which the root locus is plotted. Both continuous and discrete time domain root loci plots are illustrated in Fig. 4.28. The Kalman filter observer dynamics are much faster than the closed-loop system; hence its effect is not included in the closed-loop transfer functions.



(a)



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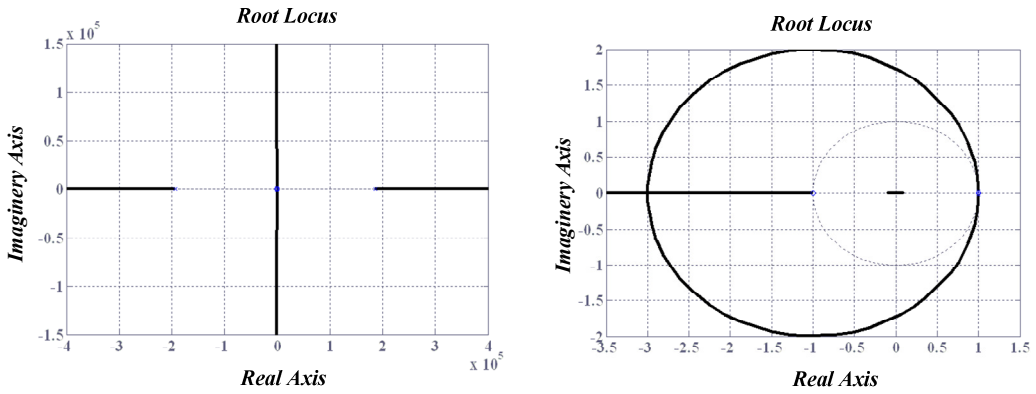
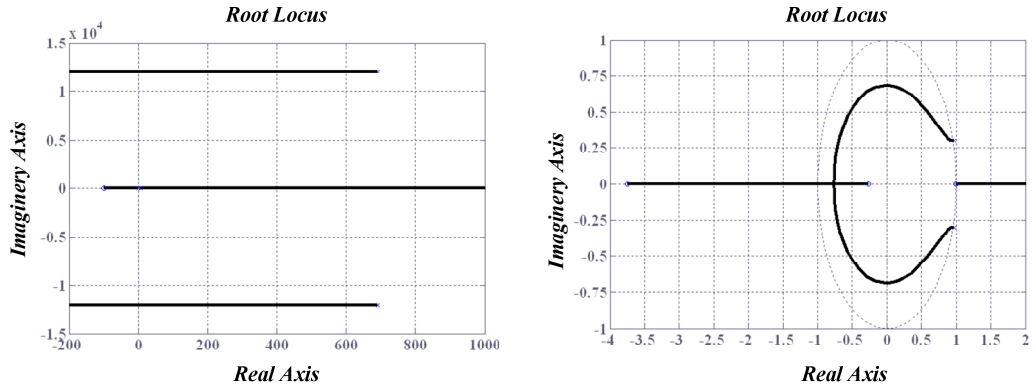


(c)



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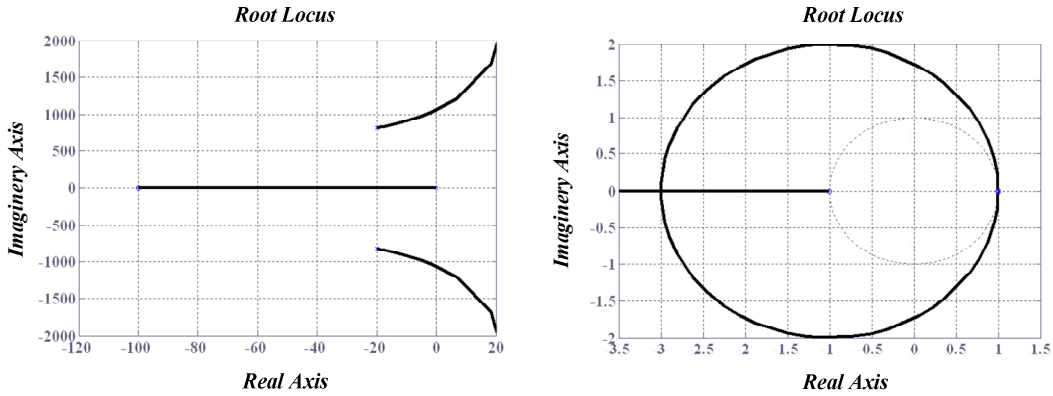


(e)

Fig. 4.28: Root loci of multi-loop control system with the inner control loop state variable being (a) i_{Ld}, (b) i_{Lq}, (c) v_{Csd}, (d) v_{Csq}, and (e) v_{Cpd}.

Fig. 4.28 shows that using i_{Ld} for the inner control loop gives better closed-loop margin of stability than the other state variables. Fig. 4.29 shows a Bode plot of the closed-loop bandwidth with the different state variables. Using i_{Ld} results in the highest closed-loop bandwidth. Compared to single-loop PI control, bandwidth is increased with i_{Ld} from 1 Hz to 120 Hz. The higher bandwidth allows faster closed-loop dynamic response and

better disturbance rejection capability. Therefore, in terms of closed-loop stability and bandwidth, it is confirmed that i_{Ld} is the best state variable for the inner control loop.

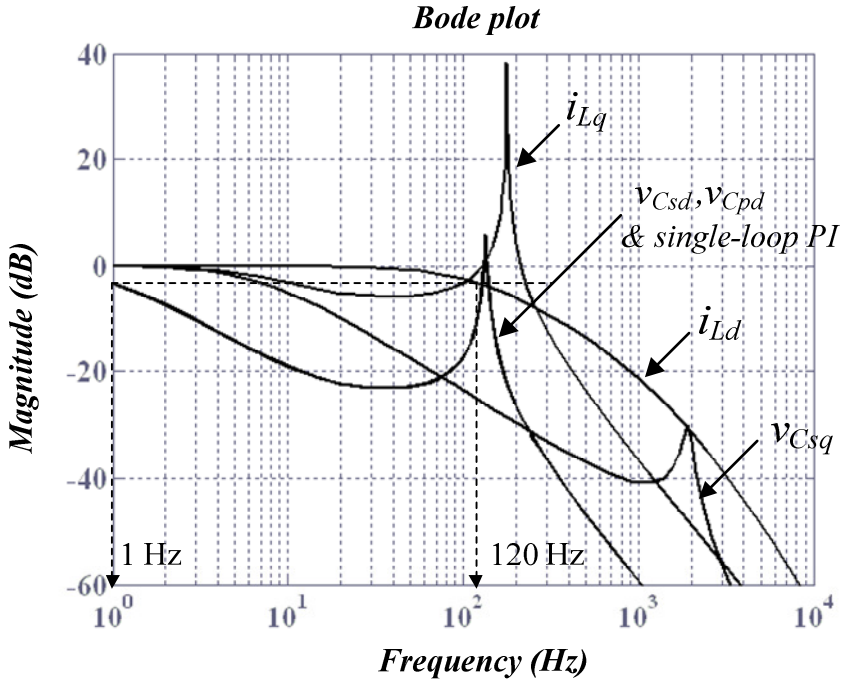
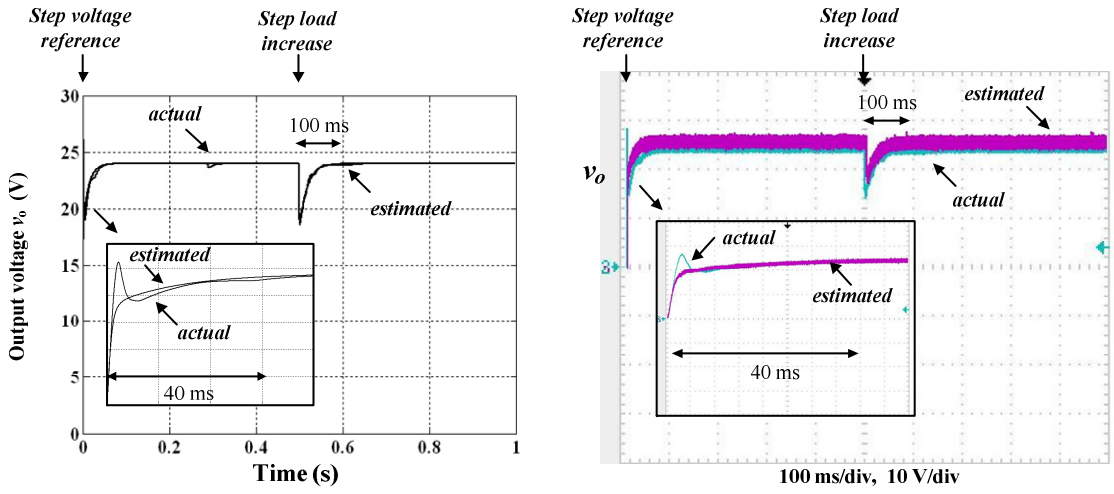


Fig. 4.29: Bode plot illustrating closed-loop bandwidth with the different state variables used for the inner control loop

4.7.7 Simulation and experimental results

Fig. 4.30 shows simulation and experimental results when implementing the proposed sensorless multi-loop PI controller in Fig. 4.25. i_{Ld} is estimated using a Kalman filter observer and is the inner control loop feedback state variable. Parameter and operational values are the same as the single-loop PI controller defined in Table 4.2, with an inner control loop gain K=40.



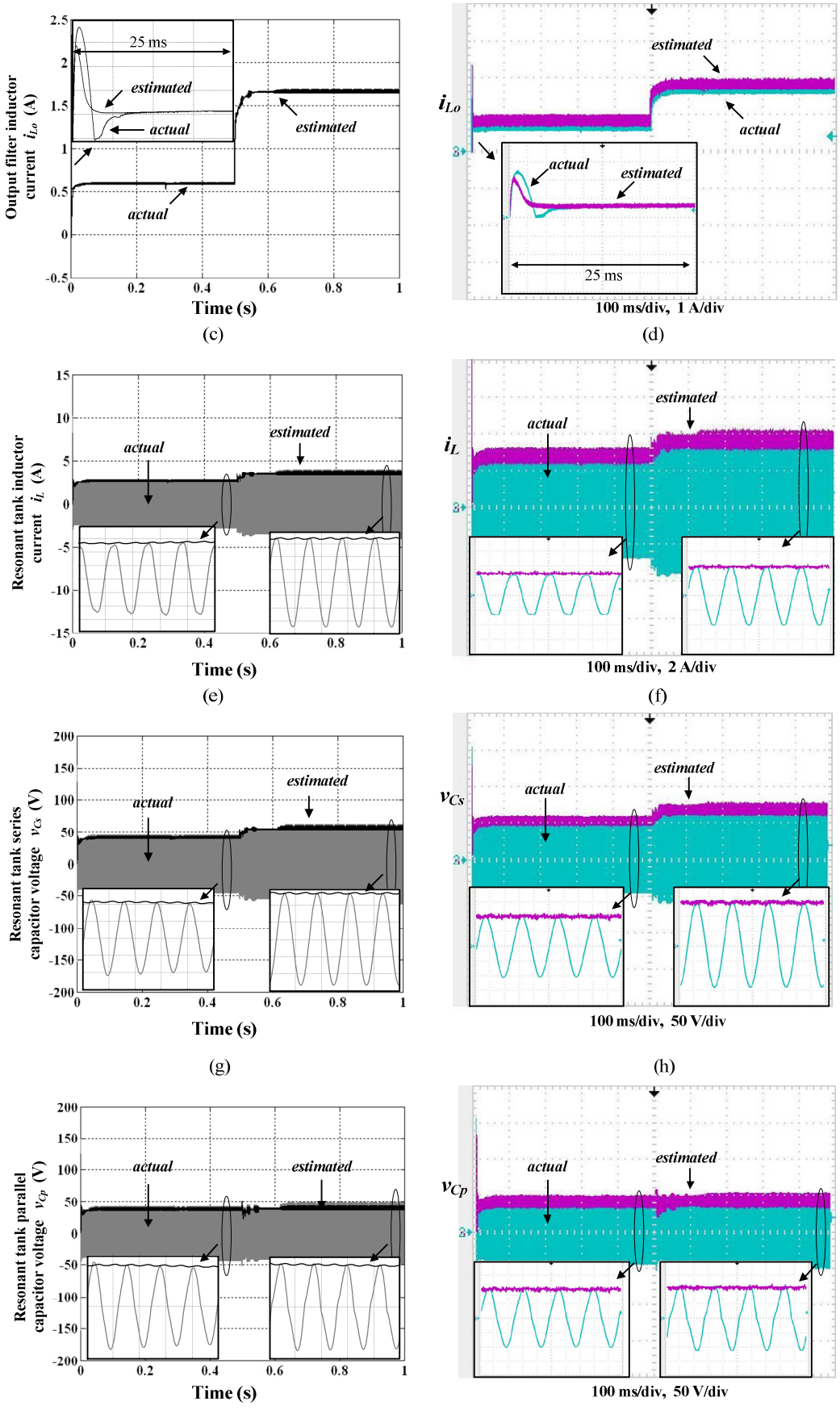


Fig. 4.30: Closed-loop operation results using the proposed sensorless multi-loop PI controller (a),(c),(e),(g)&(i) Simulation, and (b),(d),(f),(h)&(j) Experimental.

The following can be observed from Fig. 4.30:

- Fig. 4.30(a) and (b) show output voltage closed-loop response to a step reference and a step load disturbance. At start-up, the output voltage reaches steady-state in 40ms, compared to 1.0s for the single-loop PI control. At t=0.5s, a step load disturbance from minimum load (R_{Lmin}=40.5Ω) to maximum load (R_{Lmax}=14.4 Ω) is applied. Deviation from the reference output voltage (v_o^*=24V) is minimal compared to single-loop PI control where a high oscillatory response occurs at the step load instant. The high loop gain enhances the closed-loop disturbance rejection, and steady-state is restored after 100ms compared to 2.0s with single-loop PI control;
- Fig. 4.30(c) and (d) show output filter inductor current. Due to multi-loop control, dynamic response improved. At start-up, the current rises and reaches steady-state in 25ms compared to 1.0s with the single-loop PI controller. The current increases after step load application and reaches steady-state after 100ms compared to 2.0s with the single-loop PI case. The latter has a considerably higher oscillatory response. This verifies that the multi-loop control scheme increases closed-loop stability margin;
- Fig. 4.30(e)-(j) show the resonant tank ac state variables i_L, v_{Cs} and v_{Cp}. Simulation and experimental results closely match. The Kalman filter observer gives accurate estimates of the state variables compared to the actual measurements. The proposed model is therefore useful for sensorless multi-loop control of the phase-controlled SPRC which is achieved without additional sensors compared to the single-loop PI controller and with improved performance and closed-loop stability.

4.8 Summary

A new feedback scheme that employs the output filter inductor current to obtain a linearized large-signal model for the phase-controlled SPRC, was proposed in this chapter. All state variables were converted to slowly changing dc quantities which were easier to control than the fast resonant tank dynamics. The proposed state space model represents converter behaviour in response to large-signal variations, hence is useful for faster simulation in addition to estimating converter state variables for sensorless control applications. The model proved accurate when compared to the actual switching converter, and robust against circuit parameter operational variation, especially changes in the resonant tank parasitic resistance. However, it is more sensitive to changes in the resonant tank inductance. A reduced order transfer function was obtained to simplify the

closed-loop PI control design. PI control produces good closed-loop dynamics and steady-state performance. However, the limitation on increasing the proportional gain is the stability of the resonant tank. This can be improved by using multi-loop control. A Kalman filter-based estimator derived from the proposed model was used to implement sensorless multi-loop control of the phase-controlled SPRC. The proposed scheme solves problems arising from practically measuring the fast resonant tank ac state variables for inner control loop use, in addition to enhancing closed-loop dynamics and stability margins with no additional sensors. Stability considerations and closed-loop bandwidth have shown that i_{Ld} is the best state variable for inner control loop use.

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Chapter 5

Robust Control of the Phase-Controlled SPRC

In this chapter, three new robust controllers for output voltage control of the phase-controlled SPRC are presented. The objective is to improve the closed-loop system robustness and enhance dynamic response. For the subsea *All-Electric* project robustness is a necessary requirement due to the harsh subsea physical environment where several factors and disturbances may affect converter operation. The control algorithms proposed are Lyapunov control, sliding mode control (SMC) and predictive output voltage control. Results from the proposed controllers are compared with the PI control presented in chapter four, to verify their enhanced closed-loop response. Since these control algorithms are model dependent, the linearized large-signal state space model derived earlier is used. The linearization scheme has the advantage of reducing the converter model to an equivalent output filter model which significantly simplifies the robust control design process. For each controller, the control law is derived in addition to detailed stability and robustness analysis. Simulation and experimental results demonstrate and validate the proposed designs.

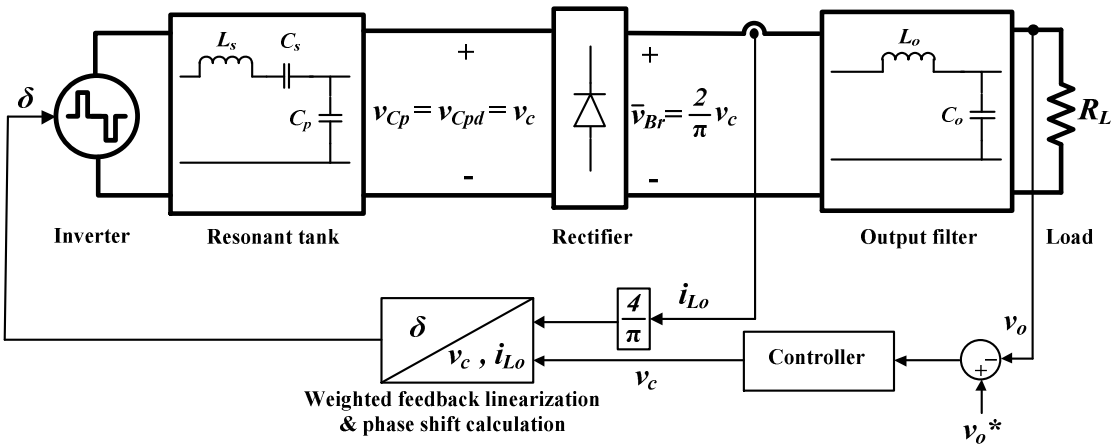
5.1 Background

Several linear and non-linear control techniques have been reported for SPRC [5.1-9]. Among them, the non-linear techniques have received particular attention due to the improvement of the transient response, robustness, and stable behaviour in response to load and input voltage variations [5.10-11]. However, non-linear control laws are usually complex, which makes practical control implementation difficult. Fast, simple and robust sliding-mode controllers were proposed for a zero current switching (ZCS) SPRC operating with quantum-mode control [5.12-13]. A sliding mode controller design approach was applied in [5.14-15] to a zero voltage switching (ZVS) SPRC using the self-sustained phase shift modulation technique introduced in [5.16]. The latter technique, although providing ZVS for the whole load range with good output voltage regulation, varies the switching frequency to obtain this goal. Practically this is usually undesirable due to EMI problems. In this chapter, three new robust controllers are introduced for the

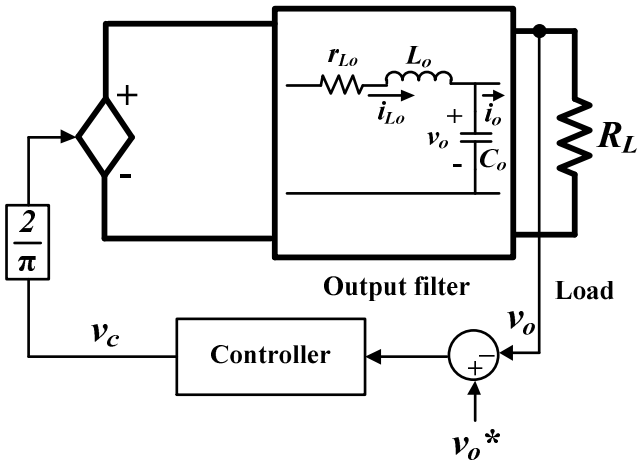
phase-controlled SPRC. The objective is to enhance closed-loop stability and dynamic performance.

5.2 Control problem formulation

The main objective of the phase-controlled SPRC is output voltage control; therefore, the control-to-output voltage transfer function $G_1(s)$ derived in (4.37) is necessary for control design. However, $G_1(s)$ is an eighth order transfer function which makes the design process cumbersome. The proposed state feedback linearization scheme enables simplification of this transfer function to an approximately equivalent second order system of the converter output filter circuit, neglecting the fast resonant tank dynamics. This approximation is highlighted in section 4.5.1 and presents one of the major advantages of the proposed linearization scheme.



(a)



(b)

Fig. 5.1: Closed-loop output voltage control configuration using the linearization scheme (a) full structure and (b) reduced equivalent model.

With the linearization scheme, the new converter control variable v_c introduced by equations (4.33)-(4.44) is directly proportional to the resonant tank peak capacitor voltage v_{Cpd} and rectifier output average voltage $\bar{v}_{Br}$. These relations are illustrated in Fig. 5.1. For this reason, the control v_c appears explicitly in a second order transfer function of the output voltage. From Fig. 5.1(b) the output filter equations can be re-written as

$$\begin{aligned} \frac{di_{Lo}}{dt} &= \frac{1}{L_o}\left(-r_{Lo}i_{Lo} - v_o + \frac{2}{\pi}v_c\right) \\ \frac{dv_o}{dt} &= \frac{1}{C_o}\left(i_{Lo} - i_o\right) = \frac{1}{C_o}\left(i_{Lo} - \frac{1}{R_L}v_o\right) \end{aligned} \tag{5.1}$$

Since the output voltage is the main control objective, it is necessary to obtain the relative degree of v_o. The relative degree is defined as the smallest number of differentiations of the state variable with regard to time until the control variable appears explicitly in the process [5.17-18]. From (5.1), it can be determined that the relative degree of v_o is two, since

$$\frac{\partial}{\partial v_c}\left(\frac{dv_o}{dt}\right) = 0 \tag{5.2}$$

$$\frac{\partial}{\partial v_c}\left(\frac{d^2v_o}{dt^2}\right) \neq 0 \tag{5.3}$$

This means that the control law for any control technique applied has to be of second order so that an expression can be obtained that includes the control variable v_c as the desired output of the control law. This will provide the basis for control law design as will be shown in the analysis of the proposed controllers.

5.3 Proposed Lyapunov controller

A Lyapunov controller uses Lyapunov's stability theory to find if there exists a control *u(x,t)* such that the system can be made asymptotically stable, that is, a system starting in a state $x \neq 0$ in some domain *D* will eventually return to $x=0$. A control Lyapunov function *V(x,u)* is a function that [5.19]

- is positive definite, i.e. $V(x,u) > 0 \quad \forall x \neq 0$
- its derivative is negative definite, i.e. $\dot{V}(x,u) < 0 \quad \forall x \neq 0$
- is proper, i.e. $V(x) \to \infty \quad |x| \to \infty$

The second condition is the key condition; which if satisfied means that for each state *x*, a control input *u* exists that will reduce *V*. This section will consider the design of a Lyapunov controller which minimizes an error signal to perform fast and stable output voltage control of the phase-controlled SPRC.

5.3.1 Construction of control law

For the phase-controlled SPRC described by equation (5.1), define an error signal *e* for output voltage control such that

$$e = v_o^* - v_o \tag{5.4}$$

where v_o^* is the reference (desired) output voltage. A positive definite first order control Lyapunov function *V(x)* is defined as

$$V = \frac{1}{2}(\dot{e} + \alpha e)^2 \tag{5.5}$$

where α is a proportionality constant. According to Lyapunov's second condition, the derivative of *V* has to be negative definite to enable stable operation

$$\dot{V} = (\dot{e} + \alpha e)(\ddot{e} + \alpha \dot{e}) < 0 \tag{5.6}$$

Since *V* is positive definite, to achieve the second condition (5.6), the required negative derivative of *V* is assumed such that

$$\dot{V} = -\beta V \tag{5.7}$$

where β is strictly a positive proportionality constant. Substituting (5.7) and (5.5) into (5.6) yields

$$(\ddot{e} + \alpha \dot{e}) = -\frac{\beta}{2}(\dot{e} + \alpha e) \tag{5.8}$$

Assuming v_o^* to be constant, then

$$\begin{aligned} \dot{e} &= -\dot{v}_O \\ \ddot{e} &= -\ddot{v}_O \end{aligned} \tag{5.9}$$

Substituting (5.9) into (5.8) yields

$$\ddot{v}_O + \alpha \dot{v}_O = \frac{\beta}{2}\left(\alpha v_O{}^* - \alpha v_O - \dot{v}_O\right) \tag{5.10}$$

It is worth noting that $\ddot{v}_O$ is made to appear in the control law (5.10) via the choice of the energy-like Lyapunov function V as a linear first order differential equation and not simply a direct function of the error signal e. The existence of $\ddot{v}_O$ in the control law fulfils the main requirement in section 5.2 for the formulation of the control law so that the control variable v_c appears explicitly. This is proven by substituting the converter dynamic equations in (5.1) into (5.10) which yields

$$v_C = \frac{\pi\alpha\beta L_O C_O}{4}\left(v_O{}^* - v_O\right) - \frac{\pi L_O C_O}{2}\left(\alpha + \frac{\beta}{2} - \frac{1}{R_L C_O}\right)\dot{v}_O + \frac{\pi}{2}\left(r_{Lo} i_{Lo} + v_O\right) \tag{5.11}$$

The control law (5.11) can be re-written as

$$v_C = \left(\frac{\pi\alpha\beta L_O C_O}{4}\right)e + \left(\frac{\pi L_O C_O}{2}\left(\alpha + \frac{\beta}{2} - \frac{1}{R_L C_O}\right)\right)\dot{e} + \frac{\pi}{2}\left(r_{Lo} i_{Lo} + v_O\right) \tag{5.12}$$

where α and β are tuneable parameters. From (5.12), the first and second terms of the controller represent a proportional-derivative (PD) controller. These terms eventually decay with the control action to zero as the system converges to the steady-state reference value. The third term of the controller represents the steady-state value of v_c which can be confirmed from equating the system derivatives in (5.1) to zero. Hence, this term can be considered as a *'feedforward'* term to stablilize controller action and speed transient response.

5.3.2 Closed-loop stability and design

The control law (5.12) can be written in the form of a PD controller with feedforward

$$v_C = k_p e + k_d \dot{e} + \frac{\pi}{2}\left(r_{Lo} i_{Lo} + v_O\right) \tag{5.13}$$

where k_p is the proportional gain and k_d is the derivative gain. The closed-loop structure is illustrated in Fig. 5.2.

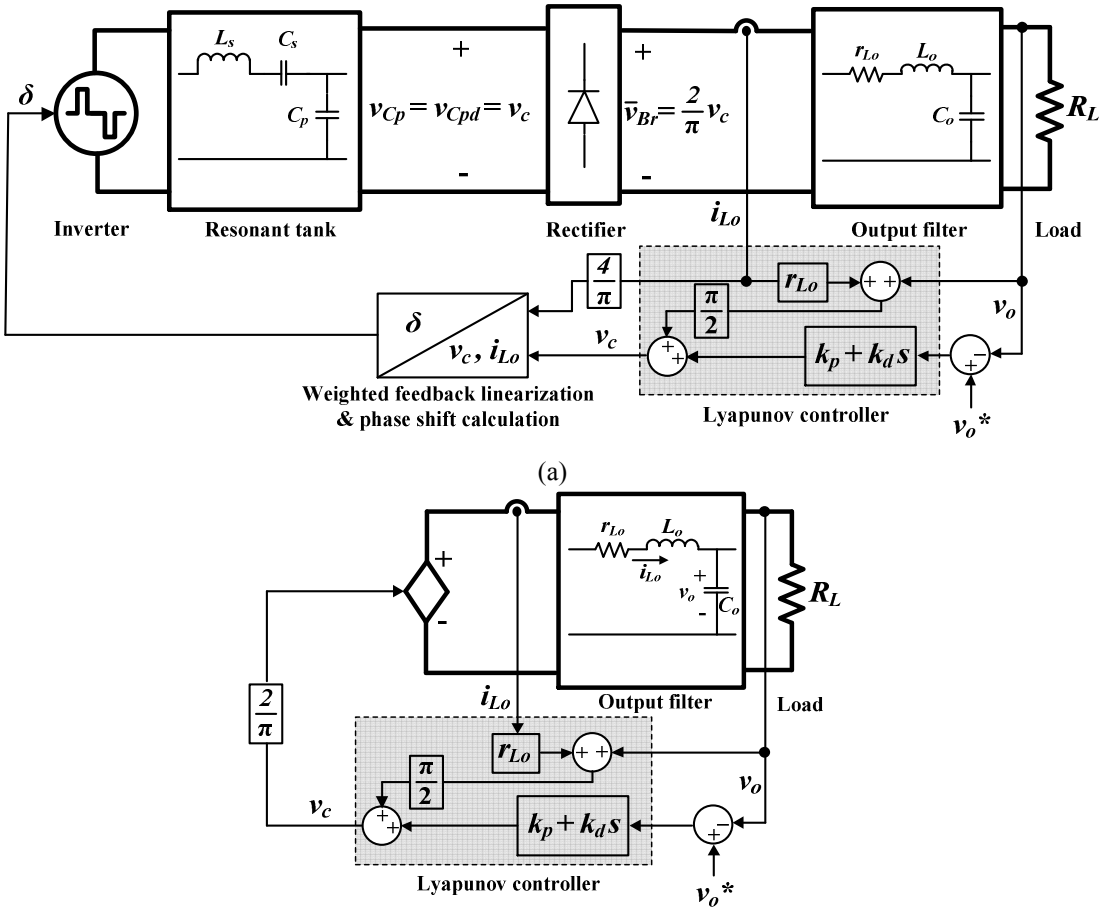
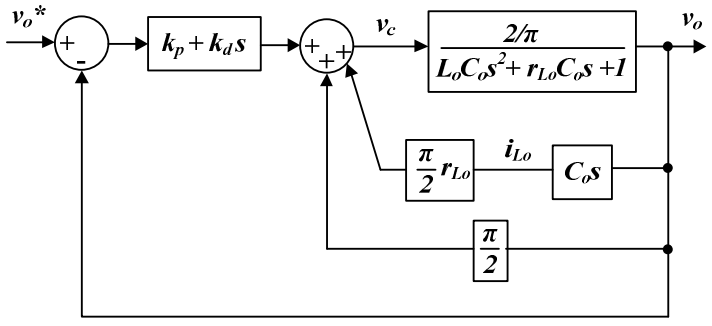


Fig. 5.2: Closed-loop output voltage control using the proposed Lyapunov controller (a) full structure and (b) reduced equivalent model.

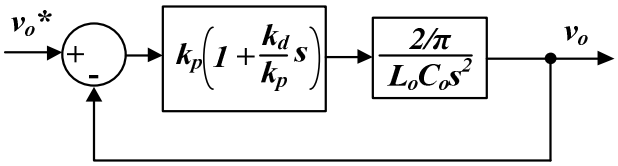
The open-loop transfer functions for the output filter system described by (5.1) can be expressed as

$$V_O(s) = \frac{\frac{2}{\pi}}{L_O C_O s^2 + r_{LO} C_O s + 1} V_C(s) - \frac{L_O s + r_{LO}}{L_O C_O s^2 + r_{LO} C_O s + 1} I_O(s) \tag{5.14}$$

Considering the control-to-output voltage transfer function only (I_o=0), the proposed Lyapunov controller can be represented as shown in Fig. 5.3.



(a)



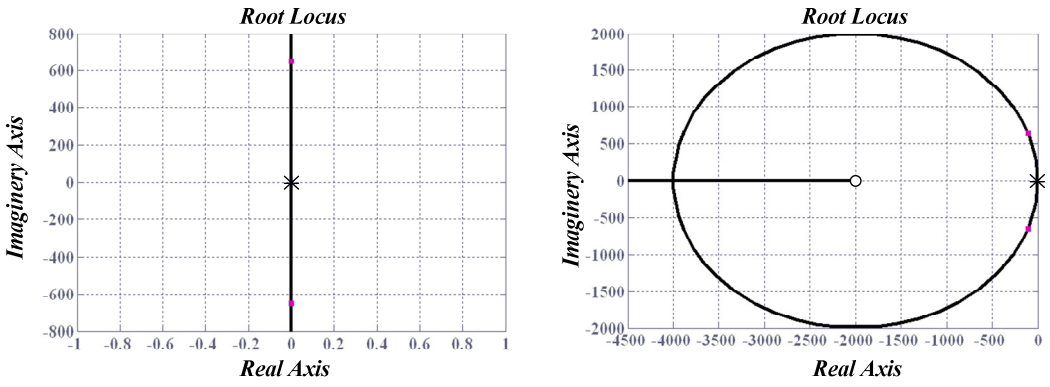
(b)

Fig. 5.3: Closed-loop system with Lyapunov controller
(a) full structure and (b) reduced equivalent structure due to feedforward scheme.

(a) Closed-loop stability

Fig. 5.3(b) shows that the feedforward part of the Lyapunov controller causes the system model to reduce to one with a double pole at the origin of the complex *s*-plane. Because this reduced plant model is marginally stable for all *K*, as shown in Fig. 5.4(a), it cannot be made stable (or unstable) using proportional gain only, hence the Ziegler-Nichols design methodology cannot be used for selection of k_p and k_d. Instead the controller parameters are tailored according to stability margins and desired closed-loop time domain characteristics from the system closed-loop poles. The root locus for the open-loop transfer function *G(s)* is plotted in Fig. 5.4(b) and is defined as

$$G(s)=\frac{\frac{2}{\pi}\left(1+\frac{k_d}{k_p}s\right)}{L_oC_os^2} \tag{5.15}$$



(a) (b)

Fig. 5.4: Root loci for system with feedforward loop of Lyapunov controller
(a) without PD control and (b) with PD control

Fig. 5.4(b) shows that the marginally stable converter transfer function can be made stable by the addition of a left hand plane zero using a PD controller. Irrespective of the value of k_d/k_p (as long as both parameters are positive) the system is stable for all k_p (since the whole root locus lies in the left hand plane). Choice of k_d and k_p determines

system speed of response and other time domain characteristics such as peak overshoot. For closed-loop stability and controller parameter tuning, the system characteristic equation is examined

$$s^2 + \frac{2k_d}{\pi L_o C_o} s + \frac{2k_p}{\pi L_o C_o} = 0 \tag{5.16}$$

By comparing (5.16) with the standard second order characteristic equation

$$s^2 + (2\zeta\omega_n) s + {\omega_n}^2 = 0 \tag{5.17}$$

where ζ is the system damping factor and ω_n is the natural frequency of oscillation, whence

$$\begin{aligned} \omega_n &= \sqrt{\frac{2k_p}{\pi L_o C_o}} \\ \zeta &= \frac{k_d}{\sqrt{2\pi k_p L_o C_o}} \end{aligned} \tag{5.18}$$

According to the Routh-Hurwitz stability criterion, a system is stable if all the characteristic equation coefficients are positive. Hence, for stable closed-loop operation

$$\begin{aligned} k_p &> 0 \\ k_d &> 0 \end{aligned} \tag{5.19}$$

(b) Lyapunov stability

The stability criteria (5.19) can be also obtained in terms of the original Lyapunov controller parameters α and β defined in (5.12). Comparing (5.12) and (5.13):

$$\begin{aligned} k_p &= \frac{\pi\alpha\beta L_o C_o}{4} \\ k_d &= \frac{\pi L_o C_o}{2}\left(\alpha + \frac{\beta}{2} - \frac{1}{R_L C_o}\right) \end{aligned} \tag{5.20}$$

Solving (5.20) simultaneously for β yields

$$\beta^2 - \left(\frac{4k_d}{\pi L_o C_o} + \frac{2}{R_L C_o}\right)\beta + \frac{8k_p}{\pi L_o C_o} = 0 \tag{5.21}$$

The Lyapunov stability is strictly attainable only if β is positive as outlined by (5.7). According to (5.21), this is true if

$$\left(\frac{4k_d}{\pi L_o C_o}+\frac{2}{R_L C_o}\right)>0$$
$$\frac{8k_p}{\pi L_o C_o}>0 \tag{5.22}$$

which reduces to

$$k_p>0$$
$$k_d>-\frac{\pi L_o}{2R_L} \tag{5.23}$$

This eventually leads to the same closed-loop stability criterion (5.19) which was obtained from the study of the control-to-output voltage transfer function irrespective of load, that is, $R_L \rightarrow \infty$. This shows that the system is infinitely stable for all values of k_p and k_d.

(c) Discrete time domain analysis

Control is carried out digitally using the Tricore Infineon DSP. Discretization therefore imposes practical stability limits on the closed-loop system. Discretizing the characteristic equation (5.16) using Euler forward method ($s \rightarrow (z\text{-}1)/T_s$), yields

$$\left(\frac{1}{{T_s}^2}\right)z^2+\left(\frac{2}{\pi L_o C_o T_s}k_d-\frac{2}{{T_s}^2}\right)z+\left(\frac{2}{\pi L_o C_o}k_p-\frac{2}{\pi L_o C_o T_s}k_d+\frac{1}{{T_s}^2}\right)=0 \tag{5.24}$$

where T_s is the sampling period. According to Jury's stability criterion for discrete systems (Appendix B), conditions for closed-loop stability can be expressed as

$$k_p<\frac{k_d}{T_s}$$
$$k_p>\frac{2k_d}{T_s}-\frac{2\pi L_o C_o}{{T_s}^2} \tag{5.25}$$

Solving (5.25) simultaneously yields

$${k_p}^*=\frac{2\pi L_o C_o}{{T_s}^2}$$
$${k_d}^*=\frac{2\pi L_o C_o}{T_s} \tag{5.26}$$

where k_p^* and k_d^* are the points of equality. Fig. 5.5 illustrates a map of possible operating values for k_p and k_d to satisfy discrete closed-loop system stability. Fig. 5.5(a) shows the k_p-k_d map with the closed-loop output voltage transfer function solely, while the effect of the load is included in Fig. 5.5(b).

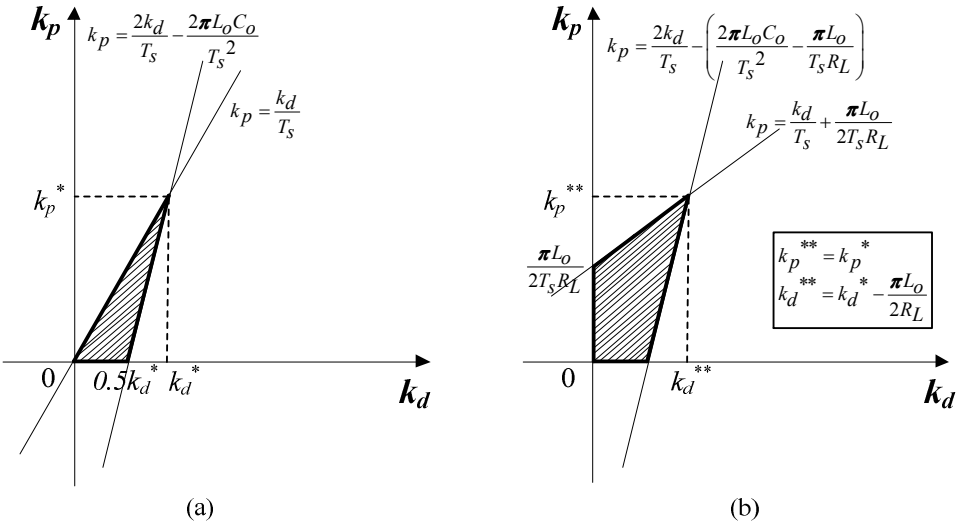


Fig. 5.5: k_p-k_d map for closed-loop output voltage control stability margins (a) at no load and (b) with load.

The discrete system root locus is shown in Fig. 5.6 to illustrate the range of stable closed-loop operation. The open-loop discrete transfer function can be obtained by re-arranging the system characteristic equation (5.24) into the form

$$1 + k_p G(z) = 0 \tag{5.27}$$

$$G(z) = \frac{\frac{2T_s}{\pi L_o C_o}\frac{k_d}{k_p}\left(z - 1 + \frac{T_s k_p}{k_d}\right)}{(z-1)^2} \tag{5.28}$$

The value of k_d/k_p determines the location of the zero on the root locus. Depending on the location of this zero, the closed-loop system stability is bounded by the critical value of the proportional gain K_{cr}. Selection of k_p and k_d are bounded by the conditions in Fig. 5.5. From (5.26), $k_p >> k_d$, therefore k_p dominates system stability. Hence, considering Fig. 5.5(b), k_p is selected such that as $k_d \rightarrow 0$

$$k_p < \frac{\pi L_o}{2T_s R_{L_{\min}}} \tag{5.29}$$

where R_{Lmin} represents the minimum converter loading (maximum resistance).

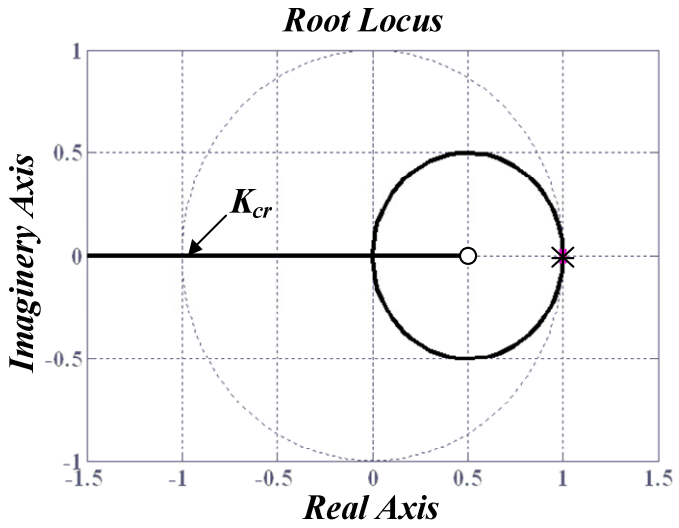


Fig. 5.6: Root locus for discretized system with Lyapunov controller.

Generally, it can be stated that k_p is responsible for system stability and oscillatory behaviour whereas k_d is responsible for increasing speed of response. This can be confirmed from the analysis of the characteristic equations (5.16) and (5.17). Using the experimental circuit parameter values defined in chapter four (Table 4.2), equation (5.29) is evaluated as

$$k_p < \left(\frac{\pi \times \left(12.5 \times 10^{-3}\right) \times 40000}{2 \times 40.5} = 19.39 \right) \tag{5.30}$$

A satisfactory closed-loop step response can be obtained with 20% peak overshoot (ζ=0.456) and a settling time of t_s=4 ms, hence k_d and k_p can be calculated using (5.18):

$$\begin{aligned} k_d &= (\zeta \omega_n) \pi L_o C_o = \left(\frac{4}{t_s}\right) \pi L_o C_o = 0.0047 \\ k_p &= \frac{{k_d}^2}{2\pi L_o C_o \zeta^2} = 11.3313 \end{aligned} \tag{5.31}$$

5.3.3 Simulation and experimental results

Fig. 5.7 and Fig. 5.8 show simulation and experimental results for the Lyapunov controller structure in Fig. 5.2(a). Parameter and operational values are defined in Table 4.2 and controller parameters in (5.31). Fig. 5.7 shows controller response to a step load disturbance from minimum load (R_{Lmin}=40.5Ω) to maximum load (R_{Lmax}=14.4 Ω) at

t=0.5s. The controller meets the desired time domain settling time and peak overshoot parameters in (5.31), at start up. Compared to the multi-loop PI control method (outlined in chapter four), the Lyapunov controller offers superior closed-loop performance. At start up, the output voltage response is much faster (4ms with Lyapunov control compared to 40ms with PI control). The proposed controller is also robust to the full-load disturbance applied at t=0.5s. Deviation from the reference output voltage is minimal compared to multi-loop PI control. The feedforward action provides high disturbance rejection capability for the proposed controller, which responds quickly to minimise the error representing the Lyapunov control function. The output voltage recovers from the full-load disturbance in 1ms compared to 100ms with PI control.

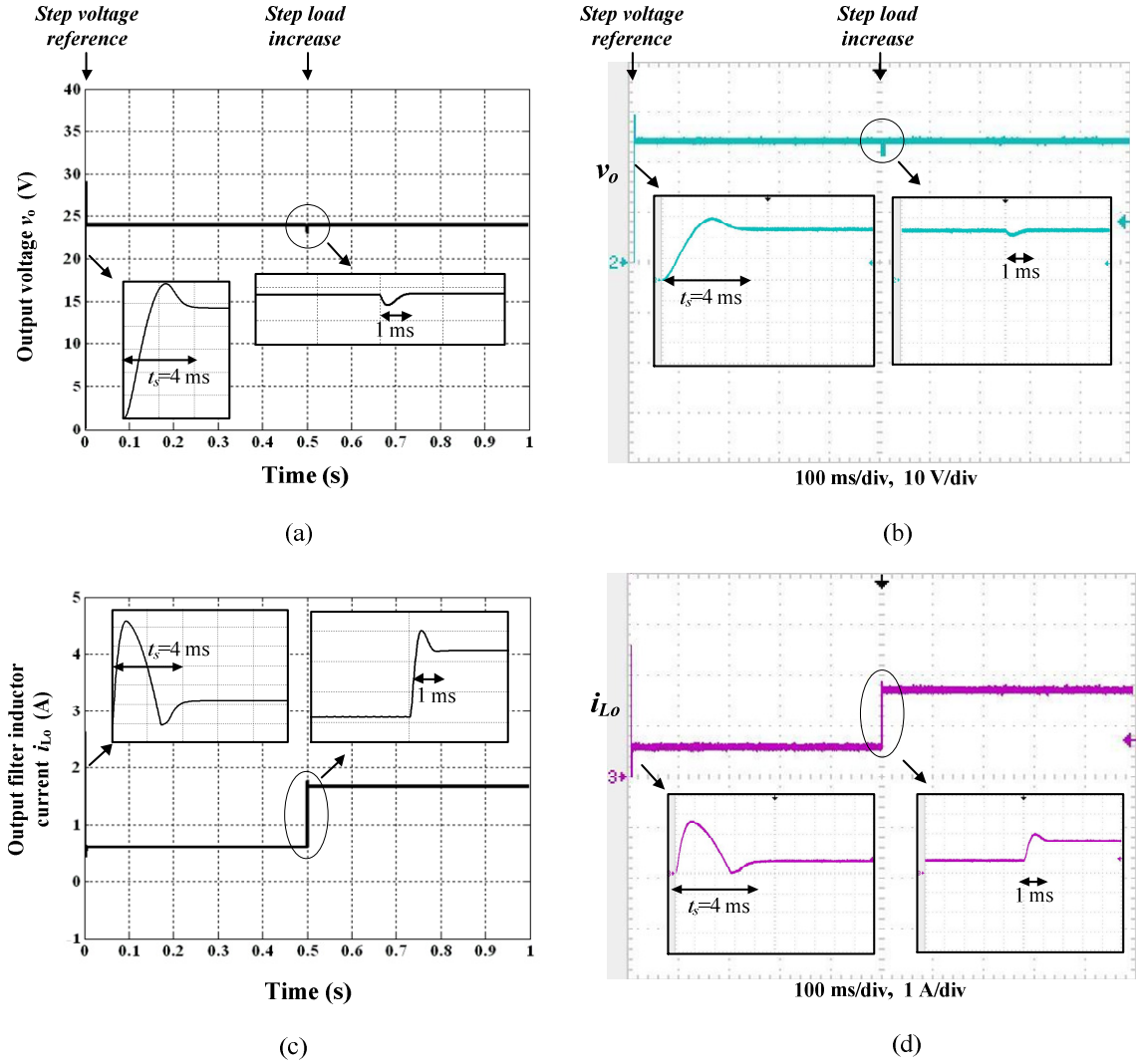


Fig. 5.7: Closed-loop operation results with step load disturbance using the proposed Lyapunov controller (a) and (c) simulation, and (b) and (d) experimental.

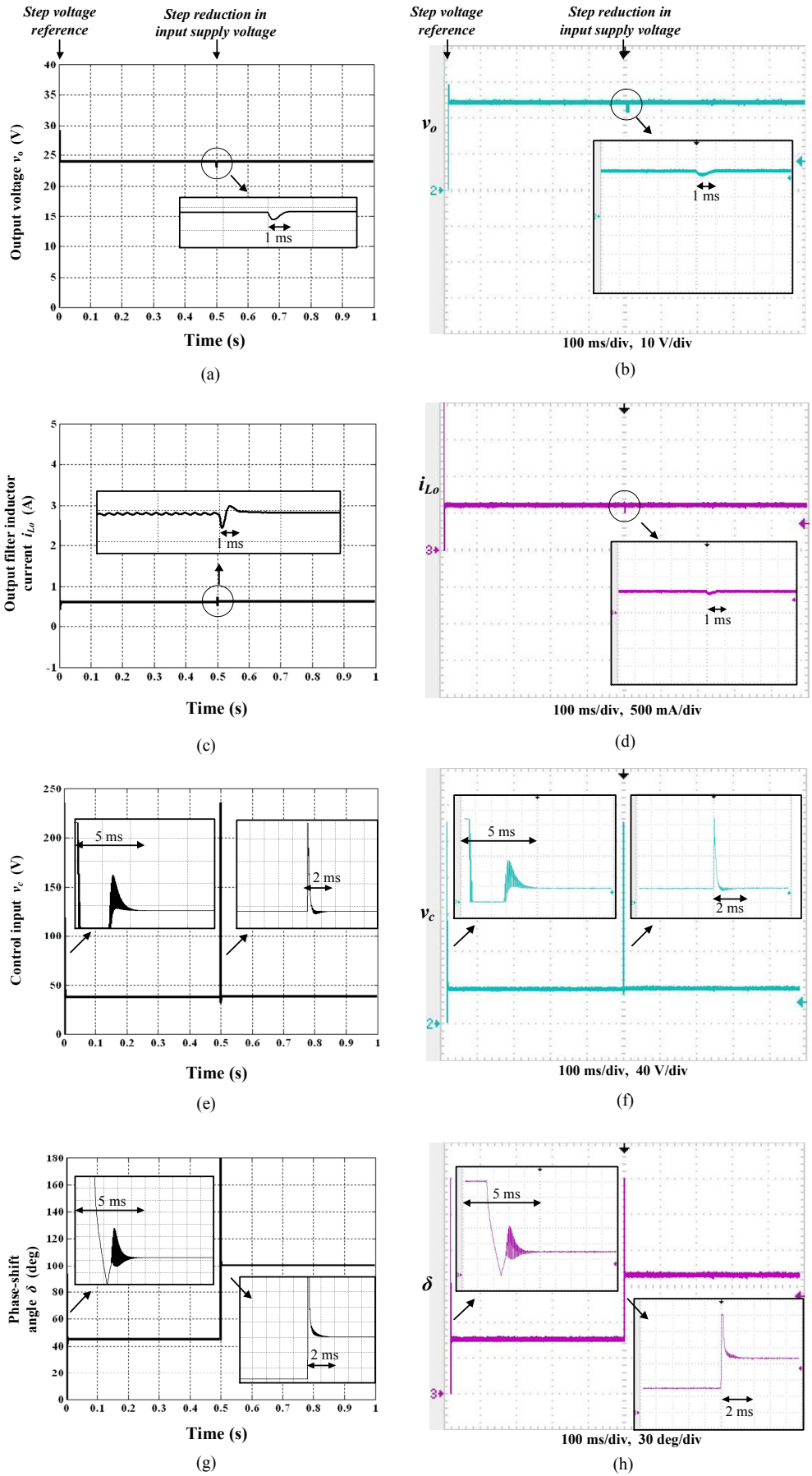


Fig. 5.8: Closed-loop operation results with step input voltage disturbance using the proposed Lyapunov controller (a), (c), (e) and (g) simulation, and (b), (d), (f) and (h) experimental.

Fig. 5.8 shows controller response to a step input voltage disturbance from full supply voltage (V_s=60V) to half supply voltage (V_s=30V) at t=0.5s, at fixed minimum load. Again, the proposed controller shows superior response to the applied disturbance with the desired output voltage achieved 1ms after the disturbance. The control v_c is near constant since it is directly proportional to the output voltage (v_c=$v_o \times \pi/2$) which is regulated by the closed-loop control. The controller takes the necessary action by increasing the corresponding phase shift angle δ from 46° at V_s to 102° at half V_s, to maintain the output voltage constant.

5.3.4 Closed-loop bandwidth

To verify the enhanced closed-loop performance of the proposed Lyapunov controller compared with the multi-loop PI controller, the system closed-loop transfer function is analysed and plotted in the frequency domain to assess the closed-loop bandwidth. Fig. 5.9 shows the closed-loop structure with the proposed Lyapunov controller (feedforward + PD controller). It is the same as Fig. 5.3(a) but with the output current included as the disturbance input.

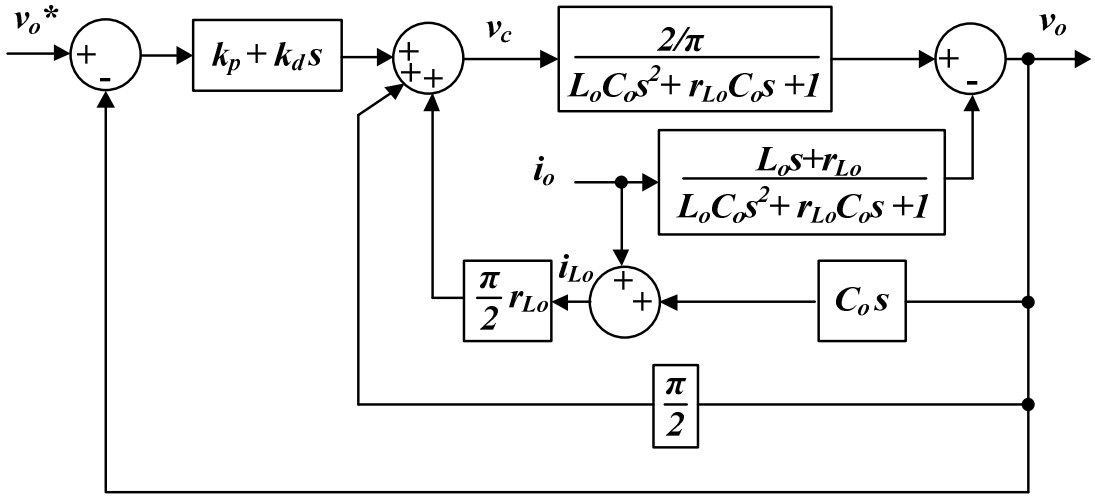


Fig. 5.9: Closed-loop system structure with Lyapunov controller.

From Fig. 5.9, the system closed-loop transfer function can be expressed as

$$V_O(s) = \frac{\frac{2}{\pi}\left(k_p + k_d s\right)}{L_oC_os^2 + \frac{2}{\pi}k_d s + \frac{2}{\pi}k_p} V_O^*(s) - \frac{L_o s}{L_oC_os^2 + \frac{2}{\pi}k_d s + \frac{2}{\pi}k_p} I_O(s) \qquad (5.32)$$

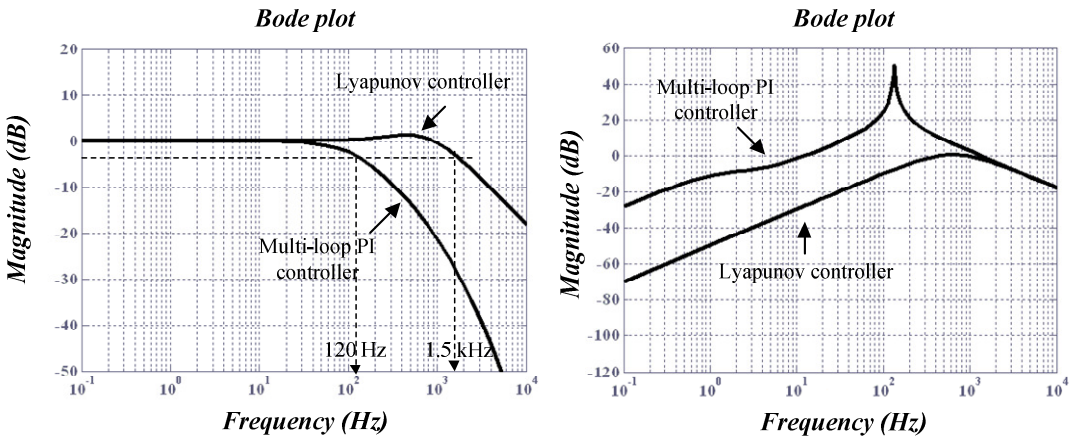


Fig. 5.10: Bode plots comparing the proposed Lyapunov controller and the multi-loop PI controller (a) closed-loop bandwidth and (b) closed-loop output impedance.

Fig. 5.10(a) shows that the proposed Lyapunov controller increases the closed-loop bandwidth from the 120 Hz of the multi-loop PI controller to 1.5 kHz: hence the fast controller dynamic response, especially at start up. Fig. 5.10(b) shows the closed-loop output impedance. The proposed controller has greater disturbance rejection capability, because of the higher attenuating nature of the closed-loop output impedance compared to that of the PI controller. This explains the minor effects that the step load and step input supply voltage changes had on closed-loop performance as illustrated from operation results.

5.3.5 Controller robustness and parameter sensitivity

The proposed controller is model based and hence, variation of system parameters during operation will inevitably affect the closed-loop response. Filter inductance, capacitance and parasitic resistances are all subject to variation due to various operational and environmental factors such as temperature, core saturation and cable overloading. It is therefore necessary to study how changes in these parameters would affect closed-loop stability and dynamic response. Boundaries for system stability are derived and also the effect on dynamic performance is analysed.

(a) System stability

Fig. 5.11 illustrates how the variation of system parameters affects the closed-loop stability boundaries. Controller operating parameters $\hat{k}_p$ and $\hat{k}_d$ are fixed and designed according to the time domain operating requirements. As system parameters vary during

operation, the stability region boundaries shift and if the selected controller parameters fall outside this region, the system becomes unstable. It is therefore necessary to calculate the ranges of change in system parameters that guarantee safe and stable operation.

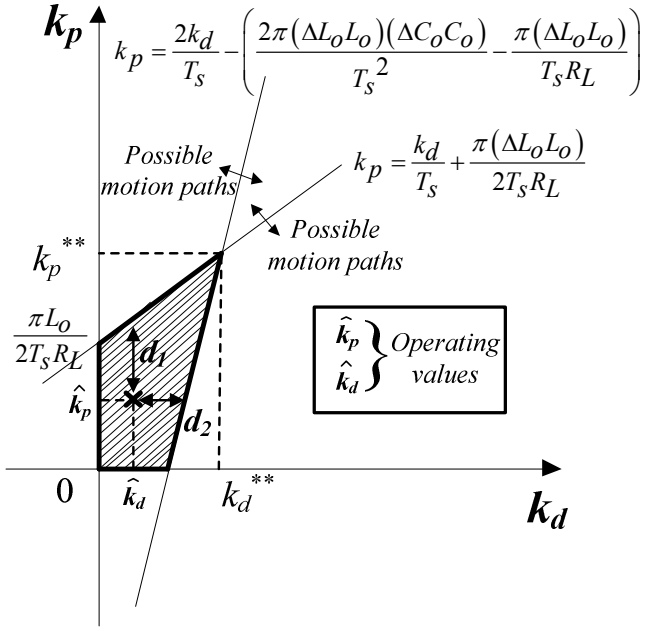


Fig. 5.11: Closed-loop stability margins for system parameter variation.

Fig. 5.11 shows the possible motion paths for the stability region boundaries as the two main circuit parameters (L_o and C_o) change. ΔL_o and ΔC_o are per unit factors representing the change in L_o and C_o such that $\Delta L_o>0$ and $\Delta C_o>0$. It is worth noting that varying these parameters affects only the axis intercepts of the region boundaries, not the line gradients which are constant since T_s is fixed. As the region boundaries shift, the main conditions, from Fig. 5.11, required for closed-loop stability to be maintained are

$$\begin{aligned} d_1 &> 0 \\ d_2 &> 0 \end{aligned} \tag{5.33}$$

where d_1 and d_2 are the distances that separate the operating points ($\hat{k}_p$ and $\hat{k}_d$) from the stability boundaries. Assuming C_o is constant (ΔC_o=1), the conditions for ΔL_o to satisfy stability can be expressed as

$$\begin{aligned} \Delta L_o &> \frac{1}{L_o}\frac{2R_L}{\pi}\left(T_s\hat{k}_p - \hat{k}_d\right) \\ \Delta L_o &> \frac{1}{L_o}\frac{2R_L}{\pi}\left(\frac{T_s\hat{k}_d - 0.5T_s^2\hat{k}_p}{2C_oR_L - T_s}\right) \end{aligned} \tag{5.34}$$

Equation (5.34) shows that for both region boundaries there exists a minimum value of L_o below which the system is unstable. This can be explained from Fig. 5.11 where as L_o increases, both boundaries move further away from the operating points $\hat{k}_p$ and $\hat{k}_d$ and the system is more stable. However, an increase in L_o will produces a more sluggish dynamic response. The larger of the two values in (5.34) provides the global condition for stability with regards to a change in L_o. Similarly, the condition for ΔC_o to satisfy stability can be obtained assuming L_o is constant (ΔL_o=1)

$$\Delta C_O > \frac{1}{C_O} T_S \frac{2R_L\hat{k}_d - T_S R_L \hat{k}_p + \pi L_O}{2\pi L_O R_L} \tag{5.35}$$

(b) Dynamic response

The closed-loop dynamic behaviour is affected by a variation in system parameters. The new time domain characteristics defined in (5.18) can be expressed as

$$\begin{aligned} \omega_n &= \sqrt{\frac{2\hat{k}_p}{\pi(\Delta L_O L_O)(\Delta C_O C_O)}} \\ \zeta &= \frac{\hat{k}_d}{\sqrt{2\pi\hat{k}_p(\Delta L_O L_O)(\Delta C_O C_O)}} \\ t_S &= \frac{4}{\zeta\omega_n} = \frac{4\pi(\Delta L_O L_O)(\Delta C_O C_O)}{\hat{k}_d} \end{aligned} \tag{5.36}$$

For fixed operating $\hat{k}_p$ and $\hat{k}_d$, equation (5.36) shows that increasing L_o and C_o delays system step response (increased t_s) and mitigates oscillatory behaviour. Fig. 5.12 shows the closed-loop output voltage step response for two extreme cases. Case one in Fig. 5.12(a), shows the effect of doubling L_o and C_o. The controller attempts to reject the applied disturbance and recovers to the reference in a stable manner. Fig. 5.12(b) shows the step response when reducing both L_o and C_o to 25% of their original values. Since the parameter values are approaching the critical stability boundary, the closed-loop system has a greater oscillatory response. The closed-loop system has lower stability margin and higher steady-state error.

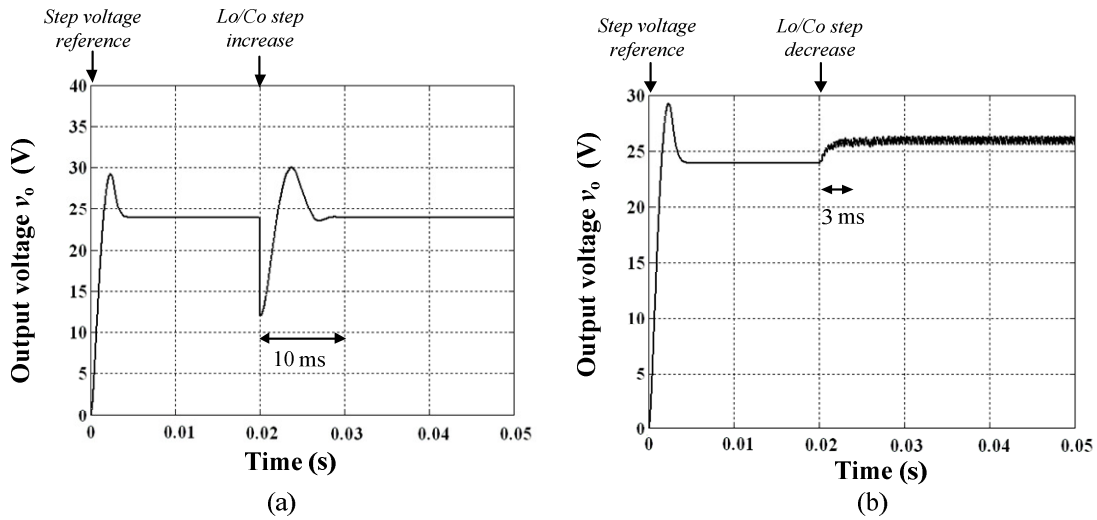


Fig. 5.12: Output voltage step response applying step changes in L_o and C_o
(a) ΔL_o=2pu and ΔC_o=2pu (b) ΔL_o=0.25pu and ΔC_o=0.25pu.

5.4 Proposed sliding mode controller

The theory of variable structure systems and the use of their associated sliding regimes for control design purposes have proven to be sound and successful. Sliding mode control (SMC) was developed in the early 1950s by V. Utkin and is able to tackle system uncertainties and external disturbances with good robustness [5.20-24]. Essentially, SMC uses a high speed switching control law to drive the nonlinear system state trajectory onto a specified user-chosen surface in the state space (called the sliding or switching surface), and to maintain the system trajectory on this surface for all subsequent time [5.25-26]. The main feature of the sliding mode is the acquired system robustness against disturbances in input voltage and load change [5.27]. The other main advantage of SMC is the ability to tailor the dynamic behaviour of the system by the appropriate choice of the switching (sliding) function. The SMC concept is illustrated in Fig. 5.13.

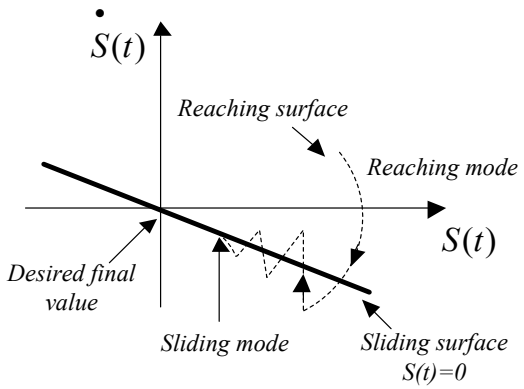


Fig. 5.13: Concept of sliding mode control.

The principle of SMC is to forcibly constrain the system, by suitable control input, to stay on the sliding surface denoted by $S(t)=0$ in Fig. 5.13. There are two conditions for the switching surface design; namely existence and the reachability conditions of the sliding motion. The existence condition states that a switching surface must be created such that sliding motion is possible on that surface. The reachability condition states that a control function must be designed that will be able to drive the state to the switching surface and keep the system in the sliding motion [5.28]. The main drawback of SMC is the issue of chattering. This arises because an ideal sliding mode controller has a discontinuous switching function and it is assumed that the control signal can be switched from one value to another instantaneously. However, in practical systems it is impossible to achieve infinitely fast switching control due to finite time delays for the control computation and limitations of physical devices [5.29]. The result is known as chatter, which is undesirable. It appears as a high-frequency oscillation near the desired equilibrium point and may excite un-modelled high frequency system dynamics [5.30].
In this section, a sliding mode controller is proposed for robust and stable output voltage control of the phase-controlled SPRC. The proposed controller is an enhancement to the discrete self-sustained phase-controlled SPRC proposed in [5.15]. The latter used a sliding mode controller to vary the phase shift angle δ between two discrete values δ_{min} and δ_{max} to obtain output voltage control. This abrupt change in δ causes sudden inverter output voltage change. Although the output voltage is well regulated, resonant tank state variables are highly oscillatory. Alternatively, the proposed sliding mode controller regulates output voltage by varying the control variable v_c between two discrete values v_{cmin} and v_{cmax}. The phase angle δ is calculated from v_c and i_{Lo} using a state feedback scheme and is therefore a continuously changing variable which reduces the oscillatory behaviour of the resonant tank variables.

5.4.1 Synthesis of sliding surface

The phase-controlled SPRC model described by equation (5.1) can be written in terms of the instantaneous control input $v_c(u)$

$$\begin{aligned}\frac{di_{Lo}}{dt} &= -\frac{r_{Lo}}{L_o} i_{Lo} - \frac{1}{L_o} v_o + \frac{2}{\pi L_o} v_c(u) \\ \frac{dv_o}{dt} &= \frac{1}{C_o}\left(i_{Lo} - i_o\right) = \frac{1}{C_o} i_{Lo} - \frac{1}{R_L C_o} v_o\end{aligned} \tag{5.37}$$

where $v_c(u)$ is the converter control input taking two discrete values v_{cmin} and v_{cmax} according to the control law that assigns its value depending on the sign of the switching (sliding) surface $S(x)$

$$v_C(u) = v_{C_{\max}} + \left(v_{C_{\min}} - v_{C_{\max}}\right)u$$
$$u = \begin{cases} u^+ = 1, & for\ S(x) > 0 \\ u^- = 0, & for\ S(x) < 0 \end{cases} \tag{5.38}$$

Since v_c is directly proportional to v_o at steady-state (v_c=½πv_o), values for v_{cmin} and v_{cmax} will be selected as fixed and related to the desired steady-state (equilibrium) value of the output voltage v_o^*

$$v_{C_{\min}} = m_1 \frac{\pi}{2} v_O^*$$
$$v_{C_{\max}} = m_2 \frac{\pi}{2} v_O^* \tag{5.39}$$

where m_1 and m_2 are tuneable parameters and $m_1<m_2$.

From (5.37), the open-loop output voltage dynamics follow a second order system behaviour. The desired closed-loop output voltage dynamics are required to be second order, taking the form

$$k_d \frac{d^2 v_O}{dt^2} + k_p \frac{dv_O}{dt} + k_i (v_O - v_O^*) = 0 \tag{5.40}$$

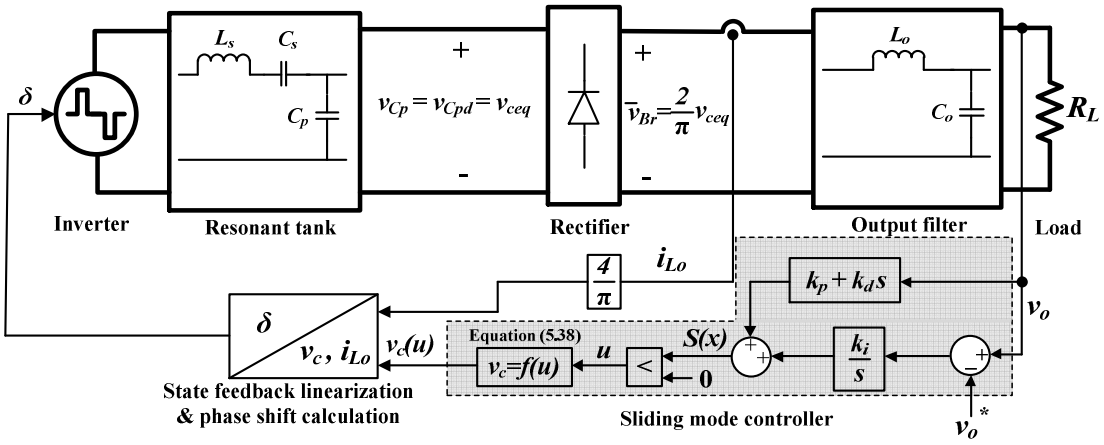
such that the steady-state (equilibrium) value of v_o is equal to v_o* and k_d, k_p and k_i are design constants. In sliding mode control, the converter dynamics are forced to evolve around the sliding surface $S(x)$ according to the invariance condition $\dot{S}(x) = 0$ [5.18]. Based on this property, the sliding surface can be found in order to guarantee the desired dynamics (5.40). Equating the desired closed-loop dynamics (5.40) to the invariance condition

$$\dot{S}(x) = k_d \frac{d^2 v_O}{dt^2} + k_p \frac{dv_O}{dt} + k_i (v_O - v_O^*) = 0 \tag{5.41}$$

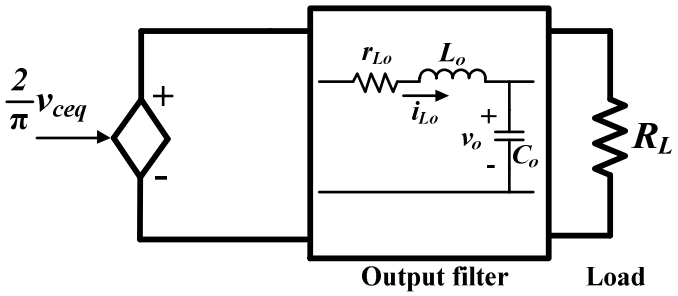
The choice of $\dot{S}(x)$ to be second order is a key design criteria for the sliding mode control law. This follows the control law property outlined in section 5.2 which states that since the relative degree of v_o is two, with respect to the control input v_c, the control law has to be second order. This is shown when extraction of the equivalent control v_{ceq} is performed later in the analysis. The latter only appears in the second derivative term d^2v_o/dt^2. Integrating (5.41) yields the final expression for the sliding surface $S(x)$

$$S(x) = k_d \frac{dv_O}{dt} + k_p v_O + k_i \int (v_O - v_O^*)\, dt \tag{5.42}$$

The closed-loop structure is shown in Fig. 5.14.



(a)



(b)

Fig. 5.14: Closed-loop output voltage control using the proposed sliding mode controller (a) full structure, and (b) reduced equivalent model using the equivalent control input v_{ceq}.

5.4.2 Sliding mode existence conditions

From Utkin theory [5.21, 24], a sliding mode exists in the vicinity of a switching surface if the following condition is satisfied

$$\dot{S}(x)S(x) < 0 \tag{5.43}$$

This is the same criterion as for Lyapunov's asymptotic stability. For inequality (5.43) there exist two cases, as follows.

(a) Case one

If *S(x)*>0, then according to (5.38) $u=u^{+}=1$ and $v_c = v_{c_{\min}} = m_1 \frac{\pi}{2} v_o^*$. From the existence condition (5.43), if $S(x) > 0$ then $\dot{S}(x) < 0$. Applying (5.43) and substituting (using the system model (5.37)) into (5.41) for the derivative terms, yields

$$Ai_{Lo} - Bv_O + Cv_O^* < 0 \tag{5.44}$$

where $A = \frac{k_p}{C_o} - k_d\left(\frac{r_{Lo}}{L_o C_o} + \frac{1}{R_L C_o{}^2}\right)$, $B = k_d\left(\frac{1}{L_o C_o} - \frac{1}{R_L{}^2 C_o{}^2}\right) + \frac{k_p}{R_L C_o} - k_i$, and $C = \frac{m_1 k_d}{L_o C_o} - k_i$.

When system (5.37) equilibrium occurs at $v_o=v_o^*$ and $i_{Lo}=i_o=v_o^*/R_L$, a necessary condition for the existence of a sliding mode on *S(x)* is that the equilibrium points belong to the sliding domain defined by (5.44). Substituting for the equilibrium point values in (5.44) yields the first sliding mode existence condition

$$m_1 < \left(1 + \frac{r_{Lo}}{R_L}\right) \tag{5.45}$$

(b) Case two

If *S(x)*<0, then according to (5.38) $u=u^{-}=0$ and $v_c = v_{c_{\max}} = m_2 \frac{\pi}{2} v_o^*$. From the existence condition (5.43), if $S(x) < 0$ then $\dot{S}(x) > 0$. Applying (5.43) and substituting using the system model (5.37) into (5.41) for the derivative terms, yields

$$Ai_{Lo} - Bv_O + Dv_O^* > 0 \tag{5.46}$$

where $D = \frac{m2 k_d}{L_o C_o} - k_i$ and $D>C$ since $m_2>m_1$. Applying the same conditions for the equilibrium point values as in case one and substituting into (5.46) yields the second sliding mode existence condition

$$m_2 > \left(1 + \frac{r_{Lo}}{R_L}\right) \tag{5.47}$$

(c) Sliding domain boundaries

Combining (5.45) and (5.47) yields the universal sliding mode existence condition

$$m_1 < \left(1 + \frac{r_{Lo}}{R_L}\right) < m_2 \tag{5.48}$$

Condition (5.48) can be also confirmed from the system model (5.37) at steady-state, which equals

$$v_c = \frac{\pi}{2} v_o \left(1 + \frac{r_{Lo}}{R_L}\right) \tag{5.49}$$

Comparing (5.39) and (5.49) taking into account equilibrium at $v_o = v_o^*$ shows that for a sliding mode to exist on $S(x)$, v_{cmin} and v_{cmax} should satisfy (5.48). The sliding domain boundaries outlined by (5.44) and (5.46) are illustrated in Fig. 5.15.

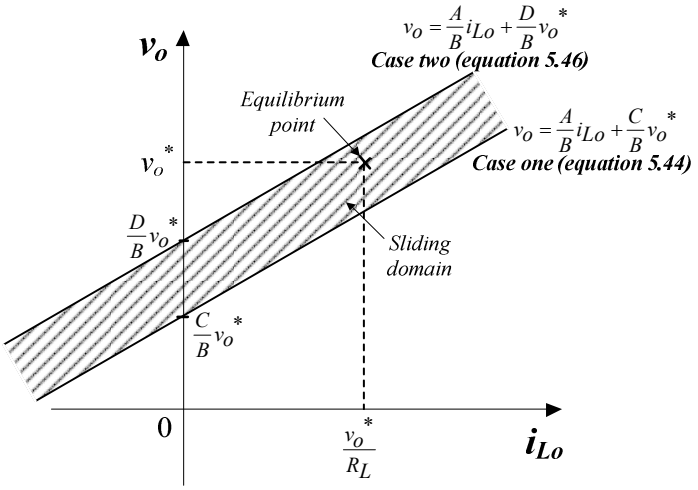


Fig. 5.15: Graphical representation of sliding domain.

5.4.3 Controller design and equations of motion

Different methods for sliding mode control design have been suggested [5.24-25, 27]. These include the controllable canonical form, the Lyapunov approach, the Fillipov systematic mathematical theory, and the equivalent control method. Based on Fillipov's theory, a straightforward technique for designing sliding surfaces is the equivalent control method proposed by Utkin [5.24]. This method is a means of determining the system motion restricted to the manifold $S(x)=0$. The equivalent control approach consists of finding the equivalent input control v_{ceq} so that the state trajectory stays on the

switching surface $S(x)=0$. Once the equivalent control is known, the ideal sliding motion can be found by substituting v_{ceq} into the state equation and the coefficients of the switching function can be designed to obtain the required response.

The equivalent control v_{ceq} can be determined by applying the invariance condition $\dot{S}(x)=0$ given by (5.41). Substituting the system model (5.37) into (5.41), exchanging $v_c(u)$ with v_{ceq} yields

$$\begin{aligned} v_{ceq} = &\frac{\pi}{2}k_p L_o C_o\left(\frac{v_o}{R_L C_o}-\frac{i_{Lo}}{C_o}\right)+\frac{\pi}{2}k_i L_o C_o(v_o{}^{*}-v_o) \\ &+\frac{\pi}{2}k_d L_o C_o\left(\frac{r_{Lo}}{L_o C_o}+\frac{1}{R_L C_o{}^2}\right)i_{Lo}+\frac{\pi}{2}k_d L_o C_o\left(\frac{1}{L_o C_o}-\frac{1}{R_L{}^2 C_o{}^2}\right)v_o \end{aligned} \tag{5.50}$$

Equation (5.50) shows the importance of the control law $\dot{S}(x)$ being of second order. otherwise the equivalent control v_{ceq} cannot be obtained for controlling v_o. This confirms the validity of the control assumption made in section 5.2. Substituting the equivalent control v_{ceq} for $v_c(u)$ into the system model (5.37) gives the ideal sliding dynamic

$$\begin{aligned} \frac{di_{Lo}}{dt} &= -\left(\frac{r_{Lo}}{L_o}+k_p-\frac{r_{Lo}}{L_o}k_d-\frac{1}{R_L C_o}k_d\right)i_{Lo}-\left(\frac{1}{L_o}-\frac{k_p}{R_L}-\frac{k_d}{L_o}+\frac{k_d}{R_L{}^2 C_o}+k_i C_o\right)v_o+k_i C_o v_o{}^{*} \\ \frac{dvo}{dt} &= \frac{1}{Co}iLo-\frac{1}{R_L C_o}v_o \end{aligned} \tag{5.51}$$

Both equilibrium points $v_o=v_o{}^{*}$ and $i_{Lo}=v_o{}^{*}/R_L$ have to satisfy the steady-state condition for the ideal sliding motion (5.51), i.e. zero derivatives. By substituting the equilibrium values in (5.51), it can be shown that this condition can only be obtained if

$$k_d = 1 \tag{5.52}$$

Therefore condition (5.52) is a restrictive condition for equilibrium point existence and stability. In this case, the ideal sliding motion equations reduce to

$$\begin{aligned} \frac{di_{Lo}}{dt} &= -\left(k_p-\frac{1}{R_L C_o}\right)i_{Lo}-\left(-\frac{k_p}{R_L}+\frac{1}{R_L{}^2 C_o}+k_i C_o\right)v_o+k_i C_o v_o{}^{*} \\ \frac{dvo}{dt} &= \frac{1}{Co}iLo-\frac{1}{R_L C_o}v_o \end{aligned} \tag{5.53}$$

Using established linear techniques, the closed-loop transfer function is

$$\frac{V_O(s)}{V_O^*(s)} = \frac{k_i}{s^2 + k_p s + k_i} \tag{5.54}$$

where k_p and k_i are tuneable parameters according to the required closed-loop response. The closed-loop transfer function (5.54) resembles the required system closed-loop dynamics outlined by (5.40) for which the SMC was tailored (for k_d=1). Considering the equivalent control (5.50) and substituting for k_d=1, v_{ceq} becomes

$$\begin{aligned} v_{ceq} &= \frac{\pi}{2} k_p L_O C_O \left(\frac{v_O}{R_L C_O} - \frac{i_{Lo}}{C_O} \right) + \frac{\pi}{2} k_i L_O C_O (v_O^* - v_O) + \frac{\pi}{2} \left(r_{Lo} + \frac{L_O}{R_L C_O} \right) i_{Lo} + \frac{\pi}{2} \left(1 - \frac{L_O}{R_L{}^2 C_O} \right) v_O \\ &= -\left(\frac{\pi}{2} k_p L_O C_O - \frac{\pi}{2} \frac{L_O}{R_L} \right) \frac{dv_O}{dt} + \frac{\pi}{2} k_i L_O C_O (v_O^* - v_O) + \frac{\pi}{2} (r_{Lo} i_{Lo} + v_O) \end{aligned} \tag{5.55}$$

For an error signal $e=v_o^*-v_o$, $de/dt=-dv_o/dt$ for constant reference voltage v_o^*. Therefore (5.55) reduces to

$$v_{ceq} = \left(\frac{\pi}{2} k_i L_O C_O \right) e + \left(\frac{\pi}{2} k_p L_O C_O - \frac{\pi}{2} \frac{L_O}{R_L} \right) \frac{de}{dt} + \frac{\pi}{2} (r_{Lo} i_{Lo} + v_O) \tag{5.56}$$

Thus the equivalent control closed-loop structure of the proposed SMC is in fact exactly the same as that of the Lyapunov controller proposed in section 5.3. The first term is equivalent to the proportional gain of the Lyapunov controller, the second being the derivative gain, and the third being the feedforward. The equivalent control closed-loop structure of the proposed SMC (5.56) is illustrated in Fig. 5.16 as $R_L \to \infty$. This shows that '*effectively*' k_i acts as the proportional gain and k_p acts as the derivative gain of the equivalent Lyapunov controller. Hence, in time domain analysis, the characteristic equation in (5.54) shows that closed-loop stability is maintained for $k_p>0$ and $k_i>0$ which is the same stability criterion with the Lyapunov controller before discretization. Table 5.1 summarizes the design conditions for the proposed sliding mode controller.

Sliding mode existence	***Equilibrium point existence***	***Closed-loop stability***
$m_1 < \left(1 + \frac{r_{Lo}}{R_L} \right) < m_2$	$k_d = 1$	$k_p > 0$, $k_i > 0$

Table 5.1: Summary of conditions for SMC design.

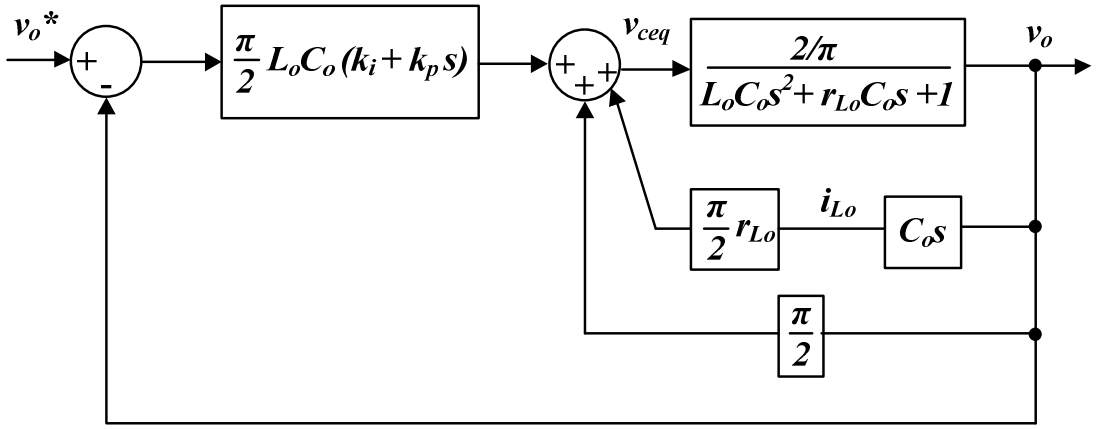


Fig. 5.16: Equivalent control closed-loop structure for the proposed SMC.

5.4.4 Closed-loop stability

Although the closed-loop system is apparently stable for all k_p>0 and k_i>0, in a practical implementation a few issues limit the selection of the control parameters, especially k_i which acts effectively as a proportional gain in the equivalent control system. These factors can be summarized as follows:

- Chattering arising due to finite switching time between one control input value and the other (v_{cmin} to v_{cmax} and vice versa). This is because in a practical implementation, control is updated at a sampling rate of 40 kHz, therefore transition from state to state takes 25μs. This causes a high frequency oscillatory behaviour around the equilibrium point and if k_i is too high this pulls the state trajectory out of the sliding domain, whence sliding motion is lost.
- At start-up, the state trajectory is outside the attraction domain. A high value of k_i will speed up the output voltage initial response by moving it closer to the attraction domain in a shorter time. However, the capability of reaching equilibrium inside the sliding domain is less due to the increased speed of the system behaviour. The result is sustained oscillation of the state trajectory in and out of the sliding domain and an equilibrium state is not reached.
- According to the sliding domain graphically represented in Fig. 5.15, the sliding domain boundaries have equal slopes and the bandwidth (boundaries separation) is determined by the y-axis intercepts. From Fig. 5.15, the bandwidth is determined by the coefficients C and D values which are defined for k_d=1 as

$$C = \frac{m_1}{L_o C_o} - k_i \text{, and } D = \frac{m_2}{L_o C_o} - k_i \tag{5.57}$$

The wider the sliding domain bandwidth, the greater the possibility of reaching equilibrium inside the shaded region of Fig. 5.15. For this reason, m_1 is selected to be a minimum m_1=0 and $m_2>(1+r_{Lo}/R_{LFL})$ where R_{LFL} is the worst case (maximum) loading. However, if k_i is high then C and $D \rightarrow -k_i$ and both sliding domain boundaries come closer until they overlap and the sliding domain eventually becomes the boundary itself. This reduces the likelihood of the state trajectory reaching equilibrium and therefore system response is unstable. Fig. 5.17 shows state trajectory behaviour during start-up illustrating typical stable and unstable system responses obtained by varying controller parameters k_p and k_i. As k_p and k_i change, coefficients A and B change, thence changing the sliding domain boundaries.

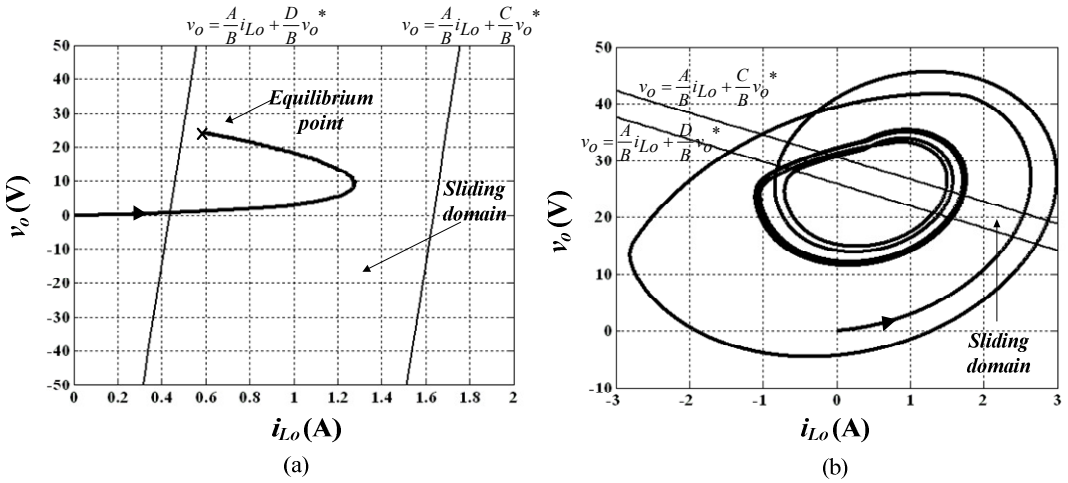


Fig. 5.17: Typical closed-loop behaviour at start-up
(a) stable response, and (b) unstable oscillatory response.

Fig. 5.17(a) shows a stable closed-loop output voltage start-up until the state trajectory reaches equilibrium inside the sliding domain. The sliding domain is 'wide' enough to guarantee stable sliding motion. Further increase in k_p and k_i leads to reduced sliding domain bandwidth, as shown in Fig. 5.17(b) since coefficients A, B, C and D are all k_p and k_i dependent. The narrower sliding domain reduces the likelihood of reaching stable sliding motion inside the domain since the high controller parameters increase the state trajectory energy. The state trajectory attempts to stablilize but keeps oscillating in and out of the sliding domain and fails to reach equilibrium.

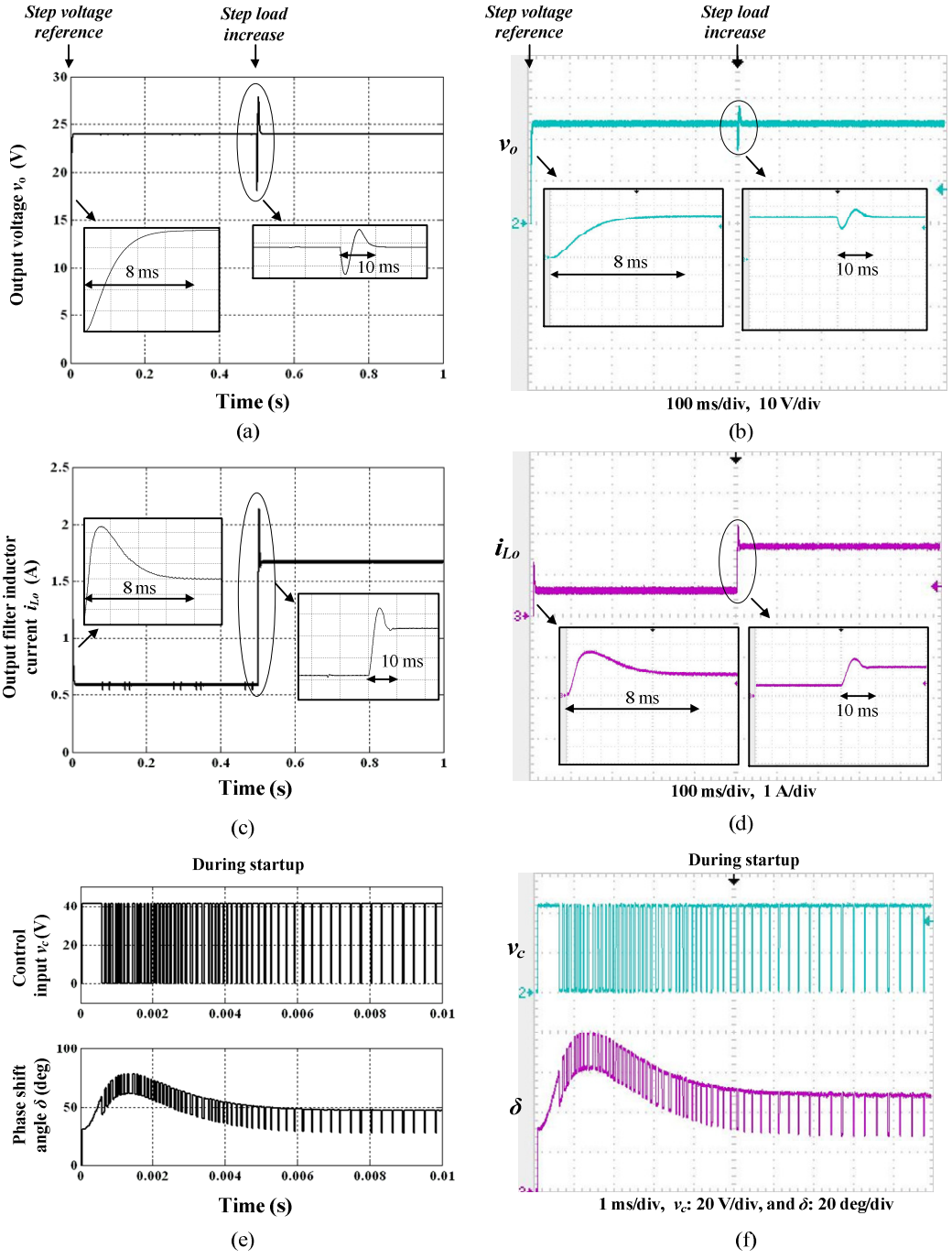
5.4.5 Simulation and experimental results

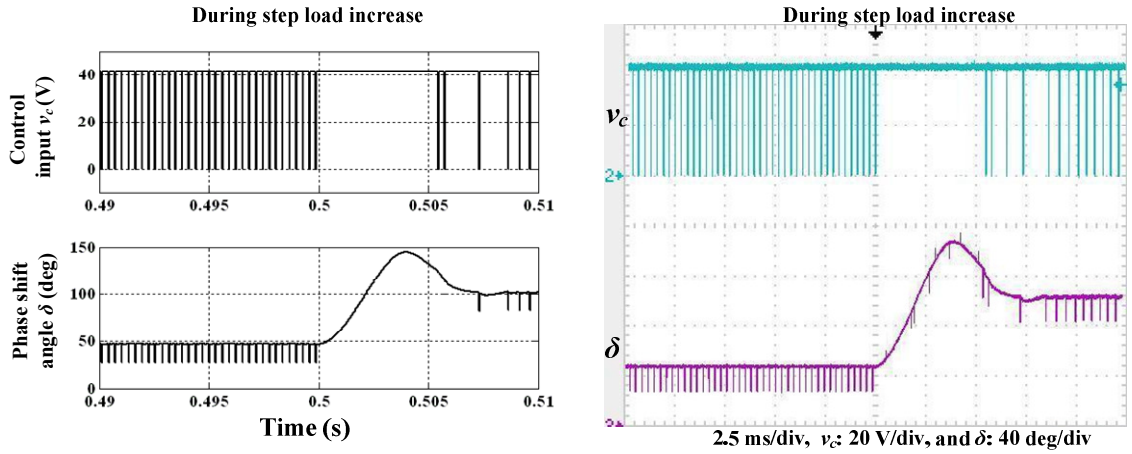
Fig. 5.18 and Fig. 5.19 show simulation and experimental results after implementing the sliding mode controller structure in Fig. 5.14(a). Since it has been proven, as shown in Fig. 5.16 , that the equivalent control sliding mode closed-loop structure is analogous to

the Lyapunov controller designed in section 5.3, the controller parameters pre-selected in (5.31) can be implemented for the SMC

$$\begin{aligned} \frac{\pi}{2} k_i L_o C_o &= 11.3313 \rightarrow k_i = 4.8\times 10^6 \\ \frac{\pi}{2} k_p L_o C_o &= 0.0047 \rightarrow k_p = 1995 \end{aligned} \tag{5.58}$$

However, the selected controller parameters produce an oscillatory closed-loop response. The implemented SMC parameters are k_i=2.5×10^5 and k_p=1000 which satisfy closed-loop settling time (t_s=8ms) and critically damped (ζ=1) step response. Fig. 5.18 shows the controller response to a step load disturbance at t=0.5s.





(g) (h)

Fig. 5.18: Closed-loop operation results with step load disturbance using the proposed sliding mode controller (a),(c),(e) and (g) simulation, and (b),(d),(f) and (h) experimental.

The following can be observed from the results:

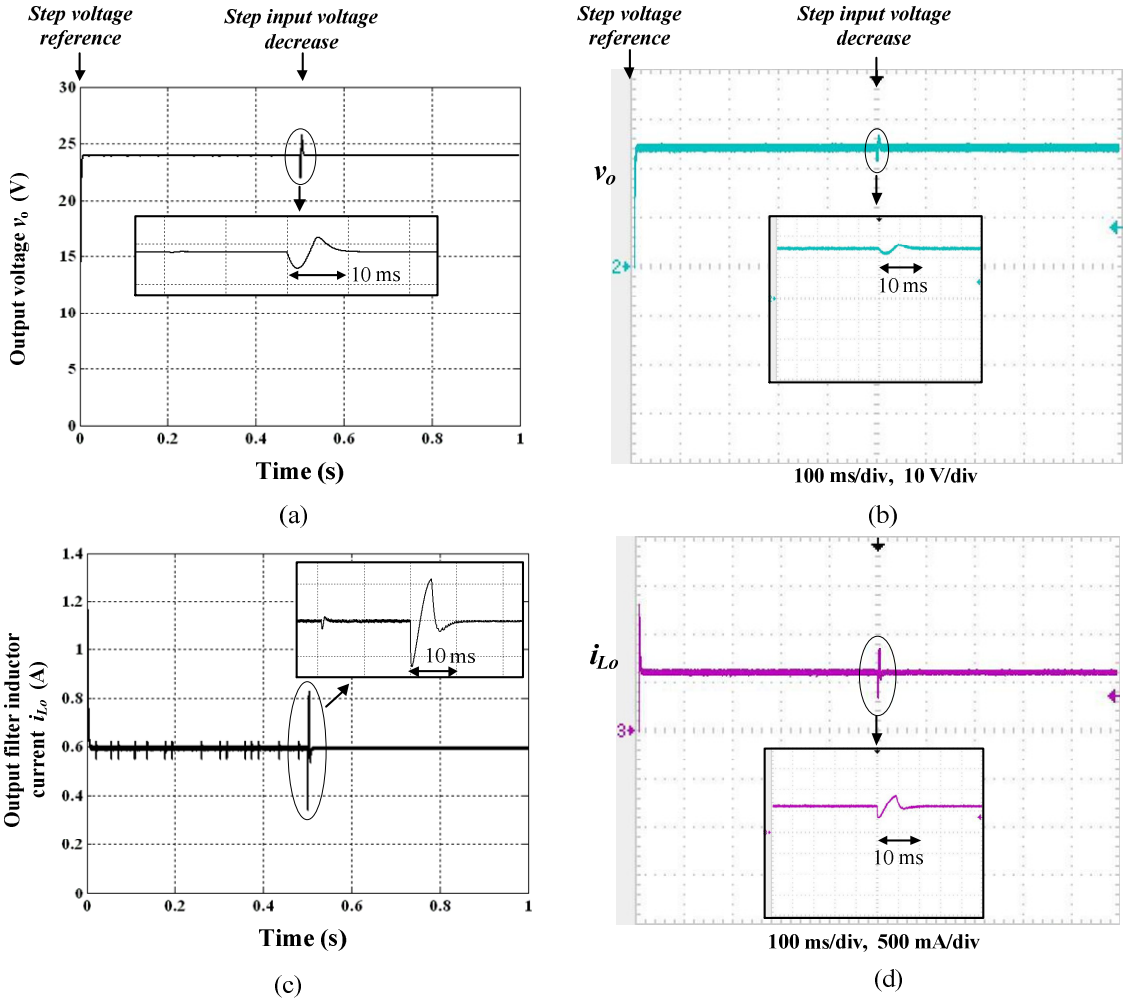
- The controller meets the desired time domain specifications at start up. The proposed SMC is robust to the full-load disturbance applied at t=0.5s and the output voltage recovers with a minor oscillatory behaviour over 10ms compared to only 1ms for the Lyapunov controller.
- The control variable v_c changes between v_{cmin}=0 (since m_1=0) and v_{cmax}=41.5 (since m_2=1.1) such that

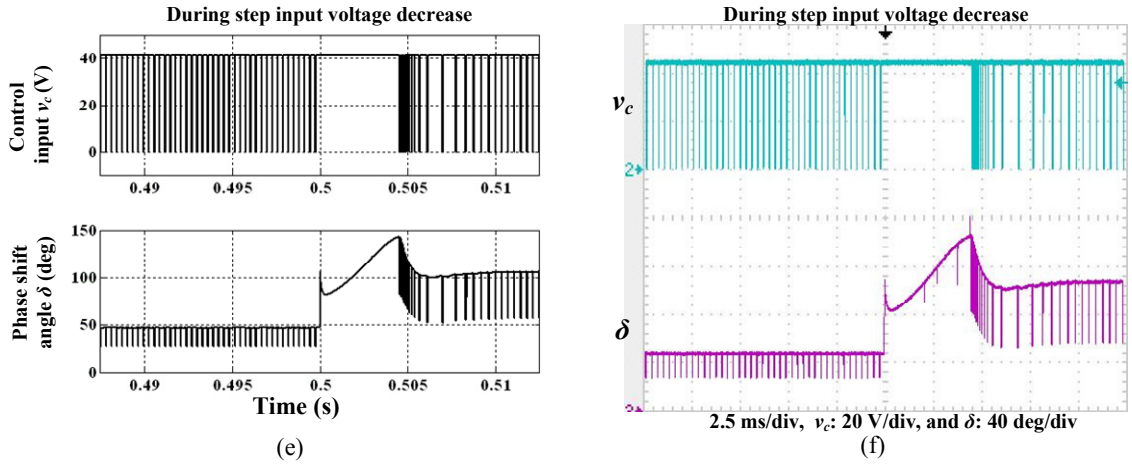
$$\begin{aligned} m_2 &> \left(1+\frac{r_{Lo}}{R_{L_{FL}}}=1+\frac{0.5}{14.4}=1.03\right) \\ v_{c_{\min}} &= m_1\frac{\pi}{2}v_o{}^*=0 \\ v_{c_{\max}} &= m_2\frac{\pi}{2}v_o{}^*=\frac{\pi}{2}(1.1)(24)=41.5 \end{aligned} \tag{5.59}$$

  Selection of m_1 and m_2 ensures a wide sliding domain bandwidth to enable closed-loop stability. However, further increase in m_2 would lead to saturation action which is inherent in the closed-loop due to δ_{max}=180°. This limits the upper boundary for the selection of m_2.

- The phase shift angle δ is calculated from the weighted state feedback linearization scheme. Since $\delta=f(v_c,i_{Lo})$ and v_c take two discrete values, δ takes the same response shape and time domain characteristics as that of the inductor current i_{Lo}. This is clear from the response of δ both at start-up and at the step load instant.

- δ is the inverter control variable and represents the effective duty cycle of the inverter output voltage. Therefore, it is essential that δ is not an abruptly changing variable like v_c to ensure stable and non-oscillatory behaviour of the resonant tank state variables. In this respect, the proposed SMC controller provides an advantage over discrete self-sustained SMC for the phase-controlled SPRC in [5.15]. The latter, instead, changes δ between two discrete values to achieve output voltage regulation.
- δ increases at the step load instant to enable regulation of output voltage to the fixed reference value v_o*=24V. During the first 6ms after step load application (t=0.5→0.506ms) v_c is held constant at v_{cmax} to compensate for the output voltage dip. Once the output voltage v_o overshoots above the reference value, control action allows v_c to toggle again between v_{cmin} and v_{cmax} to enable output voltage regulation.





(e) (f)

Fig. 5.19: Closed-loop operation results with step input voltage disturbance using the proposed sliding mode controller (a),(c)and (e) simulation, and (b),(d) and (f) experimental.

Fig. 5.19 shows the controller response to a step input voltage disturbance from full supply voltage (V_s=60V) to half supply voltage (V_s=30V) at t=0.5s, at fixed minimum load. The proposed SMC controller rejects the applied disturbance and the reference output voltage is re-gained after 10ms of disturbance application compared to only 1ms with the Lyapunov controller. The dynamic performance of the closed-loop system is inferior to that of the Lyapunov controller which rejects the disturbance quicker and with less oscillatory behaviour. The controller takes the necessary action after disturbance application by holding v_c at v_{cmax} from t=0.5→0.504ms to compensate for the voltage dip. The phase shift angle δ increases to maintain the output voltage constant.

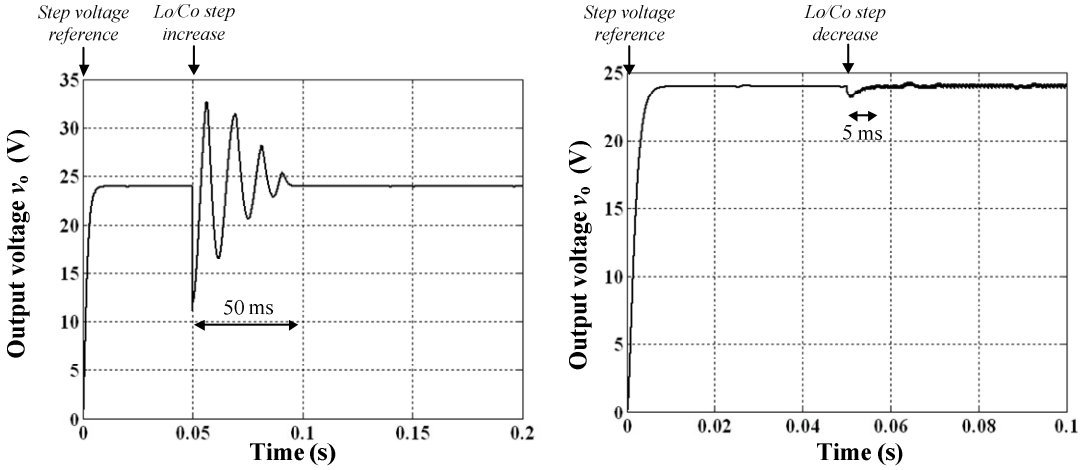
5.4.6 Controller robustness and parameter sensitivity

Similar to the Lyapunov controller robustness study, the effect on SMC performance of varying system parameters during operation is studied. Circuit parameters are subject to variation due to operational and environmental factors as discussed previously. For the proposed SMC, equilibrium point stability and existence inside the sliding domain is guaranteed by the condition outlined in (5.48)

$$m_1 < \left(1 + \frac{r_{Lo}}{R_L}\right) < m_2 \tag{5.60}$$

Therefore, if this condition is satisfied, an equilibrium point always exists in the sliding domain for all operational and circuit parameters. The sliding domain boundaries are parameter dependent (v_o^*, L_o, C_o, r_{Lo}), hence the boundaries move with parameter varia-

tion. As long as (5.60) is satisfied, an equilibrium point always exists and theoretically there exists no boundary on parameter variation. Only r_{Lo} affects condition (5.60), however, its effect is minor and it does not pull the system out of stability. This is why the sliding mode controller is known for its robustness as its main advantage. Fig. 5.20 shows the closed-loop output voltage response when applying the same parameter changes (L_o and C_o) as those for the Lyapunov controller in section 5.3.5.



(a) (b)

Fig. 5.20: Output voltage step response applying step changes in L_o and C_o
(a) ΔL_o=2pu and ΔC_o=2pu (b) ΔL_o=0.25pu and ΔC_o=0.25pu.

Fig. 5.20(a) shows the case when both L_o and C_o are doubled and in Fig. 5.20(b) when L_o and C_o are reduced to 25% of their original value. The sliding mode controller responds to both cases in a stable manner, restoring the reference value with zero steady-state error and minimum steady-state oscillation. In comparison with the Lyapunov controller, SMC provides a higher degree of robustness especially in the case of ΔL_o= ΔC_o=0.25 pu where the Lyapunov controller responds with increased steady-state oscillation and larger steady-state error. This confirms the robustness characteristics that SMC possess. However, this robustness is at the expense of a relatively poor dynamic performance. For SMC, the transient period oscillation in the first case (ΔL_o=ΔC_o=2 pu) are comparably higher and the settling time is longer (t_s=50ms) relative to the Lyapunov controller which responds more quickly (t_s=10ms) and with reduced oscillation. Therefore, for the system designer, if robustness is the main design criteria, the sliding mode controller would be the preferable choice. However, if the designer favours of good dynamic performance and robustness can be marginally sacrificed, then the Lyapunov controller would be better.

5.5 Proposed predictive controller

Predictive control is a common control algorithm in applications such as active power filters [5.31-32], PWM rectifiers [5.33], current control of PWM inverters [5.34-35], ac drives [5.36], and distributed generation systems [5.37]. Its application in the discrete time domain makes it suitable for DSP implementation. In addition, when a high switching frequency is used, it provides good static and dynamic performance.

Predictive control of the phase-controlled SPRC has not been previously investigated. This section details the design and analysis of a digital predictive controller making use of the high switching frequency implemented for resonant converters to obtain good closed-loop performance. The main objective is output voltage control. To achieve this, a two loop control system is designed with the outer loop performing output voltage regulation.

5.5.1 Controller design

The converter dynamic equations (5.1) can be expressed in discrete form as

$$v_c(k) = \frac{\pi}{2}\left(r_{Lo} i_{Lo}(k) + \frac{L_o}{T_s}\left(i_{Lo}(k+1) - i_{Lo}(k)\right) + v_o(k) \right) \tag{5.61}$$

$$i_{Co}(k) = i_{Lo}(k) - i_o(k) = \frac{C_o}{T_s}\left(v_o(k+1) - v_o(k)\right) \tag{5.62}$$

where T_s is the sampling (switching) frequency. Considering (5.62) and replacing $v_o(k+1)$ for $v_o^*(k+1)$ and $i_{Co}(k)$ for $i_{Co}^*(k)$, the output voltage loop can be constructed as:

$$i_{Co}^*(k) = k_1\left(v_o^*(k+1) - v_o(k)\right) \tag{5.63}$$

where k_1 is the voltage loop predictive gain designed to obtain fast and stable response.

With a high switching frequency (40 kHz), a change in load current $i_o(k)$ can be neglected compared to change in $i_{Lo}(k)$ and $i_{Co}(k)$, hence it is an acceptable approximation to state that

$$\begin{aligned} i_o(k) &= i_o(k+1) \\ i_{Lo}(k+1) - i_{Lo}(k) &= i_{Co}(k+1) - i_{Co}(k) \end{aligned} \tag{5.64}$$

Substituting for instant $(k+1)$ for k in (5.63) yields the modified outer voltage loop structure

$$i_{Co}^{*}(k+1) = k_1\left(v_o^{*}(k+2) - v_O(k+1)\right) \tag{5.65}$$

Equating $i_{Co}(k+1)$ to $i_{Co}^{*}(k+1)$ in equation (5.64) yields

$$i_{Co}^{*}(k+1) - i_{Co}(k) = i_{Lo}(k+1) - i_{Lo}(k) \tag{5.66}$$

Comparing (5.66) with (5.61) enables the construction of the inner current loop where the control input can be obtained

$$v_c(k) = k_2\left(i_{Co}^{*}(k+1) - i_{Co}(k)\right) + \frac{\pi}{2}\left(r_{Lo}i_{Lo}(k) + v_O(k)\right) \tag{5.67}$$

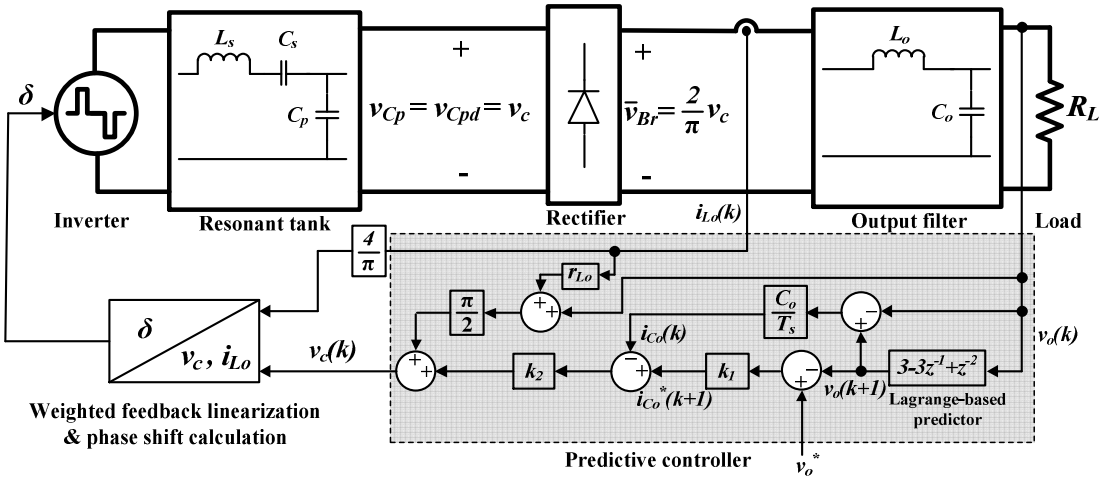
where k_2 is the inner current loop predictive gain. Equation (5.67) shows that $i_{Co}(k)$ has to be measured for inner current loop functionality. However, this is not a necessity since i_{Co} is proportional to the change in v_o. Output voltage $v_o(k)$ is measured and $v_o(k+1)$ is necessary for realisation of the outer voltage loop (5.65). The advanced sample $v_o(k+1)$ can be predicted using the second order Lagrange quadratic formula

$$v_O(k+1) = 3v_O(k) - 3v_O(k-1) + v_O(k-2) \tag{5.68}$$

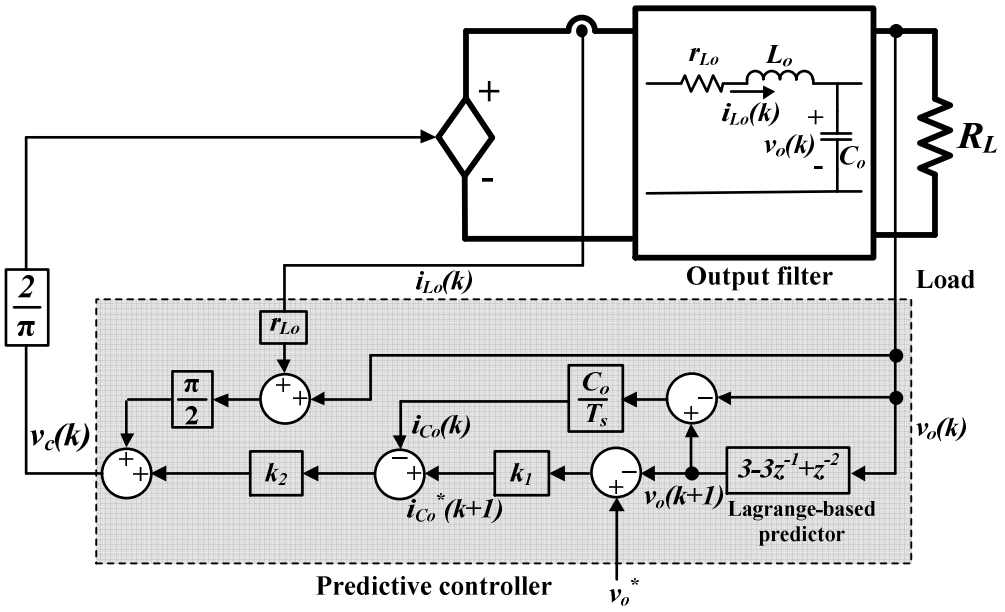
The predicted sample in advance $v_o(k+1)$ can be used to calculate $i_{Co}(k)$

$$i_{Co}(k) = \frac{C_O}{T_S}\left(v_O(k+1) - v_O(k)\right) \tag{5.69}$$

Therefore, $i_{Co}(k)$ for the inner current loop can be calculated using (5.69), with no need to sense it. Fig. 5.21 shows a schematic of the closed-loop structure using the proposed predictive controller.



(a)



(b)

Fig. 5.21: Closed-loop output voltage control using the proposed predictive controller (a) full structure and (b) reduced equivalent model.

5.5.2 Closed-loop stability

Considering the reduced system block diagram in Fig. 5.21(b), the closed-loop system transfer function in the discrete *z*-domain can be expressed as

$$\frac{V_o(z)}{V_o^*(z)} = \frac{\left(\frac{2}{\pi}k_1k_2{T_s}^2\right)z^2}{a_4z^4 + a_3z^3 + a_2z^2 + a_1z + a_0} \tag{5.70}$$

where $a_4 = L_oC_o$, $a_3 = -2L_oC_o$, $a_2 = L_oC_o + \frac{4}{\pi}k_2C_oT_s + \frac{6}{\pi}k_1k_2{T_s}^2$,

$a_1 = -\left(\frac{6}{\pi}k_2C_oT_s + \frac{6}{\pi}k_1k_2{T_s}^2\right)$ and $a_0 = \left(\frac{2}{\pi}k_2C_oT_s + \frac{2}{\pi}k_1k_2{T_s}^2\right)$.

Re-arranging the characteristic equation in (5.70) to take the form

$$1 + k_1GH(z) = 0 \tag{5.71}$$

The root locus for the open-loop transfer function *GH(z)* can be expressed as

$$GH(z) = \frac{\frac{2}{\pi}k_2{T_s}^2\left(3z^2 - 3z + 1\right)}{\left(L_oC_o\right)z^4 - \left(2L_oC_o\right)z^3 + \left(L_oC_o + \frac{4}{\pi}k_2C_oT_s\right)z^2 - \left(\frac{6}{\pi}k_2C_oT_s\right)z + \frac{2}{\pi}k_2C_oT_s} \tag{5.72}$$

In multi-loop control, the inner loop is faster than the outer loop; hence k_2 is selected to be greater than k_1. The outer loop is responsible for voltage regulation and overall closed-loop stability. Therefore, for a given inner loop controller gain k_2, the system root locus can be plotted to study the stability limit of the closed-loop system with respect to change in k_1. Fig. 5.22 shows the root loci for the closed-loop system with circuit values defined in Table 4.2 and a 40 kHz sampling frequency.

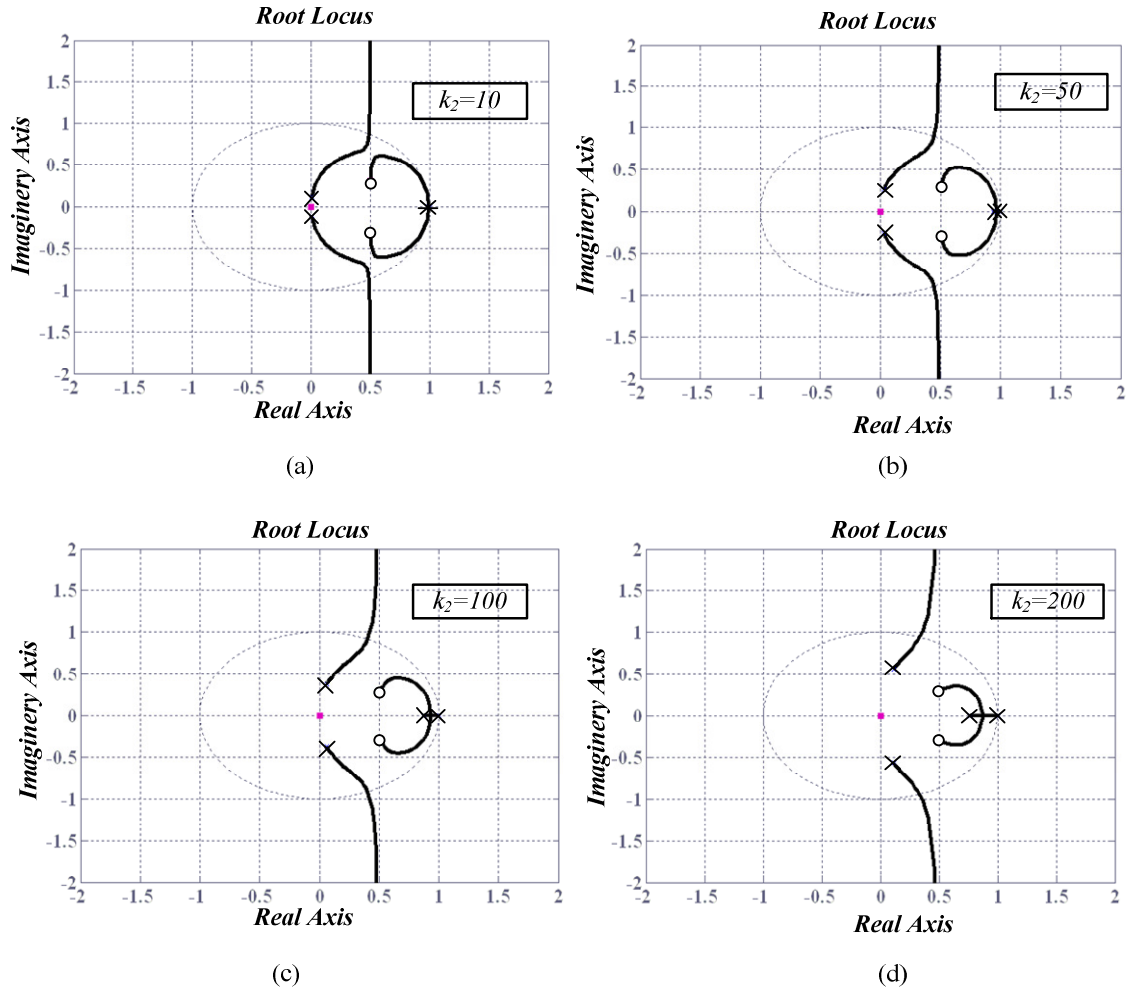


Fig. 5.22: Root loci for system with predictive controller (a) k_2=10, (b) k_2=50, (c) k_2=100, and (d) k_2=200.

Fig. 5.22 shows that the closed-loop system is more stable with smaller values of k_2. However, the inner loop dynamics are required to be faster, therefore the $k_1<k_2$ constraint would result in sluggish dynamic behaviour in the case of low gains; hence the trade-off between system speed of response and stability. In addition low gains generally result in poor controller disturbance rejection capability.

5.5.3 Simulation and experimental results

Fig. 5.23 shows output voltage results for the proposed predictive controller with controller gains k_1=0.24 and k_2=156. The same step load and step input voltage disturbances are applied as for the previous two controllers. The proposed predictive controller responds in a fast and robust manner to the applied disturbances. The dynamic behaviour is similar to the Lyapunov controller especially at start-up where steady-state is achieved after 4ms. The analogy in response is due to the proposed predictive controller implementing the same feedforward loop as the Lyapunov case and the equivalent sliding mode controller. Responses to the step load and step input voltage disturbances are robust with minimal oscillation and recovery to steady-state is after 2.5ms. This is slower than the Lyapunov controller which rejects the applied disturbances and restores the output voltage after 1ms.

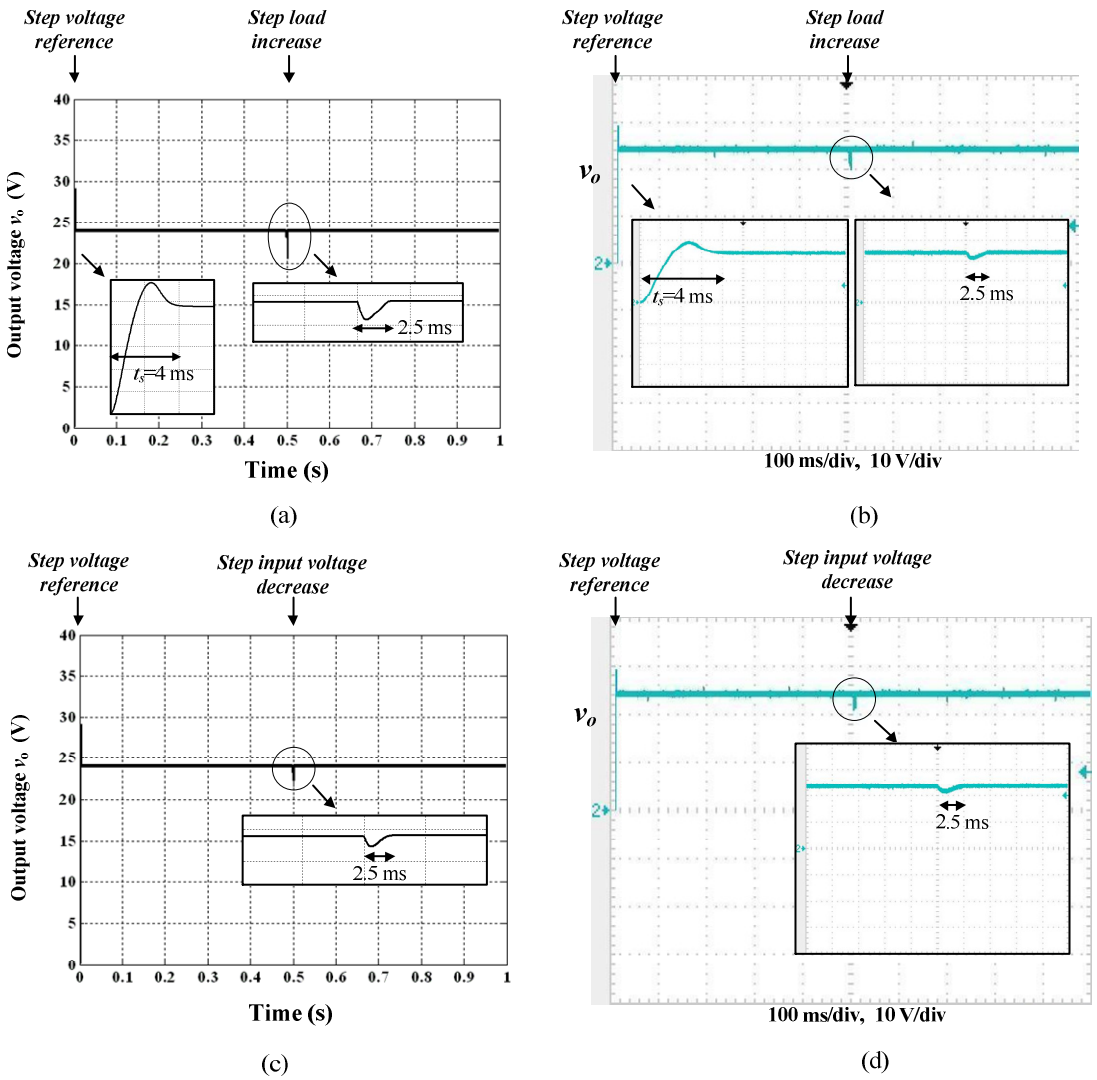


Fig. 5.23: Closed-loop output voltage results with step load and step input voltage disturbances using the proposed predictive controller (a) and (c) simulation, and (b) and (d) experimental.

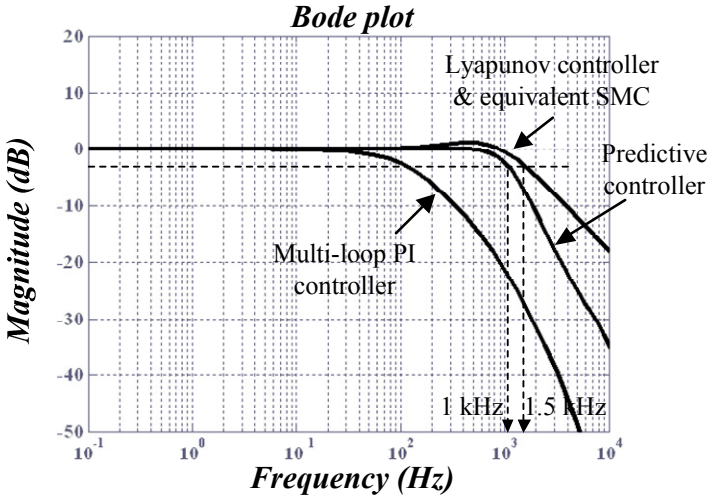


Fig. 5.24: Comparison of closed-loop bandwidth.

Fig. 5.24 shows a closed-loop bandwidth comparison for the proposed controllers. The bandwidth of the predictive controller is 1 kHz compared to 1.5 kHz for the Lyapunov controller. This explains its marginally slower dynamic performance and disturbance rejection capability. On the other hand, it has provided significant improvement to the multi-loop PI control with larger bandwidth and better dynamic performance.

5.5.4 Controller robustness and parameter sensitivity

It is apparent from the predictive control structure illustrated in Fig. 5.21 that the controller is parameter dependent, especially on the output capacitance C_o which can be seen as part of the inner current loop. Circuit parameters may vary during operation hence affecting the control which uses fixed values for these elements. Sensitivity to parameter variation is one of the main disadvantages of predictive control. Assuming per unit changes in converter filter inductance and capacitance values (ΔL_o and ΔC_o respectively), the closed-loop output voltage transfer function can be expressed as

$$\frac{V_O(z)}{V_O^*(z)} = \frac{\left(\frac{2}{\pi}k_1k_2{T_S}^2\right)z^2}{b_4z^4 + b_3z^3 + b_2z^2 + b_1z + b_0} \tag{5.73}$$

where $b_4 = (\Delta L_oL_o)(\Delta C_oC_o)$, $b_3 = -2(\Delta L_oL_o)(\Delta C_oC_o)$, $b_2 = (\Delta L_oL_o)(\Delta C_oC_o) + \frac{4}{\pi}k_2C_oT_S + \frac{6}{\pi}k_1k_2{T_S}^2$, $b_1 = -\left(\frac{6}{\pi}k_2C_oT_S + \frac{6}{\pi}k_1k_2{T_S}^2\right)$ and $b_0 = \left(\frac{2}{\pi}k_2C_oT_S + \frac{2}{\pi}k_1k_2{T_S}^2\right)$.

The characteristic equation can be re-arranged to study the effect of each parameter variation separately. Starting with ΔC_o while ΔL_o=1

$$1 + \Delta C_o GH(z) = 0 \tag{5.74}$$

$$GH(z) = \frac{L_o C_o z^2 (z-1)^2}{\left(\frac{4}{\pi} k_2 C_o T_S + \frac{6}{\pi} k_1 k_2 T_S^2\right) z^2 - \left(\frac{6}{\pi} k_2 C_o T_S + \frac{6}{\pi} k_1 k_2 T_S^2\right) z + \left(\frac{2}{\pi} k_2 C_o T_S + \frac{2}{\pi} k_1 k_2 T_S^2\right)} \tag{5.75}$$

Repeating for ΔL_o while ΔC_o=1 yields the same open-loop transfer function in (5.75). *GH(z)* is illustrated in Fig. 5.25 for the same operational parameters used for the simulation and experimental results in section 5.4.5. The root locus plot shows that there exists a minimum value for the operational change in inductance and capacitance (ΔL_{omin} and ΔC_{omin} respectively) to maintain a stable closed-loop response. In this case the minimum value for both is 0.3 per unit. Fig. 5.26 shows output voltage response when applying the same step changes in parameter values (L_o and C_o) as for the previous controllers.

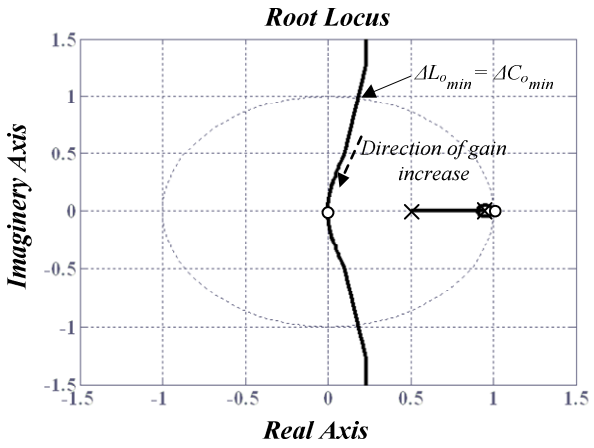
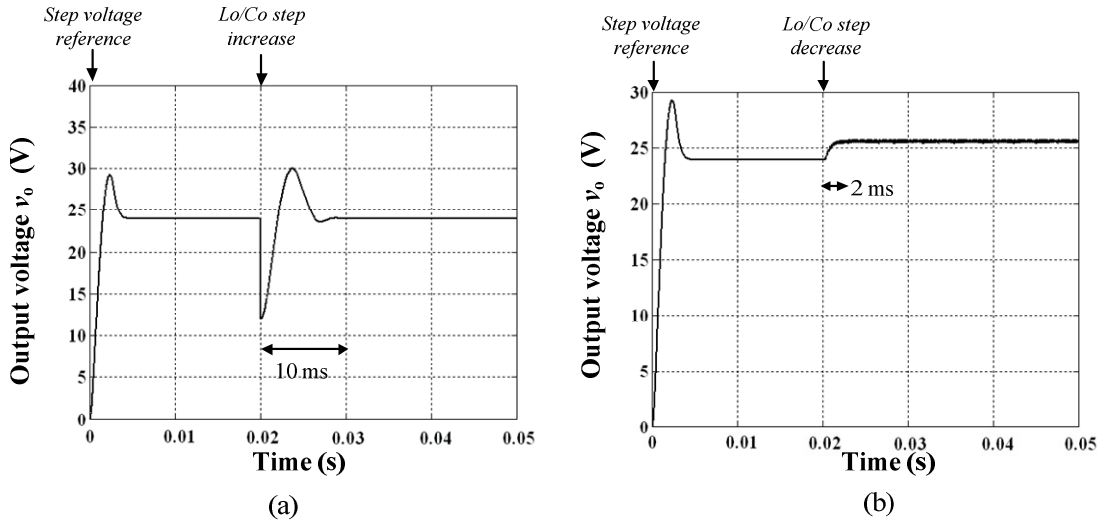


Fig. 5.25: Root locus for system with circuit parameter change.



(a) (b)

Fig. 5.26: Output voltage step response applying step changes in L_o and C_o
(a) ΔL_o=2pu and ΔC_o=2pu (b) ΔL_o=0.25pu and ΔC_o=0.25pu.

Fig. 5.26(a) shows that the closed-loop response is stable when doubling L_o and C_o. However, when reducing L_o and C_o to 0.25p.u., the closed-loop response becomes marginally stable with high frequency oscillation at steady-state in addition to the introduction of a steady-state error. The critically stable minimum per unit change deduced from Fig. 5.25 is 0.3p.u. However, it can be seen that with 0.25p.u. values, closed-loop response is close to instability. This is because the 0.3p.u. value was obtained from the closed-loop transfer function at no load. The presence of load, being the case with the results in Fig. 5.26, provides system damping and thus margin of stability is extended.

Table 5.2 summarizes the key features of the three proposed robust controllers. In terms of implementation complexity and necessary measurements for control realisation, the three proposed controllers are analogous. Measurements of output voltage and filter inductor current are taken and DSP coding performs the required controller algorithm. This makes Table 5.2 sufficient to enable a fair comparison of the controller methods.

	Lyapunov controller	***Sliding Mode Controller***	***Predictive Controller***
Feedforward implementation	Yes	Not directly, but inherently exists in equivalent control circuit	Yes
Control structure	Single loop PD control	Sliding surface implements single loop PID control	Two loop control
Response at startup	Fast	Relatively slower due to stability constrains	Fast
Disturbance rejection	Fast and stable	Slowest with more oscillations but stable	Moderate speed and stable
Robustness & parameter sensitivity	Moderate	High	Moderate
Closed-loop bandwidth	High	High	Moderate

Table 5.2: Comparison between the three proposed robust controllers.

5.6 Summary

In this chapter three new controllers have been proposed for robust control of the phase-controlled SPRC; namely Lyapunov, sliding mode and predictive controllers. Control law formulation, design, stability and robustness analysis were presented and verified through closely matching simulation and experimental results. The derived control laws

are second order derivative functions; a common feature of all the proposed controllers in spite of their different structures. It has been shown that another necessary requirement to ensure robust behaviour of the closed-loop system, is the existence of a feed forward loop in the control law. This is either explicit as with Lyapunov and predictive controllers or inherent as in the equivalent SMC. The Lyapunov controller provides the best overall performance with its fast dynamic response at start-up and high disturbance rejection capability. Chattering and reduced sliding domain bandwidth for the SMC with high controller gains both reduce controller stability margins. Therefore dynamic response is comparably slower than the Lyapunov and predictive controllers to ensure stable closed-loop operation. The predictive controller provided fast dynamic behaviour similar to the Lyapunov controller. However, its closed-loop bandwidth (1 kHz) is lower than that of the Lyapunov controller (1.5 kHz). Its discrete time domain nature makes it suited to digital control implementation. In terms of robustness of the closed-loop system to operational circuit parameter variations, SMC is the best among the proposed controllers. According to design requirements and application, the trade-off between high system robustness and fast dynamic response determines controller type selection.

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Chapter 6

Phase-Controlled SPRC Multi-module Operation

In chapter three, the load side multi-module converter structure for the *All-Electric* subsea project was designed. It consisted of phase-controlled SPRCs connected in an input-series (IS) connection for medium dc voltage step down. Output-series (OS) and output-parallel (OP) connections were used to attain the output voltage level and load current sharing respectively.

This chapter explores phase-controlled SPRC multi-module system operation aspects that have not been investigated in the literature. Associated voltage and current distribution among the series-parallel modules are considered. Focus is on the ISOP and ISOS converter connections which are applicable to the load side converter of the subsea project under investigation. Accordingly, the voltage/current distribution studies include input voltage sharing (IVS), output voltage sharing (OVS) and output current sharing (OCS) for IS, OS and OP connections respectively. The Lyapunov controller proposed in chapter five is used as the main load voltage regulator together with the necessary sharing control loops. Closed-loop behaviour is assessed for both ISOP and ISOS connections taking into account cables impedance effects. A sensorless load voltage estimation algorithm is proposed. This is potentially useful for the subsea project to enable load voltage control without remote sensing. Simulations and experiments on a two-module converter system operating with extreme parameter mismatches, validate sharing and load regulation performance.

6.1 Background

Multi-module low power dc/dc converters connected in series-parallel have been a key technology for large-capacity power converters. The modular approach offers a number of advantages over a single, high power, centralized converter. In terms of performance, the advantages include higher efficiency, better dynamic response due to higher operating frequency, and better load regulation. From the system perspective, it allows for redundancy implementation hence improved fault tolerance, expandability and ease of maintenance [6.1]. Also, since individual converter modules handle lower power, component stresses are reduced [6.2].

However, realisation of multi-module series-parallel converter systems is not always straight forward. A desirable characteristic of a series-parallel modular converter is that individual modules share the load equally and in a stable manner. Modules are usually non-identical due to finite tolerances in the power stage and control parameters, non-identical characteristics of the cables, and non-identical changes in component characteristics due to differences in component aging and environmental conditions. If special provisions are not made to distribute voltages and currents equally among the series-parallel modules, then it is possible that modules with an excessive power share will experience higher thermal stresses, and both modularity and system reliability degrade [6.3,4]. In order to achieve the appropriate sharing, a variety of approaches, with different complexities and performance outcomes, have been proposed, developed and analysed in the literature [6.5]. Fig. 6.1 shows a structural chart with the classification of sharing schemes broadly divided into droop and active sharing methods.

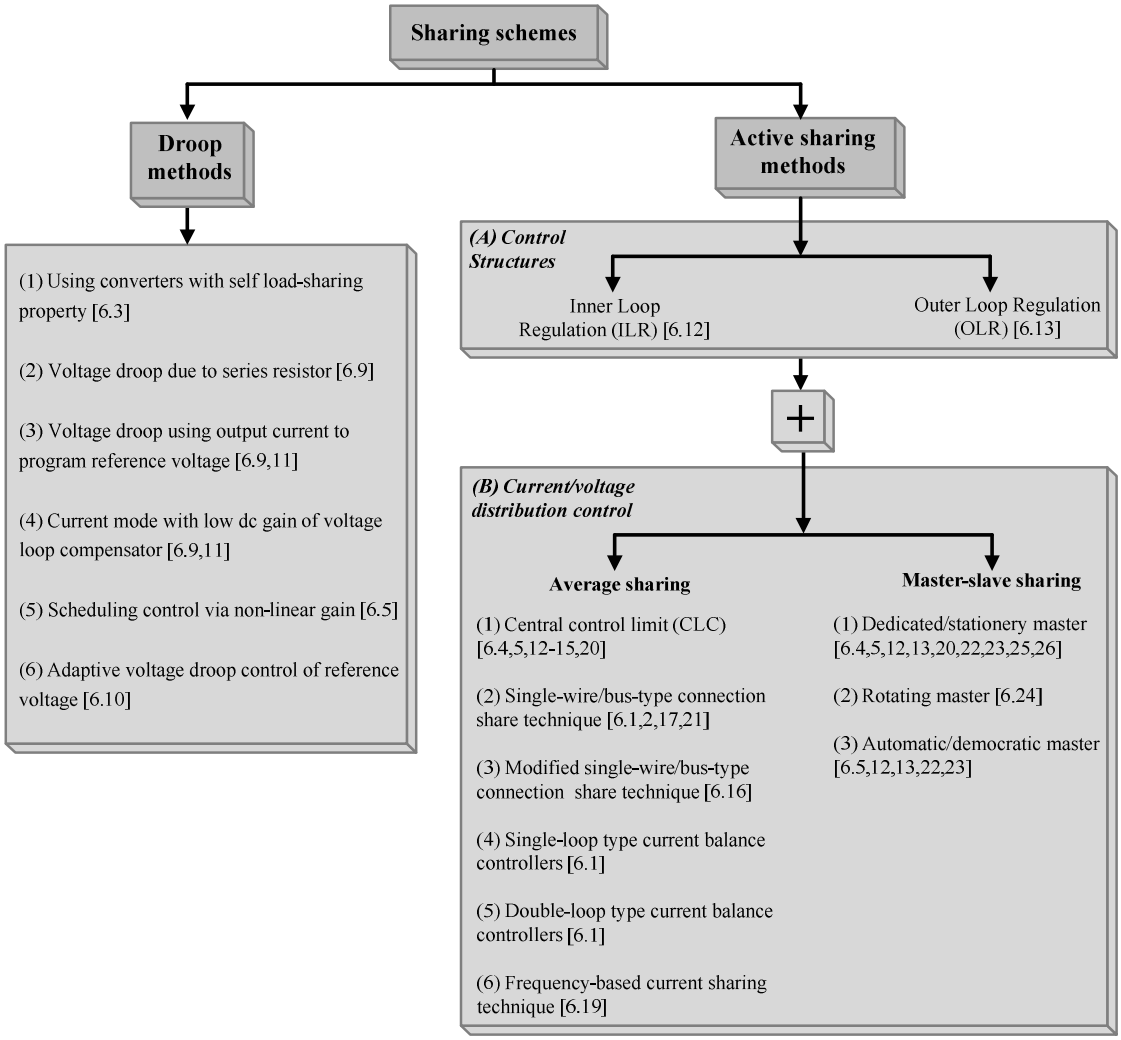
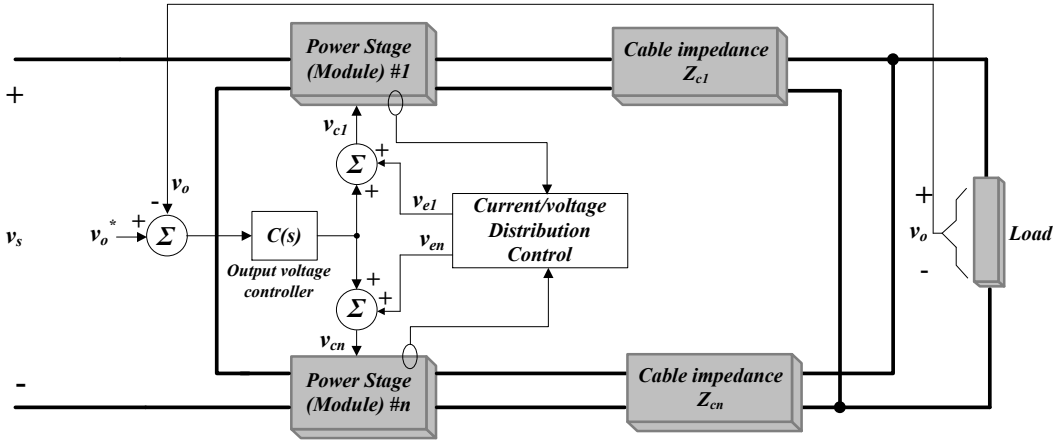


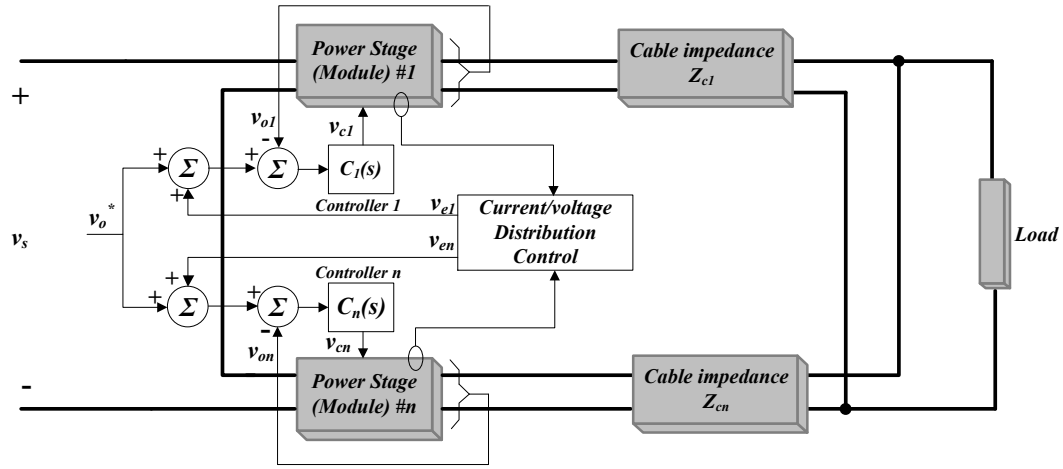
Fig. 6.1: Classification of sharing schemes for series-parallel dc/dc converters

With the droop methods, the output voltage droops with increasing load current [6.6]. Droop sharing adds virtual output impedance to the outputs of the individual converter modules. This impedance is implemented in the droop controller and is programmed to achieve equal sharing among modules [6.7]. The main advantage of a droop sharing scheme is that it needs no wire interconnections among the control circuits of the converter modules. Therefore, it is considered an open-loop technique with the output impedance of each module being programmed individually [6.8]. The main drawback of droop techniques is the trade-off between good voltage regulation and current sharing. Several droop schemes as outlined in Fig. 6.1 have been proposed in the literature to overcome the drawbacks and to give good current sharing [6.3,6-11].

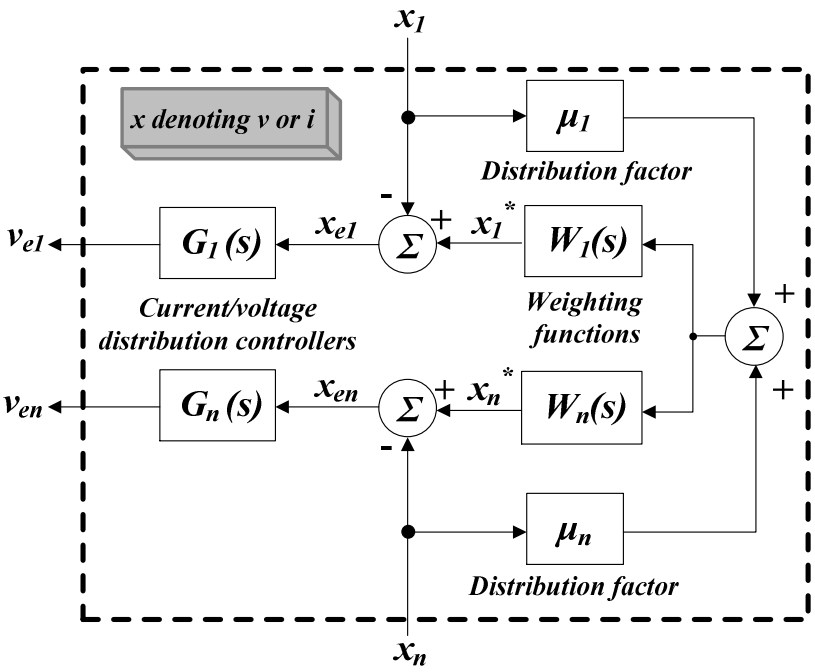
An active sharing method is a combination of a control structure and a current/voltage distribution control scheme as presented in Fig. 6.1. Fig. 6.2 illustrates how a current/voltage distribution scheme can be connected in different control structures.



(a)



(b)



(c)

Fig. 6.2: (a) Inner loop regulation (ILR) control structure, (b) outer loop regulation (OLR) control structure and (c) current/voltage distribution control

If the error signals v_{e1} to v_{en} of the current/voltage distribution control adjust the output of the output voltage controller, then the resulting control structure is termed an inner loop regulator (ILR) as shown in Fig. 6.2(a). The adjusted control signals v_{c1} to v_{cn} produce the desired current/voltage sharing. The main advantage of an ILR is the precise output voltage regulation due to a fixed reference voltage. Current/voltage sharing dynamics are not affected by the outer voltage loop since the distribution control error signals do not pass through the output voltage controller. This ensures stable and fast sharing [6.12]. If the distribution control adjusts the output voltage reference value then outer loop regulation (OLR) is achieved as depicted in Fig. 6.2(b). Compared to ILR, the dynamic voltage reference means that good current/voltage sharing may be at the expense of load regulation. Also, sharing performance is affected by the dynamics of the outer voltage loop since the distribution control error passes through the output voltage controller. This may lead to transient stability problems [6.13]. On the other hand, OLR satisfies system modularity, fault tolerance and standardization more than ILR due to individual control of each converter module. Risk of single-point failure is higher with ILR due to regulation of the load voltage rather than individual module output voltages. However, this is not a major argument from this chapter's perspective since a single central DSP controller is used for the entire sharing and load regulation task.

Fig. 6.2(c) shows a unified block diagram that describes the current/voltage distribution control. The latter communicates with all the converter modules to acquire the sharing error signal of each module which further adjusts the voltage controller output to obtain the desired sharing characteristics [6.14]. The reference signal for each module x_i^* is generated by manipulation through distribution factors μ_1 to μ_n and weighting functions $W_1(s)$ to $W_n(s)$. These can be defined, for n modules, according to whether average or master-slave distribution control techniques are applied:

- Average active sharing: $\mu_1=\ldots=\mu_n=1$ and $W_1(s)=\ldots W_n(s)=1/n$.
- Master-slave active sharing: $\mu_{master}=1$, $\mu_{slaves}=0$ and $W_1(s)=\ldots W_n(s)=1$.

The error signal x_{ei} is finally processed through the current/voltage distribution controller $G_i(s)$ to produce the final error v_{ei} which adjusts the power stage control signal v_{ci} to ensure sharing.

Both average and master-slave methods are well established active sharing techniques for dc/dc converters connected in series-parallel. Generally, average sharing methods are relatively more stable and have precise sharing [6.12-21]. This is because in master-slave control, the master module is responsible for load regulation while the slaves are devoted to equalizing current/voltage distribution. This means that there is no control over the master converter module current/voltage which causes poor transient sharing. This problem does not arise in the average sharing scheme [6.22,23]. Also, with interleaved converter module operation, the summation of currents/voltages carried out with average distribution control leads to ripple cancelation, hence smoother reference currents/voltages are generated without the need for filtering. With master-slave distribution control, the current/voltage of the master module is taken as the only reference for the remaining modules. This may cause poor transient sharing especially when modules are interleaved since currents/voltages are instantaneously unequal. On the other hand, the master-slave technique generally provides better fault tolerant operation, since in the case of master module failure, the converter with the next highest current/voltage becomes the master. In addition, the master-slave technique gives more information for fault detection. This is because one module is responsible for load voltage regulation and the remaining are devoted to equalized sharing. Therefore, fault tracking is easier than with average sharing where all converter modules play the same role [6.24-26].

6.2 Control of input-series connected converters

Control of multi-module input-series connected dc/dc converters has been the subject of vigorous research in the past. Two categories of input-series connected converters exist; the ISOP and ISOS configurations.

6.2.1 ISOP connection

For ISOP systems, several control schemes have been proposed for input voltage sharing (IVS) or output current sharing (OCS). With common duty ratio control, stable operation for an ISOP configuration can be achieved [6.27,28]. However, good IVS and OCS can only be obtained for modules with identical parameters. Charge control with input voltage feedforward is applicable to ISOP connected converters [6.29]. Nevertheless, individual module input currents and voltages have to be sensed. A controller based on a sensorless current-mode approach was also proposed for ISOP converters [6.30]. A master/slave control scheme with input current feedforward can achieve IVS, but with this control technique, the system may fail once the master module malfunctions [6.31]. Double-loop control implemented with one common output voltage regulation (OVR) loop and a uniform voltage distribution scheme [6.32-34], the decoupling IVS control scheme [6.35-37], and the general control considerations [6.38] achieve excellent IVS for the ISOP configuration. The double-loop scheme depends on the fact that direct OCS of ISOP converters leads to a runaway condition and IVS is a necessity to ensure stable operation in the case of module parameter mismatches. With only IVS, OCS is achieved automatically for ISOP configurations without the need for dedicated OCS loops. Nevertheless, a three-loop control scheme was implemented in [6.39,40] with sensing module input voltages and output currents to operate with current-mode control. The authors in [6.41,42] proposed cross feedback OCS control to achieve stable and accurate independent OCS in ISOP systems with no need for IVS loops. However the analysis and implementation are complex.

6.2.2 ISOS connection

For ISOS systems, common duty ratio control results in unstable operation, unlike in ISOP systems [6.43]. Investigation of the ideal ISOS configuration reveals weak rebalancing so long as different cells operate with interleaved switching signals [6.44]. Like ISOP systems, independent output voltage sharing (OVS) of ISOS systems leads to

a runaway condition. IVS is a necessity to obtain stable operation in the case of module parameter mismatches. In [6.36], the authors proposed a double-loop scheme with outer voltage regulation and IVS loops. This leads automatically to OVS. However, the authors in [6.45] proposed a duty cycle exchanging control scheme where stable OVS can be achieved without IVS loops. Three loop control schemes with IVS loops and current-mode programming have also been introduced in [6.43].

6.2.3 Common properties

The common feature revealed for both ISOP and ISOS systems in [6.35-37] is the indispensability of IVS control. Fig. 6.3 illustrates what happens in an ISOP connected system with no IVS even in the presence of OCS control.

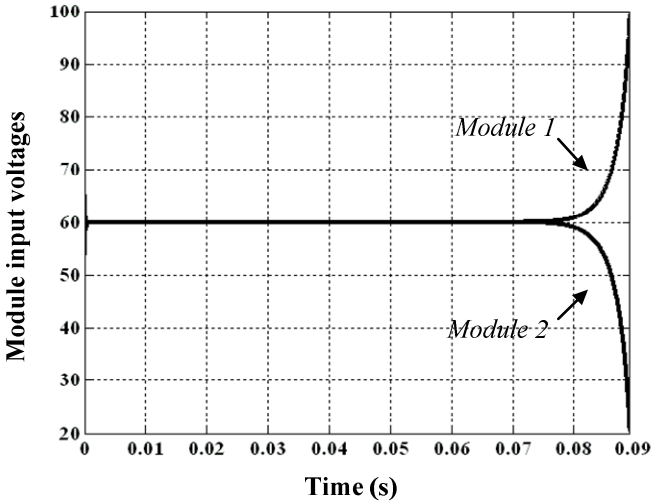


Fig. 6.3: Diverging module input voltages in an ISOP connected system with OCS and no IVS control.

With OCS the ISOP connected converters act as constant power sinks, with constant output voltage and equally shared output currents. This means that any input disturbance results in an inversely proportional current-voltage relationship, which is outlined by the negative input incremental resistance of the converter [6.39,46]. An increase in input voltage results in a decrease in the average input current to maintain the input power equal to the output power (assuming lossless conversion). This leads to a further increase in the input voltage, leading to the runaway condition illustrated in Fig. 6.3. Therefore, a dedicated input voltage control loop which adjusts the duty ratios of individual converter modules depending on the error in IVS, is required. OCS is automatically achieved for ISOP systems without dedicated control if IVS control is applied. Similarly, OVS is achieved for ISOS systems with IVS control.

6.3 Proposed multi-module system architecture

The proposed phase-controlled SPRC multi-module load side converter of the subsea project involves connecting the converter modules in ISOP and ISOS connections. A two-module converter system will be used to study each connection separately.

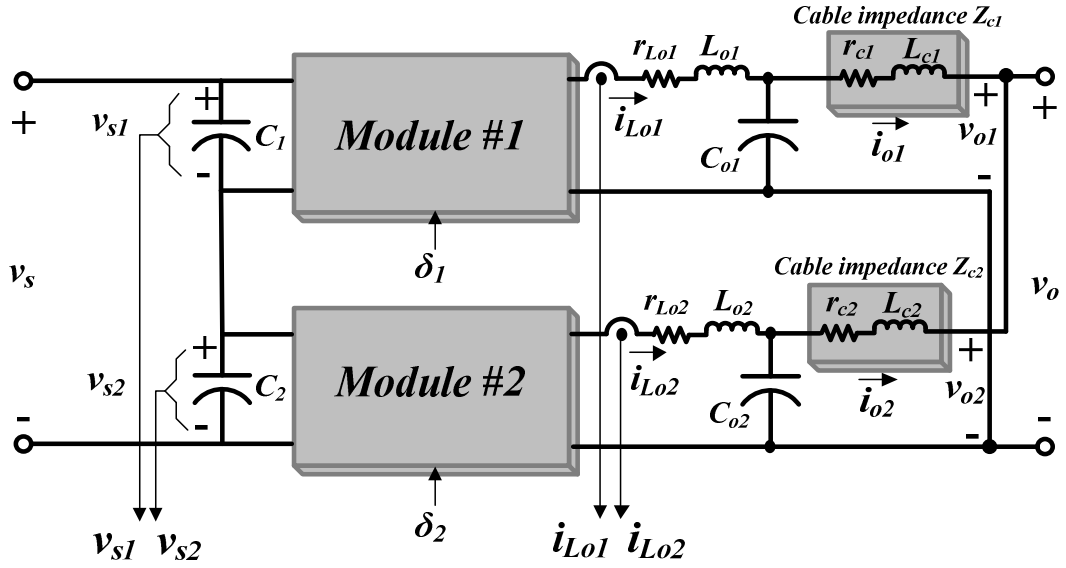
6.3.1 Control structure

Fig. 6.4(a) and (b) illustrate the two-module system in ISOP and ISOS connections. The common control configuration for both connections shown in Fig. 6.4(c) comprises a common outer voltage loop for load voltage regulation using the Lyapunov controller proposed in chapter five which provided fast, stable and robust output voltage control. Load voltage for the outer loop is not sensed but estimated using a proposed algorithm for sensorless load voltage control. Details of this algorithm are given in section 6.3.2. Output of the common PD Lyapunov controller is fed to the feedforward mechanism of each module. The latter utilises measurements of individual module filter inductor currents i_{Lo1} and i_{Lo2} together with estimated module output voltages $\hat{v}_{o1}$ and $\hat{v}_{o2}$.

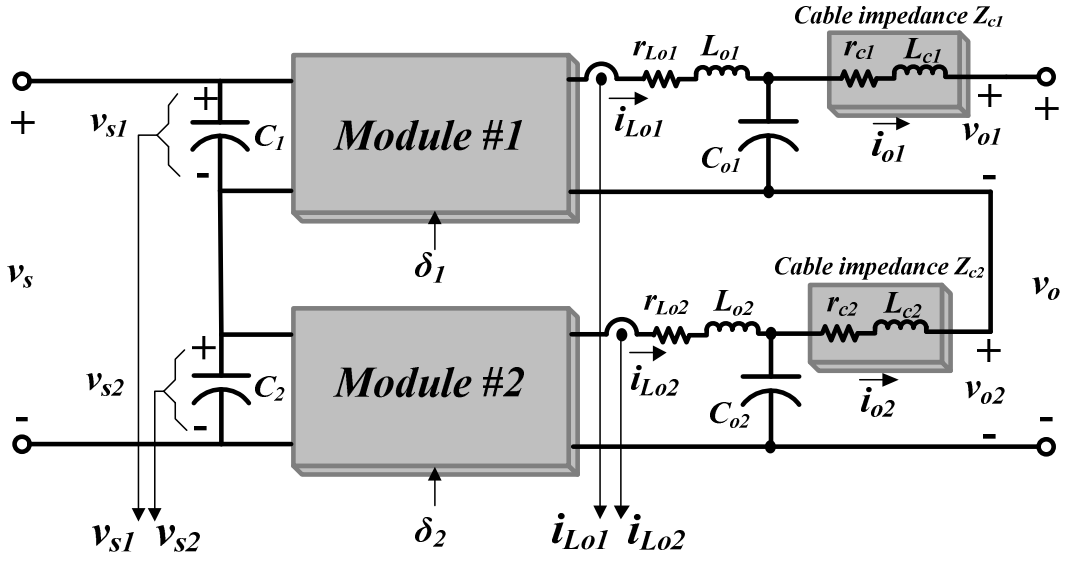
Because of the necessity of IVS, as discussed in section 6.2, the sharing loop will simply consist of an average IVS loop. Individual module input voltages v_{s1} and v_{s2} are sensed and average sharing is used to produce correcting error signals v_{e1} and v_{e2} which adjust the outputs of the load voltage Lyapunov controller accordingly to produce the control signals v_{c1} and v_{c2}. No additional OCS or OVS loops will be implemented. Average sharing is implemented as assumed with the master-slave technique since the converter modules are operated in an interleaved mode. Averaging measured signals produces a smoother ripple-free reference. However, if the master module provides the reference for the other module to follow, this may lead to poor transient sharing since interleaved voltages are instantaneously unequal. Inner loop regulation (ILR) is used due to its precise and stable load regulation compared with outer loop regulation (OLR) which uses a dynamic output voltage reference. Unlike OLR, with ILR the current/voltage distribution control loop is stable since it does not pass through the outer voltage loop. This provides decoupled control, and sharing behaviour is independent and fast. A central DSP controller will be used to process all the measured signals and will act as the main controller for both modules. Therefore, the better modularity that

OLR offers due to sensing individual module output voltages is not an important argument here.

Fig. 6.4(d) and (e) illustrate the reduced equivalent control circuit for ISOP and ISOS connections respectively. It has been shown in chapters four and five that using the state feedback linearization scheme causes the converter model to reduce to a second order circuit with the input voltage to the output filter circuit being proportional to the control signal v_c. The transformer illustrated in Fig. 6.4(d) and (e) represents the converter input-output voltage-current relationship.



(a)



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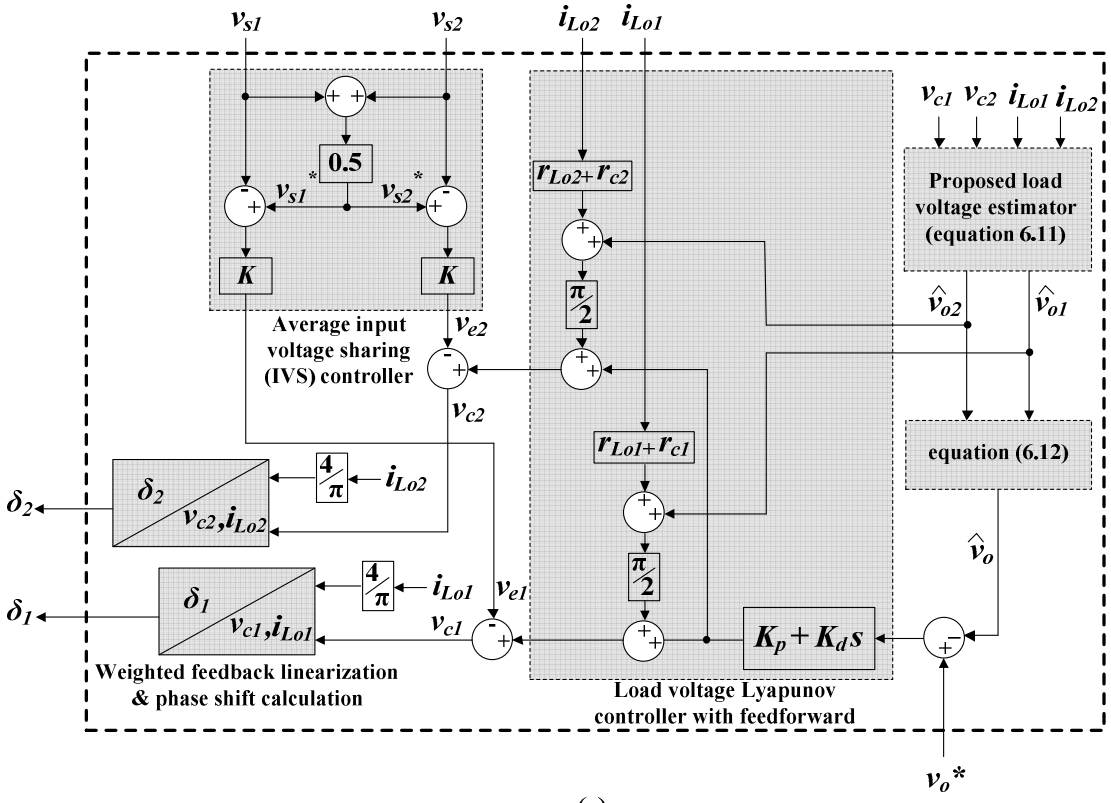

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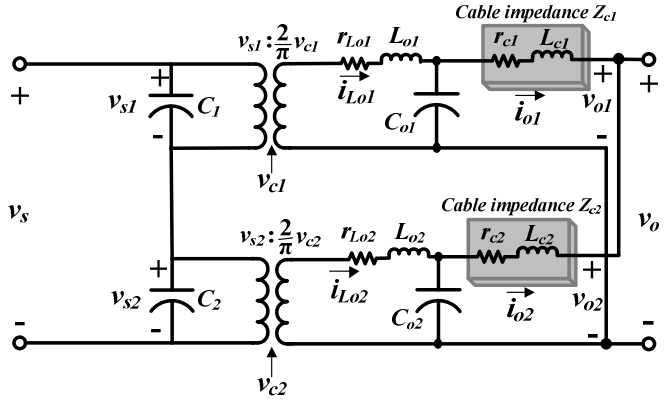
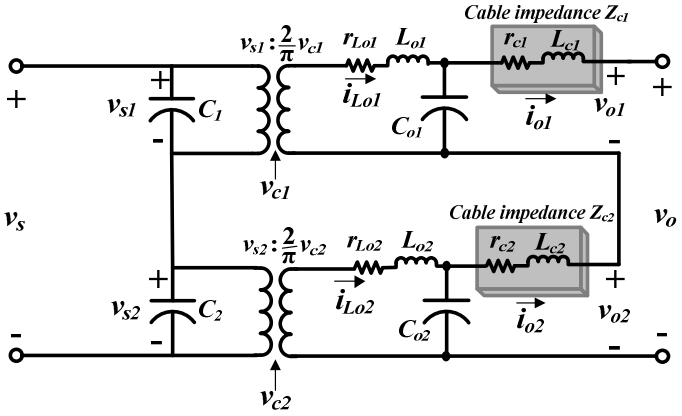


(d)



(e)

Fig. 6.4: Proposed two-module phase-controlled SPRC (a) ISOP connection, (b) ISOS connection, (c) common control structure for both connections, (d) reduced equivalent control circuit for ISOP connection, and (e) reduced equivalent control circuit for ISOS connection.

6.3.2 Sensorless remote output voltage control algorithm

The load voltage can be estimated, to perform sensorless load voltage control. This is particularly attractive in the subsea project since the load may be remotely located at a number of distant manifolds from the main converter site. This eliminates the need for remote sensing of load voltage and hence long signal cables, being a cause of noisy measurements, can be removed. Moreover, with the implementation of this algorithm and elimination of load voltage sensing, true system modularity can be achieved if dedicated DSP controllers are used to control each converter module. Measuring the common load voltage with the ILR technique rather than individual module output voltages, represents a major modularity drawback. The proposed load voltage estimator eliminates such a drawback.

The estimation scheme uses the *two-port network* methodology. Fig. 6.5 shows the equivalent circuit diagrams of the ISOP and ISOS connected two-module converter systems.

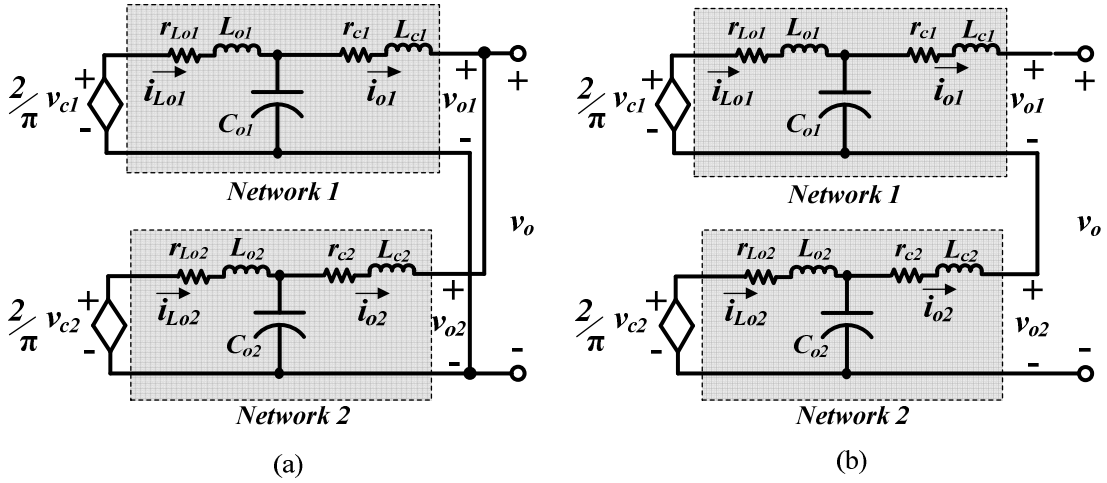


Fig. 6.5: Equivalent control circuit diagrams for (a) ISOP and (b) ISOS systems.

With the sending end voltage and current known, in addition to circuit parameter values, the receiving (load) end voltages and currents can be calculated. In terms of the *two-port networks*, this can be formulated as follows

$$\begin{bmatrix} \hat{v}_{o1} \\ \hat{i}_{o1} \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} \frac{2}{\pi} v_{c1} \\ i_{Lo1} \end{bmatrix} \tag{6.1}$$

$$\begin{bmatrix} \hat{v}_{o2} \\ \hat{i}_{o2} \end{bmatrix} = \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \begin{bmatrix} \frac{2}{\pi} v_{c2} \\ i_{Lo2} \end{bmatrix} \tag{6.2}$$

where

- v_{c1} and v_{c2} are the adjusted outputs of the load voltage controller,
- i_{Lo1} and i_{Lo2} are measured inductor filter currents, and
- ABCD are circuit parameter dependent coefficients.

In the case of ISOP systems, load voltage v_o is equal to individual module output voltages v_{o1} and v_{o2}, that is, $v_o=v_{o1}=v_{o2}$. Therefore estimated load voltage $\hat{v}_o$ can be obtained by averaging individual module output estimates $\hat{v}_{o1}$ and $\hat{v}_{o2}$

$$\hat{v}_o = \frac{\hat{v}_{o1} + \hat{v}_{o2}}{2} \tag{6.3}$$

In the case of ISOS systems, load voltage $\hat{v}_o$ is the summation of individual module output voltage estimates $\hat{v}_{o1}$ and $\hat{v}_{o2}$

$$\hat{v}_o = \hat{v}_{o1} + \hat{v}_{o2} \tag{6.4}$$

Using two-port network theory, coefficients can be derived and defined in the continuous time domain as follows

$$\begin{aligned}
A_1(s) &= (L_{c1}C_{o1})s^2 + (r_{c1}C_{o1})s + 1 \\
B_1(s) &= -\left((L_{o1}L_{c1}C_{o1})s^3 + (r_{c1}L_{o1}C_{o1} + r_{Lo1}L_{c1}C_{o1})s^2 + (L_{c1} + L_{o1} + r_{Lo1}r_{c1}C_{o1})s + (r_{Lo1} + r_{c1})\right) \\
C_1(s) &= -C_{o1}s \\
D_1(s) &= (L_{o1}C_{o1})s^2 + (r_{Lo1}C_{o1})s + 1 \\
A_2(s) &= (L_{c2}C_{o2})s^2 + (r_{c2}C_{o2})s + 1 \\
B_2(s) &= -\left((L_{o2}L_{c2}C_{o2})s^3 + (r_{c2}L_{o2}C_{o2} + r_{Lo2}L_{c2}C_{o2})s^2 + (L_{c2} + L_{o2} + r_{Lo2}r_{c2}C_{o2})s + (r_{Lo2} + r_{c2})\right) \\
C_2(s) &= -C_{o2}s \\
D_2(s) &= (L_{o2}C_{o2})s^2 + (r_{Lo2}C_{o2})s + 1
\end{aligned} \tag{6.5}$$

However, since control is implemented using a DSP controller, the load voltage estimator has to be in discrete time domain form. Only A_1, B_1, A_2 and B_2 are necessary for load

voltage calculation. These can be discretized using Euler backward method $\left(s \to \frac{z-1}{T_s z}\right)$, where T_s is the DSP sampling period, yielding

$$
\begin{aligned}
&A_1(z) = A_{11}z^{-2} + A_{12}z^{-1} + A_{13} \\
&\quad A_{11} = \frac{L_{c1}C_{o1}}{{T_s}^2}, \quad A_{12} = -\frac{2L_{c1}C_{o1} + T_s r_{c1}C_{o1}}{{T_s}^2}, \quad A_{13} = \frac{L_{c1}C_{o1} + T_s r_{c1}C_{o1} + {T_s}^2}{{T_s}^2} \\
&B_1(z) = B_{11}z^{-3} + B_{12}z^{-2} + B_{13}z^{-1} + B_{14} \\
&\quad B_{11} = \frac{L_{o1}L_{c1}C_{o1}}{{T_s}^3}, \quad B_{12} = -\frac{3L_{o1}L_{c1}C_{o1} + T_s\left(r_{c1}L_{o1}C_{o1} + r_{Lo1}L_{c1}C_{o1}\right)}{{T_s}^3}, \\
&\quad B_{13} = \frac{3L_{o1}L_{c1}C_{o1} + 2T_s\left(r_{c1}L_{o1}C_{o1} + r_{Lo1}L_{c1}C_{o1}\right) + {T_s}^2\left(L_{c1} + L_{o1} + r_{Lo1}r_{c1}C_{o1}\right)}{{T_s}^3}, \\
&\quad B_{14} = -\frac{L_{o1}L_{c1}C_{o1} + T_s\left(r_{c1}L_{o1}C_{o1} + r_{Lo1}L_{c1}C_{o1}\right) + {T_s}^2\left(L_{c1} + L_{o1} + r_{Lo1}r_{c1}C_{o1}\right) + {T_s}^3\left(r_{Lo1} + r_{c1}\right)}{{T_s}^3}
\end{aligned}
\tag{6.6}
$$

$$
\begin{aligned}
&A_2(z) = A_{21}z^{-2} + A_{22}z^{-1} + A_{23} \\
&\quad A_{21} = \frac{L_{c2}C_{o2}}{{T_s}^2}, \quad A_{22} = -\frac{2L_{c2}C_{o2} + T_s r_{c2}C_{o2}}{{T_s}^2}, \quad A_{23} = \frac{L_{c2}C_{o2} + T_s r_{c2}C_{o2} + {T_s}^2}{{T_s}^2} \\
&B_2(z) = B_{21}z^{-3} + B_{22}z^{-2} + B_{23}z^{-1} + B_{24} \\
&\quad B_{21} = \frac{L_{o2}L_{c2}C_{o2}}{{T_s}^3}, \quad B_{22} = \frac{3L_{o2}L_{c2}C_{o2} + T_s\left(r_{c2}L_{o2}C_{o2} + r_{Lo2}L_{c2}C_{o2}\right)}{{T_s}^3}, \\
&\quad B_{23} = \frac{3L_{o2}L_{c2}C_{o2} + 2T_s\left(r_{c2}L_{o2}C_{o2} + r_{Lo2}L_{c2}C_{o2}\right) + {T_s}^2\left(L_{c2} + L_{o2} + r_{Lo2}r_{c2}C_{o2}\right)}{{T_s}^3}, \\
&\quad B_{24} = -\frac{L_{o2}L_{c2}C_{o2} + T_s\left(r_{c2}L_{o2}C_{o2} + r_{Lo2}L_{c2}C_{o2}\right) + {T_s}^2\left(L_{c2} + L_{o2} + r_{Lo2}r_{c2}C_{o2}\right) + {T_s}^3\left(r_{Lo2} + r_{c2}\right)}{{T_s}^3}
\end{aligned}
\tag{6.7}
$$

Estimated module output voltages from (6.1) and (6.2) can be expressed in the z-domain

$$
\begin{aligned}
\hat{v}_{o1}(z) &= \frac{2}{\pi}A_1(z)v_{c1}(z) + B_1(z)i_{Lo1}(z) \\
\hat{v}_{o2}(z) &= \frac{2}{\pi}A_2(z)v_{c2}(z) + B_2(z)i_{Lo2}(z)
\end{aligned}
\tag{6.8}
$$

Using the coefficients in (6.6) and (6.7), and substituting into (6.8) to obtain time domain equations at the k^{th} discrete instant, yields

$$
\begin{aligned}
\hat{v}_{o1}(k) &= \frac{2}{\pi}\left[A_{11}v_{c1}(k-2) + A_{12}v_{c1}(k-1) + A_{13}v_{c1}(k)\right] \\
&\quad + B_{11}i_{Lo1}(k-3) + B_{12}i_{Lo1}(k-2) + B_{13}i_{Lo1}(k-1) + B_{14}i_{Lo1}(k) \\
\hat{v}_{o2}(k) &= \frac{2}{\pi}\left[A_{21}v_{c2}(k-2) + A_{22}v_{c2}(k-1) + A_{23}v_{c2}(k)\right] \\
&\quad + B_{21}i_{Lo2}(k-3) + B_{22}i_{Lo2}(k-2) + B_{23}i_{Lo2}(k-1) + B_{24}i_{Lo2}(k)
\end{aligned}
\tag{6.9}
$$

However, from (6.9), estimating $\hat{v}_{o1}(k)$ and $\hat{v}_{o2}(k)$ required for voltage control needs the same k^{th} instant value of the controller output values $\hat{v}_{c1}(k)$ and $\hat{v}_{c2}(k)$. This cannot be implemented unless $\hat{v}_{o1}(k)$ and $\hat{v}_{o2}(k)$ are projected one sample in advance to obtain $\hat{v}_{o1}(k+1)$ and $\hat{v}_{o2}(k+1)$. This can be performed using the Lagrange quadratic predictor formula which states that

$$\begin{aligned}\hat{v}_{o1}(k+1) &= 3\hat{v}_{o1}(k) - 3\hat{v}_{o1}(k-1) + \hat{v}_{o1}(k-2)\\ \hat{v}_{o2}(k+1) &= 3\hat{v}_{o2}(k) - 3\hat{v}_{o2}(k-1) + \hat{v}_{o2}(k-2)\end{aligned} \tag{6.10}$$

Substituting (6.10) into (6.9), using the appropriate *k* instants, yields

$$\begin{aligned}\hat{v}_{o1}(k+1) = \frac{2}{\pi}\big[&A_{11}v_{c1}(k-4) + (A_{12}-3A_{11})v_{c1}(k-3) + (3A_{11}-3A_{12}+A_{13})v_{c1}(k-2)\\ &+ (3A_{12}-3A_{13})v_{c1}(k-1) + 3A_{13}v_{c1}(k)\big]\\ &+ B_{11}i_{Lo1}(k-5) + (B_{12}-3B_{11})i_{Lo1}(k-4) + (3B_{11}-3B_{12}+B_{13})i_{Lo1}(k-3)\\ &+ (3B_{12}-3B_{13}+B_{14})i_{Lo1}(k-2) + (3B_{13}-3B_{14})i_{Lo1}(k-1) + 3B_{14}i_{Lo1}(k)\\ \hat{v}_{o2}(k+1) = \frac{2}{\pi}\big[&A_{21}v_{c2}(k-4) + (A_{22}-3A_{21})v_{c2}(k-3) + (3A_{21}-3A_{22}+A_{23})v_{c2}(k-2)\\ &+ (3A_{22}-3A_{23})v_{c2}(k-1) + 3A_{23}v_{c2}(k)\big]\\ &+ B_{21}i_{Lo2}(k-5) + (B_{22}-3B_{21})i_{Lo2}(k-4) + (3B_{21}-3B_{22}+B_{23})i_{Lo2}(k-3)\\ &+ (3B_{22}-3B_{23}+B_{24})i_{Lo2}(k-2) + (3B_{23}-3B_{24})i_{Lo2}(k-1) + 3B_{24}i_{Lo2}(k)\end{aligned} \tag{6.11}$$

According to (6.3) and (6.4), $\hat{v}_o(k+1)$ used for the outer voltage loop can be defined as

$$\hat{v}_o(k+1) = \begin{cases}\dfrac{\hat{v}_{o1}(k+1)+\hat{v}_{o2}(k+1)}{2} & \textit{for ISOP system}\\ \hat{v}_{o1}(k+1)+\hat{v}_{o2}(k+1) & \textit{for ISOS system}\end{cases} \tag{6.12}$$

Details for the practical implementation of the proposed load voltage estimator are provided in Appendix C.

6.4 Simulation and experimental results of ISOP connected phase-controlled SPRC

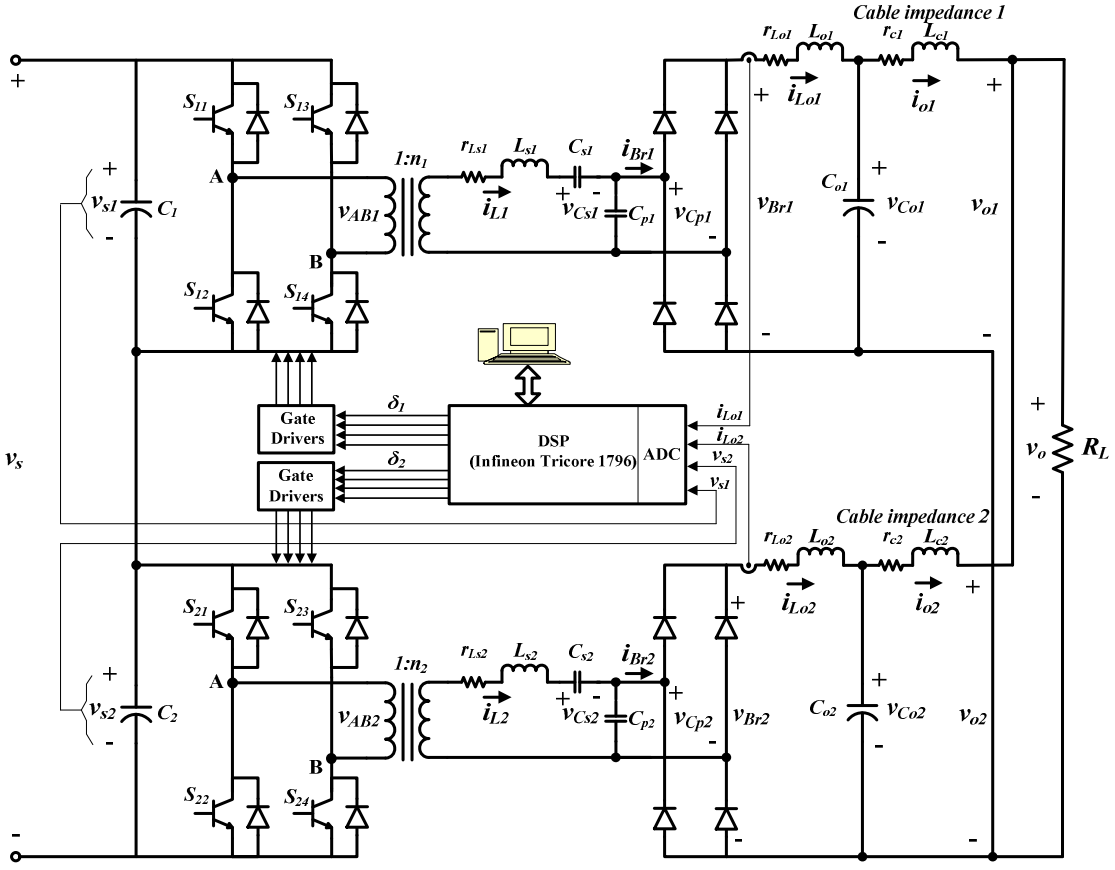
Fig. 6.6(a) **s**hows the experimental circuit for the two-module ISOP connected phase-controlled SPRC. The control algorithm implemented in the Infineon DSP comprises a sensorless remote load voltage controller with an average IVS loop which adjusts and

regulates the output of the outer loop Lyapunov load voltage controller. This structure is depicted in Fig. 6.4(c). The two-module converter system operates in an interleaved mode to minimize load voltage and current ripple. As discussed in chapter three, section 3.3.5, module #2 inverter gate signals are phase-shifted by 90° compared to those of module #1. The interleaved inverter gating patterns are illustrated in Fig. 6.6(b).

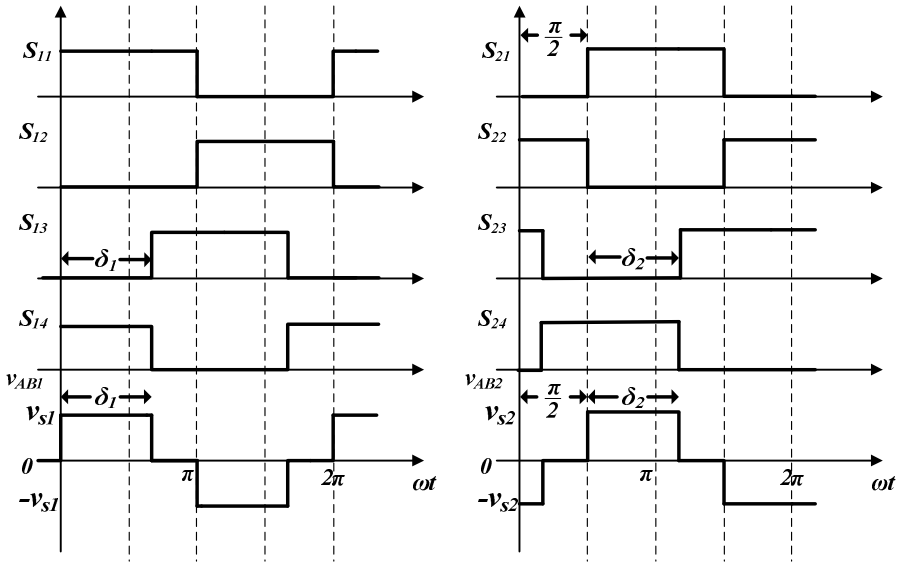
Circuit parameter values are defined in Table 6.1 and operational and control values used for the experimental prototype are given in Table 6.2. Each module is designed to operate at the same 40W prototype power level designed initially, so the two-module system will operate at 80W. In addition to the naturally unavoidable circuit parameter mismatches between the two converter modules, three major circuit parameter differences are applied to evaluate the control and sharing performance, namely

- Different series-module input capacitances to assess IVS under extreme conditions
- Different resonant tank transformer turns ratios
- Different cable impedances

The three factors are highlighted in Table 6.1 for emphasis.



(a)



(b)

Fig. 6.6: Two-module ISOP connected phase-controlled SPRC (a) circuit diagram and (b) interleaved modules inverter gating patterns.

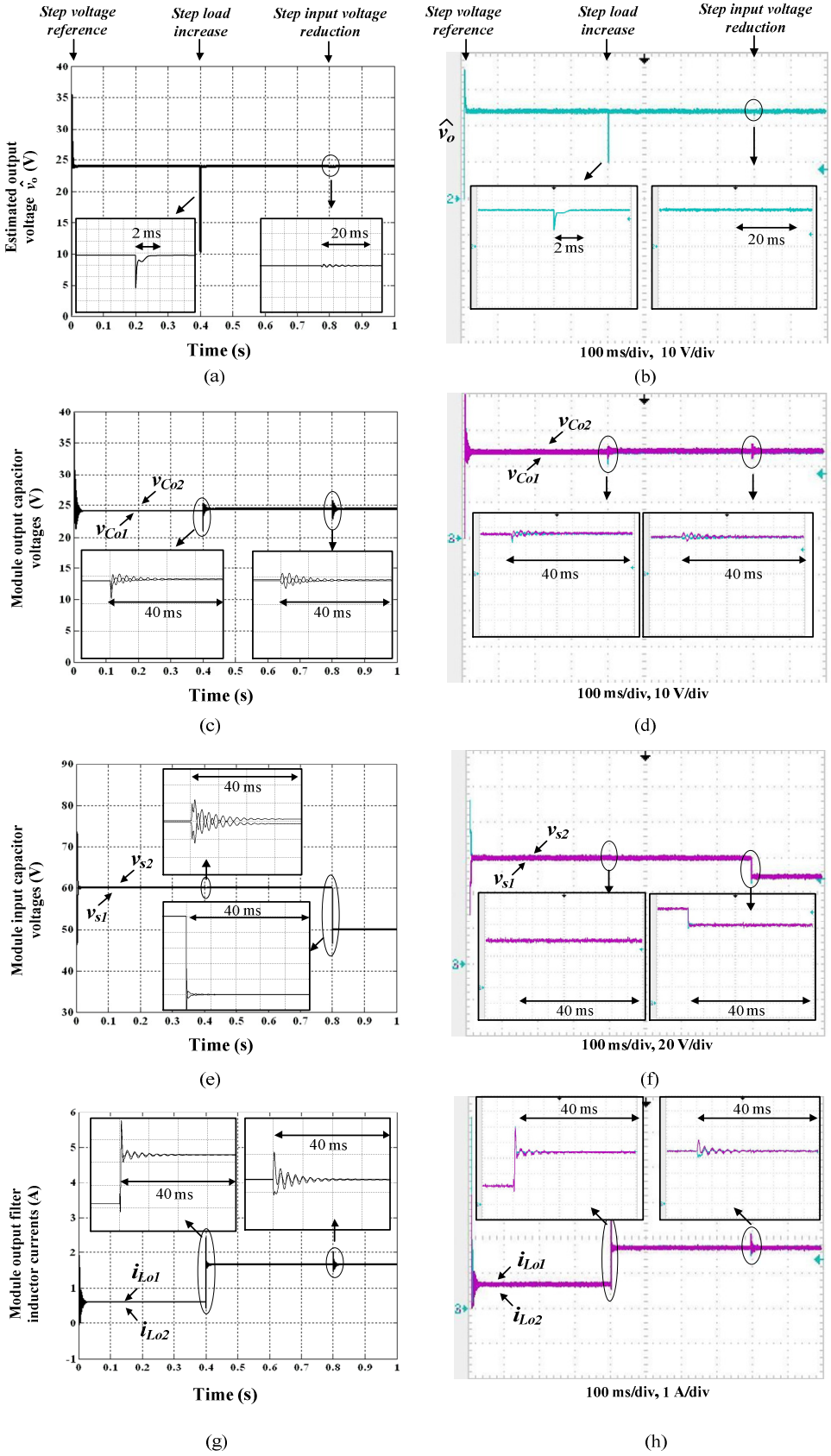
i^{th} circuit parameter	Module #1 (i=1)	Module #2 (i=2)
C_i	30 μF	60 μF
n_i	0.5	0.555
r_{Lsi}	0.1916 Ω	0.22 Ω
L_{si}	100.13 μH	102.66 μH
r_{li}	0.6 Ω	0.51 Ω
L_{li}	9.12 μH	8.78 μH
r_{Ti}	0.7916 Ω	0.83 Ω
L_{Ti}	109.25 μH	111.44 μH
C_{si}	255 nF	255 nF
C_{pi}	255 nF	255 nF
r_{Loi}	0.5 Ω	0.5 Ω
L_{oi}	12.5 mH	12.5 mH
C_{oi}	120 μF	120 μF
r_{ci}	0.2 Ω	0.3 Ω
L_{ci}	1 mH	2 mH

Table 6.1: Circuit parameter values for the two-module ISOP system

Parameter	Definition	Value
P_{FL}	Converter full-load power rating	80 W
v_s	Input supply voltage	120 V
v_o^*	Reference output (load) voltage	24 V
f	Switching frequency	40 kHz
R_{LFL}	Full-load resistance	7.2 Ω
R_{LPL}	Partial load resistance	20.25 Ω
K_p	Lyapunov controller proportional gain (as in chapter 5)	11.3313
K_d	Lyapunov controller derivative gain (as in chapter 5)	0.0047
K	Average IVS control loop gain	10

Table 6.2: Operational and control values for the two-module ISOP system.

Fig. 6.7 shows results for the ISOP connected phase-controlled SPRC. A step disturbance from partial load (R_{LPL}=20.25Ω) to full-load (R_{LFL}=7.2 Ω) is applied at t=0.4s and a step input voltage reduction from v_s=120V to v_s=100V is applied at t=0.8s.



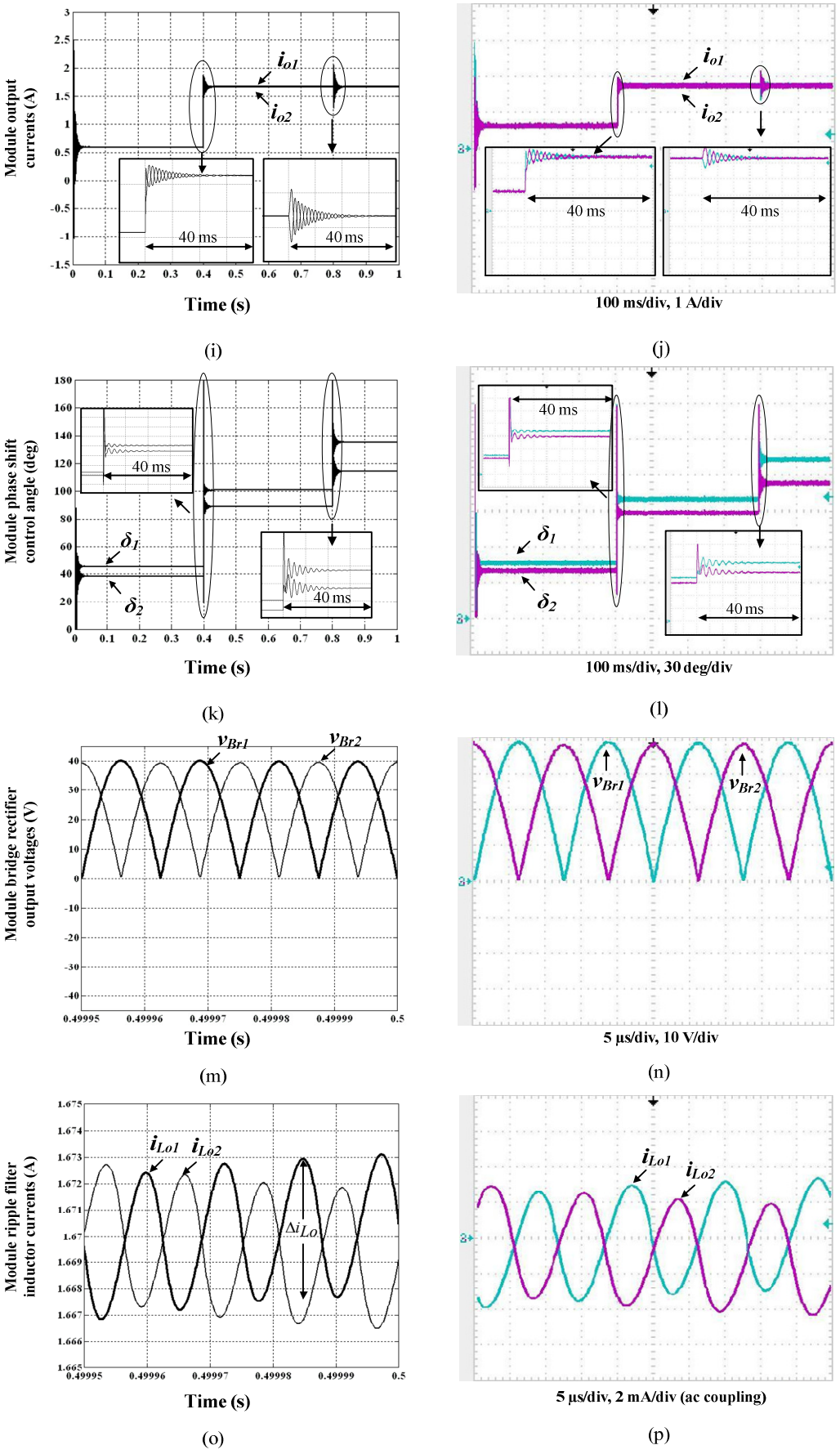


Fig. 6.7: Results for the ISOP connected phase-controlled SPRC (a),(c),(e), (g), (i), (k), (m) and (o) simulation, and (b),(d),(f), (h), (j), (l), (n) and (p) experimental.

The following can be observed from the results:

- The estimated output voltage $\hat{v}_o$ in Fig. 6.7(a) and (b) follows the desired reference voltage v_o^*=24V which verifies the accuracy of the proposed load voltage estimator. The robust Lyapunov controller rejects the step load disturbance in a fast and stable manner with a voltage dip lasting 2ms. Perturbation due to the step input voltage reduction is minimal;
- Regulation of the load voltage v_o which, in the case of ISOP connection, is equal to the individual module output voltages v_{o1} and v_{o2}. Module output capacitor voltages v_{Co1} and v_{Co2} are unregulated. This appears in Fig. 6.7(c) and (d) where after the step load application at t=0.4s, there exists a marginal increase in the values of v_{Co1} and v_{Co2} due to the added voltage drop across the cable impedance of each module after the load current increases. v_{Co2} is slightly higher than v_{Co1} since r_{c2} is higher than r_{c1};
- Fig. 6.7(e) and (f) show equal sharing between input module capacitor voltages although input capacitances are different (C_1=30μF and C_2=60μF). The full supply voltage (v_s=120V) is uniformly distributed (v_{s1}=v_{s2}=60V) and partial supply voltage (v_s=100V) after reduction at t=0.8s, is also equally shared (v_{s1}=v_{s2}=50V). IVS control provides fast and stable voltage distribution;
- Equal output current sharing is achieved automatically between the modules even without dedicated OCS control. This confirms that for ISOP systems, IVS is sufficient to obtain stable operation with OCS, even with module parameter mismatches. This is clear from results for i_{Lo1} and i_{Lo2} in Fig. 6.7(g) and (h), and also i_{o1} and i_{o2} in Fig. 6.7(i) and (j) which show uniform current sharing in spite of different cable impedances and unequal transformer turns ratios. Transient sharing in the output filter inductor currents i_{Lo1} and i_{Lo2} is better than that of module output currents i_{o1} and i_{o2}. This is because, i_{Lo1} and i_{Lo2} are sensed and used as part of the feedforward mechanism implemented by the Lyapunov controller. Being part of the control enhances the output filter inductor current transient and steady-state responses;
- The time constant of the output filter circuit and the cable impedance (neglecting the output capacitance) can be expressed by

$$\tau_1 = \frac{L_{o1} + L_{c1}}{r_{Lo1} + r_{c1}} \quad \text{and} \quad \tau_2 = \frac{L_{o2} + L_{c2}}{r_{Lo2} + r_{c2}} \tag{6.13}$$

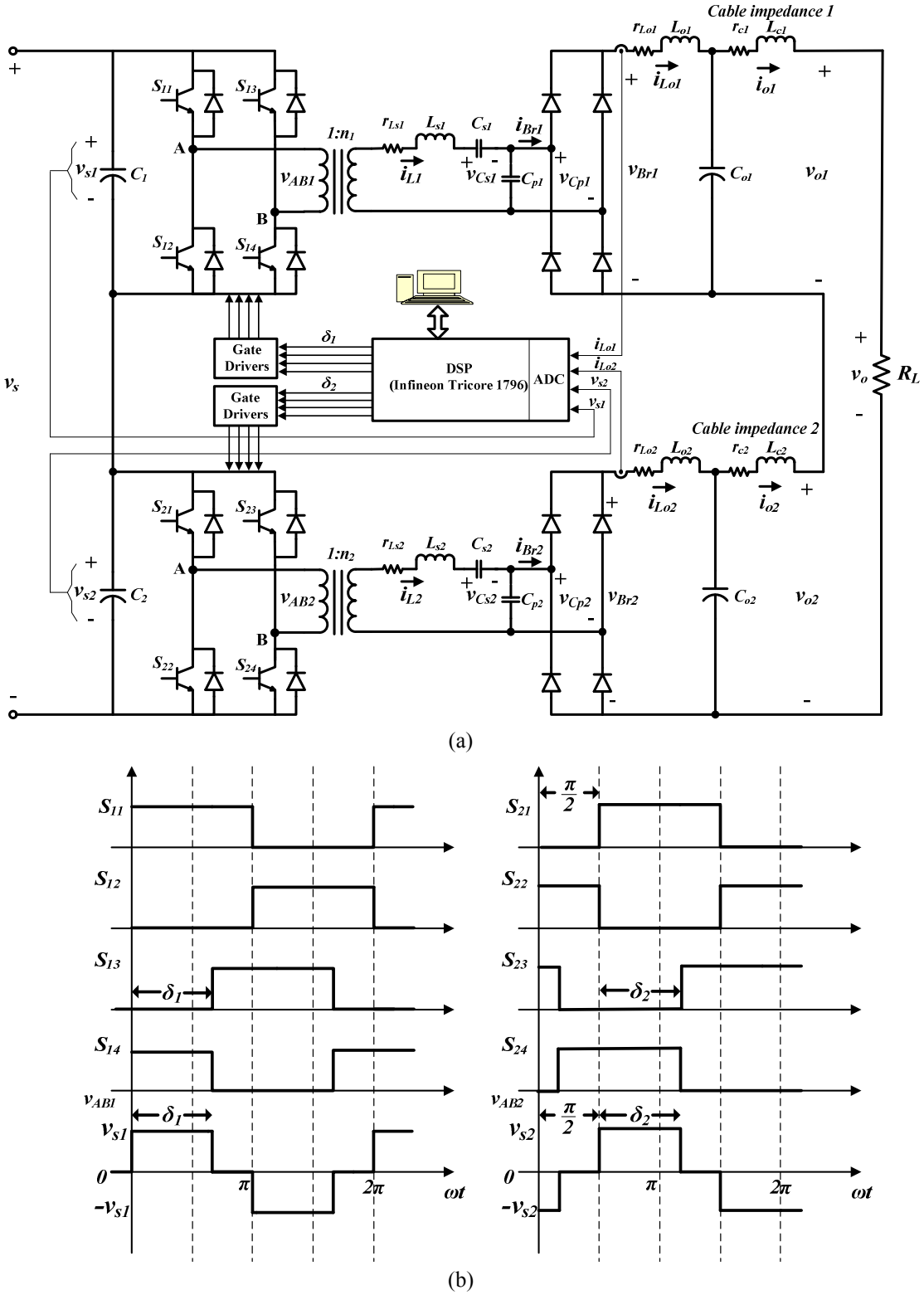
where τ_1 and τ_2 are modules #1 and #2 circuit time constants respectively. Applying step response theory for RL circuits using the time constants in (6.13), yields a settling time of 40ms for the current in response to the step disturbances applied. This can be seen in Fig. 6.7(g), (h), (i) and (j). The 40ms disturbance period appears in v_{s1} and v_{s2} since the output current disturbance is seen in the module input current being drawn from input capacitors. It also appears in all other circuit variables except the load voltage v_o due to the decoupled dynamics of the IVS loop and the outer voltage control loop;

- The phase shift control angles δ_1 and δ_2 are adjusted by control action to compensate for the mismatched transformer turns ratios. Module input voltages v_{s1} and v_{s2} are equal, therefore, module #2 with the higher turns ratio (n_2=0.555 > n_1=0.5) will always have a lower phase shift angle ($\delta_2 < \delta_1$) so that both modules produce equal resultant voltage gains. Fig. 6.7(k) and (l) illustrate the phase shift angles with $\delta_2 < \delta_1$. Phase shift angles increase at t=0.4s due to increased loading which means more average voltage (energy) needs to be delivered to the output to keep it at desired reference value. Also, when the input voltage is reduced at t=0.8s, further increases in δ_1 and δ_2 are required to compensate for the input voltage decrease; and
- Fig. 6.7(m) and (n) show the interleaved bridge rectifier output voltages v_{Br1} and v_{Br2} and Fig. 6.7(o) and (p) show the inductor ripple currents after full-load application (0.4s< t <0.8s). Individual module current ripple can be calculated as in section 3.3.5 of chapter three using

$$\Delta I_{Lo} = 0.105\frac{V_o}{fL_o} = \frac{0.105 \times 24}{40000 \times 12.5 \times 10^{-3}} = 5\text{mA} \tag{6.14}$$

6.5 Simulation and experimental results of ISOS connected phase-controlled SPRC

Fig. 6.8(a) shows the experimental circuit for the two-module ISOS connected phase-controlled SPRC. The control algorithm implemented in the Infineon DSP is exactly the same as that for the ISOP system with the structure shown in Fig. 6.4(c). The interleaved inverter gating patterns are illustrated in Fig. 6.8 (b).Circuit parameter values used are the same as in Table 6.1. Operational and control values used for the experimental ISOS system are the same as those given in Table 6.2 with the exception of v_o^*=48V, R_{LPL}=81Ω and R_{LFL}=28.8Ω to maintain full-load operation at 40W per module. The same module parameter mismatches are applied as for the ISOP system.

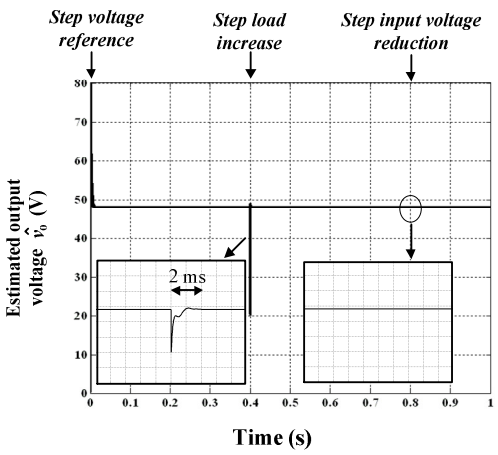


(a)

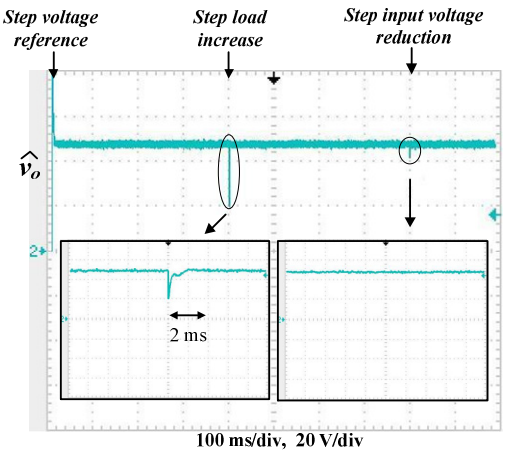
(b)

Fig. 6.8: Two-module ISOS connected phase-controlled SPRC (a) circuit diagram and (b) interleaved module inverter gating patterns.

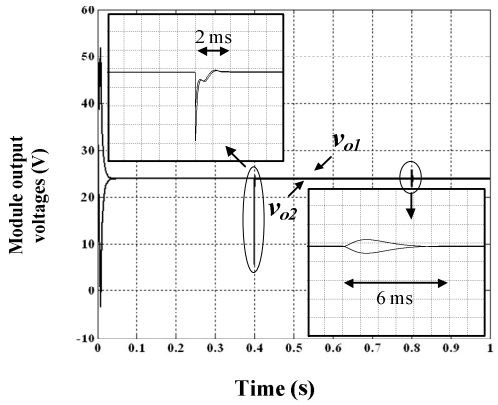
Fig. 6.9 shows results for the ISOS connected phase-controlled SPRC. Step disturbance from a partial load to full-load is applied at t=0.4s and a step input voltage reduction from v_s=120V to v_s=100V is applied at t=0.8s.


Step voltage reference
Step load increase
Step input voltage reduction
Estimated output voltage $\hat{v}_o$ (V)
2 ms
Time (s)

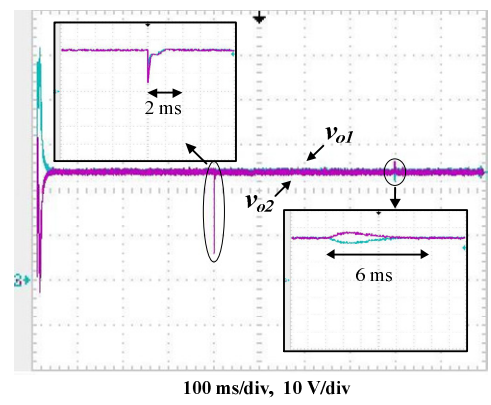
(a)


Step voltage reference
Step load increase
Step input voltage reduction
$\hat{v}_o$
2 ms
100 ms/div, 20 V/div

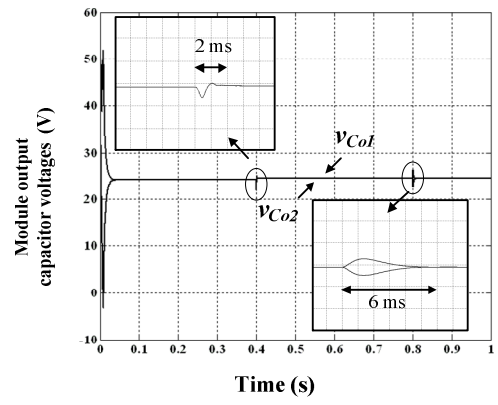
(b)


Module output voltages (V)
2 ms
v_{o1}
v_{o2}
6 ms
Time (s)

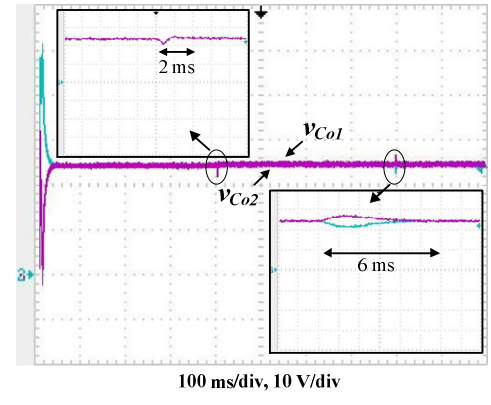
(c)


2 ms
v_{o1}
v_{o2}
6 ms
100 ms/div, 10 V/div

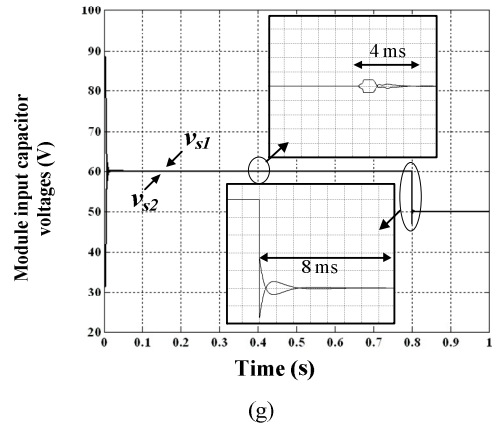
(d)


Module output capacitor voltages (V)
2 ms
v_{Co1}
v_{Co2}
6 ms
Time (s)

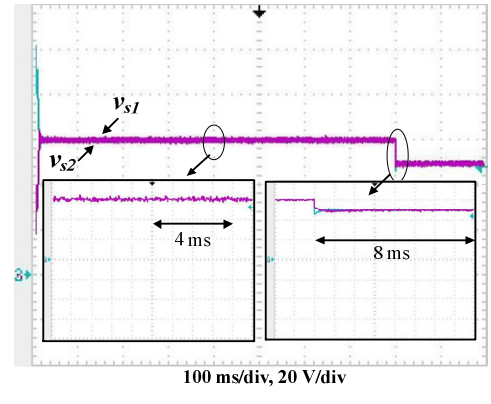
(e)


2 ms
v_{Co1}
v_{Co2}
6 ms
100 ms/div, 10 V/div

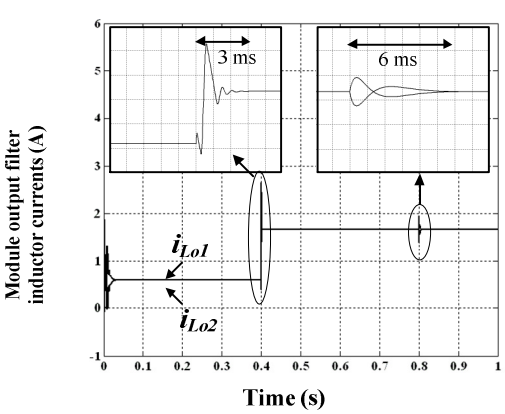
(f)


Module input capacitor voltages (V)
4 ms
v_{s1}
v_{s2}
8 ms
Time (s)

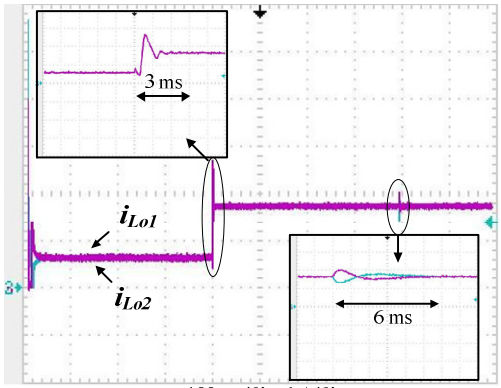
(g)


v_{s1}
v_{s2}
4 ms
8 ms
100 ms/div, 20 V/div

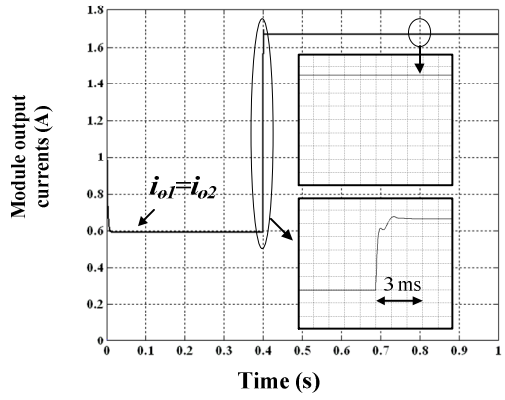
(h)


Module output filter inductor currents (A)
3 ms
6 ms
i_{Lo1}
i_{Lo2}
Time (s)

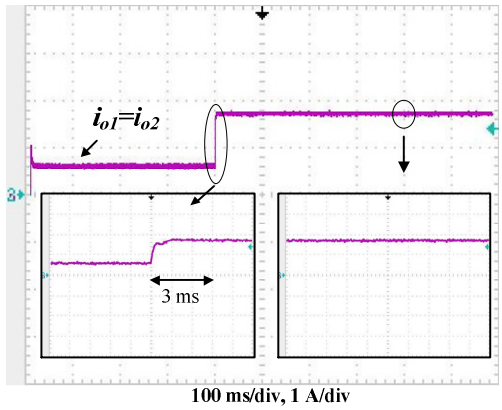
(i)


3 ms
i_{Lo1}
i_{Lo2}
6 ms
100 ms/div, 1 A/div

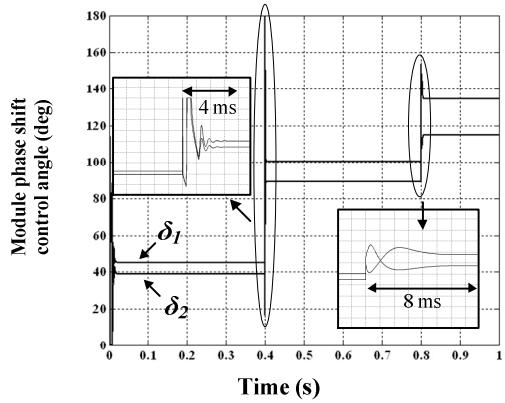
(j)


Module output currents (A)
i_{o1}=i_{o2}
3 ms
Time (s)

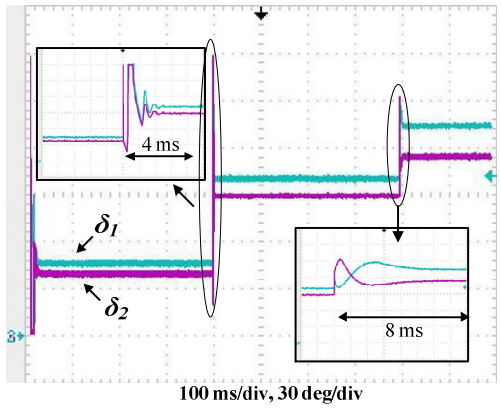
(k)


i_{o1}=i_{o2}
3 ms
100 ms/div, 1 A/div

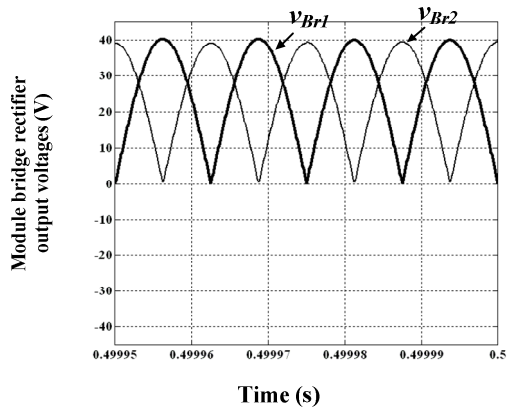
(l)


Module phase shift control angle (deg)
4 ms
δ_1
δ_2
8 ms
Time (s)

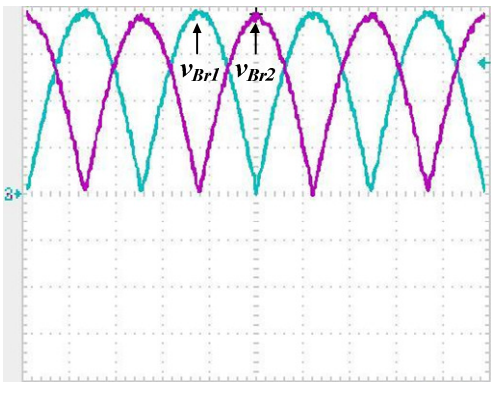
(m)


4 ms
δ_1
δ_2
8 ms
100 ms/div, 30 deg/div

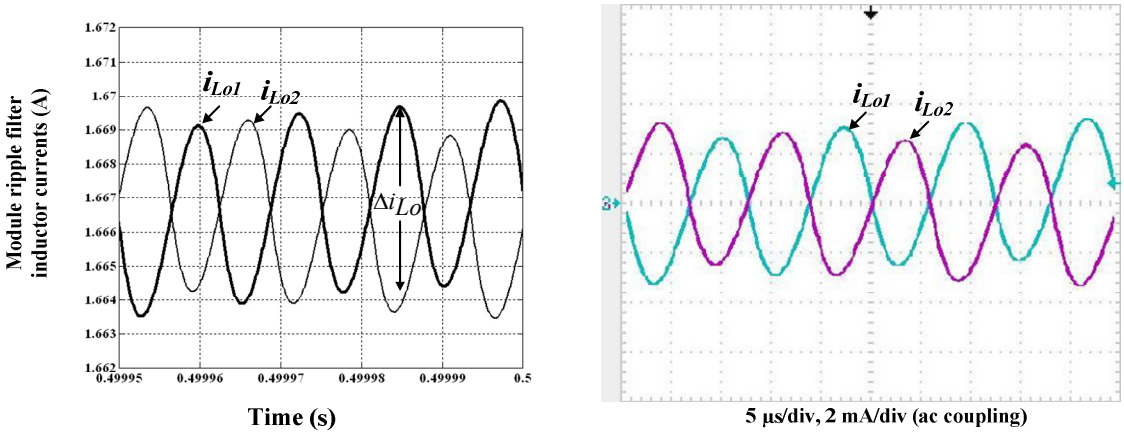
(n)


Module bridge rectifier output voltages (V)
v_{Br1}
v_{Br2}
Time (s)

(o)


v_{Br1}
v_{Br2}
5 µs/div, 10 V/div

(p)



(q) (r)

Fig. 6.9: Results for the ISOS connected phase-controlled SPRC (a),(c),(e), (g), (i), (k), (m), (o) and (q) simulation and (b),(d),(f), (h), (j), (l), (n), (p) and (r) experimental.

Results from Fig. 6.9 are similar to those achieved by the ISOP connected system. The following comments can be made:

- Fig. 6.9(a) and (b) show output voltage being regulated at the desired reference value v_o*=48V;
- By virtue of the IVS control loop, automatic module output voltage sharing occurs. This can be seen by the behaviour of v_{o1} and v_{o2} in Fig. 6.9(c) and (d). Each module operates at its nominal ratings with v_{o1}=v_{o2}=24V. Module output capacitor voltages v_{Co1} and v_{Co2} in Fig. 6.9(e) and (f) have a similar response with the added voltage drop across the cable resistance at steady-state;
- Module input voltages are equally shared, due to the IVS control loop. This is verified by Fig. 6.9(g) and (h);
- Module output currents i_{o1} and i_{o2} are equal due to the series output connection. This causes output filter currents i_{Lo1} and i_{Lo2} to be equal at steady-state. Fig. 6.9(i), (j), (k) and (l) illustrate the mentioned currents response;
- Control action compensates for the mismatched module transformer turns ratios and adjusts the modules phase-shift control angles accordingly. Module 2 with the higher turns ratio has a lower phase-shift angle (δ_2<δ_1), as seen in Fig. 6.9(m) and (n);
- Interleaved bridge rectifier output voltages and inductor ripple currents are depicted in Fig. 6.9(o), (p), (q) and (r). The individual module ripple current is consistent with the calculations in (6.14); and
- Although the same control algorithm structure is implemented for both ISOP and ISOS systems, the time elapsed by the step disturbance perturbations is lower for

ISOS (2 to 6ms) compared to ISOP systems (40ms). Load current i_o follows v_o due to the resistive load nature. In ISOS systems, $i_o=i_{o1}=i_{o2}$, which means that individual module currents follow the same load voltage time domain characteristics. This is apparent from the 2 to 4ms perturbation duration for most converter variables at t=0.4s, which is similar to that of the output voltage in Fig. 6.9(a) and (b).

Therefore, in conclusion, both input-series connections of the phase-controlled SPRC have shown satisfactory load voltage regulation using the proposed sensorless remote voltage estimation scheme with accurate and stable uniform distribution of module input voltages and output currents/voltages. For ISOS systems, the series connection of modules at the output causes module currents to follow the load voltage transient response. Since the load voltage is controlled by the Lyapunov controller which has a high disturbance rejection capability, this enhances dynamic behaviour of individual module state variables.

6.6 Load voltage estimator parameter sensitivity

The proposed load voltage estimator is based on the output filter and the interconnecting cable impedance parameters. Actual circuit parameters vary during operation due to several factors such as temperature and cable overloading. However, the estimator uses fixed pre-determined values for these circuit elements. It is therefore necessary to study how operational changes in these parameters would affect closed-loop stability and dynamic response. Fig. 6.10 shows the effect of changing the cable impedance of each converter module to five times the original values stated in Table 6.1. Variation is applied during operation (at t=0.05s) while maintaining the original values in the mathematical load voltage estimator model. In other words, if the cable impedance values are denoted by $\Delta Z_{c1}Z_{c1}$ and $\Delta Z_{c2}Z_{c2}$, then after variation

$$\Delta Z_{c1} = \Delta Z_{c2} = 5\text{p.u.} \tag{6.15}$$

Fig. 6.10(a) shows closely matching responses of the actual and estimated load voltages for the ISOP connected system. Closed-loop operation is stable and OCS is achieved successfully and in a stable manner as shown in Fig. 6.10(b). Similarly, Fig. 6.10(c) depicts close resemblance of actual and estimated load voltages for the ISOS connected system. OVS occurs successfully as shown in Fig. 6.10(d) but with a slower dynamic response due to the increased RL circuit time constant due to the series connection of the cable impedances at the module outputs.

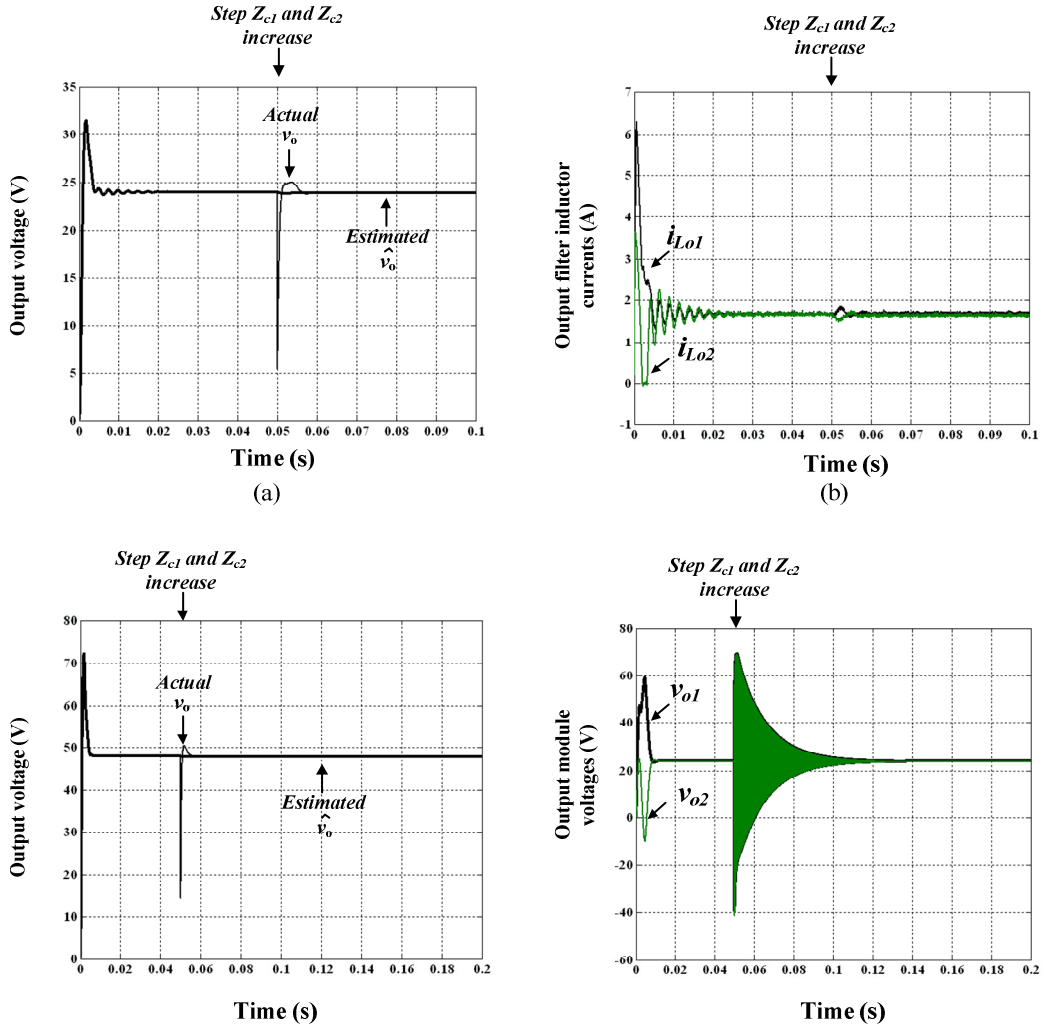


Fig. 6.10: Load voltage estimator sensitivity to varying cable impedance
(a) and (b) ISOP system, and (c) and (d) ISOS system.

6.7 Summary

Phase-controlled SPRC multi-module converter operation applicable to the load side converter of the subsea *All-Electric* project has been studied. Emphasis has been made on ISOP and ISOS connections of the converter due to their voltage step down characteristics. It has been verified that a common feature to both connections is the indispensability of input voltage sharing control to achieve stable multi-module operation. A common control structure has been proposed for control of both converter connections. It comprised an outer voltage loop for load voltage regulation using a Lyapunov controller which provided fast, stable and robust output voltage control together with an average IVS control loop to adjust the control signal produced by the outer voltage loop. OCS and OVS for ISOP and ISOS connections respectively have been achieved automatically with IVS control. A sensorless load voltage estimator has been proposed for load voltage regulation which is useful in the case of the subsea project due to the pos-

sible remote load location from the main converter site. The algorithm based on two-port network theory provided accurate estimations of the load voltage, and its sensitivity to cable impedance parameter variation has been analysed and proven to provide satisfactory closed-loop performance.

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Chapter 7

Conclusion

7.1 General Conclusion

The trend in the offshore oil and gas industry is to move production fields to the seabed with connection back to an onshore terminal, which may be located over 100km apart. This has been triggered by the emerging nodes in deeper waters and hence the need to remove offshore surface facilities. As defined by industry specifications, typical subsea actuation system power requirements are 10-15kW from a 10kVdc medium voltage dc transmission system. The use of dc power has provided a solution to many problems associated with the next generation of subsea electrical power systems. DC transmission eliminates reactive ac charging current, reduces electrical cable loss and reactive power compensation costs for dc lines are eliminated. Installed cable costs are lower. The power level demanded by the oil and gas industry subsea project is not high; therefore existing commercial HVDC technologies such as ABB HVDC Light, Siemens HVDC Plus or Alstom MaxSine are excessive in this specific low power application.

The scope of this thesis includes the analysis, design, modelling and control of modular medium-power, medium-voltage dc/dc converter-based systems. An important application for this has been the *All-Electric* subsea project. The modular approach enables design standardization, enhances system fault tolerance, enables scalability and ensures, with an appropriate level of redundancy, minimum down time due to module failure.

After a survey of existing applicable dc/dc converter topologies, the candidate dc/dc converter selected was the phase-controlled series-parallel resonant converter (SPRC). It provides key features for the subsea project requirements; high operational efficiency, transformer isolation between input and output, and most importantly soft switching characteristics enabling high frequency operation with reduced converter footprint. The first aspect of this converter studied was its steady-state analysis and design. This was reported in chapter three with detailed derivation of new steady-state relations and performance measures providing increased understanding of converter operation and insight into its characteristics. The novel design procedure was based on operation at

maximum efficiency and full-load operational conditions. Detailed nano-crystalline core transformer design, with associated loss calculations, were presented in addition to output filter design in single-module and multi-module interleaved operation modes. New mathematical expressions were presented for the interleaved filter design.

In chapter four, a novel large-signal model was proposed for the phase-controlled SPRC. The model used state feedback linearization with output filter inductor current measurement. The linearized large-signal dynamic model provided an alternative to the switched converter model for faster simulation, in addition providing a useful tool for closed-loop design and stability analysis using its reduced order equivalent. The model enabled sensorless multi-loop control of the converter. A Kalman filter based state estimator was proposed using the model to estimate resonant tank state variables, used for inner loop PI control. This enhanced closed-loop stability and dynamic response was compared to single loop PI control without using additional sensors. In chapter five, converter dynamic closed-loop behaviour was further improved by proposing three new robust controllers for output voltage control; namely Lyapunov, sliding mode and predictive control. In terms of robustness and sensitivity to parameter variation, sliding mode control offers superior performance. However, dynamic performance is sacrificed due to chattering and reduced stability margins. The Lyapunov controller provided acceptable disturbance rejection capability, with high closed-loop bandwidth with superior dynamic behaviour due to the output voltage feed forward mechanism implemented.

Converter multi-module operation was studied in chapter six with voltage and current sharing being addressed. Emphasis was placed on the load-side step down dc/dc converter for the subsea project. This comprised ISOP and ISOS connections of phase-controlled SPRCs to attain the required project operating voltage and power levels. A sensorless load voltage estimation algorithm was proposed to estimate the load voltage remotely located at manifolds, taking into account connecting cable impedances. It was verified that input voltage sharing control, in input-series connected systems, is indispensable for stable control and uniform sharing. Load voltage estimation was accurate and together with the proposed controller showed stable and robust behaviour to cable parameter operational variations.

Extensive simulation and experimental validation were performed to verify all the proposed analysis, modelling and control methods. Simulation was mainly carried out us-

ing Matlab/Simulink software. The experimental prototype was based on an Infineon Tricore DSP microcontroller driving a 40W, 40kHz, 60V/24V dc/dc phase-controlled SPRC. Multi-module operation was studied on a two-module ISOP connected SPRC with the system rated at 80W, 120V/24V. ISOS connection was also studied on a two-module SPRC rated at 80W, 120V/48V. Closely matching analytical, simulation and experimental results have proven the validity of the proposed algorithms in this thesis.

7.2 Author's contribution

The thesis contributions can be summarized as follows:

- New steady-state analysis derived for the phase-controlled SPRC; namely, voltage gain transfer function for a phase-shift control technique, voltage gain sensitivity to changes in operational parameters, modes of operation revealed with mode boundaries analytically derived, maximum power transfer criteria and operational efficiency taking into account various converter losses.
- New design procedure for the phase-controlled SPRC based on a maximum efficiency criterion. Operating frequency and full-load quality (load) factor are selected to satisfy maximum operating efficiency.
- Nano-crystalline core transformer design with loss calculations is performed.
- New mathematical expressions derived for the converter output LC filter design in an interleaved multi-module operation mode.
- A novel large-signal dynamic model for the phase-controlled SPRC using state feedback measurement of output filter inductor current.
- A Kalman filter based sensorless multi-loop controller for the SPRC. The controller utilises the derived model in providing online estimation of resonant tank state variables for use as the inner loop variable in a multi-loop PI output voltage controller.
- Three new robust controllers for robust output voltage control of the phase-controlled SPRC; namely Lyapunov, sliding mode and predictive controllers. The main objective is to improve output voltage dynamic behaviour and robustness to circuit parameter variations; the latter being an inevitable factor in the subsea environment.
- A novel control configuration for phase-controlled SPRC interleaved multi-module operation, which is common to both ISOP and ISOS connections of the converter. The controller comprises a Lyapunov controller as the main load voltage regulator together with an average input voltage sharing controller regulating the inner control

loop to ensure uniform output current sharing in an ISOP system and uniform output voltage sharing in an ISOS system.

- A sensorless load voltage estimation algorithm based on two-port network theory for remotely located loads. The algorithm accounts for interconnecting cable impedance and is particularly useful in the subsea project where loads may be situated a significant distance from the main converter site. Not only does the algorithm reduce the number of required sensors, but it also eliminates the possibility of noisy measurements resulting from lengthy signal cables.

7.3 Suggestions for future research

Potential areas for further research include:

- Optimum design of converter elements to ensure minimum size for a high power density design and reduced footprint.
- Consideration of transformer voltage insulation requirements at 10kV which makes size bulky. Starting with the transformer in the module furthest away the earthing point, full voltage insulation is necessary and this is gradually reduced the lower the module is located down the string. However, all module transformers need to be insulated at full transmission voltage with respect to earth potential to ensure true modularity and inter-changeability.
- Detailed examination of series resonant tank capacitance position with respect to the transformer. Locating the capacitor at the primary side enables blocking of dc offsets in inverter output waveforms which could saturate the transformer. However, capacitor voltage rating would be higher in case of step down operation.
- Fault analysis in multi-module converter operation. This includes investigation of methods for fault detection and isolation.
- Fault tolerant multi-module operation implementing N+1 redundancy with the associated voltage and current sharing issues as faulty modules are isolated.
- Replacement of the central DSP controller for multi-module converter operation with a dedicated controller per converter module to enhance overall system modularity and enable modules to operate in both stand-alone and sharing modes.
- Validation of the proposed converter topology and controllers at medium-voltage high-power operation level to enable a detailed case study closer to real life implementation.

Appendix A

Experimental Rig

The structure of the experimental prototype implementing two-module phase-controlled series-parallel resonant converter (SPRC) is introduced. Details of hardware components and DSP software environment are presented.

A.1 Hardware structure

The experimental test rig comprises control circuitry, power circuitry and recording and monitoring devices. The whole system is shown in Fig. A.1. Components, and their labels, are defined in Table A.1.

Component number	***Control Circuitry (C)***	***Power Circuitry (P)***	***Recording and monitoring devices (R)***
1	Digital Signal Processor	Dc power supply	Low pass filter circuit for DSP analogue output
2	Interfacing circuits	Dc link capacitors with EMI filters	Multimeters
3	Current and voltage transducer circuits	Module input capacitor (×2)	Current probes
4	Gate drive circuits	Module power inverter (×2)	Voltage probes
5	Biasing dc supply	Nano-crystalline core transformer (×2)	Digital oscilloscope
6		LCC resonant tank (×2)	
7		Bridge rectifier (×2)	
8		Output LC filter (×2)	
9		Cable impedance (×2)	
10		Load	

Table A.1: Experimental system components

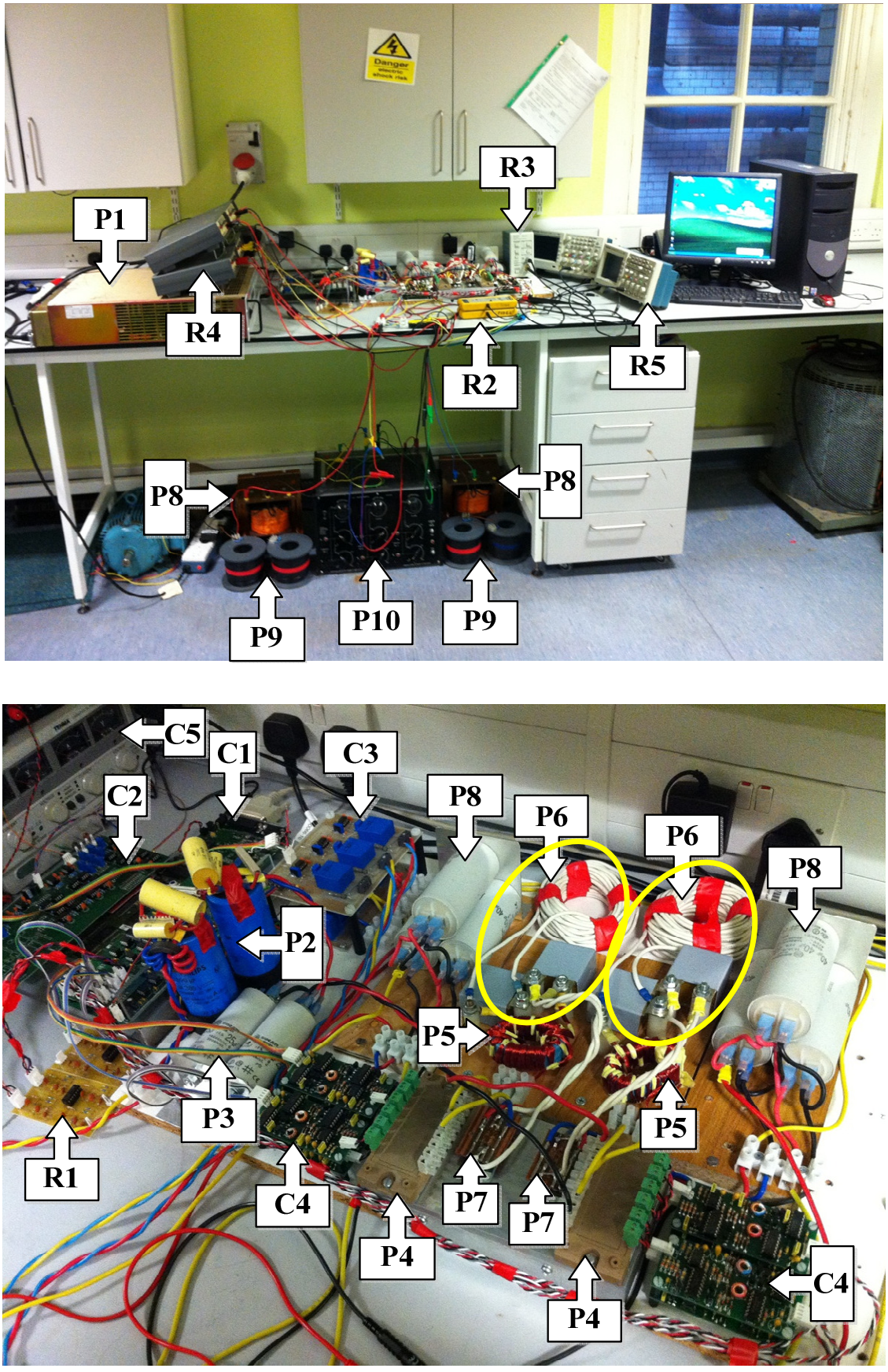


Fig. A.1: Experimental system setup

A.1.1 Control circuitry

Control circuits are mainly powered by ±15V and +5V biasing dc supplies. They consist of a digital signal processor (DSP) acting as the main system controller, interfacing circuits to galvanically isolate and scale up/down signals from other circuits with the 3.3V DSP TTL level, voltage and current sensing circuits for closed-loop realisation and gate drive circuits to drive inverter switches.

(a) Digital signal processor

The DSP acts as the main system controller. Sensed analogue signals are sampled and converted to digitally coded numbers using the embedded fast analogue to digital conversion. This is necessary since the switching (sampling) frequency at which control is updated and power inverter is switched is 40kHz. This allows 25μs for the entire control algorithm execution including analogue to digital conversion, computations and PWM signals update. In order to save time for computations, the embedded fast analogue to digital converter operating with programmable conversion time is used. Maximum possible conversion time per channel is 280ns. The various control algorithms and proposed techniques in this thesis are written using C-code and finally the necessary phase-shift angle δ between inverter legs is calculated. The gate signals with the required switching pattern then drive the inverter switches. The 32-bit Infineon Tricore TC1976 DSP shown in Fig. A.2 is implemented in the experimental prototype.

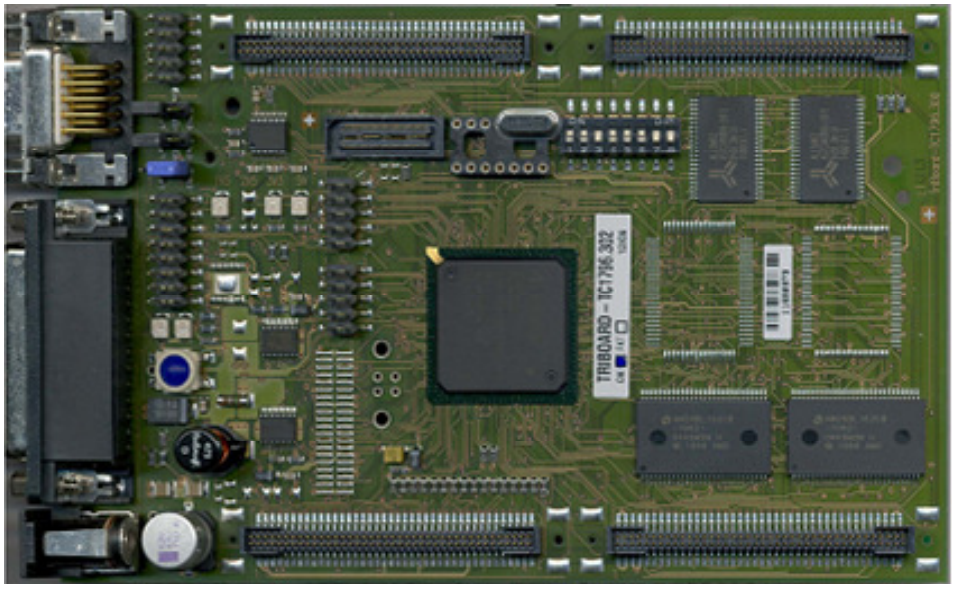


Fig. A.2: Infineon Tricore TC1796 DSP

Key DSP features are:

- High performance 32-bit super-scalar *TriCoreTM* V1.3 CPU with 4 stage pipeline
  - Superior real-time performance.
  - Strong bit handling.
  - Fully integrated DSP capabilities.
  - Single precision floating point unit (FPU).
  - 150 MHz at full automotive temperature range.
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2).
- Memories
  - 2 M embedded program flash with ECC.
  - 128 K data flash.
  - 192 K on chip SRAM.
  - 16 K instruction cache.
- 32-bit external bus interface unit with synchronous burst flash access capability
- Sophisticated interrupt system with 2x255 hardware priority arbitration levels serviced by CPU and PCP2.
- High performing triple bus structure
  - 64-bit local memory buses to internal flash and data memory.
  - 32-bit system peripheral bus for interconnections of on-chip peripherals and further functional units.
  - 32-bit remote peripheral bus serving the requirements of high speed peripherals.
- Two general purpose timer array modules plus separate LTC array with a digital signal filtering and timer functionality to realize autonomous and complex I/O management.
- 4-channel fast analog-to-digital converter unit (FADC); with10-bit resolution and 280ns maximum conversion time.
- Two 16-channel analog-to-digital converter units (ADC) with 8-bit, 10-bit or 12-bit resolution.
- 123 digital general purpose I/O lines, 4 input lines; with 3.3 V capability.
- Power management system and full automotive temperature range -40° to +125°C.
- Clock generation unit with PLL.

(b) Interface circuits

The function of the interface circuits is to galvanically isolate DSP ground from ground of other control and power circuits. Two interface circuits are used:

- One circuit to isolate ground of current and voltage transducer circuits from DSP ground. The circuit implements linear optocouplers for this purpose. The circuit also scales down the 0-10V output of the transducer circuits to the 0-3.3V range for DSP fast analogue to digital input (FADC).
- The other circuit is used to scale up the digital 3.3V PWM outputs of the DSP to 5V level for the gate drive circuits. It also performs galvanic isolation.

Fig. A.3 shows the implemented interface circuits and Fig. A.4 depicts their circuit diagrams.

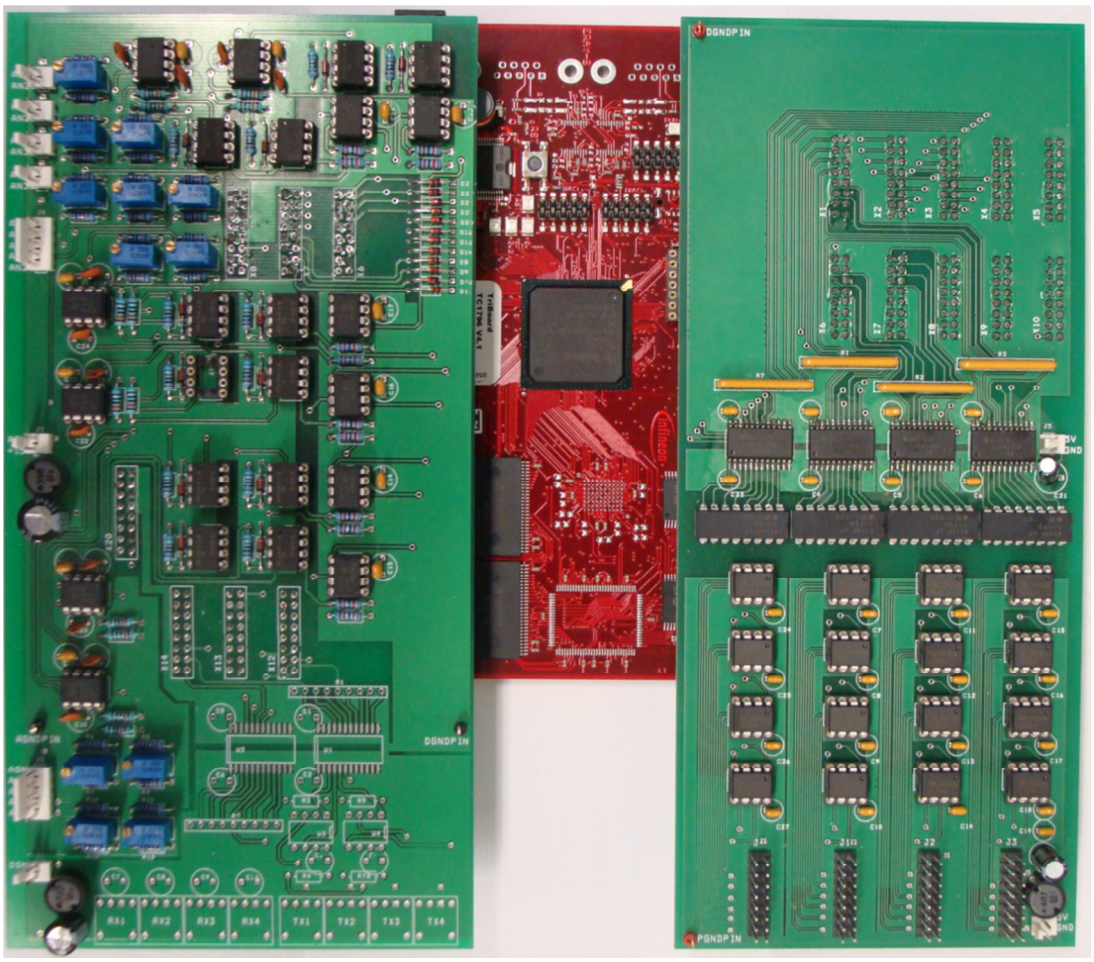
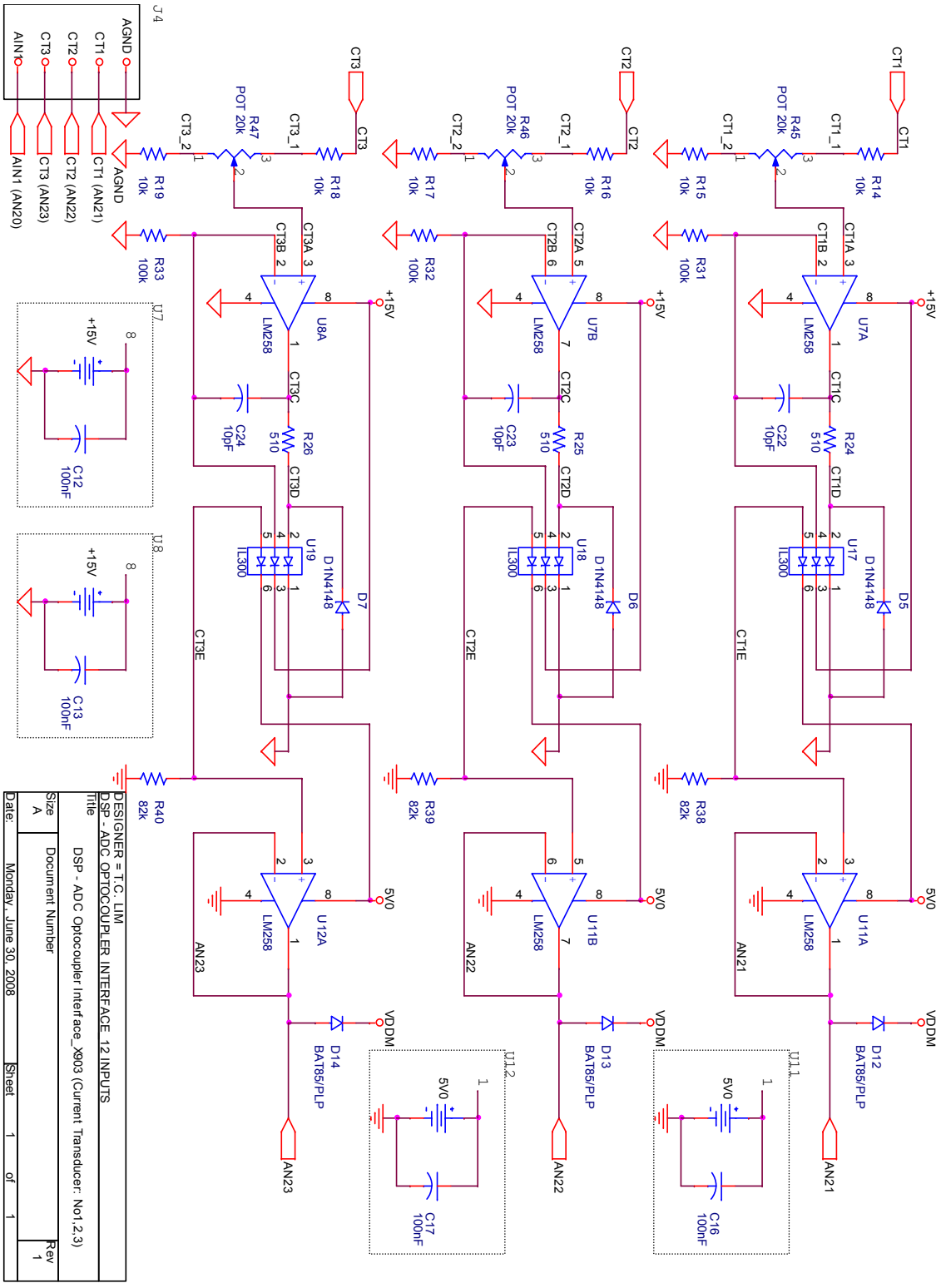


Fig. A.3: Interface circuits


J4
AGND
CT1
CT2
CT3
AIN1
AGND
CT1 (AN21)
CT2 (AN22)
CT3 (AN23)
AIN1 (AN20)
CT1
CT2
CT3
R14 10k
R15 10k
R16 10k
R17 10k
R18 10k
R19 10k
R45 POT 20k
R46 POT 20k
R47 POT 20k
CT1_1
CT1_2
CT2_1
CT2_2
CT3_1
CT3_2
R31 100k
R32 100k
R33 100k
U7A
U7B
U8A
LM258
CT1A
CT1B
CT2A
CT2B
CT3A
CT3B
CT1C
CT2C
CT3C
C22 10pF
C23 10pF
C24 10pF
R24 510
R25 510
R26 510
CT1D
CT2D
CT3D
U17
U18
U19
TL300
D1N4148
D5
D6
D7
CT1E
CT2E
CT3E
R38 82k
R39 82k
R40 82k
U11A
U11B
U12A
AN21
AN22
AN23
D12 BAT85/PLP
D13 BAT85/PLP
D14 BAT85/PLP
+15V
5V0
VDDM
U11
U12
C16 100nF
C17 100nF
U7
U8
C12 100nF
C13 100nF
DESIGNER = T.C. LIM
DSP - ADC OPTOCOUPLER INTERFACE 12 INPUTS
Title
DSP - ADC Optocoupler Interface_X903 (Current Transducer: No1,2,3)
Size
A
Document Number
Rev
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Date:
Monday, June 30, 2008
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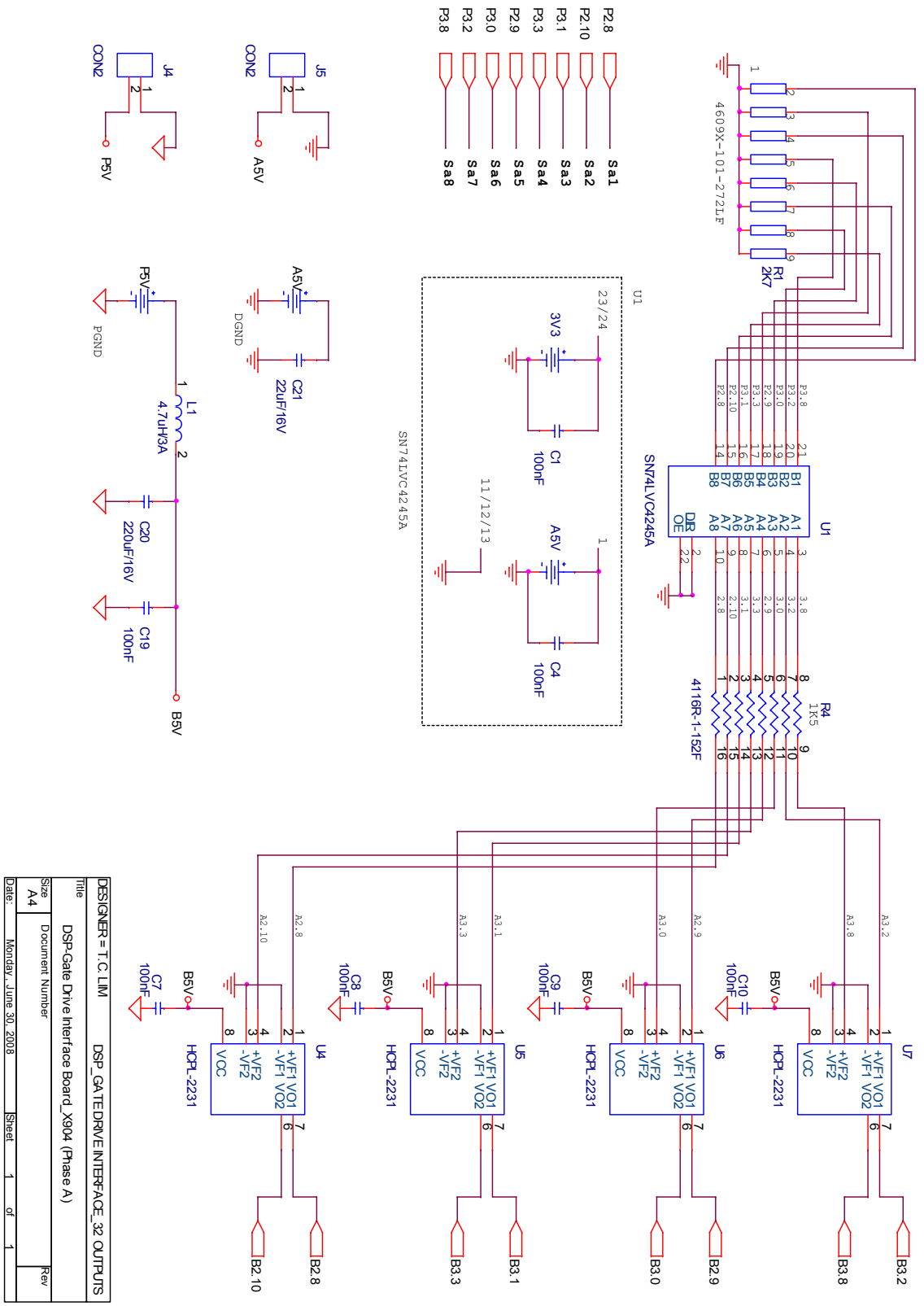
(a)



(b)

Fig A.4: Interface board circuit diagrams for (a) FADC inputs, and (b) PWM outputs

(c) Current and voltage transducer circuits

In single-module operation, sensing load voltage and output filter inductor current is necessary for output voltage control. The inductor current is necessary for the state feedback linearization scheme introduced in chapter four and used in all proposed control techniques. In multi-module operation, sensing currents and voltages is necessary for uniform sharing. For these reasons, current and voltage transducer circuits are mandatory for closed-loop realisation.

In the experimental rig, a Hall effect current sensing device LEM (LA55P) is used, which has high accuracy, good linearity and optimized response time. The sensing range is from 0A to 50A and the frequency range is from dc to 100 kHz. The output of the transducer is level-shifted and scaled using a signal conditioning circuit to 0-10V range. Circuit diagram for the implemented current transducer with its associated signal conditioning is shown in Fig. A.5.

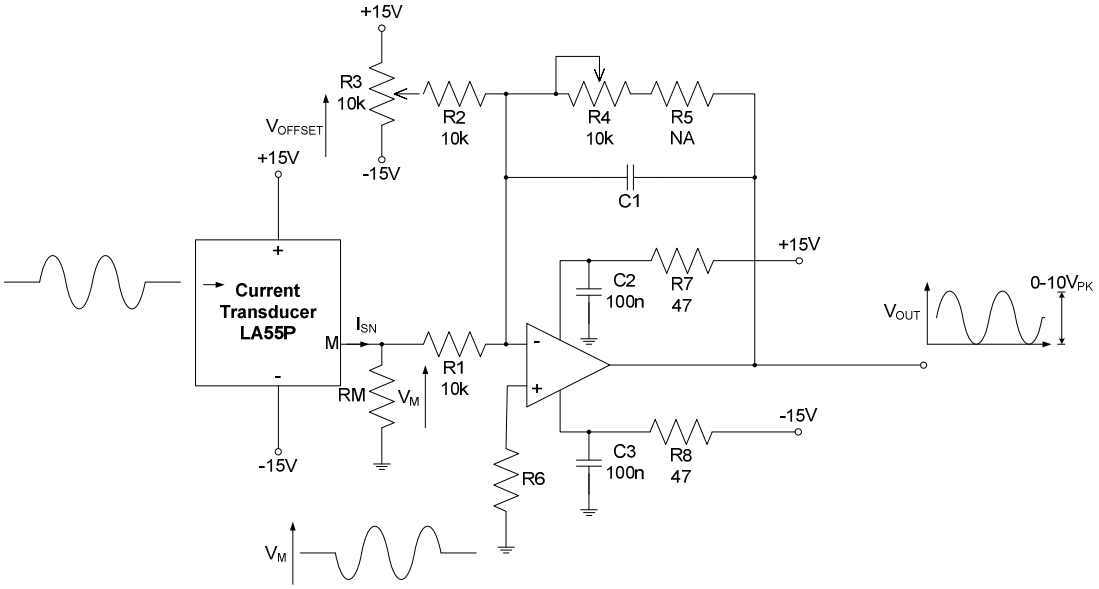


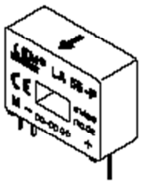
Fig. A.5: Current transducer circuit diagram

LEM

Current Transducer LA 55-P

I_{PN} = 50 A

For the electronic measurement of currents : DC, AC, pulsed..., with a galvanic isolation between the primary circuit (high power) and the secondary circuit (electronic circuit).



Electrical data

I_{PN}	Primary nominal r.m.s. current				50			A
I_P	Primary current, measuring range				0 .. ± 70			A
R_M	Measuring resistance @		T_A = 70°C		T_A = 85°C			
			$R_{M\,min}$	$R_{M\,max}$	$R_{M\,min}$	$R_{M\,max}$		
	with ± 12 V	@ ± 50 A_{max}	10	100	60	95		Ω
		@ ± 70 A_{max}	10	50	60[1]	60[1]		Ω
	with ± 15 V	@ ± 50 A_{max}	50	160	135	155		Ω
		@ ± 70 A_{max}	50	90	135[2]	135[2]		Ω
I_{SN}	Secondary nominal r.m.s. current				50			mA
K_N	Conversion ratio				1 : 1000			
V_C	Supply voltage (± 5 %)				± 12 .. 15			V
I_C	Current consumption				10 (@ ± 15 V) + I_S			mA
V_d	R.m.s. voltage for AC isolation test, 50 Hz, 1 mn				2.5			kV

Accuracy - Dynamic performance data

X	Accuracy @ I_{PN}, T_A = 25°C	@ ± 15 V (± 5 %)		± 0.65	%
		@ ± 12 .. 15 V (± 5 %)		± 0.90	%
ε_L	Linearity			< 0.15	%
			Typ	Max	
I_O	Offset current @ I_P = 0, T_A = 25°C			± 0.2	mA
I_{OM}	Residual current[3] @ I_P = 0, after an overload of 3 x I_{PN}			± 0.3	mA
I_{OT}	Thermal drift of I_O	0°C .. + 70°C	± 0.1	± 0.5	mA
		- 25°C .. + 85°C	± 0.1	± 0.6	mA
t_{ra}	Reaction time @ 10 % of $I_{P\,max}$			< 500	ns
t_r	Response time @ 90 % of $I_{P\,max}$			< 1	µs
di/dt	di/dt accurately followed			> 200	A/µs
f	Frequency bandwidth (- 1 dB)			DC .. 200	kHz

General data

T_A	Ambient operating temperature		- 25 .. + 85	°C
T_S	Ambient storage temperature		- 40 .. + 90	°C
R_S	Secondary coil resistance @	T_A = 70°C	80	Ω
		T_A = 85°C	85	Ω
m	Mass		18	g
	Standards[4]		EN 50178	

Notes : [1] Measuring range limited to ± 60 A_{max}
[2] Measuring range limited to ± 55 A_{max}
[3] Result of the coercive field of the magnetic circuit
[4] A list of corresponding tests is available

Features

- Closed loop (compensated) current transducer using the Hall effect
- Printed circuit board mounting
- Insulated plastic case recognized according to UL 94-V0.

Advantages

- Excellent accuracy
- Very good linearity
- Low temperature drift
- Optimized response time
- Wide frequency bandwidth
- No insertion losses
- High immunity to external interference
- Current overload capability.

Applications

- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Switched Mode Power Supplies (SMPS)
- Power supplies for welding applications.

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LEM Components www.lem.com

The voltage transducer circuit implements a Hall effect sensing device LEM (LV25-P) with voltage sensing range of 0 to 500V for ac and dc voltage measurements. Similar to the current transducer circuit, the output of the voltage transducer is conditioned to 0-

10V range. Fig. A.6 depicts the circuit diagram for the voltage transducer circuit. Fig A.7 shows the printed circuit board for both current and voltage transducers.

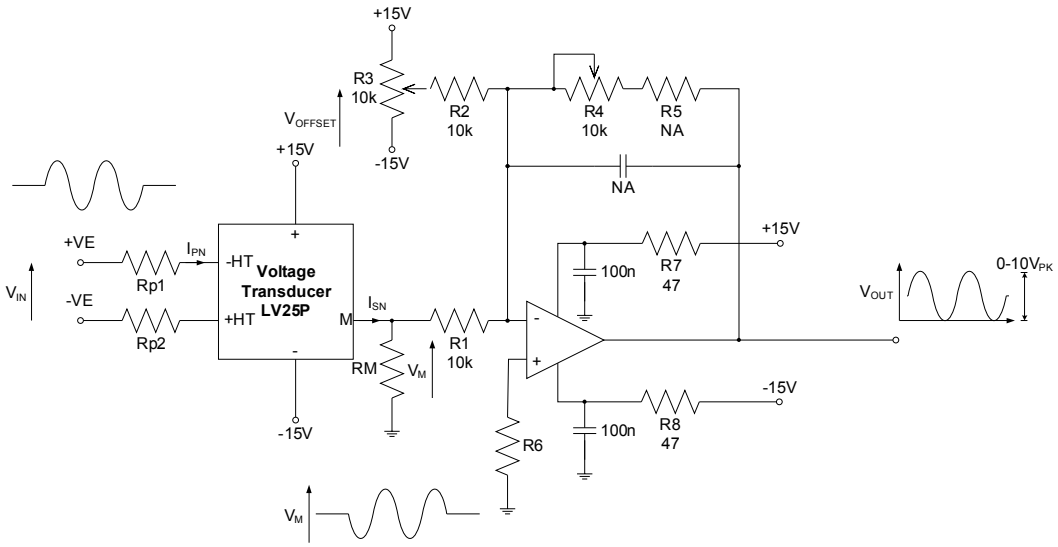


Fig. A.6: Voltage transducer circuit diagram

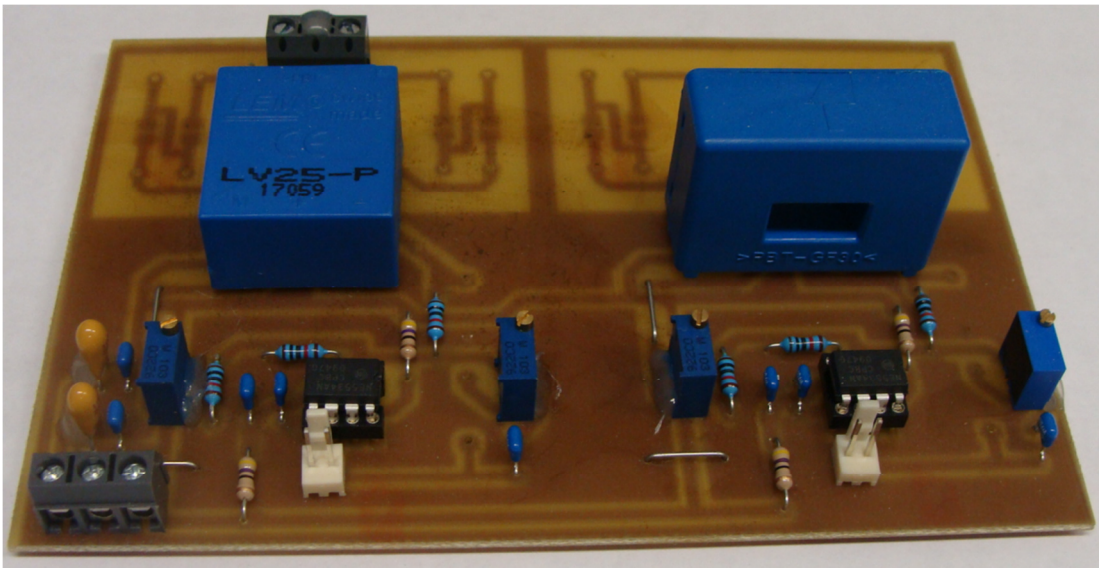
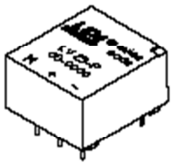


Fig. A.7: Voltage (left) and current (right) transducer circuit boards.

Voltage Transducer LV 25-P

I_{PN} = 10 mA
V_{PN} = 10 .. 500 V

For the electronic measurement of voltages : DC, AC, pulsed..., with a galvanic isolation between the primary circuit (high voltage) and the secondary circuit (electronic circuit).



Electrical data

I_{PN}	Primary nominal r.m.s. current		10		mA
I_P	Primary current, measuring range		0 .. ± 14		mA
R_N	Measuring resistance		$R_{N\,min}$	$R_{M\,max}$	
	with ± 12 V	@ ± 10 mA_{max}	30	190	Ω
		@ ± 14 mA_{max}	30	100	Ω
	with ± 15 V	@ ± 10 mA_{max}	100	350	Ω
		@ ± 14 mA_{max}	100	190	Ω
I_{SN}	Secondary nominal r.m.s. current		25		mA
K_N	Conversion ratio		2500 : 1000		
V_C	Supply voltage (± 5 %)		± 12 .. 15		V
I_C	Current consumption		10 (@±15 V)+I_S		mA
V_d	R.m.s. voltage for AC isolation test [1], 50 Hz, 1 mn		2.5		kV

Accuracy - Dynamic performance data

X_G	Overall Accuracy @ I_{PN}, T_A = 25°C	@ ± 12 .. 15 V	± 0.9		%
		@ ± 15 V (± 5 %)	± 0.8		%
ε_L	Linearity		< 0.2		%
			Typ	Max	
I_O	Offset current @ I_P = 0, T_A = 25°C			± 0.15	mA
I_{OT}	Thermal drift of I_O	0°C .. + 25°C	± 0.06	± 0.25	mA
		+ 25°C .. + 70°C	± 0.10	± 0.35	mA
t_r	Response time [2] @ 90 % of $V_{P\,max}$		40		µs

General data

T_A	Ambient operating temperature		0 .. + 70	°C
T_S	Ambient storage temperature		- 25 .. + 85	°C
R_P	Primary coil resistance @ T_A = 70°C		250	Ω
R_S	Secondary coil resistance @ T_A = 70°C		110	Ω
m	Mass		22	g
	Standards [3]		EN 50178	

Notes : [1] Between primary and secondary
[2] R_1 = 25 kΩ (L/R constant, produced by the resistance and inductance of the primary circuit)
[3] A list of corresponding tests is available

Features

- Closed loop (compensated) voltage transducer using the Hall effect
- Insulated plastic case recognized according to UL 94-V0.

Principle of use

- For voltage measurements, a current proportional to the measured voltage must be passed through an external resistor R_1 which is selected by the user and installed in series with the primary circuit of the transducer.

Advantages

- Excellent accuracy
- Very good linearity
- Low thermal drift
- Low response time
- High bandwidth
- High immunity to external interference
- Low disturbance in common mode.

Applications

- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Power supplies for welding applications.

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(d) Gate drive circuits

The gate drive circuit implemented in the experimental rig is shown in Fig. A.8 and the circuit diagram is depicted in Fig. A.9. The main functions of this circuit are:

- Step up the 5V TTL PWM signals from the DSP interface boards to 15V CMOS level for IGBT gate signals.
- Galvanically isolate the common-grounded PWM signals from the interface boards to IGBT gate signals with isolated grounds at the inverter side.
- Sourcing enough current for the IGBTs to be switched on. The maximum current that can be drawn from the interface circuits is in the range of milliamperes, while the gate terminal of the IGBT may require a large instantaneous spike of current to enable the fast charging of the gate capacitance and hence the turn on of the switch.

The first and second functions are realised using two high frequency transformers in the gate drive circuit. The first transformer magnetically isolates the PWM signal and steps it up from 5V to 15V. The step up is performed by 'NANDing' the PWM signal with a high frequency clock signal (produced from an on-chip oscillator), inverting, passing through the first transformer with 1:3 step up turns ratio and finally rectifying it to restore the original PWM signal but at 15V level. Similarly, the second transformer is for stepping up the 5V supply voltage of the interface to 15V to bias the necessary chips on the high voltage side of the transformer. IGBT gate drive current is drawn through the latter transformer. Due to the magnetic isolation offered by the gate drive circuit, only one 5V supply is needed for all inverter switches. However, this supply should be capable of withstanding the total switching current of all IGBTs it will drive.

Specifications of the gate drive circuit implemented are outlined in Table A.2.

Output voltage	15 V
Output current	±3 A
Supply voltage (max)	5 V
Signal frequency (max)	75 kHz
$t_{d\,on}$	60 ns
$t_{d\,off}$	60 ns

Table A.2 Gate drive circuit specifications

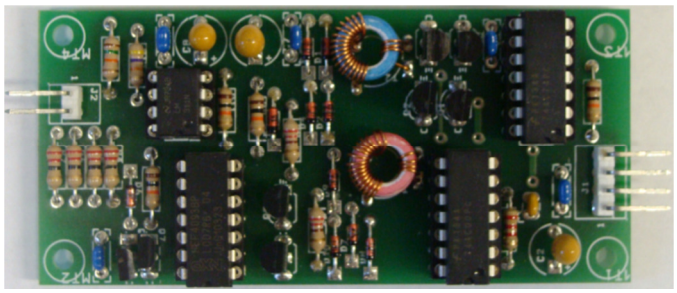


Fig. A.8: Gate drive circuit

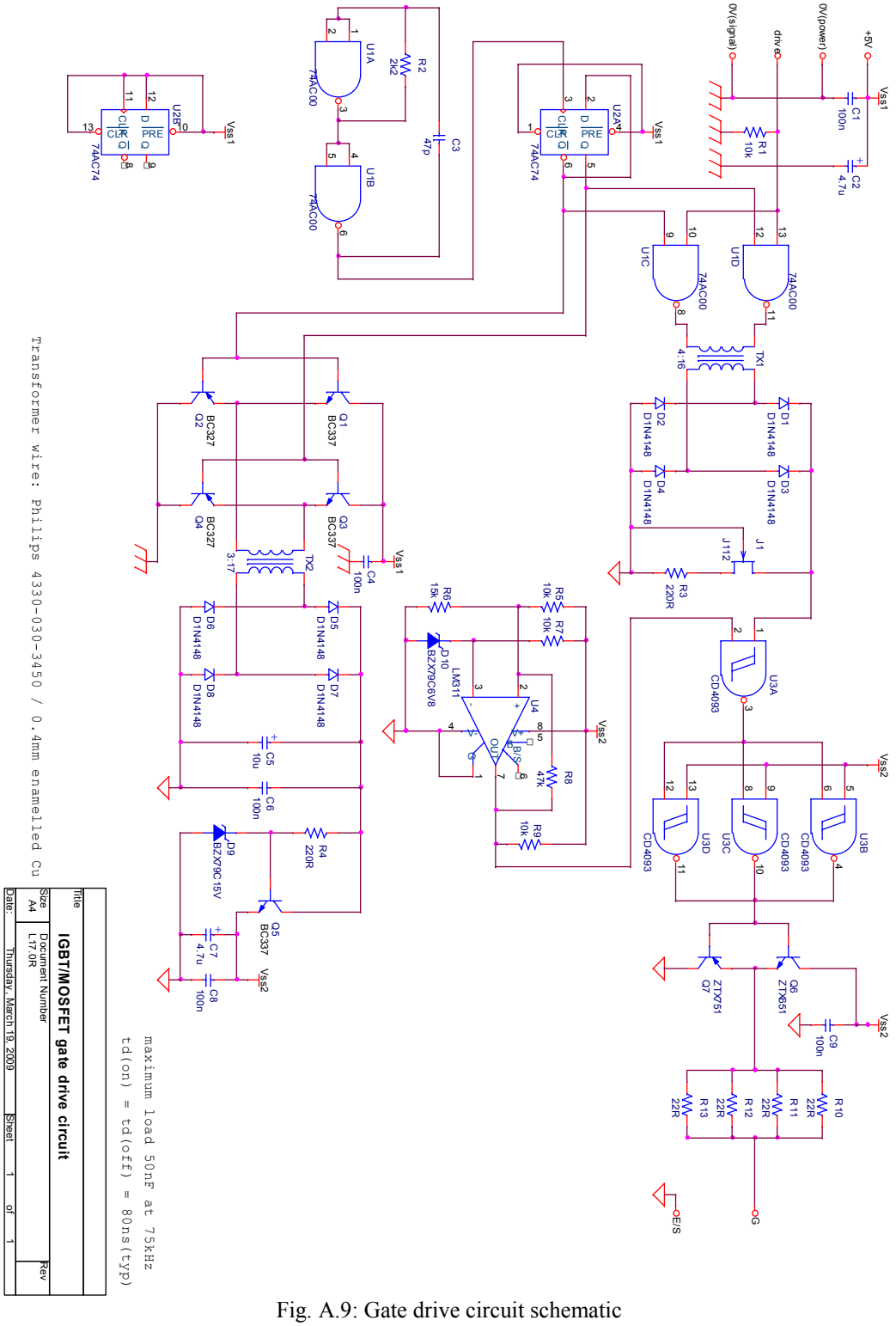


Fig. A.9: Gate drive circuit schematic

(e) Biasing dc supplies

Regulated dc supplies with different grounds are necessary to bias the various control circuits. The necessary supplies are:

- ±15V for the current and voltage transducer circuits in addition to the input interface board for the stage before the linear optocouplers isolation.
- +5V for the DSP, the input interface board after optocouplers isolation and for the output isolation board before optocouplers isolation.
- +5V for the output interface board after isolation and for the gate drive circuits.

A.1.2 Power Circuitry

The power circuit in the setup is mainly a two-module SPRC operating at 80W bench level full-load rating. Components comprising the setup are briefed in this section.

(a) Dc supply

A 600V, 25A programmable dc supply manufactured by ARGANTIX™ is used. For multi-module operation, the dc supply voltage level is set to 120V.

(b) Dc link capacitors with EMI filter

3000 μF, 385V high ripple current electrolytic capacitors from Philips™ are connected across the dc supply to provide stiff dc link voltage. Also 100nF, 1kVdc polypropylene capacitors are added for attenuation of high frequency switching components and to counter parasitic and stray inductance effects. Common mode chokes are inserted in series between the dc supply and the dc link capacitors for reduction of electromagnetic interference (EMI) and common mode voltages. It consists of two chokes mounted on the same magnetic core and inserted with opposite polarities. Circuit diagram is illustrated in Fig. A.10.

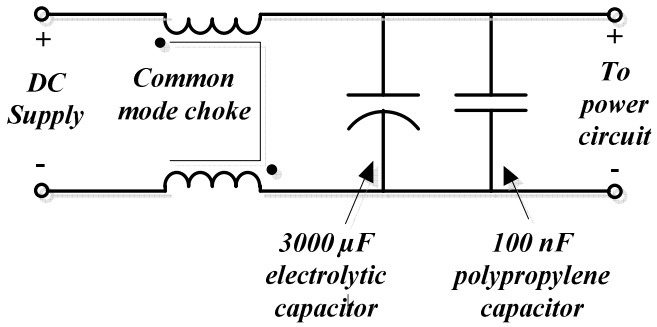


Fig. A.10: Dc link circuit diagram

(c) Module input capacitor

Two polypropylene 425V capacitors are connected in series at the module inputs. This is because this thesis studies, as in chapter six, the input-series connection of SPRC modules as a potential application for step down dc/dc converters from medium voltage to low voltage. The implemented capacitance values are made deliberately different to study input voltage sharing under extreme conditions (C_1=30µF and C_2=60µF).

(d) Module power inverter

The power inverter used is a two-level three phase IGBT-based inverter module. Each inverter leg contains two switches in series with antiparallel diodes for regenerative operation. Since the application in this thesis requires only a single-phase H-bridge type inverter, therefore one leg of the inverter is unused (gate signals shorted). The other two legs are connected to the resonant tank through the nano-crystalline core transformer. Two power inverters are used, one for each converter module. Both inverters are mounted on a heat sink for cooling. The inverter module implemented is a six pack 1200V/50A 6MBI50S-120-50 from Fuji Electric Ltd. Fig. A.11 shows the two power inverters mounted on the heat sink. Device main specifications are given by the datasheet.

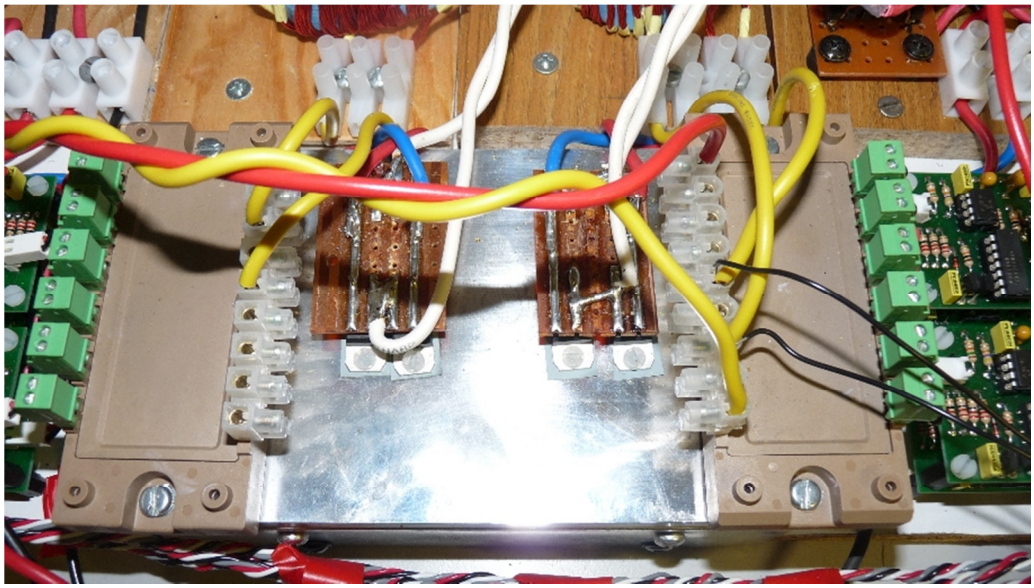


Fig. A.11: Module power inverters mounted on heat sink

3. Absolute Maximum Ratings (at Tc= 25℃ unless otherwise specified)

Items	Symbols	Conditions		Maximum Ratings	Units
Collector-Emitter voltage	VCES			1200	V
Gate-Emitter voltage	VGES			±20	V
Collector current	Ic	Continuous	Tc=25℃	75	A
			Tc=80℃	50	
	Ic pulse	1ms	Tc=25℃	150	
			Tc=80℃	100	
	-Ic			50	
	-Ic pulse	1ms		100	
Collector Power Dissipation	Pc	1 device		360	W
Junction temperature	Tj			150	℃
Storage temperature	Tstg			-40～ +125	℃
Isolation voltage(*1)	Viso	AC : 1min.		2500	V
Mounting Screw Torque (*2)				3.5	N・m

(*1) All terminals should be connected together when isolation test will be done.

(*2) Recommendable Value : 2.5～3.5 N・m (M5)

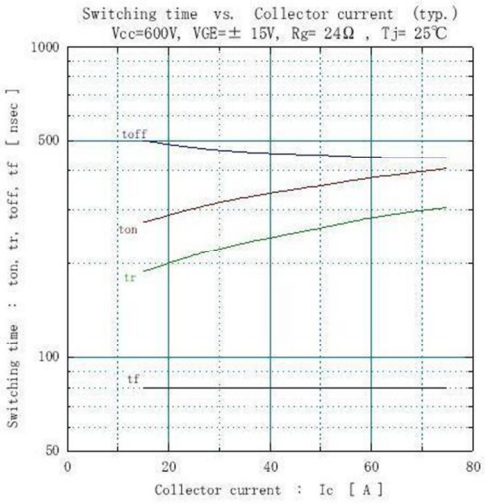
4. Electrical characteristics (at Tj= 25℃ unless otherwise specified)

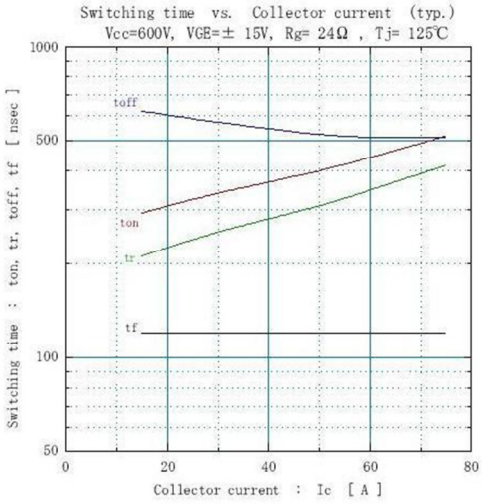
Items	Symbols	Conditions		Characteristics min.	typ.	Max.	Units
Zero gate voltage Collector current	ICES	VGE = 0 V, VCE = 1200 V		-	-	1.0	mA
Gate-Emitter leakage current	IGES	VCE = 0 V, VGE = ±20 V		-	-	200	nA
Gate-Emitter threshold voltage	VGE(th)	VCE = 20 V, Ic = 50 mA		5.5	7.2	8.5	V
Collector-Emitter saturation voltage	VCE(sat)	VGE = 15 V	Tj = 25 ℃	-	2.3	2.65	V
		Ic = 50 A	Tj = 125 ℃	-	2.8	-	
Input capacitance	Cies	VGE = 0 V		-	6000	-	pF
Output capacitance	Coes	VCE = 10 V		-	1250	-	
Reverse transfer capacitance	Cres	f = 1 MHz		-	1100	-	
Turn-on time	ton	Vcc = 600 V		-	0.35	1.2	μs
	tr	Ic = 50 A		-	0.25	0.6	
	$tr_{(i)}$	VGE = ±15 V		-	0.1	-	
Turn-off time	toff	RG = 24 Ω		-	0.45	1.0	
	tf			-	0.08	0.3	
Forward on voltage	VF	IF = 50 A	Tj = 25 ℃	-	2.5	3.3	V
			Tj = 125 ℃	-	2.0	-	
Reverse recovery time	trr	IF = 50 A		-	-	0.35	μs

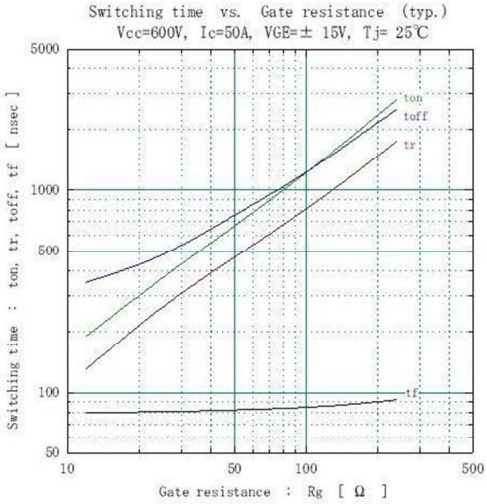
5. Thermal resistance characteristics

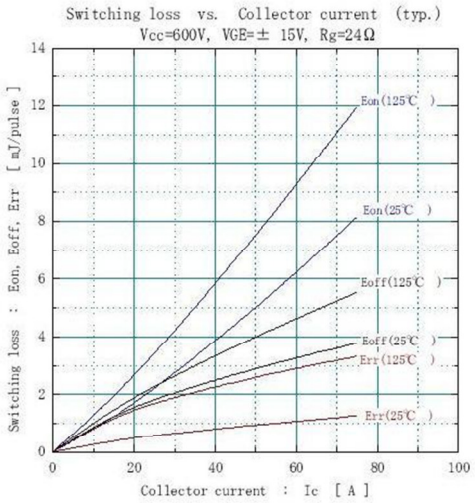
Items	Symbols	Conditions	Characteristics min.	typ.	Max.	Units
Thermal resistance (1 device)	Rth(j-c)	IGBT	-	-	0.35	℃/W
		FWD	-	-	0.75	
Contact Thermal resistance	Rth(c-f)	with Thermal Compound (※)	-	0.05	-	

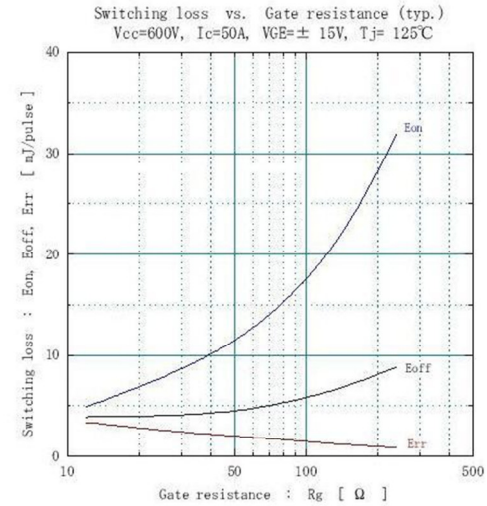
※ This is the value which is defined mounting on the additional cooling fin with thermal compound.

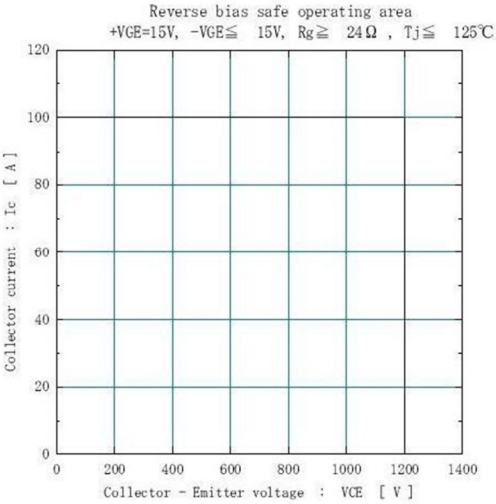












Fuji Electric Device Technology Co., Ltd.	DWG.NO.	MS5F 6174	11/14

(e) Nano-crystalline core transformer

Nano-crystalline material is favourable for high frequency operation due to its high core permeability, high magnetizing inductance, low losses and near square hysteresis loop. The transformer implemented in the experimental rig exploits nano-crystalline material due to the high inverter operating frequency (40kHz). Transformer primary is connected to inverter output and secondary winding is connected to the resonant tank. The transformer core selected, according to design procedure in chapter three, is the *Magnetec GmbH M-134-01 JM*. The core has relative permeability μ_r=30000 at 40kHz, core cross-sectional area A_c=0.8cm^2. Core dimensions and other specifications are outlined in the datasheet given. The laboratory implemented transformer is shown in Fig. A.12. Data for the two implemented transformers (one per converter module) are given in Table A.3. Turns ratio are deliberately mismatched to study converter current and voltage sharing under extreme operating conditions.

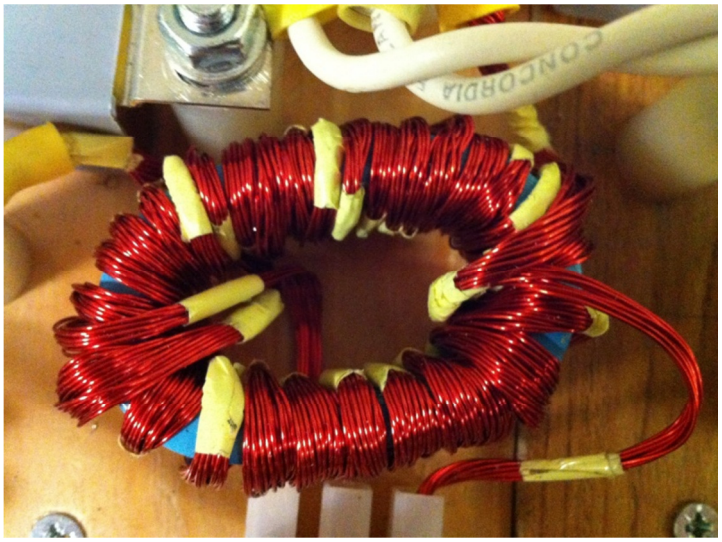


Fig. A.12: Nano-crystalline core transformer

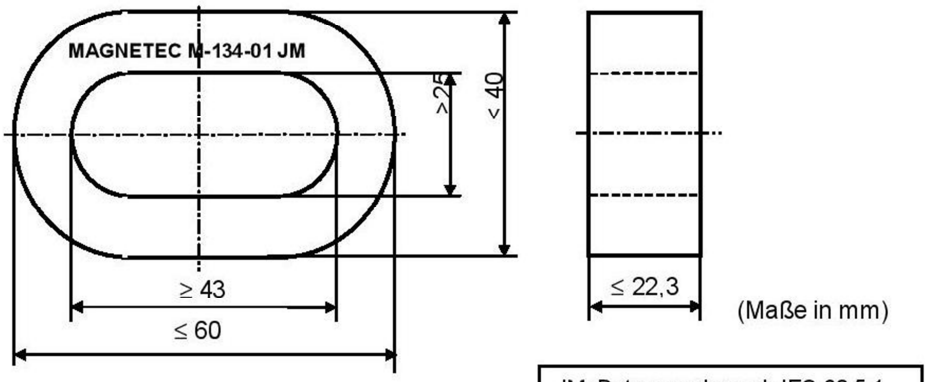
Parameter	***Module #1 transformer***	***Module #2 transformer***
Power rating	1 kVA	1 kVA
Primary winding emf	200 V(rms)	200 V(rms)
Secondary winding emf	100 V(rms)	100 V(rms)
Primary turns	20	18
Secondary turns	10	10
Turns ratio	0.5	0.555
Leakage inductance	9.12µH	8.78µH
Parasitic winding resistance	0.6Ω	0.51Ω

Table A.3: Nano-crystalline core transformer data

Ausgabe.00 Blatt 1 von 1	**Spezifikation** **für induktive Bauelemente**	**Magnetec GmbH** Industriestr. 7 D-63505 Langenselbold

Gegenstand:	EMV Wandler			Kunde:	Magnetec GmbH
Sachnummer:	M-134	Index:	01	Kundensach. Nr:	/

1. Maßbild Wandler:



(Maße in mm)

JM: Datumscode nach IEC 62 5.1

2. Ausführung: Ringbandkern epoxy-fixiert

3. Werkstoff: Nanoperm®

4. Kerndaten:

l_{FE}	=	14,1	cm
A_{Fe}	=	0,800	cm^2
m_{Fe}	=	83,1	g
η_{Fe}	=	0,80	/

5. Nennwerte: μ ca. 45.000 bei f = 10 kHz und H_{max} = 3,0 mA/cm

6. Magnetische Garantie: A_L = 20 µH bis 40 µH
bei f = 10kHz und I_{eff} x N = 30,0mA/Wdg. (Reihenersatzschaltbild)

7. Kennzeichnung: Bedruckt mit "Magnetec M-134-01 JM" (JM Fertigungsjahr/ Monat)

8. Verpackung: 14 St. Poron; 5 Poron pro Karton

Ausgabe:	Änderung:	Datum:	Name:
00		2001.08.13.	

Erstellt Datum:	02.08.2001	Geprüft Datum:	21.08.2001	Freigabe Datum:	17.08.2001
Name:	RJ	Name:	Csilla Tóthne	Name:	Martin Ferch

(f) LCC resonant tank

The LCC resonant tank is connected to the secondary winding of the nano-crystalline core transformer. It consists of an air-core inductor in series with a propylene film capacitor. Air-core is used for the inductor due to its linear magnetic characteristics and to avoid core saturation due to high frequency operation if normal ferrite cores are used. Polypropylene film capacitors are also suitable for high frequency operation. The parallel resonant capacitor is analogous to the series capacitor with its terminals connected across the bridge rectifier. Values of the resonant tank elements for the two converter modules at 40 kHz are defined in Table A.4. Fig. A.13 shows the implemented resonant tank in th experimental rig.

Element	*Module #1*	*Module #2*
Series inductance	100.13 µH	102.66 µH
Series capacitance	255 nF	255 nF
Parallel capacitance	255 nF	255 nF

Table A.4: Resonant tank element values

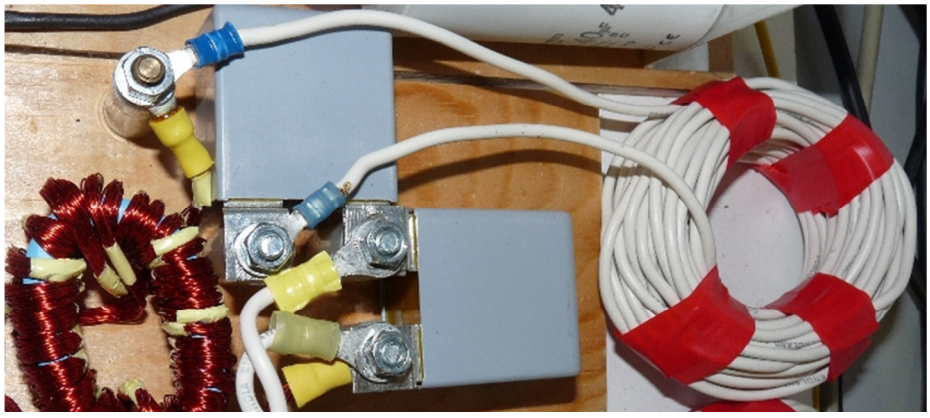


Fig. A.13: LCC resonant tank

(g) Bridge rectifier

The full bridge rectifier consists of four fast recovery diodes to rectify the parallel resonant capacitor voltage. Fast recovery diodes are essential due to the high fundamental frequency of the ac voltage across the capacitor. This ensures no overlapping conduction occurs between diodes in the same bridge leg due to delayed reverse recovery. Two bridge rectifiers are used, one per converter module. The diode switches used are the 600V/12A, ultrafast switching (25ns reverse recovery) STTH12R06 diodes from ST. the two bridge rectifiers are mounted on the same heat sink with the power inverters as shown in Fig. A.11. More device operating details can be found from the datasheet.

STTH12R06

Turbo 2 ultrafast high voltage rectifier

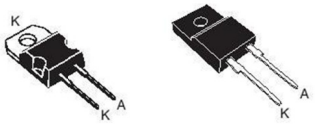
Features

- Ultrafast switching
- Low reverse recovery current
- Low thermal resistance
- Reduces switching losses
- Package insulation voltage:
  TO220AC ins: 2500 V_{RMS}
  TO-220FPAC: 2000 V_{DC}

Description

The STTH12R06 uses ST Turbo 2 600V technology and is specially suited as a boost diode in continuous mode power factor corrections and hard switching conditions.

This device is also intended for use as a free wheeling diode in power supplies and other power switching applications.



TO-220AC
STTH12R06D

TO-220FPAC
STTH12R06FP

D²PAK
STTH12R06G

TO-220AC insulated
STTH12R06DIRG

Table 1. Device summary

Symbol	Value
$I_{F(AV)}$	12 A
V_{RRM}	600 V
I_{RM} (typ)	7 A
T_j	175 °C
V_F (typ)	1.4 V
t_{rr} (max)	25 ns

1 Characteristics

Table 2. Absolute ratings (limiting values)

Symbol	Parameter			Value	Unit
V_{RRM}	Repetitive peak reverse voltage			600	V
$I_{F(RMS)}$	Forward rms current	TO-220AC / TO-220FPAC / D²PAK		30	A
		TO-220AC ins.		24	
$I_{F(AV)}$	Average forward current δ = 0.5	TO-220AC / D²PAK	T_c = 125 °C	12	A
		TO-220FPAC	T_c = 50 °C		
		TO-220AC ins.	T_c = 80 °C		
I_{FSM}	Surge non repetitive forward current		t_p = 10 ms sinusoidal	100	A
T_{stg}	Storage temperature range			-65 to + 175	°C
T_j	Maximum operating junction temperature			175	°C

Table 3. Thermal resistance

Symbol	Parameter		Value (max)	Unit
$R_{th(j-c)}$	Junction to case	TO-220AC / D²PAK	1.7	°C/W
		TO-220FPAC	4.4	
		TO-220AC ins.	3.3	

Table 4. Static electrical characteristics

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
I_R	Reverse leakage current	T_j = 25 °C	$V_R = V_{RRM}$			45	µA
		T_j = 125 °C			50	600	
V_F	Forward voltage drop	T_j = 25 °C	I_F = 12 A			2.9	V
		T_j = 125 °C			1.4	1.8	

To evaluate the conduction losses use the following equation:
$P = 1.16 \times I_{F(AV)} + 0.053\ I_{F^2(RMS)}$

Table 5. Dynamic Characteristics

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
t_{rr}	Reverse recovery time	T_j = 25 °C	I_F = 0.5 A, I_{rr} = 0.25 A, I_R = 1 A			25	ns
			I_F = 1 A, dI_F/dt = -50 A/µs, V_R = 30 V			45	
I_{RM}	Reverse recovery current	T_j = 125 °C	I_F = 12 A, V_R = 400 V, dI_F/dt = -200 A/µs		7.0	8.4	A
S factor	Softness factor				0.2		
Q_{rr}	Reverse recovery charges				180		nC
t_{fr}	Forward recovery time	T_j = 25 °C	I_F = 12 A, dI_F/dt = 96 A/µs, V_{FR} = 1.1 x V_{Fmax}			200	ns
V_{FP}	Forward recovery voltage					5.5	V

Figure 1. Conduction losses versus average current

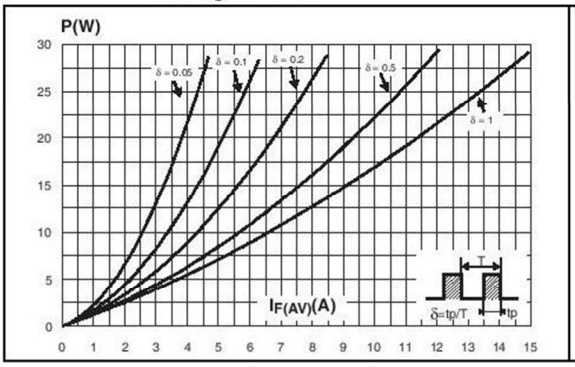


Figure 2. Forward voltage drop versus forward current

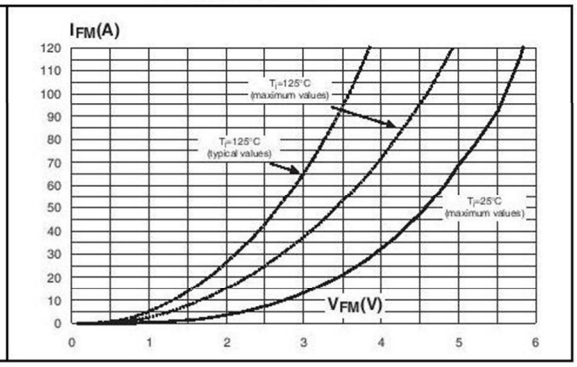


Figure 3. Relative variation of thermal impedance junction to case versus pulse duration

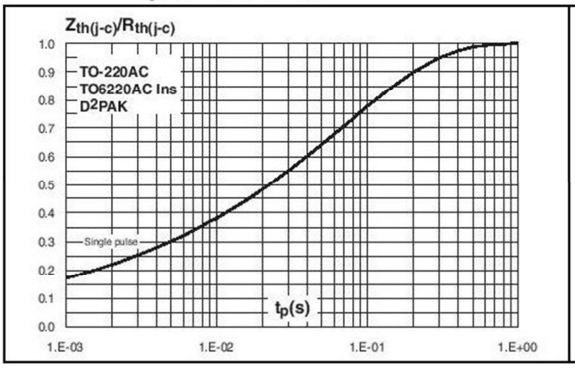
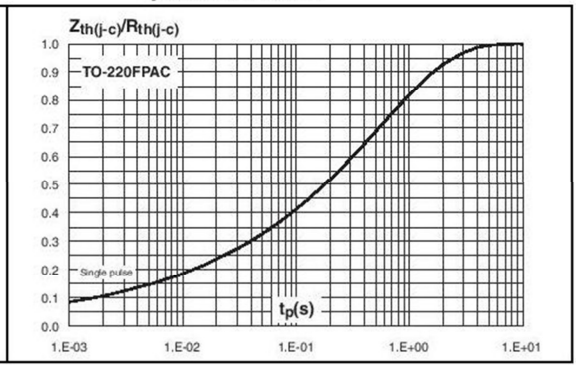


Figure 4. Relative variation of thermal impedance junction to case versus pulse duration



(h) Output LC filter

The function of the output LC filter is to attenuate even order harmonics from the bridge rectifier dc output and obtain low ripple output voltage. For this purpose, the LC filter is designed with a large time constant relative to the fast dynamics of the resonant tank to perform better filtering. Inductor current and output capacitor voltage ripple contents can be designed using the design equations in chapter three. The inductor used utilises

an internal air gap in its design to provide high reluctance path for core flux to avoid saturation resulting from operation with dc current. Filter LC parameters for both converter modules are L_{o1}=L_{o2}=12.5mH and C_{o1}=C_{o2}=120μF. Fig. A.14 shows the LC filter implemented in the experimental rig.

(a) (b)

Fig. A.14: Output LC filter (a) inductance, and (b) capacitance

(i) Cable impedance

In real world, load may be remotely located from the main converter site. Interconnecting cables have finite impedance which, accordingly, has to be taken into account for accurate dynamic and steady-state system modelling. To emulate this phenomenon in the laboratory, typical cable impedance data are used from providers such American Wire Gauge (AWG) and implemented using lump RL elements. Table A.5 states the values of the implemented cable impedances for the two converter modules. Note that they are selected to be different to assess current and voltage sharing under extreme operating conditions. Fig A.15 shows a sample of the implemented lump RL cable impedance emulator.

Parameter	***Module #1 cable***	***Module #2 cable***
Parasitic resistance	0.2Ω	0.3Ω
inductance	1 mH	2 mH

Table A.5: Cable impedance values

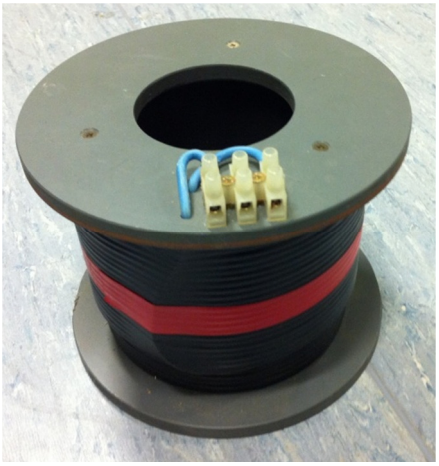


Fig. A.15: Cable impedance emulator

(j) Load

The converter is loaded with resistive load for testing the behaviour of the various proposed control techniques under partial load (R_{LPL}) and full-load (R_{LFL}). A step load increase is applied to assess the controller's dynamic response and disturbance rejection capabilities. A 7.2 kW, 240V, 10A three-phase resistive load is readily available in the laboratory which is shown in Fig. A.16. Necessary connections are used to reach required operating resistance values. Operating partial and full-load values are listed in Table A.6 for the different operating modes of the converter.

Operating mode	***Partial load resistance (R_{LPL})***	***Full-load resistance (R_{LFL})***
Single-module	40.5 Ω	14.4 Ω
Multi-module (ISOP connection)	20.25 Ω	7.2 Ω
Multi-module (ISOS connection)	81 Ω	28.8 Ω

Table A.6: Resistive load values implemented for the different converter operating modes

Fig. A.16: Resistive load

A.1.3 Recording and monitoring devices

Devices to measure, monitor and record voltages and currents from the experimental prototype are necessary. A brief account is given about such devices in this section.

(a) Low pass filter circuit for DSP analogue output

The Infineon Tricore DSP used does not provide an on-chip digital to analog converter. Calculated control or state variables within the DSP program code are sometimes needed to be viewed online as they dynamically change and not offline. Examples include the display of control phase-shift angle δ and the comparison of estimated state variables produced by the new model introduced in chapter four with actual circuit measurements.

This can be obtained by pulse width modulating the required signal (to be viewed) with a high frequency carrier signal (carrier frequency implemented is 40 kHz). The modulated digital output signal is passed through a sixth-order Butterworth low pass filter whose cut-off frequency is 4 kHz. Fig. A.17 shows the low pass filter conditioning circuit where the low pass filter is realized using quad op-amp LM2902. Circuit diagram is illustrated in Fig. A.18 and circuit parameter values are listed in Table A.7.

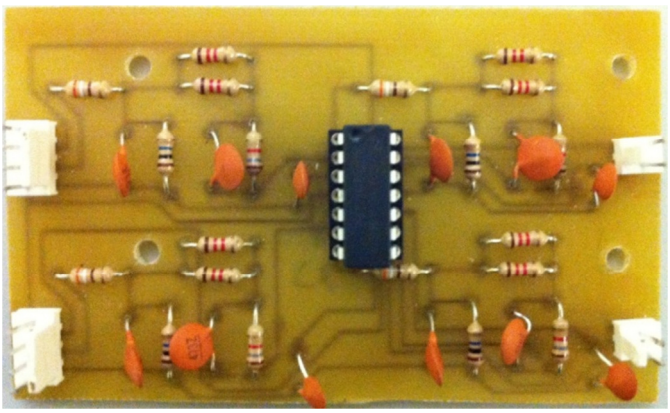


Fig. A.17: Low pass filter circuit for DSP analogue output

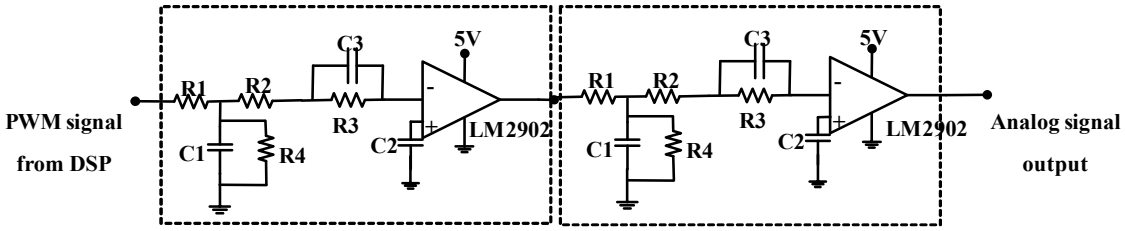


Fig. A.18: Circuit diagram for Low pass filter circuit for DSP analogue output

R1= 400 Ω	C1= 0.1 μF
R2= 600 Ω	C2= 0.01 μF
R3= 1.8 Ω	C3= 0.047 μF
R4= 1 MΩ	

Table A.7: Low pass filter circuit parameters

LM324, LM324A, LM224, LM2902, LM2902V, NCV2902

Single Supply Quad Operational Amplifiers

The LM324 series are low−cost, quad operational amplifiers with true differential inputs. They have several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 V or as high as 32 V with quiescent currents about one−fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

Features

- Short Circuited Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 32 V
- Low Input Bias Currents: 100 nA Maximum (LM324A)
- Four Amplifiers Per Package
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Industry Standard Pinouts
- ESD Clamps on the Inputs Increase Ruggedness without Affecting Device Operation
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes
- Pb−Free Packages are Available

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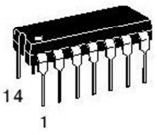
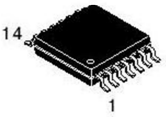
http://onsemi.com



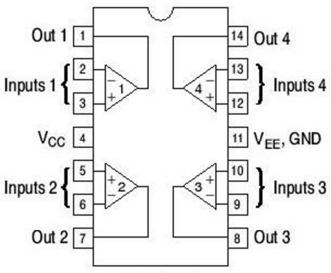
PDIP−14
N SUFFIX
CASE 646

SOIC−14
D SUFFIX
CASE 751A



TSSOP−14
DTB SUFFIX
CASE 948G

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 12 of this data sheet.

LM324, LM324A, LM224, LM2902, LM2902V, NCV2902

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages Single Supply Split Supplies	 V_{CC} V_{CC}, V_{EE}	 32 ±16	Vdc
Input Differential Voltage Range (Note 1)	V_{IDR}	±32	Vdc
Input Common Mode Voltage Range	V_{ICR}	−0.3 to 32	Vdc
Output Short Circuit Duration	t_{SC}	Continuous	
Junction Temperature (Note 2)	T_J	150	°C
Thermal Resistance, Junction−to−Air (Note 3) Case 646 Case 751A Case 948G	$R_{\theta JA}$	118 156 190	°C/W
Storage Temperature Range	T_{stg}	−65 to +150	°C
ESD Protection at any Pin Human Body Model Machine Model	V_{esd}	 2000 200	V
Operating Ambient Temperature Range LM224 LM324, 324A LM2902 LM2902V, NCV2902 (Note 4)	T_A	 −25 to +85 0 to +70 −40 to +105 −40 to +125	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Split Power Supplies.
2. For supply voltages less than 32 V, the absolute maximum input voltage is equal to the supply voltage.
3. All $R_{\theta JA}$ measurements made on evaluation board with 1 oz. copper traces of minimum pad size. All device outputs were active.
4. *NCV2902 is qualified for automitive use.*

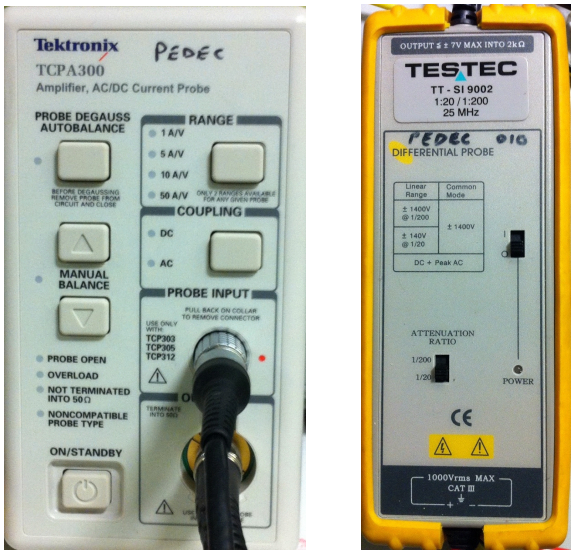
(b) Multimeters

Multimeters for measuring currents and voltages at various circuit points are necessary. Although the multimeters only provide mean or rms measurements, these are yet important for circuit monitoring due to the possibility of short circuit fault occurrence. The multimeters used can measure up to 1000V and 10A. It is shown in Fig. A.19.

Fig. A.19: Mulitmeter for circuit current and voltage monitoring

(c) Current and voltage probes

In order to record and view current and voltage signals on oscilloscope, test probes are necessary for signal conditioning and isolation. The oscilloscope demands same-ground signal inputs to its channels. However, different signals at different circuit locations may need to be measured simultaneously. Also, appropriate signal scaling is needed to view high and low voltages. Grounding isolation and signal conditioning are performed by the test probes. A Tektronix TCPA300 current probe and TESTEC TT-SI9002 voltage probe, both with high frequency precision, are used in the test rig. These are shown in Fig. A.20.



(a) (b)

Fig. A.20: Test probes (a) current, and (b) voltage.

(d) Oscilloscope

A 20 MHz, 20GS/s four-channel TDS2024 digital storage oscilloscope from Tektronix is used for measuring and recoding voltages and currents for the different control algorithms. The oscilloscope is shown in Fig. A.21.

Fig. A.21: Digital oscilloscope.

A.2 DSP software environment

Software environment to implement the DSP control algorithms consists of two development tools; Digital Application Virtual Engineer (DAVE) and TASKING Embedded Development Environment (TASKING EDE). The PC is used to host the two software programs, write, debug, compile and download the code to the Infineon Tricore DSP via the parallel port. The final code is then stored in the DSP EPROM. Brief descriptions of both software packages are given in this section.

A.2.1 DAVE

DAVE is the package to initially configure the TC1796 DSP registers and generate optimized C-code. The system clock is set to 10 MHz in the General Purpose Timer Arrays (GPTA) clock module. PWM generation timers are configured in the GPTA0. Seventeen local timer cells (LTC) are used to generate 4 gate signals for each module inverter, i.e. a total of 8 gate signals for the two converter modules. The first LTC is clocked by the 10 MHz system bus clock with 0.1μs period. It is configured to produce an interrupt every pre-defined number of clock pulses to determine the carrier or switching period. In this work, it counts 250 clock pulses per switching cycle, hence achieving a switching frequency of 40kHz. The remaining local timer cells are configured in the compare mode to determine the rising and falling edge of the gate signals during one switching cycle. In other words, two LTCs are used to generate one gate signal; one for the rising edge and the other for the falling edge. For protection, the LTCs mode can be changed to push the output to be zero in case of short circuit and over loading conditions. Additional LTCs are used for the PWM signals required for the analogue output.

Fast analogue to digital converter (FADC) is also configured for the measured voltages and current signals. This operates with 10-bit resolution and programmable conversion times up to 280ns per channel. FADC is necessary since time for entire program execution (including analogue to digital conversions, control computations and PWM signal generation) is only 25μs. Four FADC channels are available. In case of multi-module converter operation, these four channels are used to measure the two input capacitor voltages and the two output filter inductor currents. Sensing load voltage is compensated for by the sensorless load voltage estimation algorithm proposed in chapter six. This means that the four available FADC channels are sufficient for the application.

Finally, compilation of the DAVE project file generates optimized C-code template files with initially configured DSP registers. Generated files include main.h, main.c, GPTA0.h and GPTA0.c. These files contain the basic program structure to be completed by insertion of the required control algorithm in TASKING EDE. Fig. A.22 shows the general interface configuration for DAVE v2.1.

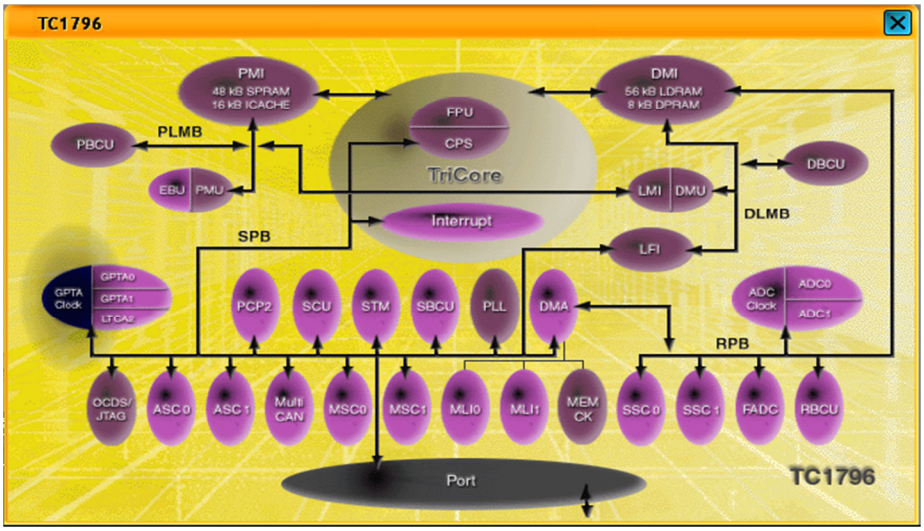


Fig. A.22: DAVE v2.1

A.2.2 TASKING EDE

TASKING EDE is a package of program building, editing, code generation and debugging tools. Options such as the DSP on-chip memory used can be further configured with TASKING EDE. Files with configured registers are imported from DAVE and loaded into TASKING EDE. Necessary user codes to implement the proposed control algorithms are written in ANSI-standard C-code and inserted into the generated templates. The code is then debugged and compiled to generate a hex file. The latter is downloaded to the DSP EPROM using a software platform called Crossview Pro Debugger embedded within TASKING EDE. Crossview has no real time monitoring capability but enables offline variable monitoring. Sample C-codes developed by the author can be found in Appendix D.

Appendix B

Jury Stability Criterion for Lyapunov Controller

The discretized system closed-loop characteristic equation can be expressed as

$$a_2 z^2 + a_1 z + z_0 = 0 \tag{B.1}$$

where, $a2 = \frac{1}{T_S{}^2}$, $a1 = \frac{2}{\pi L_O C_O T_S} k_d - \frac{2}{T_S{}^2}$, $a0 = \frac{2}{\pi L_O C_O} k_p - \frac{2}{\pi L_O C_O T_S} k_d + \frac{1}{T_S{}^2}$

Jury stability criterion for the closed-loop system is outlined in Table B.1.

Row number	***Operation***	***Coefficients***		
R1	Characteristic equation coefficients	a_2	a_1	a_0
R2	Reverse order of *R1* coefficients	a_0	a_1	a_2
R3	$R1 - R2 \times \frac{a_0}{a_2}$	b_2	b_1	*0*
R4	Reverse order of *R3* non-zero coefficients	b_1	b_2	*0*
R5	$R3 - R4 \times \frac{b_1}{b_2}$	c_2	*0*	*0*

Table B.1: Jury stability criterion

Coefficients b_1, b_2 and c_2 in Table B.1 can be defined as

$$b_1 = a_1 - \frac{a_0 a_1}{a_2}, \qquad b_2 = a_2 - \frac{a_0{}^2}{a_2}, \qquad c_2 = b_2 - \frac{b_1{}^2}{b_2} \tag{B.2}$$

According to Jury, closed-loop system is stable if coefficients of the odd-numbered rows of the first column are positive

$$a_2 > 0, \qquad b_2 > 0, \qquad c_2 > 0 \tag{B.3}$$

Applying (B.3) and using coefficient definitions in (B.1) and (B.2), the closed-loop system is stable if

$$a2 > 0 \Rightarrow \frac{1}{T_S{}^2} > 0 \tag{B.4}$$

$$a_2 > a_0 \Rightarrow \frac{1}{{T_s}^2} > \left(\frac{2}{\pi L_o C_o} k_p - \frac{2}{\pi L_o C_o T_s} k_d + \frac{1}{{T_s}^2} \right) \tag{B.5}$$

$$a_2 + a_0 > a_1 \Rightarrow \left(\frac{1}{{T_s}^2} + \frac{2}{\pi L_o C_o} k_p - \frac{2}{\pi L_o C_o T_s} k_d + \frac{1}{{T_s}^2} \right) > \left(\frac{2}{\pi L_o C_o T_s} k_d - \frac{2}{{T_s}^2} \right) \tag{B.6}$$

Condition (B.4) is inevitable as the sampling period T_s is always a positive variable. Therefore, stability conditions (B.5) and (B.6) can re-formulated into their final forms

$$\begin{aligned} k_p &< \frac{k_d}{T_s} \\ k_p &> \frac{2k_d}{T_s} - \frac{2\pi L_o C_o}{{T_s}^2} \end{aligned} \tag{B.7}$$

Appendix C

Matlab Software Programs

In this appendix, details of realisation of the Kalman filter state estimation algorithm used in chapter four as well as the load voltage estimator used in chapter six are given. The Kalman filter is written in Matlab m-file using an s-function and is then converted using Simulink embedded compiler to equivalent C-code that is compatible with the Tricore Infineon DSP. The algorithm is then called as a function in the main DSP code given in Appendix D (section D.3). The load voltage estimation algorithm introduced in chapter six is built using Simulink and compiled using the same method and used within the main DSP code for multi-module converter operation (complete DSP code given in Appendix D section D.1).

C.1 Kalman filter code for state variable estimation

Fig. C.1 shows the s-function in Simulink necessary for the practical implementation of the Kalman filter state estimation algorithm. The m-file code follows.

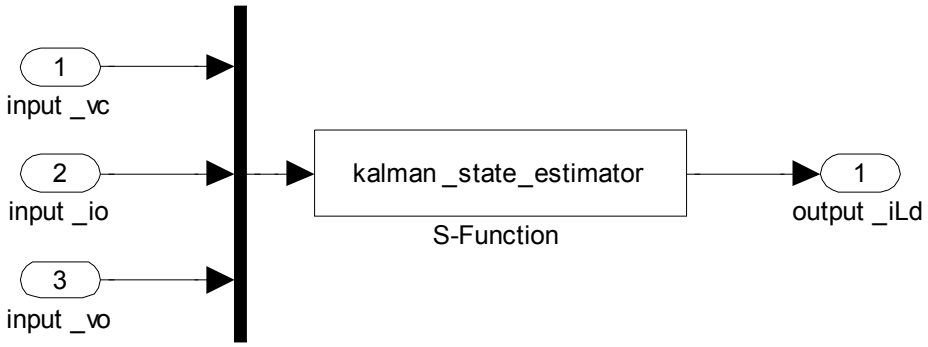


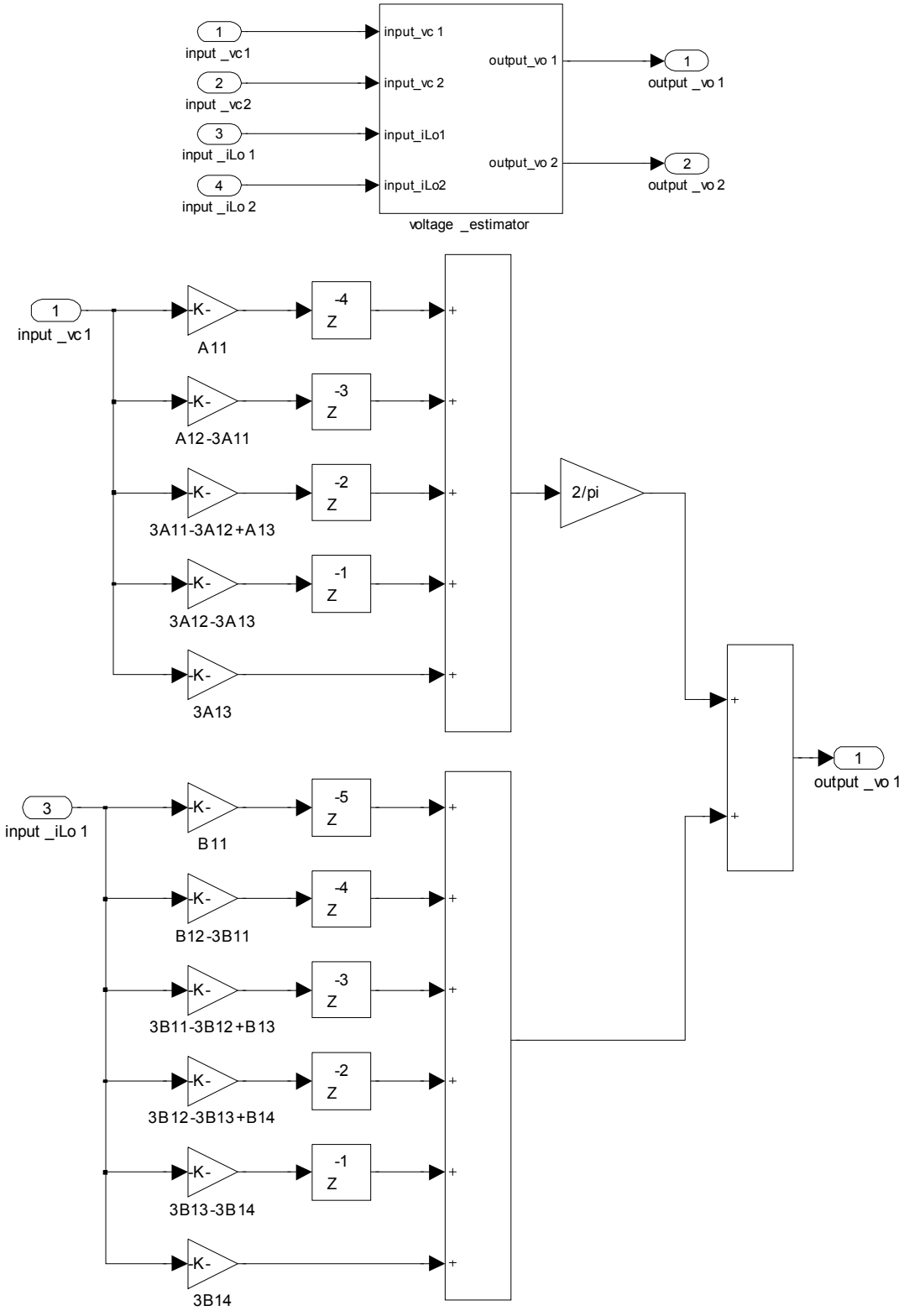
Fig. C.1: Kalman filter state estimator as an s-function in Simulink

```
function [sys,x0,str,ts] = kalman_state_estimator(t,x,u,flag)
global A B C D Ad Bd f T rLs Ls Cs Cp rLo Lo Co ws rT LT rl Ll k1 k3 k5 k7 Pk xk_ Pk_ Q
Lk H R xk sys_c sys_d

switch flag,
  case 0
    sys = [0,8,1,3,0,1,1]; %8 discrete states, 3 inputs (vc, io and the measurement vo) and
                           %1 output (iLd)
    x0=zeros(8,1);
    str=[];
    f=40000;
    T=1/f; %sampling period
    ts  = [T 0];
    Pk=zeros(8,8);   %error covariance
    Q=eye(8)*0.001;  %process noise covariance
```

```
H=[0 0 0 0 0 0 0 1]; % measurement vector used for correcting the initial estimation
                     %(measurement z(k)=vo)
R=0.001; %measurement noise covariance

rLs=0.1916;
Ls=100.13e-6;
Cs=255.22e-9;
Cp=Cs;
rLo=0.5;
Lo=12.5e-3;
Co=120e-6;
rl=0.6;
Ll=9.12e-6;
rT=rl+rLs;
LT=Ll+Ls;
ws=2*pi*f;

k1=(1+(Cp/Cs)-(ws^2*Cp*LT));
k3=rT;
k5=rT*ws*Cp;
k7=(ws*LT)-(1/ws/Cs)

A=[-rT/LT ws -1/LT 0 -1/LT 0 4*k3/pi/LT 0;-ws -rT/LT 0 -1/LT 0 -1/LT 4*k7/pi/LT 0;1/Cs
    0 0 ws 0 0 0 0;0 1/Cs -ws 0 0 0 0 0;1/Cp 0 0 0 0 ws -4/pi/Cp 0;0 1/Cp 0 0 -ws 0 0 0;0 0 0
   0 2/pi/Lo 0 -rLo/Lo -1/Lo;0 0 0 0 0 0 1/Co 0];
B=[k1/LT 0;k5/LT 0;0 0;0 0;0 0;0 0;0 0;0 -1/Co];
C=[1 0 0 0 0 0 0 0]; %output of the estimator is iLd (the first state variable)
D=zeros(1,2);

sys_c=ss(A,B,C,D);
sys_d=c2d(sys_c,T);
Ad=sys_d.a;
Bd=sys_d.b;

case 2

xk_=Ad*x+Bd*[u(1);u(2)]; %project the state ahead
Pk_=Ad*Pk*Ad'+Q; %project the error covariance ahead

sys=xk_;

case 3


Lk=Pk_*H'*inv(H*Pk_*H'+R); %compute the kalman gain
xk=xk_+(Lk*(u(3)-H*xk_)); % update state estimates with measurement z(k)=vo
Pk=(eye(8)-Lk*H)*Pk_; %update the error covariance
sys=C*xk; %output of the estimator is iLd (the first state variable)

case {2,4,9}
  sys=[];

otherwise
 error(['Unhandled flag = ',num2str(flag)]);
end
```

C.2 Load voltage estimation

Fig. C.2 shows the block Simulink diagram for the load voltage estimation algorithm introduced in chapter six. The diagram implements equations (6.11) and (6.12). Coefficients are defined in chapter 6, equations (6.6) and (6.7).



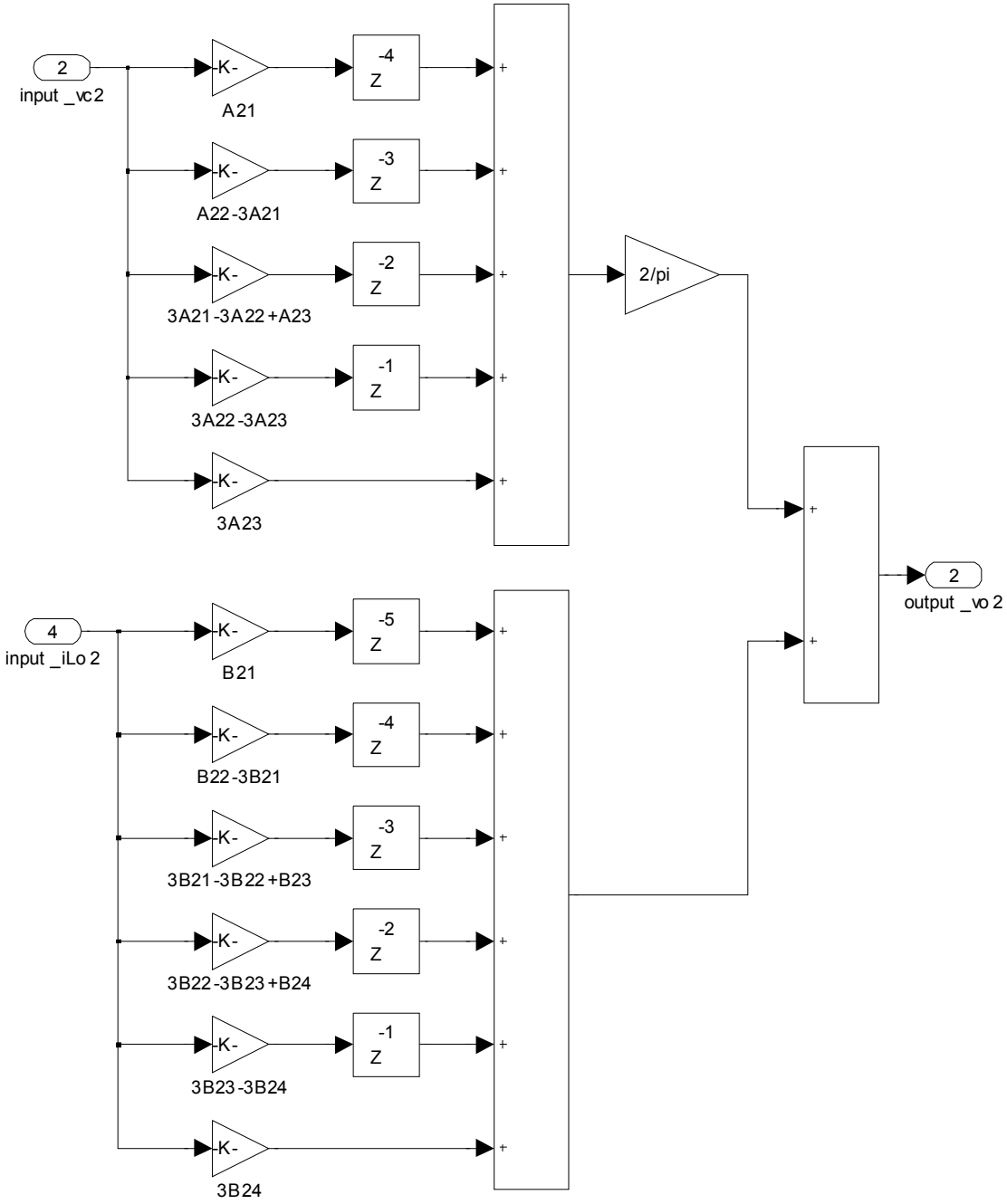


Fig. C.2: Simulink block diagram of load voltage estimation algorithm

Appendix D

Sample DSP Codes for Experimental Implementation

C-codes for selected control algorithms proposed in this thesis are presented here; namely, multi-module ISOP converter operation (chapter six), the sliding mode controller (chapter five) and the Kalman filter based sensorless multi-loop PI controller (chapter four). For the sake of simplicity and clarity of code presented, introductory portions of the code with DSP register configurations are omitted. Only variable declarations and the control algorithm code implemented are included here.

D.1 Multi-module converter operation

```
// USER CODE BEGIN (GPTA0_General,2)
#include "MAIN.h"
#include "stdio.h"
#include "math.h"
#include "rtwtypes.h"
#include "voltage_estimator.h"
#include "voltage_estimator_private.h"
#include "voltage_estimator_types.h"

int m=0, db=5, del1=0, del2=0, analog1=0, analog2=0;
float Dis1[2000], Dis2[2000], Dis3[2000];
float Vo=0, Vo1=0, Vo2=0, ILo1=0, ILo2=0, Vs1=0, Vs2=0;
float fadc_res0=0, fadc_res1=0, fadc_res2=0, fadc_res3=0;
float k1_1=0.2403, k3_1=0.7916, k5_1=0.0507, k7_1=11.8541;
float k1_2=0.205, k3_2=0.73, k5_2=0.0408, k7_2=12.4045;
float Kp=11.3313,Kd=0.0047, K=10.0;
float rLo1=0.5, rc1=0.2, rLo2=0.5, rc2=0.3, n1=0.5, n2=0.555, pi=3.14;
float  Voref=24, Vsref=0;
float vcon1=0, vcon2=0, ve1=0, ve2=0;
float VerrOld=0, VerrNew=0, VABd1=0, VABq1=0, VABd2=0, VABq2=0 ;
float VAB1=0, VAB2=0, Y=0, YoPD=0, delta1=0, delta2=0, vc1=0, vc2=0;
// USER CODE END

// USER CODE BEGIN (SRN22,4)
P3_OUT_P8=0; // reset pin 3.8 at program start and set at program end to calculate pro
                    //gram execution time using pulse width
////////////////////////////////////////////////////////////////////////////////
////OUTPUT GATE SIGNALS FOR CONVERTER 1////
////////////////////////////////////////////////////////////////////////////////
GPTA0_LTCXR02=db;
GPTA0_LTCXR03=124;
GPTA0_LTCXR04=249;
GPTA0_LTCXR05=124+db;
```

```
GPTA0_LTCXR06=db+del1;
GPTA0_LTCXR07=del1+124;
GPTA0_LTCXR08=del1;
GPTA0_LTCXR09=124+db+del1;
////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
////OUTPUT GATE SIGNALS FOR CONVERTER 2 WITH INTERLEAVING//////////
////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
GPTA0_LTCXR10=db+62;
GPTA0_LTCXR11=186;
GPTA0_LTCXR12=62;
GPTA0_LTCXR13=186+db;
GPTA0_LTCXR14=62+db+del2;
GPTA0_LTCXR15=del2+186;
GPTA0_LTCXR16=del2+62;
GPTA0_LTCXR17=186+db+del2;
////////////////////////////////////////////////////////////////////////
////////////////////ANALOG FILTER OUTPUT//////////
////////////////////////////////////////////////////////////////////////
GPTA0_LTCXR18=1;
GPTA0_LTCXR19=analog1;
GPTA0_LTCXR20=1;
GPTA0_LTCXR21=analog2;
////////////////////////////////////////////////////////////////////////////////////////////////////////////////
////////////FAST ADC CONVERSION for Vs1, Vs2, ILo1 and ILo2//////////
////////////////////////////////////////////////////////////////////////////////////////////////////////////////
FADC_vStartTimer(0,1);
FADC_vStopTimer(0);
fadc_res0=FADC_vGetChannelConversionResult(0);

FADC_vStartTimer(1,1);
FADC_vStopTimer(1);
fadc_res1=FADC_vGetChannelConversionResult(1);

FADC_vStartTimer(2,1);
FADC_vStopTimer(2);
fadc_res2=FADC_vGetChannelConversionResult(2);

FADC_vStartTimer(3,1);
FADC_vStopTimer(3);
fadc_res3=FADC_vGetChannelConversionResult(3);

Vs1=fadc_res0*100.0/1023.0; // 10-bit resolution conversion
Vs2=fadc_res1*100.0/1023.0;
ILo1=fadc_res2*5.0/1023.0;
ILo2=fadc_res3*5.0/1023.0;
////////////////////////////////////////////////////////////////////////
///////////////LYAPUNOV CONTROLLER //////////////
////////////////////////////////////////////////////////////////////////
VerrNew=Voref-Vo;
Y=40000.0*(VerrNew-VerrOld)*Kd;
```

```
VerrOld=VerrNew;
YoPD=Y+Kp*VerrNew;

vcon1=YoPD+(((ILo1*(rLo1+rc1))+Vo1)*pi/2.0);
vcon2=YoPD+(((ILo2*(rLo2+rc2))+Vo2)*pi/2.0);
////////////////////////////////////////////////////////////////////////////////
///////////////AVERAGE IVS SHARING CONTROL //////////////
////////////////////////////////////////////////////////////////////////////////
Vsref=0.5*(Vs1+Vs2);
ve1=(Vsref-Vs1)*K;
ve2=(Vsref-Vs2)*K;
////////////////////////////////////////////////////////////////////////////////////////////
//////////////////CALCULATION OF PHASE SHIFT/////////////////////
////////////////////////////////////////////////////////////////////////////////////////////
vc1=vcon1-ve1;
vc2=vcon2-ve2;

VABd1=(k1_1*vc1)+(k3_1*ILo1*4.0/pi);
VABq1=(k5_1*vc1)+(k7_1*ILo1*4.0/pi);
VAB1=sqrt(VABd1*VABd1+VABq1*VABq1);

VABd2=(k1_2*vc2)+(k3_2*ILo2*4.0/pi);
VABq2=(k5_2*vc2)+(k7_2*ILo2*4.0/pi);
VAB2=sqrt(VABd2*VABd2+VABq2*VABq2);

delta1=2.0*asin(VAB1*pi/4.0/Vs1/n1);
delta2=2.0*asin(VAB2*pi/4.0/Vs2/n2);
del1=floor(delta1*125.0/pi);
if(del1>125.0)
{ del1=125.0; }
del2=floor(delta2*125.0/pi);
if(del2>125.0)
{ del2=125.0; }
////////////////////////////////////////////////////////////////////////////
//////////LOAD VOLTAGE ESTIMATOR//////////////////
////////////////////////////////////////////////////////////////////////////
voltage_estimator_U.input_vc1=vc1;
voltage_estimator_U.input_vc2=vc2;
voltage_estimator_U.input_iLo1=ILo1;
voltage_estimator_U.input_iLo2=ILo2;
voltage_estimator_step();
Vo1= voltage_estimator_Y.output_vo1;
Vo2= voltage_estimator_Y.output_vo2;

Vo=0.5*(Vo1+Vo2);
////////////////////////////////////////////////////////////////////////////
//////////////////////////////DISPLAY//////////////////////////////
////////////////////////////////////////////////////////////////////////////
analog1=del1*249.0/125.0;
analog2=del2*249.0/125.0;
```

```
if (m==2000)
m=0;
Dis1[m]=Vo;
Dis2[m]=Vo1;
Dis3[m]=Vo2;
++m;

 P3_OUT_P8=1;

 // USER CODE END
//  End of function GPTA0_viSRN22
```

D.2 Sliding mode controller

```
// USER CODE BEGIN (GPTA0_General,2)
#include "MAIN.h"
#include "stdio.h"
#include "math.h"

int m=0, db=5, del=0, analog1=0, analog2=0;
float Dis1[2000], Dis2[2000], Dis3[2000];
float Vo_old=0, Vo_new=0, ILo=0;
float fadc_res0=0, fadc_res1=0;
float k1=0.2403, k3=0.7916, k5=0.0507, k7=11.8541;
float Kp=1000.0,Kd=1.0, Ki=250000.0;
float n=0.5, pi=3.14, Voref=24.0, Vs=60.0;
float VerrOld=0, VerrNew=0,Ynew=0, Yold=0, VABd=0, VABq=0, VAB=0;
float Y=0, Yo=0, delta=0, vc=0, vcmin=0, vcmax=41.5, X=0, CON=0, S=0, u=0;
// USER CODE END

// USER CODE BEGIN (SRN22,4)
P3_OUT_P8=0; // reset pin 3.8 at program start and set at program end to calculate pro
                    //gram execution time using pulse width
//////////////////////////////////////////////////////////////
///////////OUTPUT GATE SIGNALS ///////////
//////////////////////////////////////////////////////////////
GPTA0_LTCXR02=db;
GPTA0_LTCXR03=124;
GPTA0_LTCXR04=249;
GPTA0_LTCXR05=124+db;
GPTA0_LTCXR06=db+del;
GPTA0_LTCXR07=del+124;
GPTA0_LTCXR08=del;
GPTA0_LTCXR09=124+db+del;
//////////////////////////////////////////////////////////////////////////
//////////////////////ANALOG FILTER OUTPUT//////////
//////////////////////////////////////////////////////////////////////////
GPTA0_LTCXR18=1;
```

```
GPTA0_LTCXR19=analog1;
GPTA0_LTCXR20=1;
GPTA0_LTCXR21=analog2;
////////////////////////////////////////////////////////////////////////////////
//////////////FAST ADC CONVERSION for Vo and ILo//////////
////////////////////////////////////////////////////////////////////////////////
FADC_vStartTimer(0,1);
FADC_vStopTimer(0);
fadc_res0=FADC_vGetChannelConversionResult(0);

FADC_vStartTimer(1,1);
FADC_vStopTimer(1);
fadc_res1=FADC_vGetChannelConversionResult(1);

Vo_new=fadc_res0*100.0/1023.0;  //10-bit resolution conversion
ILo=fadc_res1*5.0/1023.0;
////////////////////////////////////////////////////////////////////////////
///////////////SLIDING MODE CONTROLLER ///////////////
////////////////////////////////////////////////////////////////////////////
VerrNew=Vo_new-Voref;
Ynew=Yold+((0.000025/2.0)*(VerrOld+VerrNew))*Ki+X;
Yold=Ynew;
VerrOld=VerrNew;
Y=40000.0*(Vo_new-Vo_old)*Kd;
Vo_old=Vo_new;
Yo=Ynew+Y+Kp*Vo_new;

CON=Yo;

if(Yo>100.0)
{   CON=100.0;  }
 if(Yo<0.0)
{ CON =0.0;  }

X=(CON-Yo)*Ki; // anti-windup to reset integrator
S=CON; // sliding surface


if(S>0)
{   u=1.0;  }
 if(S<0)
{ u=0;  }

vc=vcmax+((vcmin-vcmax)*u);
////////////////////////////////////////////////////////////////////////////////////////
//////////////////CALCULATION OF PHASE SHIFT/////////////////////
////////////////////////////////////////////////////////////////////////////////////
VABd=(k1*vc)+(k3*ILo*4.0/pi);
VABq=(k5*vc)+(k7*ILo*4.0/pi);
VAB=sqrt(VABd*VABd+VABq*VABq);
```

```
delta=2.0*asin(VAB*pi/4.0/Vs/n);
del=floor(delta*125.0/pi);
if(del>125.0)
{ del=125.0; }
////////////////////////////////////////////////////////////////////////
//////////////////////////////DISPLAY///////////////////////////////////
////////////////////////////////////////////////////////////////////////
analog1=del*249.0/125.0;
analog2=vc*249.0/37.7;

if (m==2000)
m=0;
Dis1[m]=Vo;
Dis2[m]=ILo;
Dis3[m]=u;
++m;

 P3_OUT_P8=1;

 // USER CODE END
//  End of function GPTA0_viSRN22
```

D.3 Sensorless multi-loop PI output voltage controller

```
// USER CODE BEGIN (GPTA0_General,2)
#include "MAIN.h"
#include "stdio.h"
#include "math.h"
#include "rtwtypes.h"
#include "kalman_state_estimator.h"
#include "kalman_state_estimator.h"
#include "kalman_state_estimator.h"


int m=0, db=5, del=0, analog1=0, analog2=0;
float Dis1[2000], Dis2[2000], Dis3[2000];
float Vo=0, ILo=0;
float fadc_res0=0, fadc_res1=0;
float k1=0.2403, k3=0.7916, k5=0.0507, k7=11.8541;
float Kp=0.1, Ki=10.0, K=10.0;
float n=0.5, pi=3.14, Voref=24.0, Vs=60.0;
float VerrOld=0, VerrNew=0,Ynew=0, Yold=0, Yo=0, VABd=0, VABq=0, VAB=0;
float delta=0, vc_old=0, vc_new=0, X=0, CON=0, iLd_ref=0, iLd=0;
// USER CODE END

// USER CODE BEGIN (SRN22,4)
P3_OUT_P8=0; // reset pin 3.8 at program start and set at program end to calculate pro
                    //gram execution time using pulse width
```

```
////////////////////////////////////////////////////////////
//////////OUTPUT GATE SIGNALS //////////
////////////////////////////////////////////////////////////
GPTA0_LTCXR02=db;
GPTA0_LTCXR03=124;
GPTA0_LTCXR04=249;
GPTA0_LTCXR05=124+db;
GPTA0_LTCXR06=db+del;
GPTA0_LTCXR07=del+124;
GPTA0_LTCXR08=del;
GPTA0_LTCXR09=124+db+del;
////////////////////////////////////////////////////////////////////////
////////////////////ANALOG FILTER OUTPUT//////////
////////////////////////////////////////////////////////////////////////
GPTA0_LTCXR18=1;
GPTA0_LTCXR19=analog1;
GPTA0_LTCXR20=1;
GPTA0_LTCXR21=analog2;
////////////////////////////////////////////////////////////////////////////////
////////////FAST ADC CONVERSION for Vo and ILo//////////
////////////////////////////////////////////////////////////////////////////////
FADC_vStartTimer(0,1);
FADC_vStopTimer(0);
fadc_res0=FADC_vGetChannelConversionResult(0);

FADC_vStartTimer(1,1);
FADC_vStopTimer(1);
fadc_res1=FADC_vGetChannelConversionResult(1);

Vo=fadc_res0*100.0/1023.0;   //10-bit resolution conversion
ILo=fadc_res1*5.0/1023.0;
////////////////////////////////////////////////////////////////////////
////////////////////////PI CONTROLLER ////////////////////////
////////////////////////////////////////////////////////////////////////
VerrNew=Voref-Vo;
Ynew=Yold+((0.000025/2.0)*(VerrOld+VerrNew))*Ki+X;
Yold=Ynew;
VerrOld=VerrNew;
Yo=Ynew+Kp*VerrNew;

CON=Yo;

if(Yo>10.0)
{   CON=10.0;  }
 if(Yo<0.0)
{ CON =0.0;  }

X=(CON-Yo)*Ki; // anti-windup to reset integrator
iLd_ref=CON; // reference current iLd for inner loop
```

```
////////////////////////////////////////////////////////////////////////////////
//////////INNER LOOP CURRENT CONTROLLER ////////////
////////////////////////////////////////////////////////////////////////////////
vc_new=K*(iLd_ref-iLd); // iLd is the estimated d-axis resonant inductor current using
                                    //the Kalman filter algorithm
////////////////////////////////////////////////////////////////////////////////////////////
//////////////////CALCULATION OF PHASE SHIFT//////////////////////
////////////////////////////////////////////////////////////////////////////////////////////
VABd=(k1*vc_new)+(k3*ILo*4.0/pi);
VABq=(k5*vc_new)+(k7*ILo*4.0/pi);
VAB=sqrt(VABd*VABd+VABq*VABq);

delta=2.0*asin(VAB*pi/4.0/Vs/n);
del=floor(delta*125.0/pi);
if(del>125.0)
{ del=125.0; }
////////////////////////////////////////////////////////////////////////////////////////////
//////////KALMAN FILTER ESTIMATION ALGORITHM//////////
////////////////////////////////////////////////////////////////////////////////////////////
kalman_state_estimator _U.input_vc=vc_old;
kalman_state_estimator _U.input_io=ILo;
kalman_state_estimator _U.input_vo=Vo;
kalman_state_estimator _step();
iLd= kalman_state_estimator _Y.output_iLd;
vc_old=vc_new;
////////////////////////////////////////////////////////////////////////
////////////////////////////DISPLAY////////////////////////////
////////////////////////////////////////////////////////////////////////
analog1=del*249.0/125.0;
analog2=vc_new*249.0/37.7;

if (m==2000)
m=0;
Dis1[m]=Vo;
Dis2[m]=ILo;
Dis3[m]=iLd;
++m;

 P3_OUT_P8=1;

 // USER CODE END
//  End of function GPTA0_viSRN22
```

Appendix E

List of Tables and Figures

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List of Figures

Chapter 1 Introduction

Chapter 2 High-Power DC/DC Converters

Chapter 3 Steady-state Analysis and Design of the Phase-Controlled Series-Parallel Resonant Converter

Chapter 4 Novel Large-Signal Converter Modelling using State Feedback Linearization

Appendix F

Author's Publications

[1] A. A. Aboushady, K. H. Ahmed, S. J. Finney, and B. W. Williams, "Linearized Large-signal Modelling, Analysis, and Control Design of Phase-Controlled Series-Parallel Resonant Converters using State Feedback," *Power Electronics, IEEE Transactions on,* 2012, accepted for publication

Abstract

This paper proposes a linearized large-signal state-space model for a fixed-frequency phase-controlled series-parallel resonant converter. The proposed model utilizes state feedback of the output filter inductor current to perform linearization. The model combines multiple-frequency and average state-space modelling techniques to generate an aggregate model with dc state variables that are relatively easier to control and slower than the fast resonant tank dynamics. The main objective of the linearized model is to provide a linear representation of the converter behaviour under large-signal variation which is suitable for faster simulation and large-signal estimation/calculation of the converter state variables. The model also provides insight into converter dynamics as well as a simplified reduced order transfer function for PI closed-loop design. Experimental and simulation results from a detailed switched converter model are compared with the proposed state-space model output to verify its accuracy and robustness.

[2] A. A. Aboushady, K. H. Ahmed, S. J. Finney, and B. W. Williams, "Steady-state Analysis of the Phase-Controlled LCC-type Series-Parallel Resonant Converter Operating Above Resonance," in *Applied Power Electronics Conference and Exposition, 2013. APEC '13,* accepted for publication.

Abstract

This paper presents new analysis providing further insight into the steady-state characteristics of the phase-controlled LCC-type series-parallel resonant converter operating above resonance. An analytical expression is obtained for the converter voltage transfer function in terms of phase angle. The effect of varying the phase angle on ZVS and ZCS of the inverter switches is studied and, accordingly, converter modes

of operation are classified and illustrated. Mode boundaries are analytically derived and graphically represented to ease the determination of converter operating mode at any loading, frequency and phase angle combination. Finally, maximum power transfer criterion is obtained and plotted for the converter. The analysis presented is helpful with converter design and determination of the suitable operating conditions.

[3] A. A. Aboushady, K. H. Ahmed, S. J. Finney, and B. W. Williams, "State feedback linearized model for phase-controlled series-parallel resonant converters," in *IECON 2011 - 37th Annual Conference on IEEE Industrial Electronics Society*, 2011, pp. 1590-1595.

Abstract

This paper proposes a linearized large-signal state space model for phase-controlled series-parallel resonant converter. The model combines multiple-frequency and average state-space modelling techniques to generate a universal model with DC state variables that are easier to control compared to the fast resonant tank dynamics. In order to perform linearization, the proposed model utilizes a state feedback scheme from output filter inductor current. The model also serves as a tool for large-signal prediction/estimation of converter state variables. The model accuracy was verified by comparing with a detailed switching model of the converter built in MATLAB simulation environment.

[4] A. A. Aboushady, K. H. Ahmed, S. J. Finney, and B. W. Williams, "Fuzzy self-tuning PI controller for phase-shifted series resonant converters," in *Power Engineering, Energy and Electrical Drives (POWERENG), 2011 International Conference on*, 2011, pp. 1-6.

Abstract

A linearized model of the phase-shifted series resonant converter is necessary for closed-loop design. With fixed PI control design, the converter does not have good disturbance rejection capability and cannot always cope with a wide range of uncertainties. In this paper, a PI self-tuning mechanism based on a fuzzy logic scheme is proposed. It

corrects the PI gains, initially designed using small-signal modelling, to improve converter dynamic response and disturbance rejection. The algorithm is based on continuous change/adaptation of the PI gains until best dynamic response is achieved. Simulation results compare responses for the PI fixed parameters with the fuzzy-adapted controller gains under different disturbance conditions.

[5] A. A. Aboushady, K. H. Ahmed, S. J. Finney, and B. W. Williams, "Discrete time domain small-signal modelling of full-bridge phase-shifted series resonant converter," in *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*, 2010, pp. 2019-2024.

Abstract

This paper provides an analytical discrete small-signal state-space model of the phase-shift modulated series resonant converter used to obtain an explicit linearized phase-shift to output voltage transfer function. This transfer function is useful for linear closed-loop control design. Initially, the effective duty-ratio to output voltage transfer function is derived. It is then proven, analytically and through results, that it is linearly related to the phase-shift to output voltage which is the main research concern. The analysis is carried out using state-plane diagrams. Small-signal state-space model representation is derived which is used for closed-loop controller gain calculations. Results validate the calculated control gains based on the proposed linearized model.

[6] A. A. Aboushady, K. H. Ahmed, S. J. Finney, and B. W. Williams, "Steady-state analysis of full-bridge series resonant converter with phase-shift and frequency control," in *Power Electronics, Machines and Drives (PEMD 2010), 5th IET International Conference on*, 2010, pp. 1-6.

Abstract

This paper presents steady-state ac analysis of the series resonant converter with phase-shift and frequency control. Analysis for the converter operation above resonance is performed. A simple analytical expression for the converter input/output voltage gain as a function of phase-shift and frequency is derived. Different converter operation modes

are demonstrated with simulation results. Analytical expressions for mode boundaries and maximum power transfer to load are derived, discussed, and graphically represented.

[7] A. A. Aboushady, K. H. Ahmed, S. J. Finney, B. W. Williams, and Z. M. Shafik, "Performance analysis of a new modular nano-crystalline core transformer based converter for medium voltage dc transmission applications," in *Power Electronics, Machines and Drives (PEMD 2010), 5th IET International Conference on*, 2010, pp. 1-6.

Abstract

This paper proposes a new modular configuration for ac/dc conversion based on the concept of "building block" converter units. The modular system architecture comprises low-power units which can be connected in parallel to achieve higher power levels. Using such a design, medium voltage dc levels can be reached without the need of bulky step-up transformers or series connected switching devices. The converter configuration is introduced with its typical designed ratings and main features. Detailed design of the nano-crystalline core transformer is performed to verify size reduction. Simulation results for single and multi-module parallel operation are presented and discussed. Load current sharing between parallel modules is also investigated.

[8] A. A. Aboushady, K. H. Ahmed, S. J. Finney, and B. W. Williams, "Predictive Voltage Control of Phase-Controlled Series-Parallel Resonant Converter," in *Power Engineering, Energy and Electrical Drives (POWERENG), 2013 International Conference on*, 2013, submitted.

Abstract

This paper proposes a predictive output voltage controller for the phase-controlled series-parallel resonant converter. The objective of this controller is to enhance closed loop system robustness and dynamic performance compared to conventional PI control. First, the converter non-linear large signal behavior is linearized using a state feedback based scheme. Consequently, the converter preserves its large signal characteristics

while modeled as a linear system. A reduced order model is then used for the detailed design of the proposed predictive controller. Stability analysis and controller gains selection are addressed. Finally, simulation and experimental results are demonstrated to validate the improved system performance in contrast with PI control.

[9] A. A. Aboushady, K. H. Ahmed, S. J. Finney, and B. W. Williams, "Compact Multi-Modular Design of High-Power DC/DC Resonant Converters for Offshore Wind Energy HVDC Transmission," in *IEEE Power and Energy Society General Meeting*, 2013, submitted.

Abstract

Besides research on reliability, efficiency and grid impact challenges imposed by the wind energy industry, research on compact design of multi-modular interfacing DC/DC converters is growing rapidly. This paper addresses the application of multi-modular resonant-type DC/DC converters for offshore wind high power HVDC transmission systems. The attractive feature about resonant converters is their soft switching characteristics which enables higher frequency operation and hereby reduced converter footprint. The paper focuses on one important aspect leading to increased power density; the output filter design. New analytical expressions are derived for filter ripple content in DC/DC resonant converters. This has not been investigated previously. Further mathematical relations are derived for multi-module interleaved operation of DC/DC resonant converters with both series and parallel connections of output filter. Results are demonstrated to validate the derived design equations highlighting the advantage of interleaving with multi-modular structures in achieving highly compact designs.

[10] A. A. Aboushady, K. H. Ahmed, S. J. Finney, and B. W. Williams, "New Steady-State Analysis and Maximum Efficiency Based Design of the Phase-Controlled Series-Parallel Resonant Converter," in *Power Electronics, IEEE Transactions on,* 2013, prepared for submission.

Abstract

This paper presents new steady-state analysis for the phase-controlled series-parallel resonant converter which gives further insight into the converter characteristics relative

to well established literature. Modes of operation under phase-shift control are revealed with mode boundaries analytically derived and graphically represented. Converter voltage gain sensitivity is addressed with respect to variation in operational parameters such as switching frequency and load. Maximum power transfer criterion and operational efficiency are also derived; the latter considering analytical expressions for inverter, rectifier and parasitic element losses. Based on maximum efficiency opearting criterion, selection of optimum full-load quality factor and switching frequency is made. A detailed design procedure of resonant tank parameters and output filter is then performed. Simulation and experimental results are demonstrated to validate the proposed converter design.

[11] A. A. Aboushady, K. H. Ahmed, S. J. Finney, and B. W. Williams, "Robust Control of the Phase-Controlled Series-Parallel Resonant Converter," in *Power Electronics, IEEE Transactions on,* 2013, prepared for submission.

Abstract

This paper proposes two controllers for robust control of the phase-controlled series-parallel resonant converter; namely Lyapunov and sliding mode controllers. The objective is to enhance closed loop system robustness and dynamic performance compared to conventional PI control. Since the control algorithms are model dependent, the converter non-linear large signal behavior is firstly linearized using a state feedback based scheme. Hence, the converter preserves its large signal characteristics while modeled as a linear system. The linearization scheme has the advantage of reducing the converter model to an equivalent output filter model which significantly simplifies the robust control design process. For each controller, the control law is derived in addition to detailed stability and robustness analysis. A comparative analysis is performed between the two proposed controllers in addition to comparing with conventional PI. Finally, results from simulations using MATLAB and DSP-driven experimental prototype are demonstrated to verify performance enhancement.

[12] A. A. Aboushady, K. H. Ahmed, S. J. Finney, and B. W. Williams, "Power Sharing Control for Input-Series Phase-Controlled Series-Parallel Resonant Converters with

Sensorless Load Voltage Control," in *Power Electronics, IEEE Transactions on,* 2013, prepared for submission.

Abstract

This paper addresses the voltage and current sharing in multi-modular structures of the phase-controlled dc/dc series-parallel resonant converter (SPRC). Input-series connections of the converter are studied comprising the input-series output-parallel (ISOP) and input-series output-series (ISOS) connections. A novel control configuration for interleaved multi-module operation common to both ISOP and ISOS connections is introduced. The controller comprises a robust Lyapunov-based controller as the main load voltage regulator. In addition, there exists an average input voltage sharing controller regulating the inner control loop to ensure uniform output current sharing (OCS) in ISOP systems and uniform output voltage sharing (OVS) in ISOS systems. A sensorless load voltage estimation algorithm based on two-port network theory is also proposed. The algorithm accounts for interconnecting cable impedance and is useful since it reduces the number of required sensors and eliminates load voltage measurement requirement. The latter degrades system modularity due to being a source of single-point failure. Simulation and experimental results are demonstrated to validate the performance of the proposed controller structure.