Design, Analysis, and Operation of Hybrid Modular Multilevel Converters for HVDC Applications

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This thesis is the result of the author’s original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

Signed: Date:

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Abstract

This thesis investigates the design, analysis, and operation of modular multilevel converters (MMC) for HVDC applications. Based on the operation principles of the MMC, the operation of MMC under asymmetrical arm impedance conditions is analysed using three equivalent sub-circuits at different freqeuncy. Detail analysis of the impact of asymmetrical conditions on the differential-mode current, the common-mode current and sub-module (SM) capacitor voltages, is performed. Based on the analysis, the corresponding control targets and an improved control strategy are designed to improve the operation performance. Considering the advantages of half-bridge based SM (HBSM) and full-bridge based SM (FBSM), a hybrid MMC (H-MMC) configuration consisting of FBSMs and HBSMs is proposed. By adopting the negative voltage state for some of the FBSMs, the output voltage range is extended to increase converter power transmission capability. By considering the relationships between the AC and DC voltages, AC, DC and arm currents, the ratio of the numbers of the FBSM to HBSM is analysed in order to maintain capacitor voltage balance and retain DC fault blocking capability. An equivalent circuit for the H-MMC is proposed, which considers each arm to be consisted of two individual voltage sources. This model is used to analyse SM capacitor voltage balancing and ripple. A two-stage selection and sorting algorithm is developed to ensure capacitor voltage balancing among the SMs. The proposed H-MMC is compared to other topologies in terms of power device utilization and power losses, and it shows that the H-MMC has higher device utilization and lower power loss than the conventional FBSM based MMC; Furthermore, The DC fault ride-through capability of the H-MMC are discussed. It is found that the H-MMC can not only isolate the DC fault, but also coniture operating at a wide DC voltage range from zero to rated value. Such two features of the H-MMC show the advantages in the hybrid configurations over the conventional FBSM and HBSM systems. Finally, two applications based on the proposed H-MMC are presented; one is a high power DC/DC converter with fault blocking capability for interconnecting large HVDC systems, and the other is a hybrid HVDC transmission system comprising a wind farm side VSC based on the H-MMC and a grid side LCC for transmitting wind power to AC grid.

List of Symbols

*	Reference value
~	AC component
–	DC component
C	Capacitor in SM
e	Inner emf
i	Output AC current
i_{cm}	Common-mode current
i_d	Output AC current in *d*-axis coordinates
i_{dc}	DC current
i_{dm}	Differential-mode current
I_m	Peak value of AC current
i_n	Lower arm current
i_p	Upper arm current
i_q	Output AC current in *q*-axis coordinates
L_0	Arm inductor
m	Modulation index
v_{ac}	Output AC voltage
V_c	Rated capacitor voltage in Sub Module
V_{c0}	Capacitor initial voltage

V_{dc}	DC voltage
v_p	Upper arm voltage
v_n	Lower arm voltage
$\mathrm{V_m}$	Peak value of AC voltage
P	Active power
Q	Reactive power
φ	Voltage and current phase angle
ΔE	Energy variation on capacitors
ω_0	Fundamental frequency

List of Abbreviations

AC	Alternative Current
ACCB	Alternative Current Circuit Breaker
CDSM	Clamp Double half-bridge based Sub Module
DC	Direct Current
DCCB	Direct Current Circuit Breaker
DSP	Digital Signal Processor
HVDC	High Voltage Direct Current
HVAC	High Voltage Alternative Current
IGBT	Insulated Gate Bipolar Transistor
LCC	Line-Commutated Converter
VSC	Voltage Source Converter
MMC	Modular Multilevel Converter
PWM	Pulse Width Modulation
HBSM	Half-Bridge based Sub Module
FBSM	Full-Bridge based Sub Module
H-MMC	Hybrid Modular Multilevel Converter
HPF	High-Pass Filter
PD	Phase Disposition
PI	Proportional and Integrator

PR	Proportional and Resonant
PS	Phase Shift
SCR	Short Circuit Ratio
SM	Sub Module
STATCOM	Static Synchronous Compensator
WF	Wind Farm

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Chapter 1

Introduction

1.1 Background

With the increasing penetration of renewable energy sources such as wind power and solar power into the power grid in Europe, the existing high-voltage alternating current (HVAC) grids face more and more challenges and an urgent upgrade is required. However, the solution based on upgrading existing HVAC grids is unlikely to be feasible in densely populated European areas, due to legal, political and environmental issues [GOR2006][HER2010A][HER2010B][AHM2011]. In addition, renewable energy sources are mostly remote and intermittent, so balancing them and transmitting the power efficiently from remote locations to load centres are two of main issues for renewable energy integration [BRE2008][HIO2010]. To tackle the above mentioned issues, European supergrid as a potential solution has been proposed to build high-voltage direct current (HVDC) grids for interconnecting the various European countries and integrating large renewable energy sources into the power grids [DES2007] [WOY2008] [DEC2009].

Fig. 1. 1 Infrastructure of European Supergrid [NCE2011]

1.2 DC versus AC for electrical power transmission

Since the first electric station was invented by Thomas A. Edison in 1882, direct current, as a type of electric power transmission method, has been developing over one hundred years. Although following advent of the transformer, poly-phase circuits and the induction motor led to AC electric power systems, and AC systems with ultra-high-voltage (UHV) techniques are capable of delivering massive electric power over long distances, the AC transmission method is not regarded as a potential technology for the European supergrid, due to the following reasons [ALE2002] [REI2005]:

(1) The right-of -way of AC transmission is larger than that of DC transmission, which is a critical restraint for AC systems in terms of environmental, health and political reasons in Europe;

(2) AC transmission cables have high charging current which would deteriorate the power factor and increase the cable loss, and limit power delivery distance.

(3) Renewable resources, especially for offshore resources are difficult to access to the main grid using AC transmission.

(4) The interconnection of AC systems is more difficult than DC interconnected systems, due to the synchronous issues.

DC transmission, especially HVDC transmission, has much fewer problems when delivery electric power over long distance.

1.3 High voltage direct current transmission

HVDC transmission has characteristics that make it especially attractive for certain transmission application, such as long distance bulk power transmission, asynchronous AC grids interconnections, and long submarine cable crossings [BAH2007] [BAH2008]. Nowadays, there are two HVDC types: line-commutated current-source converter (LCC) based HVDC system and self-commutated voltage-source converter (VSC) based HVDC system [BAH2008] [FLO2009] [XU2007B] [OKB2012B].

1.3.1 Line-commutated current-source converter based HVDC

The most common and mature technology in HVDC transmission is based on LCC. Thyristor-based LCC HVDC transmission, as shown in Fig. 1.2, has been widely used due to its high power capacity, and high economical efficiency and reliability. Nowadays, a single LCC HVDC has a power rating up to 6 GW at a voltage level of ±600 kV and up to 10 GW at ±800 kV. But, there are some critical disadvantages in the conventional thyristor-based LCC HVDC as follows:

(1) It needs external voltage source for commutation, and is vulnerable to commutation failures during AC network disturbances.

(2) Bulk AC and DC filters are required to eliminate the low-order harmonic components.

(3) Coupled control of active and reactive power flow at each AC network.

These drawbacks make LCC-based HVDC transmission technology unsuitable for connecting weak AC system, island networks and renewable sources into main grids.

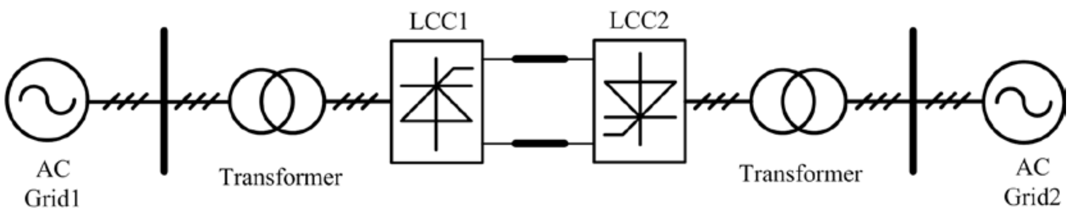


Fig. 1. 2 Structure of conventional thyristor-based LCC HVDC transmission

1.3.2 Voltage-Source Converter based HVDC

With the development of power semiconductor devices, the increased voltage/current ratings and improved performance of self-commutated semiconductor devices have made HVDC transmission based on VSC possible. VSC based HVDC system, as shown in Fig. 1.3, overcomes the above mentioned disadvantages of the LCC based HVDC system, due to the following principal characteristics of VSC transmission [SCH2000] [AND2001] [AND2002]:

(1) It needs no external voltage source for commutation.

(2) It can independently control the reactive power flow at each AC network.

(3) Reactive power control is independent of active power control.

These features make VSC based HVDC transmission technology attractive for connecting weak AC system and integrating renewable sources into main grids. However, the drawbacks of VSC based HVDC are higher power losses and cost compared to conventional LCC based HVDC system though the recent developments in device technology and new converter topology have significantly reduced the power losses and cost for VSC HVDC system.

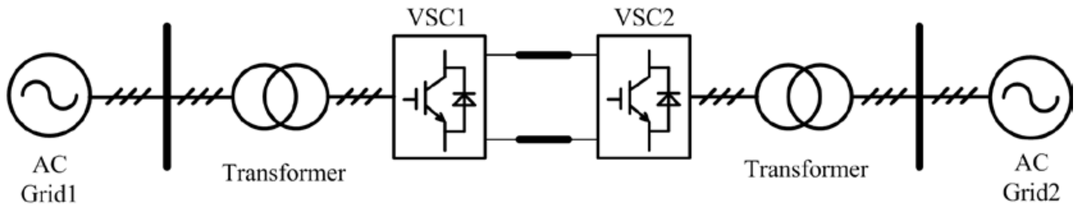


Fig. 1. 3 Structure of Conventional VSC-based HVDC transmission

1.4 VSC topologies for HVDC system

Currently there are two main VSC configurations for HVDC transmission system, such as two-level VSC topology and multi-level VSC topology (i.e. MMC), according to the number of voltage level. The two-level converter is shown in Fig. 1.4. It employs pulse width modulation (PWM) method to synthesize a two-level output voltage waveform. But it has some inherent drawbacks, which limit its performance and application in HVDC fields: [XU2007B]

(1) Passive AC filter is required to suppress undesired harmonic current flowing into the AC grids.

(2) A high pulse frequency of approx. 40 times of the line frequency is necessary to make a reasonable compromise regarding AC-filter size.

(3) High slope (d*v*/d*t* or d*i*/d*t*) of voltage or current generates unwanted EMC-disturbance and constrain physical arrangement and construction of converters.

(4) A large DC-link capacitor required for energy storage to smooth DC voltage ripples would result in extremely high fault current.

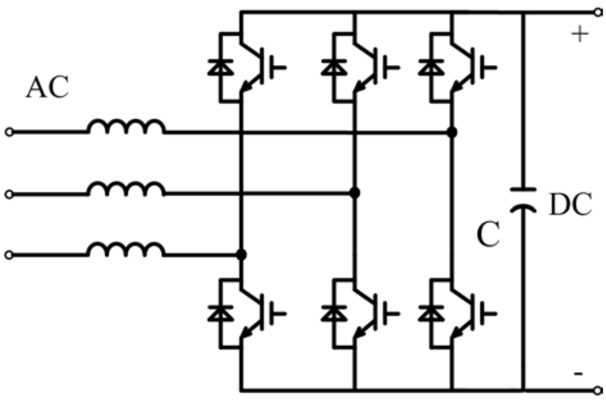
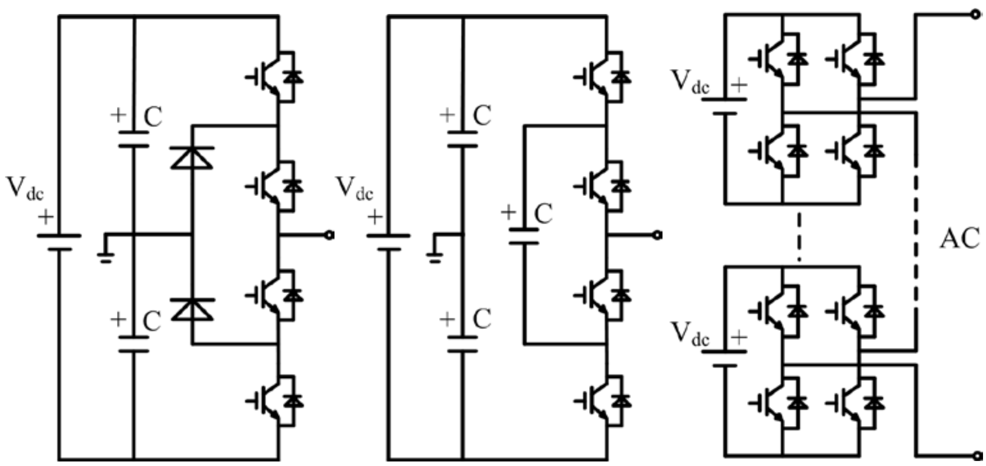


Fig. 1. 4 Structure of conventional two-level VSC topology



(a) diode-clamped converter (b) flying capacitor converter (c) Cascaded H-bridge

Fig. 1. 5 Single-phase structure of multilevel VSC topology

The other configuration is multilevel VSC, as a very important alternative topology in the area of high-power and high-voltage applications. It has drawn significant attentions in the recent years due to its distinct features, such as voltages with reduced harmonic contents, smaller input and output filters, reduced voltage derivatives (d*v*/d*t*), and increased efficiency [ROD2002] [MEY2002] [ROD2007] [KOU2010].

There are four typical multilevel converter topologies, namely diode-clamped converter [NAB1981], flying capacitor converter [MEY1997], full-bridge cascaded converter [MAR1988], and modular multilevel converter (MMC) [LES2003]. The diode-clamped multilevel converter, as shown in Fig. 1.5 (a), suffers from DC voltage imbalance for configurations with more than three voltage levels, thus an external circuit is required to keep the DC link capacitor voltages balanced [NEW1997]. Similarly, the flying capacitor multilevel converter, as shown in Fig. 1.5 (b), has bulk DC capacitors and a complex capacitor balancing control strategy is needed to stabilize the capacitor voltages [XU2004]. These two multilevel topologies are often used as three-level converter, since the configuration would be much more complicated following the increase of voltage level. The full-bridge cascaded multilevel converter, as shown in Fig. 1.5 (c) requires independent DC voltage source for each sub-module, and the topology has no common DC link terminal. So the cascaded topology is generally suitable for the static synchronous compensator (STATCOM) AC rather than for HVDC transmission system [TOL1999] [TOL2002].

Modular multilevel converter (MMC) has drawn significant attentions since it was first proposed in 2003. As shown in Fig. 1.6 (a), like the cascaded configuration, the basic building block in a MMC is a sub-module (SM), and each leg is consisted of two arms where each arm comprises several (e.g. tens or hundreds of) SMs and an arm inductor. When compared with other multilevel converter topologies, the MMC has the following unique features: [ALL2008] [MAR2010] [MAR2011]

(1) Modular construction and scalability to meet any voltage level requirements.

(2) Inherent redundancy for failure management and interior failure tolerance.

(3) High efficiency by minimizing semiconductor switching frequencies.

(4) Reduced passive filters at AC side.

(5) Absence of DC-link capacitors.

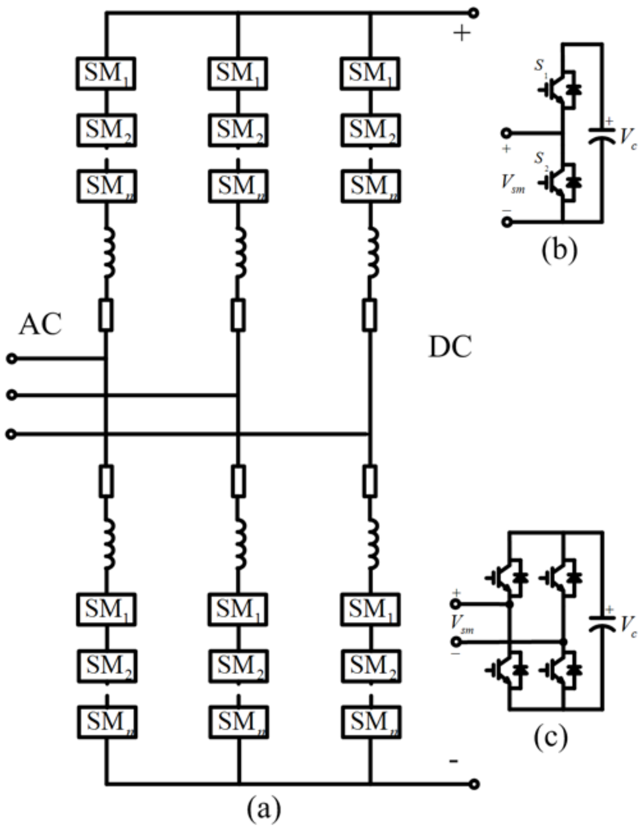


Fig. 1. 6 Structure of MMC and its sub-module topologies

Based on these characteristics, nowadays, there are several MMC-based HVDC systems in operation. The 400 MW Trans Bay Cable project was the first commercial MMC based HVDC system built by Siemens in 2010 [TEE2011]. It connects Pittsburgh to San Francisco by an 88 km submarine cable at a DC voltage of ±200 kV. A back-to-back MMC configuration was adopted to connect two asynchronous AC grids in [KHA2013]. Another prospective application of the MMC is to connect offshore wind farms to the onshore grid via DC transmission. Considering the requirement of submarine cable, wind farm power capacity, space for the offshore converter station platform, the MMC has several advantages over AC transmission and LCC based HVDC transmission in terms of transmission efficiency and system costs [XU2013A]. A relative engineering project is TenneT Offshore Wind Farm Complex [PER2015], which is located in the North Sea. It is consisted of several wind farms connections with a total rated power of 5GW [HUS2012] [TEN2013].

There are two classic SM configurations, i.e. the half-bridge SM (HBSM) as shown in Fig. 1.6 (b) and the full-bridge SM (FBSM) as shown in Fig. 1.6 (c). The critical disadvantage of HBSM based MMC is the lack of DC fault blocking capability, thus it has to rely on AC or DC circuit breakers to isolate DC faults [TAN2007] [JIN2012]. This becomes problematic for both the converter as it has to withstand a high fault current and the connected network as it could take considerable time for the system (especially a multi-terminal system) to recover [CHE2011A]. To address such issues, the FBSM was proposed which has the inherent advantage of DC fault blocking capability. However, the number of SM power devices is doubled compared to the HBSM. This not only increases the cost but also results in higher power loss, as the current in each SM flows through two power devices instead of one power device in a HBSM.

1.5 Scope of thesis

1.5.1 Research motivation

Conventional MMC topologies with HBSM or FBSM have their own critical drawbacks, i.e. the HBSM based MMC (HB-MMC) does not have DC fault blocking capability, while the FBSM based MMC (FB-MMC) doubles the number of SM power devices with increased power loss. Thus, how to enhance the performance of the conventional MMC and how to improve the topology of MMC to combine the advantages of these two classic topologies are interesting and practical issues that should be investigated.

1.5.2 Research Objective

The research in this thesis focuses on two aspects. The first aspect is to enhance the performance of the conventional MMC. Considering the FBSM can generate a negative voltage state but this has not been used yet in normal operation, a boost FB-MMC is introduced in the thesis to extend the output voltage range by adopting the negative voltage state, so as to increase power transmission capability of the FB-MMC. The thesis conducts a further analysis on the control and operation of conventional MMCs under asymmetric arm impedance conditions. The second aspect is to propose a hybrid MMC (H-MMC) topology combining HBSMs and FBSMs in each arm. Compared with the FB-MMC, the proposed topology has the same DC fault blocking capability but uses fewer power devices hence has lower power loss. The following issues on the proposed H-MMC topology in terms of control strategy, capacitor balancing, DC fault ride-through capability and pre-charging process, as well as its applications in HVDC system are also considered and analysed in depth.

1.5.3 Main contribution in the thesis

(1) Analysing the influence and control of using the negative voltage state of the FBSM in the FB-MMC under normal operation conditions.

(2) Analysing and proposing a control strategy for the MMC under the asymmetric arm impedance conditions.

(3) Proposing a hybrid MMC topology and its corresponding control strategy to combing the advantages of the conventional FB-MMC and HB-MMC.

(4) Presenting a three-terminal DC/DC converter based on the proposed H-MMC with DC fault blocking capability for HVDC system interconnection.

(5) Investigating a coordinated control strategy for a hybrid HVDC system comprising a wind farm side VSC using the proposed H-MMC and a grid side LCC for integrating wind power, under communication failure at the LCC side.

1.5.4 Thesis Organization

This thesis is organized into seven chapters.

Chapter 1 briefly introduces the background of HVDC transmission system and the development of converter topologies that can be used for HVDC applications. The research motivation, objectives and main contributions in the thesis are presented.

Chapter 2 presents a general overview of the configurations and operations of MMCs, such as modelling, control strategies, modulation, circulating current suppression, capacitor voltage balance, fault ride-through capability, and etc..

Chapter 3 presents the operation of HB-MMC and FB-MMCs. Mathematic models and control principles for the MMCs are provided. FBSMs using negative voltage state are considered and the link between capacitor voltage variation and the maximum modulation index is analyzed. Different MMC topologies are compared and the different behaviours of HB-MMC and FB-MMC under the DC fault conditions are also analysed. Simulation results from a three-phase MMC model using Matlab/Simulink and experimental results from a single-phase MMC prototype are provided to demonstrate the feasibility and validity of the operation performance of the HB-MMC and FB-MMC.

Chapter 4 proposes a detailed analysis and improved control strategy for MMCs under asymmetric arm inductance conditions. A theoretical analysis of the effect of asymmetric conditions on MMC operation is carried out using equivalent circuits at different frequencies. A control strategy for the control of differential-mode current, common-mode current and upper and lower arm energy balance is designed. The feasibility and validity of the proposed analysis and control strategy are demonstrated by simulation results from a three-phase MMC system and experimental results from the single-phase prototype MMC system.

Chapter 5 proposes a H-MMC combining FBSM and HBSM which has DC fault blocking capability but with fewer power devices and lower power loss compared to FB-MMC. The optimal ratio of FBSMs and HBSMs, and the number of FBSMs generating negative voltage states are evaluated to ensure successful DC fault blocking and capacitor voltage balancing. Equivalent circuits of each arm consisting of two individual voltage sources are proposed and two-stage selecting and sorting algorithms for capacitor voltage balancing are developed. Experimental results during normal operation and DC fault conditions demonstrate the feasibility and validity of the proposed H-MMC.

Chapter 6 presents two applications of the H-MMC. The first one is for high-power multi-terminal DC/DC converters with fault blocking capability for interconnecting HVDC systems. The proposed DC/DC converter operation is analysed and simulation results are presented to demonstrate the robust performance during DC fault conditions. The other application is a hybrid HVDC system comprising a wind farm side MMC and a grid side LCC for integrating wind power. The configuration and operation principle of the hybrid HVDC system are described with special consideration on inverter commutation failure. Simulation results are presented to demonstrate the robust performance during LCC inverter commutation failure to validate the operation and recovery of the hybrid system with the proposed control strategies and hybrid MMC configuration.

Chapter 7 draws the conclusions and provides recommendations for future work.

Chapter 2

Review on modular multilevel converters

The Modular Multilevel Converter (MMC), since first proposed in 2003 [LES2003], has become increasingly popular due to its many advantages, such as modular design, high efficiency and scalability, and excellent output waveform with low harmonic distortion [ALL2008] [MAR2010] [MAR2011] [SAE2011]. In view of such advantages, the MMC is considered as an ideal converter for high voltage and high power applications, such as HVDC transmission [ALL2008] [SAE2011], electric railway supplies [WIN2010] [ANG2011A] [ANG2011B], high-power motor drives [HIL2009] [HAG2010] [KOR2010] [ANT2014]. Over the last few years, extensive research work has been carried out to address the technical challenges referring to topologies, operation and control of the MMC.

This chapter presents an overview of the MMC in terms of its topology, modulation, and control strategy under normal and special operation conditions. Capacitor voltage balancing, circulating current suppression, system modelling, as well as some classic engineering project for HVDC transmission systems will also be discussed.

2.1 Main MMC topology

The main characteristic of the MMC is modular design with serial connection of a large numbers of power sub-modules (SMs). A schematic diagram of a three-phase MMC is shown in Fig. 2.1 (a), where each phase is consisted of two arms and each arm contains N numbers of SMs and an arm inductor L_0.

The basic building block in a MMC is the SM. According to the type of SM circuit, there are three main MMC configurations as follows.

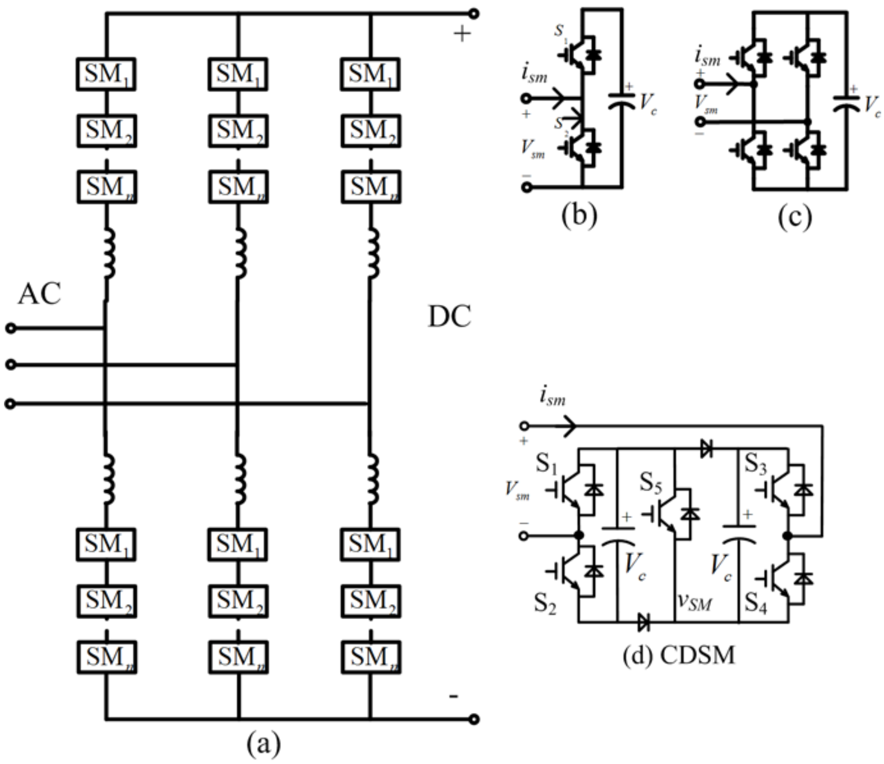


Fig. 2. 1 Structure of a three-phase MMC and three SM topologies

(1) Half-bridge based SM (HBSM) [LES2003]. As shown in Fig. 2.1 (b), the output voltage of a HBSM can be its capacitor voltage V_c when S_1 is on (i.e. insert condition) or zero when S_2 is on (i.e. bypass condition). Thus, there is inevitably a DC component in the arm voltage, which means HBSM based MMC only can be used to connect to DC systems [PER2015]. The switching states of the HBSM are listed in Table 2-1.

(2) Full-bridge based SM (FBSM) [GLI2005]. As shown in Fig. 2.1 (c), the output voltage of a FBSM has three voltage states: positive voltage state V_c, zero and negative voltage state $-V_c$. Since the FBSM can generate positive, zero and negative output voltage state, so FBSM based MMC can be used to connect to either a DC or an AC system [PER2015]. The switching states of the FBSM are listed in Table 2-2. But one of the drawbacks of the FBSM is the number of semiconductor devices used is twice of that used for the HBSM, leading to higher device cost and power losses. [MAR2010]

(3) Clamp double half-bridge based sub-module (CDSM) [MAR2010] [MAR2011]. As shown in Fig. 2.1 (c), a CDSM is consisted of two HBSMs with one additional IGBT and two extra diodes. Under normal operation, the additional IGBT S_5 is always on and the CDSM is equivalent to two series-connected HBSMs. Since the output voltage state of a CDSM is either positive or zero, so CDSM based MMC also only can be used to connect to DC systems. The switching states of the CDSM are listed in Table 2-3. Compared with the HBSM and FBSM on device cost and power losses, CDSM is slightly worse than the HBSM but better than the FBSM.

A summary of the comparisons on various SM circuits in terms of output voltage levels, devices numbers, power losses, is provided in Table 2-4.

Table 2- 1 Switch states of HBSM

STATE	S_1	S_2	v_{sm}	$V_c\,(i_{sM}>0)$
1	1	0	V_C	*charging*
2	0	1	0	*bypassed*
BLOCK	0	0	-	-

Table 2- 2 Switching states of FBSM

STATE	S_1	S_2	S_3	S_4	V_{SM}	$V_C\ (i_{SM} > 0)$
1	1	0	0	1	V_C	*charging*
2	0	1	0	1	0	*bypassed*
3	1	0	1	0	0	*bypassed*

4	0	1	1	0	$-V_C$	*discharging*
BLOCK	0	0	0	0	-	-

Table 2- 3 Switching states of CDSM

STATE	S_1	S_2	S_3	S_4	S_5	V_{SM}
1	0	1	1	0	1	$2V_C$
2	0	1	0	1	1	V_C
3	1	0	1	0	1	V_C
4	1	0	0	1	1	0
BLOCK	0	0	0	0	0	-

Table 2- 4 Comparisons of the three SM topologies

Item	HBSM	FBSM	CDSM
Voltage level states	Vc, 0	±Vc, 0	2Vc, Vc, 0
IGBTs/Diodes	2/2	4/4	5/7
DC fault blocking capability	No	Yes	Yes
Power losses	Low	High	Moderate

2.2 Control and modulation methods

When a MMC is used as an AC/DC converter, the output AC and DC voltages, currents and power flows have to be controlled. A conventional vector control method, as shown in Fig. 2.2, including an inner current control loop to regulate the inductor current, is described in [TU2011B], which is similar to the vector control strategy of two-level VSCs [XU2005]. Due to the MMC's unique configuration, there are complex interactions involving its different currents and voltages, and extensive researches have been conducted on the operation of the MMC, such as capacitor voltage, circulating current, modulation, and system operation under special conditions.

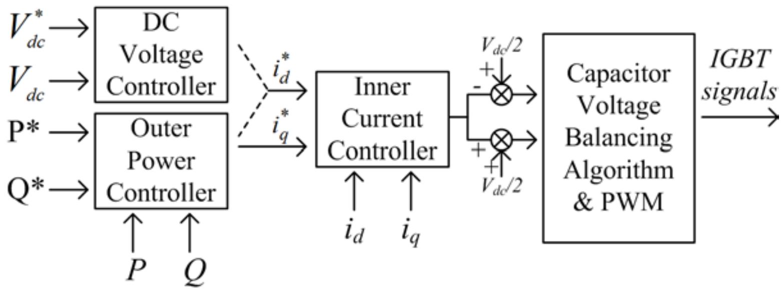


Fig. 2. 2 Control structure of a conventional vector control method

2.2.1 Capacitor pre-charging process and voltage balancing methods

Since the MMC employs the distributed capacitor in each SM, for stable operation, pre-charging all SM capacitors to the pre-set value is required. In addition, the average capacitor voltages must remain balanced during operation in one fundamental period. This means the absorbed and discharged energy of the capacitors in one period must be equal under steady-state.

The pre-charging process for a MMC can be divided into two groups, according to the voltage source from AC side or DC side, as shown in Fig. 2.3, and the processes include two stages of uncontrolled charging and controlled charging. In the uncontrolled charging stage, all capacitors are charged equally, but their voltages will be insufficient for the normal operation of the MMC. Under the controlled charging stage, various schemes have been proposed either adopting external voltage sources

[LES2003] [XU2011A], additional resistors [DAS2011], PWM mode to charge from the DC side [SHI2012], or using sequentially controlled charging methods to charge from AC side [XUE2014]. A charging scheme for MMC was proposed in [LES2003] by employing a DC breaker and an auxiliary DC source equalling to the rated voltage of the SM capacitor. However, due to the need for a high-voltage DC breaker, this method can be expensive. An accelerated, synchronous pre-charging circuit for all SMs was proposed in [XU2011A], which is consisted of four thyristors per SM and an extra DC source. However, his brings in additional complexity and cost to the system. In order to avoid any auxiliary voltage source, a pre-charging method with an additional resistor in series with the SMs in each arm was proposed in [DAS2011]. The additional resistor is used to limit the peak arm charging current. But the main disadvantage of this method is an additional resistance is inserted in each arm for both charging and discharging process, which would increase power losses. An improved pre-charging method without any auxiliary devices was presented in [SHI2012], through operating one of SMs in pulse width modulation mode. Another method with a grouping sequentially controlled charge process was proposed in [XUE2014], in which the capacitors is charged group by group so that each capacitor can share sufficient and equal stored energy.

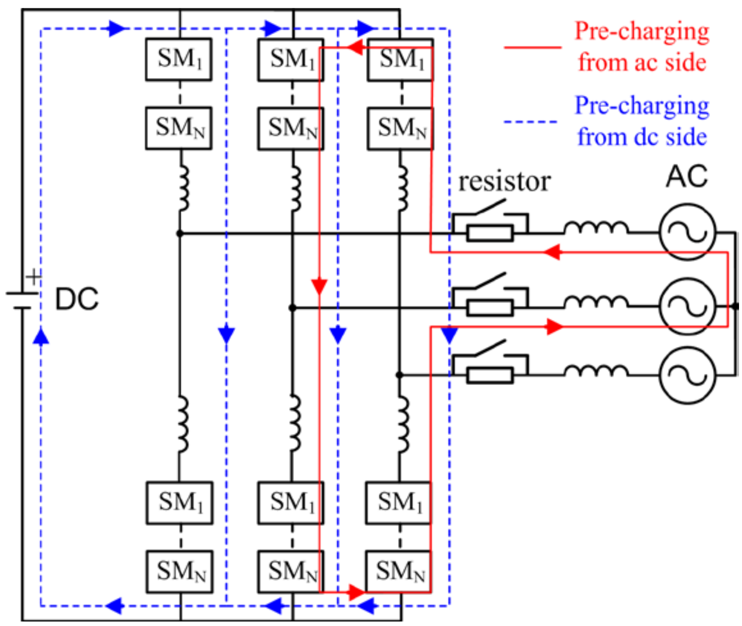


Fig. 2. 3 Pre-charging current paths for the MMC

One of the other technical challenges associated with the capacitor voltage is to keep the capacitor voltage in each SM balanced and to maintain the voltage at the nominal value. The most popular voltage balancing method is based on a sorting and selecting method [ROH2010A] [SAE2011]. The process sorts the capacitor voltage and then selects the SMs according to the direction of arm current. If the arm current is positive (i.e. $i_{sm} > 0$), SM with the lowest capacitor voltage is selected to charge; while if the arm current is negative, SM with the highest capacitor voltage is selected to discharge. For the capacitors in the bypassed SMs, their voltages will remain unchanged regardless of the direction of the arm current. Although this method is easy to implement, it has two main drawbacks:

(1) For a large-scale MMC system with hundreds of SMs in each arm, it is quite complex and time-consuming to sort all capacitor voltages and select the suitable SMs.

(2) It has unnecessary switching transitions among the SMs. For example, even the required total numbers of inserted SMs within two consecutive control periods are not changed, if the sorting sequence has changed, the inserted or bypassed state of SMs may change leading to increased switching frequency.

To improve the sorting and selecting method, several methods have been proposed to reduce the switching frequency. A modified phase-shifted carrier-based pulse-width-modulation (PSC-PWM) scheme was proposed in [TU2011B]. In this method, only unselected SMs could probably be inserted when the required total number of inserted SMs within two consecutive control periods is changed. Otherwise, the switching states are not changed. Balancing methods with fundamental switching frequency were presented in [ILV2011] and [QIN2013]. In [ILV2011], the switching pattern is chosen by calculating the stored energy in each SM under the fixed fundamental switching frequency period. The main disadvantage of this method is the increase of implementation complexity for an MMC with large numbers of SMs. A hybrid balancing strategy including a modified slow-rate sorting method, a predictive voltage error sorting method and a fundamental-frequency sorting method was proposed in [QIN2013]. But this hybrid balancing method is also complicated in terms of computational complexity. In [GUA2011], an optimized balancing method was proposed. In this method, only the SMs whose capacitor voltages exceed the set voltage limit are selected to change the switching states, while the other SMs whose capacitor voltages are within the voltage limits remain the same switching states. Predictive algorithms based on model predictive control [QIN2012] and stored energy changes in SM [ILV2013A] were used to balance the capacitor voltage, respectively.

2.2.2 Circulating current control

The relationship between the arm current and capacitor voltage was analysed in [ILV2012A] and [SON2013]. One of the special characteristics of the MMC is the circulating current which usually includes a DC component and even-order (mainly the second-order) harmonic components. The circulating current flows through the three-phase legs of the MMC, affecting the SM capacitor voltage and the energy variation in each arm, though it does not affect the AC side current (differential-mode current), as shown in Fig. 2.4.

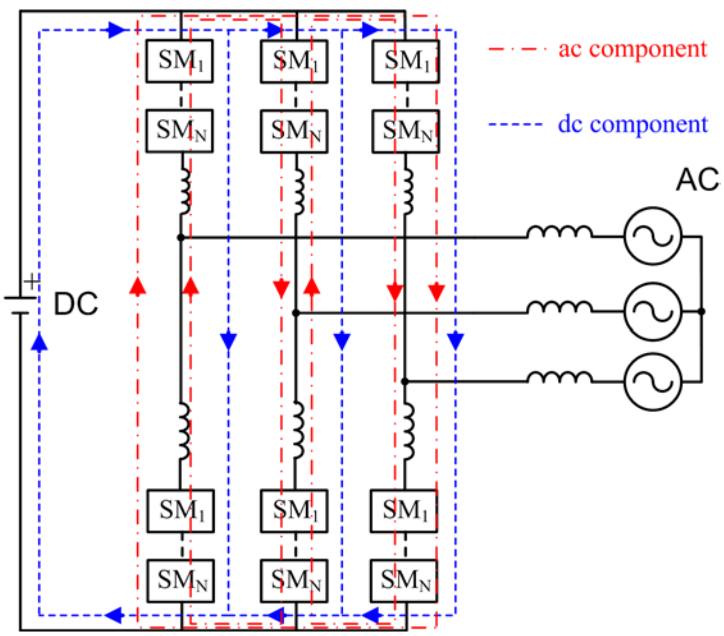
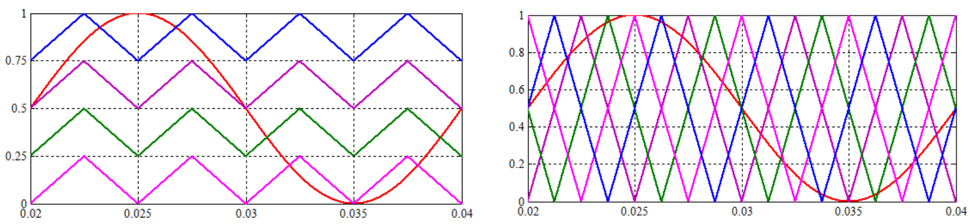


Fig. 2. 4 Circulating current flowing path inside the MMC

Since the circulating harmonic currents distort the arm voltage and induce extra power losses, various circulating current suppression methods have been proposed. a passive circulating current suppression method by designing the arm inductor was presented in [ILV2012B] and [TU2010], though this lead to large arm inductor with increased cost. Several active circulating current suppression methods have been proposed [ANT2009] [ANG2011A] [ANG2011B] [ANT2014] [TU2011B] [XU2012] [LI2013D] [ZHA2014] [HE2015]. An improved modulation method eliminating the harmonics in the arm currents and controlling the capacitor energies in the arms under various loading conditions was proposed, but this method relies on the precise model and system parameters [ANT2009] [ANG2011A] [ANG2011B] [ANT2014]. A second-order harmonic circulating current suppressing controller under the double line-frequency, negative-sequence rotational frame was proposed in [TU2011B]. Since the circulating harmonic currents are mainly even-order components, a series of resonant controllers tuned at even-order harmonic frequencies [LI2013D] and a plug-in repetitive controller [ZHA2014] [HE2015] were adopted in each leg to suppress the lower-order harmonic currents. A model-based predictive control strategy was proposed in [QIN2012] though the drawback of this method is the calculation complexity, especially for MMCs with large numbers of SMs.

2.2.3 Modulation techniques

The well-known modulation method at high switching frequency based on triangular-wave carrier waveforms with phase disposition (PD) [KON2009] [SAE2011] [HAS2012] and phase shift (PS) [HAG2009] [TU2011B] are presented in Fig. 2.5 (a) and (b), respectively. The PD PWM displaces N identical triangular carrier waveforms symmetrically with respect to the y axis. According to the phase among the carrier waveforms, the PD method can be further catalogued into: (1) phase disposition (2) phase opposition disposition (POD) (3) alternate phase opposition disposition (APOD). The disadvantage of these methods is the unequal distribution of the switching signal, which results in unbalanced capacitor voltage. To improve the performance of the PD PWM method on capacitor voltage balancing, a modified PD PWM method with voltage balancing control was proposed in [SAE2011]. In [MEI2014], a PD PWM method with selective loop bias mapping method for capacitor voltage balancing was presented. In this method, the maximum/minimum capacitor voltages and the direction of arm current are used to distribute the switching signals to SMs. The PS PWM method arranges *N* triangle carrier waveforms each with a phase shift of 2π/N. In contrast to the PD PWM method, the PS PWM method offers an equal distribution of the switching signals to SMs and has better capacitor voltage balancing performance. In [ILV2015], the effect of the switching frequency on the capacitor voltages, circulating currents and alternating voltages using the PS PWM method was analysed. In [LI2015], the harmonic characteristics of the PS PWM were analysed. Based on the analysis, the optimum displacement angles were specified for output voltage harmonic minimization and circulating current cancellation. An improved PS PWM method eliminating DC-link current ripple and ensuring balanced capacitor voltage was proposed in [DEN2015]. To reduce the switching frequency of the PS PWM technique, a reduced switching-frequency voltage balancing algorithm was developed [TU2011B].



(a) PD PWM (b) PS PWM

Fig. 2. 5 Two main modulation methods for the MMC

Modulation methods with lower frequency, especially on fundamental switching frequency were presented and analysed in [TU2011A] [KOU2007] [ILV2012B]. A nearest level control (NLC) modulation method was proposed [TU2011A], in which the voltage level was calculated by the reference voltage versus the nominal capacitor voltage. The NLC technique is easy to implement with less computational complexity and a lower switching frequency, compared to the other PWM techniques.

2.2.4 Control strategies under special operation conditions

A. Unbalanced conditions

Although extensive work on the modelling and control of the MMC has been carried out, most of the studies were based on symmetric conditions (i.e. balanced input voltages and symmetric arm impedances). MMC operation under unbalanced input AC voltage conditions was analyzed in [TU2012] [GUA2012] [MOO2013] [ZHO2013] [SHI2015]. It revealed that under such unbalanced conditions, the common-mode current not only contains a DC component and even-order circulating harmonic components, but also includes a second-order zero-sequence harmonic component within the three converter legs, resulting in second-order harmonic components in the DC voltage and current. To eliminate the second-order harmonic oscillations on the DC voltage and current, two methods were proposed: one suppresses the DC voltage ripple [TU2012], and the other directly eliminates the zero-sequence harmonic current [GUA2012][MOO2013][ZHO2013]. In [ZHO2013], the possible impact of MMC with asymmetric arm impendence was briefly mentioned and it revealed unequal split of the AC current between the upper and lower arms, resulting in a fundamental frequency component in the common-mode current. However, the detailed system analysis and investigations of the influence of the common-mode current flowing into both AC and DC sides caused by asymmetric arm impedance have not been conducted, and the specific control requirement has not been considered. In [SHI2015], the analysis and control of a modular multilevel converter-based HVDC transmission system under unbalanced input AC voltage conditions caused by three possible single-line-to-ground fault conditions with special focus on the investigation of their different fault characteristics was presented, and a corresponding control strategy with proportional resonant controller was adopted to regulate the positive-, negative and zero-sequence components.

B. Fault conditions

For HVDC transmission systems, operation and protection during DC faults has become one of the main challenges for the expansion, especially into multi-terminal HVDC systems. In contrast to the conventional two-level VSCs which contain a single large DC capacitor that can cause severe discharging current under a DC fault, MMC avoids such issue due to its configuration of large numbers of small distributed DC capacitors connected in each SM which are bypassed after the blocking of the

SMs. However, the conventional HB-MMC does not have DC fault blocking capability. As shown in Fig. 2.6 (a), in case of a DC fault the fault current flows through the anti-parallel diodes of the SMs from the AC side to the DC side, even after IGBT blocking. This could potentially damage the diodes and results significant disturbance to the connected AC networks. To solve such issues in HB-MMC, several methods have been proposed for protecting the converters and AC systems:

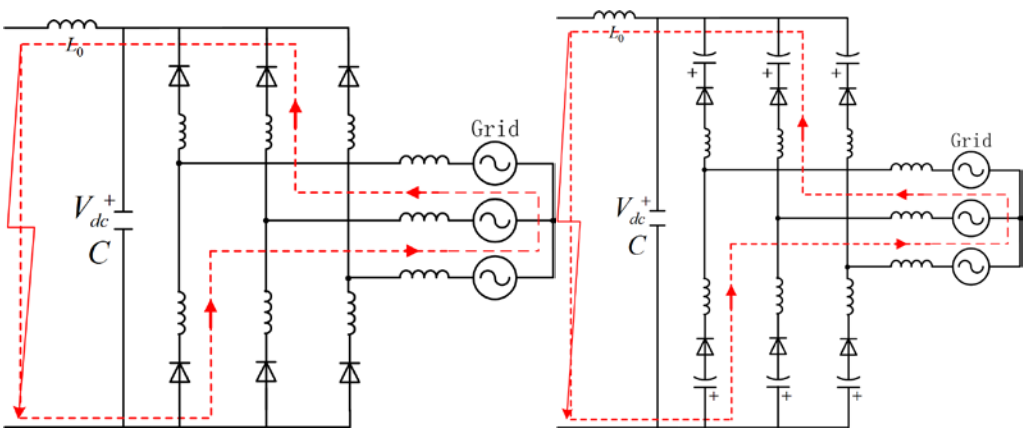
(1) Adopting AC circuit breakers (ACCBs) [TAN2007] [CAN2011]. The drawback of this method is the slow response of ACCB with a delay of a few cycles. This becomes problematic for both the converter as it has to withstand high fault current and the connected networks since it could take considerable time for the system (especially multi-terminal system) to recover from such a DC fault [JIN2013].

(2) Adopting DC circuit breakers (DCCBs). Using DCCB is a quick and efficient method to isolate the DC fault, especially for the multi-terminal HVDC systems. But, unlike AC systems, no zero crossing in the DC current indicates DCCBs have to adopt different designs compared to ACCBs. Although the DCCB has recently been developed, the technique is not mature and is costly [BUC2012] [SAN2014].

(3) Thyristor for bypassing SM. Thyristors connected in parallel to the AC outputs of the SMs have been employed [FRI2010] [LI2013B] to bypass short-circuit current and protect the free-wheeling diodes. However, this method cannot isolate DC fault and additional devices are still required for fast fault isolation.

(4) Improved MMC topology with DC fault blocking capability. One classical topology is FB-MMC. For FB-MMC during the DC fault, as shown in Fig. 2.6(b), the capacitor voltages of the FBSMs in each arm appear as serially connected voltage sources and have opposite polarity to the direction of the fault current flown from the AC side. Since the total series voltage is higher than the AC voltage, DC faults can be blocked. However, the number of power devices is doubled in each SM compared to the HBSM. This not only

increases the costs for high power MMC systems but also results in higher power loss as the current in each SM has to flow thought two power devices instead of one in a HBSM. In view of this, CDSM was proposed in [MAR2010][MAR2011], which has reduced number of power semiconductor devices compared to FBSM while retaining DC fault blocking capability, as shown in Fig. 2.7. In normal operation, a CDSM is equivalent to two serial HBSMs, as S_5 is always closed. So the total losses are slightly increased. In case of a DC fault, S_5 is turned off, the fault current has two parallel path to flow through the capacitors in each arm, which can offer enough reverse voltage to block the fault current.



(a) HB-MMC (b) FB-MMC

Fig. 2. 6 Equivalent circuit of the MMC under blocking mode

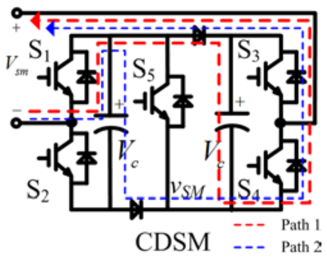


Fig. 2. 7 Fault current path flowing through different SM topologies

2.3 MMC design principles

Apart from selecting suitable semiconductor devices, other main design parameters for MMC systems include capacitor value and arm inductor value. These parameters are determined by short-circuit current limits, arm current ripples, capacitor voltage ripples, reliability, and power losses [DEB2015].

2.3.1 Capacitor and arm inductor values

The capacitor value is considered as a trade-off by two aspects, i.e. voltage ripple and size. The capacitor voltage ripple has been analyzed in depth under various operation conditions in [GUA2010] [CEB2011] [ENG2011] [YAN2011] [BAR2012]. It is found that the capacitor voltage ripple is related to the active power transmitted, the nominal voltage of capacitor, modulation index and the power factor. In [BAR2012], the relationship of the stored energy, maximum voltage ripple limit, and the active power transmitted was presented for choosing the capacitor value.

The arm inductors in the MMC have two main purposes: (1) reduce the high-frequency harmonics in the arm current; (2) restrain the rising time of the fault current flowing through the arms during a DC fault. With respect to these two aspects, constrains for arm inductor value were analyzed in [TU2010] [LI2013C] [SHI2013]. The design principle for arm inductors in terms of the requirement for suppressing the circulating current, mitigating switching ripple and limiting DC fault current was presented in [SHI2013].

2.3.2 Loss evaluation

As one of the most attractive features of MMC for HVDC applications, the power losses in the MMC can be potentially reduced to less than 1% (0.92% quoted in [MOD2011]), compared to the conventional two-level VSC system with power losses higher than 1% (1.6% in [AHM2012]). Semiconductor power losses include the conduction loss and the switching loss [DEB2015]. The conduction loss is defined by multiplying the on-state saturation by the on-state current [DAH1995]

$$P_{CL} = V_{on} \cdot I_{on} \tag{2.1}$$

where I_{on} is the conducting current flowing through switching devices, and V_{on} is the voltage drop across switching device, equalling $V_{on} = R_{on} \cdot I_{on} + V_{ce0}$, R_{on} is the on-state resistance, and V_{ce0} is voltage drop with no load.

Thus, the conduction loss can be calculated as

$$P_{CL} = \frac{1}{T}\int_0^T v_{on}(t)\cdot i_{on}(t)dt = \frac{1}{T}\int_0^T \left(R_{on}\cdot i_{on}(t) + V_{ce0}\right)i_{on}(t)dt = R_{on}\cdot I_{rms}^2 + V_{ce0}\cdot I_{av} \qquad (2.2)$$

Where T is switching period, I_{rms} and I_{av} is the RMS and average value of current ion over one switching period, R_{on} and V_{ce0} can be derived from the datasheet of IGBT.

In MMC system, I_{rms} and I_{av} are relevant to the switching function d_i of each IGBT and corresponding arm current i_{arm} across IGBT. So the conduction loss of each IGBT in MMC can be calculated as

$$P_{CL} = R_{on}\cdot d_i\cdot i_{arm}^2(t) + V_{ce0}\cdot d_i\cdot i_{arm}(t) \qquad (2.3)$$

A simple switching loss evaluation is to linearize the switching energy as a function of collector-emitter current

$$E_{SL} = k_1\cdot i_{on} + k_2 = k_1\cdot d_i\cdot i_{arm} + k_2 \qquad (2.4)$$

Where: k_1, k_2 are derived from the datasheet of IGBT.

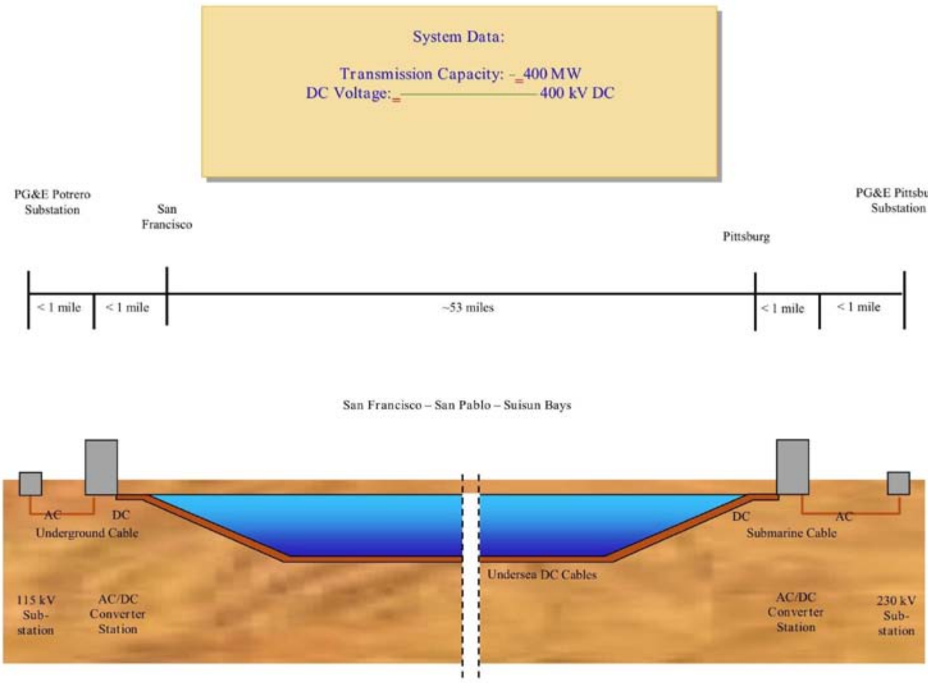
So the average switching losses for the MMC can be expressed as

$$P_{SL} = \frac{f_s}{2\pi}\int_\alpha^\beta \left(k_1\cdot d_i\cdot i_{arm} + k_2\right)d\omega t \qquad (2.5)$$

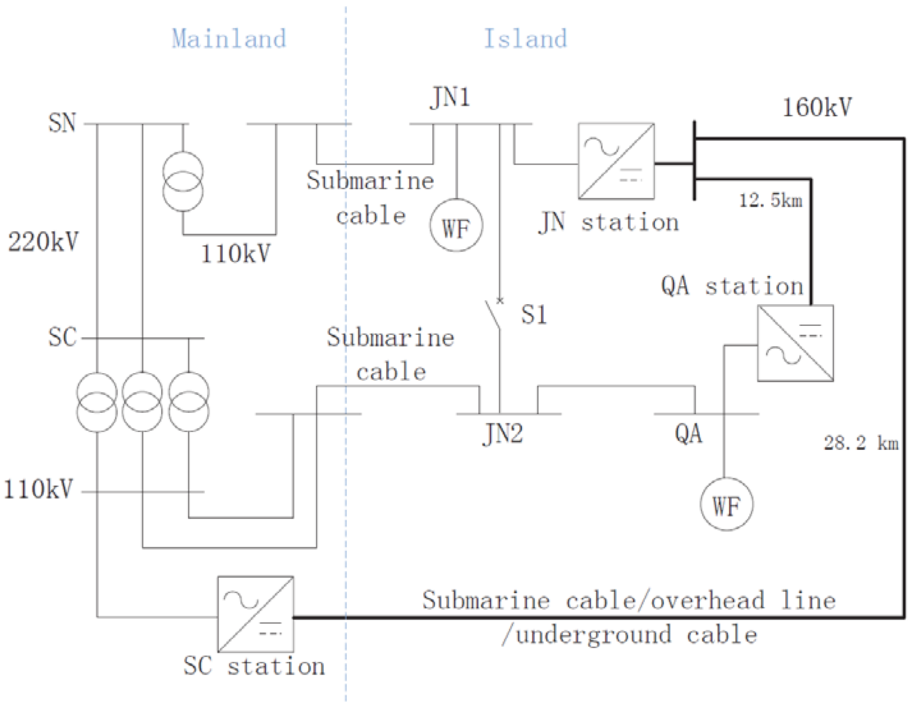
There are two main calculation methods to evaluate the power losses. The first method is based on mathematical modelling and analytical equations to calculate the conduction losses and the switching losses during one period, as presented in [MOD2011] [OAT2011]. But this method has a potential error since it is based on the simplified modelling and waveforms of voltage and current. The other method is based on the simulation data acquired from the professional software [ROH2010B] [LIU2011]. It can provide relatively accurate evaluations for power losses, but it has a computational complexity in a large-scale MMC system.

2.4 Applications for commercial HVDC projects

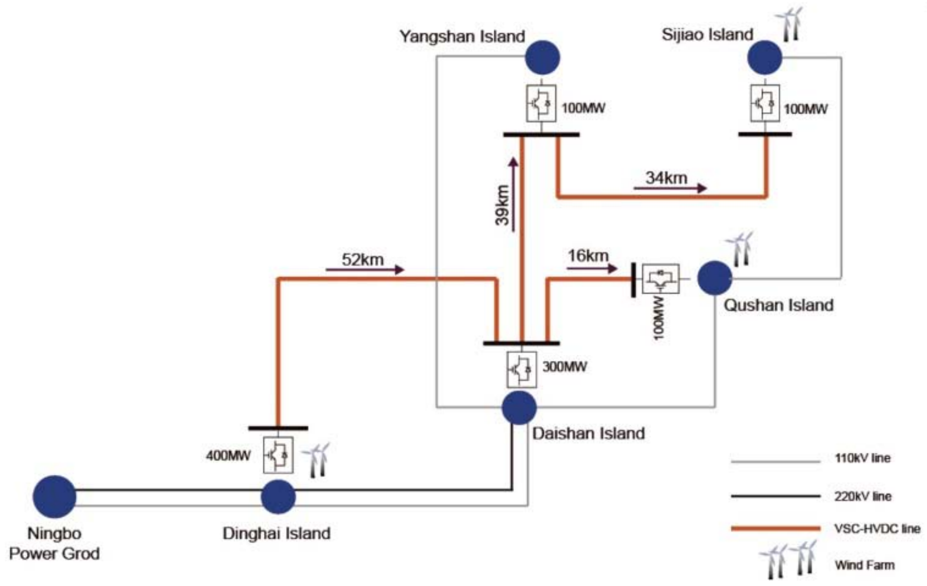
With the distinct advantages of the MMC in the high-power and high-voltage field, many commercial HVDC projects have been developed or planed all over the world, such as the Trans Bay Cable Project commissioned by Siemens in 2010 [TBC2010] [KNA2011] [TEE2011], Nanao Three-terminal VSC-HVDC Project by China Southern Power Grid in 2014 [FU2014] [LI2014B] and Zhoushan Five-terminal VSC-HVDC project by State Grid Corporation of China in 2014 [HAO2014]. The Trans Bay Cable Project is the first commercial VSC-HVDC project adopting MMC topology in the world, which is used to deliver power from Pittsburgh converter station in North-East of San Francisco to the Potrero converter station in the centre of the city by a 88 km submarine DC cable. The rated power is 400 MW with a DC voltage of ±200kV. The schematic diagram is illustrated in Fig. 2.8 (a). Following this successful project, two multi-terminal VSC-HVDC projects based on MMC technique are constructed in China in 2014. The Nanao Three-Terminal VSC-HVDC project is the first multi-terminal VSC-HVDC industrial project using MMC, which is designed to extract wind energy from the wind-wealthy area on the Nanao Island to the bulk power system at the mainland of China by 32km submarine DC cable. The rated power is 200 MW with a DC voltage of ±160kV, the schematic diagram is shown in Fig. 2.8 (b). The Zhoushan Five-Terminal VSC-HVDC project based on MMC is also commissioned in China in 2014, which is featured as the highest voltage, most terminals and largest single-terminal capacity in the world. The total rated power is 1GW with a DC voltage of ±200kV. The configuration of five-terminal system is presented in Fig. 2.8 (c).



(a) Trans Bay Cable Project [TBC2010]



(b) Nanao Three-Terminal VSC-HVDC Project [LI2014B]



(c) Zhoushan Five-Terminal VSC-HVDC Project [HAO2014]

Fig. 2. 8 Schematic diagrams for some commecial HVDC projects based on MMC

2.5 Summary

The MMC, since it was proposed in 2003, has drawn much attention in academic and industry research, due to its salient features for high-power and high-voltage applications, such as modular design, high efficiency and scalability, and excellent output waveform with low harmonic distortion. In this chapter, a general literature review of MMCs has been conducted, considering the most significant research points, such as topologies, control and modulation methods and design principles. A thorough comparison of the main topologies of SM circuit is used to highlight the advantages and disadvantages of various SM topologies. For the control and modulation methods, the key issues are discussed on controlling the capacitor voltage balancing and eliminating circulating current. Since the MMC is consisted of a large amount of power semiconductors used for high-power and high-voltage application, the device costs and power losses should be carefully considered. Thus, in the third part, review on design principles has been discussed with respect to the determinant factors for the value of the basic components, such as capacitor and arm inductor, as well as two popular evaluation methods for power loss evaluations of the

MMC. Finally, three typical commercial HVDC projects based on MMC configuration are introduced.

Chapter 3

Analysis and operation of the conventional modular multilevel converter

This chapter presents the operation of the conventional MMC with HBSMs or FBSMs. The mathematic models of the MMC are provided to analyse its control principles. Based on the general review conducted in Chapter 2, the widely-used phase disposition modulation method with sorting and selecting algorithm for capacitor voltage balancing [SAE2011] is adopted as the basic control strategy of the MMC. Compared with the HBSM, the FBSM can generate negative voltage states which will change the relationship among its AC/DC voltages and currents. A detailed analysis on the relationship between capacitor voltage variation and the maximum modulation index for the FB-MMC with the negative voltage state is carried out. The conventional HB-MMC, FB-MMC, and boost FB-MMC are then compared in terms of the number of semiconductor devices and power losses. The different behaviours of HB-MMC and FB-MMC under DC fault conditions are also analysed in depth. A three-phase MMC simulation model is developed using Matlab/Simulink and corresponding simulation results are presented. A single-phase MMC prototype is developed for experimental verification. Simulation and experiment results demonstrate the feasibility and validity of the operational performance for the HB-MMC and FB-MMC.

3.1 Basic operation principles

Fig. 3.1 shows the structure of one phase of a MMC. V_{dc} is the DC-link voltage, L_0 is the arm inductor in each arm and C is the capacitor in each SM. v_{pa} and v_{na} are the total voltages generated by all the SMs in the upper and lower arms, respectively. i_{pa} and i_{na} are the current in the upper and lower arms, respectively. i_a is the output AC phase current.

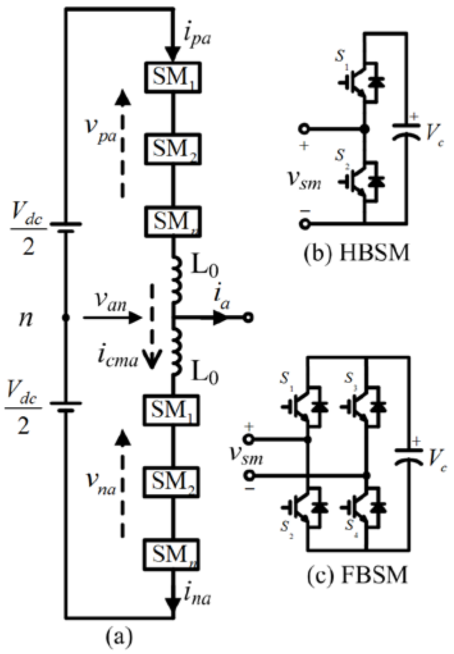


Fig. 3. 1 Basic structure of a MMC and different sub-module arrangement

According to Fig. 3.1 (a), the phase *a* arm current i_{pa} and i_{na} can be expressed as

$$i_{pa} = \frac{i_a}{2} + i_{cma} \tag{3.1}$$

$$i_{na} = -\frac{i_a}{2} + i_{cma} \tag{3.2}$$

where i_{cma} is the common-mode current in phase *a* flowing through both the upper and lower arms and has no effect on the output phase current. It can be given as

$$i_{cma} = \frac{i_{pa} + i_{na}}{2} \tag{3.3}$$

Taking the neutral point *n* of the DC link as the reference point, the voltage equations can be expressed as

$$L_0 \frac{di_{pa}}{dt} = e_a - v_{an} \tag{3.4}$$

$$L_0 \frac{di_{na}}{dt} = v_{an} - e_a \tag{3.5}$$

where e_a is the inner emf generated in phase a and is expressed as

$$e_a = \frac{V_{dc}}{2} - v_{pa} = -\frac{V_{dc}}{2} + v_{na} = \frac{v_{na} - v_{pa}}{2} \tag{3.6}$$

Combing (3.4) and (3.5) with (3.1) and (3.2), the relationship among the output current i_a, the inner emf e_a and the AC voltage v_{an} can be expressed as

$$\frac{L_0}{2}\frac{di_a}{dt} = e_a - v_{an} \tag{3.7}$$

It is observed that i_a can be regulated by controlling the inner emf e_a. Thus, the classic current vector control strategy for conventional two-level VSC based on dq coordinates, including an outer power controller and an inner current controller can also be used in MMC, as schematically shown in Fig. 3.2. As shown, P* and Q* denote the reference values of the active and reactive power; P and Q denote the measured active and reactive power; i_d* and i_q* are the reference values of the AC currents in dq coordinates; i_d and i_q are the measured AC currents. A common phase deposition modulation method with sorting and selecting capacitor voltage balancing strategy is adopted to produce the required arm voltage and to ensure the capacitor voltages in each SM are balanced. As this has been well documented [SAE2011] [TU2011B], no further details are given here.

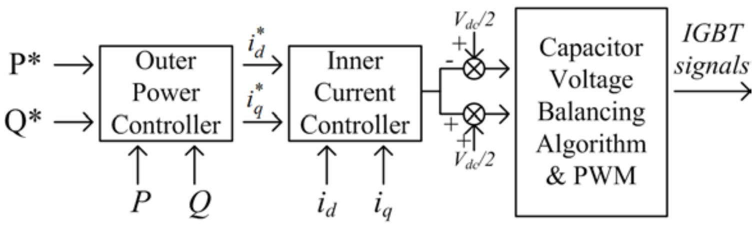


Fig. 3. 2 Control structure of the AC current controller for the MMC system

For the operation of a MMC, the following equation defines the DC voltage and must be satisfied under any conditions

$$v_{pa} + v_{na} = V_{dc} \tag{3.8}$$

Combine (3.6) and (3.8), the required arm voltage references are calculated as

$$v_{pa}^* = \frac{V_{dc}}{2} - e_a\,, \quad v_{na}^* = \frac{V_{dc}}{2} + e_a \tag{3.9}$$

As shown in Fig. 3.1 (a), the circulating current i_{cma} can be written as

$$L_0 \frac{di_{cma}}{dt} = \frac{v_{dc} - (v_{pa} + v_{na})}{2} \tag{3.10}$$

Thus, the common-mode current i_{cma} can be controlled by regulating the sum of the upper arm voltage v_{pa} and the lower voltage v_{na}. To eliminate the AC current with double fundamental frequency in the common current AC as analysed in [ILV2012A], a PR (proportional and resonant) controller with the resonant frequency of $2\omega_0$ (ω_0 is the fundamental frequency) is adopted in each leg, and the transfer function of the PR controller is [HU2009]

$$G(s) = K_p + \frac{2K_{r1}s}{s^2 + (\omega_0)^2} \tag{3.11}$$

The control structure for phase *a* is shown in Fig. 3.3, where the high pass filter (HPF) removes the DC component and extracts the AC components $\tilde{i}_{cma}$ from the common mode current i_{cma}. The cut-off frequency of the HPF can be set at a low frequency, e.g. a few Hz, due to the fact that dynamic response is not the main concern for this controller. $\tilde{i}_{cma}^*$ is the reference value for the AC common mode current which is set to zero to completely eliminate such components. The output from the PR controller, Δv_a, is added/subtracted to/from the normal upper and lower arm voltage references (i.e. v_{pa}^* and v_{na}^*) generated by the AC current controller shown in Fig. 3.2.

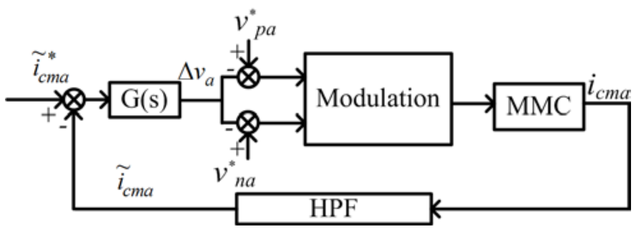


Fig. 3. 3 Control structure of the common-mode current for phase *a*

The complete MMC control structure is shown in Fig. 3.4, where i_{cm} denotes the common-mode current. The voltage references v_p^* and v_n^* are generated by the AC current controller which regulates the active and reactive power, and the circulating current controller which suppresses the double frequency circulating current.

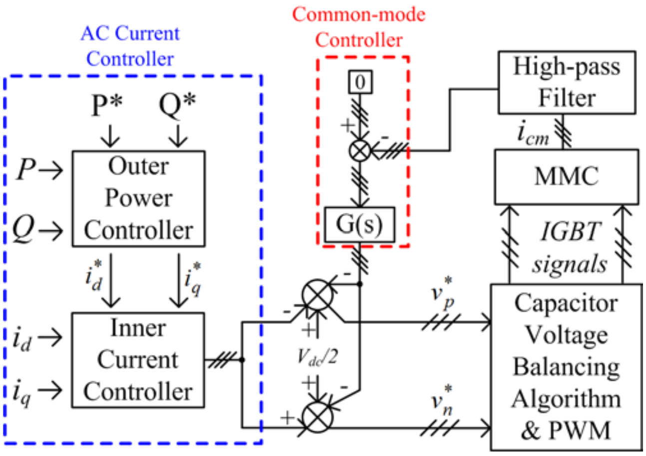


Fig. 3. 4 Overall control structure for the three-phase MMC system

3.2 Analysis of FBSM with negative voltage state

Tables 3-1 and 3-2 show the switch states for an FBSM and HBSM, respectively. Compared with the HBSM which can generate voltage states of V_c and 0, each FBSM can generate a third state of $-V_c$. Since adopting the negative voltage state in FBSM changes the relationship of AC/DC voltages and AC/DC side power, the arm current will also be affected, resulting in the change of capacitor voltage ripple in each SM. Thus, to keep a stable system, the limit on the number of FBSMs allowing generating the negative voltage state needs be investigated.

Table 3- 1 Switching states of FBSM

STATE	S_1	S_2	S_3	S_4	V_{SM}	V_C ($i_{SM} > 0$)
1	1	0	0	1	V_C	*charging*
2	0	1	0	1	0	*bypassed*

3	1	0	1	0	0	*bypassed*
4	0	1	1	0	$-V_C$	*discharging*
BLOCK	0	0	0	0	-	-

Table 3- 2 Switch states of HBSM

STATE	S_1	S_2	v_{sm}	$V_c\,(i_{sM}>0)$
1	1	0	V_C	*charging*
2	0	1	0	*bypassed*

3.2.1 Principle of -V_c operation

The principle of the scheme is to make some of the SMs in each arm generate the voltage state of $-V_c$ so as to alter the voltage relationship between the DC and AC sides.

Considering the total number of SMs in each arm is N and the voltages across all the SM capacitors are balanced at V_c, the maximum voltage range each arm can produce is between 0 and NV_c for conventional method without using the $-V_c$ state. Therefore, the maximum value of the peak phase and DC voltages are given as

$$V_{dc} = NV_c, \quad V_{m\_\max} = \frac{NV_c}{2} = \frac{V_{dc}}{2} \tag{3.12}$$

If a maximum number of M SMs are allowed to operate at the $-V_c$ state in each arm ($M < N$), the maximum voltage range each arm can produce is now between $-MV_c$ and NV_c. Under such conditions, the peak phase voltage and DC voltage are given as

$$V_{dc} = (N-M)V_c,\ V_{m\_\max} = \frac{(N+M)V_c}{2} = \frac{V_{dc}}{2}\frac{(N+M)}{(N-M)} \tag{3.13}$$

Take $M = N/3$ as an example, i.e., one third of the SMs in each arm is allowed to produce $-V_c$, (3.13) can be written as

$$V_{dc} = \frac{2NV_c}{3}, \quad V_{m\_\max} = \frac{2NV_c}{3} = V_{dc} \tag{3.14}$$

Comparing (3.14) and (3.12), if V_c remains unchanged, it can be seen that although the DC voltage is now reduced with the proposed operation, the maximum AC voltage that the MMC can produce increases from $NV_c/2$ to $2NV_c/3$ (for this reason, it is named here as Boost FB-MMC, i.e. higher dc ultilization). Alternatively, if the DC voltage is to remain at the same level after introducing the $-V_c$ state, the number of SMs needs be increased by 50% but the AC output voltage increases by 100% compared to conventional control without using $-V_c$.

3.2.2 Capacitor voltage ripple

Since the modulation index, arm current and DC current in the Boost FB-MMC after introducing the $-V_c$ state are different to those in the conventional method, the capacitor voltages in each SM are analysed to ensure they can remain balanced.

Neglecting converter power loss, the power balance equation between the three-phase AC and DC can be expressed as

$$P_{dc} = V_{dc}I_{dc} = \frac{3V_m I_m \cos\varphi}{2} = P_{ac} \tag{3.15}$$

$$V_m = \frac{mV_{dc}}{2} \tag{3.16}$$

where I_m is the peak value of the output phase current, m is the equivalent modulation index, and φ is the voltage and current phase angle.

Assuming the arm current is directly controlled with no second-order harmonic circulating current, the arm voltage and current (taking phase *a* as an example) can be given respectively as

$$\begin{aligned} v_{pa} &= \frac{V_{dc}}{2} - V_m \sin \omega t \\ i_{pa} &= \frac{I_{dc}}{3} + \frac{I_m \sin(\omega t - \varphi)}{2} \end{aligned} \tag{3.17}$$

Combining (3.15) (3.16) and (3.17) yields the arm current as

$$i_{pa} = \frac{m I_m \cos\varphi}{4} + \frac{I_m \sin(\omega t - \varphi)}{2} \tag{3.18}$$

The instantaneous power flowing through the upper arm can be calculated as

$$p_{pa} = v_{pa} \times i_{pa} = \left(\frac{V_{dc}}{2} - V_m \sin \omega t\right)\left(\frac{I_{dc}}{3} + \frac{I_m}{2}\sin(\omega t - \varphi)\right) \tag{3.19}$$

Integrating (3.19) and substituting I_{dc} with (3.15) and (3.16), the energy variation $\Delta E(t)$ on the capacitors can be expressed as

$$\Delta E(t) = \frac{V_m I_m}{8\omega}\sin(2\omega t - \varphi) - \frac{V_{dc} I_m}{4\omega}\cos(\omega t - \varphi) + \frac{V_m^2 I_m}{2\omega V_{dc}}\cos\omega t \cos\varphi \tag{3.20}$$

According to $\Delta E(t) = \left[C V_c^2(t) - C V_{c0}^2\right]/2$, the voltage on each SM capacitor can be calculated as

$$V_c(t) = \sqrt{\frac{2\Delta E(t)}{C} + V_{c0}^2} \tag{3.21}$$

where V_{c0} refers to the capacitor initial voltage.

Assuming the initial capacitor voltage is balanced at $V_{dc}/(N\text{-}M)$ as seen from (3.13), the SM capacitor voltage is given as

$$V_c(t) = \sqrt{\frac{V_m I_m}{4\omega C}\sin(2\omega t - \varphi) - \frac{V_{dc} I_m}{2\omega C}\cos(\omega t - \varphi) + \frac{V_m^2 I_m}{\omega C V_{dc}}\cos\omega t \cos\varphi + \left(\frac{V_{dc}}{N - M}\right)^2} \tag{3.22}$$

For a simplified system containing 3 FBSM for each arm and rated at 6 kV DC and 9 MW, Fig. 3.5 compares the calculated capacitor voltage ripples using (3.22) and the simulation results using Matlab/Simulink. The nominal capacitor voltage in each SM is 3 kV and the DC voltage of 6 kV is defined as the unit voltage. It can be seen that the waveforms match well. The slight differences in the maximum and minimum values are caused by the fact that the arm current used for calculation only includes the DC and fundamental components whereas the arm current in the simulation contains small 2nd order circulating current.

For different M/N ratios, the capacitor voltage ripples within a 360 degree fundamental cycle are calculated using the previous parameters and illustrated in Fig. 3.6. It can be observed that voltage ripples are relatively lower when M is less than N/3, which is comparable to conventional case without using negative voltage state (i.e., M=0). According to (3.13), (3.15) and (3.16), the increase of M results in increased modulation index *m*. This in turn will make the arm current largely positive for inverter operation (and largely negative for rectifier operation), as seen in (3.18). For example, when M > N/3, $m > 2$ and the arm current i_{pa} becomes purely positive (for unit power factor i.e., $\cos\varphi = 1$). This significantly affects the charging and discharging periods for the capacitors in the SMs and results in higher voltage ripple. Thus, in order to keep balanced capacitor voltage, M is chosen to be less than N/3.

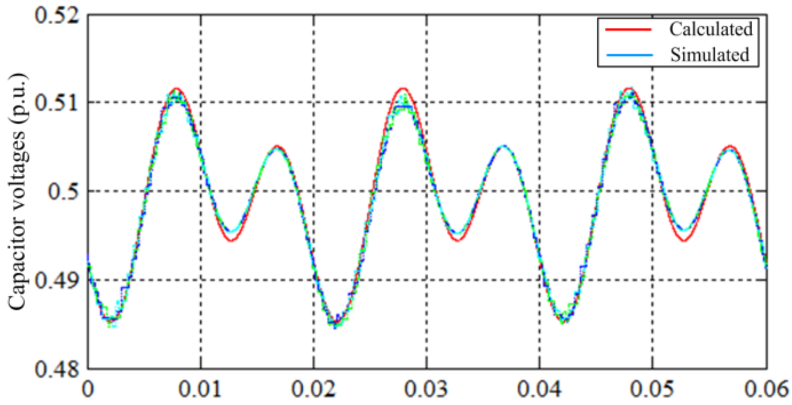


Fig. 3. 5 Comparison of calculated and simulated capacitor ripples (N = 3, M = 1, V_{dc}=6 kV, P=9 MW, m = 1.6, $\cos\varphi = 1$, C = 1000 uF)

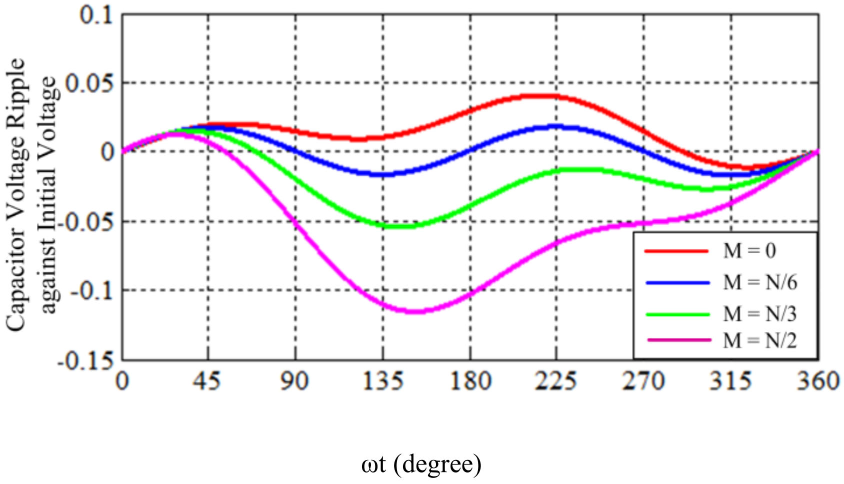


Fig. 3. 6 Voltage ripples with different ratios of M/N

3.2.3 DC fault blocking

For the boost FB-MMC with the proposed control, the AC voltage is increased for the same DC voltage and thus it is important to check that the arm capacitor voltage is still sufficiently high to block the fault current.

According to (3.13), (3.14) and (3.16), in the proposed strategy the maximum modulation index is 2 and the maximum peak line-to-line AC voltage seen by the MMC during a DC fault is

$$u_{\max} = \sqrt{3} \times \frac{N+M}{2(N-M)} V_{dc} \tag{3.23}$$

The arm voltage formed by the voltages of the N capacitors is given as

$$u_{arm} = NV_c = \frac{N}{(N-M)} V_{dc} \tag{3.24}$$

Therefore, the blocking voltage formed by the two arm voltages (one upper arm and one lower arm) and the AC line-to-line voltage has the following relationship

$$u_{\max} = \frac{\sqrt{3}}{2} \frac{N+M}{(N-M)} V_{dc} < \frac{2N}{(N-M)} V_{dc} = 2u_{arm} \tag{3.25}$$

This proves that although the AC voltage in the boost FBSM is increased, the converter still has sufficient capacitor voltage to block any DC faults. For case of M=N/3, the maximum AC line-to-line voltage is $\sqrt{3}V_{dc}$ compared to the blocking DC voltage of $3V_{dc}$ formed by the two arms.

3.3 Loss evaluation

To evaluate the power losses of the three MMC configurations, a simple loss calculation method based on the simulation data is adopted [ROH2010B]. The main parameters of the semiconductor module are derived from the datasheet of the 5SNA 1200G450300 [BAC2012], and the main parameters of the four MMC systems are shown in Table 3-3. The carrier frequency is 2.5 kHz for all four MMCs and the actual switching frequency for the SMs are also shown in Table 3-3. It is found that the boost FB-MMC employs 33.5% less number of power semiconductors than that of conventional FB-MMC, under the same rated-power conditions. It also should be noted that the HB-MMC is the most efficient among these three types of MMC, but the boost FB-MMC is more efficient than the FB-MMC, since it doubles the power transmission capacity, although it adds 50% number of SMs in each arm.

Table 3- 3 Parameters of the comparison system

Item	HB-MMC	FB-MMC	Boost FB-MMC
MMC rated power	6 MW	6 MW	12 MW
DC voltage	6 kV	6 kV	6 kV
AC voltage (phase-phase rms)	3 kV	3 kV	6 kV
AC current (rms)	1154.7 A	1154.7 A	1154.7 A
Number of SMs per arm	2	2	3

Number of IGBTs/diodes per SM	2	4	4
SM capacitor	2200 uF	2200 uF	2200 uF
SM capacitor voltage	3 kV	3 kV	3 kV
Inductance per arm	20 mH	20 mH	40 mH
MMC switching frequency	2.5 kHz	2.5 kHz	2.5 kHz
Power capability per IGBT (p.u.)	4.17%	2.08%	2.78%
Conduction Losses	23.98 kW (0.4% p.u.)	39.2 kW (0.65% p.u.)	72.38 kW (0.6% p.u.)
Switching Losses	43 kW (0.72% p.u.)	43 kW (0.72% p.u.)	82.5 kW (0.69% p.u.)
Total conversion losses	66.98 kW (1.12% p.u.)	82.2 kW (1.37% p.u.)	154.88 kW (1.29% p.u.)

3.4 Simulation results

To verify the system behaviours of the boost FB-MMC, a grid-connected boost FB-MMC is developed using Matlab/Simulink, and is shown in Fig. 3.7. The boost FB-MMC consists of 3 FBSMs in each arm, one of them allowed to generating *–Vc* state. The AC grid voltage is 110 kV, connecting a step-down transformer with a ratio of 110 kV/60 kV. Because of the use of $-V_c$ state, the phase-to-phase AC voltage at the secondary side of transformer is 60 kV for a DC voltage of 60 kV, being higher than the conventional MMC system for the same DC voltage. Each SM has a voltage of 30 kV, i.e., half of the nominal DC voltage of 60 kV. In the simulation, the rated power is 90 MW, the capacitance for all the SMs is 1500 uF, and a conventional phase-disposition PWM method with a carrier frequency is 2.5 kHz is used. The commonly-used sorting and selecting method is used to achieve capacitor voltage balancing, and the common-mode current is suppressed using the aforementioned proportional resonant (PR) controller.

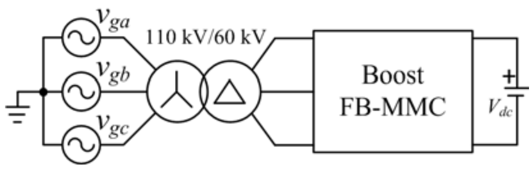


Fig. 3. 7 Schematic diagram of the simulation platform

Fig. 3.8 shows the simulation results illustrating the steady-state performance of the boost FB-MMC. As shown in Figs. 3.8 (c) and (d), although the arm current in the boost FB-MMC is mostly negative (rectifier operation), the SM capacitors can still be charged during $-V_c$ state, ensuring balanced capacitor voltage.

Figs. 3.9 and 3.10 present the different behaviours of the boost FB-MMC and the HB-MMC under a pole-to-pole DC fault conditions. As shown from Fig. 3.9, when the boost FB-MMC is blocked, the fault currents decrease to zero rapidly, which demonstrates its excellent DC fault blocking capability. For the conventional HB-MMC, it can be seen from Fig. 3.10 that when the HB-MMC is blocked, there is large AC fault current flowing from AC to the DC side. It can also be observed from Fig. 3.10 (f) that the capacitor voltage is unchanged during the DC fault period, because the arm fault current is bypassed via the anti-parallel diodes. The results also show the HB-MMC has to rely on the AC breakers which open at 2.1s to isolate the DC fault from the AC grid and to extinguish the fault current.

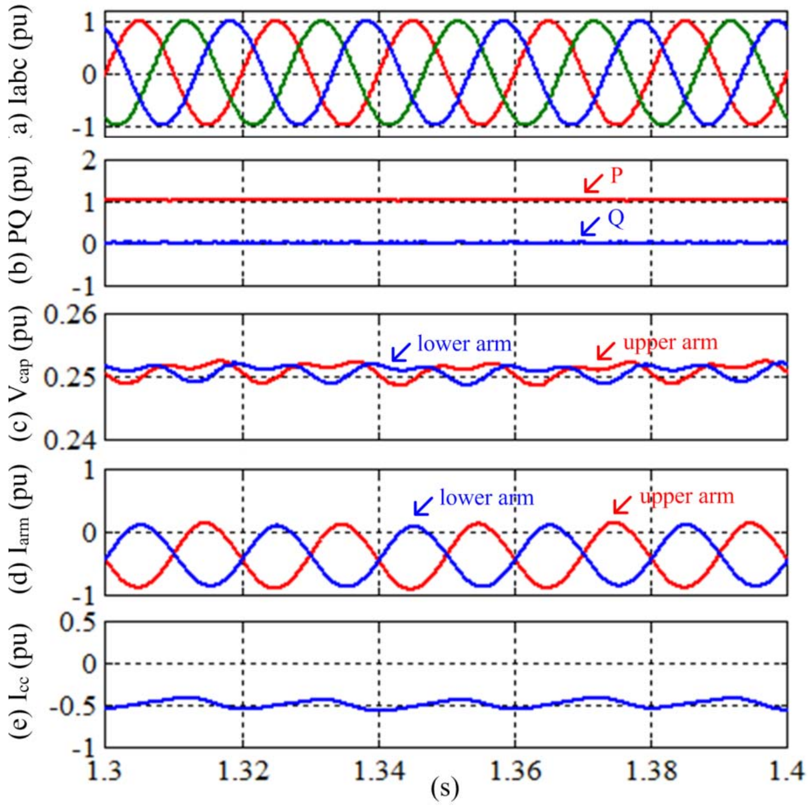


Fig. 3. 8 Simulation results demonstrating the steady-state performance of the boost FB-MMC , (a) AC currents; (b) converter output P and Q; (c) FBSM capacitor voltages; (d) arm currents; (e) common mode arm current.

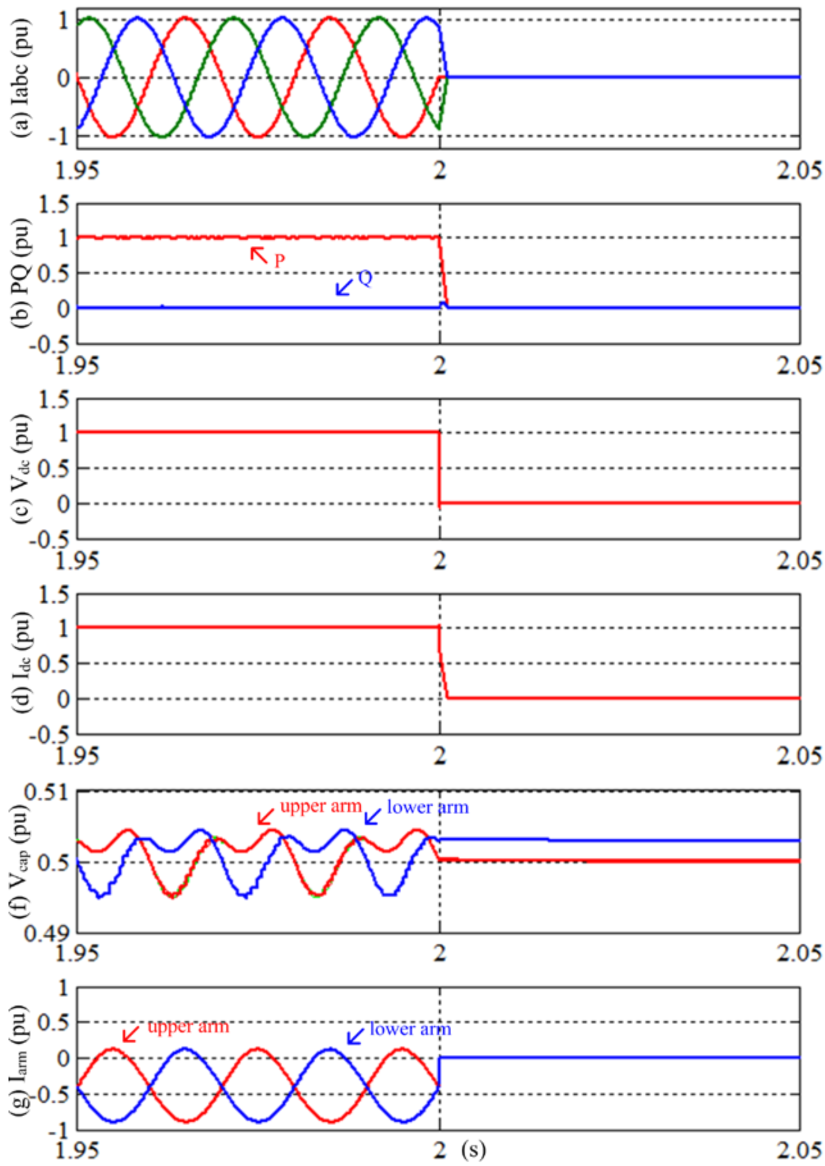


Fig. 3. 9 Behaviours of the boost FB-MMC under a pole-to-pole DC fault conditions, (a) AC currents; (b) converter output P and Q; (c) DC voltage; (d) DC current; (e) capacitor voltages; (f) arm currents.

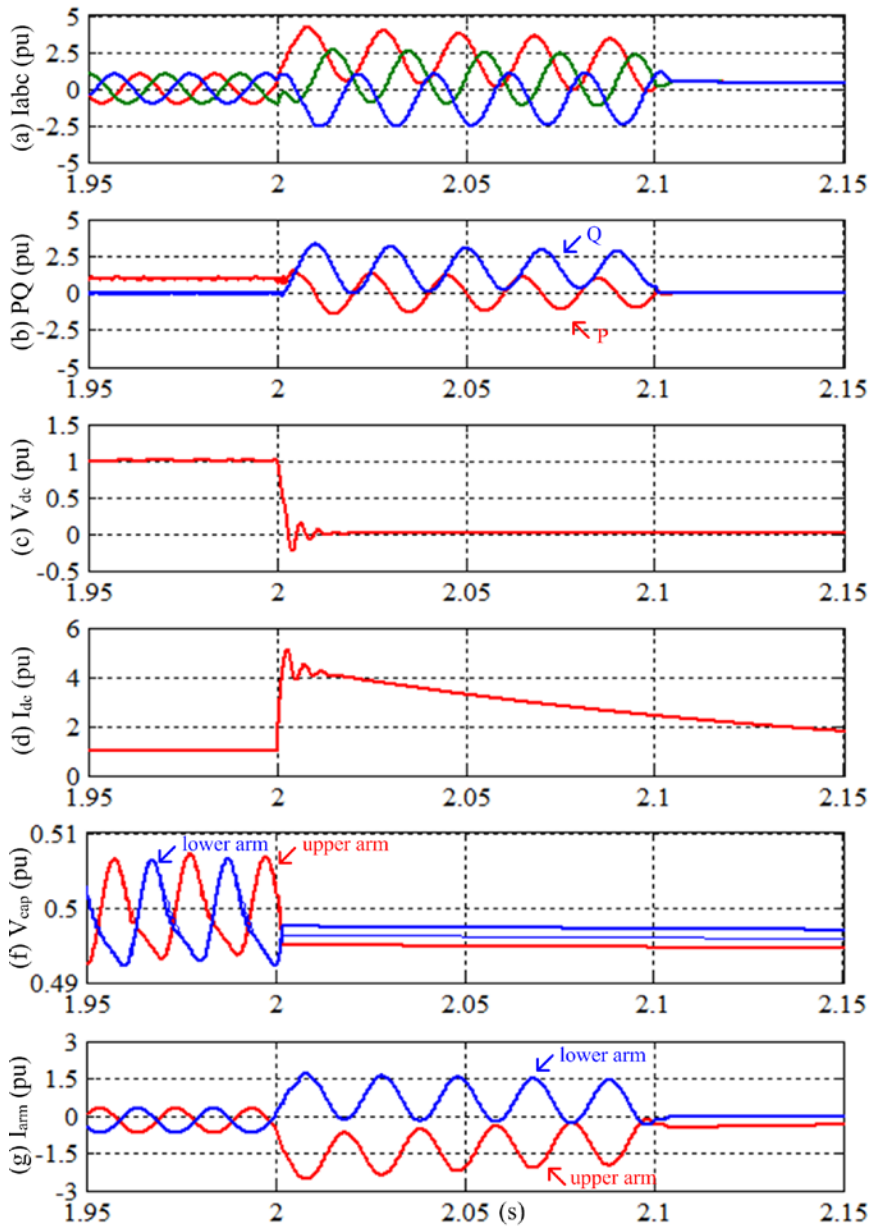


Fig. 3. 10 Behaviours of the conventional HB-MMC under a pole-to-pole DC fault conditions, (a) AC currents; (b) converter output P and Q; (c) DC voltage; (d) DC current; (e) capacitor voltages; (f) arm currents.

3.5 Experiment results

To test the boost FB-MMC, a prototype single-phase MMC rated at 400 W was developed and its schematic diagram and photo are shown in Figs. 3.11 and 3.12, respectively. The control system is implemented using a TMS320F2812 DSP and the main parameters are listed in Table 3-4. Two large DC capacitors connected in series to the DC power supply are used to form the neutral point.

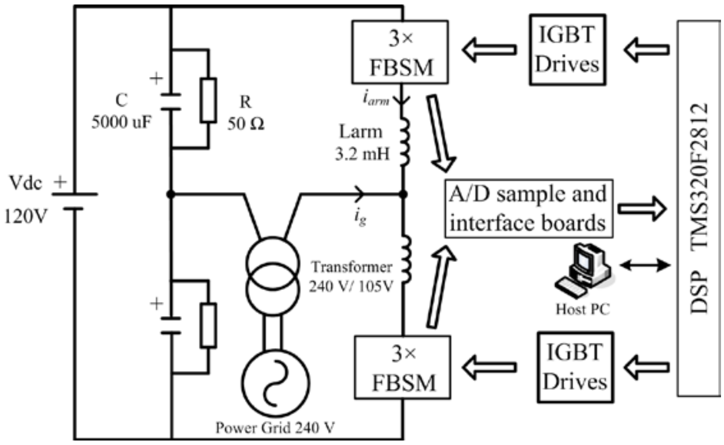


Fig. 3. 11 Schematic diagram of the boost FB-MMC experimental system

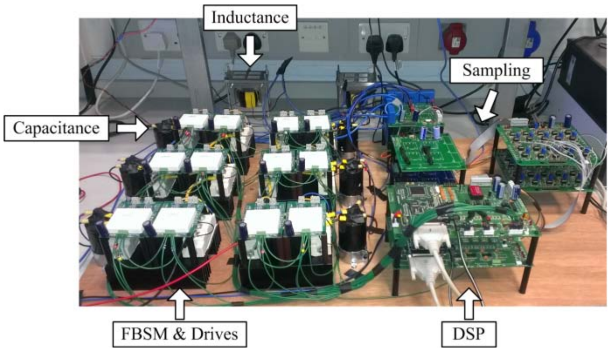


Fig. 3. 12 Experimental platform of the boost FB-MMC

Table 3- 4 Parameters of the experimental MMC system

Item	Values
MMC rated power	400 W
DC voltage	120 V
AC voltage (phase-ground peak)	105 V

Number of SMs per arm	3
DC voltage per SM	60 V
SM capacitor	2200 uF
Inductance per arm	3.2 mH
MMC switching frequency	2.5 kHz

Operating the boost FB-MMC as an inverter in grid-connected mode, i.e. active power flows from the DC to AC, Figs. 3.13 and 3.14 show the steady-state and dynamic performances respectively. As shown in Fig. 3.13, the output current is nearly sinusoidal with very small distortion. Although the i_{arm} is mostly positive, the SM capacitors can still be discharged during $-V_c$. As the SM capacitance used is fairly big in the tests there is only very small capacitor voltage ripple but it remains balanced throughout the tests. In Fig. 3.14, the active power is stepped from 150 W to 350 W. It can be seen that the boost FB-MMC can track the current and power changes quickly and smoothly, demonstrating excellent dynamic performance.

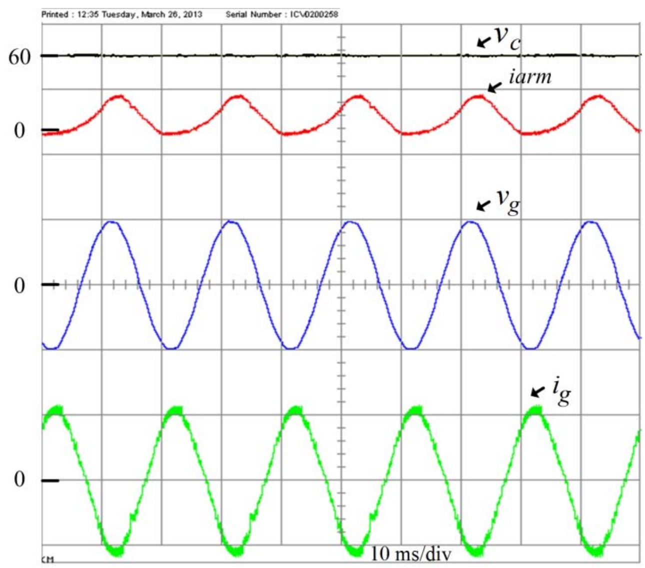


Fig. 3. 13 Steady-state operation as an inverter; v_c: SM capacitor voltage (50V/div); i_{arm}: arm current (6A/div); v_g: grid voltage (105V/div); i_g: grid current (6A/div)

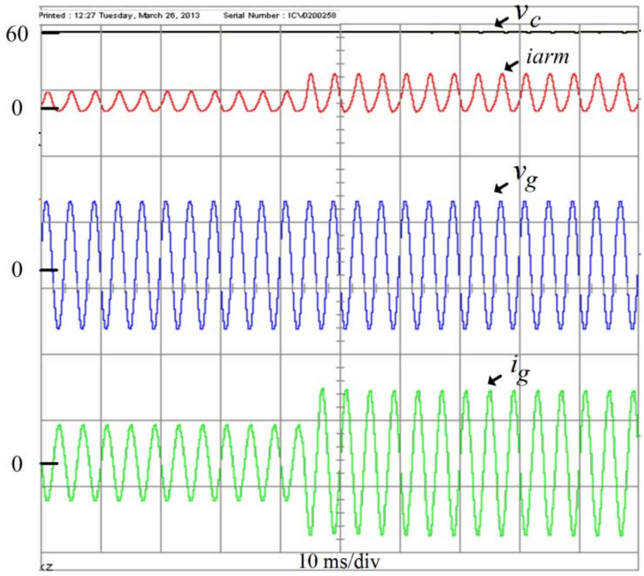


Fig. 3. 14 Dynamic operation as an inverter during active power step; v_c: SM capacitor voltage (50V/div); i_{arm}: arm current (6A/div); v_g: grid voltage (105V/div); i_g: grid current (6A/div)

To further illustrate the different operation and the impact of negative voltage state on system voltage and current, Figs. 3.15 and 3.16 show the voltage produced by the SMs in the upper arm during the transfer from traditional control strategy (i.e. FBSMs only generate two voltage states of positive and zero) to the proposed control strategy (i.e. the negative voltage state of FBSMs is adopted) in inverter mode. In stage I, the system is under traditional control strategy with each SM voltage being 40 V (for 120 V total DC voltage and three SMs per arm). The range of arm voltage is thus from 0 to 120 V, including three voltage levels shown in Fig. 3.16 (a). In stage II, the MMC stops and goes into a pre-charging period to increase the SM capacitor voltage to 60 V (the DC voltage remains at 120 V). In stage III, the MMC operates under the proposed control strategy with 1 out of 3 SMs in each arm permitting to produce -60 V (i.e., -V_c). The range of arm voltage is thus from -60 to 180 V (i.e., from –V_c to 3V_c), consisting of four voltage levels shown in Fig. 3.16 (b). As shown in the results, under the same DC-link voltage, the MMC based on the proposed strategy doubles the output peak-to-peak voltage from 120 V to 240 V with 50% increase of the capacitor voltage from 40 V to 60 V.

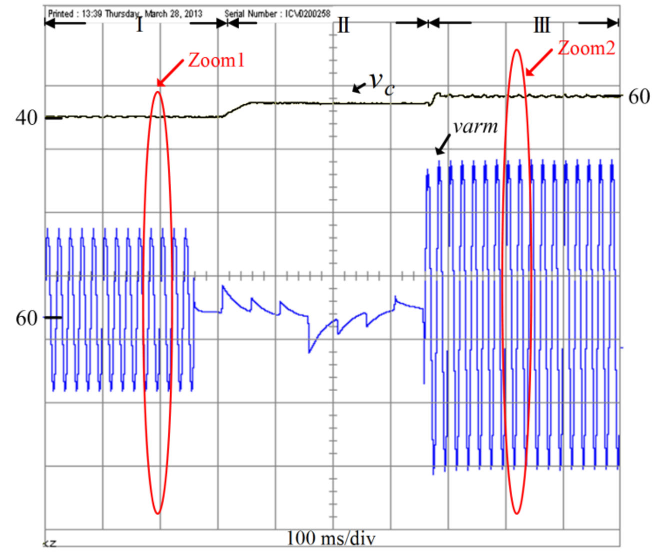
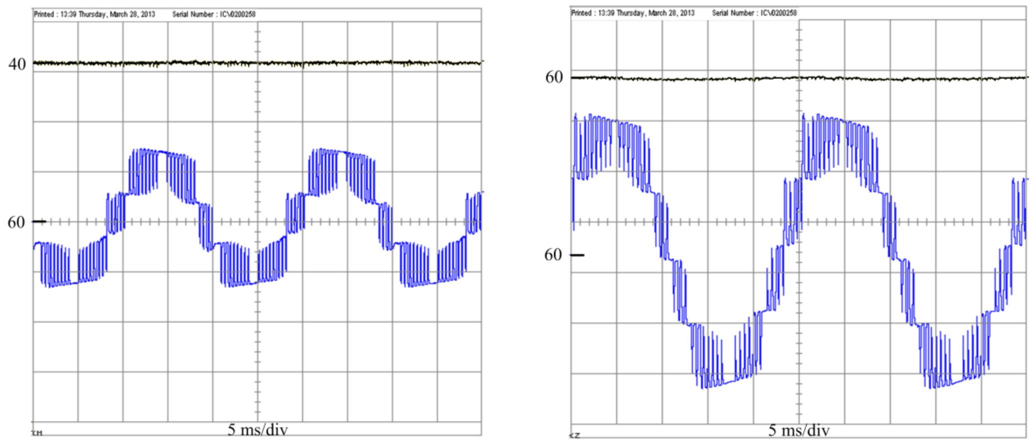


Fig. 3. 15 Test results during the switching of the control mode with the MMC operated as an inverter; v_c: SM capacitor voltage (50V/div); v_{arm}: upper arm voltage (50V/div);



(a) Zoom 1

(b) Zoom 2

Fig. 3. 16 Detailed SM and arm voltages; v_c: SM capacitor voltage (50V/div); v_{arm}: upper arm voltage (50V/div)

3.6 Summary

In this chapter, the basic operation principle of the conventional HB-MMC and FB-MMC has been presented. Based on the general review in Chapter 2, commonly used methods for capacitor voltage balancing, common-mode current suppression etc. have been introduced and adopted for the basic control of the MMC. A boost FB-MMC adopting the negative voltage state in the FBSM is discussed, and a detailed analysis on the link between the capacitor voltage variation and the maximum modulation index is carried out since the use of negative voltage state of the FBSM changes the relationship among AC/DC voltages and currents in the MMC. Different MMC configurations including the conventional HB-MMC, FB-MMC, and boost FB-MMC are compared in terms of the numbers of semiconductor devices and power losses to show the potential advantages of the boost FB-MMC over the conventional HB-MMC and FB-MMC. The principle of DC fault blocking and different behaviours of HB-MMC and FB-MMC under DC fault conditions are also analyzed in depth. A three-phase MMC simulation model is developed using Matlab/Simulink and the simulation results show the performance of the boost FB-MMC. Finally, a single-phase MMC experimental platform and the relative experiment results are given to demonstrate the feasibility and validity of the operation performance for the boost FB-MMC.

Chapter 4

MMC operation under asymmetrical arm impedances conditions

This Chapter presents a detailed analysis and improved control strategy for Modular Multilevel Converters (MMC) under asymmetric arm impedances conditions. Unlike symmetric conditions, the fundamental AC current is not split equally between the upper and lower arms under asymmetric conditions, and the DC and double-frequency components in the common-mode current can also flow into the AC side. To solve these issues, a theoretical analysis of the effect of asymmetric conditions on MMC operation is carried out using equivalent circuits at different frequencies. Based on the developed mathematical model, three control targets are presented to eliminate the negative impacts caused by the asymmetric arm impedance. New control strategy is proposed to control the differential-mode current, common-mode current and power balance. The feasibility and validity of the proposed analysis and control strategy are demonstrated by simulation results from a three-phase MMC system and experimental results from a single-phase MMC system.

4.1 Modelling of the MMC with asymmetrical arm impedance

The circuit configuration of a three-phase MMC is shown in Fig. 4.1 where v_{pa}, v_{pb}, v_{pc} and v_{na}, v_{nb}, v_{nc} are the total voltages generated by all the SMs in the upper and lower arms, respectively. i_{pa}, i_{pb}, i_{pc} and i_{na}, i_{nb}, i_{nc} are the currents in the upper and lower arms, respectively. i_a, i_b, and i_c are the output AC phase currents.

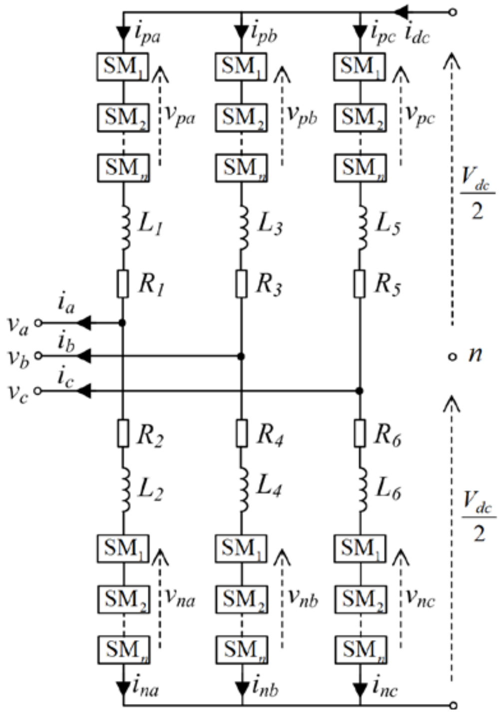


Fig. 4. 1 Basic structure of a three-phase MMC

Under normal operation, the arm current contains one differential-mode current i_{dmj} and one common-mode current i_{cmj} where the subscript j refers to the three-phase quantities of a, b, and c. During symmetrical conditions with six identical arm reactors, the differential-mode current flows to the three-phase AC side and the common-mode current flows within the upper and lower arms without affecting the AC side. Taking phase a as an example, the arm currents i_{pa} and i_{na} can therefore be expressed as

$$\begin{cases} i_{pa} = \dfrac{i_{dma}}{2} + i_{cma} \\ i_{na} = -\dfrac{i_{dma}}{2} + i_{cma} \end{cases} \tag{4.1}$$

where i_{dma} and i_{cma} can be expressed as [TU2011B]

$$\begin{cases} i_{dma} = I_m \sin(\omega t - \phi) \\ i_{cma} = \dfrac{I_{dc}}{3} + I_{cma2} \sin(2\omega t - \phi_{cma2}) \end{cases} \tag{4.2}$$

In (4.2), I_m is the peak AC side current, I_{cma2} is the peak of the double frequency component (higher order harmonic currents are neglected due to their small magnitudes) in the common-mode current, and I_{dc} is the DC side current.

Taking the neutral point n of the DC link as the voltage reference, the arm voltage can be expressed as

$$\begin{cases} v_{pa} = \frac{1}{2}V_{dc} - \left(Ri_{pa} + L\frac{di_{pa}}{dt} \right) - e_a \\ v_{na} = \frac{1}{2}V_{dc} - \left(Ri_{na} + L\frac{di_{na}}{dt} \right) + e_a \end{cases} \tag{4.3}$$

Combining (4.1) and (4.3) yields,

$$\begin{cases} 2\times\left(Ri_{cma} + L\frac{di_{cma}}{dt} \right) = V_{dc} - \left(v_{pa} + v_{na}\right) = u_{cma} \\ \frac{1}{2}\left(Ri_{dma} + L\frac{di_{dma}}{dt} \right) = \frac{1}{2}\left(v_{na} - v_{pa}\right) - e_a = u_a - e_a \end{cases} \tag{4.4}$$

where u_a is the equivalent phase voltage in phase a and can be used to regulate the differential-mode current. u_{cma} is the voltage difference between the DC voltage and the total leg voltage formed by the upper and lower arms which can be used to control the common-mode current.

Based on (4.4), the upper and lower arm voltages are:

$$\begin{cases} v_{pa} = \frac{V_{dc}}{2} - u_a - \frac{u_{cma}}{2} \\ v_{na} = \frac{V_{dc}}{2} + u_a - \frac{u_{cma}}{2} \end{cases} \tag{4.5}$$

Thus, the instantaneous power flowing into the upper and lower arms can be expressed as the product of the arm voltage in (4.5) and the arm current in (4.1) as

$$\begin{cases} p_{pa} = v_{pa}i_{pa} = \left(\frac{1}{4}V_{dc}i_{dma} - \frac{1}{4}u_{cma}i_{dma} - u_a i_{cma} \right) + \frac{1}{2}\left(V_{dc}i_{cma} - u_{cma}i_{cma} - u_a i_{dma}\right) \\ p_{na} = v_{na}i_{na} = -\left(\frac{1}{4}V_{dc}i_{dma} - \frac{1}{4}u_{cma}i_{dma} - u_a i_{cma} \right) + \frac{1}{2}\left(V_{dc}i_{cma} - u_{cma}i_{cma} - u_a i_{dma}\right) \end{cases} \tag{4.6}$$

Fig. 4.2 shows the equivalent circuit of an asymmetrical MMC, since in reality impedances in all the arm reactors will not be equal. $\tilde{v}_{pa}$, $\tilde{v}_{pb}$, $\tilde{v}_{pc}$ and $\tilde{v}_{na}$, $\tilde{v}_{nb}$, $\tilde{v}_{nc}$ represent the AC components in the generated arm voltages which mainly contain fundamental and second order harmonic components whereas $\bar{v}_{pa}$, $\bar{v}_{pb}$, $\bar{v}_{pc}$ and $\bar{v}_{na}$, $\bar{v}_{nb}$, $\bar{v}_{nc}$ denote the DC offsets in the arm voltages.

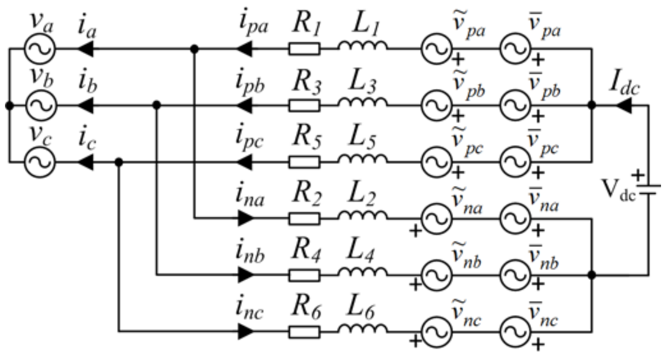


Fig. 4. 2 Equivalent circuit of an asymmetrical MMC

The linear circuit shown in Fig. 4.2 can be divided into three sub-circuits using the superposition principle, giving different frequency voltage sources, i.e. DC, fundamental frequency AC and double frequency AC sources.

4.1.1 Fundamental frequency sub-circuit

For conventional MMC control [SON2013], the upper and lower fundamental frequency voltage sources within each phase are identical but with opposite signs. Fig. 4.3 presents the MMC equivalent circuit for the fundamental frequency quantities. $\tilde{v}_{a1}$, $\tilde{v}_{b1}$, and $\tilde{v}_{c1}$ denote the fundamental frequency voltage source in phase *a*, *b*, and *c*, respectively. Note the opposite directions for the voltages in the upper and lower arms in Fig. 4.3.

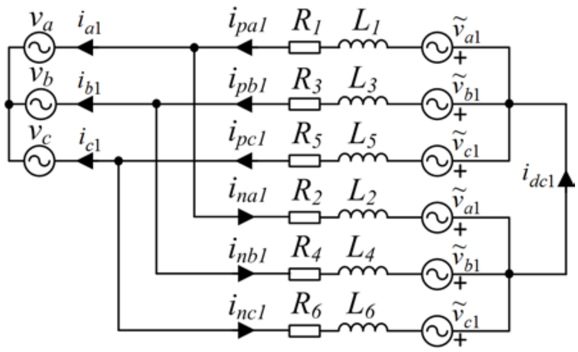
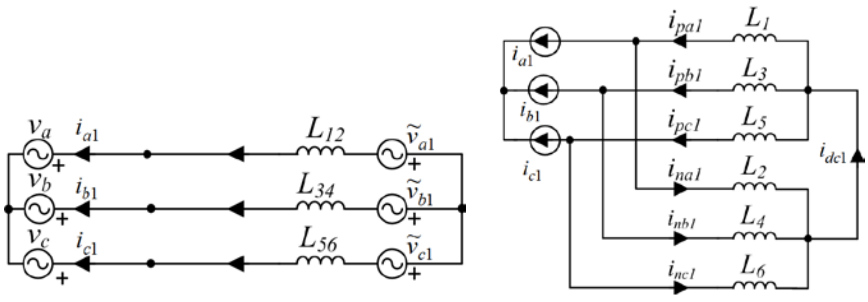


Fig. 4. 3 Sub-circuit illustrating the fundamental frequency quantities

The circuit in Fig. 4.3 can be analysed in two steps. The first step uses Thevenin's equivalent circuit to calculate the AC output current i_{a1}, i_{b1}, and i_{c1}. The simplified circuit is shown in Fig. 4.4 (a) where the arm resistances are neglected for ease of calculation, and

$$
\begin{aligned}
L_{12} &= \frac{L_1 L_2}{L_1 + L_2} \\
L_{34} &= \frac{L_3 L_4}{L_3 + L_4} \\
L_{56} &= \frac{L_5 L_6}{L_5 + L_6}
\end{aligned}
\tag{4.7}
$$

The circuit in Fig. 4.4 (a) can be analyzed by considering the three-phase unbalanced inductances which results in unbalanced line currents i_{a1}, i_{b1}, and i_{c1} [HU2008].



(a) (b)

Fig. 4. 4 Equivalent circuit at fundamental frequency for: (a) calculating AC current and (b) calculating arm and DC current.

The second step then considers the output AC currents as three-phase current sources as shown in Fig. 4.4 (b). The steady-state arm current and the current flow through the DC side can then be calculated as

$$
\begin{aligned}
& i_{pa1} = \frac{L_2}{L_1 + L_2} i_{a1} \qquad i_{na1} = \frac{-L_1}{L_1 + L_2} i_{a1} \\
& i_{pb1} = \frac{L_4}{L_3 + L_4} i_{b1} \qquad i_{nb1} = \frac{-L_3}{L_3 + L_4} i_{b1} \\
& i_{pc1} = \frac{L_6}{L_5 + L_6} i_{c1} \qquad i_{nc1} = \frac{-L_5}{L_5 + L_6} i_{c1} \\
& i_{dc1} = i_{ap1} + i_{bp1} + i_{cp1} \neq 0
\end{aligned}
\tag{4.8}
$$

Thus, asymmetrical inductances in the two arms in each phase result in different fundamental arm currents, i.e. unequal current sharing between the upper and lower arms. Additionally, there can also be fundamental current through the DC side which causes extra DC voltage and current ripples.

4.1.2 Double frequency sub-circuit

Based on the analysis in [SON2013], the double frequency components in the common-mode current are generated by the common-mode voltage ripples in the upper and lower arms. Fig. 4.5 shows the equivalent circuit for the double frequency quantities, where $\tilde{v}_{a2}, \tilde{v}_{b2}, \tilde{v}_{c2}$ denote the double frequency voltage sources. The circuit shown can be analyzed using the same approach as for the fundamental components shown in previous sections. When the arm impedances are symmetrical, the upper and lower arm currents for each phase are identical, e.g. $i_{pa2} = i_{na2}$ for phase a. This leads to $i_{a2} = 0$ which means the second order harmonic current only appears as common mode in the arms without affecting the AC output current. Under such a condition, the sum of the three-phase double frequency common-mode currents is also zero indicating such current components do not appear on the DC side, i.e. $i_{dc2} = 0$. Under asymmetrical conditions, however, the double frequency common-mode currents flowing through the upper and lower arms in each phase are not equal and their difference will flow to the AC side ($i_{a2} \neq 0$, $i_{b2} \neq 0$, $i_{c2} \neq 0$). Meanwhile, the sum of the three-phase double frequency current is not zero, and will appear on the DC side, i.e. $i_{dc2} \neq 0$.

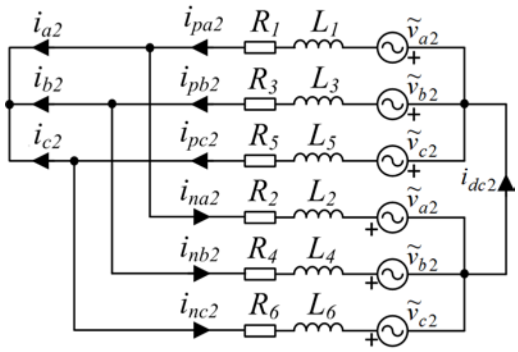


Fig. 4. 5 Sub-circuit illustrating the double frequency quantities

4.1.3 DC sub-circuit

Adopting the conventional control strategy, the DC offsets in the upper and lower arms are equal and have the same orientation. Fig. 4.6 shows the equivalent circuit for the DC quantities where $\bar{V}_a = \bar{V}_b = \bar{V}_c = V_{dc}/2$. Under symmetrical conditions, the upper arm currents $\bar{i}_{pa}$, $\bar{i}_{pb}$, and $\bar{i}_{pc}$ are identical to the lower arm currents $\bar{i}_{na}$, $\bar{i}_{nb}$, $\bar{i}_{nc}$, and all equal $\frac{1}{3}I_{dc}$. For system with different arm resistances, the DC currents in the upper and lower arms also become unequal and consequently, a DC current component appears on the AC side, i.e. $\bar{i}_a \neq 0$ taking phase *a* as an example.

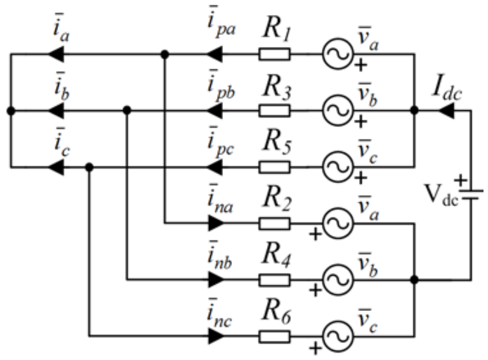


Fig. 4. 6 Sub-circuit illustrating the DC quantities

4.1.4 Power flow analysis

According to the previous analysis, under asymmetrical conditions, the differential-mode and the common-mode currents in phase *a* can be expressed as

$$\begin{cases} i_{dma} = I_{dma0} + I_m \sin(\omega t - \varphi) + I_{dma2} \sin(2\omega t - \varphi_{dma2}) \\ i_{cma} = I_{cma0} + I_{cma1} \sin(\omega t - \varphi_{cma1}) + I_{cma2} \sin(2\omega t - \varphi_{cma2}) \end{cases} \tag{4.9}$$

Combining the three sub-circuits, the arm voltages in leg *a* can be expressed as

$$\begin{cases} v_{pa} = \tilde{v}_{a1} + \tilde{v}_{a2} + \bar{v}_a \\ v_{na} = -\tilde{v}_{a1} + \tilde{v}_{a2} + \bar{v}_a \end{cases} \tag{4.10}$$

Rewriting (4.6), the instantaneous power in the upper and lower arms is

$$\begin{aligned} p_{pa} &= \frac{1}{2} i_{dma} \tilde{v}_{a1} + i_{cma}(\tilde{v}_{a2} + \bar{v}_a) + \frac{1}{2} i_{dma}(\tilde{v}_{a2} + \bar{v}_a) + \tilde{v}_{a1} i_{cma} \\ p_{na} &= \frac{1}{2} i_{dma} \tilde{v}_{a1} + i_{cma}(\tilde{v}_{a2} + \bar{v}_a) - \frac{1}{2} i_{dma}(\tilde{v}_{a2} + \bar{v}_a) - \tilde{v}_{a1} i_{cma} \end{aligned} \tag{4.11}$$

Thus, the difference in energy stored between the upper and lower arms can be calculated as

$$\begin{aligned} e_{pn} &= \int (p_{pa} - p_{na}) dt = \int (i_{dma}(\tilde{v}_{a2} + \bar{v}_a) + 2\tilde{v}_{a1} i_{cma}) dt \\ &= \int \begin{pmatrix} I_{dma0} \bar{v}_a + 2I_{cma1} \sin(\omega t - \varphi_{cma1}) \tilde{v}_{a1} + I_{dma2} \sin(2\omega t - \varphi_{dma2}) \tilde{v}_{a2} \\ + (I_m \sin(\omega t - \varphi) + I_{dma2} \sin(2\omega t - \varphi_{dma2})) \bar{v}_a \\ + (2I_{cma0} + 2I_{cma1} \sin(\omega t - \varphi_{cma1}) + 2I_{cma2} \sin(2\omega t - \varphi_{cma2})) \tilde{v}_{a1} \\ + (I_{dma0} + I_m \sin(\omega t - \varphi) + I_{dma2} \sin(2\omega t - \varphi_{dma2})) \tilde{v}_{a2} \end{pmatrix} dt \end{aligned} \tag{4.12}$$

The energy difference between the upper and lower arms is not zero in one complete period under the following two conditions:

- The differential-mode current (i.e. the output AC current) has a DC component ($I_{dma0} \neq 0$) or a double frequency component ($I_{dma2} \neq 0$);
- The common-mode current includes a fundamental frequency component ($I_{cma1} \neq 0$).

From this analysis, it can be concluded that under asymmetrical impedance conditions, the following potential issues exist which could significantly affect MMC system operation:

- Unequal fundamental current distribution in the upper and lower arms, and the existence of fundamental current ripple on the DC side;
- Existence of second order harmonic current on the output AC and DC sides;
- Unequal energy in the upper and lower arms which results in SM capacitor voltage divergence between the upper and lower arms.

Therefore, to maintain stable operation of the MMC under asymmetrical conditions, three control targets need to be achieved: (1) ensure the AC fundamental frequency current is split equally between the upper and lower arms; (2) eliminate the second order harmonic current in the differential-mode (AC output) current; and (3) regulate the DC common-mode current to maintain balanced power between the upper and lower arms.

4.2 Improved control strategy for asymmetric MMC

According to the previous analysis, to ensure stable MMC operation under asymmetrical conditions, a control strategy including the following three controllers is proposed.

4.2.1 Output AC (differential-mode) current controller

The output AC (differential-mode) current controller is implemented similar to conventional VSC control based in the synchronous *dq* frame [TU2011B]. The controller generates the required arm voltage for each phase, e.g. v^*_{pa} and v^*_{na} for phase *a*. As this has been documented, no further details are given here.

4.2.2 Common-mode current controller

From previous analysis, elimination of the fundamental frequency common-mode current ensures equal distribution of the AC output current between the upper and the lower arms. In addition, the second order harmonic current problem on the AC and DC sides can be resolved if the second order common-mode harmonic current is completely eliminated. Thus, the purpose of this controller is to eliminate both the common-mode fundamental (which is unique to asymmetrical conditions) and double-frequency current components.

According to Fig. 4.2 and (4.4), the mathematical equation for the common-mode current is

$$\begin{cases} \left((R_1 + R_2) + (L_1 + L_2)\dfrac{d}{dt}\right) i_{cma} = -\left(\tilde{v}_{pa} + \tilde{v}_{na}\right) \\ \left((R_3 + R_4) + (L_3 + L_4)\dfrac{d}{dt}\right) i_{cmb} = -\left(\tilde{v}_{pb} + \tilde{v}_{nb}\right) \\ \left((R_5 + R_6) + (L_5 + L_6)\dfrac{d}{dt}\right) i_{cmc} = -\left(\tilde{v}_{pc} + \tilde{v}_{nc}\right) \end{cases} \tag{4.13}$$

Controlling the AC components in the arm voltages can regulate the common-mode current. To eliminate the main components in the common-mode current under asymmetrical conditions, a PR (proportional and resonant) controller with two resonant frequencies at ω_0 and $2\omega_0$ (ω_0 is the fundamental frequency) is adopted in each leg, and the transfer function of the PR controller is [HU2009]

$$G(s) = K_p + \frac{2K_{r1}s}{s^2 + (\omega_0)^2} + \frac{2K_{r2}s}{s^2 + (2\omega_0)^2} \tag{4.14}$$

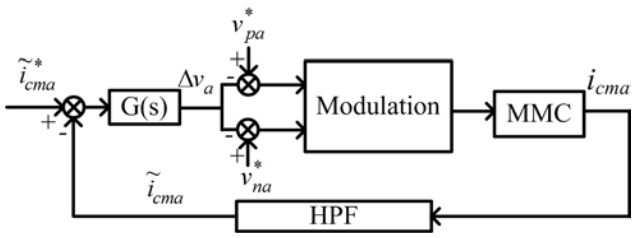


Fig. 4. 7 Control structure of the common-mode current for phase '*a*'

The control structure for phase *a* is shown in Fig. 4.7, where the high pass filter (HPF) removes the DC component and extracts the AC components $\tilde{i}_{cma}$ from the common mode current i_{cma}. The cut-off frequency of the HPF can be set at a low frequency, e.g. 2 Hz, due to the fact that dynamic response is not the main concern for this controller. $\tilde{i}_{cma}^*$ is the reference value for the AC common mode current which is set to zero for their complete elimination. The output from the PR controller,

Δv_a, is added/subtracted to/from the normal upper and lower arm voltage references generated by the AC (differential mode) current controller.

4.2.3 Power balance controller

With a common-mode current controller, the fundamental frequency and double frequency common-mode currents can be eliminated by adding Δv_{a1} (for fundamental frequency) and Δv_{a2} (for double frequency) to the upper and lower arm voltages. Based on (4.9), the arm voltages in the proposed control strategy can be expressed as

$$\begin{cases} v_{pa} = \tilde{v}_{a1} + \Delta v_{a1} + \tilde{v}_{a2} + \Delta v_{a2} + \bar{v}_{pa} \\ v_{na} = -\tilde{v}_{a1} + \Delta v_{a1} + \tilde{v}_{a2} + \Delta v_{a2} + \bar{v}_{na} \end{cases} \tag{4.15}$$

where Δv_{a1} and Δv_{a2} denote the additional voltage components generated by the common-mode current controller. $\bar{v}_{pa}$ and $\bar{v}_{na}$ denote the DC offsets in the upper and lower arms respectively, which might be slightly different under asymmetrical conditions due to different arm resistances.

Rewriting (4.6), the instantaneous powers in the upper and lower arms are

$$\begin{cases} p_{pa} = \left(\tfrac{1}{2} i_{dma}\tilde{v}_{a1} + i_{cma}\left(\Delta v_{a1} + \tilde{v}_{a2} + \Delta v_{a2}\right)\right) \\ \qquad + \left(\tfrac{1}{2} i_{dma}\left(\Delta v_{a1} + \tilde{v}_{a2} + \Delta v_{a2}\right) + i_{cma}\tilde{v}_{a1}\right) + \left(\tfrac{1}{2} i_{dma} + i_{cma}\right)\bar{v}_{ap} \\ p_{na} = \left(\tfrac{1}{2} i_{dma}\tilde{v}_{a1} + i_{cma}\left(\Delta v_{a1} + \tilde{v}_{a2} + \Delta v_{a2}\right)\right) \\ \qquad - \left(\tfrac{1}{2} i_{dma}\left(\Delta v_{a1} + \tilde{v}_{a2} + \Delta v_{a2}\right) + i_{cma}\tilde{v}_{a1}\right) + \left(-\tfrac{1}{2} i_{dma} + i_{cma}\right)\bar{v}_{na} \end{cases} \tag{4.16}$$

Thus, the difference in stored energy between the upper and lower arms is

$$e_{pn} = \int \left(i_{dma}\Delta v_{a1} + i_{cma}\left(\bar{v}_{pa} - \bar{v}_{na}\right) + 2 i_{cma}\tilde{v}_{a1} + i_{dma}\left(\tilde{v}_{a2} + \Delta v_{a2}\right) + \frac{1}{2} i_{dma}\left(\bar{v}_{pa} + \bar{v}_{na}\right)\right) dt \tag{4.17}$$

Eq. (4.17) indicates that energy difference e_{pn} exists between the upper and lower arms in one complete period. Consequently, the total energy stored in the upper arm SM capacitors and lower arm capacitors can be different which results in the divergence of their voltages. Thus, to ensure balanced SM capacitor voltages in the upper and lower arms, a power balance controller is required in each phase.

Detailed analysis of (4.17) reveals that there exist two power balance methods. The second component in (4.17) indicates that the energy difference can be controlled by slightly changing $(\bar{v}_{pa} - \bar{v}_{na})$, i.e. the DC offsets of the upper and lower arm voltages, since the common-mode current i_{cma} now only contains the DC current. The schematic diagram using this control principle is shown in Fig. 4.8 for phase a. As shown, the difference between the total upper arm capacitor voltage (i.e. $\sum_{i=1}^{n} v_{pci}$ where v_{pci} is the capacitor voltage of the i^{th} SM in the upper arm, and n is the total number of SMs in an arm) and the lower arm total capacitor voltage (i.e. $\sum_{i=1}^{n} v_{nci}$ where v_{nci} is the capacitor voltage of the i^{th} SM in the lower arm) is passed through a notch filter tuned at fundamental frequency ω_0 to remove the fundamental frequency voltage ripple and extract the DC voltage unbalance $\Delta\bar{v}_{dcpn}$. i_{cma0} is the DC component of the common mode current and equals to $I_{dc}/3$ under normal steady state condition. Their product is fed to a PI regulator whose reference input is zero to produce a small DC offset which is added to the upper and lower arm voltages with opposing polarities. The response of the PI regulator can be tuned at a low frequency due to the slow dynamics of the voltage divergence. The limitation of this method is that the controller becomes ineffective when the DC component in the common-mode current is zero, i.e. when the converter is not transmitting real power. To solve this issue, a supplementary method derived from the third component in (4.17) is adopted. If a small common-mode current at the fundamental frequency, which has the same phase angle as the generated AC arm voltage, is added, the energy difference can be regulated. Fig. 4.9 shows the structure of the supplementary power balance method for phase a. As shown, ωt is the phase angle of the generated arm AC voltage and thus m_{sa} is in phase with the fundamental frequency arm AC voltage with a magnitude of 1. Δi_{cma} is the injected common-mode current which is added to the normal common-mode current reference of zero to feed to the common-mode current controller shown in Fig. 4.7.

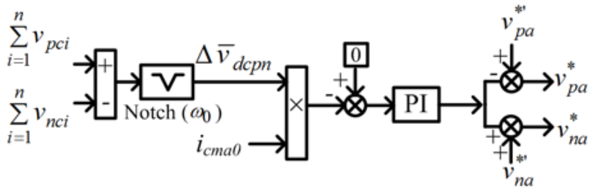


Fig. 4. 8 Structure of the power balance controller for phase *a* using DC components

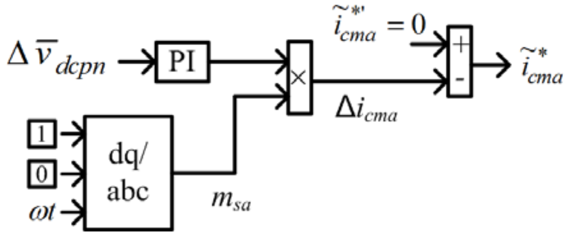


Fig. 4. 9 Structure of the power balance controller for phase *a* using AC components

The complete MMC control structure is shown in Fig. 4.10, where the superscript "*" denotes the reference values, and v_{pj}^*, v_{nj}^*, i_{cmj}, $\tilde{i}_{cmj}$, i_{cmj0} denote the required upper and lower arm voltages, common-mode current, and the AC and DC components in common-mode current in phase a, b, c ($j = a, b, c$), respectively. The voltage reference is generated by three controllers, of which the differential-mode current controller regulates the active and reactive powers, the common-mode current controller suppresses the 50 Hz and 100 Hz circulating currents, and the power balance controller ensures the total voltages across the upper and the lower arm capacitors are equal.

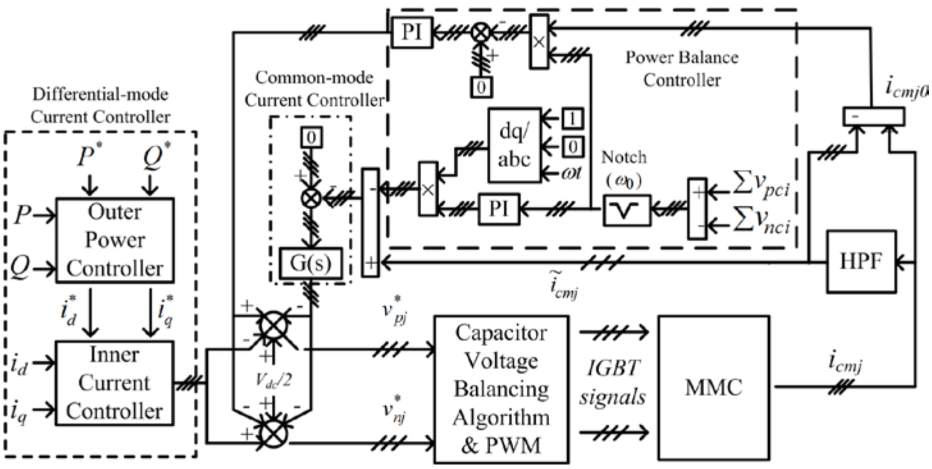


Fig. 4. 10 Overall control structure for an asymmetrical MMC

The three additional voltage components generated by the proposed controller, i.e. the DC, fundamental and double frequency voltages, are added to the upper and lower arm voltages to compensate the unbalanced voltage drop across the asymmetrical arm reactors, the double frequency SM capacitor voltage ripple, and the capacitor voltage imbalance between the upper and lower arms. Consequently the AC voltage seen at the converter terminal will be free from any voltage unbalance and harmonics to ensure no DC and double frequency current in the AC output. Therefore, the injected components have no adverse effect on the MMC AC output.

4.2.4 Consideration of compensation limits for the proposed control strategy

The proposed controller injects additional arm voltages but the maximum arm voltage that can be generated is limited by the operating point of the converter. Thus the relationship between the converter operating point (modulation index, DC voltage and AC current) and the unbalance ratio of the arm impedance is considered.

As the control scheme ensures the arm current only contains fundamental and DC components, only the fundamental voltage drop across the asymmetrical arm reactor is considered. According to previous analysis, in order to share the fundamental AC current equally, the voltages across the upper and lower arms including the voltage generated by the SMs and the voltage drop across the arm reactors must have identical amplitude and 180º phase shift. The additional injected arm voltage generated by SMs in each arm therefore needs to compensate the voltage difference caused by the different upper and lower arm impedances. An extreme condition is considered here, in which one arm (e.g. upper arm) has the minimum arm impedance L_{min} whereas the other arm in the same phase (e.g. lower arm) has the maximum arm impedance L_{max}. As illustrated in Fig. 4.3, the fundamental frequency quantities can be expressed as

$$\tilde{v}_1 + \Delta\tilde{v}_1 + \frac{I_{ac}}{2}\sin(\omega t - \varphi) \times j\omega L_{\min} = \tilde{v}_1 - \Delta\tilde{v}_1 + \frac{I_{ac}}{2}\sin(\omega t - \varphi) \times j\omega L_{\max} \qquad (4.20)$$

where $\tilde{v}_1$ is the normal voltage generated by the SMs, $\Delta\tilde{v}_1$ is the additional injected arm voltage, and I_{ac} is the amplitude of AC current.

The unbalance ratio of k and the additional injected arm voltage $\Delta\tilde{v}_1$ are defined as

$$k = \frac{L_{\max} - L_{\min}}{L}, \quad \Delta\tilde{v}_1 = \Delta m \times \frac{V_{dc}}{2}\sin(\omega t + \theta_1) \tag{4.21}$$

where Δm and θ_1 are the modulation index and phase angle of the additional voltage component, and L is the average arm inductance.

Substituting (4.21) into (4.20) yields

$$\Delta m = \frac{\omega L \times I_{ac}}{2V_{dc}} k, \quad \theta_1 = \frac{\pi}{2} - \varphi \tag{4.22}$$

Thus in order to perform the compensation, the converter must have the extra modulation index margin Δm.

4.3 Simulation results

To verify the proposed control strategy, a three-phase MMC was simulated using Matlab/Simulink. Fig. 4.11 shows the simulation system where the MMC employs the configuration in Fig. 4.1 with slightly different impedances in each arm. The main circuit parameters are listed in Table 4-1.

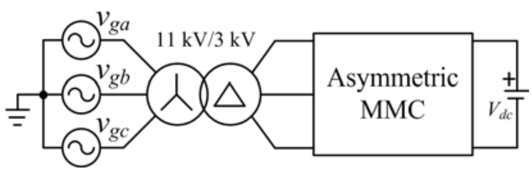


Fig. 4. 11 Structure of the simulation system

Table 4- 1 Simulated MMC system parameters

Item	Values
MMC rated power	2.25 MW

DCDC voltage	6 kV
Source voltage (L-L rms)/frequency	11 kV / 50 Hz
Transformer ratio	11 kV/3 kV
Rated impedance	6.93 Ω
Transformer leakage impendence	0.002 + j0.2 p.u.
Number of SMs per arm	4
DC voltage per SM	1.5 kV
SM capacitor	2200 μF
$R_1 + j\omega L_1$	0.0036 + j0.09 p.u.
$R_2 + j\omega L_2$	0.0044 + j0.11 p.u.
$R_3 + j\omega L_3$	0.0041 + j0.105 p.u.
$R_4 + j\omega L_4$	0.0036 + j0.09 p.u.
$R_5 + j\omega L_5$	0.0044 + j0.11p.u.
$R_6 + j\omega L_6$	0.0040 + j0.10 p.u.
MMC carrier frequency	4.0 kHz

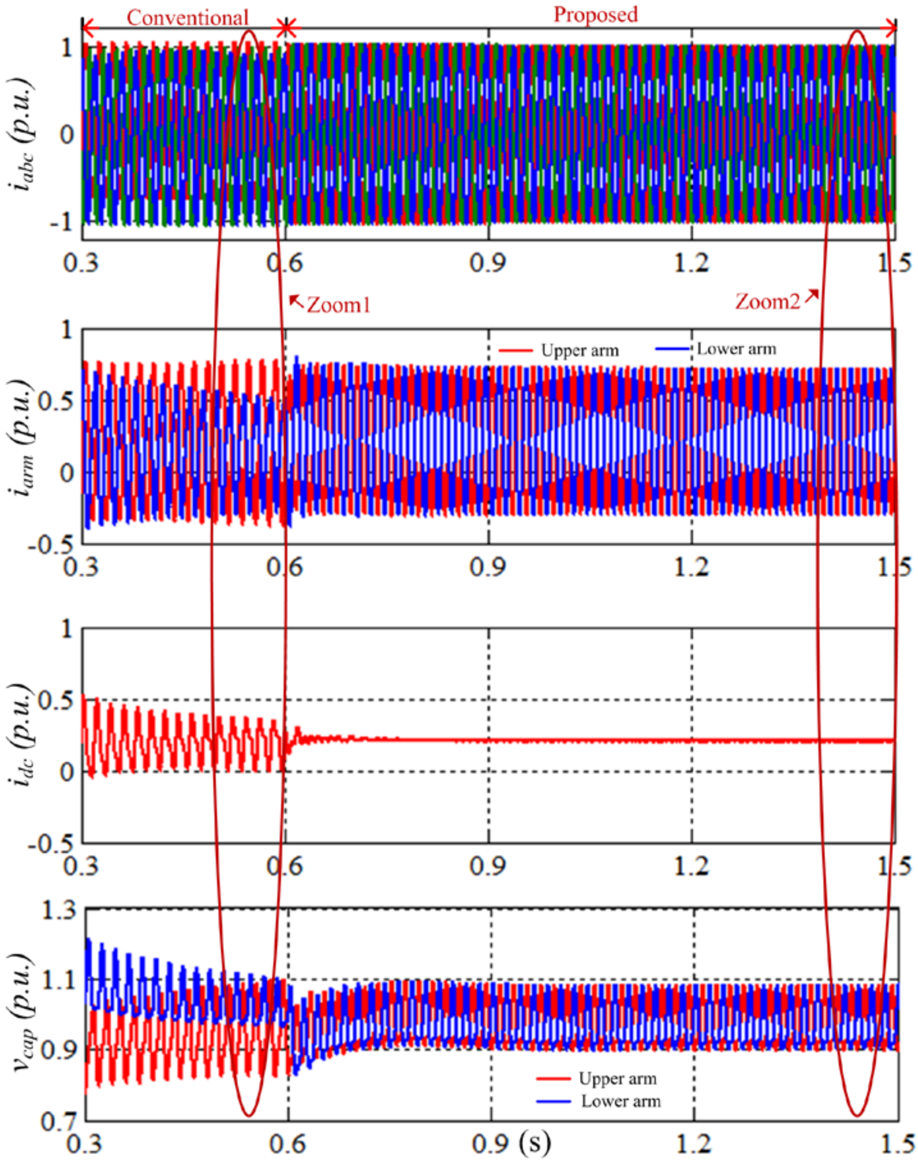
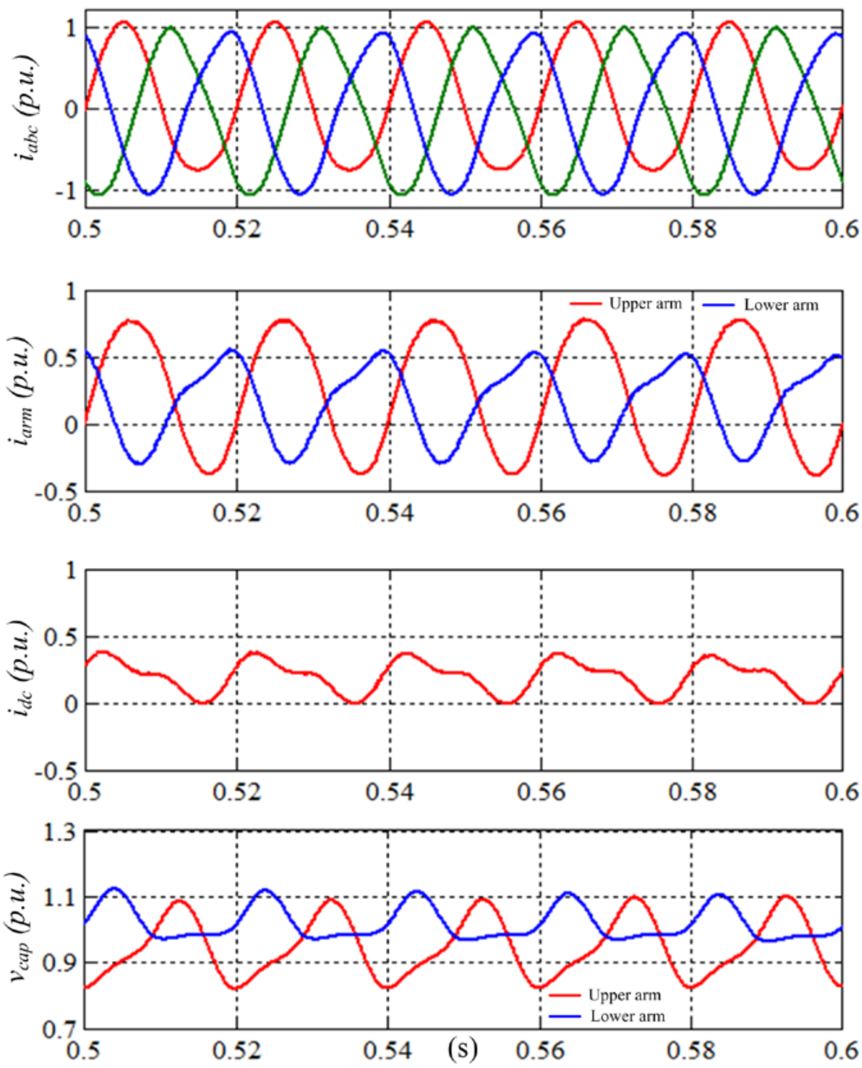
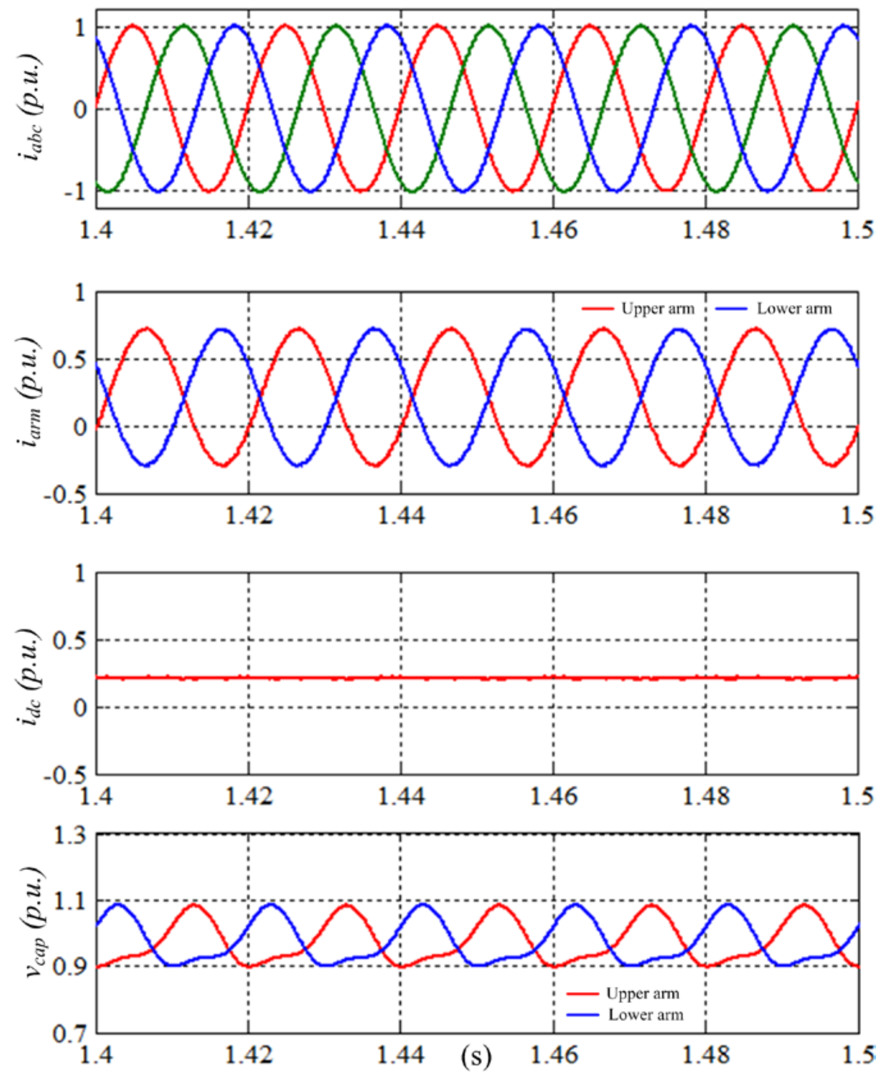


Fig. 4. 12 Simulation results for the asymmetrical MMC with approximately 10% arm impedance unbalance ratio; i_{abc}: input AC current; i_{arm}: phase a upper and lower arm current; i_{dc}: DC link current; v_{cap}: sum of the capacitor voltages in upper and lower arms.



(a) Zoom 1: 05.-0.6s



(b) Zoom 2: 1.4-1.5s

Fig. 4. 13 Enlarged view of the simulation waveforms for the asymmetrical MMC with 10% arm impedance mismatch.

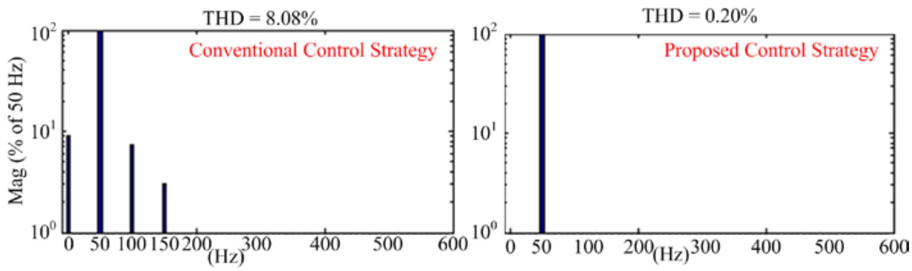
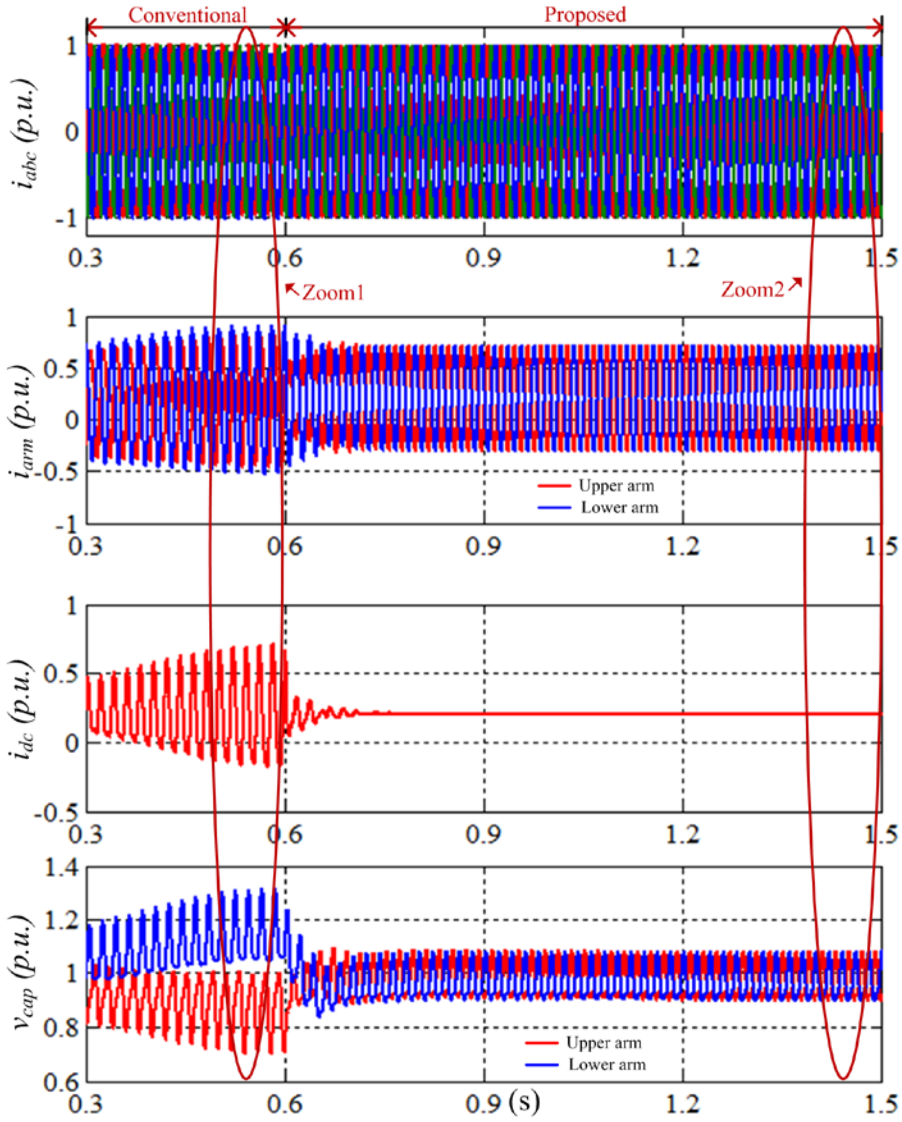


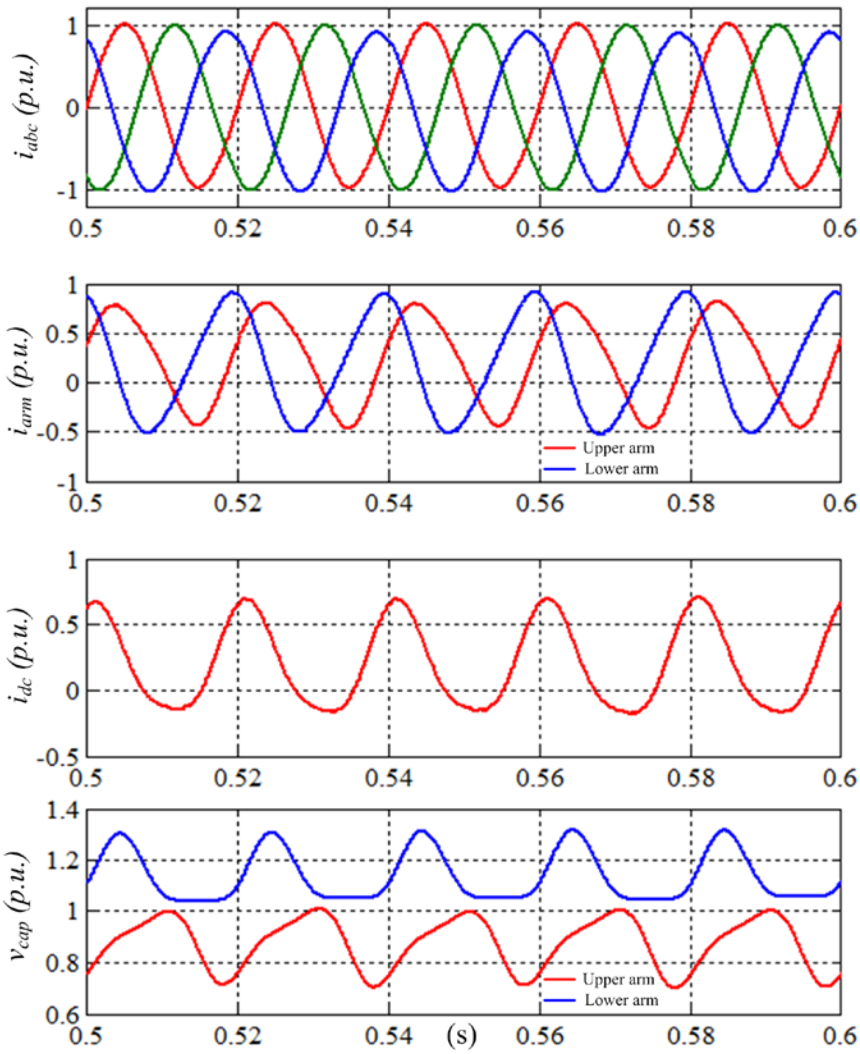
Fig. 4. 14 Comparison of harmonic spectra and THD of the AC side current with a small arm impedance unbalance ratio of 10%

Fig. 4.12 shows the simulation results for the asymmetrical MMC with approximately 10% unbalance ratio between the arm impedances. Before 0.6 s, the system adopts the conventional control strategy, i.e. only with differential-mode current control, and the proposed control method is enabled at 0.6 s. The enlarged waveforms in Zooms 1 and 2 are shown in Fig. 4.13 (a) and (b) respectively. Fig. 4.14 compares the harmonic spectra and THD of the AC output current for the conventional and proposed methods. It can be observed from Figs. 4.12 and 4.13 (a) that under conventional control the AC side current is unbalanced with DC offsets and second order 100 Hz harmonics (see Fig. 4.14). This confirms the previous analysis that with asymmetric arm impedances the common-mode currents (both DC and 100 Hz) flow out to the AC side. As can also be seen from Figs. 4.12 and 4.13(a), the DC current contains large 50 Hz and 100 Hz ripples. The capacitor voltages in the upper and lower arm also diverge. Again, these observations are in good agreement with the previous analysis. After the adoption of the proposed control strategy at 0.6 s, the AC side current immediately becomes balanced and the DC and 100 Hz harmonics are largely eliminated, as shown in Figures. 4-12(b) and 4-13. In addition, the 50 Hz ripple in the DC current is also largely suppressed, as shown in Fig. 4.13(b). The capacitor voltages in the upper and lower arms are quickly rebalanced after enabling the balancing control. The improvement in the output AC current by the proposed method is also evident from the harmonic spectra and THD shown in Fig. 4.14. The simulation results clearly demonstrate the previous analysis and the effectiveness and validity of the proposed control strategy.

Further studies with a small arm impedance unbalance ratio of approximately 2% were carried out and the simulation results are shown in Fig. 4.15. It was found that even with such a relatively small unbalance in arm reactance, it still has similar issues as the previous case shown in Figs. 4.12 – 4.14, although the current harmonic amplitude is reduced. As is shown in Figure 4.15 (d), under such conditions, significant 2nd order harmonic current still exists in the AC output resulting in a current THD of 2.29%. This is reduced to 0.18% once the proposed control scheme is enabled indicating a significant improvement.

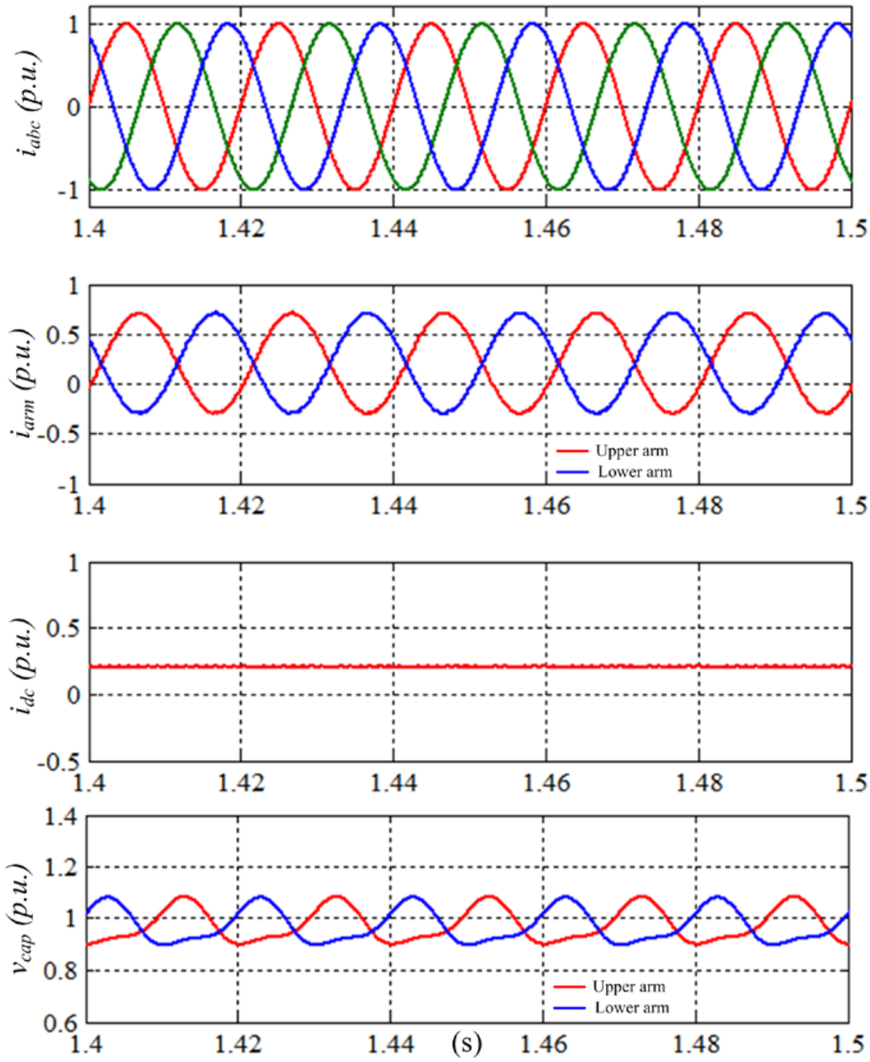


(a) Transferring from the conventional control strategy to the proposed control strategy.

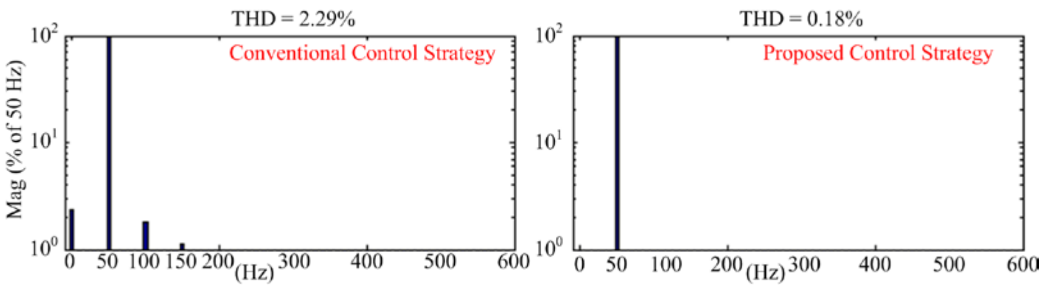


i_{abc} (p.u.)
i_{arm} (p.u.)
Upper arm
Lower arm
i_{dc} (p.u.)
v_{cap} (p.u.)
Upper arm
Lower arm
(s)

(b) Zoom 1



(c) Zoom 2



(d) Comparison of harmonic spectra and THD of AC side currents.

Fig. 4. 15 Simulation results for the asymmetrical MMC under the unbalance ratio of 2.0%

4.4 Experiment results

To test the presented analysis and the proposed control strategy, a prototype single-phase MMC schematically shown in Fig. 4.16 was developed. The control system is implemented using a TMS320F2812 DSP and the main circuit parameters are listed in Table 4-2. Two DC power sources are connected in series to form the DC neutral point. The unbalance ratio of the upper and lower arm inductances is approximately 6.4%.

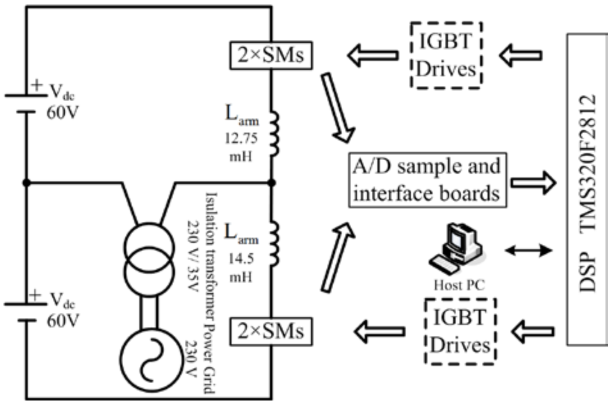


Fig. 4. 16 Schematic of the asymmetrical MMC experimental system

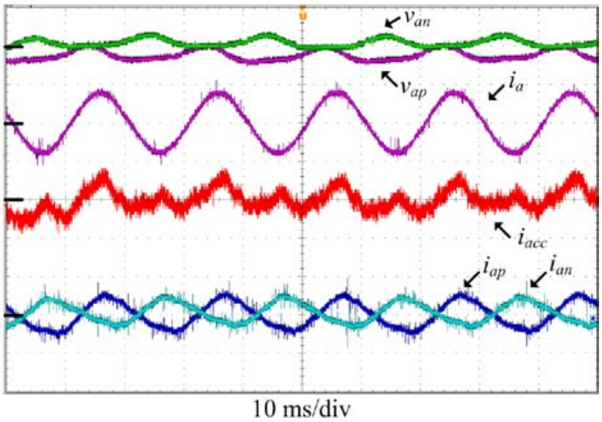
Table 4- 2 Parameters of the experimental MMC system

Item	Values
MMC rated power	150 W
DC voltage	120 V
AC voltage (peak)	50 V
Number of SMs per arm	2
DC voltage per SM	60 V
SM capacitor	940 μF

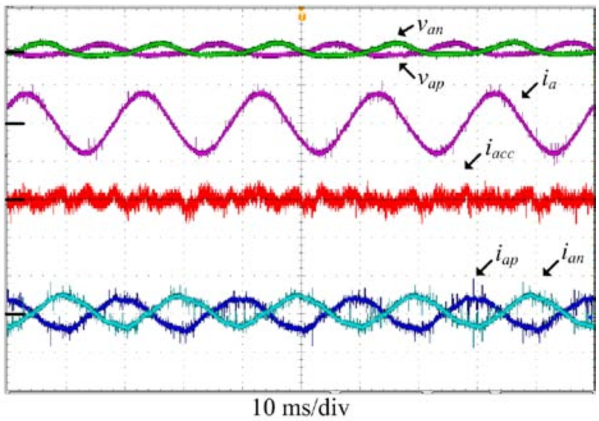
Upper arm inductance	12.75 mH
Lower arm inductance	14.50 mH
Transformer leakage inductance	16.8 mH
Transformer voltage ratio (rms.)	230 V / 35 V
MMC carrier frequency	4.0 kHz

Figs. 4.17 (a) and 4.17 (b) show the steady-state operation of the MMC under the conventional and proposed control strategies, respectively. As shown in Fig. 4.17 (a), the upper arm current is larger than the lower arm current (due to the smaller arm inductance in the upper arm), and the common-mode current includes large 50 Hz and 100 Hz ripple components. Fig. 4.17 (a) shows that the difference between the average capacitor voltages in the upper and lower arms is around 10V, representing 8.3% of the total DC voltage. By contrast, Fig. 4.17 (b) shows that once the proposed control strategy is adopted the common-mode current becomes mainly DC and the capacitor voltages in the upper and lower arms are balanced. Further analysis of the AC current i_a, arm current i_{ap} and i_{an}, and the common-mode current i_{acm} are carried out and the results are shown in Table 4-3. As is shown, the conventional control results in unequal sharing of the 50 Hz AC current between the upper and lower arms and the common-mode current contains significant 50 Hz and 100 Hz components. In addition, the output AC current also contains DC and 100 Hz harmonics. By contrast, the proposed method significantly reduces the 50 Hz and 100 Hz components in the common-mode current and results in equal current sharing in the upper and lower arms. The DC and 100 Hz components in the output AC current are also reduced from 0.5% and 1.8% to 0.05% and 0.5% respectively.

Fig. 4.18 shows the MMC dynamic operation when the system switches from the conventional control strategy (Stage I) to the proposed control strategy (Stage II). As is shown, the proposed control strategy achieves the three objectives quickly and smoothly.



(a) With conventional control strategy



(b) With the proposed control strategy

Fig. 4. 17 Steady-state operation as a grid-connected inverter; v_{ap}: upper arm capacitor voltage (20V/div); v_{an}: lower arm capacitor voltage (20V/div); i_a: AC side current (5A/div); i_{acc}: common-mode current (2.5A/div); i_{ap}: upper arm current (5A/div); i_{an}: lower arm current (5A/div).

Table 4- 3 Current components for the conventional and proposed methods

	i_{ap}	i_{an}	i_{acm}		i_a	
			50Hz	**100Hz**	**DC**	**100Hz**
Conventional	54.6%	45.4%	5.5%	7.9%	0.5%	1.8%
Proposed	50.0%	50.0%	1.0%	0.5%	0.05%	0.5%

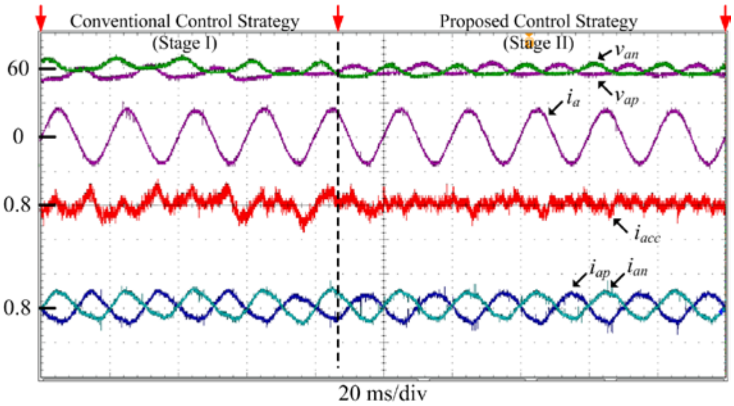


Fig. 4. 18 Dynamic response when the system switches from conventional control to the proposed method, v_{ap}: upper arm capacitor voltage (20V/div); v_{an}: lower arm capacitor voltage (20V/div); i_a: AC side current (5A/div); i_{acc}: common-mode current (2.5A/div); i_{ap}: upper arm current (5A/div); i_{an}: lower arm current (5A/div).

4.5 Summary

This chapter proposes an MMC control strategy for asymmetrical arm impedance conditions. An equivalent circuit of the asymmetrical MMC is presented, and detailed analysis of the impact of asymmetrical conditions on the differential-mode current, the common-mode current and capacitor voltages, was performed. Based on the analysis, three control targets were proposed to improve asymmetrical MMC performance, i.e. (1) ensuring the AC fundamental frequency current is split equally between the upper and lower arms; (2) eliminating the second order harmonic current in the differential-mode current; and (3) regulating the DC common-mode current to maintain balanced power between the upper and lower arms. To achieve these three control targets, an improved control strategy was proposed which contains three controllers for controlling the differential-mode current, common-mode current and power balance, respectively. Detailed control system design was presented and the effectiveness of the proposed scheme in a three-phase MMC system and a single-phase MMC system was confirmed by the simulation studies and experimental results.

Chapter 5

Hybrid modular multilevel converter

This chapter presents a Hybrid Modular Multilevel Converter (H-MMC), which combines FBSM and HBSM. In contrast to the conventional HB-MMC, the FB-MMC has the advantage of DC fault blocking capacity, but at the expense of increased power semiconductor devices and power losses. Combining the relative advantages of HB–MMC and FB-MMC, the proposed topology has the same DC fault blocking capability but uses fewer power devices and has less power loss than the FB-MMC. To increase power transmission capability of the proposed H-MMC, negative voltage states of the FBSMs are adopted to extend the output voltage range. The optimal ratio of FBSMs and HBSMs, and the number of FBSMs generating negative voltage states are calculated to ensure successful DC fault blocking and capacitor voltage balancing. Equivalent circuits which use two voltage sources per arm structure are proposed and two-stage selecting and sorting algorithms for capacitor voltage balancing are developed. Comparative studies for different circuit configurations considering DC fault blocking capability, power losses, and device utilization show excellent performance of the proposed H-MMC. The pre-charging process and transient DC fault ride-through capability of the H-MMC are also investigated Simulation and experiment results demonstrate feasibility and validity of the proposed configuration.

5.1 H-MMC design principle

5.1.1 Basic configuration

Fig. 5.1 shows one leg of the proposed H-MMC. Each of the two arms in the leg has N sub-modules, comprising F FBSMs, notated as $SM_{f(1)}$ to $SM_{f(F)}$ and N-F HBSMs denoted as $SM_{h(1)}$ to $SM_{h(N-F)}$. The total voltages generated by all the SMs in the upper and lower arms are represented by v_{pa} and v_{na}, respectively. i_{pa} and i_{na} are the upper and lower arm currents, respectively, and i_a is the output AC phase current.

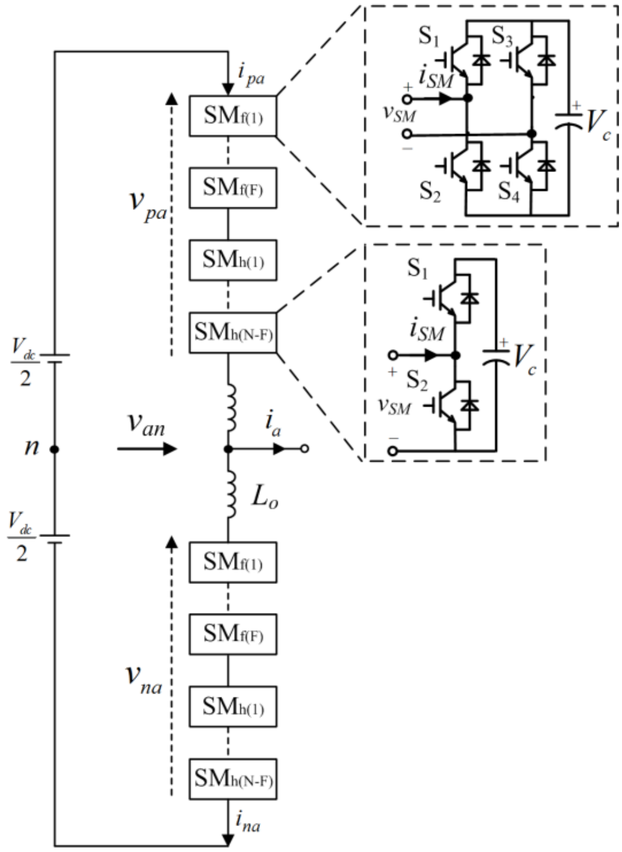


Fig. 5. 1 Basic Structure of a H-MMC

Tables 5-1 and 5-2 show the switch states for an FBSM and HBSM, respectively. Compared to the HBSM which can generate voltage states V_c and 0, each FBSM can generate a third state of -V_c. In the proposed scheme, some of the FBSMs are allowed to generate the -V_c voltage state to increase the AC output voltage.

Table 5- 1 Switch states of FBSM

STATE	S_1	S_2	S_3	S_4	v_{sm}	$V_c (i_{sM}>0)$
1	1	0	0	1	V_C	*charging*

2	0	1	0	1	0	*bypassed*
3	1	0	1	0	0	*bypassed*
4	0	1	1	0	$-V_C$	*discharging*
BLOCK	0	0	0	0	-	-

Table 5- 2 Switch states of HBSM

STATE	S_1	S_2	v_{sm}	$V_c\,(i_{sM}>0)$
1	1	0	V_C	*charging*
2	0	1	0	*bypassed*

For the hybrid configuration shown in Fig. 5.1, the range of the generated total arm voltage is from 0 to NV_c for the conventional method without using the $-V_c$ state of the FBSMs. Thus, considering a maximum modulation index *m* of 1, the DC and peak AC phase voltages are:

$$V_{dc} = NV_c, \qquad V_{an\_peak} = \frac{1}{2}NV_c = \frac{1}{2}V_{dc} \tag{5.1}$$

If *M* FBSMs in the H-MMC are allowed to generate the $-V_c$ state in each arm ($M < F$), the arm voltage range will be extended to the range from $-MV_c$ to NV_c. Under such conditions, the DC and peak AC phase voltages are:

$$
\begin{aligned}
V_{dc} &= (N-M)V_c \\
V_{an\_peak} &= \frac{1}{2}(N+M)V_c = \frac{1}{2}V_{dc} + \frac{MV_{dc}}{N-M}
\end{aligned}
\tag{5.2}
$$

From (5.2) the peak AC phase voltage can be extended due to M FBSMs generating the -V_c state. The above relationship is illustrated in Fig. 5.2.

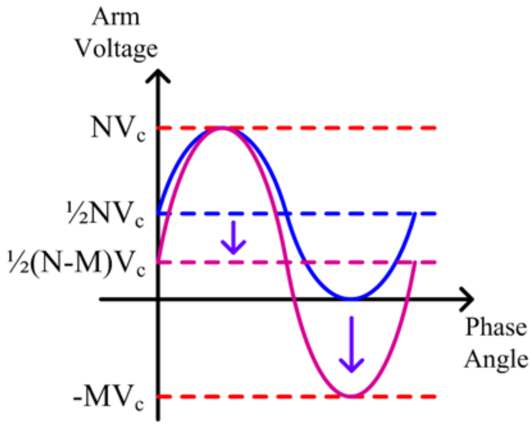


Fig. 5. 2 Relationship of DC and peak arm voltages extension

5.1.2 Capacitor voltage balancing consideration

For satisfactory MMC operation it is necessary to ensure the capacitor voltage in each SM can be balanced. In contrast to FBSMs that can charge and discharge their SM capacitors without having to change the external current direction, HBSM capacitors can only be charged during positive arm current and discharged during negative arm current. As the number of FBSMs generating a -V_c state increases, the relationships among the AC voltage, DC voltage, and DC current also change. Thus it is necessary to analyze the impact of the number of FBSMs generating the -V_c state on the charging and discharging times for the SM capacitors.

Neglecting converter power loss, the steady-state three-phase AC and DC powers are:

$$
P_{dc} = V_{dc}I_{dc} = \frac{3}{2}V_m I_m \cos\varphi = P_{ac} \tag{5.3}
$$

where V_m and I_m are the peak AC output phase voltage and current, φ is the voltage and current phase angle, and I_{dc} is the DC current.

Substituting $V_m = \frac{1}{2} mV_{dc}$ into (5.3) yield

$$I_{dc} = \frac{3mI_m \cos\varphi}{4} \tag{5.4}$$

where m is the modulation index.

Considering the fundamental frequency and DC components, the arm currents are given by

$$\begin{cases} i_p = \dfrac{I_m \sin(\omega t - \varphi)}{2} + \dfrac{I_{dc}}{3} \\ i_n = -\dfrac{I_m \sin(\omega t - \varphi)}{2} + \dfrac{I_{dc}}{3} \end{cases} \tag{5.5}$$

Substituting (5.4) into (5.5) yields

$$\begin{cases} i_p = \dfrac{I_m \sin(\omega t - \varphi)}{2} + \dfrac{mI_m \cos\varphi}{4} \\ i_n = -\dfrac{I_m \sin(\omega t - \varphi)}{2} + \dfrac{mI_m \cos\varphi}{4} \end{cases} \tag{5.6}$$

To ensure sufficient charging and discharging times for the HBSMs, the arm currents must be both positive and negative within one complete period. So the following equation must be satisfied:

$$\frac{mI_m \cos\varphi}{4} \le \frac{mI_m}{4} \le \frac{I_m}{2} \tag{5.7}$$

Thus the modulation index m must be less than or equal to 2. According to (5.2), the following relationship can be derived:

$$\frac{V_{dc}}{2} + \frac{MV_{dc}}{N-M} \le V_{dc}, \qquad M \le \frac{N}{3} \tag{5.8}$$

It can be concluded that for the H-MMC, M (the number of FBSMs generating -

V_c) must not be greater than ⅓ N in order to ensure sufficient charging and discharging times for the HBSMs to balance their capacitor voltages within each fundamental period.

5.1.3 DC fault blocking consideration

As previously described, if the series voltage formed by all the FBSM capacitors along a fault current path is higher than the AC line-to-line voltage, a DC fault can be blocked once all the IGBTs are switched off. In view of this requirement, the minimum number of FBSMs within each arm can be derived.

According to (5.2), the peak line-to-line AC voltage for the MMC during a DC fault is

$$u_{\max} = \sqrt{3} \times \frac{N+M}{2(N-M)} V_{dc} \tag{5.9}$$

Each arm has F FBSMs, thus the arm voltage formed by the FBSMs during DC faults is

$$u_{arm} = FV_c = \frac{F}{(N-M)} V_{dc} \tag{5.10}$$

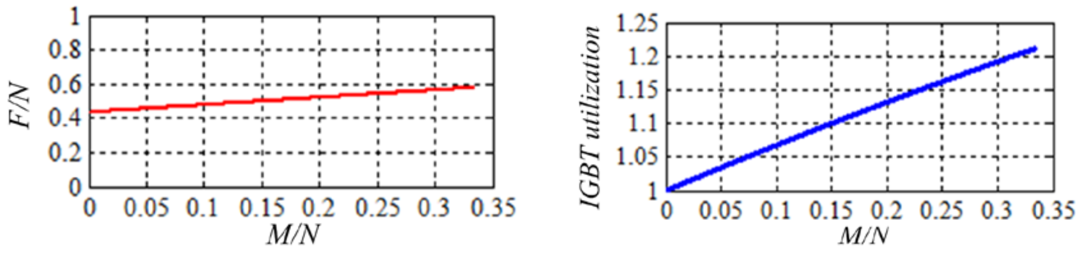
Therefore, the blocking voltage formed by two series arm voltages (one upper arm and one lower arm in different legs) and the AC line-to-line voltage should meet the following criteria

$$u_{\max} = \frac{\sqrt{3}}{2} \frac{N+M}{(N-M)} V_{dc} \le \frac{2F}{(N-M)} V_{dc} = 2u_{arm} \tag{5.11}$$

Thus, to successfully block DC faults, the total number of FBSMs has to meet the following requirement

$$F \ge \frac{\sqrt{3}}{4}(N+M) \tag{5.12}$$

According to this analysis, both (5.8) and (5.12) need be satisfied when designing the H-MMC. Fig. 5.3 (a) shows the minimum allowed *F/N* value, which results in the lowest number of required power device, for the variation of *M/N* from 0 to 1/3. In Fig. 5.3 (b), the normalized maximum IGBT utilization where the value at M = 0 is defined as 1 (higher value means better use of the IGBT or for delivering same power, less IGBT would be required), is illustrated. As can be seen, the maximum device utilization increases with the increase of the *M/N* value.



(a) (b)

Fig. 5. 3 Impact of M variation on *F* value and IGBT device utilization

5.1.4 Two specific H-MMCs

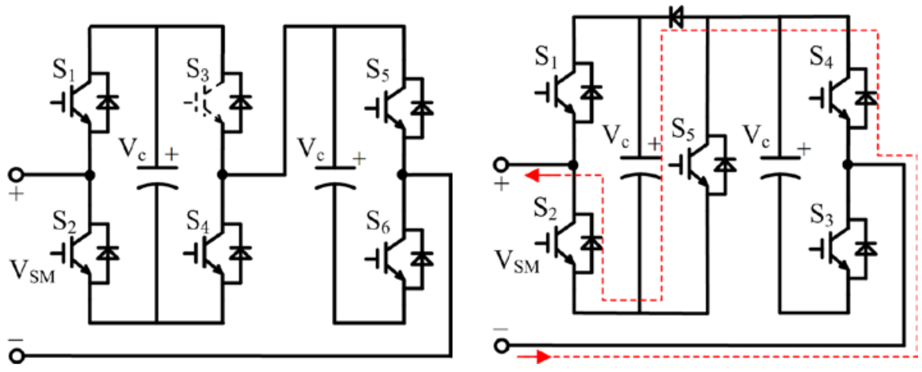
According to the above analysis, two specific conditions are considered.

1) M = 0, *F* = ½*N (the first configuration)*

In this scenario, the H-MMC consists of half HBSMs and half FBSMs and no -V_c voltage state is used for the FBSMs. Fig. 5.4 (a) shows a SM comprising of a pair of series-connected FBSM and HBSM, and its switching state is shown in Table 5-3.

According to Table 5-1, without using the –V_c voltage state in the normal operation, S_3 can be off permanently and therefore can be removed. However, the diode is still required to provide a path for the fault current during a DC fault. Thus, the simplified circuit is redrawn in Fig. 5.4 (b). Compared to the conventional HBSM, it requires one extra switch and two diodes for a hybrid SM. The normal operation of the hybrid converter is identical to the conventional HBSM based MMC systems with S_4 being switched on permanently. When a DC fault is detected, all the switching devices are then blocked to ensure one of the capacitors is connected to the fault current path as shown in Fig. 5.4 (b).

The conventional control strategy for the HB-MMC [SAE2010] can be adopted. No further discussion is presented here.



(a) FBSM + HBSM (b) Simplified topology

Fig. 5. 4 Structure of a hybrid SM in a hybrid MMC configuration

Table 5- 3 Switching states of hybrid SM

STATE	S_1	S_2	S_3	S_4	S_5	S_6	V_{SM}
1	1	0	0	1	0	1	$2V_C$
2	1	0	0	1	1	0	V_C
3	0	1	0	1	0	1	V_C
4	0	1	0	1	1	0	0
BLOCK	0	0	0	0	0	0	-

2) M = ⅓N, F = ⅔N (the second configuration)

In this scenario, the H-MMC consists of ⅓N HBSMs and ⅔N FBSMs (i.e., F=⅔N). Among the ⅔N FBSMs, the maximum number of SM generating -V_c state is half of the total FBSMs, i.e., ⅓ of the total number of SMs ($M=⅓N$).

5.1.5 Comparison of different topologies

The H-MMC systems are compared to the conventional HB-MMC and FB-MMC. Since the basic building blocks in the H-MMC are the same HBSM and FBSM as in the conventional MMC, the reliability of the H-MMC would be similar to the HB-MMC and FB-MMC.

Table 5- 4 Comparison among the four types of MMC

	HB-MMC	FB-MMC	H-MMC	
			M = 0, F = ½N	M = ⅓N, F = ⅔N
DC link voltage	V_{dc}	V_{dc}	V_{dc}	V_{dc}
Maximum AC voltage	$0.5V_{dc}$	$0.5V_{dc}$	$0.5V_{dc}$	V_{dc}
SMs/per arm	$2n$	$2n$	$2n$	$3n$
IGBTs/per arm	$4n$	$8n$	$6n$	$10n$
Diodes/per arm	$4n$	$8n$	$6n$	$10n$
Power capacity (p.u.)	1	1	1	2
Power capacity per IGBT	$1/(4n)$	$1/(8n)$	$1/(6n)$	$1/(5n)$
DC fault blocking	No	Yes	Yes	Yes

Table 5- 5 Parameters of the different systems

Item	HB-MMC	FB-MMC	H-MMC	
			M = 0, F = ½N	M = ⅓N, F = ⅔N
MMC rated power	5 MW	5 MW	5 MW	10 MW
DC voltage	5 kV	5 kV	5 kV	5 kV
AC voltage (L-L rms.)	2.5 kV	2.5 kV	2.5 kV	5 kV
No. of SMs per arm (N)	2	2	2	3
No. of IGBTs per arm	4	8	6	10
SM capacitor voltage	2.5 kV	2.5 kV	2.5 kV	2.5 kV
Average Switching frequency per SM (kHz)	1.25	1.25	1.25	FBSM: 1.05 HBSM: 0.40
Conduction Losses	24.0 kW (0.40%)	49.4 kW (0.82%)	36.7 kW (0.62%)	81.6 kW (0.68%)
Switching Losses	13.4 kW (0.22%)	13.4 kW (0.22%)	13.4 kW (0.22%)	38.0 kW (0.32%)

Total conversion losses	37.4 kW (0.6%)	62.8 kW (1.1%)	50.1 kW (0.8%)	119.6 kW (1.0%)

Table 5-4 shows the number of power semiconductors required for the different types of MMC. Taking the required semiconductor devices for the conventional HB-MMC as the bases for comparison, where 4*n* IGBT and 4*n* diode are required for each arm, for delivering the same power, the conventional FB-MMC doubles the required number of IGBT and diode (i.e., 8*n*). In comparison, the proposed H-MMC (M = 0, F = ½N) uses 50% more IGBT and diode (i.e., 6*n*) and the H-MMC (M = ⅓N, F = ⅔N) only has 25% increase in the total number of IGBT and diode (i.e., 5*n*) compared to HB-MMC. This indicates that the proposed H-MMC system can provide DC fault blocking capability without significantly increasing the total semiconductor devices.

To evaluate the power losses of the four MMC configurations, a simple loss calculation method based on the simulation data acquired from Matlab/Simulink is adopted [ROH2010]. The main parameters of the semiconductor module are derived from the datasheet of the 5SNA 1200G450300 [BAC2012], and the main parameters of the four MMC systems are shown in Table 5-5. The carrier frequency is 2.5 kHz for all four MMCs and the actual switching frequency for the SMs are also shown in Table 5-5.

The conduction and switching losses of the four MMC systems are also shown in Table 5-5. As expected, the conventional HB-MMC is the most efficient among the four MMC types. The proposed H-MMCs are shown as more efficient than the conventional FB-MMC due to the reduced switch number, hence conduction loss. The two hybrid configurations also have different features; M =⅓N, F = ⅔N results in a higher power density but slightly higher power loss than the configuration of M = 0, F = ½N, since the former needs extra switching for capacitor voltage balancing.

5.2 Capacitor voltage balancing for the second hybrid configuration

Due to the use of the negative voltage state for some FBSMs, the total voltage in each arm can be considered as two series-connected voltage sources as shown in Fig. 5.5. As shown, u_{p1} and u_{n1} refer to the AC voltages having amplitudes of ¼mV_{dc} generated by the M (i.e., ⅓N) FBSMs utilizing the -V_c state. u_{p2} and u_{n2} are the voltages generated by the remaining N-M SMs with the same AC voltage amplitudes of ¼mV_{dc} but with a DC offset of ½V_{dc}.

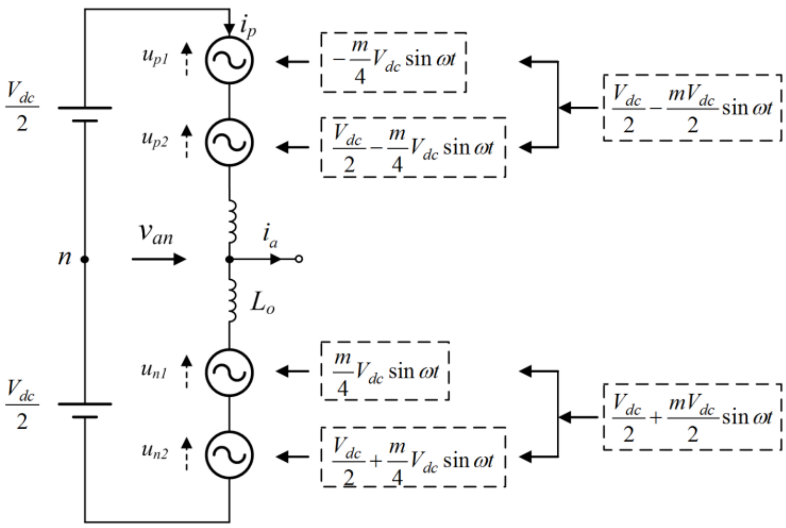


Fig. 5. 5 Equivalent circuit for the H-MMC

5.2.1 Steady-state analysis

Since the analysis in the upper and the lower arms in a leg is the same, the following analysis is based on the upper arm.

According to the presented analysis, the total arm voltage can be divided into two parts:

$$\begin{cases} u_{p1} = -\dfrac{mV_{dc}\sin\omega t}{4} \\ u_{p2} = \dfrac{V_{dc}}{2} - \dfrac{mV_{dc}\sin\omega t}{4} \end{cases} \tag{5.13}$$

The instantaneous power into each voltage source is

$$p_{p1} = u_{p1} \times i_p = -\frac{mV_{dc}}{4}\sin\omega t \times \left(\frac{I_m}{2}\sin(\omega t - \varphi) + \frac{mI_m}{4}\cos\varphi\right)$$
$$= -\frac{m^2 V_{dc} I_m}{16}\cos\varphi \sin\omega t - \frac{mV_{dc}I_m}{16}\cos\varphi + \frac{mV_{dc}I_m}{16}\cos(2\omega t - \varphi) \tag{5.14}$$

$$p_{p2} = u_{p2} \times i_p = \left(\frac{V_{dc}}{2} - \frac{mV_{dc}}{4}\sin\omega t\right)\left(\frac{I_m}{2}\sin(\omega t - \varphi) + \frac{mI_m}{4}\cos\varphi\right)$$
$$= \frac{V_{dc}I_m}{4}\sin(\omega t - \varphi) - \frac{m^2 V_{dc} I_m}{16}\cos\varphi \sin\omega t + \frac{mV_{dc}I_m}{16}\cos\varphi + \frac{mV_{dc}I_m}{16}\cos(2\omega t - \varphi) \tag{5.15}$$

Integrating the instantaneous power in one fundamental period yields the net energy flowing into each voltage source as

$$\Delta E_{p1} = \int_0^{2\pi} p_{p1} dt = -\frac{\pi m V_{dc} I_m \cos\varphi}{8} \le 0 \tag{5.16}$$

$$\Delta E_{p2} = \int_0^{2\pi} p_{p2} dt = \frac{\pi m V_{dc} I_m \cos\varphi}{8} \ge 0 \tag{5.17}$$

$$\Delta E = \Delta E_{p1} + \Delta E_{p2} = 0 \tag{5.18}$$

From (5.18), although the net energy transferring in one fundamental period in each arm is zero, the net energy in the two separate u_{p1} and u_{p2} is not zero. Therefore, in order to maintain capacitor voltage balance, it is necessary to exchange energy between u_{p1} and u_{p2} within each fundamental period. For this H-MMC configuration, ⅓N FBSMs are operated in u_{p1}, and the other ⅓N FBSMs are operated in u_{p2}. Thus, if each FBSM can be arranged to operate in both u_{p1} and u_{p2} by specific sorting and selecting algorithms, they can be used as a bridge for transferring energy between u_{p1} and u_{p2}.

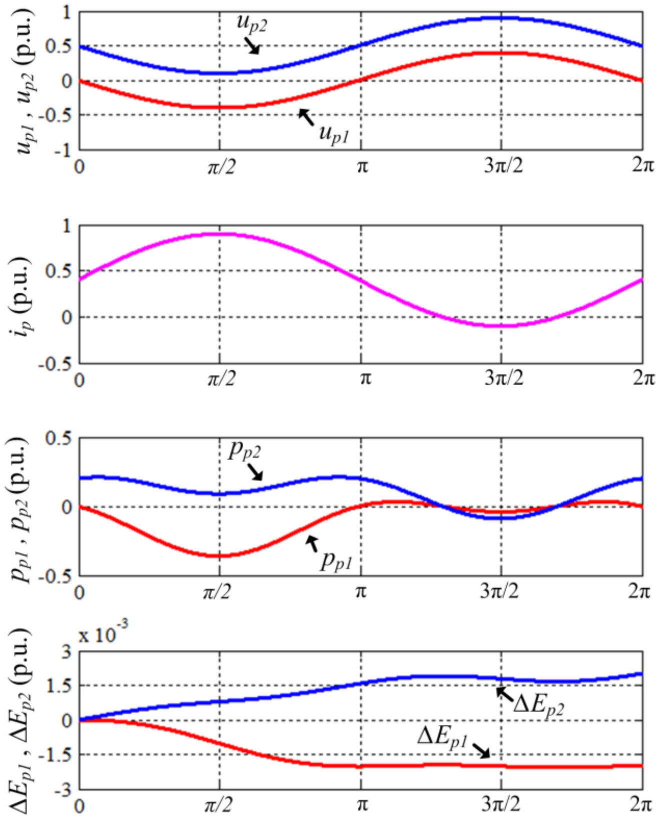


Fig. 5. 6 Transferring energy through u_{p1} and u_{p2}

5.2.2 Modified sorting and selection algorithm

As indicated in (5.6), increasing m in the proposed H-MMC gradually reduces the time intervals when the upper arm current i_p is negative. This affects capacitor voltage balance in the HBSMs due to the reduced discharging time. Thus, in contrast to the conventional capacitor voltage balancing algorithm [SAE2010], in which only capacitor voltage and arm current direction are used for SM selection, the selection of SMs in the H-MMC has to consider the differences in their behaviour, and charging and discharging periods between the FBSMs and HBSMs.

For illustrative purposes, Fig. 5.6 shows the reference voltages, arm current, and transferred energy in u_{p1} and u_{p2} in one complete period for φ = 0. From Fig. 5.6, ΔE_{p1} and ΔE_{p2} cannot reach balance in one complete period, as previously illustrated in (5.16) and (5.17). In the first half-cycle (0 to π), u_{p1} delivers energy while u_{p2} absorbs energy. Thus it is necessary to transfer energy between these two voltage sources to ensure their respective net energy flow can remain balanced in one complete period. A modified sorting and selecting algorithm is thus proposed, as shown in Fig. 5.6.

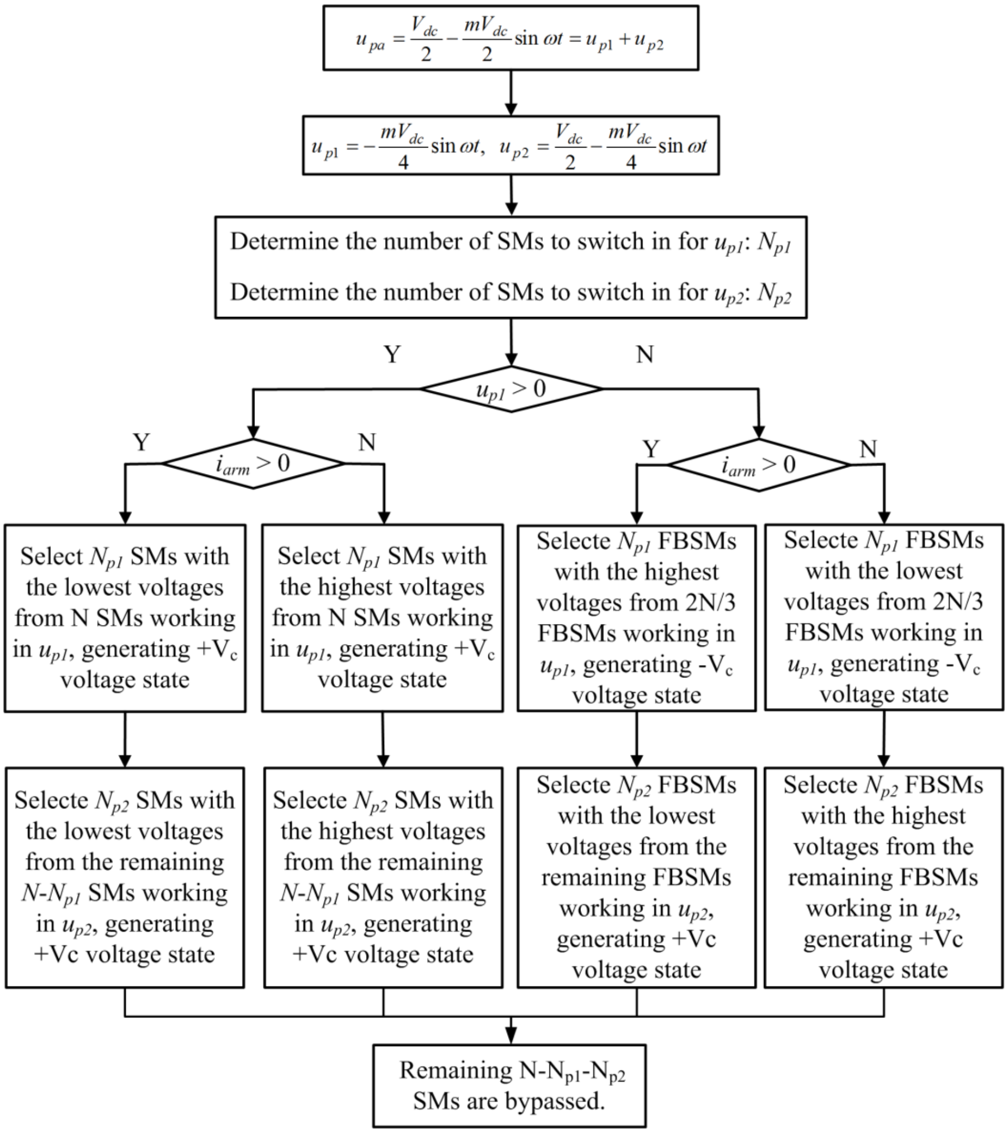


Fig. 5. 7 Modified sorting and selection algorithm for the hybrid MMC

The basic principles of the modified sorting and selection algorithm are summarized as follows.

- In the first half-cycle period (0 to π), all ⅔N FBSMs are sufficient to generate the required reference voltages in u_{p1} and u_{p2} (within 0 - ±0.5 p.u.). Thus only the ⅔N FBSMs are sorted and selected in this period with all the HBSMs producing zero output (i.e., their capacitors are bypassed). When the arm current is positive, the

FBSMs having the highest capacitor voltages are selected to operate in u_{p1} producing $-V_c$ output and their capacitors are discharged. The FBSMs having the lowest capacitor voltages are assigned to u_{p2} producing $+V_c$ output and their capacitors are charged. This selection is reversed when the arm current is negative. This ensures the capacitor voltages in all the $\frac{2}{3}N$ FBSMs are balanced.

- In the second half-cycle period (π to 2π), no $-V_c$ state is required. The sorting process is thus carried out within all N SMs where the SMs with the lowest capacitor voltages (for positive arm current) or the highest capacitor voltages (for negative arm current) are selected to operate in u_{p1} and u_{p2} producing $+V_c$ output. All the unselected SMs are bypassed generating zero voltage.

As the FBSMs are switched between u_{p1} and u_{p2} which effectively transfers energy between the two equivalent sources, all the capacitor voltages can be balanced.

5.2.3 Variations on capacitor energy storage

Due to the interactive behaviour between the FBSMs and HBSMs, their capacitor voltage ripple is now considered.

For the example in Fig. 5.6, the maximum discharging energy variation on the FBSM capacitors occurs in the first half-cycle, and can be expressed as

$$\begin{aligned}\Delta E_{fd\max} &= \max\left|\int\left(p_{p1}+p_{p2}\right)dt\right| = \max\left|\int_0^{\theta}\left(p_{p1}+p_{p2}\right)dt\right| \\ &= \left|\int_0^{\theta_1}\left(\begin{array}{l}\frac{V_{dc}I_m\sin(\omega t-\varphi)}{4}-\frac{m^2V_{dc}I_m\cos\varphi\sin\omega t}{8}\\ +\frac{mV_{dc}I_m\cos(2\omega t-\varphi)}{8}\end{array}\right)dt\right|\end{aligned} \tag{5.19}$$

where θ_1 refers to the phase angle resulting in maximum discharging energy variation.

The charging energy variation on capacitors in the FBSMs occurs in the second half-cycle before the arm current is negative. Initially, the FBSMs are selected to be charged so as to compensate the discharged energy in the first half-cycle. After compensation is completed, the following charged energy is then assumed to be equally distributed among the ⅔N FBSMs and ⅓N HBSMs groups. So the maximum charging energy variation in the FBSM capacitors is

$$\Delta E_{fc\max} = \frac{2\left|\int_0^{\theta_2} \left(p_{p1} + p_{p2}\right)dt\right|}{3} \tag{5.20}$$

where θ_2 is the phase angle when the arm current becomes negative.

Thus, the maximum energy variation on the FBSM capacitors is calculated as

$$\Delta E_{f\max} = \Delta E_{fc\max} + \Delta E_{fd\max} \tag{5.21}$$

For the HBSMs, the total energy flowing in the whole second half-cycle is zero for the capacitor voltages to be balanced. Since HBSMs can be discharged only when $i_{arm} < 0$, if the discharge energy is assumed to be equally distributed among the ⅔N FBSM and ⅓N HBSM groups, the maximum energy variation on the HBSM capacitors can be estimated by considering one third of the total discharging energy when $i_{arm} < 0$, i.e.:

$$\Delta E_{h\max} = \frac{\left|\int_{\theta_2}^{\theta_3} \left(p_{p1} + p_{p2}\right)dt\right|}{3} \tag{5.22}$$

where θ_2 to θ_3 is the period when the arm current is negative.

According to $\Delta E_{\max} = E_{\max} - E_{\min}$, the maximum energy variation can also be estimated:

$$\Delta E_{f\max} = \frac{C_f}{2}\left(u_{fc\max}^2 - u_{fc\min}^2\right)F = \frac{V_{dc}^2\left(D_{f\max}^2 - D_{f\min}^2\right)F}{2\left(N-M\right)^2}C_f \tag{5.23}$$

$$\Delta E_{h\max} = \tfrac{1}{2}C_h\left(u_{hc\max}^2 - u_{hc\min}^2\right)\times\left(N-F\right) = \frac{V_{dc}^2\left(D_{h\max}^2 - D_{h\min}^2\right)\left(N-F\right)}{2\left(N-M\right)^2}C_h \tag{5.24}$$

where D_{fmax}, D_{hmax} and D_{fmin}, D_{hmin} denote the per unit maximum and minimum capacitor voltage for the FBSMs and HBSMs, respectively.

Substituting (5.21) and (5.22) into (5.23) and (5.24), the capacitance for the FBSMs and HBSMs can be expressed as

$$C_f = \frac{2(N-M)^2}{V_{dc}^2\left(D_{f\max}^2 - D_{f\min}^2\right)F} \times \Delta E_{f\max} \tag{5.25}$$

$$C_h = \frac{2(N-M)^2}{V_{dc}^2\left(D_{h\max}^2 - D_{h\min}^2\right)(N-F)} \Delta E_{h\max} \tag{5.26}$$

The required capacitances for the HBSMs and FBSMs are different for the same voltage ripple and are also affected by operating conditions (i.e., ΔE_{fmax} and ΔE_{hmax} vary under different operation conditions). Taking the experimental prototype for example, when the capacitance ratio of the FBSM and HBSM is 4.46:1, the maximum capacitor voltage ripples are equal (N = 3, F = 2, M = 1, m = 1.6, V_{dc} = 120V, I_m = 7A, φ = 0).

5.2.4 Operation under reduced DC voltage

The above analysis is based on the normal operation with the DC voltage controlled at nominal values. However, large disturbances, e.g. faults on DC side can cause severe DC voltage drop. Under such a condition, a conventional HB-MMC based system could lose its control capability and has to be blocked to protect the IGBTs. With the proposed hybrid configuration, the relationship between the AC and DC voltages can be altered by changing the total number of SMs switched in (i.e. N) and the number of FBSMs generating -V_c state (i.e. M). However, the capacitor voltage balance in the FBSMs and HBSMs needs be considered carefully.

The total number of required SMs selected is now N' and the number of FBSMs generating the $-V_c$ state is M'. Assuming the AC system voltage remains the same whereas the DC voltage has dropped from V_{dc} to V_{dc}', the DC and AC phase voltages can be expressed as,

$$V_{dc}^{'} = kV_{dc} = k(N-M)V_c = \left(N^{'} - M^{'}\right)V_c \tag{5.27}$$

$$V_m = \frac{1}{2}(N+M)V_c = \frac{1}{2}\left(N^{'}+M^{'}\right)V_c \tag{5.28}$$

where *k* is the ratio between the new and initial DC voltages, and $k < 1$.

According to (5.27) and (5.28), the *N’* and *M’* are then calculated as,

$$\begin{cases} N^{'} = \frac{N}{2}(1+k) + \frac{M}{2}(1-k) < N \\ M^{'} = \frac{M}{2}(1+k) + \frac{N}{2}(1-k) > M \end{cases} \tag{5.29}$$

It is noted that the *N’* will have to decrease and *M’* to increase following the drop of DC voltage. Under the extreme condition of $V'_{DC} = 0$ (i.e. $k = 0$), $M' = N' = (M+N)/2$. For previous design of $M = ⅓N$, $F = ⅔N$, this leads to $M' = N' = ⅔N$. This means the selection is carried out in the FBSMs and all the HBSMs are bypassed indicating the H-MMC is capable of operating during zero DC voltage. Under other lower DC voltage conditions, the HBSMs will still be used.

The power on AC and DC sides are given as,

$$P^{'}_{dc} = V^{'}_{dc} I^{'}_{dc} = \frac{3}{2} V_m I^{'}_m \cos\varphi^{'} = P^{'}_{ac} \tag{5.30}$$

where I'_{DC} is the new DC current, I'_m and φ' are the new AC current amplitude and power factor angle, respectively.

The upper arm current is now rewritten as,

$$i^{'}_p = \frac{1}{2} I^{'}_m \sin\left(\omega t - \varphi^{'}\right) + \frac{1}{3} I^{'}{}_{dc} \tag{5.31}$$

Substituting (5.30) into (5.31) yields,

$$i^{'}_p = \frac{V^{'}_{dc}}{3V_m \cos\varphi} I^{'}{}_{dc} \sin\left(\omega t - \varphi^{'}\right) + \frac{1}{3} I^{'}{}_{dc} \tag{5.32}$$

To ensure sufficient charging and discharging times for the HBSMs, the arm currents must have both positive and negative periods within one complete cycle. So the following equation must be satisfied:

$$\frac{V_{dc}^{'}}{3V_m \cos\varphi} I^{'}_{dc} \geq \frac{1}{3} I^{'}_{dc} \tag{5.33}$$

Substituting (5.27) and (5.28) into (5.33) gives the required power factor as

$$\cos\varphi^{'} \leq \frac{2k(N-M)}{(N+M)} \tag{5.34}$$

Equation (5.33) indicates that the power factor should be reduced following the drop of DC voltage. That means the control system needs use reactive current to ensure enough discharging period for HBSMs so as to maintain SM capacitor voltage balancing. Again for the proposed design of $M=⅓N$, this leads to $\cos\varphi^{'} \leq k$ (k<1).

Thus, the proposed H-MMC can continue operating under reduced DC voltage with proper selection of the total number of SMs to be used (i.e., N'), the number of FBSMs generating $-V_c$ (i.e., M'), and the output power factor (i.e., φ'). The previously proposed sorting and selection algorithm is still applicable for maintaining SM capacitor voltage balancing and the system operates in the same way as normal condition, e.g. controlling the AC output and circulating currents. The maximum energy variations on FBSMs and HBSMs can still be derived from (5.23) and (5.24) by replacing N, M, φ with N', M' and φ' from (5.29) and (5.34), and the SM capacitor voltage ripple can be estimated accordingly.

5.3 Pre-charging process

As illustrated in Fig. 5.4(b), when the arm current flows from the negative terminal of a SM (i.e., current flow from AC to DC), only the capacitor in the FBSM is charged while the capacitor in the HBSM is bypassed when all IGBTs are gated off. Thus, compared to other types of MMC, pre-charging the proposed H-MMC has a unique issue of unbalanced charging among the HBSMs and FBSMs. Thus it is necessary to investigate the pre-charging scheme for the H-MMC.

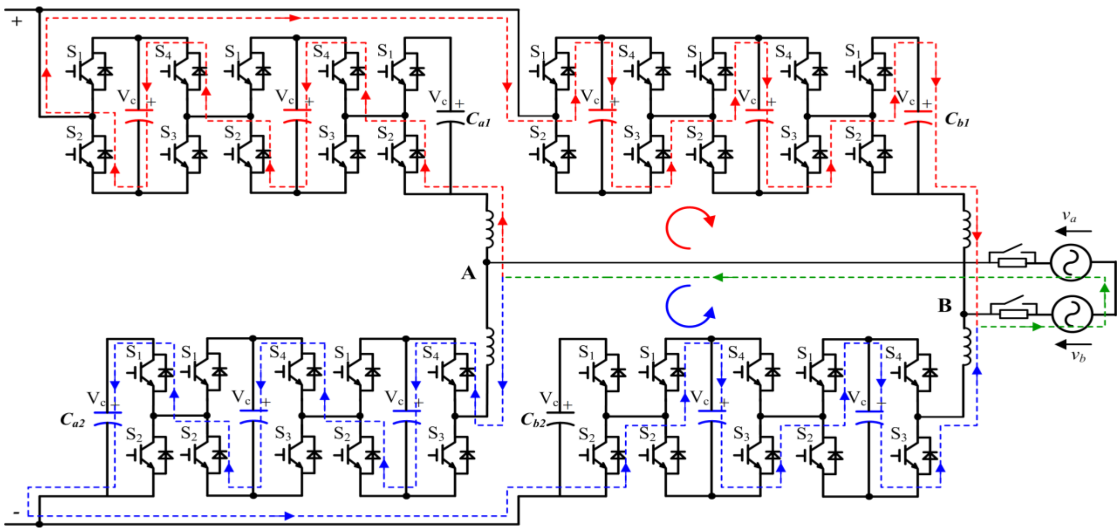


Fig. 5. 8 Two charging current loops under the uncontrolled charging stage

To illustrate the pre-charging process of the H-MMC, Fig. 5.8 shows a two-phase example of a simplified MMC with each arm consisting of 2 FBSMs and 1 HBSM. In this example, $v_a > v_b$ so the initial AC charging current flows from phase *a* to phase *b*.

5.3.1 Uncontrolled charging stage

Initially, all SM capacitors voltages are assumed to be zero. To prevent large inrush current, pre-charging resistors may be inserted at the AC side. As shown in Fig. 5.7, the uncontrolled charging has two parallel loops in this example, one formed by the upper two arms and the other by the lower two arms. As seen, all FBSM capacitors are being charged but the charging of the HBSM capacitors is dependent on the current direction, i.e., only the HBSM capacitors in the lower phase *a* arm and upper phase *b* arm (marked as C_{a2} and C_{b1} in Fig. 5.8) are being charged whereas the HBSM capacitors in the upper phase *a* arm and lower phase *b* arm (marked as C_{a1} and C_{b2} in Fig. 5.8) are being bypassed. When the AC charging current changes direction, the charging for all the FBSM capacitors continues but the charging for the HBSM capacitors is changed, i.e., C_{a1} and C_{b2} will be charged and C_{a2} and C_{b1} bypassed. This indicates that there is unequal charging between the capacitors in the HBSMs and FBSMs. When the combined capacitor voltages within each current path become higher than the maximum value of the phase-to-phase AC voltage, the charging current gradually goes to zero and the uncontrolled charging stage ends.

5.3.2 Controlled charging stage

A grouping sequentially controlled charge method was proposed in [XUE2014] to solve the insufficient charging issue for the conventional MMC. However, to handle the unique issue of unbalanced capacitor charging in the H-MMC, a new method is proposed as follows.

Step1: The FBSMs and HBSMs in each arm are arranged into j and k groups, respectively. Each time only one group is chosen for charging with all the IGBTs in the chosen group are turned off. The other unselected groups are bypassed by turning on the appropriate IGBTs (v_{SM} = 0). When the sum of the series-connected capacitors voltages in the two chosen groups in the two-phase arms becomes higher than the maximum value of the phase-to-phase AC voltage of $\sqrt{3}V_{dc}$ (according to (5.9)), the charging current reduces to zero. Thus, to ensure the capacitors in the chosen group are charged to the pre-set value of $1.5V_{dc}/N$ (as M=N/3), the number of j and k should meet the following requirement,

$$\begin{aligned} &\frac{2N}{3j}\times\frac{1.5V_{dc}}{N}\times 2\le\sqrt{3}V_{dc}, \qquad j\ge\frac{2\sqrt{3}}{3}\approx 1.2 \\ &\frac{N}{3k}\times\frac{1.5V_{dc}}{N}\times 1\le\sqrt{3}V_{dc}, \qquad k\ge\frac{\sqrt{3}}{6}\approx 0.3 \end{aligned} \tag{5.35}$$

Equation (5.35) indicates that for simple and fast charging, the FBSMs in each arm can be separated into 2 groups (i.e., j=2) and the HBSMs are in one single group (i.e., k=1).

Step 2: After all capacitors in the charging group reach the pre-set value of $1.5V_{dc}/N$, SMs in this group are bypassed and the charging for the next group can start.

Step 3: When the charging processes for all the groups complete, the controlled charging stage completes.

5.4 Ride-through capability under a transient DC fault

By using the negative voltage state of the FBSMs, the SMs can generate negative arm voltage. In such a way, the H-MMC can continue operating under the reduced DC-link voltage (even V_{dc} = 0). This means the H-MMC can not only block DC fault, but also continue operating to regulate its output AC current, e.g., to support the healthy AC grid and to provide fast fault recovery and system restart. The control sequence can be divided into following three stages.

Stage 1: When a DC fault occurs, the DC link voltage collapses immediately. Under such a condition, the *d*-axis reference AC current for active power reduces proportionally, (i.e. when V_{dc} = 0, I_d^* = 0), while the *q*-axis reference AC current for reactive power can remain unchanged or set to a new value to support the AC grid. For systems using over-head-line (OHL), automatically system recovery may be required as the DC fault might be temporary. For future large multi-terminal HVDC system using cables, the faulty branch maybe isolated by protection devices, e.g., DC circuit breaker and rapid system restart for the health network might be required. In this case, the control process moves to Stage 2 for the recovery operation.

Stage 2: A small DC-link reference voltage is provided and the system tries to build up the DC-link voltage. If the DC voltage can be built up successfully indicating the clearance of the DC fault, the control process moves to Stage 3. Otherwise, the DC-link reference voltage sets to zero again and the system waits for the next attempt for rebuilding the DC-link voltage.

Stage 3: The restart process can be considered under an initial condition of V_{dc} = 0 in accordance to (3.9). A ramp signal for the DC voltage reference can then be set and by controlling the *d*-axis and *q*-axis AC current the DC-link voltage can be built up smoothly.

5.5 Simulation results

To verify the behaviours of the H-MMC, a grid-connected H-MMC is developed using Matlab/Simulink, and is shown in Fig. 5.9. The H-MMC contains 4 FBSMs and 2 HBSMs in each arm, in which two of the FBSMs are allowed to generate $-V_c$

state The AC grid voltage is 110 kV, connecting a step-down transformer with a ratio of 110 kV/60 kV. Because of the use of -V_c state, the phase-to-phase AC voltage at the secondary side of transformer is 60 kV for a DC voltage of 60 kV, being higher than the conventional MMC system for the same DC voltage. Each SM has a voltage of 15 kV, i.e., ¼ of the nominal DC voltage of 60 kV. In the simulation, the rated power is 90MW, the capacitance for all the SMs is 2200 uF, and a conventional phase-disposition PWM method with a carrier frequency of 2.5 kHz is used. The voltage balancing method is the proposed two-stage sorting and selecting algorithm, as presented in Fig. 5.7.

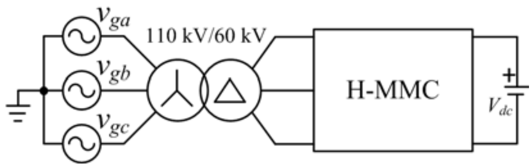


Fig. 5. 9 Schematic diagram of the simulation platform

Fig. 5.10 shows the simulation results illustrating the steady-state performance of the H-MMC. From Fig. 5.10, it can be observed that although the charging and discharging periods for the FBSMs and HBSMs are different in the H-MMC, all capacitor voltages can be balanced within each fundamental period.

Fig. 5.11 shows the operation of the H-MMC including the pre-charging process and DC fault ride-through and system recovery. In the simulation, it is assumed that the DC fault is cleared itself due to the use of OHL. However, the recovery process can also be used for future multi-terminal HVDC systems where the faulty branch is cleared by using other protection devices, e.g., DC circuit breaker etc. As illustrated in Figs. 5.11 (b) and (c), at the end of the uncontrolled charging stage (Stage I), the capacitor voltages in the FBSMs are higher than that in the HBSMs due to the unequal charging process. During stage II, the FBSMs are divided into two groups while the HBSMs are combined into one group according to (5.35). At 0.2s, the first FBSM group begins to be charged, and after all the capacitors in the first group reach the pre-set value, the charging process shifts to the second FBSM group, and then to the HBSM group. As shown, the presented pre-charging scheme successfully solves the unbalanced charging issue in the H-MMC. After the pre-charging process, the H-MMC starts building the DC-link voltage (stage III). A ramp signal for the DC voltage reference (1 pu / 0.1 s) is provided and the DC-link voltage is built up smoothly. The H-MMC then resumes normal mode (Stage IV) at 1.0 s by increasing its active power transmission to 1.0 pu with 0.4 s.

At 1.8 s, a temporary 250 ms pole-to-pole DC fault is applied (stage V). The DC voltage quickly drops to zero, the H-MMC reduces the active power to zero accordingly and meanwhile, it supplies 0.3 p.u. reactive power to the AC grid. It demonstrates that the H-MMC can not only block the DC fault, but also continue operating to regulate the AC current, indicating an excellent DC fault ride-through capability. At 1.9 s and 2.0 s, two attempts for building up the DC-link voltage are carried out by setting a small DC-link reference voltage though both attempts are failed due to the existing fault. As the DC fault is cleared at 2.05 s, the third attempt by the H-MMC at 2.1 s successfully builds up a small DC-link voltage and the process then moves to the DC-link voltage building stage. At 2.2 s, the DC voltage has fully recovered and the active power is then gradually increased and the system recovers to normal operation (stage VI).

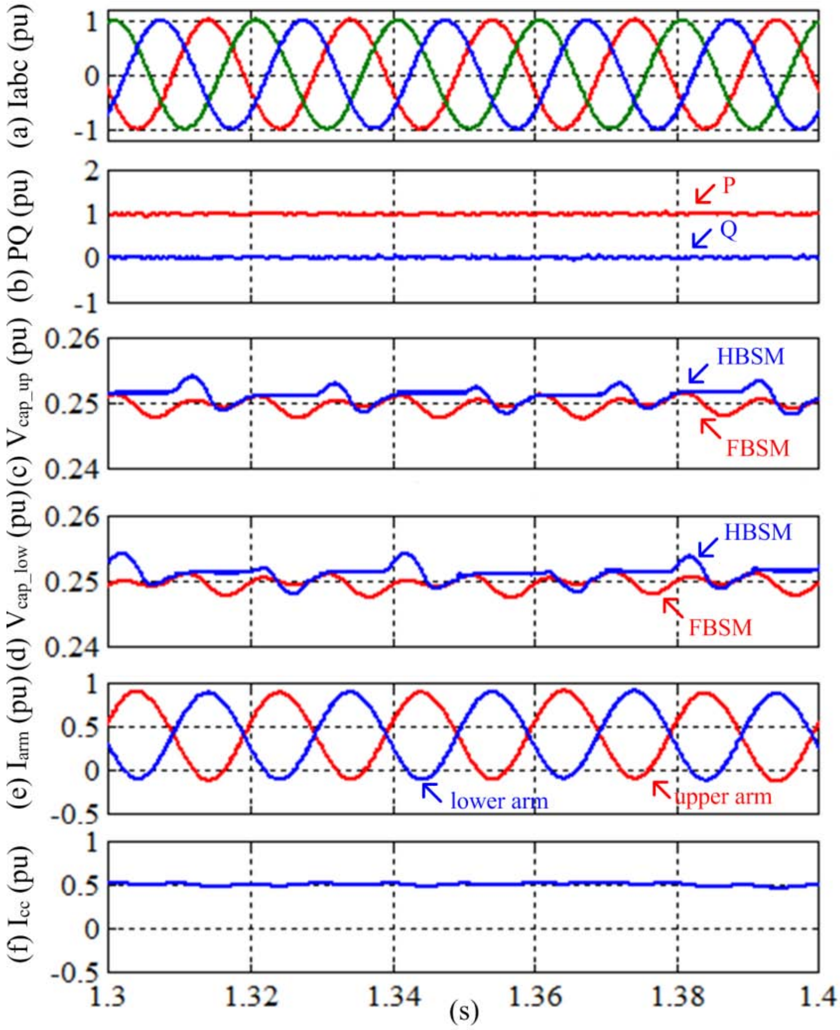


Fig. 5. 10 Simulation results for the H-MMC, (a) AC current; (b) converter output P and Q; (c) upper arm capacitor voltages; (d) lower arm capacitor voltages (e) arm currents; (e) common mode arm current.

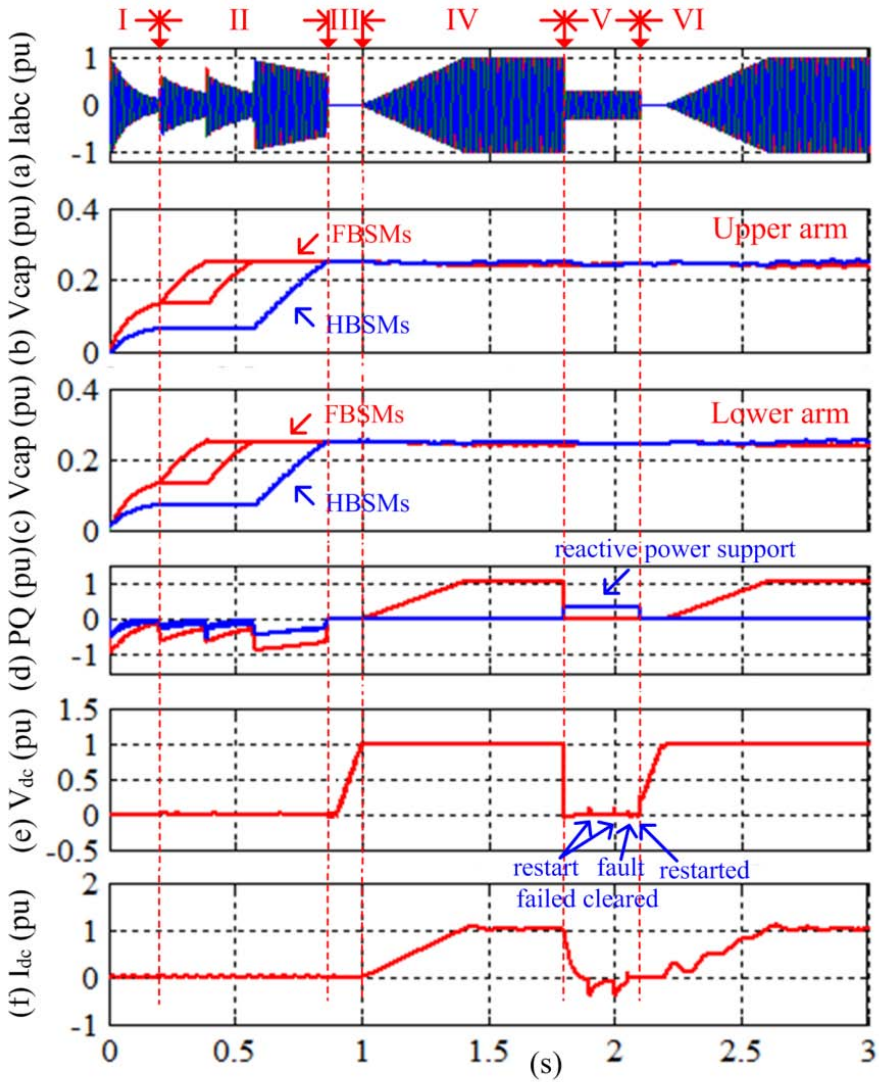


Fig. 5. 11 Simulation results demonstrating DC fault ride-through capability of HVDC transmission systems based on the H-MMC, (a) AC current; (b) phase a upper arm SM capacitor voltages; (c) phase a lower arm SM capacitor voltages; (d) converter output P and Q; (e) DC-link voltage; (f) DC link current.

5.6 Experiment results

To verify the presented analysis for the H-MMC with $M = ⅓N$ and $F = ⅔N$, a prototype single-phase H-MMC rated at 400 W was developed and its layout is shown in Fig. 5.12. Each arm contains two FBSMs and one HBSM. The control system is implemented using a TMS320F2812 DSP and the main parameters are listed in Table 5-6. Two series-connected large DC capacitors are parallel connected across the DC power supply to create the neutral point.

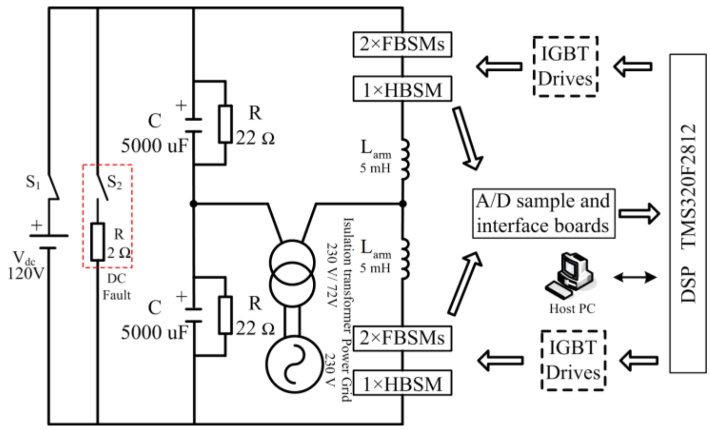


Fig. 5. 12 Schematic diagram of the experimental system

Table 5- 6 Parameters of the experimental MMC system

Item	Values
MMC rated power	400 W
DC voltage	120 V
AC voltage (phase-ground rms.)	72 V
Number of SMs per arm	3
Number of FBSMs per arm	2
Number of HBSMs per arm	1
DC voltage per SM	60 V
SM capacitor	940 µF
Inductance per arm	5 mH

MMC switching frequency	2.5 kHz

Figs. 5.13 and 14 show the respective steady-state and dynamic performances of the proposed H-MMC operating as an inverter in grid-connected mode, i.e. active power flows from the DC to AC. The output current shown in Fig. 5.13 is almost sinusoidal with low distortion. The peak-to-peak voltage ripple on the FBSM capacitors is approximately 11.7% whereas the voltage ripple on the HBSM capacitors is about 2.7%, being lower than that of the FBSMs due to the same capacitance being used (940μF). These values are in good agreement with the calculated ripple of 11.99% and 2.69% using (5.23) and (5.24) for the FBSMs and HBSMs, respectively. The HBSM is bypassed during the first half-cycle period, verifying the previous sorting analysis. All capacitor voltages remain balanced. In Fig. 5.14, the active power is stepped from 220W to 400W at 75ms. The H-Hybrid MMC tracks the current and power changes quickly and smoothly, and the capacitor voltages remain balanced during the transient. The FBSM capacitor voltage ripple is considerably larger after the power step (current increase) due to increased ΔE_{fmax}.

To further validate the relation between the voltage ripple and SM capacitance, Fig. 5.15 shows the measured voltage ripple for different capacitances. In these tests, the FBSM capacitance is fixed at 940μF, while capacitance for the HBSMs is varied at 940μF, 470μF and 235μF, respectively. As shown in Fig. 5.15, for the same capacitance, the maximum voltage ripples in the FBSMs and HBSMs with 940μF are approximately 11.7% and 2.7%, respectively. The respective maximum voltage ripple in the HBSM rises to 6.7% with 470μF and 10.0% with 235μF. These values are again in good agreement with the calculated HBSM capacitor voltage ripples of 2.69%, 5.37% and 10.75% for 940μF, 470μF and 230μF, respectively.

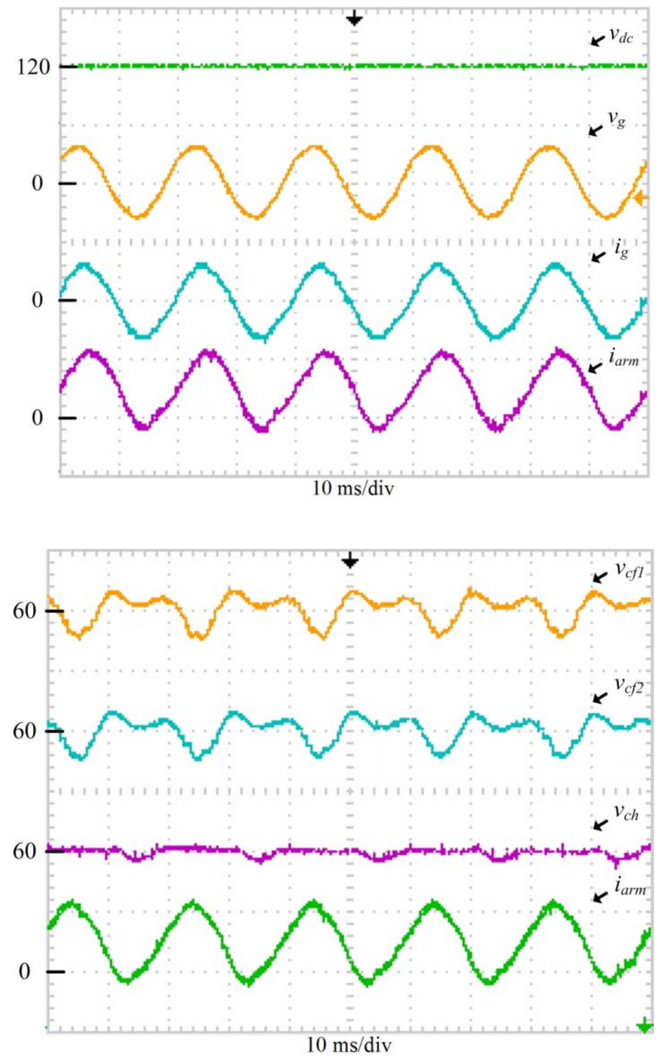


Fig. 5. 13 Steady-state operation as an inverter, V_{dc}: DC voltage (120V/div); v_g: grid voltage (170V/div); i_g: grid current (12A/div); i_{arm}: arm current (6A/div); v_{cf1}: capacitor voltage in FBSM1 (10V/div); v_{cf2}: capacitor voltage in FBSM2 (10V/div); v_{ch}: capacitor voltage in HBSM (10V/div)

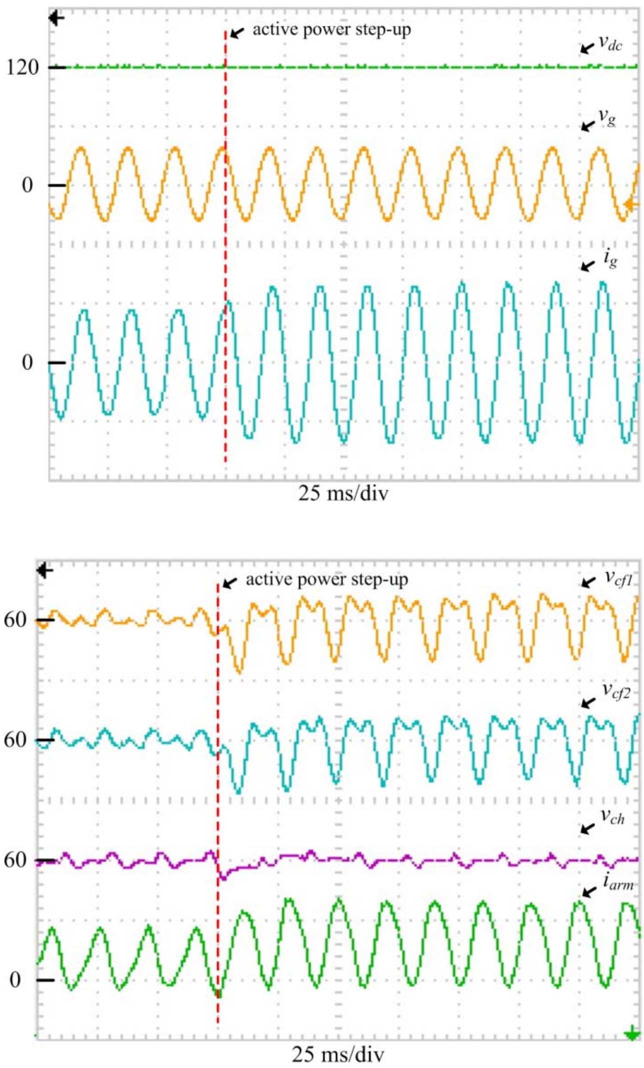


Fig. 5. 14 Dynamic operation as an inverter during active power step, V_{dc}: DC voltage (120V/div); v_g: grid voltage (170V/div); i_g: grid current (6A/div); i_{arm}: arm current (6A/div); v_{cf1}: capacitor voltage in FBSM1 (10V/div); v_{cf2}: capacitor voltage in FBSM2 (10V/div); v_{ch}: capacitor voltage in HBSM (10V/div)

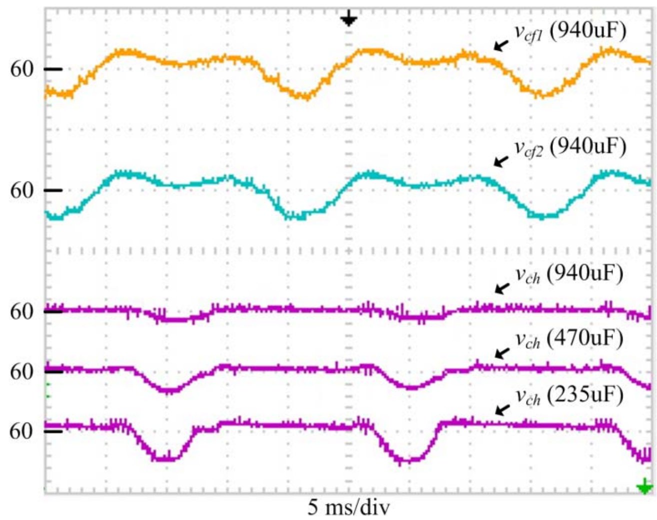
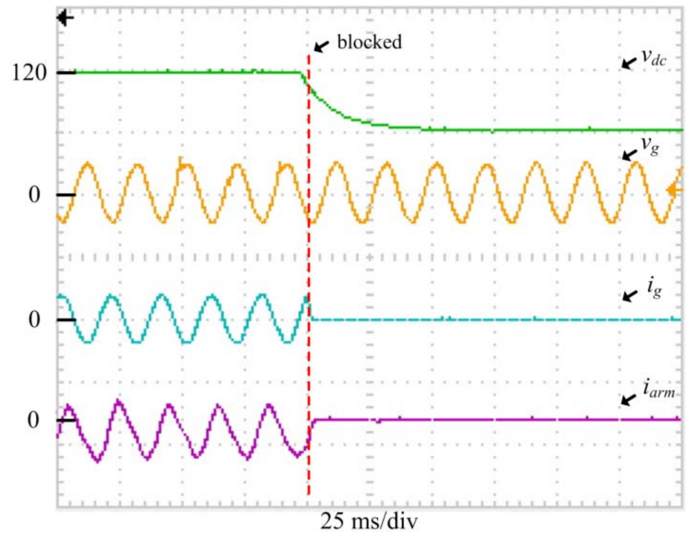


Fig. 5. 15 Relation between capacitor ripple and capacitor value, v_{cf1}: capacitor voltage in FBSM1 (10V/div); v_{cf2}: capacitor voltage in FBSM2 (10V/div); v_{ch}: capacitor voltage in HBSM (10V/div)

Fig. 5.16 shows the experimental results during a DC line-to-line fault applied on the H-MMC system. Initially, the H-MMC operates as a rectifier, absorbing active power (-245W) from the AC grid into the DC side (S_1 in Fig. 5. 12 is open). A DC fault is emulated by connecting a 2Ω resistor across the DC link (S_2 is closed). Immediately after the fault, the MMC remains operational until it is blocked when the over-current is detected as shown in Fig. 5.16 where i_{arm} increases rapidly after the emulated DC fault. The capacitors in the selected SMs discharge before converter blocking. The DC voltage collapses quickly. Once the IGBTs are blocked, the fault current flows through the series capacitors in the FBSMs, while the capacitor in the HBSM is bypassed. There is a short charging period for the FBSM capacitors, whereas the HBSM capacitor voltage remains constant after IGBT blocking. Since the total series voltage formed by the FBSMs is higher than the AC voltage, the AC current and arm current quickly reduce to zero and the DC fault is thus blocked.

Fig. 5.17 illustrates the operation performance of the H-MMC during significant DC voltage drop. Initially, the H-MMC operates as a rectifier, absorbing active power (370W) from the AC grid into the DC side with a nominal DC voltage of 120V. The DC voltage is then reduced from 120V to 70V (42% drop). For conventional VSC, such a large voltage drop would disable the converter operation since the DC voltage is now less than the AC voltage. For the proposed H-MMC, the active power is decreased proportionally to 215W (a reduction of 42%) and a reactive power of 100VAr is added to ensure sufficient charging period for the HBSMs. Under such condition, the modulation index rises to around 2.9. As shown in Fig. 5.17, the output AC current is still well controlled under such a large DC voltage drop, and the H-MMC can regulate the active and reactive power demonstrating excellent operation and flexibility during DC voltage drop.

To test the operation performance of the H-MMC under zero DC voltage conditions, Fig. 5.18 shows the experimental results of the H-MMC under severe DC voltage drop. It is observed the converter can still operate and supply reactive power to the AC grid for supporting the AC system, although the DC voltage drops from 120V to 0V (100% drop). This result shows that the H-MMC can continue controlling the AC current under a wide DC voltage range from 0 to rated value (i.e. 120V).



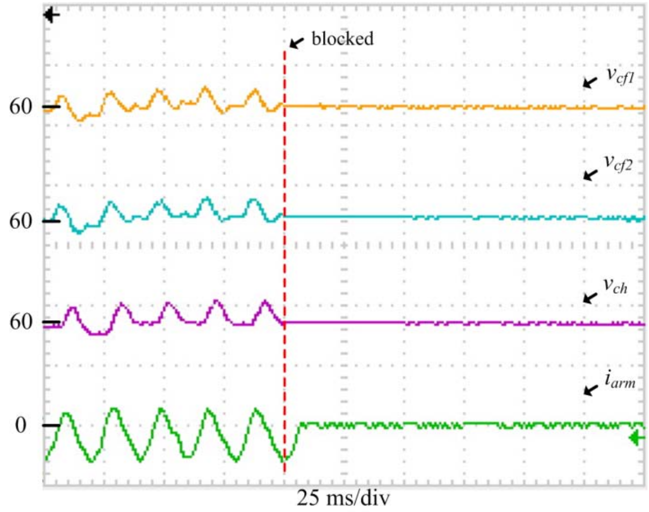


Fig. 5. 16 DC fault, V_{dc}: DC voltage (120V/div); v_g: grid voltage (170V/div); i_g: grid current (12A/div); i_{arm}: arm current (6A/div); v_{cf1}: capacitor voltage in FBSM1 (20V/div); v_{cf2}: capacitor voltage in FBSM2 (20V/div); v_{ch}: capacitor voltage in HBSM (20V/div)

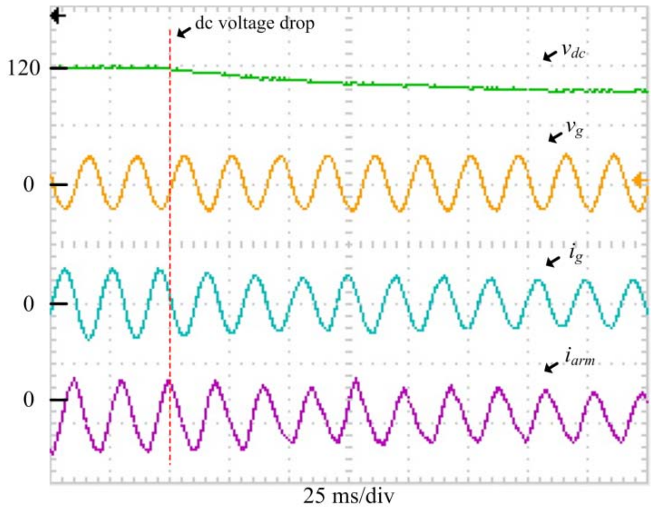


Fig. 5. 17 DC voltage drop, v_{dc}: DC voltage (120V/div); v_g: grid voltage (170V/div); i_g: grid current (12A/div); i_{arm}: arm current (6A/div)

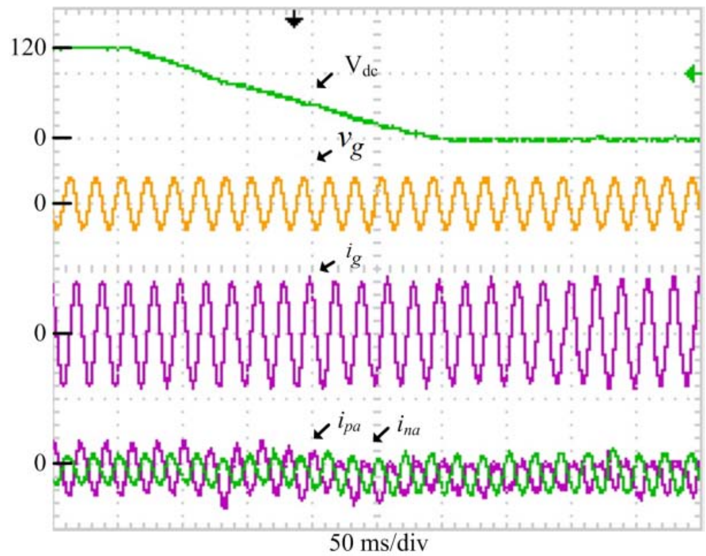
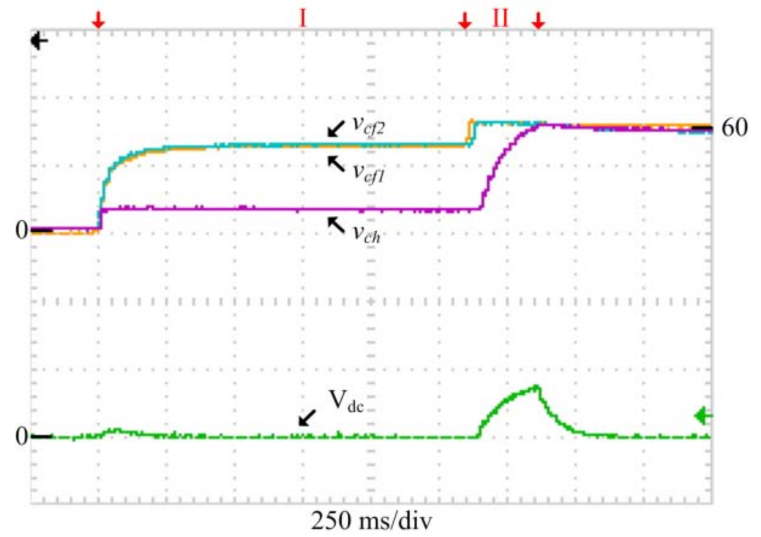


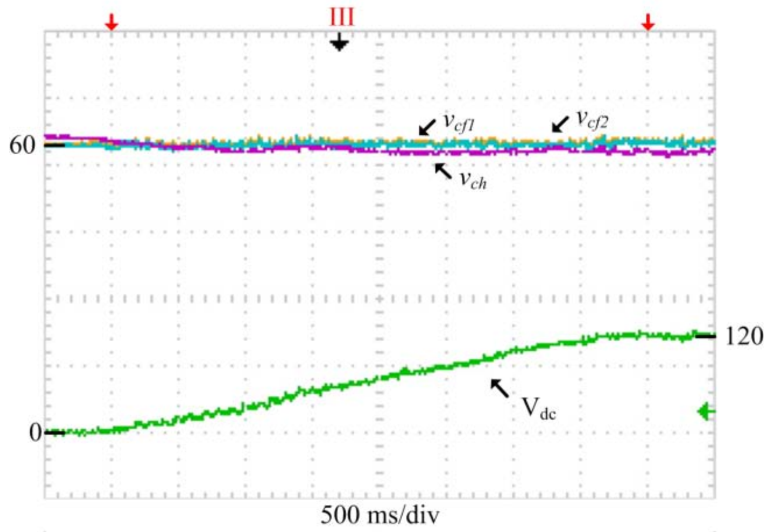
Fig. 5. 18 Operation of the H-MMC under DC fault conditions, V_{dc}: DC voltage (85V/div); v_g: AC voltage (255V/div); i_g: AC current (5A/div); i_{pa}: upper arm current (5A/div); i_{na}: lower arm current (5A/div).

To verify the pre-charging process of the H-MMC, in this test, the 120V DC source is removed. As previously described, for normal three-phase H-MMC, the system has two parallel charging loop one formed by the upper arms and the other formed by the lower arms. For the prototype single-phase H-MMC shown in Fig. 5.12, the two resistors on the DC side also forms two parallel charging loops for the upper and lower arms, and enables similar pre-charging process to be tested in the single-phase prototype.

Fig. 5.19 (a) shows the pre-charging process of the H-MMC. At 0.25s, the uncontrolled charging stage (Stage I) begins. As can be seen from Fig. 5.19 (a), the capacitor voltage in the FBSM is higher than that in HBSM and the capacitor voltages are insufficient and unbalanced at the end of the uncontrolled charging stage, which is in a good agreement with the previous illustration in Section 5.3. Then, at the controlled charging stage (Stage II), two FBSMs are divided into two groups, and one HBSM is set into the third group, according to (5.35). It can be observed that the presented pre-charging scheme successfully solves the unbalanced charging issue in the H-MMC. Following the pre-charging process, a DC voltage building process is presented in Fig. 5.19 (b). At this stage (Stage III), a ramp signal of 30 V/s is set to build up the DC voltage. It is observed that the DC voltage can track the ramp signal well and the building process is very smooth.



(a) Pre-charging process



(b) DC voltage building process

Fig. 5. 19 Operation of the H-MMC for the pre-charging process, V_{dc}: DC voltage (85V/div); v_{cf1}: capacitor voltage in FBSM1 (40V/div); v_{cf2}: capacitor voltage in FBSM2 (40V/div); v_{ch}: capacitor voltage in HBSM (40V/div)

5.7 Summary

This chapter proposes a hybrid MMC (H-MMC) configuration consisting of FBSMs and HBSMs. By adopting the negative voltage state for some of the FBSMs, the output voltage range is extended to increase converter power transmission capability. Considering the relationships between the AC and DC voltages, AC, DC and arm currents, the ratio of FBSM to HBSM were analysed in order to maintain capacitor voltage balance and retain DC fault blocking capability. An equivalent circuit for the hybrid MMC is proposed, which considers each arm to be consisted of two individual voltage sources. This model is then used to analyse SM capacitor voltage balancing and ripple. A two-stage selection and sorting algorithm is developed to ensure capacitor voltage balancing among the SMs. The proposed H-MMC is compared to other topologies in terms of power device utilization and power losses, and it shows that the H-MMC has higher device utilization and lower power loss than the conventional FB-MMC; Furthermore, The DC fault ride-through capability of the H-MMC are discussed. Such two features of the H-MMC show the advantages in the hybrid configurations over the conventional FB-MMC and HB-MMC systems. Additional, the pre-charging process is also studied and a modified group charging method is proposed to handle the unbalanced charging issue among the FBSMs and HBSMs in one arm. Both simulation and experimental results during steady state, power step, pre-charging process and DC fault (DC voltage drop) validate the theoretical analysis.

Chapter 6

Hybrid MMC for HVDC applications

This chapter presents two system configurations making use of the proposed hybrid MMC (H-MMC). One application is a multi-terminal high-power DC/DC converter configuration with DC fault blocking capability for interconnecting multi-terminal HVDC systems. Its main functions include bidirectional power flow, DC voltage step-up and step-down operation and fault isolationDC. In contrast to the conventional MMC based DC/DC converter consisting of two MMCs connected on the AC sides through a medium-frequency transformer [KEN2011], the proposed DC/DC converter with H-MMC configuration has the advantage of being able to block the DC/DC converter terminal connected to faulty DC grid section, while continue operating the other terminals connected to healthy DC grid sections. The second configuration is a hybrid HVDC system for integrating large wind farms comprising a wind farm side VSC based on the proposed H-MMC and a grid side LCC. Such configuration combines the advantages of both VSC and LCC, as VSC is suitable to connect wind farm into main grid, and LCC is cost-effective, which bring benefits of reduced device cost and power losses, according to the introduction in Chapter 1. This configuration can also be extended to multi-terminal systems with new VSC and/or LCC converters added to existing HVDC networks. For example, in China significant numbers of LCC HVDC systems are already in operation and a VSC converter could be added for integrating a new wind farm with the DC side connected to existing HVDC networks to form a large hybrid multi-terminal HVDC system. Since the LCC operates as an inverter, commutation failure is prone to occur which effectively results in DC short circuit and is equivalent to a pole-to-pole DC fault for the VSC. With the advantages of being able to operate at reduced DC voltage by the H-MMC, a coordinated control strategy for the hybrid HVDC system is proposed to improve its transient response under commutation failure conditions. The simulation results presented in this chapter for these two utilizations demonstrate the distinct advantages of the proposed H-MMC configuration for HVDC applications in terms of flexible system operation especially during DC fault (commutation failure for hybrid HVDC) conditions.

6.1 Hybrid MMC for DC/DC converters

6.1.1 Introduction

HVDC transmission has become the preferred solution for large-scale integration of renewable energy, especially for offshore wind farms over long distance [FLO2009] [XU2007B]. Of the many technique challenges, the interconnection of DC grids with similar or different voltage levels has become one of the main barriers for the development of large scale HVDC transmission system due to the difficulties in fault handling especially DC faults. To solve such issues, DC/DC converters, as a key component for interconnecting future DC grids, should have the following features: 1) bidirectional power flow; 2) step-up and step-down voltage levels; 3) DC fault blocking [KIS2015].

Due to high-voltage and high-power requirements for the DC/DC converters in HVDC systems, the conventional DC/DC topologies designed for lower or medium voltage and power ranges are unlikely to be suitable for HVDC applications. There are many studies on using two MMCs connected by a medium/high-frequency transformer to compose a DC/DC converter [KEN2011] [KEN2012] [SCH2013] [LUT2014] [KIS2015] [KEN2015]. In [KEN2011], a DC/DC converter formed by two MMCs connected on the AC sides through a transformer was proposed. In case of a DC short circuit on one side, both primary and secondary converters are blocked and the short circuit current through the converters can be avoided. DCDCAlthough such a DC/DC configuration can handle DC fault without additional circuits, it has to block both the primary and secondary side MMCs simultaneously to isolate the fault. For a DC/DC converter with more than two terminals connecting large number of DC grid sections, DC fault on one section will lead to the blocking of all the converters in the DC/DC converter which will affect the power transmission among the healthy DC sections in such a multi-section HVDC interconnection system.

To tackle the above mentioned issues, an improved 3-terminal DC/DC converter based on a simplified H-MMC configuration (the first configuration of the H-MMC in Chapter 5) is proposed for multi-terminal DC grids interconnection. As analysed in Chapter 5, this MMC structure is a simplified configuration based on the half HBSMs and half FBSMs configurationDC. With such advantages, the proposed DC/DC converter can isolate the faulty DC grid section, while continue operating the healthy DC grid sections.

6.1.2 System configuration

Fig. 6.1 presents the proposed three-terminal DC/DC converter interconnecting three independent HVDC grid sections with similar or different voltage levels. DC Grid 1 is connected to an offshore wind farm, while DC Grid 2 and DC Grid 3 are connected to separate AC grids. The 3-terminal DC/DC converter operates as a DC hub in the system to connect and manage power flow among these three DC grids. It comprises three simplified H-MMC based on half FBSMs and half HBSMs configuration with two isolation transformers (or a three-winding transformer shown in Fig. 6.1), as shown in Fig. 6.2(a). In order to reduce the footprint of the transforms, the AC output of the hybrid MMC can be higher than nominal AC system frequencies of 50/60 Hz, e.g. in the range of a few hundred Hz.

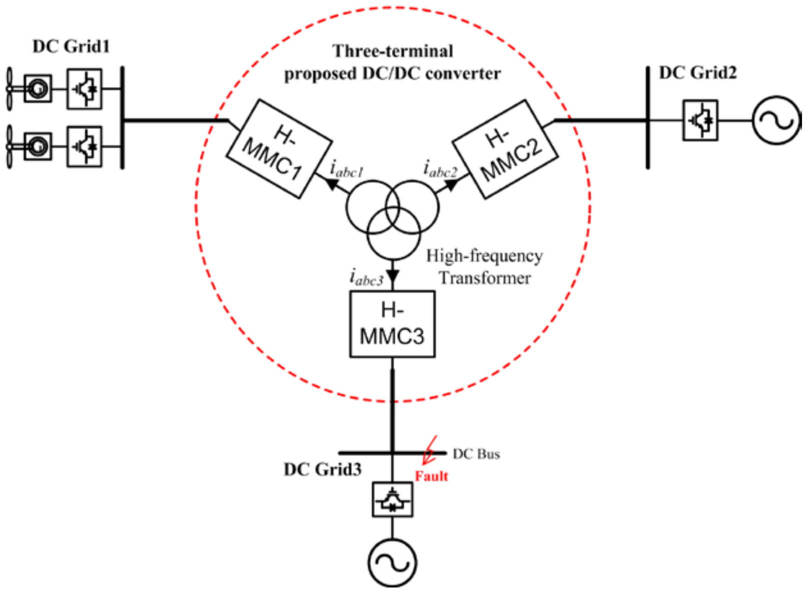


Fig. 6. 1 Layout of a three interconnected DC grids

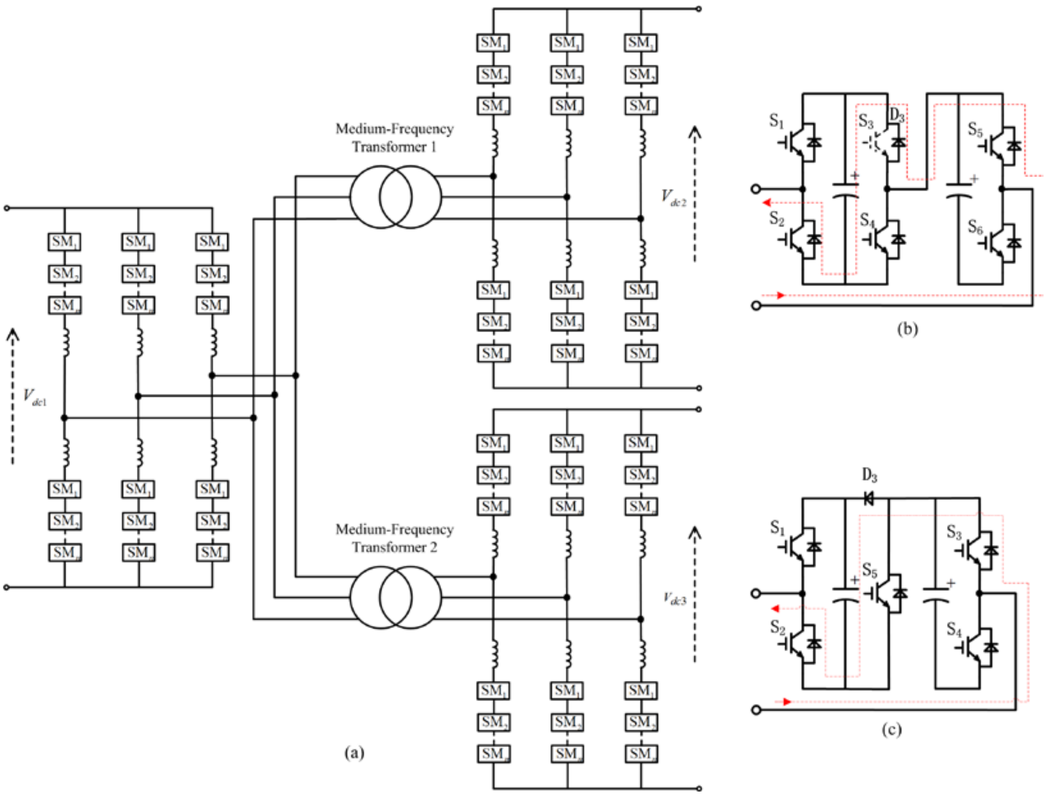


Fig. 6. 2 Configuration of the proposed H-MMC based DC/DC converter

According to the analysis in Chapter 5, this MMC structure has the advantage of inherent DC fault blocking capability. In case of a DC fault happened in one DC grid (i.e. DC Grid 3 in Fig. 1), the H-MMC3 can be blocked and the other two (H-MMC1 and H-MMC2 shown in Fig. 6.1) can continue operating and transmitting power between Grid 1 and Grid 2.

6.1.3 Control strategy for the proposed DC/DC converter

The DC/DC converter is consisted of a number of MMC based DC/AC converters depending on the number of DC terminal required. Among the different MMC converters, one MMC operates as a voltage source to generate a medium-frequency AC voltage for the common AC side and the other converters control their power exchanges between the AC and DC sides so as to control the power flow among the connected different DC sections.

One of the primary requirements for the MMC operating as a voltage source is to generate a medium-frequency AC voltage with constant amplitude and frequency. The schematic diagram of the control strategy for the MMC operating as a voltage source is shown in Fig. 6.3. It is consisted of double control loops, including an outer voltage loop with PI controllers to control the *d*- and *q*- axis voltage space vector, and an inner current loop with PI controllers to track the AC current reference. The d-axis voltage reference V_{id}^{*} is set to be the rated AC peak phase voltage and V_{iq}^{*} is set to be 0. The AC frequency is set to a constant value of f_i. The output of the control scheme is the equivalent phase voltage used to calculate the required arm voltage references.

For the other MMCs, the task is to control the power flows between the local medium-frequency AC voltage and connected DC terminals. The schematic diagram of the control strategy is shown in Fig. 6.4 where reactive power reference (q-axis current) can be simply set to zero. It also includes double control loops, an outer voltage loop with PI controllers to control the active and reactive power tracking the reference value, and an inner current loop with PI controllers to track the AC current references.

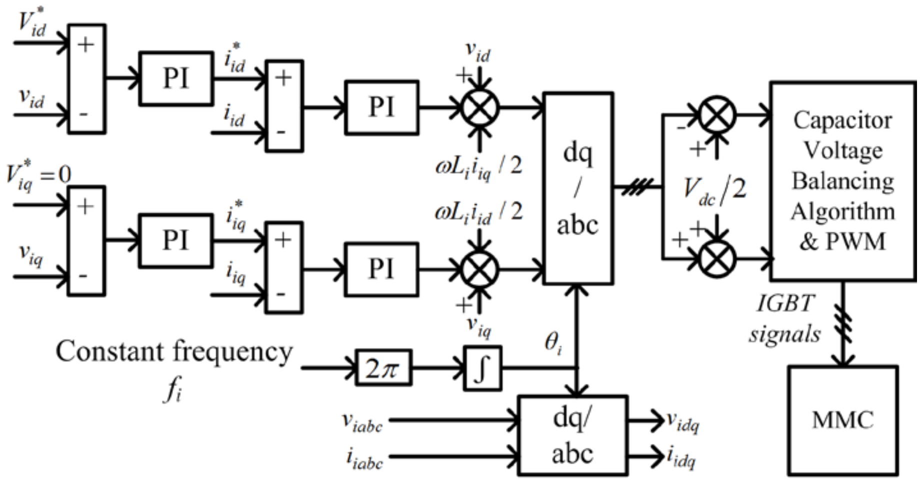


Fig. 6. 3 Schematic diagram of the controller for the MMC operating as a voltage source

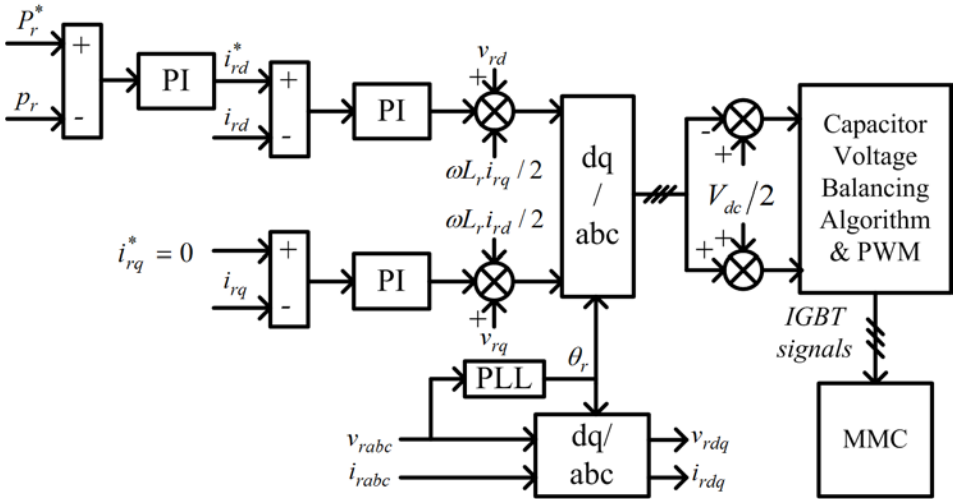


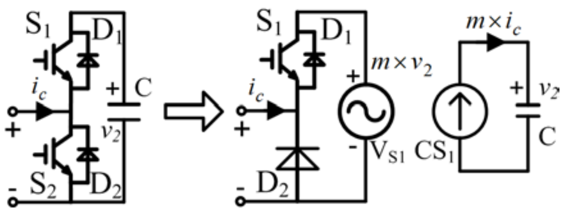
Fig. 6. 4 Schematic diagram of the controller for the other MMC

6.1.4 Converter average model development

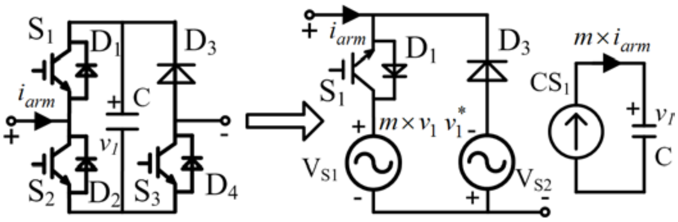
It is known that detailed modelling of the MMCs consisted of large numbers of switching devices, can result in excessive computational complexity and long simulation time. For a multi-terminal interconnected DC grids system, it is not efficient and practical to using detailed models to build the whole system [XU2013B] [LUS2014]. In order to solve this issue, a simplified simulation model using average converter model for the proposed DC/DC converter using H-MMC topology is adopted. The average model replaces the strings of SMs in each arm with a single average value cell as shown in Fig. 6.5. Since the basic building block in the H-MMC can be considered as one simplified FBSM and one HBSM, all SMs in one arm are lumped together and modelled as one FBSM and one HBSM. Fig. 6.5(a) and Fig. 6.5(b) show the average modelling for the HBSM and the FBSM, respectively. The produced arm voltage is represented by one controllable voltage source and one controllable current source, in which the control signals are coupled. The controllable voltage source represents the capacitor voltage, which is fed by a controllable current source representing the arm current flowing through the SM. The reference value for the controllable current source is the product of the arm current and the modulation index *m*. The reference value for the controllable voltage source is the product of the capacitor voltage and the modulation index *m*.

Additional semiconductor devices have been added so that the model can accurately replicate all possible current paths in a real converter during DC faults. As shown in the right hand side of Fig. 6.5 (a), during normal operation in the HBSM, switch S_1 is closed, allowing current to flow in both the positive and negative directions through S_1 or D_1. D_2 is reversely biased and has no effect. For the FBSM average model shown in the right hand side of Fig. 6.5 (b), switch S_1 is closed and D_3 is reverse biased during normal operation. Under DC fault conditions, all IGBTs are blocked in the detailed model, which is replicated by switching off S_1 in the average model and the diode D_3 offers the fault current path. For the FBSM, when switch S_1 switches off, the controllable voltage source V_{S2} (equals v_1) would replicate the blocking voltage formed by the FBSM capacitor voltages.

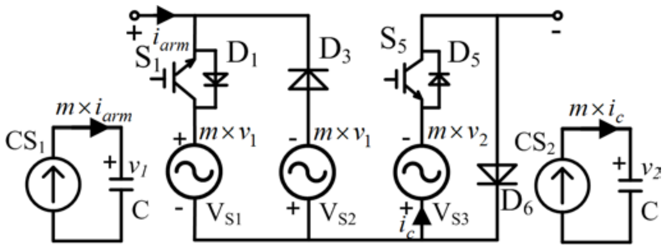
Fig. 6.5 (c) presents the average model of one hybrid SM. In case of a DC fault, all IGBTs are blocked, the fault current bypasses the controllable voltage source V_{S3} (capacitors in the HBSMs) through D_6 but flows through the controllable voltage source V_{S2} and D_3, which matches the characteristics of the actual hybrid SM shown in Fig. 6.2 (c).



(a) Average modelling for the HBSM



(b) Average modelling for the FBSM



(c) Average modelling for the hybrid SM

Fig. 6. 5 Average modelling replacing SMs in each arm of the H-MMC

6.1.5 Simulation studies

To verify the above mentioned configuration and control strategy of the proposed DC/DC converter, a three-terminal DC/DC converter model shown in Fig. 6.1 is developed using Matlab/Simulink. H-MMC1 operates as a voltage source to generate a 400 kV (phase-phase rms.) / 500 Hz AC voltage. H-MMC2 and H-MMC3 control their active power flow to DC Grid 1 and DC Grid 2. The main parameters are listed in Table 6-1. Due to the use of higher frequency, the SM capacitor size can be significantly reduced compared to normal MMC operating at line frequency.

Table 6- 1 Parameters of the simulation Hybrid hvdc system

Items		Values
H-MMC1	Rated power	1000 MW
	AC side voltage	400 kV, 500Hz
	DC side voltage	800 kV
	Number of SMs	320
	Equivalent capacitance per SM	2.1 uF

H-MMC2	Rated power	500 MW
	AC side voltage	300 kV, 500Hz
	DC side voltage	600 kV
	Number of SMs	240
	Equivalent Capacitance per SM	1.8 uF
	Transformer 1	400kV/300kV
H-MMC3	Rated power	500 MW
	AC side voltage	200 kV, 500Hz
	DC side voltage	400 kV
	Number of SMs	160
	Equivalent Capacitance per SM	4.2 uF
	Transformer 2	400kV/200kV

Figs. 6.6-6.7 show the steady-state and dynamic operation of the proposed DC/DC converter. The frequency of the AC voltage generated by H-MMC1 is 500 Hz, and the active power flows from H-MMC1 to H-MMC2 and H-MMC3 with equal sharing. The reactive power at both H-MMC2 and H-MMC3 is set to 0. It can be observed from Fig. 6.6 that the AC voltage generated by H-MMC1 is sinusoidal with constant amplitude and constant frequency, and H-MMC2 and H-MMC3 can

precisely track the reference value of active and reactive power. Under the power step tests, at 0.6s, the active power reference of H-MMC2 decreases from 0.5 p.u. to 0.3 p.u., and the reactive power reference of H-MMC3 increase from 0 to 0.2 p.u.. It can be seen from Fig. 6.7 that H-MMC2 and H-MMC3 can track the change of active and reactive power reference, and H-MMC1 has a corresponding change in the active and reactive power, since the power flow direction is from H-MMC1 to H-MMC2 and H-MMC3.

Fig. 6.8 shows the behaviour of the system under DC fault conditions. When a DC fault occurs at the H-MMC3 side (t = 1.0s), there are large fault current and the DC voltage collapses at H-MMC3 side. This immediately affects the medium-frequency AC voltage generated by H-MMC1 in the transformer and consequently, it can be seen that the AC current and active and reactive power in H-MMC2 side are also affected. The fault is quickly detected and the H-MMC3 is blocked immediately. The fault current i_{abc3} goes to zero quickly and the fault is effectively isolated by H-MMC3. Thus, the other two healthy DC sections connected via H-MMC1 and H-MMC2 continue operating without blocking. It is demonstrated that the proposed DC/DC converter can quickly isolate the local DC fault and keep the other healthy parts of the system without blocking.

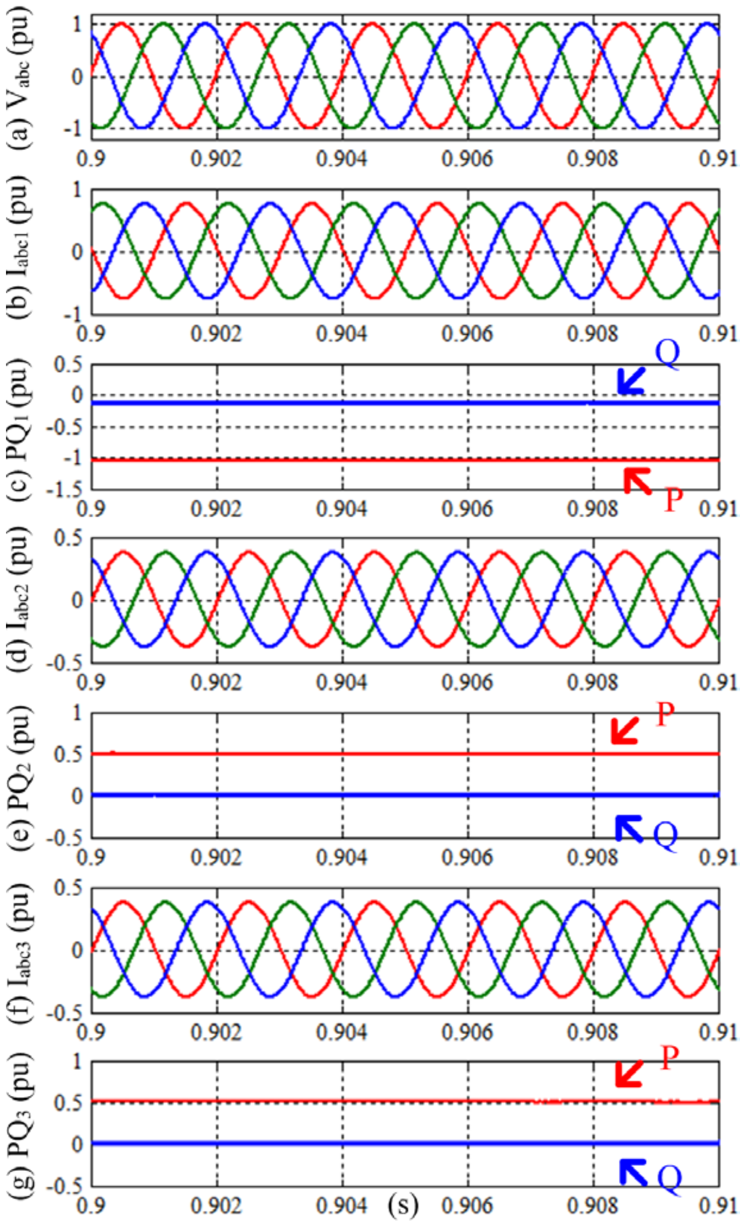


Fig. 6. 6 Simulation results demonstrating the steady-state operation performance of the proposed DC/DC converter, (a) AC voltage at the AC transformer; (b) AC current at H-MMC1; (c) active and reactive power at H-MMC1; (d) AC current at H-MMC2; (e) active and reactive power at H-MMC2; (f) AC current at H-MMC3; (g) active and reactive power at H-MMC3.

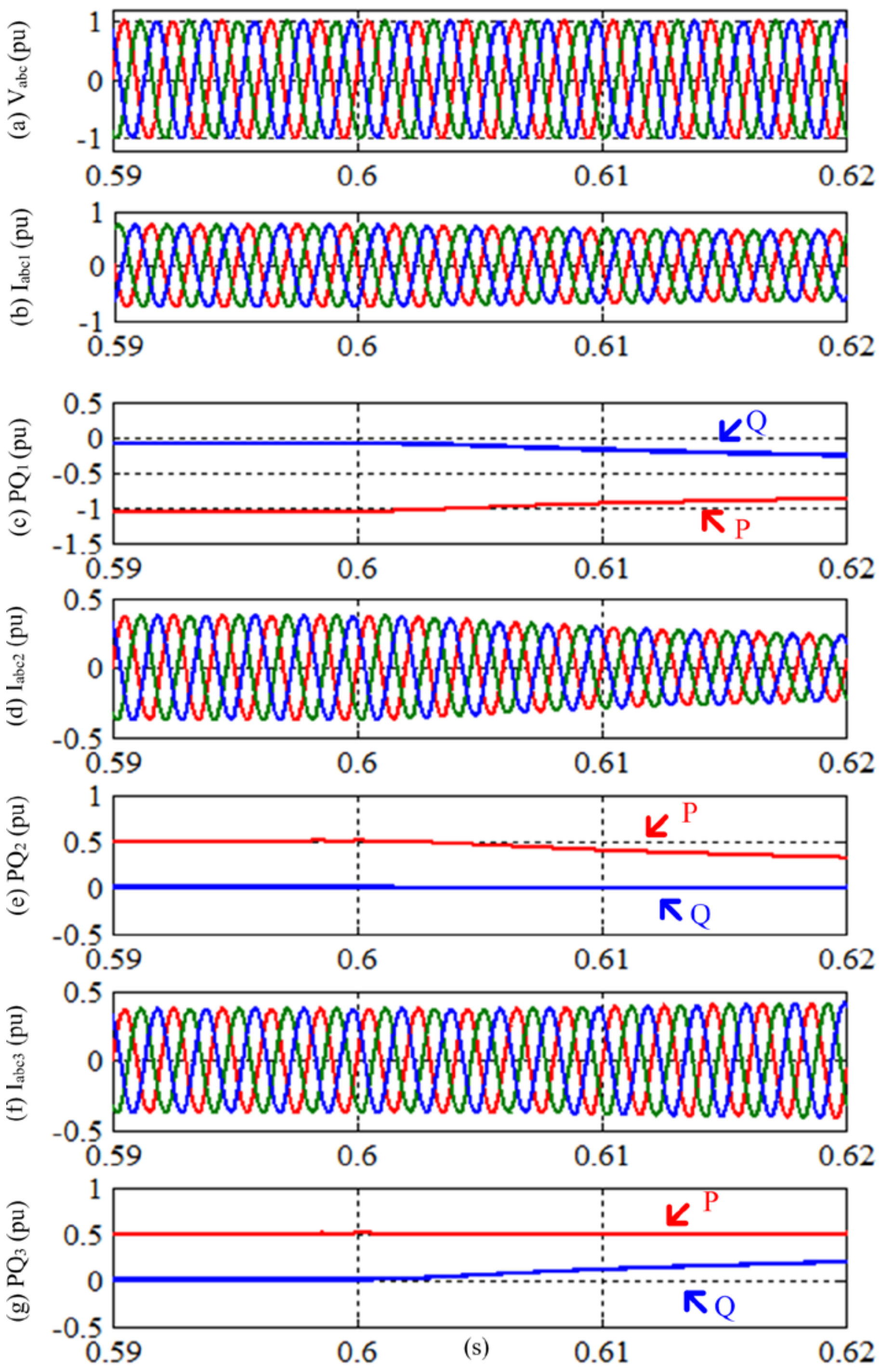


Fig. 6. 7 Simulation results demonstrating the dynamic operation performance of the proposed DC/DC converter, (a) AC voltage at the AC transformer; (b) AC current at H-MMC1; (c) active and reactive power at H-MMC1; (d) AC current at H-MMC2; (e) active and reactive power at H-MMC2; (f) AC current at H-MMC3; (g) active and reactive power at H-MMC3.

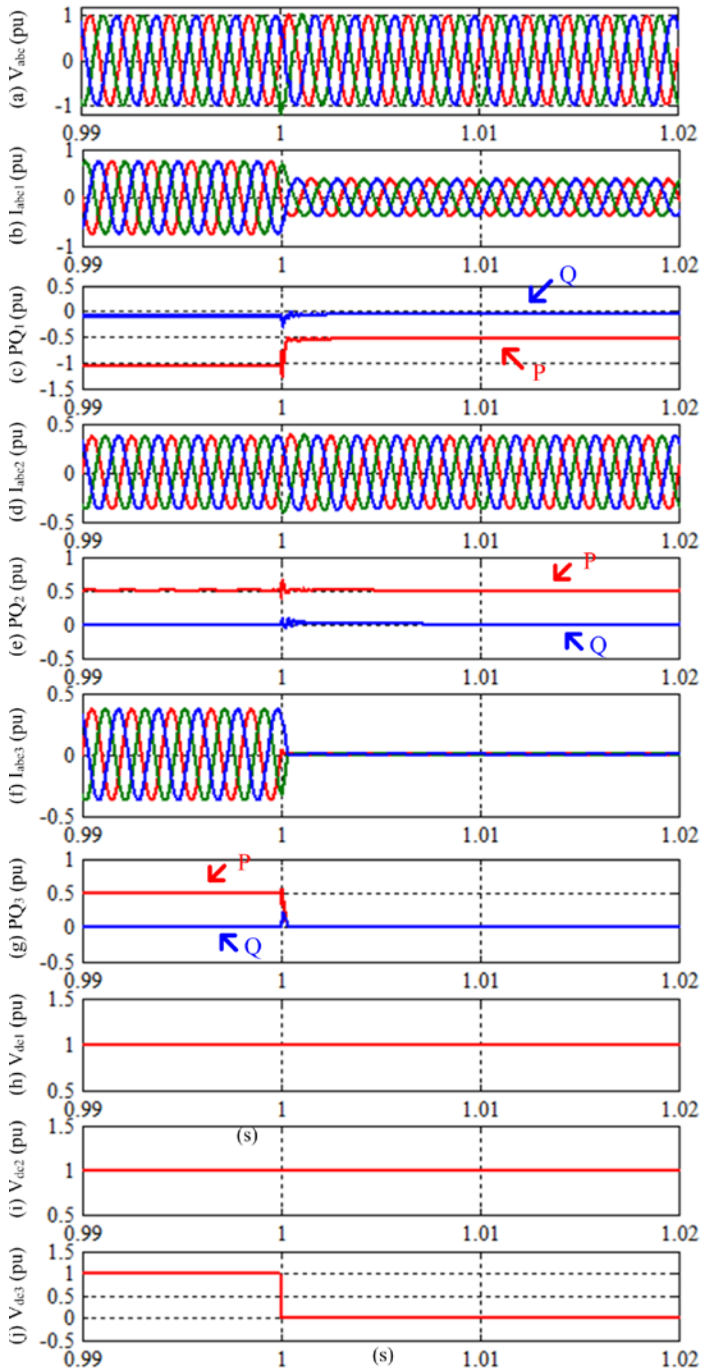


Fig. 6. 8 Simulation results demonstrating the behaviours of the proposed DC/DC converter under DC fault conditions, (a) AC voltage at the AC transformer; (b) AC current at H-MMC1; (c) active and reactive power at H-MMC1; (d) AC current at H-MMC2; (e) active and reactive power at H-MMC2; (f) AC current at H-MMC3; (g) active and reactive power at H-MMC3; (h) DC voltage at H-MMC1; (i) DC voltage at H-MMC2; (j) DC voltage at H-MMC3.

6.2 Hybrid MMC for hybrid HVDC system integrating VSC and LCC

6.2.1 Introduction

It has been widely accepted that VSC based HVDC system using IGBT is the preferred DC technology for connecting wind farms due to its many advantages of independent active and reactive power control, flexible AC system control which is particularly important for offshore wind farms [XU2007B] [XU2008] [FLO2009] [JIN2010] [XU2011B] [JIN2011]. However, the high cost of the VSC technology at very high voltage and high power (above 1 GW) has raised serious concerns. On the other hand, the conventional line commutated converter (LCC) based HVDC system using thyristor has long been used for bulky power transmission and proven to be superior to VSC systems for high power rating in terms of cost and reliability [FOS2008] [SER2008]. However, LCC system requires a relatively strong AC system to operate, is difficult to supply an island network (e.g., offshore wind farm), and requires large footprint (thus difficult for offshore installation).

Considering the advantages of the LCC and VSC systems, a hybrid HVDC system comprising a VSC converter at one terminal and a LCC at the other terminal was proposed as a cost-effective solution for wind farm energy transmission [FUA2005] [PAN2006] [CHE2011B] [ZHO2011] [TOR2012] [TOR2012] [LIU2013] [MAN2013] [ZHA2013] [TAN2014] [ZHA2014] [LI2014A]. Such configuration can also be extended to multi-terminal systems with additional VSC and LCC converters connected to the DC network. A five-terminal hybrid HVDC system was proposed with detailed study on system control and operation [CHE2011B]. But the LCC converter in the proposed system operates as a rectifier connecting the wind farms which becomes less practical due to the various issues previously outlined. A hybrid configuration where the VSC connects the wind farm and the LCC operates as the inverter was presented and studies on system control and operation under normal operation conditions were carried out [LI2014A] [PAN2006]. However, system operation during large transients, e.g. LCC commutation failure due to disturbance in the receiving end AC grid, was not considered. Commutation failure is not a serious issue for LCC HVDC systems due to their nature of being current source, and detailed analysis on mechanism as well as control and protection strategies were well documented [ZHA2002] [HAN2000] [THI1996] [GAL1984]. In the hybrid system, however, a commutation failure in the LCC inverter is equivalent to a short circuit on the DC side, which can result in serious consequences for the VSC on the other terminal due to the existence of the freewheeling diodes.

In [LIU2013], a hybrid HVDC system with a VSC rectifier and LCC inverter was presented. For this structure, the VSC controls the DC voltage and the LCC regulates the DC current control. In order to reduce the probability of commutation failure, the voltage dependent current limit control is added to the LCC inverter. However, this method has two limits. First, an extra communication between the VSC and LCC is needed to request the VSC to reduce DC voltage when disturbance on the LCC AC network is detected. Secondly, the DC voltage margin for the conventional VSC is very narrow, since the VSC needs almost constant voltage to ensure stable operation. Therefore, the effectiveness of this control strategy is largely limited.

The objective of this section is to investigate system behaviour and operation of the hybrid HVDC system, with MMC based VSC connecting wind farms and LCC operating as an inverter feeding power to the AC network. Transient system behaviour during LCC inverter commutation failure which effectively results in a DC line-to-line short circuit is analyzed and control and protection strategies during such event is investigated. Conventional MMC using HBSMs and the proposed H-MMC with mixed HBSMs and FBSMs will be studied.

6.2.2 System configuration

Fig. 6.9 shows the configuration of the hybrid HVDC transmission system. In this example a large offshore wind farm is considered though the concept is also applicable to connecting large remote onshore wind farms which are connected to weak local AC grids. The wind farm side converter uses MMC based VSC (WFVSC) technology as shown in Fig. 6.10 where each arm contains large numbers of SMs [TU2011B]. On the grid side receiving terminal, the converter uses LCC (GSLCC) technology as schematically shown in Fig. 6.11.

The use of MMC based VSC at the wind farm side takes its full advantages of voltage and frequency regulation for the wind farm AC network and independent control of the active and reactive power. On the other side the use of LCC at the receiving AC grid side provides increased system reliability and reduced cost and power loss compared to VSC designs.

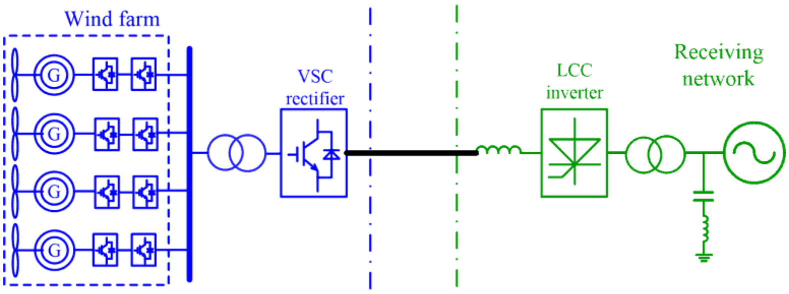


Fig. 6. 9 Layout of the hybrid HVDC transmission system

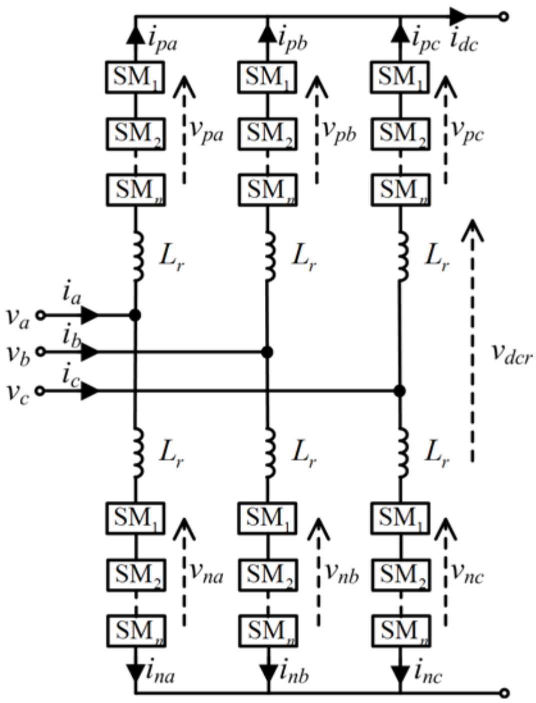


Fig. 6. 10 Configuration of the modular multilevel converter

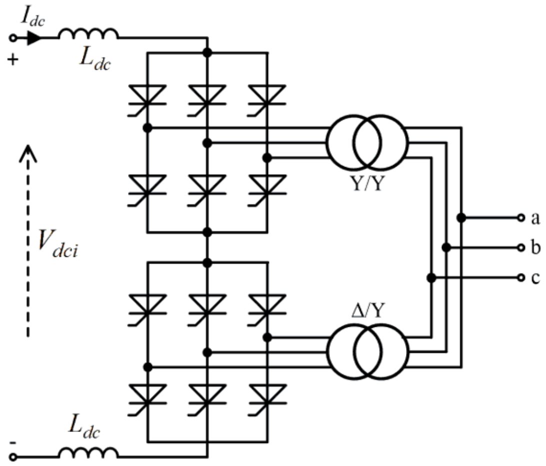


Fig. 6. 11 Configuration of the line commutated converter

6.2.3 Transient behaviour of the hybrid HVDC system

Normal operation of a VSC requires its DC link voltage to be maintained at a near constant value. For the hybrid HVDC system, the GSLCC on the receiving terminal is assigned to control the DC link voltage, to ensure the energy absorbed by the WFVSC is transmitted to the AC grid network. For the case of connecting offshore wind farm, the WFVSC on the sending terminal regulates the AC voltage and frequency of the local wind farm power network to the desirable values and absorbs power generated by the wind farm. For the case of connecting remote onshore wind farms with a weak local AC system, the WFVSC controls active power flow and provides network support to the local AC system, e.g. AC voltage control, network damping etc. The control and operation of the WFVSC [XU2007B] [XU2008] [XU2011] [JIN2011] and the GSLCC [FOS2008] [SER2008] [ZHA2014] on normal conditions have been well understood and no more descriptions are provided here. Similar for the MMC, its control strategy, capacitor voltage balancing algorithm and PWM modulation method all have been well documented [SAE2010] [TU2011B], again no further details are given here.

(A) LCC commutation failure

LCC inverters suffer from commutation failure during AC voltage drop and/or phase shift resulting from transient events on the connected AC network [ZHA2002]. During a commutation failure the DC terminal is effectively short-circuited by the upper and lower arm thyristors on the same converter phase leg. For the hybrid system proposed here, LCC inverter commutation failure and the effective short circuit of the DC side can result in serious consequences for the MMC based VSC on the other terminals due to the presence of their freewheeling diode. Fig. 6.12 shows the equivalent circuit of the hybrid system during inverter commutation failure and after the blocking of the IGBTs in the MMC. As way of example, only one 6-pulse LCC converter is drawn here. For this example, when the LCC inverter fails to commutate resulting in the simultaneous conduction of T_3 and T_6 in the same phase leg, the DC side is short-circuited. The MMC on the wind farm terminal blocks the IGBTs quickly due to over current and/or low DC voltage. However, the diodes (in the example shown, D_1 and D_2) will continue feeding AC fault current into T_3 and T_6. This can not only severely affect the sending end AC network, the MMC and LCC converters, but also makes system recovery from such commutation failure difficult due to the potential large DC fault current flowing through the thyristors in LCC inverter leg. Besides, the blocking of MMC would loss the control for the wind farm AC grid, and the large AC fault current feeding from the wind farm AC grid distorts it voltage waveforms and could lead to wind farm disconnection.

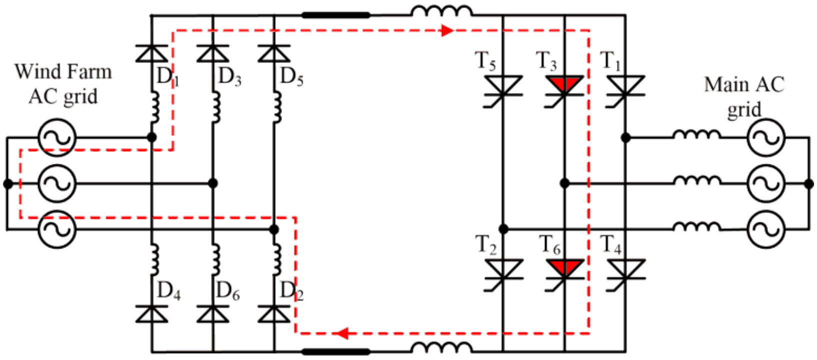


Fig. 6. 12 Equivalent circuit of the hybrid system during inverter commutation failure

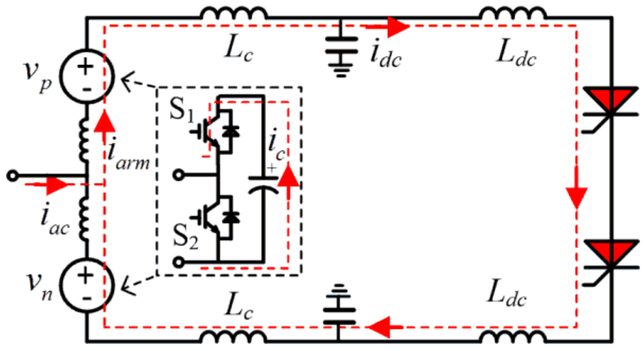


Fig. 6. 13 Simplified equivalent circuit during the fault

To analyse the behaviours of the hybrid HVDC system during commutation failure, two stages are considered.

Stage 1: MMC not blocked

Before the MMC is blocked, the DC cable capacitor and some of the capacitors within the SMs whose S_1 is ON (named as switched-in SM capacitors, see Fig. 6.13 will discharge. As this stage is very short, fault current from AC side is insignificant due to the relatively large transformer leakage impedance and thus, the fault current on the converter arm and DC side is primary due to the DC capacitor discharging. The arm current in the MMC rises quickly and after the fault is detected by over-current on the converter arms and/or DC under voltage, the MMC will be blocked. The system then moves to Stage 2. The simplified circuit during Stage 1 is shown in Fig. 6.13 where the capacitor voltages formed by the switched-in SM capacitors are shown as v_p and v_n for the upper and lower arms, respectively.

Stage 2: MMC blocked

After blocking the MMC, system behaviour can be quite different depending on the configuration of the wind farm AC system. If the wind farm is an offshore island system, the local AC system is usually regulated by the MMC and the blocking of the MMC could lead to the drifting of the AC system frequency and voltage. This could potentially lead to system collapse unless the wind turbines actively takeover the AC voltage and frequency regulation. The system is further complicated by the fact that the MMC acts as an uncontrollable rectifier feeding fault current into the

LCC inverter side where commutation failure occurred. Thus even the wind turbines try to control the local AC system, they are likely to operate in current limit mode and the local AC system voltage will stay low. Under this condition, the fault current will be limited but the wind farm AC voltage will have to be re-established after the LCC recovered from the commutation failure before normal power transmission can be resumed.

If the WFVSC connects to a weak AC network with large onshore wind farms, the blocked MMC simply acts as an uncontrollable rectifier as shown in Fig. 6.12. Large AC and DC fault current will be produced and the wind farm side AC voltage will also be pulled down.

The potential large DC fault current flowing through the DC line from the AC side of the sending terminal could make it difficult for the GSLCC to recover. Thus, commutation failure is a very critical issue for the hybrid HVDC system and the conventional control and protection strategies for LCC based HVDC system are unlikely to be suitable for the hybrid HVDC system.

(B) Control and protection strategies for the hybrid HVDC system

To enhance the operation performance of the hybrid HVDC under the commutation failure conditions, a coordinated control scheme between the WFVSC and GSLCC has to be adopted.

For the GSLCC, a phase-locked-loop (PLL) based AC voltage monitor can be adopted to fast detect the AC voltage disturbance and a corresponding advanced firing angle, derived from the change of AC voltage amplitude and/or phase angle shift, can be added to the normal firing angle to increase the commutation margin so as to avoid potential commutation failure. This scheme can decrease the commutation failure possibility for the LCC inverter [HAN2000]. But the drawback of this method is that advancing the firing angle on the LCC inverter side will decrease the DC link voltage. Large reduction of the DC voltage could lead to the discharging of SMs' capacitors on the rectifier MMC resulting in large DC and arm current, which could lead to converter blocking. So the margin of the allowed DC voltage decrease is relatively small in the hybrid HVDC system, (i.e. 10%), and this would limit the effectiveness of advancing the firing angle.

Under severe AC voltage disturbances, commutation failure will occur and large fault current could continuously flow through the DC line from the WFVSC to the GSLCC side. Under such condition, the primary task is to ensure the LCC to recover from commutation failure as soon as possible.

In order to assist fast system recovery, when commutation failure is detected, a fixed firing angle of 90 degrees is applied to the LCC inverter such that once the AC voltage recovers the LCC system can regain forward voltage blocking and recover from the commutation failure quickly. The normal DC voltage control loop of the LCC can then be enabled to build up the DC voltage again and consequently the DC fault current will diminish. Normal system operation can be resumed by enabling the WFVSC. However, for offshore wind farm case, if the wind farm side AC system has collapsed, a restarting sequence will have to be implemented before normal power transmission can be resumed which means a prolonged system outrage will be experienced.

6.2.4 Alternative MMC topology for the hybrid HVDC system

As discussed earlier, although the GSLCC can recover from commutation failure, the main problem is the disruption caused to the wind farm AC network which could lead to the collapse of the offshore AC system and result in the disconnection of the wind farms.

To tackle this issue, a H-MMC topology combining HBSMs and FBSMs is adopted as the WFVSC, and its configuration is shown in Fig. 5.1. The H-MMC can not only isolate the DC side fault, but also continue operating at reduced DC voltage, or even zero DC voltage condition. With such advantages, the coordinated control for the hybrid HVDC system can be more flexible and the impact on the wind farm AC system during inverter commutation failure can be minimized. The coordinated control system for the new hybrid HVDC system involves the following two steps.

- When an AC voltage disturbance at the LCC side is detected, an advanced firing angle can be added for the LCC to increase the commutation margin, resulting in reduced DC voltage and consequently the DC current rises quickly.

- The hybrid based WFVSC will then operate at reduced DC voltage conditions to restrain the DC current rise. It also continues regulating the active and reactive power (or AC voltage and frequency) of the wind farm AC network.

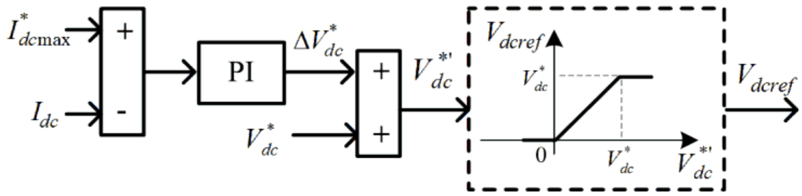


Fig. 6. 14 Schematic diagram of the controller for the maximum DC current

To achieve this target, a closed-loop controller for the maximum DC current is added to limit the DC current rise by regulating the DC voltage in the H-MMC on the wind farm side. The schematic diagram of the controller is shown in Fig. 6.14, where $I^*_{dc\max}$ is the maximum DC current reference during fault, I_{dc} is the measured DC current, and V^*_{dc} is the rated DC voltage. The saturation function of V_{dcref} is used to limit the reference of DC voltage ranging from 0 to rated value, which means the controller is non-functional when the DC current is lower than the maximum DC current reference. Under normal operation, since the actual DC current is less than $I^*_{dc\max}$, this control loop has no effect and the DC voltage is purely controlled by the LCC. However, when DC over-current occurs due to reduced DC voltage on the LCC inverter side, this control loop will limit the DC current to the preset maximum value by reducing the MMC output DC voltage accordingly. Under such operating conditions, the voltages on the AC and the upper and lower arms (taking phase *a* as an example), and the DC side are given as

$$v_{pa} = \frac{1}{2}V_{dcref} - V_a \sin(\omega t), \quad v_{na} = \frac{1}{2}V_{dcref} + V_a \sin(\omega t) \tag{6.1}$$

$$v_{an} = \frac{v_{na} - v_{pa}}{2} = V_a \sin(\omega t) \tag{6.2}$$

$$V_{dc} = v_{pa} + v_{na} = V_{dcref} \tag{6.3}$$

where V_a refers to the required phase a peak AC voltage from the MMC, v_{pa} and v_{na} represent the upper arm voltage and lower arm voltage, as shown in Fig. 5.1, respectively.

As can be seen from (6.3), the DC voltage drops according to V_{dcref} and the MMC continues controlling the wind farm AC voltage as v_{an} is not affected. Obviously the MMC is not able to transmit active power during zero DC voltage and therefore, wind farm de-loading process will need to be implemented. Due to the limited DC fault current (i.e., to the value of $I^*_{dc\max}$, say 1.3 p.u.) and the decrease of the DC voltage, the GSLCC can be prevented from commutation failure or can recover from commutation failure quickly. After the recovery of the inverter side AC voltage, the GSLCC returns to the normal control of DC voltage by increasing its firing angle. Consequently, the DC voltage rises and the DC current decreases. The DC voltage loop at the WFVSC terminal ceases action due to the reduced DC current and switches back to normal active power control.

6.2.4 Simulation studies

To verify the above analysis of the behaviours of the hybrid HVDC transmission system, a two-terminal hybrid HVDC system model configured as symmetrical monopole with one MMC based rectifier terminal and one LCC inverter terminal is developed using Matlab/Simulink, as shown in Fig. 6.15. The rectifier MMC adopts two configurations, i.e., conventional HBSM based MMC and the H-MMC illustrated in Fig. 5.1. The wind farm is considered as connected to a weak AC network with a SCR of 3, and the LCC uses a 12-pulse three-phase bridge structure. The main parameters of the hybrid HVDC system are listed in Table 6-2.

Table 6- 2 Parameters of the simulation hybrid HVDC system

Item	Values

System rated power	1000 MW
DC rated voltage	±450 kV
Wind farm AC network	400 kV / 50 Hz / SCR=3
Main AC grid network	400 kV / 50 Hz / SCR=5
LCC DC smooth reactor	0.5 H
MMC arm reactor	60 mH

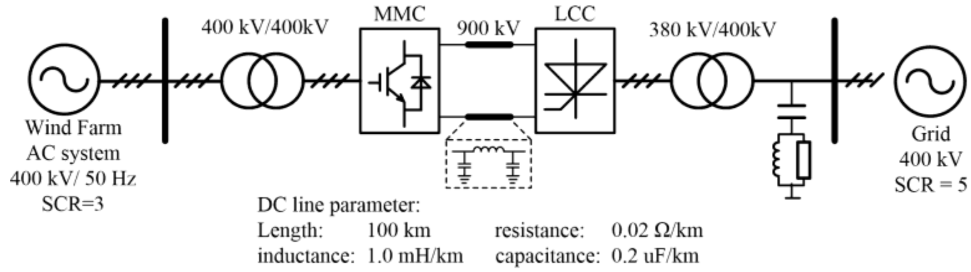


Fig. 6. 15 Structure of the simulated hybrid HVDC configuration

To illustrate the operation characteristics of the hybrid HVDC system under normal and fault conditions, simulation studies are carried out and the results are presented in Figs. 6.16-20. For the results shown in Figs. 6.16-17, the hybrid HVDC system operates at the steady-state and dynamic normal conditions, with the GSLCC controlling the DC voltage to the rated value, and the WFVSC regulating the active power and reactive power on the wind farm AC grid. In Fig. 6.17, at 1.5s, the transmitted power is ramped down from 1.0 p.u. to 0.5 p.u.. As can be seen that the DC voltage is well controlled during power variation and the operation of the system is satisfactory.

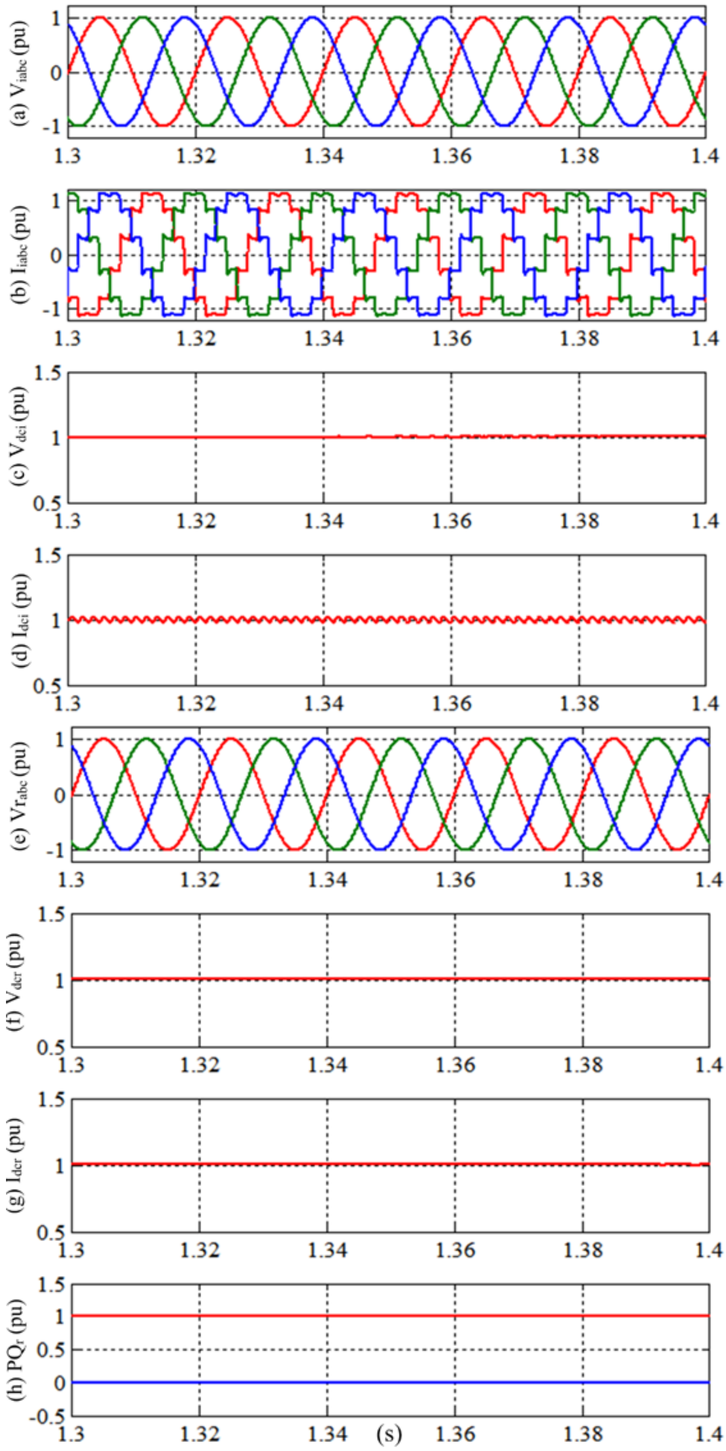


Fig. 6. 16 Steady-state normal operation of the hybrid HVDC system, (a) AC voltage at the GSLCC side; (b) AC current at the GSLCC side; (c) DC voltage at the GSLCC side; (d) DC current at the GSLCC side; (e) AC voltage at the WFVSC side; (f) DC voltage at the WFVSC side; (g) DC current at the WFVSC side; (h) active and reactive power at the WFVSC side.

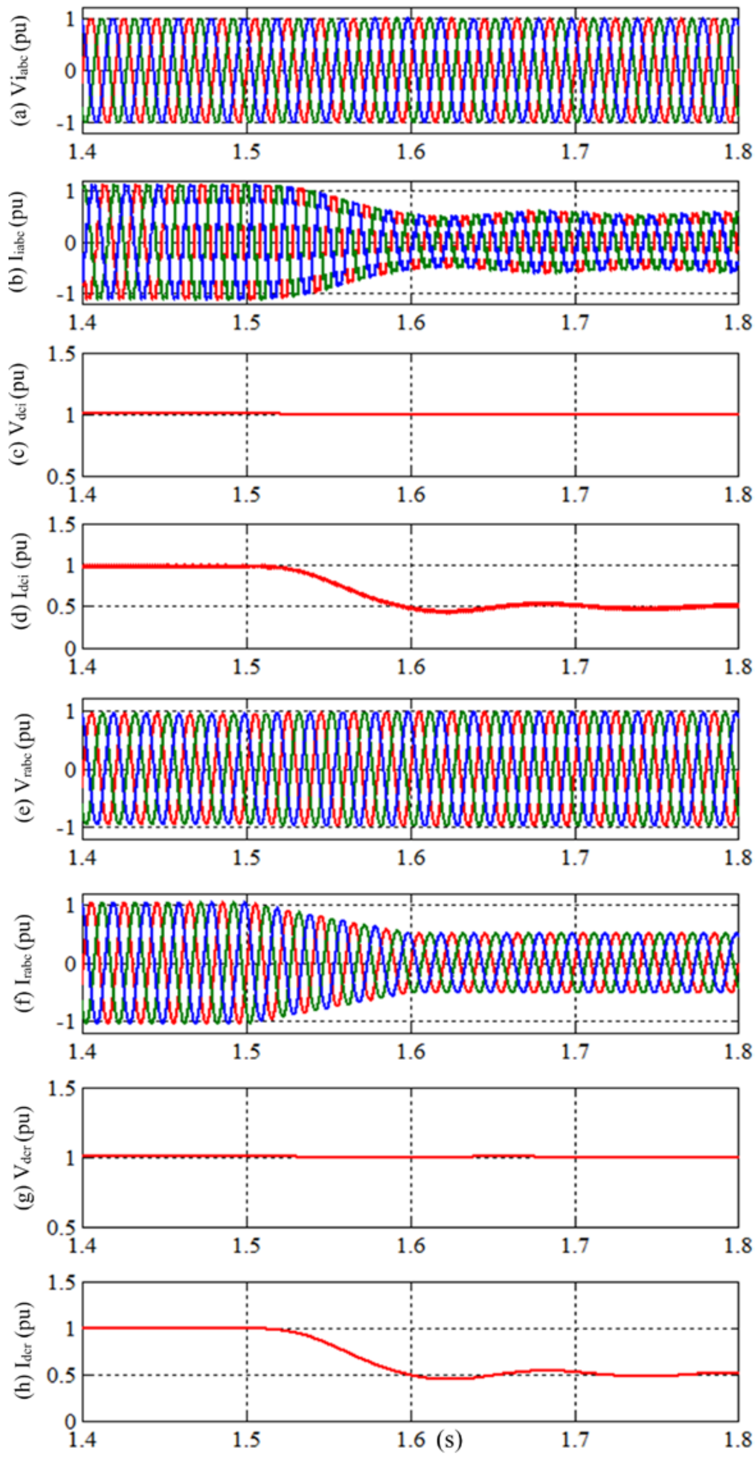


Fig. 6. 17 Dynamic normal operation of the hybrid HVDC system, (a) AC voltage at the GSLCC side; (b) AC current at the GSLCC side; (c) DC voltage at the GSLCC side; (d) DC current at the GSLCC side; (e) AC voltage at the WFVSC side; (e) AC current at the WFVSC side; (g) DC voltage at the WFVSC side; (h) DC current at the WFVSC side.

At 1.5s, a 60ms AC fault happens at the receiving power grid, resulting in a drop of three-phase AC voltage from 1.0 p.u. to 0.5 p.u. Fig. 6.18 shows the response of the conventional half-bridge MMC and GSLCC without using firing angle advancing control. When the fault occurs, LCC fails commutation and results in the short circuit of the DC link. Consequently the DC voltage collapses to near zero and the DC current rises immediately. The MMC immediately experiences over-current and is blocked 20μs after the occurrence of the commutation failure. At this point, the MMC is equivalent to a three-phase uncontrolled rectifier. The DC current continuously increases to 6 p.u. with significant oscillations. The current at the WFVSC AC side also increases, resulting in reduced AC terminal voltage. In addition, as can be seen, after the clearance of the inverter AC fault and the recovery of the AC voltage, the GSLCC fails to recover from the commutation failure due to the large DC fault current.

Fig. 6.19 shows the behaviours of the hybrid HVDC system with the firing angle advancing control under a more severe AC fault which reduces the AC voltage to 0.2 p.u.. Commutation failure occurs after the AC fault, the MMC on the wind farm side has to be blocked and an uncontrollable DC current (4 p.u.) flows through the DC line during the fault period. The firing angle of the LCC is advanced to 90 degrees after the detection of commutation failure, such that the GSLCC recovers from the commutation failure after the fault clearance and the disturbance caused to the wind farm side AC system is less severe compared to those shown in Fig. 6.18.

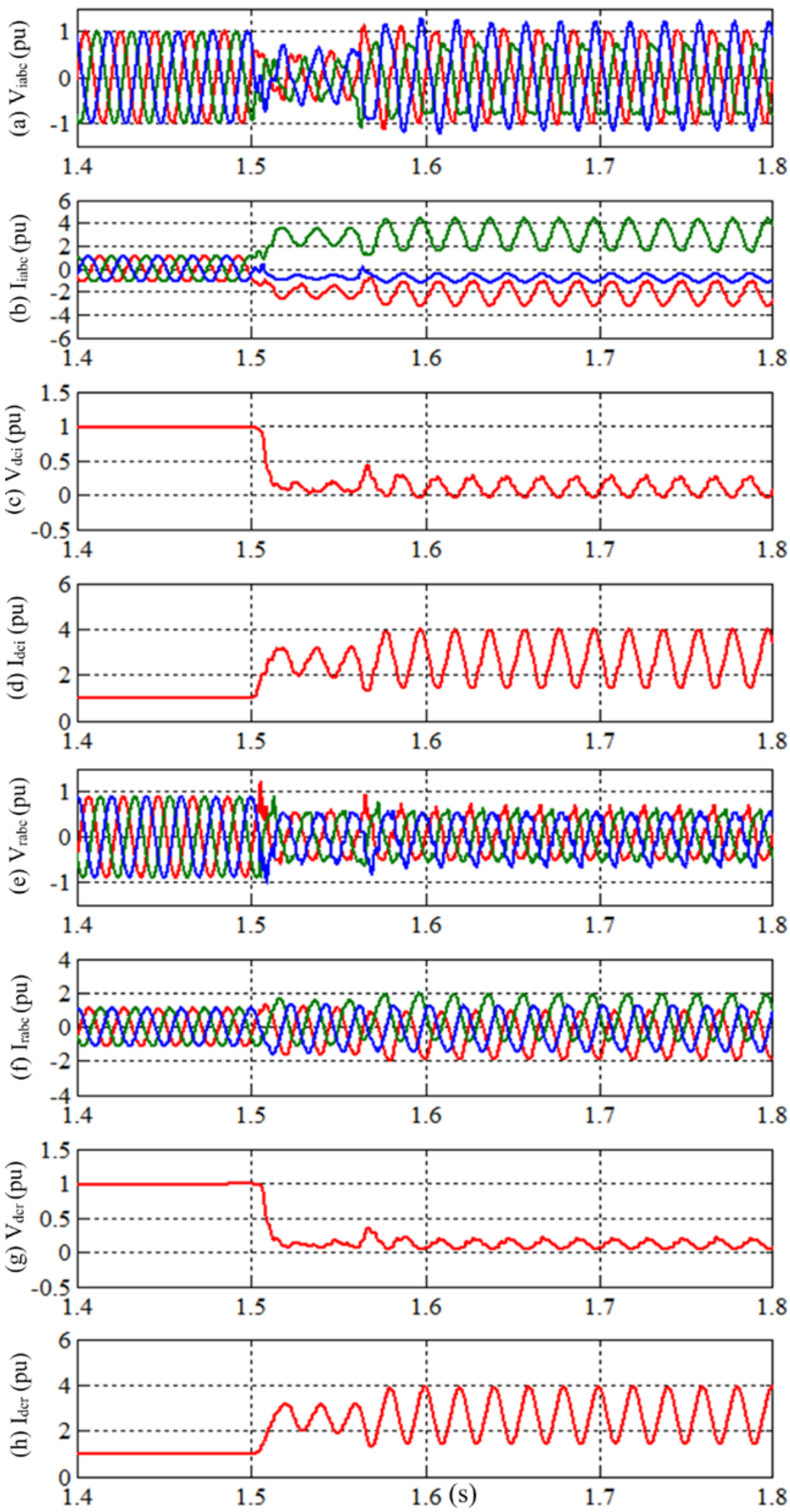


Fig. 6. 18 Conventional MMC based WFVSC and GSLCC without the firing angle advancing control during AC fault.

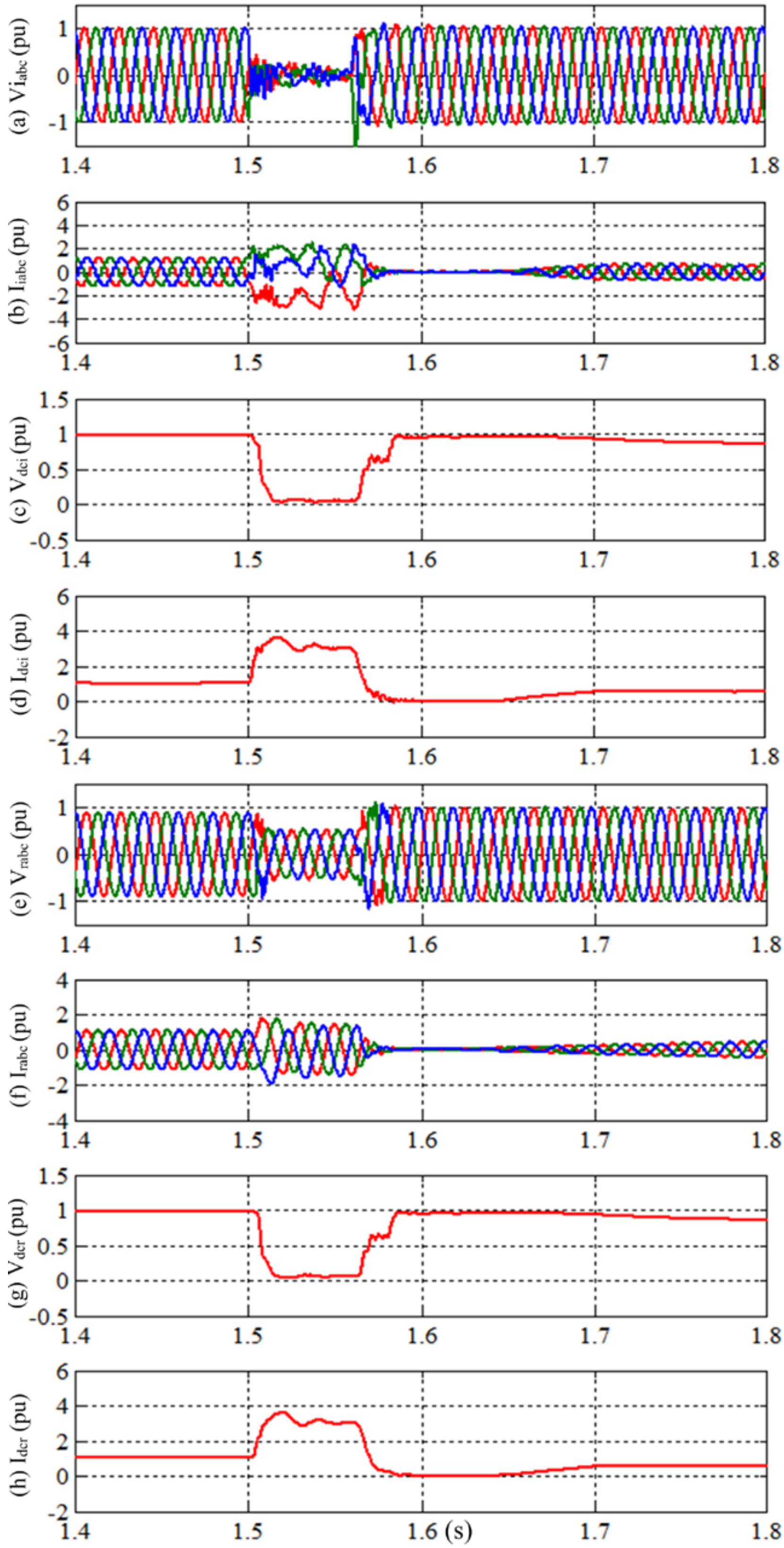


Fig. 6. 19 Conventional MMC based WFVSC and GSLCC with firing angle advancing during AC fault.

Fig. 6.20 shows the results of the hybrid HVDC system with the hybrid MMC configuration. Under the same severe AC fault at 1.5s, the firing angle of the GSLCC is quickly advanced, which results in the reduction of the DC voltage at the LCC inverter side as can be seen from Fig. 6.20 (c). Consequently, the DC current rises and hits the 1.3 p.u. limit set by the maximum DC current controller of the hybrid MMC on the rectifier side, shown in Figs. 6.20 (d) and (h). Thus, the DC voltage of the hybrid MMC decreases automatically to restrain the DC current to around 1.3 p.u.. The AC current on the WFVSC (hybrid MMC) shown in Fig. 6.20 (f) reduces accordingly due to the reduction of active power transfer but remains being fully controlled. Due to the reduction of the DC voltage and current, commutation failure is being prevented in this study. After the fault clearance, the DC voltage at the LCC inverter terminal rises and the DC current drops. The maximum DC current controller automatically moves out of action and the system quickly returns to normal operation. Throughout the whole process, the effect on the wind farm AC network is only on the reduction of active power transmission. This can be particularly beneficial for offshore wind farms since potential AC voltage collapse can be completely avoided and the reduction of transmitted active power transmission can be compensation at turbine level. The simulation results verify excellent fault ride-through performance of the hybrid HVDC with the hybrid MMC based WFVSC and the proposed control strategy.

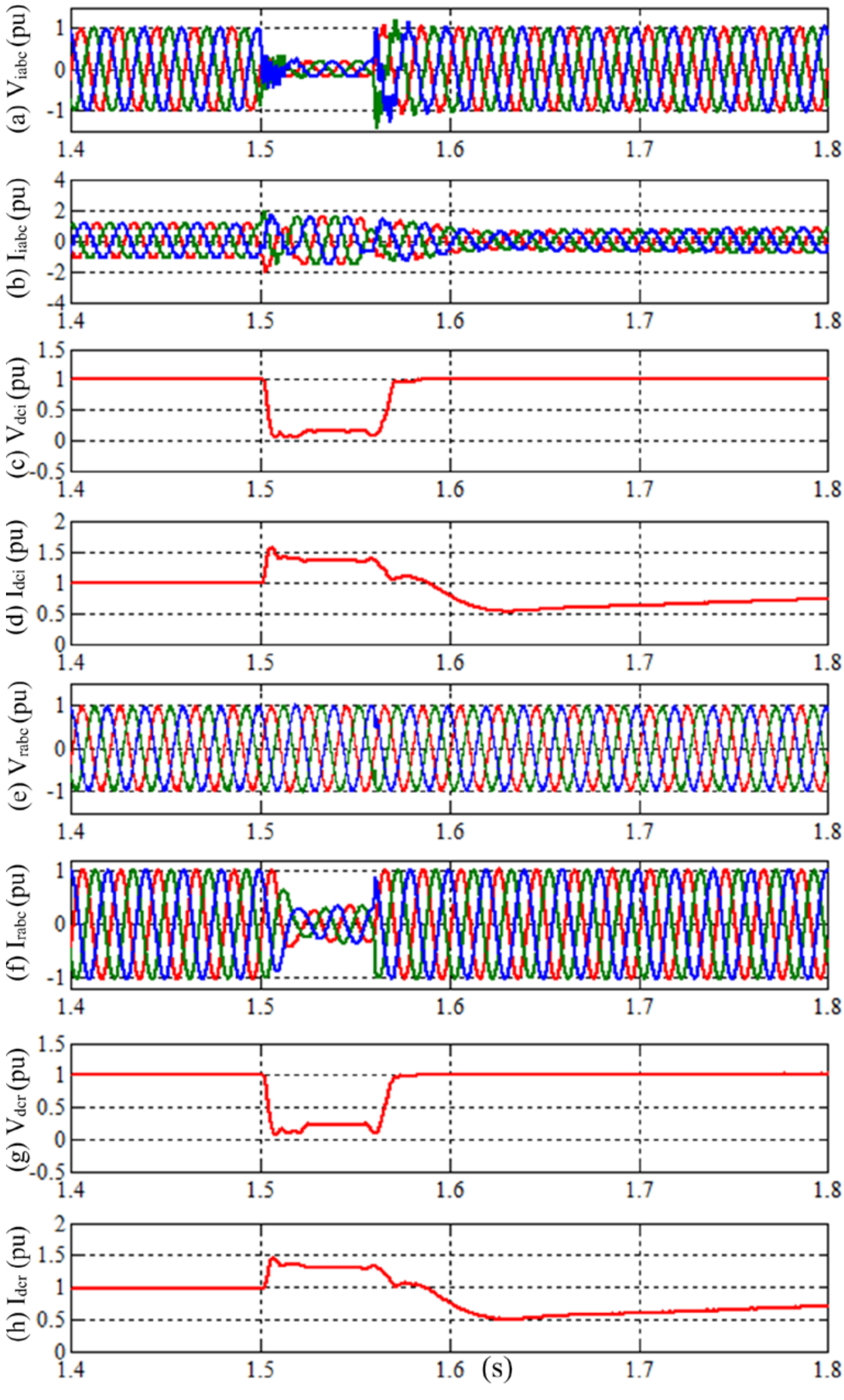


Fig. 6. 20 Hybrid MMC based WFVSC and GSLCC during AC fault

6.3 Summary

This chapter presents two different applications using the proposed H-MMC, taking its advantages of flexible operation under DC fault conditions.

In the first section, a multi-terminal high power DC/DC converter based on hybrid MMC topology with fault blocking capability for interconnecting large HVDC systems is studied. The configuration and control strategy for the proposed DC/DC converter are presented. The proposed DC/DC converter is able to continue operating the healthy parts of the DC grid system rather than blocking the complete DC/DC converter in the conventional MMC-based DC/DC converter system. Simulation results using a 3-terminal DC/DC converter connecting three separate DC grid sections are presented to demonstrate the robust performance of the proposed configuration during a DC fault on one DC network section.

Hybrid HVDC transmission system comprising a VSC based rectifier and a LCC inverter for wind farm integration has also been studied in the second section. The principles of the presented system operation and control have been described. Since the LCC operates as an inverter, impacts of commutation failures on the hybrid HVDC system have been analysed and relevant control and protection strategies have been investigated. Commutation failures in the LCC result in large fault current on both the MMC and DC side and cause large disturbances to the sending end AC system. System recovery after the clearance of the LCC AC grid fault could also be jeopardized. Advancing the LCC firing angle during fault helps the hybrid HVDC system to recover quickly after the fault clearing, but the remaining issues of large uncontrollable DC current and disturbance to the wind farm AC system still exist. To further solve these issues, the previously proposed hybrid MMC topology with capability of operating at reduced DC voltage is adopted and the corresponding coordinated control strategy for the hybrid HVDC system is proposed. The simulation results demonstrate the distinct advantages of this scheme in terms of response and protection during the receiving end AC grid fault and quick recovery after fault clearance.

Chapter 7

Conclusion and future work

7.1 General conclusions

The thesis focuses on the analysis, design, and operation of MMCs for HVDC applications. A comprehensive overview of the recent research work on the characteristics and operation performance of MMCs has been carried out. Based on the general review, the basic operation principles for the conventional MMC using HBSM and FBSM have been introduced. The use of negative output voltage state of the FBSM in the FB-MMC, named the boost FB-MMC has been investigated. The principle of the scheme is to make some of the FBSMs in each arm generate the negative voltage state so as to alter the voltage relationship between the DC and AC sides. It was found that under the same DC voltage conditions, using the proposed scheme can increase the AC output voltage by 100% if the numbers of SMs are increased by 50%. Since the modulation index, arm current and DC current in the FB-MMC with the negative voltage state are different to those in the conventional method without the negative voltage state, a detailed analysis on the links between capacitor voltage variation and the maximum modulation index, and the DC fault blocking capability for the FB-MMC with the negative voltage state was conducted. It was found that in order to keep capacitor voltage balanced, the number of FBSMs allowed to generate the negative voltage state should be less than one third of the total number of FBSMs in one arm. In addition, although the AC voltage is increased by the proposed scheme, the boost FB-MMC still has the DC fault blocking capability. The boost FB-MMC is compared to the conventional FB-MMC and HB-MMC in terms of number of power semiconductors and power losses. It was found that the boost FB-MMC employs 33.5% less number of power semiconductors than that of conventional FB-MMC for the same power rating. It also should be noted that the HB-MMC is the most efficient among these three types of MMC, but the boost FB-MMC is more efficient than the FB-MMC.

The operation of MMC under asymmetrical arm impedance conditions has been investigated. Unlike asymmetric conditions, the fundamental AC current is not split equally between the upper and lower arms, and the DC and double-frequency components in the common-mode current can also flow into the AC side. Theoretical analysis using equivalent circuits at different frequencies was carried out, and the impacts of asymmetrical conditions on the differential-mode current, the common-mode current and capacitor voltages, was investigated. It was found that the following potential issues existed under the asymmetrical arm impedance which can significantly affect MMC system operation: (1) unequal fundamental current distribution in the upper and lower arms, and the existence of fundamental current ripple on the DC side; (2) existence of second order harmonic current on the output AC and DC sides; (3) unequal energy in the upper and lower arms which results in SM capacitor voltage divergence between the upper and lower arms. Thus, to maintain stable operation of the MMC under asymmetrical conditions, three control targets need to be achieved: (1) ensure equal split of the AC fundamental frequency current between the upper and lower arms; (2) eliminate the second order harmonic current in the differential-mode (AC output) current; and (3) regulate the DC common-mode current to maintain balanced power between the upper and lower arms. To fulfil these three control targets, an improved control strategy was proposed, involving three controllers: differential-mode current, common-mode current and power balance controllers. Both simulation and experimental results show the effectiveness of the proposed strategy.

Conventional MMC topologies using HBSM or FBSM have their own critical drawbacks, i.e. the HB-MMC does not have DC fault blocking capability, while the FB-MMC doubles the number of SM power devices with increased power loss. Thus, an improved Hybrid MMC configuration consisting of FBSMs and HBSMs is proposed, which has the same DC fault blocking capability but uses fewer power devices and has less power loss than the FB-MMC. To increase power transmission capability of the proposed H-MMC, negative voltage states of the FBSMs are adopted to extend the output voltage range. In contrast to FBSMs that can charge and discharge their SM capacitors without having to change the external current direction, HBSM capacitors can only be charged during the arm current flowing into the capacitors and discharged during the arm current flowing out the capacitors. As the number of FBSMs generating the negative voltage state increases, the relationships among the AC voltage, DC voltage, and DC current also change. Thus it is necessary to analyse the impact of the number of FBSMs generating the negative voltage state on the charging and discharging times for the SM capacitors. It was found that for the H-MMC, the number of FBSMs generating the negative voltage state must not be greater than one third of the total number of SMs in each arm, in order to ensure sufficient charging and discharging times for the HBSMs to balance their capacitor voltages within each fundamental period. The other design principle of the H-MMC is to consider the DC fault blocking capability. It was found that, to successfully block DC faults, the total number of FBSMs in each arm has to be greater than 43.3% of the sum of the total number of SMs in the arm plus the number of FBSMs in the arm generated the negative voltage state.

Based on the above mentioned these two design principles, two specific configurations of the H-MMC are proposed. The first configuration of the H-MMC is consisted of half HBSMs and half FBSMs and no $-V_c$ voltage state is used for the FBSMs, and the second configuration of the H-MMC is consisted of one-third HBSMs and two-third FBSMs, in which only one-third FBSMs are allowed to generate the negative voltage state. These two H-MMC configurations are compared to the conventional HB-MMC and FB-MMC in terms of number of power semiconductors and power losses. For the number of power semiconductor devices, the first H-MMC configuration uses 50% more and the second one only has 25% increase compared to HB-MMC. This indicates that the proposed H-MMC system can provide DC fault blocking capability without significantly increasing the total semiconductor devices. In comparison on power losses, the conventional HB-MMC is the most efficient among the four MMC types. The proposed H-MMCs are shown as more efficient than the conventional FB-MMC due to the reduced switch number, hence conduction loss.

Due to the use of the negative voltage state for some FBSMs in the second H-MMC configuration, an equivalent circuit for the hybrid MMC was proposed, which considers each arm to be consisted of two series-connected voltage sources. This model was used to analyse SM capacitor voltage balancing and ripple. To ensure capacitor voltage balancing among the SMs, a two-stage selection and sorting algorithm was developed.

When the arm current flows from the negative terminal of a SM (i.e., current flow from AC to DC), only the capacitor in the FBSM is charged while the capacitor in the HBSM is bypassed when all IGBTs are gated off. Thus, pre-charging the proposed H-MMC has a unique issue of unbalanced charging among the HBSMs and FBSMs. In order to solve this issue, a new pre-charging method was proposed for the H-MMC, in which the FBSMs and HBSMs in each arm are arranged into different groups, and then conduct the pre-charging process group by group until all the groups complete.

One significant advantage of the proposed H-MMC is the ride-through capability under a transient DC fault. By using the negative voltage state of the FBSMs, the SMs can generate negative arm voltage. In such a way, the H-MMC can continue operating under reduced DC-link voltage (even zero DC-link voltage conditions). This means the H-MMC can not only block DC fault, but also continue operating to regulate its output AC current, e.g. to support the healthy AC grid and to provide fast fault recovery and system restart.

With the distinct advantages of the proposed H-MMC on the DC fault ride-through capability, two system configurations making use of the proposed H-MMC were presented. One application is a multi-terminal high-power DC/DC converter configuration with fault blocking capability for interconnecting multi-terminal HVDC systems. In contrast to the conventional MMC based DC/DC converter consisting of two MMCs connected on the AC sides through a medium-frequency transformer, the proposed DC/DC converter with H-MMC configuration has the advantage of being able to block the DC/DC converter terminal connected to faulty DC grid section, while continue operating the other terminals connected to healthy DC grid sections. The second configuration is a hybrid HVDC system for integrating large wind farms comprising a wind farm side VSC based on the proposed H-MMC and a grid side LCC. Such configuration combines the advantages of both VSC and

LCC, as VSC is suitable to connect wind farm into main grid, and LCC is cost-effective, which bring benefits of reduced device cost and power losses. Besides this configuration can also be extended to multi-terminal systems with new VSC and/or LCC converters added to existing HVDC networks. For example, in China significant numbers of LCC HVDC systems are already in operation and a VSC converter could be added for integrating a new wind farm with the DC side connected to existing HVDC networks to form a large hybrid multi-terminal HVDC system. Since the LCC operates as an inverter, commutation failure is prone to occur which effectively results in DC short circuit and is equivalent to a pole-to-pole DC fault for the VSC. Taking the advantages of the H-MMC capable of operating at reduced DCor even zero DC voltage condition, a coordinated control strategy for the hybrid HVDC system was proposed to improve its transient response under commutation failure conditions. When an AC voltage disturbance at the LCC side is detected, an advanced firing angle is added for the LCC to increase the commutation margin, resulting in reduced DC voltage and consequently the DC current rises quickly. The H-MMC based WFVSC will then reduce its DC voltage to restrain the DC current rise using a closed-loop DC current controller but continues regulating the active and reactive power (or AC voltage and frequency) of the wind farm AC network.

Extensive simulation and experiment results were presented to verify all the proposed analysis, modelling and control methods. Simulation was mainly carried out using Matlab/Simulink software, and experiment results were taken from a 400W single-phase MMC platform with three SMs in each arm. Closely matching analysis, simulation and experiment results have demonstrated the validity of the proposed topology and control strategy in the thesis.

7.2 Author's contributions

The thesis contains the following main contributions:

- A boost FB-MMC adopting negative voltage state in the FBSMs under normal operation has been discussed to increase power transmission capability, and a detailed analysis on the link between capacitor voltage variation and the maximum modulation index considering the negative voltage state of the FBSM has been conducted.

- A control strategy for MMC under asymmetrical arm impedance conditions has been proposed. Equivalent circuits of the asymmetrical MMC were presented, and detail analysis of the impact of asymmetrical conditions on the differential-mode current, the common-mode current and capacitor voltages, was performed. Based on the analysis, an improved control strategy was proposed for controlling the differential-mode current, common-mode current and power balance.

- A hybrid MMC combining FBSMs and HBSMs has been proposed. The proposed topology has the same DC fault blocking capability but uses fewer power devices hence has lower power losses. Two-stage selecting and sorting algorithms for ensuring capacitor voltage balancing have been developed. The pre-charging process and transient DC fault ride-through capability are investigated for the hybrid MMC.

- A multi-terminal high-power DC/DC converter configuration based on the hybrid MMC topology with fault blocking capability for interconnecting HVDC systems has been proposed. By contrast to the conventional MMC based DC/DC converter, the proposed DC/DC converter with hybrid MMC configuration has the advantage of being able to block the DC/DC converter terminal connecting to the faulty DC grid section, while continue operating the other terminals connected to healthy DC grid sections.

- A hybrid HVDC system comprising a wind farm side VSC based on the hybrid MMC and a grid side LCC for integrating wind power has been investigated. A coordinated control strategy for the hybrid HVDC system is proposed to improve the transient response of the hybrid HVDC system under the commutation failure conditions.

7.3 Suggestions for future research

Potential areas for future research include:

- Optimized design for converter components to ensure minimum size for a high power design and reduced footprint, and modular design for the hybrid SM should also be considered for the practical applications.

- Enhanced control strategies on capacitor voltage balancing and circulating current control in the proposed hybrid MMC can be considered as further investigation to improve the operation performance of the hybrid MMC.

- Influences of the hybrid MMC on hybrid multi-terminal HVDC systems integrating various types of converters, such as LCC, conventional HB-MMC and FB-MMC, also need to be further investigated.

Appendices

Appendix A Experiment rig

The structure of the experimental prototype for theoretical verifications is introduced. Details of hardware components, electrical parameters and schematic diagram of the system are presented.

The experimental test rig is a single-phase modular multilevel converter (MMC) with three sub-modules (SMs) in each arm, and the control system is implemented using a TMS320F2812 DSP. The whole system is shown in Figs. A.1 – A.2, and the relative electrical parameters are listed in Table A-1, schematic diagram of system is presented in Fig. A.3.

Table A- 1 Parameters of the experimental MMC system

Item	Values
MMC rated power	400 W
DC voltage	120 V
AC voltage (phase-ground peak)	105 V
AC transformer (rms.)	230V/75V
Number of SMs per arm	3
SM type	3 FBSMs (Chapter 3)
	2 FBSMs (Chapter 4)
	2 FBSMs plus 1 HBSM

	(Chapter 5)
SM capacitor	940 uF
Inductance per arm	3.2 mH
MMC switching frequency	2.5 kHz

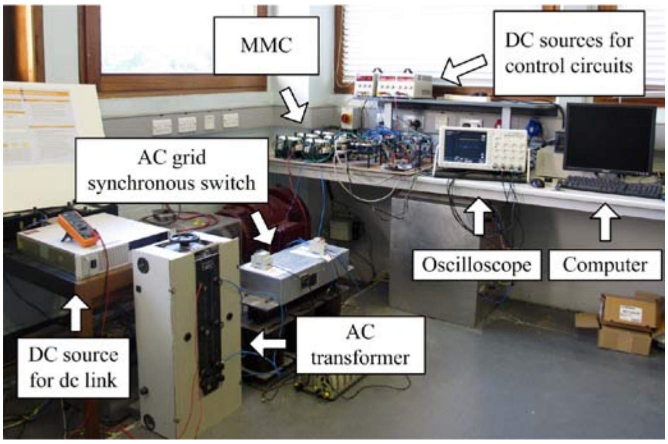


Fig. A. 1 Whole experimental prototype

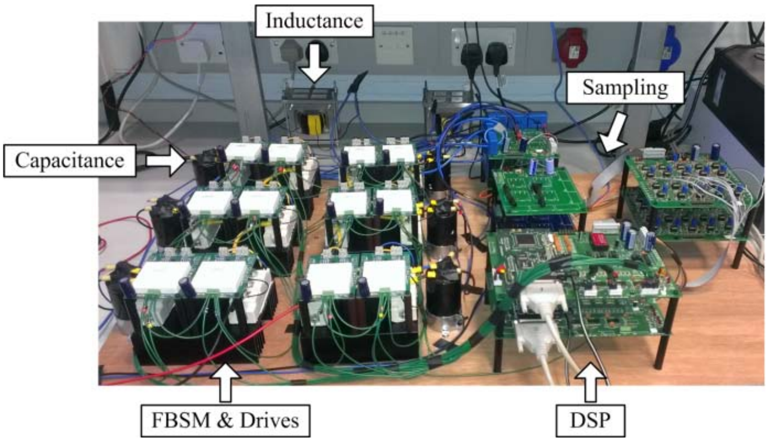


Fig. A. 2 MMC platform and its control circuits

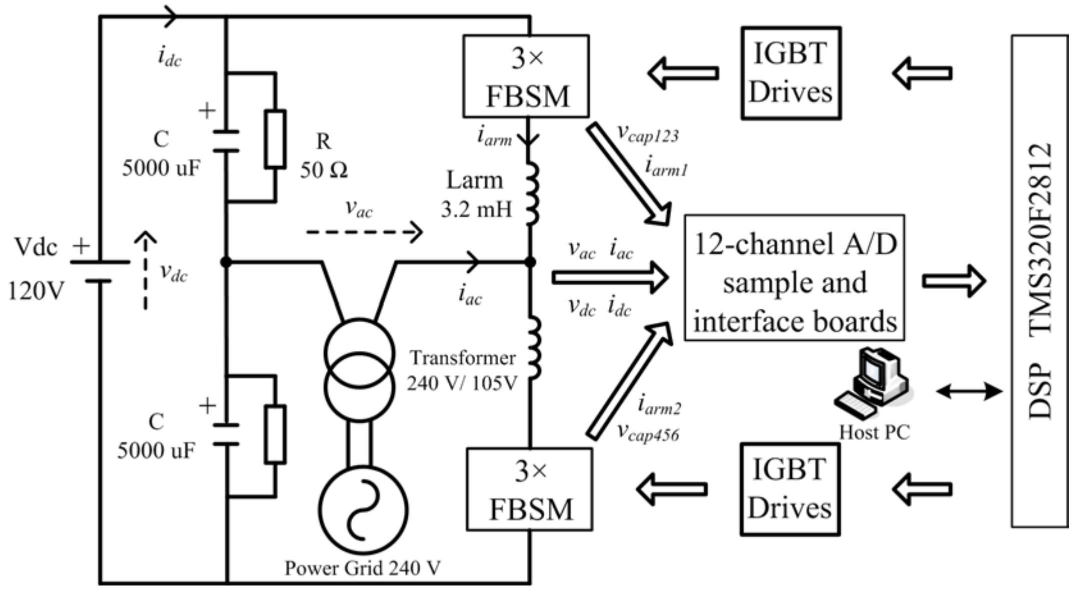


Fig. A. 3 Schematic diagram of the MMC system

Appendix B List of Tables and Figures

B.1 List of Tables

B. 2 List of Figures

Appendix C Reference

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Appendix D Author's Publications

[1] Rong Zeng, Lie Xu, Liangzhong Yao, and Barry W Williams, "Design and Operation of a Hybrid Modular Multilevel Converter", *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1137-1146, Mar. 2015.

Abstract

This paper presents a hybrid Modular Multilevel Converter (MMC), which combines full-bridge sub-modules (FBSM) and half-bridge sub-modules (HBSM). Compared with the FBSM based MMC, the proposed topology has the same dc fault blocking capability but uses fewer power devices hence has lower power losses. To increase power transmission capability of the proposed hybrid MMC, negative voltage states of the FBSMs are adopted to extend the output voltage range. The optimal ratio of FBSMs and HBSMs, and the number of FBSMs generating a negative voltage state are calculated to ensure successful dc fault blocking and capacitor voltage balancing. Equivalent circuits of each arm consisting of two individual voltage sources are proposed and two-stage selecting and sorting algorithms for ensuring capacitor voltage balancing are developed. Comparative studies for different circuit configurations show excellent performance balance for the proposed hybrid MMC, when considering dc fault blocking capability, power losses, and device utilization. Experimental results during normal operation and dc fault conditions demonstrate feasibility and validity the proposed hybrid MMC.

[2] Rong Zeng, Lie Xu, and D. John Morrow, "Pre-charging and DC Fault Ride-Through of Hybrid MMC Based HVDC Systems", *IEEE Trans. Power Del.*, early access.

Abstract

Compared to half-bridge based MMCs, full-bridge based systems have the advantage of blocking dc fault, but at the expense of increased power semiconductors and power losses. In view of the relationships among ac/dc voltages and currents in full-bridge based MMC with the negative voltage state, this paper provides a detailed analysis on the link between capacitor voltage variation and the maximum modulation index. A hybrid MMC, consisting of mixed half-bridge and full-bridge circuits to combine their respective advantages is investigated in terms of its pre-charging process and transient dc fault ride-through capability. Simulation and experiment results demonstrate the feasibility and validity of the proposed strategy for a full-bridge based MMC and the hybrid MMC.

[3] Rong Zeng, Lie Xu, Steve J. Finney, Derrick Holliday and Barry W. Williams, "Analysis and Control of Modular Multilevel Converters under Asymmetric Arm Impedance Conditions," *IEEE Trans. Ind. Electron.*. (under second-round review).

Abstract

This paper presents a detailed analysis and improved control strategy for Modular Multilevel Converters (MMC) under asymmetric arm inductance conditions. Unlike symmetric conditions, the fundamental ac current is not split equally between the upper and lower arms under asymmetric conditions, and the dc and double-frequency components in the common-mode current also flow into the ac side. To solve these issues, a theoretical analysis of the effect of asymmetric conditions on MMC operation is carried out using equivalent circuits at different frequencies. Three control targets are then presented to enhance the operational performance. A control strategy providing the control of differential-mode current, common-mode current and power balance is designed. The feasibility and validity of the proposed analysis and control strategy are demonstrated by simulation results from a three-phase MMC system and experimental results from a single-phase MMC system.

[4] Rong Zeng, Lie Xu, Liangzhong Yao, and Steve J. Finney, "Hybrid HVDC System for Integrating Wind Farms with Special Considerations on Transient Response," *IEEE Trans. Power Del.*. (under second-round review).

Abstract

This paper presents the control and operation of a hybrid HVDC system comprising a wind farm side VSC rectifier and a grid side LCC inverter for transmitting wind power to AC grid. The configuration and operation principle of the hybrid HVDC system are described. Commutation failure in the LCC inverter during an AC network disturbance is considered and its impact on the hybrid system operation is analyzed. An enhanced control strategy for the LCC and an alternative MMC topology using mixed half-bridge and full-bridge modules

are proposed. Simulation results using Matlab/Simulink are presented to demonstrate the robust performance during LCC inverter commutation failure to validate the operation and recovery of the hybrid system with the proposed control strategies and MMC configuration.

[5] Rong Zeng, Lie Xu, and Liangzhong Yao, "An Improved Modular Multilevel Converter with DC Fault Blocking Capability," in *Proc. IEEE Power & Energy Society General Meeting (PESGM)*, Jul. 2014, pp. 1-5.

Abstract

In contrast to the conventional half-bridge based MMC (HB-MMC), the full-bridge based MMC (FB-MMC) has the advantage of dc fault blocking capacity, but at the costs of increased power semiconductor devices and power losses. This paper proposes a hybrid modular multilevel converters (MMC) comprising of half half-bridge and half full-bridge sub-modules. The proposed topology takes the advantages of dc fault blocking capability of FB-MMC with less semiconductor devices and lower power losses than the FB-MMC. Comparative studies on power losses for different circuit configuration are conducted. Detailed pre-charge scheme for the proposed Hybrid MMC are designed and verified by simulations. Experiment results are provided to demonstrate the feasibility and validity of the proposed Hybrid MMC under normal operation and dc fault condition.

[6] Rong Zeng, Lie Xu and Liangzhong Yao, "A DC/DC Converter based on hybrid MMC with fault blocking capability for HVDC interconnection," in *Proc. Conf. on AC and DC Power Transmission*, Feb. 2015.

Abstract

This paper presents a multi-terminal high-power DC/DC converter configuration based on hybrid MMC topology with fault blocking capability for interconnecting HVDC systems. Its main functions include bidirectional power flow, step-up and step-down operation and fault isolation equivalent to a DC circuit breaker. By contrast to the conventional MMC based DC/DC converter, the proposed DC/DC converter with hybrid MMC configuration has the advantage of being able to block the DC/DC converter terminal connecting to faulty DC grid section, while continue operating the other terminals connected to healthy DC grid sections.

The proposed DC/DC converter operation is analysed and its control is described. Simulation results using Matlab/Simulink are presented to demonstrate the robust performance during dc fault conditions.