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Protection of Physically Compact Multiterminal DC Power Systems

by

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Abstract

The use of DC for primary power distribution has the potential to bring significant design, cost and efficiency benefits to microgrid, shipboard and aircraft applications. The integration of active converter technologies within these networks is a key enabler for these benefits to be realised, however their influence on an electrical network's fault response can lead to exceptionally demanding protection requirements. This represents a significant barrier to more widespread adoption of DC power distribution. The principle challenge within the field is to develop protection solutions which do not significantly detract from the advantages which DC networks offer. This objective leads the thesis to not only consider how the protection challenges may be overcome but also how this can be achieved in a manner which can benefit the overall design of a system, inclusive of various system design objectives. The thesis proposes that this objective can be achieved through the operation of network protection within the initial transient period following the occurrence of a fault.

In seeking to achieve this aim, the work presented within this thesis makes a number of contributions. The thesis categorises converter type based on the components which influence their fault response and then presents an analysis of the natural fault response of compact multiterminal DC power distribution networks containing these converters. Key factors such as the peak magnitudes and formation times of fault current profiles are determined and quantified as a function of network parameters, enabling protection system operating requirements to be established. Secondary fault effects such as voltage transients are also identified and quantified to illustrate the impact of suboptimal protection system operation. The capabilities of different protection methods and technologies for achieving the proposed operating requirements are then analysed. Significant conclusions are: solid state breaking technologies are essential to achieving operating targets and severe limitations exist with the application of protection methods available within literature for this application. To overcome these shortfalls, novel fault detection approaches are proposed and analysed. These approaches enable fault detection time targets to be met as well as aid with the effective integration of future circuit breaking technologies.

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Glossary

Term	*Definition*
i^2t	Integral of the square of the current with respect to time A^2s
Δi	Difference in current
V_s	Voltage of source
V_d	Diode on state voltage drop
$v_{CX}(t)$	Continuous voltage across capacitor X
$v_{CX}(0)$	Initial voltage across capacitor X at time $t = 0$
$\frac{dv_{CX}(t)}{dt}$	Rate of change of voltage across capacitor X
$i_L(t)$	Continuous current through inductance L
$i_L(0)$	Initial current through inductance L at time $t = 0$
$\frac{di_L}{dt}$	Rate of change of current through inductor L
$Z(t)$	Instantaneous impedance
Z_{FP}	Impedance of fault path
C_F	Main source converter filter capacitance
C_L	Load converter filter capacitance
ESR	Equivalent series resistance
C_{XESR}	ESR of C_X
R	Combined fault path resistance
L	Combined fault path inductance
$s_{1,2}$	Roots of characteristic Laplace equation, $s_{1,2} = -\alpha \pm \sqrt{\alpha^2 - {\omega_0}^2}$
α	Neper frequency, $\alpha = \frac{R}{2L}$
ω_0	Resonant radian frequency, $\omega_0 = \frac{1}{\sqrt{LC_F}}$
ω_d	Damped radian frequency, $\omega_d = \sqrt{{\omega_0}^2 - \alpha^2}$
Z_0	Surge impedance, $Z_0 = \sqrt{\frac{L}{C_F}}$
t_{peak}	Time to first current peak of capacitor discharge
E_L	Energy stored in inductor L
t_{CB}	Time of circuit breaker initial opening
i_{CB}	Theoretical counter current produced by circuit breaker during its operation
v_{CB}	Voltage developed across circuit breaker during its operation
v_{CBpeak}	Peak voltage developed across circuit breaker during its operation
T_2	Period between circuit breaker opening (t_{CB}) and current
t_{thres}	Time at which a specifically defined threshold has been reached
n	Proportion of line length
n_f	Proportion of line length at which a fault occurs

L_{Lim}	Inductance required to limit current to a specified magnitude
C_{snub}	Magnitude of capacitive snubber
R_{FCL}	Resistance of fault current limiter
t_L	Time to detect and discriminate fault location
t_f	Time of fault occurrence
Δt	Time measurement synchronisation error
$I_{threshold}$	Operating current threshold for a current differential scheme
$\frac{di(t\rightarrow 0)}{dt}$	Initial $\frac{di}{dt}$ as time approaches zero
L_{meas}	Measured inductance
t_m	Required measurement time for accurate fault discrimination
$n_f - t_m$ characteristic	Relationship between fault location and required measurement time
$L_{meas_{v_t}}$	Measured inductance using continuous voltage measurement
$\frac{di_{ave}}{dt}$	$\frac{di}{dt}$ determined by the measurement of current samples at different times
$L_{meas\,\frac{di_{ave}}{dt}}$	Measured inductance using average $\frac{di}{dt}$ measurement
$L_{meas\,\frac{di_{ave}}{dt}v_t}$	Measured inductance using continuous voltage and average $\frac{di}{dt}$ measurements
Fault clearance time	Total time from fault inception until fault extinction (current zero)
Circuit breaker operation time	Time between breaker receiving a trip signal and beginning to operate
Fault detection time	Time from fault inception to fault detection
'Simulated'	Used when an electrical network simulation package is used to determined network behaviour
'Calculated'	Used when derived equations are used to determined network behaviour

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Chapter 1

Introduction

There is an increasing interest in the use of DC power distribution throughout the power industry. This interest is largely driven by the increased usage and advance of power electronic technologies which have facilitated more interconnected and efficient use of DC systems. Recently proposed applications for DC range from large scale multiterminal DC systems, such as for offshore grid applications [1–3], to more physically compact network types primarily considered within this thesis. In particular, DC power distribution has been proposed for use within microgrid [4–6], shipboard [7–9] and aircraft [10–13] applications in recent years. The compact and islanded nature of these network types makes them prime candidates for the implementation of innovative power system architectures, and therefore opportunity exists for them to take advantage of the potential benefits of DC power distribution.

To gain an appreciation of why such a radical shift in the means of power distribution is being considered, it is useful to first review the benefits that DC power distribution can bring to these applications. For clarity these potential benefits are listed below and nested within this list is a discussion of why these benefits are particularly relevant for microgrid, shipboard and aircraft applications.

1. It is possible to transmit more DC power through a cable of a given voltage rating than with AC

There are a number of reasons why this is the case. The first relates to the insulation limits of cables. Whilst the power delivered through an AC conductor is determined by the voltage RMS, cable requirements are determined by the peak voltage level. This is not the case for DC conductors which can transmit power at the full voltage limit set by the cable insulation. Due to this higher average voltage level, a DC system can therefore transfer up to $\sqrt{2}$ times the power of

an AC system operating at the same AC (peak) voltage [9]. Alternative cabling arrangements, such as dividing the DC voltage into a two-bus arrangement with positive and negative voltage rails, can achieve even greater improvements in power transfer. For example, [6] claims that up to 16 times more power can be transmitted in DC than AC using the same cables and carefully selecting voltage levels. Furthermore, DC systems are free from skin effect (under steady state conditions) and reactive voltage drop, further improving power transfer.

These inherent characteristics of DC distribution provide a number of potential benefits. First, they can facilitate a reduction in cable sizes, potentially reducing cost (which is particular important for making DC distribution economic within the microgrid domain [6]), as well as reducing weight and volume of associated conductors [9, 14]. The indirect efficiency savings achieved by reducing the weight of the electrical system can be of significant benefit to ship and aircraft applications. For example, American Airlines claims that removing 1 pound (≈0.45kg) from each of the aircraft in its fleet will save more than 11000 US gallons (≈3.78 litres per gallon) in fuel per year [15], which, based on 2011's average jet fuel costs of $3.05 per gallon [16], equates to an annual cost saving of $33500 per pound of weight removed from the airframe. Whilst this only provides a high level approximation, it highlights that even small weight saving can result in significant reductions in operating costs in the long term and so incentivises design changes to reduce the weight of an aircraft's electrical system. Doerry [17] also provides an example of this from the marine sector, stating that for a small ship (such as surface combatants or offshore supply vessels) to carry an additional 1 ton ($\approx 1000kg$) of payload, the overall weight of ship must increase by approximately 9 tons to support it. This ratio reduces to 1 ton of payload to an additional 1.2 tons of ship for larger vessels. This again serves to highlight that the power system can have a much wider impact on the overall system design.

These characteristics also enable conductors to be better utilised where network voltage is fixed or limited by design constraints of the application. For example, in aviation the reduced pressure at altitude lowers the breakdown voltage of the surrounding air, increasing the risk of partial discharge [18]. Therefore within this sector, there is a reluctance to increase voltage in order to avoid this issue. Another example from within the shipping industry is the need for specially trained crew when the operating voltage is ≥1000V [19,20]. Although a practical rather than technical constraint, this can have cost and operability implications. This is a particular issue for small but power dense ships, such as offshore supply vessels, and has in part lead to low voltage system designs despite the potentially

significant on board power requirements [21, 22]. In both cases, a DC network solution would provide more power for the available voltage.

2. Using DC distribution can reduce the number of required power conversion stages between source and load

Within marine and aerospace sectors, the development of more-electric and all-electric design concepts, and the novel technologies associated with their realisation, are driving the requirement for greater electrification of secondary systems [23]. Increasingly, this creates a requirement for converter interfaced generation and load systems [9–11, 24–26]. Similarly within microgrids, distributed resources, such as small-scale generation, back-up energy storage, and some industrial and sensitive electronic loads increasingly rely on the use of power converters [4, 27].

Utilising DC, it is possible to reduce the number of these power converters used in a network. For systems that generate at variable frequency, two conversion stages (rectification and inversion) are required to distribute power on a standard AC bus. This could be reduced to one rectification stage if DC distribution was used. There are also many novel loads which have unique voltage and frequency requirements. For an AC system, two conversion stages are usually required to get the power in the desired form. This again can be reduced to one with DC distribution. Removal of these nugatory rectification and inversion stages could reduce the number of power converters, and subsequent conversion losses, by up to 50% [9, 27]. Additionally, many energy storage devices such as batteries, naturally output DC. This makes it easier to connect to a DC bus rather than AC as no inversion stage is required.

These factors have a potentially significant impact on the cost, complexity, volume and weight of future network designs. George [27] shows a clear example of this, highlighting that for a data centre containing 1000 servers (that use DC power), $3.5 million could be saved annually on power supply costs based on the reduced conversion losses and associated cooling requirements when utilising DC distribution. Efficiency savings of this order may be the difference between the commercial viability of a project as well as reducing its carbon footprint and therefore provide a high incentive for moving to DC.

Similar cost data for aerospace and marine sectors was not found within the public domain, however the increasing power requirements and reliance on power electronics anticipated within future platforms would suggest that significant efficiency savings could be made. Perhaps more important is the indirect efficiency

savings achieved by reducing the weight of the electrical system through the removal of redundant components, the potential advantages of which are highlighted above.

3. DC distribution better facilitates the paralleling of multiple non-synchronous sources

There are multiple points to consider here, many of which are equally relevant to AC systems. The following discusses these and highlights where specific benefits can be gained in the utilisation of DC distribution.

The first is that the paralleling of any sources provides the opportunity to increase the efficiency of power generation through optimised power sharing between the sources based on their individual operating characteristic. This principle has been applied for a number of years on grid based applications to control the output of power stations through the use of economic dispatch [28], and can be applied within AC and DC systems. However the paralleling of generators onto a DC bus is easier than for an AC bus, as the requirement for tight frequency regulation of the supply is removed [29]. This can enable faster connection of sources to a network, potentially providing better dynamic performance. For microgrids, this may allow the greater use of renewable sources under intermittent conditions, whereas within ships and aircraft, it can facilitate more efficient power sharing between multiple generators [12, 22, 30].

The second point relates to the use of non-synchronous generation sources, which are more likely to be smaller scale distributed energy resources and prime movers. The advantages of decoupling the generator frequency from that of the main distribution system are that it allows the prime movers to be operated at the most efficient speeds [7,9], or indeed any speed (which is of benefit to intermittent sources such as renewables). Generators could also, at least in certain applications, be operated at very high speed to increase power density [31]. Therefore the use of non-synchronous generation sources offer potential for both increased power density and efficiency. Again these advantages can be captured for both AC and DC systems, although additional conversion stages may be required to achieve a fixed AC output, the drawbacks of which are discussed above.

From the above points it is clear that several significant design and operability benefits exist through the adoption of DC distribution, particularly where multiple sources and power electronic interfaces are connected to the network. However until now a number of factors have held back the use of DC distribution. Historically this was an issue of voltage transformation and achievable transmission

distance [32], limiting the application of DC to very low voltage or certain niche applications. Despite advances in technology having overcome these issues, the limited application of DC to date means that, unlike AC electrical systems, a profound understanding of DC electrical systems is yet to be established within the power industry. This creates a psychological entry barrier to developing DC systems. This is evident from (and compounded by) the lack of appropriate standards in this area, particularly those related to the protection of DC networks, meaning that targets for which a system should be designed to are more difficult to establish.

Beyond these issues, key research challenges which exist for the current state of the art in DC distribution networks and technologies, is their control and protection. For example, network control problems such as negative impedance instability are introduced when interconnecting a number of power electronic converters. Many loads such as motors and actuators operate with constant power. Converters supply this constant power by tightly regulating their terminal voltage and drawing the required current from the network. The operation of these loads can result in the incremental impedance of the system becoming negative and the system becoming unstable [33]. This concept however, is now generally understood and converter control strategies can be used to cancel out this effect [33, 34].

The key research challenges which exist in the protection of multiterminal DC networks relate to both fundamental issues associated with the protection of DC networks coupled with those that have developed as a result of the adoption of new network and converter designs.

DC power distribution often increases the cost and physical burden of the associated network protection systems. In a faulted DC systems, no natural zero crossings exist in the fault current waveform in which the circuit can be broken. As such, larger, heavier and more costly circuit breakers must be employed to break DC current [14].

The nature of physically compact converter interfaced DC networks are such that electrical fault conditions can develop extremely rapidly, creating extremely high fault currents and severe transient voltage conditions, the sources of which will be described in detail in later chapters. This creates significant protection problems; network components must be capable of handling or be protected against these transients, DC circuit breakers must handle higher magnitude and more rapidly rising fault currents than previously expected to, network protection must be capable of coordinating its operation when faced with these fault

conditions.

Based on these challenges, three key research questions have been posed. These are:

1. How can the protection system performance requirements within future DC networks be quantified?

2. Can existing protection methods be used to achieve required fault detection times whilst maintaining sufficient levels of protection system coordination?

3. Are developments in circuit breaker technologies required to achieve desired operating speeds with suitable current and voltage ratings, and can this be achieved in a size, weight and cost efficient manner?

To investigate these questions, this thesis covers a number of areas. An analytical study of DC network fault response is conducted and methods of deriving key factors such as the peak magnitudes and formation times of fault current profiles as a function of network parameters are shown. This analysis enables the quantification of protection system operating requirements based on a number of scenarios and from this a desired optimal protection approach is identified. The thesis goes on to assess the capabilities of different methods and technologies for achieving these aims and novel protection approaches are proposed to overcome areas in which these currently available approaches fall short. The ultimate objective of this work is to develop protection solutions which do not significantly detract from the advantages which DC networks offer and the thesis concludes by highlighting areas where future work is necessary to achieve this objective.

1.1 Summary of key contributions

In addressing the research questions outlined in the previous section, a number of contributions are made within this thesis. These are summarised below.

1. Through the analysis of example converter topologies, the thesis identifies the key design characteristics of converters which influence their fault response and protection requirements. Converter topologies are categorised based on these characteristics, enabling the protection issues associated with each converter type to be generalised and common solutions to be explored.

2. A detailed analytical study of typical converter interfaced DC networks is presented, with new analytical tools developed to accurately represent

the different stages of the response. This work builds upon relevant standards and fault response calculation literature to provide methods which can be accurately applied to active converter interfaced DC networks. The methods developed underpin many of the conclusions within this thesis and enable the quantification of a number of relevant parameters. These include: the time at which specified current and voltage thresholds occur, circuit breaker current interruption, energy dissipation, voltage and energy let through requirements and he magnitude of post fault clearance voltage transients.

3. Quantification of protection operating times allows comparison with the capabilities of available circuit breaker devices. Given that fast device operation is often needed, it is shown that electromechanical and hybrid circuit breaker devices often fail to match operating time requirements and hence recommendations are made for an increased use of solid state circuit breaking devices. This is significant, particularly given the relative immaturity of SSCB technologies and has the potential to impact on the adoption of DC systems within the near term.

4. The thesis establishes that the use of conventional non-unit methods can be sub-optimal when attempting to achieve fast and discriminative protection system operation within converter interfaced DC networks. This conclusion is significant as the use of non-unit techniques is very common within distribution and low voltage networks, and hence this would require a shift in common protection practice. In turn this would impact the viability of any DC network implementation.

5. The use of current differential protection is identified as a potential fault detection solution and the inherent challenges in its implementation to DC systems are analytically assessed and quantified. Areas of particular novelty include the quantification of the required scheme decision making time and the impact of varying degrees of measurement synchronisation on the selectivity of a current differential scheme. This analysis enables the required performance of any current differential scheme implemented in a network to be accurately determined.

6. Based on assessment of conventional protection methods, a design framework is proposed for DC networks which provides a means of optimising protection scheme design to achieve the required fault discrimination and

operating speed whilst seeking to minimise installation costs. This is particularly important for microgrid systems where available investment in infrastructure is more limited relative to marine and aerospace sectors.

7. A 'pilot wire' current differential protection implementation approach is proposed which enables faults to be detected very shortly after their inception and with minimal synchronisation error. The proposed approach has the potential to reduce fault detection time by at least an order of magnitude below that of standard AC current differential schemes.

8. A novel fault detection and location method is proposed. The method, which is based on the estimation of fault path inductance from the measurement of a converter capacitor's initial discharge characteristic, is insensitive to fault resistance and fast acting, has the potential to overcome a number of the shortfalls of present non-unit based detection methods.[1]

9. A detailed study of potential implementation issues of the method proposed in point 8 is presented. This defines both its potential applications and limitations and presents methods to calculate the measurement requirements to achieve acceptable performance in a range of network types and fault conditions. Additionally, numerous areas of future work have been identified to both develop the method to ensure its accurate operation.

1.2 Dissemination of research outcomes

1.2.1 Publications

The publications which have arisen from this thesis relating to the development of analytical tools and methods and the determination of protection system operating requirements are:

- **S. D. A. Fletcher**, P. Norman, S. Galloway, and G. Burt, "Determination of protection system requirements for dc unmanned aerial vehicle electrical power networks for enhanced capability and survivability," IET Electrical Systems in Transportation, vol. 1, no. 4, pp. 137-147, 2011.

[1]During the course of applying for a patent on this novel approach, an arc fault detection scheme was discovered which utilises a similar concept [35], albeit for a different purpose. However the application dates of the respective patents highlight that the work presented within this thesis was developed independently and without knowledge of this other detection method. The patent application has proceeded on the basis that as [35] was not publically available at the time of submission, it could not be considered as prior knowledge.

- **S. D. A. Fletcher**, P. J. Norman, S. J. Galloway, G. M. Burt, "Impact of converter interface type on the protection requirements for DC aircraft power systems," SAE International Journal of Aerospace, vol. 5, no. 2, pp.532-540, October 2012, doi:10.4271/2012-01-2224.

- **S. D. A. Fletcher**, P. J. Norman, S. J. Galloway, G. M. Burt, "Impact of converter interface type on the protection requirements for DC aircraft power systems," in SAE Power Systems Conference 2012, Arizona, paper number 2012-01-2224.

- **S. D. A. Fletcher**, P. Norman, S. Galloway, and G. Burt, "Solid state circuit breakers enabling optimised protection of dc aircraft power systems," in 14th European Conference on Power Electronics and Applications (EPE 2011), September 2011.

- **S. D. A. Fletcher**, P. J. Norman, S. J. Galloway, G. M. Burt, "Mitigation against Overvoltages on a DC Marine Electrical System", 2009 Electric Ship Technologies Symposium (ESTS09), Baltimore, April 2009, ISBN: 978-1-4244-3438-1.

- **S. D. A. Fletcher**, P. J. Norman, S. J. Galloway, G. M. Burt, "Evaluation of Overvoltage Protection Requirements for a DC UAV Electrical Network," 2008 SAE Power Systems Conference, Seattle, November 2008, Paper no. 2008-01-2900.

- **S. D. A. Fletcher**, P. J. Norman, S. J. Galloway, G. M. Burt, "Overvoltage Protection on a DC Marine Electrical System," 43rd Universities Power Engineering Conference (UPEC), Padova, September 2008, ISBN: 978-1-4244-3294-3.

Publications related to demonstrating the challenges for current protection methods and their potential role in future DC systems are:

- **S. D. A. Fletcher**, P. Norman, P. Crolla, S. Galloway, and G. Burt, "Optimizing the Roles of Unit and Non-Unit Protection Methods within DC Microgrids" IEEE Transactions on Smart Grid, vol. 3, no. 4, pp. 2079-2087, Dec 2012.

- **S. D. A. Fletcher**, P. Norman, S. Galloway, and G. Burt, "Analysis of the effectiveness of non-unit protection methods within dc microgrids," in IET Renewable Power Generation conference, Edinburgh, September 2011.

Publications related to the development of a novel fault detection system, and potential challenges in its use are:

- **S. D. A. Fletcher**, P. J. Norman, S. J. Galloway, and J. E. Hill, "Protection System for an Electrical Power Network," UK Patent application GB1102031.0, February 2011.
- **S. D. A. Fletcher**, P. J. Norman, S. J. Galloway, G. M. Burt, "Fault detection and location in DC systems from initial di/dt measurement," in Euro TechCon 2012, Glasgow, November 2012.
- **S. D. A. Fletcher**, I. M. Elders, P. J. Norman, S. J. Galloway, G. M. Burt, J. McCarthy, J. E. Hill, "The impact of incorporating skin effect on the fault analysis and protection system performance of dc marine and aerospace power systems," 2010 IET Developments in Power System Protection conference, Manchester, March/April 2010.
- **S. D. A. Fletcher**, I. M. Elders, P. J. Norman, S. J. Galloway, G. M. Burt, C. G. Bright, J. McCarthy, "Consideration of the impact of skin effect in the transient analysis of dc marine systems," 2009 IMarEST Engine as a Weapon III Conference, Portsmouth, June 2009, pp. 134-143.

Finally, related publications (two of which include a conference publication which was subsequently selected for a journal) that discuss the impact of electrical power system architecture, including energy storage usage, on the protection requirements and challenges are:

- **S. D. A. Fletcher**, P. Norman, S. Galloway, P. Rakhra, G. Burt and V. Lowe, "Modeling and simulation enabled UAV electrical power system design" in SAE International Journal of Aerospace, vol. 4, no. 2, pp.1074-1083, November 2011, doi:10.4271/2011-01-2645.
- P. Rakhra, P. Norman, **S. D. A. Fletcher**, S. Galloway, G. Burt, "A Holistic Approach towards Optimizing Energy Storage Response during Network Faulted Conditions within an Aircraft Electrical Power System" SAE International Journal of Aerospace, vol. 5, no. 2, pp.548-556, October 2012, doi:10.4271/2012-01-2229.
- **S. D. A. Fletcher**, P. Norman, S. Galloway, P. Rakhra, G. Burt and V. Lowe, "Modeling and simulation enabled UAV electrical power system design" in SAE Aerotech 2011, Toulouse, paper no. 2011-01-2645, October 2011.

- P. Rakhra, P. Norman, **S. D. A. Fletcher**, S. Galloway, G. Burt, "A Holistic Approach towards Optimizing Energy Storage Response during Network Faulted Conditions within an Aircraft Electrical Power System" in SAE Power Systems Conference 2012, Arizona, paper number 2012-01-2229, October/November 2012.

- P. Rakhra, P. Norman, **S. D. A. Fletcher**, S. Galloway, G. Burt, "Toward Optimising Energy Storage Response during Network Faulted Conditions within an Aircraft Electrical Power System" in Electrical Systems for Aircraft, Railway and Ship Propulsion (ESARS) 2012, Bologna, October 2012.

- J. Shaw, **S. D. A. Fletcher**, P. Norman, S. Galloway, "More Electric Power System Concepts for an Environmentally Responsible Aircraft (N+2)" in UPEC 2012, London, September 2012.

In addition to the papers listed above, a number of other technical reports have also been produced in support of relevant aerospace and marine electrical system projects. These include one invention disclosure report in addition to the patent application described above.

1.3 Thesis outline

An outline of the work contained within this thesis is presented below.

Chapter 2 introduces a number of power system architectures, technologies and methods which will be referred to throughout the thesis. It also highlights the importance of effective protection within electrical networks generally, and specifically highlights the unique challenges associated within the protection of small scale islanded DC power systems. As part of this, the chapter identifies the key design characteristics of relevant DC system converters which influence their fault response and protection requirements. Key publications will also be reviewed to provide context for the area of research and illustrate the importance and necessity for the work presented within this thesis.

Chapter 3 presents an analysis of the natural fault response of power electronic fed, compact multi-terminal DC power distribution networks, typical of those proposed for future aircraft, ships and microgrid designs. The analytical tools developed and methods demonstrated within this chapter will be used throughout this thesis, both in the identification of protection system requirements and the assessment of protection methods within compact DC power systems.

Chapter 4 illustrates how the analytical tools developed within Chapter 3 can be utilised to first quantify specific challenges in the protection of DC networks and then uses this information to determine operating requirements for a network's protection system.

Chapter 5 demonstrates the challenges in applying non-unit fault detections techniques within compact DC networks, then assesses the potential for unit protection schemes to overcome these challenges. The chapter then discusses how the roles of non-unit and unit performance methods could be optimised to achieve required levels of fault discrimination whilst seeking to minimise installation costs.

Chapter 6 presents an example case study where a 'pilot wire' based current differential protection scheme is implemented on UAV electrical system. The chapter demonstrates how the approach may be a viable method of implementing high speed, coordinated protection system operation.

Chapter 7 proposes a novel fault detection method for converter interfaced networks based on the initial $\frac{di}{dt}$ of a converter's capacitive filter following the occurrence of a fault. The chapter will first build on the analysis developed in earlier chapters to describe the $\frac{di}{dt}$ response and how it can be used for fault detection. The concept is then analysed for various networks configurations under ideal measurement conditions to assess whether anything would prevent successful fault detection. Having assessed the ideal operating case, the issues for practical implementation are investigated. These include areas such as measurement requirements and integration into a wider protection scheme.

Finally, chapter 8 draws together the conclusions and potential avenues for future work identified in previous chapters and again highlights the contributions of this work.

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Chapter 2

DC power networks: architectures, technologies and protection

Whilst the use of lower voltage DC distribution is not yet prevalent within the aerospace, marine and microgrid sectors, it has attracted a significant amount of research, both establishing its potential and in the development of electrical system architectures and necessary power electronic and protection devices. From this available literature, this chapter will introduce the key components contained within future DC networks, the fundamentals and state of the art for network protection and how both of these are currently being applied on DC networks.

2.1 DC power network design

The use of DC distribution can bring a number of advantages, be that in terms of reduced cabling [1], reduction in conversion requirements [2, 3] or increase overall system efficiency [4]. However the importance of these benefits in terms of the overall system depends on the design objectives of the particular application. How they are capitalised on depends on the architecture of the power system. These two issues are discussed in the following sections.

2.1.1 Power system design objectives

Karimi [5] provides an example of power system design objectives by identifying a number of attributes upon which one can evaluate an aircraft electrical system design. These attributes include:

- Power system efficiency
- Weight
- Volume
- Total cost
- Safety
- Thermal efficiency
- Reliability
- Maintainability
- Functionality
- Cost effective rapid technological insertion
- Green systems

In the design of aircraft networks, safety and reliability are of extreme importance given the potentially grave consequences of a power system failure. For this reason, certification requirements are particularly stringent for aircraft networks, where the probability of total loss of power should be lower or equal to 10^{-9} per flight hour for civil aircraft [6, 7]. This probability is increased to 10^{-7} per flight hour for military applications [7], reflecting the differing view of risk versus performance between applications.

Beyond the safety constraints, the other design drivers are becoming increasingly important, both from a perspective of operating cost and for meeting efficiency targets of future aircraft designs, such as those defined by NASA in 2010 [8]. This increases the importance of attributes such as power system efficiency as well as weight and volume which will impact fuel burn, and hence the through life costs of the aircraft. Each of these design attributes could also be applied to ships given the continued necessity to increase efficiency and decrease cost within the application area [9]. As Doerry's [10] example (as discussed in Chapter 1) served to highlight, the power system can have a much wider impact on the overall system and hence there is value in exploring means of optimising its design.

For microgrid systems, factors such as weight are far less consequential but given the lower value of land based distribution systems, minimisation of cost

(whilst maintaining a suitable supply reliability) is likely to feature more heavily in the design process.

Each of these factors must also be taken into consideration in the design of network protection. The following section will provide examples of networks from each of the three application types, highlighting how these design attributes are taken into account.

2.1.2 Review of current and state of the art DC power system architectures

The extent to which the potential benefits of DC distribution are exploited partly depends on the architecture of the power system. There are four general architectures which are either in use or have been proposed for use within DC networks; radial, busbar, zonal and ring architectures. Examples of these networks, taken from various domains, are illustrated within figures 2.1, 2.2, 2.3 and 2.4 respectively.

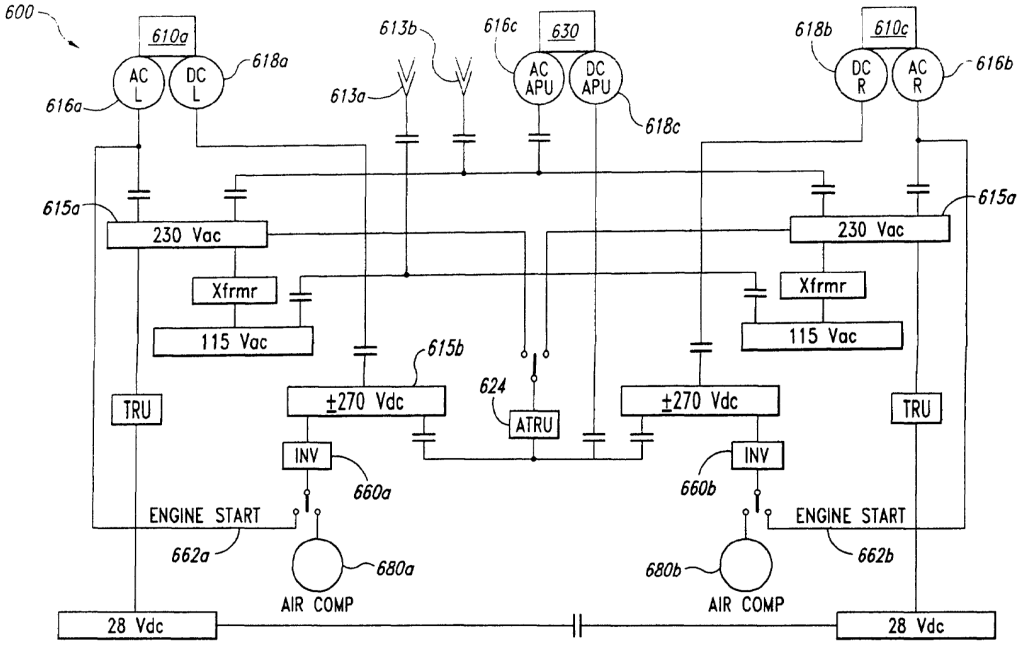

Figure 2.1: Single line diagram of Boeing 787 electrical system architecture [11]

Figure 2.1 presents a single line diagram of the Boeing 787 aircraft power system architecture [11]. Within this architecture there are mixed AC and DC network sections, though DC sections are limited to either $28VDC$, which has been used within aircraft systems for many decades, or reasonably contained $\pm 270VDC$ sections. This indicates that whilst there is some benefit in utilising

DC, it is not necessarily mature enough to be implemented more widely within the network, with the contained sections fairly straight forward to protect. In part, protection can be more easily achieved due to the highly redundant electrical system design (generation, supply paths and loads) within these types of architectures, the primary purpose of which is to achieve high reliability targets for power supply within aircraft. This redundancy within the design enables the disconnection of large network sections without significant loss of functionality, reducing the requirement of protection device coordination. Furthermore, the DC sections within figure 2.1 are supplied by DC generators or via Autotransformer Rectifier Units (ATRU) and therefore the architecture will not suffer from the protection issues associated with the use of fully controlled converters, as described later in this chapter. Fully controlled converter technologies may however be required to efficiently extend use of DC within the network, as the architectures below highlight.

The network illustrated within figure 2.2 is proposed for a microgrid application [12]. The network distributes power at $400V_{DC}$, is connected to the main grid via a voltage source converter (converter topology which is described in section 2.3), has battery energy storage connected directly to the distribution busbar and two loads interfaced through DC/DC converters. This architecture provides an example of how multiple power sources and loads can be efficiently paralleled on to a DC busbar. Drawbacks of this type of network is the susceptibility to faults, in particular those occurring on the distribution busbar. Work presented within [12] describes the protection issues related to this network and these are discussed further in section 2.4.

Multiple variations of zonal networks exist within literature, with 'zones' ranging from supply zones to zones containing load centres. One general, and differentiating, characteristic of zonal networks is the continuous connection (bus ties are not considered to be a continuous connection in this case as they are normally open) of a portion of the network (be that a distribution point like a busbar or a load centre) to two or more main supply paths. These main supply paths are usually geographically separated to reduce the probability of a single fault impacting both supply paths [9]. One example of this type of network is shown within figure 2.3, which illustrates a proposed shipboard electrical system architecture [13]. This network is similar in nature to busbar type network shown in figure 2.2 however in addition, it connects two supply busbars together through normally closed contactors and a 100m length of cable (labelled 14 and 8 respectively in figure 2.3). This architecture takes advantage of the option to parallel

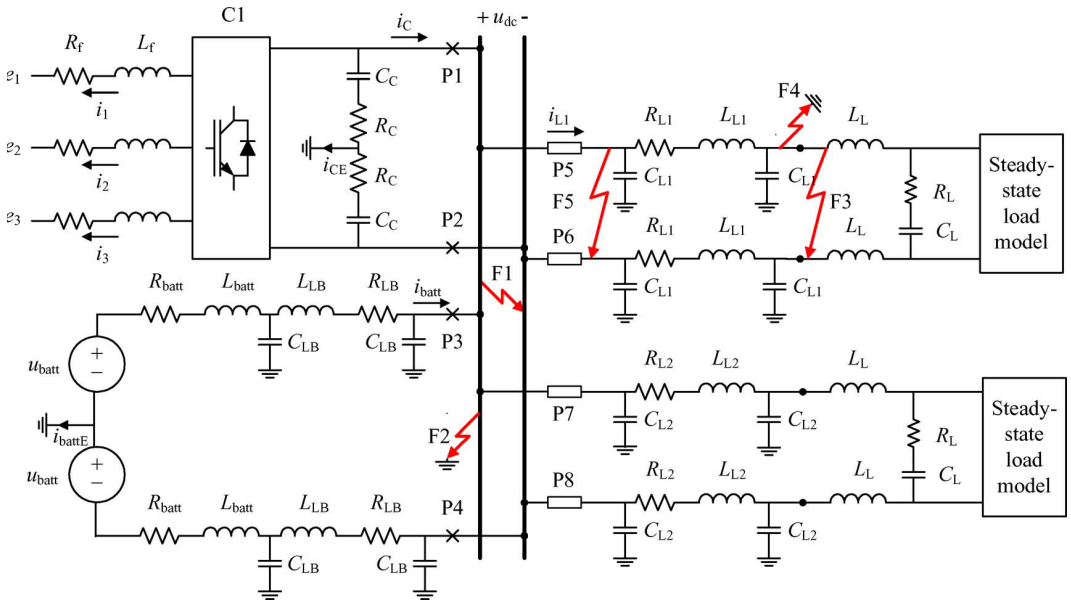

Figure 2.2: Example of a DC microgrid network section [12]

multiple asynchronous power sources onto a DC bus, increasing redundancy of supply and presenting the opportunity to optimise the power dispatch of generation across the entire network. Following the paralleling of generation on the DC bus, standard AC distribution is utilised to enable compatibility with standard equipment. As above, a drawback of this network type is the susceptibility to faults, where DC busbar faults would lead to the loss of a significant proportion of total generation. However the self-sustaining nature of the two supply zones means that the fault tolerance of the network can be increased through correct protection operation at the interconnection points. Zonal networks appear to be of particular interest for shipboard applications (AC or DC), with [9] reporting that weight and cost can be significantly reduced compared to radial distribution systems. Even greater benefits are achievable by considering a zonal DC system [9].

The final architecture type considered is the ring architecture, as illustrated within figure 2.4. Figure 2.4 is designed specifically for an unmanned aerial vehicle (UAV) application and is derived from work such as that presented within [15]. One of the main benefits of a ring architecture is the opportunity for increased fault tolerance, given the addition of a parallel supply path. Architectures of this type are more suited to safety critical but small scale systems, such as aircraft, where continuity of supply is vital but there is not necessarily the opportunity to have network sections with their own back up supply, as was the case with the zonal architectures.

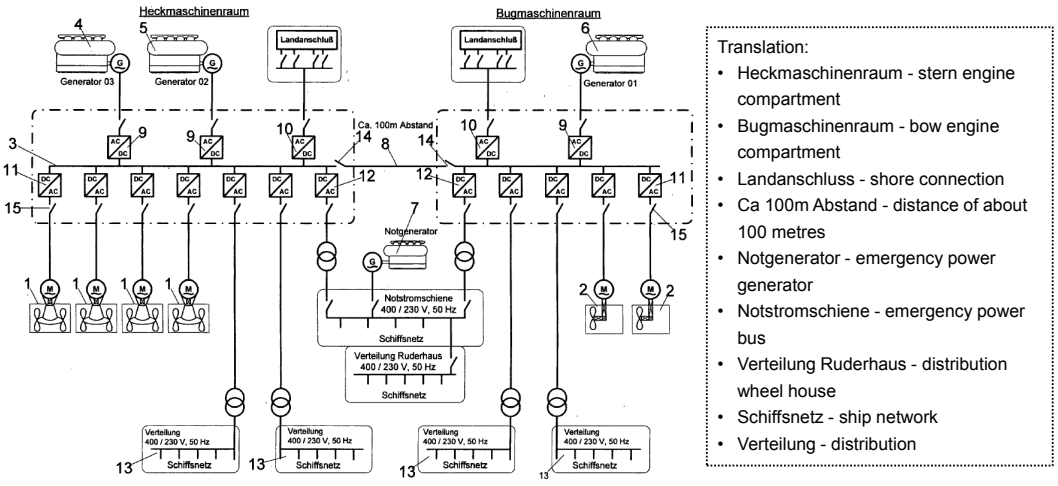

Figure 2.3: Example of a proposed shipboard electrical system architecture based on interconnected DC busbars [13]

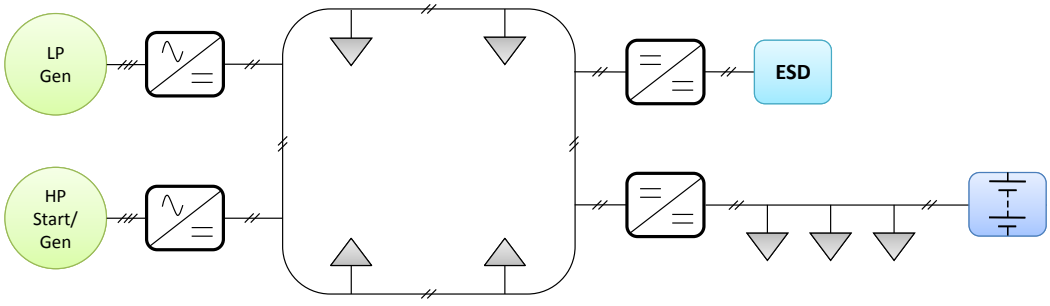

Figure 2.4: Example of a DC ring electrical power system architecture for a UAV

Throughout the thesis, a mix of all four network types is used to illustrate the many the protection issues considered. Whilst the particular protection issues are different for each network, the most significant challenges exist due to common components within each of these networks. This will be highlighted in later sections.

2.2 DC power network protection fundamentals

As the main subject of the work presented within this thesis, later chapters go into greater depth on the protection challenges and solutions for the types of systems considered. The intention of this section is therefore to simply introduce the fundamental concepts related to the protection of electrical networks and highlight the unique differences between the protection of AC and DC systems generally, and more specifically, the converter interfaced networks considered throughout the work.

2.2.1 Protection system objectives

Reference [16] outlines the key design criteria for any protection system. These are:

- *Reliability* - Requirement for highly reliable design and settings to ensure that the protection system will operate under all required conditions and refrain from operating when required. Reliable protection equipment and rigorous testing are also key criteria for protection systems.
- *Selectivity* - When a fault occurs, the protection scheme is required to trip only those circuit breakers whose operation is required to isolate the fault. This is also known as 'discrimination'.
- *Stability* - The protection system should remain unaffected by conditions external to the protected zone (usually associated with unit protection).
- *Speed* - The protection system should aim to isolate faults on a network as rapidly as possible to reduce fault related damage and prevent cascading faults through collapse of network voltage.
- *Sensitivity* - Protection system should be sensitive to minimum operating level.

As with the system design objectives, the importance of each of these factors varies with the requirements of a particular application area. The above points do however provide further details on how the network design attributes will impact on the protection requirements. For example, the reliability of a network's design will not only be influenced by the number of parallel supply paths but also the ability of the network protection to quickly remove faults in a manner which maintains supply to non-faulted network sections.

2.2.2 Protection philosophies and their application to DC systems

The methods by which faults are detected within electrical systems are categorised as either '*unit*' or '*non-unit*'. These two categories refer to the measurement and decision making processes utilised when detecting faults and are described in the following sections.

Non-unit protection

Non-unit protection does not protect a clearly bounded zone of the power system and will operate whenever its threshold is violated; non-unit schemes have inherent backup capabilities and will act to protect the system if a neighbouring protection system fails to operate [17]. To detect faults, non-unit methods look into a network from a single point, comparing relevant measurements taken at that point in the network with a preset threshold. Typical non-unit measurements include current, voltage, impedance, frequency (only in AC systems) and the rate of change of these variables. The following sections briefly describe how these types of measurements can be used to coordinate protection system operation as well as some of the challenges in their application within DC power systems.

Overcurrent protection Overcurrent protection works on the principle that when a fault occurs on a system, the resulting current is significantly higher than that experienced under normal operating conditions. This allows an upper current threshold to be set (above normal operating current) and when current rises above this threshold, it indicates that there is a fault on the system. This fault current will be of a varying magnitude depending on the location of the fault and so this gives different fault levels at different parts of the system. This is illustrated in figure 2.5.

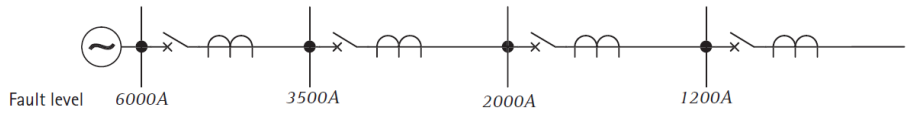

Figure 2.5: Radial current distribution line with reducing fault level [17]

As stated in section 2.2.1, the performance of a protection scheme is measured on its ability to locate and isolate faults with minimum disruption to the rest of the network. This is achieved here by co-ordinating the relay settings, so only the relay closest to the fault will trip. To provide backup, upstream relays may also operate for faults downstream of other relays after a time delay.

In many applications, overcurrent protection is implemented using overcurrent relays with an inverse time-current characteristic. This means that if the current reaches a certain magnitude range the relay will trip the breakers after a time inversely proportional to the value of the current. Therefore, the higher the current, the shorter the trip time. It will also be set to trip instantaneously if the current exceeds a certain value. These values can be manually adjusted, either changing the delay times or changing the current thresholds.

An alternative means of implementing overcurrent protection based in both current and time is to measure the network's I^2t (also known as the 'Joule Integral') response, measured in A^2s. I^2t is the integral of the square of current over time 't'. It is primarily a measurement of thermal energy associated with current flow, and so is extremely useful in determining the impact of faults on factors such as conductor heating. For example, the peak prospective I^2t describes the maximum stress which network components will experience during short circuits [18], and so helps to determine network design and protection requirements.

In the setting of protection devices, I^2t is usually referred to as 'let through energy', where the protection device would operate once the 'let through energy' threshold was exceeded. This operating point is inherent for thermally operated protection devices such as fuses and moulded case circuit breakers. Device operation based on a I^2t threshold can also be digitally programmed; an example of this is the Solid State Power Controllers (SSPC) used within modern aircraft networks which have an inbuilt I^2t operating function [19].

One particular issue in the application of overcurrent protection to all converter interfaced networks is the potential for the converter to limit fault current [20]. The effect of any current limiting action is that fault current level may become constant throughout the network, potentially extending fault detection times and allowing the fault to remain on the network for longer. Solutions to

this include uprating converters in order to supply more fault current, enabling faster fault detection, however this has size, weight and cost implications for the converter design. Section 2.3 discusses how the more developed converter topologies, which are capable of limiting current, may cause this to be an issue when used within DC networks.

There are two issues which relate specifically to the application of overcurrent methods to DC networks. The first is the challenge of coordinating device operation within the high initial capacitive discharge current period. The second is the potential for variable fault resistance and the impact this has on fault current. This is a particular issue for compact networks where, due to small line impedance, any fault resistance will make up a greater proportion of overall fault path impedance. This can lead to similar responses being presented for many different fault locations, potentially causing protection selectivity issues. These issues are investigated in detail within Chapter 5.

Rate of current rise Rate of current rise (ROCR) fault protection operates on the principle that current will rise more rapidly under fault conditions than under normal operating conditions [21]. This method is not too far removed from overcurrent protection however its main advantage is that faults can be detected earlier, while current is rising rather than at its peak, so full fault current does not need to develop to allow detection and discrimination. Early detection and isolation is advantageous as it can help minimise the disruption to the rest of the network and reduce stress on circuit breaking equipment. Figure 2.6 illustrates the various levels of ROCR which a network may experience.

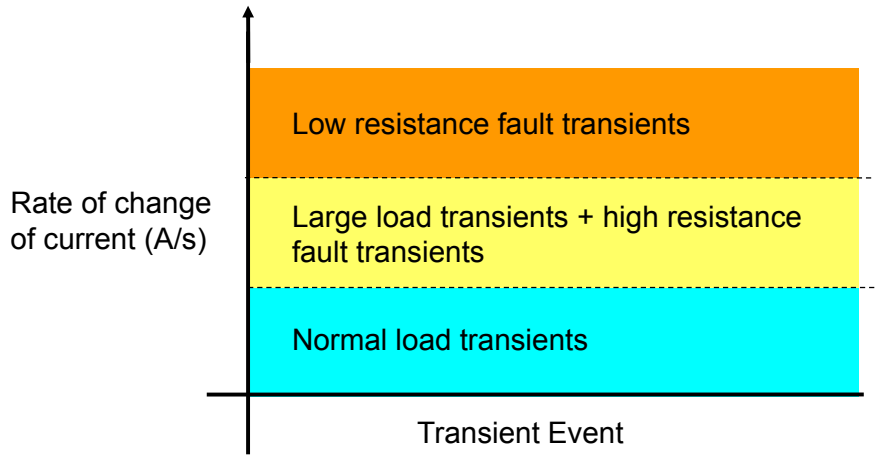

Figure 2.6: Fault detection regions for $\frac{di}{dt}$ protection systems

Figure 2.6 shows that there are two distinct regions where load transients

and fault transients would normally lie in terms of ROCR. However there are also two overlapping areas where distinguishing between large load transients and high resistance faults becomes difficult. Partly for this reason ROCR is not usually used in isolation, and is normally accompanied by a current magnitude measurement to avoid spurious protection system operation [22]. Chapter 7 of this thesis describes a novel approach to improve the accuracy of rate of current change fault detection methods.

Distance protection Distance (also known as impedance) protection works on the principle that the impedance of a transmission line is proportional to the length of the line, and so by measuring the impedance, the length of a line can be derived [23]. Distance protection is implemented by measuring voltage and current at a point on the network and from that the impedance of the line downstream of that point can be calculated. If a fault occurs on the network it effectively shortens the length of the line from the point of measurement to the point of fault and so will change the impedance measured. The impedance characteristic is illustrated in figure 2.7.

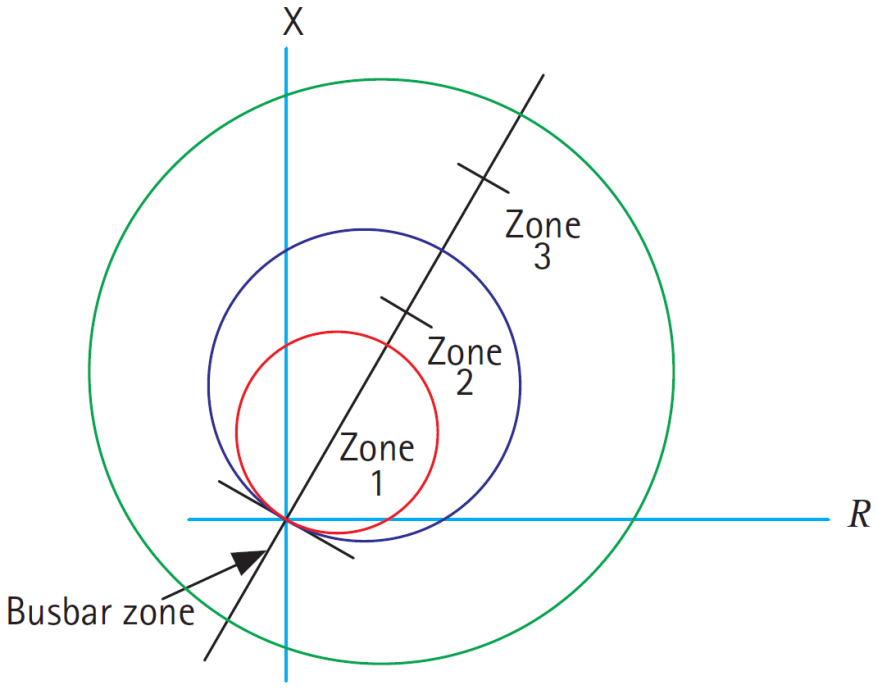

Figure 2.7: Mho characteristic with zones of protection [23]

Figure 2.7 shows three zones of protection covered by the relay physically located at the crossing between the X and R axis. These zones are in part used due to the uncertainty in both measurement and line parameters, which makes

it impossible to protect an exact length of line. Overlapping zones are used to compensate for this uncertainty, which enables each part of the line to be protected. Faults in Zone 1 are tripped instantaneously, and Zones 2 and 3 with increasing time delays respectively.

Distance protection is commonly employed on long lengths of line (such as transmission lines) but it is not as common in smaller systems as the desired levels of discrimination are difficult to achieve, as Chapter 5 illustrates. However the technique presented in Chapter 7 does build upon the principles of distance protection, therefore it is possible that the understanding of this fault detection method can facilitate the development of more relevant techniques tailored to the requirements of compact networks.

Travelling waves and wavelet analysis The idea of using high frequency travelling waves for fault detection has been around for a number of years [24] and is increasing common within DC traction systems [22, 25] and HVDC links [26]. This method is based on the concept that the occurrence of an electrical fault sets up a travelling wave which propagate out from the point of fault. Current and voltage travelling waves are related in both time and origin which, using wavelet analysis, allows a fault's location to be determined. Given that these waves travel at close to the speed of light, faults can be detected very quickly. Furthermore, as the travelling wave did not exist prior to the fault, much of the information it contains relates to the fault.

However a major disadvantage of travelling waves is their poor detection of close up faults. Theoretically, no matter where the fault occurs it can be identified [25]. However, due to the very short travel time from the close up faults, the travelling waves cannot be easily distinguished without the use of excessively high measurement speeds and sampling [24, 25]. This makes traditional travelling wave location methods more suited to large networks than those primarily considered within this thesis.

An alternative fault detection and location approach based on the analysis of travelling waves is proposed within [27] which is more suitable for smaller scale systems. As opposed to measuring the initial travelling waves resulting from the occurrence of a fault on the system, the proposed approach is based on the injection of current pulses into a network to facilitate fault location. It is the reflections from these injected currents which can be used to determine fault location. Drawbacks of this approach are that an additional indicator is required to trigger this injection of current, limiting its potential for use as primary protection system.

However this factor also has advantages, where current injection can also enable fault location within a de-energised network, meaning that the network would not be required to continue to supply fault current to aid fault location. This would be particularly useful within networks which allow the disconnection of larger network sections under fault conditions. For these networks, more detailed fault location information could be gathered following the disconnection of these larger sections (as well as allowing more precise network sectionalising) without exposing healthy parts of the network to the fault for prolonged periods of time.

Unit protection

Unit protection protects a clearly bounded zone of the power system and will not operate for faults external to this zone. In contrast to non-unit schemes, it does not provide backup to adjacent elements of the system [28]. A common form of unit protection is current differential protection, which operates by comparing all currents' magnitudes and/or relative directions at the boundaries of a specified element within a network [28]. This operation is highlighted in figures 2.8 and 2.9.

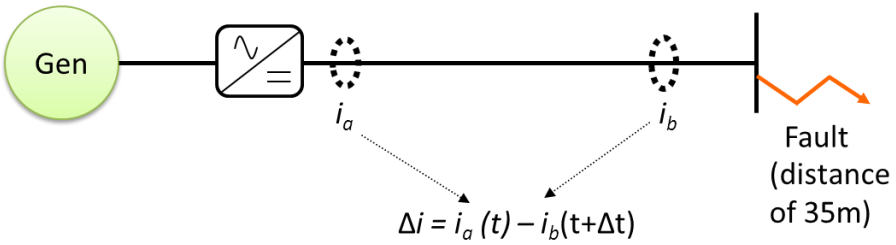

Figure 2.8: Current differential scheme with fault external to the protected zone

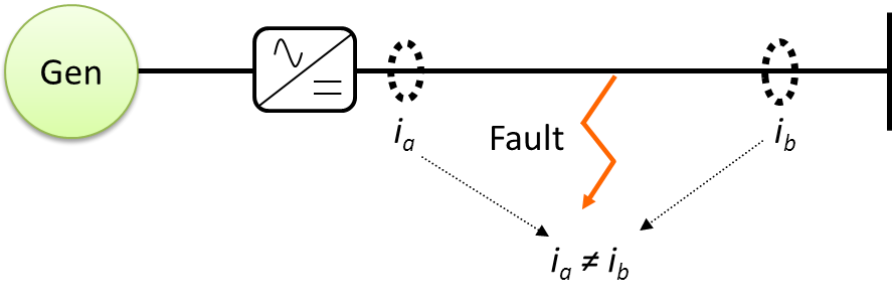

Figure 2.9: Current differential scheme with fault within the protected zone

As the figures suggests, the presence of a fault is determined by comparing the currents entering and exiting the differential current zone. When these are not equal (as in figure 2.9) it indicates that an alternative current path has formed, which in turn is indicative of a fault. Measurement of this inequality in current

(also referred to as non-zero differential sum) is then used to operate appropriate protection devices within the network.

To ensure that these protection devices only operate when faults exist on the network (and not due to transient charging or leakage current effects or measurement errors), they are restrained by the use of a bias on the differential sum. In the simplest terms, the difference in current between i_a and i_b in the example above must be above this bias in order for the protection scheme to operate.

Standard bias characteristics can be either fixed current magnitudes, approximately proportional to the measured current or a combination of the two. Figure 2.10 provides an illustration of a typical bias characteristic of a protection relay [28].

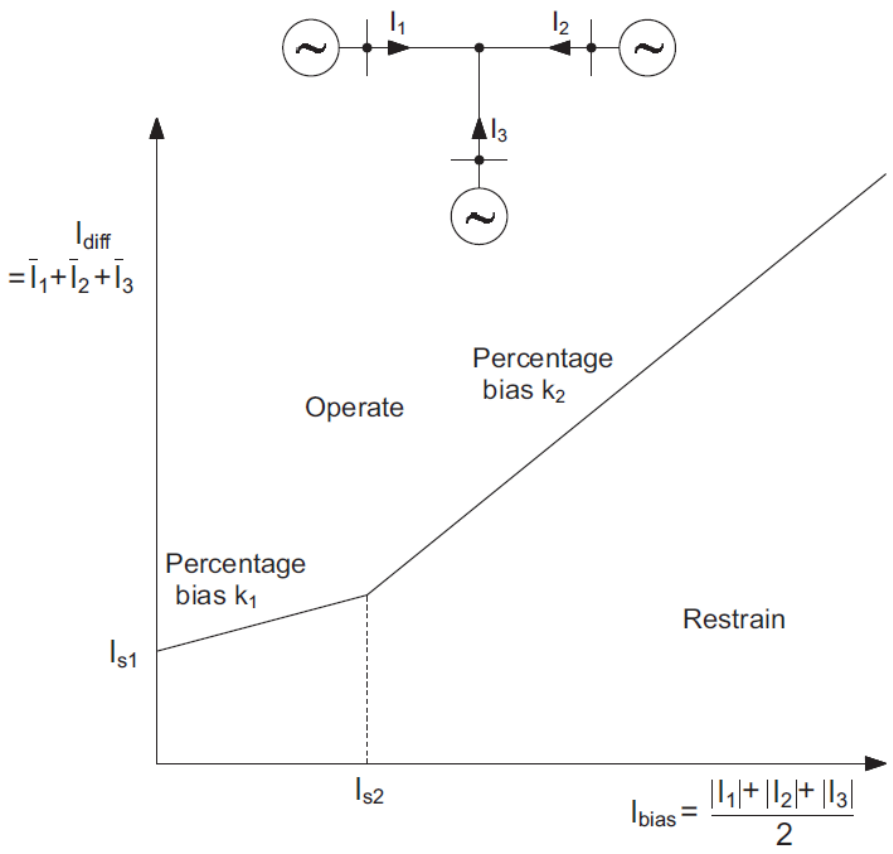

Figure 2.10: Typical bias characteristic of a relay [28]

The nature of current differential protection is such that it is far less susceptible to the effects of variable fault levels and impedances than non-unit methods [29, 30], facilitating more effective protection selectivity in a network. However a major challenge for the implementation of a differential protection scheme within compact DC networks, is achieving the protection operating decision within the desired time frame.

Modern differential current schemes propose the use of communications even for relatively compact systems to take advantage of the benefits of IEC 61850 [31], a communication standard for protection and control systems. However given the inherent processing and communication propagation delays, it may be challenging to meet stringent time criterion when utilising communication networks for this purpose [28]. Furthermore, due to the high rate of change of measured data possible within compact DC networks, near exact time synchronisation would be required under transient fault current conditions. Measurement accuracy may also be an issue for current differential schemes that compensate for current flow to and from the capacitance [32] in the differential calculation. This compensation needs to be performed with high accuracy due to the potentially dominant magnitude of the capacitor fault current. These aspects all provide further challenges for implementation and will be explored in later chapters.

2.2.3 Protection devices

Circuit breaker technologies

The implementation of DC distribution in a network will typically increase the physical burden of the protection system. There is no natural zero crossing in the fault current waveform of a DC system and as such, the size and weight of DC circuit breakers is greater than the equivalent AC device [33]. As space and weight can be at a premium in certain applications, the increase in size for electromagnetic circuit breakers (EMCB) makes the use of DC distribution undesirable. Additionally, in the time taken for the EMCB to break the circuit, the fault could potentially propagate throughout the network to healthy loads causing further problems, as Chapters 3 and 4 will illustrate. As an alternative, fuse based protection has been implemented on equivalently sized DC auxiliary installations and demonstrator rigs [34, 35]. Fuses are comparatively small and can operate very quickly to isolate a fault, however they are single use devices and so are largely unsuitable for the considered applications.

Solid state circuit breaker (SSCB) technologies offer a potential alternative to bulky and heavy EMCBs [33]. Through the utilisation of power electronic turn off devices, such as Insulated Gate Bipolar Transistors (IGBTs), Gate Turn-Off thyristors (GTOs) and Emitter Turn-Off thyristors (ETOs), these breakers can operate extremely quickly after the detection of a fault in order to break the circuit. Whilst there has been some encouraging research in this area [36], few commercial devices exist which can operate at the voltage and current lev-

els required for lower voltage DC applications. Developments in new materials such as silicon carbide may significantly enhance the capabilities of these technologies [37]. The device shown in figure 2.11 is an example of a DCCB which utilises an ETO device [36]. Additionally, hybrid circuit breakers, by combining both mechanical and solid state elements, offer significant speed increases over EMCBs [38, 39]. The capability of each of these technologies to achieve desired performance levels is assessed within Chapter 4.

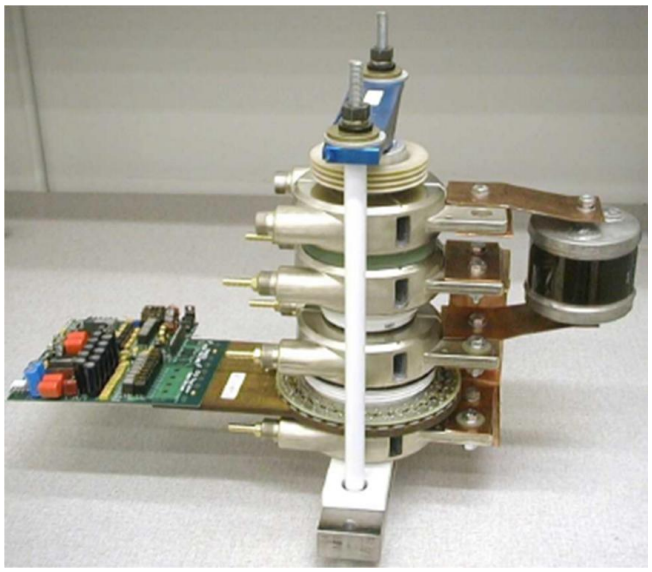

Figure 2.11: Prototype of an ETO based DCCB [36]

DC current measurement

Protection systems for AC applications rely upon current transformers to transform current to safe values, and also to provide electrical isolation. However, given that these devices cannot be used within DC systems, alternatives are required. In place of current transformers, devices such as Hall effect current transducers and Rogowski coils are often used, and more recently optical current transducers [40]. Use of these alternatives can in fact be advantageous from a protection perspective, particularly where highly dynamic currents may exist. First, under high rate of change conditions, current transformers may temporarily saturate and distort the output current [41]. The alternatives listed can be designed with a much higher bandwidth and therefore more accurately track large changes in current. A further advantage, is that the output from a current transducer will be in the form of voltage which facilitates easier integration with digital processing devices. Later chapters will illustrate how this characteristic can help enable very fast fault detection.

Fault containment devices

For cases where the isolation of faulted parts of a network using circuit breakers is either not possible or does not sufficiently protect the network components, fault containment or suppression devices can be used. These devices are often used to transiently suppress a network's fault response and can be used to protect against the impacts of both overcurrent and overvoltage. Examples of current and voltage suppression devices are discussed in the following sections.

Fault current limiters Fault current limiters (FCL) provide a means of reducing fault current to be reduced to a selected level rather than be dictated by the network. This has a number of advantages such as reducing the required circuit breaker ratings and stress on the system components during faults. Therefore the use of FCLs are one potential approach to tackling the issues of high fault levels and severe transients which DC systems can present. Two general approaches to current limiting have been identified; impedance based and switching device based current limiting. Examples of these are highlighted in the following sections.

Impedance based current limiters Both resistive [42] and inductive [43] FCL devices could could potentially be utilised within DC systems. Whilst not always considered for DC applications, inductive devices would reduce transient current magnitude and frequency, with minimal losses under steady state conditions. However inductive FCL devices would have the disadvantage of increasing stored energy in the network during the fault, potentially resulting in higher circuit breaker energy dissipation requirements and higher post fault overvoltages. This is demonstrated in Chapter 4.

Resistive devices have the benefit of being able to limit both continuous DC currents as well as transients within the network. Unfortunately this often comes at the cost of additional losses within the network. To minimise resistive voltage drop under steady state conditions whilst also providing effective current limiting, resistive FCLs are usually triggered 'on' at a threshold current, at which point they begin to develop a resistance and limit current. The behavioural aspect which separates these devices from the switching FCLs (described below), is that the development of resistance with current is an inherent property of the device. This lack of required external control leads to an intrinsically safer protection system.

Two candidate technologies have been identified which demonstrate this be-

havioural characteristic; superconducting [42, 44] and solid state devices. Superconducting FCLs (SFCL) operate by keeping a length of conductor in a superconducting state under normal conditions, reducing its impedance to close to zero. However any current passing through the SFCL with a magnitude in excess of its critical current causes heating within the device. Once the conductor temperature increases sufficiently, the SFCL transitions to a resistive state where it begins to limit current [45]. The cooling of the superconducting material is achieved through the use of cryogenics, as illustrated in figure 2.12. The necessity for cryogenics is a limiting factor for the use of SFCLs due to their size, cost and power consumption. This is a particular issue for size and weight critical applications such as aircraft.

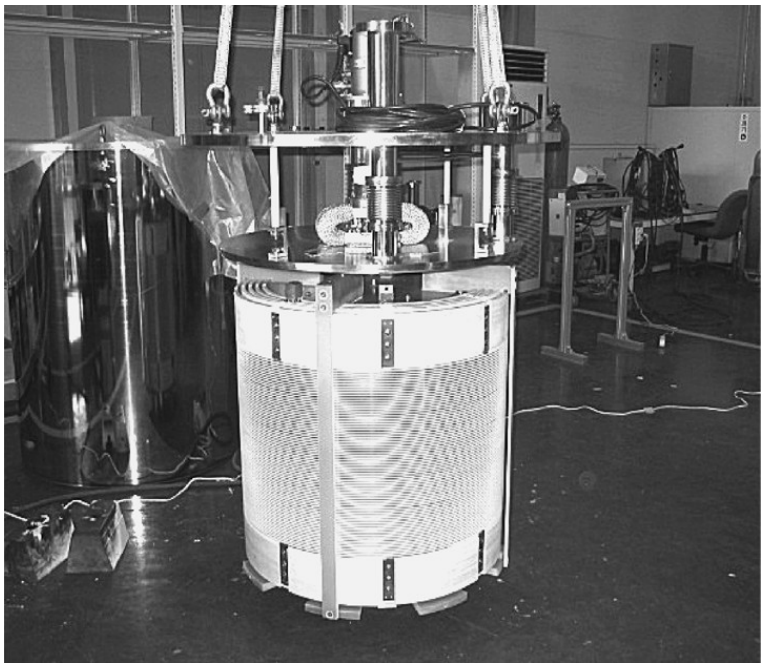

Figure 2.12: Cryogenic system with DC reactor [44]

Solid state options are also emerging which also intrinsically limit current. The device presented within [46] is a prime example of this, which is based on silicon carbide Junction Field Effect Transistor (JFET) technology. The device operates on a similar basis to the SFCL, where excessive currents lead to device heating, which subsequently increases its on-state resistance and reduces its saturation current; both of which help to limit through current. Whilst the current power ratings of these devices are still lower than required for many applications, their operating speeds and small size could potentially make them very useful within future DC applications.

Switching device based current limiters In addition to the intrinsic current limiters described in the previous section, some more active current limiting approaches have been proposed within literature. A key difference between these and the impedance based approaches is how their switching elements are employed. More specifically, impedance based devices act to limit current (which may facilitate the operation of lower rated circuit breakers) before any fault isolation occurs, whereas switching device based current limiters typically operate by switching something in or out of the network prior to current limiting taking place.

One example of this type of approach is shown within [47], which describes a fuse based current limiter named the Is-limiter. This device limits current by disconnecting or separating parts of the network, which acts to lower the available fault current. Options to achieve this include the separation of parallel network sections, effectively increasing the impedance of the separate sections, or the disconnection of distributed generation resources, as illustrated in figure 2.13. Given the Is-limiter uses fuses in its operation, it retains the fail safe operating characteristic of the impedance based current limiters. However this aspect of its design also mean that it is a 'one shot' device, meaning that the network would have to continue to operate in its degraded state even after the fault condition had been cleared.

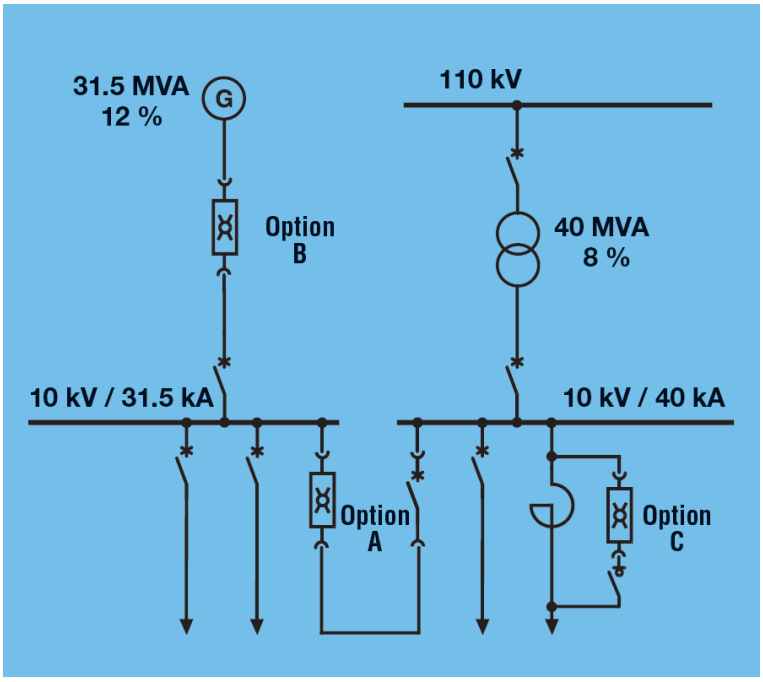

Figure 2.13: Application of Is-limiters [47]

Jin and Dougal [48] aim to achieve current limiting through a different means

and propose the use of a controlled solid state switch with which to control over-currents. The proposed approach is to connect a solid state switch in series with the rest of the network, with through current being controlled by the switching period of the switch, as illustrated in figure 2.14. Drawbacks of this type of approach include the voltage and current ripples generated by the current limiting actions as well as the on-state power losses of the solid state switches.

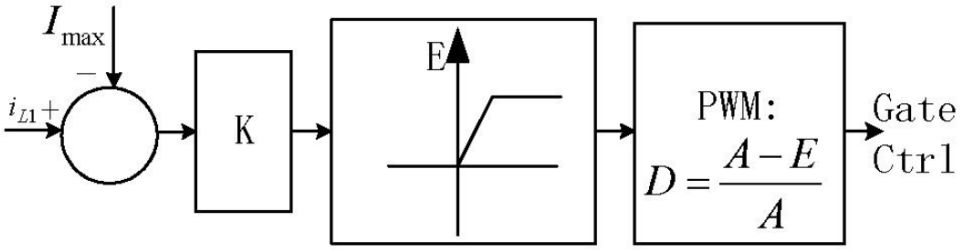

Figure 2.14: Pulse by pulse current limiting switch control circuit block diagram [48]

To overcome some of the issues associated with the on-state losses of solid state switches, hybrid current limiters can be utilised [38]. In a similar manner to hybrid circuit breakers, these combine fast mechanical switching elements with solid state elements, allowing the mechanical switch to carry current under normal operating conditions with minimal losses. Under fault conditions, the devices commutate current onto a solid state parallel path to enable current limiting to take place. Steurer et al [38] provide an example of how this can be achieved and their proposed hybrid limiter design is illustrated in figure 2.15. Within figure 2.15, the switch FTS carries the current in normal operation and the semiconductor block is an intermediate stage to commutate the current onto the positive temperature coefficient (PTC) resistor. As the current through the PTC resistor increases (and so raising its temperature), its resistance increases, which limits further rise in current. This gives an opportunity for switch LS to open and break the circuit under limited current conditions. Whilst this device primarily limits current for circuit breaking purposes, it does provide an example of how a hybrid approach to current limiting could be achieved.

Crowbarring An alternative means of limiting the current output from a generator or converter on to a network is to utilise a crowbar. A crowbar can be applied by either activating a physical crowbar on the source side [49] or by turning on the active switches within a leg of the converter (as will be illustrated within section 2.3) to create an internal crowbar [50], effectively providing the

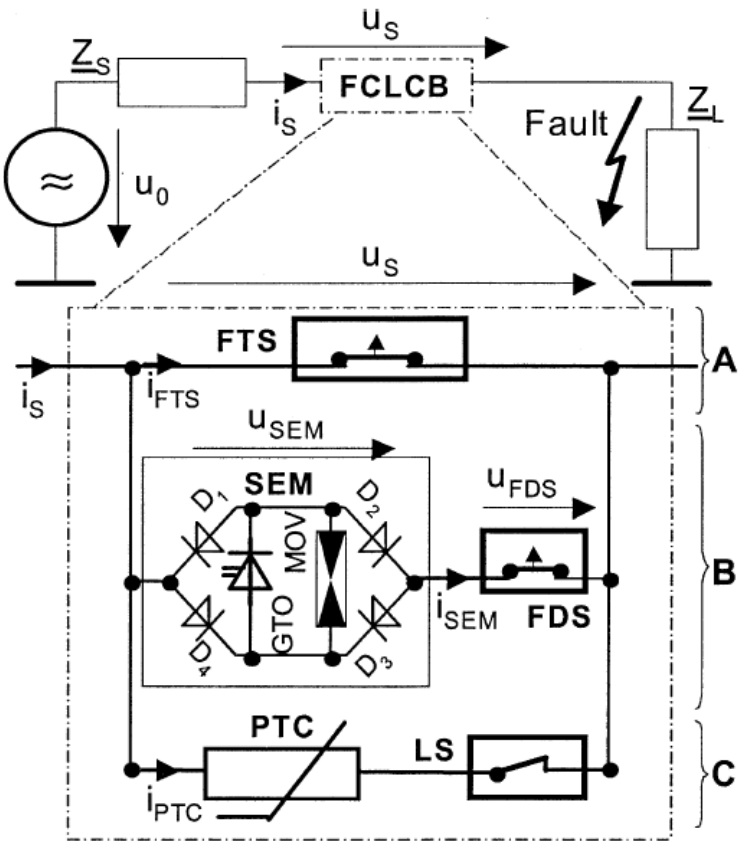

Figure 2.15: Hybrid fault current limiting circuit breaker [38]

converter with current limiting capability. The degree to which the crowbar could limit fault current would depend on the impedance of the crowbar itself and that of the fault path. Application of a crowbar would likely to lead a scenario where current is split between the crowbar and the fault. In any case, it is essential that the crowbar is capable of handling high currents for a sustained period, which may require the use of highly rated switches [50]. This requirement also applies to the source, which would be required to sustain an effective short circuit across its terminals without causing itself damage.

System integration issues The inclusion of fault current limiting devices into a traditional protection scheme can cause a number of problems. For many non-unit protection schemes, clearing time is proportional to the current seen by the device. By limiting current upstream of that device, this can lead either to the clearing time being prolonged or the non-detection of a fault. Effects of this may include extended periods of depressed of system voltage and the propagation of fault effects. These types of issues will be investigated further in later chapters.

One specific example of the types of FCLs discussed above impeding network

protection operation is presented within [51]. This study analyses the impact of integrating a SFCL into an AC network which primarily uses distance protection. It was found that the addition of the FCL in certain locations on the network, which limited the fault current to 2.25 pu, prevented the distance relay from detecting the fault. The operation of switching current limiters were also found to impact on the operation of distance protection, with [52] reporting that fast switching FCL could significantly change the Mho characteristic of the line.

Voltage suppression devices Voltage suppression devices are often employed within various electrical applications to provide protection against high magnitude voltage transients which can be potentially damaging to the power electronic converters and other sensitive equipment types found within these networks [53, 54]. A number of established technologies exists with which to provide this protection. One example of this type of device is a surge arrestor. A surge arrestor operates by rapidly decreasing its internal impedance when the voltage across its terminals exceeds a threshold level. This behaviour is illustrated within figure 2.16, which shows a typical V-I curve for a surge arrestor.

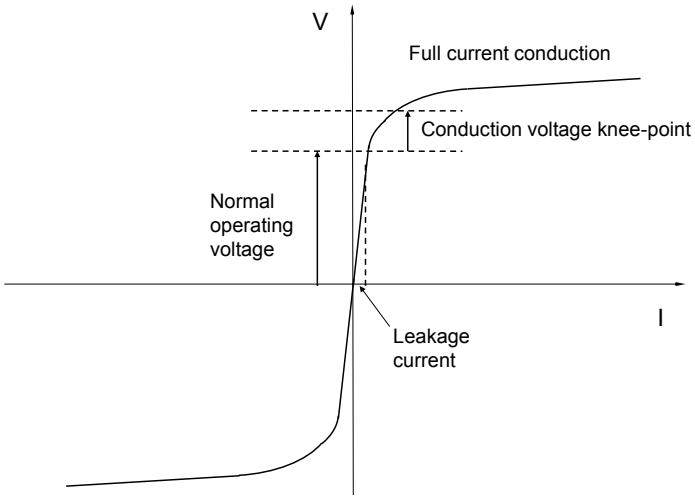

Figure 2.16: Typical surge arrestor V/I response

Whilst initially designed for lightning protection of land based power systems [55], these types of devices could have an important role in the protection of future DC power systems, particularly given the potential for fault clearance related transients (an issue discussed in later chapters). Indeed, a Raycap StrikeSorb 80-20 surge arrestor [55] (of which a cross sectional diagram is shown in figure 2.17), was fitted to the Engine Systems Validation Rig (ESVR) [34] (a practical DC demonstration rig) for the protection of converter interfaces.

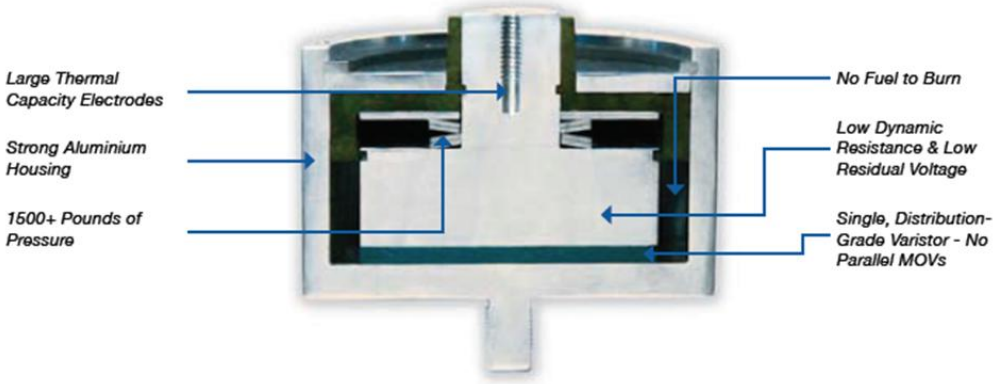

Figure 2.17: Cross Section of a Raycap StrikeSorb surge arrestor [55]

2.3 DC power network converter technologies

The adoption of DC distribution necessitates an increased penetration of power electronic interfaces within a power system, as is highlighted within the review of architectures in section 2.1. The converter interfaces utilised within these networks can have a significant influence on the fault response of these networks and hence standard approaches to the protection must change in order to accommodate these differences. This influence can vary widely, depending on the topology of converter, its filter requirements and its control strategy and examples of this will be shown within this section. As such, the precise impact converters have on the fault response of these networks is often difficult to quantify.

This section aims to simplify this problem by distinguishing different converter topologies based on their general fault response. There are two key behavioral components which influence a converter's response to network fault conditions; first, the extent of the converter's fault current limiting capability and second, the filter requirements of the converter (and hence the natural response of its passive components to a fault). As the work is set in the context of a DC system, the size of the capacitive filters is specifically considered as these have been identified as a source of potentially significant fault current [14, 56]. The following sections will first review some standard converter topologies, highlighting how different aspects of their design can alter their fault response.

2.3.1 Review of active converter topologies and types

In order to establish the different categories of converter which may be utilised within DC networks, this section considers the response of converters at a functional level. It is considered to be outwith the scope of the section to perform a detailed analysis of each converter's fault response (although this will be carried

out for specific cases in later chapters), particularly given the massive number of converter topology options which exist. The intention at this stage is rather to draw out the key characteristics of a converter's design which impact its response under network fault conditions, from which any potential protection system issues can be inferred. Specific categories for converter type are then defined based on these characteristics.

Six-switch voltage source converter topologies

The six-switch topology is relatively standard for a Voltage Source Converter (VSC) and this is the topology adopted within much of the literature for DC networks. Examples of this are shown in [12, 14, 57], although VSCs are more limited for use in motor drives within aerospace applications at present [58, 59]. VSCs have a number of advantages compared to more conventional line commutated, current source converters or passive devices. General advantages include: better output power quality, improved system stability, ability to feed power into passive networks without local power generation [60]. Additionally, VSCs do not require to reverse voltage polarity to reverse power flow and have no restriction on multiple infeeds [61]. These factors are particularly important for their use in multiterminal DC networks. The standard VSC topology consists of six turn off switches (which are often IGBTs), with antiparallel diodes connected across each of the switches, and a capacitive output filter, as illustrated within figure 2.18.

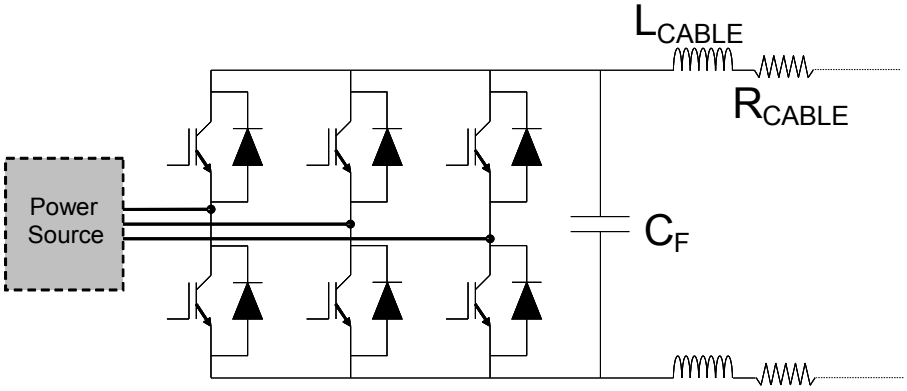

Figure 2.18: Standard six switch VSC converter

The topology of the six switch VSC converter is such that significant capacitance is often required to achieve sufficient levels of power quality [12, 62]. This capacitance, C_F within figure 2.18, is also required to provide a back-biasing voltage across the antiparallel diodes to prevent conduction under normal operation. However, under DC network fault conditions, this voltage may be lost. Under

these conditions, the diodes would begin to conduct and the converter would be unable to block the flow of current to the fault [57, 62].

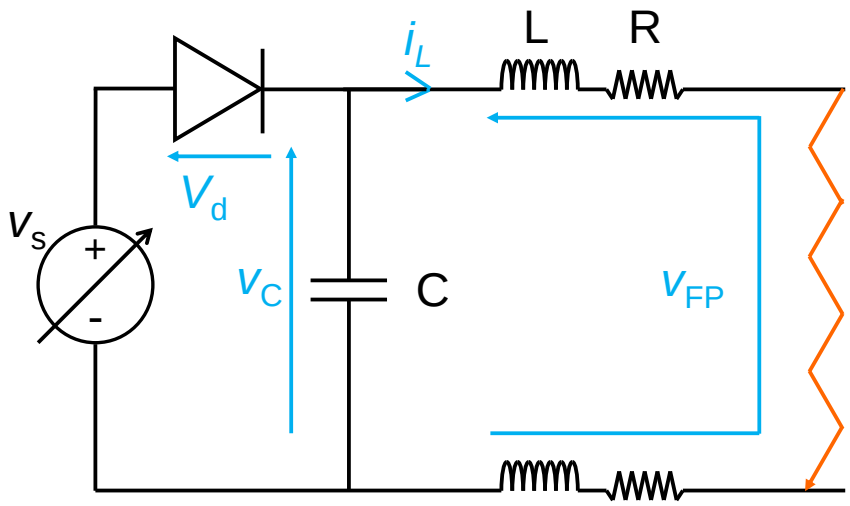

Figure 2.19: Simplified circuit highlighting the antiparallel diode conduction path and back biasing voltages for a VSC

This situation occurs when voltage on the source side exceeds the network voltage by more than the diode switch-on voltage. This is illustrated in the simplified circuit in figure 2.19. From this figure, the fault conditions under which diode conduction occurs are

$$Z_{FP} \times i_L \leq V_S - V_d \tag{2.1}$$

where Z_{FP} is the impedance of the fault path (including the line and fault), I_{CONV} is the converter output current and V_D is the on-state voltage of the antiparallel diodes in the converter. Equation (2.1) highlights that the level at which the converter can continue to control current is highly dependent on the impedance of the fault path. For compact systems with relatively low voltage drops on the conductors, it is clear that this control would be lost in the majority of fault conditions, and would only be retained where the fault itself had reasonably large impedance. This is particularly problematic as the fault current withstand of VSCs is low compared to more robust thyristor based converter topologies [12,14]. Therefore current must be limited or interrupted much more quickly to prevent damage to internal components when supplying fault current, within 2ms in some cases [12].

Previous work has also highlighted that the fast discharge of capacitors used as filters on the DC terminals of the VSC can damage both the capacitors themselves

and any other sensitive components in the fault path [14]. Furthermore, [62] illustrates the potential for voltage reversal if DC side faults are not cleared within an adequate time frame. The voltage reversal can cause significant currents to flow through converter freewheeling diodes, causing damage to these devices. These aspects of the converter's transient fault response will be investigated in depth throughout this thesis.

Two switch buck-boost DC/DC converter

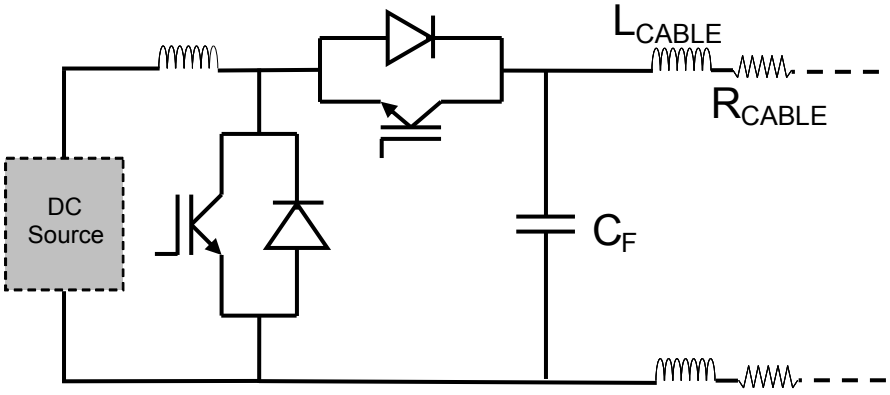

Figure 2.20: Two switch buck-boost DC/DC converter topology [63, 64]

Figure 2.20 illustrates the topology of the conventional two switch buck-boost DC/DC converter, a converter which has been proposed for use to interface energy storage elements to a DC network in electric vehicle and aerospace applications [63, 64]. This type of converter has similar characteristics to that of the VSC, requiring large filter capacitance (which can be prohibitively large in some cases [65]) and containing antiparallel diodes. As with the VSC, the location of these antiparallel diodes means that if output voltage was lost, the diodes would conduct current. As the converter switching elements would be bypassed, it could no longer control current magnitude.

Interleaved DC/DC converter

The design of the interleaved DC/DC converter has evolved from the conventional two switch converter and enables a reduction in converter size and an increase in efficiency and reliability [65]. An example the interleaved DC/DC converter topology is illustrated in figure 2.21.

The key benefits of the interleaved design are derived from the converter's parallel switches and coupled inductors, which reduce the burden on the capac-

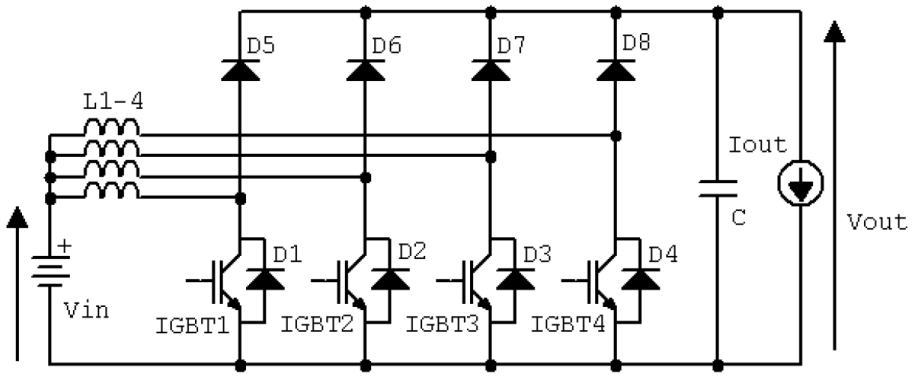

Figure 2.21: Interleaved 4-channel boost DC/DC converter [66]

itive output filter, enabling a reduction in its size. The extent to which these filtering requirements can be reduced is partly dependent on the number of parallel channels utilised; an increase the number of channels will decrease output voltage ripple [66]. The performance improvement through the use of an interleaved topology does however come at the cost of additional inductors and power switching devices [65]. Furthermore, the location of the diodes within this converter topology is such that they would be unable to block current during loss of DC side voltage, as with the previous converter types.

Fault tolerant VSC topologies

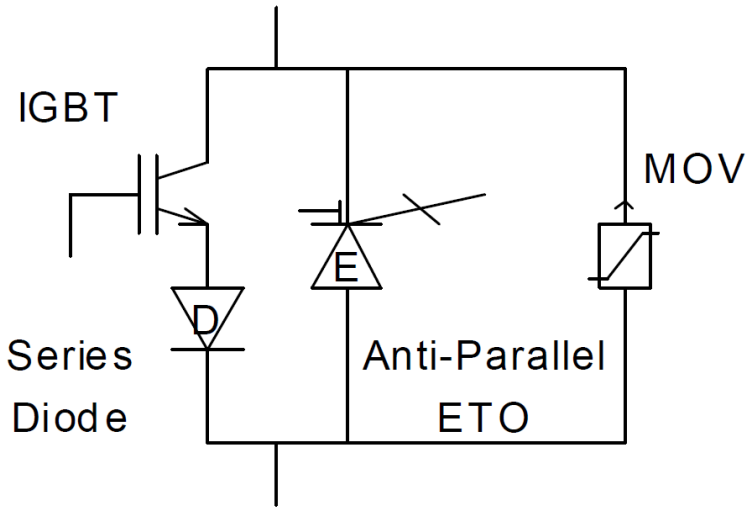

Figure 2.22: Switch realisation with IGBT and anti-parallel ETO device [67]

Figure 2.22 illustrates a modified version of a single switch segment of the standard VSC design, and has been proposed within [67]. The design has been modified to replace the antiparallel diode with a turn-off device; in this case an

emitter turn-off (ETO) device has been selected, the design of which is described in [36]. Furthermore, a metal-oxide varistor (MOV) has been connected in parallel to suppress voltage transients across the converter during switching events. The primary purpose of replacing the antiparallel diode is to prevent the constant conduction of these diodes following the loss of the back-biasing DC voltage. The usually turned on ETO gives the converter the capability to limit or interrupt current, albeit at the cost of increased conduction loss in the antiparallel diode path. As the capacitive filter is located on the DC side of the converter, the discharge phase the fault response remains, however the topology change enables control of the secondary fault infeed from the AC side.

Whilst this topology would add some cost and complexity to the converter design compared to the standard VSC, it does serve as an example of how a converter can be used to limit current into a faulted DC network.

Multilevel and modular multilevel VSC topologies

The application or proposed application of multilevel VSCs has so far tended towards medium or high voltage applications, such as the multiterminal DC schemes presented within [60, 61, 68–71].

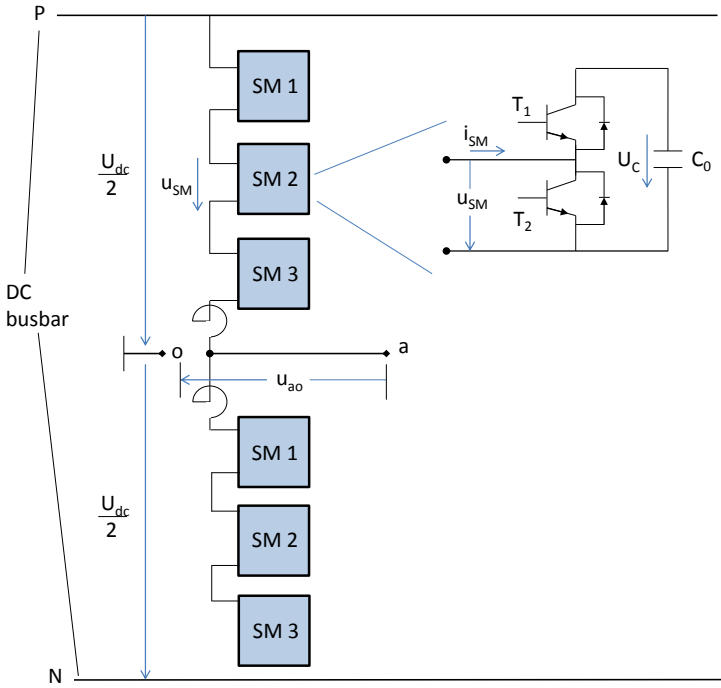

Figure 2.23: Single phase diagram of the modular multilevel VSC [71]

One of the main benefits of multilevel converter designs is the capability to produce a DC output with low harmonic content, though this is at the cost of

additional switch components. This enables filter requirements to be minimised, potentially alleviating the protection problems which stem from the converter's natural response. Modular multilevel designs, an example of which is illustrated within figure 2.23, take this a step further by removing the central bus capacitance and instead distributing it between the different converter levels. In certain module configurations, this enables blocking of the capacitive discharge part of the fault response completely.

However the potential for application of these types of converters to lower voltage and more compact applications remains unclear, with cost, complexity and power density likely to count against their utilisation in the short to medium time scales. These converters do however provide an example of a design which has minimal filter requirements and current limiting capability.

Converter type categorisation

From the review within previous sections of the key behavioral components, converter type has been classified in four ways:

1. Non-current limiting - high capacitance
2. Current limiting - high capacitance
3. Non-current limiting - low capacitance
4. Current limiting - low capacitance

Examples of these converter types are shown above. Standard VSCs fit into the 'non-current limiting - high capacitance' category, whereas a topology such as the interleaved DC-DC converter is representative of a 'non-current limiting - low capacitance' converter. Within these categories, the terms 'high' and 'low' capacitance are somewhat imprecise, however the intention is to capture cases where, and where not, the current contribution from the capacitive filter significantly contributes to the overall fault current. From the examples above, 'high capacitance' is in the order of millifarads and 'low capacitance' is in the order of microfarads. The unique set of challenges associated with their protection of each of these four converter types are first introduced in the following sections before being explored in more depth in later chapters.

2.3.2 Impact of converter interface type on the protection requirements

As the previous section highlights, changes in converter topology can affect the fault response in a number of ways. The following sections will generalise this impact under the derived converter categories, assessing both protection issues which may result from a specific converters use and potential protection solutions. The section goes on to discuss potential design trade-offs between converter and network protection.

Non-current limiting - high capacitance converter types

Protection issues A number of protection issues have been identified within the literature for 'non-current limiting - high capacitance' converter types, some of which have been touched upon within earlier sections. For clarity these issues are summarised below:

- High magnitude current discharge of capacitors can potentially damage sensitive components in the fault path or even the capacitors themselves [14,36].
- A large difference between the initial fault current peak, as produced by the discharge of filter capacitors, and sustained fault current produced by converter interfaced generators can cause significant problems for the coordination of the network protection [56].
- Rapid undervoltage conditions created by the discharging filter capacitors has the potential to cause internal protection of power electronic converters throughout the network to operate [34], resulting in poor protection selectivity and the propagation of fault effects.
- Oscillations between inductance and capacitance in the circuit can cause the voltage across the converter's filter capacitor to become negative. This has the potential to cause significant currents to flow through the converter's antiparallel diodes, presenting a risk of the diodes being damaged [62].

For networks containing these converter types to be effectively protected, these issues must be accommodated. Potential options identified within literature to overcome these significant challenges are discussed below.

Potential solutions The protection issues outlined in the previous section are very challenging to overcome. Whilst there are examples within literature which tackle aspects of the problem, a single solution does not yet exist. One potential solution, as proposed in [56], looks to overcome the fault detection and discrimination issues by operating protection on the sustained fault current input from the network converters. This however requires network components and protection devices to withstand the initial fault transients as well as extended fault clearance times, and so necessitates the use of more robust converter switches and diodes and protection devices. This would potentially impact the overall cost, size and weight of the electrical system and increase energy dissipated at the point of fault. An alternative solution, as proposed within [14], is to operate protection during initial transients, based on instantaneous overcurrent trip at a capacitor's output, in order to protect capacitors and other network components. However the solution, as currently proposed at least, is at the expense of wider fault discrimination, which would not be acceptable within all applications. Further details on these two approaches are provided within section 2.4 and potential methods of implementing this transient interruption approach in a more coordinated manner are presented within later chapters of this thesis.

Non-current limiting - low capacitance converter types

Protection issues Due to the low capacitive filter requirements of the converter type considered within this section, the potential for component damage and poor protection system discrimination as a result of large capacitive discharge currents is less of an issue. However one transient protection issue that this converter type has in common with the higher capacitance converter types is the potential for voltage reversal if DC side faults are not cleared within an adequate time frame. In fact, the lower capacitance at the converter terminals may accelerate the occurrence of the voltage reversal scenario as less transient voltage support is offered to the DC network. Methods to quantify operating requirements based on this characteristic are presented within later chapters.

One further protection consideration which must be made when utilising low capacitance converters is their susceptibility to overvoltage transients given the smaller available transient energy storage at the converter terminals. It is therefore important to ensure that these converters are neither damaged by these voltage transients nor caused to disconnect from the network due to overvoltage protection operation, either of which events could result in the effects of the fault expanding beyond the initial point of inception. This subject is also explored in

more detail within later chapters.

Potential solutions Whilst the lower capacitance of the converter filter has made the initial fault transient less severe, the potential for voltage reversal transients to occur across the converter terminals still remains. Therefore the requirements of the protection system remain similar to that previous; either design the system to withstand the expected transients, which in the case of voltage reversal could involve using diodes with higher rated transient current withstand, or operate protection to isolate the fault before the severe transient develops, which would be in a similar time frame to that discussed above.

Potential solutions to avoid these overvoltages, include the use of voltage suppression devices and the utilisation of converter components that can withstand these voltage transients. These, as well as more active solutions to the prevention of overvoltage, are presented within Chapter 4.

Current limiting - high capacitance converter types

Protection issues At a high level, the protection issues which exist for this converter type are similar to those of the 'non-current limiting - high capacitance' converters. As high capacitance is common to the two converter types, there is also the potential for high magnitude current transients immediately following fault inception as the current flow from the capacitive source is unaffected by converter topology. Another issue this converter type has in common with the non-current limiting case is the potentially large difference between the initial fault current peak and the sustained fault current produced by the converter. The extent to which this differs between the two cases depends both on the level to which current is limited and the capacity and fault response of the source connected at the source side of the converter. However it is anticipated that any fault discrimination issues would be more pronounced where a converter was limiting through-current.

One area where a current limiting topology may be particularly beneficial is in its response to voltage reversal effects, although these benefits would depend on how current limiting is realised. For the example topology shown in figure 2.22, the replacement of antiparallel diodes with ETOs would enable the current induced by the negative voltage to be interrupted when desired.

Potential solutions As discussed previously, no single definitive solution yet exists for the protection of networks containing large capacitive filters. For this

converter type it would be desirable to operate protection on the capacitive current, both to mitigate the impact of this transient and to avoid discriminating fault location based in the limited converter contribution, as this could lead to the fault remaining on the system for longer than necessary. As stated, options to achieve this performance are discussed within later chapters.

Current limiting - low capacitance converter types

Protection issues The fault response of 'current limiting - low capacitance' converter types is the least severe of all the converters considered, and despite initial capacitive discharge and voltage reversal conditions still occurring, these should not cause significant issues for network protection. A challenge which does remain is the accurate and timely discrimination of fault location. This is a particular issue for this converter type due to the lack of any significant fault current source which would indicate the presence or location of a fault [17].

One additional issue is the potential for overvoltages due to fault clearance transients, as reported previously. However the probability of these would be reduced compared to the 'current limiting - low capacitance' case due to the expected lower breaking currents.

Potential solutions Given that this converter type places no unique demands on the protection system, such as the necessity to mitigate high magnitude transients, it is anticipated that standard protection approaches, as outlined in section 2.2, could be utilised. The only limit on this would be whether overcurrent based approaches could achieve acceptable detection times under the low fault current conditions. If not, more selective approaches, such as current differential protection may be required.

Trade off between converter interface and protection system design

One general theme coming out of the previous sections is that the more complex the converter design, i.e. those with the greater number of components and switches, the lower the requirements on the protection system. This presents an interesting system design trade off, where the size and rating of protection devices would vary with that of the converter type within the network. Tables 2.1 and 2.2 attempt to summarise these protection system and converter design factors respectively. These are particularly relevant given the number of competing design objectives within the particular application's power system as discussed in section 2.1.

Table 2.1: Summary of protection issues associated with the different converter types

	Non-current limiting	Current Limiting
High capacitance	**1.** Require faster fault detection and interruption or high system tolerance **2.** Fault discrimination challenging	**1.** As across **2.** As across **3.** Minimises effects of voltage reversal
Low capacitance	**1.** Greater voltage oscillation and potential for voltage reversal **2.** Susceptible to overvoltage transients	**1.** Fault discrimination challenging

Table 2.2: Summary of converter design requirements associated with the different converter types

	Non-current limiting	Current Limiting
High capacitance	**1.** Simple design **2.** High withstand requirement	**1.** Higher switch count (turn off freewheel path) **2.** Increased switching losses
Low capacitance	**1.** Minimal voltage support on bus requires tight control **2.** High withstand requirement **3.** Higher switch and component count	**1.** Higher switch and component count

In order to capitalise on any design benefits associated with optimising the converter and protection system design it is first necessary to quantify the impact of different protection operating strategies on the system. From table 2.1 and the previous sections, it is clear that the most onerous protection issues are presented through the use of 'non-current limiting - high capacitance' converters. However this converter types design tends to be the simplest, which may reduce converter weight and cost and so have benefit the overall system design. Therefore, in order to derive the greatest benefit of an effective protection system, the remainder of this thesis will focus on this converter type, and in particular the standard VSC design, and aim to tackle the protection issues it presents. It should however be noted that the analysis presented in later chapters is equally applicable to the described alternative converter types.

2.4 Assessment of significant literature

In addition to the concepts and technologies introduced already within this chapter, there are specific pieces of literature which are worthy of individual consideration. These provide both context for work presented in later chapters and further justification for why it was considered important to carry out. Only a small subset of available material is reviewed in the sections below, however literature found to be relevant is referred to where appropriate throughout this thesis.

2.4.1 BS EN/IEC 61660-1:1997

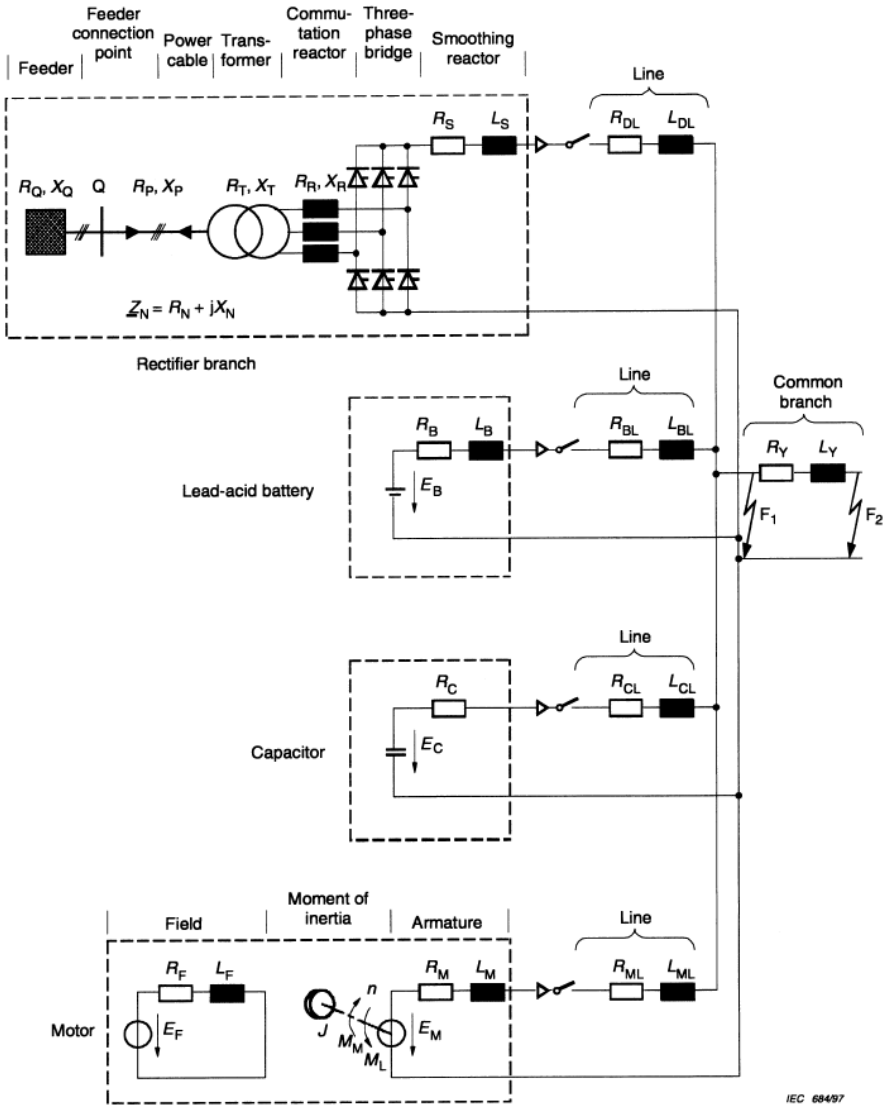

Figure 2.24: BS-EN/IEC 616660-1 standard equivalent circuit for fault current calculation

The BS-EN/IEC 616660-1 standard [72] describes methods of quantifying the protection requirements for DC auxiliary power supplies within substations. Although this application area is significantly different to that primarily considered within this thesis, the standard does consider the fault response of similar components, with the most applicable being capacitors and batteries. Given that no equivalent standard yet exists for the types of systems considered, this is the most comprehensive DC system protection standard, particularly when considering the connection of multiple parallel fault current sources. Of most relevance to this thesis is the part of this standard which addresses capacitive fault response and this will be the focus of this review.

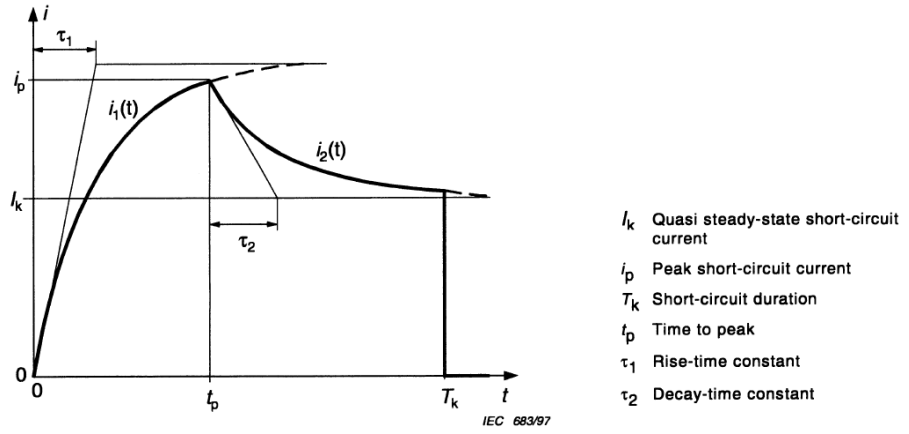

Figure 2.25: BS-EN/IEC 616660-1 standard fault current approximation function

For the type of system addressed in the standard (illustrated within figure 2.24), the fault response from the AC side of the converter (in this case the main grid) can be much more substantial compared to the systems considered within this thesis and therefore the capacitive fault current contribution is less significant in terms of overall network fault response [35]. As a result of this, the level of detail in which the capacitor response is considered is reduced. This has the impact of disguising some potential protection issues when applied to VSC connected systems.

Two main examples of this within the standard have been identified. First, in calculating capacitive fault current the standard effectively averages the decay period of the current response following the capacitive current peak (shown as $i_2(t)$ in figure 2.25). The impact of this is that the calculated response would neither capture periods of freewheel diode conduction or ongoing current oscillations. Means of achieving this are described in Chapter 3.

An additional shortfall of this standard is the inaccurate representation of

parallel capacitive sources. This is due to oversimplication within the standard, where fault current contribution is first calculated individually from sources, assuming series connection between source and fault. For common branch faults (illustrated within figure 2.24) calculated currents are then subsequently corrected to account for parallel connection using resistive current division. This approach ignores the effect of inductance in parallel lines on this current division.

The error created by this omission is highly dependent on the inductance in series with the particular source being assessed. An example within [73] highlights that the magnitude of smoothing reactor and internal battery and motor winding inductance dominates that of the line. Therefore the change in total loop inductance (series plus combined parallel branches, where the parallel element will tend to the smallest inductance, i.e. the common branch line inductance) will be negligible and so the approach will be acceptable for these source. However, given the typically small magnitude of capacitor ESL, line inductance is far more important in determining the capacitive fault response, as later chapters will emphasise. Hence the simplified approach taken within the standard would potentially create large errors when multiple capacitive current sources exist.

2.4.2 The status of DC micro-grid protection

The work presented by Cuzner and Venkataramanan [56] reviews the current literature and technologies within the area of DC microgrid protection. There are two aspects to the paper which have particular relevance to this thesis. The first is the stipulation of protection system requirements and key protection system design criteria, which has already been discussed in section 2.2.

More specific to DC protection, the paper reviews the capabilities of current and future protection devices and challenges for their implementation. In a review of circuit breaker devices, the paper focuses on the inadequacies of moulded-case circuit breakers (MCCB) for providing coordinated protection system operating in DC applications. When these devices are utilised in systems with capacitive fault current sources, the initial discharge current can be high enough to occupy the instantaneous trip region of multiple series connected MCCBs. The impact of this could be to cause upstream and downstream protection devices to operate simultaneously, or even just the upstream device. This would cause significant protection coordination issues and unnecessary isolation of non-faulted elements of the system. Recognition of this behaviour has led the authors to conclude that the implementation of graded overcurrent protection is virtually impossible unless the protection scheme can ride through the initial capacitive discharge.

This position is supported with a more depth study within Chapter 5 of this thesis.

The main weakness of this paper is that the challenges are only described at a high level. Therefore the paper does not sufficiently quantify the technical challenges to enable the benefit of any proposed solutions to be effectively assessed. This shortfall is addressed within this thesis through the detailed analysis of fault response and quantification of fault detection and circuit breaker operating times.

2.4.3 Overcurrent protection on voltage-source-converter-based multiterminal DC distribution systems

The work presented by Mahajan and Baran within [14] represents one of the most comprehensive efforts to design a protection scheme for a VSC interfaced network. It recognises some of the problems with capacitive fault response within compact networks, in particular the potential damage to the capacitive components and sensitive components within the network. The paper also recognises the protection issues in using VSCs (as highlighted in section 2.3), namely the lack of control under DC fault conditions due to freewheeling diode conduction. For both of these issues, the paper presents potential solutions which are discussed below.

For the issue of capacitive discharge, the authors in [14] propose the use of instantaneous overcurrent protection inherent in power electronic switches to interrupt capacitive discharge currents. This is achieved through the connection of an ETO device in series with the capacitive element, as illustrated within figure 2.26.

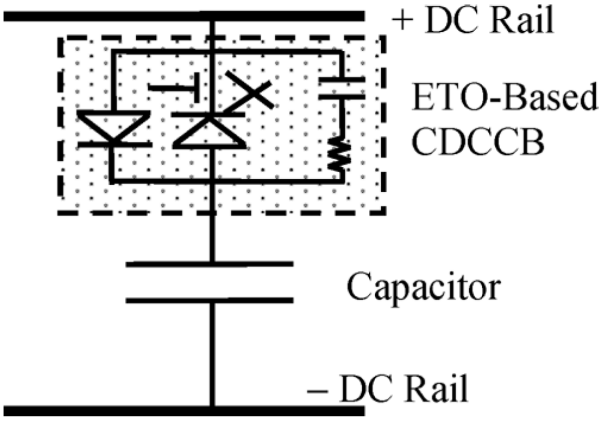

Figure 2.26: ETO based capacitive discharge circuit breaker [14]

Whilst this approach is suitably fast acting to solve the issue of capacitive

discharge for the network described within the paper, the approach is far less effective when higher levels of protection selectivity, that is, ensuring that only the local protection operates for a fault at a particular location in the network, are desired. In these cases issues can arise in the implementation of overcurrent protection, especially where instantaneous overcurrent protection is utilised. For example, given the limited circuit breaking capability of the power electronic circuit breaker, instantaneous overcurrent protection located at a filter capacitor output could potentially lead to the isolation of this capacitor for more distant faults, due to the high initial fault current. This would lead to the uncoordinated tripping of this capacitor's breaker (when downstream protection should isolate the fault instead) and delayed or non-tripping of load protection due to the removal of the main fault current source. Furthermore, power quality may be degraded for the period of capacitor disconnection. Coordination of protection for these types of network is a subject area explore in detail in later chapters.

To prevent the conduction of freewheeling diodes following the loss of DC voltage, the paper proposes the use of the fault tolerant VSC already illustrated in figure 2.22 within section 2.3. Drawbacks of this solution (as discussed in previous sections) include the additional cost and complexity of converter design as well as potentially causing fault discrimination through the limitation or interruption of fault current.

2.4.4 Protection of low-voltage DC microgrids

The final piece of literature which merits specific discussion at this stage is the work presented by Salomonsson et al. [12], which describes the design of a DC microgrid protection scheme mainly based on the use of commercially available protection devices.

Information of particular value within this paper is the identification of the limited current withstand of VSCs. This impacts on the required protection system operating time, which is claimed to be around 2ms following the occurrence of a short circuit network fault in order to prevent damage to freewheel diodes contained within the VSC. More generally, the paper provides a detailed DC microgrid architecture (shown in figure 2.2 within section 2.1) with relevant component and device data. This has been utilised within Chapter 5 to perform a protection study within a DC microgrid environment.

Two significant shortfalls have been identified from the work presented within this paper. The first relates to the proposed application of MCCBs within the DC network. As reported previously, Cuzner and Venkataramanan [56] iden-

tify potential issues using these devices within highly capacitive networks, issues which do not appear to have been considered within this paper. The second shortfall of this paper relates to the analysis of fault response, and in particular that of the VSC's capacitive filter. The approach taken within the paper was to neglect inductance between the capacitor and fault, both for developed models and equations. This leads to a massive, peak current instantaneously following the occurrence of a fault and will cause inaccuracies within the proposed detection methods, such as those based on derivative current. Analysis within later chapters of this thesis highlights the significant impact that inductance has on the capacitive fault response and why it important not to neglect.

2.5 Areas identified for research

From the assessment of relevant literature and technologies it is clear that no established protection approaches exist for the protection of converter interfaced DC networks. This is particularly true of network's containing high capacitance converter types, where the potential for extremely large transient currents can create challenging conditions for effective network protection operation. As discussed in section 2.3.2, proposed protection approaches range from adopting standard protection methods [56] (provided the network components are suitably robust to withstand high magnitude transients) down to the immediate (within microseconds) interruption of overcurrent transients [14]. In order to bring greater clarity to how these protection issues should be tackled, as well as make a novel contribution to the research field, two clear opportunities for future research have been identified.

First, an opportunity exists to develop a set of tools to enable a converter interfaced DC network's fault response to be readily determined and analysed. In particular, a detailed analytical study would allow the key factors impacting on a fault response to be identified. Developing a detailed understanding of converter interfaced networks' fault response in this way would enable a more general approach to defining protection system operating requirements, aiding the creation of relevant standards, and reduces the reliance on the simulation of specific network models. Contributions related to this are reported within Chapters 3 and 4.

Second, an opportunity exists to better coordinate fast acting network protection and better integrate modern circuit breaker technologies. In particular, there is an opportunity to develop fast fault detection methods based on an un-

derstanding of the initial fault response. With the exception of [14], none of the reviewed literature attempts to operate protection in a coordinated fashion during the capacitive discharge period (and in the case of [14] protection discrimination is limited). The reasons for this are mainly a matter of DC network and technology maturity. For example, issues such as capacitive discharge have only developed due to the recent increase in the use of active converter technologies. Furthermore, the lack of appropriate circuit breaker technologies with which to operate protection within such a short time frame has meant that opportunity to achieve this performance has been limited until now.

However, fault detection based on the initial transient response could be particularly beneficial for system operation as it would enable protection to operate in the early stages following a fault, potentially minimising: energy delivered to the fault, stress on components, current being interrupted and subsequent post-fault transients. Furthermore, having the ability to detect faults from the perspective of the DC side of the converter has the added advantage of being least dependent on AC network conditions and configuration as well as converter design and control strategies. Therefore any protection solution developed to primarily operate on the natural response of DC side filters, as opposed to the controlled converter output, could be more generic and deployable within multiple applications. Means of very rapidly detecting faults and coordinating protection system operation based on this type of approach are investigated in substantial detail in later chapters of this thesis.

2.6 Chapter 2 summary

This chapter introduces a number of fundamental concepts in the design and protection of DC networks. It first introduces the types of network architectures considered for current and future DC applications, highlighting how the development of active power converter technologies is enabling the wider utilisation of DC distribution. State of the art of DC protection methods and technologies are also introduced and it is discussed how the development of fault current limiting and solid state technologies may lead to a fundamental change in how future networks are protected. The pertinent converter types which may be employed in future are identified and their potential impact on system protection was established. Finally, the key references within the field are reviewed to highlight current gaps within the literature.

From this review of relevant literature and protection technologies, several key

conclusions were drawn. First, the use of high capacitance converter types create the most challenging protection requirements. However given the simplicity of their design compared to other converter types, their use would be more desirable from a network design perspective. Therefore the remainder of this thesis will focus on the development of protection solutions for this converter type, and in particular the standard VSC design, to derive the greatest benefit of an effective protection system.

Second, it was concluded that in order to accurately define the requirements of network protection, a detailed understanding of converter interfaced networks' fault response is required. To enable this understanding, a set of analytical tools should be developed with the purpose of quantifying key factors impacting on a fault response.

Third, it was concluded that to better coordinate fast acting network protection and integrate modern circuit breaker technologies, methods capable of detecting and discriminating faults based on the initial transient response of the network are required. These points are addressed within the following chapters.

The work presented in this chapter contributed to three publications (including two journal publications), the details of which are shown in [74–76].

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Chapter 3

DC system transient response during faulted, fault clearance and post fault conditions

Chapter 2 identified that in order to develop general approaches to defining protection system operating requirements, there is a need to develop an analytical approach to accurately assess a converter interfaced DC network's fault response. To help meet this need, an analysis of the natural fault response of power electronic fed, compact multiterminal DC power distribution networks, typical of those proposed for future aircraft, ships and microgrid platforms will be presented. Key factors such as the peak magnitudes and formation times of fault current profiles are determined and quantified, as a function of network parameters, in order to establish the operating requirements for associated protection systems. Secondary fault effects such as voltage transients are also identified and quantified to illustrate the impact of suboptimal protection system operation. The system behaviour during fault clearance is then analysed in order to assess the impact of varying protection system operating time on the requirements of circuit breakers within a network. The chapter concludes with a section which validates these analytical solutions against an example network simulation.

The analytical tools developed and methods demonstrated within this chapter will be used throughout this thesis, both in the identification of protection system requirements and the assessment of protection methods within compact DC power systems.

3.1 Analysis of compact DC networks fault response

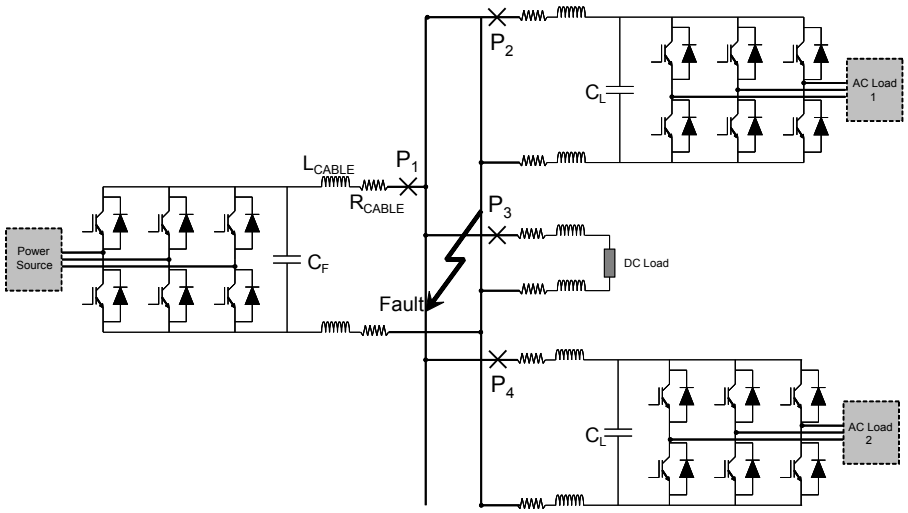

Figure 3.1: Example multiterminal DC network

This section will present analytical expressions to describe the typical fault response of compact DC networks. It will initially draw from methods presented in existing literature [1, 2], but will build upon these to more accurately reflect the specific characteristics of physically compact DC networks containing active converters.

To analyse the general fault behaviour of physically compact DC networks, consider the example network shown in figure 3.1. This network has specifically been designed by the author for a UAV application, however it can be considered to be representative of any of the busbar architectures proposed for alternative DC applications (see section 2.1). The network employs VSCs to interface sources and AC loads to the network, which utilise capacitive only filters as is often the case within multiterminal DC networks as highlighted within [3–8]. Table 3.1 presents the network parameters for figure 3.1. These parameters were selected as representative values and derived from a number of sources [9–11]. The response of the network is clearly sensitive to changes in these component values, with resistance and inductance of cables in particular likely to vary in a given network. Reference [2] provides some useful equations for the calculation of alternative values for different network configurations. Cable capacitance has been neglected from this network, and subsequent modelling and analysis, due to its small magnitude ([6] provides an example cable capacitance of $0.1nF/m$) compared to the filter capacitance around the network.

Table 3.1: Network Parameters

$Voltage$	P_{GEN}	P_{LOAD}	R_{CABLE}	L_{CABLE}	C_F	C_L	$C_{F_{ESR}}$	$C_{L_{ESR}}$
270V	20kW	6kW	0.801mΩ/m	0.65μH/m	10mF	0.5mF	5mΩ	79mΩ

Prior to developing analysis of the fault response for this type of network, it is worthwhile to first give an example of how this response may look. Considering the response to the busbar fault illustrated in figure 3.1, there are two main sources of fault current. For compact VSC interfaced DC networks, the discharge of the filter capacitors throughout the network typically dominates the fault current profile immediately following the fault, whilst the contribution from converter interfaced generation sources and loads (where applicable) forms the latter part of the response [2,3,12]. A simulation of this fault current is illustrated in figure 3.2. The network in figure 3.1 was simulated using the SimPowerSystems (SPS) simulation package within Matlab [13]. The converter interfaces are modelled in a functional fashion; the power source's output is modelled by a controlled current source (where network voltage is the control parameter and its magnitude is controlled around the nominal network voltage using a proportional-integral controller) with a parallel diode connected prior to its output capacitance to account for converter freewheeling diodes . Converter interfaced loads are modelled as parallel resistor-diode branches downstream of the converter capacitance.

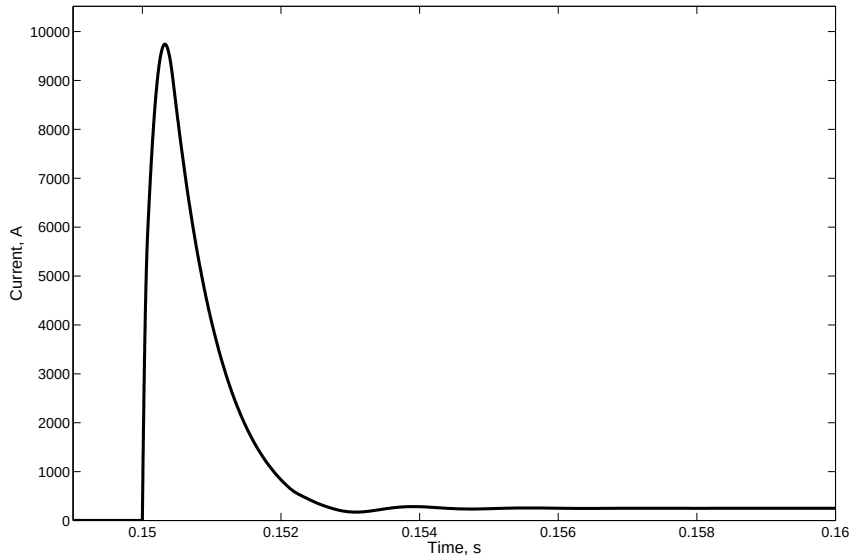

Figure 3.2: Simulated fault current for a short-circuit fault on the busbar at 0.15s

Figure 3.2 illustrates that the potential peak current resulting from the discharge of network capacitors is around 9.74kA without the operation of any protective devices. A fault response of this type can cause two major issues for

the protection of the network. First, a current discharge of this magnitude and rate of change has the potential to cause damage to both the capacitors themselves and any sensitive components in the network, such as power electronic switches [3, 14], as well as induce large short term electromagnetic forces on conductors [15]. Second, the peak of 9.74kA is approximately 130 times greater than the sustained converter contribution. Whilst this response will change with the network impedance characteristics, filter size and configuration and the converter and generation technologies employed, it is clear that such disparity between transient and steady state conditions will cause problems for the protection of the network. These aspects will be addressed in more detail in later sections.

Given the severity and dominance of the initial fault transient, the analysis within this chapter will focus primarily on the natural response of the DC network under fault conditions. This approach will characterise the capacitive discharge in the appropriate detail to aid in determining the electrical protection system requirements for future DC applications.

3.1.1 Analysis of capacitor discharge

Under short circuit conditions, charged filter capacitors act as high fault level sources. These capacitors, in conjunction with low impedance interconnecting cables (associated with the physically compact nature of the electrical systems considered), create conditions for rapidly developing and potentially severe short circuit faults, as figure 3.2 illustrated. This effect is less evident in other applications which utilise longer, higher impedance interconnections, as the analysis will highlight.

The typical fault current profile from discharging capacitors can be described by considering the natural response of an equivalent RLC circuit (see figure 3.3) with appropriate initial capacitor voltage and inductor current representing pre-fault network operation. Equivalent second order circuits and expressions are used throughout the analysis in order to best illustrate behaviour and derive the parameters of interest. Expansion of the analysis to cover multiple RLC branches can result in much larger analytical expressions with which it becomes far more difficult to usefully derive parameters. For these higher order expressions, [16] early substitution of parameter values is recommended (an example is provided within [16] to emphasise this aspect).

The natural response of the RLC circuit illustrated in figure 3.3 can be defined in two separate phases [5]. These are covered in the following two subsections.

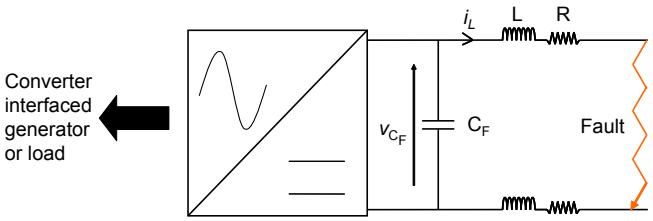

Figure 3.3: Equivalent circuit for the faulted network

First phase characterisation

In the Laplace domain, the current response of the RLC circuit in figure 3.3 is

$$i_L(s) = \frac{\frac{v_{CF}(0)}{L} + i_L(0)s}{s^2 + \frac{R}{L}s + \frac{1}{LC_F}} \tag{3.1}$$

where $i_L(0)$ is the initial current through the inductor and $v_{CF}(0)$ is the initial voltage across the capacitor C_F. The resistance R represents the combined sum of the line resistance of both cable connections to the converter plus equivalent series resistance of the filter capacitor. Similarly, the inductance L represents the total line inductance of both incoming and outgoing cables (the capacitor equivalent series inductance is usually insignificant compared to this). The expression (3.1) assumes that any changes in the output of the converter are negligible in comparison to the magnitude of the discharge current for the period immediately following the occurrence of the fault [2].

Taking the inverse Laplace transform of (3.1), the general current representation in the time domain is

$$i_L(t) = A_1 e^{s_1 t} + A_2 e^{s_2 t} \tag{3.2}$$

where $A_{1,2}$ are coefficients which depend on initial conditions and $s_{1,2}$ are the roots of the characteristic equation (the denominator of the Laplace expression) which are equal to

$$s_{1,2} = -\alpha \pm \sqrt{\alpha^2 - {\omega_0}^2}. \tag{3.3}$$

In (3.3), α is the damping factor (or Neper frequency) and is defined as

$$\alpha = \frac{R}{2L}. \tag{3.4}$$

The term ω_0 is the resonant radian frequency and is defined as

$$\omega_0 = \frac{1}{\sqrt{LC_F}}. \tag{3.5}$$

In (3.3), the relative magnitudes of α^2 and ω_0^2 determine the form of the current response, where $\alpha^2 > \omega_0^2$, $\alpha^2 = \omega_0^2$ and $\alpha^2 < \omega_0^2$ represent over, critically and underdamped fault responses respectively. For underdamped systems, the roots $s_{1,2}$ are complex and the current response is oscillatory. Applying the Euler identity to (3.2) and substituting terms for initial conditions, the underdamped current response can be derived as

$$i_L(t) = \frac{v_{CF}(0)}{L\omega_d} e^{-\alpha t} \sin(\omega_d t) + i_L(0) e^{-\alpha t} \left[\cos(\omega_d t) - \frac{\alpha}{\omega_d} \sin(\omega_d t) \right]. \tag{3.6}$$

In (3.6), ω_d is the damped resonant frequency and is defined as

$$\omega_d = \sqrt{{\omega_0}^2 - \alpha^2}. \tag{3.7}$$

The time taken for the current magnitude to reach its peak can be derived from (3.6) by equating its derivative to zero and solving for t. To take the derivative of (3.6) it is more straight forward to first collect the sine and cosine terms together, which gives

$$i_L(t) = X e^{-\alpha t} \sin(\omega_d t) + Y e^{-\alpha t} \cos(\omega_d t). \tag{3.8}$$

where $X = \frac{1}{L\omega_d} \left(v_{CF}(0) - \frac{i_L(0)R}{2} \right)$ and $Y = i_L(0)$. Differentiating by applying the product rule to both terms gives

$$\frac{di_L}{dt} = X \left[-\alpha e^{-\alpha t} \cos(\omega_d t) - \omega_d \sin(\omega_d t) \right] + Y \left[-\alpha e^{-\alpha t} \sin(\omega_d t) + \omega_d \cos(\omega_d t) \right]. \tag{3.9}$$

Substituting for X and Y and grouping voltage and current terms gives

$$\frac{di_L}{dt} = \frac{v_{CF}(0) e^{-\alpha t}}{L} \left[\cos(\omega_d t) - \frac{\alpha}{\omega_d} \sin(\omega_d t) \right] + i_L(0) e^{-\alpha t} \left[-2\alpha \cos(\omega_d t) + \left(\frac{\alpha^2}{\omega_d} - \omega_d \right) \sin(\omega_d t) \right] \tag{3.10}$$

which provides an expression for the underdamped current derivative. However to enable (3.10) to be solved for t, it must first be simplified. This can be achieved

through an understanding of the application type. As a result of the typically large filter capacitance and relatively low cable inductance (resulting from the short cable lengths associated with compact network applications), the dominant part of the underdamped fault current characteristic shown in (3.6) will be due to the initial voltage across the converter filter capacitance. As such, the expression for fault current profile can be reduced to

$$i_L(t) \approx \frac{v_{CF}(0)}{L\omega_d} e^{-\alpha t} \sin(\omega_d t). \tag{3.11}$$

For highly underdamped conditions (where $\omega_0^2 >> \alpha^2$ and ω_d tends to ω_0) equation (3.11) can be further reduced to

$$i_L(t) \approx \frac{v_{CF}(0)}{Z_0} e^{-\alpha t} \sin(\omega_0 t), \tag{3.12}$$

where Z_0 is the surge impedance of the fault path and is defined as

$$Z_0 = \sqrt{\frac{L}{C_F}}. \tag{3.13}$$

Similarly, (3.10) can be simplified by assuming that the dominant part of the fault current results from the initial capacitor voltage. Therefore by neglecting initial current, (3.10) becomes

$$\frac{di_L}{dt} = \frac{v_{CF}(0)e^{-\alpha t}}{L} \left[\cos(\omega_d t) - \frac{\alpha}{\omega_d} \sin(\omega_d t) \right]. \tag{3.14}$$

When current is at its peak magnitude, its derivative will be equal to zero and, assuming the initial current is zero, the term $\omega_d t$ will be equal to $\frac{\pi}{2}$. Substituting these factors into (3.14) and solving for t gives

$$t_{peak} = \frac{1}{\omega_d} \arctan \frac{\omega_d}{\alpha}. \tag{3.15}$$

Again, for the underdamped case where $\omega_0^2 >> \alpha^2$, and ω_d tends to ω_0, (3.15) reduces to

$$t_{peak} \approx \frac{1}{\omega_0} \arctan \frac{\omega_0}{\alpha}. \tag{3.16}$$

Using a similar approach, expressions for peak fault current magnitude and time to peak for overdamped networks (where the roots $s_{1,2}$ are real) can be

developed. The equation for current is given by

$$i_L(t) = \frac{v_{CF}(0)}{L(s_1 - s_2)}\left(e^{s_1 t} - e^{s_2 t}\right) + \frac{i_L(0)}{s_1 - s_2}\left[e^{s_2 t}(s_1 + \frac{R}{L}) - e^{s_1 t}(s_2 + \frac{R}{L})\right]. \quad (3.17)$$

Differentiating (3.17), the derivative overdamped current is

$$\frac{di_L}{dt} = \frac{v_{CF}(0)}{L(s_1 - s_2)}\left(s_1 e^{s_1 t} - s_2 e^{s_2 t}\right) + \frac{i(0)}{s_1 - s_2}\left[e^{s_2 t}\left(\omega_0^2 + 2\alpha s_2\right) - e^{s_1 t}(\omega_0^2 + 2\alpha s_1)\right]. \quad (3.18)$$

As before, by assuming that the dominant part of the fault current results from the initial capacitor voltage these equations can be simplified in many cases to neglect initial current. Therefore current and its derivative simplify to

$$i_L(t) = \frac{v_{CF}(0)}{L(s_1 - s_2)}\left(e^{s_1 t} - e^{s_2 t}\right). \quad (3.19)$$

and

$$\frac{di_L}{dt} = \frac{v_{CF}(0)}{L(s_1 - s_2)}\left(s_1 e^{s_1 t} - s_2 e^{s_2 t}\right). \quad (3.20)$$

respectively. Equating (3.20) to zero (to find t_{peak}) gives

$$\frac{v_{CF}(0)}{L(s_1 - s_2)}\left(s_1 e^{s_1 t} - s_2 e^{s_2 t}\right) = 0 \quad (3.21)$$

and after rearrangement

$$\frac{e^{s_1 t}}{e^{s_2 t}} = \frac{s_2}{s_1}. \quad (3.22)$$

Taking the natural logarithm of both sides of (3.22) and solving for t results in a peak current time of

$$t_{peak} = \frac{\ln\left({}^{s_2}/_{s_1}\right)}{s_1 - s_2}. \quad (3.23)$$

Equations (3.17) and (3.23) can also be applied to find the underdamped response. However the complex roots $s_{1,2}$ make these expressions difficult to solve analytically. The unlikelihood of a critically damped fault response occurring, and given that it is a less challenging fault condition to deal with (underdamped conditions lead to higher currents and overdamped conditions lead to greater detection challenges), means that derivation of specific equivalent expressions

would be of little benefit.

From the expressions for current, equivalent under and overdamped expressions can be derived for the voltage across the filter capacitor. This voltage is proportional to the capacitor size and integral of current and the voltage under fault conditions is described by,

$$v_{CF}(t) = \frac{1}{C_F}\int i_L(t)dt + V_{final} \tag{3.24}$$

where V_{final} is the capacitor voltage as $t\to\infty$. V_{final} is assumed to be zero for the purposes of this analysis as no other voltage sources are considered to be present and so the capacitor voltage will eventually decay to zero. This assumption is made throughout this analysis due to the typically large difference in response time between other sources within the network [2] and as the initial response is the main period of interest.

For underdamped circuit conditions, (3.6) is substituted for current in the above equation, which gives

$$v_{CF}(t) = \frac{1}{C_F}\int \frac{v_{CF}(0)}{L\omega_d}e^{-\alpha t}\sin(\omega_d t) + i_L(0)e^{-\alpha t}\left[\cos(\omega_d t) - \frac{\alpha}{\omega_d}\sin(\omega_d t)\right]dt \tag{3.25}$$

Collecting terms this becomes,

$$v_{CF}(t) = \frac{1}{C_F}\int Ae^{-\alpha t}\sin(\omega_d t) + Be^{-\alpha t}\cos(\omega_d t)dt \tag{3.26}$$

where $A = \frac{1}{L\omega_d}\left(v_{CF}(0) - \frac{i_L(0)R}{2}\right)$ and $B = i_L(0)$. To take the integral of (3.26) it is necessary to integrate by parts due to the transcendental nature of the functions. Integrating these terms in isolation gives

$$\int e^{-\alpha t}\sin(\omega_d t) = \frac{e^{-\alpha t}}{\omega_0^2}\left[-\omega_d\cos(\omega_d t) - \alpha\sin(\omega_d t)\right] \tag{3.27}$$

and

$$\int e^{-\alpha t}\cos(\omega_d t) = \frac{e^{-\alpha t}}{\omega_0^2}\left[\omega_d\sin(\omega_d t) - \alpha\cos(\omega_d t)\right]. \tag{3.28}$$

Substituting (3.27) and (3.28) into (3.26) gives

$$v_{CF}(t) = \frac{1}{C_F}\left(\frac{Ae^{-\alpha t}}{\omega_0^2}\left[-\omega_d\cos(\omega_d t) - \alpha\sin(\omega_d t)\right] + \frac{Be^{-\alpha t}}{\omega_0^2}\left[\omega_d\sin(\omega_d t) - \alpha\cos(\omega_d t)\right]\right). \tag{3.29}$$

Substituting the expressions for A and B within (3.29) and simplifying gives

$$v_{CF}(t) = v_{CF}(0)e^{-\alpha t}\left[-\cos(\omega_d t) - \frac{\alpha}{\omega_d}\sin(\omega_d t)\right] + \frac{i_L(0)e^{-\alpha t}}{C_F\omega_d}\sin(\omega_d t). \quad (3.30)$$

As (3.30) was derived from an expression representing current flowing away from the capacitance, it is of negative polarity. A more relevant voltage expression is therefore

$$v_{CF}(t) = v_{CF}(0)e^{-\alpha t}\left[\cos(\omega_d t) + \frac{\alpha}{\omega_d}\sin(\omega_d t)\right] - \frac{i_L(0)e^{-\alpha t}}{C_F\omega_d}\sin(\omega_d t), \quad (3.31)$$

which neglecting initial current can be simplified to

$$v_{CF}(t) = \frac{v_{CF}(0)e^{-\alpha t}}{\omega_d}\left[\omega_d\cos(\omega_d t) + \alpha\sin(\omega_d t)\right]. \quad (3.32)$$

Expressions for the overdamped voltage can be derived in a more straight forward manner. The integral of (3.17) with respect to time is

$$v_{CF}(t) = \frac{v_{CF}(0){\omega_0}^2}{(s_1 - s_2)}\left(\frac{e^{s_1 t}}{s_1} - \frac{e^{s_2 t}}{s_2}\right) + \frac{i_L(0)}{C(s_1 - s_2)}\left(\frac{e^{s_2 t}}{s_2}\left[s_1 + \frac{R}{L}\right] - \frac{e^{s_1 t}}{s_1}\left[s_2 + \frac{R}{L}\right]\right) \quad (3.33)$$

which is again of negative polarity. The positive voltage expression is therefore

$$v_{CF}(t) = \frac{v_{CF}(0){\omega_0}^2}{(s_1 - s_2)}\left(\frac{e^{s_2 t}}{s_2} - \frac{e^{s_1 t}}{s_1}\right) - \frac{i_L(0)}{C(s_1 - s_2)}\left(\frac{e^{s_1 t}}{s_1}\left[s_2 + \frac{R}{L}\right] - \frac{e^{s_2 t}}{s_2}\left[s_1 + \frac{R}{L}\right]\right) \quad (3.34)$$

and again when simplifying to neglect initial current, this equals

$$v_{CF}(t) = \frac{v_{CF}(0){\omega_0}^2}{(s_1 - s_2)}\left(\frac{e^{s_2 t}}{s_2} - \frac{e^{s_1 t}}{s_1}\right). \quad (3.35)$$

These current and voltage equations, and the approaches adopted to derive them, will be employed throughout this thesis.

Second phase characterisation

In compact DC electrical networks the time to peak for the capacitor discharge current is typically very short [3], and as such it is also important to consider the second phase of the fault current profile which usually occurs shortly after the

current peak [5].

The analysis of the second phase of the fault current profile is notably different to that associated with the characterisation of the first phase. This is a result of the presence of freewheeling diodes in parallel with the active devices within the converter [3–5].

Following the occurrence of the peak current, L-C oscillations in the circuit can cause the voltage across the converter's filter capacitor to become negative [5]. This has the effect of reversing the voltage at the converter terminals and, provided this voltage is sufficiently high, causing the freewheeling diodes to conduct. This provides an alternative current path, regardless of the state of the active switching devices within the converter, and so changes the response of the network. Figure 3.4 shows a newly developed yet simple equivalent circuit which can be used to represent the generation and active load interface in the network shown in figure 3.3 during the period of voltage reversal. In this figure, V_d is equal to the sum of the diodes' on-state voltages in any converter leg and R_d is equal to the series and parallel combinations of the diodes' on-state resistances.

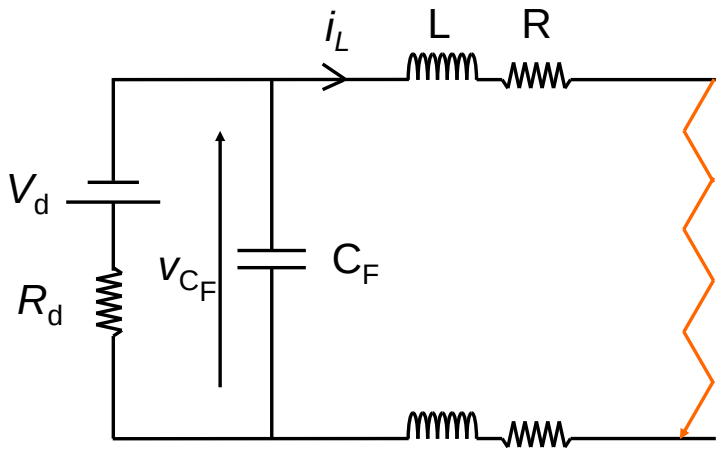

Figure 3.4: Equivalent circuit of the faulted circuit with conducting freewheeling diodes

In a similar manner to that previously presented, expressions defining the behaviour of the reverse polarity circulating current can be derived. The general expression for current $i(t)$ is

$$i_L(t) = \frac{V_d}{R_d + R} + B_1 e^{s_1 t} + B_2 e^{s_2 t}, \tag{3.36}$$

where the roots $s_{1,2}$ are defined in (3.3) and

$$\alpha = \frac{R}{2L} + \frac{1}{2R_d C}, \tag{3.37}$$

$$\omega_0 = \sqrt{\frac{1}{LC} + \frac{R}{R_d LC}}, \tag{3.38}$$

$$B_1 = \frac{i_L(0)(s_2 + \frac{R}{L}) - \frac{v_{CF}(0)}{L} - \frac{V_d s_2}{R_d + R}}{s_2 - s_1} \tag{3.39}$$

and

$$B_2 = i_L(0) - B_1 - \frac{V_d}{R_d + R}. \tag{3.40}$$

Equations specific to damping conditions can be found using methods from the previous section.

To assess the period of this second phase of the fault response, the voltage across the diode-capacitor parallel branch must be derived (as this indicates when the reverse voltage is greater than the turn on voltage of the diodes). The diode-capacitor parallel branch voltage is equal to the voltage across the line resistance R and inductance L, assuming the voltage developed across the fault is negligible. Therefore, the voltage v_{CF} across the diode-capacitor parallel branch is

$$v_{CF}(t) = i(t)R + L\frac{di}{dt}. \tag{3.41}$$

By employing methods already demonstrated and substituting using the expression for current $i_L(t)$ given in (3.36), equation (3.41) can be expanded to give

$$v_{CF}(t) = \frac{V_d}{R_d + R} + (R + s_1 L)B_1 e^{s_1 t} + (R + s_2 L)B_2 e^{s_2 t}. \tag{3.42}$$

Equation (3.42) is transcendental and so no analytical solution exists. The resulting equation can be written as a recurrence relation and therefore an iterative numerical method is required to find the duration of the freewheeling diode conduction.

One such numerical method is Newton's Method, which is a root-finding algorithm often represented by the expression

$$x_{n+1} = x_n - \frac{f(x_n)}{f'(x_n)}. \tag{3.43}$$

Given an appropriate starting value for x_0, the algorithm works iteratively us-

ing information about the derivative to find a solution for x where $f(x_n) \approx 0$ and hence $x_{n+1} \approx x_n$. The algorithm can be applied to solve for the period of diode conduction by setting the function $f(x_n)$ to $V(t_n)$. The Newton's Method equation for diode conduction time can therefore be expressed as

$$t_{n+1} = t_n - \frac{V(t_n)}{V'(t_n)} \tag{3.44}$$

where t_n is the time at which (3.42) is evaluated and $V(t_n)$ and $V'(t_n)$ are the voltage and derivative voltage respectively at t_n.

To solve for the period of diode conduction, $v_{CF}(t)$ in (3.42) should be set equal to the combined switch-on voltage of the diodes in the conduction path within the converter. It is likely that two solutions exist to (3.44), the first as the diode begins to conduct (at $t = 0$) and the second as the diode ceases conduction. To aid the convergence of (3.44) towards the latter, t_n should be given a non-zero initial value.

The total current through all of the converter's freewheeling diodes during this period of conduction can be expressed as a function of the voltage $v_{CF}(t)$ in (3.42) and diode parameters V_d and R_d. Equation (3.44) provides the time period of this current conduction. Current through the freewheeling diode path $i_d(t)$ is therefore

$$i_d(t) = \frac{v_{CF}(t) - V_d}{R_d}. \tag{3.45}$$

After the time in (3.44) elapses, the circuit returns to its previous operating characteristic, albeit at a lower current magnitude due to the energy dissipated within the diodes.

Natural response for earth fault conditions

A mid-point earthing configuration is typically utilised at the converter output terminals on DC distribution systems [5, 17]. This configuration is illustrated in figure 3.5(a), which also indicates the distribution of capacitance and voltage in the network under normal operating conditions.

Under rail to earth fault conditions, the fault only appears across one of these capacitances, and this changes the response compared to the rail to rail fault analysed previously. The equivalent faulted circuit is illustrated in figure 3.5(b). This can be analysed as before, substituting new values for voltage and capacitance. Note that figure 3.5(b) does not include any additional earth cabling or earth path impedance which may alter the fault response.

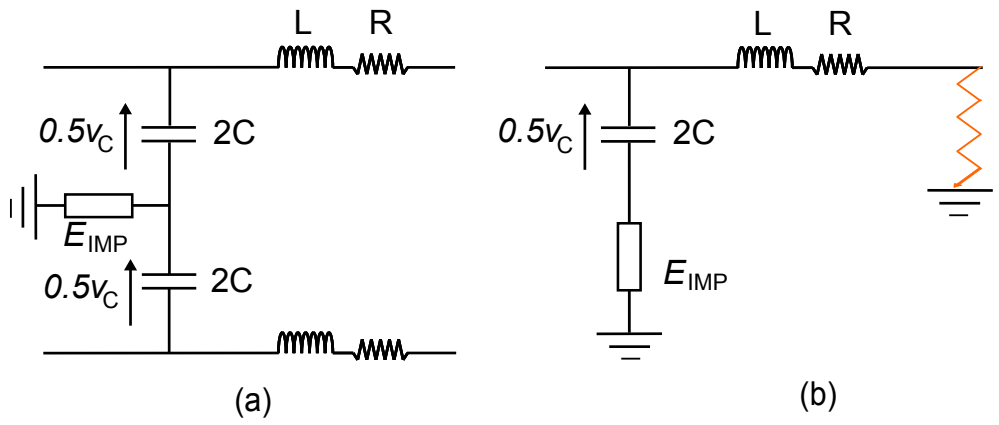

Figure 3.5: (a) Mid-point earthing of converter output filter capacitors (b) Equivalent circuit for a rail to earth fault

A major influence on the earth fault response is the selected earthing impedance E_{Imp}. There are a number of aspects to consider when selecting an appropriate earthing impedance. For example, a solidly connected earth point helps to quickly clear earth faults as it attracts a high current, whilst high impedance connections to earth provide ride-through capability in the event of an earth fault. A number of sources discuss the relative merits of the different approaches [8, 18, 19] and so this thesis will not discuss these issues further.

3.1.2 Contribution from converter interfaced sources

Whilst this chapter emphasises the role of the natural response of the DC network (i.e. that of the DC side filter components) in determining the protection system operating requirements, it is essential not to overlook the contribution from other sources, such as that of converter interfaced sources [4, 5, 20] and energy storage systems [2,6,21] (depending on the technologies and control strategies employed). Indeed, substantial research has been conducted on the behaviour of these systems under fault conditions, which is largely applicable.

For example [6,20,21] illustrate that the fault current contribution of a battery can be both high in magnitude and rapid developing when connected directly to a distribution busbar. A direct connection requires a battery voltage equal to that of the network, and this voltage is achieved through the series connection of a number of battery cells. Depending on the application type, this is not always feasible, particularly if space and weight are restricted, and so battery storage is often interfaced to a DC network through DC-DC converters [22, 23]. Depending on its topology, this converter interface can result in a range of protection issues for battery systems as discussed in Chapter 2.

Other the key areas of interest, particularly for the aerospace sector, are the impact of novel generation types not typically seen in other multiterminal DC network applications, such as switched reluctance and permanent magnet synchronous machines [7]. In particular, the specification of an integrated protection system that inherently accommodates the natural characteristics of these technologies would be of great value. However as stated in Chapters 1 and 2, the aim of much of the work in this thesis is to enable protection to operate based on the response of the DC side filter components. Whilst the natural response is not completely disconnected from the converter response, it is seen that this characteristic is dominated by circuit initial conditions, hence the emphasis of this chapter on this aspect of the fault response. As Chapter 2 also discusses, whilst the idea of operating on a network's natural response is challenging, the design of a protection scheme operated primarily on the response of DC side network components reduces the knowledge required about the generator or converter fault response, which will vary depending on the technology and control system employed. This may reduce the complexity of protection system design as less factors would need to be taken into consideration whilst also enabling greater reusability of a protection system design.

3.2 Analysis of system behaviour during circuit breaker operation

The time varying nature of typical fault current profiles in DC networks (as illustrated in figure 3.2) is such that the timing of circuit breaker (CB) operation has a significant impact on the breaking current and voltage developed across the device. It is clear that the higher the current magnitude, the higher the breaking requirements of the CB. However because of the nature of DC systems, where a fault is cleared through the creation of a current zero rather than during periodically existing current zeros as in AC systems, there a number of additional aspects in the design and operation of DC circuit breakers to consider. In particular, this section will present analysis to show how the CB operating time impacts on the energy dissipation requirements of the CB, the voltage developed across the breaker and the total time taken to clear the fault.

3.2.1 Calculation of circuit breaker energy dissipation

For the CB to create a current zero, and hence clear the fault, it is necessary to dissipate the stored energy in any series line inductance [25, 26]. Depending on the CB technology utilised, this dissipation may take place in an arc (EMCB) or voltage snubber (HCB or SSCB). However in each case the same analysis can be applied. For simplification, the following sections treat the CB as a single device. In cases where more than one device exists in a line (e.g. where CBs are placed on the positive and negative conductors), it is anticipated that energy will be divided approximately equally between the respective devices, provided they are of the same rating.

For the interruption of fault current, it is anticipated that a significant majority of the storage energy will be contained within the line inductance in series with the CB at the time of its operation, with minimal contribution from elsewhere in the network due to the CB operation. It can therefore be approximated that the energy stored within the line is

$$E_L = \frac{1}{2} L {i_L}^2 \tag{3.46}$$

where I is described in (3.6) or (3.17), depending on the damping conditions in the network. Substituting (3.6) into (3.46) as an example, and neglecting initial current as before, gives

$$E_L = \frac{{v_{CF}(0)}^2}{2L{\omega_d}^2} e^{-2\alpha t_{CB}} \sin^2(\omega_d t_{CB}) \tag{3.47}$$

where t_{CB} represents the time instant of circuit breaking operation, which is inclusive of protection system decision time (illustrated more clearly in the following section).

By assuming that all of this line inductance energy is dissipated in the circuit breakers (as opposed to within line or fault resistance), then the CB energy requirement can be determined for a specific operating current. An example of this, and how it may impact circuit breaker design is included within Chapter 4.

3.2.2 Calculation of circuit breaker voltage and fault clearance time

Whilst the previous section gives a general idea of how the protection operation time could potentially impact on the CB design, further analysis is needed to establish how the CB voltage requirements can change and how this impacts on

the clearance of the fault. Greenwood [25] provides some approaches to analyse this problem and these are particularly useful in the simplification of a complex (and often non-linear in the case of arc voltage).

To describe this approach, consider the equivalent circuit illustrated in figure 3.6 and simplified fault current and circuit breaker voltage shown in figure 3.7. Note that within figure 3.6, line parameters R and L represent the combined fault path impedances and the CB represents all series CB devices.

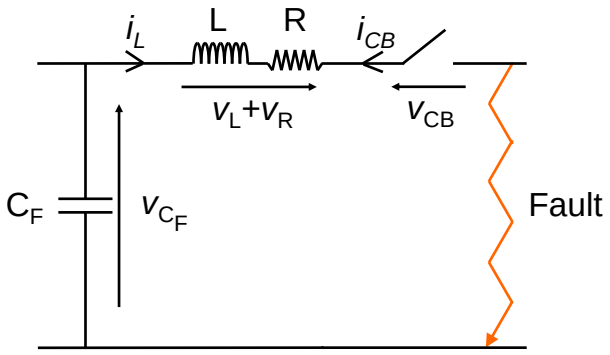

Figure 3.6: Equivalent circuit for the faulted network with CB operation

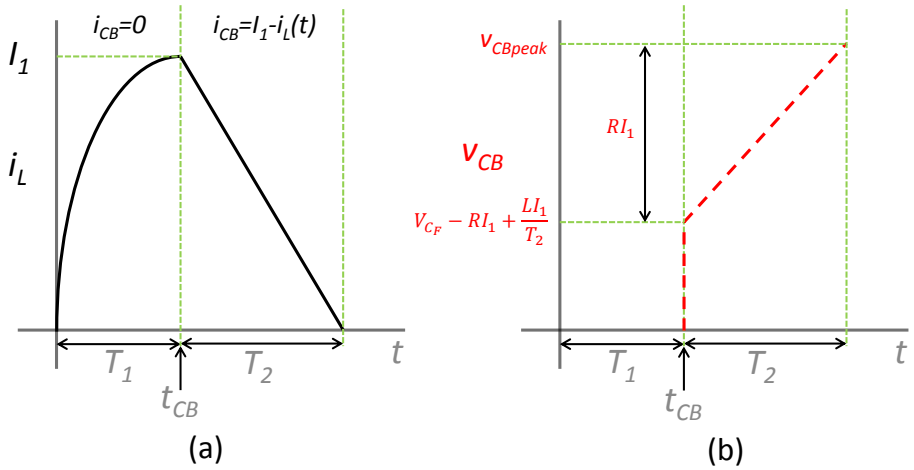

Figure 3.7: Simplified fault current (a) and circuit breaker voltage (b) response before and after circuit breaker operation

To circumvent some of the complexity in the circuit breaking process, Greenwood [25] derives the circuit breaker voltage, v_{CB}, using superposition of the fault current from the circuit, i_L, and the counter current associated with the circuit breaker, i_{CB}. Within figure 3.7, i_{CB} is the current required to drive i_L to zero within T_2 seconds, where T_2 is the time difference between the time instant of CB opening, t_{CB}, and current reaching zero. i_{CB} is assumed to increase linearly

over the period of T_2 seconds and so can be represented by a current ramp. This counter ramp current can be mathematically described as

$$i_{CB}(t) = \frac{I_1 t}{t_{CB} + T_2}. \tag{3.48}$$

From figure 3.6, assuming that the voltage developed across the fault is negligible (fault voltage would lead to decreased CB requirements), it is evident that

$$v_{CB} = v_{CF} + v_L + v_R \tag{3.49}$$

where v_L and v_R are developed by i_{CB}. To solve (3.49) for the maximum CB voltage conditions, [25] derives the expression

$$v_{CBpeak} = v_{CF} + \frac{LI_1}{T_2} \tag{3.50}$$

Figure 3.7 also helps illustrate that equation (3.50) is based on the assumption that following an initial voltage step to arrest the rise in current (where voltage must be equal to the system voltage and the constant inductor voltage due to the constant $\frac{di}{dt}$ from the current ramp), the voltage across the CB increases linearly until current reaches zero. Therefore the current zero corresponds with the peak CB voltage. Based on this initial assumption, two further assumptions can be made in (3.49) to derive (3.50). The first of these is to set v_R to zero, which is valid when the line current is also equal to zero. Second, as the final current is zero, the rate of change of current through the inductor (which is proportional to its voltage) can be determined by the current at which the CB operates, divided by T_2.

However, in contrast to the approach taken in [25], the supply voltage in the network illustrated in figure 3.6 cannot be considered constant due to the high rate of change of the voltage across the capacitor. Instead voltage will now decrease for the duration of the fault. Defining the exact capacitor voltage in (3.50) is a complex problem as its rate of decay will depend not only on the operating time of the circuit breakers but also on v_{CB}, the value being calculated. This type of co-dependency is better dealt with in a dynamic simulation environment, which is out with the scope of this section. However for the purposes of an analytical study it is reasonable to assume that v_{CF} remains constant during the period of CB operation (which significantly reduces the discharge rate of the filter capacitor). Under these conditions v_{CF} can be defined as in section 3.1.1, where t is equal to the operating time of the circuit breakers, t_{CB}. Substituting the underdamped voltage expression (3.32) and the underdamped current expres-

sion (3.11) into (3.50) as an example, and cancelling equal terms, the maximum CB voltage v_{CBpeak} becomes

$$v_{CBpeak} = v_{CF}(0)e^{-\alpha t_{CB}} \left[\cos(\omega_d t_{CB}) + \frac{\left(\frac{1}{T_2} + \alpha\right)}{\omega_d} \sin(\omega_d t_{CB}) \right]. \tag{3.51}$$

Within (3.51) the term T_2 describes the time difference between CB operation and current reaching zero. However this time is dependent on the v_{CBpeak} and hence will also vary with time. This analysis is utilised in Chapter 4 which provides an illustration into how these characteristics will impact circuit breaker voltage and fault clearance time, and discusses the impact on overall protection system design requirements.

3.2.3 Calculation of fault energy let through

This section assesses the impact of the total CB operation and fault clearance time on the I^2t energy delivered to the fault. To achieve this, current is calculated in two discrete stages. These stages represent the circuit conditions before and during the CB operation (as shown in equations in (3.6) and (3.52) respectively). As discussed in the previous section, one option is to linearly approximate the current profile as it decreases from the value at the point of CB operation ($i(t_{CB})$) to zero over the period T_2. The current after CB operation can therefore be approximated as

$$i(t) \approx i(t_{CB}) - \frac{i(t_{CB})}{T_2} t \tag{3.52}$$

where $t_{CB} < t < T_2$. If both the appropriate underdamped or overdamped current expression and equation (3.52) are squared and integrated, it is possible to determine the I^2t energy which flows into the fault, both prior to and during CB operation.

Assessing the underdamped case in the first instance, expression (3.11) will be used. The square of (3.11) is equal to

$$i^2(t) = \frac{v_{CF}(0)^2}{L^2 {\omega_d}^2} e^{-2\alpha t} \sin^2(\omega_d t). \tag{3.53}$$

In the context of this section, (3.53) should be integrated between the definite

intervals of 0 and t_{CB}. This integral is therefore

$$\int_0^{t_{CB}} i^2(t)dt = \frac{v_{CF}(0)^2}{L^2{\omega_d}^2} \int_0^{t_{CB}} \left[e^{-2\alpha t}\sin^2(\omega_d t)\right] dt. \tag{3.54}$$

Taking the integral of (3.54) using an integrator tool provided by [27], substituting for the appropriate intervals and collecting equal terms gives

$$I^2 t_{underdamped} = \frac{v_{CF}(0)^2 C_F}{2{\omega_d}^2 R}\left({\omega_d}^2 + e^{-2\alpha t_{CB}}\left[-\alpha^2 - {\omega_d}^2 + \alpha^2\cos(2\omega_d t_{CB}) - \alpha\omega_d \sin(2\omega_d t_{CB})\right]\right) \tag{3.55}$$

which provides an expression for the fault energy up to the time at which protection operates, as required. An equivalent expression for the overdamped case can be found in a similar manner as described below.

Taking the square of (3.17) and integrating between the intervals of 0 and t_{CB} gives

$$\int_0^{t_{CB}} i^2(t)dt = \frac{v_{CF}(0)^2}{L^2(s_1 - s_2)^2} \int_0^{t_{CB}} \left(e^{2s_1 t} - 2e^{s_1+s_2 t} + e^{2s_2 t}\right) dt. \tag{3.56}$$

Integrating (3.56) and collecting equal terms gives

$$I^2 t_{overdamped} = \frac{v_{CF}(0)^2}{L^2(s_1 - s_2)^2}\left[\frac{1}{2s_1}\left(e^{2s_1 t_{CB}} - 1\right) + \frac{2}{s_1 + s_2}\left(1 - e^{(s_1+s_2)t_{CB}}\right) + \frac{1}{2s_2}\left(e^{2s_2 t_{CB}} - 1\right)\right]. \tag{3.57}$$

As stated, equations (3.55) and (3.57) provide a means of calculating I^2t up until the point of protection operation. To determine the I^2t response whilst circuit breakers are operating, (3.52) can be used to represent current. This will be squared and integrated between the intervals of 0 and T_2. The lower limit is set at 0, as opposed to t_{CB}, as the term T_2 represents the time difference between t_{CB} and current zero rather than the total time from fault inception. Taking the square of (3.52) and integrating gives

$$\int_0^{T_2} i_{CB}(t)^2 dt = i(t_{CB})^2 \int_0^{T_2} \left(1 - \frac{t}{T_2}\right)^2 dt. \tag{3.58}$$

which becomes

$$\int_0^{T_2} i_{CB}(t)^2 dt = i(t_{CB})^2 \left[t - \frac{2t^2}{2T_2} + \frac{t^3}{3{T_2}^2} \right]_0^{T_2}. \tag{3.59}$$

Evaluating 3.59 between limits T_2 and 0 and simplifying gives

$$I^2 t_{CB} = \frac{i(t_{CB})^2 T_2}{3} \tag{3.60}$$

where $i(t_{CB})$ and T_2 can be calculated from previous equations, or the expressions for these can be substituted into (3.60).

Finally, the total I^2t delivered to a fault from fault inception to clearance can be found from the sum of either (3.55) and (3.57) (as appropriate) and (3.60). As is the case within other sections of this chapter, an example of the use of these equations and how they help assess protection system performance and requirements is provided within Chapter 4.

3.3 Analysis of post-fault clearance network voltage transient behaviour

Following the clearance of a fault, the network voltage will transiently change before settling to a steady state value. This transient behaviour occurs due to two well known effects, the transient recovery voltage and current chopping [16]. The transient recovery voltage occurs due to the connection of differently charged capacitors, while current chopping occurs when circuit breakers create a current zero in the faulted path but where current is still flowing towards the fault from other branches. These effects will be highlighted within the following analysis and later chapters will illustrate how they can result in significant post-fault voltage transients propagating throughout the remaining healthy portions of the network.

To illustrate this effect, consider a scenario on the network illustrated in figure 3.1 where a fault has occurred at a load and the fault is subsequently cleared, disconnecting the load from the network. The response of the remaining network will be analysed using a simplified equivalent circuit shown in figure 3.8. The circuit consists of the filter capacitance at the converter output C_1, line resistance R and inductance L, and the total capacitance of the remaining load converters C_2.

The resultant circuit in figure 3.8 consists of the filter and load capacitors in series with the line resistance and inductance. This circuit configuration permits

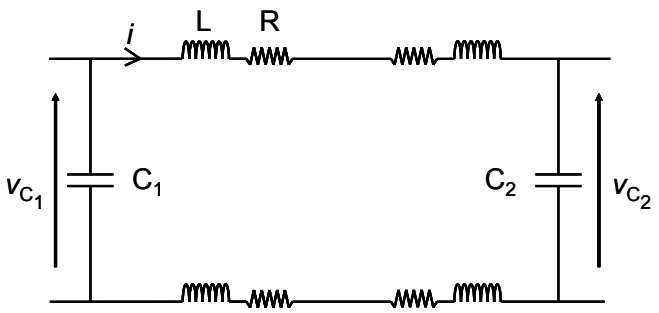

Figure 3.8: Equivalent circuit for the post fault clearance network

the second order analysis described in section 3.1.1 to be applied. Assuming the response is underdamped, the current flowing in the line following the clearance of the fault is

$$i_L(t) = \frac{v_{C1}(0) - v_{C2}(0)}{L\omega_d} e^{-\alpha t} \sin(\omega_d t) + i_L(0) e^{-\alpha t} [\cos(\omega_d t) - \frac{\alpha}{\omega_d} \sin(\omega_d t)] \quad (3.61)$$

where all initial conditions reflect the currents and voltages at all the circuit locations at the time of protection operation. The total capacitance C is now equal to the series combination of the load and filter capacitors, which varies C in (3.5), changing ω_0 (and hence ω_d) in the post-fault network. The subsequent voltage response across the load capacitance will be

$$v_{C_2}(t) = \frac{v_{C1}(0)C_1 + v_{C2}(0)C_2}{C_1 + C_2} + \frac{(v_{C1}(0) - v_{C2}(0))C_1 e^{-\alpha t}}{C_1 + C_2} \times \left[-\cos(\omega_d t) - \frac{\alpha}{\omega_d} \sin(\omega_d t) \right] + \frac{i_L(0) e^{-\alpha t}}{C_2 \omega_d} \sin(\omega_d t). \quad (3.62)$$

In (3.62) the first two terms show the charging effects of the larger filter capacitance C_1 on the smaller load capacitance C_2, this being the transient recovery voltage [16]. For highly underdamped networks, v_{C2} can reach approximately twice the magnitude of $v_{C1}(0)$, provided $C_1 >> C_2$. However, as results in Chapter 4 will show, while the voltage difference does have an impact on the transient voltage, if high currents are being interrupted, the dominant term in (3.62) is likely to be that of the initial current (I_0) (this being the chopped current). Taking this into account, (3.62) shows that the higher the breaking current and the smaller the remaining load capacitance, the greater the magnitude of the subsequent voltage transient. Chapter 4 provides an example of these transient voltages and considers how they impact protection operation and network design.

3.4 Validation of DC fault analysis

Given that the equations derived within this chapter will be employed at various stages throughout this thesis, it is useful to validate that they accurately represent a network's transient behaviour to ensure confidence in later results. The means through which these equations have been validated are described in the following sections. Note that the equations derived in section 3.2 on the circuit breaking process are explicitly analysed in Chapter 4 and so will not be separately validated within this section.

3.4.1 Validation of calculated RLC circuit natural response

In order to validate the calculated natural response of the equivalent RLC circuits presented earlier in this chapter, the circuit presented in figure 3.9 was simulated using the SimPowerSystems (SPS) simulation package within Matlab [13]. The parameters for this circuit are shown in table 3.2. These are based on those shown in table 3.1 with a total cable length of $10m$. Component R_{Fault} will be defined within the following sections depending on the damping conditions of interest. With the given data, ${\omega_0}^2 = 15.39{\times}10^6$ and so if $R_{Fault} > 0.04\Omega$ then the response will be overdamped. A fault resistance of 0.1Ω has been used to represent this condition. To ensure all transients are accurately captured within the simulation, a small time step of $0.1\mu s$ is utilised.

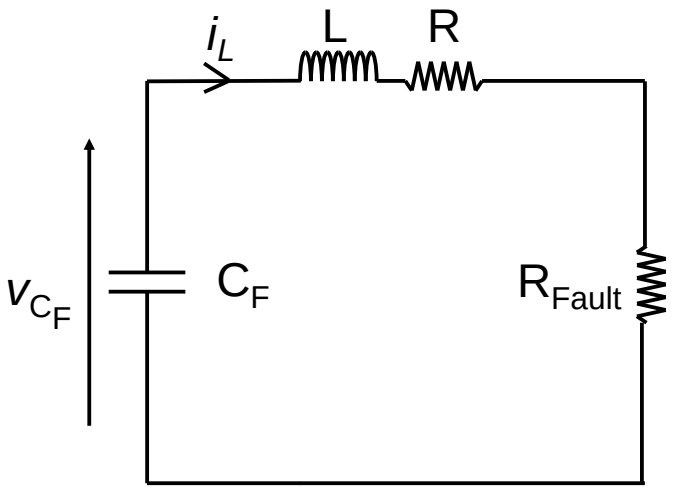

Figure 3.9: Simulated RLC circuit

A comparison of the simulated and calculated responses for the underdamped and overdamped current, voltage, $\frac{di}{dt}$, $\frac{dv}{dt}$ and i^2t of this circuit is presented figures 3.10 to 3.19 in the following sections. Note that $\frac{dv}{dt}$ has been derived sepa-

Table 3.2: RLC circuit Parameters

$V_{C_F}(0)$	$i_L(0)$	R	L	C_F	$C_{F_{ESR}}$
270V	20A	8.01mΩ	6.5μH	10mF	5mΩ

rately within section 5.1 of Chapter 5 but has been validated here for completeness.

It is clear from these figure that each of the equations derived for underdamped and overdamped current, voltage, $\frac{di}{dt}$, $\frac{dv}{dt}$ and i^2t do match that of the simulated response and therefore accurately reflects the transient behaviour of the equivalent RLC circuit.

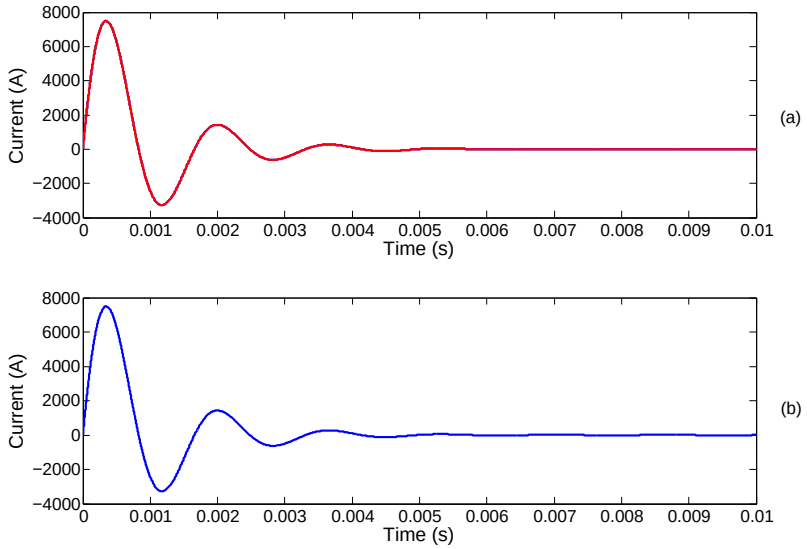

Figure 3.10: Comparison of simulated (a) and calculated (b) underdamped RLC circuit current

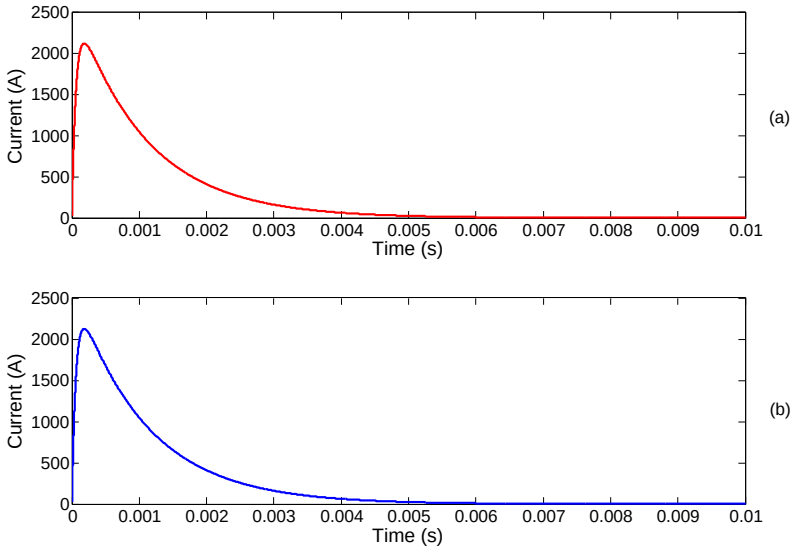

Figure 3.11: Comparison of simulated (a) and calculated (b) overdamped RLC circuit current

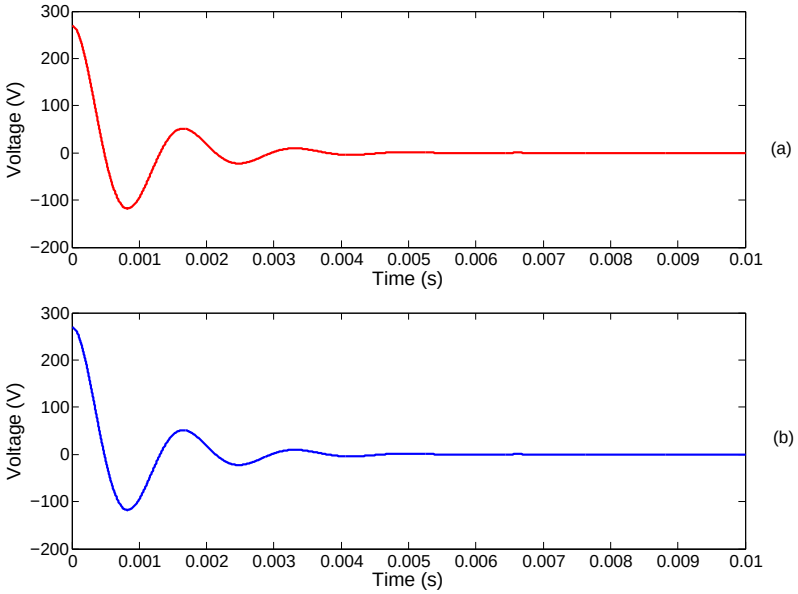

Figure 3.12: Comparison of simulated (a) and calculated (b) underdamped RLC circuit voltage

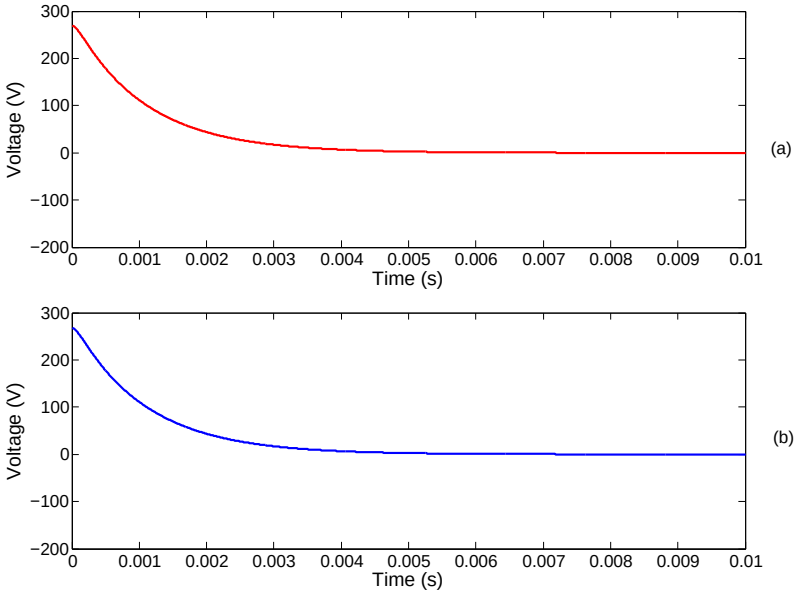

Figure 3.13: Comparison of simulated (a) and calculated (b) overdamped RLC circuit voltage

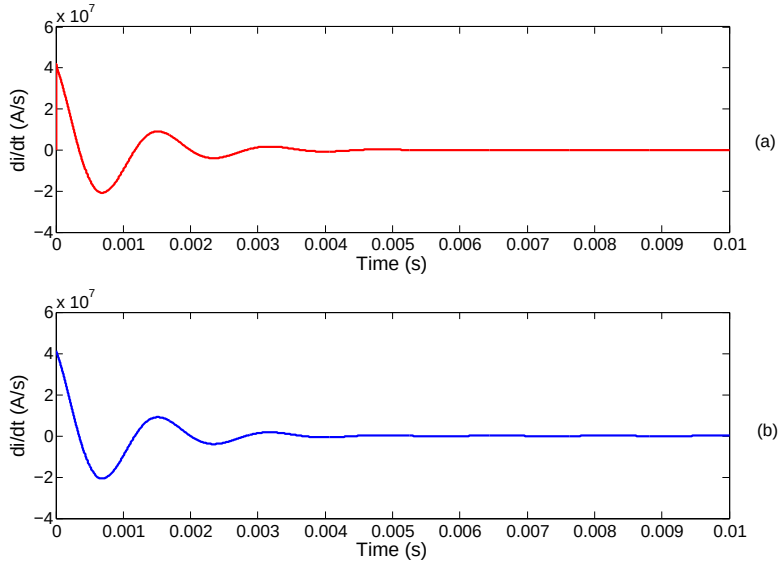

Figure 3.14: Comparison of simulated (a) and calculated (b) underdamped RLC circuit $\frac{di}{dt}$

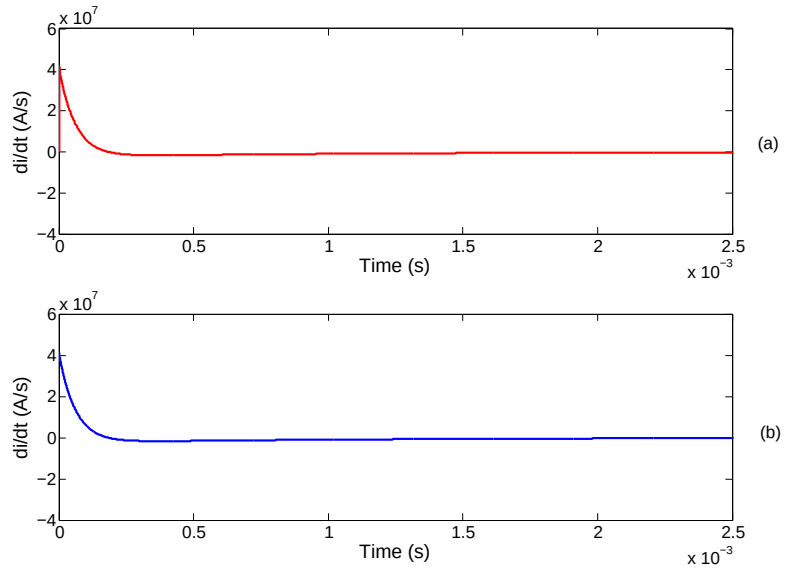

Figure 3.15: Comparison of simulated (a) and calculated (b) overdamped RLC circuit $\frac{di}{dt}$

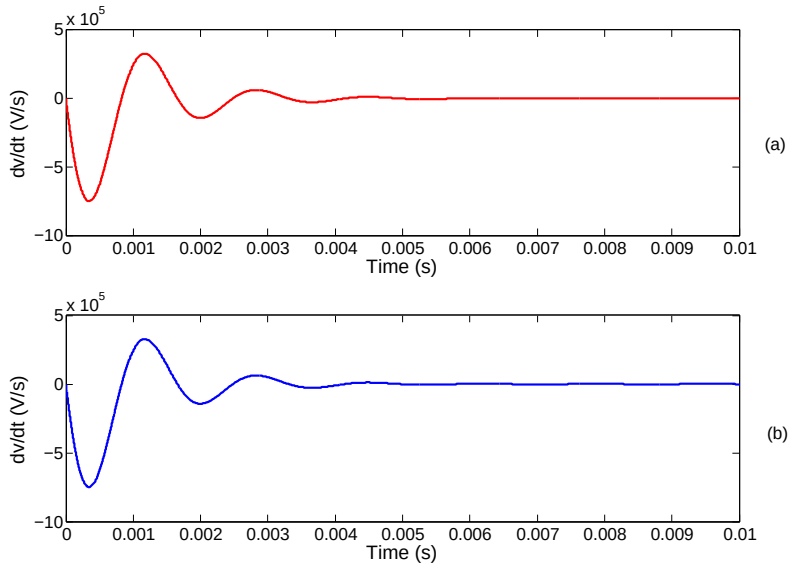

Figure 3.16: Comparison of simulated (a) and calculated (b) underdamped RLC circuit $\frac{dv}{dt}$

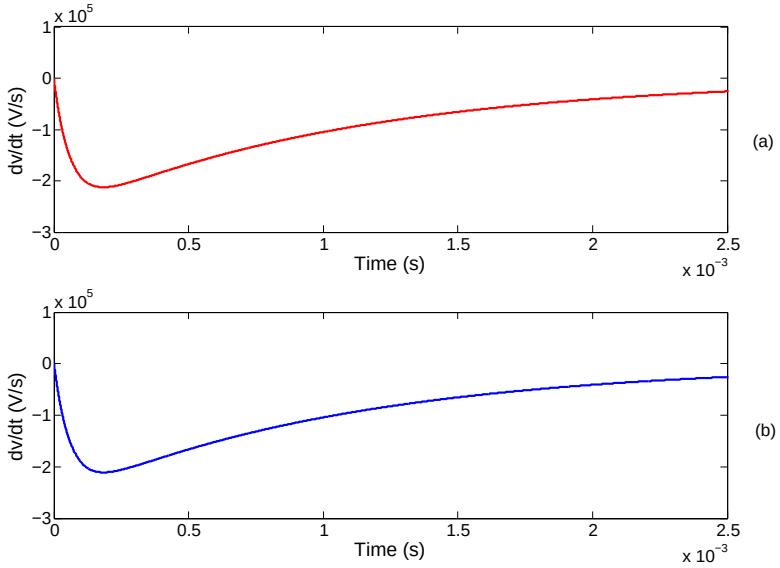

Figure 3.17: Comparison of simulated (a) and calculated (b) overdamped RLC circuit $\frac{dv}{dt}$

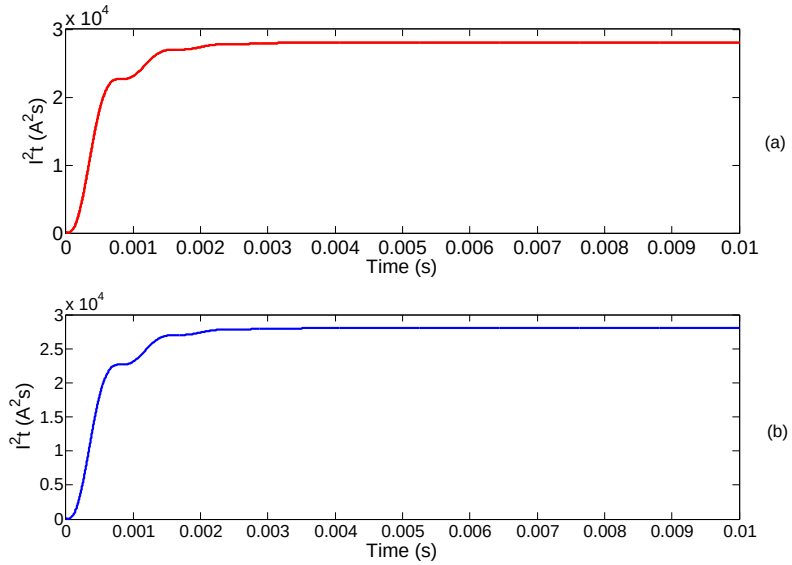

Figure 3.18: Comparison of simulated (a) and calculated (b) underdamped RLC circuit I^2t response

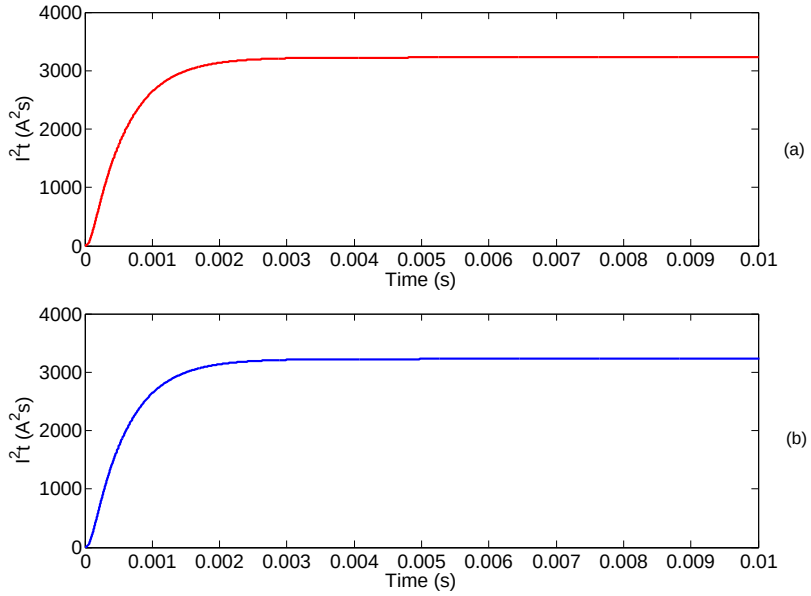

Figure 3.19: Comparison of simulated (a) and calculated (b) overdamped RLC circuit I^2t response

3.4.2 Validation of calculated RLC circuit response including diode conduction path

This section validates equations (3.42) and (3.45) for voltage and current respectively derived for the second phase of the fault response, where freewheeling diodes begin to conduct current. These equations are validated against a SPS model of the equivalent circuit shown in figure 3.4. The parameters which differ from table 3.2 are shown in table 3.3, which includes appropriate initial conditions to reflect the later stage of the fault response.

A comparison of simulated and calculated voltages and currents for this fault condition are shown in figures 3.20 and 3.21. These again highlight that the simulated and calculated responses are consistent and hence validates the accuracy of the derived equations.

Table 3.3: Equivalent diode circuit parameters

$V_{C_F}(0)$	$i_L(0)$	V_d	R_d
-0.8V	5000A	0.8V	1mΩ

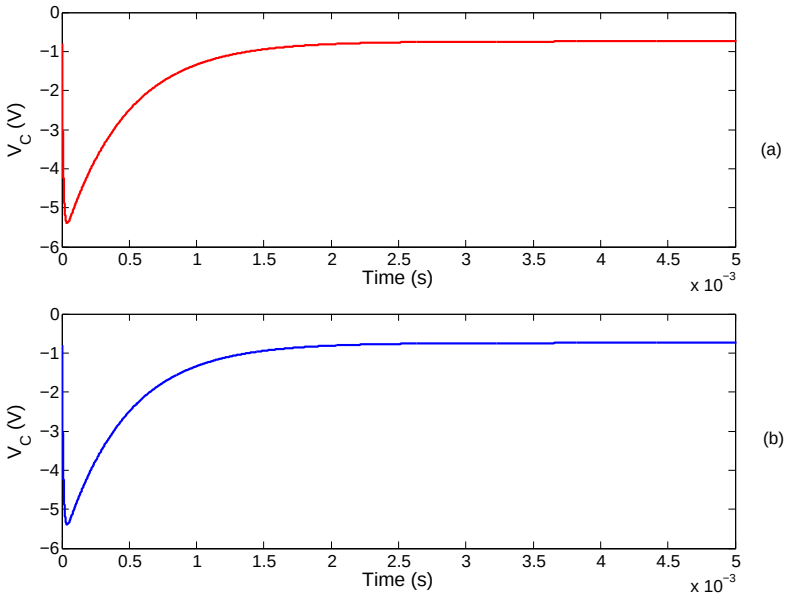

Figure 3.20: Comparison of simulated (a) and calculated (b) RLC circuit current with diodes conducting following voltage reversal

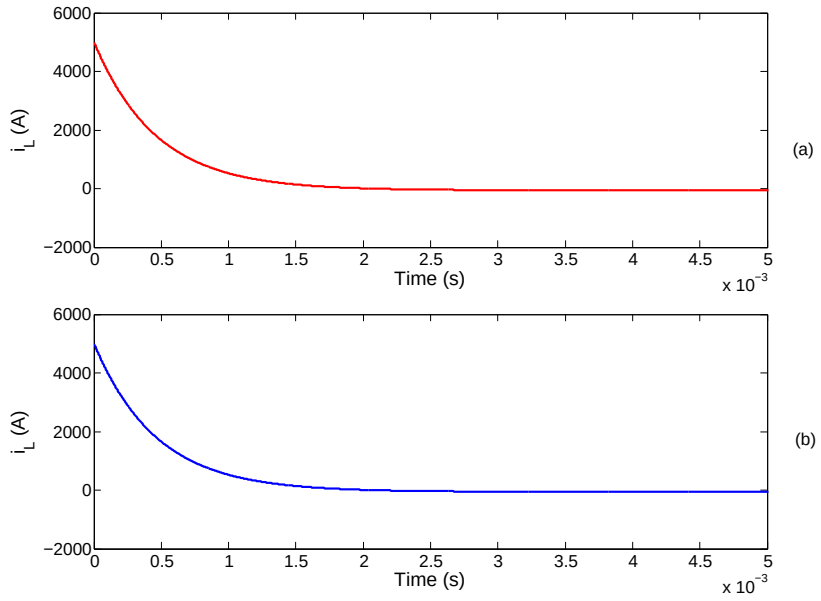

Figure 3.21: Comparison of simulated (a) and calculated (b) RLC circuit current with diodes conducting following voltage reversal

3.4.3 Validation of post fault clearance transient calculations

This section validates the post fault clearance transient voltage equation, (3.62) derived in section 3.3, through comparison with a simulation of the equivalent circuit illustrated in figure 3.8. Circuit parameters for simulation and calculation are presented in table 3.4.

Table 3.4: Parameters for the post fault clearance equivalent circuit

$V_{C_1}(0)$	$V_{C_2}(0)$	$i_L(0)$	R	L	C_1	$C_{1_{ESR}}$	C_2	$C_{2_{ESR}}$
100V	25V	2500A	8.01mΩ	6.5μH	10mF	5mΩ	0.5mF	79mΩ

A comparison of the simulated and calculated response is shown in figure 3.22. The figure again shows consistency between the simulated and calculated responses and validates the response of the derived post fault clearance transient voltage equation.

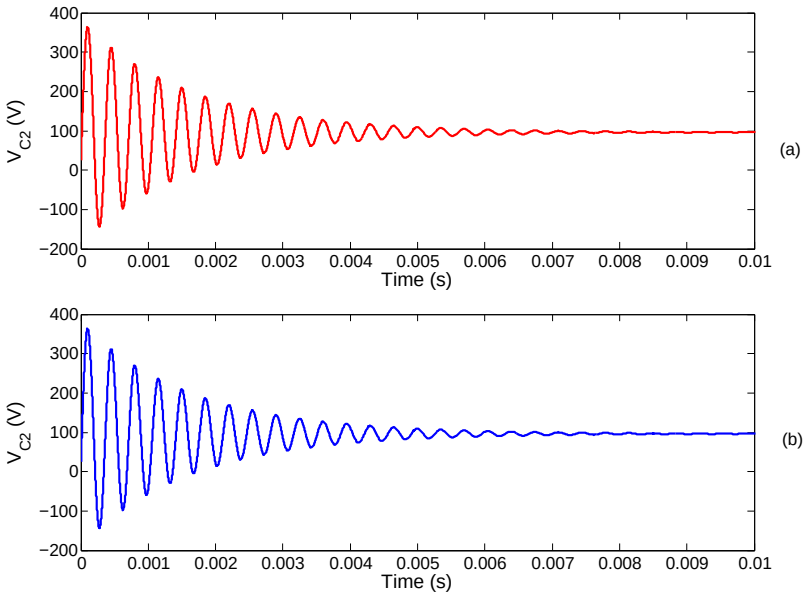

Figure 3.22: Comparison of simulated (a) and calculated (b) post fault clearance equivalent circuit voltage transient

3.5 Chapter 3 summary

This chapter has derived the necessary analytical expressions to allow the specific protection challenges caused by the natural response of highly capacitive converter interfaced DC networks to be quantified. Three discrete periods for the network were considered, with detailed analytical expressions presented for not only the initial fault response but also how the network responds during protection operation and following the clearance of a fault. The understanding of network response provided by these equations during these phases enables the various protection requirements of a specific DC power system to be determined and this will be demonstrated in subsequent chapters.

3.6 Bibliography for Chapter 3

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Chapter 4

Determination of protection system requirements for DC electrical power networks

This chapter will illustrate how the analytical tools developed within Chapter 3 can be utilised to first quantify specific challenges in the protection of DC networks and then use this information to determine operating requirements for a network's protection system. Aspects of this quantification are supported using power system simulation software, however the chapter will highlight the value in also having the understanding and capability to analytically define the various aspects of a system's fault response. Particular benefits of this approach are that it becomes more straight forward to identify dominant parameters or variables influencing a systems response and quantify the impact of a range of different initial operating conditions. This is emphasised in later sections of the chapter which describe simplified methods for assessing fault response, based on the more detailed analysis beforehand, whose use is enabled by having identified these dominant factors. Within this chapter, these techniques are effectively employed to readily quantify the impact of component changes on the fault response within a network.

Prior to illustrating how operating requirements can be quantified, the following section will first discuss how the network and protection system design may influence the protection strategy employed. In particular the section discusses how having the capability to operate circuit breakers before severe transients develop may facilitate a reduction in network components (protection devices and system redundancy) and benefit overall system design and operation. On the basis of this identified protection strategy, the rest of the chapter utilises the

analysis presented within Chapter 3 to quantify the requirements to achieve these goals. Requirements are quantified in terms of operating time for different fault types/locations and network configurations and the subsequent impact this may have on post fault transients and circuit breaker requirements. Finally, the chapter assesses the impact of the derived operating criteria on the choice of circuit breaker technology utilised within a particular application's network. The work presented in this chapter has formed the basis of a number of publications, the details of which are shown in [1–4].

4.1 Optimising protection system to match design criteria

From the review of network architectures and potential protection solutions and devices conducted within Chapter 2, four general approaches to ensure safe operation of any electrical network during fault related transients are apparent. These are:

1. Design the network components to withstand and ride through the transient conditions.

2. Place suppression devices (such as snubbers) in the network to reduce the severity of the transients to acceptable levels.

3. Provide redundancy in the network functionality such that if any component or group of components is adversely affected by a fault transient, a backup healthy system is available.

4. Install a fast acting protection system to isolate the fault before the severe transient develops.

In practice, it is likely that a suitable mix of all four methods would be applied within a network design. However, the extent to which each is employed is dependent on the requirements of the application. The first three methods could represent a substantial increase in overall system size and weight and as such are less desirable, in aircraft and ship systems at least, than the fourth option. However the approach taken will be a question of how best to achieve the levels of reliability required for the application. For example in current aircraft designs, the safety critical nature of the electrical system is such that option 3 is often extensively employed [5, 6].

The author believes that the fourth option presents what appears to be the ideal, and novel, solution and this is the focus of the research reported in this chapter. It is a potentially lightweight method (as it does not require any additional components unlike options 1-3 above) and would minimise both damage to components and disruption to the rest of the network due to the early interruption of the fault. This however is a very challenging solution to implement. To provide a measure of this challenge, the following sections within this chapter provide methods to quantify protection operation requirements for a range of criteria, network and fault types.

4.2 Impact of current response on protection system requirements

Chapter 3 provided a number of expressions to represent the current response under fault conditions as well as emphasising that analysis of the current during the period of capacitive discharge is of particular importance in the protection of compact DC networks. It is the purpose of this section to more clearly illustrate how the different characteristics between networks of varying scale can impact the requirements of the protection system.

Building upon the analysis developed within Chapter 3, the section will derive parameters of particular relevance to the protection requirements of a network. Appropriate examples will be provided to support this analysis.

4.2.1 Impact of peak fault current and time to peak on protection system requirements

The time taken for the current to reach its peak magnitude can be approximated from equations

$$t_{peak} = \frac{1}{\omega_d} \arctan \frac{\omega_d}{\alpha} \tag{4.1}$$

and

$$t_{peak} = \frac{\ln \left({}^{s_2}/_{s_1} \right)}{s_1 - s_2} \tag{4.2}$$

which were derived in the previous chapter. To provide an illustration of how (4.1) and (4.2) can be used to help determine protection system requirements table 4.1 shows the parameters of a typical UAV network (such as that shown in figure 3.1) compared to that of two different sized sections of a ship [7] and a microgrid [8].

The characteristics of compact DC UAV and small aircraft networks are such that under short circuit fault conditions, current response is more likely to be underdamped, and hence (4.1) would be used in these cases. In contrast; microgrid, ship and many other multi-terminal DC networks considered within the literature are more likely to represent overdamped cases due to their longer line lengths (and hence reduced ω_0). The differences between these can impact the operating requirements of associated protection systems.

The calculated peak magnitude and time to peak for the fault currents associated with the converter interfaces of the UAV, ship and microgrid networks, with fault distance relative to network size, are presented within table 4.1. Within this table, the parameters relating to the UAV network are derived from those presented within Chapter 3, the microgrid network from [8] and the ship network from a combination of parameters presented in [7] and representative cabling data. Data based on larger cable area (and hence lower resistance) was adopted for the shipboard application due to its typically higher current carrying requirements [7].

Table 4.1: Comparison of calculated typical fault current response for different DC system applications

Parameters/Network Type	UAV	Ship (30m)	Ship (60m)	Microgrid
Operating Voltage (V)	270	440	440	400
Main filter capacitance size (mF)	10	30	30	56
Capacitor equivalent series resistance (mΩ)	5	3	3	2
Cable inductance (μH/m)	0.65	0.387	0.387	0.34
Cable resistance (mΩ/m)	0.801	0.083	0.083	0.641
Total cable length in fault path (m)	10	30	60	60
Time to fault current peak (μs)	357.0	852.8	1203	1048
Peak magnitude of fault current (kA)	7.49	18.28	12.86	7.41

There are a number of key factors which determine the fault response characteristics demonstrated in this table. For example, differences in voltage levels and the size of the rectifier filter capacitor have a significant impact on peak current magnitude. Table 4.1 also illustrates the important impact cable length (and associated network damping levels) has in determining fault response. This is particularly evident when comparing the two ship sections in this table, as the 30m section has a significantly higher peak current and it occurs far earlier than for the 60m ship section.

The general trend shown in table 4.1 is that the more compact the network,

the shorter the time from fault inception to current peak. The rapid fault development in the UAV network in particular creates far more demanding operating requirements for the network protection system if severe transients are to be prevented. This aspect is explored further in section 4.6.

A further point to note is that the times to current peak in table 4.1 are far shorter than the standard protection operating time of aircraft [9,10], ship [11] and microgrid systems [8]. Therefore the attempted operation of protection within these time frames requires a much faster response than is currently implemented.

4.2.2 Impact of an upper current threshold on the protection system requirements

Whilst establishing a representative figure for the peak current and time to peak allows better understanding of a network's fault response, it is an inexact measure as the network response is highly variable with fault type (voltage, impedance etc) and location. For example, within table 4.1, although the ship and microgrid systems are larger than UAVs and so faults may typically be more distant, a fault could also occur much closer to the converter terminals. In this case, the time to peak for all three networks would be more similar. Therefore the time to peak figures in table 4.1 do not represent a fixed protection operating criterion (instead focusing on a single fault location).

To derive a more precise operating requirement, this section instead assesses the time at which current reaches a specific threshold value for a range of fault locations. This current threshold could represent a range of conditions such as the maximum circuit breaker rating or maximum allowed current through certain components and hence the network design would contribute to the operating characteristic.

To assess the time at which current reaches this threshold, t_{thres}, for a particular current threshold, labelled I_p, Newton's method can be used, as was described in Chapter 3. To assess t_{thres} at I_p, the Newton's method equation becomes

$$t_{thres+1} = t_{thres} - \frac{i_L(t) - I_p}{\frac{di}{dt}} \tag{4.3}$$

where $i(t)$ and $\frac{di}{dt}$ are the appropriate under or overdamped expressions identified previously. Within (4.3), $i(t)$ and $\frac{di}{dt}$ will vary with fault type and location as the parameters R and L (and hence ω_d and α) will change. To illustrate the impact of changing fault location, a new parameter which represents the proportion of line length along which a fault occurs, named n_f, is introduced. This parameter

is illustrated within the network shown in figure 4.1, where n_f is representative of the proportional distance between the converter terminals and the busbar.

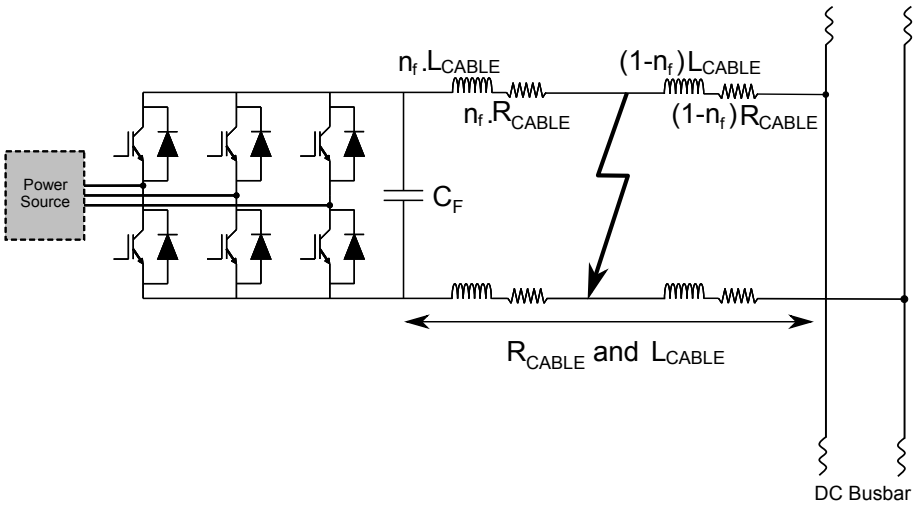

Figure 4.1: Line protection with variable zone coverage and fault detection areas

For the network setup shown in figure 4.1 using the UAV network parameters described in the previous section, figure 4.2 provides an example output from (4.3) under zero impedance fault conditions and with a range of current thresholds. The figure plots the time at which the specific threshold is reached for a given fault location (n_f). Within this figure the current thresholds, from top to bottom are: $8kA$ (green line), $7kA$ (blue line), $5kA$ (lime green line), $3kA$ (dashed green line), $1kA$ (dashed lime green) line, $0.5kA$ (dashed blue line).

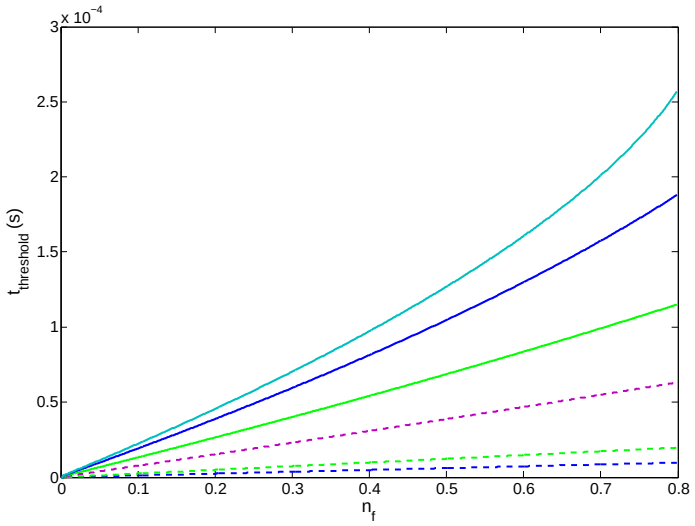

Figure 4.2: Comparison of calculated time to current threshold for a range of fault locations

Figure 4.2 illustrates that there is a wide variability of protection operating time requirements depending on both current threshold and fault location. In

general, the lower the current threshold, the stricter the operating requirement. However, the exception to this is for very close up faults, where the required operating time for all the thresholds tend towards zero. For these cases it is clear that very little time exists for wider protection system coordination, although this may not be necessary for these close up fault conditions. This response suggests that dedicated capacitor protection, as proposed within [12], may be required to ensure protection operates sufficiently quickly. However, as Chapter 2 discusses, the coordination of dedicated capacitor protection with the wider protection system for more distant faults remains a barrier to its implementation. Later chapters discuss how this can be achieved in a more coordinated way.

4.3 Impact of voltage response on protection system requirements

The protection operation requirements pertaining to a network's voltage response can be derived in a similar manner to that outlined in the previous section. However, as Chapter 3 identifies, the occurrence of both undervoltage and overvoltage conditions are of interest when considering voltage response. Both of these conditions have the potential to cause protection to operate (such as that of power electronic interfaces), with overvoltage conditions in particular having the potential to cause damage to sensitive network components. This section therefore provides analysis to quantify how a faulted network voltage response impacts on the protection operation requirements, beginning with undervoltage protection presented in the following section.

4.3.1 Undervoltage protection

Following the occurrence of a fault, the network voltage tends to decrease. The fault location and impedance determine the rate of decrease and final steady state voltage. Under short circuit or low impedance fault conditions it is likely that voltage will rapidly decay to around zero, potentially causing any undervoltage protection within the network to operate. This would result in poor protection system coordination.

The time at which the network voltage will decay to this undervoltage threshold can be calculated in a similar way to that presented within section 4.2 using Newton's Method. To determine the time at which voltage will reach a specific

threshold, labelled V_p, the Newton's method equation becomes

$$t_{thres+1} = t_{thres} - \frac{v_{CF}(t) - V_p}{\frac{dv}{dt}} \tag{4.4}$$

where $v(t)$ is the under or overdamped voltage expression derived previously and $\frac{dv}{dt}$ is their respective derivatives (expressions for under or overdamped $\frac{dv}{dt}$ are developed in Chapter 5 but are not presented here to avoid repetition).

To give an example of how (4.4) may be applied, figure 4.3 plots a comparison of time to voltage threshold for a range of fault locations and thresholds using the UAV network parameters described in section 4.2. Within figure 4.3, the voltage thresholds, from top to bottom, are: $0V$ (dashed dark green line), $10V$ (dashed black line), $50V$ (dashed lime green line), $100V$ (dashed blue line).

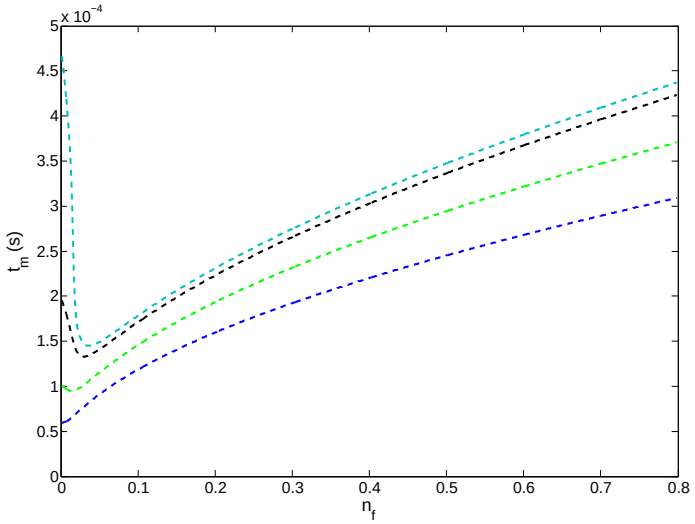

Figure 4.3: Comparison of calculated time to voltage threshold for a range of fault locations and voltage thresholds

Figure 4.3 highlights that the higher the undervoltage threshold and the closer the fault to the source, the stricter the protection operating requirement. Whilst the time of undervoltage is smallest for close up conditions, the rate of voltage decrease is more limited by the capacitor ESR than current and so none of the characteristics tend to $t \approx 0$ in the same way. Therefore if a current threshold does exist then this is likely to be a dominant factor in determining operating requirements for the close up fault conditions. Figure 4.3 does however highlight that where current is not considered, the requirement to operate protection prior to an undervoltage threshold still leads to a tight operating time (less than $50\mu s$ in this case) compared with that of traditional power system protection.

4.3.2 Impact of converter voltage reversal on protection system requirements

Chapter 3 also discusses a situation where, following the occurrence of the fault current peak, the voltage at the converter terminals can reverse, causing current to flow through the freewheeling diodes of the converter. This current was derived to be

$$i_d(t) = \frac{v_{CF}(t) - V_d}{R_d}. \tag{4.5}$$

The effective total on-state resistance of the freewheeling diodes (R_d) is typically in the order of a few milliohms [13] and as such, even small voltage reversals may result in significant currents flowing through these diodes. An example of this type of response is presented in figure 4.4, which illustrates the reverse voltage across and subsequent current through a freewheeling diode following a short circuit fault, again using the UAV network parameters for the purposes of illustration. Within this figure, time $t = 0$ is representative of the point when the diode begins to conduct. In addition to the parameters already described in table 4.1, $V_d = -0.8V$, $R_d = 1m\Omega$ and an initial current of $i_L(0) = 7.49kA$ are utilised within this example. These parameters are representative figures and will vary with the converter interface.

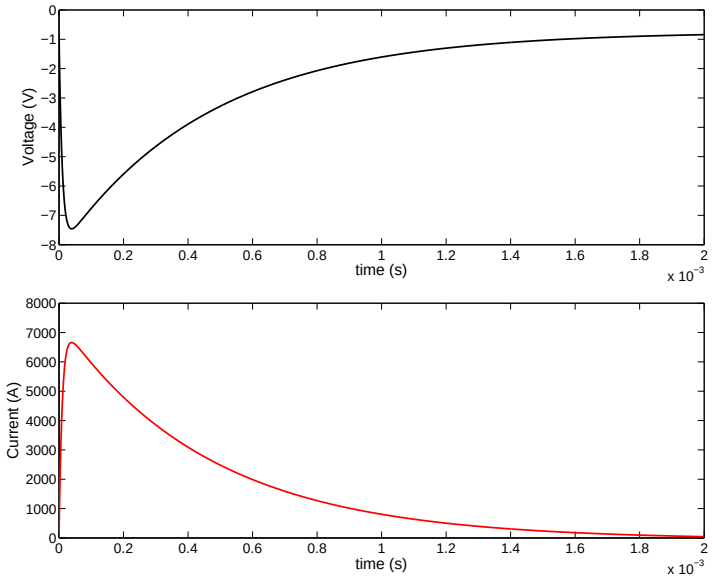

Figure 4.4: Calculated: (a) Voltage across a converter freewheeling diode and (b) subsequent current through the diode

A magnitude of current flow, such as that illustrated within figure 4.4, presents a risk of the diodes being damaged [8, 14], and the active switch overcurrent

thresholds being exceeded (in the case where these are switched on in parallel with the diodes) and the converter shutting down (if it has not done so already). In order to accommodate this risk, potential solutions include using diodes with higher rated transient current withstand or installing current suppression devices to reduce the initial transient. Either option is likely to have associated space and weight penalties. These options can be avoided if the relevant protection systems can be guaranteed to operate before the voltage reversal occurs.

4.3.3 Impact of overvoltage transients on protection system requirements

Section 4.1 discussed the benefits of utilising fast acting protection within compact DC power systems, and subsequent sections have highlighted specific areas where it can be beneficial. However, consideration must also be given to the transient voltage effects produced by operating at near peak fault current levels. Chapter 3 highlights the possibility of high voltage transients occurring on the smaller load capacitors on the DC network, through either transient recovery voltage or current chopping effects. This section will illustrate in particular how changes in the operation time of network protection can influence the magnitude of post fault voltage transients.

To show how the maximum voltage transient changes with time, the network in figure 3.1, using UAV network parameters, was simulated with a fault across a converter interfaced load. Simulation is utilised in this case to capture all transient effects from parallel conduction paths. The network converters are modelled as described in Chapter 3. The nearby circuit breakers were then set to operate for a range of fault clearance times after fault inception. The results are illustrated in figure 4.5, where maximum transient voltage magnitude is plotted against circuit breaker operating time and fault current at the time of protection operation. Maximum voltage magnitude in this top plot is measured through a number of iterative simulations with circuit breaker operating time iteratively increasing. The voltage difference between the load and filter capacitors is also shown in the subplot to illustrate its effect on maximum transient voltage magnitude.

Figure 4.5 illustrates that there is a period after the fault inception where the operation of protection may cause voltage spikes of up to 1.75 times the nominal system voltage at load converter terminals. The peak voltage transient is shown to occur just before the interruption of peak fault current. It does not coincide exactly with the peak current due to the changing voltage difference between the load and filter capacitors.

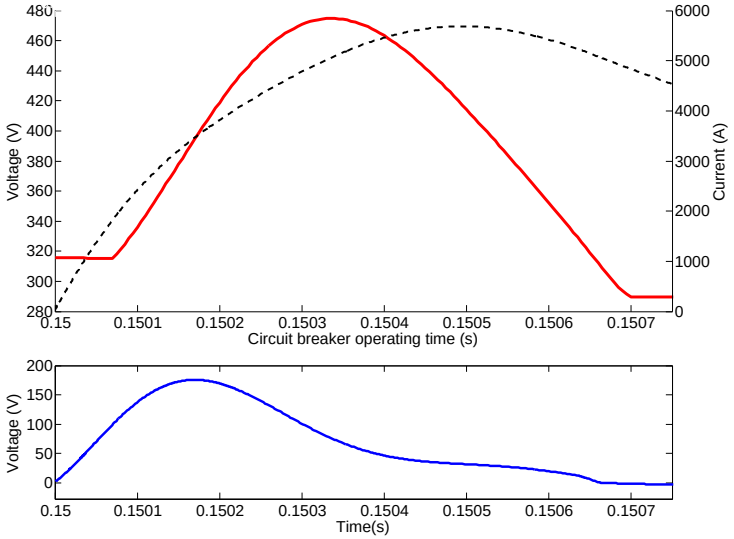

Figure 4.5: Simulated maximum voltage caused by circuit breaker operation (upper plot - solid line) after a short circuit fault occurs at 0.15s compared to varying initial conditions. Potential fault current (upper plot - dashed line), capacitor voltage difference (lower plot).

Given that the capacitors considered in this example are connected across converters, care must be taken that these converters are not damaged through fault clearance events [15], or almost as importantly, do not trip due to overvoltage protection operation. Either of these events could results in the effects of the fault propagating into healthy parts of the network causing cascaded tripping and equipment damage.

As in previous sections, solutions to the issue of overvoltage transients include up-rating components [15], employing voltage suppression devices, both of which have associated weight penalties, or operating the circuit breakers early enough in advance of the fault current peak (or at least actively managing the circuit breaker operating time to avoid conditions where its operation would cause significant voltage transients). The latter option is consistent with previously discussed requirements for voltage reversal prevention and maximisation of system survivability and is hence the preferred, although most demanding, solution.

4.4 Impact of circuit breaker performance on protection system requirements

Due to the time varying nature of typical fault current profiles in DC networks, the timing of circuit breaker (CB) operation can impact the performance of the devices. With suitable examples, this section will illustrate how the CB operating time impacts on the energy dissipation requirements of the CB, the voltage developed across the breaker and the total time taken to clear the fault.

4.4.1 Impact on circuit breaker energy dissipation

One means of measuring how the protection operating time can impact circuit breaker design and performance is to assess how it influences the energy which must be dissipated in order to clear the fault. As Chapter 3 states, this dissipation may take place in an arc but its impact is perhaps easier to quantify by assessing the impact on the design of a voltage snubber circuit [16].

To derive a representative value for these energy dissipation requirements, the analysis in Chapter 3 assumes that all series line inductance energy is dissipated in the circuit breakers. An example of how this energy varies with operating time for the UAV network described in table 4.1, is shown in figure 4.6.

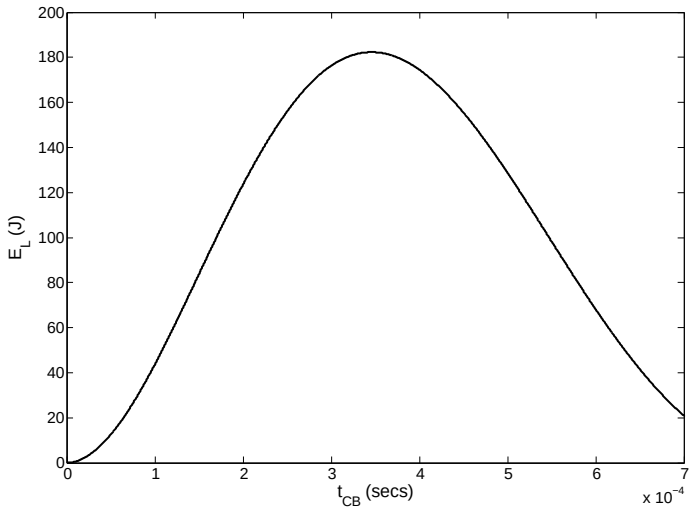

Figure 4.6: Calculated inductive stored energy to be dissipated in the CB against operating time

Figure 4.6 illustrates that there is a significant variation in the energy dissipation requirements of the CBs depending on the time at which they operate,

with a range of close to $0J$ (this is zero in the plot as pre-fault (load) current is neglected) to around $180J$. The required energy dissipation for a particular CB will impact on its arc or snubber requirements, the device size and weight, and ultimately, the overall power system design. It is clear from figure 4.6 that guaranteed early or late operation of the breaker would minimise the energy dissipation requirements, although late operation is less desirable as it would require the CB to carry a large current and would permit more energy to be delivered to the fault. This aspect is also investigated in further detail in later sections.

4.4.2 Impact on circuit breaker voltage and fault clearance time

Within equation (3.51) in Chapter 3 it is shown that the time in which fault current is driven to zero, T_2, and the peak voltage developed across the circuit breaker, v_{CBpeak}, are dependent on one another. Therefore to appropriately illustrate the relationship between T_2, v_{CBpeak} and the circuit breaker operating time, t_{CB}, it is necessary to plot v_{CBpeak} for a range of both T_2 and t_{CB}. An example output of this plot, using the UAV network parameters, is shown in figure 4.7.

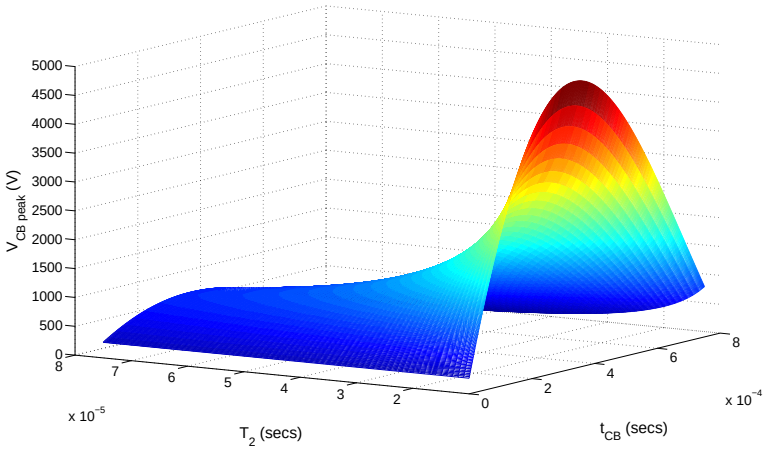

Figure 4.7: Calculated impact of CB operation time and fault clearance time on required circuit breaker voltage

Figure 4.7 describes the relationship between v_{CBpeak}, T_2 and t_{CB} with a selected range of 0 to $750\mu s$ for t_{CB} and $10\mu s$ to $750\mu s$ for T_2 for this particular illustration. Figure 4.7 shows that v_{CBpeak} is greatest when t_{CB} corresponds to the peak fault current magnitude and when T_2 is at its minimum (hence forcing current to zero more quickly). For this example, the maximum voltage condition is around 5kV, which for a 270V system is clearly unacceptable. The figure shows

that if the CB voltage is to remain within an acceptable range there is a trade off between t_{CB} and T_2. To further illustrate this point figure 4.8 shows a plot of T_2 against t_{CB} for a fixed v_{CBpeak} of 540V (two times the nominal voltage level).

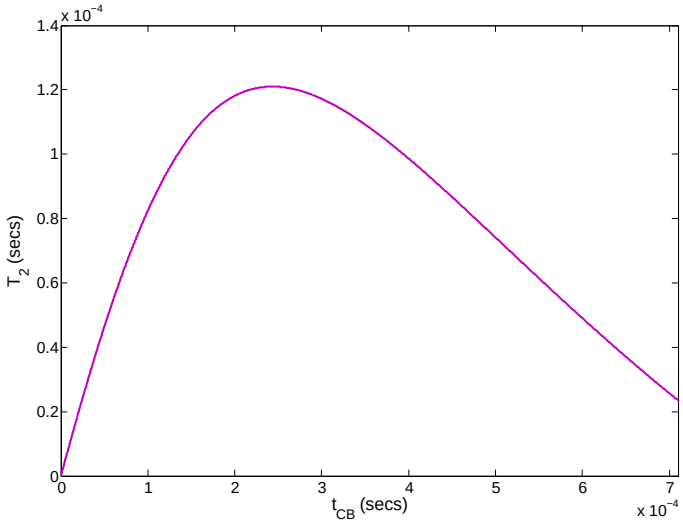

Figure 4.8: Calculated example T_2 against t_{CB} plot for a peak CB voltage of 540V

Figure 4.8 illustrates that the above analysis can be used to set voltage limits on the CBs from which the relationship between T_2 against t_{CB} can be derived. The figure shows that specifying a maximum CB voltage leads to a wide range of clearance times as the fault current extinction is limited to adhere to this peak device (or conductor) voltage.

4.4.3 Impact on fault energy let through

To illustrate how fault energy let through (I^2t) varies with t_{CB} and T_2, the example case shown in figure 4.8 (where v_{CBpeak} is limited to 540V) is analysed. This can be achieved using equations derived in section 3.2 of Chapter 3. The results of this analysis are presented in table 4.2.

Table 4.2 highlights that operating protection early minimises T_2 and hence the energy delivered into the fault. As t_{CB} and T_2 increase so does the respective I^2t energy delivered within each period, as is to be expected. The table emphasises that due to the rapid increase in the fault current, the increase in I^2t energy is proportionally much greater than the increase in time. For example, an increase in the circuit breaker operating time from $50\mu s$ to $600\mu s$ (a factor of 12), increases the total I^2t fault energy by a factor of 175. In these terms, it is clearly beneficial to operate protection within the minimum time possible.

Table 4.2: Calculated comparison of I^2t fault energy for a range of circuit breaker operation and fault clearance times

t_{CB} (μs)	T_2 (μs)	Clearance time (μs)	I^2t ($t \leq t_{CB}$) (A^2s)	I^2t ($t > t_{CB}$) (A^2s)	Total I^2t (A^2s)
50	46.4	96.4	62	60	122
100	82.4	182	481	370	851
250	121	371	5222	1935	7157
400	98.7	499	13.3×10^3	1768	15.1×10^3
600	49.1	649	21.1×10^3	343	21.4×10^3

4.4.4 Discussion of results

This section has presented analysis which aids the assessment of the impact of circuit breaker operating time on the environment within which they operate for a representative UAV network. It has shown that there can be significant differences in energy absorption and voltage or clearance times, as well as energy delivered to the fault. As each factor has the potential to influence the optimal design of the circuit breakers utilised within the network, the work aims to not only quantify the requirements of CB devices under certain operating conditions, but also understand which protection operation conditions are the most favourable for overall aircraft network design. By highlighting how requirements change with operating strategy, it is hoped that the protection scheme can be designed in a way to target these most favourable operating conditions and hence optimise the design of the protection system and/or the overall network.

The analysis also highlights that a trade off often exists between optimal circuit breaker design and optimal network operation. A particular example of this is the analysis of circuit breaker voltage and fault clearance time. Operationally it may be best to use larger, higher voltage circuit breakers to minimise the time taken to clear the fault. However, this would have associated space and weight penalties, potentially impacting on overall system design. It is therefore essential that electrical system protection is considered at the earliest design stages to ensure that this trade off is managed most efficiently.

Within each of the above sections however, it is clear that the very early operation of network protection can minimise the requirements of circuit breakers without compromising the level of network protection offered.

4.5 Analysis of networks containing addition filter or current limiting components

The networks considered so far in this thesis do not contain fault current limiting devices or additional filter components, beyond that of the converter terminal capacitance. Whilst the networks containing these devices fundamentally behave in the same way as those assessed previously (and hence can be analysed in the same way), from a practical perspective, the analysis of their impact on protection requirements is worthy of consideration, particularly given their potential to mitigate large fault transients. As introduced in Chapter 2, both resistive [17] and inductive [18] fault current limiter (FCL) devices could be utilised to reduce current magnitude and rate of current rise of multiple fault current sources, allowing the transient to be reduced to a more manageable level.

This section therefore provides examples of the possible impact of these devices on protection system performance requirements. As part of this section, methods are presented to help simplify the analysis presented in Chapter 3 to readily quantify the effect of placing additional inductance and resistance on the network between the capacitance and main busbar connection on the fault response. These cases are analysed and discussed in follow two sub-sections, beginning with the impact of increasing line inductance.

4.5.1 Consideration of converters containing series inductive filters or current limiters

The majority of proposed network architectures for future DC networks which employ VSCs operate without the use of inductive filters [8, 12, 14, 19–21], however where they exist these devices will impact on the network fault response. Similarly, inductive FCLs [18] are not always considered for use in DC systems, as they do not limit steady state current. However their potential to help manage current transients makes their impact worth considering. Assessment of the impact of either of these additional sources of inductance can be easily accommodated into the analysis presented earlier in this section by setting inductance L equal to the sum of line and filter or FCL inductances. The following sections will consider the impact of these devices on the magnitude of current and rate of current rise as well as relating this back to the analysis of circuit breaker operating requirements.

Effect on peak current magnitude

The impact of the additional series inductance is most clearly shown by first considering a representative lossless (without resistance) network. An expression for the lossless circuit current can be derived from (3.12) in Chapter 3 by neglecting resistance. This equals

$$i_{peak} = \frac{v_{CF}(0)}{Z_0} + i_L(0) \tag{4.6}$$

where all terms are as defined previously. From (4.6) if it is again assumed that initial current $i_L(0)$ is negligible, it can be approximated that the peak current is equal to $\frac{v_{CF}(0)}{Z_0}$. The peak therefore becomes inversely proportional to $\sqrt{L}$. Therefore increasing L by 50 times, for example, would decrease the current peak by 7.07 times. As resistance is not included in this calculation, the impact of inductance is at its maximum and hence $\sqrt{L}$ is the maximum by which the current peak changes.

To illustrate how the simplified expression in (4.6) can be best utilised, consider its application to sizing a FCL device. If applying a current limiting device, it is desirable to design the system to limit current to a specific current level. To determine the inductance required to achieve this, (4.6) can be simply rearranged to make the limiting inductance the subject of the equation. This inductance is

$$L_{lim} = \left(\frac{v_{CF}(0)}{i_{peak}}\right)^2 \times C_F \tag{4.7}$$

where L_{lim} is the total inductance required to limit the peak capacitor output current to i_{peak}, including line inductance.

Relating this to the UAV network example shown in table 4.1, the peak capacitive current contribution, neglecting resistance, is

$$i_{peak} = \frac{270}{\sqrt{\frac{6.5\times10^{-6}}{10\times10^{-3}}}} = 10.59kA. \tag{4.8}$$

Note that this is greater than the value reported in table 4.1 due to the removal of resistance for this analysis.

If the capacitor contribution is limited, to say 1.5kA ($\approx$ 7.07 times less than (4.8)), by increasing inductance, this limiting inductance can be calculated from (4.7). Substituting parameter values into (4.7) gives

$$L_{lim} = \left(\frac{270}{1.5k}\right)^2 \times 10 \times 10^{-3} = 324\mu H \tag{4.9}$$

where L_{lim} is the total inductance required to limit the peak capacitor output current to 1.5kA. L_{lim} in (4.9) includes line inductance, and so this can be subtracted depending on considered fault location, however the inductance calculated would need to ensure that current is limited to 1.5kA for all fault locations.

Effect on time to current peak

Of perhaps more significance from a fault detection perspective is the impact of the additional inductance on the rise time and time to peak of the current response. Simplifying (3.15) in Chapter 3 by again neglecting resistance, a direct relationship can be seen between time to peak, t_{peak}, and inductance. When resistance is neglected, t_{peak} occurs when $\sin(\omega_0 t) = 1$ and so equals

$$t_{peak} = \frac{\frac{\pi}{2}}{\omega_0}. \tag{4.10}$$

From (4.10) it can be seen that t_{peak} is now directly proportional to $\sqrt{L}$. Therefore if inductance is increased by a factor of 50, t_{peak} would increase by approximately 7.07 times. To illustrate this point, again consider the response of the UAV network in table 4.1. Without resistance t_{peak} can be calculated as

$$t_{peak} = \frac{\frac{\pi}{2}}{\frac{1}{\sqrt{10\times10^{-3}\times6.5\times10^{-6}}}} = 400.5\mu s. \tag{4.11}$$

Now substituting the limiting inductance derived in the previous section into (4.10), t_{peak} changes to

$$t_{peak} = \frac{\frac{\pi}{2}}{\frac{1}{\sqrt{10\times10^{-3}\times324\times10^{-6}}}} = 2.83ms \tag{4.12}$$

This revised t_{peak} represents a significant increase on the previous value (and that reported in table 4.1). Depending on the protection operating strategy, this potentially allows more time for the detection and isolation of faults, reducing demands on the protection system.

Effect on stored energy and circuit breaking requirements

Additional inductance will change the amount of stored energy in the network under steady-state and transient conditions, which will impact on circuit breaker energy dissipation requirements and post-fault clearance voltage transients. To illustrate this difference in stored energy, the peak stored energy of the limited and non-limited current responses from the previous section will be compared. In

the calculation initial load current is required to be included to take account of the difference in stored energy pre-fault. The example UAV network has a peak steady state input of 74.07A (20kW at 270V). Including this, the peak stored energy without the FCL is

$$E_L = \frac{1}{2} L I_{peak}^2 \tag{4.13}$$

and substituting values

$$E_L = \frac{1}{2} \times 6.5 \times 10^{-6} \times (10.59k + 74.07)^2 = 369.6J. \tag{4.14}$$

With the FCL in place the peak stored energy is

$$E_L = \frac{1}{2} \times 324 \times 10^{-6} \times (1.5k + 74.07)^2 = 401.4J. \tag{4.15}$$

The calculations show that there is some increase in peak stored energy when the additional inductance is included in the network, although this is reasonably modest due to the limited steady state current. This energy increase is a function of load current prior to the fault and the fault path inductance. The energy contribution from the capacitance will be the same in both cases as the system considered is lossless and all energy will be transferred from capacitance to inductance, although this transfer will occur at a slower rate when the larger inductance is in place. The increase in inductive stored energy in the current limited circuit will result in higher post fault overvoltages when current is interrupted, as described in section 4.3.3. It will also result in higher circuit breaker energy dissipation requirements, as section 4.4 describes.

The inclusion of additional inductance will also impact circuit breaker voltage, fault clearance time and fault energy let through, however the analysis of these variables (as described in sections 3.2 and 4.4) is such that they are not readily quantifiable in the simplified style presented above. However an alternative method of analysing how inductance changes the maximum circuit breaker requirements is to consider the snubber or voltage suppression requirements of a CB device, in particular a SSCB. The voltage across a SSCB device can be limited with a resistive-capacitive snubber [16]. If this is simplified to be purely capacitive, the size of this capacitance for a set maximum voltage transient can be easily quantified for the limited and non-limited circuit cases. Limiting the voltage across the SSCB to say 540V (twice the nominal aircraft voltage level of 270V), and assuming that all of the energy stored in the inductance is transferred to the capacitive snubber, the required capacitance can be calculated. For the

non-limited circuit, the required capacitance is

$$C_{snub} = \frac{2E_L}{V_{max}^2} \tag{4.16}$$

and substituting values

$$C_{snub} = \frac{2 \times 369.6}{540^2} = 2.53mF. \tag{4.17}$$

For the circuit with the inductive FCL, with the SSCB operating at peak current, the required capacitance is

$$C_{snub} = \frac{2 \times 4.01.4}{540^2} = 2.75mF. \tag{4.18}$$

This shows that there is some increase in capacitor size requirements when interrupting peak current levels. Although this increase is again modest for this example, in general greater snubber capacitance has additional space requirements and, in a similar way to reducing arcing voltage (as described in section 4.4), a larger capacitance leads to a slower voltage increase and hence later current zero and slower interruption of fault.

4.5.2 Effect of including resistive FCLs

The only practical purpose for the connection of additional series resistance into a power network is for current limiting. When considering the impact of an additional series resistance, the expressions are not as straight forward to simplify because of the important role the line inductance plays in the initial current response. Definition of the analytical response of a network containing resistive FCL is further complicated by the variable resistance of the FCLs themselves, which can change depending on various aspects such as current and temperature [17]. Therefore the analysis presented in this section will provide an approximation of how the network response changes with a resistive FCL installed but will not replace dynamic simulation in terms of accuracy measuring their impact. This is less of an issue for the inductive FCLs as under normal operating conditions these are typically lossless for DC systems and so can remain in the network as fixed values.

For the analysis to be conducted, rather than deriving further expressions, Greenwood and Lee [22] provide a useful method of visualising the relative effects of resistance and surge impedance in a second order RLC circuit by looking at

the ratio of these two quantities. To aid with this, a term η is defined, which is the ratio of surge impedance to resistance, given formally as

$$\eta = \frac{Z_0}{R}. \tag{4.19}$$

Greenwood and Lee [22] then derive a set of generalised curves based on η and these curves have been replicated within figure 4.9.

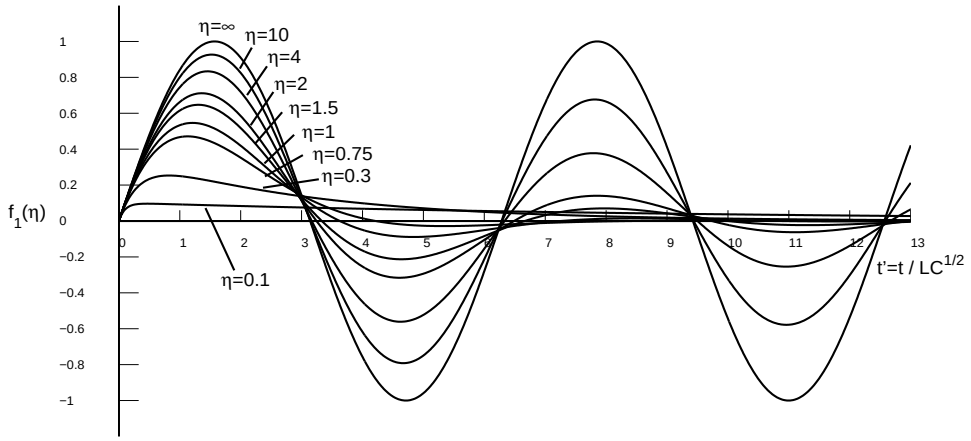

Figure 4.9: Generalised damping plots for series RLC circuits based on the ratio of surge impedance to resistance

The vertical axis on figure 4.9 shows the relative magnitude of any transient compared to the lossless case and the horizontal axis shows the relative change in phase. Therefore changes in η are shown in terms of current peak and time to peak. This makes these curves a useful tool for considering the effect of different levels of resistance in the network.

Again consider the UAV example from table 4.1. Without any resistive FCL, η can be found to be

$$\eta = \frac{\sqrt{\frac{6.5\times10^{-6}}{10\times10^{-3}}}}{13\times10^{-3}} = 1.96. \tag{4.20}$$

On figure 4.9, $\eta = 1.96$ approximately corresponds to a peak magnitude of 0.72 on the vertical axis. (This can be confirmed to be correct by multiplying this value with the lossless current peak in the previous section to find the peak current value found in table 4.1.) Therefore when no FCL is in place, the peak current is approximately 72% of that of the lossless case.

As an example, consider reducing the peak current significantly so that it corresponds to the bottom curve, where $\eta = 0.1$. For this curve the magnitude on the vertical axis is approximately 0.09, so around 9% of lossless case. The re-

duced peak current therefore now equals 982.8A, excluding the converter current contribution. The required limiting resistance to achieve this can be calculated as

$$R = \frac{Z_0}{\eta} \tag{4.21}$$

and substituting values

$$R = 0.255\Omega. \tag{4.22}$$

Taking account of line resistance, the additional limiting resistance required is

$$R_{FCL} = 0.255 - 13 \times 10^{-3} = 0.242\Omega. \tag{4.23}$$

These equations show how required resistance for a set current level (based on a proportion to the lossless case) can be easily derived based on the information contained within the generalised damping curves. The result also emphasises how a small resistance can significantly reduce current due to the relatively low impedance of the interconnecting cables.

In a similar way to the above example, the use of the generalised plots can also be used to help with the analysis of the effect of different fault and earthing resistances. The impact of variable inductance, such as the use of inductive FCLs, including the effect of resistance can also be analysed in a straight forward manner use these generalised curves. This simply involves varying the L term, which in turn changes Z_0 and η. However as L increases the response tends towards that of the lossless response and hence the previous analysis, shown in equations (4.6) to (4.9), becomes more valid.

4.5.3 Discussion on use of addition filter or current limiting components

The potential for reduction in fault current and increase in rise time suggests that, in terms of fault response, additional filter or current limiting components can be beneficial. However, as earlier sections discuss, their inclusion can increase system size and weight and contribute to undesired post-fault clearance transients (in section 4.1 the devices come into the 'snubber category'). Furthermore, additional network inductance is shown to increase circuit breaker voltage, energy dissipation requirements and fault clearance time, whilst resistive current limiters will likely lead to increased system losses during non-faulted operation. Therefore, without discounting the potential for their use, the remainder of this thesis focuses on a potentially more optimal and novel solution, without the use of any suppression

devices, based on extremely fast acting protection.

4.6 Impact of operating requirements on protection system implementation

Within previous sections it was concluded that the presence of a fast operating and selective protection system could minimise the protection equipment requirements whilst potentially providing benefits in weight, survivability and minimisation of fault effects. This section will utilise the analysis conducted previously to determine the key operating requirements for the application specific electrical protection systems such that the derived operating requirements and these benefits may be realised.

The total protection operating time can be generally defined in two discrete stages; first, the time to detect and locate the fault and determine the appropriate course of action and second, the time for the breaker to operate. The former is a function of the detection method, and the latter relates to the capabilities of DC circuit breaker technologies. The following subsections will consider these aspects in more detail, starting with the circuit breaker technologies.

4.6.1 Implications for circuit breaker technologies

In order to better appreciate the applicability of different circuit breaker types to the proposed fast acting network protection system it is first necessary to consider the range of typical operating times. For this purpose, this section compares typical operating times for different circuit breaker technologies with the typical times to current peak derived in section 4.2, which has been selected as the protection operating criteria. Depending on the specific requirements of a network, this could be substituted with time to current or voltage threshold (or an appropriate alternative), as described in previous sections. Figure 4.10 shows a range of typical operating times for solid state (SSCB) [16,23,24], hybrid (HCB) [25,26] and electro-mechanical circuit breakers (EMCB) [27,28] in relation to the derived time to peak for fault currents within UAV, ship and microgrid electrical networks. Whilst the actual time taken for the fault current to reach its peak may vary, this specific example provides a good illustration of the impact upon the choice of circuit breaker technologies for the three applications. For further information, table 4.3 provides the voltage and current ratings of the devices compared within figure 4.10.

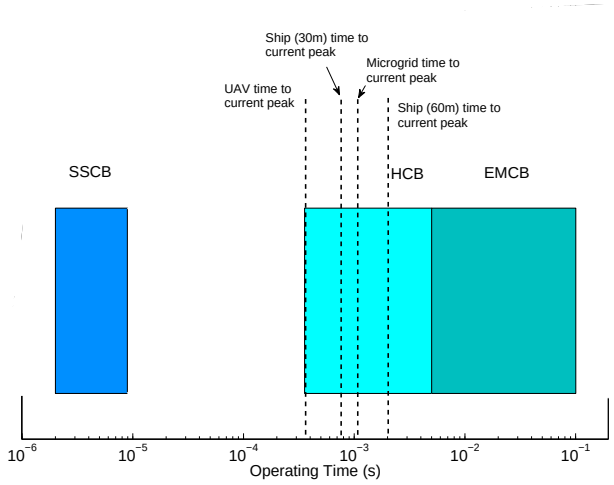

Figure 4.10: Comparison of circuit breaker operating time with time to current peak in different applications

Table 4.3: Example circuit breaker current and voltage ratings compared to operating time

Circuit Breaker Type	Rated Operating Voltage (V)	Rated Breaking Current (kA)	Operating Time (s)
SSCB	2500	1.5	5μ
SSCB	2800	4.8	10μ
HCB	1500	4	350μ
HCB (rated for AC)	12000	20	$5m$
EMCB	900-3600	2.6	3-$10m$
EMCB	270	3	$20m$

Figure 4.10 shows that the typical operating times of EMCBs are far greater than that required for all three applications. The quickest operating HCBs may be suitable for UAV applications although options for their use would be limited as there would be little additional time for fault detection and location. However, based on this time comparison, HCBs may be the technology of choice for microgrids and ships where a longer time to peak is anticipated.

The comparison between circuit breaker operating times and typical times to peak suggests that only SSCBs are currently suited for use within UAV networks, as well as allowing for longer times for discrimination in ship and microgrid protection systems. SSCBs also potentially represent the most lightweight solution [24]. Whilst few, if any, commercially available devices exist for the low voltage levels considered in the applications which have high enough current break capabilities for the currents described in section 4.2 [16] (as table 4.3 suggests), the development of these technologies will provide greater opportunity for use in future systems.

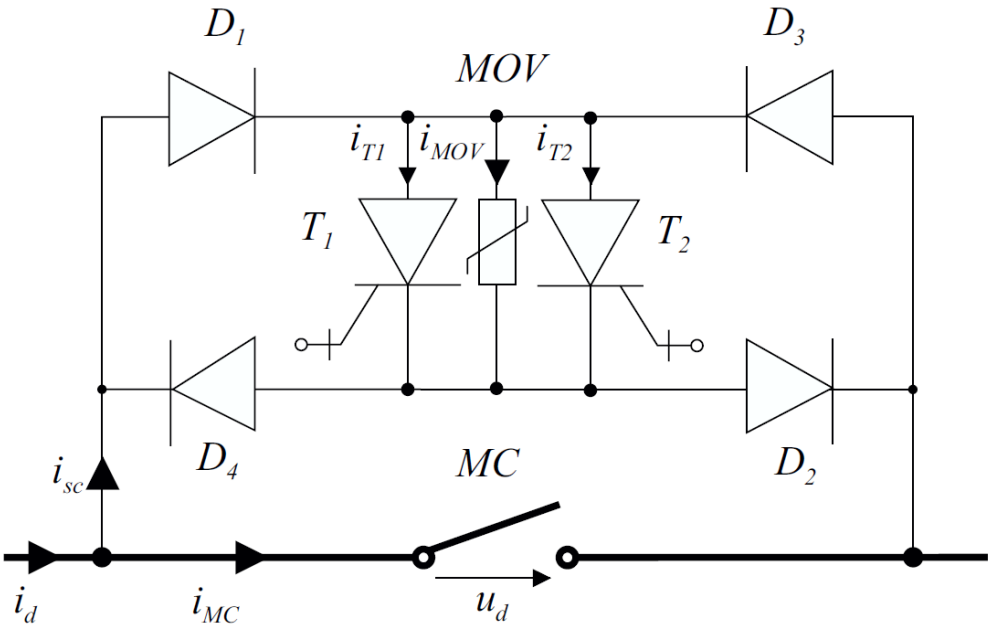

Figure 4.11: Example hybrid circuit breaker design [25]

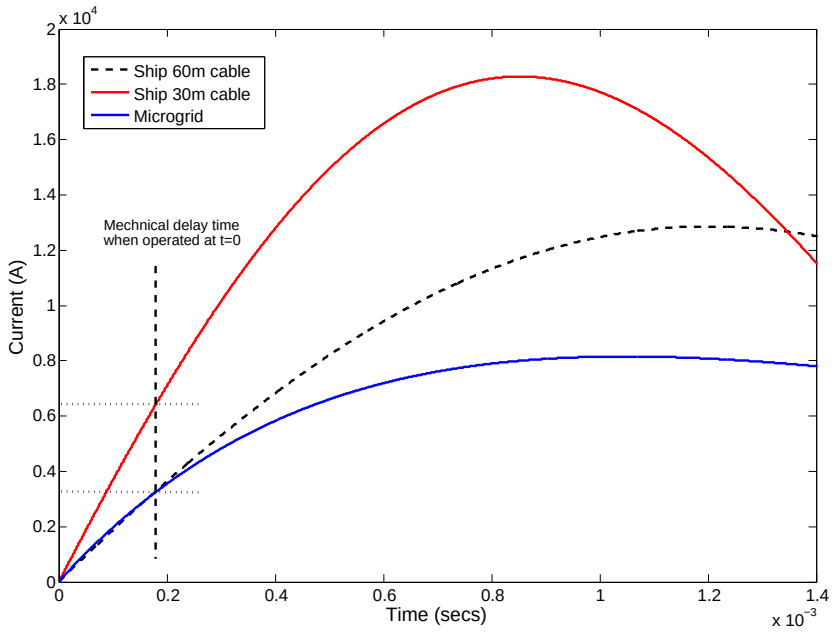

Figure 4.12: Calculated fault current profile for the microgrid and ship systems described in table 4.1

While some HCBs from table 4.3 appear to match the current breaking levels required, such as devices presented in [25, 26] which claim to operate for up to 20kA, further consideration must be given into how this is achieved. The general design of HCBs consists of a fast mechanical switch with parallel solid state switching devices, an example of which is illustrated in figure 4.11 [25]. Under fault conditions, the role of the mechanical switch is to quickly open and commutate the current to the solid state devices, with this branch containing four diodes (labelled $D_{1..4}$) to guide bidirectional current flows, two thyristors (labelled $T_{1,2}$) to control current magnitude in the solid state path and a metal oxide varistor (MOV) to mitigate switching voltage transients. To facilitate fast operation, the mechanical switch is small in design and so is not rated to interrupt full fault current. In compact systems however, the rate of current rise is such that the rated breaking current magnitude of the switch may be exceeded by the time of operation, potentially preventing correct HCB operation. To provide an example of this, figure 4.12 illustrates the calculated fault current profile for the microgrid and ship networks described in table 4.1 for a fault at time $t = 0$ (where plots are identifiable from their peak fault current). The mechanical delay time, taken from [25], is indicated from $t = 0$ on the plot, showing the minimum potential fault current which the mechanical switch would have to interrupt. Note that this indicated time does not account for the time taken to detect and locate the fault and operate the HCB. As such, the mechanical switch may operate later than indicated and be required to interrupt even greater current magnitudes. Figure 4.12 illustrates that even for the artificially short operating times indicated, the fast mechanical switch current rating would be required to be between $3kA$ and $7kA$. Whilst it is not impossible for this current to be interrupted by the HCB, multiple fast switches may need to be paralleled to achieve these current breaking levels [29].

This is an area worthy of further attention to determine whether suitable commercial devices develop from this area of research. Certainly, without the availability of the appropriate fast acting switching technologies, with suitable voltage and current ratings, truly optimised protection of DC networks will be very challenging.

4.6.2 Implications for fault detection and location methods

Figure 4.10 provides a basis for determining the maximum permissible fault location times for each of the applications protection systems. This is simply,

$$t_L < t_{peak} - t_{CB} \tag{4.24}$$

where t_{CB} is the circuit breaker operating time and t_L is the required time for the protection system to send a trip signal to the associated circuit breakers (from the time of fault inception) in order to ensure circuit breaker operation prior to the occurrence of the fault current peak. For alternative operating targets (such as a current threshold), the term t_{peak} can simply be substituted with that value.

For the UAV network, figure 4.10 and table 4.3 indicate that, acting in conjunction with SSCBs, any protection system must locate the fault within approximately $300\mu s$ in order to operate the circuit breaker before the current peak. This target time may become even less depending on the network specific requirements for avoiding the creation of post-fault overvoltage transients, as investigated in section 4.3.3. Using a similar measure for the other applications, the ship system should locate the fault within approximately $1.15ms$ (for the longer line length) and the microgrid within approximately $1ms$.

The achievement of this is constrained by the bandwidth of sensing technologies and the methods used to ensure coordination between multiple protection devices. Therefore the performance of various protection schemes, when operating within such time constraints, is an area of great research interest. The following chapter assesses the potential for available protection methods to meet this strict operating criterion.

4.7 Chapter summary

This chapter introduces the concept of how fast acting protection could have a positive impact on network design aspects such as reducing component withstand requirements and protection equipment. On this basis, the analysis developed in Chapter 3 has been used to define protection operating time requirements to achieve this level of performance. More generally, the chapter has illustrated how operating requirements for a range of different current or voltage thresholds can be quantified .

The derived requirements for representative UAV, ship and microgrid net-

works have also been compared to typical operating times for available circuit breaker technologies. From this comparison, suitable breaker technologies can be identified for a particular application. In a comparison of typical time to current peaks for the networks, it is shown that EMCBs and HCBs often fail to match operating time requirements, suggesting SSCBs are the technology of choice. This even more apparent when considering close up faults for all networks as section 4.2 highlights. This would represent a significant shift in current practice and so could represent a significant barrier to DC system implementation until SSCB technologies mature.

Finally, the comparison of operating requirement and typical breaker operating time has allowed approximate fault detection times to be derived, which are significantly smaller than those achieved currently. Potential methods for achieving these ambitious fault detection times are the subject of the following chapters. As stated, the work presented in this chapter has contributed to a number of publications, the details of which are shown in [1–4].

4.8 Bibliography for Chapter 4

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Chapter 5

Optimising the roles of unit and non-unit protection methods within future DC networks

The basic precepts of how non-unit and unit protection methods are used for fault detection were introduced within Chapter 2. To assess how these methods may be best applied to meet the unique protection challenges of physically compact DC networks, this chapter employs previously derived equations and builds on the understanding these provide with the use of appropriate case studies. Given that traditional methods were designed with much larger operating time frames in mind, and are generally based on sustained rather than transient fault behaviour, clear challenges exist for them to be employed effectively within DC networks.

To address this issue, this chapter has two main purposes. The first is to assess the capability of these existing methods to meet the strict operation criteria laid out in the previous chapter. Comparison of protection methods with these operating times has only been done to a very limited degree within literature (section 2.4.3 of Chapter 2 provides one example of this) and so this, coupled with the analytical approach taken, presents a novel angle on the assessment of traditional methods. The second main aim of the chapter is to identify the aspects of the DC network fault response which provide an alternative, and novel, means of fault detection. Two novel methods which have developed from this analysis are explored in chapters 6 and 7 respectively.

This chapter contains three main sections. It first demonstrates the challenges in applying non-unit fault detections techniques within compact DC networks and then assesses the potential for unit protection schemes to overcome these challenges. The chapter concludes by discussing how the roles of non-unit and

unit performance methods could be optimised to achieve required levels of fault discrimination whilst seeking to minimise installation costs.

5.1 Non-unit protection implementation within compact DC networks

Non-unit protection does not protect a clearly bounded zone of the power system and will operate whenever its predetermined threshold is violated; non-unit schemes have inherent backup capabilities and will act to protect the system if a neighbouring protection system fails to operate [1].

Due to the potentially high fault levels under short circuit fault conditions within DC networks, non-unit techniques, and in particular overcurrent, can be utilised to very rapidly detect faults. For example, the authors in [2] propose the use of instantaneous overcurrent protection inherent in power electronic switches to interrupt capacitive discharge currents far faster than the protection operation target of around 300μs set out in Chapter 4. However when higher levels of selectivity, i.e. ensuring that only the local protection operates for a fault at a particular location in the network, are desired, issues can arise in the implementation of overcurrent protection. This is especially true where instantaneous overcurrent protection is utilised, as will be shown within this chapter. These issues are particularly apparent where multiple relays are graded using overcurrent protection in highly capacitive networks. For example, if moulded-case circuit breakers (MCCB) are utilised at P_1 and P_2 in figure 5.1 (in the next section), for a fault across a DC load, the initial discharge current can be high enough to occupy the instantaneous trip region of both MCCBs [3], potentially tripping both P_1 and P_2 or even just P_1 [4]. This would cause significant protection coordination issues and unnecessary isolation of non-faulted elements of the system. The consequences of this would vary depending the application area, but could range from the loss of supply to customer in microgrid based systems or the loss of supply to flight critical loads in an aerospace application.

When applying non-unit methods there is also the issue of variable fault resistance and the impact this has on fault current. This is a particular issue for compact networks where, due to small line impedance, any fault resistance will make up a greater proportion of overall fault path impedance. The full effect of fault impedance on fault response will be illustrated within later sections of this chapter.

Due to these potential issues with the use of non-unit protection, the first

part of this section investigates the capability of non-unit protection methods to achieve effective protection selectivity within compact DC systems, whilst operating within the time frame identified within Chapter 4. Rather than analyse the merits of the numerous individual non-unit methods, the section first describes the current, voltage, $\frac{di}{dt}$, $\frac{dv}{dt}$, and impedance profiles as measured at a converter output for a range of fault locations and impedances within an example busbar network architecture. Both equations and simulation will be utilised within this section to analysis the potential use of these various responses. The key findings from this analysis are then reinforced using a protection scheme design case study for a microgrid network.

5.1.1 Impact of fault resistance on non-unit methods of protection discrimination

In order to illustrate fault response and assess numerous protection methods, this section makes extensive use of analysis. The expressions which are used are intended to aid understanding of transient fault response and derive parameters of interest. These are also supported by more detailed simulation. To achieve this, while still maintaining reasonable accuracy but without using unnecessarily complicated expressions, a number of assumptions have been made.

First, second order circuits and expressions are used throughout the analysis, as with previous chapters. These expressions accurately represent short circuit conditions but are more approximate where there are parallel paths to the fault or the fault itself has resistance. Use of second order approximations avoids expanding the analysis to cover multiple RLC branches, which can result in much larger analytical expressions. Reference [5] does provide a method to compensate for current flows to non-faulted parts of the network after the initial second order calculation is made. However, as discussed within Chapter 2, this lacks accuracy when calculating capacitive currents as it does not account for the impact of inductance on the current flow in parallel branches.

Second, the expressions assume that any changes in the output of the converter are negligible in comparison to the magnitude of the capacitor discharge current for the period immediately following the occurrence of the fault, due to the high rate of change of capacitor output compared to the converter [5].

Third, Chapter 3 describes the fault response as having two phases, the second of which includes voltage reversal conditions. For the purposes of this chapter, only the first phase, which represents the normal RLC circuit response, will be considered when comparing the effectiveness of various protection methods as

this is the targeted operating region.

The equivalent circuit for the faulted network which will be simulated throughout this section is illustrated within figure 5.1. Faults F_1 and F_2 have been placed at locations 5 metres and 30 metres respectively from the converter, with fault resistances of $1m\Omega$ and $500m\Omega$ simulated at each location. This network has the same basic architecture as that introduced within Chapter 3 but will be populated with example microgrid parameter data derived from [6]. This parameter data is presented in table 5.1.

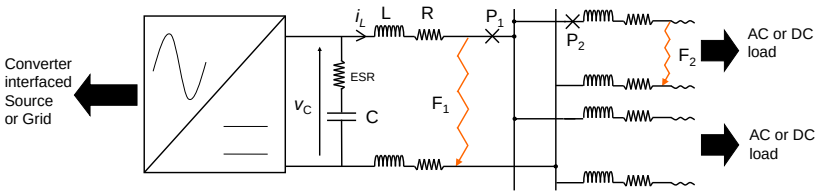

Figure 5.1: Equivalent circuit for the faulted network

Table 5.1: Microgrid Network Parameters

$Voltage$	P_{SOURCE}	P_{LOAD}	R_{CABLE}	L_{CABLE}	C_F	C_{ESR}
$400V$	$320kW$	50kW	$0.641m\Omega/m$	$0.34\mu H/m$	$56mF$	$2m\Omega$

Use of current measurement for protection discrimination

Expressions for the underdamped and overdamped transient fault current were derived in Chapter 3. These were

$$i_L(t) = \frac{v_{CF}(0)}{L\omega_d} e^{-\alpha t} \sin(\omega_d t) + i_L(0) e^{-\alpha t} \left[\cos(\omega_d t) - \frac{\alpha}{\omega_d} \sin(\omega_d t) \right]. \tag{5.1}$$

for the underdamped case and

$$i_L(t) = \frac{v_{CF}(0)}{L(s_1 - s_2)} \left(e^{s_1 t} - e^{s_2 t} \right) + \frac{i_L(0)}{s_1 - s_2} \left[e^{s_2 t}(s_1 + \frac{R}{L}) - e^{s_1 t}(s_2 + \frac{R}{L}) \right] \tag{5.2}$$

for the overdamped case. Initial current is retained in the above as it becomes useful when building upon these equations in later sections.

From equations (5.1) and (5.2), the effect of varying resistance and inductance (for example as a function of fault location or resistance) on the network current response can be determined. Whilst the peak current magnitudes of the capacitive discharge do largely reflect the distance to the fault location, these are much more

sensitive to fault impedance in a microgrid application (as a result of the low impedance interconnecting cables of the compact network). Therefore setting protection based on peak fault current alone will result in poor selectivity for some fault conditions.

This observation is further illustrated in figure 5.2 and table 5.2, which shows the simulated response of the microgrid network to faults at two different locations (as indicated on figure 5.1).

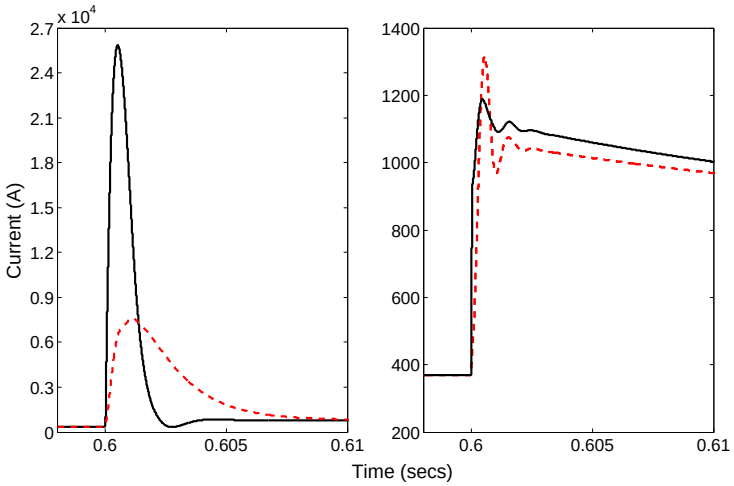

Figure 5.2: Simulated network current response for $1m\Omega$ (left) and $500m\Omega$ (right) faults at F_1 (solid) and F_2 (dotted)

Table 5.2: Summary of key current response characteristics

Fault Type	Peak Current (A)	Time to peak (s)	Steady State current (A)	Settle time (s)
$F_1 - 1m\Omega$	25.9k	500μ	800	0.01
$F_1 - 500m\Omega$	1.19k	450μ	800	0.15
$F_2 - 1m\Omega$	7.60k	1.1m	800	25m
$F_2 - 500m\Omega$	1.32k	500μ	800	0.15

Figure 5.2 and table 5.2 show that for the $1m\Omega$ faults the peak current magnitudes do largely reflect the distance to the fault location, and as such it is possible to discriminate between the fault locations on this basis. However comparing this to the response to the $500m\Omega$ fault, there are two key points to note. First, the peak current for the $F_1 - 500m\Omega$ fault is significantly lower than that for the $F_2 - 1m\Omega$ fault. This makes it very difficult to set protection to operate for the $F_1 - 500m\Omega$ fault whilst remaining insensitive to more distant faults without fast acting protection elsewhere in the network. Second, the current response to faults

$F_1 - 500m\Omega$ and $F_2 - 500m\Omega$ are extremely similar, except for the longer rise time for $F_2 - 500m\Omega$. This emphasises the potential dominance of the fault impedance within the microgrid network and indicates that these fault conditions cannot be discriminated based on current magnitude.

Figure 5.2 and table 5.2 do show that it may be possible to implement instantaneous overcurrent trips for fast protection operation when low impedance faults occur nearby to a given protection relay. However, by waiting until this peak has occurred, very high rated circuit breakers would be required to interrupt the fault current. Therefore it may be desirable for the protection devices to operate before this current peak to optimise protection, as discussed in Chapter 4.

As an alternative to overcurrent, time based current grading [1] would offer a means of discriminating between the fault locations, however the performance of such an approach would not necessarily be optimal. A detailed example of this is shown in section 5.1.2.

Use of voltage measurement for protection discrimination

The voltage across the converter output is determined by the voltage across the filter capacitor. As was shown within Chapter 3, this voltage is proportional to the capacitor size and integral of current and, neglecting initial current, the voltage under fault conditions is described by

$$v_{CF}(t) = \frac{v_{CF}(0)e^{-\alpha t}}{\omega_d}\left[-\omega_d \cos(\omega_d t) - \alpha \sin(\omega_d t)\right] \tag{5.3}$$

for underdamped circuit conditions and

$$v_{CF}(t) = \frac{v_{CF}(0){\omega_0}^2}{(s_1 - s_2)}\left(\frac{e^{s_1 t}}{s_1} - \frac{e^{s_2 t}}{s_2}\right) \tag{5.4}$$

for overdamped circuit conditions.

As before, by considering equations (5.3) and (5.4), the key parameters affecting voltage response can be determined. In line with that observed for the current response, it can be seen that the voltage response of the network is far more sensitive to fault impedance than location. This is particularly apparent in the calculation of the damping terms, α, and the exponential decay terms in (5.3) and (5.4). As such, discrimination of fault location based on this response would be very difficult to achieve.

Figure 5.3 illustrates the simulated voltage response of the microgrid network for the two fault locations previously considered, with table 5.3 summarising some key characteristics. It is shown that for the $1m\Omega$ fault cases a reasonable

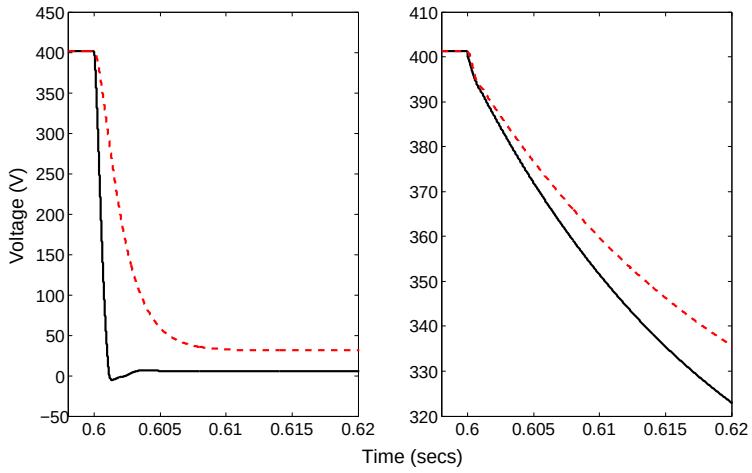

Figure 5.3: Simulated network voltage response for $1m\Omega$ (left) and $500m\Omega$ (right) faults at F_1 (solid) and F_2 (dotted)

Table 5.3: Summary of key voltage response characteristics

Fault Type	Min Voltage (V)	Time to voltage min (s)	Steady state voltage (V)	Settle time (s)
$F_1 - 1m\Omega$	-5.28	1.4m	5.95	10m
$F_1 - 500m\Omega$	278.5	150m	278.5	0.15
$F_2 - 1m\Omega$	31.2	15m	31.2	15m
$F_2 - 500m\Omega$	295.5	130m	295.5	0.13

distinction can be made between the locations F_1 and F_2, with a slower transient decay and higher final voltage for the most distant fault. However as was seen with the current responses, discrimination between the different conditions for higher resistance faults is a significant challenge.

The voltage response does show that there is potential for undervoltage protection to be employed as a backup protection method, particularly for the lower resistance faults. This would operate if the fault, and resulting undervoltage, had not been cleared by primary methods within a suitable period. Again, the application of this would be limited for the higher resistance faults as the sustained generator output may maintain the faulted network voltage above an undervoltage threshold. Voltage controlled overcurrent methods (where overcurrent protection threshold is proportional to voltage magnitude) [7] may have an application in these longer time frame operating cases.

One further challenging aspect in the use of capacitor branch voltage for fault discrimination is the role of capacitor ESR and the potential for significant voltage drop across it during high current flows. Despite being easily accommodated

within the simulation with a voltage measurement across the capacitor branch (as indicated in figure 5.1), the potential for ESR increase with age or vary with temperature [8] would mean it would be difficult to accurately compensate for any voltage dropped across it. This in turn would create even greater difficulty in using voltage for protection coordination within compact networks with limited cable impedance.

Use of rate of change of current measurement for protection discrimination

Expressions for rate of change of current ($\frac{di}{dt}$) can be developed by taking the derivatives of (5.1) and (5.2) as shown within Chapter 3. These were

$$\frac{di_L}{dt} = \frac{v_{CF}(0)e^{-\alpha t}}{L}\left[\cos(\omega_d t) - \frac{\alpha}{\omega_d}\sin(\omega_d t)\right] + i_L(0)e^{-\alpha t}\left[-2\alpha\cos(\omega_d t) + \left(\frac{\alpha^2}{\omega_d} - \omega_d\right)\sin(\omega_d t)\right]. \quad (5.5)$$

for the underdamped case and

$$\frac{di_L}{dt} = \frac{v_{CF}(0)}{L(s_1 - s_2)}\left(s_1 e^{s_1 t} - s_2 e^{s_2 t}\right) + \frac{i_L(0)}{s_1 - s_2}\left[e^{s_2 t}\left(\omega_0^2 + 2\alpha s_2\right) - e^{s_1 t}(\omega_0^2 + 2\alpha s_1)\right]. \quad (5.6)$$

for the overdamped case.

From equations (5.5) and (5.6) it can be derived that while the $\frac{di}{dt}$ fault response is more dependent on fault impedance than location, there is an initial period where both underdamped and overdamped response are approximately equal. This initial $\frac{di}{dt}$ response can be established by analysing (5.5) and (5.6) as time tends to zero. This will be shown in more detail in Chapter 7.

Table 5.4: Summary of key $\frac{di}{dt}$ response characteristics

Fault Type	Peak $\frac{di}{dt}$ (A/s)	Time to peak (s)	Settle time (s)
$F_1 - 1m\Omega$	117.3M	0	18m
$F_1 - 500m\Omega$	117.3M	0	0.2
$F_2 - 1m\Omega$	14.8M	250μ	38m
$F_2 - 500m\Omega$	8.3M	0	0.2

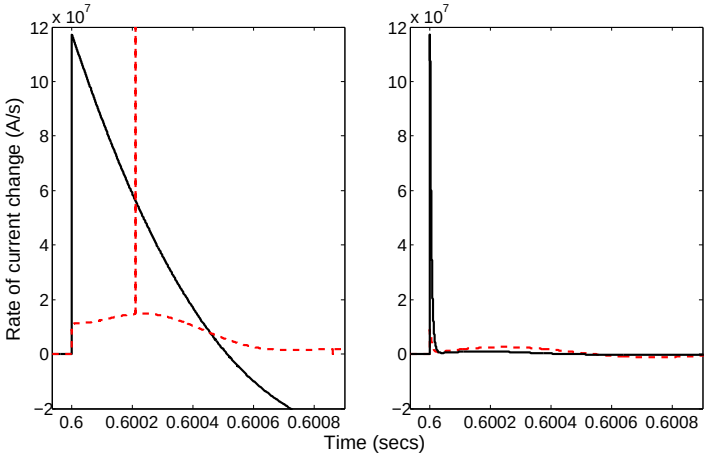

Figure 5.4: Simulated network $\frac{di}{dt}$ response for $1m\Omega$ (left) and $500m\Omega$ (right) faults at F_1 (solid) and F_2 (dotted)

Figure 5.4 and table 5.4 show the simulated $\frac{di}{dt}$ response of the representative microgrid network for the four fault conditions. It is illustrated that there is a similarity initially in the response for both low and high impedance fault conditions at a specific fault location, although for higher impedance faults, the high $\frac{di}{dt}$ decays very rapidly. The response to fault $F_2 - 1m\Omega$ is slightly different from the others in that the peak $\frac{di}{dt}$ does not correspond to the switching time (though note that the vertical spike at around 0.6002s is a numerical error within the simulation). This is due to the initial voltage support across the fault from the stored energy within line inductance, the impact of which is assessed in more detail in Chapter 7.

The similarity in the initial output suggests that some protection selectivity may be possible by monitoring the $\frac{di}{dt}$ response, though the time scale for this is very short. Applications areas where $\frac{di}{dt}$ fault detection techniques are currently utilised for fault detection were introduced in Chapter 2, however in contrast to the response here, these techniques rely on sustained periods of high $\frac{di}{dt}$ [9]. As such, accurate fault detection using this approach would be far more demanding for compact network applications than for other cases considered in the literature but represents an opportunity for the development on a novel protection scheme. Techniques for exploiting this opportunity are described in Chapter 7.

Use of rate of change of voltage measurement for protection discrimination

Expressions for rate of voltage change $\frac{dv}{dt}$ can be developed in two ways; either by taking the derivative of voltage equations (5.3) and (5.4) or by simply dividing current equations (5.1) and (5.2) by the capacitance, i.e.

$$v_{CF}(t) = \int \frac{i_L(t)}{C} dt. \tag{5.7}$$

The derivative of the underdamped voltage (5.3), neglecting initial current, is

$$\frac{dv_{CF}(t)}{dt} = \frac{v_{CF}(0){\omega_0}^2}{\omega_d} e^{-\alpha t} \sin(\omega_d t) \tag{5.8}$$

and the derivative of the overdamped voltage (5.4) is

$$\frac{dv_{CF}}{dt} = \frac{v_{CF}(0){\omega_0}^2}{(s_1 - s_2)} \left(e^{s_1 t} - e^{s_2 t}\right). \tag{5.9}$$

Comparing equations (5.8) and (5.9) to current equations (5.1) and (5.2) respectively, it can be seen that as the $\frac{dv_{CF}}{dt}$ response is equal to the current multiplied by a constant and their general shape is very similar.

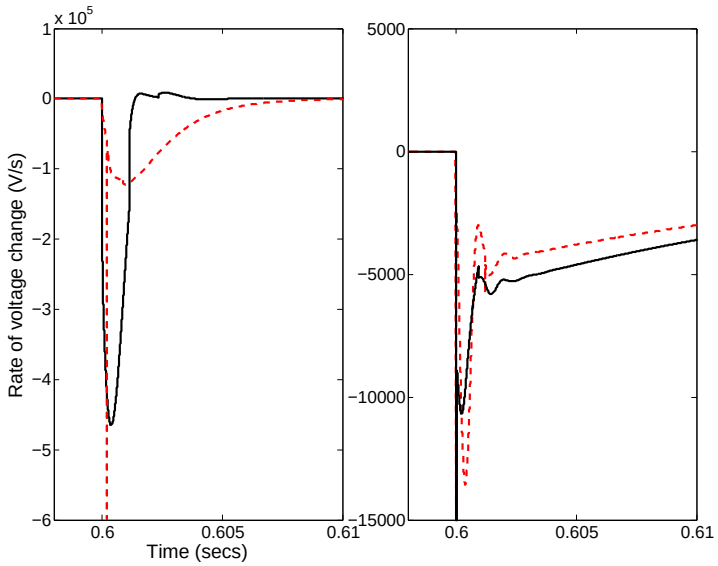

Figure 5.5: Simulated network $\frac{dv}{dt}$ response for $1m\Omega$ (left) and $500m\Omega$ (right) faults at F_1 (solid) and F_2 (dotted)

This finding is reflected within figure 5.5 and table 5.5, which illustrate the simulated $\frac{dv}{dt}$ response of the faulted microgrid network. It is shown that the $\frac{dv}{dt}$ response of the microgrid network is similar, albeit inverted, to the current response (with the exception of some discontinuity errors within the simulation resulting

Table 5.5: Summary of key $\frac{dv}{dt}$ response characteristics

Fault Type	Min $\frac{dv}{dt}$ (V/s)	Time to minimum (s)	Settle time (s)
$F_1 - 1m\Omega$	-465k	390μ	18m
$F_1 - 500m\Omega$	-10.7k	250μ	0.2
$F_2 - 1m\Omega$	-122.9k	1.08m	38m
$F_2 - 500m\Omega$	-13.6k	400μ	0.28

from the derivative measurement), as was expected from the analysis. Therefore it can be concluded that the protection discrimination offered is essentially the same as found with current.

Use of instantaneous impedance measurement for protection discrimination

Impedance is a steady state concept and as such its traditional use within network protection schemes would be ineffective for fault detection over the transient period. Instead this section will consider the instantaneous impedance response of the network, that is the ratio of instantaneous voltage and current. Unfortunately, due to the relatively short cable lengths in the applications considered within this thesis, impedance based protection (instantaneous or otherwise) is unlikely to be suitable to achieve reliable protection selectivity. The purpose of this section is therefore only to derive expressions which help quantify the issues presented when attempting to use an impedance measurement in compact networks. These transient fault impedance expressions do however have wider research value in assessing the use effectiveness of impedance techniques in larger DC power systems.

Expressions for network impedance under fault conditions can be found through the division of the voltage expressions given in equations (5.3) and (5.4) by the equivalent current expressions presented in equations (5.1) and (5.2) (but neglecting initial current) . For the underdamped impedance response this gives

$$Z(t) = \frac{\frac{v_{CF}(0)e^{-\alpha t}}{\omega_d}\left[-\omega_d \cos(\omega_d t) - \alpha \sin(\omega_d t)\right]}{\frac{v_{CF}(0)}{L\omega_d} e^{-\alpha t} \sin(\omega_d t)} \tag{5.10}$$

and cancelling equal terms, this is equal to

$$Z(t) = \frac{-L\omega_d \cos(\omega_d t)}{\sin(\omega_d t)} - L\alpha. \tag{5.11}$$

Further simplification results in

$$Z(t) = -L\omega_d \cot(\omega_d t) - \frac{R}{2}. \tag{5.12}$$

The equivalent overdamped impedance response can be found from

$$Z(t) = \frac{\frac{v_{CF}(0)}{LC(s_1 - s_2)} \left(\frac{e^{s_1 t}}{s_1} - \frac{e^{s_2 t}}{s_2} \right)}{\frac{v_{CF}(0)}{L(s_1 - s_2)} \left(e^{s_1 t} - e^{s_2 t} \right)} \tag{5.13}$$

and cancelling equal terms, this becomes

$$Z(t) = \frac{\left(\frac{e^{s_1 t}}{s_1} - \frac{e^{s_2 t}}{s_2} \right)}{C \left(e^{s_1 t} - e^{s_2 t} \right)}. \tag{5.14}$$

These equations highlight that over the transient period, measured impedance can vary from zero to infinity (however when including initial current this becomes less extreme). For the underdamped system, impedance could not provide protection selectivity because of its oscillatory nature. For overdamped systems, the final response is likely to be dominated by the fault resistance in compact systems. Therefore, it is clear that fault location through impedance measurement cannot be reliably achieved over the transient period and therefore does not meet the required criteria for the detection of faults.

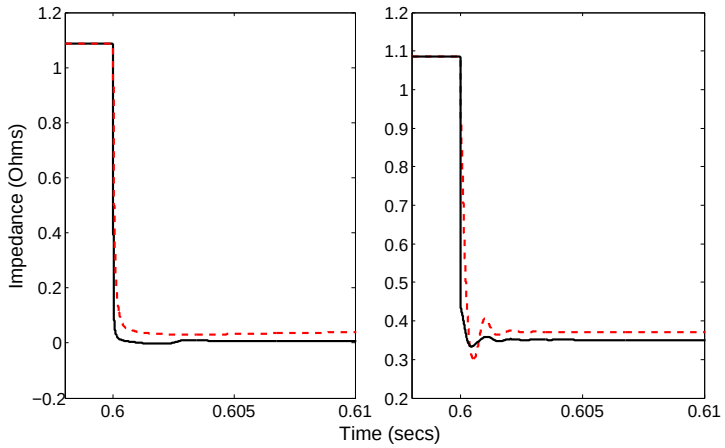

Figure 5.6: Simulated network impedance response for $1m\Omega$ (left) and $500m\Omega$ (right) faults at F_1 (solid) and F_2 (dotted)

The simulated impedance response shown in figure 5.6 reinforces the conclusions from the above analysis, as does table 5.6. The network impedance is seen

Table 5.6: Summary of key impedance response characteristics

Fault Type	Min Impedance (Ω)	Time to minimum (s)	Steady state Impedance (Ω)	Settle time (s)
$F_1 - 1m\Omega$	-1.2m	2.3m	7.4m	6m
$F_1 - 500m\Omega$	334m	500μ	348m	0.11
$F_2 - 1m\Omega$	30.5m	3.2m	39m	15m
$F_2 - 500m\Omega$	301m	580μ	369m	0.15

to change rapidly over the transient period, and so over this period the position of a fault along the line could not be determined as accurately as desired. Non-synchronisation of voltage and current measurements (a subject analysed in section 5.2) may also lead to significant errors in the impedance calculation. Following the transient period, the steady state characteristic tends towards the fault impedance (or the parallel combination of fault and load impedance) and so does not offer discrimination between the two fault locations.

Discussion of findings

Given that little advantage can be seen from considering any alternative non-unit measurements other than current (with the possible exception of $\frac{di}{dt}$ measurements), the following section will demonstrate the challenges in implementing overcurrent techniques to provide effective protection to the network illustrated in figure 5.7, looking specifically at the network's current and i^2t responses to a range of fault conditions.

5.1.2 Illustration of detection challenges based on an all overcurrent protection scheme

The work presented within this section focuses more on the coordination of protection device operation within a VSC interfaced network rather than purely operating to mitigate the impact of the network natural response, as has been considered up to this point. However, as will be highlighted in the following sections, the natural response still has a significant impact on device coordination and must be considered within the protection scheme design.

To highlight this aspect, the section first quantifies the protection system operating requirements based on relevant network responses, which have been derived from network simulations, before a scheme is designed, based on the use of overcurrent techniques, to operate towards this operating requirement.

Quantification of DC protection system operating requirements

Cuzner et al. [4] outlines the key design criteria for any protection system and these relate to the operability and cost of a protection system. From the criteria presented, the performance of the protection system is assessed on its ability to provide continuity of supply to loads where other parts of the network are experiencing faults.

The expanded DC microgrid network used as the basis for comparison within this section is presented within figure 5.7, with the network parameters (similar to those presented within table 5.1) being presented in table 5.7. This network has been derived from example architectures within the literature [2, 6] and is supplied by a VSC. Only a single source has been considered within figure 5.7 to simplify analysis and to aid illustration however, it is anticipated that findings will be applicable to networks with multiple sources. To ensure minimum disruption to the network presented within figure 5.7 in the event of a fault, protection devices P_1 to P_7 must operate in a coordinated way, such that only the device immediately upstream from the fault operates.

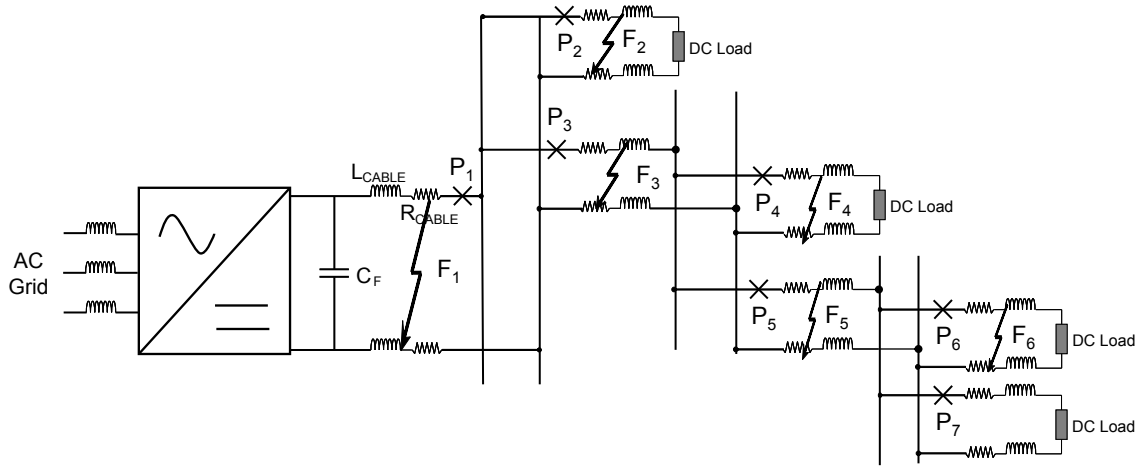

Figure 5.7: Network diagram

Table 5.7: Network Parameters

Voltage (V)	P_{SOURCE} (kW)	P_{LOAD} (kW)	R_{CABLE}(mΩ/m)	L_{CABLE}(μH/m)	C_F (mF)	C_{ESR}($m\Omega$)
400	320	20	0.641	0.65	56	2

However there are a number of factors which influence the time-frame within which the network protection has to coordinate its devices operation. Many of these factors centre around the use of a VSC as the main network supply. A number of these aspects have been covered in previous chapters but are worth revisiting here to emphasise the impact they have on operating requirements.

Previous work has highlighted that the fast discharge of capacitors used as filters on the DC terminals of the VSC can damage both the capacitors themselves and any other sensitive components in the fault path [2]. Considerable short term electromagnetic forces on conductors can also be induced [10], creating risks of physical damage to mountings or insulation. Furthermore, previous chapters have illustrated the potential for voltage reversal if DC side faults are not cleared within an adequate time frame. The voltage reversal can cause significant currents to flow through converter freewheeling diodes, causing damage to these devices [11].

The fault current withstand of VSCs is low compared to more robust thyristor based converter topologies [2,6], therefore current must be limited or interrupted much more quickly to prevent damage to internal components when supplying fault current.

The typical topology of VSC devices is such if the back-biasing DC voltage is lost after the occurrence of a fault, the antiparallel diodes across the switching devices will begin to conduct, meaning the converter is unable to block the flow of current to the fault [12]. For these converter types, it necessary for network protection to act quickly to prevent damaging currents from flowing through the diodes, within 2ms in some cases [6].

Alternative VSC topologies contain their own internal protection functionality, which enables the interruption of current flow through the converter. An example topology capable of this is provided within [2] (and is illustrated in Chapter 2), where anti-parallel diodes are replaced with emitter turn-off devices. Internal converter protection can be sensitive to overcurrent, overvoltage or undervoltage [13, 14]; however as the only source of fault current within figure 5.7 it is essential that the converter protection coordinates with protection devices P_1 to P_7 to ensure that only the appropriate protection device operates prior to converter protection operation.

Operational standards do exist for AC and HVDC systems which describe the requirements for converter connection in the event of network fault conditions. For example, [14] stipulates that in the event of a network undervoltage, converters are required to remain connected for a minimum of 140ms to avoid sympathetic tripping [15] for faults elsewhere in the network. However it is difficult to see how these requirements apply to less robust converter types, where connection for this period of time may result in the flow of damaging current magnitudes flowing through the converter.

Whilst converter undervoltage protection is typically not as important as overcurrent for preventing device damage, for a DC system the undervoltage is a

consequence of filter capacitor discharge, which in itself may cause problems. An undervoltage will be followed by an overcurrent condition on the AC side of the converter, as more current is drawn to attempt to recover the DC voltage. The DC side undervoltage can also be linked to the operation of AC side protection, which may monitor both DC voltage and current to determine its operation [13].

Given the DC voltage is linked to a number of aspects of the network and converter protection, it is useful to consider the voltage response when deriving protection system operating criteria. Considering the DC voltage response has the added advantage of being least dependent on AC network conditions and configuration, and hence provides a DC side solution which could be deployed within multiple applications. For these reasons, this section assesses the potential for current fault detection methods to coordinate with a converter undervoltage threshold for the network described within figure 5.7.

To derive a fixed operating point, an undervoltage threshold of 200V (half the nominal system voltage) has been selected. It should however be noted that the observations in the following sections are relevant for various voltage thresholds. Table 5.8 highlights the time at which this voltage threshold is reached following the occurrence of a 1mΩ fault at the six fault locations indicated in figure 5.7. These voltage responses have been determined from the simulation of figure 5.7.

Table 5.8: Required tripping times for undervoltage threshold of 200V for a $1m\Omega$ fault at various fault locations

Fault Location	Time to undervoltage threshold after fault (ms)
F_1	0.9
F_2	2.2
F_3	2.2
F_4	3.7
F_5	3.7
F_6	5.3

From table 5.8 it is clear that, for the range of low impedance faults considered, the rapid loss of voltage at the converter terminals creates particularly challenging times for the operation of protection if it is to act to prevent the undervoltage occurring. The times identified are much shorter than required for AC converter connection [14], although they are in fact similar in magnitude to the requirements derived in [6] for prevention of overcurrent through the converter diodes, highlighting the unique challenges for the type of network considered.

The following sections will demonstrate the challenges in achieving discriminatory protection system operation within the time frames outlined using of

non-unit methods.

Coordination of Protection Devices

To assess the capabilities of an overcurrent protection scheme to deliver the required levels of performance, this section looks at the coordination of pairs of upstream and parallel downstream devices, relating them to the previously derived operating requirements, and highlighting how these operating requirements differ depending on the connection of downstream devices. The merits of specific current-time graded protection schemes are not analysed, as is perhaps more standard, as the author believes the issues are more clearly demonstrated with a study of network response rather than detailed device characteristics. However, [16] has conducted research in this area, work which discusses the potential issues in coordinating current-time characteristics for networks with large capacitive sources. It is worth noting however that a relay operated on the extremely inverse current-time characteristic (designed for fast operating conditions) would behave in a similar manner to a device operated on i^2t [1].

Whilst it is standard practice to coordinate protection device operation beginning with the furthest downstream device, the section instead first assesses the coordination of upstream devices because of the challenges associated with operating close to the capacitive source and the impact this has on downstream protection operation. These challenges are illustrated in the following sections.

Coordination of P_1 with P_2 and P_3 To achieve good performance when coordinating P_1 with P_2 and P_3, the protection system must ensure that: any faults on line P_1 are quickly discriminated and cleared, P_1 remains stable for faults on downstream lines but provides backup in the event that P_2 or P_3 fail to operate.

As will be shown in later figures, the detection and discrimination of a low impedance fault at F_1 is reasonably straight forward given the excessive overcurrent produced compared to more distant faults. Therefore the objective for the protection system for close up faults is to operate sufficiently quickly to prevent damage at the point of fault and to components supplying fault current. Instead, the key coordination challenge in setting the overcurrent threshold at P_1 relates to the network fault response for higher impedance faults. To illustrate why this is the case, consider the plot shown in figure 5.8.

Figure 5.8 illustrates the response of the network to $1m\Omega$ and $500m\Omega$ faults at F_1, values which have been chosen to be representative of low and high impedance

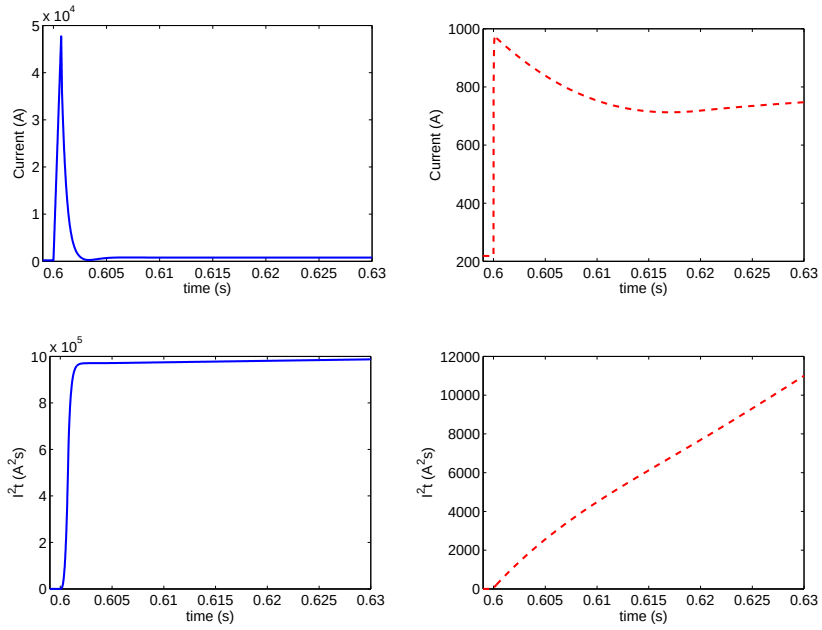

Figure 5.8: Simulated current (top) and i^2t (bottom) response for $1m\Omega$ (left) and $500m\Omega$ (right) faults at F_1

fault conditions. It can be seen from figure 5.8 that for the two fault types, the peak fault current is vastly different, emphasising the dominance of the fault impedance relative to the total fault path impedance. However in both cases the steady state output of the converter tends to the same level as the converter attempts to maintain output voltage to nominal levels. The magnitude of this steady state current will depend on either AC side fault level or converter rating (if the converter is capable of limiting current for DC faults). For the higher impedance fault conditions the network voltage will not decay to the same extent (and potentially not reducing below the defined voltage threshold), therefore the operating requirement will relate to the converter's ability to supply this fault current without damage being caused.

This causes a problem in setting the overcurrent threshold for P_1. For example, if an initial threshold is set for P_1 as the i^2t at the undervoltage threshold (set in the previous section as $0.9ms$, at which point i^2t equals $7.5 \times 10^5 A^2s$), expanding the i^2t plot for the 500mΩ fault within figure 5.8 will show that it takes $1.18s$ after fault inception to reach the same A^2s value. This would lead to the converter supplying fault current for longer than desired, and hence there is a requirement to lower this operating threshold from this initial level. However to maintain coordination with downstream devices, there is a limited degree to which this can be achieved. To assess the scope for the reduction, consider the current and

i^2t for 1mΩ fault at F_2 and F_3 shown in figure 5.9. Note that due to faults F_2 and F_3 being the same distance from the converter, and suitably low impedance, the responses to either fault is equivalent.

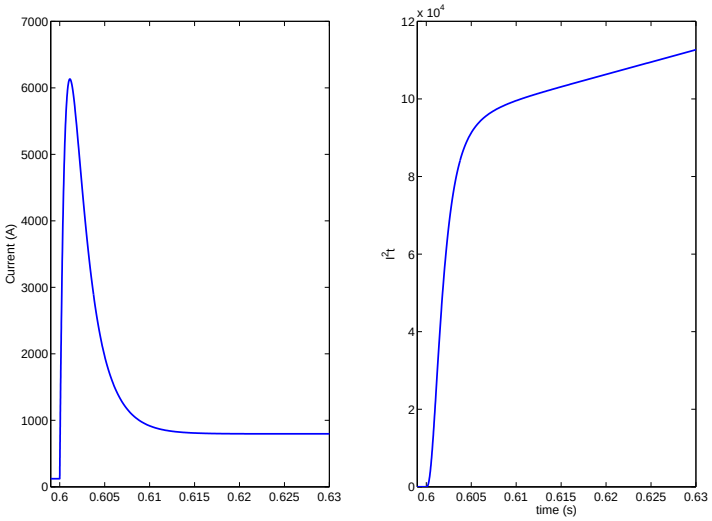

Figure 5.9: Simulated current (left) and i^2t (right) response for 1mΩ fault at F_2 and F_3

From a comparison of figure 5.9 and table 5.8 it can be determined that the undervoltage threshold crossing at $2.2ms$ corresponds to an i^2t value of $6 \times 10^4 A^2s$. Relating this value to the previous fault case, $6 \times 10^4 A^2s$ is reached $0.16s$ following the inception of fault F_1 - 500mΩ. Whilst this is perhaps longer than is desirable, it is reasonable to assume that the converter could supply current for this shorter time given the slower decay of DC side voltage. Therefore one protection setting option would be to reduce the threshold at P_1 to this level. However to maintain a suitable time margin between the operating points of upstream and downstream protection (to enable device coordination), it is also necessary to reduce the thresholds of P_2 and P_3. This however brings its own problems given the need for P_3 to coordinate with further downstream devices and hence reduces the scope for threshold reduction. The necessity to reduce thresholds to achieve acceptable operating times does indicate that options to ride through the initial capacitive discharge, as suggested in [4, 16], are limited.

To continue this example, consider the potential for circuit breaker coordination when reducing the threshold setting of P_2 and P_3 to $3 \times 10^4 A^2s$ (half the original setting). Table 5.9 summarises the times at which the thresholds will be reached for the initial and revised protection settings.

Table 5.9 highlights that whilst the initial protection settings were challenging to meet because of the short time frame, a sufficient time margin existed between

Table 5.9: Summary of operating threshold times of P_1, P_2 and P_3 for a fault at F_2 or F_3

Fault Location	t_{P_1} (initial)	$t_{P_{2,3}}$ (initial)	t_{P_1} (revised)	$t_{P_{2,3}}$ (revised)	$\Delta t_{P_1-P_{2,3}}$ (initial)	$\Delta t_{P_1-P_{2,3}}$ (revised)
$F_{2,3}$	1.02s	2.2ms	2.2ms	1.2ms	1.02s	1ms

upstream and downstream protection to ensure coordinated protection operation. However given the requirement to reduce the upstream i^2t threshold to achieve reasonable operating times under impedance fault conditions, the time margin between device operations has now reduced to a level such that protection coordination is extremely difficult to achieve. This is in part due to the typical delay time between detection and circuit breaker operation, as discussed in Chapter 4.

In order to increase the time margin between different device operations, there may be some scope for reduction in the threshold of P_2, albeit limited, given that it does not need to coordinate with further downstream devices. This is not the case for P_3, so further reduction in its threshold is not necessarily an option. The following sections therefore investigate the response of downstream protection to quantify the impact of upstream device coordination issues.

Coordination of P_3 with P_4 and P_5 The potential for P_3 threshold reduction can be examined from analysis of downstream faults $F_{4,5}$. The initial threshold for $P_{4,5}$, derived from the undervoltage cut off, is $4.1 \times 10^4 A^2 s$. As this is greater than the revised threshold for P_3 in the previous section, there is a need to reduce this level. To maintain consistency with the previous section, the threshold for $P_{4,5}$ has been reduced to $1.5 \times 10^4 A^2 s$ (half that of P_3). A summary of the impact of this on required operating time and time margins is shown in table 5.10.

Table 5.10: Summary of operating threshold times of P_3, P_4 and P_5 for a fault at F_4 or F_5

Fault Location	t_{P_3} (initial)	$t_{P_{4,5}}$ (initial)	t_{P_3} (revised)	$t_{P_{4,5}}$ (revised)	$\Delta t_{P_3-P_{4,5}}$ (initial)	$\Delta t_{P_3-P_{4,5}}$ (revised)
$F_{4,5}$	9.2ms	3.7ms	2.5ms	1.5ms	4.1ms	1ms

Table 5.10 highlights that the difference in required operating time for the initial undervoltage thresholds is already very tight and the impact of the reduced operating threshold compounds this problem, making the setting of devices extremely difficult. As with the previous case, given that the required operating time is already small, there is little scope for accelerating protection operation through threshold reduction. However for completeness, and to quantify challenges further downstream protection, the following section assesses the options

for coordination of P_5 with P_6 and P_7.

Coordination of P_5 with P_6 and P_7 In a similar manner to the previous section, the potential for device coordination is assessed through comparison of the initial and revised overcurrent thresholds. The initial i^2t threshold for P_6 or P_7 was $3.13 \times 10^4 A^2 s$, which is again greater than revised upstream levels, and so in line with previous sections the $P_{6,7}$ threshold has been reduced to $0.75 \times 10^4 A^2 s$ (half of P_5). A summary of initial and revised operating times for a fault at F_6 is presented in table 5.11.

Table 5.11: Summary of operating threshold times of P_5 and P_6 for a fault at F_6

Fault Location	t_{P_5} (initial)	t_{P_6} (initial)	t_{P_5} (revised)	t_{P_6} (revised)	$\Delta t_{P_5-P_6}$ (initial)	$\Delta t_{P_5-P_6}$ (revised)
$F_{4,5}$	9.4ms	5.3ms	2.3ms	1.4ms	4.1ms	0.9ms

Table 5.11 shows a similar trend to the previous section in terms of both required operating time and time difference between upstream and downstream devices. Therefore the device coordination challenges are similar to those reported previously.

5.1.3 Overall discussion of results

The results presented in the previous sections have demonstrated the challenges which exist in the coordination of protection in compact DC power systems using overcurrent based protection schemes.

In each scenario it was illustrated that the time margin between upstream and downstream protection operation was prohibitively small, creating a risk of upstream protection operation for downstream faults. This was in part due to the tight operating requirements from the network voltage response. However the need for reduction in the threshold of P_1 (to achieve a reasonable operating time under impedance fault conditions) has a cascading effect on the downstream device settings and hence reduces operating margins. From this, it is worth noting that in tables 5.10 and 5.11 the time difference between the initial upstream and the revised downstream threshold is twice that of the difference between the two initial settings. This suggests that if the constraint of lowering the upstream threshold is removed, a greater opportunity for device coordination exists.

It is also worth considering how the difference in required operating time compares to that of the physical operating speeds of circuit breakers. Chapter 4 highlights that the requirement for fast acting protection can limit the range of

protection devices which can be employed in DC microgrid networks. For example, the operating time of DC electro-mechanical circuit breakers (EMCB) was identified to be around $3ms$ [17], which exceeds the time difference in the scenarios described in the previous section, meaning coordination is not necessarily possible using the methods presented.

Solid state (SSCB) and hybrid circuit breaker (HCB) technologies offer a potential alternative to EMCBs. However there are greater limitations on the operating voltage and current levels of these devices than for EMCBs, as has been discussed previously.

It must also be appreciated that DC current breaking cannot be achieved instantaneously and there is a finite time when current is driven to zero (refer to chapters 3 and 4 for analysis on this subject). During this period current will continue to flow through upstream devices and this could, depending on network conditions, cause an upstream device to operate before the fault is fully cleared.

Acknowledging these shortfalls, it can be concluded that the non-unit methods analysed are sub-optimal for the derived operating requirements. Within future DC networks it is likely that a higher level of fault discrimination will be desirable, particularly if DC is to be proven a viable alternative to AC distribution. For these future networks, it has been demonstrated that for this to be achieved, non-unit protection cannot be relied upon and so more robust protection approaches are required. The following section investigates the potential and challenges for unit protection to provide this required protection performance.

5.2 Unit protection implementation within compact DC networks

The basic principles of unit protection and the primary challenges in its implementation within compact networks were introduced in Chapter 2. These challenges included the achievement of fast operating times and the synchronisation of measurement devices. To investigate the effectiveness of unit protection in achieving rapid fault detection and reliable selectivity for compact DC networks, this section will analyse the response of a current differential scheme for a typical section of DC network. This analysis will then be used to quantify the challenges in implementing current differential protection in a way to enable it to achieve the desired performance.

To begin with the simplest setup, the initial case studies contain only a single protection zone. This zone encompasses the area between a converter output and

busbar. The scheme should trip for faults inside this protected zone and remain immune to any external fault. In order to provide greater clarity in the findings, analysis is presented for a single load connected to the supply converter. Passive and active load types are considered in this analysis to illustrate the change in system response.

5.2.1 Differential current behaviour and measurement requirements for different loading conditions

This section will first define expressions for the two measured currents in the differential scheme and their difference under various loading and fault conditions. This analysis enables the definition of expected protection system operation times under ideal measurement conditions and the assessment of the effect of measurement synchronisation error for the different load connections. Whilst built on the circuit analysis principles described previously, equations have been derived exclusively for this analysis, with no similar examples being found within the literature.

Network response for ideal measurement conditions

Internal zone fault response with passive load connected To illustrate the operation of the current differential scheme with the connection of a passive load, consider the network shown in figure 5.10.

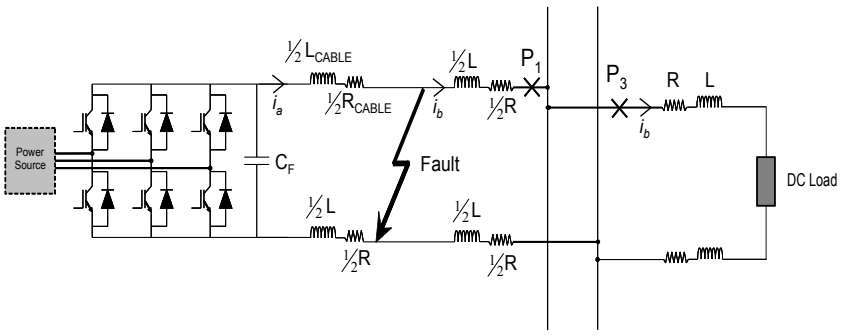

Figure 5.10: Current differential scheme with passive load connected

The current differential scheme detects faults on the generator to busbar line by looking at the difference between i_a and i_b, i.e. $\Delta i = i_a - i_b$. To analytically quantify the response of the current differential scheme to a fault within the protection zone, i_a and i_b must be defined. Figure 5.10 represents a section of a larger network, such as that considered in the previous section, and illustrates that i_a flows around an RLC circuit, meaning its response will be second order.

i_b flows around a section of circuit containing only resistors and inductors and its response will be first order. For these two currents to be clearly defined, it is assumed that no current from i_a flows into i_b and vice versa. As was the case in with analysis in section 5.1, this gives an accurate response for short circuit faults and shows more approximate behaviour when looking at impedance faults.

As section 5.1 and previous chapters discuss, the form of the expression will depend on the damping conditions in the circuit. For underdamped circuit conditions i_a is

$$i_a(t) = \frac{v_{CF}(0)}{L_a\omega_{da}} e^{-\alpha_a t}\sin(\omega_{da}t) + i_L(0)e^{-\alpha_a t}\left[\cos(\omega_{da}t) - \frac{\alpha_a}{\omega_{da}}\sin(\omega_{da}t)\right]. \quad (5.15)$$

Here i_b will be driven only by the stored energy in the inductance. Its first order response is therefore equal to

$$i_b(t) = i_L(0)e^{-\frac{R_b}{L_b}t}. \quad (5.16)$$

As stated, the differential current sum is equal to,

$$\Delta i = i_a - i_b \quad (5.17)$$

and when substituting for i_a and i_b with (5.15) and (5.16) respectively, it becomes

$$\Delta i = \frac{v_{CF}(0)}{L_a\omega_{da}} e^{-\alpha_a t}\sin(\omega_{da}t) + i_L(0)e^{-\alpha_a t}\left[\cos(\omega_{da}t) - \frac{\alpha_a}{\omega_{da}}\sin(\omega_{da}t)\right] - i_L(0)e^{-\frac{R_b}{L_b}t}. \quad (5.18)$$

Collecting like terms, the above can be further reduced to

$$\Delta i = \frac{v_{CF}(0)}{L_a\omega_{da}} e^{-\alpha_a t}\sin(\omega_{da}t) + i_L(0)\left[e^{-\alpha_a t}\left(\cos(\omega_{da}t) - \frac{\alpha_a}{\omega_{da}}\sin(\omega_{da}t)\right) - e^{-\frac{R_b}{L_b}t}\right]. \quad (5.19)$$

Where overdamped circuit conditions exist i_a is

$$i_a(t) = \frac{v_{CF}(0)}{L(s_1 - s_2)}\left(e^{s_1 t} - e^{s_2 t}\right) + \frac{i(0)}{s_1 - s_2}\left[e^{s_2 t}(s_1 + \frac{R}{L}) - e^{s_1 t}(s_2 + \frac{R}{L})\right] \quad (5.20)$$

The form of the expression for i_b remains the same and so substituting for the

overdamped case, the difference expression becomes

$$\Delta i = \frac{v_{CF}(0)}{L(s_1 - s_2)}\left(e^{s_1 t} - e^{s_2 t}\right) + \frac{i(0)}{s_1 - s_2}\left[e^{s_2 t}(s_1 + \frac{R}{L}) - e^{s_1 t}(s_2 + \frac{R}{L})\right] - i_L(0)e^{-\frac{R_b}{L_b}t} \tag{5.21}$$

and again collecting like terms, this gives

$$\Delta i = \frac{v_{CF}(0)}{L(s_1 - s_2)}\left(e^{s_1 t} - e^{s_2 t}\right) + i(0)\left[\frac{e^{s_2 t}(s_1 + \frac{R}{L}) - e^{s_1 t}(s_2 + \frac{R}{L})}{s_1 - s_2} - e^{-\frac{R_b}{L_b}t}\right]. \tag{5.22}$$

In equations (5.19) and (5.22) the dominant term will come from the initial voltage across the capacitor (see Chapter 3). However when assessing differential current, the initial current may have more impact as the energy stored in the line inductance initially maintains current flow to the load. This will effect the time which the differential current exceeds the threshold level. The extent to which this current is maintained is dependent on the ratio of R_b and L_b, as the exponential term in (5.16) shows.

As (5.19) and (5.22) show the expected differential current behaviour, they facilitate the accurate evaluation and assessment of associated protection schemes. For example, (5.19) and (5.22) could potentially be used when establishing the expected protection operating time for a range of current difference thresholds (also known as bias currents).

Internal zone fault response with converter interfaced load connected
The response of the current differential scheme will change with the connection of a converter interfaced (also known as active) load type due to the contribution of the load capacitor into the fault. This can be seen from the network diagram in figure 5.11.

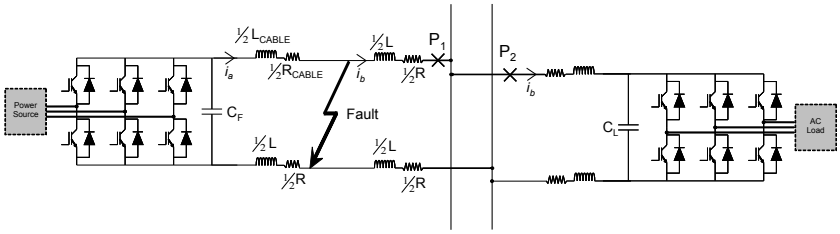

Figure 5.11: Current differential scheme with active load connected

First, assuming underdamped conditions for both i_a and i_b, Δi is given by

$$\Delta i = \frac{v_{CF}(0)}{L_a\omega_{da}} e^{-\alpha_a t}\sin(\omega_{da}t) + i_L(0)e^{-\alpha_a t}\left[\cos(\omega_{da}t) - \frac{\alpha_a}{\omega_{da}}\sin(\omega_{da}t)\right] - \left(-\frac{v_{CF}(0)}{L_b\omega_{db}} e^{-\alpha_b t}\sin(\omega_{db}t) + i_L(0)e^{-\alpha_b t}\left[\cos(\omega_{db}t) - \frac{\alpha_b}{\omega_{db}}\sin(\omega_{db}t)\right]\right) \quad (5.23)$$

and collecting like terms, this becomes

$$\Delta i = v_{CF}(0)\left[\frac{1}{L_a\omega_{da}} e^{-\alpha_a t}\sin(\omega_{da}t) + \frac{1}{L_b\omega_{db}} e^{-\alpha_b t}\sin(\omega_{db}t)\right] + i_L(0)\left[e^{-\alpha_a t}\left(\cos(\omega_{da}t) - \frac{\alpha_a}{\omega_{da}}\sin(\omega_{da}t)\right) - e^{-\alpha_b t}\left(\cos(\omega_{db}t) - \frac{\alpha_b}{\omega_{db}}\sin(\omega_{db}t)\right)\right]. \quad (5.24)$$

Equation (5.24) shows that the two initial voltage terms sum to create a larger difference in current between the two measurement points. This is due to the opposite polarity of the currents flowing into the fault.

As the two RLC circuits have a different natural response, the discharge current magnitude and frequency is different for the two circuits. Therefore the damping conditions for the two circuits are not necessarily the same. To illustrate this, consider a scenario where a fault is of low impedance, however the network characteristics are such that i_a is overdamped. As the load capacitance is smaller (and ω_0 is likely higher), the load side RLC circuit could be underdamped. In these conditions the current differential response is made up of a mixture of overdamped and underdamped expressions. Differential current in this case is

$$\Delta i = \frac{v_{CF}(0)}{L_a(s_{1a} - s_{2a})}\left(e^{s_{1a}t} - e^{s_{2a}t}\right) + \frac{i(0)}{s_{1a} - s_{2a}}\left[e^{s_{2a}t}(s_{1a} + \frac{R}{L}) - e^{s_{1a}t}(s_{2a} + \frac{R}{L})\right] - \left(-\frac{v_{CF}(0)}{L_b\omega_{db}} e^{-\alpha_b t}\sin(\omega_{db}t) + i_L(0)e^{-\alpha_b t}\left[\cos(\omega_{db}t) - \frac{\alpha_b}{\omega_{db}}\sin(\omega_{db}t)\right]\right) \quad (5.25)$$

and collecting like terms this is

$$\Delta i = v_{CF}(0)\left[\frac{e^{s_{1a}t}-e^{s_{2a}t}}{L_a(s_{1a}-s_{2a})}+\frac{e^{-\alpha_b t}}{L_b\omega_{db}}\sin(\omega_{db}t)\right]$$
$$+i_L(0)\left[\frac{\left(e^{s_{2a}t}(s_{1a}+\frac{R_a}{L_a})-e^{s_{1a}t}(s_{2a}+\frac{R}{L})\right)}{s_{1a}-s_{2a}}-e^{-\alpha_b t}\left(\cos(\omega_{db}t)-\frac{\alpha_b}{\omega_{db}}\sin(\omega_{db}t)\right)\right] \tag{5.26}$$

For the case where both i_a and i_b are overdamped, the resultant current differential expression is

$$\Delta i = \frac{v_{CF}(0)}{L_a(s_{1a}-s_{2a})}\left(e^{s_{1a}t}-e^{s_{2a}t}\right)+\frac{i(0)}{s_{1a}-s_{2a}}\left[e^{s_{2a}t}(s_{1a}+\frac{R_a}{L_a})-e^{s_{1a}t}(s_{2a}+\frac{R_a}{L_a})\right]$$
$$-\left[-\frac{v_{CF}(0)}{L_b(s_{1b}-s_{2b})}\left(e^{s_{1b}t}-e^{s_{2b}t}\right)+\frac{i(0)}{s_{1b}-s_{2b}}\left[e^{s_{2b}t}(s_{1b}+\frac{R_b}{L_b})-e^{s_{1b}t}(s_{2b}+\frac{R_b}{L_b})\right]\right] \tag{5.27}$$

and again collecting like terms this gives

$$\Delta i = v_{CF}(0)\left[\frac{e^{s_{1a}t}-e^{s_{2a}t}}{L_a(s_{1a}-s_{2a})}+\frac{e^{s_{1b}t}-e^{s_{2b}t}}{L_b(s_{1b}-s_{2b})}\right]$$
$$+i_L(0)\left[\frac{\left(e^{s_{2a}t}(s_{1a}+\frac{R_a}{L_a})-e^{s_{1a}t}(s_{2a}+\frac{R_b}{L_b})\right)}{s_{1a}-s_{2a}}-\frac{\left(e^{s_{2b}t}(s_{1b}+\frac{R_b}{L_b})-e^{s_{1b}t}(s_{2b}+\frac{R_b}{L_b})\right)}{s_{1b}-s_{2b}}\right]. \tag{5.28}$$

Comparing the respective active and passive load responses, it can be seen that the current difference will increase with an active load connected compared to a passive load, due to the initial source of fault current flowing into the protected zone (provided current is measured directionally as opposed to purely on magnitude). This will lead to any operating threshold being met more quickly and hence faster operation of protection. As with the passive load, equations (5.24), (5.26) and (5.28) facilitate the evaluation of current differential schemes for internal faults with active load connection.

External fault response

For any fault external to the protected current differential zone $i_a(t) = i_b(t)$ (with the exception of capacitive current flow which has been neglected from the analysis as described in Chapter 3). Under ideal measurement conditions

the differential sum would not be influenced by loading conditions will be equal to zero and so would not cause the current differential scheme to mal-operate. Non-ideal conditions are assessed in the following section.

5.2.2 Inherent challenges in the implementation of fast acting unit protection schemes

There are two main challenges for the implementation of unit protection within the highly transient environment described in the previous sections. The first is, can currents be compared and fault location determined within the required time frame? The second is, can the current measurements at different points in the network be accurately synchronised to ensure correct protection system operation? These issues are assessed in the following sections.

Assessment of differential current scheme response within target operating time

The previous section analytically defines the differential current response under various operating conditions. This allows for the derivation of the time at which a certain differential current threshold would be reached, and hence informs on the potential detection time of the differential scheme.

Combining this derived time parameter, which will be called $t_{\Delta i}$, with the peak current and circuit breaker operating times defined in Chapter 4, the potential for the differential scheme to achieve the required operating time can be assessed.

Analysing the protection operation in further depth, there are two discrete stages to the differential scheme detecting a fault. The first is the time taken for the currents to exceed the differential current threshold (the magnitude of which is set by the protection system designer) and the second is the time taken for a processing device to accept measured currents, calculate the differential current magnitude and output a trip signal. The required performance of the second stage can therefore be defined by substituting these two stages for t_L in the operating time equation in Chapter 4, (4.24). The allowed differential device calculation time is therefore equal to

$$t_{diffcalc} < t_{req.op} - t_{CB} - t_{\Delta i}. \tag{5.29}$$

The output of (5.29) is the time allowed for current differential relay/decision making element stage of the protection operation process. This time enables

the selection of an appropriate processing technology to allow for the protection criteria to be met.

This can be highlighted with an example calculation. Consider the faulted case in section 5.1 where a short circuit occurs half way between the converter terminals and the busbar (distance of 15m), with a passive load connected as in section 5.2.1. The differential current response in this case is described by (5.19). To determine $t_{\Delta i}$, the Δi operating threshold current must first be defined. This bias characteristic is often based on a small percentage of current output [18], and as the difference between peak fault and steady state current is so great, it is likely that a similar method would be implemented. However for clarity, this example will consider a constant current bias of 100A, i.e. once $\Delta i \geq 100A$ then the protection should operate.

For the scenario described, the time at which the differential current equals 100A can be calculated to be $0.9\mu s$ (from (5.19)). If this time is substituted into (5.29) along with the target maximum operating time (say $500\mu s$ in this case, which is the time to peak within table 5.2) and an appropriate solid state circuit breaker operating time ($10\mu s$ is an appropriate time as shown in Chapter 4), (5.29) becomes

$$t_{diffcalc} < 500\mu - 10\mu - 0.9\mu. \tag{5.30}$$

The allowed processing time of the differential device would therefore be

$$t_{diffcalc} < 489\mu s. \tag{5.31}$$

Analysis of example digital processing devices [19, 20] suggests that the total conversion and processing time ($< 10\mu s$ as shown in the following chapter) is far less than this derived parameter. Therefore a current differential approach may be a viable method of implementation for high speed, coordinated protection system operation. There is also potential for detection much earlier than the current peak which has the added advantage of reducing the circuit breaker operating current, reducing the stress on the breaker itself and post fault clearance transients, as discussed in Chapter 4. As previously stated, SSCBs are best equipped to take advantage of this early operation, due to their significantly shorter operating time compared to hybrid and electromechanical circuit breakers.

Challenges in the implementation of unit systems when operating under high rate of change fault conditions

For a current differential scheme to operate completely accurately, time synchronised current measurements are required [18], otherwise errors can occur in the differential sum. However due to the high $\frac{di}{dt}$ over the transient period in compact DC systems, this can be challenging to achieve.

There are a number of sources of this poor time synchronisation. These include timing errors between communicating devices (even where devices are synchronised through GPS time stamping) [21] and non-synchronous current sampling. The following sub-sections will illustrate the impact of varying degrees of time difference on the operation of the current differential scheme to faults internal and external to the protected zone.

Internal fault conditions To assess the impact of unsynchronised measurements on the detection of faults internal to the protection zone, the change in the time of the current differential sum reaching a certain threshold is compared to the ideal conditions. For this purpose the same conditions were used as in section 5.2.1, with passive load connection and a constant current difference operating threshold of 100A. The time of measurement of current i_a is taken as a reference with the measurement of i_b being increasingly delayed. Due to the passive load connection, results are derived from (5.15) and (5.16), which represent i_a and i_b respectively. The results of this comparison are presented in table 5.12.

Table 5.12: Calculated difference in time for current differential sum reaching a threshold of 100A for different synchronisation errors

t_{sync} (μs)	$t_{\Delta i}(\mu s)$	Change in operating time (μs)
0	0.736	n/a
-1	0.874	0.138
-2	1.031	0.295
-5	1.614	0.878
-10	3.023	2.287

Table 5.12 illustrates that while the timing of the differential sum reaching 100A is slightly delayed, and that this delay is proportional to the difference in measurement timing, the time difference is reasonably insignificant. Taking into consideration the measurement sampling rate of the differential processing device, table 5.12 suggests that the device would be unlikely to notice this change in timing, except perhaps for the $10\mu s$ unsynchronised case. Therefore the protection

operation time would be unaffected unless measurements were unsynchronised to a greater degree.

External fault conditions For any fault external to the protected current differential zone $i_a(t) = i_b(t)$ and so the differential sum should be equal to zero (again with the exception of capacitive current flow). However in the case where current measurements are not exactly synchronised, one of the current measurements will be displaced in time. During periods where rate of current change is high this may result in a non-zero differential sum. This rate of change is likely to be greatest with underdamped circuit conditions, which will be considered here to assess the worst case scenario. The current differential expression now is

$$\Delta i = i_a(t) - i_b(t + \Delta t). \tag{5.32}$$

where Δt is the difference in measurement time between $i_a(t)$ and $i_b(t)$. Substituting underdamped current expressions to illustrate the most onerous conditions, (5.32) becomes

$$\begin{aligned}\Delta i = \frac{v_{CF}(0)}{L\omega_d} e^{-\alpha t} \sin(\omega_d t) + i_L(0) e^{-\alpha t} \left[\cos(\omega_d t) - \frac{\alpha}{\omega_d} \sin(\omega_d t)\right] \\ - \left(\frac{v_{CF}(0)}{L\omega_d} e^{-\alpha(t+\Delta t)} \sin(\omega_d (t + \Delta t)) \right. \\ \left. + i_L(0) e^{-\alpha(t+\Delta t)} \left[\cos(\omega_d (t + \Delta t)) - \frac{\alpha}{\omega_d} \sin(\omega_d (t + \Delta t))\right] \right)\end{aligned} \tag{5.33}$$

and collecting like terms this equals

$$\begin{aligned}\Delta i = \frac{v_{CF}(0)}{L\omega_d} \left[e^{-\alpha t} \sin(\omega_d t) - e^{-\alpha(t+\Delta t)} \sin(\omega_d (t + \Delta t))\right] \\ + i_L(0) \left[e^{-\alpha t} \cos(\omega_d t) + e^{-\alpha(t+\Delta t)} \cos(\omega_d (t + \Delta t)) \right. \\ \left. - \frac{\alpha}{\omega_d} \left(e^{-\alpha t} \sin(\omega_d t) - e^{-\alpha(t+\Delta t)} \sin(\omega_d (t + \Delta t))\right)\right].\end{aligned} \tag{5.34}$$

Equation (5.34) represents the fault response shifting in time but not the pre-fault current. For $i_a(t)$ it is only valid when t is greater or equal to the fault time, t_f, and for i_b it is only valid for $t \geq (t_f + \Delta t)$, as $(t_f + \Delta t)$ is the time at which i_b is first measured after the fault occurs. As (5.34) contains both i_a and i_b, it is valid for $t \geq (t_f + \Delta t)$.

To provide an example of the issues that can be caused by measurement non-synchronisation, consider the output of the converter capacitance for a short circuit fault on a load within a microgrid network, such as those shown in figures 5.1 and 5.7 (where load is 35m away from the capacitance). Figure 5.12 plots the current difference function in (5.34) against time for a relevant sample of measurement time differences, with the fault occurring at $t = 0$. Initial conditions of $v_{CF}(0) = 400V$ and $i_L(0) = 125A$ (supply to $50kW$ load at $400V$) are used to represent steady state conditions prior to the fault.

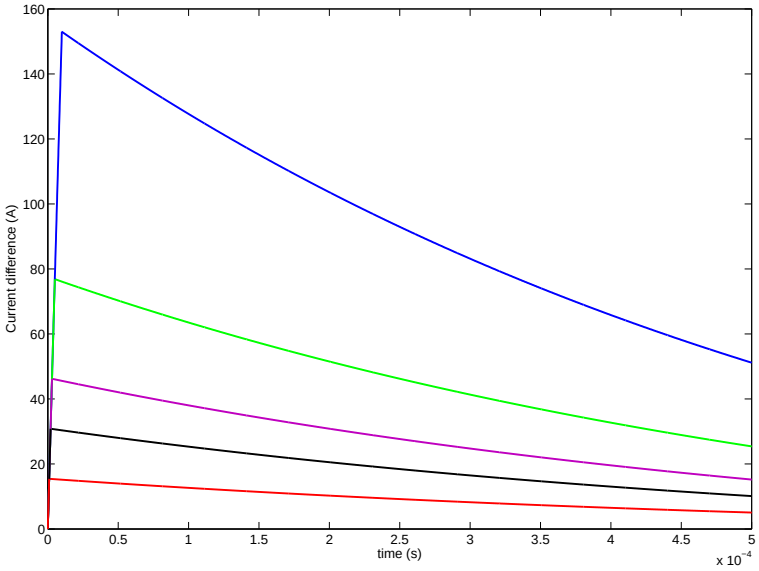

Figure 5.12: Calculated comparison of current difference resulting from non-synchronisation of current differential zone measurements. From bottom to top the time synchronisation error is $1\mu s$ (Red), $2\mu s$ (Black), $3\mu s$ (Purple), $5\mu s$ (Green), $10\mu s$ (Blue)

Figure 5.12 shows that over the transient period, the difference in the time at which i_a and i_b are measured causes a non-zero current differential sum over the initial capacitor discharge period. The magnitude of the error in the differential sum is proportional to the difference in measurement time, as is illustrated.

The figure shows that there are short periods of high differential current which could potentially cause a scheme to mal-operate. This would cause major issues for protection coordination in unit schemes. As it is desirable that the scheme correctly detects faults under transient conditions it will not necessarily be possible to wait an extended time period to filter out these erroneous current differences. Solutions to overcome these non-synchronisation issues which are more suited to the needs of the application are discussed in Chapter 6.

5.3 Optimising the roles of unit and non-unit protection methods within DC networks

Section 5.1 demonstrated the challenges in effectively implementing non-unit protection and concluded that more robust protection approaches are required to achieve correct coordination of network wide protection devices. To achieve greater levels of fault discrimination within these networks, the implementation of a unit protection scheme was identified as being necessary provided that the performance issues highlighted in the previous sections can be addressed. However the scope for the implementation of unit protection is typically limited due to the additional cost (and space and weight for many transport applications) associated with the necessary communication and relay technology. With this in mind, and using the case study presented within section 5.1.2 for reference, the following section considers how unit protection may be applied to improve protection system performance in an economic manner.

5.3.1 Impact of unit protection implementation on overall protection scheme

To assess where unit protection may be applied most effectively within the network presented in figure 5.7, this section specifically considers how the implementation of unit protection upstream within a network may ease the constraints of downstream non-unit protection. The analysis assumes that the implementation challenges presented within section 5.2 can be overcome.

Within figure 5.7, one example of this would be the application of a current differential scheme between the supply converter output and the first parallel connection point (prior to P_2 and P_3) in place of an overcurrent scheme. The major impact this would have on downstream protection would be to remove the constraint of reducing the P_1 threshold to achieve acceptable operating times under impedance fault conditions. This could be achieved as the unit protection zone would be insensitive to external faults and hence not operate even with high current throughput. The subsequent effect of this would be to enable the remainder of the protection settings within the network to return to the initial values derived from the time of undervoltage, increasing the time margin between the operation of different devices. However this still leaves very tight operating time requirements, particularly where devices have to coordinate with other downstream protection devices.

Section 5.1.2 shows that the time margin between adjacent devices from P_3 onwards is similar, and this is due to the uniform fault separation and cable parameters within the network. To adhere to the requirements for operating protection prior to a network undervoltage, it was shown in section 5.1.2 that the only means of increasing this time margin is to decrease the downstream threshold. This is possible between P_3 and P_4, however due to the connection of additional parallel loads downstream for P_5, potential reduction in the overcurrent threshold at P_5 is limited. The application of unit protection at each of these parallel connection points would not only ensure accurate fault detection for internal zone faults but also that there is sufficient time available for the operation of protection devices for load connection points. Protection of these parts of the network could be achieved through the use of simpler non-unit techniques such as those described previously.

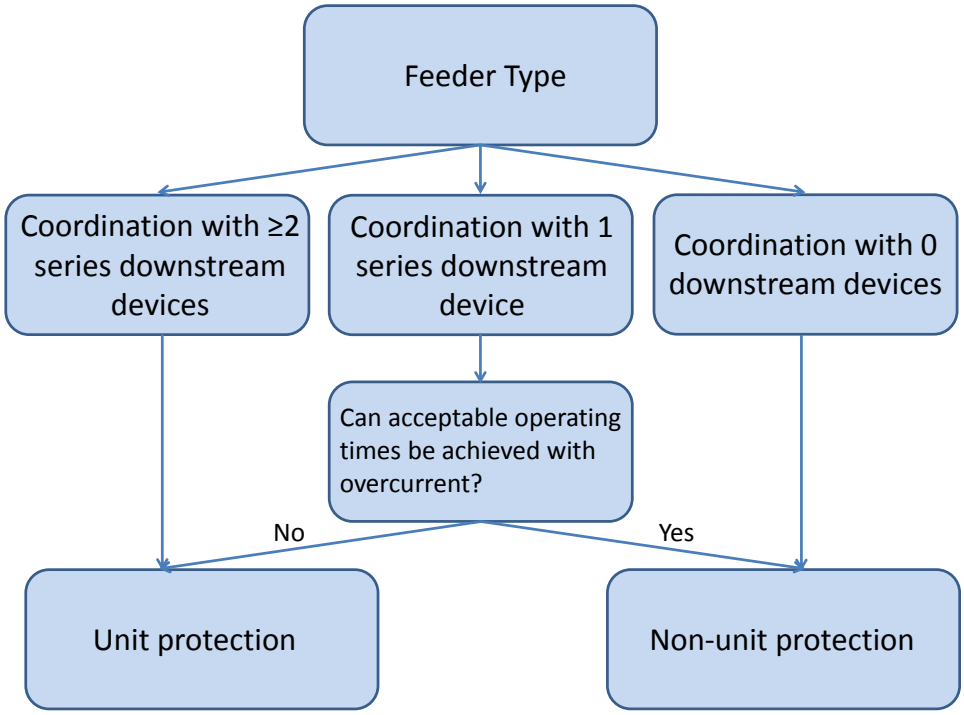

Figure 5.13: Protection scheme approach decision tree

By capturing and simplifying the findings of previous studies, figure 5.13 presents a framework to provide guidance in the design of effective converter interfaced DC network protection schemes. Within the figure the three feeder types can be traced back to the main network diagram (figure 5.7), where P_1 and P_3 coordinate with ≥ 2 downstream devices, P_5 coordinates with 1 series downstream device (either P_6 or P_7) and P_2, P_4, P_6 and P_7 do not coordinate

with any other network protection devices.

The approach does not give a definitive solution but highlights that a balance can be struck between the uses of the two protection philosophies. This enables optimisation of the network protection implementation, trading between required system performance and cost.

5.4 Chapter summary

The development of effective protection system solutions is a critical step in the development of high performance multiterminal DC systems. The key contribution of this chapter is to identify the means with which to achieve fast and effective protection system operation, whilst seeking to minimise installation costs, against a set of very strict operating requirements. The section has demonstrated the limitations of non-unit protection methods to achieve effective fault discrimination within derived operating times and concludes that more robust protection approaches are required. The use of current differential protection is introduced as a potential solution and the inherent challenges in its implementation to DC networks are assessed, with the availability of a high bandwidth communications system being essential to operate effectively within the derived operating times, although this has implications for system cost and complexity. Following the analysis of these protection methods, the potential roles of unit and non-unit protection methods are defined within the example microgrid network. Extrapolating this analysis, a design framework is proposed for DC microgrid systems which provides a means of optimising protection scheme design to achieve required fault discrimination and operating speed whilst seeking to minimise installation costs.

The work presented within this chapter has formed the basis of two publications, the details of which are described in [22, 23].

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Chapter 6

Novel methods of unit protection implementation within DC networks

When applied in AC systems current differential protection typically has a target operation time of 1-2 cycles, which often represents an operation time of $> 20ms$ [1,2]. In comparison, the various operating time requirements derived in chapters 4 and 5 are much shorter. Therefore alternative implementation methods must be deployed in order to meet these operating times.

One factor which prevents the reduction in operating time of an AC current differential system is the requirement for individual phase current measurement and phasor comparison [3]. As discussed in Chapter 2, this requirement does not exist for DC implementation, where only current magnitudes need to be compared. Furthermore, as DC current will be measured using a current transducer (such as a Hall Effect device) rather than via a current transformer, the measurement will be in the form of voltage which facilitates easier integration with processing devices. This property has been utilised within the proposed methods described within the following sections.

6.1 'Pilot wire' current differential protection implementation

Due to the compact size of the applications considered in this thesis, they lend themselves to a pilot wire type scheme [3] where current measurements are directly compared. As current transformers cannot be used on DC systems, a

differential current calculation cannot be performed using circulating currents as is traditionally the case in AC systems [3]. However as the nature of DC current measuring devices is such that the differential current would be established through a comparison of the devices output voltage, which is proportional to current, this allows some more flexibility in the summing and comparison of these measurements.

To achieve coordinated protection system operation within the derived time constraints using a current differential scheme, this chapter proposes the use of a central processing device to compare current measurements. This could involve either physically summing currents prior to the central device or the direct input of analogue measurements to the central device, where analogue to digital conversion would take place, before the sum of currents is compared to trip threshold and the decision sent to the circuit breakers. To investigate the feasibility and effectiveness of this approach, this chapter will assess both implementation options as potential methods of achieving current differential busbar protection on the example UAV network illustrated in figure 6.1. This network is similar in style to the other busbar networks considered throughout this thesis but with generation and load ratings representative of a UAV system [4]. Within the figure, loads referred to as 'Active' represent those which are converter interfaced as within the previous chapter.

6.1.1 Current differential scheme with synchronised measurements

Figure 6.2 illustrates the portion of the network considered within the following studies. For the case studies presented within this section, a single protection zone is considered. This zone encompasses the upper busbar of the UAV network and assumes that appropriate current monitoring and breaking systems are present at each connection to this busbar. Also, in order to provide greater clarity in the findings presented, the UAV network is modelled with only one generator, one active load and both passive loads in operation, as indicated by the open and closed switch positions in figure 6.2.

On this network, the first current differential system modelled assumes that the differential calculation is performed in hardware using analogue busbar current measurements (hence achieving synchronism of inputs). The summed output is then passed to a microcontroller/relay, where an analogue to digital signal conversion and comparison to a trip threshold is performed. On the basis of this final comparison, a trip or no-trip signal is sent to the associated breakers around

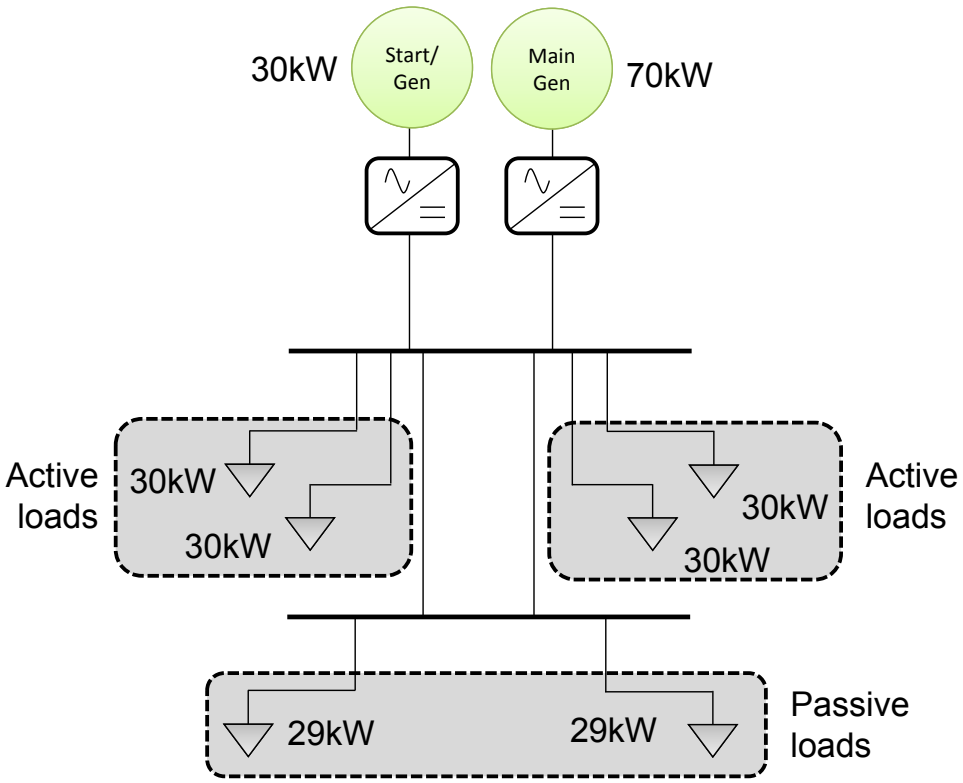

Figure 6.1: Representative UAV electrical system architecture

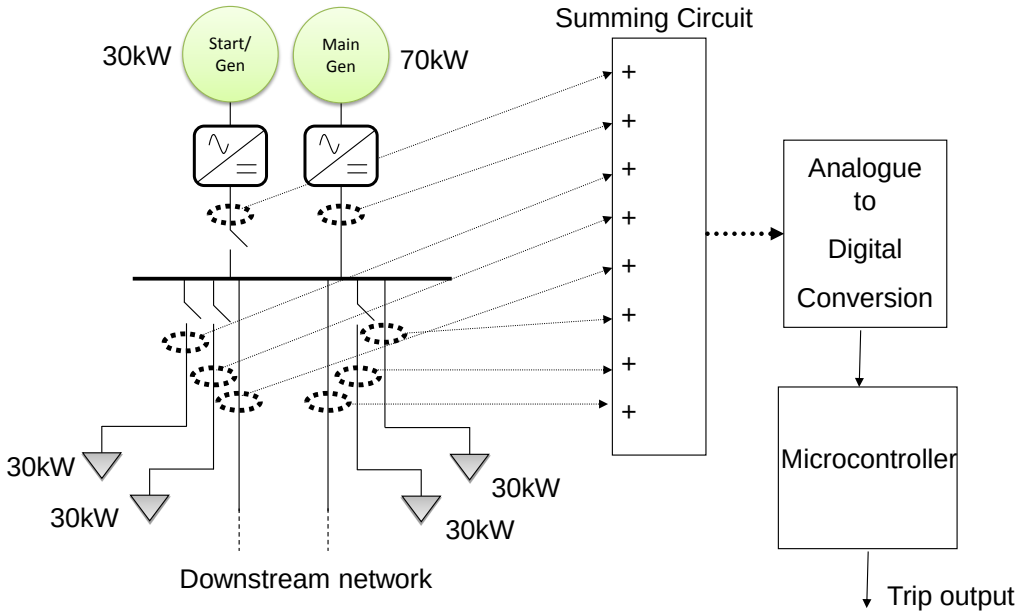

Figure 6.2: Proposed current differential scheme with physically summed currents and central microcontroller

the upper busbar.

The implemented model also incorporates the finite response time of the current transducers, which in this case are Hall Effect devices, to account for any impact this may have on the current differential protection system operating time. A response time of 500ns is utilised for all Hall Effect units which has been derived from an example device datasheet [5]. It should be noted that whilst the Hall Effect devices can track the rate of change of current to a sufficiently accurate degree for the application considered [5], their current rating can typically be low compared to other measurement technologies. Therefore in practice, higher current rated measurement devices may be required for the current based protection scheme to ensure high magnitude currents were accurately represented. The issue of sensor saturation is not considered within this study but should be investigated in future work.

The protection scheme model also includes an additional delay of 500ns to represent the operation of the summing circuit, which has been approximated from typical slew rate properties of operational amplifiers. The output from the summing circuit is fed to the modelled microcontroller which compares this to the operating threshold of the current differential scheme. As Chapter 2 describes, proportional biasing can used to compensate for the various sources of error in the differential calculation such that spurious tripping may be avoided [3]. This biasing can be used to supplement any fixed operating current threshold. For the busbar protection devices, the large difference in steady state and peak fault current magnitudes dictates that a variable threshold scheme is preferable. For the case studies presented, a threshold which is proportional to the generators' current output (as measured at the busbar connection) is employed with an additional constant component defining the minimum operating level. The mathematical expression for this operating threshold is given by

$$I_{threshold} = 1 + 0.02 I_{Busbarinput}. \tag{6.1}$$

Note that this threshold current is not necessarily optimised (and in fact is significantly lower than would be used in practice for the potentially high levels of fault current) but provides a satisfactory illustration of the role of the biasing element within current differential schemes. If the output of the summing circuit is greater than the threshold current, the microcontroller/relay will send a trip signal to all relevant breakers around the protection zone. Within the modelled system, this trip signal is generated after a delay of $6.7\mu s$, representing the signal conversion and algorithm processing delays. This figure is based on data obtained

for the Freescale MCF52235 ColdFire Integrated Microcontroller [6]. Again the microcontroller utilised within this example is not necessarily optimised for this application but does provide a satisfactory illustration of the impact of conversion and processing delays on the operation of the current differential scheme.

The following subsections illustrate the performance of the current differential scheme when faults are applied within and outwith the protection zone.

Busbar faults

This section will illustrate the response of the differential scheme to faults on the upper busbar (i.e. within the protection zone). Both low ($1m\Omega$) and high ($500m\Omega$) impedance faults will be considered.

Low impedance busbar fault A $1m\Omega$ rail to rail fault is applied across the upper busbar after 0.6s of simulation time. Figure 6.3 shows fault current profile and figure 6.4 shows the differential current sum less the applied threshold current.

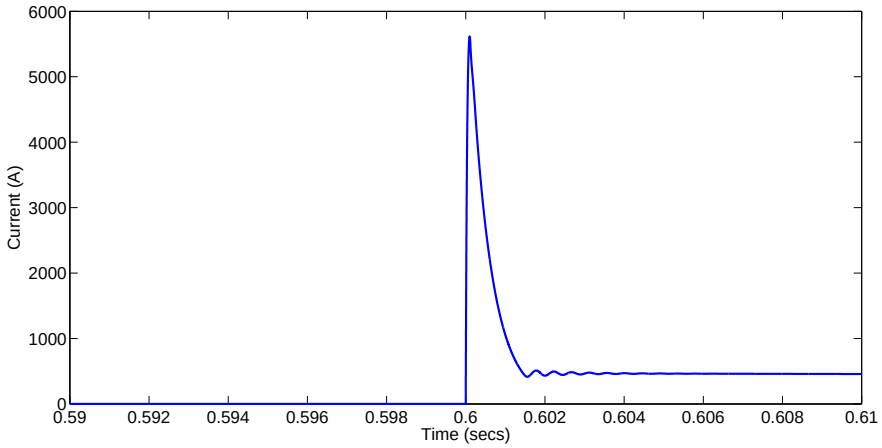

Figure 6.3: Simulated fault current for a low impedance busbar fault

Prior to the occurrence of the fault, the applied threshold current is approximately 3A due to sum of the constant threshold element, 1A, and the proportional initial load current (2% of 111A). Therefore, current sum less this threshold is -3A. When the fault occurs, this current sum increases rapidly, crossing zero approximately 120ns after the occurrence of the fault. Incorporating all process delays described above, the total time for the trip signal to be generated is approximately $7\mu s$, which is well in advance of the occurrence of the current peak (providing the opportunity to break at low current magnitudes). The speed of operation and successful discrimination achieved by the current differential scheme is far greater than appears to be possible with traditional non-unit schemes.

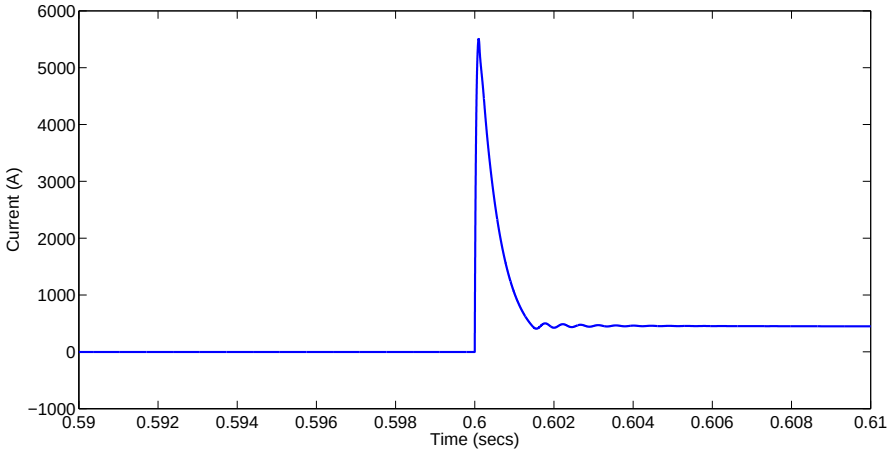

Figure 6.4: Simulated current sum less applied threshold current for a low impedance busbar fault

High impedance busbar fault A $500m\Omega$ rail to rail fault is applied across the upper busbar after 0.6s of simulation time. Figure 6.5 shows fault current profile and figure 6.6 shows the differential current sum less the applied threshold current.

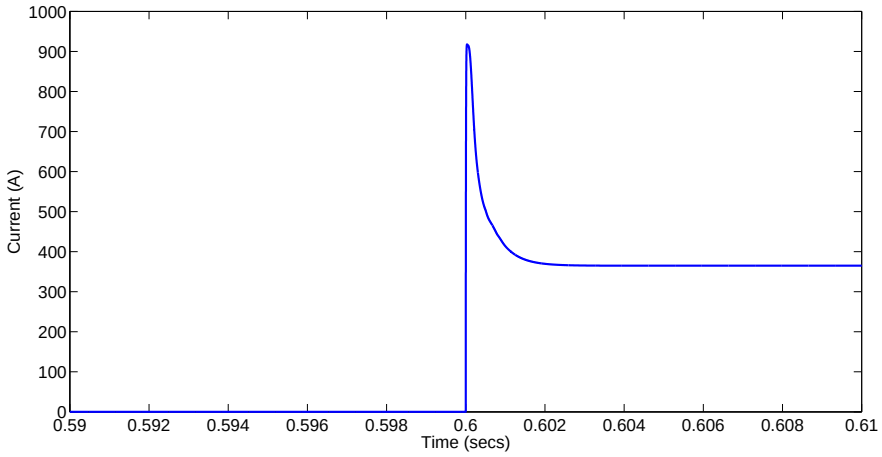

Figure 6.5: Simulated fault current for a high impedance busbar fault

In the case of a high impedance fault being applied across the upper busbar, the initial fault current profile (which is primarily of function of fault path inductance) is similar to that of the low impedance fault case. This aspect in conjunction with the low trip threshold employed results in a coordinated protection system response of near identical speed to that demonstrated in the previous case study. Under these operating conditions, it is clear that the differential approach outperforms any of the non-unit methods considered in Chapter 5.

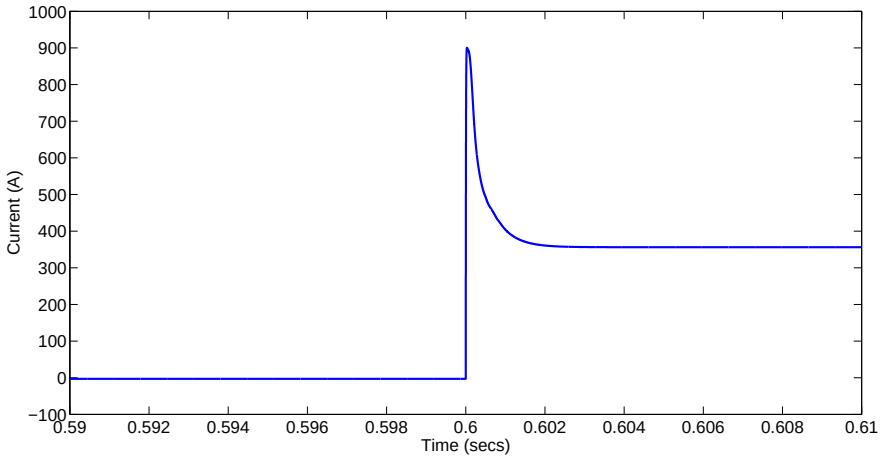

Figure 6.6: Simulated current sum less applied threshold current for a high impedance busbar fault

External faults

This section examines the response of the current differential system to a low impedance fault on a section of cable 5m outside the protection zone. This fault condition produces a substantial through-current condition which may cause the current differential scheme to spuriously trip. Figure 6.7 shows fault current profile and figure 6.8 shows the differential current sum less the applied threshold current.

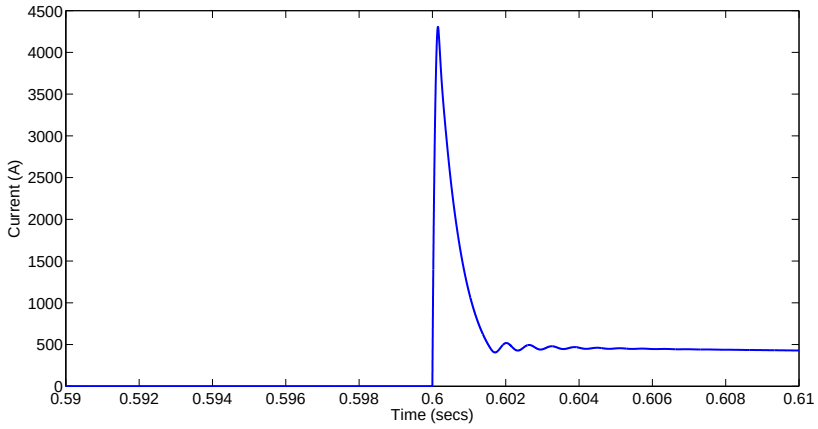

Figure 6.7: Simulated fault current for a low impedance external zone fault

In this case, current sum less the applied threshold current is always negative in polarity and never approaches zero. As such, the current differential scheme has shown the ability to minimise any errors by very closely synchronising current measurements. This enables fast and accurate discrimination between faults

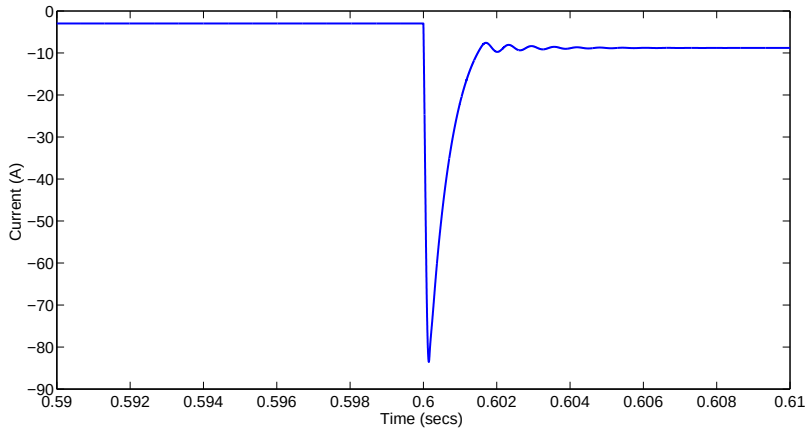

Figure 6.8: Simulated current sum less applied threshold current for a low impedance external zone fault

within and outwith the designated protection zone.

6.1.2 Current differential scheme with non-synchronised inputs

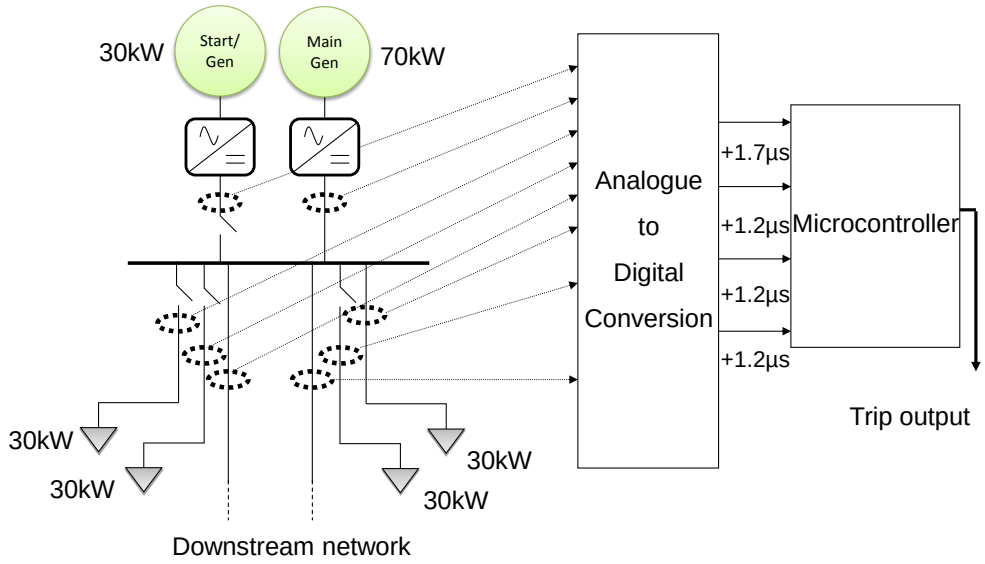

Figure 6.9: Proposed current differential scheme with individually sampled currents digitally summed

This section examines the performance of a second current differential scheme which operates with non-uniform delays applied to the current sum inputs. As such, they are not perfectly synchronised like the previous scheme considered. This second model is representative of a protection scheme implemented using a microcontroller which converts all analogue measurements to digital form before

they are summed and compared to a trip threshold. The parameters employed within the model are based on the Freescale MCF52235 Coldfire Microprocessor [6]. As before, this device was chosen purely for illustrative purposes.

The chosen microcontroller has two A/D converters, allowing two measurements to be converted simultaneously. These measurements are then stored in a memory buffer as the subsequent two measurements are converted and so on until all inputs are converted. At this point the summing and comparing algorithm is run. As all inputs are not converted simultaneously, the synchronisation error between each pair of measurements is equal to the time taken to convert the previous inputs. For the microcontroller modelled, the first conversion takes $1.7\mu s$ with subsequent conversions taking $1.2\mu s$. These conversions are modelled as variable delays. All other modelled measurement and processing delays are consistent with the current differential scheme presented in section 6.1.1.

The following subsections will focus on the response of the current differential scheme to faults outside the protection zone in order to illustrate the impact of poor synchronisation between current sum inputs.

Response to external faults

A $1m\Omega$ rail to rail fault occurs across a section of cable 5m outside the protection zone after 0.6s of simulation time. Figure 6.10 shows the differential current sum (without subtraction of the threshold).

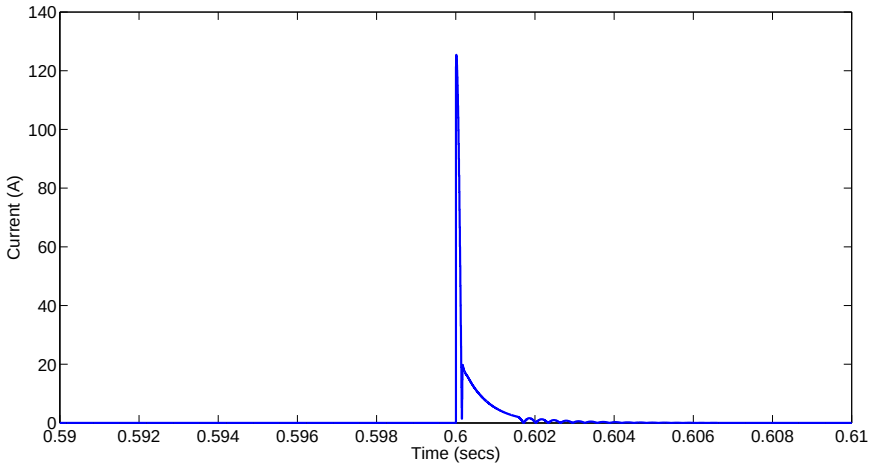

Figure 6.10: Simulated current sum for a low impedance external zone fault

In the case of the ideal current differential scheme (with perfectly synchronised inputs), this current sum was zero for faults occurring outwith the protection zone. However, with the current measurements now staggered over a period of

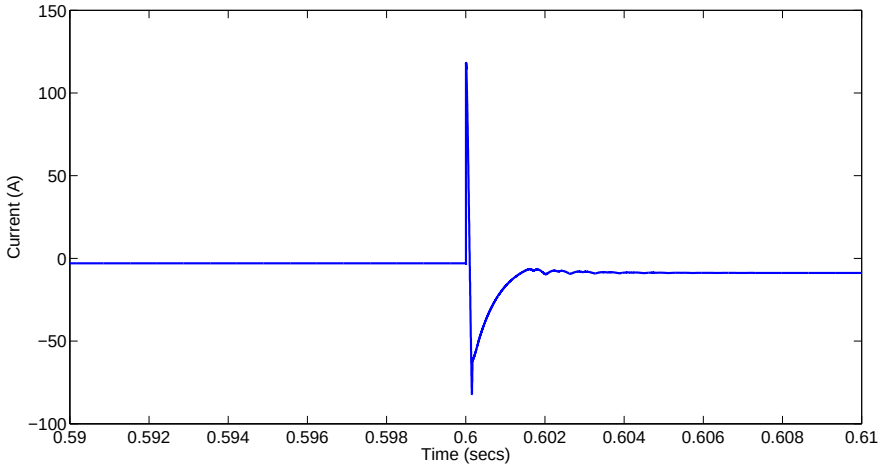

Figure 6.11: Simulated current sum less applied threshold current for a low impedance external zone fault

nearly $5\mu s$, the current sum is transiently non-zero, reaching a peak of 125A. The resulting differential current sum with threshold current subtracted has been illustrated in figure 6.11.

Immediately following the fault, the current sum becomes far greater than the threshold, causing protection to spuriously operate. The peak difference is approximately 116A before the differential sum decreases in magnitude and the threshold current increases in magnitude, restoring the negative difference.

Operation of scheme with increased threshold current This section investigates how changing the threshold current on the differential calculation can prevent spurious tripping for faults outwith the protection zone as well as discussing the impact of this on the differential scheme sensitivity.

In the previous example, the peak difference between the current sum and threshold was approximately 116A. Increasing the constant component of the threshold to 120A would prevent spurious tripping during the fault condition considered. To illustrate this effect, figure 6.12 shows the current sum less the new applied threshold during the occurrence of a simulated $1m\Omega$ fault, 5m outside the protection zone.

By employing the increased threshold, the net difference between the current sum and the threshold does not cross zero. As such, spurious tripping for this particular external fault is avoided. Further fine tuning of the threshold current characteristic would facilitate a similar response for all faults outwith the protection zone.

Whilst increasing the threshold utilised within the current differential scheme

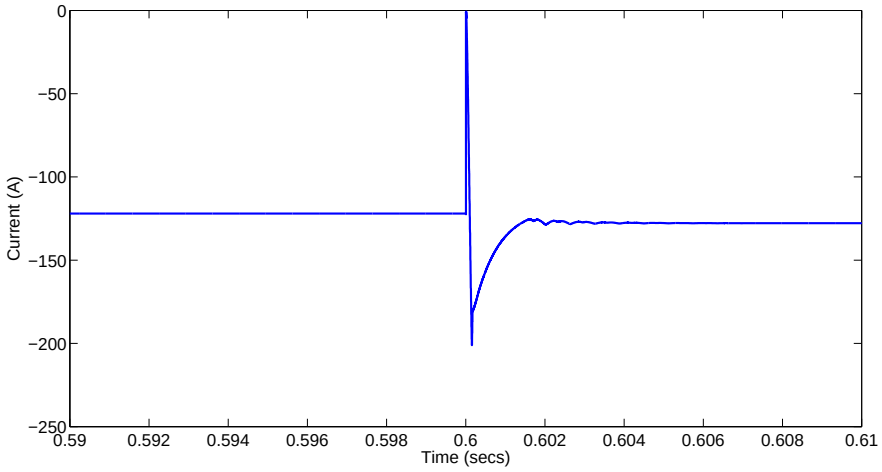

Figure 6.12: Simulated current sum less larger applied threshold current for a low impedance external zone fault

can prevent spurious tripping during through-fault conditions, it also reduces the sensitivity of the scheme to faults within the protection zone. This could potentially result in the non-detection of very high impedance faults (i.e. those which produce a fault current of less than the 120A needed to exceed the constant threshold) on the upper busbar. Further research is required to determine the impact of this limitation. However, it should be noted that non-unit methods would have similar difficulties in detecting such high impedance faults.

6.1.3 Discussion on current differential scheme effectiveness

The compact nature of the UAV network and the resulting highly transient fault response is such that the sensitivity, speed of operation and discrimination capabilities of any current differential scheme employed are highly dependent on the summation and data processing approach and associated devices selected. In particular, the key factor in the effectiveness of any current differential scheme is the synchronisation of current measurements utilised in the summation process. The two case studies presented in sections 6.1.1 and 6.1.2 illustrate the response of a particularly effective and particularly poor system respectively. In practice, the response of a typical scheme would be expected to lie somewhere in between the two examples given, especially if a microcontroller more suited to this application was selected. More specifically, a microcontroller with the capability to simultaneously convert additional parallel channels would ensure measurement synchronisation. Alternatively, sample and hold circuitry could also be utilised

prior to analogue to digital conversion stage (combining the analogue and digital summing approaches described in earlier sections) to provide this function [7]. Whatever the means of achieving this synchronisation, the results highlight the potential of this type of approach to achieve very fast and coordinated protection operation.

6.2 Alternative use of threshold currents to overcome the synchronisation effects

As the previous section shows, the error in the current differential stems from any relative time difference between the measured currents. The examples given illustrate the potential for mal-operation of a unit scheme for faults external to the protected zone. It is therefore essential that these issues are prevented or overcome to achieve reliable protection system performance.

Whilst the approach outlined in the previous sections goes some way to address these issues, cases will always exist where measurements cannot be accurately synchronised in time. The source of this error might simply be due to processor conversion time, as in the previous example, or in situations where the physical connection of analogue measurements to a central point may be more difficult to achieve, such as for physically larger networks or in an electrically noisy environment, in which case communications would likely be employed.

Within previous sections, expected current differences were overcome with the use of fixed threshold currents. However, as previously discussed, this reduces the sensitivity of the scheme to faults within the protection zone. Greater sensitivity of differential schemes operating under wider ranging current conditions is typically achieved by making the magnitude of the threshold current proportional to the fault current. However, in the scenario described, the maximum differential error occurs when $\frac{di}{dt}$ is near its peak, i.e. at low current levels. Hence a threshold proportional to fault current may still not prevent protection mal-operation. Novel biasing approaches may be required to overcome this issue and this is an area for future work.

6.3 Chapter summary

The initial test results presented within this chapter suggest that either of the proposed approaches may be a viable methods of implementing high speed, coordinated protection system operation. A review of literature highlights that these

methods have the potential to accelerate protection operating speed beyond anything in current applications. Further research is required to determine whether this type of DC current differential scheme could operate quickly enough in a practical environment to meet the fault detection requirements and whether this approach is easily scalable to larger networks, such as shipboard and microgrid networks. However if similar levels of performance could be demonstrated in a practical environment, this would be a significant step towards achieving the optimal protection, at least for small, power dense networks. Therefore this is an important research area to pursue in future.

6.4 Bibliography for Chapter 6

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Chapter 7

Fault detection and location in DC systems from initial $\frac{di}{dt}$ measurement

Chapter 5 identified the difficulties in utilising non-unit methods for protection selectivity over the capacitive discharge period in physically compact systems. These difficulties stem from the small line impedance between different parts of the network which results in higher impedance faults tending to dominate the network fault response. However it was observed that in the period immediately following a fault, the rate of current discharge from converter capacitors was relatively insensitive to fault resistance. Instead it was seen that line inductance played a far more significant role in defining this rate of change. From this characteristic it was identified that protection selectivity could potentially be achieved through non-unit methods by measuring the initial $\frac{di}{dt}$ from the DC side converter capacitance. It is worth noting that [1] has also recognised the potential for inductance estimation, and hence fault location, using this type of measurement. Whilst the intended application was for the location of temporary cable arc faults (the location information would then be used to assist maintenance of faulted cable sections) rather than primarily for fault discrimination and protection coordination, [1] does help to validate the concepts presented within this chapter.

To assess this possibility, this chapter will investigate the potential for reliable fault detection and selectivity using this type of measurement. The work in this chapter will first build on previous analysis to describe the $\frac{di}{dt}$ response and highlight why it is insensitive to fault resistance. The potential use of this measurement in a protection scheme and application areas will be discussed. Hav-

ing illustrated the concept, the initial $\frac{di}{dt}$ response will be analysed under various circuit conditions and the limiting factors will be discussed. Ideal measurement conditions will initially be considered to assess whether anything would prevent successful fault detection and then issues for practical implementation are investigated. These include areas such as measurement requirements and integration of the measurement into a wider protection scheme. Finally, areas of future work to develop the concept will be discussed.

7.1 Concept analysis

When a switching event occurs (i.e. a fault), the voltage at the point of the fault will initially decrease creating a difference between the capacitor and fault voltages. To balance these voltages, the capacitor will discharge current. To illustrate this, consider the equivalent RLC circuit diagram shown in figure 7.1.

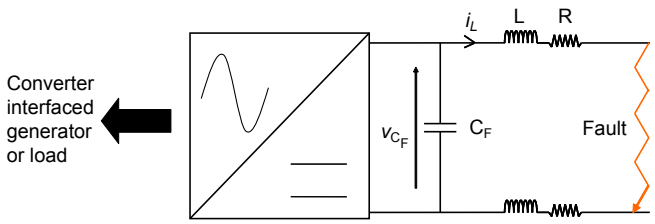

Figure 7.1: Equivalent circuit for the faulted network

It has been shown in previous chapters that the derivative of this discharge current for this circuit is

$$\frac{di_L}{dt} = \frac{v_{CF}(0)e^{-\alpha t}}{L}\left[\cos(\omega_d t) - \frac{\alpha}{\omega_d}\sin(\omega_d t)\right] + i_L(0)e^{-\alpha t}\left[-2\alpha\cos(\omega_d t) + \left(\frac{\alpha^2}{\omega_d} - \omega_d\right)\sin(\omega_d t)\right] \quad (7.1)$$

for underdamped circuit conditions and

$$\frac{di_L}{dt} = \frac{v_{CF}(0)}{L(s_1 - s_2)}\left(s_1 e^{s_1 t} - s_2 e^{s_2 t}\right) + \frac{i_L(0)}{s_1 - s_2}\left[e^{s_2 t}\left(\omega_0^2 + 2\alpha s_2\right) - e^{s_1 t}(\omega_0^2 + 2\alpha s_1)\right] \quad (7.2)$$

for overdamped fault conditions. To thoroughly assess the derivative current response under all damping conditions it is helpful to convert either of these

expressions to the Laplace domain. This can be achieved using a number of standard Laplace properties. The equivalent Laplacian expression of (7.1) is

$$\mathscr{L}\frac{di_L}{dt} = \frac{v_{CF}(0)}{L}\left[\frac{s+\alpha}{s^2+2s\alpha+\alpha^2+\omega_d^2} - \frac{\alpha}{\omega_d}\frac{\omega_d}{s^2+2s\alpha+\alpha^2+\omega_d^2}\right] + i_L(0)\left[-2\alpha\frac{s+\alpha}{s^2+2s\alpha+\alpha^2+\omega_d^2} + \left(\frac{\alpha^2}{\omega_d}-\omega_d\right)\frac{\omega_d}{s^2+2s\alpha+\alpha^2+\omega_d^2}\right] \quad (7.3)$$

Multiplying out and collecting terms, this becomes

$$\mathscr{L}\frac{di_L}{dt} = \frac{v_{CF}(0)}{L}\left[\frac{s}{s^2+2s\alpha+\omega_0^2}\right] - i_L(0)\left[\frac{2s\alpha+\omega_0^2}{s^2+2s\alpha+\omega_0^2}\right]. \quad (7.4)$$

To assess the initial conditions of all Laplacian expressions, the initial value theorem is used. This theorem states $f(t \to 0) = sF(s \to \infty)$. Applying this to (7.4), the higher order 's' multipliers dominate both numerator and denominator of both voltage and current terms as $s \to \infty$, therefore the expression for (7.4) simplifies to

$$sF(s \to \infty) = \frac{v_{CF}(0)}{L}\left[\frac{s^2}{s^2}\right] - i_L(0)\left[\frac{2s^2\alpha}{s^2}\right]. \quad (7.5)$$

Substituting terms and simplifying, this becomes

$$sF(s \to \infty) = \frac{v_{CF}(0) - i_L(0)R}{L}. \quad (7.6)$$

From equation (7.6) it can be seen that immediately after the switching event the derivative current response, under all damping conditions, is proportional to the voltage difference between the capacitor and fault (including initial fault voltage) divided by the line inductance. If it is assumed that $i(0)R$ is negligible (the case where it is not is covered in later sections), due the relatively low line resistance and initial current, then the measurement of $\frac{di}{dt}$ and $v_{CF}(0)$ would allow L to be determined. The time domain equivalent function for this measured inductance is therefore

$$L_{meas} = \frac{v_{CF}(0)}{\frac{di_L(t\to 0)}{dt}}. \quad (7.7)$$

With knowledge of inductance per unit length of the line (H/m), distance from the capacitor to the switching location can be calculated from (7.7). It is proposed that if a measurement is made sufficiently close to time zero then L

can be accurately determined, and hence the location of a fault. The challenges for achieving this are studied in depth within this chapter. If this fault location can be successfully achieved, then this measurement will provide a means of very rapidly detecting and locating a fault on a compact DC network. As Chapter 5 discusses, this approach would differ from currently implemented $\frac{di}{dt}$ methods as it focuses on the initial rather than sustained $\frac{di}{dt}$ characteristic. It would also have the additional benefit of enabling the protection system to operate before full fault current develops and so helping to achieve the protection aims laid out in previous chapters.

The following section discusses how and in what type of network this protection technique could be employed.

7.2 Potential application areas and method implementation

The fault detection method proposed in this chapter is primarily designed for DC distribution networks where generators, energy storage devices and loads (both AC and DC) are interfaced through power electronic converters to the network. As the capacitor fault response provides the mechanism for fault location rather than the response of source or load itself, the converter interface is essential. The following presents an initial proposal into how the fault detection method could be utilised within an example network.

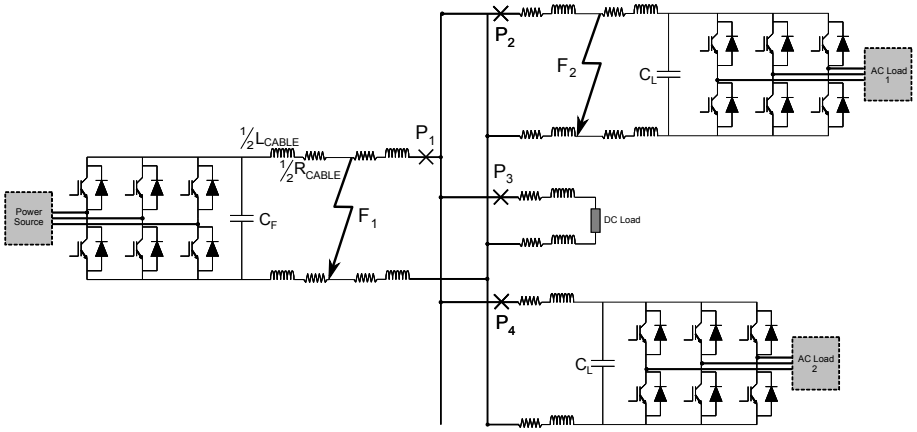

Figure 7.2: Multi-terminal DC network with faults located at the source and active load

Referring to the standard busbar network used for illustration throughout this thesis and shown in figure 7.2, the desired protection system response to the two fault locations would be for the local protection devices to operate to isolate faults

on their branch. This would mean P_1 would act to isolate F_1 and P_2 would act to isolate F_2. For faults occurring on other branches in the network, the non-faulted branches should remain connected. In the example network, there is no means of isolating faults on the DC busbar and these faults can only be cleared through the disconnection of all sources of fault current. To achieve the desired discrimination for branch faults, an initial $\frac{di}{dt}$ measurement could be set on each of the converter output capacitors and, operating in isolation from each other, these would trip on a certain threshold. In this case, if protection is to operate for faults on a branch up to the busbar, the threshold would be set to trip breakers when the inductance measured is less than the inductance of the conductor connecting the capacitor to the busbar. For faults beyond the protected zone it is assumed that protection elsewhere in the network will act to isolate the fault.

For this relatively simple primary protection scheme, the process of operation would be:

1. Determine loop inductance up to the busbar (L_{CABLE})
2. Set relay to trip when $\frac{v_{CF}}{\frac{di_L}{dt}} < L_{CABLE}$
3. Continuously measure $\frac{di_L}{dt}$ and send trip signal to circuit breakers when the threshold is exceeded.

Section 7.5 of this chapter will present various options for how both V_C and $\frac{di}{dt}$ might be measured in the practical implementation and assesses how this and measurement time would impact on the measured inductance compared the initial response.

Ideally this scheme would provide protection of the full branch up to the busbar, however because of measurement and parameter uncertainties this cannot be easily achieved. As is the case with more traditional distance schemes, it is likely that the method would only primarily protect a certain portion of the line to avoid any overreach on to or beyond the busbar [2]. Again, the impact of this on implementation of this method in a protection scheme is assessed in later sections.

Prior to considering the more detailed protection scheme design challenges using initial $\frac{di}{dt}$ measurements for fault detection, the following sections identify a number of practical implementation issues which will potentially limit the range of applications and highlight areas where further development of the concept may be required.

7.3 Practical limiting aspects and initial assumptions

The remainder of this chapter will provide in depth analysis of how different circuit configurations and fault conditions impact on the ability of an initial $\frac{di}{dt}$ measurement to accurately detect a fault. However it is first worth highlighting some assumptions made throughout the chapter as well as some aspects of the method that may limit its application within a practical environment. These are discussed in the following subsections.

7.3.1 Fault resistance/impedance

An area not discussed yet within this chapter is the possibility that a fault may itself contain an inductance which would influence the initial $\frac{di}{dt}$ response, that is, the fault has an impedance rather than being purely resistive. Whilst this cannot be ruled out, there is some evidence at least to suggest that this is unlikely to be a problem for common fault types. For example, the study of arcing faults has shown that the arc voltage and arc current are always in phase [3], and hence are purely resistive.

The inductance in a short circuit fault is more difficult to define due to the large range of possible causes of short circuit. If a short circuit is considered as a conductor of variable length (where length is the distance between the two parts of a circuit being shorted), then the inductance will be equal to the conductor length multiplied by its inductance per unit length. Therefore some inductance will exist in the fault, but its magnitude will vary with many factors such as conductor length, size and material.

Later sections of this chapter calculate the potential error introduced into the line length measurement and discuss that this error must be accommodated by the protection system to enable reasonable coverage of a line. As such, it will be assumed that any expected error introduced into the initial $\frac{di}{dt}$ measurement by fault inductance is negligible, or at least can be accommodated within the expected measurement error. However to fully validate this assumption, or to define the range of fault types under which it is valid, further work is required.

7.3.2 Internal component resistance and inductance

The internal resistance and inductance of any component is likely to have some impact on the initial $\frac{di}{dt}$ response of the network and hence it is important that

it is factored into any analysis. Previous chapters have noted that capacitor ESL is usually negligible in comparison to line inductance and despite inductance being more significant when considering initial $\frac{di}{dt}$, this assumption is maintained for all subsequent analysis in this chapter. Of more importance is the impact of capacitor ESR. A general observation is that as capacitance decreases, ESR increases and as such, the damping is generally higher for smaller capacitors. Whilst this will not affect the initial $\frac{di}{dt}$, the rate at which it decays will increase, impacting on required measurement times. Required timing of measurements is an aspect analysed in detail later in this chapter.

Application to battery systems

One application initially considered for the utilisation of the initial $\frac{di}{dt}$ protection method was that of battery systems connected to a network at rated voltage (i.e. no conversion stage). An example of this type of system is shown in [4], where a battery is directly connected to a DC busbar at 400V within a microgrid (see figure 2.2 within Chapter 2). As shown in [4, 5] the fault current output from a battery can be calculated from

$$i_{batt}(t) = \frac{U_{batt}(0)}{R}(1 - e^{-\frac{t}{\tau}}) \tag{7.8}$$

where $U_{batt}(0)$ is the initial open circuit voltage of the battery, $\tau = \frac{L}{R}$, $R = R_{batt} + R_{line}$ and $L = L_{batt} + L_{line}$. The derivative of (7.8) is

$$\frac{di_{batt}}{dt} = \frac{U_{batt}(0)}{L}e^{-\frac{t}{\tau}}, \tag{7.9}$$

which when assessed under initial conditions becomes

$$\frac{di_{batt}}{dt} = \frac{U_{batt}(0)}{L}. \tag{7.10}$$

Equation (7.10) shows that the fundamental initial response of a battery system is equal to that the capacitive network analysed in above sections, and hence initial $\frac{di}{dt}$ measurements could theoretically be used for fault detection. However unlike capacitive networks, the internal inductance of a battery can be substantial relative to the inductance within an interconnecting cable. An example of this can again be found in [4]. Therefore the magnitude of the battery inductance is such that it is likely to dominate the initial fault response, hence masking any relatively small changes in line inductance caused by shorting of the line under fault conditions and making fault discrimination more difficult. Furthermore [6]

suggests that battery inductance is not constant with state of charge and so compensating for this inductance may also be difficult and lead to measurement inaccuracies.

The combination of these factors suggests that the application of initial $\frac{di}{dt}$ measurements will be relatively ineffective for directly connected battery systems and other protection techniques should be utilised. It should however be emphasised that for battery systems interfaced through a power converter, the capacitance at the network side of the converter may still provide a suitable point for fault detection using initial $\frac{di}{dt}$ measurements.

7.3.3 Varying conductor parameters

For a network such as that shown in figure 7.2 it is possible that a protection zone will encompass more than one conductor type. Within these zones, the resistance and inductance parameters per unit length may be different for these different conductors. Whilst this will not impact on the fault response of the network, it will make protection discrimination more challenging as physical and electrical distance of conductors will not be equal.

7.3.4 Maximum $\frac{di}{dt}$ from the capacitor

One final assumption made within this chapter is that the maximum $\frac{di}{dt}$ seen within the network will be that from the capacitor output in faulted conditions, with the converter output current having a much slower rise time. There are two aspects to the converter output which must be considered within this assumption, the first being the fault response of the converter (or the general controller response) and the second being the harmonic output caused by the converter switching.

From inspection of different converter fault responses from a variety of studies [4, 7–9] it is apparent that a typical converter output is significantly slower than a capacitor, often at least an order of magnitude less. This observation can also be supported through calculation of a converter's response [5, 8].

The impact of switching harmonics can be illustrated through the simulation of an example converter interface. As is the case throughout this thesis, a six switch IGBT converter with freewheeling diodes will be utilised for this illustration. To ensure an accurate representation of current harmonics, a detailed switched converter model is connected to a high speed permanent magnet synchronous generator model within the simulation. The DC side of the converter

is connected to a capacitive filter, representative cable impedance and a resistive load, as illustrated in figure 7.3. The switching pattern of the converter is determined using phase angle control, which is utilised to maintain a constant DC output voltage [10]. To represent different sets of harmonic conditions, two sizes of capacitive filter are considered, the first (C_1) to illustrate normal operating conditions and the second (C_2) representing a high penetration of harmonics into the network. All relevant simulation parameters are summarised in table 7.1 and network outputs shown in figures 7.4 and 7.5.

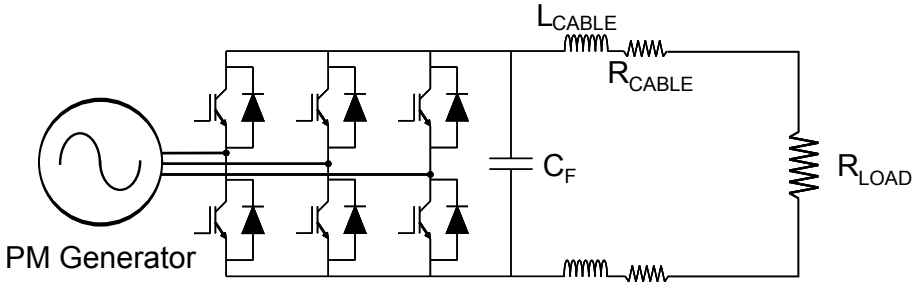

Figure 7.3: Permanent Magnet generator connected to a representative 270VDC network through a controlled six pulse IGBT converter

Table 7.1: Network Parameters

Parameter	Value
Voltage	270V
C_{F_1}	10mF
C_{F_1} ESR	$5m\Omega$
C_{F_2}	1mF
C_{F_2} ESR	$15m\Omega$
R_{load}	4.86Ω
L_{line}	$0.65\mu Hm^{-1}$
R_{line}	$0.801m\Omega m^{-1}$
PWM Carrier frequency, F_s	5000Hz

Figures 7.4 (a) and 7.5 (a) show that in both cases, the $\frac{di}{dt}$ flowing into the filter capacitors is significant and is often similar or greater than that which is typically expected from the fault response (which is in the order of $10^9 As^{-1}$ as described in Chapter 5), although much of this may be due to simulation error. Therefore measurement of $\frac{di}{dt}$ on the capacitive branch would lead to a distortion of any high $\frac{di}{dt}$ caused by a fault. However, figure 7.4 (b) in particular shows that when measured on the line (i.e. after the filter stage), the $\frac{di}{dt}$ caused by converter switching reduces to several orders of magnitude less than the fault response. Therefore the fault response would be readily distinguishable from harmonic response, and the potential for spurious protection operation would be significantly reduced. This is also highlighted in figure 7.5 (b), which illustrates

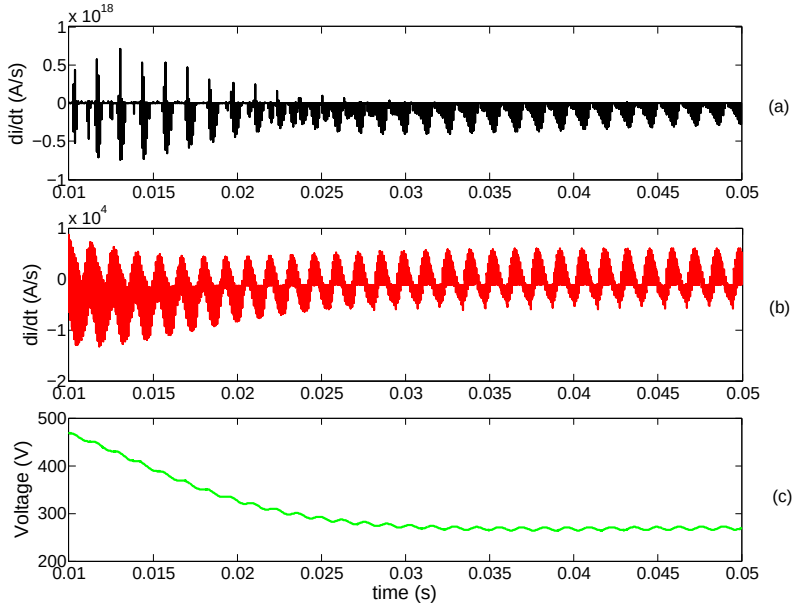

Figure 7.4: $\frac{di}{dt}$ into the capacitance , (a), filtered $\frac{di}{dt}$ on the line ,(b), and DC network voltage, (c), with a 10mF filter capacitance at converter output

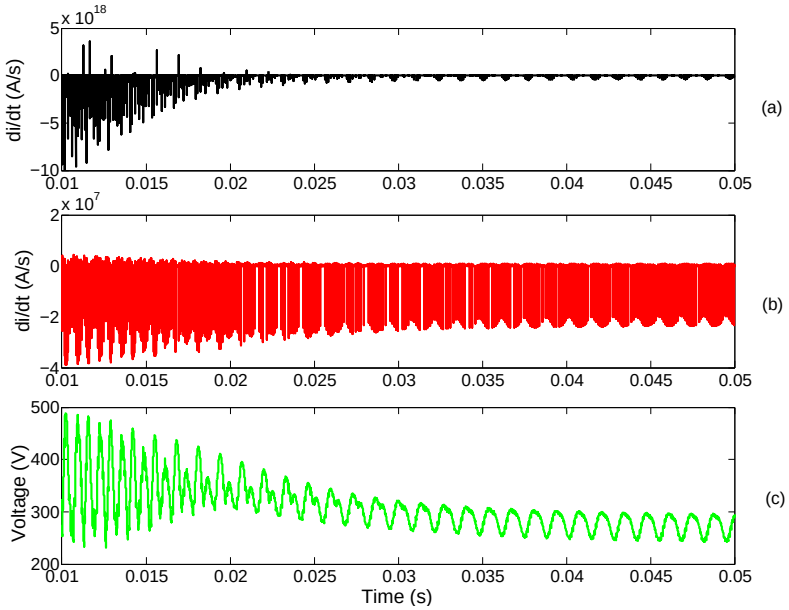

Figure 7.5: $\frac{di}{dt}$ into the capacitance , (a), filtered $\frac{di}{dt}$ on the line ,(b), and DC network voltage, (c), with a 1mF filter capacitance at converter output

that this distinction should still be clear where a high level of harmonics exists on the network, suggesting that the protection method would still function within equivalent networks.

7.4 Analysis of initial $\frac{di}{dt}$ under various circuit conditions

Section 7.1 introduced a relatively idealised case for the applying the initial $\frac{di}{dt}$ technique. This section will explore the aspects which must be properly quantified for it to be successfully employed in a protection scheme. To ensure that there is no network state that would prevent successful fault detection, an analysis of various circuit conditions and configurations is presented. Given that the response at $t = 0$ is the same for all damping conditions, as shown in section 7.1, this section will only present analysis for the underdamped expressions to prevent the unnecessary repetition.

7.4.1 Initial $\frac{di}{dt}$ response to resistive load switching

The nature of the proposed method of implementation of the initial $\frac{di}{dt}$ protection scheme is such that it should be immune to resistive load switching. Analysis in previous sections has shown that the peak $\frac{di}{dt}$ is from the capacitor output and that this is dependent on the line inductance between capacitance and switching event. Therefore provided that the load is outwith the protected zone then the measured inductance will always be higher than that required to operate protection, and hence spurious protection operation will not occur.

A more challenging detection scenario exists where a resistive load is connected within the protected zone. In this case there would be difficulty in distinguishing between high resistance faults and load switching without the use of additional signalling equipment. One option for this would be to block protection operation during load switching periods, however future work is required to determine the feasibility of this approach to overcome these detection issues.

7.4.2 Impact of opposing initial voltage on initial $\frac{di}{dt}$ response

Section 7.1 discusses that there are two main sources of opposing initial voltage, the voltage across the line and the voltage across the fault. The impact which

opposing voltage has on the measured inductance is to increase the apparent length of the line by decreasing the initial $\frac{di}{dt}$.

The voltage across the line exists prior to the fault and by design should be relatively small to ensure correct voltage regulation in the supply to the loads. This can be easily quantified for various fault locations from expected current flows and the resistance up to the fault. It can also be compensated for with reasonable accuracy, as will be illustrated in section 7.6.

The initial voltage drop across the fault is less well known. While the initial current parameter is known, the resistance of the fault is not and this can vary significantly. For short circuit and low resistance faults, the opposing voltage will be small and fault detection will relatively unaffected. However for high resistance faults, the opposing voltage may initially be tens of volts, even for small initial current. This could have a reasonably significant impact on the detection of high resistance faults.

To fully quantify the impact of both line and fault resistance, it would take a large number of calculations due to numerous possible initial current and resistance combinations. As such, it is more illustrative to simply consider their impact of a rising initial voltage for a set system voltage. This can be achieved by considering the percentage error which the initial voltage introduces.

Section 7.1 derives that initial $\frac{di}{dt}$ as

$$\frac{di_L(t=0)}{dt} = \frac{v_{CF}(0) - i_L(0)R}{L} \tag{7.11}$$

where L was defined as the actual inductance from the capacitance to the fault. The measured inductance was derived to be

$$L_{meas} = \frac{v_{CF}(0)}{\frac{di_L(t=0)}{dt}}. \tag{7.12}$$

Substituting (7.11) into (7.12) gives

$$L_{meas} = \frac{v_{CF}(0)}{\frac{v_{CF}(0) - i_L(0)R}{L}}. \tag{7.13}$$

Rearranging (7.13) to find the error in measurement gives

$$\frac{L_{meas}}{L} = \frac{v_{CF}(0)}{v_{CF}(0) - i_L(0)R} \tag{7.14}$$

and from (7.14), percentage error is equal to

$$\% \text{ Line length error } = \left(\frac{v_{CF}(0)}{v_{CF}(0) - i_L(0)R} - 1 \right) \times 100\%. \tag{7.15}$$

Equation (7.15) can be used to quantify the impact of opposing voltage on the measured line length. Figure 7.6 illustrates this by plotting the percentage error in line length against opposing voltage for a 270V DC system. Figure 7.6 shows that the increase in error is approximately linear to begin with, with an increasing error gradient as $i_L(0)R$ increases. By quantifying the potential error introduced figure 7.6 enables it to be compared to the requirements of the protection system to assess whether suitably accurate fault detection can be achieved.

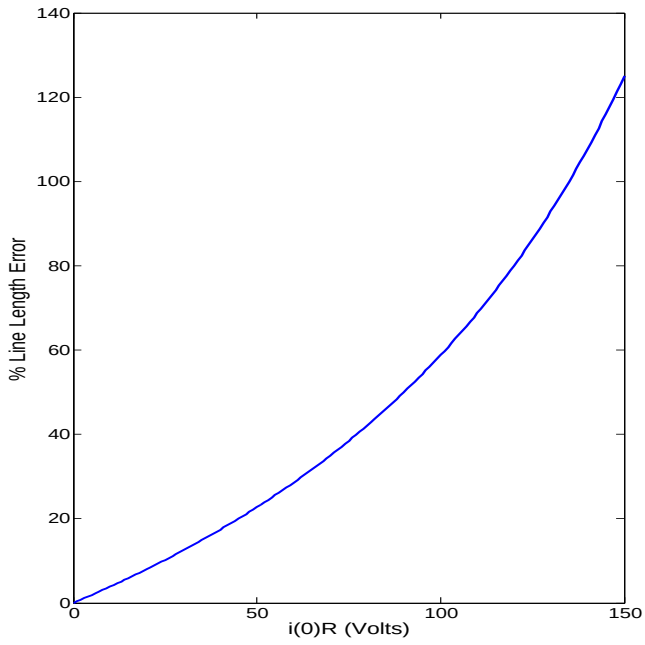

Figure 7.6: Calculated percentage increase in measured line length due to the initial opposing line and fault voltage

While figure 7.6 does provide information on the measurement error, it does not give the complete picture in terms of the impact on fault detection, as this is also dependent on a faults location along a line. For example, consider two different fault locations along a line as illustrated in the network section in figure 7.7. Fault F_1 is located 20% along the line length up to busbar from the capacitor and F_2 is 80% along the line. Now say, for example, that both fault conditions create an opposing voltage of 50V, which increases the measured line length by around 23%. Measuring initial $\frac{di}{dt}$, F_1 will appear to be at 43% along the line

and hence protection covering the whole length of the line will still operate for this fault. However for F_2, the measured fault location will now be 103% along the line and so will appear outwith the protected zone and so protection will not operate. This illustrative case study suggests that while the initial $\frac{di}{dt}$ measurement cannot be relied upon to detect all high resistance fault conditions, there is still potential for a number of fault types to be detected, although those close up will be detected more consistently. As Chapter 5 highlights, this still represents a significant improvement in protection selectivity compared to more traditional non-unit techniques.

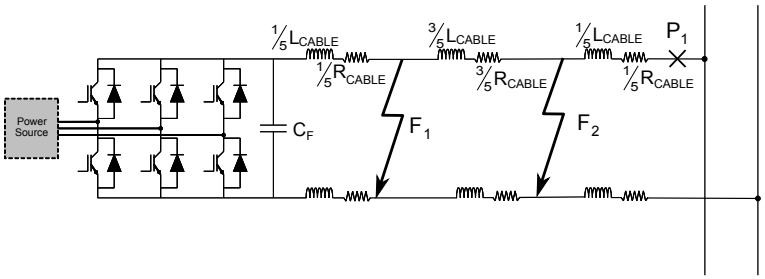

Figure 7.7: Network section with faults placed 20% and 80% along the line up to the busbar

7.4.3 Initial $\frac{di}{dt}$ response with opposing initial current flow

The previous sections have so far conducted analysis on the assumption that the general current flow is away from the capacitive component where current is measured. This section considers a case where current flow may be bidirectional, and hence current would occasionally flow in the opposite direction. Examples of this are converter interfaced loads or starter/generator systems [11–13]. The equivalent circuit to analyse this case is presented in figure 7.8.

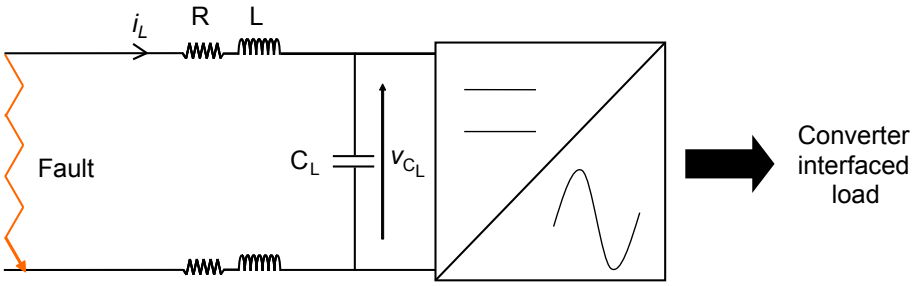

Figure 7.8: Equivalent circuit for the load section of the faulted network with initial current flowing away from the fault

Figure 7.8 illustrates that the main difference in the analysis of this case, is the different polarity of initial current flow. Continuing to assess the underdamped case only, $\frac{di}{dt}$ from C_L is equal to

$$\frac{di_L}{dt} = \frac{v_{CL}(0)e^{-\alpha t}}{L}\left[\cos(\omega_d t) - \frac{\alpha}{\omega_d}\sin(\omega_d t)\right] - i_L(0)e^{-\alpha t}\left[-2\alpha\cos(\omega_d t) + \left(\frac{\alpha^2}{\omega_d} - \omega_d\right)\sin(\omega_d t)\right]. \quad (7.16)$$

Assessing under initial conditions, (7.16) becomes

$$\frac{di_L}{dt}(0) = \frac{v_{CL}(0) + i_L(0)R}{L}. \quad (7.17)$$

Equation (7.17) illustrates that any initial voltage drop across the line (or fault) acts to increase the initial $\frac{di}{dt}$. Therefore unlike previous analysis where line length appears to be longer due to initial voltage, this effect will cause a fault to appear closer than it is. This creates the possibility of a fault outwith a protection zone appearing as if it is within, and hence the protection scheme operating spuriously for faults outwith its protection zone. As before, the impact of the opposing current flow will depend on the relative magnitude of $i_L(0)R$ compared to $v_{CL}(0)$, and so this will be less of an issue on higher voltage systems, but lower voltage systems may be more susceptible to higher percentage location errors. The impact of line voltage drop can be compensated for, which will reduce the likelihood of protection mal-operation (see section 7.6.3). However in cases where high initial fault voltages exist, such as high resistance faults, there is an increased likelihood of false protection operation.

This aspect of the system behaviour clearly has the potential to cause problems for protection selectivity when considering the protection of converter interfaced loads within the proposed time frames. Whilst the increased line length error described previously may prevent the protection system from detecting a fault, it can usually be assumed that a suitable backup would detect it, albeit over a longer time frame. However, the impact of false fault detection is more difficult to evaluate. Obvious issues include the loss of functionality through the removal of non-faulted parts of the network, and subsequently, how the actual fault location is determined and how non-faulted loads are reconnected. Therefore this issue would need to be resolved prior to using this method for any bidirectional network sections. However being the primary intended application area for this fault detection method, the remaining analysis in this chapter evaluates the operation of the protection scheme from the perspective of the generator converter interface.

7.4.4 Initial $\frac{di}{dt}$ response with a capacitive load

To assess the case when a converter interfaced device with a DC side capacitance is connected to a network, this section considers the initial $\frac{di}{dt}$ response where a capacitor is switched into the network. The equivalent circuit required to analyse this response is the same as that use for the overvoltage analysis, and is illustrated again in figure 7.9.

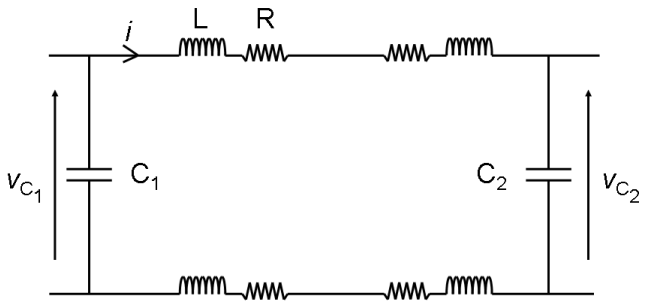

Figure 7.9: Equivalent circuit for the RLC circuit connected to an additional capacitance

As the same equivalent circuit is the used, expressions for current response are also equal. Therefore, as derived in Chapter 3, current is equal to

$$i_L(t) = \frac{v_{C1}(0) - v_{C2}(0)}{L\omega_d} e^{-\alpha t} \sin(\omega_d t) + i_L(0) e^{-\alpha t} [\cos(\omega_d t) - \frac{\alpha}{\omega_d} \sin(\omega_d t)]. \quad (7.18)$$

Taking the derivative of this, $\frac{di}{dt}$ is equal to

$$\frac{di_L}{dt} = \frac{(v_{C1}(0) - v_{C2}(0))e^{-\alpha t}}{L} \left[\cos(\omega_d t) - \frac{\alpha}{\omega_d} \sin(\omega_d t)\right] + i_L(0) e^{-\alpha t} \left[-2\alpha \cos(\omega_d t) + \left(\frac{\alpha^2}{\omega_d} - \omega_d\right) \sin(\omega_d t)\right]. \quad (7.19)$$

To find the initial $\frac{di}{dt}$ response, (7.19) must be assessed under initial conditions. Therefore as $t \to 0$, (7.19) becomes equal to

$$\frac{di_L}{dt}(0) = \frac{v_{C1}(0) - v_{C2}(0) - i_L(0)R}{L}. \quad (7.20)$$

Equation (7.20) shows that the initial $\frac{di}{dt}$ response differs from the resistive case due to the voltage term $v_{C2}(0)$ across the switched capacitance. If this capacitance is uncharged, then it would initially appear as a short circuit on the network. Provided this switching occurred outwith the zone of protection,

then no spurious operation of protection would occur. As $v_{C2}(0)$ subtracts from $v_{C1}(0)$ in (7.20), any positive voltage would act to reduce $\frac{di}{dt}$ and hence reduce the chance of incorrect operation. Spurious operation would only occur if the polarity of $v_{C2}(0)$ was opposite to that of $v_{C1}(0)$. However for a DC system this would not occur under normal operating conditions (unlike capacitor bank switching in AC systems [14]). Therefore the connection of capacitive load types would not adversely impact on the capability to accurately detect faults.

7.4.5 Initial response with parallel capacitors and common branch fault location

There will be a number of fault locations in a network where a common branch exists between two or more of the contributing fault current sources. In these cases, there is a division of current between the branch containing the fault and the other parallel branches due to the impedance of the common branch and fault. The parallel branches also have an impact on the initial $\frac{di}{dt}$ between a capacitor and the fault because of the inductance in the parallel lines. To provide an example of this, consider the network illustrated in figure 7.10. This network is similar in architecture to that used previously but with converters and resistive components removed to aid illustration.

The simplification of figure 7.10 to only capacitive and inductive components is only valid when analysing the initial network response. For the analysis of initial response, this simplification can be made by assuming the resistive voltage drop is zero and recognising that the voltage across each of the capacitors remains constant at $t = 0$. Constant capacitor voltage implies that an equal opposing voltage is divided between series and parallel line inductances.

To illustrate how this voltage divides between the various line inductances, consider the initial output of capacitor C_F. To simplify analysis the network voltage is set to 500V and line inductance parameters are made equal, i.e. $L_1 = L_2 = L_3 = L_4$. In figure 7.10, there is the series inductance L_1 and the parallel combination of L_2, L_3, L_4 between C_F and the fault. At time $t = 0$ the initial $\frac{di}{dt}$ through the line containing L_1 is equal to

$$\frac{di_{L1}(0)}{dt} = \frac{v_{L1}(0)}{L_1 + L_P}. \tag{7.21}$$

where L_P is equal to the parallel combination of line inductances. The term $v_{L1}(0)$ can be calculated from the superposition of all the series and parallel capacitive

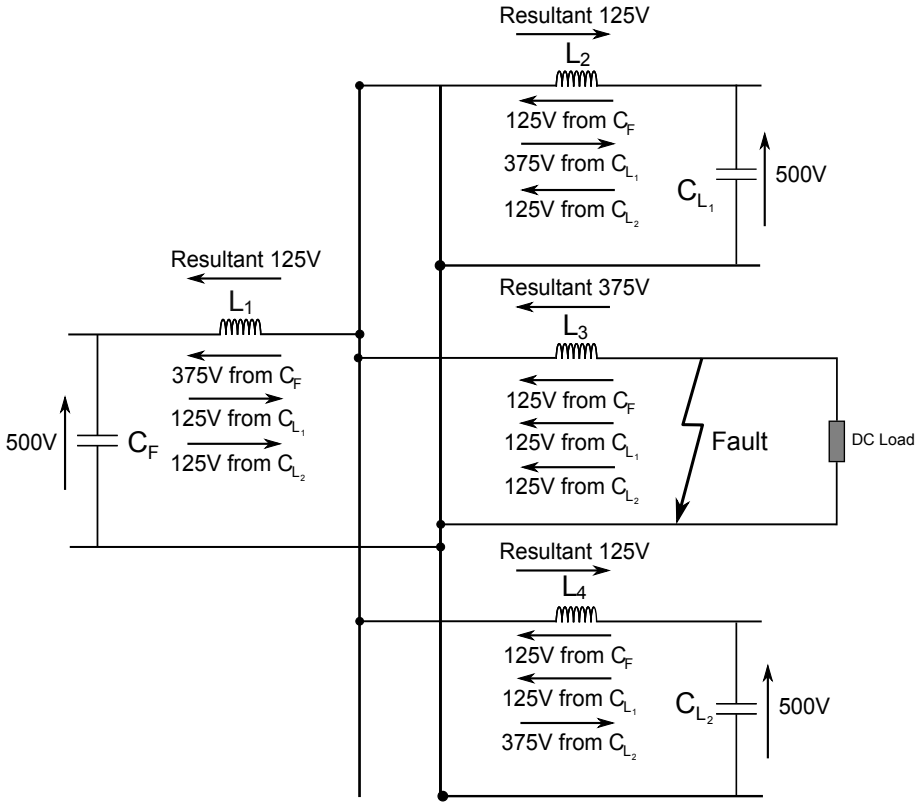

Figure 7.10: Equivalent network with initial voltage response from parallel capacitors with common branch fault

voltage sources thus,

$$v_{L1}(0) = \frac{L_1}{L_1 + L_P} v_{CF}(0). \tag{7.22}$$

As all inductances are assumed equal for this analysis, (7.22) becomes

$$v_{L1}(0) = \frac{3}{4} v_{CF}(0) \tag{7.23}$$

and so substituting $v_{CF}(0) = 500V$

$$v_{L1}(0) = 375V. \tag{7.24}$$

From this, it is also calculable that $v_P(0) = 125V$. Similar calculations can be made for the other capacitive sources in the network and figure 7.10 shows both individual voltage contributions and the resultant voltage on each line inductances.

The outcome of this analysis is to illustrate that when a common branch between multiple sources exists to a fault, the voltage support of the other branches acts to significantly reduce $\frac{di}{dt}$. In terms of using initial $\frac{di}{dt}$ measurements for fault

detection, there are two main points to note from this observation.

The first is that common branch faults cannot be reliably detected in a selective manner, from measurements taken at one common capacitive source, unless the initial conditions in other branches are known. If multiple measurements were instead managed by a central controller it may be possible to identify the fault's location on the common branch, although the merit of installing the additional communication components required to implement this approach would have to be justified against other centrally controlled or communication based protection schemes. It should be noted however that whilst the output of C_F, C_{L1} and C_{L2} may not accurately locate the fault, the existence of a capacitor on the DC load side of the fault in figure 7.10 would enable the fault to be detected as the output of this capacitor could be measured on this branch. Therefore it appears that the fault detection and protection selectivity issues mainly exist for passive loads, however this is an area which requires further study for a range of network architectures.

The second point to consider is how the protection of branches with capacitive sources is affected. If protection is operated on the basis outlined in section 7.2, where protection only operates for faults up to the busbar, then the reduced $\frac{di}{dt}$ for common branch faults can be beneficial. This can be illustrated by comparing (7.21) with the minimum $\frac{di}{dt}$ required to operate protection. Thus,

$$\frac{V_{CF}(t)}{L_1} >> \frac{v_{L1}(0)}{L_1 + L_P}. \tag{7.25}$$

Equation (7.25) suggests that for common branch faults outwith the protected zone, the measured inductance will be significantly greater and hence the possibility of false protection operation will be equally reduced.

Whilst this section highlights the behavioural changes for common branch faults through the assessment of initial circuit behaviour directly after the occurrence of a short circuit, further work is required to fully quantify the impact of parallel sources on the $\frac{di}{dt}$ response over a longer time period. This will provide greater insight into how beneficial this can be for the prevention of false protection operation.

7.4.6 Impact of circuit breaking transients on initial $\frac{di}{dt}$ response

Chapter 3 showed that when a fault is cleared, there is a redistribution of stored energy. This energy redistribution can result in significant current flowing into

the capacitors in the DC network and represents a scenario where high $\frac{di}{dt}$ may exist. This case can be readily analysed in the same way as section 7.4.4 where initial $\frac{di}{dt}$ was found to be (7.20). During circuit breaking however, the initial conditions are likely to be very different, with initial current now being a dominant factor when interrupting large fault currents. If it is assumed that $v_{CF}(0)$ and $v_{CL}(0)$ from (7.20) reduce to zero during the fault (providing the worst case scenario), (7.20) can be simplified to

$$\frac{di_L}{dt}(0) = \frac{-i_L(0)R}{L} \tag{7.26}$$

where $t = 0$ is now representative of the instant in time at which the fault is cleared.

Equation (7.26) provides a means of comparing the initial $\frac{di}{dt}$ due to the clearance of a fault to that necessary to operate the protection scheme. It shows that there is potential for a similar magnitude of initial $\frac{di}{dt}$ necessary to operate the protection scheme to develop, provided the product of $i_L(0)$ and R (which is the sum of R_{Line} and capacitor ESR) is comparable to the nominal system voltage. The $\frac{di}{dt}$ in this case however is negative and so any potential for operation of protection in one part of the network causing incorrect operation elsewhere could easily be prevented by incorporating a directional element to the $\frac{di}{dt}$ measurement.

7.5 Implementation and measurement requirements of an initial $\frac{di}{dt}$ based protection scheme

Analysis so far within this chapter has focused on the initial conditions within the network, however the accuracy of the method also greatly depends on the time at which measurements are made. To illustrate the time critical nature of the method, this section will highlight the limitations of the method in terms of the measurement and parameter uncertainty and measurement time requirements. It will also provide further analysis to help quantify these measurement time requirements depending on the fault detection accuracy desired and assess how the practical measuring methods will effect these requirements.

7.5.1 Initial $\frac{di}{dt}$ fault detection with variable zone coverage due to parameter and measurement uncertainty

The first part of this chapter introduces a potential application for an initial $\frac{di}{dt}$ based protection scheme within an example network section, as shown in figure 7.11. The desired scheme performance is that it will operate for faults up to the busbar but remains insensitive to faults beyond. However, as discussed, due to line parameter and measurement uncertainties, it is extremely difficult to protect an exact length of line [2]. Therefore by attempting to set protection to cover the distance up to the busbar, there is a danger that it will under- or over-reach, and so either leave parts of the line unprotected or potentially operate for faults outwith its intended zone of operation. Traditional distance protection counters this problem by subtracting the maximum likely uncertainty (including line parameters, measurements etc) from the line length to ensure that protection does not overreach [2]. More distant parts of the line are then protected by overlapping zones of protection. Similarly this approach can be taken for the implementation of the initial $\frac{di}{dt}$ based scheme, though initially without the use of additional zones. Its effect is illustrated in figure 7.11.

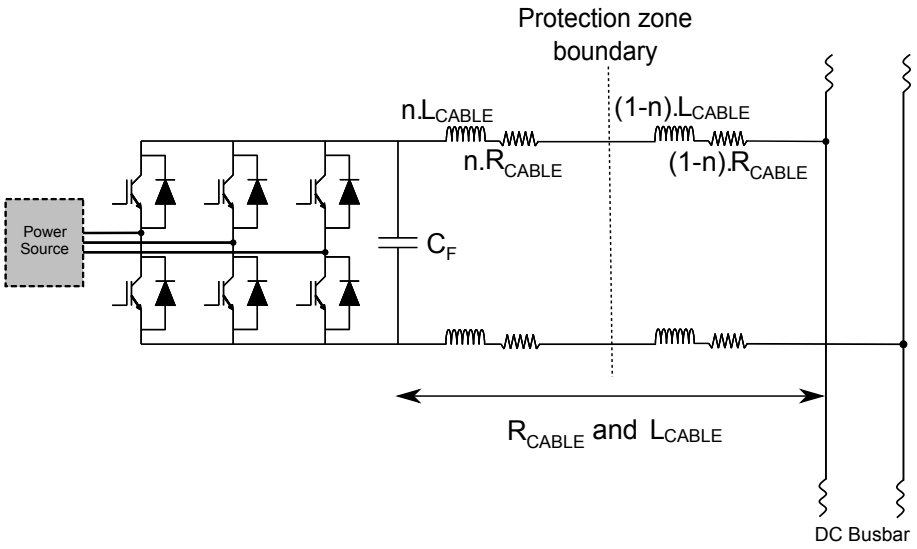

Figure 7.11: Line protection with variable zone coverage

Figure 7.11 shows a length of cable connecting a converter to the DC busbar. The connecting line has been divided up into the protected and unprotected zones, with the multiplying term n representing the proportion of the total line covered by the zone. To meet the performance criteria, n would be set such that the protection system will not overreach in any circumstances. However the time dependent nature of the $\frac{di}{dt}$ response is such that it places an additional constraint

on the coverage area of the protection scheme. The impact of this is described in the following sections.

7.5.2 Variable zone coverage due to exponential decay of $\frac{di}{dt}$

The characteristics of the $\frac{di}{dt}$ response are such that rapid measurement is often essential to ensure an accurate inductance, and hence fault location, is calculated from the $\frac{di}{dt}$ measurement. This requirement is due to the exponential decay of $\frac{di}{dt}$ over time, meaning that a delay in measurement could see a smaller $\frac{di}{dt}$ measured than appeared initially and hence the possible non-detection of a fault condition. The impact of this decay is that for faults close to the zone boundary, and hence operating condition, there is a very small time period where successful detection can be made. For faults on the boundary, only a measurement at $t = 0$ would place the fault inside the zone, so realistically this fault location would not be covered. This means that in addition to the $(1 - n)$ line length in figure 7.11, there will be a further length of line where faults will not be detected, further reducing the coverage of the protection beyond that of the uncertain zone. This additional area of line is not constant but instead is a function of the fault type and time after fault inception within which $\frac{di}{dt}$ is measured. To illustrate this further, and assess the size of this area under different conditions, consider the additional parameters indicated in figure 7.12.

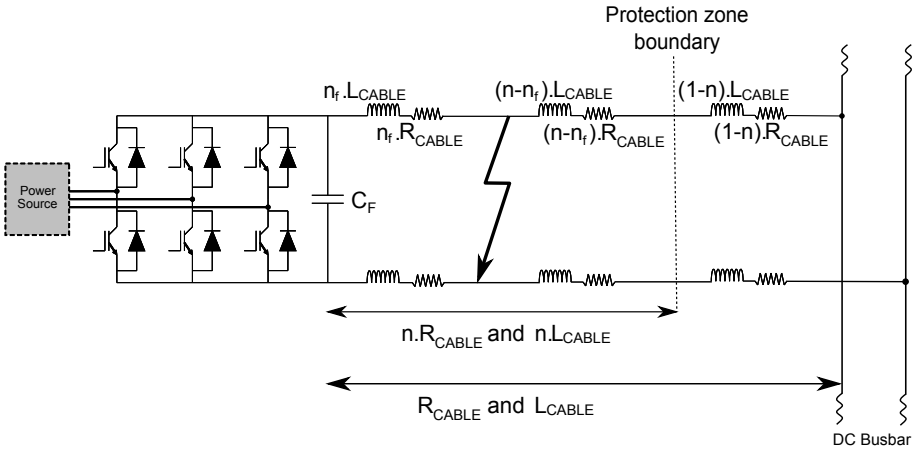

Figure 7.12: Line protection with variable zone coverage and fault detection areas

In figure 7.12 a new factor, n_f, has been introduced, which represents the proportion along the total line length where a fault occurs. The introduction of n_f allows the assessment of the measurement requirements for all possible fault locations along the line, as is described below.

For a fault on the line to be detected using this method, the minimum protection operating condition must be met. The inclusion of the protection zone boundary means that this is now equal to

$$\frac{v_{CF}}{\frac{di}{dt}} = nL_{Cable}. \tag{7.27}$$

If an expression for the derivative fault current, $\frac{di_f}{dt}$, (which is dependent on n_f) is substituted for $\frac{di}{dt}$ in (7.27) (to indicate the measured inductance), then the time at which $L_{meas}(t) = nL_{Cable}$ can be calculated. This is the time within which a measurement must be made for successful fault detection. Note that for this preliminary analysis, v_{CF} will be considered as a constant equal to its initial voltage. Later sections expand on this analysis to assess the impact of utilising continuous time measurements for both voltage and $\frac{di}{dt}$.

Assessing initially for underdamped conditions by substituting the appropriate expression for $\frac{di}{dt}$ into (7.27), the underdamped expression for L_{meas} is

$$L_{meas} = \frac{v_{CF}(0)}{\frac{v_{CF}(0)e^{-\alpha t}}{n_f L_{Cable}}\left[\cos(\omega_d t) - \frac{\alpha}{\omega_d}\sin(\omega_d t)\right]} \tag{7.28}$$

which can be simplified to

$$L_{meas} = \frac{n_f L_{Cable}}{e^{-\alpha t}\left[\cos(\omega_d t) - \frac{\alpha}{\omega_d}\sin(\omega_d t)\right]} \tag{7.29}$$

where α and ω_d are defined as previous and are proportional to n_f. By cancelling the initial voltage terms it means that (7.29) is independent of initial conditions. This has significance as this analysis is now only dependent on circuit parameters, and so any outcomes theoretically apply to all voltage levels (although previous sections have identified that other initial conditions, not considered here, can have a negative impact on fault detection). Equating (7.29) to (7.27) and substituting t_m for t, where t_m is the maximum allowed measurement time to enable fault detection, gives

$$nL_{Cable} = \frac{n_f L_{Cable}}{e^{-\alpha t_m}\left[\cos(\omega_d t_m) - \frac{\alpha}{\omega_d}\sin(\omega_d t_m)\right]}. \tag{7.30}$$

Solving (7.30) for t_m gives an indication of the measurement requirements for a given fault resistance and location or n_f. Whilst some simplification of (7.30) is possible, due to its transcendental nature, iterative techniques are required

to obtain the solution for t_m. As was found in previous chapters, the use of Newton's method is an appropriate numerical method with which to solve this type of equation. The following section will illustrate how Newton's method can be used to establish a fault location versus required measurement time (or $n_f - t_m$) characteristic for fault detection in a network.

7.5.3 Use of Newton's method to define $n_f - t_m$ characteristic for multiple fault conditions

As described in previous chapters, Newton's method is a root-finding algorithm that is often represented by the expression

$$x_{n+1} = x_n - \frac{f(x_n)}{f'(x_n)}. \tag{7.31}$$

Given an appropriate starting value for x, the algorithm works iteratively to find a solution for x where $f(x_n) \approx 0$ and hence $x_{n+1} \approx x_n$. The algorithm can be applied to solve for the time when $L_{meas} = nL_{Cable}$ by setting the function $f(t) = L_{meas} - nL_{Cable}$. The result of this is that any solution for t which gives $f(t) = 0$ will also be the time when $L_{meas} = nL_{Cable}$. This solution is the required measurement time. The Newton's method equation therefore becomes

$$t_{m+1} = t_m - \frac{L_{meas} - nL_{Cable}}{\frac{d(L_{meas} - nL_{Cable})}{dt}} \tag{7.32}$$

where the expression for L_{meas} is dependent on circuit damping conditions, nL_{Cable} is constant and $\frac{d(L_{meas} - nL_{Cable})}{dt}$ is the derivative of these two terms. As nL_{Cable} is constant, the derivative term can be simplified to $\frac{d(L_{meas})}{dt}$. For the full range of fault conditions, both underdamped and overdamped expressions need to be derived for L_{meas} and $\frac{d(L_{meas})}{dt}$, as damping conditions may change with fault location and resistance.

An expression for the underdamped L_{meas} was derived in the previous section and is shown in (7.29). The derivative of (7.29) can be derived by applying the Chain rule, which gives

$$\frac{dL_{meas}}{dt} = \frac{L_f \left[2\alpha \cos(\omega_d t) - \left(\frac{\alpha^2}{\omega_d} - \omega_d \right) \sin(\omega_d t) \right]}{e^{-\alpha t} \left[\cos(\omega_d t) - \frac{\alpha}{\omega_d} \sin(\omega_d t) \right]^2}. \tag{7.33}$$

The overdamped expression for L_{meas}, with previously derived terms substi-

tuted, is

$$L_{meas} = \frac{v_{CF}(0)}{\frac{v_{CF}(0)}{L(s_1-s_2)}\left(s_1 e^{s_1 t} - s_2 e^{s_2 t}\right)} \tag{7.34}$$

where s_1 and s_2 are defined as previous and are dependent on n_f. Cancelling equal terms this becomes

$$L_{meas} = \frac{L(s_1 - s_2)}{\left(s_1 e^{s_1 t} - s_2 e^{s_2 t}\right)}. \tag{7.35}$$

As before, the derivative of (7.35) can be derived using the Chain rule and this is

$$\frac{dL_{meas}}{dt} = \frac{L(s_1 - s_2)\left(s_1^2 e^{s_1 t} - s_2^2 e^{s_2 t}\right)}{\left(s_1 e^{s_1 t} - s_2 e^{s_2 t}\right)^2}. \tag{7.36}$$

For the $n_f - t_m$ characteristic to be plotted, it is required that the appropriate set of equations is used for each value of n_f. Using the line parameters from the example UAV network (as repeated in table 7.2), figure 7.13 plots this characteristic for incrementally increasing n_f and a range of fault resistances. Within the figure the respective fault resistances, from top to bottom, are 0Ω (black line), 0.01Ω (red line), 0.03Ω (purple line), 0.1Ω (lime green line), 0.2Ω (purple dashed line), 0.5Ω (red dashed line) and 1Ω (black dashed line).

Table 7.2: UAV Network Parameters

$Voltage$	P_{GEN}	R_{CABLE}	L_{CABLE}	C_F	$C_F ESR$
270V	20kW	0.801mΩ/m	0.65μH/m	10mF	5mΩ

Figure 7.13 illustrates the impact that measurement times and fault resistances can have on the ability of an initial $\frac{di}{dt}$ based protection scheme to detect faults at different locations along a line. First, it can be seen that fault resistance can have a significant impact on the faults which can be detected for a given measurement time. This is because fault resistance greatly affects the damping levels in the network. For low fault resistance, t_m remains reasonably high for most values of n_f, meaning that the majority of the line could be covered at measurement rate comparable to many standard protection devices [15].

As the fault resistance increases, the required measurement time decreases significantly, with microsecond level measurements required to provide reasonable line coverage in the example shown. Whilst this requirement is in excess of more traditional protection system operation [15], it may be achievable given the use of appropriate measurement and processing technologies as discussed in Chapter 6.

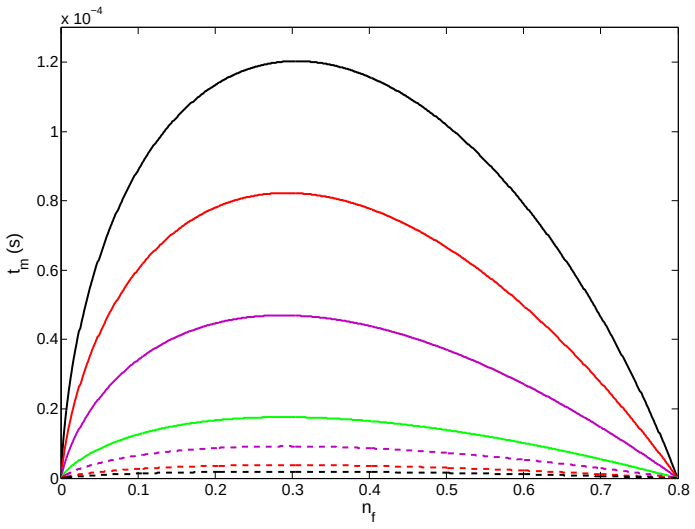

Figure 7.13: n_f line proportion for a range of measurement times (t_m) and fault resistances

The characteristic for each of the fault resistances is parabolic, with t_m peaking midway along the protected zone and reaching a minimum as n_f approaches 0 or 0.8, i.e. either boundary of the protected zone. This t_m minimum as n_f approaches 0.8 is expected given the faults proximity to the zone boundary. As n_f approaches 0, $\frac{di}{dt}$ is initially at a maximum, and so L_{meas} should be easily distinguishable from the protection operating condition and so a t_m minimum is less expected. However under these close up fault conditions, the limited energy in the capacitance can only to sustain the high $\frac{di}{dt}$ for a short period and so t_m reduces accordingly.

It is clear from figure 7.13 that for faults at all locations to be detected, measurement requirements will be dominated by the response to faults close to either the source or protection zone boundary. For these two conditions, t_m can be prohibitively small. However the method of defining the measurement requirements shown in this section is only one measurement approach and not necessarily representative of real world conditions. Therefore the following section considers alternative ways of analysing this problem for different measurement approaches.

7.5.4 Impact of practical measurement conditions

In an operational environment, the means by which voltage and $\frac{di}{dt}$ are measured will alter the inductance measurement. In the implementation of the scheme, there are four main combinations of voltage and $\frac{di}{dt}$ measurements which may be

used to estimate L_{meas}. These are listed below:

1. Assume constant network voltage ($v(0)$) and use an instantaneous $\frac{di}{dt}$ measurement.
2. Use continuous voltage ($v(t)$) and instantaneous $\frac{di}{dt}$ measurements.
3. Assume constant network voltage ($v(0)$) and use an average $\frac{di}{dt}$ measurement.
4. Use continuous voltage ($v(t)$) and average $\frac{di}{dt}$ measurements.

List item 1, which was used for the illustration in the previous section, can be achieved through setting a constant voltage reference equal to the nominal level of the network and taking an instantaneous measurement of $\frac{di}{dt}$. An instantaneous measurement of $\frac{di}{dt}$ would require specific measurement devices to be used, where measured output is proportional to $\frac{di}{dt}$. One example of such a device is a Rogowski coil [16], which typically has the additional benefit of having a high bandwidth, making it more suitable for a highly transient application. Benefits of this approach include: the assumption of constant voltage minimises the number of measurements required to be made and instantaneous $\frac{di}{dt}$ gives a true measurement of $\frac{di}{dt}$ at any point in time, therefore providing an output more closely aligned with circuit theory described so far.

List item 2 can be achieved through the addition of a continuous voltage measurement into the network. This voltage measurement would substitute for $v(0)$ in the calculation of L_{meas}. Benefits of this approach are that calculation of L_{meas} will remain accurate over a larger voltage range. Therefore, in conditions where voltage is lower than the nominal level (e.g. load switch on) the scheme should still operate and where voltage is higher (e.g. load switch off or additional source connection) the potential for false protection operation is reduced.

List item 3 can be achieved through the calculation of $\frac{di}{dt}$ from sampled current measurements, which has the effect of averaging $\frac{di}{dt}$ between two points in time. This approach enables the measurement of $\frac{di}{dt}$ through more conventional means of current measurement.

Finally, list item 4 combines the continuous voltage measurement with average $\frac{di}{dt}$, providing more accurate tracking of voltage with conventional current measurement.

The following subsections derive alternative expressions to enable the varying measurement requirements of these approaches to be assessed. As before,

measurement requirements are judged on the ability to discriminate fault location within the specific region identified in figure 7.12. Comparison is then made between the requirements for discrimination and those stipulated in previous chapters for effective protection operation.

Impact of continuous voltage measurement compared to initial voltage

To quantify the impact of including a continuous voltage measurement rather than $v_{CF}(0)$, $v_{CF}(t)$ is substituted for $v_{CF}(0)$ in the expression for L_{meas}, where $v_{CF}(t)$ is the continuous voltage term derived in Chapter 3. The expression for L_{meas} therefore becomes

$$L_{meas_{v_t}} = \frac{v_{CF}(t)}{\frac{di_f}{dt}}. \tag{7.37}$$

For underdamped conditions, substituting for $v_{CF}(t)$ and $\frac{di_f}{dt}$, (7.37) becomes

$$L_{meas_{v_t}} = \frac{v_{CF}(0)e^{-\alpha t}\left[\cos(\omega_d t) + \frac{\alpha}{\omega_d}\sin(\omega_d t)\right]}{\frac{v_{CF}(0)e^{-\alpha t}}{L\omega_d}\left[\omega_d \cos(\omega_d t) - \alpha \sin(\omega_d t)\right]}. \tag{7.38}$$

By cancelling equal terms and rearranging, (7.38) simplifies to

$$L_{meas_{v_t}} = \frac{L_f\left[\omega_d \cos(\omega_d t) + \alpha \sin(\omega_d t)\right]}{\left[\omega_d \cos(\omega_d t) - \alpha \sin(\omega_d t)\right]}. \tag{7.39}$$

To solve (7.39) for the required measurement time using Newton's method as previous, its derivative is required to be calculated. Applying the quotient rule, the derivative of (7.39) can be derived to be

$$\frac{dL_{meas_{v_t}}}{dt} = \frac{\begin{array}{c} L_f\left[(\omega_d \cos(\omega_d t) - \alpha \sin(\omega_d t))(-\omega_d^2 \sin(\omega_d t) + \omega_d \alpha \cos(\omega_d t))\right] \\ -(\omega_d \cos(\omega_d t) + \alpha \sin(\omega_d t))(\omega_d^2 \sin(\omega_d t) + \omega_d \alpha \cos(\omega_d t)) \end{array}}{\left[\omega_d \cos(\omega_d t) - \alpha \sin(\omega_d t)\right]^2}. \tag{7.40}$$

Multiplying out and applying appropriate trigonometric identities, (7.40) becomes

$$\frac{dL_{meas_{v_t}}}{dt} = \frac{L_f\left(\alpha {\omega_d}^2 + \omega_d \alpha^2\right)}{\left[\omega_d \cos(\omega_d t) - \alpha \sin(\omega_d t)\right]^2}. \tag{7.41}$$

The overdamped expressions can be derived in a similar manner. Substituting

overdamped expressions for $v_{CF}(t)$ and $\frac{di}{dt}$ into (7.37) gives

$$L_{meas_{v_t}} = \frac{\frac{v_{CF}(0){\omega_0}^2}{(s_1-s_2)}\left(\frac{e^{s_2 t}}{s_2} - \frac{e^{s_1 t}}{s_1}\right)}{\frac{v_{CF}(0)}{L(s_1-s_2)}\left(s_1 e^{s_1 t} - s_2 e^{s_2 t}\right)}. \tag{7.42}$$

Cancelling equal terms and simplifying, (7.42) becomes

$$L_{meas_{v_t}} = \frac{\frac{e^{s_2 t}}{s_2} - \frac{e^{s_1 t}}{s_1}}{C_F\left(s_1 e^{s_1 t} - s_2 e^{s_2 t}\right)}. \tag{7.43}$$

Taking the derivative of (7.43) (by applying the quotient rule as before), the derivative overdamped expression for L_{meas} can be derived as

$$\frac{dL_{meas_{v_t}}}{dt} = \frac{e^{(s_1+s_2)t}\left(s_1 - s_2 - \frac{s_2^2}{s_1} - \frac{s_1^2}{s_2}\right)}{C_F\left(s_1 e^{s_1 t} - s_2 e^{s_2 t}\right)^2}. \tag{7.44}$$

From the analysis of the new expressions for L_{meas} (equations (7.39) and (7.43)), it can be deduced that as both the numerator and denominator have time varying terms, a change in one term will be reflected in the other. This characteristic could potentially increase t_m (extending allowed measurement time) compared to the case in the previous section. For example, when a fault occurs, the scheme would no longer divide a fixed voltage by a decreasing $\frac{di}{dt}$. Instead both terms will decrease with time. Therefore L_{meas} will resemble its initial state for longer, giving more time to make measurements. This is reflected in the plots shown in figure 7.14 which illustrates the $n_f - t_m$ characteristic for the measurement approach in the example network. Within the figure the respective fault resistances, from top to bottom, are 0Ω (blue line), 0.01Ω (red line), 0.03Ω (purple line), 0.1Ω (lime green line), 0.2Ω (purple dashed line), 0.5Ω (red dashed line) and 1Ω (black dashed line).

Figure 7.14 shows that, compared to figure 7.13, the maximum t_m for each of the fault conditions has increased, as the analysis above suggested would be the case. However the impact on the actual measurement requirement, i.e. the minimum t_m for successful fault detection throughout the line, is unclear. This may still be at a similar level to before due to the limitations of the method at the extremes of the protection zone.

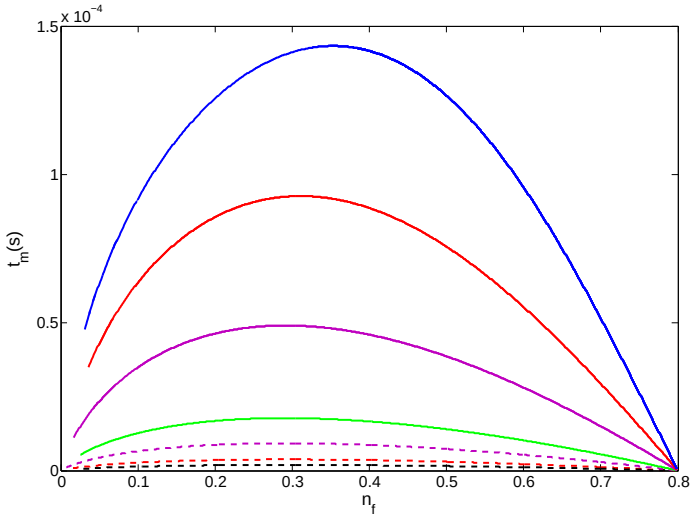

Figure 7.14: n_f line proportion for a range of measurement times (t_m) and fault resistances with continuous voltage function considered

Impact of average $\frac{di}{dt}$ measurement compared to instantaneous $\frac{di}{dt}$

This section considers the impact of using discrete current measurements to calculate $\frac{di}{dt}$, and hence averaging $\frac{di}{dt}$ between the two points in time, as opposed to taking an instantaneous measurement of $\frac{di}{dt}$. For the purposes of this analysis it is presumed that the first current measurement is taken at the time of fault inception, and so t_m is calculated as the time at which the next current measurement needs to be made. The result of this is that the analysis calculates the strictest measurement requirements when using average $\frac{di}{dt}$ measurements as the smallest window of opportunity is provided to take the second current measurement. Using the averaged $\frac{di}{dt}$, L_{meas} is made equal to

$$L_{meas\,\frac{di_{ave}}{dt}} = \frac{v_{CF}(0)}{\frac{di_{ave}}{dt}}. \tag{7.45}$$

Within (7.45), the average $\frac{di}{dt}$ can be calculated from

$$\frac{di_{ave}}{dt} = \frac{i_L(t_2) - i_L(t_1)}{t_2 - t_1} \tag{7.46}$$

where t_1 and t_2 are two current measurement times and $t_2 > t_1$. If, for the purpose of this analysis, it is assumed that the initial (pre-fault) current $i(t_1) = 0$ and $t_1 = 0$ (as is the case throughout this section) and that $t_2 = t$, (7.46) reduces to

$$\frac{di_{ave}}{dt} = \frac{i_L(t)}{t}. \tag{7.47}$$

Starting with the underdamped case, substituting $i_L(t)$ for the previously

derived underdamped current expression, (7.47) becomes

$$\frac{di_{ave}}{dt} = \frac{v_{CF}(0)e^{-\alpha t}\sin(\omega_d t)}{tL_f\omega_d}. \tag{7.48}$$

Now substituting (7.48) into (7.45), the expression for L_{meas} becomes

$$L_{meas_{\frac{di_{ave}}{dt}}} = \frac{v_{CF}(0)}{\frac{v_{CF}(0)e^{-\alpha t}\sin(\omega_d t)}{tL_f\omega_d}}. \tag{7.49}$$

Cancelling equal terms and rearranging this equals

$$L_{meas_{\frac{di_{ave}}{dt}}} = \frac{tL_f\omega_d}{e^{-\alpha t}\sin(\omega_d t)}. \tag{7.50}$$

As previous, the derivative of (7.50) is required to allow it to be solved using Newton's method. Applying the quotient rule to the full expression, and the product rule to the denominator, derivative of (7.50) can be derived as

$$\frac{dL_{meas_{\frac{di_{ave}}{dt}}}}{dt} = \frac{L_f\omega_d e^{-\alpha t}\left\{\sin(\omega_d t) - t\left[-\alpha\sin(\omega_d t) + \omega_d\cos(\omega_d t)\right]\right\}}{e^{-2\alpha t}\sin^2(\omega_d t)}. \tag{7.51}$$

Rearranging and cancelling equal terms, (7.51) reduces to

$$\frac{dL_{meas_{\frac{di_{ave}}{dt}}}}{dt} = \frac{L_f\omega_d\left\{\sin(\omega_d t)\left[1 + t\alpha\right] - t\omega_d\cos(\omega_d t)\right\}}{e^{-\alpha t}\sin^2(\omega_d t)}. \tag{7.52}$$

For the overdamped case, substitution of the appropriate expression for current into (7.47) gives

$$\frac{di_{ave}}{dt} = \frac{v_{CF}(0)\left(e^{s_1 t} - e^{s_2 t}\right)}{tL(s_1 - s_2)}. \tag{7.53}$$

Substituting (7.53) into (7.45) to get the overdamped expression for L_{meas} results in

$$L_{meas_{\frac{di_{ave}}{dt}}} = \frac{v_{CF}(0)}{\frac{v_{CF}(0)(e^{s_1 t} - e^{s_2 t})}{tL(s_1 - s_2)}} \tag{7.54}$$

and cancelling equal terms and rearranging this equals

$$L_{meas_{\frac{di_{ave}}{dt}}} = \frac{tL(s_1 - s_2)}{\left(e^{s_1 t} - e^{s_2 t}\right)}. \tag{7.55}$$

The derivative of (7.55) can be found by applying the quotient rule as appro-

priate, and this equal to

$$\frac{dL_{meas\,\frac{di_{ave}}{dt}}}{dt} = \frac{L_f(s_1 - s_2)\left(e^{s_1 t}(1 - s_1 t) + e^{s_2 t}(-1 + s_2 t)\right)}{\left(e^{s_1 t} - e^{s_2 t}\right)^2}. \tag{7.56}$$

The difference in response of the above functions compared to previous cases is most clearly visualised (prior to plotting) by considering the difference in behaviour between the average and instantaneous $\frac{di}{dt}$ functions. As $\frac{di_{ave}}{dt}$ measures rate of current change over the period between two current measurements it will decay at a slower rate than instantaneous $\frac{di}{dt}$. For example, when current is at its peak, instantaneous $\frac{di}{dt} = 0$, whereas for a measurement at that time $\frac{di_{ave}}{dt}$ will equal the difference between peak and initial currents divided by the time to peak. This slower decay would suggest that t_m would generally be greater when using $\frac{di_{ave}}{dt}$ measurements but more importantly, $\frac{di_{ave}}{dt}$ would be less sensitive to the instantaneous decay in $\frac{di}{dt}$ for close up faults. Therefore the excessive measurement requirements will be reduced for these close up fault conditions.

The required measurement time t_m for the full range of fault positions along the line can again be found by applying Newton's method using the appropriate underdamped and overdamped expressions above. The output of this analysis for the example network is shown in figure 7.15. Within the figure the respective fault resistances, from top to bottom, are 0Ω (black line), 0.01Ω (red line), 0.03Ω (purple line), 0.1Ω (lime green line), 0.2Ω (purple dashed line), 0.5Ω (red dashed line) and 1Ω (black dashed line).

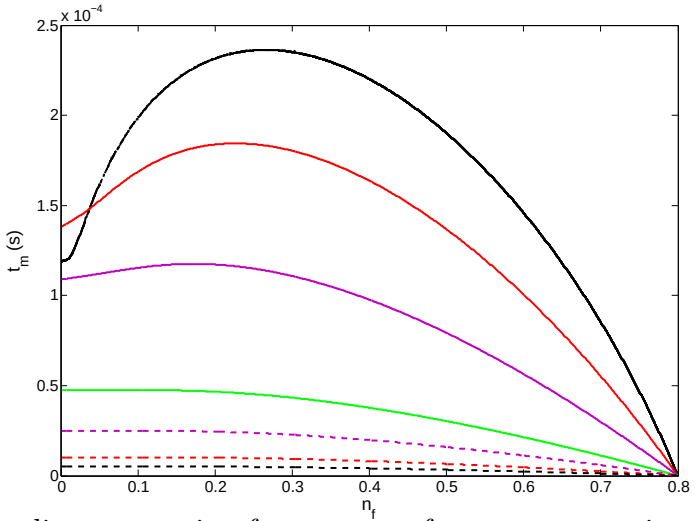

Figure 7.15: n_f line proportion for a range of measurement times (t_m) and fault resistances with average $\frac{di}{dt}$ function considered

Comparing figure 7.15 with previous results, there are two key points to note. First, the use of $\frac{di_{ave}}{dt}$ has significantly increased the maximum t_m for each of the

fault conditions. Second, and more significantly, the extremely high requirement for the discrimination of nearby faults has been removed, as was anticipated from the analysis. Therefore, only the response to faults close to the protection zone boundary continues to inhibit the use of initial $\frac{di}{dt}$ measurements for fault discrimination.

One unusual result within figure 7.15 is the crossover between the respective 0Ω and 0.01Ω characteristics. The plots show that t_m is smaller for a very close up 0Ω fault compared to the 0.01Ω fault, a characteristic which opposes the usual damping response where $\frac{di}{dt}$ decays (and hence L_{meas} increases) at a greater rate with higher resistance. The source of this unusual behaviour can be seen by plotting the L_{meas} function (equation (7.50) or (7.55) where appropriate) for these close up faults. This is illustrated in figure 7.16 which both compares the 0Ω and 0.01Ω characteristics (left plot) as well as illustrating the 0Ω characteristic over a longer time period (right plot).

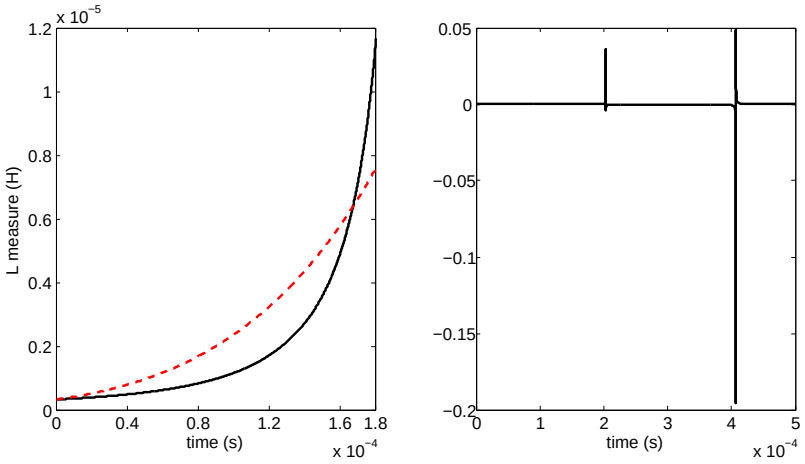

Figure 7.16: Measured inductance over time using the average $\frac{di}{dt}$ function for 0Ω (black line) and 0.01Ω (red dotted line) fault resistances with a fault location of $n_f = 0.05$

Within figure 7.16, the 0Ω characteristic is underdamped and the 0.01Ω characteristic is overdamped. This difference is the key factor which introduces the crossover in required measurement time. Figure 7.16 shows that the 0.01Ω L_{meas} characteristic increases at a reasonably steady rate whereas the 0Ω characteristic increases at a much larger gradient beyond around $1.4 \times 10^{-4} s$. This behaviour is in accordance with the cosecant $(\frac{1}{sin(\omega_d t)})$ within the underdamped function (7.50), where the response tends towards $\pm\infty$ as $\omega_d t$ approaches 0 or π.

This is more clearly illustrated in the right hand plot of figure 7.16 where

the measured inductance can be seen to spike positively and negatively beyond a certain time. The point to note from this is that measurements should be taken prior to any unstable points in the function. This however should be inherently achieved through the smaller t_m associated with the detection and discrimination of higher resistance faults.

Impact of both average $\frac{di}{dt}$ and continuous voltage measurement

The final combination of measurements which will be analysed is the use of both an average $\frac{di}{dt}$ and a continuous voltage measurement to calculate L_{meas}. For this case, the expression for L_{meas} is

$$L_{meas_{\frac{di_{ave}}{dt}v_t}} = \frac{v_{CF}(t)}{\frac{di_{ave}}{dt}}. \tag{7.57}$$

Considering the underdamped case in the first instance, substituting the underdamped expressions for $v_{CF}(t)$ and $\frac{di_{ave}}{dt}$ gives

$$L_{meas_{\frac{di_{ave}}{dt}v_t}} = \frac{v_{CF}(0)e^{-\alpha t}\left[\cos(\omega_d t) + \frac{\alpha}{\omega_d}\sin(\omega_d t)\right]}{\frac{v_{CF}(0)e^{-\alpha t}\sin(\omega_d t)}{tL_f\omega_d}} \tag{7.58}$$

and cancelling equal terms and rearranging this equals

$$L_{meas_{\frac{di_{ave}}{dt}v_t}} = t\left(L_f\omega_d\cot(\omega_d t) + \frac{R_f}{2}\right). \tag{7.59}$$

The derivative of (7.59) is

$$\frac{dL_{meas_{\frac{di_{ave}}{dt}v_t}}}{dt} = \frac{R_f}{2} + L_f\omega_d\left(\cot(\omega_d t) - \frac{t\omega_d}{\sin^2(\omega_d t)}\right). \tag{7.60}$$

For the overdamped case, substituting the appropriate expressions into (7.57) and simplifying gives

$$L_{meas_{\frac{di_{ave}}{dt}v_t}} = \frac{t\left(\frac{e^{s_2 t}}{s_2} - \frac{e^{s_1 t}}{s_1}\right)}{C_F\left(e^{s_1 t} - e^{s_2 t}\right)}. \tag{7.61}$$

Taking the derivative of (7.61) and simplifying gives

$$\frac{dL_{meas_{\frac{di_{ave}}{dt}v_t}}}{dt} = \frac{\begin{array}{r}\left(e^{s_1 t} - e^{s_2 t}\right)\left[\frac{e^{s_2 t}}{s_2} - \frac{e^{s_1 t}}{s_1} + t(e^{s_2 t} - e^{s_1 t})\right] \\ -t\left(\frac{e^{s_2 t}}{s_2} - \frac{e^{s_1 t}}{s_1}\right)\left(s_2 e^{s_2 t - s_1 e^{s_1 t}}\right)\end{array}}{C_F\left(e^{s_1 t} - e^{s_2 t}\right)^2}, \tag{7.62}$$

which can be simplified to

$$\frac{dL_{meas}{}_{\frac{di_{ave}}{dt}v_t}}{dt} = \frac{-\frac{e^{2s_1t}}{s_1} - \frac{e^{2s_2t}}{s_2} - e^{s_1+s_2t}\left[\frac{1}{s_1} + \frac{1}{s_2} + t\left(2 - \frac{s_2}{s_1} - \frac{s_1}{s_2}\right)\right]}{C_F\left(e^{s_1t} - e^{s_2t}\right)^2}. \tag{7.63}$$

Inspection of equations (7.59) and (7.61) shows that they are equal to the expression previously derived for transient impedance in Chapter 5 multiplied by time. Therefore as with the impedance characteristic, there is the potential for large positive and negative spikes in the calculation of L_{meas}, which would cause problems for successful fault discrimination. These spikes are mainly a result of voltage reaching zero before $\frac{di_{ave}}{dt}$, which occurs because of the way $\frac{di_{ave}}{dt}$ is now calculated. The impact of this on the analysis can be seen from figures 7.17 and 7.18, which illustrate the $n_f - t_m$ characteristic for the combined continuous voltage and average $\frac{di}{dt}$ measurements on the example UAV network. Within figure 7.17 the respective fault resistances, from top to bottom, are 0Ω (black line), 0.01Ω (red line), 0.03Ω (purple line), 0.1Ω (lime green line), 0.2Ω (purple dashed line), 0.5Ω (red dashed line) and 1Ω (black dashed line). In figure 7.18, plots for 0Ω and 0.01Ω faults are removed for clarity.

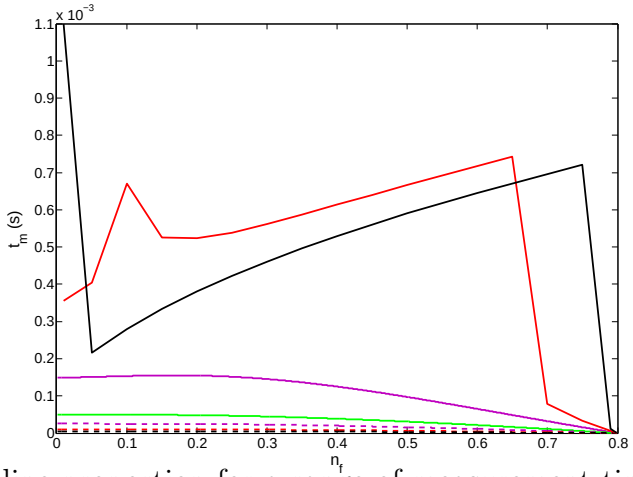

Figure 7.17: n_f line proportion for a range of measurement times (t_m) and fault resistances with both average $\frac{di}{dt}$ and continuous voltage functions considered and including manual measurements

Figure 7.17 illustrates the curves for the combined continuous voltage and average $\frac{di}{dt}$ measurements, with figure 7.18 more clearly showing the requirements for the higher impedance faults. For the zero and 0.01Ω faults, similar curves to previous are not achievable using Newton's method, and so manual measurements (using plots of the function L_{meas} at different fault locations) have been plotted with fewer data points. To show why the behaviour is different for these cases, consider the plots in figure 7.19, which show the behaviour of L_{meas}, voltage and

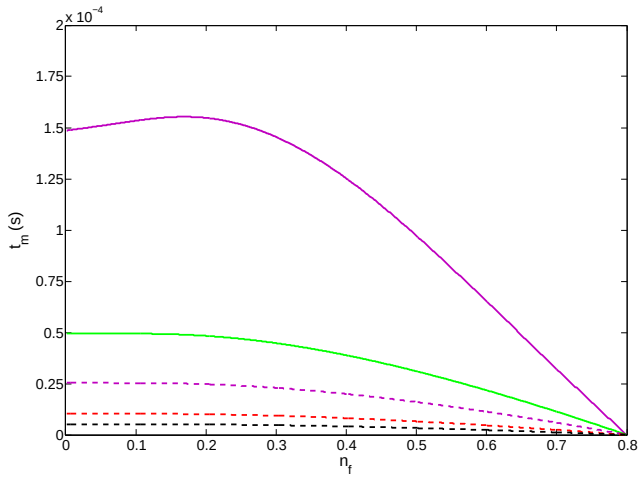

Figure 7.18: n_f line proportion for a range of measurement times (t_m) and fault resistances with both average $\frac{di}{dt}$ and continuous voltage functions considered, excluding manual measurements

$\frac{di_{ave}}{dt}$ for an example fault condition where fault resistance is 0Ω and $n_f = 0.4$.

Figure 7.19 (a) shows that after the fault occurs L_{meas} begins to increase, as is usually the case due to a decay in $\frac{di}{dt}$, but then decays before reaching the threshold ($nL_{Cable} = 5.2\mu H$). As the protection threshold is not exceeded initially, a solution for t_m where $L_{meas} = nL_{Cable}$ will not exist until much later (see figure 7.19 (d)). This is the cause of the erratic behaviour of the $n_f - t_m$ characteristic for certain fault types in figure 7.17. Figure 7.19 (b) and (c) highlight that L_{meas} behaves in this manner for the lower impedance fault conditions because voltage is decaying at a faster rate than $\frac{di_{ave}}{dt}$ as t_m increases.

A further consequence of this decaying inductance measurement is that faults outwith the protection zone may appear within it, potentially causing maloperation of protection. This issue is illustrated in figure 7.20, which shows L_{meas} for a 0Ω fault when $n_f = 0.9$ (i.e. outside the protection zone).

Figures 7.19 and 7.20 therefore indicate that to ensure L_{meas} is correctly represented, there is a maximum level at which t_m must be set. This would be set such that $\frac{di_{ave}}{dt}$ more closely tracks the instantaneous $\frac{di}{dt}$ and decays at a similar (or faster) rate to the voltage under low impedance fault conditions. To prevent the decay in L_{meas}, t_m would therefore be set to at least equal the initial peak in L_{meas}, which in figure 7.19 (a) is at around $50\mu s$. However comparison of this time with figures 7.17 and 7.18 suggests that if discrimination of higher resistance faults is to be achieved, then t_m should already be sufficiently small to prevent this problem occurring.

In spite of these additional considerations, figures 7.17 and 7.18 do show that

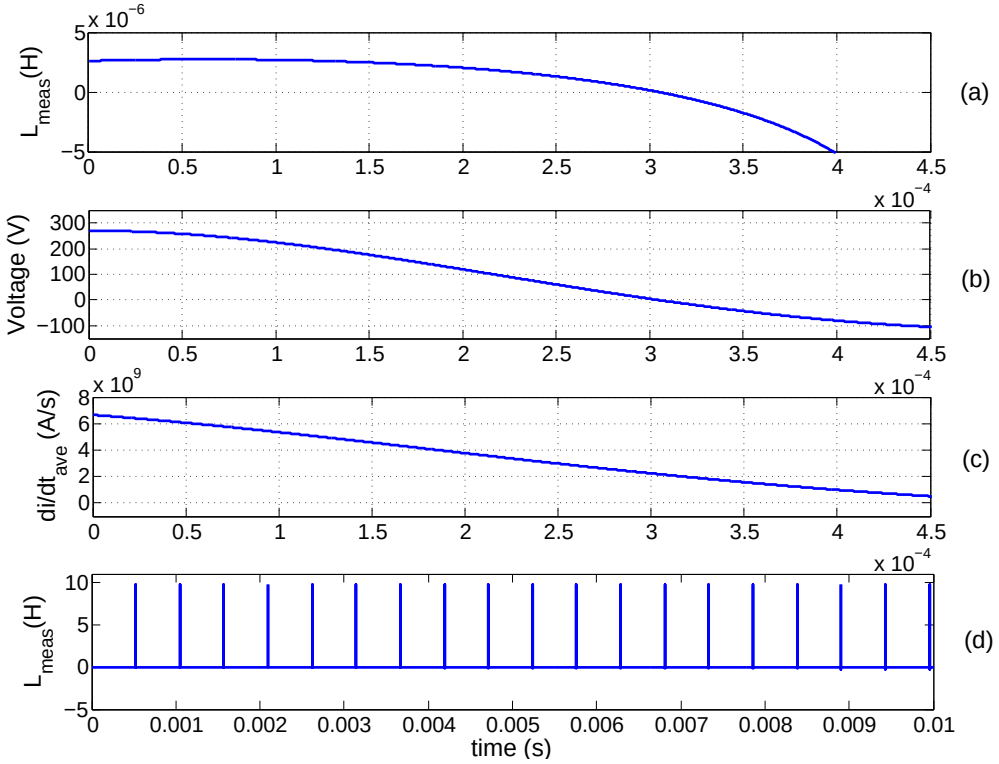

Figure 7.19: Calculated L_{meas}, voltage and $\frac{di_{ave}}{dt}$ response for 0Ω fault at $n_f = 0.4$

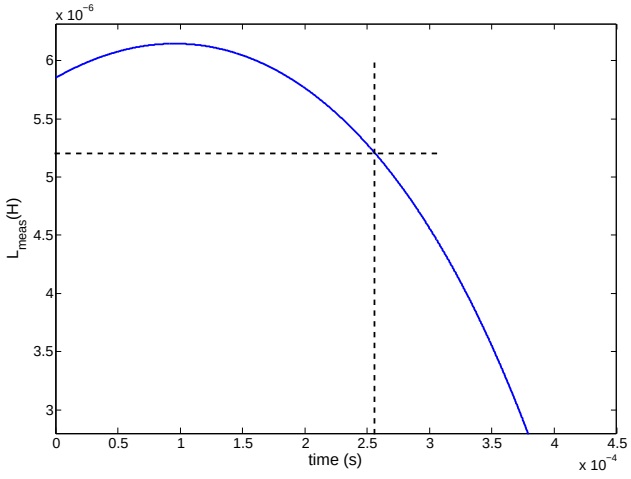

Figure 7.20: Calculated L_{meas} response for 0Ω fault outwith protected zone ($n_f = 0.9$)

for the other fault conditions illustrated, there is a reasonable increase in the maximum and minimum measurement time t_m for most values of n_f, except those close to the distant zone boundary $n_f \approx 0.8$. This suggests that, in terms of minimising measurement requirements (or maximising measurement accuracy for a given t_m), this measurement approach is the most favourable.

To discuss how this analysis can be considered within a wider context, the following section will illustrate how the measurement characteristics can be compared to other operating criteria.

7.5.5 Comparison of measurement requirements for discrimination and other protection operation criteria

Whilst it is of great importance to ensure discriminative operation of a protection scheme, there are other drivers which will influence the required measurement and operating time. Examples of these were described in Chapter 4, where methods were presented to determine the time at which the response reached specific voltage and current thresholds. To identify which of these factors dominate the measurement requirements within a network, the following subsections compare the example $n_f - t_m$ characteristics derived within this chapter to those current and voltage thresholds.

Comparison of measurement requirements for discrimination and voltage thresholds

Chapter 4 showed that to assess the time at which a particular voltage (V_p) occurs, the Newton's method equation is

$$t_{m+1} = t_m - \frac{v_{CF}(t) - V_p}{\frac{dv_{CF}}{dt}} \tag{7.64}$$

Equation (7.64) enables the comparison of the time these voltage thresholds occur with t_m for fault discrimination. The comparison can simply be achieved through plotting the $n_f - t_m$ characteristic for both voltage and fault discrimination on the same graph. This is illustrated for the 0Ω and $10m\Omega$ faults, using the constant voltage and average $\frac{di}{dt}$ to find L_{meas} (since the continuous voltage and average $\frac{di}{dt}$ produces erratic behaviour for these resistances), in figures 7.21 and 7.22 respectively. These two fault conditions are illustrated as they are the cases where voltage decays most rapidly. Within both figures the voltage thresholds, from top to bottom, are: $0V$ (dashed dark green line), $10V$ (dashed purple line), $50V$

(dashed lime green line), $100V$ (dashed blue line).

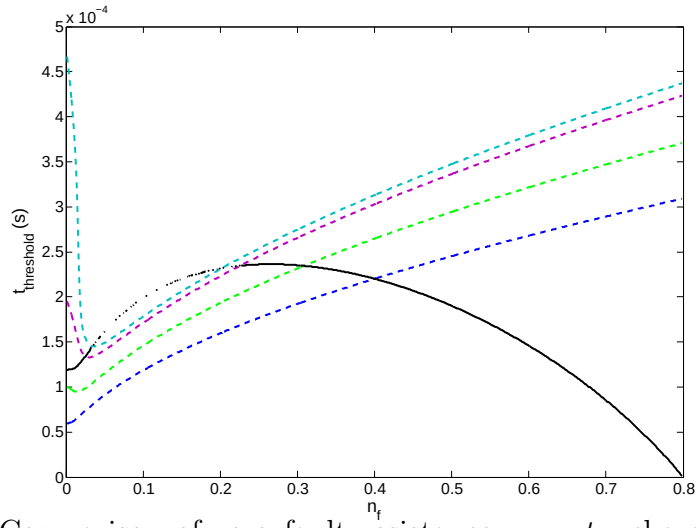

Figure 7.21: Comparison of zero fault resistance $n_f - t_m$ characteristic (black line) to a range of lower voltage thresholds

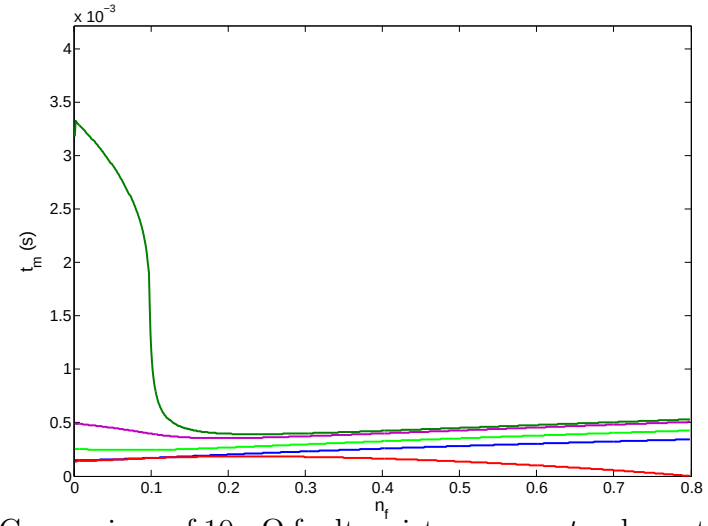

Figure 7.22: Comparison of $10m\Omega$ fault resistance $n_f - t_m$ characteristic (red line) to a range of lower voltage thresholds

Figures 7.21 and 7.22 help illustrate how the required measurement time can be based on multiple criteria, in this case fault discrimination and an undervoltage threshold. For the plots shown, t_m is simply determined by the lesser time of the two criteria. In both figures it can be seen that for faults close to the protection zone boundary, the dominant factor is the L_{meas} response and the need to quickly measure to discriminate fault location. As n_f decreases and the fault moves closer to the source, the voltage thresholds begin to dominate the measurement requirements. This is because of the more rapid decay in voltage as the cable length shortens. However contrary to this, both figures 7.21 and 7.22 show an increase in t_m as n_f approaches zero. This is result of a weakness in the Newton's

method algorithm employed, rather than any inconsistent circuit behaviour. In each case the solver misses the initial voltage threshold and instead presents the solution for the next point in the oscillating voltage waveform that the threshold is reached. This results in a larger t_m. Given that these errors only occur for extremely close up fault cases ($< 1m$ in length), their practical impact on the results is minor.

If attempting to coordinate protection with an undervoltage threshold, as was done in Chapter 5, then the above plots highlight that, whilst the measurement time to discriminate fault location from L_{meas} is often small compared to more traditional protection techniques, the typical response of the network is such that faster measurement is already a requirement for desired protection performance. Whilst this section has only illustrated the voltage thresholds for the 0Ω and $10m\Omega$ faults, comparison to the other fault conditions can be easily achieved using the methods outlined above. However for higher resistance faults it is likely that requirements for discrimination will dominate the value of t_m.

Comparison of measurement requirements for discrimination and current threshold

In a similar manner to the previous section, the measurement requirement for fault discrimination can be compared to the time of occurrence for a range of fault current thresholds. Chapter 4 showed that to assess t_m for a particular current threshold, labelled I_p, the Newton's method equation is

$$t_{m+1} = t_m - \frac{i_L(t) - I_p}{\frac{di_L}{dt}}. \tag{7.65}$$

Comparisons between the $n_f - t_m$ characteristics for the 0Ω and $10m\Omega$ faults for average $\frac{di}{dt}$ measurements and this current threshold analysis are illustrated in figures 7.23 and 7.24 respectively. These fault conditions are again chosen as they represent the cases where current magnitude will be greatest. Within both figures the current thresholds, from top to bottom, are: $8kA$ (green line), $7kA$ (blue line), $5kA$ (lime green line), $3kA$ (dashed green line), $1kA$ (dashed lime green line), $0.5kA$ (blue line).

Figures 7.23 and 7.24 illustrate that for the 0Ω and $10m\Omega$ faults, the dominant factor in the measurement time requirement is mainly the current threshold. This indicates that for the protection system to operate to an upper current threshold, the measurement requirements to achieve fault discrimination are not a limiting factor in the application in this type of protection system for lower resistance

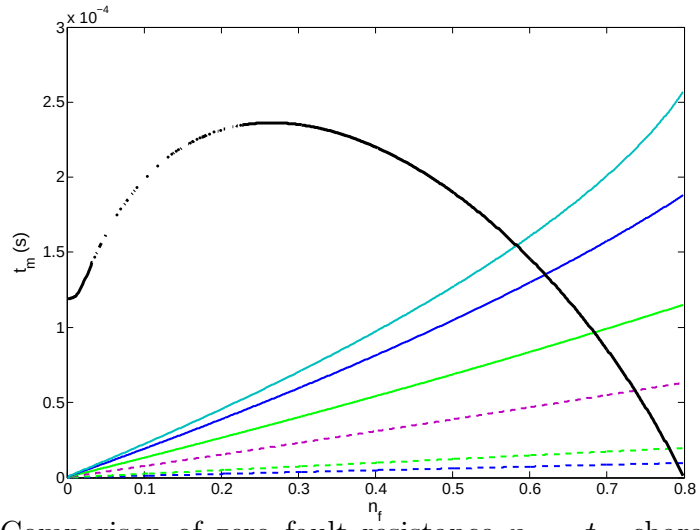

Figure 7.23: Comparison of zero fault resistance $n_f - t_m$ characteristic (black line) to a range of upper current thresholds

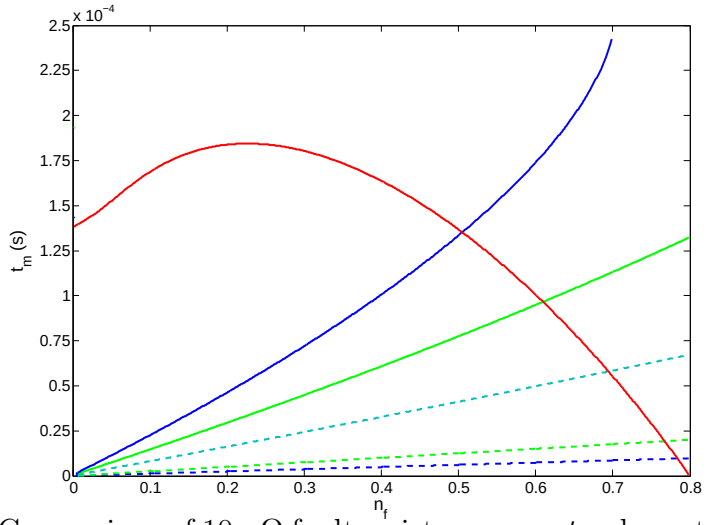

Figure 7.24: Comparison of $10m\Omega$ fault resistance $n_f - t_m$ characteristic (red line) to a range of upper current thresholds

fault conditions. Figures 7.23 and 7.24 do however show that when comparing the current response to a threshold level, the measurement requirements significantly increase as the fault moves closer to the capacitive source. For these cases, sufficient operation of protection remains a challenge and additional protective elements may need to included within the network. This aspect is discussed in more detail within the next section.

A similar comparison can be made for the higher resistance faults in the same manner as described above. However as fault resistance increases, the rate of current rise will decrease and conversely the measurement requirements for fault discrimination will increase. Therefore measurement requirements will tend to be dominated more by the requirement for fault discrimination. However, to help assess the operating condition which has the highest measurement requirements, it is worthwhile comparing the $n_f - t_m$ characteristic for fault discrimination of the 1Ω fault (or alternatively the highest resistance of interest) to the current thresholds for the 0Ω fault, as these represent the two strictest measurement requirements. This comparison is illustrated in figure 7.25.

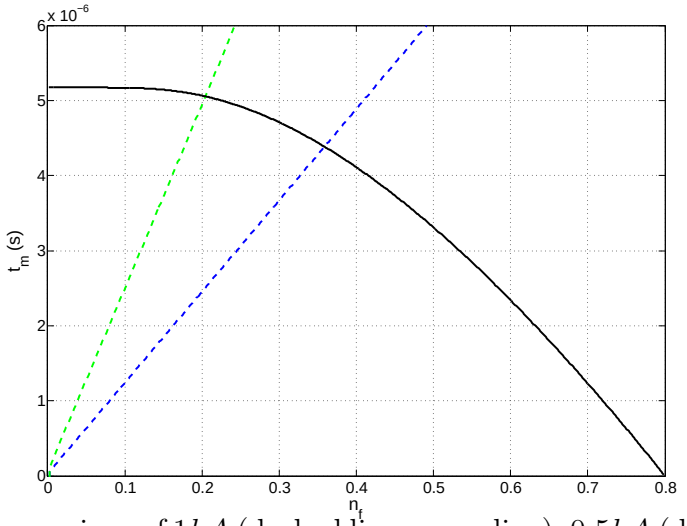

Figure 7.25: Comparison of $1kA$ (dashed lime green line), $0.5kA$ (dashed blue line) current threshold for 0Ω fault with $n_f - t_m$ characteristic for fault discrimination of the 1Ω fault (black solid line)

Figure 7.25 in particular highlights that the time at which the response to the close up 0Ω fault reaches the two current thresholds is comparable to that of the required measurement time for detection of a 1Ω fault near to the distant protection zone boundary. Therefore the measurement requirements to achieve accurate discrimination are similar to those needed to operate before either current threshold. This means that, for this case at least, no significant additional

measurement capability is required to implement a protection scheme using initial $\frac{di}{dt}$ than should already exist. Therefore the measurement requirements to discriminate fault location using initial $\frac{di}{dt}$ measurements should not be a limiting factor in its implementation.

7.5.6 Discussion of results

The above sections describe how the time criticality for $\frac{di}{dt}$ measurements potentially impacts upon the accuracy of the initial $\frac{di}{dt}$ fault detection method for a range of fault locations and resistances through the use of detailed analysis of a number of measurement approaches. It has been demonstrated that although measurement requirements for the method to correctly discriminate fault location are generally high in comparison to standard protection practices, they are often not the dominant factor when compared to relevant voltage and current thresholds. This suggests that in order for protection to operate in a sufficient time frame to respond to these voltage and current thresholds (i.e. provide the desired protection system performance laid out in previous chapters), this measurement and processing capability may already need to be employed on the network. Analysis of processing devices similar to those identified in Chapter 6 [17,18] suggests that the typical sampling rate for a microprocessor is such that sufficiently fast measurements could be taken (assuming acceptable performance of the measurement transducer) to accurately discriminate fault location in the majority of cases.

Whilst the sections do assess a range of conditions, the measurement requirements will generally be determined by one point and that is the minimum measurement time. For the criteria discussed, this minimum measurement time will either be determined by the minimum (short circuit) or maximum fault resistances of interest. The minimum fault resistance will see the fastest rise of current and fall in voltage, and therefore would breach any threshold first, whereas the maximum resistance would require the fastest measurement for fault discrimination. Depending on the nature of the circuit, the voltage and current thresholds or the maximum resistance, either of these factors could be dominant in determining minimum measurement time.

There are certain fault locations where the required measurement time approaches zero, as illustrated in the previous sections. These faults are those very close up to the capacitor or very close to the protection boundary. For these conditions accurate fault detection may not be achieved without additional steps being taken. Possible steps are discussed below.

For the close up faults, a fault current limiting device could be connected in series (or close to on the line), with the capacitance to limit the current magnitude below the current threshold, or at least slow the rise of current to along a measurement to be attained more easily. However the integration of such a device would add cost, weight and complexity to the network and hence detract from some of the benefits of a fast acting fault detection system. An alternative strategy for dealing with this problem would be to implement instantaneous overcurrent or undervoltage protection at the capacitor output to prevent either threshold being breached. As part of this scheme, fault discrimination could be maintained by setting the required protection operating time for the rest of the network to the minimum time at which the undervoltage or overcurrent threshold may be reached for faults on the protection zone boundary. This would enable protection to operate for undervoltages or overcurrents for faults within the protected branch but allow another protection scheme to operate for faults elsewhere in the network. The merits of this approach will be explored in section 7.6.

For faults on the protection zone boundary, L_{meas} is only equal to the operating threshold nL_{Cable} at $t = 0$ and hence the fault would not be detected. Previous sections have also shown that measurement time may also be prohibitively small in cases where the fault location is close to the zone boundary. This highlights a limitation of the proposed method which prevents the protection of a fixed line length. Detection of these faults would require additional capability. This could be provided by an additional zone, encompassing more of the network and providing greater range to the method. This would however provide additional challenges for discrimination, particularly where there is a connection to parallel branches. One means of expanding this protection zone is described in the following section.

This chapter only presents results using data for an example UAV DC network, however all the analysis presented can be similarly applied to larger DC networks. Due to the particularly compact nature of the UAV system, the initial $\frac{di}{dt}$ fault detection method has been assessed in the most demanding environment to achieve fault discrimination. Therefore it is anticipated that conclusions drawn on the UAV network will also be applicable on larger networks, where there may even be more scope to discriminate fault location. One conclusion of this section is that measurement requirements for close up faults are likely to be dominated by voltage or current thresholds (provided these exist on the given converter interface). As the response of large and small systems can be similar under these conditions due to similar cable impedance between capacitance and fault, it can

lead to similar measurement requirements. Therefore discrimination may not be the main challenge to overcome in terms of measurements requirements for various types of DC system.

7.6 Additional operating schemes, considerations and applications

The feasibility and performance analysis of using initial $\frac{di}{dt}$ measurements for fault detection within previous sections was centred on a relatively straight forward operating scheme. Moving beyond this, this section will identify a number of areas for modification or capability expansion of the fault detection method. The section will also outline areas where it is considered that further study is required to fully establish the accuracy and applicability of the method. In some cases, preliminary analysis has been developed to support these areas however full testing has yet to be carried out. Finally, potential areas for wider application are identified.

7.6.1 Integration of instantaneous overcurrent and initial $\frac{di}{dt}$ protection

Protection against close up faults in a coordinated way remains a significant challenge, particularly when attempting to operate with a fixed current threshold. In the previous section, it was suggested that this issue could be overcome by effectively employing both instantaneous overcurrent and initial $\frac{di}{dt}$ as the primary means of fault detection (fast current differential protection, as described in Chapter 6 could also be utilised instead of initial $\frac{di}{dt}$). This builds on work within previous literature [7], which does employ instantaneous overcurrent protection at a capacitor's output but in a non-discriminatory way, as was highlighted in Chapter 2. Protection coordination will be maintained in this case through the derivation of a maximum time for other network protection to operate to prevent the instantaneous overcurrent protection operating for more distant faults. This is described below.

If designing protection to primarily operate for faults on the same branch (as set out previously in this chapter), then operating requirements will be determined by the time taken to reach a certain current threshold for a fault on or close to the protection zone boundary. The purpose of this is to enable instantaneous overcurrent protection to clear faults within the protection zone but provide the

opportunity for protection elsewhere in the network to clear the fault first. This operating requirement can be easily calculated using methods described in section 7.5.5. Table 7.3 illustrates potential operating times for a sample of current thresholds and fault locations within the UAV architecture assessed in section 7.5.

Table 7.3: Time to $I_{threshold}$ for two specific fault locations

n_f	$I_{threshold}$ (A)	Time to $I_{threshold}$ (μs)
0.5	500	6.1
0.5	1000	12.3
0.5	2000	25.1
0.8	500	9.8
0.8	1000	19.8
0.8	2000	40.6

Table 7.3 highlights that coordination of network protection with elements of instantaneous overcurrent protection can lead to short operating time requirements, although in many cases this is less than the sampling requirements described within section 7.5. The threshold values shown within table 7.3 will be a function of threshold current and network component parameters and therefore will vary with application. The assessment of the UAV network again leads to the derivation of the strictest operating requirements due to particularly small cable lengths. Whilst the case study suggests this may be a viable protection solution, more robust assessment is required as part of future work.

7.6.2 Addition of a blocking zone for distant faults using initial $\frac{di}{dt}$ measurement

In addition to the use of initial $\frac{di}{dt}$ measurements for fault detection, the characteristic response is such that it could be utilised to restrain the operation of protection for faults outwith the protection zone. It is proposed that this could be achieved for more distant faults, where a low initial $\frac{di}{dt}$ would indicate that a fault does not exist within or nearby the protection zone. It is anticipated that this would be particularly effective where parallel sources exist, with section 7.4.5 highlighting that the parallel sources can significantly reduce the $\frac{di}{dt}$ output when the fault does not occur on the same branch as the capacitive source. Using this approach, the operation of either primary or back up protection systems could be restrained, which would allow more time for other parts of the network to clear a fault, potentially improving protection system coordination.

With the addition of a blocking zone, a protection scheme based on initial $\frac{di}{dt}$ measurements could be viewed as having three discrete zones, as illustrated in figure 7.26. This figure shows the typical busbar network divided into three protection zones, from the perspective of the main filter capacitance. The length of the 'Trip' zone, where protection should operate if a fault occurs within, will depend on a number of uncertainties as section 7.5 describes.

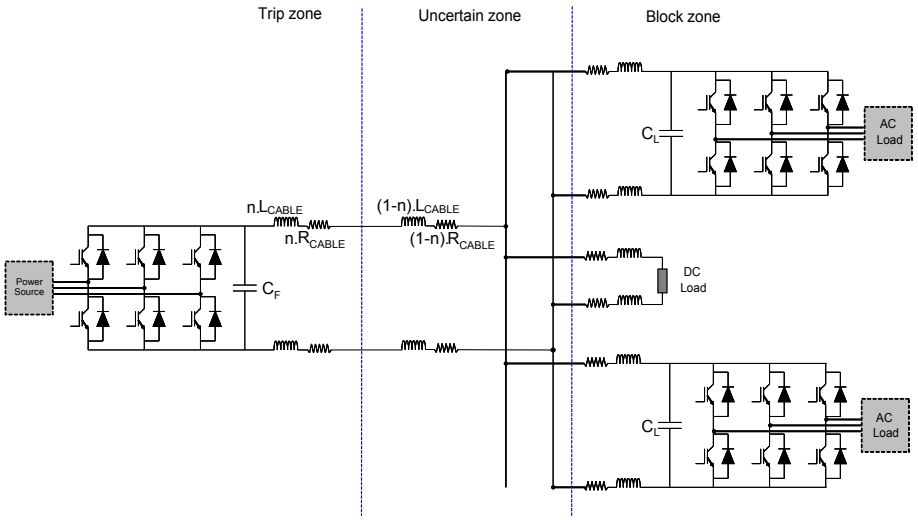

Figure 7.26: DC network with multiple protection zones

The 'Uncertain' zone represents the area close to the 'Trip' zone boundary, where initial $\frac{di}{dt}$ is not significantly less than that for faults within the 'Trip' zone. Therefore faults within the 'Uncertain' zone should not cause primary protection to operate but they are sufficiently close that it is undesirable to block or restrain protection operation. The detection of faults within the 'Uncertain' zone remains a challenge, particularly through the use of initial $\frac{di}{dt}$ measurements, and further work is required to determine correct protection operation for these fault conditions. Within figure 7.26, the 'Uncertain' zone encompasses the distribution busbar. For these scenarios, busbar protection [19], the setup for which was demonstrated in Chapter 6, could be utilised.

The 'Block' zone is an area sufficiently distant from the capacitive source such that the initial $\frac{di}{dt}$ magnitude is low enough to indicate that a fault does not exist within or nearby the protection zone. This information could be used to allow protection local to the fault more time to operate. How this would be achieved will depend on the means of fault detection from the main filter capacitance. For example, if undervoltage protection is utilised as back up, it may be possible to have two discrete thresholds, a higher voltage threshold for normal protection operation and a lower voltage threshold for restrained operation. In this way

back up is still provided, but its operation will be delayed. In closely coupled systems, the changing of operating thresholds may help the coordination of less discriminative back up protection systems. However to quantify the benefits of this and how a blocking zone could be utilised most effectively, further work is required with a more specific test network.

7.6.3 Compensation of initial line voltage drop

It was discussed in section 7.4.2 that an opposing initial voltage can reduce the accuracy of fault detection using the initial $\frac{di}{dt}$ measurement. While it is not possible to accurately compensate for the initial voltage across a fault due to its unknown resistance (which unfortunately is likely to be the highest source of error for high resistance faults), measurement accuracy can be improved by compensating for line voltage drop. Compensation can be particularly useful when the line contains high resistance elements or devices such as solid state circuit breakers or fault current limiters with a constant on-state voltage drop.

Compensation approach

To illustrate this, consider the network configuration in figure 7.27 and response to the four fault locations indicated. Due to the number of cable sections considered, the R-L sections have lumped together, including the return path, to simplify the diagram. Furthermore, for the purpose of this analysis it will be assumed that fault resistance is zero. Figure 7.27 indicates the boundary of the protected zone and so for this network the protection scheme will be set to operate when $\frac{di}{dt} \geq \frac{v_{CF}(0)}{3L}$.

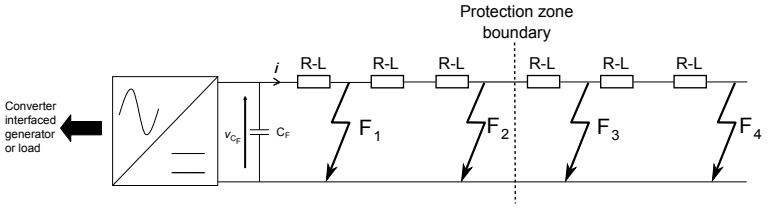

Figure 7.27: Equivalent network section with lumped parameters and four fault locations

First, consider the initial $\frac{di}{dt}$ response for the four fault locations in figure 7.27. For F_1 the response is

$$\frac{di_L(t \to 0)}{dt} = \frac{v_{CF}(0) - i_L(0)R}{L}, \tag{7.66}$$

for F_2 it is

$$\frac{di_L(t \to 0)}{dt} = \frac{v_{CF}(0) - 3i_L(0)R}{3L}, \tag{7.67}$$

for F_3 it is

$$\frac{di_L(t \to 0)}{dt} = \frac{v_{CF}(0) - 4i_L(0)R}{4L}, \tag{7.68}$$

and for F_4 the response is

$$\frac{di_L(t \to 0)}{dt} = \frac{v_{CF}(0) - 6i_L(0)R}{6L}. \tag{7.69}$$

Comparing these responses to the protection operating condition, it is likely that despite the initial $\frac{di}{dt}$ for F_1 being slightly reduced by the opposing line voltage protection should still operate. However as F_2 occurs on the zone boundary, the apparent lengthening of the line due to the $-3i_L(0)R$ term will cause measured $\frac{di_L}{dt}$ to be less than $\frac{v_{CF}(0)}{3L}$. In this case the fault would not be detected. Both F_3 and F_4 occur outwith the protected zone and so would not cause protection operation. The opposing voltage in each case again acts to lengthen the line measurement. For faults outwith the protected zone, this has the positive impact of making the fault look further away and hence reducing any likelihood of false protection operation.

Clearly the non-detection of faults at or close to the zone boundary results in non-optimal protection system performance. It is therefore proposed that the impact of the initial line voltage can be mitigated to improve fault detection in this region. This can be achieved by adding the maximum potential line voltage drop up to the zone boundary, $3i_L(0)R$, to the measured $v_{CF}(0)$ to compensate for any potential opposing line voltage. For the added $3i_L(0)R$, $i_L(0)$ is the measurable parameter of line current and R is a known line parameter.

Considering the impact of the additional compensating voltage on the four measured initial $\frac{di}{dt}$, the response for F_1 is now

$$\frac{di_L(t \to 0)}{dt} = \frac{v_{CF}(0) + (3-1)\, i_L(0)R}{L}, \tag{7.70}$$

for F_2

$$\frac{di_L(t \to 0)}{dt} = \frac{v_{CF}(0) + (3-3)\, i_L(0)R}{3L}, \tag{7.71}$$

for F_3

$$\frac{di_L(t \to 0)}{dt} = \frac{v_{CF}(0) + (3-4)\, i_L(0)R}{4L} \tag{7.72}$$

and for F_4

$$\frac{di_L(t \to 0)}{dt} = \frac{v_{CF}(0) + (3-6)\, i_L(0)R}{6L}. \tag{7.73}$$

Equations (7.70) to (7.73) show that for each of the fault cases the measured $\frac{di}{dt}$ would increase and hence the apparent line length is reduced. For F_1, the addition of the compensating factor has increased $\frac{di}{dt}$ beyond the $\frac{v_{CF}(0)}{L}$ expected without line voltage. Therefore, close up fault conditions are more likely to be detected due to the inflated $\frac{di}{dt}$. For F_2, the impact of line voltage has been removed and so the measured $\frac{di}{dt}$ is now equal to the minimum setting required to operate the protection. If no additional uncertainties exist, this would allow the fault to be successfully detected (although section 7.5 illustrates how time of measurement influences this detection). For faults F_3 and F_4, the compensating factor provides a more accurate fault location measurement and despite the faults appearing closer to the zone boundary, $\frac{di}{dt}$ will still be less than the protection setting and so the protection will remain immune to the more distant faults.

For lines containing power electronic components with an on-state voltage drop, this compensating factor can be easily altered to include a constant term, which would be added to the total voltage. Whilst making only small changes to the implementation of the initial $\frac{di}{dt}$ method, these compensation approaches could be used to improve measurement and detection accuracy.

7.6.4 Measurement of second derivative

There is also some merit in examining any information which can be derived from the second derivative of the capacitive response, as will be highlighted below. Earlier sections have shown that for underdamped circuit conditions $\frac{di}{dt}$ is equal to

$$\frac{di_L}{dt} = \frac{v_{CF}(0)e^{-\alpha t}}{L}\left[\cos(\omega_d t) - \frac{\alpha}{\omega_d}\sin(\omega_d t)\right] + i_L(0)e^{-\alpha t}\left[-2\alpha\cos(\omega_d t) + \left(\frac{\alpha^2}{\omega_d} - \omega_d\right)\sin(\omega_d t)\right]. \tag{7.74}$$

Taking the derivative of (7.74) using the product rule and simplifying gives

$$\frac{d^2 i_L}{dt^2} = \frac{v_{CF}(0)e^{-\alpha t}}{L}\left[\left(\frac{\alpha^2}{\omega_d} - \omega_d\right)\sin(\omega_d t) - 2\alpha\cos(\omega_d t)\right] + i_L(0)e^{-\alpha t}\left[\left(3\alpha^2 - \omega_d\right)\cos(\omega_d t) + \left(3\alpha\omega_d - \frac{\alpha^3}{\omega_d}\right)\sin(\omega_d t)\right]. \quad (7.75)$$

Assessing (7.75) as time approaches zero results in

$$\frac{d^2 i_L}{dt^2}(t \to 0) = i_L(0)\left[\frac{R^2}{L^2} - \frac{1}{LC}\right] - \frac{v_{CF}(0)R}{L^2}. \quad (7.76)$$

As discussed in earlier sections, although equation (7.76) is derived from the underdamped response, when assessing initial conditions, it is representative of all damping conditions.

Equation (7.76) shows that when analysing the second current derivative, the response is more sensitive to resistance, as resistance now multiples both current and voltage terms. This suggests that in terms of fault detection, the second derivative is less useful than the first. However this function could potentially be used as a measure of resistance in a fault path, and perhaps more importantly, of the fault itself. If it is assumed that all parameters other than R in (7.76) are known, where L is calculated from initial $\frac{di}{dt}$, then it is possible to estimate fault resistance.

Further work is required to fully identify both the likely accuracy and potential use of this measurement but the fault resistance measurement could be useful in helping to identify the type of fault that has occurred, and aid the protection or prevention of these faults in future. This fault identification could be carried out as part of a post fault diagnosis process.

7.6.5 Detection of earth faults

Chapter 3 described how the natural response of the network under rail to earth fault conditions can differ to that of rail to rail faults. These differences will likely cause significant difficulties in the detection of earth faults using the method described in this chapter. Of particular significance it was illustrated that where a mid-point earthing configuration is utilised at the converter output terminals, the total capacitance doubles but terminal voltage halves when a fault occurs due to the capacitors now being connected in parallel. This will also half the magnitude of the initial $\frac{di}{dt}$, significantly impacting on measured inductance where changing voltage is not taken into consideration.

The impedance of the earth path and earthing strategy are also important aspects to consider. For the rail-rail faults considered throughout this chapter, protection settings have been based on an inductance loop containing only forward and return paths of the conductor which are easily calculable given appropriate line parameter data. Under earth fault conditions, the current path between point of fault and ground is less defined and hence the inductance loop can be unpredictable. This would become even more challenging where systems are grounded through an impedance [20–22]. Therefore further investigation is required to establish whether initial $\frac{di}{dt}$ measurements can be used in the detection of earth fault conditions.

7.6.6 Impact of incorporating skin effect on the analysis of fault response

So far the analysis of DC system fault characteristics presented within this thesis has focused on the evaluation of transient and frequency domain response without considering the impact of skin effect. This is commonly the case within literature as the following examples highlight [4, 5, 7–9, 23]. While neglecting skin effect may be reasonable in the context of normal system operation, the architecture of future platforms can result in load and fault current transients to be of greater magnitude and frequency than experienced in previous systems, which has been highlighted throughout this thesis. The action of the skin effect on these high-frequency currents will have an impact on the system behaviour under fault conditions, which could have implications for the design and effectiveness of protection systems employed. This is of particular relevance in the assessment of initial $\frac{di}{dt}$ measurements for protection, as for these to be most usefully employed, accurate knowledge of line parameters is essential. Thus it is appropriate to re-evaluate the relevance of skin effect to the fault analysis of compact DC power systems. For this purpose, this section describes a compact equivalent circuit model of skin effect in a conductor and applies it to a DC marine zonal power system (typical of that proposed for modern naval Integrated Full Electric Propulsion (IFEP) vessels), the parameter data for which was presented in table 4.1 within Chapter 4. The section illustrates the impact of including skin effect within fault related transient simulation studies, quantifying the difference in peak fault current levels and network damping.

Skin effect in DC systems

The skin effect describes an electromagnetic phenomenon whereby alternating current tends to flow along the surface of a conductor (its 'skin') rather than flowing throughout the cross section of the conductor in a distributed fashion [24–26]. The depth of this skin reduces with increasing frequency, effectively reducing the cross-sectional area of the cable available to carry the current. In this manner, the effective resistance of a cable increases for progressively higher frequencies of conducted current.

Wang [26] presents an example of how the resistance and inductance of a traction system power rail may vary with frequency. This is illustrated in figure 7.28.

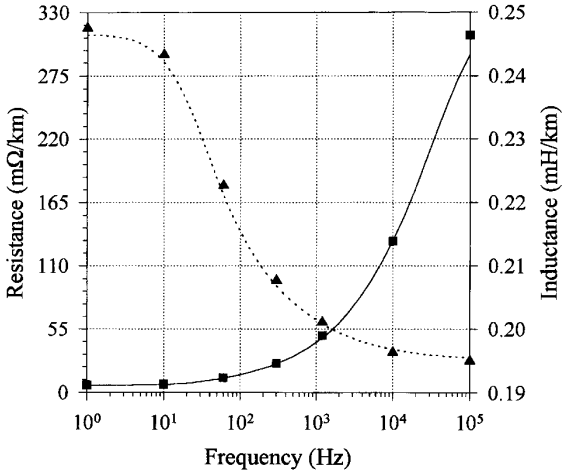

Figure 7.28: Rail resistance (solid line) and inductance (dashed line) for a traction system [26]

Figure 7.28 suggests that both resistance and inductance remain largely constant until skin depth is smaller than the radius of the conductor. Resistance begins to rise significantly as frequency increases beyond this point, reaching more than twenty times the DC resistance at 100kHz. Conversely, inductance actually decreases with frequency, although this is to a lesser extent than the increase in resistance. Figure 7.28 also illustrates how inductance tends towards a constant value at very high frequencies which can be attributed to the externally-caused inductance in the conductor. This is unaffected by the skin depth and as such remains constant for all frequencies. For the conductor represented in figure 7.28, the external inductance makes up around 80% of the total low frequency inductance.

At high frequencies, the reactance of the conductor dominates the total line impedance. As such, a model of this particular cable including skin effect will

have 20% less impedance than that of a simple R-L model. For physically compact networks with particularly high resonant frequencies during fault transients (as a result of the low impedance of interconnecting cables), this disparity could make a notable difference to the peak magnitude and damping of the fault current profile.

Compact equivalent circuit model

A common method used for the modelling of the skin effect is the use of an equivalent ladder circuit, containing resistive and inductive components [24, 26, 27]. An example of this modelling approach is shown in Figure 7.29.

The model shown in figure 7.29 divides the conductor into four concentric areas. Values of the individual components in the model relate to these four numbered sections. Section four represents the largest area and hence the smallest resistance, with the resistance of subsequent sections increasing as area decreases. Total inductance is made up from internal and external sources and these are represented individually. External inductance is constant with frequency and so can be modelled as an inductor in series with the ladder circuit. Internal inductance is directly proportional to conductor area and so decreases in relation to this. It is assumed that no internal inductance exists for the outer section as internal flux (which causes inductance) drops to zero.

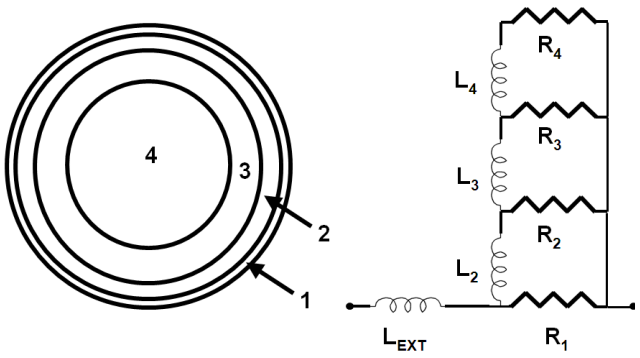

Figure 7.29: Four ladder compact circuit model and corresponding concentric areas of conductor

The components in the model are chosen to give the effect of resistance increasing and inductance decreasing with frequency. This is achieved by directing current through the appropriate $R-L$ branch (or combination of branches) at a given frequency. Kim and Neikirk [27] provide details on how the R and L components can be selected depending on the frequency range of interest; however some key requirements are highlighted. These are: the parallel combination of

the resistors in the model tends to the actual DC resistance of the conductor; the sum of the four inductors is equal to the low frequency inductance; and components R_1 and L_{EXT} are equal to the resistance and inductance at the maximum frequency of interest respectively.

The next section investigates the impact on the fault current profile and I^2t energy delivered to a fault of replacing conventional $R-L$ cable models with skin effect models within a representative of marine network architecture.

Impact of skin effect on the simulation of fault transients

To investigate the influence of skin effect on the performance of protection devices, the network shown in figure 7.30, representing a portion of a zonal marine DC power system is modelled. Within figure 7.30, the points labelled A, B and C indicated locations of relays on the network and points labelled 1, 2 and 3 indicate different fault locations. Within this section, the majority of these are not referred to as they are utilised for part of a wider study of the impact of skin effect on the operation of network protection. This work is presented in full in [28].

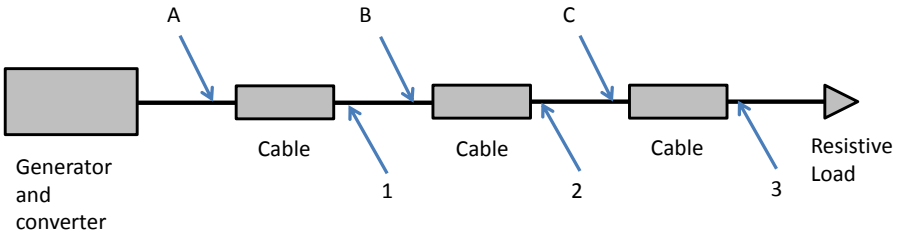

Figure 7.30: Zonal marine DC power system

Figure 7.31 shows the fault current at point 3 when the cables are modelled using both the conventional R-L approach and using the skin effect model described above. As can be seen, there is a significant transient peak in fault current as the converter smoothing capacitors discharge, following which the current is sustained (with initial damped oscillation) at the 1000A constant infeed provided by the converter irrespective of fault location.

Figure 7.31 shows that the peak magnitude of the fault current is increased in the skin effect model, but the current then decays more rapidly to the constant value, so that for the later part of the transient the fault current is lower in the skin effect case than in the R-L case. These effects are due to the lower total inductance and the higher resistance of the skin effect compact equivalent model compared to the conventional R-L model. Since the behaviour of some protective devices (e.g. fuses) can be represented using a characteristic based on the square

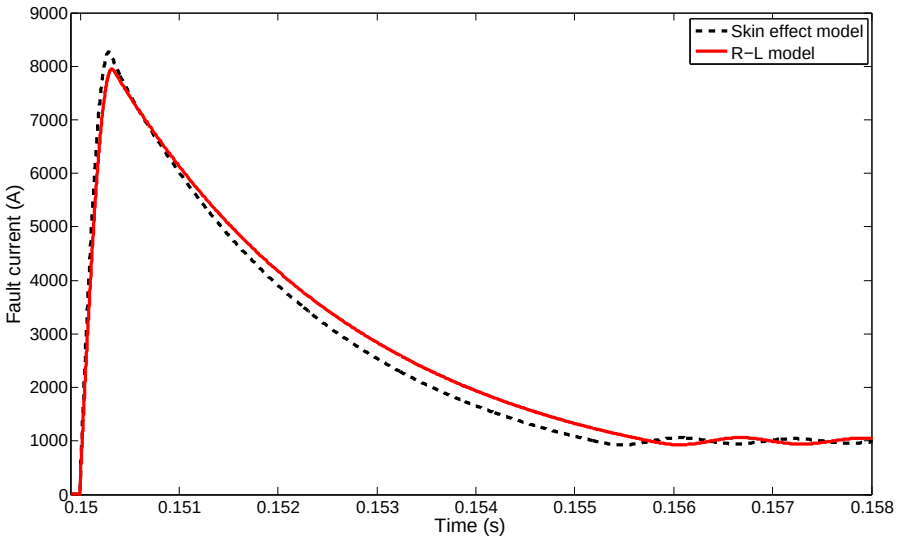

Figure 7.31: Simulated fault current at point 3

of the fault current, figure 7.32 shows I^2t - the integral of the square of the current with respect to time.

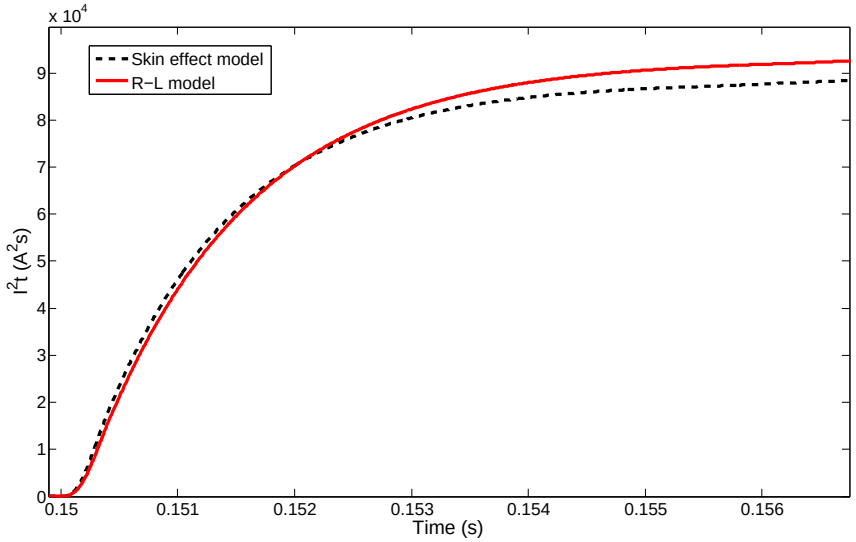

Figure 7.32: Simulated I^2t at point 3

Figure 7.32 also illustrates the effect of the reduced fault current in the later part of the simulation in the skin effect case. It shows the effects of the faster rise of the current transient in the skin effect model - for the first $2ms$ after fault inception I^2t is larger than in the R-L model. Both the current and I^2t effects might be expected to impact on the behaviour of protection devices in this network.

Discussion of results

From the results in the previous section, it can be seen that the skin effect does lead to measurably different fault current behaviour in DC power systems. There are two key points of particular relevance to the assessment of an initial $\frac{di}{dt}$ based protection scheme which should be considered for further study.

The first relates to the variance in the line inductance during a transient event. The previous analysis within this section is based on the assumption of constant line inductance, therefore if inductance does significantly change during the faulted period then it would impact on the validity of this analysis. However, if any change in inductance can be understood and accurately quantified then this could potentially be accommodated into the protection settings. This could be achieved either by changing operating thresholds to reflect the lower inductance immediately after a fault occurs or increasing the percentage of line length uncertainty, as discussed in section 7.5.

Figure 7.28 illustrates that inductance change may be significant for current following through a railway line and this is reflected in the modelled behaviour, which is based on this observation. Whilst figure 7.28 indicates expected behaviour, further study is required for more appropriate conductor types for more compact networks. Furthermore, the model used in this section is a steady state skin effect model applied within a transient environment. It is reported in [29] that under transient conditions, during the first half cycle of an AC current waveform, the current distributes itself closer to the surface of a conductor than for steady state AC; therefore the skin effect will be more pronounced. This behaviour is more challenging to represent in modelling and simulation, but the results presented in this section suggest that investigation of such behaviour within DC networks would be worthwhile.

The second key area for further study is the impact of skin effect on network damping. As the previous sections describe, skin effect causes resistance to increase and inductance to decrease, and as network damping is proportional to the ratio of resistance and inductance, damping will increase. Section 7.5 highlighted that damping levels will impact on the required measurement times, as $\frac{di}{dt}$ will decay faster under higher damping conditions. Therefore some revision to the analysis may be necessary to ensure accurate determination of measurement requirements.

7.6.7 Impact of varying mutual inductance within compact and power dense networks

When current carrying conductors are placed suitably close to one another, the magnetic coupling between the fields of each conductor can induce an EMF in the other [30]. The effect of the induced EMF is to create a mutual inductance between conductors, which contributes to the total inductance of a line. Faraday's Law says that to induce an EMF in the nearby conductor, a varying flux is required, which in turn requires a varying current. Therefore within DC systems under steady state conditions, this EMF and hence mutual inductance is likely to be limited, other than the contribution from AC sections of the network such as generator outputs. However under transient conditions such as faults, where current (and hence flux) can change rapidly, mutual inductive effects may be created between conductors. Therefore this has the potential to alter the inductance of parallel lines, which would change the apparent location of a fault when using measurements of fault path inductance to determine fault location. Assessment of the impact of these effects on any inductance measurement would be worthwhile as part of any future work.

7.6.8 Impact of means of fault onset/inception and changing fault conditions

The simulation and analysis work considered throughout this thesis makes the assumption of constant fault conditions, where a fault is applied instantly and remains at a constant resistance and location until the operation of protection. However in a practical environment it is possible that after fault inception these conditions may change. For example [30] discusses the possible movement of an arc fault between different phases in an AC network and [31] highlights the potential for an arc fault to degrade into a bolted short circuit fault, or even self extinguish. Clearly where fault conditions change, so will the fault response of the network.

In order to establish whether this will impact on the ability to detect faults through initial $\frac{di}{dt}$ measurements, further research is required to accurately determine how the fault appears to the rest of the network during its inception and during the transition from one state to another. Further information in this area will provide a clearer picture of the types of fault which could be detected with initial $\frac{di}{dt}$ measurements.

7.6.9 Application in HVDC and AC transmission systems

Initial $\frac{di}{dt}$ fault detection may also have an application in larger transmission and distribution networks (both AC and DC) where significant capacitance is present in the network, such as for filtering at the converter output of wind turbines, tidal or wave generators, or photovoltaic systems. Its application could also be extended to network sections with reactive power compensation capacitors or HVDC links. In a similar fashion to the method described for compact DC systems, monitoring of the initial derivative current within these networks would indicate fault path inductance, from which fault location can be derived. For AC systems, the frequency of any fault transient from the capacitive discharge is likely to be far higher than the system frequency and so it is expected that the measured fault current derivative would be easily distinguishable from any current waveform. An issue with the application in AC systems is the variable voltage across the capacitance. As the magnitude of $\frac{di}{dt}$ is proportional to this voltage, a fault occurs around a voltage zero then $\frac{di}{dt}$ will be very small relative to peak levels, potentially causing the non-detection of the fault.

7.6.10 Use of dedicated network capacitance for fault detection

This chapter has so far focused on using the response of the output capacitance of converters, which already exists within the network, for fault detection. However it is also possible that a dedicated capacitance could be included within the network to perform a similar operation. This could consist of a single centralised capacitor or a number of small capacitors connected at key points in the network. These could be connected through a resistance to ensure fault level is not significantly increased. Use of these fault detection capacitors could provide wider coverage in existing DC networks, such as the protection of non-converter interfaced loads, and also extend the range of possible applications as there would not be the need for converter interfaced sources and loads.

7.6.11 Integration with converter protection systems

As a practical application consideration, given that the initial $\frac{di}{dt}$ fault detection method is designed to operate at a converter output, it could be built into the converter protection rather than the network protection. This could enable internal converter protection to better coordinate with network protection when responding to faults. This could help prevent the unnecessary and undesirable

tripping of converters under fault conditions and so help the coordination of internal converter and network protection systems.

7.7 Chapter summary

Whilst the novel fault detection method proposed within this chapter is at an early stage of development, there is clear potential for its use within converter interfaced DC networks. Development and analysis of the method has highlighted the benefits of the detailed analytical approach taken within this thesis, and this has also been utilised to define both its potential applications and limitations. In order to help progress this method to use within a practical environment, a number of key areas of future work have also been identified.

The fault detection concept presented within this chapter has so far lead to a patent application [32] and a conference publication [33]. The analysis of skin effect in DC systems is also the subject of two conference papers [28, 34].

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Chapter 8

Conclusions, contributions and future work

The work presented within this thesis covers a number of key issues related to the protection of multiterminal DC networks. The thesis highlights that a range of converter technologies are being developed which will influence future protection requirements. Through conducting a detailed analysis of the response of the converter type most prevalent in literature (and with the most demanding protection requirements), methods of quantifying the key factors which shape a networks fault response are derived. From this, a desired protection approach is identified which is based on the mitigation of fault transients through the fast operation of protection in order to achieve design and operability benefits. The capabilities of different methods and technologies for achieving these aims are then analysed and the most promising of these are identified as part of design framework for DC networks. Finally, two novel fault detection techniques are proposed which have the potential to overcome a number of the shortfalls of present protection systems. Conclusions and contributions from each of these aspects of the thesis are presented in the following section.

8.1 Review of chapter conclusions and contributions

From work presented within each of the previous chapters a number of key conclusions have been drawn. These are summarised according to chapter in the following paragraphs.

Chapter 2

Chapter 2 reviewed a number of concepts in the design and protection of DC networks, considering how application type, network architecture and converter technologies all influence the protection system requirements. Within this chapter it was identified that the use of high capacitance converter types create the most challenging protection requirements but also the greatest potential benefit of an effective protection system given the simplicity of their design compared to other converter types.

The chapter also highlighted that a lack of effective protection solutions existed within literature to effectively accommodate these converter types. The chapter identified that there were two clear areas where a contribution could be made in order to meet these challenges. These were the development of analytical approach to represent fault response and the development of methods to ensure fault detection within the transient period during fault inception. Both of these issues were addressed within subsequent chapters.

The review of protection challenges, DC network architectures and converter technologies presented in this chapter contributed to two journal publications and one conference publication.

Chapter 3

Chapter 3 presented a detailed analytical study of typical DC network fault response, inclusive of the initial fault response, current interruption and post fault transient phases of the fault response. This analysis builds upon relevant standards and fault calculation literature by developing new methods which can be specifically applied to active converter types to accurately determine a network's fault response for a range of scenarios. The work presented within this chapter underpins much of the analysis which is conducted within subsequent chapters.

Chapter 4

Chapter 4 illustrates how the analytical tools developed within Chapter 3 can be utilised to quantify a range of different factors which would impact on the operating requirements for a network's protection system. Developing on this analysis, the concept of how fast acting protection could have a positive impact on network design aspects is introduced. In particular, it is discussed how the operation of protection before certain thresholds would potentially enable reductions in component withstand requirements and protection equipment. For

applications where electrical system mass and volume are key design factors, such as aircraft, this type of approach may drive improvements in fault detection and circuit breaking technologies.

The chapter highlights how the aim of achieving fast acting protection can limit the range of protection devices which can be successfully employed. In particular, the comparison of typical circuit breaker operating times with a range of performance criteria illustrated that EMCBs and HCBs often fail to match requirements, suggesting SSCBs are the technology of choice. This is significant, particularly given the relative immaturity of SSCB technologies and has the potential to impact on the adoption of DC systems within the near term.

The work presented in this chapter has so far contributed to one journal and three conference publications.

Chapter 5

Chapter 5 first demonstrates the challenges in applying non-unit fault detection techniques within highly capacitive interfaced DC networks, where it is illustrated that the use of conventional non-unit methods can be sub-optimal when attempting to achieve discriminative protection system operation within the time scales laid out in Chapter 4. This conclusion is particularly significant as the use of non-unit techniques is very common within distribution and low voltage networks, and hence this would require a shift in common protection practice. In turn this would impact the viability of any DC network implementation.

The use of current differential protection is introduced as a potential solution and the inherent challenges in its implementation to DC networks are analytically assessed and quantified. The parameters which are quantified include the required scheme decision making time and the impact of varying degrees of measurement non-synchronisation on the current sum error within a current differential scheme. The availability of a high bandwidth communications system is identified as being essential to operate effectively within the derived operating times, although this has implications for system cost and complexity.

Based on this assessment of conventional protection methods, a design framework is proposed for DC microgrid systems which provides a means of optimising protection scheme design to achieve required fault discrimination and operating speed whilst seeking to minimise installation costs.

The work presented within this chapter has to date contributed to one journal paper and one conference paper.

Chapter 6

Chapter 6 presents an example case study where a 'pilot wire' based current differential protection scheme is implemented on UAV electrical system. The approach is based on the use of standard current differential techniques and a reasonably basic microprocessor. However it demonstrates how the natural characteristics of DC networks, namely the voltage output of current transducers and the need to only compare current magnitude, create the opportunity for very fast fault detection. The approach is therefore considered to be a viable method of implementing coordinated protection system operation in a far quicker manner than is currently achieved in practice.

Chapter 7

The novel fault detection method proposed within Chapter 7 is based on the estimation of fault path inductance from the measurement of a converter capacitor's initial discharge characteristic. Its focus of operating on the initial $\frac{di}{dt}$ is a key factor which differentiates the method from protection schemes currently in use. It is insensitive to fault resistance and fast acting and hence has the potential to overcome a number of the shortfalls of present protection systems. The fault detection method was conceived through the detailed assessment of a DC network's natural fault response presented within earlier chapters. This analysis also enabled the scope of the methods applications to be identified. Whilst the method is at an early stage of development, there is clear potential for its use within converter interfaced DC networks. In order to help progress this method to use within a practical environment, a number of key expansion and risk areas were identified.

A patent application has been made in relation to this proposed fault detection technique. It is also the subject of a conference publication.

8.2 Key areas of future work

A number of areas of future work have been identified which have the potential to advance both the work presented within this thesis and the wider research area. These are discussed in the following sections.

8.2.1 Optimisation of protection system design through combination of operating requirements

The analysis methods developed in this thesis consider the factors which may influence the protection system requirements on an individual basis. Whilst this approach does help illustrate how these factors vary, is slightly fragmented as it does not fully capture the fact that all the factors are interlinked. For example, Chapter 4 has identified that interrupting high magnitudes of current can lead to higher circuit breaker energy dissipation requirements and/or overvoltage conditions, however does not consider these factors simultaneously. An approach which establishes a relationship between these different operating requirements which could then be used to calculate the most favourable protection operation conditions would make best use of the analysis developed and be a powerful design tool. By highlighting how requirements change with operating strategy, it is hoped that the protection scheme can be designed in a way to target these most favourable operating conditions and hence optimise the design of the protection system.

From the work presented within this thesis, it is clear that the very early operation of network protection, with subsequently low breaking current, can minimise the requirements a number of factors without compromising the level of network protection offered. However without a proven means of achieving this, a trade off between various requirements, at a later operating time, may be the approach to take. To facilitate this, a more thorough review of commercially available technology would be required to determine how various available protection devices would impact on the achievable level of protection performance. Analysis of this type would inform network designers as to whether a specific design may be successfully protected, first by attempting to operate via the fast acting methods proposed in this thesis, but then also through the inclusion of additional devices such as fault current limiters.

8.2.2 Quantification of the impact of protection system operation on overall system design

Throughout this thesis it is argued that the way in which the protection system is operated not only impacts on its own design but also that of the overall network in which it protects. Chapter 4 highlights the reasoning behind this, discussing how fault clearance time may impact component withstand requirements and required snubber equipment as well as potentially impacting requirements for

system redundancy. The influence of these different factors will depend on the application in which the network is operating, with cost likely to be a main design objective for microgrid networks, whereas space and weight of network components is of greater concern for shipboard and aircraft networks.

This is a new avenue of research and therefore tools to quantify the impact of different protection operating strategies on various design factors do not necessarily exist. However the development of such tools could provide network designers with a clearer picture of the impact of alternative protection approaches at a system design level. This could enable network protection to be considered at an earlier stage of the design process and hence maximise any potential design benefits.

8.2.3 Demonstration of microprocessor based current differential schemes

The proposed approach to implementing current differential protection, as described in Chapter 6, has the potential to deliver high speed, coordinated protection system operation. Successful demonstration of such an approach in a practical environment, perhaps in conjunction with SSCB technology, would be a significant step towards achieving optimal protection for small, power dense networks. This piece of work could also involve the development of novel biasing methods as highlighted in Chapter 6.

8.2.4 Development and demonstration of $\frac{di}{dt}$ based protection schemes

There are two key themes to consider in the development of the initial $\frac{di}{dt}$ based protection scheme proposed in Chapter 7. The first is to define the accuracy with which inductance can be measured using the proposed approach, factoring in electromagnetic effects such as Skin Effect. The second is the development of protection schemes to maximise the use of the available fault location information. Possible schemes have been proposed in Chapter 7 however should be developed along with accuracy measurements as part of future work.

8.3 Concluding remarks

From the work presented within this thesis, it is clear that more challenges than solutions exist for the development of future DC power system architectures and

the relative immaturity of the DC protection technologies suggest that it will be a number of years before they are economically competitive. However before reaching that stage, there is still the requirement to overcome a number of technical issues and the development of effective protection system solutions is a critical step in the development of high performance DC systems. This thesis has defined operating requirements and proposed a number of solutions to how these may be achieved, however as has been identified, the required performance of protection devices is in excess of that currently implemented. Demonstration of these concepts within a hardware environment will be a key step in realising their potential.