Modern Voltage Source Converter Topologies for Future DC Grids
PhD Thesis

Dimitrios Vozikis

PEDEC Group
Department of Electronic and Electrical Engineering
University of Strathclyde, Glasgow

February 2019

Abstract

This thesis presents a comprehensive comparison of state-of-the-art HVDC converters with DC fault-blocking capability, based on the modular multilevel converter (MMC) including half-bridge, full-bridge and mixed cell variants, and the alternate arm converter (AAC) topologies. The comparison includes AC and DC power quality, and semiconductor losses considering different operating conditions and design parameters, such as the number of cells and component sizing. In addition a thorough comparison of the transient behaviours is also presented. The transient behaviours of the aforementioned converters are assessed under various conditions including charging sequence, operation in unbalanced grids, and DC fault recovery. Such thorough comparative studies have been performed using high-fidelity converter models which include detailed representation of the control systems that reflect real-scale projects, and of the converter thermal circuit. The main findings of the investigation are intended to assist in the selection of the most suitable converter, given specific performance specifications such as power losses and quality, control range, capacitor voltage ripple, cell capacitor requirements, and improved response during transient operation.

The findings of the state-of-the-art HVDC converter comparison inspired two novel topologies, which represent extension of the MMC and AAC topologies. An Enhanced MMC (EMMC) is proposed where the number of output voltage levels is related to the product of the numbers of half-bridge and full-bridge cells rather than the sum. In this way a large number of voltage levels is achievable using a reduced number of cells. In comparison with the conventional MMC, the EMMC reduces the structural complexity and removes the passive filtering, while it has compact footprint for high and medium voltage applications. An improved AAC (IAAC) is proposed which removes completely the need for a DC filter and reduces the DC fault current levels, whilst retaining small footprint and good efficiency.

A flexible laboratory scale prototype converter is designed and constructed, providing experimental evidence to support the off-line simulations studies.

Acknowledgements

First and foremost I would like to thank my family for providing me the foundation of being a man.

I would like to thank my supervisors, Prof. Stephen Finney and Dr. Derrick Holliday for their immense support and guidance that they provided for completing the thesis. I would also like to thank Dr. Grain Adam for his inspiring conversations, technical discussions and his inexhaustible knowledge that he shared with me.

I am thankful for the support of RTE-France. Especially I would like to express my gratitude to Dr. Olivier Despouys and Dr. Pierre Rault as they were the main drivers of this thesis, and along with their great expertise and constructive criticism I was able to evolve into a truly independent researcher.

I am also thankful for the support of the EU BestPaths Demo2 project. Through the project I had the chance to travel around the Europe and have in-depth discussions with TSOs, manufacturers and universities, providing great insight which helped me during my research and in my professional career.

Also I would like to thank my friends Dr. Xavier Bellekens, Dr. Kamilla Nieradzinska, Dr. Kamyab Givaki, Dr. Habib Rahman and Dr. Dimitrios Athanasiadis for their support as they made my PhD life tolerable.

Finally, I am really grateful for the unconditional support from Elham; thank you so much.

Contents

List of Figures

List of Tables

List of Abbreviations

AAC	Alternate Arm Converter
AC	Alternate Current
AC-R	AC limiting Resistor
ACCB	AC Circuit Breaker
APF	Active Power Filter
APOS	Alternative Phase Opposition Disposition
CBA	Capacitor Balancing Algorithm
CCC	Capacitor-Commutated Converter
CCSC	Circulating Current Suppressing Controller
CTB	Controlled Transition Bridge
DAB	Dual Active Bridge
DC	Direct Current
DC-D	DC Disconnector
DC-R	DC limiting Resistor
DCCB	Direct Current Circuit Breaker
DR	Diode Rectifier
DRU	Diode Rectifier Unit
DS	Director Switch
DSM	Detailed Switching Model
EMF	Electromagnetic Force
EMI	Electromagnetic Interference
EMMC	Enhanced Modular Multilevel Converter

EMTP	Electromagnetic Transient Program
ESR	Equivalent Series Resistance
FB	Full Bridge
FC	Flying Capacitor
FRT	Ride Fault Through
FS	Function Switching
HS	Hybrid Switch
HB	Half Bridge
HVDC	High Voltage Direct Current
IAAC	Improved Alternate Arm Converter
IGCT	Integrated Gate-Commutated Thyristor
IGBT	Insulated-Gate Bipolar Transistor
LCC	Line Commutated Converter
LPOF	Low-Pressure Oil-Filled
MC	Mixed Cell
MCU	Micro-Controller Unit
MMC	Modular Multilevel Converter
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
MOV	Metal Oxide Varistor
MV	Medium Voltage
NL	Non-Linear Model
NLC	Nearest Level Control
OpAmp	Operational Amplifier
Ph	Physics model
PCB	Printed Circuit Board
PI	Proportional Integral
PLL	Phase Lock Loop
PR	Proportional Resonant

PMG	Permanent Magnet Generator
PD	Phase Disposition
POD	Phase Opposition
RMS	Root Mean Square
RSTR	Reduced Scale Test Rig
PWM	Pulsed Width Modulation
RES	Renewable Energy Systems
RS	Reference System
Si	Silicon
SiC	Silicon Carbide
SHE	Selective Harmonic Elimination
STATCOM	Static Synchronous Compensator
SBD	Silicon Body Diode
SCL	Short Circuit Level
SVM	Space Vector Modulation
TAC	Transition Arm Converter
THI	Third Harmonic Injection
THD	Total Harmonic Distortion
UN	United Nations
VCO	Voltage-Controlled Oscillator
WF	Wind Farm
WT	Wind Turbine
XLPE	Extruded Cross-Link Polyethylene

List of Symbols

C_{DCf}	DC filter capacitance
C_{cell}	Cell capacitance
$C_{cell_{DSTR}}$	Cell capacitance of reduced-scale test-rig
$C_{MMC_{eq}}$	Equivalent phase arm capacitance
$C_{cell_{qMMC}}$	Cell capacitance of qMMC
$cos\phi$	Power factor
Δt	Time step
E_{arm}	Energy of cell capacitor
E_{phase}	Arm energy requirement
E_{sw}	IGBT switching energy
f	Fundamental frequency
f_{DC_f}	Tuned frequency of DC filter
f_{eff}	Effective switching frequency of converter
H	Inertia
$I_{DC_{fault}}$	DC fault current during a pole to pole fault
$I_{DC_{ptg-fault}}$	DC fault current during a pole to ground fault
I_{igbt}	Rated IGBT current
$i_{j,k}$	Arm current
$i_{cell_{N,j,k}}$	Cell current

$i_{j,AC}$	Converter AC current
$i_{j,cm}$	Common-mode current
i_{DC}	DC current
$i_{j,DC}$	DC component of the common-mode current.
$i_{j,cc}$	Circulating current
K_{uti}	Utilisation constant of IGBT
K_T	Thermal correction for the switching losses
L_{arm}	Arm inductance
L_{AC}	AC-side inductances
$L_{arm-max_{AAC}}$	Maximum inductance value for AAC
$L_{arm-min_{AAC}}$	Minimum inductance value for AAC
$L_{arm_{DSTR}}$	Arm inductance of reduced-scale test-rig
L_{DCf}	DC filter inductance
M	Magnitude of modulation index
$m_{j,k}(t)$	Modulation index
$m_{DC-j,k}$	DC component of the modulation index
$m_{chain_{j,k}}$	Modulation index of chain-link
N_{DSTR}	Number of cells of reduced-scale test-rig
N	Number of cells in MMC
N^o_{MMC}	Number of voltage levels in an MMC
N^o_{EMMC}	Number of voltage levels in an EMMC
n	Number of IGBTs mounted on the same heatsink
n_s	Number of series connections of semiconductors
n_p	Number of parallel connections of semiconductors

ω	Angular frequency
P	Active power
P_{cond_S}	Conduction losses in IGBT
P_{cond_D}	Conduction losses in diode
P_{sw_S}	Total IGBT switching losses
Q	Reactive power
Q_{DC_f}	Quality factor of DC filter
R_{jS}	Junction to case thermal resistance
R_{cS}	Case to heatsink thermal resistance
R_{hs}	Heatsink to ambient thermal resistance
S	Apparent power
$S_{DS_{j,k}}$	Switching function of director switches
$s_{cell_{N,j,k}}$	Cell switching function
T_{amb}	Ambient temperature
T_S	IGBT switch temperature
T_D	Diode temperature
t_{over}	AAC overlap period
t_{pm}	Short conduction time of hybrid switch
V_C	Magnitude of Cell voltage
$V_{c_{tot}}$	Total arm cell voltage
V_{DC}	DC voltage
V_{AC_j}	Converter ac voltage
V_{ce}	IGBT collector emitter conduction voltage drop
$V_{loss_{cell}}$	Cell voltage drop

V_{chain}	Chain-link voltage
V_{igbt}	Rated IGBT voltage
V_{c-max}	Maximum value of cell capacitor voltage
V_{LL}	Line to Line voltage
$v_{j,cm}$	Common-mode voltage
$v_{cell_{N,j,k}}$	Cell voltage
$v_{arm_{j,k}}$	Arm voltage
$v_{j,diff}$	Differential phase arms voltage

Chapter 1

Introduction

1.1 Background

In 1992 in Rio de Janeiro, the United Nations (UN) stimulated the first motion to control anthropogenic interference in climate change, including the reduction in emissions of greenhouse gasses such as carbon dioxide (CO_2) [1]. In 1997, the Kyoto Protocol was agreed where each signatory committed to generating at least 20% of their country's power production from renewable energy systems (RES) [2]. As a follow up to the Kyoto Protocol, the Paris Agreement in 2015 placed further action on combating global warming [3]. One of the main contributions of the UN's treaties is decentralised energy production, generated from RES such as wind, tidal and solar energy harvesting, usually in remote locations [4]. As an example, Europe has great offshore wind generation potential in the North Sea, which is ideal for wind farms (WFs). A by-product of employing RES for energy production is the enabling of energy-sufficient states, countries or unions which can remove the reliance on fossil fuels [5]. Furthermore, electrical interconnection of multiple territories can increase the stability of regions which can be further expanded to economic and political levels. Examples of this include the EuroAsia [6] and EuroAfrica [7] Interconnections between Greece, Cyprus, Israel and Egypt. Additionally, by increasing energy production from RES, achieving power balance in future power systems will be a major challenge. Consequently, there is an increasing need to create multi-connections [8] between countries in order to match the continuous energy demand, and achieve optimal and flexible energy supply. Increased decentralised power generation creates the need for long distance, efficient energy transmission.

AC based transmission has inherent limitations including reactive power consumption, increased power losses over long lines, increased conductor cost due to skin effect, and inability to interconnect asynchronous systems directly [9]. The

utilisation of DC technology for energy transfer is considered to be a viable option as it allows multi-interconnections. However, the initial capital cost is considered to be much higher than that of AC transmission technology [10]. It is therefore only considered to be financial viable once the transmission distance exceeds a critical value, where the operational efficiency outranks the initial capital cost when compared to AC based technology [11]. Initially, high voltage direct current (HVDC) systems were based on current source converters (CSC), namely line commutated converters (LCC). However, due to the lack of flexibility in terms of grid synthesis and operation, and difficulties in realising multi-terminal grids using LCC, the industry and scientific community focussed attention on voltage source converters (VSC).

Before the renewable energy era, VSC were mainly used in motor drive systems and operated in controlled environments. Nevertheless, after the increasing growth of renewable energy penetration during the 1990s, the VSC was adopted as the main technology for interfacing wind turbines (WTs), satisfying grid code requirements such as voltage and current harmonic content, and providing ride-through capability. Consequently, incorporation of VSC in HVDC systems allowed increased operational flexibility such as independent control of the active and reactive power, fast power response, connection to weak networks, and start-up without the need for an external power source (black-start) [12]. The initial VSC HVDC topologies included the two-level and neutral-point clamped converters. Despite the limitations of early VSC, including high losses and voltage stress on the interfacing transformer, industry developed further VSC technology by introducing multilevel converters that are able to address the aforementioned limitations.

With the advent of multilevel VSC two main events revolutionised HVDC [13]. Firstly, the multilevel converter architecture allowed implementation of additional features such DC fault blocking operation and flexible DC voltage control, and facilitated development of new structural topologies of VSC, including the modular multilevel converter (MMC) and other hybrid variants such as the alternate arm converter (AAC). Secondly, the early VSC topologies were dependent on series connection of IGBTs. This technology was only offered by a single company (ABB) [14]. The multilevel structure removed the need for series connection of IGBTs resulting in the VSC-HVDC converter market being opened to other manufacturers such as Siemens [15], GE [16], and Mitsubishi.

1.2 Motivation

In order to synthesise and construct practical multi-terminal DC grids, several issues need to be addressed including power flow control, dynamic behaviour, system integration and DC fault ride through. Also, the implementation of the key equipment for HVDC grids has to be efficient in order to reduce the operational cost due to thermal losses in the passive equipment and semiconductor devices. Additionally, in order to reduce the initial invested capital cost, the equipment has to have a small footprint. The benefit of small footprint is key when the installation is in an environment with confined space, such as an offshore platform.

One of the inherent disadvantages of VSC when compared to LCC is DC fault tolerance. In LCC, thyristors which can withstand large DC surge currents are used. However, the VSC uses IGBT technology and cannot tolerate large fault currents. Moreover, DC fault current can develop rapidly and can reach very high values, depending upon the equivalent fault impedance, in only a few ms. Therefore, VSC based HVDC grids demand rapid fault blocking operation in order to protect the grid equipment.

There are three main, contenders for DC fault blocking equipment. The first is the DC circuit breaker (DCCB) which is an additional device incorporated into the system and whose only purpose is to block DC faults. The cost of this device increases significantly the initial capital cost of the HVDC grid as it does not provide any other functionality. However it is considered to be one of the key components for future meshed multi-terminal DC grids. The second is the 'DC transformer', which is a DC to DC converter that can interface different DC grids operating at different DC voltage levels. However, the 'DC transformer' increases both the capital cost and the operational cost, as they usually consist of two AC to DC converters. The third option, which is the subject of this thesis, is DC fault blocking through AC to DC converters. Although, AC to DC converters can achieve very fast blocking operation, the increased operational costs cannot yet justify such functionality. Moreover, blocking the AC to DC converter in a meshed grid immediately interrupts the power flow to other locations of the grid. In spite of this, AC-DC converters can be readily enhanced to incorporated features such as DC voltage controllability, reduced footprint, pole-to-ground fault ride through, unbalance operation, possible reduction of DCCBs requirements, and decreased initial capital cost of a multi-terminal DC grid. The additional functionality a reduced capital costs are traded against increased operational costs (losses). However, the functionality and the capital cost reduction potentially become even more significant and offer great advantages as the grid

is expanded. As multi-terminal operation tends to expand through countries and continents, various manufacturers may introduce different VSC technologies for the same DC grid. This introduces a new challenge regarding converter compatibility, as each manufacturer may be reluctant to share information regarding the accurate operation of each converter. This may lead to interoperability issues regarding the interactions of the controllers, due to different control and different hardware implementations. In the case of supergrid development, it is crucial to initially quantify and address such issues.

1.3 Scope

The main focus of the thesis is summarised as follows:

- Establish high fidelity and resource efficient HVDC converter models suitable for full-scale time-domain simulations, including various control layers, and thermal and loss models based on real converters currently produced by major manufacturers.
- Investigation of state-of-the-art multilevel HVDC converters, in terms of their efficiency, dynamic response and suitability for future HVDC grids. The comparisons establish the absolute steady-state operation limits of different multilevel HVDC converters.
- Investigation of state-of-the-art multilevel HVDC converters during transient operation, focusing on potential faulty and uncontrollable operation. The comparisons aim to establish the features and functionalities of each converter topology being considered.
- Development of novel topologies which address some of the shortcomings of the state-of-the-art HVDC converters.
- Development of a flexible low-voltage laboratory test set-up which can validate the aforementioned investigations and developments.

1.4 Thesis organisation

The thesis is organised according to Fig. 1.1 and the outline is presented as follows.

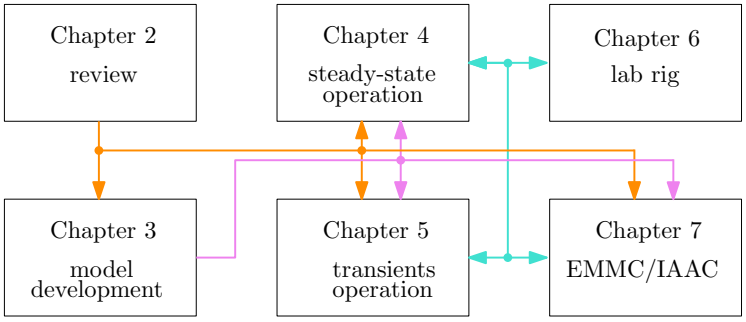


Figure 1.1: Thesis organisation.

Chapter 2 provides a thorough open-literature review of researched HVDC technologies. The review includes AC to DC and DC to DC converter topologies, HVDC grid architectures, transmission lines, and protection equipment such as DCCBs and DC choppers. The Chapter includes the necessary material related to HVDC energy conversion and the crucial equipment which is related to safe and robust HVDC grids.

Chapter 3 presents the mathematical analysis and model development of high fidelity, efficient time-domain models which were used in the course of the research studies documented in this thesis. Models include accurate representation of the semiconductor valves and control layers in order to reflect realistic transient-based simulation studies. The models developed were compared to assess accuracy computational overhead.

Chapter 4 investigates and analyses the absolute operational limits of state-of-the-art converters, including the capability to dynamically control currents and voltages for the AC and DC sides of an HVDC grid. The investigation includes the realisations of multilevel converters from various manufacturers, as well as converters with DC fault blocking capability. The investigation compares the converters according to efficiency, active and reactive power capabilities, AC and DC power quality, and the operational levels of DC link voltage.

Chapter 5 investigates the transient behaviour of converter topologies that are analysed in Chapter 4. The investigation highlights the operation during unbalanced AC grid, pole-to-ground and pole-to-pole DC faults, and the charging sequence from the AC and DC sides. Furthermore, an investigation was conducted on a modified converter in order to observe its ability to

limit DC fault current, in order to reduce the requirements of the DCCB technology.

Chapter 6 describes the development of a low-voltage laboratory test-rig which allows validation of selected offline simulation results through hardware tests. The experimental investigation also enables the limitations of a real-world implementation, rather than just a simulation, to be highlighted.

Chapter 7 presents a novel MMC for medium and high voltage applications. The EMMC achieves increased power quality with reduced numbers of cells. Simulations and experimental studies were used to validate the proposed converter and its feasibility was assessed by comparison with the conventional MMC. Furthermore, the novel topology was investigated for its appropriateness in medium voltage applications such as WT converters. Also the chapter proposes a novel multilevel converter which improves the AAC. The specific topology achieves functionalities and features similar to an AAC without the need for a DC filter. Converter functionality is validated through offline simulations, whilst DC fault blocking capability is also investigated.

Chapter 8 includes the conclusions of the thesis and summarises the findings, outcomes and contributions of this research work. Additionally, suggestions for potential future research are included.

1.5 Contributions

The main contributions of the thesis are the following:

- Detailed full-scale models of various HVDC converter topologies. Development of high fidelity computationally efficient models of HB-MMC, FB-MMC, MC-MMC, and AAC. Development of pragmatic controllers which offer realistic, practical voltage and current responses. Detailed design of realistic hardware implementation of various HVDC converters.

- Detailed comparison between a number of converter topologies, in terms of power losses, AC and DC power quality, and design considerations, beyond any existing in the open literature. Comparison of AC and DC power quality for various topologies and their variants. Exposure of the relationship between AC and DC power quality, quantifying the produced internal voltage and current harmonics and ripples, for various topologies and their variants.

- Comprehensive dynamic and transient capability assessments of the state-of-the-art converter topologies. Thorough investigation of realistic limitations and operation of various topologies, exposing design advantages and disadvantages regarding topological and controller realisations.

- Proposal of two new enhanced converter topologies for point-to-point and HVDC grids. The first new topology increases the power quality of MMC with reduced volume and complexity, and the second addresses fundamental disadvantages of AAC.

- Experimental validation of the proposed topologies and comparison with the existing topologies. Design of an efficient and flexible hardware demonstrator for use in a low voltage laboratory environment, to facilitate examination of the functionality, limitations and operation of different converter topologies.

1.6 List of publications

List of journal papers.

1. 'Steady-state performance of state-of-the-art modular multilevel and alternate arm converters with DC fault-blocking capability'. D. Vozikis, G. P. Adam, P. Rault, D. Tzelepis, D. Holliday, and S. Finney. International Journal of Electrical Power & Energy Systems, no. 3 (2018): 618-629.

2. 'Enhanced Multilevel Modular Converter With Reduced Number of Cells and Harmonic Content. D. Vozikis, G. P. Adam, P. Rault, O. Despouys, D. Holliday, and S. Finney'. IEEE Journal of Emerging and Selected Topics in Power Electronics. doi: 10.1109/JESTPE.2019.2904205

3. 'Single-Ended Differential Protection in MTDC Networks using Optical Sensors'. D. Tzelepis, A. Dysko, G. Fusiek, J. Nelson, P. Niewczas, D. Vozikis, P. Orr, N. Gordon, C. Booth. IEEE Transactions on Power Delivery, Vol. 32, No. 3, 30.06.2017, p. 1605-1615.

List of conference papers.

1. 'Fault blocking converters for HVDC transmission : a transient behaviour comparison'. D. Vozikis, P. Rault, D. Holliday, and S. Finney. 2018. 9th IET International Conference on Power Electronics, Machines and Drives, Liverpool, United Kingdom.

2. 'An Improved Alternate Arm Converter for HVDC applications'. D.Vozikis, G. P. Adam, D. Holliday, S. Finney. 2018. IECON 2018, Washington DC, United States.

3. 'Assessment of interoperability in multi-vendor VSC-HVDC systems : interim results of the Best Paths DEMO #2'. O. Despouys', P. Rault, A. Burgos, D. Vozikis, X. Guillaud, T. Larsson. 2018 CIGRE Session. Paris, 2018. B4-134.

4. 'Implementation of a dedicated control to limit adverse interaction in multi-vendor HVDC system'. P. Rault, O. Despouys, A. Petit, H. Saad, D. Vozikis, S. Gao, J. Freytes, D. Fonteyne, M. Zeller, P. Askvid. 2019. 15th IET International Conference on AC and DC Power Transmission, Coventry, United Kingdom.

5. 'Experimental results on interoperability in multi-vendor HVDC systems from Best Paths DEMO #2 project'. O. Despouys, P. Rault, C. Wikstrom, A. Burgos, J. Rimez, D. Vozikis, X. Guilluad. 2019. CIGRÉ International Symposium, Aalborg, Denmark.

6. 'Impact of VSC converter topology on fault characteristics in HVDC transmission systems'. D. Tzelepis, S. Ademi, D. Vozikis, A. Dysko, S. Subramanian, H. Ha. 2016. 8th IET International Conference on Power Electronics, Machines and Drives, Glasgow, United Kingdom.

7. 'Analysis of integration of multi-terminal HVDC network to weak grids'. Kamyab K. Givaki, Md H. Rahman, D. Vozikis, A. Giveki. 2018. 14th IET International Conference on AC and DC Power Transmission, Chengdu, China.

Chapter 2

State-of-the-art and future technologies for HVDC grids

2.1 Introduction

HVDC networks consist of a variety of equipment for safe and robust energy conversion and transmission. The expansion of HVDC networks and grids demands new equipment, which offers a variety of functionalities. Due to the nature of DC transmission, the effectiveness and efficiency of the system rely completely on the installed equipment. With the advent of high power density semiconductors it is possible to manipulate the electrical quantities, directing and constructing equipment that is tailored to the requirements of HVDC. This chapter reviews the equipment that is required for HVDC transmission, from simple to super grids. The review includes the equipment which is responsible for AC to DC, DC to AC and DC to DC energy conversion, the DC protection equipment and the transmission lines.

2.2 HVDC converters

This section includes a review of HVDC converter technology, which allows AC and DC network interconnection. The converter's primary operation is to convert the energy from AC to DC and vice versa, efficiently and safely [8]. Secondary features are desired, such as improved power quality, and AC-DC fault limitation and blocking, but without undermining the converter's primary operating features.

2.2.1 Diode rectifier unit

A diode rectifier unit (DRU) is an uncontrolled naturally commutated AC to DC converter, as shown in Fig. 2.1. The benefit of introducing DRUs in HVDC is the reduction of operational and capital costs by 20% and 30% respectively, compared to controllable converters [17]. Also the volume and weight requirements of the incorporated off-shore platform are reduced significantly, due to the absence of large passive components for energy conversion [17]. Furthermore, due to the simplicity of the circuit and the high robustness of the HV diodes, the design of a DRU is characterised by high modularity and reliability with low maintenance costs [18]. However, a DRU does not allow power reversal, while DC faults may jeopardise the stability of the AC system [19].

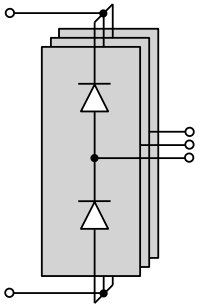


Figure 2.1: Diode rectifier unit.

2.2.2 Line commutated converters

Line commutated converters (LCC), shown in Fig. 2.2, are able to transfer bulk power up to 12GW between two points at 1100 kV [20]. Thyristor based technology allows higher power density converters compared to IGBT based VSCs. Furthermore, the device forward voltage is lower hence the total semiconductor losses are low.

Additionally, thyristors are robust devices capable of withstanding 6.2 kA during steady-state operation, while they have the ability to manage surge currents up to 140 kA. As a result LCC can manage and survive DC fault currents. Nevertheless, the LCC has several disadvantages [21]:

- In order to retain unity power factor under various operating conditions, during different thyristor firing angles, the converter consumes reactive power.
- Low frequency harmonic content in the DC and AC sides is high due to the nature of the thyristor-bridge rectifying operation. Passive filters are

necessary to attenuate the low frequency harmonics on the AC side to comply with the THD requirements, while high value DC reactors have to be incorporated to suppress the high magnitude DC ripple.

- Although the LCC semiconductors are of higher power density compared to VSC and the valve size is reduced, the necessity for reactive power compensation and AC/DC filtering increases the footprint dramatically compared to VSC. As a result, it is challenging to establish an LCC station on offshore platforms and in populated areas.

- To avoid commutation failures in the LCC valves, the converter has to be connected to a sufficiently strong network, to assist the valve current commutations with the appropriate AC voltage. An LCC cannot generate its own AC voltage, therefore it cannot be connected to passive systems or initiate the grid from zero voltage (black start).

- To achieve have power reversal in LCC systems, the DC voltage polarity has to be reversed. This function is restrictive in multi-terminal LCC operation as the coordination of the converters is challenging. Additionally, to support DC voltage reversal, oil impregnated cables have to be installed, which have increased cost and which are considered to pose increased risk to the environment.

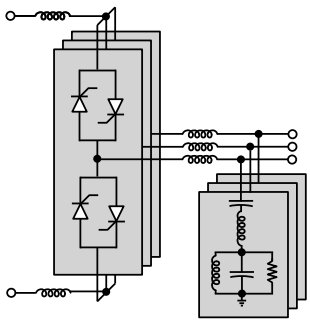
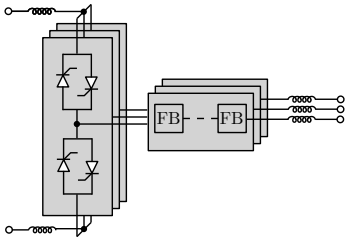


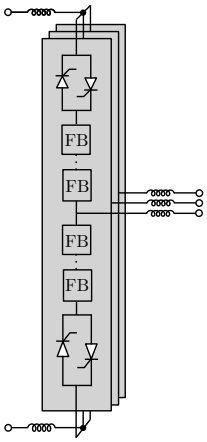
Figure 2.2: Line Commutated Converter.

To allow the LCC operate in weak grids, active voltage injection is necessary to achieve power factor correction. The capacitor-commutated converter (CCC) offers a passive approach to address this issue, but it has been shown that voltage injection lacks controllability and leads to commutation failure following grid faults [22]. A more sophisticated solution involved the combination of an LCC with an active filter, where the LCC and filter can be combined in different ways to offer design trade-offs between active and reactive power capabilities, operational

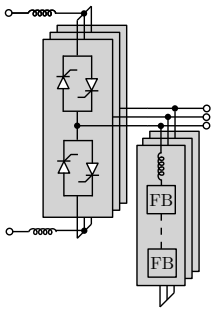
cost and sizing of the active filter. The topologies in Figs. 2.3(a) [23] and 2.3(b) [24] require only low voltage rated FB cells, compared to those in Figs. 2.3(c) [25] and 2.3(d) [26]. However, the topologies in Figs. 2.3(c) and 2.3(d) increase the LCC's active and reactive power capabilities. The topologies in Figs. 2.3(a),



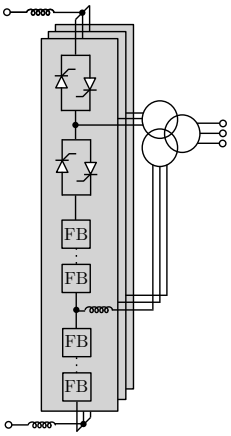
(a) LCC with AC side FB chain-link



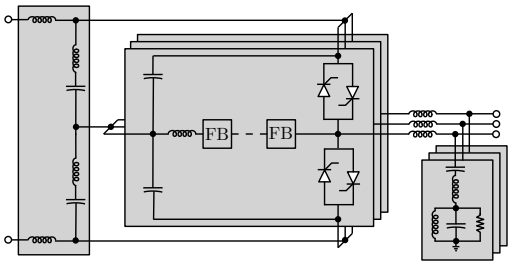
(b) LCC with DC side FB chain-link



(c) LCC with shunt FB chain-link



(d) LCC in series with FB chain-link



(e) LCC with active forced commutated FB chain-link

Figure 2.3: LCC hybrid topologies.

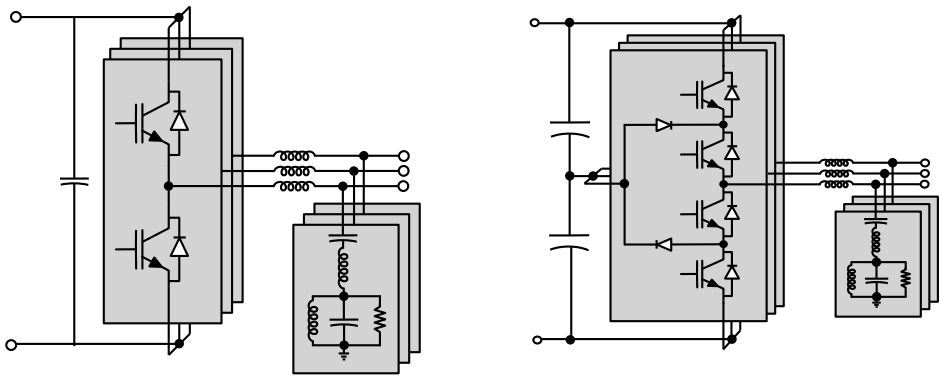
2.3(b) and 2.3(d) allow control of the DC voltage, whilst the topologies in Figs.

2.3(b) and 2.3(d) reduce the thyristor voltage requirements. Finally, the topology in Fig. 2.3(e) achieves active and reactive power capabilities similar to a VSC while it has better efficiency than a multilevel VSC and can manage DC pole-to-pole faults [27].

2.2.3 Two and three level voltage source converters

The basic structures of two-level and three-level neutral-point-clamped converters are illustrated in Fig. 2.4 [28]. The two-level converter was the first realisation of a VSC to be used in HVDC applications, but it was succeeded by the three-level converter which offered better harmonic performance. Both converters require series-connected IGBTs, achieving IGBT valves with blocking capability up to 600 kV [29]. In the two-level converter the upper and lower IGBT valves switch in a complementary manner with an intermediate dead-band to prevent short-circuits. The frequency of the switching pattern is dictated by comparison of high-frequency triangular carrier and sinusoidal reference waves.

The result of this comparison is a high-frequency pulse train, which is fed to the valves resulting in generation of a square-wave AC voltage. As the current generated by the converter has a similar shape to the voltage, a series inductor placed on the AC side acts as a low-pass filter to reject high-frequency components and enable production of sinusoidal AC currents. Three-level converters, such as the neutral-point-clamped converter, have similar operation but, instead of having only two voltage levels, can also produce zero AC voltage, allowing better harmonic performance and reduced filter requirements.



(a) Two-level converter (b) Neutral-point-clamped converter

Figure 2.4: Non-modular early VSC topologies for HVDC.

Compared to the LCC, the VSC has desirable characteristics such as suitability for connection to weak networks, reduced footprint, and full active and reactive power capabilities.

However, early realisations of HVDC VSC introduced the following disadvantages [21].

- Early VSCs required a DC filter capacitor across the DC link, which increased the fault current levels during DC faults.
- Operation of high numbers of series-connected IGBTs demands simultaneous switching of the semiconductors. For high-voltage operation there are hard physical limits regarding the switching frequency and achievable total blocking voltage.
- The generation of high dv/dt due to the high voltage switching operation generates electromagnetic interference (EMI) and increases the filter requirements, and also impacts upon the insulation requirements of the AC interface transformer.
- Series connection of IGBTs introduces large stray inductance. Hence overvoltages are generated due to high di/dt.

2.2.4 Multilevel voltage source converter

The multilevel VSC addresses the demanding AC and DC filter requirements, and the high dv/dt and di/dt that are characteristic of two and three level converters [30]. Multilevel converters generate voltages by switching on an off small portions of the total DC voltage with the help of sub-circuits that can temporarily store energy for such a function. This allows generation of high-fidelity, near-sinusoidal voltages, reducing the harmonic content, transformer insulation requirements, overvoltages due to di/dt, and EMI. Furthermore, the DC-side filter is reduced or may even be removed. Multilevel converters do not require series-connected IGBTs for their operation, opening the market to other manufacturers to produce such converters.

Cell topologies

The key sub-circuit for HVDC multilevel converters is the cell circuit. An arrangement of series-connected cells creates a cell chain-link which allows creation of high-fidelity waveforms. There are numerous cell topologies, with each designed

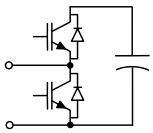
to achieve specific requirement regarding the functionality, efficiency, redundancy and complexity [31].

Fig. 2.5 illustrates the cell topologies that are used for multilevel converters. The cells are categorised as unipolar, and symmetrical or asymmetrical bipolar cells. Unipolar cells can achieve two to three levels of single polarity voltage (0, V_C, $2V_C$), whilst bipolar cells can achieve three to five symmetrical double polarity voltages ($2V_C$, -V_C, 0, V_C, $2V_C$) or four asymmetrical double polarity voltages (-V_C, 0, V_C, $2V_C$), assuming that all cell capacitor voltages are well balanced.

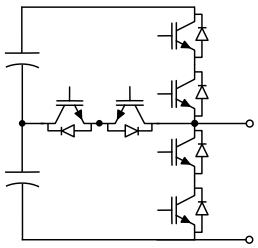
Unipolar cells have a reduced number of semiconductors in the conduction path, hence efficiency is higher when compared to bipolar cells. Nevertheless, the use of unipolar cells does not allow the converter to operate with DC voltage below the critical peak line-to-line AC voltage (rectification voltage). Furthermore, due to their incapability of producing negative voltages, it is not possible for unipolar cells to contribute to limiting or blocking DC faults. By utilising three-level type cells, such as T-type (Fig. 2.5(b)) [32], flying capacitor (Fig. 2.5(c)) [33], neutral-point-clamped (Fig. 2.5(d)) [34], and double HB (Fig. 2.5(e)) [35], it is possible to reduce weight and capital cost by reducing the number of isolated DC power supplies and gate drivers required by the cells. However, flying-capacitor cells compromise the reliability and modularity of the converter due to different operational voltages across each capacitor. Also, T-type and active neutral-point clamped cells require more complex capacitor voltage balancing algorithms. In addition they suffer from limited switching state redundancy, which leads to increased voltage ripple. In each case, the three voltage levels can only be produced by certain switch combinations. However, the double HB cell, shown in Fig. 2.5(e), can achieve lower losses compared to two conventional HB cells, shown in Fig. 2.5(a) and, unlike the other unipolar cell topologies, does not require a bypass safety thyristor [35]. Lastly, the unipolar-double-clamped cell, shown in Fig. 2.5(f) [34], offers fault blocking capability. At first such a function seems to be attractive, but the increase in losses without the provision of any extra functionality cannot be justified.

Bipolar cells, shown in Fig. 2.5(g) to 2.5(i), have a higher number of conducting semiconductors hence the conduction losses are higher than for unipolar cells. However, their ability to produce negative voltages can be exploited and over-modulation can be achieved, allowing an increased control range of the DC voltage for any given AC voltage [36]. Inclusion of sufficient bipolar cells in a converter provides DC fault blocking capability.

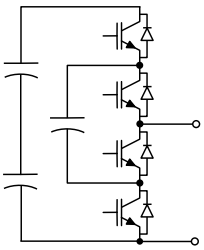
Compared to asymmetrical bipolar cells, symmetrical bipolar cells such as



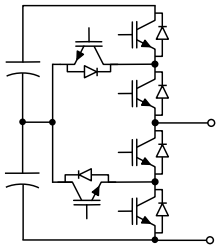
(a) Unipolar 2-level HB



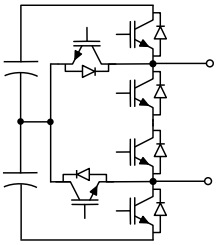
(b) Unipolar 3-level T-type



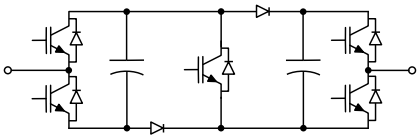
(c) Unipolar 3-level flying capacitor



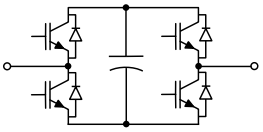
(d) Unipolar 3-level active neutral-point clamped



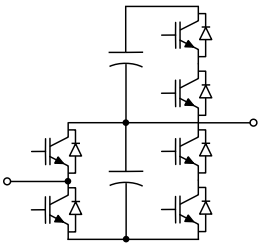
(e) Unipolar 3-level double HB



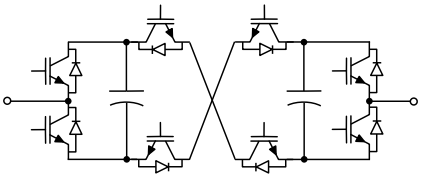
(f) Unipolar 3-level double-clamped



(g) Symmetrical bipolar 3-level FB



(h) Asymmetrical bipolar 4-level



(i) Symmetrical bipolar 5-level cross-connected

Figure 2.5: Cell topologies.

FB and five-level-cross-connected cells, shown in Figs. 2.5(i) [34] and 2.5(g) [37] respectively, enable a greater range of DC voltage control as they produce the same number of positive and negative voltage levels.

Converter topologies

MMCs, as shown in Fig. 2.6, can be realised by using a combination of different types of cells. This facilitates performance optimisation and leads to a range of hybrid multilevel converter designs.

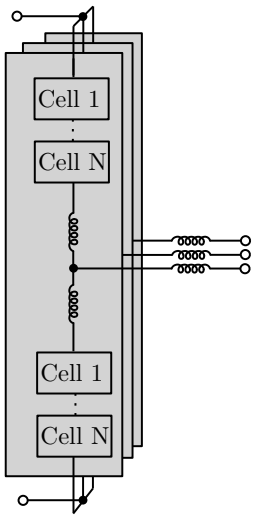


Figure 2.6: Modular multilevel converter.

Most of these hybrid converters were motivated by the design trade-offs between DC fault ride-through, efficiency and footprint. In the broader context, MMCs and hybrid converters that employ asymmetrical and symmetrical bipolar cells, or a mixture of different cells, achieve DC fault blocking and greater control flexibility at the expense of higher semiconductor losses compared to those employing only unipolar cells. Other hybrid multilevel converters, such as AAC and hybrid cascaded two-level converters, use bipolar cells, with director switches (DS) that operate at extremely low-frequency to achieve DC fault blocking capability at reduced footprint and semiconductor losses. The MMC consists of arrangements of two chain-links per phase, operating in complementary mode, synthesising high-fidelity AC waveforms. The benefits of such a topology include:

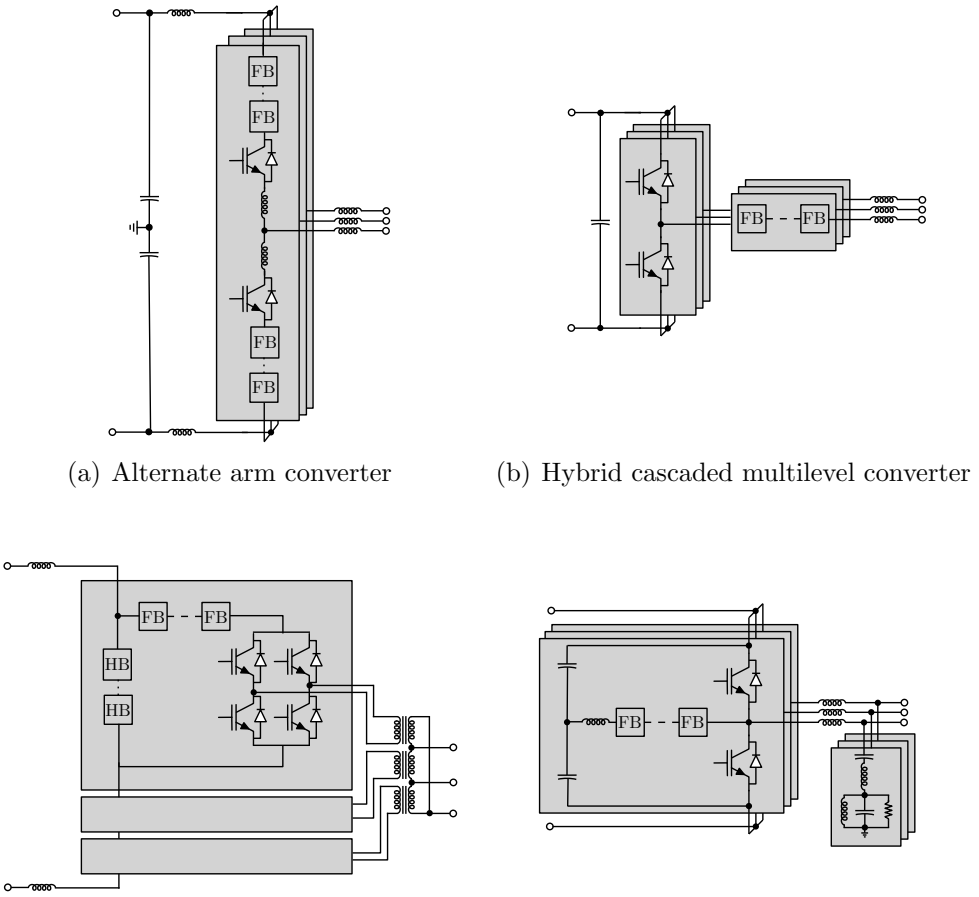
- No DC link filter capacitor. Each cell provides distributed and shared energy storage for each voltage step. Modular design, simplifying construction and maintenance, and without the need for series-connected semiconductors.

- The internal circuit may operate at relatively low switching frequency (<200 Hz) allowing low complexity cells.
- Very low total harmonic distortion (i.e. dv/dt), hence the removal of the need for AC filters. Standard transformers (i.e. no special insulation requirements) may be used.
- Tailored functionality according to grid requirements by installing different ratios of unipolar/bipolar cells.

However, an MMC has the following inherent disadvantages. Due to the low-frequency voltage ripple on the cell capacitors, the cell energy storage requirement is increased hence the size and the volume of each cell is high. The consequent increase in weight means that valves cannot be suspended from the roof of the converter hall, as with two-level converters and LCC. Valves are therefore more prone to ground faults. Furthermore, the additional functionality offered by inclusion of bipolar cells is traded against the increased capital and running costs due to the increased number of semiconductors.

The AAC [38], illustrated in Fig. 2.7(a), consists of an arrangement of a chain-links in series with a DS formed by the series-connection of IGBTs. For a given DC link voltage, an AAC requires a lesser rated arm chain-link voltage compared to an MMC, leading to a smaller footprint [38]. Furthermore, the discontinuous arm current in the AAC provides reduced conduction losses even though FB cells are incorporated.

Similar in operation to the AAC is the hybrid cascaded multilevel converter [39], shown in Fig. 2.7(b), where the FB chain-link is established on the AC side of the converter. This converter may therefore provide potential footprint reduction and reduced semiconductor losses compared to an FB-MMC. Even though the AAC provides some promising features, it suffers from lower power quality and limited reactive power capabilities for a specific efficiency when compared to an MMC. Additionally, the necessary DC filter discharges during DC faults, leading to higher DC fault currents. The hybrid multilevel converter with half-bridge chain-links across the DC link [40] is illustrated in Fig. 2.7(c). Each HB chain-link generates a rectified voltage waveform at the input of each H-Bridge cell. Initially this concept allowed a reduced footprint for the total converter. However, in order to have full control of the AC voltage it is necessary to incorporate an FB chain-link between the HB chain-link and the H-Bridge, resulting in increased conduction losses. The controlled transition bridge (CTB) [41] illustrated in Fig. 2.7(d), potentially offers a reduced footprint and similar semiconductor losses compared to an HB-MMC, but it requires a DC filter.



(a) Alternate arm converter

(b) Hybrid cascaded multilevel converter

(c) Hybrid multilevel converter with HB chain-link across DC link

(d) Controlled transition bridge converter

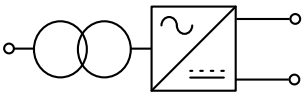
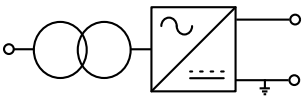
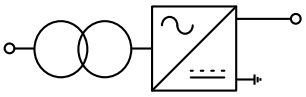
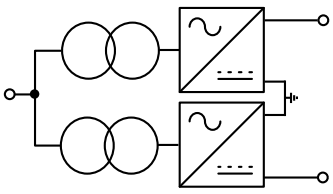
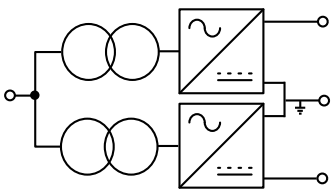
Figure 2.7: Hybrid multilevel converters.

Table 2.1 shows various VSC configurations with their associated return paths [42]. Their main advantages and disadvantages, mainly in terms of cost, fault path, redundancy, and environmental impact, are highlighted.

2.2.5 DC-DC converters

DC-DC converters may be a key technology for interfacing multi-terminal HVDC grids and providing additional features such as DC fault blocking. DC grids may, in future, be expanded or interconnected to include sections that operate at different voltage levels, and DC-DC converters may be the catalyst that enables this [43]. DC-DC converters are also expected to have a crucial role in managing and protecting the DC grid during DC faults, thereby resulting in a reduction in

Table 2.1: VSC configurations and return paths.

VSC configuration	Advantages	Disadvantages
(a) symmetric monopole 	Transformer is not exposed to an increased DC voltage offset during DC pole-to-ground faults. No DC pole-to-ground fault current. AC grid does not contribute to DC pole-to-ground faults	Requirement of fully rated DC cables, hence increased cost. Limited redundancy.
(b) asymmetric monopole with metallic return 	Metallic return needs less insulation. No DC pole-to-ground fault current. Can be upgraded to bipolar.	Transformer is exposed to DC voltage stresses. Limited redundancy.
(c) monopole with ground return 	Cost and line losses are reduced. Can be upgraded to bipolar	Transformer is exposed to DC voltage stresses. Limited redundancy. AC grid contribute to DC pole-to-ground faults. Environmental concerns due to the use of grounding electrodes.
(d) symmetric bipolar with ground return 	50% redundancy.	AC grid contributes to pole-to-ground faults. Transformer is exposed to DC voltage stresses. Environmental concerns due to the use of grounding electrodes.
(e) symmetric bipolar with metallic return 	50% redundancy. Increases transmission capacity without changing the DC voltage rating.	Transformer is exposed to DC voltage stresses. It requires an additional low-voltage DC conductor. DC return path must be fully rated to achieve 50% redundancy.

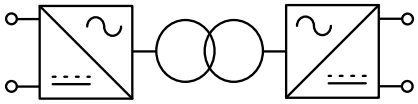


Figure 2.8: Isolated DC-DC converter.

installed DCCBs [44]. In a general an HVDC DC-DC converter is constructed by connecting DC-AC and AC-DC converters as shown in Fig. 2.8.

The interfacing transformer provides galvanic isolation where each DC grid zone will operate with a dedicated ground plane. As the interfacing transformers are not connected to any AC grid, the fundamental AC frequency can be much higher than 50-60 Hz, hence the volume of the transformer can be reduced. Also simpler modulation schemes can be used, e.g. trapezoidal modulation. Even though high-frequency operation reduces the size of the passive components and equipment, the impact of high-step, high-frequency dv/dt may jeopardise the insulation of the transformers. Furthermore, low-order harmonics may have greater impact on the power transfer. When designing a DC-DC converter the following should be considered [44]:

- Use of an interfacing transformer introduces galvanic isolation. This allows better utilisation of the semiconductor devices, especially on the high DC voltage side converter.
- An interfacing transformer prevents propagation of DC faults through the DC-DC converter.
- DC converters should match different DC voltages. Nevertheless, they should control the DC voltage and the DC power at each end.
- dv/dt should be minimised and controlled to avoid stressing the interfacing transformer.
- The AC fundamental frequency internal to the DC-DC converter should be maintained low, e.g. below 1 kHz, to limit switching losses and mechanical stresses on the interfacing transformer.
- A full positive modulation index is required for each side of the converter to achieve black-start functionality and re-start following a DC fault.

Many HVDC DC-DC structures are based on existing AC-DC converter topologies which are connected through a high frequency transformer. For example, the dual active bridge (DAB) DC-DC converter, shown in Fig. 2.4(a), is created by connecting two two-level converters through the interfacing transformer.

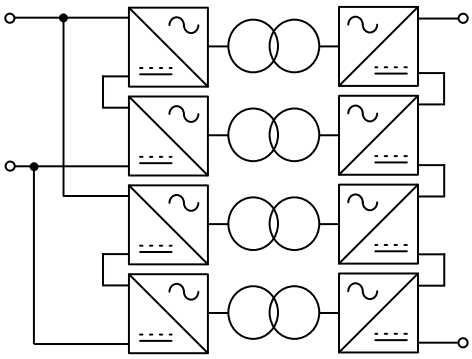


Figure 2.9: Modular DC-DC converter arrangement.

Although the DAB provides a reduced footprint, it is limited by the series-connection of semiconductors as well as an increased dv/dt. An alternative to the DAB is the modular topology illustrated in Fig. 2.9, which allows high voltage operation to be achieved by series-connection of DC-DC converter modules, where each module is rated according to a single semiconductor device. The main disadvantage of this arrangement is the increased number of transformers and the dedicated high voltage insulation levels for each transformer.

The CTB converter, based on the topology of Fig. 2.7(d), subjects the interfacing transformer to reduced stresses compared to DAB. However, as with the two-level converter, the DC filter contributes to the DC fault current levels. The MMC and the transition arm converter (TAC), based on the topologies in Figs. 2.6 and 2.10 [45] respectively, provide reduced dv/dt by incorporating a trapezoidal modulation waveform so that the cell capacitor size can be reduced. Furthermore, the TAC offers reduced semiconductor footprint.

AAC and cascaded two-level converters illustrated in Figs. 2.7(a) and 2.7(b)

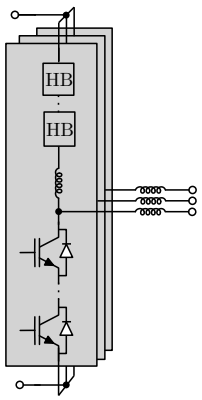
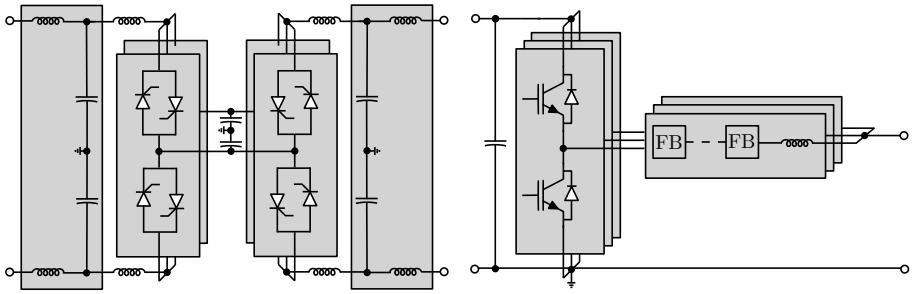


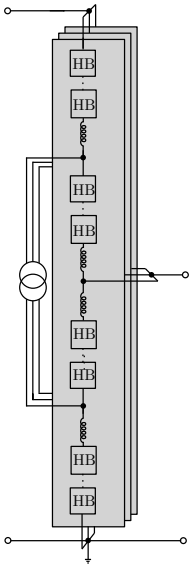
Figure 2.10: Quasi two-level DC-DC converter based on trapezoidal AC waveform.

respectively, are not suited for use in HVDC DC-DC converters as the increased losses they incur are not sufficiently offset by their DC fault blocking capability. Moreover, the required DC filter capacitor increases the potential DC fault current. If galvanic isolation is not required, resonant DC-DC converters, as shown in Fig. 2.11(a), may be considered [46]. The absence of an interfacing transformer is an attractive feature due to cost and volume reduction. However, their reduced DC power quality, increased component sizing and additional passive filtering requirements are undesirable. Furthermore, during high DC voltage mismatch between the input and output, high AC circulating currents flow which increase the reactive energy circulation, and therefore losses. The hybrid cascaded DC converter, shown in Fig. 2.11(b), provides an attractive alternative for transformerless operation [47]. However, due to the incorporation of FB cells, semiconductor losses are increased while the DC filter increases the DC fault cur-



(a) Resonant DC converter

(b) Hybrid cascaded DC converter



(c) DC auto-transformer

Figure 2.11: Non-isolated DC-DC converter topologies.

rent levels. The DC autotransformer shown in Fig. 2.11(c) provides an efficient alternative [48]. To prevent DC fault propagation, FB cells must be incorporated and this leads to increased losses.

2.3 Power flow controllers

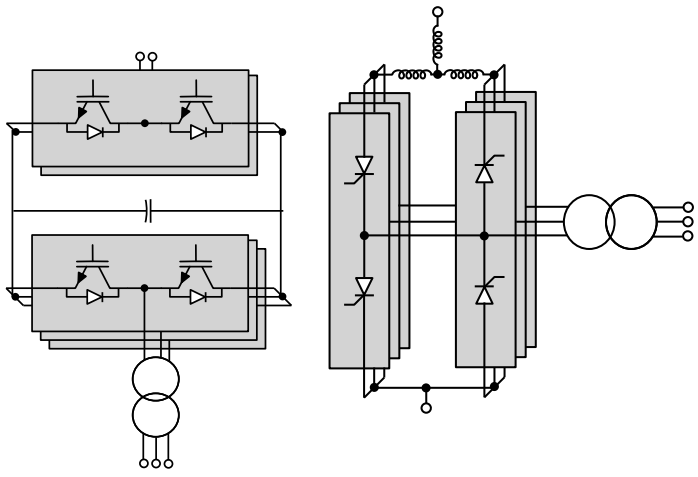
In a meshed multi-terminal DC grid the current flow is driven through the existing resistance of the conductors. A power flow controller (PFC) is a device that can dictate the required current flow to avoid overloading of the conductors.

Simple DC power flow control can be achieved by using a controlled variable resistor, but this has a limited range of control and increases power losses [49].

Another solution is to incorporate back-to-back converters which are powered through the AC side, as shown in Fig. 2.12. The back-to-back converter PFC regulates the power flow by adjusting the voltage which is applied to the DC side conductors. However, AC-DC PFCs require an extra transformer, while the semiconductors have to be rated for the DC voltage, which increases the power losses [50].

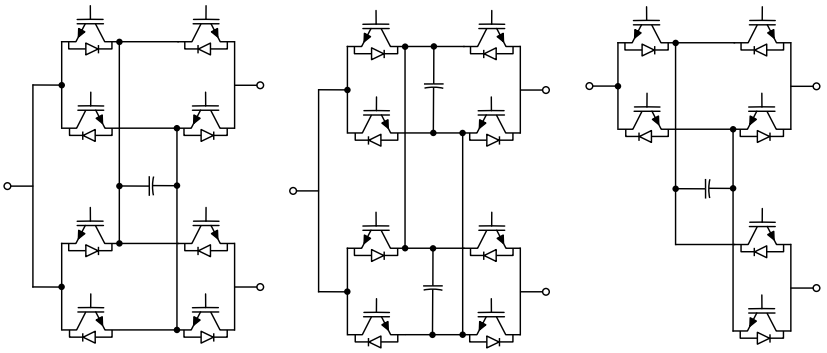
DC-DC converters can be employed as PFCs. However the increased volume and number of semiconductors that a DC-DC converter requires does not justify its explicit operation as a PFC [51].

To avoid excessive component sizing and losses, the current flow controllers (CFC) can be employed, as shown in Fig. 2.13. The CFC does not require

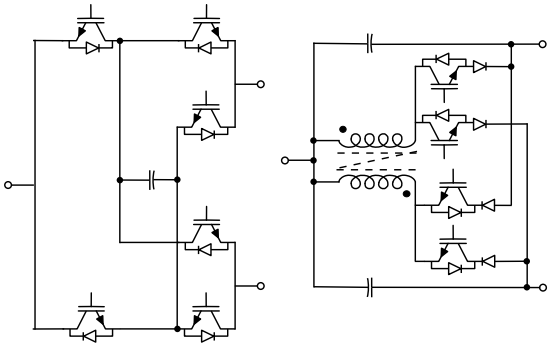


(a) IGBT based PFC (b) Thyristor based PFC

Figure 2.12: Voltage based power flow controllers.



(a) CFC variation 1 (b) CFC variation 2 (c) CFC variation 3



(d) CFC variation 4 (e) IDCPFC

Figure 2.13: DC current flow controllers.

a transformer and the voltage requirement is low [52]. As a result a CFC has a small footprint and low losses. The main CFC structure consists of an FB topology for each DC conductor path, as shown in Fig. 2.13(a) and 2.13(b). Figs. 2.13(c) [53], 2.13(d) [54] and 2.13(e) [55] show variations of CFCs with reduced conduction paths and complexity.

2.4 Protection equipment

Amongst the biggest challenges in HVDC systems are the safe interruption of DC faults and system recovery back to normal operation following fault clearance. Converters that have the ability to block DC faults are considered as good candidates for such an operation as they can rapidly produce a counter voltage to interrupt the DC fault current. However, such operation also immediately interrupts power flow. Therefore, converters with DC fault blocking capability are not considered to be an ideal candidate for meshed DC networks. However, connecting DCCB at the DC nodes of meshed DC grids allows isolation and clearance of

DC faults. However, DCCB have a much more difficult task compared to those in AC systems. DCCBs are required to interrupt a fully developed DC fault current which does not have a natural zero current crossing point. The resulting high di/dt can result in destructively high voltage levels. Usually, AC breakers achieve current interruption the moment that the AC current passes through zero, and the generation of high voltages is therefore avoided. DCCB require two main functionalities to operate. The first is creation of a counter voltage to oppose the rapid di/dt caused by the DC fault. The mechanisms and architectures for achieving this define three main categories of DCCB: solid-state, resonant, and hybrid. The second requirement is for the DCCB to withstand the breaking energy and dissipate it safely without jeopardizing DC grid equipment. As a result, the main duties of the DCCB are to [56]:

- withstand the normal operating DC currents during steady-state and dynamic operation.
- apply and withstand a counter voltage for extinguishing DC fault currents.
- withstand and dissipate the fault energy safely.
- allow relatively quick system restart following fault clearance.

Another significant challenge to the realisation of DCCB is cost. Since DCCBs are required at each network node, the cost increases as the network is expanded. Running cost is dependent upon the circuit breaker design. DC fault currents propagate very quickly, so the time between detection and interruption must be very short in order to protect the rest of the DC grid equipment (converters). However, this requirement is again grid-dependent, since expanding the grid by including more lines and interconnections increases the total energy stored in the equivalent line capacitance, resulting in increased DC fault current levels. Furthermore, each converter topology may employ DC filters (capacitance) further increasing fault current levels. Even with state-of-the-art DCCB technology, which may achieve interruption speeds of 3 ms, this may not be sufficiently fast as the grid is further expanded. A DCCB must therefore meet the major challenges of fast DC fault interruption, irrespective of the amount of energy stored in the DC grid, and have low capital, running, maintenance and upgrade costs. Unlike a conventional converter, a DCCB only performs a single function, which is to block DC pole-to-pole faults. The high costs incurred in achieving this limited functionality make the feasibility of DCCB questionable.

2.5 DC breaker topologies

A DCCB may be realised using different topologies including solid-state based, resonant, and hybrid.

2.5.1 Solid-state DC breakers

The solid-state DCCB, illustrated in Fig. 2.14, consists of semiconductors to interrupt the DC fault current, and metal-oxide varistors (MOVs) to absorb the breaking energy. The solid-state DCCB does not have any mechanical or moving parts, resulting in high-speed fault interruption. The most common design for a solid-state DCCB is a string of series connected bidirectional switches (realised using IGBTs) rated at the pole-to-pole DC voltage, with parallel-connected surge arresters to absorb and dissipate the breaking energy. During the steady state, current flows through the antiparallel diodes according to the current direction. When the breaker is tripped, all switches are turned-off and the voltage across the string of switches rises. When this breaking voltage reaches the DC link voltage, current is driven into the MOVs. The main advantage of the solid-state breaker is its reaction speed due to the use of semiconductors. However, the voltage drop across the series connected switches during steady-state operation is high due to the large number devices required. This results in high losses. Each solid-state DCCB incurs approximately the same losses as an HVDC converter [57]. Deployment in a meshed grid, therefore, would significantly increase operating costs.

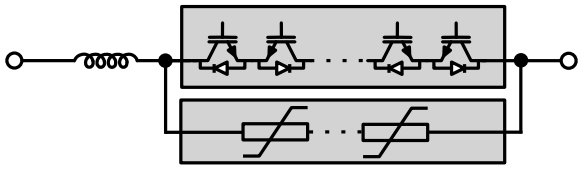


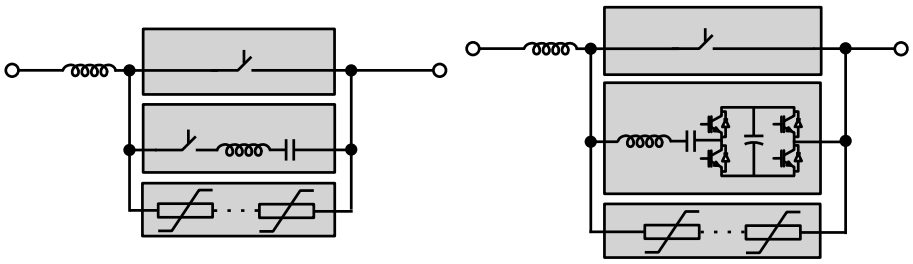
Figure 2.14: Solid-state DCCB.

2.5.2 Resonant DC breakers

Resonant DC breakers extinguish the DC fault firstly by forcing the DC current to oscillate (resonate) around zero, imitating AC current, and then interrupting the current as it crosses through zero. In its most basic form, a resonant DC breaker consists of an AC circuit breaker in parallel with a resonant LC circuit. A parallel-connected MOV is also included to absorb the breaking energy. The

main steady-state current path switch can be formed using thyristors or IGBTs to support only low-voltage during normal operation. As a result, the total operating losses are not significant. However, since operation is dependent upon the development of the oscillations and on mechanical interruption, the total breaking timing exceeds that of a solid-state breaker.

Resonant breakers may be active or passive. The passive resonant breaker, shown in Fig. 2.15(a), relies upon the build-up of the oscillatory current according to the characteristics of the arc and the LC network. However, this method considered to be too slow for VSC-HVDC grids [58]. The active resonant breaker relies on an active development of the oscillatory current through a charge capacitor, an external AC source or active voltage pulses, as shown in Fig. 2.15(b) [59, 60]. The time taken for the oscillatory current to develop is less than for the passive resonant breaker [61], but the capital cost of the active resonant breaker has increased due to the extra equipment that is needed to create the active oscillations. Resonant breakers have much lower construction cost compared to solid-state breakers as current interruption is achieved with a mechanical AC breaker. Also, in active resonant breakers, the power semiconductors that are required for the active pulses can be rated in the range of a few kV, hence the total footprint of such a breaker can be small.



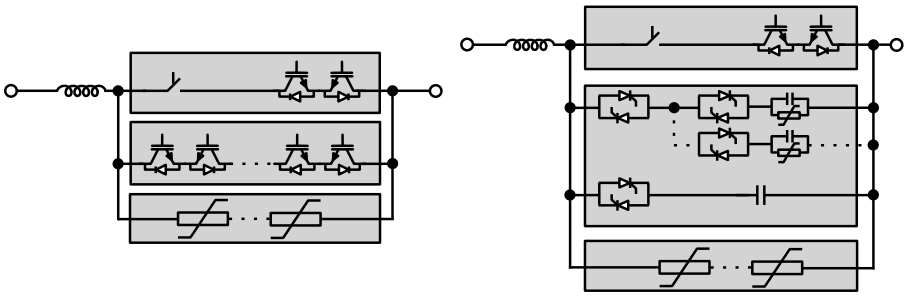
(a) Passive resonance DCCB (b) Active resonance DCCB

Figure 2.15: Resonant DCCB.

2.5.3 Hybrid DC breakers

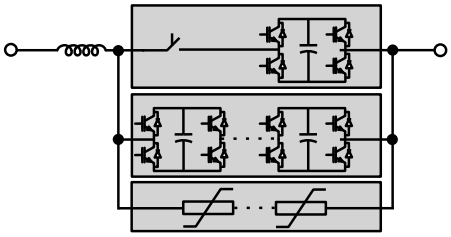
Hybrid DCCB combine the use of fast switches, as found in resonant DCCBs, with the breaking capability of solid-state DCCBs. The fast switch is connected in parallel with the breaking semiconductor branch. MOVs are connected in parallel to absorb the breaking energy. Hybrid breakers achieve the steady-state efficiency of resonant converters and the breaking capability of solid-state breakers. However, the hybrid DCCB is not as fast as it is solid-state [62]. The breaker

semiconductor branch must be sized according to the DC link voltage. This is achieved by series-connection of semiconductor switches. Changes to the semiconductor arrangement results in hybrid breaker variants. The most common arrangement consists of single bidirectional switch (realised by using IGBT) for the fast and the breaking branches, shown in Fig. 2.16(a) [63]. Other arrangements including, for example, thyristors, are shown in Fig. 2.16(b) [64], or FB cells as shown in Fig. 2.16(c) [65]. The hybrid breaker can achieve breaking times of 4-5 ms, which is promising for VSC-HVDC based grids. However, due to the large number of semiconductors required the initial capital cost of the breaker is high.



(a) IGBT based hybrid DCCB

(b) Thyristor based hybrid DCCB



(c) FB based hybrid DCCB

Figure 2.16: Hybrid DCCB.

2.5.4 DC fault current limitation

Following expansion of the DC grid, the fault current level is increased requiring reduced circuit breaker operating times. The capability of a given DCCB technology may have a hard limit with regards to communication, protection and breaking speeds. One solution is to limit the rise time of the DC fault current to increase the time available for a DCCB to react. Furthermore, as previously mentioned, breaking speeds and cost are directly linked. As a result, by allowing

slower DC fault current interruption the running and capital cost may decrease. One approach to current limiting is installation of DC current reactors, which delay the development of DC fault current. However, only relatively high values of DC reactor can delay the fault current sufficiently, and they are effective only during the first stages of the fault [66]. Moreover, DC reactors with very large inductance may be problematic due to the interactions with the outer controllers of the converters in the DC grid. Superconductors can be employed to imitate the operation of variable resistance during a fault. During the development of the DC fault current, the temperature of the superconductive connector increases, resulting in higher resistance and partial limitation of the current [67]. Although this approach is promising, it is dependent upon the reliability and efficiency of the associated cooling system.

2.5.5 DC chopper

A controlled dynamic braking resistance (DC chopper), as shown in Fig. 2.17, is needed in DC grids in case of abnormal energy influx [68]. In the case of a DC grid connected to a WF, which may not incorporate any active power control, unregulated energy transfer may result in overvoltage and potential insulation failure. The DC chopper absorbs the energy excess in the DC grid, avoiding any harmful overvoltage. There are various designs of DC chopper, including HB or FB topologies with combinations of batteries or super-capacitors for enhancing the transient operation of the grid.

DC chopper sizing must cater for the worst case scenario, which is the absorption of the maximum energy supplied by the Wind Farm. Furthermore, DC choppers can be employed for fault ride through of pole-to-ground faults. Due to the voltage collapse of one pole relative to ground, a pole-to-ground fault jeopardises the insulation of the DC lines and the converter transformer. By enabling the DC chopper connected to the healthy pole, the voltage seen at the healthy pole is controlled to be half of the pole-to-pole voltage, i.e. it is maintained at

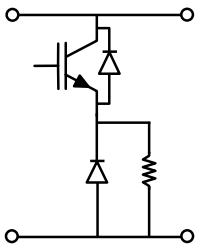


Figure 2.17: Equivalent circuit of DC chopper.

its normal operating value. This protects the cable insulation and also prevents any destructive DC offset from appearing at the AC side of the converter, i.e. applied to the transformer. Although DC choppers are considered back-up protection equipment, they increase the capital cost of the DC grid. Moreover, they demand increased space and volume which is problematic in remote areas, such as offshore platforms, where space is at a premium.

2.6 Transmission lines

For HVDC transmission, both cables and overhead lines can be used. The cost of cables is higher than overhead lines but in VSC applications, the latter may still be preferable due to the following characteristics [21]:

- The environmental impact of cables often is less than that of overhead lines.
- VSC can reverse power flow without the need of DC voltage reversal. This allows single polarity cables which have reduced cost and are simpler to construct, e.g. XLPE DC cables.
- Cables are less prone to faults than overhead lines.
- Permanent faults are easier to repair on overhead lines.
- In the case of cables, the power outage may be prolonged as the repair time might be significant.

Most existing VSC HVDC links incorporate cables with only one project (ULTRANET) planned to have overhead line.

2.6.1 Cables materials

The choice between cables is often influenced by environmental constrains as well as considerations regarding total capital cost and system reliability. Cables may be defined as either underground or submarine, the main differences being the conductor material and armour layer. Copper conductors have high electrical conductivity, favourable mechanical properties, and are easy to connect together. However, they are heavy and expensive, and are therefore used mainly in submarine applications which require good mechanical properties. Aluminium cables have lower conductivity, less favourable mechanical properties, and are more difficult to join. However, aluminium conductors are lighter and cheaper than copper

and may therefore be used in underground installations. The armour layer is normally only found in submarine cables which are subject to large axial mechanical tension during installation and operation.

2.6.2 Cables types

The most common cable types are [69]:

- Mass-impregnated (MI) insulation cables
- Low-pressure oil-filled (LPOF) cables
- Extruded cross-link polyethylene (XLPE) cables.

MI single core cables are made by winding Kraft paper around the conductor. A viscous oil impregnates the paper, increasing the insulation's electrical strength. More recently, a polypropylene laminated paper has been used, allowing the cable to operate at higher temperatures and therefore higher current ratings. MI cables can be installed at sea depths of 1000m with virtually unlimited length. Most submarines cables are of the MI type. Furthermore MI cables can tolerate fast DC voltage reversal making them compatible with any type of HVDC converter, including FB and LCC.

LPOF cables are insulated with paper impregnated, under pressure of a few bars, with low viscosity oil. For underground installations, this cable may be used at voltages up to 500 kV and 1000 MW. It is suitable for both AC and DC applications. The need for oil flow along the cable limits its use to distances of approximately 80km. The oil constitutes a potential environmental risk.

XLPE cables can operate at higher temperature, and use an overlapped thin dry polyethylene film insulator extruded over the cable core. XPLE cables are suited to long and deep submarine installation, which is associated with increased electrical operational stresses. A bonded metal-polyethylene lamination can enhance the cable's physical integrity. Although XPLE's insulation does not allow DC voltage polarity reversal, the lower cost, simpler construction and low environmental risk are suited for VSC HVDC applications were single polarity voltage is required for power transfer. Environmental impact

Underground DC cables generate low frequency magnetic fields of approximately 50 μT, which is much lower than the 400 mT which is the accepted limit for human risk. Additionally, HVDC cables are installed in pairs with small distance between them. By carrying the same current in opposite directions, the magnetic fields that are creating along the cable cancel each other out. As a result, the magnetic field may drop to zero a short distance from the cables [69]. Heat

dissipated by the cable is dependent upon cable loading. The impact of heating is low with cable temperatures typically being 1°C above surface temperature at a depth of 1 m [21].

2.7 Summary

In this chapter a thorough open-literature review of HVDC equipment is presented. The review includes energy conversion equipment, such as voltage and current source converter architectures for AC to DC and DC to DC conversion. Furthermore, a summary of potential converter arrangements is presented, as well as the cable designs that exist. Additionally, the review includes potential future equipment, such as DCCB, DC energy absorbers and fault limiters, for the protection of multi-terminal DC grids.

The review of state-of-the-art and future HVDC equipment provides insight to and understanding of future HVDC grids, regarding the requirements and the feasibility of each device. It has been shown that bulk energy transfer can be achieved using current source technologies (LCC). However this approach poses significant challenges in terms of grid interface, e.g. power factor correction and connection with weak grids. Whilst some of these issues may be solved using, for example active filter techniques, the LCC is not suitable for multi-terminal applications and this remains a major barrier to its use.

VSCs allow the interface of multiple converters, and synthesis of multi-terminal DC grids, enabling optimisation of energy transfer. According to the requirement of each terminal, variants of the VSC offer design trade-offs between efficiency, footprint and fault management. Two potential pieces of key equipment, DC to DC converters and DCCBs, are reviewed. In the context of HVDC, the feasibility of such equipment is still under discussion. However, development of such equipment may, in future, justify the potential high capital and operating costs. Finally, a review of cable technologies is presented, describing different constructions and attributes, and suggesting the most appropriate choices for HVDC applications.

This chapter lays the foundation for the new converter topologies proposed in Chapters 7. In particular this Chapter identifies all of the key issues that must be addressed when designing new converter topologies. Desirable converter features are identified, and the ease with which proposed new converter topologies may be interfaced with existing HVDC technology is considered.

Chapter 3

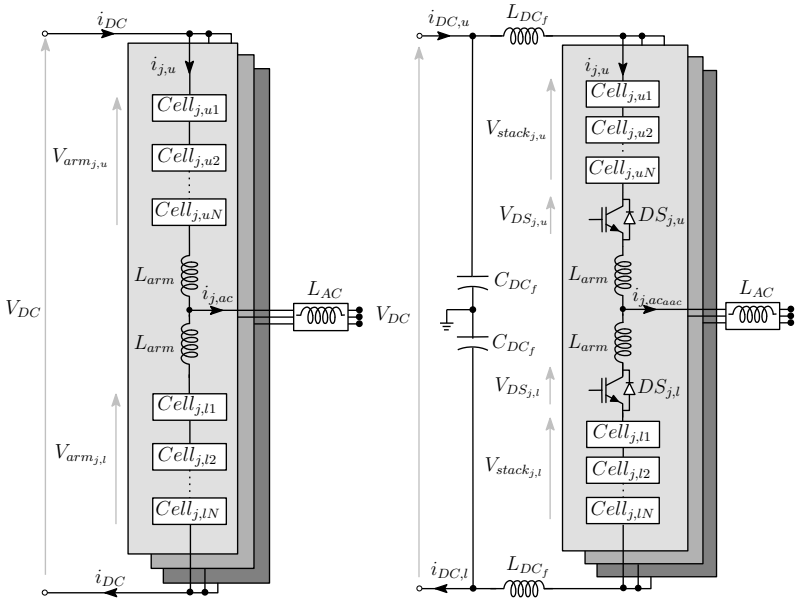
Modelling of HVDC multilevel converters

3.1 Introduction

Typical modern multilevel HVDC converters have complex power circuit structures with internal dynamics (inter-cell, inter-arm and inter-phase dynamics), that require a number of well-designed dedicated controllers to ensure converter stability over the entire operating range. Analytical performance evaluation of such converters is time-consuming and could be ineffective. For example, it is cumbersome to account for the effect of complex Capacitor Balancing Algorithms (CBAs) in average models. This is due to the fact that CBAs affect the average switching frequency per switching device (switching loss), arm energy balance and inter-arm dynamics, and hence, average models are unable to reproduce such effects. This Chapter presents a concise description of the operating principles and modelling of each converter topology, including the formulae which govern operation, and accurately reflects the internal and external dynamics, thermal behaviour and semiconductor losses.

3.2 Converter analysis

This section reviews the theoretical background which underpins the operating principles, control, and modelling of the MMC and AAC. Fig. 3.1 shows one phase leg each for generic MMC and AAC circuits with N cells per arm, where subscript j defines the phase index (i.e. $j = a, b, c$) and k defines the upper and lower position of the arm (i.e. $k = u$ for the upper arm and $k = l$ for the lower arm).



(a) MMC (b) AAC

Figure 3.1: Multilevel HVDC converter topologies.

3.2.1 Modular multilevel converter

From Fig. 3.1(a) the cell capacitor current of each individual cell can be described in terms of arm current $i_{j,k}$ and the switching function $s_{cell_{N,j,k}}$ $\{1, 0, -1\}$. The modulation waveform which drives the converter chain-link is described as:

$$m_{j,k}(t) = M \cdot \cos(\omega t + \delta) + m_{DC-j,k} \tag{3.1}$$

where M and $m_{DC-j,k}$ are the index and the DC component of the modulation waveform respectively. Equation (3.1) can also be described by the summation of the switching states as:

$$m_{j,k}(t) = \sum_{i=1}^{N} (s_{cell_{N,j,k}}) \tag{3.2}$$

Fig. 3.2 illustrates the modulation index capabilities of HB, MC with 50% HB and 50% FB cells, and FB-MMC and the voltage range that each topology can achieve for reduced DC voltage operation.

The cell current $i_{cell_{N,j,k}}$ is a function of the current that flows through the arm according to the cell switching operation.

$$i_{cell_{N,j,k}} = s_{cell_{N,j,k}} \cdot i_{j,k} \tag{3.3}$$

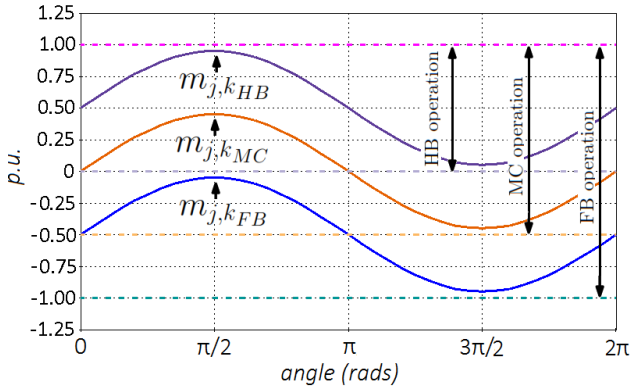


Figure 3.2: Chain-link modulation signals for HB, MC and FB-MMC.

Each arm voltage $v_{arm_{j,k}}$ as described in (3.5), is formed by the summation of individual cell voltages, $v_{cell_{N,j,k}}$ shown in (3.4).

$$v_{cell_{N,j,k}} = \frac{1}{C_{cell}} \cdot \int_0^{\Delta t} i_{cell_{N,j,k}}(\tau) d\tau \tag{3.4}$$

where Δt is the time step of the discrete integration. The arm voltage $v_{arm_{j,k}}$ is the sum of the operating cell voltages:

$$v_{arm_{j,k}} = \sum_{i=1}^{N} (s_{cell_{N,j,k}} \cdot v_{cell_{N,j,k}}) \tag{3.5}$$

The arm voltage $v_{arm_{j,k}}$ can also be described as:

$$v_{arm_{j,k}} = m_j, k \cdot V_{c_{tot}} \tag{3.6}$$

where $V_{c_{tot}}$ is the summation of total arm capacitor voltages.

The instantaneous common-mode voltage $v_{j,cm}$ the MMC phase legs present at its DC terminal can be expressed in terms of the instantaneous upper and lower arm voltages as:

$$v_{j,cm} = v_{arm_{j,u}} + v_{arm_{j,l}} = V_{DC} + \Delta V_j \tag{3.7}$$

where ΔV_j represents the DC voltage drops across the internal resistances of the arm reactors and the switching devices of the upper and lower arms. By assuming ideal arm voltage operation (3.5), V_{DC} can be described as (3.5), which reflects the voltage across the DC link and can be expressed just by the instantaneous

upper and lower arm voltages of the same phase leg.

$$V_{DC} = v_{arm_{j,u}} + v_{arm_{j,l}} \tag{3.8}$$

Considering Fig. 3.1(a), the following voltage equations can be defined:

$$\frac{V_{DC}}{2} = v_{j,l} + \frac{L_{arm}}{2} \cdot \frac{di_{j,l}}{dt} + L_{AC} \cdot \frac{di_{j,AC}}{dt} - e_j \tag{3.9}$$

$$\frac{V_{DC}}{2} = v_{j,u} + \frac{L_{arm}}{2} \cdot \frac{di_{j,u}}{dt} - L_{AC} \cdot \frac{di_{j,AC}}{dt} + e_j \tag{3.10}$$

where L_{arm} and L_{AC} are the arm and AC-side inductances respectively (as shown in Fig. 3.1(a)) and L_{AC-j} is the AC-side grid phase voltage. By subtracting (3.9) from (3.10) the converter operation of the AC voltage V_{AC_j} can be described:

$$V_{AC_j} = \frac{v_{arm_{j,l}} - v_{arm_{j,u}}}{2} - L_{AC} \cdot \frac{di_j}{dt} \tag{3.11}$$

The upper and lower arm currents in each phase can be expressed by (3.12) and (3.13) respectively

$$i_{j,u} = \frac{i_{j,AC}}{2} + i_{j,cm} \tag{3.12}$$

$$i_{j,l} = -\frac{i_{j,AC}}{2} + i_{j,cm} \tag{3.13}$$

where $i_{j,AC}$ and $i_{j,cm}$ are the AC output phase and common-mode currents respectively. Common-mode currents $i_{j,cm}$ are described in (3.14) while DC current i_{DC} is composed by summing the DC components of each phase, as shown in (3.15).

$$i_{j,cm} = \frac{i_{j,u} + i_{j,l}}{2} = i_{j,DC} + i_{j,cc} \tag{3.14}$$

$$i_{j,DC} = i_{a,DC} + i_{b,DC} + i_{c,DC} \tag{3.15}$$

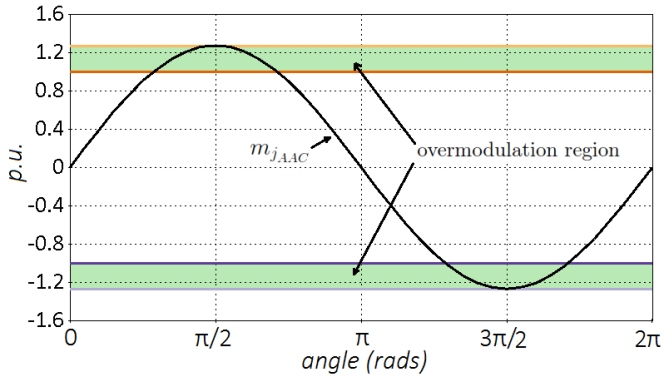
where $i_{j,DC}$ is the DC component of the common-mode current. Circulating current $i_{j,cc}$ flows through the upper and lower arms and occurs due to the unbalanced voltages between the upper and lower arms in each phase resulting from the equivalent total capacitor voltage ripple. However, the circulating current does not contribute to the AC output current.

The differential voltage $v_{j,diff}$ between the upper and lower arms is defined in (3.16) and can be considered as the electromotive force (EMF) generated in each phase.

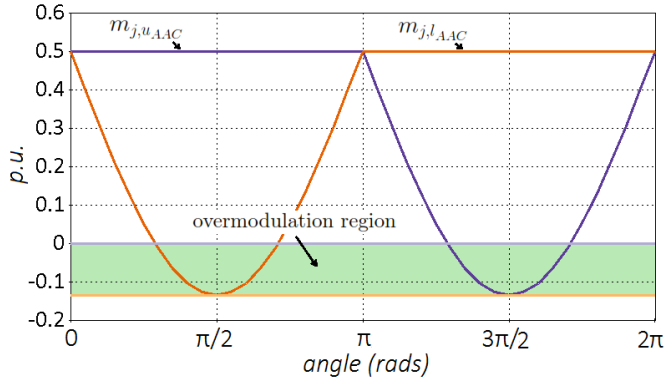
$$v_{j,diff} = \frac{V_{DC}}{2} - v_{j,u} = -\frac{V_{DC}}{2} - v_{j,l} = \frac{v_{j,u} - v_{j,l}}{2} \tag{3.16}$$

3.2.2 Alternate arm converter

As illustrated in Fig. 3.1(b), each AAC arm consists of series-connected FB cells and a DS. Cell capacitor current and voltage can be described as in (3.3) and (3.4), and therefore voltage $v_{chain_{j,u}}$ is considered to be identical to the arm voltage as described by (3.5). Fig. 3.3 shows the ability of the AAC to operate in the over-modulation region, to achieve energy equilibrium on the AC and DC sides. Effectively, Fig. 3.3(a) shows the modulation signal for each arm chain-link. The chain-link is rated for operation up to $\frac{4}{\pi}$ of the DC voltage, which is sufficient to synthesise half of the peak AC voltage. This is achieved through over-modulation which is requires operation in the negative DC voltage region, as shown in Figs. 3.3(a) and 3.3(b).



(a) Converter modulation signal



(b) Chain-link modulation signal

Figure 3.3: AAC modulation signals.

The AAC may be considered as a combination of an MMC and a two-level converter, and its operation can be described by the following three distinctive stages [38]:

- Stage I: Single arm conduction

- Stage II: Overlap
- Stage III: Off-state

During Stage I, the arm voltage is equal to $v_{chain_{j,k}}$ and the arm current is equal to $i_{j,AC_{AAC}}$. In Stage II, the AAC operates as an MMC where both the upper and lower arms conduct simultaneously for a very short period of time, in order to re-balance the voltages across the upper and lower chain-links. In Stage III, the DS in the outgoing arm is turned off to stop the current flow, and enable the outgoing arm to block the full DC voltage. The time frames in (3.17) summarise AAC operation during Stages I, II and III.

$$\begin{cases} t_{j,u_1} = -\frac{T}{2} + \frac{t_{over}}{2} + T \cdot s_{DS_{j,u}} \\ t_{j,u_2} = \frac{T}{2} - \frac{t_{over}}{2} + \frac{T \cdot s_{DS_{j,u}}}{2} \\ t_{j,l_1} = -\frac{T}{2} + \frac{t_{over}}{2} + T \cdot (1 - s_{DS_{j,l}}) \\ t_{j,l_2} = \frac{T}{2} - \frac{t_{over}}{2} + \frac{T \cdot (1 - s_{DS_{j,l}})}{2} \end{cases} \tag{3.17}$$

where T is the fundamental period, t_{over} is the overlap time and sDS is the switching function of DS. Considering (3.17), the output DC voltage can be expressed in terms of the average voltage of the upper and lower arms, as in shown in (3.18).

$$\begin{aligned} V_{DC} = \ & \frac{1}{T} \cdot \int_{t_{j,u_1}}^{t_{j,u_2}} v_{chain_{j,u}}(\tau) + v_{DS_{j,l}}(\tau) d\tau \\ & + \frac{1}{T} \cdot \int_{t_{j,l_1}}^{t_{j,l_2}} v_{chain_{j,l}}(\tau) + v_{DS_{j,u}}(\tau) d\tau \end{aligned} \tag{3.18}$$

It is evident from (3.19) that the AC current in mainly composed by the conducting arm current $i_{j,k_{AAC}}$. AC current flows during Stages I and II.

$$\begin{aligned} & i_{j,AC_{AAC}} = \frac{1}{T} \cdot \int_{t_{j,u_1}}^{t_{j,u_2}} i_{j,u_{AAC}}(\tau) d\tau \cdot s_{DS_{j,u}} + \\ & + \frac{1}{T} \cdot \int_{t_{j,l_1}}^{t_{j,l_2}} i_{j,l_{AAC}}(\tau) d\tau \cdot (1 - s_{DS_{j,l}}) \\ & = i_{j,u_{AAC}} + i_{j,l_{AAC}} \end{aligned} \tag{3.19}$$

The instantaneous $\frac{V_{DC}}{2}$ can be expressed by (3.20) and (3.21) for the upper and lower arms respectively.

$$\frac{V_{DC}}{2} = v_{chain_{j,u}} + v_{DS_{j,l}} + L_{arm} \cdot \frac{di_{j,u_{AAC}}}{dt} - L_{AC} \cdot \frac{di_{j,AC_{AAC}}}{dt} \tag{3.20}$$

$$\frac{V_{DC}}{2} = v_{chain_{j,l}} + v_{DS_{j,u}} - L_{arm} \cdot \frac{di_{j,l_{AAC}}}{dt} + L_{AC} \cdot \frac{di_{j,AC_{AAC}}}{dt} \tag{3.21}$$

In an AAC the DC currents i_{DC_u} and i_{DC_l} are composed according to (3.22). Due to the fact that AAC arm current flow is similar to that in a two-level converter, inherently DC currents contain a 6th harmonic ripple component.

$$\begin{cases} i_{DC_u} = i_{a,u_{AAC}} + i_{b,u_{AAC}} + i_{c,u_{AAC}} \\ i_{DC_l} = i_{a,l_{AAC}} + i_{b,l_{AAC}} + i_{c,l_{AAC}} \end{cases} \tag{3.22}$$

3.3 Controllers

In this section the generic control structure for all MMC and AAC being developed is described, similar to the CIGRE DC test system [70]. The controller, which consists of master, upper and lower level controls, is shown if Fig. 3.4, and the detailed controlled structure is highlighted as shown. Within the Upper level controller structure the outer and inner controllers are common to all topologies, as is the Lower level controller structure. The valve balance controller is specific to each converter topology. The master controller is defined by the system operator and will provide the desired references to the upper level control in order to operate the HVDC network.

- Master controller
- Upper level
  - Outer controller
  - Inner controller
  - Valve balance controller
- Lower level
  - CBA
  - Modulation techniques

The detailed structure and the tuned parameters of the controllers that were used in the thesis are described in Appendix A.

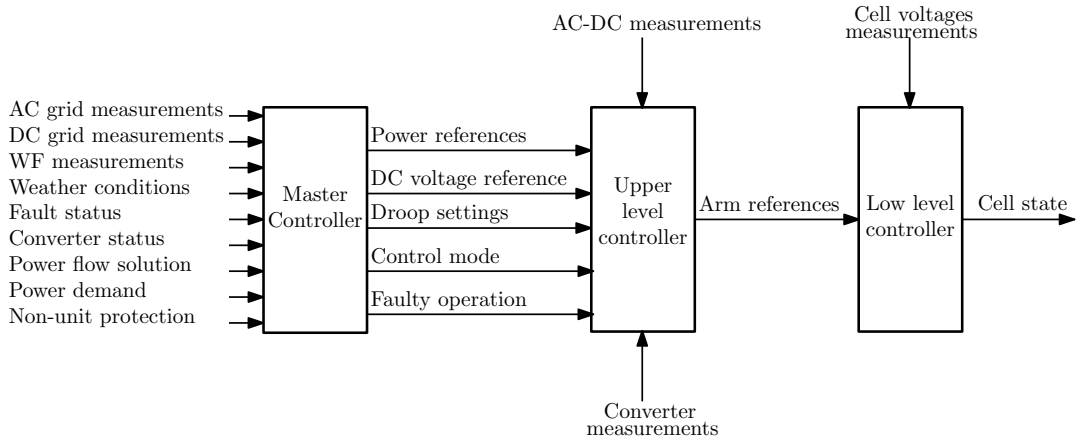


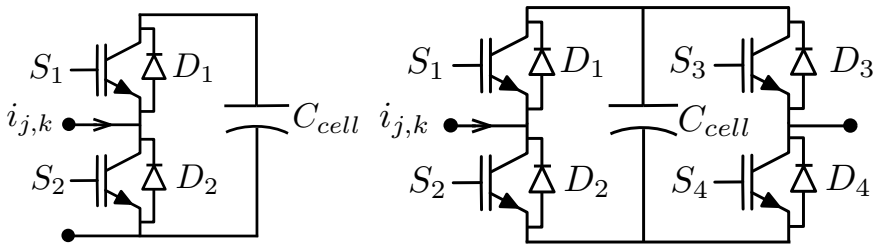
Figure 3.4: Overall controller structure.

3.4 Converter modelling

This section describes the methods of modelling converters for large scale simulations, and which can reflect the dynamics and operation of each converter topology. The semiconductor losses are incorporated to reflect the exact operation of the converter.

3.4.1 Semiconductor loss calculation

Since semiconductor losses represent the major portion of the total converter station losses, all other losses such as those incurred in transformer windings, passive components, etc., have been excluded. The IGBT losses consist of conduction losses during the ON state, and switching losses during the transition between ON and OFF states and vice versa. Tables 3.1 and 3.2 show the switching transitions and conduction paths corresponding to the FB and HB cells shown in Fig. 3.5.



(a) HB cell (b) FB cell

Figure 3.5: Basic cell topologies. The arrow shows the direction of positive current.

Typically, a piecewise representation of switching energy during turn-on and turn-off events is used to calculate IGBT switching losses, while the IGBT voltage drop is used to estimate conduction losses. The piecewise information is extracted from semiconductor manufacturer datasheets, and are implemented in equation (3.23). The losses are calculated based on an initial junction temperature that is similar to ambient T_{amb}. The voltage drop V_{ce} during IGBT conduction can be defined as a function of arm current and operating temperature, as shown in (3.23).

$$\begin{cases} V_{ce_{data}} = V_{ce}\left(\frac{|i_{arm}|}{n_p}, T_S\right)_{data} \\ V_{f_{data}} = V_f\left(\frac{|i_{arm}|}{n_p}, T_D\right)_{data} \end{cases} \tag{3.23}$$

The temperature terms shown in (3.23) are calculated using a steady-state thermal model that considers the thermal resistance for each part of an IGBT, as

Table 3.1: HB cell operation, conduction and switching pattern.

Current	Cell state	Transition	Conduction
Positive	0 to V_C	$D_{1_{ON}}$, $S_{2_{OFF}}$	D_1
	V_C to 0	$D_{1_{OFF}}$, $S_{2_{ON}}$	S_2
Negative	0 to V_C	$D_{2_{OFF}}$, $S_{1_{ON}}$	S_1
	V_C to 0	$S_{1_{OFF}}$, $D_{2_{ON}}$	D_2

Table 3.2: FB cell operation, conduction and switching pattern.

Current	Cell state	Transition	Conduction
Positive	0 to V_C	$D_{1_{ON}}$, $S_{2_{OFF}}$	D_1, D_4
	V_C to 0	$D_{1_{OFF}}$, $S_{2_{ON}}$	S_2, D_4
	0 to -V_C	$D_{4_{OFF}}$, $S_{3_{ON}}$	S_2, S_3
	-V_C to 0	$S_{3_{OFF}}$, $D_{4_{ON}}$	S_2, D_4
Negative	0 to Vc	$D_{2_{OFF}}$, $S_{1_{ON}}$	S_1, S_4
	V_C to 0	$S_{1_{OFF}}$, $D_{2_{ON}}$	D_2, S_4
	0 to -V_C	$D_{3_{ON}}$, $S_{4_{OFF}}$	D_2, D_3
	-V_C to 0	$D_{3_{OFF}}$, $S_{4_{ON}}$	D_2, S_4

shown in (3.24)

$$\begin{cases} T_S = P_{cond_S} \cdot (R_{j_S} + R_{c_S} + R_{hs}) + T_{amb} \\ T_D = P_{cond_D} \cdot (R_{j_D} + R_{c_D} + R_{hs}) + T_{amb} \end{cases} \tag{3.24}$$

where R_{jS}, R_{cS}, R_{hs} are the junction-to-case, case-to-heatsink and heatsink-to-ambient-thermal resistances respectively. The combined voltage drop of a cell is calculated from (3.25).

$$V_{loss_{cell}} = V_{ce_{data}} + V_{f_{data}} \tag{3.25}$$

IGBT and diode conduction losses are calculated according to (3.26)

$$\begin{cases} P_{cond_S} = \frac{1}{T} \int_{t-T}^{t} V_{ce_{data}} \cdot \frac{|i_{arm}|}{n_p} \cdot K_{uti} \cdot n_s \cdot n_p \, d\tau \\ P_{cond_D} = \frac{1}{T} \int_{t-T}^{t} V_{f_{data}} \cdot \frac{|i_{arm}|}{n_p} \cdot K_{uti} \cdot n_s \cdot n_p \, d\tau \end{cases} \tag{3.26}$$

where n_s and n_p are the numbers of series and parallel-connected IGBTs is described by (3.27) and (3.28) respectively

$$n_s = ceil\left(\frac{V_{chain}}{V_{igbt} \cdot N_{cell}}\right) \tag{3.27}$$

$$n_p = ceil\left(\frac{i_{j,k}}{I_{igbt}}\right) \tag{3.28}$$

and K_{uti} is the utilisation constant described by (3.29)

$$K_{uti} = \frac{V_{chain}}{V_{igbt} \cdot n_s \cdot N} \tag{3.29}$$

where V_{chain} is the total voltage across the chain-link in a given arm, and I_{igbt} and V_{igbt} are the continuous rated current and blocking voltage of a single IGBT respectively.

The energy dissipated during the switching process can be defined as a function of the instantaneous arm current and the switching energy of the IGBT, as shown in (3.30). Thereafter, the switching losses are calculated according to (3.31)

$$E_{sw} = \left(\frac{|i_{arm}|}{n_p}\right) \cdot \left(E_{S_{on}} + E_{S_{off}} + E_{D_{off}}\right)_{data} \tag{3.30}$$

$$P_{sw_S} = \frac{1}{T} \sum_{t-T}^{t} E_{sw} \cdot K_{uti} \cdot K_T \cdot n_s \cdot n_p \tag{3.31}$$

where K_T, defined in (3.32), is a thermal correction factor and is utilised to normalise the temperature according to the IGBT thermal model.

$$K_T = \frac{T_S, T_D}{T_{max_{data}}} \tag{3.32}$$

3.4.2 Valve modelling

Studying electromagnetic transient phenomena requires high-fidelity, accurate converter models in order to clearly represent phenomena which may affect the system. The computational burden can be extremely large as thousands of components (e.g. IGBT, snubber circuits, etc.) affect the operation of the converter. There is no single solution in the construction of efficient and accurate models as the level of detail required is dictated by the needs of each study [71]. However, in order to reduce the computational time and effort, simplified models are developed with reduced number of nodes, according to the required depth of analysis.

Detailed switching model

A detailed switching model (DSM) typically includes very detailed simulation of the semiconductor switching profiles and conduction voltage drops, based on a detailed semiconductor model that includes key physical (Ph) phenomena with durations of a few ns to μs. Although this type of implementation is very accurate, the number of nodes and the computational effort required to simulate an event that lasts a few seconds is prohibitive. An alternative to the Ph model is the non-linear model (NL). In this case the characteristics of the IGBT are emulated through a V/I look-up table. Additionally, the on and off switching procedures are considered to be instantaneous. The trade-off between the complexity and fidelity exists. Fig. 3.6 shows the circuits representing the Ph and NL model in the simulation platform. Additionally, a DSM allows a detailed representation of the cell, where the ESR of the capacitor and leakage inductance of the circuit are also included. Even though each cell consists of only three to four nodes, the computational burden for simulations with high numbers of cells per arm is high. Such a model is used when the converter internal operation at IGBT level needs to be observed during transient operation. However, if the simulation time step is increased the fidelity of the simulation drops and the high-frequency phenomena (1μs and below) cannot be reflected thus diminishing the need of this type of model.

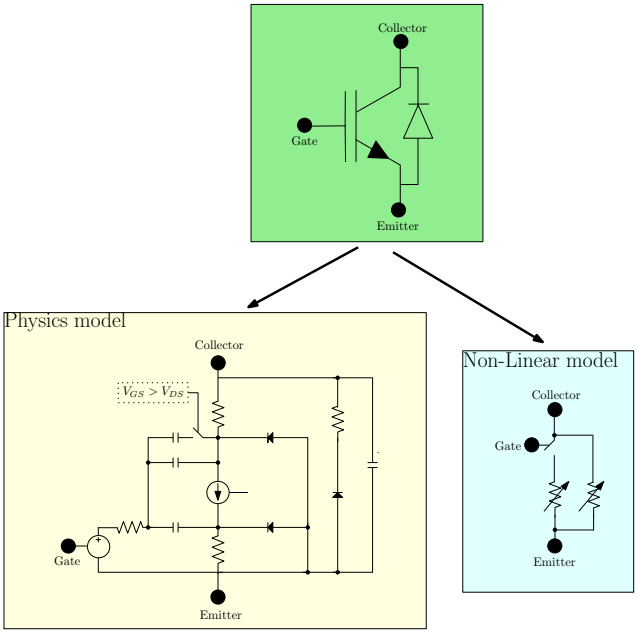


Figure 3.6: Implementation of IGBT for detailed switching models, Ph and NL.

Function switching model

Full-scale representation of AAC and MMC with large numbers of cells per arm using detailed switched models are characterised by large numbers of electrical nodes, which increases the size of the admittance matrix; thus computation burden on the processor is increased [72]. A simplified cell model can be used where it is not necessary to observe internal IGBT. Each cell operates in a simplified on/off manner and reflects accurate arm voltage operation by including the capacitor cell voltages imbalances. Such a model has a very low number of nodes, regardless the number of cells, therefore it is highly efficient for large HVDC networks where observation of cell-level transient phenomena is required.

There are two main variations of the specific model. The first is the cell Thevenin equivalent model, and the second is the cell switching function [73].

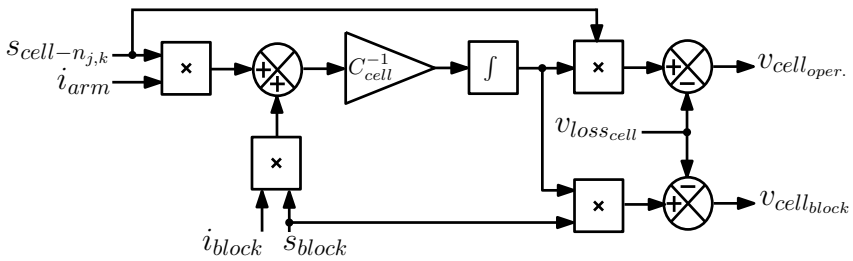
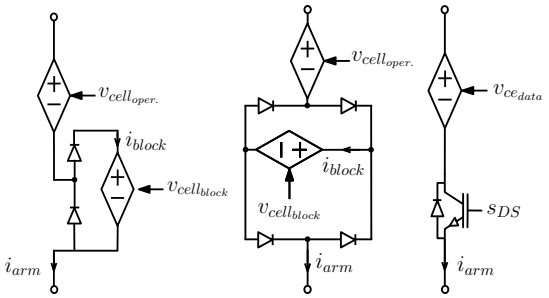


Figure 3.7: Cell voltage block diagram of FS model.



(a) HB (b) FB (c) DS

Figure 3.8: Equivalent representations of arm components.

The latter is considered to be easier for implementation and more efficient for offline and real-time simulations. Fig. 3.7 shows the switching function (FS) representation of the cells in terms of arm current and firing order, as described in (3.3) and (3.4). As the discrete integration of (3.4) determines the fidelity of the results, a small time step of 5μs is necessary in order to achieve high accuracy.

An enhanced version of the switching model is used, by representing the switching losses through calculated voltage drop $v_{loss_{cell}}$ as described in (3.25). Fig. 3.8 illustrates the HB and FB cell chain-links, as described in (3.5), and the DS. The controlled voltage source added into the DS model in Fig. 3.8(c) accounts for its switching and conduction losses, which are critical for accurate estimation of semiconductor losses in AAC. For example, series connection of the chain-links Fig. 3.8(a) and 3.8(b) represents the arm of an MC-MMC, whilst series connection of the chain-links in Fig. 3.8(b) and the DS in Fig. 3.8(c) represents an AAC.

The complete block diagram for loss calculation, integrating thermal models, switching patterns and manufacturer data sheets, is depicted in Fig. 3.9.

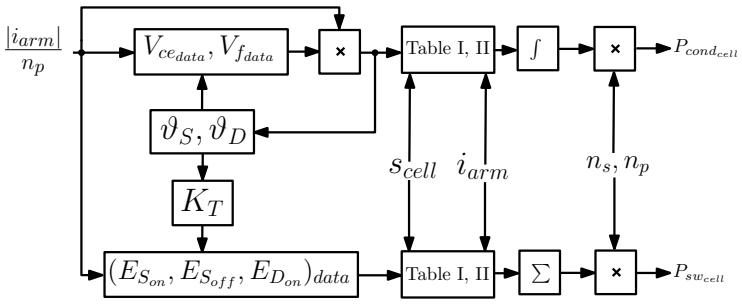


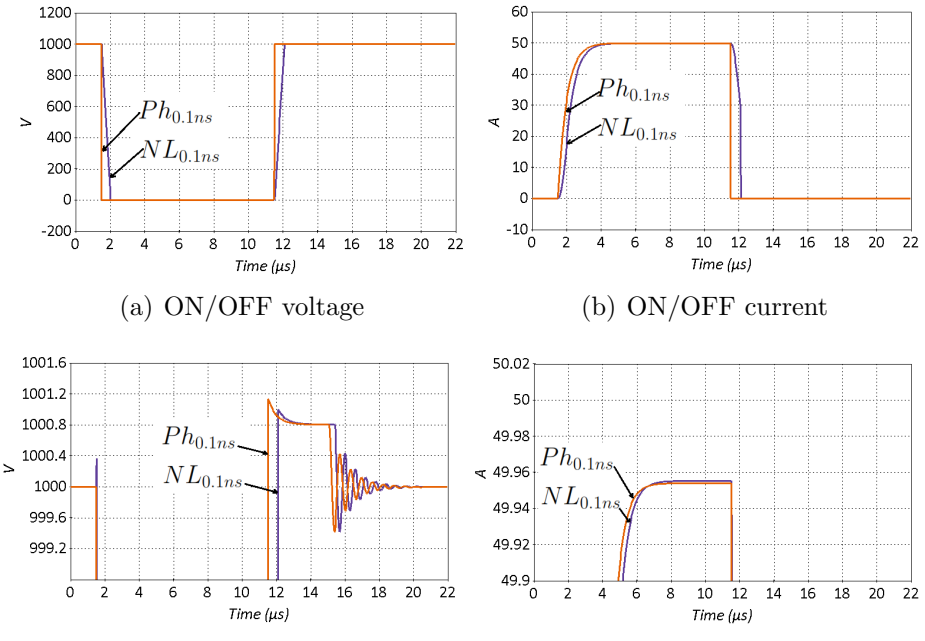
Figure 3.9: Block diagram of loss calculation scheme.

Average model

For simulations where only the internal energies of the converter need to be observed an average model is utilised. Each arm is represented as a controlled voltage source, where the cell capacitors are combined to one lumped total capacitance assuming the average arm voltage and perfectly balance cell voltages. However, one major disadvantage of this model is the very narrow bandwidth of operation which assumes very high resolution times. Average models are employed for arm-level phenomena and validation of control concepts. Computation efficiency is increased as the total number of converter nodes is reduced.

3.4.3 Model verification

This section presents verification of the off-line models based on the MMC and AAC topologies, using the EMTP-RV simulation platform. Model verification is conducted in two stages: the first is at semiconductor level and the second is at converter level. Fig. 3.10 shows the on and off switching operation of one IGBT with an inductive load for Ph and NL models. The different current and voltage gradients are mainly due to the fidelity of the piecewise V/I curve of the NL model. From Figs. 3.10(a) and 3.10(b) both models achieve the same steady-



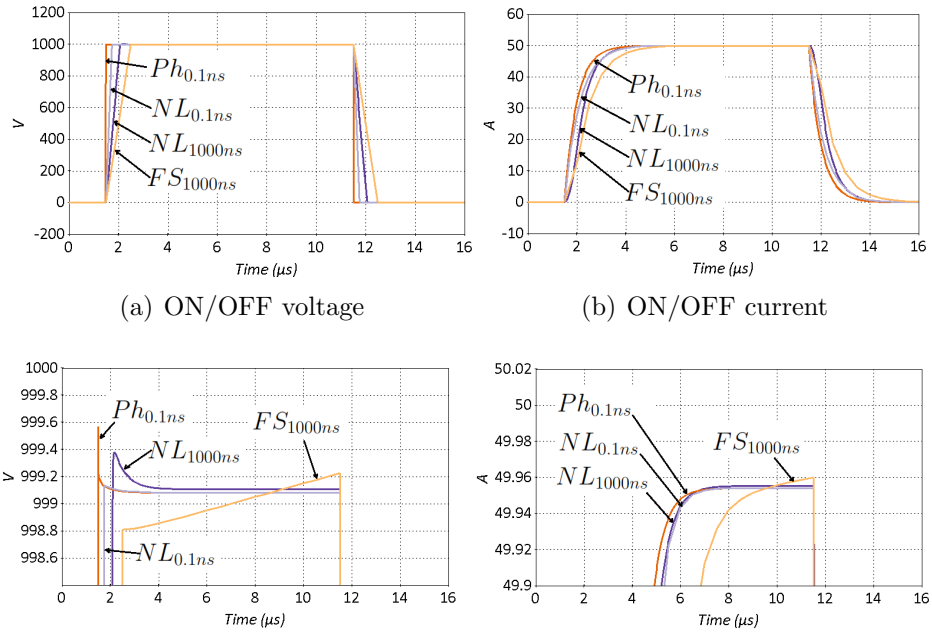
(a) ON/OFF voltage

(b) ON/OFF current

(c) Focused ON/OFF voltage

(d) Focused ON/OFF current

Figure 3.10: Comparison of Ph and NL variants of DSM model of an IGBT on inductive load for simulation time step $\Delta t = 0.1$ ns.



(a) ON/OFF voltage

(b) ON/OFF current

(c) Focused ON/OFF voltage

(d) Focused ON/OFF current

Figure 3.11: Comparison of DSM variants and FS model of an HB cell on resistive load for simulation time steps $\Delta t = 0.1$ ns and $\Delta t = 1000$ ns.

state current and voltage; however, the NL model responds with a small delay of approximately 500 ns when compared to the Ph model. Even for high-fidelity simulations, the delay does not affect the actual operation of the converter as the inclusion of phenomena such dead-time, which can last 2-3 μs, renders this type of error negligible. Nevertheless, Figs. 3.10(c) and 3.10(d) shows good agreement, including overshoot and oscillations between the two models during turn-on and turn-off.

Fig. 3.11 illustrates the turn on and off processes of an HB cell for DSM and FS models. The Ph and NL variants of the DSM model shows good agreement for a variety of time-steps. However the accuracy of the FS model is highly dependent on the time-step, hence the mismatch when compared to the DSM model as shown in Figs. 3.11(c) and 3.11(d). Additionally, due to accuracy of the piecewise thermal model an observable error is produced compared to the DSM model. The difference, however is still only a few mV over the 1 kV operating range.

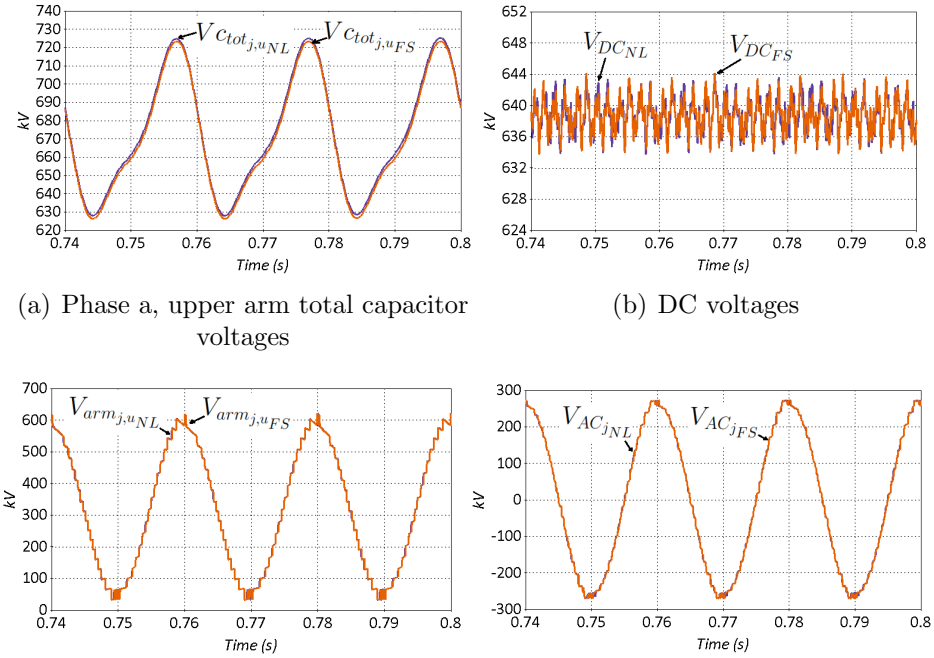
When simulating at cell and single device level, the DSM and FS approaches have been shown to yield similar results. Although the FS approach is less accurate than either of the DSM variants, performance is still acceptable particularly in view of the reduced computational burden of the FS modelling technique. The

following simulations now compare the NL-DSM and FS approaches to modelling at converter level. In Figs. 3.10 and 3.11, the NL-DSM and Ph-DSM approaches are shown to yield very similar results. For the purposes of the following simulations, therefore, the NL approach is selected as being indicative of DSM performance.

The following simulation studies will focus on modelling MMC and AAC converters during open-loop operation. The controllers, described in Section 3.3 are not included so as to remove any uncertainty that any variations between the modelled results are due to the power circuit or the controller. Additionally, converter model validation is conducted using by using fixed modulation index on a fixed load. Figs. 3.12 and 3.13 compare the NL-DSM and FS modelling approaches to an open-loop MMC. The figures show that for each modelling approach all voltages and all currents are in good agreement.

Figs. 3.14 and 3.15 show the same comparison for an open-loop AAC. Again, the figures show that for each modelling approach all voltages and all currents in good agreement. For both MMC and AAC the simulations are for converters with low number of cells ($N = 20$).

Consequently, in a real application where the number of cells will be signifi-



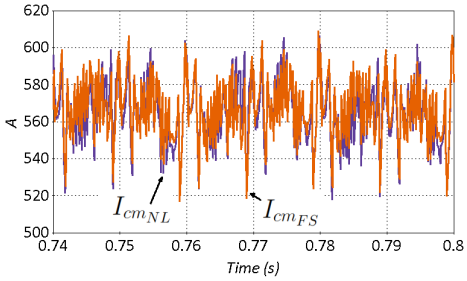
(a) Phase a, upper arm total capacitor voltages

(b) DC voltages

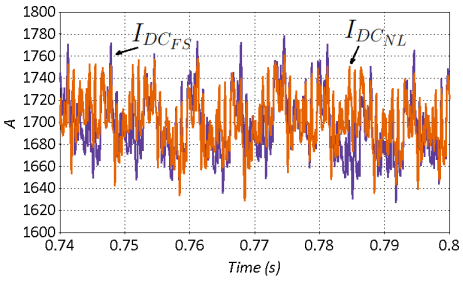
(c) Phase a, upper arm voltage

(d) Phase a AC voltage

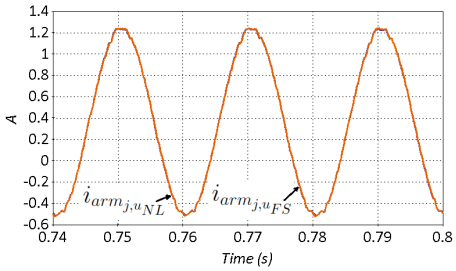
Figure 3.12: Voltage comparison of NL-DSM and FS modelling approaches to an open-loop MMC.



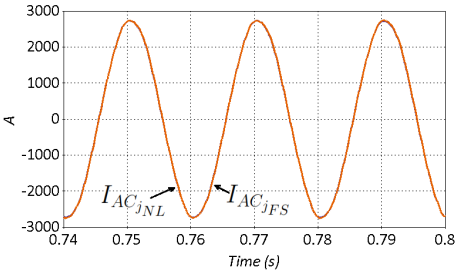
(a) common-mode current



(b) DC current

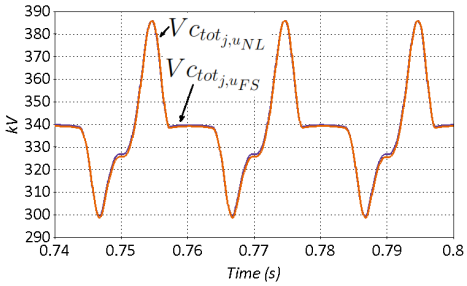


(c) Phase a, upper arm current

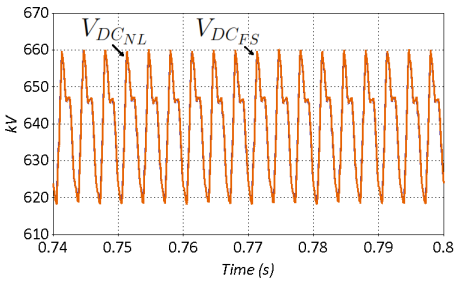


(d) Phase AC current

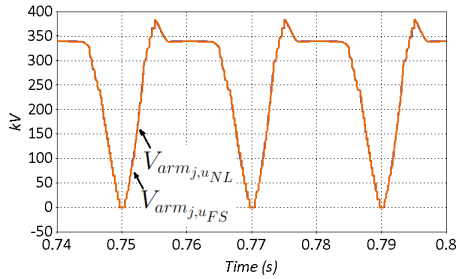
Figure 3.13: Current comparison of NL-DSM and FS modelling approaches to an open-loop MMC.



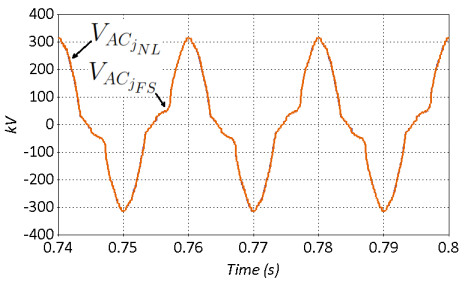
(a) Phase a, upper arm total capacitor voltages



(b) DC voltages

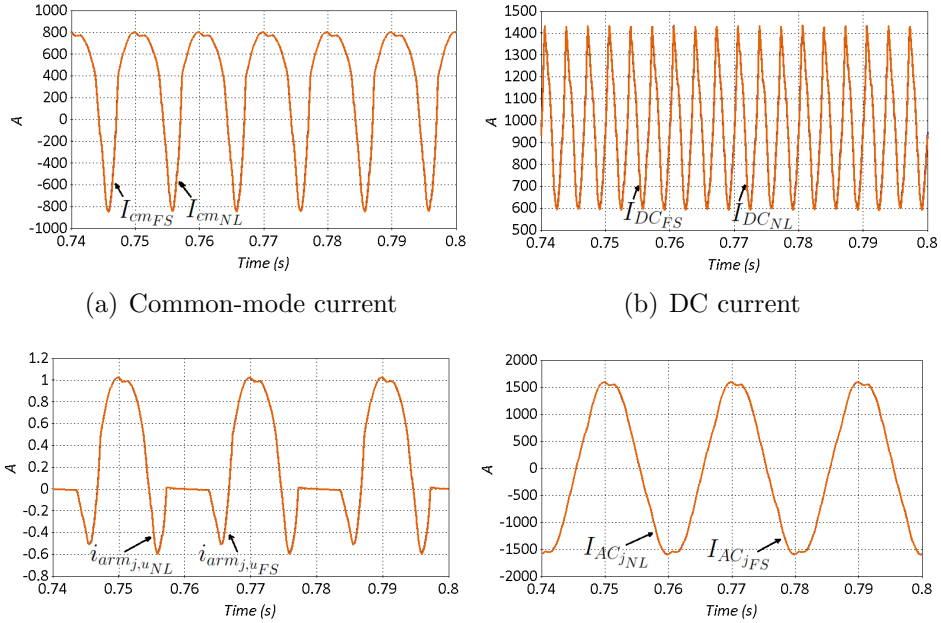


(c) Phase a, upper arm voltage



(d) Phase a AC voltage

Figure 3.14: Voltage comparison of NL-DSM and FS modelling approaches to an open-loop AAC.



(a) Common-mode current

(b) DC current

(c) Phase a, upper arm current

(d) Phase AC current

Figure 3.15: Current comparison of NL-DSM and FS modelling approaches to an open-loop AAC.

cantly greater, any differences between the models highlighted by the simulation results of Fig. 3.13 to 3.15 will be significantly reduced. As a result of this extensive comparison of simulation methods at both device and converter levels, it is concluded that the FS approach offers the best compromise in terms of accuracy and computational burden. The FS approach will therefore be adopted as the preferred modelling method in the remainder of this study.

3.5 Summary

This chapter presents a detailed mathematical analysis of MMC and AAC which provides a basis for understanding converter operation in detail and subsequent development of control strategies. A typical control structure is defined and the various levels of essential control are developed and explained in detail. These controllers are incorporated in studies detailed in later chapters. Different approaches to converter modelling are examined in detail. DSM and FS approaches to modelling MMC and AAC operating in open-loop mode are developed. The FS approach is further developed by including the semiconductor loss, according to the thermal impedances. The losses are computed simultaneously with the electrical circuit and they are part of the simulation solution. Comparison of

these modelling approaches shows that the FS model provides the best compromise between computational burden and accuracy. This approach is therefore used in the remainder of this thesis. This chapter therefore provides a solid basis upon which the remaining chapters, which examine steady-state converter performance and transient operation, and which propose new converter topologies, are developed.

Chapter 4

Power quality, steady-state and dynamic operation

4.1 Introduction

At present, there are two alternative approaches to the realisation of MMCs. The first approach utilises a large number of cells per arm, where the blocking capability of each cell is small and is defined by the rating of a single switching device (i.e. 2-3 kV). The second approach adopts a reduced number of cells per arm, with each cell rated for high DC operating voltage, ranging between 16-20 kV. Thus, the latter approach requires the adoption of series-connected semiconductor devices. This chapter presents a research approach which utilises detailed converter models and a well-designed set of test scenarios to compare the performance of different converters, with emphasis given to AAC and MMC and its derivatives, namely the FB-MMC and MC-MMC. Both FB-MMC and HB-MMC are investigated, even though the HB-MMC does not have blocking capability. The main results obtained from this detailed modelling exercise are thoroughly discussed and the main factors that affect the power quality on the AC and DC sides, losses and potential design trade-offs are identified.

4.2 Design methodology

This section describes the procedures followed for designing the converters, including choice of semiconductors, the number of cells, and the passive component values (i.e. cell capacitor and arm inductance). For ease of comparison, the design has been accomplished assuming the same rated power, DC voltage and voltage stress per device for all converters.

4.2.1 Sizing of passive components

Correct sizing of passive components (such as cell capacitors and arm inductance) is critical for stable operation of AAC and MMC. Passive components have to be sized for stable and transient operation while allowing safe operation of the converter according to operational requirements. The passive components dictate converter response and behaviour during dynamic and transient operation. Therefore, it is necessary to size according to the application, and the functionality of the converter.

Cell capacitance

Since cell capacitors in AAC and MMC experience low-frequency current, large cell capacitance will be required to ensure acceptable voltage ripple. There are two requirements for capacitor sizing. The first is to achieve minimum voltage ripple in the steady state according to the PQ capabilities of the converter. This specifies the minimum cell capacitance value. Cell capacitor energy E_{cell}, is defined according to

$$E_{cell} = \frac{N \cdot C_{cell} \cdot V_c^2}{2} \tag{4.1}$$

where, N is the number of cell, V_c is the cell voltage and the cell capacitance C_{cell} is defined as

$$C_{cell} = \frac{N \cdot \Delta E_{cell}}{2 \cdot V_{DC}^2 \cdot \Delta V_{c-max}} \tag{4.2}$$

where ΔV_{c-max} is the maximum cell voltage ripple while the maximum arm energy deviation ΔE_{cell} can be described as

$$\Delta E_{cell} = \frac{2 \cdot S}{3 \cdot \omega \ M} \tag{4.3}$$

where S is the apparent power.

As a result, by combining (4.2) and (4.3) cell capacitance can be described as

$$C_{cell} = \frac{N \cdot S}{3 \cdot \omega \cdot M \cdot V_{DC}^2 \cdot \Delta V_{c-max}} \tag{4.4}$$

where the maximum voltage ripple amplitude occurs for zero real power transfer. Cell capacitor energy deviation ΔE_{cell} increases at low values of modulation index M.

The second requirement is to size the capacitor in order to ensure compliance with the design value of cell capacitor voltage ripple during transient operation. For example, during DC faults, the DC voltage collapses almost immediately,

which leads to significant energy deviation in the cell capacitors. Also due to control signal delays, the cells are not bypassed or blocked immediately. The resulting variation in capacitor energy causes significant cell voltage ripple. The cell capacitor must be sized to accommodate this before system protection is enabled, to avoid a voltage ripple that exceeds the insulation ratings of the cell. To ensure stable operation over a wide modulation index, AAC energy storage capability is assumed to be similar to that of the MMC (i.e. 40 kJ/MW) [74, 75], which covers the minimum requirement for steady-state and transient operation.

Arm inductance

In an MMC the arm inductance L_{arm} (or accumulated DC side inductance) can act as a filter for the circulating currents and can prolong current rise time in the event of a DC-side fault. The minimum installed arm inductance is defined by (4.5)

$$L_{arm} = \frac{5 \cdot M \cdot V_{DC}^2 \cdot \Delta V_{c-max}}{f_{eff} \cdot S} \tag{4.5}$$

and is dependent on the cell capacitor voltage ripple, the modulation index M, and the effective switching frequency f_{eff} of the converter. Arm inductance is not affected by the number of cells. However, (A.1) shows that f_{eff} is depended upon the number of cells for fixed cell switching frequency. As a result, the required magnitude of L_{arm} decreases as the number of cells increases.

In the case of AAC, the arm inductance should be sufficient to enable the arm current to be transferred between arms during the overlap period [76]. Therefore the maximum value of arm inductance is

$$L_{arm-max_{AAC}} = \frac{N}{C_{cell}} \left(\frac{t_{over}}{\pi} \right)^2 \tag{4.6}$$

Arm inductance must also provide a degree of current filtering in order to suppress di/dt and reduce EMI. As a result the minimum AAC arm inductance is

$$L_{arm-min_{AAC}} = \frac{\hat{V}_{arm}}{2 \cdot f_{eff} \cdot \Delta \hat{I}_{arm}} \tag{4.7}$$

where $\hat{V}_{arm}$ is the peak arm voltage and $\hat{I}_{arm}$ is the peak arm current.

Equation (4.7) shows that arm inductance is not dependent upon cell voltage deviation. This is due to the lack of continuous energy exchange between the upper and lower arms, which is a feature of the MMC. As a result the AAC arm inductance does not make a major contribution to converter dynamics. Ad-

ditionally, in view lower value of inductance in AAC, AC side power quality is ensured by insertion of additional AC inductance. This additional inductance is also necessary to ensure control and good dynamic performance of AAC.

DC filter

An AAC requires a sizeable DC filter to attenuate 6^th harmonic current and its multiples. Initially L_{DCf} according to application specific requirements. The filter capacitance C_{DCf} is then calculated according (4.8). A major consideration is to reduce as far as possible the size of C_{DCf} to ensure minimal impact on DC fault current levels. A resistor connected in parallel with the inductor is then chosen to yield the specified quality factor Q_{DCf} according to (4.9).

$$f_{DC_f} = \frac{1}{\pi\sqrt{L_{DC_f} \cdot C_{DC_f}}} \tag{4.8}$$

$$Q_{DC_f} = R_{DC_f}\sqrt{\frac{C_{DC_f}}{L_{DC_f}}} \tag{4.9}$$

As a result, the component values for a DC filter that sufficiently suppresses the 6th AAC harmonic, over a wide operating range, are L_{DCf} = 10 mH, and C_{DCf} = 28.15 μF.

4.2.2 Number of cells and semiconductors

The number of cells is defined by two factors. Firstly, the AC power quality requirements need to be fulfilled according to the Grid Code of each country. The higher the number of cells, the better the quality of the AC voltage generated by the converter, except if AC filtering is considered or for specific modulation techniques [77]. The second factor is related to the converter's operating power and DC voltage. Each cell must be rated to support V_{cell}=$\frac{V_{chain}}{N}$. The use of parallel IGBTs reduces the semiconductor losses and allows the use of lower current-rated IGBTs, while series connection reduces the number of cells, and hence power circuit and control complexity, and creepage and clearance requirements. Since series connection of IGBTs is not a straightforward task, it is more common to design cells to support voltage across single IGBT devices. Practically, the blocking voltage V_{igbt} of an IGBT is selected to enable stable operation and prolonged lifespan, and to sustain transient overvoltages. Induced cosmic rays and potential transient (overvoltage) operation have significant impact on IGBT reliability, therefore the applied voltage needs to be 60% or less of the rated

voltage. Consequently, 3.3 kV IGBTs [78] with $V_{igbt} = 1.8$ kV are used for the presented studies.

The converters being compared are assumed to have a similar utilisation factor K_{uti} (the ratio of the required blocking voltages V_{chain} to the installed blocking voltage capability of the chain-link) with respect to the semiconductors in each chain-link and DS, as described in (3.29). An increased value of K_{uti} results in lower conduction losses as the silicon is used more effectively. To facilitate continuous operation during cell failure, redundant cells should be included in each chain-link, so that the failed cell can be replaced during a maintenance cycle. As a result the MMC and AAC topologies are tested with 400 and 244 cells per arm respectively [79], which includes approximately 11% extra cells in each case. Since in HVDC applications an AAC must contribute to AC voltage or reactive power control, its V_{chain} modulation index can be controlled around the typical optimal operating point $M = \frac{4}{\pi}$, benefiting from the AC and DC voltage decoupling offered by the FB cells. By exploiting this feature and the redundancy of FB cells, the converter AC line-to-line voltage is increased to 500kV, in order to achieve flexible operation as the AAC varies its power exchange.

4.2.3 Types of cell semiconductors

The main semiconductor component used in HVDC VSCs, including multilevel converters, is the silicon (Si) IGBT due to its high voltage blocking and high current rating capabilities. Although the use of Si IGBTs is straightforward, the efficiency offered by these devices even when combined in simple arrangements such as HB cells, may not be as good as that which may be achieved using other devices or semiconductor materials.

An alternative solution would be to use thyristor devices, such as the integrated gate-commutated thyristor (IGCT). The conduction loss of these device is limited to almost half that of that of a Si IGBT. Despite the very low conduction losses, the switching losses are almost three time higher than those of an IGBT due to increased energy loss incurred in the IGCT gate driver. Devices such as the fast-switching Silicon Carbide (SiC) MOSFET, which uses wide bandgap SiC, offer a potential alternative to IGBTs, which suffer from relatively slow turn-on and turn-off times and, therefore, increased switching losses. However, in SiC MOSFETs, conduction losses are slightly increased while the current capabilities are still limited to a few hundred amps. Therefore, it is necessary to connect multiple SiC MOSFETs in parallel to achieve the same capabilities as a single Si IGBT, thus increasing the complexity of the cell topology.

Another alternative to a single Si IGBT is the hybrid switch (HS) [80], which

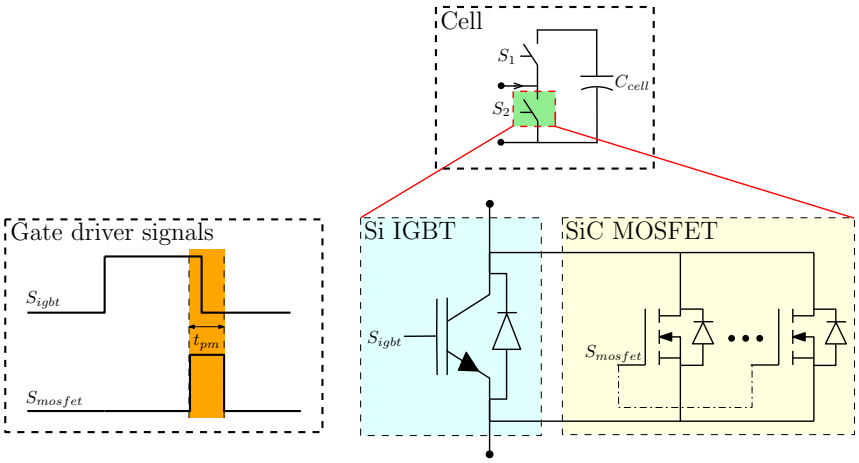
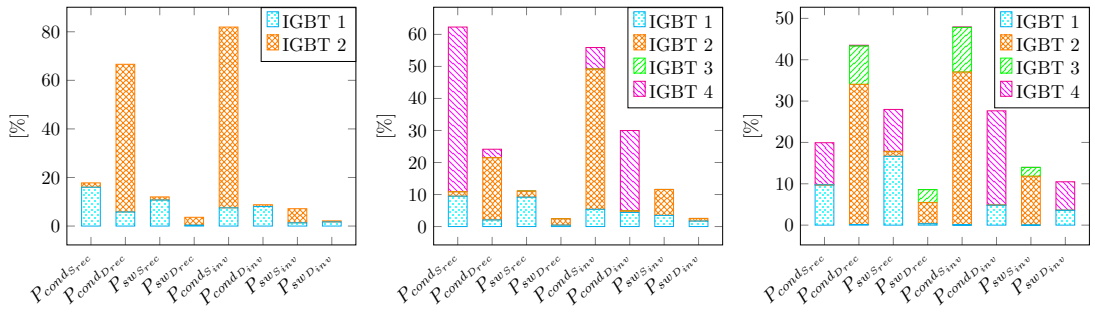


Figure 4.1: Arrangement of hybrid switch.

includes parallel-connected Si and SiC devices, as illustrated in Fig. 4.1, resulting in reduced switching losses. The HS is controlled in such a way that the SiC MOSFET conducts the main current during turn-off. In this way, the IGBT on-state loss and MOSFET switching speed performances are both exploited to achieve minimal loss. As shown in Fig. 4.1 the SiC MOSFET experiences a short duration current pulse, enabling peak currents that significantly exceed the rated value. However, the HS device topology results in increased semiconductor area which may impact overall reliability. Additionally, switching signal control adds to the complexity, as the SiC MOSFET needs to turn-on before the turn-off of the Si IGBT. When deployed in HB or FB cells, the possibility of having to introduce extended underlap (dead times) may increase the switching losses.

4.3 Semiconductor losses

Detailed loss distribution between individual switching devices of the FB and HB cells in MMC and AAC converters and between the diodes and IGBTs in a IGBT module are shown in Fig 4.2 according to the semiconductor arrangement in Fig. 3.5. In an IGBT module, which incorporates an inherent anti-parallel diode, the IGBT incurs more power loss than the diode. Hence, an HB cell incurs lower power loss during rectification operation (i.e. power flow from the AC to the DC side which is assumed as positive power flow). This is because during rectification mode, the majority of conduction is through the diode. In an FB cell, the loss distribution remains similar during inverter and rectifier modes. This is due to the fact that the numbers of diodes and IGBTs in the conduction path remain the same in both inverter and rectifier modes. Even though the number



(a) HB-MMC cell (b) FB-MMC cell (c) FB-AAC cell

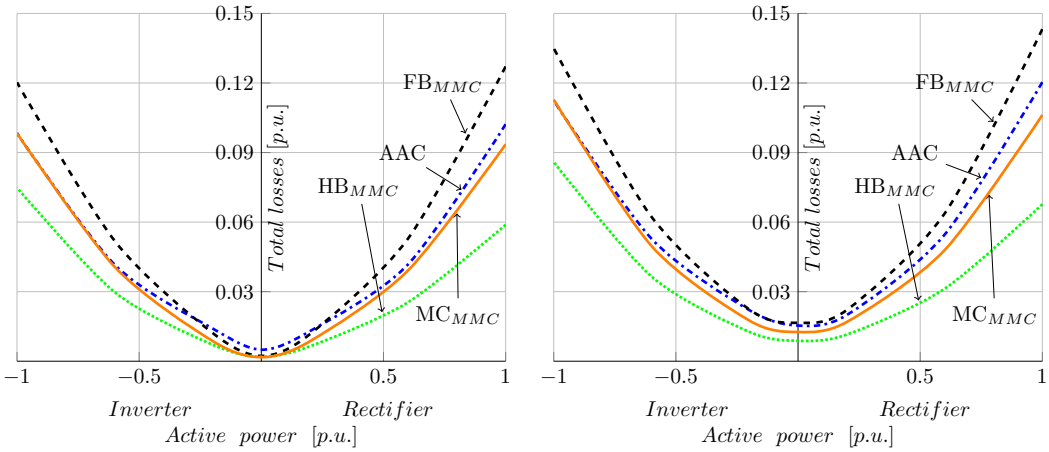
Figure 4.2: Cell loss distribution over the total cell losses during inverter (inv) and rectification (rec) mode.

of semiconductor devices in the conduction path in an AAC is the same as that in an MMC, the detailed loss distribution in the FB cell of the AAC exhibits different behaviour to that in the MMC. Table 4.1 illustrates the contribution of FB and HB cells, and DS to conduction and switching losses in each topology (where applicable).

Among the MMC topologies, the switching losses remain the same as only two switches are required to change their states (Tables 3.1 and 3.2), while the increased switching losses observed in the AAC are due to operation in the over-modulation region where a cell's negative polarity voltage must be exploited, and the switches operate more frequently. Fig. 4.3 shows that the total semiconduc-

Table 4.1: Loss contributions (inverter mode: $P = 1$ p.u., $Q = 0$ p.u.).

[kW]	AAC	FB	HB	MC
Cond. FB	4477 (44%)	11592 (91%)	-	5794 (62%)
Cond. HB	-	-	4749 (81%)	2372 (26%)
Cond. DS	4058 (39%)	-	-	-
Sw. FB	1686 (17%)	1119 (9%)	-	595 (6%)
Sw. HB	-	-	1136 (19%)	593 (6%)
Sw. DS	0 (0%)	-	-	-



(a) $Q = 0$ MVAr (b) $Q = 300$ MVAr

Figure 4.3: Total semiconductor losses at various operating points for AAC and MMC.

tor losses when the HB-MMC operates in inverter mode are more than half those of the FB-MMC, as the majority of the conduction is through the IGBTs. However, such losses are lower in rectification mode, as the majority of conduction is through the diodes. The DS in the AAC are responsible for almost half of the conduction losses while they produce zero switching losses due to zero voltage switching. Table 4.2 shows that the reduction in the number of cells increases the switching losses, since a larger number of series-connected IGBTs switch for any given value of instantaneous current, while the conduction losses are only affected by the values of the utilisation factor K_{uti}.

Table 4.2: Effect of K_{uti} on MMC.

N_{cell}	K_{uti}	*Cond. Losses* [kW]	*Sw. Losses* [kW]
20	0.99	4268	1246
100	0.89	4747	1222
400	0.89	4749	1136

The tested converters use the NLC strategy, whilst the effective switching frequency for 20, 100 and 400 cells per arm is 4 kHz, 20 kHz and 80 kHz respectively. For a reduced number of levels, PWM is employed, which may lead to higher switching losses as the cells switch according to the carrier switching frequency.

Table 4.3 shows the losses among different semiconductor implementations

of hybrid switches, defined in Cases 1 to 4, in the cells of a 400 cell HB-MMC. Short conduction time $t_{pm} = 10$ μs may allow the SiC devices to operate above rated current. SiC MOSFETs are arranged to match the ratings of a 3.3 kV, 1500 A Si IGBT [78]. Mitsubishi and Cree SiC MOSFETs are considered. The Mitsubishi SiC MOSFET arrangement consists of 16 parallel-connected 3.3 kV SiC MOSFETs and silicon body diodes SBD [81]. The Cree arrangement consists of two series connected 1.7 kV SiC MOSFETs [82]. Due to the use of incomplete data-sheet, variations of one, two and three rows in parallel are considered, as the true limitations of the semiconductor are still unknown. The tested cases can be summarised as:

Case 1 One Si IGBT in parallel with 27 Mitsubishi 3.3 kV SiC MOSFETs.

Case 2 One Si IGBT in parallel with one row of two-series connected Cree 1.7 kV SiC MOSFETS.

Case 3 One Si IGBT in parallel with two rows of two series-connected Cree 1.7 kV SiC MOSFETS.

Case 4 One Si IGBT in parallel with one row of three series-connected Cree 1.7 kV SiC MOSFETS.

Table 4.3: Effect of hybrid switch on total losses per arm.

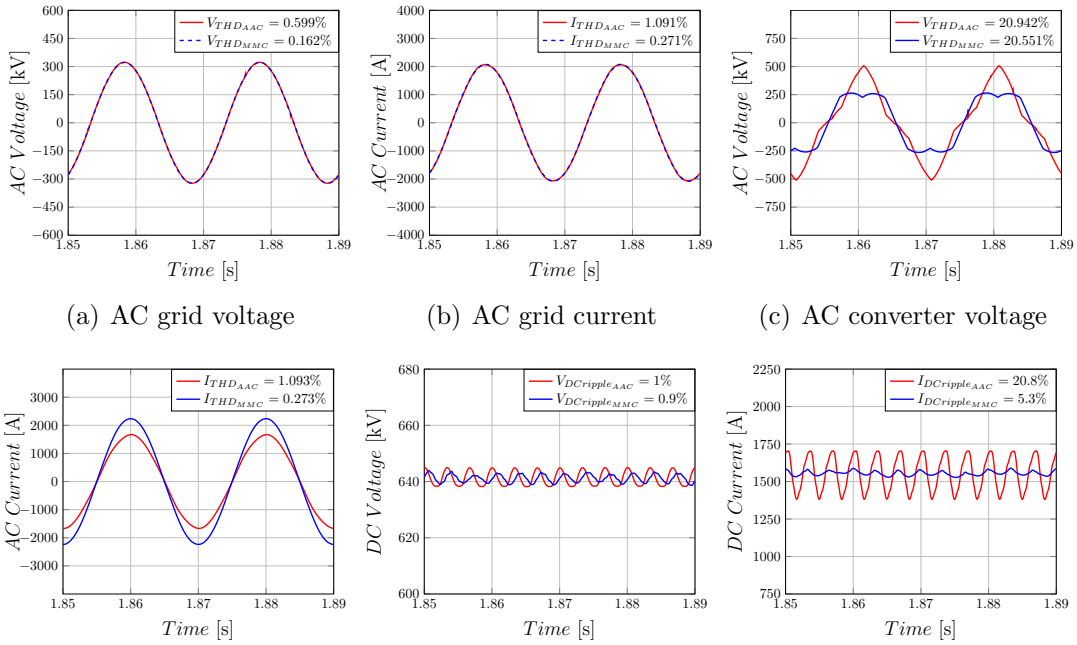
Losses		Basic MMC	Case 1	Case 2	Case 3	Case 4
IGBT	Cond. Losses [kW]	764.5	764.5	764.5	764.5	764.5
	Sw. Losses [kW]	-	0.6	11.7	4.9	2.7
MOSFET	Cond. Losses [kW]	301.6	161.1	161.1	161.1	161.1
	Sw. Losses [kW]	-	76.2	11.8	23.9	36.1
Total	Cond. Losses [kW]	301.6	237.3	172.9	185.0	197.2
	Sw. Losses [kW]	764.5	765.1	776.2	769.4	767.2
% loss change	Cond. Losses [%]	0.0	-21.3	-42.7	-38.7	-34.6
compared to	Sw. Losses [%]	0.0	0.1	1.5	0.6	0.4
basic MMC	Total losses [%]	0.0	-6.0	-11.0	-10.5	-9.5

In all cases the cell conduction losses are slightly increased as the IGBTs and MOSFETs conduct simultaneously for a brief period. However, the IGBT switching losses are reduced by more than half, and the reduction in switching losses outweighs the slight increase in conduction losses. Increasing the number of parallel-connected MOSFET strings reduces total losses, although switching loss reduction decreases as more MOSFETS are switched for a given voltage. However, by parallel-connecting more semiconductors, the HS should show high reliability due to the increased current sharing resulting in reduced device stress. The reduction in switching losses is, however, noticeable.

SiC MOSFETs have increased forward voltage drop even at lower temperatures (25^oC, $R_{DS} = 8$ mΩ per MOSFET), while the arrangements of SiC MOSFETs detailed in Cases 1 to 4, have a forward voltage drop equal to 4.8 V. The equivalent Si IGBT (25 ^oC, 3.3 kV, 1500 A) has only 2-2.8 V saturation voltage due to conductivity modulation. For SiC MOSFETs at higher temperatures, the voltage drop will worsen due to higher R_{DS}. Parallel connection of the MOSFETs may reduce the conduction losses. It would require approximately 10 parallel connected SiC MOSFETs to match the conduction losses of an IGBT module. However, conduction losses are also dependent on the overlap conduction time t_{pm} (0-5 μs) shown in Fig. 4.1, and the over current capacity of the SiC MOSFETs.

4.4 Power quality

Fig. 4.4 shows that both converters have high-quality AC waveforms with very low total harmonic distortion (THD). However, for future DC grids, which involve connections with multiple converters, DC power quality should also be considered. DC current I_{DC} determines the fluctuations in cable loading while DC voltage affects the design of cable insulation [83]. According to IEC-60287 (the standards applicable to the conditions of steady-state operation of cables at all alternating voltages), the DC current response of the cables is a function of the differential temperature variation between the conductor and ambient. Cable insulation requirements are calculated based on temperature variation, which is affected by low-frequency current ripple [84]. Consideration of DC current ripple is critical during the design process of DC cables, and potential integration of AAC into multi-terminal systems. From Fig. 4.4(f), it is evident that the DC current of the AAC exhibits high-magnitude 6^th harmonic ripple, which is due to the fundamental operation of the AAC. The quality of DC waveforms is affected by the number of cells employed in each arm, as shown in Fig 4.5. A low

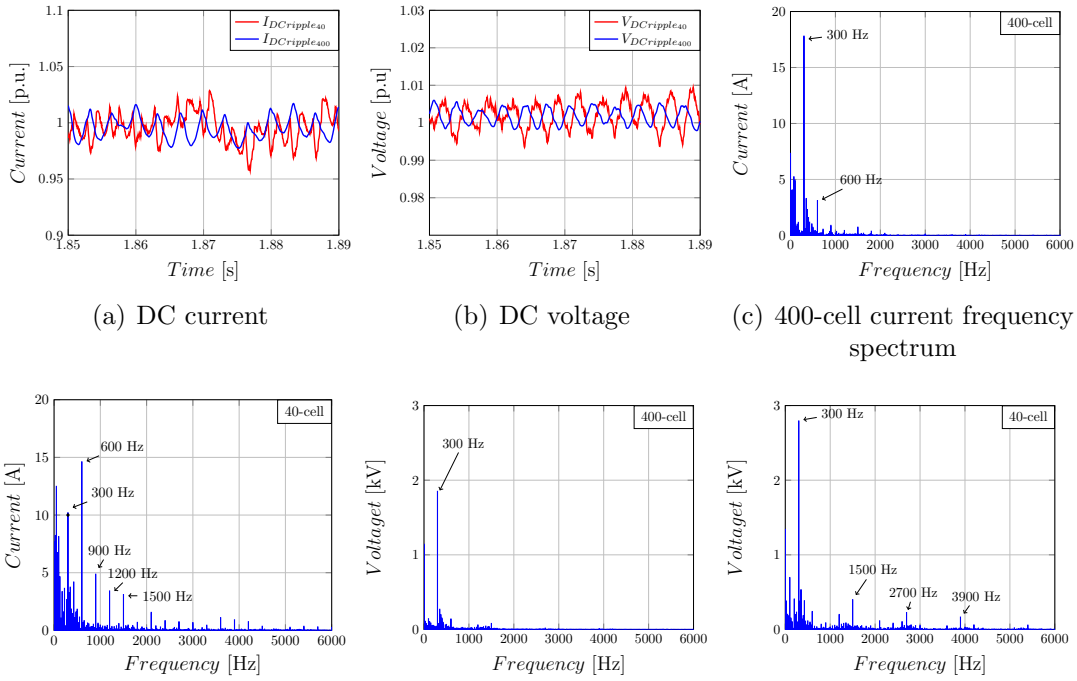


(a) AC grid voltage (b) AC grid current (c) AC converter voltage

(d) AC converter current (e) DC voltage (f) DC current

Figure 4.4: MMC and AAC output voltage and current quality.

number of cells per arm leads to higher voltage step transitions, and this causes larger voltage mismatches between the differential voltage and DC voltage. By comparing the DC current and DC voltage ripple for a 40-cell and a 400-cell MMC, it can be deduced that the higher the number of cells, the lower the DC current and voltage ripple range. The voltage and current ripples show in the DC side are primarily at 300 Hz, and are more likely due to the interactions between different controllers that maintain the internal dynamics of the MMC. Typically, these ripples are attenuated by installing DC filters at the converter DC bus. The plots for THD of the AC-side waveforms (pre-filter, line-to-line voltages and phase currents) in Fig. 4.4, and those of pole-to-pole DC voltage and DC link current ripple in Fig. 4.6, indicate the inferiority of the AAC compared to the MMC in terms of AC and DC power quality. It should be noted that the AC and DC side power quality of the MMC with large and reduced numbers of cells remains practically unchanged. This due to the fact that converters operate at rated active power and between rated capacitive and inductive reactive power. Nevertheless, the quality of the DC waveforms in AAC worsens as its reactive power output increases, while the DC voltage ripple of the AAC quickly exceeds 3%, which is accepted as an informal standard [85], during steady state operation and within the rated capability of the converter. Normally, THI does not appear in the DC voltage of the MMC, as it is cancelled by the complementary opera-



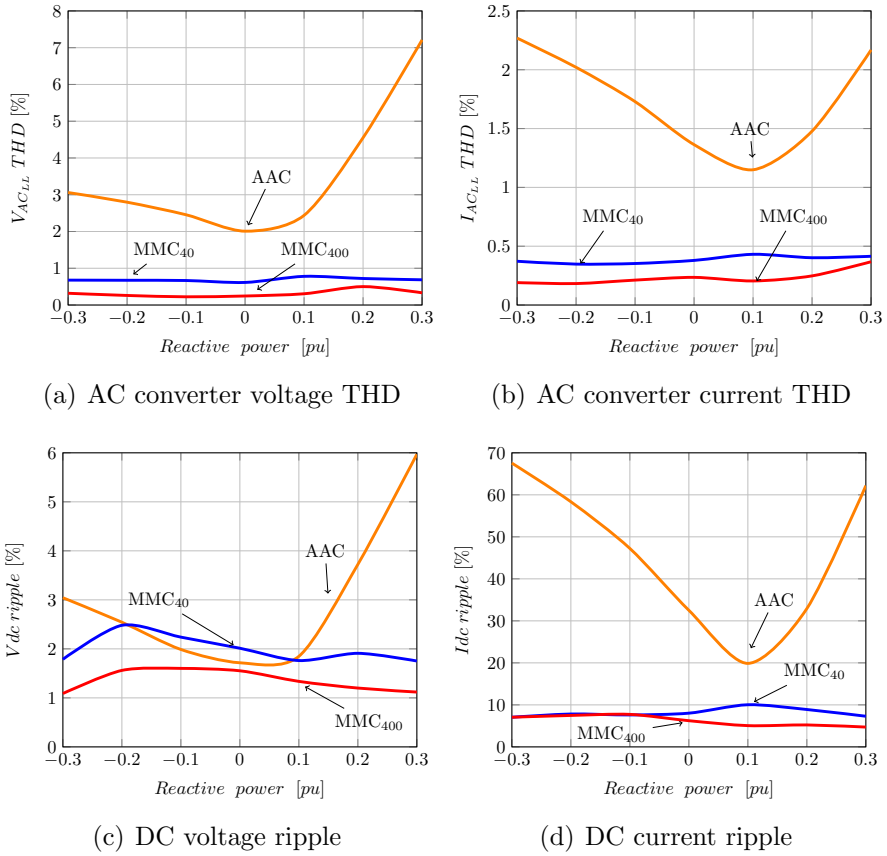
(a) DC current (b) DC voltage (c) 400-cell current frequency spectrum

(d) 40-cell current frequency spectrum (e) 400-cell voltage frequency spectrum (f) 40-cell voltage frequency spectrum

Figure 4.5: MMC DC voltage and current harmonics for 40 and 400 cells per arm.

tion of the arm voltage. However due to the fundamental operation of AAC, any injected harmonic in the arm voltages appears in the DC voltage as an added component. Therefore, a dedicated DC filter for THI must be implemented to cancel the 3^{rd} and 6^{th} harmonics and their multiples. The plots in Fig. 4.6 show the AAC DC current ripple when DC smoothing inductors with values of 10 mH, 50 mH, 100 mH and 300 mH are considered. Fig. 4.7 includes the DC current ripple when an enhanced filter is used for 3^{rd}, 6^{th} and 12^{th} harmonic attenuation, with lumped values $L_{DCf} = 0.3$ mH and $C_{DCf} = 145.5$ μF, which is similar to the short overlap method [86]. The high-value capacitance used in the enhanced filter will increase the amount of energy discharged during a DC fault.

The same harmonic components can be suppressed with an only inductive low-pass filter. As the AAC does not need arm inductance due to the fast operation of the DS, the lumped values of the upper and lower arm inductances can be placed on the positive and negative poles on the DC side. However, a small value inductance must be present in the arms in order to absorb the high-frequency switching components [86]. The 12.5% (100 mH) DC inductance at the DC link of the AAC reduces the DC current ripple to 10%, which is similar to that



(a) AC converter voltage THD

(b) AC converter current THD

(c) DC voltage ripple

(d) DC current ripple

Figure 4.6: AAC and MMC, AC and DC power quality during variable Q for P = 1 p.u.

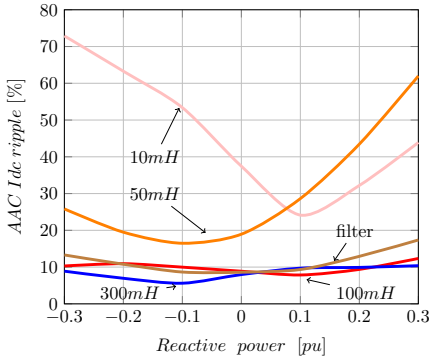


Figure 4.7: AAC DC current ripple for various installed DC inductances and filters.

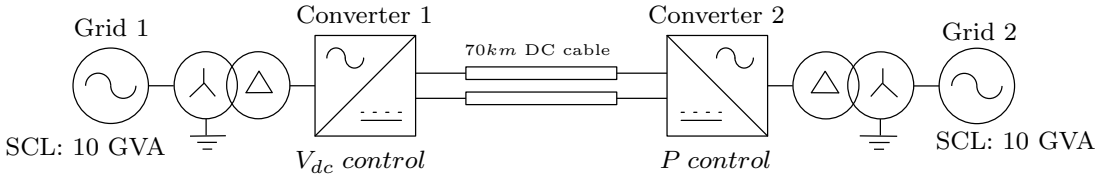
achieved in the extended overlap method [87]. No reduction of great significance can be observed in the DC current ripple when increased inductance of 300 mH is used. DC inductances of 100 mH and 300 mH gives similar harmonic performance to the enhanced filter which included increased capacitance. It should be noted

that, whilst the DC smoothing inductor reduces current ripple, it must be sized for rated DC current.

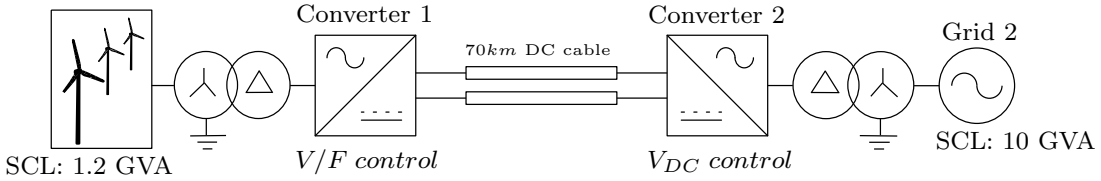
4.5 Dynamic operation

Controller operation is tested through offline simulations, in order to validate the dynamic action of the converters for their dedicated PQ envelope of capabilities. The network consists of two converters in a symmetric monopole configuration which are connected via DC cables (wideband cable model). In each case the controllers are tuned accordingly to minimise interactions between the converter controllers. Three types of controllers, P, V_{DC} and V/f shown in Fig. 4.8, are applied in the demonstration of dynamic variation of active and reactive power, and DC voltage over all four quadrants of operation. The strong grids are modelled as equivalent Thevenin voltage sources with short circuit level (SCL) = 10. V/f control is applied to demonstrate the ability of the converter to operate in islanding mode connected to a WF. The details for the model of the WF are provided in Appendix C.

Table 4.4 shows the rating and design specifications for each converter topology, similar to the INELFE project [89]. The P-Q capabilities of the MMC and AAC are given in Fig. 4.9. Both converters have similar capabilities regarding the power delivery during inverter and rectifier modes for unity power factor. For any DC voltage value, power delivery is limited by the current carrying capability of the cables. Hence, if the converter has the ability to operate at lower DC voltage, the DC current always has a fixed limit resulting in lower power operation.



(a) Point to point HVDC network connected to strong AC grids.



(b) Point-to-point HVDC network connected to a WF and a strong AC grid

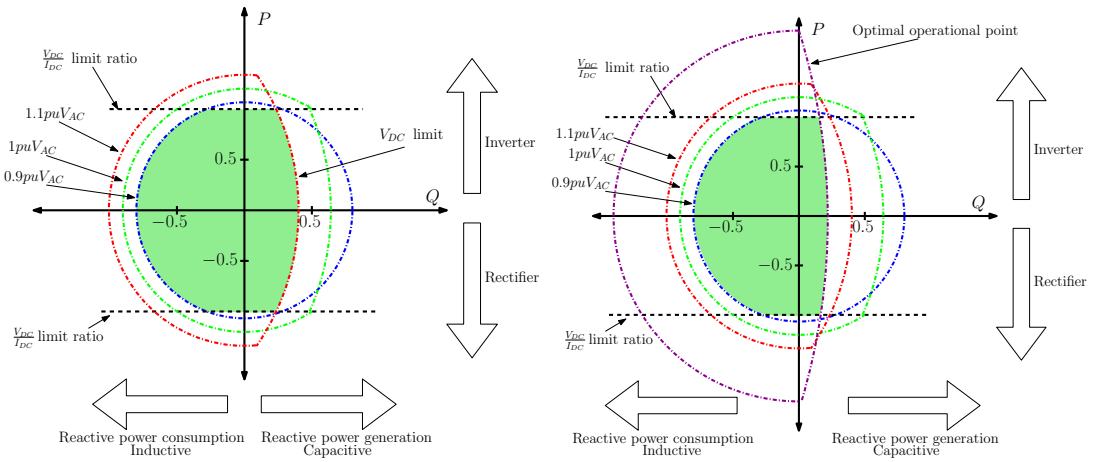
Figure 4.8: HVDC test networks.

Both converters have similar reactive power consumption ability, limited by the AC voltage value, which cannot be less than 90% of the nominal value. This limit also defines the cell capacitor voltage ripple which tends to be in the range of 10% of the nominal DC voltage. In the case of reduced DC voltage operation the cell capacitors experience higher voltage ripple, hence the reactive power operation is further limited. This leads to the main difference between the MMC and the AAC, which is their reactive power generation capabilities. During capacitive operation, the converter has to generate higher AC voltage for leading AC current.

Table 4.4: AAC and MMC parameters.

Parameter		AAC	MMC
Active power	S[MVA]	1045	
DC voltage	V_{DC}[kV]	640	
Transformer reactance	X_{tr}[%]	18	
Cell capacitor energy	$E[\frac{kJ}{MVA}]$	35	
Number of cells per chain-link	N	20	
Chain-link and DS voltage	V_{chain}/V_{DS}[kV]	388/604	640/-
Grid and converter LL voltage	$V_{LL_{grid}}/V_{LL_{conv}}$[kV]	400/500	400/320
Arm inductance	L_{arm}[mH]	11.14	65.36
Phase reactor	L_{ph}[mH]	37.8	-

The increased AC voltage may reach the voltage thresholds of the converter, regarding insulation levels and cell voltage ripple, for lower equivalent reactive power than that consumed during inductive operation. Hence the reactive power generation limit is further reduced compared to that during inductive operation. In the case of the MMC, the limit is bounded to the upper AC voltage threshold which is approximately 110% of the nominal AC voltage value. However, in AAC, due to the over-modulation procedure for creating the optimal operating point, the reactive power generation limit is further reduced. For any type of converter the reactive power capabilities are bound to the DC voltage. Therefore, if DC voltage is limited, reactive power is further limited. Nevertheless, the MC-MMC and FB-MMC can further benefit from their extended DC voltage operation capability and continually operate within the designed P-Q envelope. MC-MMC and FB-MMC, due to their degree of freedom on modulation index, can maintain



(a) MMC (b) AAC

Figure 4.9: Active and reactive capability converter envelope.

the AC voltage for reduced DC voltage operation, which allows the exploitation of active and reactive power limited only by the DC current thresholds and cell capacitor voltage ripple. In Fig. 4.9 the shaded area shows the nominal operating region of the converters. However, in reality, the reactive capabilities are further limited to operate within a safe margin, and to protect converter insulation. Hence, in the case studies, the converters are designed to operate with maximum active power $P = 1$ p.u. and reactive power $Q = 0.25$ p.u.

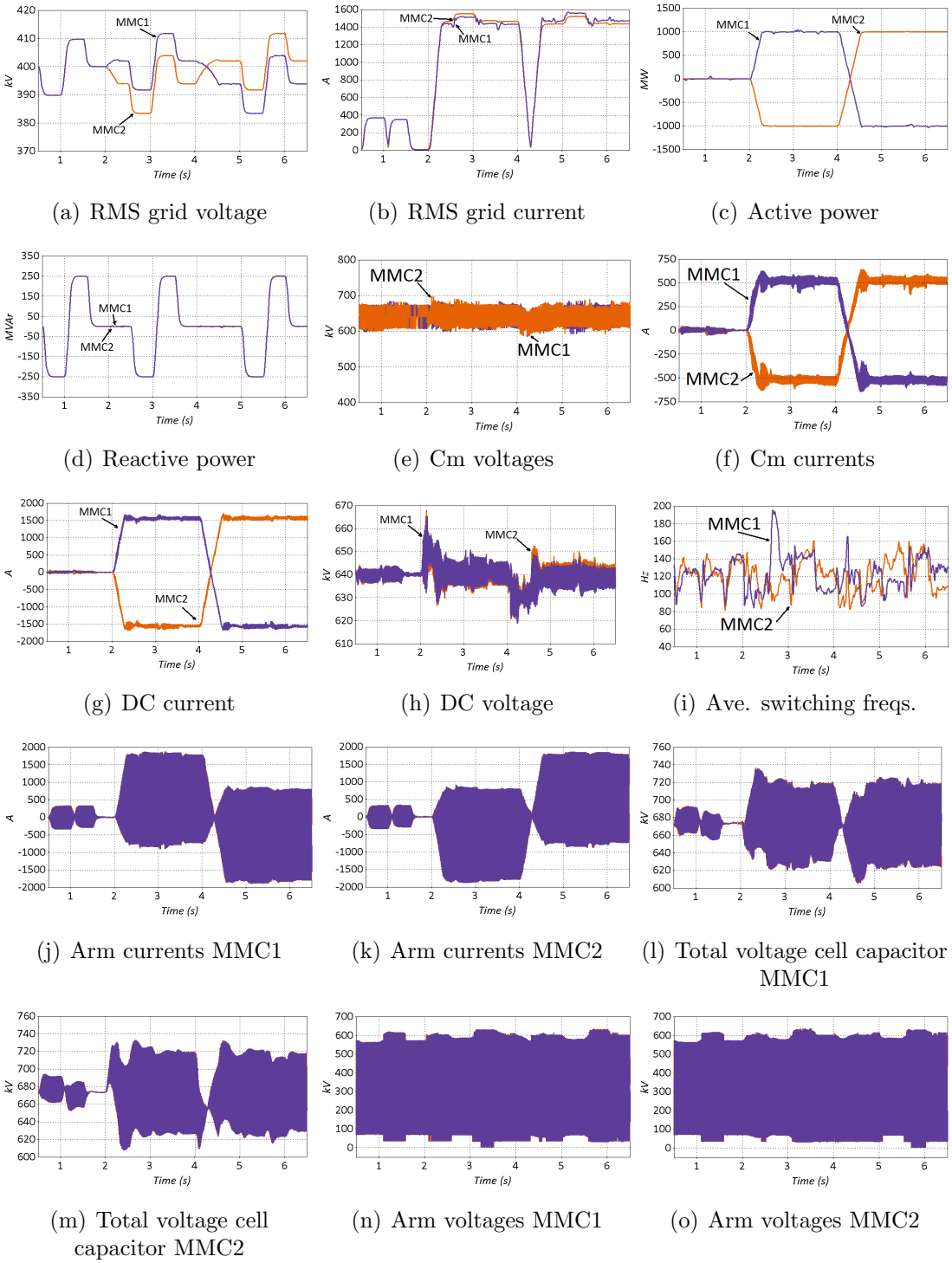
4.5.1 Operation over four quadrants with P control

This section shows the MMC and AAC converter and control abilities operating under P control, as shown in Fig. 4.8(a), during active and reactive power dynamic operation, over the entire P-Q range of the converter with ramp rate 4 p.u./s.

MMC

A full P-Q envelope demonstration for the MMC is illustrated in Fig. 4.10. As the DC voltage is limited to operate at its fixed nominal value, the following results are representative for all types of MMC (HB, MC and FB) as the need for over-modulation is not incorporated.

During the first 2 seconds of operation, the MMC operates as a STATCOM and provides and consumes reactive power. The AC converter voltages are generated as the arm voltages are adjusted according to the modulation index. The common-mode (cm) and DC currents are observed to stay zero, while arm cur-



(a) RMS grid voltage (b) RMS grid current (c) Active power

(d) Reactive power (e) Cm voltages (f) Cm currents

(g) DC current (h) DC voltage (i) Ave. switching freqs.

(j) Arm currents MMC1 (k) Arm currents MMC2 (l) Total voltage cell capacitor MMC1

(m) Total voltage cell capacitor MMC2 (n) Arm voltages MMC1 (o) Arm voltages MMC2

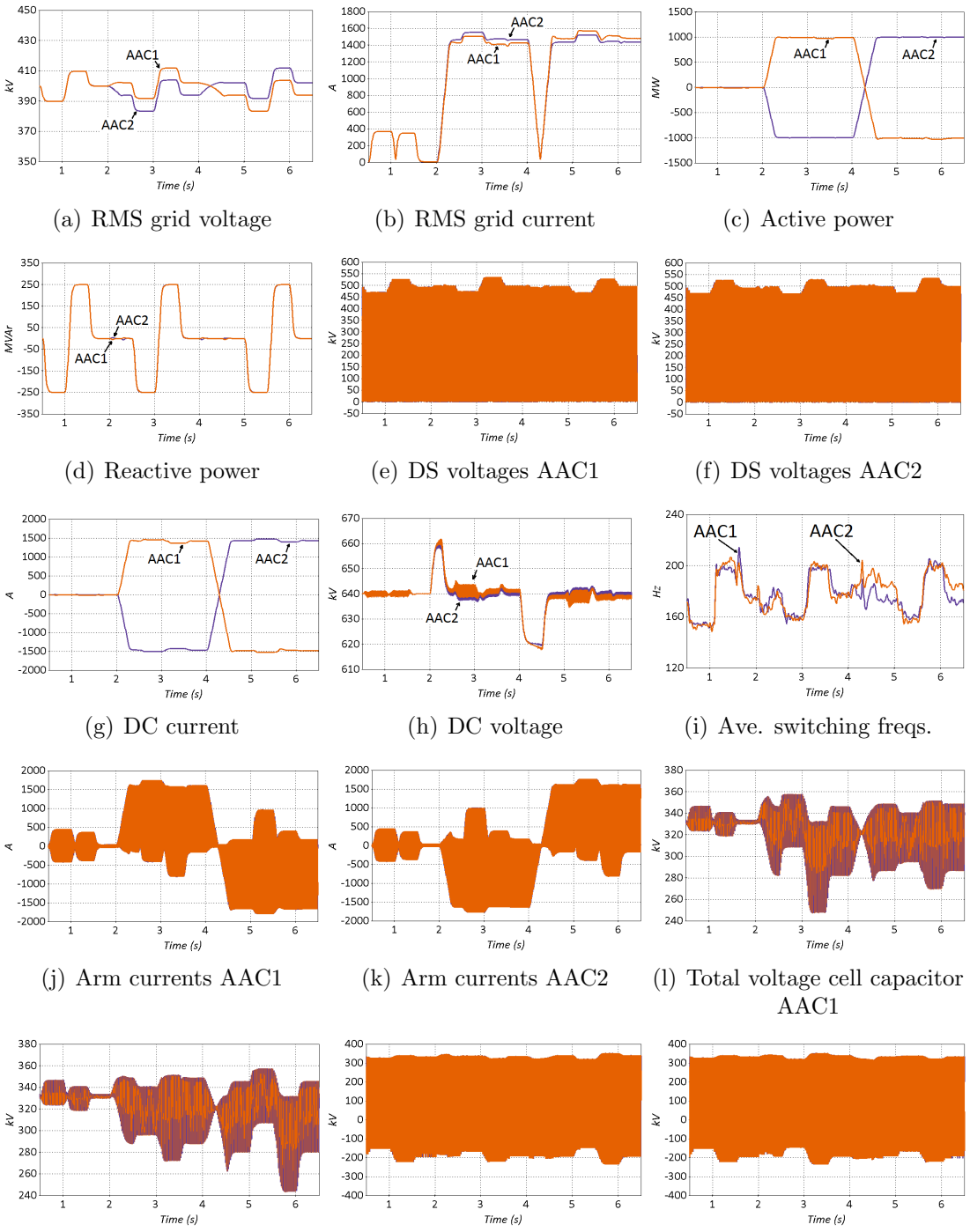
Figure 4.10: Dynamic response of active and reactive power controllers in a point-to-point MMC DC network.

rents provide the reactive currents, which can also be seen in the grid currents. As the DC voltage is maintained, and the reactive power that is provided is relatively lower than the nominal active power, the reactive currents are small in magnitude. Hence, the capacitor voltages experience low voltage ripple.

Ramping the active power, at $t = 2$ s, the DC voltage experiences an overshoot. For lower ramp-rate the converter DC voltage may have lower DC overshoot, until it settles to its nominal value under the control of Converter1 (MMC1 in this case). The cm current also oscillates for a few milliseconds. Additionally, due to the relatively low number of cells, the arm voltage quality increases the cm voltage and current ripple. A power reversal occurs at $t = 4$ s, which causes an undershoot in the DC voltage. The effect of power reversal can also be observed in the arm, cm and DC currents. Furthermore, the capacitor voltages are well balanced around the nominal value, while the ripple fluctuates according to power factor cosϕ. AC voltage and current deviate according to converter operating mode (rectification or inversion) and power factor. Additionally, the AC current difference between MMC1 and MMC2 during active power operation can indicate the losses in the DC grid. The average the cm voltage is relatively constant and exhibits error equivalent to one cell capacitor voltage, even during power reversal. This indicates arm voltage balance in each phase. Finally, the average switching frequency of the converter is kept low, showing that the switching losses and the temperature increase due to switching are well regulated.

AAC

A full P-Q envelope demonstration for AAC is illustrated in Fig. 4.11. Identical as with on MMC, the AAC shows STATCOM operation during the first seconds of operation. The modulation index changes which result from the P control action only affect the negative chain-link voltages, whilst the positive chain-link voltages stay relatively constant. The negative chain-link voltage profile is mirrored in the voltage seen across the DS. The DC voltage experiences lower ripple than in the MMC due to the DC filter. The AC voltages and currents are adjusted to be identical to those in the MMC in the previous demonstration, to provide the required active and reactive powers. Fig. 4.12 shows expanded waveforms over a narrow time span of those shown in Fig. 4.12(a), during three distinct modes of operation, i.e. STATCOM, unity power factor and cosϕ=0.97. During STATCOM (t = 0-2 s) and unity power factor (t = 2-5 s) operation, the arm currents di/dt do not generate any phase voltage overshoot, as confirmed by the cm voltage shown in Fig 4.13. However, during simultaneous transfer of active and reactive power transfer, the hard-switched DS interrupts the arm currents.



(a) RMS grid voltage (b) RMS grid current (c) Active power

(d) Reactive power (e) DS voltages AAC1 (f) DS voltages AAC2

(g) DC current (h) DC voltage (i) Ave. switching freqs.

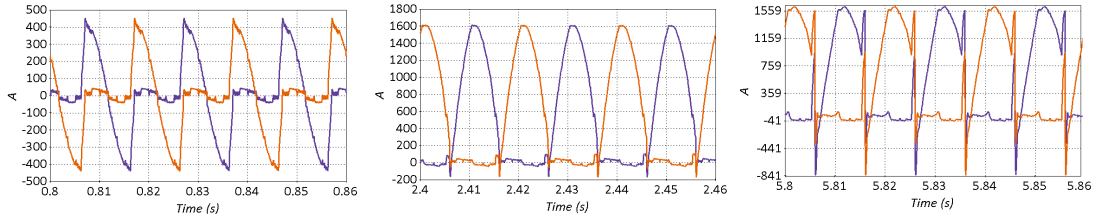
(j) Arm currents AAC1 (k) Arm currents AAC2 (l) Total voltage cell capacitor AAC1

(m) Total voltage cell capacitor AAC2 (n) Chain-link voltages AAC1 (o) Chain-link voltages AAC2

Figure 4.11: Dynamic response of Active and Reactive power controllers in a point-to-point AAC DC network.

The consequent di/dt results in overvoltage across the phase as shown in the common-voltage in Fig. 4.13.

Such overvoltages can be destructive for the converter insulation, since Fig. 4.13 shows that the exceed the nominal voltage by 90% for extended periods of operation. The surge arresters that are placed in each arm have to suppress the overvoltages to achieve nominal operation, which may deteriorate the power quality and the reliability of the converter. Additionally, during operation with the surge currents, the capacitor voltage ripple is increased. Nonetheless, the average switching frequency of the converter is well regulated, and the temperature increase due to switching loss is maintained within design limits.



(a) P=0 MW, Q=250 MVAr (STATCOM) (b) P=1000 MW, Q=0 MVAr (cosϕ=1) (c) P=1000 MW, Q=250 MVAr (cosϕ=0.97)

Figure 4.12: AAC arm currents for various operating set-points.

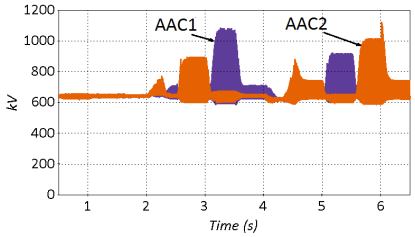


Figure 4.13: AAC common-mode arm voltages

4.5.2 Operation over four quadrants with V_{DC} control

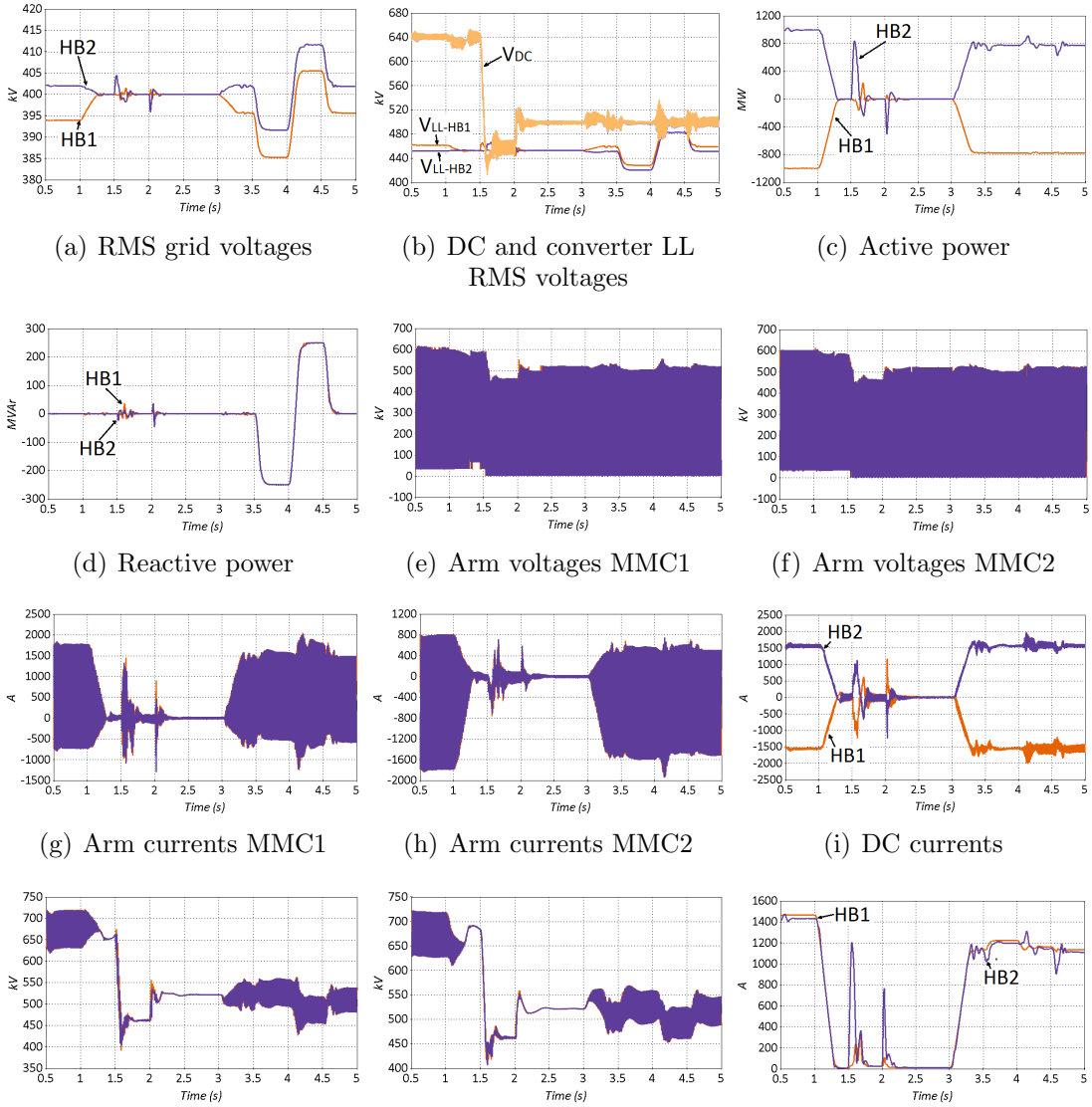
This section demonstrates how the converter performs when transferring rated power at reduced DC voltage. Whilst the preceding section was able to consider all variants of the MMC in a single study, the following study must consider each variant individually due to the different voltage capabilities of their cells.

HB-MMC

In an HB-MMC the minimum controllable operating DC voltage V_{DC} is equal to the magnitude of the rectified line-to-line AC voltage. In order to exploit the PQ capabilities of the converter the cell capacitor voltage ripple dV_{cell} must also be considered. The minimum operating DC voltage for an HB-MMC is therefore defined by:

$$V^*_{DC_{min}} = \widehat{V}_{AC_{LL}} + 2\frac{V_{DC}}{N}dV_{cell} \tag{4.10}$$

Fig. 4.14 shows the operation of an HB-MMC during reduced DC voltage. In order to reduce the risk of losing control of the converter, the active power has been set to zero. DC voltage is therefore initially reduced to $\frac{V_{DC}}{\sqrt{2}}$. The DC voltage controller dynamics produce a voltage undershoot at $t = 1.5$ s as shown in Fig. 4.14(b). This undershoot can also be seen in the capacitor voltage shown in Figs. 4.14(j) and 4.14(k). As a result, converter control is briefly lost, leading to surge currents in the converter arms and on the DC and AC sides, as shown in Fig. 4.14(i) and 4.14(l) respectively. A $t = 2$ s, a new voltage reference is set according to (4.10). At the new value of DC voltage the amount of power transfer is limited by the DC current as shown in Fig. 4.14(i). During non-unity power factor operation, the AC voltage is adjusted for inductive and capacitive reactive power. During inductive reactive power flow, the converter operates normally as the AC voltage is reduced, as shown in Fig. 4.14(a) at $t = 3.5$ s. However, during capacitive reactive power transfer the converter briefly reaches the AC voltage limit, at $t = 4.2$ s. Surges are observed in the DC and arm currents as shown in Figs. 4.14(i), 4.14(g) and 4.14(h). These currents are a direct consequence of the dynamics of the reactive power controller. During reduced DC voltage operation, the controller generates modulation indices that exceed the capabilities of the converter. Nevertheless, the converter operates up to unity modulation index where the lower limit of the arm voltages is zero, as shown in Figs. 4.14(e) and 4.14(f), as they cannot take a negative value in order to operate in the over-modulation region.



(a) RMS grid voltages

(b) DC and converter LL RMS voltages

(c) Active power

(d) Reactive power

(e) Arm voltages MMC1

(f) Arm voltages MMC2

(g) Arm currents MMC1

(h) Arm currents MMC2

(i) DC currents

(j) Total cell capacitor voltages MMC1

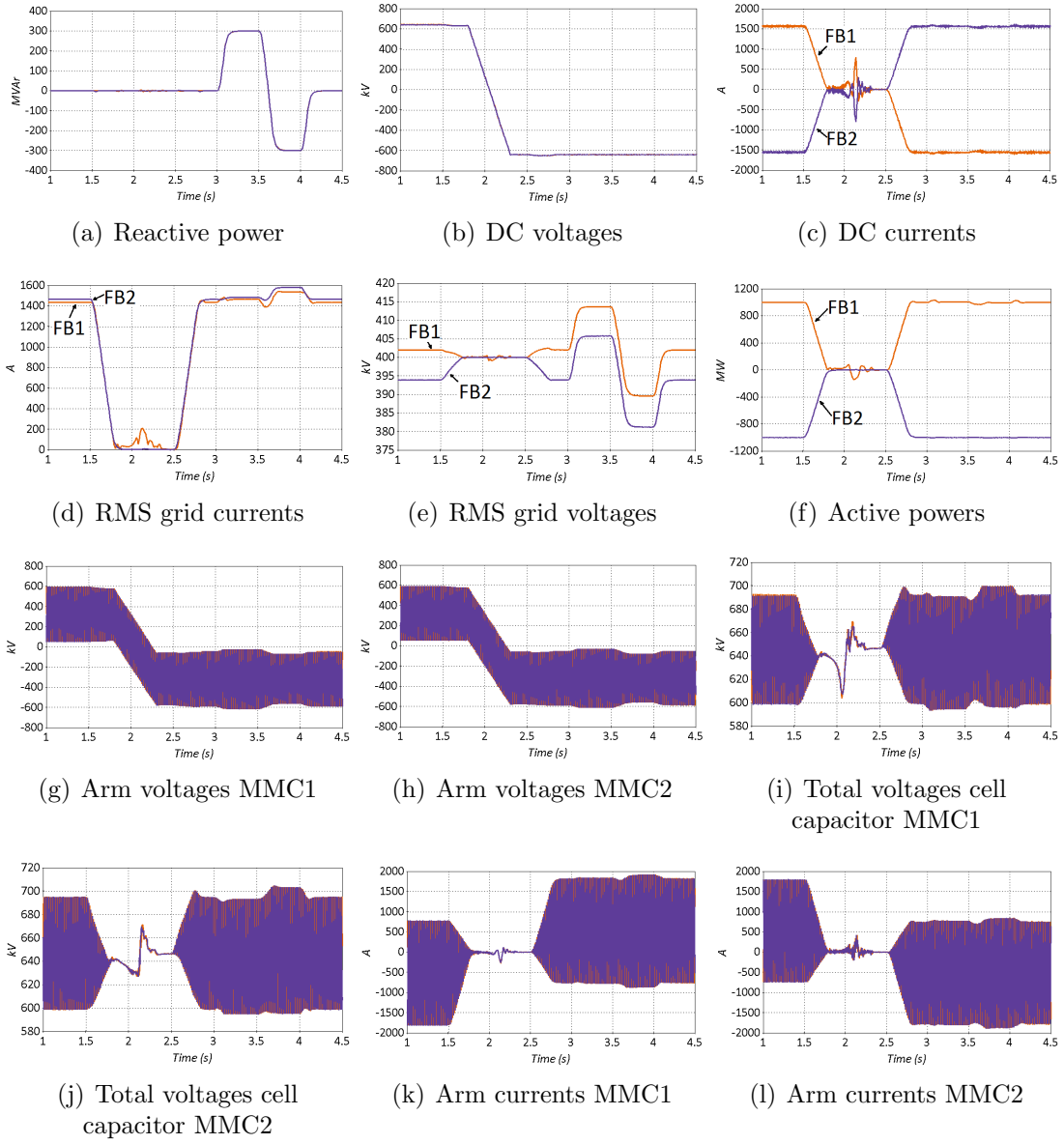
(k) Total cell capacitor voltages MMC2

(l) RMS grid currents

Figure 4.14: Dynamic response of DC and Reactive power controllers on a point-to-point HB-MMC DC network.

FB-MMC

An FB-MMC is able to operate in the full over-modulation region, which allows the generation of the negative arm voltages up to negative DC link voltage. Fig. 4.15 shows the ability of an FB-MMC to reverse the DC voltage.



(a) Reactive power (b) DC voltages (c) DC currents

(d) RMS grid currents (e) RMS grid voltages (f) Active powers

(g) Arm voltages MMC1 (h) Arm voltages MMC2 (i) Total voltages cell capacitor MMC1

(j) Total voltages cell capacitor MMC2 (k) Arm currents MMC1 (l) Arm currents MMC2

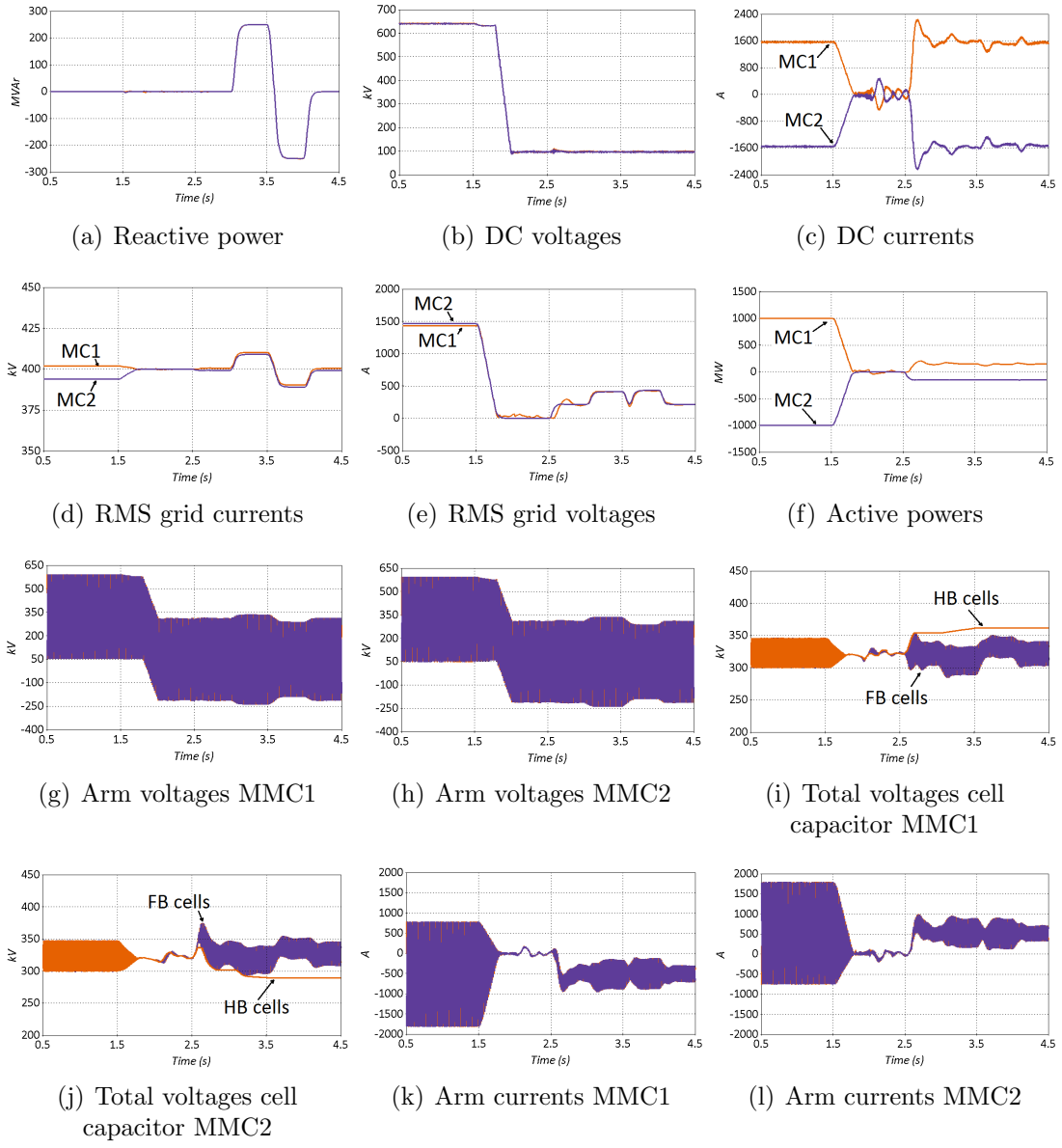
Figure 4.15: Dynamic response of DC and Reactive power controllers on a point-to-point FB-MMC DC network.

During DC voltage reversal, the active power has to be zero to avoid surge currents. During DC voltage reversal, the voltage passes through zero, at which point the converter enters a region of uncontrollability as zero voltage does not allow natural maintenance of the cell capacitor voltages. Surge currents therefore occur. After V_{DC} settles to a negative DC voltage determined by the controller DC voltage reference, the cell capacitor voltages settle to their nominal value and the arm voltages are negative. Throughout the DC voltage reversal the AC

voltage does not change as shown in Fig. 4.15(e). Following DC voltage reversal full power transfer is still possible if the current direction is also reversed as shown Figs. 4.15(f) and 4.15(c) respectively. This operation can be achieved for a hybrid HVDC grid which incorporates an LCC and VSC technologies, as in LCC power reversal is achieved by reversing the DC voltage. However, such an operation has to be combined with the appropriate cable technology, as the XLPE cables that are used mainly in HVDC-VSC do not allow DC voltage reversal due to the way their insulation is manufactured [90]. This functionality can be achieved with oil impregnated cables, but these are considered to be environmentally hazardous.

MC-MMC

The MC-MMC can be considered to be an FB-MMC with a limited over-modulation range. In the case where the converter does not need to create negative DC link voltages, an MC-MMC with a cell ratio of HB:FB=1 is sufficient to create zero DC link voltages and block DC faults. In this study the DC voltage is reduced to 15% of the nominal value allowing full P-Q capabilities, restricted only by the DC current limits. In order to reduce the DC voltage the active power reference is set to zero. After setting the DC voltage to the new limited value (15% of nominal), the arm voltage operates between the positive and negative voltages shown in Fig. 4.16(g) and 4.16(h) allowing the AC voltage shown in Fig. 4.16(e) to be unaffected by the reduced DC voltage as shown in Fig. 4.16(b). Setting the active power to be limited according to the new DC voltage allows the converter to operate at the DC current limit. However, the DC current can be high due to the controller dynamics and the equivalent power ramp rate. For 1 p.u. DC voltage, the power ramp rate of 4 p.u./s is set according to 4 p.u./s DC current. However due to the limited DC voltage, the 0.15 p.u. DC voltage equates the 4 p.u./s power ramp rate to 26.67 p.u./s DC current ramp rate. As a result, the dynamics of the outer and inner controllers cause DC current overshoots as shown in Fig. 4.16(c) at $t = 2.5$ s. As a result a limited power ramp rate is required. Nevertheless, during the reduced DC voltage operation the HB cells cease to operate as the FB cells are sufficient to create the positive and negative arm voltages as shown in Figs 4.16(i) and 4.16(j).



(a) Reactive power (b) DC voltages (c) DC currents

(d) RMS grid currents (e) RMS grid voltages (f) Active powers

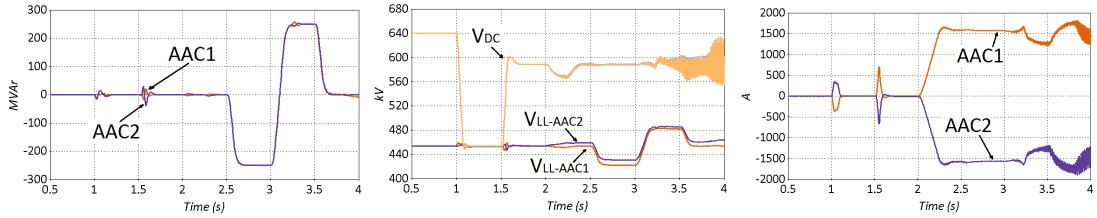
(g) Arm voltages MMC1 (h) Arm voltages MMC2 (i) Total voltages cell capacitor MMC1

(j) Total voltages cell capacitor MMC2 (k) Arm currents MMC1 (l) Arm currents MMC2

Figure 4.16: Dynamic response of DC and Reactive power controllers on a point-to-point MC-MMC DC network.

AAC

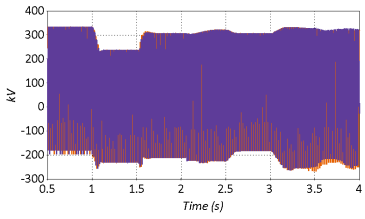
The AAC has an absolute minimum DC voltage $\frac{V_{DC}}{\sqrt{2}}$. In order to maintain the energy balance between the AC and DC sides the converter has to operate at an optimal operating point, as described in detail in Chapter 3. However, if this optimal operating point is violated it is not possible to operate in the nominal operating region of the P-Q envelope, as described in Fig. 4.9(b). To operate at reduced DC voltage the active power reference must be set at zero.



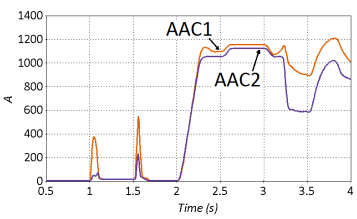
(a) Reactive power

(b) DC and converter LL RMS voltages

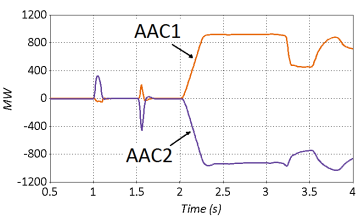
(c) DC currents



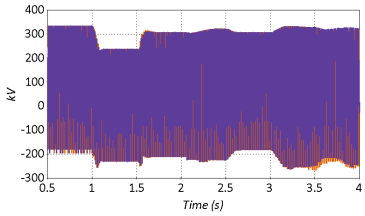
(d) RMS grid voltages



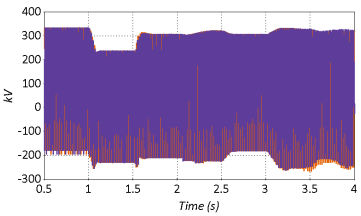
(e) RMS grid currents



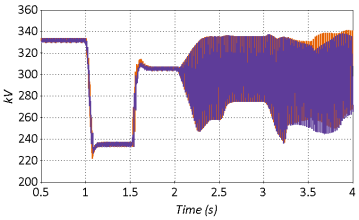
(f) Active powers



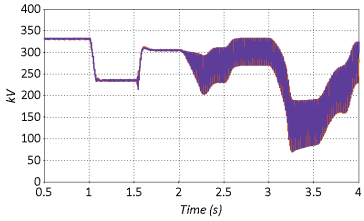
(g) Chain-link voltages AAC1



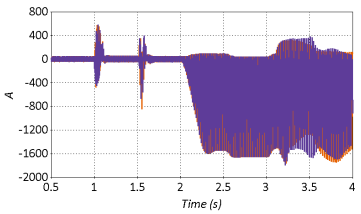
(h) Chain-link voltages AAC2



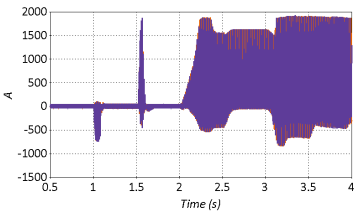
(i) Total voltages cell capacitor AAC1



(j) Total voltages cell capacitor AAC2



(k) Arm currents AAC1



(l) Arm currents AAC2

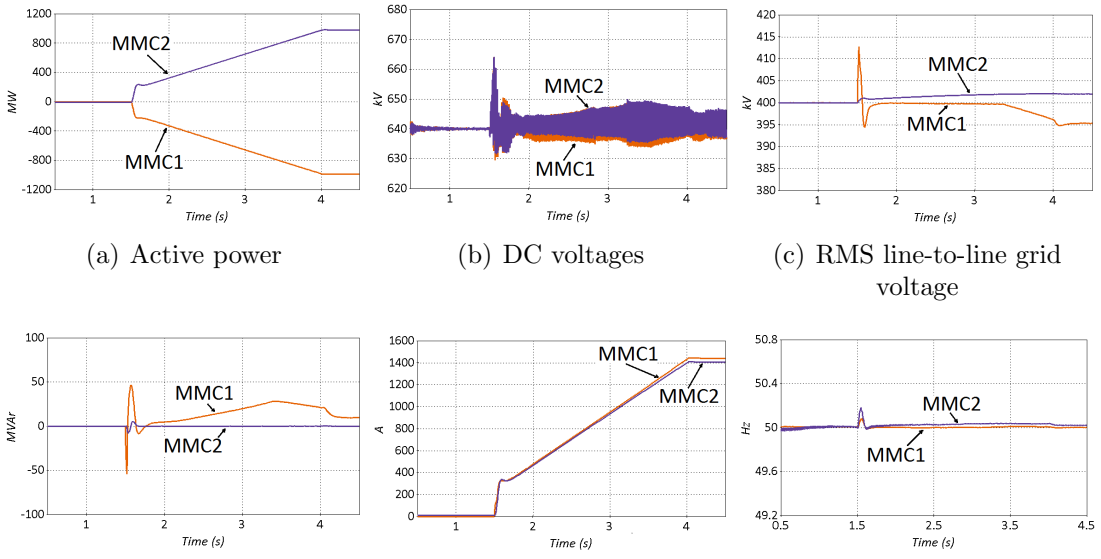
Figure 4.17: Dynamic response of DC and Reactive power controllers on a point-to-point AAC DC network.

At $t = 1$ s the new DC voltage reference is set to $\frac{V_{DC}}{\sqrt{2}}$ as shown in Fig. 4.17(b). However, in order to maintain the optimal operating point while achieving power flow the DC voltage is set at 90% of the nominal value at $t = 1.5$ s. When inductive reactive power is demanded at $t = 2.5$ s the converter continues to operate as normal. At $t = 3$ s when the capacitive reactive power is demanded converter operation moves away from the optimal operating point. Energy balance the AC and DC sides is lost and converter control is lost as shown in Fig. 4.17(e). This

demonstrates that AAC is not able to operate with reduced DC voltage over the entire PQ envelope.

4.5.3 Operation over four quadrants with V/f control

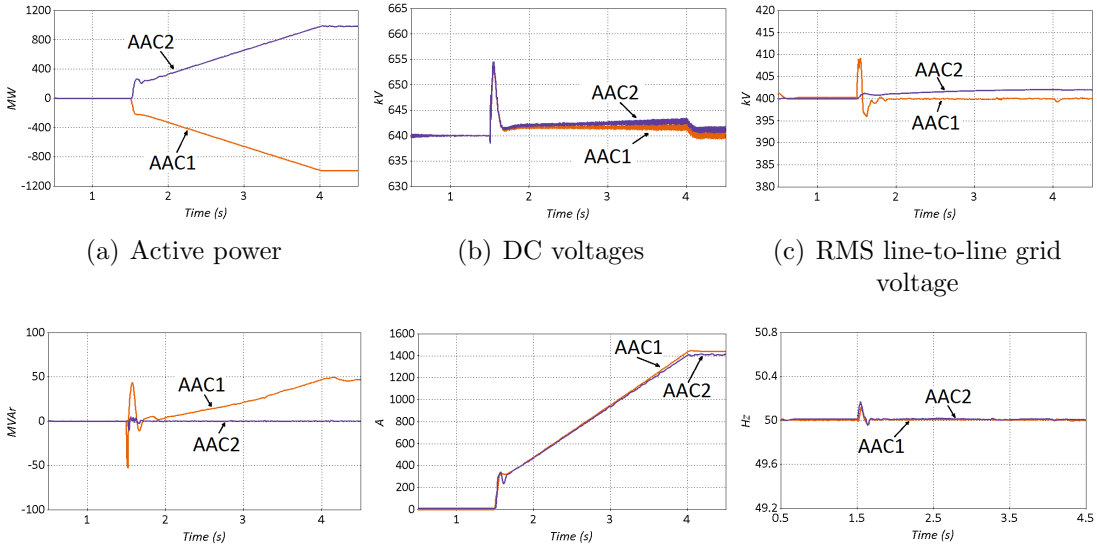
This section shows converter and controller operation for a point-to-point network which includes an islanded converter under V/f control, and a non-islanded converter under DC voltage control, as is illustrated in Fig. 4.8(b). The converter under V/f control is connected to an aggregated WF which is equivalent to 167 WTs of 6 MW each [88]. Fig. 4.18 shows simulations of WF connection and power transfer for an MMC based network. Fig. 4.19 illustrates the same investigation for an AAC based network. In both cases, when the AC circuit breakers are closed at $t = 1.5$ s, connecting the WF to the network, the WT pitch controller gradually increases the power supplied to the network. The different converter topologies generate different magnitudes of AC voltage, as shown in Figs. 4.18(c) and 4.19(c), in order to achieve the required output frequency, as shown in Figs. 4.18(f) and 4.19(f). However, as shown in Fig. 4.18(d) and Fig 4.19(d), to achieve the same goal the AAC reactive power requirement is greater than that of the MMC resulting in marginally increased stress on the AAC.



(a) Active power (b) DC voltages (c) RMS line-to-line grid voltage

(d) Reactive power (e) Activeff power (f) PLL frequency

Figure 4.18: Dynamic responses of MMC on V/f controller with WF connection.



(a) Active power (b) DC voltages (c) RMS line-to-line grid voltage

(d) Reactive power (e) Active power (f) PLL frequency

Figure 4.19: Dynamic responses of AAC on V/f controller with WF connection.

4.6 Summary

This Chapter presents a comprehensive comparison between AAC and MMC topologies, using high-fidelity converter models, and including all the necessary controllers for ensuring overall converter stability. The main conclusions drawn from these studies are summarised as follows.

- At unity power factor, the power quality at the DC side (DC current and voltage waveforms) of the AAC is marginally lower than that of the MMC, and deteriorates as power factor decreases. This means that an HVDC link that employs an AAC requires substantial DC filtering to prevent penetration of the low-frequency harmonics from the converter into the DC side.

- The power quality at the AC side (AC current and voltage waveforms) of the AAC is marginally lower than that of the MMC. However, the rate of the deterioration of the AC power quality with power factor is much slower than that observed in the DC sides. This means smaller AC filters could be sufficient to meet the harmonic requirements at the point of common coupling.

- The MMC with a reduced number of cells exhibits lower DC-side power quality when compared to that with an increased number of cells. This implies that DC filters are necessary to prevent penetration of high-frequency

harmonics from the converter into the DC link. There is only a slight difference in AC power quality between two configurations.

- The presented results reveal that in rectification mode, the AAC has higher losses than the MC-MMC, and the power losses of each converter converge as active power increases in inverter mode. Among the modular designs, the FB-MMC and HB-MMC have been found to possess the highest and lowest losses respectively.

- The semiconductor power loss distributions between the individual switching devices of the FB cell in MMCs (FB-MMC, MC-MMC) and AACs, differ even when the operating conditions for both topologies are the same. The MMC with a reduced number of cells exhibits higher switching losses compared to an MMC with a higher number of cells. This is on the grounds that the switching losses will be greatly influenced by the number of IGBTs to be switched simultaneously during turn-on and turn-off, for a given arm current.

- A switching loss reduction can be achieved by incorporating state-of-the-art semiconductors by synthesising a hybrid switch, exploiting the robustness of Si-IGBTs during the conduction period, and the switching speed and reduced losses of the SiC-MOSFETs during turn-off operation.

- At rated power in rectification mode, the HB-MMC semiconductor losses represent 50% of those of the FB-MMC, while in inverter mode they increase to nearly 60% of those of the FB-MMC.

- In AAC the optimal operating point has to be maintained across the full range of P-Q capabilities. Any deviation in DC voltage amplitude may violate the optimal operating point and result in loss of converter control.

- MMC can achieve the full range of P-Q operation for different values of DC voltage. The HB, MC and FB MMC variants offer full P-Q operation over different ranges of DC voltage. For each variant appropriate cell capacitor voltage, DC current, and AC and DC voltage thresholds must be observed at all times to ensure normal operation.

Chapter 5

Performance comparison of state-of-the-art voltage source converters during transient operation

5.1 Introduction

This chapter presents an exhaustive study of state-of-the-art HVDC converters, having a common specification and operating under a range of transient conditions. All converters are subjected to an identical set of test scenarios to enable a true like-for-like comparison of performance. Converter operation is assessed to determine true performance advantages and limitations over a wide-range of operating scenarios. This enables informed selection of the converter topology most suited to a given application. It provides guidance in the design of innovative converter topologies, such as that presented in Chapter 7, and informs the development of solutions to converter-specific operating challenges.

Studies of the dynamic and transient performance of the AAC and MMC topologies, with DC fault blocking capability, are presented. The studies focus on start-up sequences, operation during unbalanced AC phase-to-ground faults, reduced DC voltage operation, and pole-to-pole DC faults, including system re-energisation. Simulation results are used to highlight the capabilities of each converter topology, and the operating strategies that are required to ensure safe and stable DC network operation. In multi-terminal HVDC systems, converters with DC blocking capability are an attractive solution due to their ability to quickly recover from DC-side faults. The MMC and the AAC are both the subject of considerable industry and research interest. Both MMC and AAC

topologies include FB cells which can reverse the cell voltage and therefore block DC current. Reverse blocking MMCs may be based on two alternative structures with blocking capability: namely the FB-MMC and the MC-MMC, where the MC-MMC exhibits better efficiency.

A converter station must be protected from overvoltage stresses in order to sustain the lifespan of the components, and overcurrent to avoid equipment overheating. Moreover, transient phenomena must be supressed in order to secure robust operation of the AC and DC grids. The full spectrum of transient behaviours needs to be observed in order to conclude which topology is more viable for a given application. A well-designed set of tests, employing accurate time-domain models is used to evaluate and compare the relative merits and performance trade-offs between different converter implementations during the charging sequence, unbalanced AC faults, and DC faults. The study is conducted using high-fidelity models developed in Chapter 3 in order to ensure efficient use of simulation resources, and to reflect realistic attributes that are characteristic of real-scale projects. Converters are compared using performance indicators such as cell capacitor voltage ripple, arm current, and DC and AC side voltages and currents.

5.2 Simulation set-up

Each MMC arm includes a series connection of FB or HB cells which determine the converter's characteristics and attributes. Specifically, in the case of the HB-MMC, the operational modulation index is only positive and, consequently, there is no DC fault blocking capability. The HB topology ensures that total semiconductor losses are kept low. If, however, the installed cells are a mixture of HB and FB cells, the operational modulation index can also be negative, leading to more flexible operation. Specifically if the ratio of FB to HB cells exceeds 50% then the converter can block DC faults at the expense of increased losses, as explained in Chapter 4. Each AAC arm consists of an array of series-connected FB cells, referred to as a 'chain-link', and a series connection of IGBTs which forms the DS. Due to the FB cells, an AAC can block DC faults whilst the semiconductor losses are kept relatively low. However, the AAC requires a DC filter in order to ensure acceptable DC power quality over a wide operating range.

To verify the operation of the converters and their dedicated controllers, a point-to-point HVDC network is utilised as shown in Fig. 5.1. The network consists of two converters in a symmetric monopole configuration which are con-

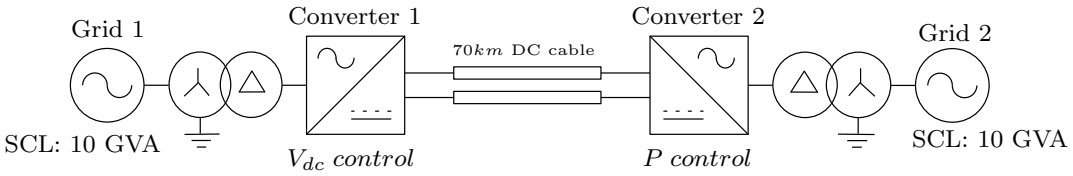


Figure 5.1: Simulated DC network.

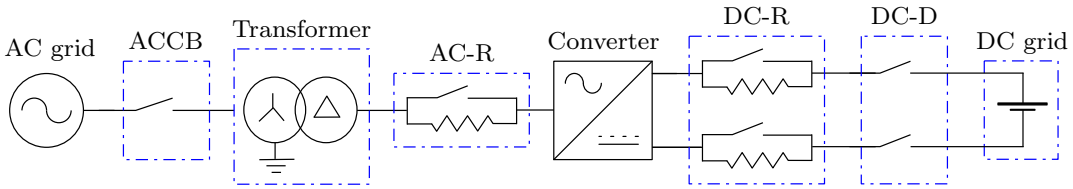


Figure 5.2: HVDC converter station equipment.

nected via DC cables (represented using the wideband cable model [91]).

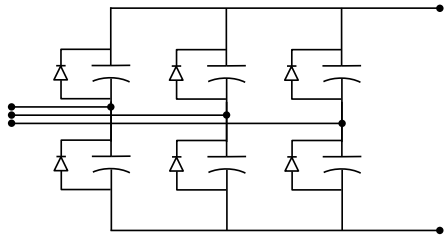
In each test, Converters 1 and 2 in Fig. 5.1 are of the same type in order to avoid interactions due to mixed converter topologies. Fig. 5.2 represents the HVDC converter stations shown in Fig. 5.2.

The ACCB is the AC circuit breaker capable of clearing AC faults and disconnecting the converter from the AC network. The transformer ensures galvanic isolation between the DC network and the AC grid whilst matching the AC converter and grid voltages, and sets the converter AC voltage according to the DC voltage level. Transformer leakage reactance filters current harmonics and contributes to AC current control. In some cases, the transformer is employed with the converter controller to adjust the voltage through tap changers to regulate the circulating currents. The AC-side pre-insertion resistors (AC-R) are employed during the charging process from the AC side in order to reduce the inrush currents that affect the converter. Usually they are inserted/bypassed with the help of a slow mechanical switch. The DC-side resistors (DC-R) have the same functionality as the AC-side resistors, being responsible for suppressing inrush currents that originate from the DC grid when the converter is energised from the DC side. DC-D is a slow mechanical DC disconnector which isolates the converter from the rest of the DC grid. Its operation is similar to that of the ACCB but, since it can only be opened when current flowing through it is near zero, it cannot be used to clear DC faults. Unlike its AC counterpart, this device must be capable of closing almost simultaneously to avoid voltage unbalance when the DC cable is already energised.

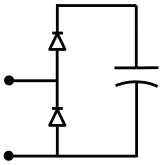
5.3 Start-up, charging operation

To ensure smooth and fast energisation, carefully managed start-up schemes are crucial in multilevel converter based HVDC systems. The start-up procedure for both MMC and AAC is complicated due to the need to charge distributed cell capacitors. Fig. 5.3(a) shows the equivalent uncontrolled charging circuit for MMC and AAC. In order to provide an active current path between the AC and DC sides, the HB cells must be in their blocking state, as shown in Fig. 5.3(b).

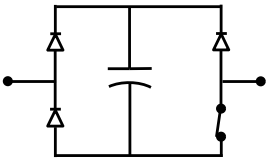
Fig. 5.3(c) shows the equivalent operation of an FB cell required to emulate the operation of an HB cell. If the FB cells do not emulate the operation of an HB cell, the DC grid cables are not able to charge, as the converter will block the current path. Fig. 5.4 shows detailed current paths during the uncontrolled



(a) MMC and AAC



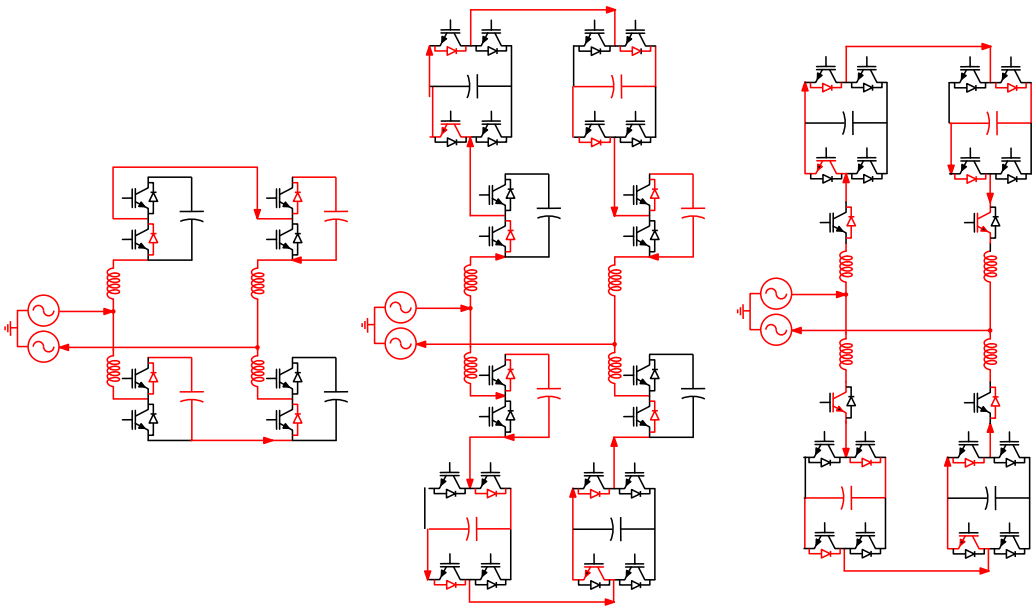
(b) HB-cell



(c) FB-cell

Figure 5.3: Equivalent circuits during charging process.

charging mode for HB-MMC, MC-MMC and AAC. The figure shows that for each converter, the current path between one pair of phases and shows that some cell capacitors are charged whilst others are bypassed. The uncharged cell capacitors will be charged according to the current path between another pair of phases. All cell capacitors will be charged in sequence according to the three-phase supply. In point-to-point systems such as that shown in Fig. 4.8(a), both converter stations are energised simultaneously and any transient effects are minimised [92]. This may not, however, be the case in multi-terminal grids where a converter may need to be isolated and then reconnected a short time later, whilst the rest of the grid remains operational. Transient effects may therefore significant. In very weak grids the AC supply cannot be used to charge the converter, and this instead must be achieved from the DC grid. The converter that controls the DC voltage



(a) HB-MMC (b) MC-MMC (c) AAC

Figure 5.4: Current path during uncontrolled charging from the AC side.

must always charge from the AC side: this converter assumes the role of the master converter which regulates the DC voltage.

5.3.1 MMC

In this section, the MMC start-up sequence is analysed, showing the charging procedures for MC, HB and FB-MMC topologies. Simulation results showing the current and voltage waveforms for the point-to-point network where the converter stations are both MC-MMC converters are presented in Fig. 5.2. The start-up sequence is described by Fig. 5.5.

In MMC station 1 (Converter Station 1 in Fig. 4.8(a)), the ACCB is closed at $t = 0.1$ s connecting the converter with the AC grid whilst the AC-R resistors are inserted, thereby minimising inrush current as shown in Figs. 5.6(a), 5.6(b) and 5.6(c). Also at $t = 0.1$ s, a transient in PLL frequency occurs, as shown in Fig. 5.6(d). Whilst this transient is compliant with the Grid Code, it may nonetheless activate protection relays. MMC station 2 (Converter Station 2 in Fig. 4.8(a)) is not affected as it is completely isolated by the DC-D. At time $t = 0.1$ s, MMC 1 enters the uncontrolled charging state, emulating a blocked MC-MMC where the converter is in a fixed state that allows AC current to charge the cell capacitors while the DC cables are also charged. As illustrated in Fig. 5.6(e), the capacitors charge simultaneous to the DC voltage increase. It should

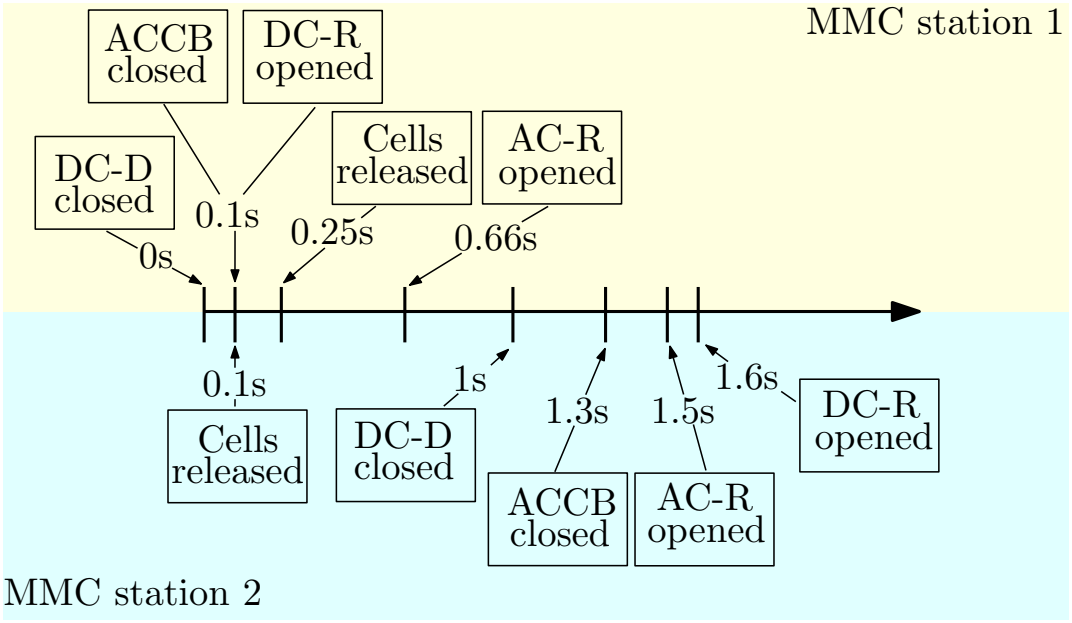


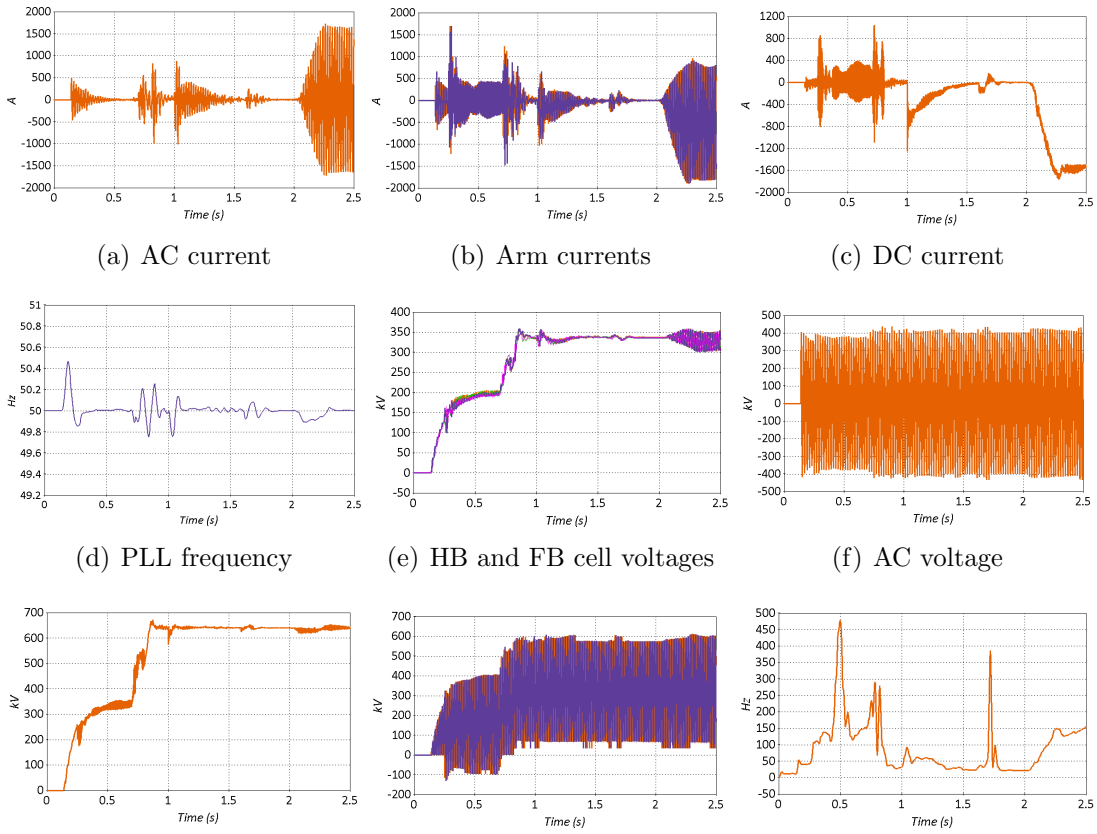
Figure 5.5: MC-MMC start-up sequence timings.

be noted that the DC-D and DC-R are disconnected throughout the AC charging process. The aforementioned uncontrolled charging state continues until $t = 0.6$ s when the arm voltage reaches the peak value of the rectified AC voltage, shown in Fig 5.6(f). Figs. 5.6(g), 5.6(e) and 5.6(h) show that the DC voltage, the cell capacitor voltages, and the arm voltage follow the same profile.

At $t = 0.7$ s the converter average switching frequency shows a distinct increase due to the rate of change of the cell voltages. This is the result of the controlled capacitor voltage balancing process, which attempts to track a voltage reference equal to the average value of capacitor voltage. This does not have any actual effect on the cell voltage as the cells are in the blocked/charging mode.

When the total cell capacitor voltage is equal to the RMS AC voltage, the cells are unblocked and enter the normal controlled operating mode. It is necessary that the AC-R are disconnected after the cells are unblocked in order to absorb any inrush currents due to unblocking of a large number of cells. As a result, the cells are unblocked at $t = 0.6$ s without any noticeable effect.

At $t = 0.65$ s the AC-R are disconnected. This is characterised by the mild AC current inrush due to the voltage recovery resulting from the removal of the connected resistors, as shown in Fig. 5.6(a). Also at this time, MMC station 1 establishes the DC network voltage, which increases to its nominal value. The ramp rate of the DC voltage controller reference affects two things. Firstly the switching frequency increases, which may increase the energy dissipation and thus



(a) AC current (b) Arm currents (c) DC current

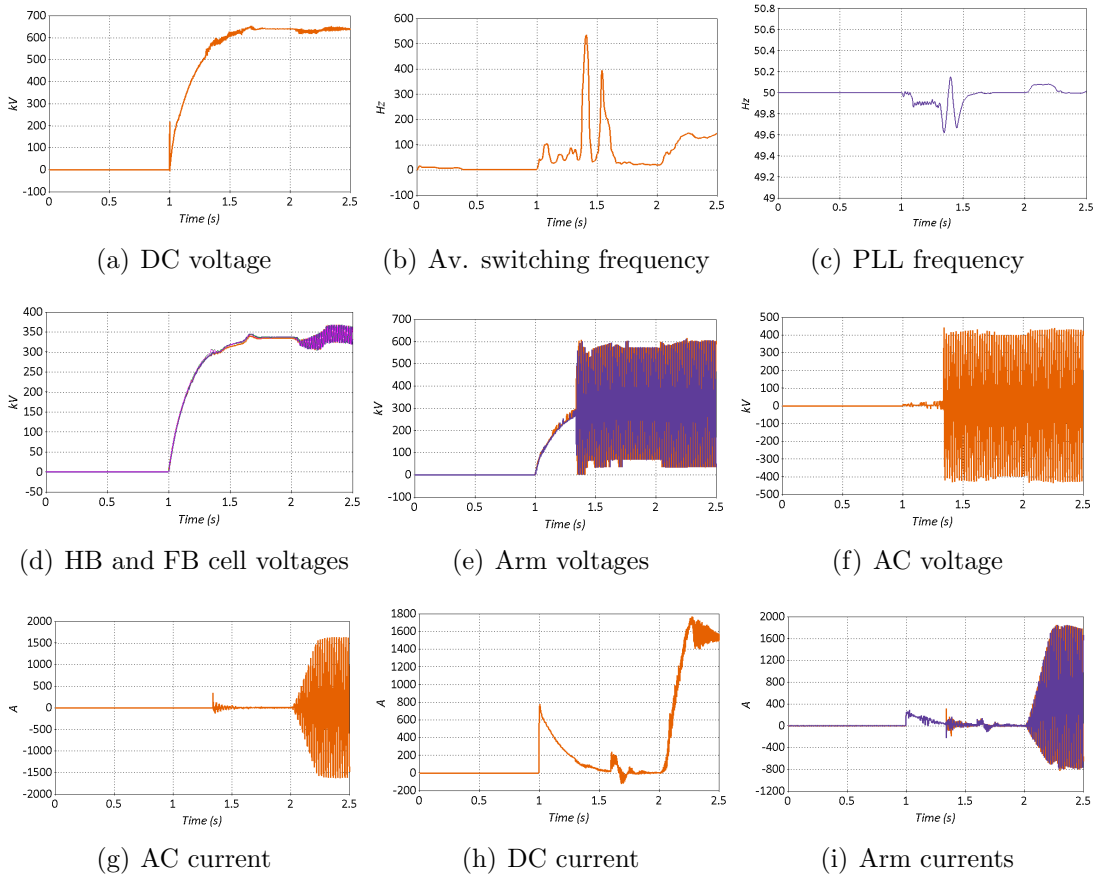
(d) PLL frequency (e) HB and FB cell voltages (f) AC voltage

(g) DC voltage (h) Arm voltages (i) Av. switching frequency

Figure 5.6: MC-MMC station 1 charging sequence.

the temperature of the IGBTs, and secondly any rapid increase of the cell voltage will trigger second stage inrush currents in the capacitors, as illustrated in the AC currents of Fig. 5.6(a) and the arm currents of Fig. 5.6(b). Although these voltage and current transients can be tolerated by the converter, the switching operation may cause undesirable semiconductor stresses. This may be avoided by increasing the slope of the DC voltage reference ramp, and tuning the DC controller to give increased settling time.

At $t = 1$ s, where nominal DC voltage is achieved, the MMC station 2 DC-D closes. As a result a high inrush current will flow through the DC link which will charge the MMC2 cells from the DC side. The DC inrush current will be limited by the MMC station 2 DC-R. Due to the high rate of change of current, a voltage drop occurs in the DC link; hence, the converter switching frequency momentarily increases, as shown in Fig. 5.6(i). Furthermore, when the DC voltage achieves its nominal value, the MMC station 2 DC-D closes allowing MMC2 to connect to the DC network.



(a) DC voltage (b) Av. switching frequency (c) PLL frequency

(d) HB and FB cell voltages (e) Arm voltages (f) AC voltage

(g) AC current (h) DC current (i) Arm currents

Figure 5.7: MC-MMC station 2 charging sequence.

The DC-side charging procedure commences, as shown in Fig. 5.7, and the uncontrolled charging period of MMC2 starts, as shown in Fig. 5.7(a). Just after $t = =1$ s, MMC1 switching frequency reduces, as the average capacitor voltage is within its tolerance band and the CBA is no longer saturated, as shown in Fig. 5.7(b) in the interval $1 < t < 1.4$ s. At $t = 1.3$ s the ACCB of MMC 2 closes enabling synchronisation of the converter with the AC grid, which leads to a high rate of change of frequency, seen at $t = =1.5$ s in Fig. 5.7(c), which may be detected by external relays. Meanwhile the MMC 2 cell capacitors charge, shown in Fig. 5.7(d), but do not achieve their nominal voltage due to the voltage drop across the DC insertion resistors, DC-R. Cells in MMC 2 are unblocked during the whole charging process in order to avoid any insertion/bypass transients.

The effect on the arm voltages of connection to the AC grid can be observed in Fig. 5.7(e), where at that moment the converter controller takes its reference from the AC grid, shown in Fig. 5.7(f), and regulates the arm voltage according to the AC voltage. Again due to the AC-R, the AC current is limited as shown in

Fig. 5.7(g). The AC-R are disconnected at $t = 1.5$ s, affecting only the switching frequency of MMC 2 due to fast internal relocation of the converter currents.

At $t = 1.6$ s the DC-R are disconnected, leading to a mild DC current overshoot due to the sudden DC voltage increase, shown in 5.7(h). At that point, DC network impedance returns to its nominal value, enabling the controllers to operate normally and to remove DC and cell capacitor voltage oscillations, as shown in Figs. 5.7(d) and 5.6(e). At this stage the switching frequencies of both converters are increased in order to readjust the rapid change of voltage. At $t = 1.8$ s the cell capacitor voltages in both converters are at their nominal values, DC voltage is set without any undesirable oscillation, and all residual currents are zero. As a result, at $t = 2$ s the power reference is now set to its nominal value, and at $t = 2.4$ s the AC and DC voltages and currents in both converters operate at their desired values. It should be noted that the capacitor voltages in both HB and FB cells charge simultaneously, while the total steady-state capacitor voltage in each arm is half of V_{DC} (approximately 320 kV) as the MC-MMC arm consists of equal numbers of HB and FB cells. The start-up sequences for the rest of the MMC variants (HB, FB) are alike when identical timings are used.

5.3.2 AAC

The following start-up sequence is proposed for the AAC is described by Fig. 5.8. The ACCB is closed at $t = 0.05$ s and, similar to the MMC, the AAC 1 is connected to the AC grid with the AC-R active. AAC 2 is completely isolated from the DC network through the DC-D. The converter operates in uncontrolled charging mode until the DC voltage is equal to the AC RMS line-to-line voltage, as shown in Figs. 5.9(a) and 5.9(b). However due to the fact that in AAC, the chain-link voltage rating is chosen to support only a portion of the DC voltage, shown in Fig. 5.9(c), the capacitor voltages are charged to this voltage. This is shown in Fig. 5.9(a) where the DC voltage reaches 500 kV at approximately $t = 0.5$ s, while the capacitor voltages have a similar profile but the voltage magnitude is less, as shown in Fig. 5.9(d). At $t = 0.65$ s the AC-R are disconnected, resulting in mild inrush current, shown in Figs. 5.9(e) and 5.9(f). At $t = 0.85$ s the DC voltage starts to ramp up to its nominal value, which is reached at $t = 1$ s. Additionally, at $t = 1$ s the DC-R are disconnected.

Additionally at the beginning of the uncontrolled charging sequence, the current phase may shift significantly due to the inrush currents resulting from the series cell capacitors. This leads to a mismatch between the calculated overlap time for the DS and the time required for the stored energy in the arm inductors to be exchanged between the upper and the lower converter arms. Due to the en-

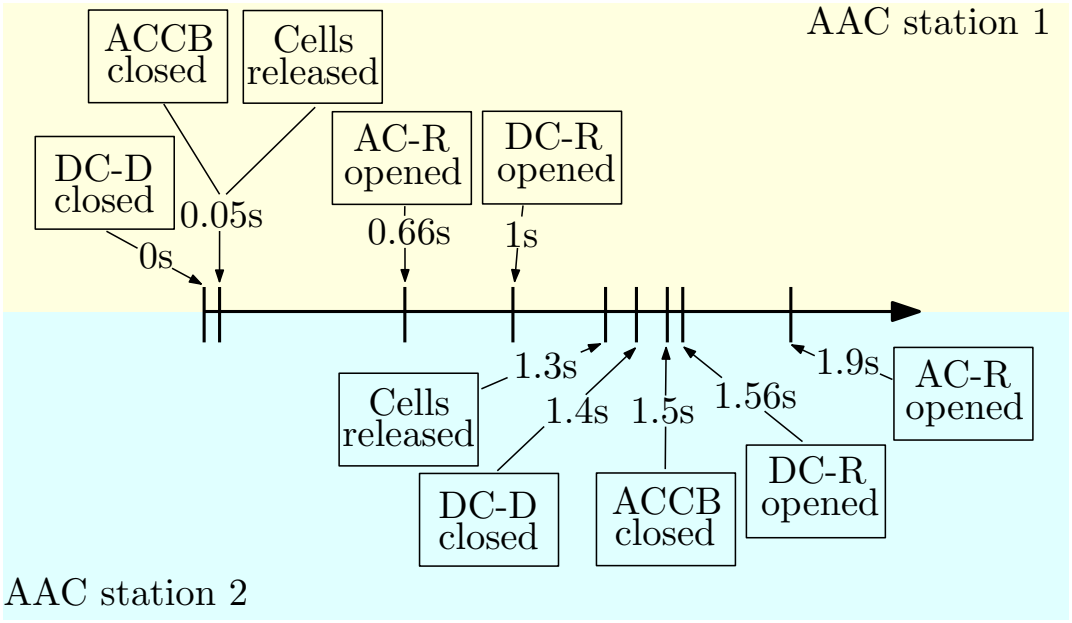
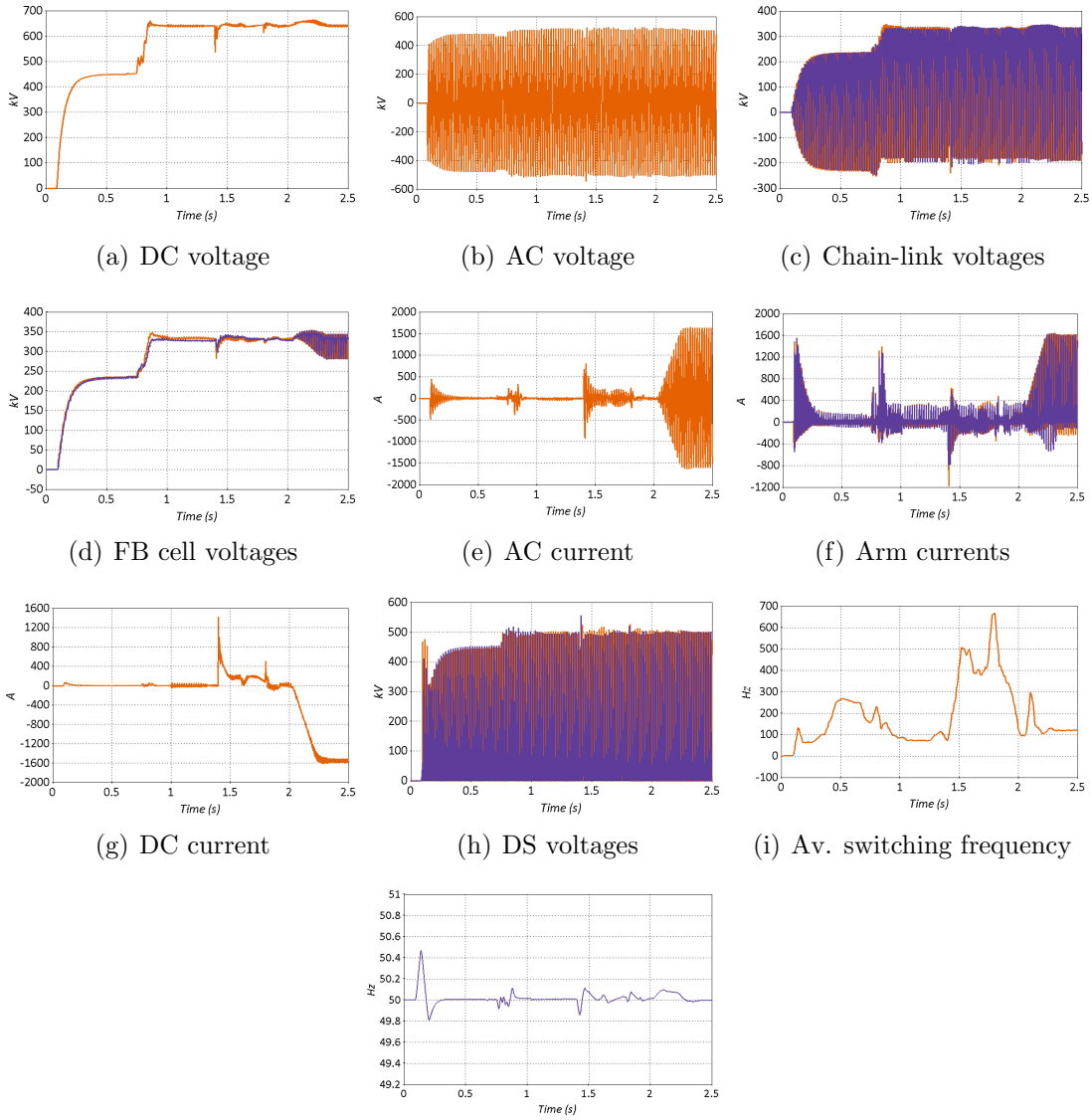


Figure 5.8: AAC start-up sequence timings.

ergy stored in these inductors, high overvoltage occurs during DS overlap, shown in Fig. 5.9(h). Two solutions to this issue are applied. Firstly, an appropriately sized RC snubber is employed for the DS, which absorbs the fast energy exchange from the arm inductors. Secondly, a surge arrester is employed across the DS, for protection against overvoltages during IGBT commutation when the current is high. As the AAC cm current profile is different to that for an MMC, overcurrent or overvoltage must be limited at valve level. Throughout the charging process of AAC1 the short duration and limited deviation in switching frequency before achieving its final value, shown in Fig. 5.9(i), will not significantly thermally stress the semiconductors. With regard to AAC station 2, the DC-D closes at t = 1.4 s with the DC-R employed and the ACCB open, whilst the cells are enabled at t = 1.3 s. Due to the sudden connection of the DC voltage to AAC2, shown in Fig. 5.10(a), a high inrush DC current appears but does not exceed the nominal value, as shown in Fig. 5.10(b). At t = 1.5 s the ACCB of AAC station 2 closes, enabling converter synchronisation with the AC grid, shown in 5.10(c). A small AC inrush current flows and is limited by the AC-R as illustrated in Fig. 5.10(d). At this point, the chain-link and DS voltage controllers take their references from the AC voltages and the current controller is fully operational, as shown in Figs. 5.10(e) and 5.10(f). Due to the inrush current, the capacitor voltages are rearranged through the capacitor balancing algorithm leading to the increased switching frequency observed in Fig. 5.10(g). At t = 1.8 s the DC-R



(a) DC voltage (b) AC voltage (c) Chain-link voltages

(d) FB cell voltages (e) AC current (f) Arm currents

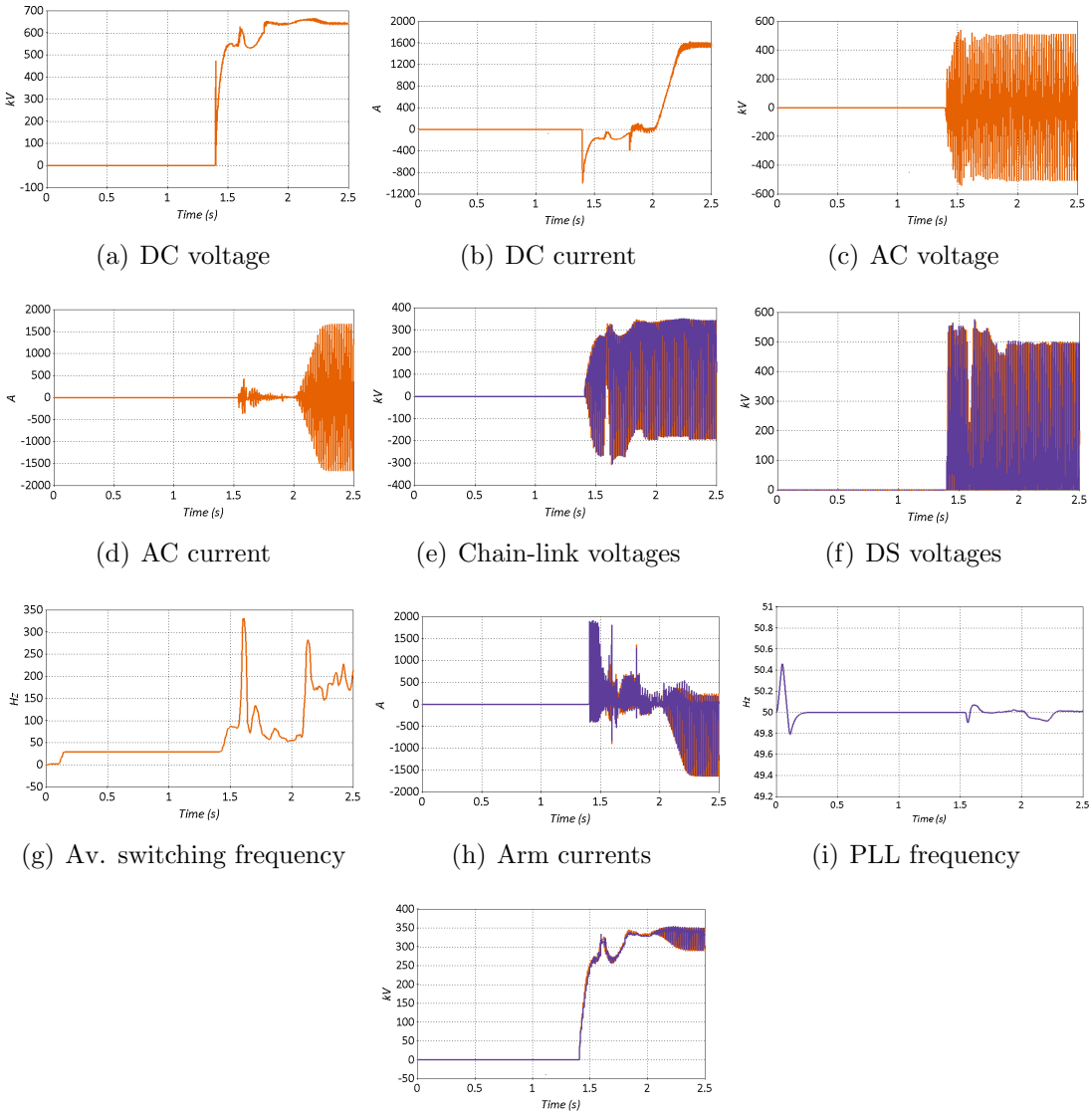
(g) DC current (h) DS voltages (i) Av. switching frequency

(j) PLL frequency

Figure 5.9: AAC station 1 charging sequence.

are bypassed resulting in further inrush current due to the resulting voltage increase, as illustrated by the arm currents in Fig. 5.10(h). Lastly the AC-R are disconnected at $t = 1.9$ s without any noticeable effect as the controller operates as required and the voltages are at their nominal values. The converter increases power to its nominal value at $t = 2$ s, with a natural under-voltage on the DC link and a disturbance in the PLL frequencies as shown in Fig. 5.10(i). The capacitor voltages are fully balanced around the desired value, shown in Fig. 5.10(j).

In conclusion, the AAC has a slightly different start-up sequence when compared to the MMC. The appearance of overcurrent in the arms during overlap



(a) DC voltage (b) DC current (c) AC voltage

(d) AC current (e) Chain-link voltages (f) DS voltages

(g) Av. switching frequency (h) Arm currents (i) PLL frequency

(j) FB cell voltages

Figure 5.10: AAC station 2 charging sequence.

periods make necessary the employment of the DC-R even during the AC charge-up sequence. As a result a smooth start-up sequence is achieved for the AAC.

5.4 DC pole-to-pole fault

This section presents a simulation study for a DC pole-to-pole fault at the middle of the DC cables (70 km from each converter). The case study will demonstrate the DC fault reverse blocking and controlled recovery capabilities of the MMC and AAC as they act to protect the symmetrical monopole DC link, whilst keeping

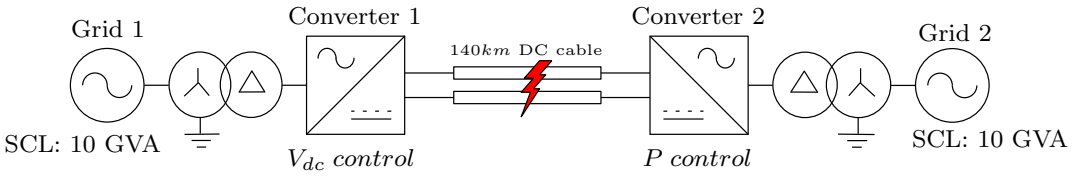


Figure 5.11: Test network for DC pole-to-pole fault.

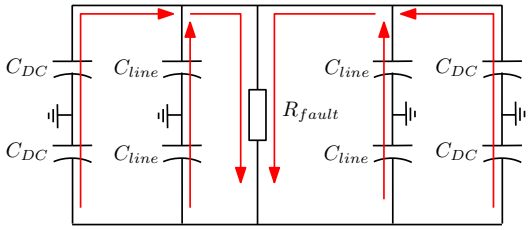


Figure 5.12: DC fault stage one. DC filter and line capacitance discharge.

the current and voltage stresses on the converter stations within tolerable limits. The DC link of Fig. 5.11 is subjected to an illustrative temporary pole-to-pole DC fault with 5ms duration at $t = 1$ s.

5.4.1 DC pole-to-pole fault analysis

The DC pole-to-pole fault can be characterised in three stages for any multilevel converter. The first stage is illustrated in Fig. 5.12 and can be described as a capacitor (DC filter) discharge. During this stage, the line and DC capacitances are discharged in the short-circuit connection between the two poles. The line capacitance value is dependent on the type of the line (i.e. overhead lines or underground cables) while the DC filter capacitance depends on the type on the converter. An AAC converter may have increased DC capacitance, while in MMC the DC capacitance exists mainly to provide a ground reference for measurement purposes. The fault current is given by

$$I_{DC_{fault}} = C_{DC_{eq}} \frac{dV_{DC}}{dt} \tag{5.1}$$

This can be rearranged as (5.2) which shows that the rate of change of the DC voltage $\frac{dV_{DC}}{dt}$ is dependent upon the fault resistance R_{fault} and the installed capacitance on the DC side $C_{DC_{eq}} = C_{DC} + C_{line}$.

$$\frac{dV_{DC}}{dt} = \frac{V_{DC}}{-R_{fault} \cdot C_{DC_{eq}}} \tag{5.2}$$

The second stage can be described as cell capacitor discharge through the fault, illustrated in Fig. 5.13. As soon as the DC voltage is lower than the cm voltage the fault current starts to circulate through the converter arms. As a result the arm cell capacitors discharge into the fault, whilst the 'block' command has not yet been issued by the control system. Furthermore, due to the DC voltage collapse, the AC side of the converter feeds the fault with high currents through the converter arms. Hence, even if the converter is able to execute the switching patterns through the IGBTs, the controllability of the converter has been lost, resulting in uncontrollable DC voltage, and active and reactive power. During normal operation, approximately 50% of the cells are inserted, hence N cells (equivalent to one arm) contribute to the fault. The equivalent arm phase capacitance for the MMC $C_{MMC_{eq}}$ is

$$C_{MMC_{eq}} = \frac{C_{cell}}{N} \tag{5.3}$$

with each phase contributing to the fault current as follows:

$$i_{fault-j} = -\frac{C_{cell}}{N}\frac{d(v_{j,u} - v_{j,l})}{dt} \tag{5.4}$$

During the third and final fault stage, shown in Fig. 5.14, a protection signal is enabled which allows the cells to block the fault current.

The converters then operate as uncontrolled diode-rectifiers. A new steady-state operating point is achieved, with the arm voltages collapsed whilst the AC side contributes to the fault. At this stage the maximum DC fault current is calculated as:

$$I_{DC_{fault}} = \frac{3}{2} \cdot \frac{v_j}{L_{AC} + \frac{L_{arm}}{2}} \tag{5.5}$$

When the converter blocks the DC fault current, the equivalent circuit is as shown in Fig. 5.15.

The DC mid-point of the converter is isolated from the AC side through high impedance grounding. As a result the DC fault current does not have a direct path to the AC side.

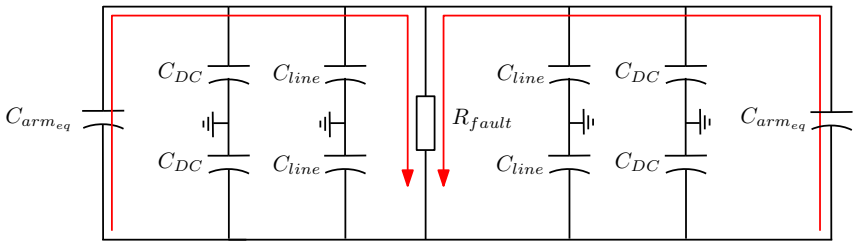


Figure 5.13: DC fault stage two. Arm capacitors discharge.

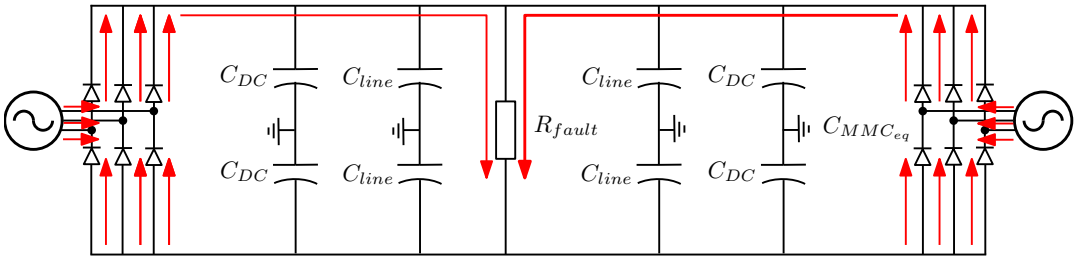


Figure 5.14: DC fault stage three. AC feed through diode rectifier.

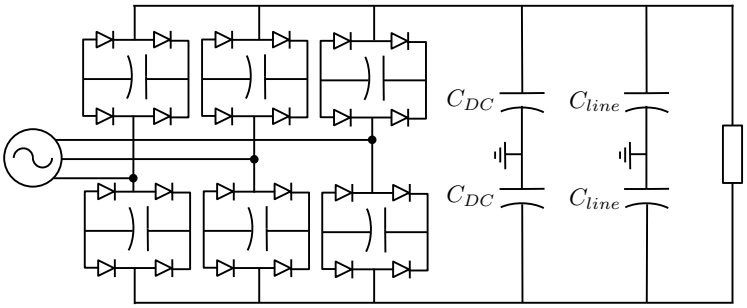


Figure 5.15: DC fault stage three, DC fault blocking.

5.4.2 MMC

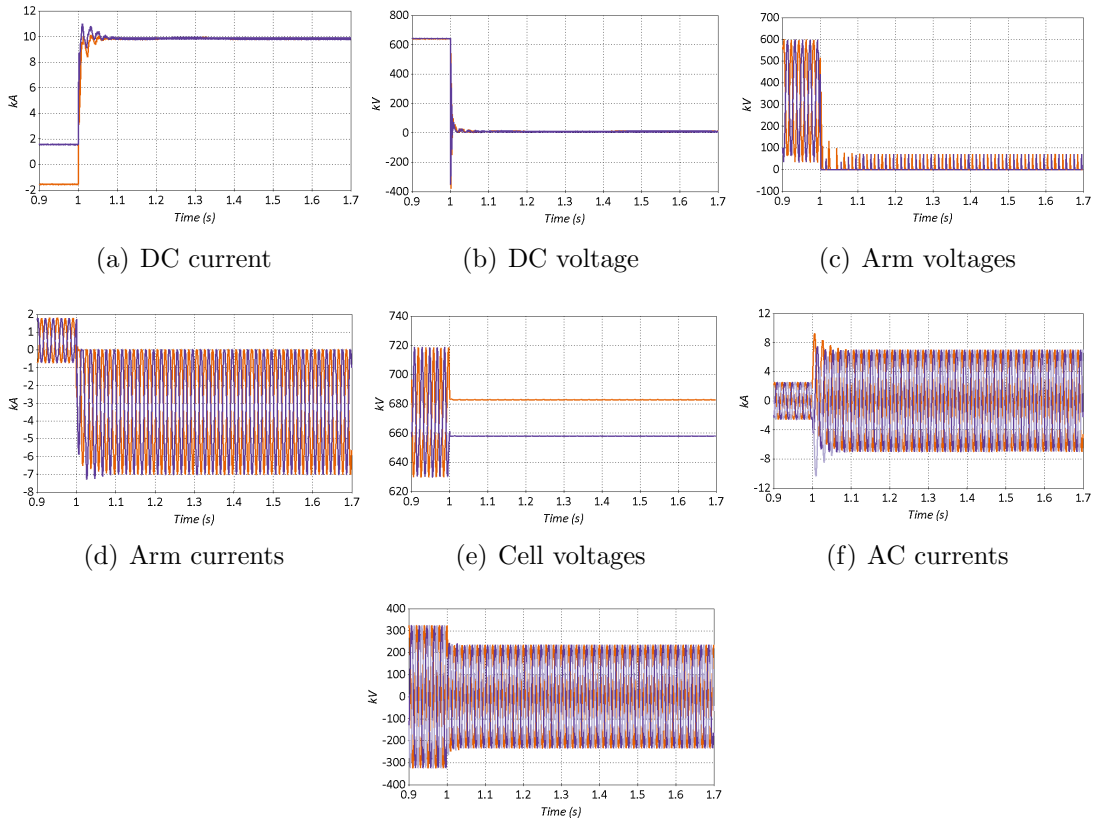
This section focuses on the DC pole-to-pole fault blocking performance of MMC. This is illustrated through detailed examination of the HB, MC and FB MMC variants.

HB-MMC

The structure of HB-MMC means that it offers no DC fault blocking capability. Fig. 5.16 shows HB-MMC operation during a DC pole-to-pole fault. As it can be observed, the moment that the fault occurs at $t = 1$ s, the DC current in Fig. 5.16(a) increases rapidly due to stage one and two capacitor discharge, while the DC and arm voltages collapses as shown in Figs. 5.16(b) and 5.16(c). The fault is detected through the arm currents, shown in Fig. 5.16(d), and the converter is blocked and operates similar to a diode rectifier, maintaining the constant cell capacitor voltage, as shown in Fig. 5.16(e). In order to protect the diodes during stage three of the DC fault, the thyristors which are connected across each cell to provide protection are activated to conduct the high-magnitude DC current. The DC current is sustained in a high value through the AC currents feed, as shown in Fig. 5.16(f). In reality the ACCB will operate after 3 cycles in order to prevent the AC current from feeding into the DC fault.

MC-MMC

In the case of an MC-MMC the converters detect overcurrent through arm current measurement and enable the 'block' command in order to switch off all the semiconductors in the converter cells. The arm voltages provide the required reverse voltage to block the DC fault, as shown in Fig. 5.17(a). At the instant the DC fault occurs, the current rises approximately to 3.5 p.u., shown in Fig. 5.17(e), whilst the DC voltage collapses to zero, as shown in Figs. 5.17(b). The capacitor voltages are locked in the blocked state, with minimum decay through parallel-connected bleed resistors, shown in 5.17(c). The arm currents shown in Fig. 5.17(d) experience a fault current which is within the limits of what can be tolerated by the IGBTs. After a time interval of 100 ms, the converter attempts to recommence operation by detecting whether or not the fault has been cleared. The method of detecting whether or not the fault is permanent is by operating the FB cell as an HB cell (Fig. 5.3(c)) as is also done during the start-up sequence. By employing this method, the DC current and voltage are measured.



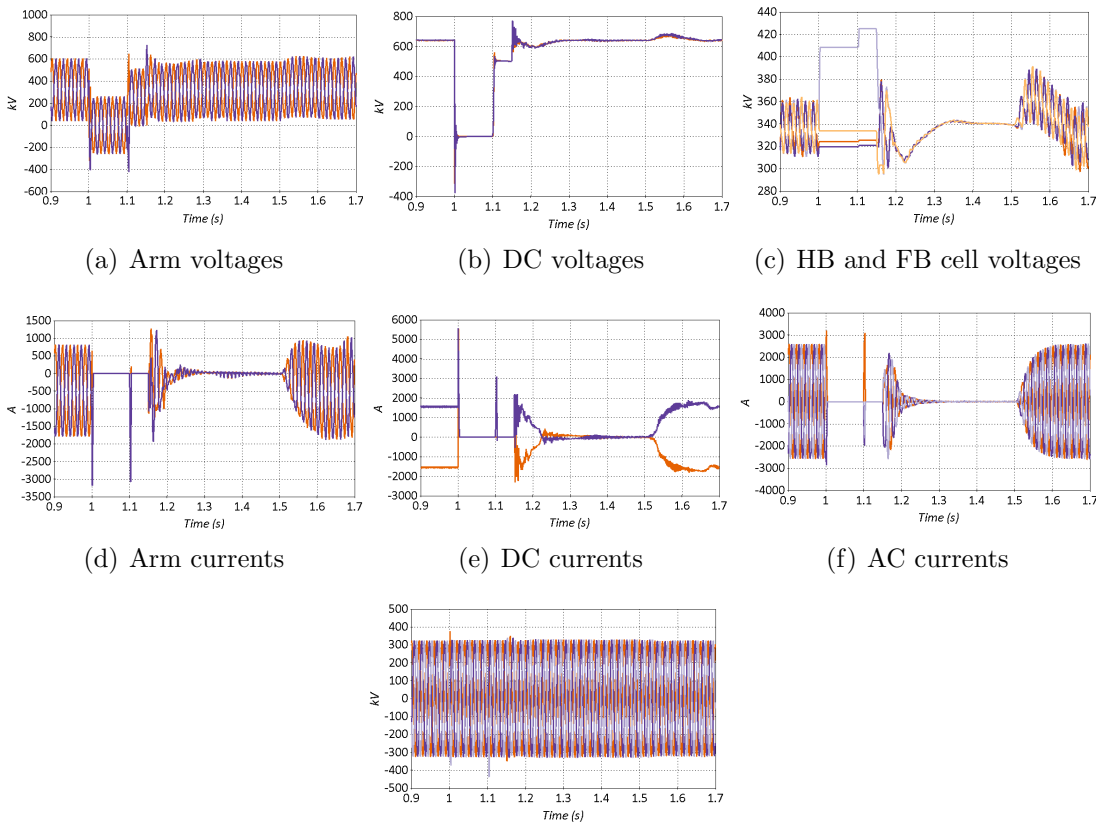
(a) DC current (b) DC voltage (c) Arm voltages

(d) Arm currents (e) Cell voltages (f) AC currents

(g) AC voltages

Figure 5.16: HB-MMC during a DC pole-to-pole fault.

During temporary unblocking of the cells, if DC current increases whilst the DC



(a) Arm voltages (b) DC voltages (c) HB and FB cell voltages

(d) Arm currents (e) DC currents (f) AC currents

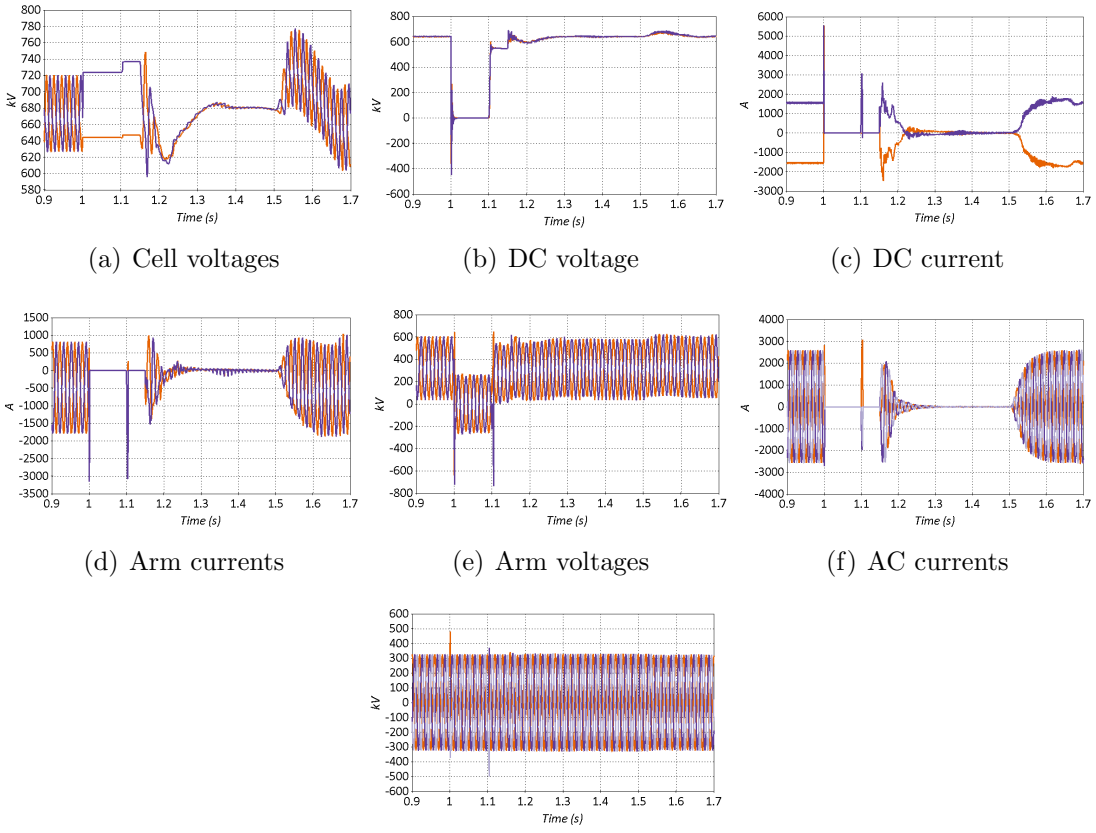
(g) AC voltages

Figure 5.17: MC-MMC during a DC pole-to-pole fault.

voltage remains below 0.1 p.u. then this indicates that the DC fault still exists. However a DC voltage increase indicates that the fault is cleared and it is safe to recommence converter operation. An arbitrary check at $t = 1.1$ s shows that DC voltage has reached 80% of its nominal value, as depicted in Fig. 5.17(b), and that the fault is cleared. Inrush current can be observed in the currents shown in Figs. 5.17(d) and 5.17(f). After a time delay of 50 ms, the converter cells are fully unblocked, and the DC link assumes its nominal voltage. A high inrush current flows to charge the capacitors back to the nominal voltage. Following this, the DC and capacitor voltages are correctly set. As a result, at $t = 1.5$ s the controller begins to ramp power, meaning that the time between the fault and recommencement of full operation is less than 1 s. This simulation shows that MC-MMC is capable of DC fault blocking and can recover normal operation whilst the AC voltage is not affected as shown in Fig. 5.17(g).

FB-MMC

Fig. 5.18 illustrates the DC pole-to-pole fault performance of an FB-MMC, and shows that it is very similar to that of an MC-MMC. The main difference between these two MMC variants is the stress that the cell capacitors experience. In the MC-MMC the HB cells are blocked at a constant voltage, as shown in Fig. 5.17(c). However, in extreme cases such as rectifier mode, the FB cells are 'locked' at a new higher voltage. The worst case overvoltage happens during rectifier mode, as shown in Fig. 5.17. The overvoltage is increased by increasing the blocking delay in both stations. However, the cell IGBTs can withstand this overvoltage as they are operated well within their ratings. With the FB-MMC, the cell capacitor voltage overshoot is smaller, as shown in Fig. 5.18(a), as there are more cells to absorb the fault faster. As with the MC-MMC system described previously, fault status is checked at $t = 1.1$ s. During this process the capacitors overcharge slightly, illustrated by the cell capacitor voltage increase shown in Fig. 5.18(a).



(a) Cell voltages (b) DC voltage (c) DC current

(d) Arm currents (e) Arm voltages (f) AC currents

(g) AC voltages

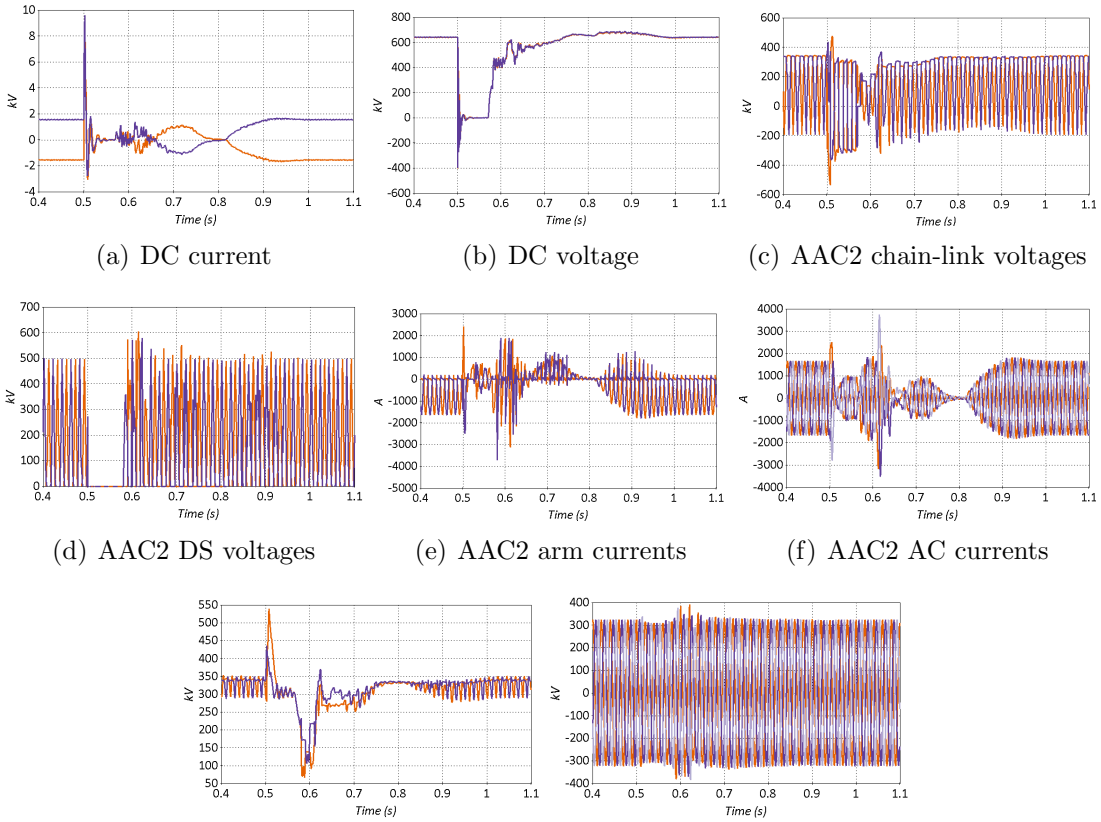
Figure 5.18: FB-MMC during a DC pole-to-pole fault.

5.4.3 AAC

This section focuses on the DC pole-to-pole fault block performance of an AAC, shown in Fig. 5.19. The AAC detects the fault current through an overcurrent measurement. AAC fault current is higher than that of an MMC due to the discharge of the DC capacitor filter and the reduced combined inductance installed in the arms and the DC filter. DC fault current therefore reaches 15 p.u., as shown in Fig. 5.19(a). At the same instant, the DC voltage collapses, as shown in Fig. 5.19(b). The blocking command is issued to the chain-link, and the DS are commanded to remain in the constantly conducting state, as illustrated by the DS voltages in Figs. 5.19(c) and 5.19(d) which drop to zero. The reverse DC voltage across the chain-link is sufficient to block the DC link and therefore to block the fault. At $t = 0.51$ s, the fault is cleared and the converter enters into STATCOM mode, where AC current is supported as shown in Figs. 5.19(e) and 5.19(f). At $t = 0.55$ s the converter attempts to re-energise the DC link, as illustrated in Fig. 5.19(b). At approximately $t = 0.76$ s the DC voltage is settled at its nominal value, and at $t = 0.8$ s the power is ramping towards to its nominal value. The small DC voltage perturbation observed beyond $t = 0.8$ s is due to the power ramp. The cell capacitors experience an overvoltage when the converter transits to STATCOM operation and an undervoltage when restart operation is attempted, as shown in Fig. 5.19(g).

5.4.4 MC-MMC fault current control capability for reduction of DCCB requirements.

In previous cases the blocking functionality of various converter topologies during a DC pole-to-pole fault was illustrated. Even if it is possible and feasible to use these converters to isolate and clear DC faults, it is not the best solution for meshed grids due to the inherent interruption of power flow. As a result, DC circuit breakers (DCCB) are considered to be a more promising solution for isolating faulted sections of a network. However, state-of-the-art DCCB technology does not allow a cost-efficient solution as the cost and the size of such DC breakers are similar to those for one converter station [43]. Moreover, the speed of interrupting DC currents is limited regardless the DCCB technology. Additionally, a DCCB station has to be upgraded whenever the DC grid is expanded, as the DC current fault levels increase according to the energy stored in the converters and lines. A solution to delay the rise in fault current is to install high value DC inductors. However, to introduce an effective time delay requires excessively large inductors, which are impractical and which may also interfere with control



(a) DC current (b) DC voltage (c) AAC2 chain-link voltages

(d) AAC2 DS voltages (e) AAC2 arm currents (f) AAC2 AC currents

(g) AAC2 cell voltages (h) AAC2 AC voltages

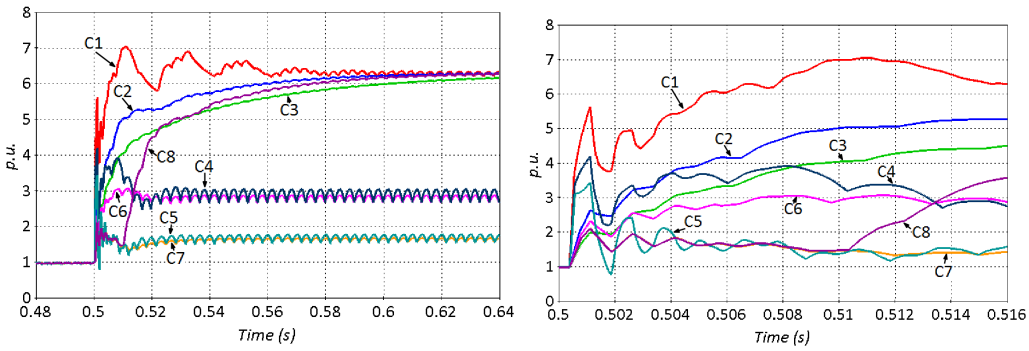
Figure 5.19: AAC during a DC pole-to-pole fault.
This simulation shows that AAC is capable of DC fault blocking and can recover normal operation whilst the AC voltage is not affected as shown in Fig. 5.19(h).

system dynamics, as mentioned in Chapter 2.

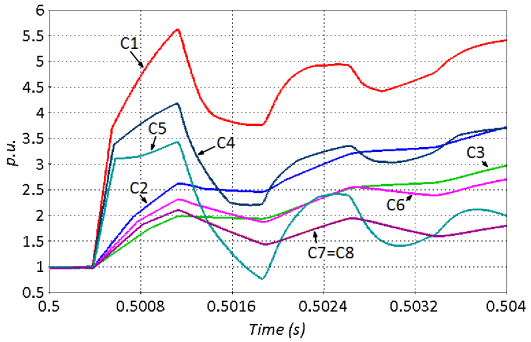
A proposed solution therefore is to control the fault current trajectory through the application of a reverse polarity voltage, achieved by appropriate connection of a few FB cells in an MC-MMC. An MC-MMC with a small portion of FB cells, in the range of 15 to 25% of the total arm cells, could reverse briefly a small portion of the DC voltage and limit the fault current trajectory in such a way as to increase the time available for DCCB operation. This would be at the expense of the fault blocking capability offered by a conventional MC-MMC.

Even with the inclusion of only a small portion of FB cells (15 to 25%), many of the benefits of the MC-MMC are still available. For example, the efficiency of the converter remains high, while it benefits from a flexible modulation index which can be further exploited for expanding the P-Q capabilities for reduced DC voltage operation as shown in Chapter 4.

The following case studies compare the DC fault current profiling performance



(a) DC fault current time window 160ms (b) DC fault current time window 16ms



(c) DC fault current time window 4ms

Figure 5.20: DC fault current analysis based on the cases detailed in Table 5.1.

of the proposed MC-MMC arrangement with that of an HB-MMC. The investigation also considers different proportions of FB cells in the MC-MMC and the inclusion of relative high value of DC inductors. A case study is also included to illustrate the internal protection of the FB cells in MC-MMC. The specific set of illustrative studies is detailed in Table 5.1. Fig. 5.20 shows the results of the eight case studies of Table 5.1. for a variety of time windows. Cases C2 and C3 show that the inclusion of DC inductance reduces the initial current overshoot.

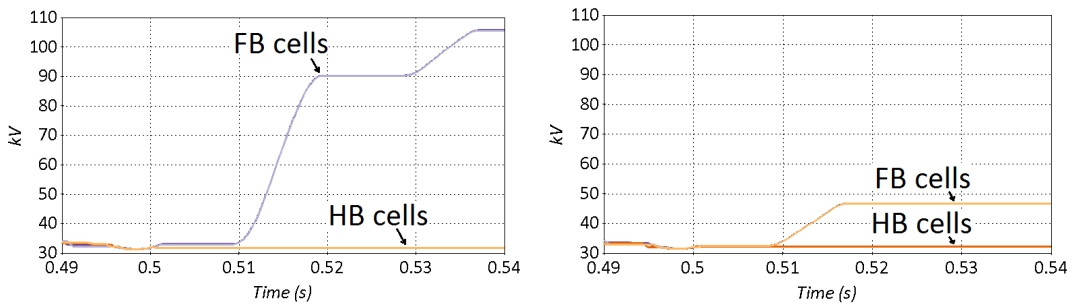
Table 5.1: Cases for DC fault current trajectory.

Case study	Description
C1	HB-MMC
C2	HB-MMC with 100mH DC inductances
C3	HB-MMC with 200mH DC inductances
C4	MC-MMC with 15% FB cells
C5	MC-MMC with 25% FB cells
C6	MC-MMC with 15% FB cells and 100mH DC inductances
C7	MC-MMC with 25% FB cells and 100mH DC inductances
C8	C7 with enabling cell Thyristors

However, the fault currents for cases C4 and C5 increase to values of 4 and 4.2 p.u. respectively within 1ms of fault initiation, as shown in Figs. 5.20(b) and 5.20(b). This is insufficient time for successful DCCB operation and would result in system breakdown. Cases C4 and C5 for the proposed MC-MMC with 15% and 25% FB cells, shows a high initial current overshoot. This indicates that, on its own, the proposed MC-MMC method does not offer advantage over the method that uses DC reactors during the initial development of the DC fault. Cases C6 and C7 combine the MC-MMC and DC reactor approaches. Cases C6 and C7 with 15% and 25% FB cells respectively, and 100 mH inductance shows significant fault current overshoot. However Case C7 with 25% FB cells and 100mH inductance shows the DC fault current is significantly reduced, having an amplitude of only 1.5p.u. 5ms after fault initiation. In both cases C6 and C7, DC fault current rate of change and magnitude is significantly reduced.

- C2 and C3, initial overshoot suppression, later full development of DC fault current.
- C4 and C5, has increased initial overshoot and reduced DC fault current development.
- C6 and C7 have reduced initial overshoot and reduced DC fault current development.

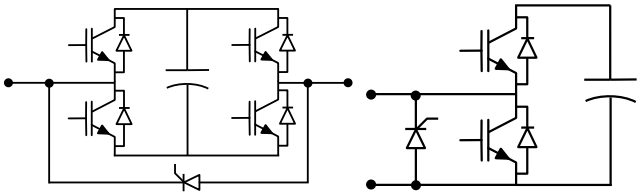
In the proposed MC-MMC topology the full DC voltage must be supported by the small number (15%-25%) FB cells. The effects of this are presented in Fig. 5.21. As the fault current continues to flow, the FB cell capacitors continue to charge, leading to voltage increase and potential insulation damage, as show in Fig. 5.21(a). To protect the FB cells from overcharging a thyristor can be used



(a) Cell voltages without bypassing

(b) Cell voltages with bypassing

Figure 5.21: The effect of constant implementation of FB cells into DC fault and bypassing.



(a) FB cell (b) HB cell

Figure 5.22: Cell topologies with bypass thyristors.

to bypass the cell when cell capacitor voltage exceeds a predetermined threshold, as shown in Fig. 5.22(a). This arrangement is commonly seen in FB cells, as shown in Fig. 5.22(a). The effect of this protection mechanism on the converter is shown in Fig. 5.21(b), which illustrates the significant reduction in voltage across the FB cells. The external consequence, i.e. the effect on DC fault current profile, is shown in case C8 in Fig. 5.20. In case C8, which is the same as case C7 but incorporating the thyristor protection strategy, fault current remains at 1 p.u. for approximately 11.5 ms following fault initiation. At approximately 11.5 ms the cell voltage reaches the threshold required to trigger the Thyristor protection mechanism and fault current increases towards its natural final value. However the 11.5 ms prior to this is more than the double the time required for successful DCCB operation. As a result, the proposed solution of MC-MMC with a small proportion of FB cells and DC reactors relaxes the challenging design requirements for future DCCB, and therefore DCCB size and cost.

5.5 DC pole-to-ground fault

This section presents a simulation study for a DC positive pole-to-ground fault at the midpoint of the DC cables (70 km from each converter). The purpose of this study is to assess the DC pole-to-ground fault ride through (FRT) capability of the MMC and the AAC. In comparison with the DC pole-to-pole fault, the nature of the pole-to-ground fault is significantly different and poses a risk to both the transformer and the conductor insulation. The ability of each converter control action to protect the transformer whilst also maintaining current and voltages stresses on the converter stations within tolerable limits will be assessed. In the case that this protection is successful and the converters continue operating under fault, the ability of each converter to continue to transfer power during the fault will be also investigated. The system under test is illustrated in Fig. 5.23 and is subjected to a permanent pole-to-ground DC fault at $t = 1$ s.

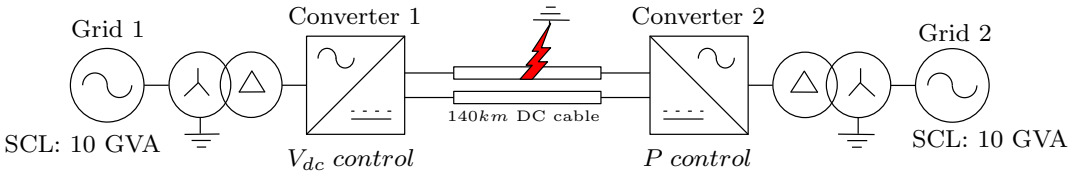


Figure 5.23: Test network for DC pole-to-ground fault.

DC pole-to-ground fault analysis

In multilevel converters, a pole-to-ground DC fault can be categorised in two stages. The first stage is illustrated in Fig. 5.24 and can be described as capacitor (DC filter) discharge. During this first stage, the line and DC capacitances are discharged in the short-circuit connection between the ground points. The second

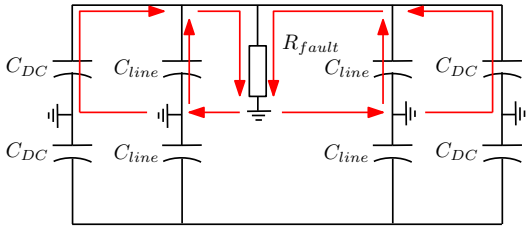


Figure 5.24: DC pole-to-ground fault stage one, DC capacitor discharge.

stage creates a short circuit connection between the grounds of the DC and AC sides, as illustrated in Fig. 5.25. This occurs regardless of the type of grounding

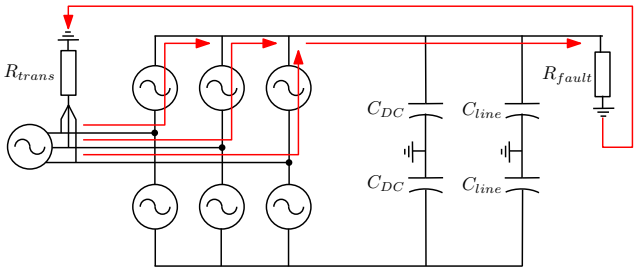


Figure 5.25: DC pole-to-ground fault stage two, permanent connection through ground points.

that is installed on the converter station transformer [93]. The steady-state fault current $I_{DC_{ptg-fault}}$ is determined by the transformer's impedance R_{trans} and the fault resistance R_{fault}.

$$I_{DC_{ptg-fault}} = 0.5\frac{V_{DC}}{R_{fault} + R_{trans}} \tag{5.6}$$

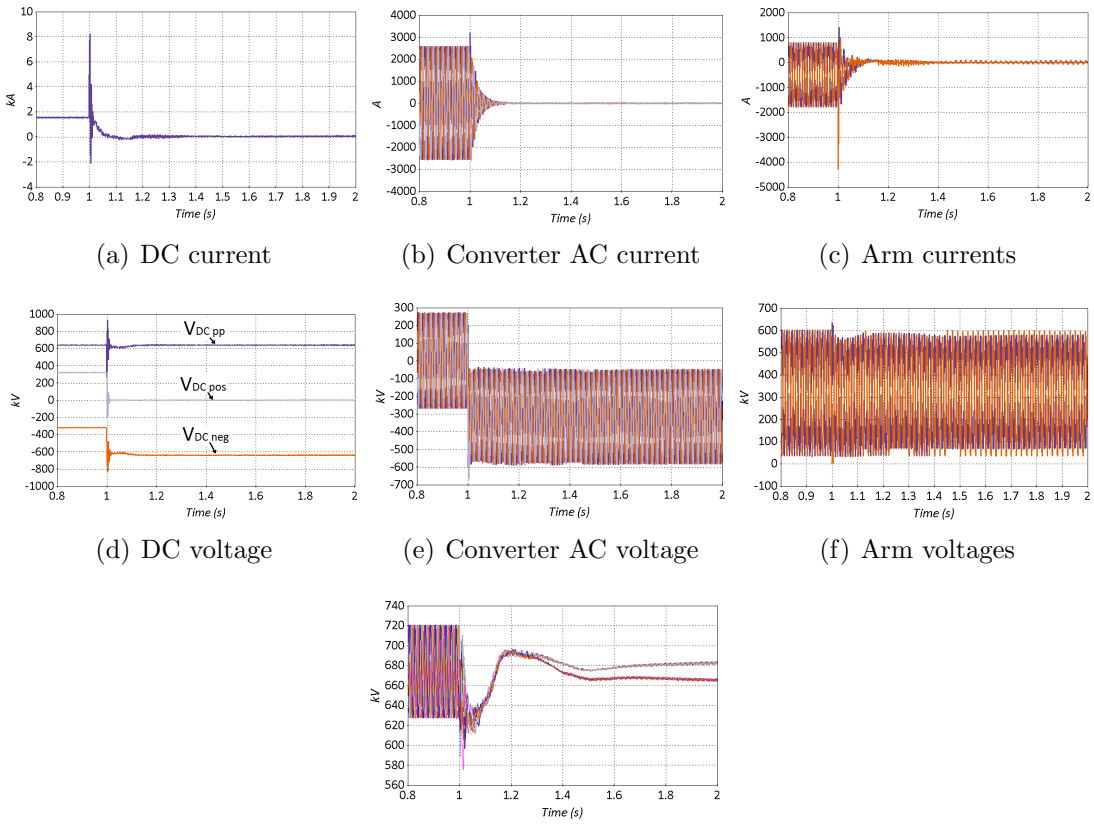
Since $R_{fault} < R_{trans}$ the voltage collapses at the faulty pole, whilst the healthy pole sustains V_{DC}.

MMC

This section focuses on the DC pole-to-ground fault FRT ability of MMC. This is illustrated through detailed examination of the HB, MC and FB MMC variants.

HB-MMC

Fig. 5.26 shows the operation of an HB-MMC which does not have any over-modulation capability to support a pole-to-ground DC fault. As shown in Fig. 5.26(a), the moment that the fault occurs at $t = 1$ s, the DC current increases rapidly and then collapses. This results in zero power transfer as shown in AC and arm currents in Figs 5.26(b) and 5.26(c) respectively. The faulty-pole voltage also collapses to zero while the healthy pole tries to sustain V_{DC}, illustrated in Fig. 5.26(d). Due to the short-circuit path between the grounded fault and the



(a) DC current (b) Converter AC current (c) Arm currents

(d) DC voltage (e) Converter AC voltage (f) Arm voltages

(g) Cell capacitor voltages

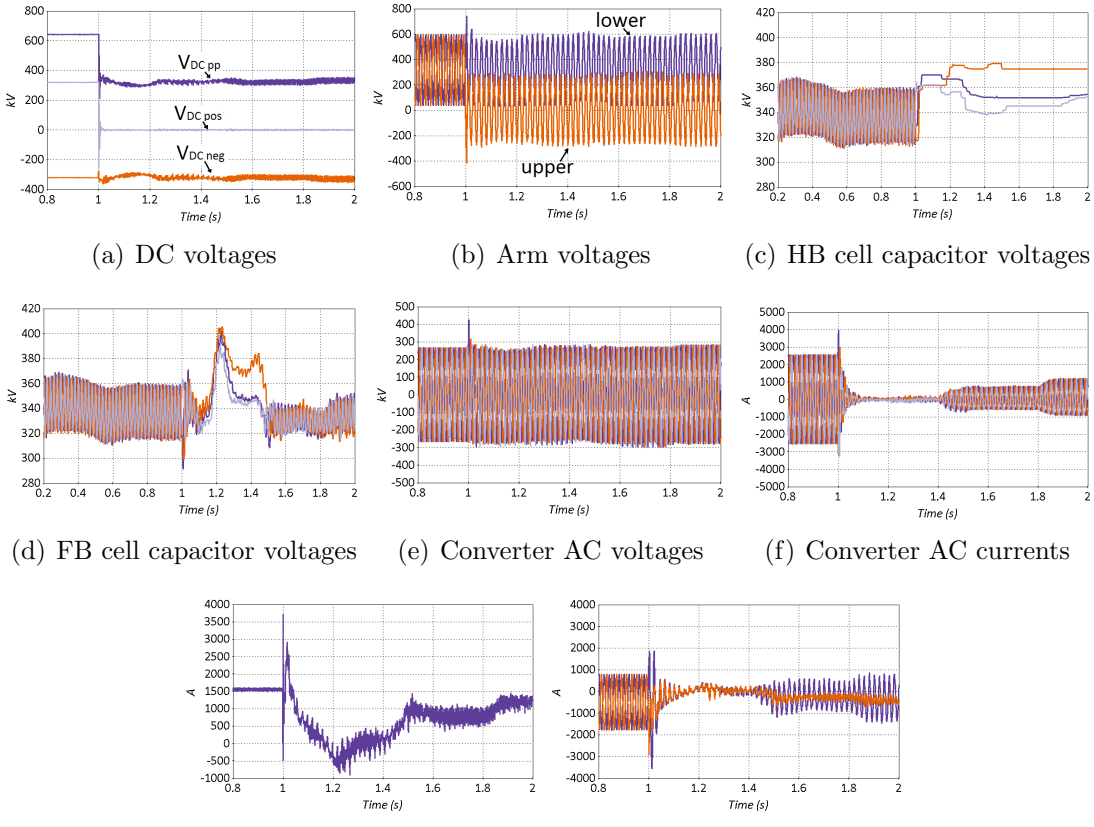
Figure 5.26: HB-MMC pole-to-ground fault.

grounding on the converter side of the transformer, as shown Fig. 5.25, the AC converter voltage shown in Fig. 5.26(e) has a DC offset which exceeds the nominal insulation breakdown voltage. During the fault the arm and cell capacitor voltages are not affected, as shown in Figs. 5.26(f) and 5.26(g) respectively.

The conventional solution for pole-to-ground faults in HB-MMC is to block the converter and interrupt the connection with the AC grid through the ACCB. Then, the fault current can be extinguished and the overvoltage can be eliminated. The converter is therefore protected but, due to its blocking action, active and reactive power flow to and from the AC grid is interrupted.

MC-MMC

Fig. 5.27 illustrates the simulation results of an MC-MMC with 50% FB and 50% HB cells. The moment that the pole-to-ground fault occurs the voltage at the faulted pole collapses to zero as can been seen in Fig. 5.27(a). At the exact same instant the DC voltage reference applied in the DC voltage controller is set to 0.5



(a) DC voltages (b) Arm voltages (c) HB cell capacitor voltages

(d) FB cell capacitor voltages (e) Converter AC voltages (f) Converter AC currents

(g) DC current (h) Arm currents

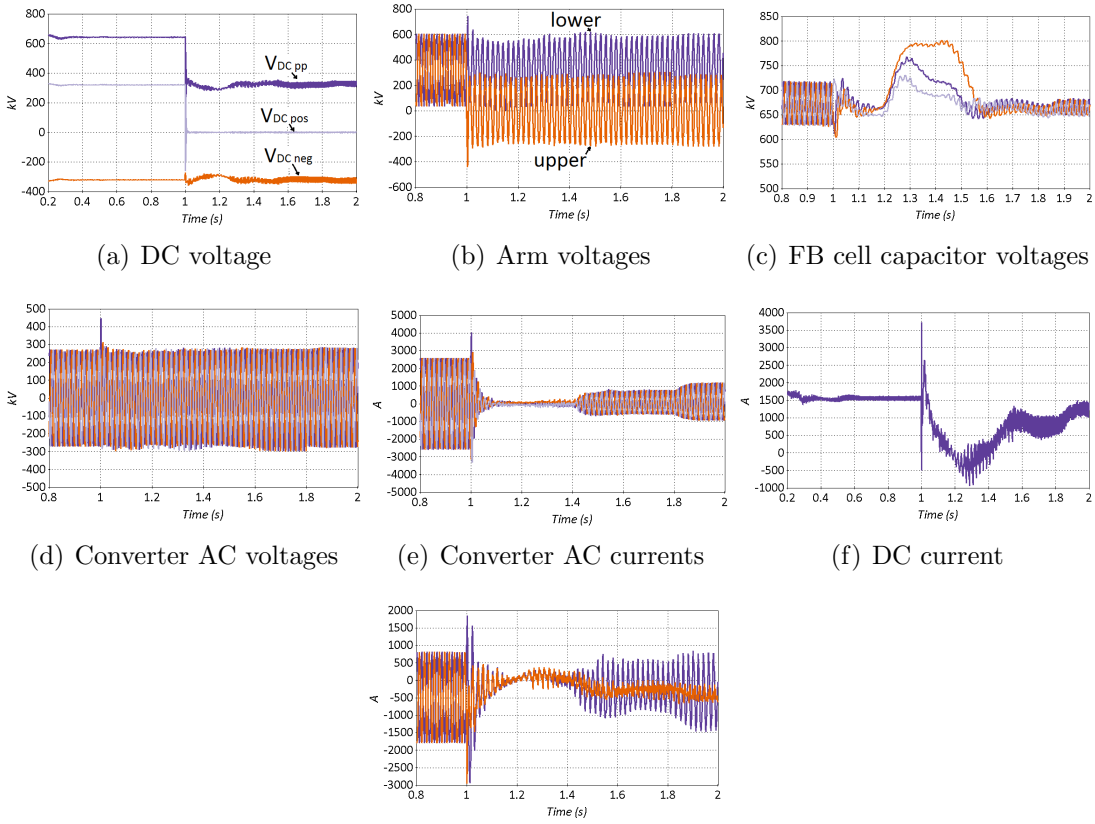
Figure 5.27: MC-MMC pole-to-ground fault.

p.u. The DC offset component of the modulation index reference, as described in Chapter 3, applied to the faulty arm also reduced by 0.5 p.u. Following this control action $\frac{V_{DC}}{2}$ is supported across both MC-MMC arms. This is illustrated in Figs. 5.27(b) where the converter arm connected to the healthy pole operates normally, i.e. as it did before the fault occurred, and the arm connected to the faulty pole produces a mixture of positive and negative voltages and is over-modulated. It is also evident from Figs. 5.27(c) and 5.27(d) that the CBA is able to distinguish between HB and FB cells and balances the capacitor voltages.

This control action protects the transformer and conductor insulation, and the converter is able to continue operating. The target of supporting the converter side AC voltage is achieved and the AC voltage spike, which is actually a DC voltage offset, is extinguished, as illustrated in Fig. 5.27(e). Because the converter continues to operate it is able to transfer power, albeit at reduced DC voltage level. To transfer the same amount of pre-fault power, the DC current has to be increased accordingly. Two power reference sets are applied at $t = 1.4$ s and $t = 1.8$ s. In both cases power is transferred in response to these demands, as shown by the AC and DC currents in Figs. 5.27(f) and 5.27(g) respectively. The amount of power that can actually be transferred is however limited by the current ratings of the cables, as illustrated in Fig 5.27(g), which shows that DC current flow is has returned to its nominal value. The current in the 'healthy' arm is increased in comparison to that in the 'faulty' arm and makes a correspondingly larger contribution to the active power, as shown in Fig. 5.27(h). The DC current and voltage have increased ripple and high frequency components. However in view of the reduced DC voltage amplitude these should not pose any risk to either insulation or thermal limits of the cables. This simulation study shows that the MC-MMC with 50% FB cells and 50% HB cells can survive a DC pole-to-ground fault whilst continuing power transfer.

FB-MMC

Simulation results for an FB-MMC subjected to a DC pole-to-ground fault are shown in Fig. 5.28. These results show that operation of the FB-MMC is very similar to that of an MC-MMC, and that it is also to survive the fault whilst continuing transfer power. Whilst it may be considered the FB-MMC could offer advantage during a fault due to its capability to generate full negative DC voltage, this attribute becomes redundant during a DC pole-to-ground fault since the DC voltage is controlled to be 0.5 p.u.



(a) DC voltage (b) Arm voltages (c) FB cell capacitor voltages

(d) Converter AC voltages (e) Converter AC currents (f) DC current

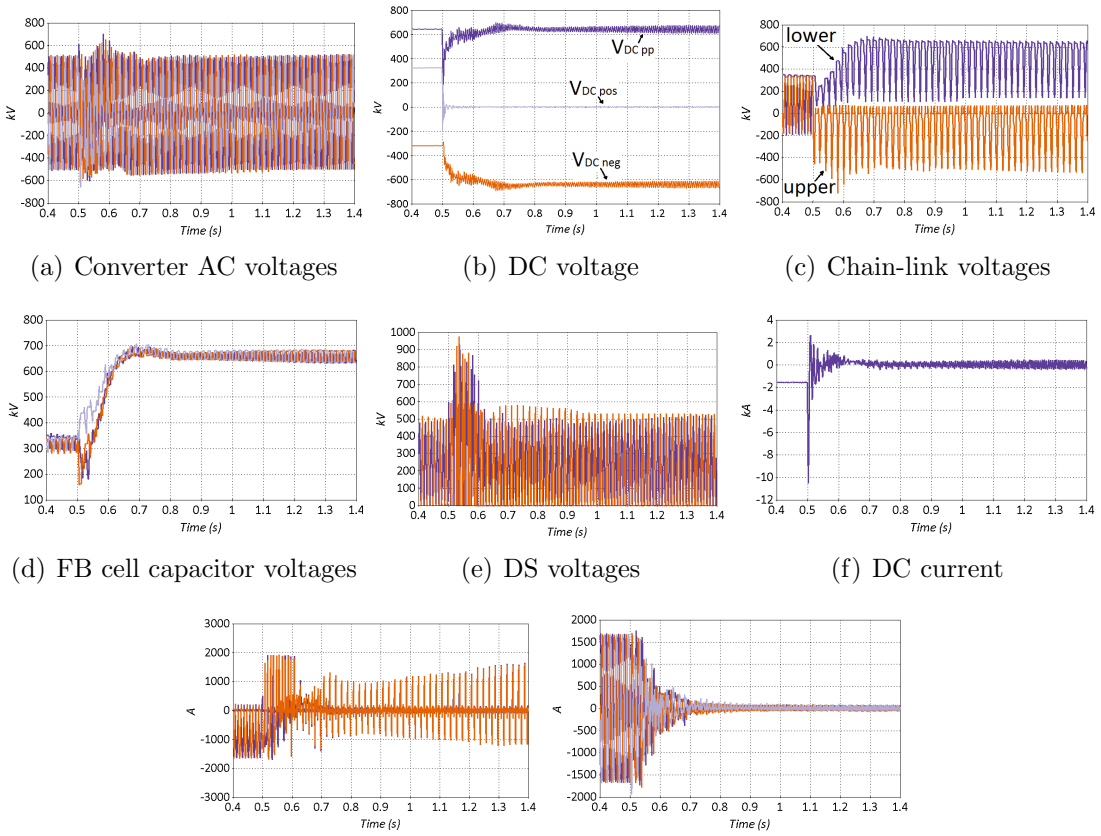
(g) Arm currents

Figure 5.28: FB-MMC pole-to-ground fault.

AAC

During a DC pole-to-ground fault, the AAC is over-modulated, in a similar manner to the MC-MMC, as the converter tries to support the AC voltage, as shown in Fig. 5.29(a). The AAC is unable to achieve 0.5 p.u. of DC voltage operation as its modulation index range is limited as explained in Chapter 4. Therefore when the voltage collapses at the faulted pole, the healthy pole has to sustain the full V_{DC}, as illustrated in Fig. 5.29(b), resulting in instantaneous collapse of the cable insulation. Additionally, in order to operate the arm in over-modulation mode, due to the internal operation of the AAC, the chain-link voltages shown in Fig. 5.29(c) must exceed the nominal value. This also results in increased cell capacitor voltage as shown in 5.29(d). Furthermore the DS voltages exceed their nominal value and exceed their insulation levels, as shown in Fig. 5.29(e). A high magnitude DC current is developed due to the DC filter discharge, as shown in 5.29(f). The arm and AC currents drop to zero resulting in zero power exchange, as shown in Figs. 5.29(g) and 5.29(h) respectively. As a result, in contrast to

the MC and FB-MMC which are both capable of DC pole-to-ground FRT, the AAC achieves an unstable condition and is unable to achieve pole-to-ground FRT without damaging the internal insulation.



(a) Converter AC voltages (b) DC voltage (c) Chain-link voltages

(d) FB cell capacitor voltages (e) DS voltages (f) DC current

(g) Arm currents (h) Converter AC currents

Figure 5.29: AAC pole-to-ground fault.

5.6 Unbalanced AC faults

HVDC converters are likely to experience unbalanced conditions due to AC phase-to-ground or AC phase-to-phase faults. It has been proven that it is possible to comply with the Grid Code regarding FRT by employing control systems which make it possible to keep the converter connected for a long period during unbalanced AC faults without tripping. Multiple solutions have been proposed [94, 95], but many include multiple control loops hence they are over-complicated. The controller that is used in this thesis is simpler and can suppress the $2^n d$ order current harmonics under all operation conditions. The focus of this section, therefore, is to achieve FRT using a very simple control technique and to demonstrate

the effects of the unbalanced fault and the consequent controller action on the rest of the DC network.

A simulation study of MMCs and AACs converters under unbalanced AC operation is presented. In this study the objective is to control the converter AC currents. In both cases, this is achieved using a simple double-frame current controller which injects positive sequence currents and sets the negative sequence currents to zero, as described in Chapter 3. In the case of MMC, the excessive distortion at a frequency of 2ω that appears on the cm currents during unbalanced operation is easily suppressed by a PR (proportional resonant) controller tuned to twice the fundamental frequency.

In order to observe the functionality of the converters and their dedicated controllers, a case study are tested as shown in Fig. 5.30. In this case study, a severe single AC phase-to-ground fault occurs between phase a and ground, at $t =$ 1 s and lasting for 0.4 s, with $R_{fault} = 0.1\ \Omega$. The applied fault is considered to be the worst-case scenario as it occurs on the grid side of the converter controlling V_{DC}, without any cable impedance to limit fault current. Due to the power exchange imbalance between the AC and DC sides, the DC voltage will affect the DC current by increasing or decreasing according to the direction of power flow, as shown in Fig. 5.31. In the case of inverter mode the DC voltage exceed the rated values jeopardising the insulation, while in inverter mode the DC voltage is reduced to the rectification voltage (see Chapter 3), and during recovering the DC current exceed the overload operation for a considerable amount of time.

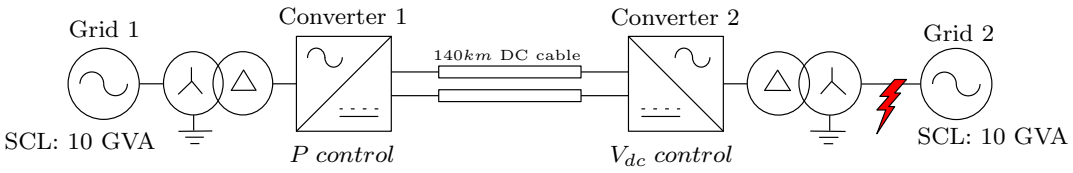
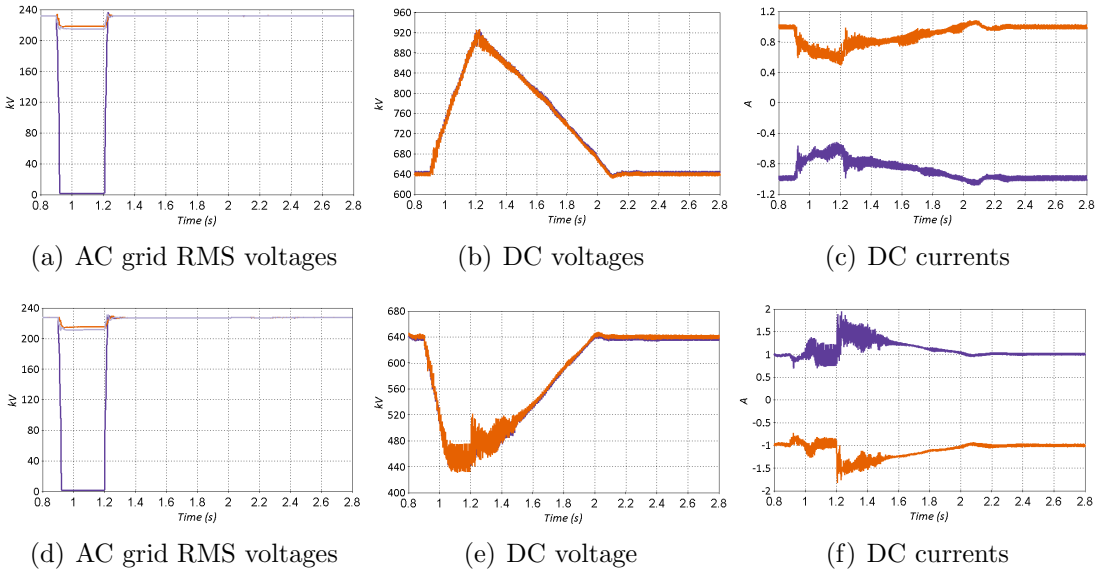


Figure 5.30: Test network for AC unbalanced operation.

To avoid this, the power reference must be reduced, to maintain the power equilibrium between the AC and DC sides. It is assumed that the master controller communicates with both converter stations and that it will set appropriate power references. Alternatively, in all cases, a DC chopper may be employed to absorb excess power resulting from DC voltage increase. However the DC chopper adds to the capital cost, and in the case of an offshore platform the real estate cost increases dramatically.



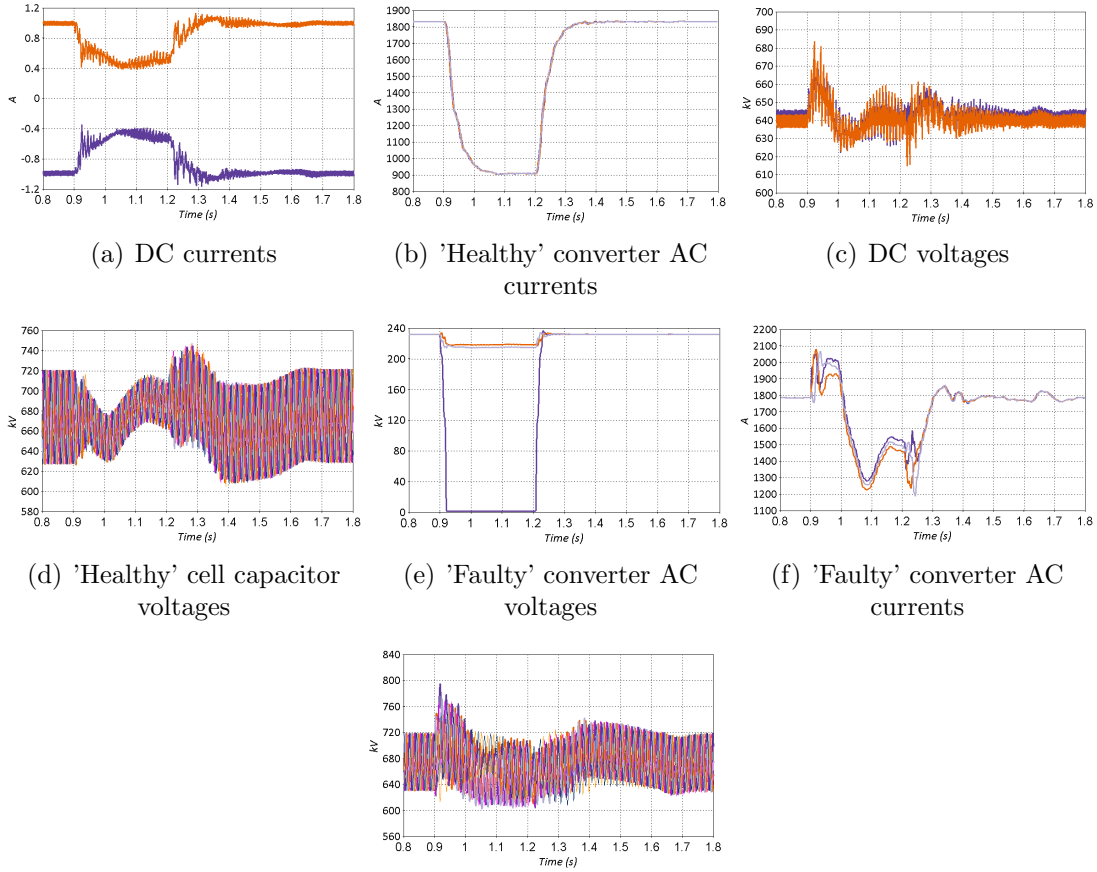
(a) AC grid RMS voltages (b) DC voltages (c) DC currents

(d) AC grid RMS voltages (e) DC voltage (f) DC currents

Figure 5.31: AC unbalanced operation on V_{DC} controlled MMC without power reduction during inverter (upper row) and rectifier (lower row) mode.

5.6.1 MMC

During unbalanced operation an MMC does not need to operate in over-modulation mode. The behaviours of the HB, MC and FB variants of the MMC are therefore identical. The simulation results presented are therefore based on HB-MMC. The reduction in power resulting from the AC fault in indicated by the reduction in the DC and AC currents in the healthy converter, as shown in Fig. 5.32(a) and 5.32(b). The DC voltage is also affected, exhibiting some small-amplitude oscillation, shown in Fig. 5.32(c). In the healthy converter, the capacitor voltage ripple is of low magnitude as the capacitors experience lower current, shown in Fig. 5.32(d). With regards to the 'faulted' converter, the faulted phase is indicated by the significant drop in grid phase voltage, as shown in 5.32(e). Although the three-phase voltages at the grid side are severely unbalanced, the simple double-frame controller provides effective support and maintenance of the AC currents by keeping the negative-sequence components to zero and balance the converter AC currents, as shown in Fig. 5.32(f). Furthermore, the PR controller ensures that the magnitudes of the circulating second-order harmonic currents are suppressed and do not penetrate the DC current. The overall strategy achieves AC current control with minimal DC current and voltage oscillations and with low capacitor voltage ripple, as shown in Figs. 5.32(a), 5.32(c) and 5.32(g) respectively.



(a) DC currents

(b) 'Healthy' converter AC currents

(c) DC voltages

(d) 'Healthy' cell capacitor voltages

(e) 'Faulty' converter AC voltages

(f) 'Faulty' converter AC currents

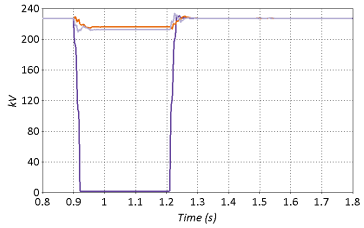
(g) 'Faulty' cell capacitor voltages

Figure 5.32: HB-MMC AC unbalanced operation with power reduction.

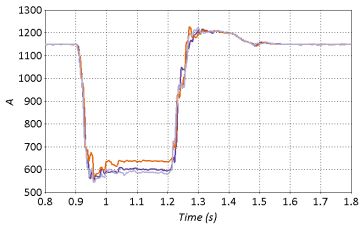
5.6.2 AAC

The performance of AAC during unbalanced operation is similar to that of the MMC. Fig. 5.33 illustrate the waveforms of the healthy and 'faulted' AAC during unbalanced operation. The unbalanced AC voltage on 'faulty' converter grid side is shown in Fig. 5.33(a), which lead to a power reduction from the 'healthy' converter side as shown in the reduced AC currents in Fig. 5.33(b). The 'faulty' converter regulates its AC currents effectively, shown in Fig. 5.33(c)) by keeping the negative-sequence current to zero. Due to the arm current discontinuity the DC current contains high magnitude ripple during the fault. Also, the AAC does not have any circulating current controller to regulate the double fundamental frequency oscillations. These oscillations are transferred to the DC voltage and current, as shown in Figs. 5.33(d) and 5.33(e) respectively. As a result, the AAC DC current and voltage are distorted by high-magnitude and high-frequency

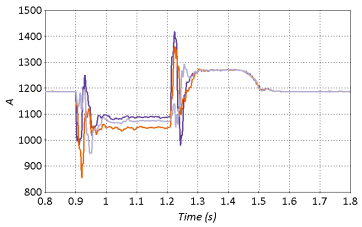
components. Current oscillations at double the fundamental frequency affect the overlap control, resulting in poor DC current quality. The high-frequency currents also affect the cell capacitor voltages in both converters, leading to marginal collapse of the voltage balancing process, as illustrated in Figs 5.33(f) and 5.33(g). This results in an oscillatory DC voltage profile which is not characteristic of the MMC and which is a significant disadvantage during AC unbalanced operation.



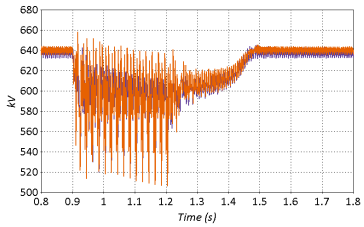
(a) 'Faulty' converter AC voltages



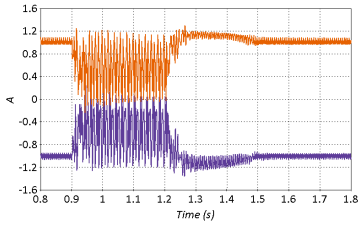
(b) 'Healthy' converter AC currents



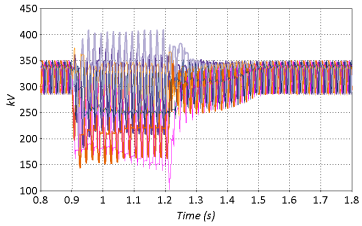
(c) 'Faulty' converter AC currents



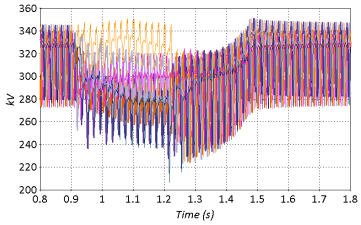
(d) DC voltages



(e) DC currents



(f) 'Faulty' cell capacitor voltages



(g) 'Healthy' cell capacitor voltages

Figure 5.33: AAC AC unbalanced operation with power reduction.

5.7 Partial DC voltage loss on diode rectifier based HVDC

In this section the ability of the MC-MMC to operate at reduced DC voltage is presented. The study is based around the system shown in Fig. 5.34, which shows an HVDC system consisting of a point-to-point DC grid where a strong

AC grid is interfaced to several weak grids through an MC-MMC. The output of each weak grid is converted to DC through a diode rectifier unit (DRU), and the outputs from each DRU are series connected before connection to the DC grid. Each DRU has a switch S_{BP} which allows it to be bypassed if it becomes faulted. The benefits of this grid topology are the reduction in semiconductor

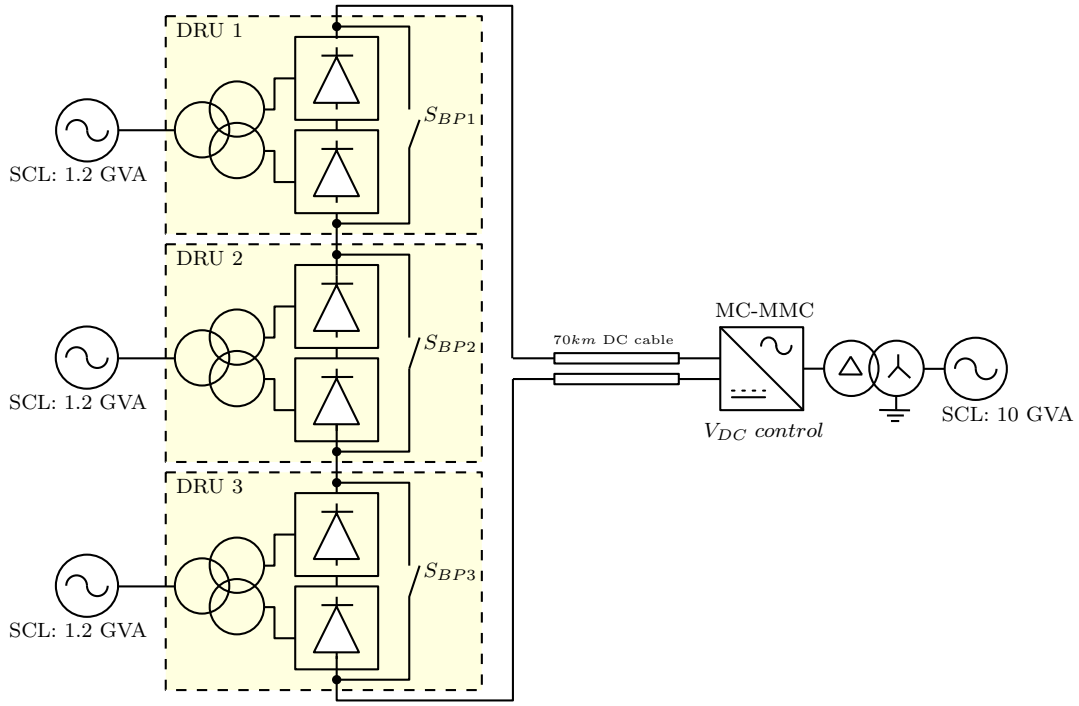
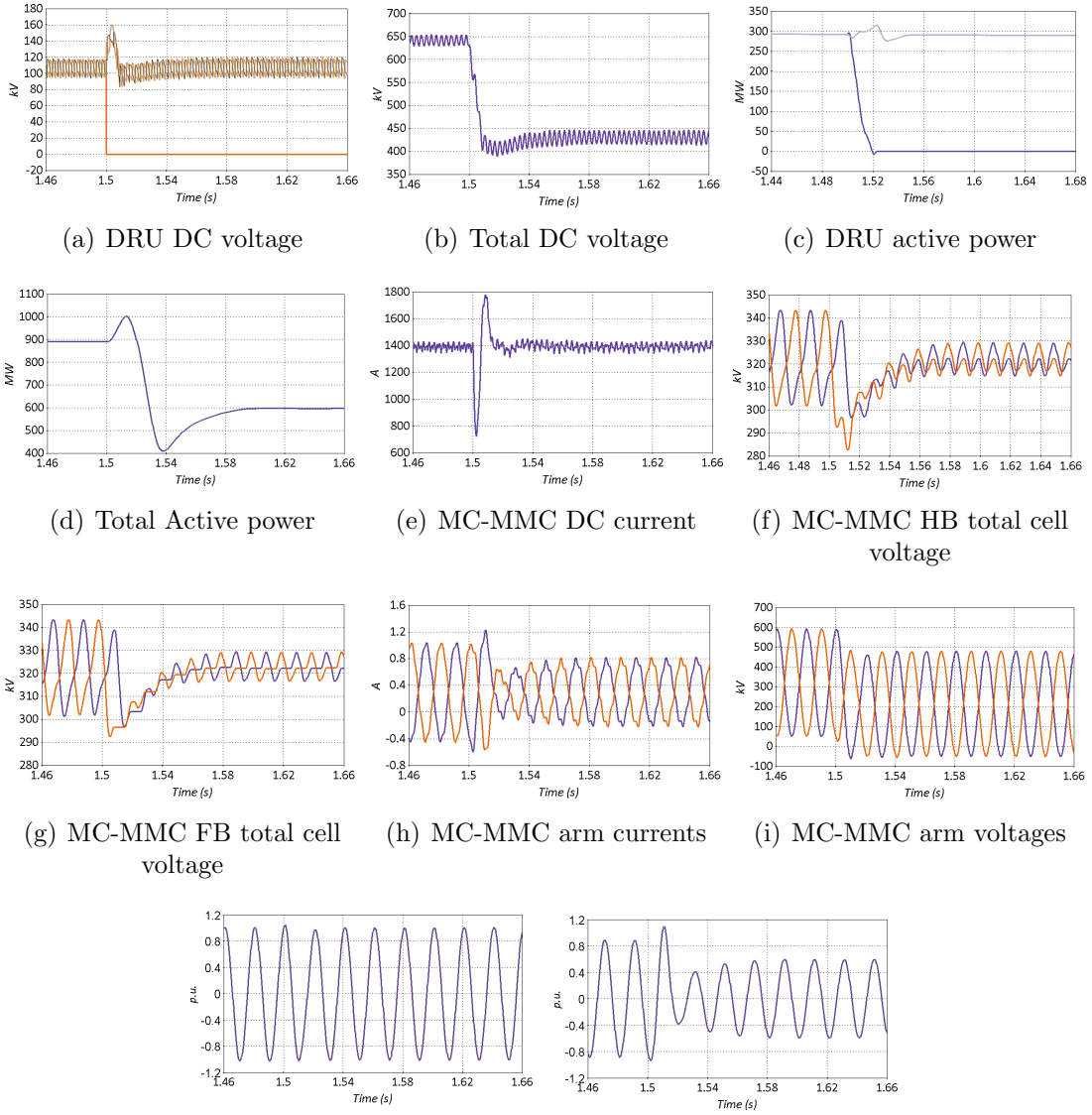


Figure 5.34: Point-to-point HVDC system with grids connected to an arrangement of DRU and MC-MMC.

losses and the smaller footprint of the DRU when compared to a more complex converter topology. This enables siting of DRU on redundant oil platforms. This re-purposing of an existing offshore structure significantly reduces the capital cost of the system. The DRU is considered to be a unipolar uncontrolled rectifier, which means that the DRU cannot control actively either power or DC voltage. As a result, the power is regulated directly from the weak grids, while the DC voltage is regulated from the MC-MMC.

The modular series connection of the DRUs allows the synthesis of high DC voltage. However, in the case of a fault which requires disconnection of one or more DRU from the grid, the magnitude of the aggregated DC voltage is immediately and significantly reduced. This would be a significant challenge in systems that used an HB-MMC or an AAC to interface to the strong AC grid, as it was shown in Chapter 4 that these converters cannot operate if the DC voltage is significantly reduced. Appropriate candidates for reduced DC voltage

operation are the MC and FB-MMC, which can both operate with reduced DC voltage without affecting AC voltage as power is transferred. The MC-MMC is however considered the better option as it is more efficient, as shown in Chapter 3, and is therefore is used as the strong AC grid interface converter in this study, as shown in Fig. 5.34.



(a) DRU DC voltage (b) Total DC voltage (c) DRU active power

(d) Total Active power (e) MC-MMC DC current (f) MC-MMC HB total cell voltage

(g) MC-MMC FB total cell voltage (h) MC-MMC arm currents (i) MC-MMC arm voltages

(j) MC-MMC converter AC voltage (k) MC-MMC converter AC current

Figure 5.35: Partial loss of DC voltage in a DRU-MMC HVDC system.

The simulation study now examines the case where a DRU becomes faulty and is bypassed, thereby reducing the DC voltage supplied to the point-to-point DC grid. The simulation results are presented in Fig. 5.35. Referring to Fig. 5.34,

bypass switch S_{BP2} is enabled at $t = 1.5$ s and DRU 2 is disconnected. DRU 1 and DRU 3 continue to operate as normal whilst the output from DRU 2 falls to zero, as shown in Fig. 5.35(a). Consequently, the aggregated DC voltage is reduced by 33% as shown in Fig. 5.35(b). The MC-MMC, which controls the DC voltage, sets the new reference to be 66% of the original value. The power outputs from DRU 1 and DRU 3 remain unchanged whilst the power output from DRU 2 falls to zero, as shown in Fig. 5.35(c), and the total aggregated power is 33% as shown in Fig. 5.35(d). DC current falls rapidly but recovers to its nominal value, with a large overshoot, shown in Fig. 5.35(e), as the MC-MMC regulates the DC voltage in response to the new reduced reference whilst continuing to transfer power at a reduced level. Internally, the MC-MMC cell capacitor voltages, shown in Figs. 5.35(f) and 5.35(g), are well balanced after a brief undershoot, with a reduced voltage ripple due to reduced arm current, as shown in Fig. 5.35(h). The arm voltages in Fig. 5.35(i) show that the MC-MMC can react quickly and operate successfully at reduced DC voltage without affecting the converter AC voltage and current, shown in 5.35(j) and 5.35(k) respectively. From this simulation study it can be concluded that MC-MMC is able to manage the loss of DRU without interrupting or affecting the operation of rest of the HVDC grid.

5.8 Summary

This Chapter presents a set of simulation scenarios to compare AAC and MMC converter topologies during start-up, a DC pole-to-pole fault, a DC pole-to-ground fault and an AC phase-to-ground fault. During charging for all converter topologies FB cells must emulate the operation of HB cells −otherwise the converter and the grid cables are not able to charge. In converters which mix HB and FB cells, both HB and FB cell capacitors charge simultaneously. In weak grids the AC supply cannot be used to charge the converter, and this instead must be achieved from the DC grid. The start-up sequences for both AAC and MMC are similar.

The DC pole-to-pole fault is characterised and analysed for all multilevel converters. MC and FB-MMC, and AAC are able to block and recover from a DC pole-to-pole fault. A technique to control DC fault current trajectory that combines an MC-MMC incorporating a small number of FB cells and DC link reactors is investigated and presented as a method that may be used to relax the challenging design requirements for future DCCBs.

The DC pole-to-ground fault is characterised and analysed for all multilevel converters. This simulation study shows that the MC-MMC and FB-MMC can

Table 5.2: Converter functionality.

Converter topologies	Pole-to-pole DC fault	DC fault current limit	Pole-to-ground DC fault	Partial DC loss
HB-MMC	No	No	No	No
MC-MMC (15-25% FB)	No	Yes	No	Limited
MC-MMC (50% FB)	Yes	Blocking	Yes	Yes
FB-MMC	Yes	Blocking	Yes	Yes
AAC	Yes	Blocking	No	No

survive a pole a DC pole-to-ground fault whilst continuing power transfer. The FB-MMC could offer advantage during a fault due to its capability to generate full negative DC voltage. However this attribute becomes redundant during a DC pole-to-ground fault since the DC voltage is controlled to be 0.5 p.u. In contrast to the MC and FB-MMC, the AAC is unable to achieve DC pole-to-ground fault ride through without damaging the internal insulation.

During unbalanced AC voltage operation, all MMC variants achieve FRT with minimal DC current and voltage oscillations, and with low capacitor voltage ripple. In contrast, the AAC achieves FRT which is characterised by an oscillatory DC voltage profile which a significant disadvantage during AC unbalanced operation.

A structure that aggregates power from multiple weak grids and connects them to an HVDC network through series-connected DRUs has recently been proposed. It has been shown that the MC-MMC is a suitable converter for interfacing the HVDC system to the strong AC grid as it is able to manage and react quickly to partial DC voltage loss without interrupting HVDC grid operation and whilst continuing to transfer power.

The converter attributes are summarised in Table 5.2. Even if the initial design of most of the converter topologies was to block a DC pole-to-pole fault, this chapter shows that there are in general other faulty and transient situations that the converter should compensate. The AAC was originally developed to provide efficient DC pole-to-pole FRT. However, its inability to survive pole-to-ground faults and its reduced power quality during AC unbalanced faults are significant disadvantages. The MC-MMC, however, does not suffer from these

disadvantages and is able to survive faults whilst maintaining high power quality. The MC-MMC is also a suitable converter for inclusion in hybrid HVDC networks that incorporate DRU.

Chapter 6

Reduced-scale experimental set-up for multilevel converters and HVDC grids

6.1 Introduction

Off-line simulation provides fast validation of concepts and ideas, and requires minimal investment. However, simulation studies may exclude many real-world considerations, such as global radiation, whilst assumptions (e.g. uniformity of passive elements, communication delays) may also be made to reduce system complexity and thereby reduce computational effort. Real-time simulation maybe used to validate control architectures, where the target is to execute the simulated control system algorithm in the same time period as the actual controller. Although real-time simulations are a valid method for validating controllers [96], power circuit simulation is complicated by the considerations and assumptions mentioned previously. Also, the time steps used in the solvers, either off-line or in real-time, if not considered carefully, may result in ambiguous results. Ideally, a full-scale hardware replica of the off-line simulation models offers the best validation of a concept, including the controller and the engineering configuration. However, this is cost and time inefficient, and a reduced scale hardware system is more practical. In the case of reduced scale test hardware, the controller operation, converter structure, and the real-life non-ideal elements can provide experimental validation of the off-line simulations. However, phenomena such as the interaction of components at high-voltage, actual semiconductor losses, physical dimensioning and volume cannot be validated as they cannot be scaled down. This chapter reports the design and construction of a reduce scale test-rig for experimental validation of AAC and MMC topologies. The test-rig is used to

provide evidence of valid operation of several of the off-line case studies presented in Chapters 4 and 5, and the proposed enhanced MMC converter presented in Chapter 7.

6.2 System design

The experimental converter consists of six arms, with four FB cells per arm. Each arm includes an inductor and a single IGBT. In this arrangement the experimental set-up is able to operate in AAC and MMC modes, as described in Chapter 3. In an AAC mode the single IGBT in each arm operates as the DS, while in MMC mode where a DS is not required, the arm IGBT is permanently in the on-state. The schematic of the multilevel converter experimental set-up is shown in Fig. 6.1.

6.2.1 Sizing and dimensioning of experimental set-up

The selection of the passive components of the reduced-scale test-rig (RSTR) are based on the reference system (RS) specifications that are used in Chapters 4 and 5. The RS is based on a 400 kV, 1 GW HVDC link, similar to the INELFE project [89]. The RSTR converter is a scaled down version of the RS, as described in Table 6.1, according to the methodology that was used in BestPaths Demo #1 project [97].

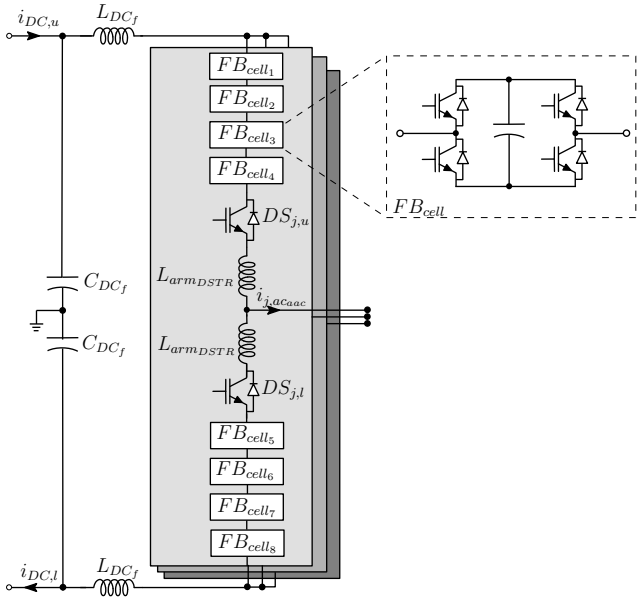


Figure 6.1: Experimental set-up of the multilevel converter.

Table 6.1: Reference and test-rig specifications.

Value	Reference system (RS)	Reduced-scale test-rig (RSTR)
DC voltage	640 kV	300 V
Apparent power	1060 MVA	4 kVA
Converter AC line-to-line voltage	320 kV	150 V
Number of cells	400	4
Effective switching frequency	80 kHz	40 kHz
Cell capacitance	13 mF	2.2 mF
Arm inductance (MMC)	65 mH (18 p.u.)	5 mH (24 p.u.)
Transformer inductance (MMC)	65 mH (18 p.u.)	1.2 mH (5.8 p.u.)
Arm inductance (AAC)	11 mH (1.4 p.u.)	2.5 mH (5.5 p.u.)
DC inductance (AAC)	100 mH (12.5 p.u.)	9 mH (19.5 p.u.)
Transformer inductance (AAC)	150 mH (18 p.u.)	1.2 mH (0.15 p.u.)

The reduced scale system should maintain and preserve as much as possible the dynamics of the full-scale system with regard to converter stored energy. Moreover, the following criteria are also considered.

- Each arm chain-link contains only 4 cells in order to reduce cost, and control and circuit complexity. Additionally, the low number of cells facilitates demonstration of the effects of large voltage errors among the arms.

- Semiconductors voltage ratings are deliberately over-sized in order to maximise system reliability. The voltage rating of each cell is the DC voltage divided by the number of levels, and is therefore small. At the reduced voltage and power levels, MOSFETs would be a more appropriate semiconductor choice. However, IGBTs are chosen in order to ensure high system reliability, as they have higher voltage ratings for reduced cost.

- In general, considerations regarding reduced complexity and increased reliability are traded for reduced efficiency as the target of the reduced scale test-rig is to validate concepts rather than to meet manufacturing and economic-technical requirements.

Transformer inductance The reference model transformer inductance is 0.18 p.u. However, achieving such a high impedance for a low power and voltage rated transformer is very costly. As a result, a conventional wye-delta transformer with 0.06 p.u. impedance is used. The reduced transformer inductance is compensated by increasing the arm inductance.

Arm inductance The arm inductance must be able to sustain overload current in order to avoid saturation. Although air-cored inductors are considered an efficient choice with low losses, iron-core inductors are chosen due to their smaller footprint. The reference model arm inductance is 0.18 p.u. However, to compensate for the reduced transformer inductance, the test-rig arm inductance is chosen to be 0.24 p.u. The arm inductance is calculated by (6.1) according to the values in Table 6.1.

$$L_{arm_{DSTR}} = \frac{V_{AC_{RS}}^2}{V_{AC_{DSTR}}^2} \frac{S_{RS}}{S_{DSTR}} L_{arm_{RS}} \tag{6.1}$$

The DC component of the arm current which dictates the iron losses, and which is dependent on the cm and circulating currents, must also be considered in order to avoid overheating.

Cell capacitor The cell capacitors for an MMC are designed to allow a $\pm 10\%$ voltage ripple during suppressed circulating currents. When the circulating currents are not suppressed the voltage ripple is expected to double [98]. As a result, cell capacitor voltage ripple of $\pm 20\%$ represents a worst case scenario for steady-state MMC operation, without considering any transient phenomena. The nominal cell voltage is 75 V, but the capacitor voltage is specified to be 150 V in order to sustain transient operation and increased capacitor voltage ripple. Cell capacitance is sized according to the reference model, resulting in cell capacitance of 2.2 mF, as calculated using:

$$C_{cell_{DSTR}} = \frac{N_{DSTR}}{N_{RS}} \frac{V_{AC_{RS}}^2}{V_{AC_{DSTR}}^2} \frac{S_{RS}}{S_{DSTR}} C_{cell_{RS}} \tag{6.2}$$

EMI Considerations Due to the rapid and frequent switching of voltages and currents, power electronic systems will produce interference in the radio frequency range which can be transmitted into sensitive equipment. This EMI exist due to the magnetic or electrical coupling of low voltage and current systems, such as microcontrollers, with the higher power system. Also due to the concentration of both high and low power components in a small space, sensitive equipment such as microcontrollers and signal hubs are prone to EMI. In order to suppress the EMI emissions from the power circuit, certain techniques can be applied [99]. Electrical coupling can be minimised by reducing the parasitic capacitance between the signal connectors, while the magnetic coupling can be reduced by minimising parasitic inductance in the signal paths. In both cases, this can be achieved by reducing the length of signal conductors and by minimising signal

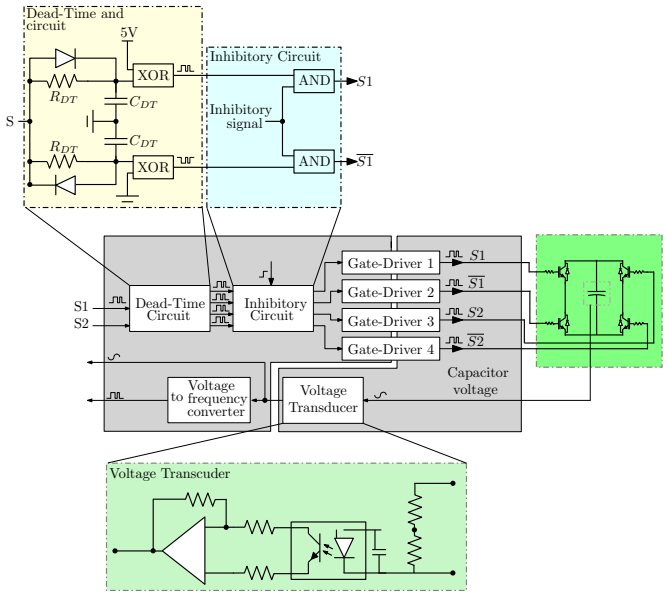
return paths. Additionally, careful design of signal zero-volt references through isolation of ground planes helps to preserve signal integrity. This is particularly important when dealing with safety-critical signals, such as the 'inhibit' command required to block the converter. EMI can be also be minimised by using twisted pairs of conductors. In printed circuit board (PCB) design it is advantageous to run tracks orthogonally and through a multilayer structure to minimise coupling and path length. CMOS based logic components have increased noise immunity when compared to TTL components. Finally, signal transmitted through fibre optic cables are immune to EMI.

Cell board

The cell is the key sub-circuit of the modern multilevel converter. It is therefore crucial to design and construct a robust cell which allows, through different arrangements, testing of a variety of multilevel converters. As mentioned in Chapter 2, there are numerous cell topologies which offer good efficiency and low complexity. To reduce construction complexity and to increase converter flexibility, the FB cell structure, which offers bipolar operation, is selected for the reduced-scale test-rig.

FB cell design An FB cell requires four input signals: one for each semiconductor in the bridge. In an MMC this will result in a large number of connections. Additionally the need to provide four control signal for each FB cell imposes a significant burden on the microcontroller. To address both of these issues, a strategy which requires only two outputs per FB cell from the microcontroller and which redeploys some of the computational effort to an auxiliary circuit is chosen, as shown in Fig. 6.2. The auxiliary circuit acts on the two control inputs to generate the four switching signals required to operate the FB, and includes dead-time generation, using a RC-diode network, and a cell inhibit facility. To address EMI, fibre optic cables are used to connect the microcontroller to the auxiliary circuits. The reduction in the number of connections required significantly reduces the construction cost.

The nominal dead-time is 2.5 μ s, which is achieved using a 3.3 kΩ resistor R_{DT} and a 2.5 nF capacitor C_{DT}. Because the upper and lower switches in a bridge leg are not driven independently, a dedicated inhibit signal and circuit are necessary to ensure that the cell can switched into a blocking state. The inhibit signal is set directly from the master controller, where the protection and detection algorithms are included. Each signal, S1 and its complement shown in 6.2, supplies a gate driver which consists of an optocoupler with a dedicated isolated



(a) Schematic

(b) Photograph

Figure 6.2: Experimental FB cell.

power supply which provides the voltage and current levels required to operate the IGTB. A gate resistance of 15 Ω is introduced according to manufacturer's recommendation. A low cost, low footprint voltage transducer in the form of an isolated power amplifier is used, as shown in 6.2. The voltage input to the transducer is scaled down using a voltage divider. The high-resistance divider network and the high-impedance transducer input draw very low current. A film capacitor is connected in parallel with the transducer input to provide high fre-

quency noise rejection. The differential output from the voltage transducer feeds an operational amplifier (OpAmp) circuit, which matches the requirement (DC offset and magnitude) the microcontroller analogue input. If a digital signal representation is required, a low cost and computational effort solution is to feed the OpAmp output into a voltage-to-frequency converter (VCO). The output of the VCO is connected directly to a digital input of the microcontroller, which translates the frequency to a voltage magnitude. The cell capacitors are of the electrolytic aluminium variety, allowing a higher capacitance at higher voltages and at lower cost. Electrolytic capacitors have relative high equivalent series resistance (ESR) which increases the total losses of the converter. A method of reducing ESR is to parallel-connect multiple capacitors. This method also allows accurate synthesis of a given capacitance value. However, the total cell footprint may increase by adding more capacitors in parallel. Small value polypropylene film capacitors are connected in parallel with the electrolytic cell capacitor to provide a low ESR path for high frequency current, to reduce switching noise. Moreover, polypropylene film snubber capacitors are used to reduce the IGBT voltage overshoot resulting from the PCB track parasitic inductance.

Cooling

The FB cell IGBTs are connected to the same heatsink. A representation of this arrangement is shown in Fig. 6.3. The thermal resistance of the heatsink is calculated to ensure that the IGBT junction temperature T_j (T_S and T_D) does not exceed 120^oC for ambient temperature T_{amp} of 25^oC. This junction temperature is well within the manufacturer's specification [100].

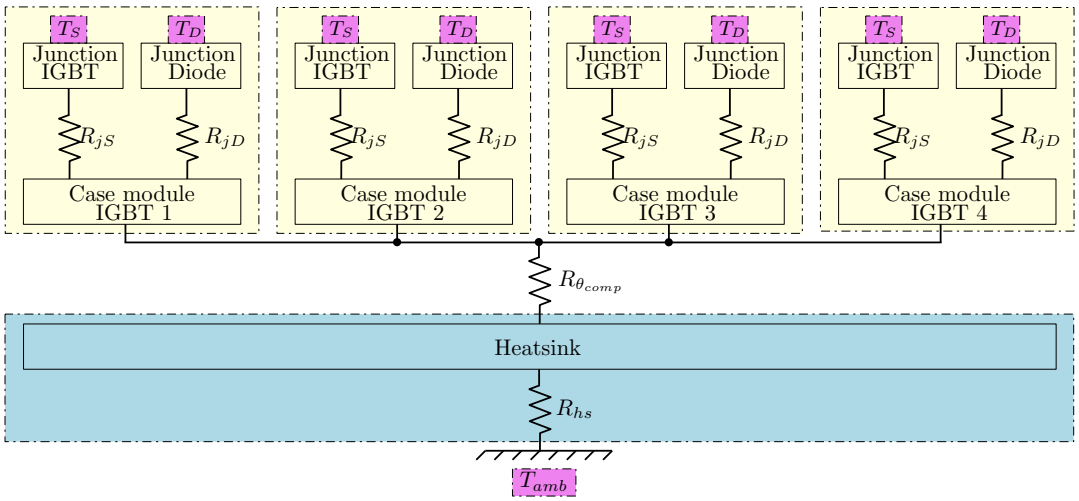


Figure 6.3: Thermal model showing four IGBTs connected to a single heatsink.

The IGBT case-to-junction thermal resistance $R_{mod_{j-c}}$ given by (6.3), where R_{jS} and R_{jD} are the case-to-junction thermal resistances for the switch and diode respectively.

$$R_{mod_{j-c}} = \frac{R_{jS} \cdot R_{jD}}{R_{jS} + R_{jD}} \tag{6.3}$$

Each IGBT is connected to the heatsink through $R_{\theta_{comp}}$ which represents the thermal resistance of the heatsink compound used. The total thermal resistance R_c between the junction and the heatsink for all four IGBTs is therefore given by (6.4).

$$R_c = \frac{4}{R_{mod_{j-c}} + R_{\theta_{comp}}} \tag{6.4}$$

The heatsink-to-ambient resistance R_h is calculated according to the number of mounted IGBT modules n and the corresponding power dissipation of each module P_{TL-mod}, and is given by (6.5).

$$R_{hs} < \frac{t_j - T_{amb}}{n \cdot P_{TL-mod}} \tag{6.5}$$

Table 6.2 specifies the thermal characteristics of the Infineon IKW40N120H3 IGBT selected for the reduced scale test-rig.

Table 6.2: Cell thermal characteristics.

Description	Value
Thermal junction-to-case resistance IGBT R_{jS}	0.31 K/W
Thermal junction-to-case resistance diode R_{jD}	1.11 K/W
Thermal resistance of heatsink compound $R_{\theta_{comp}}$	0.9 K/m·W
Thermal resistance of heatsink-to-ambient R_h	1.1 K/W
Total cell losses $n \cdot P_{TL-mod}$ (5 kW)	32.6 W

The cell power losses are calculated according to the analysis of Chapter 3. Cell losses are considered for the case where the reduced scale test-rig operates at 5 kW, exceeding the nominal power specification of 4 kW. This is considered to represent extreme operation that includes long duration transient phenomena. In the case of fast, high current (>20 A) transients, protection algorithms will block the converter and prevent the IGBTs from overcurrent and overheating. When operated at 300 V and 5 A with a 20 kHz square-wave reference, cell thermal behaviour is acceptable with device junction temperature of 76.1^oC as shown in Fig. 6.4.

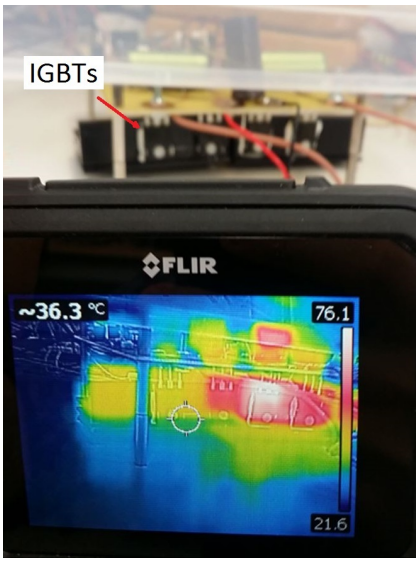


Figure 6.4: Thermal image of IGBTs in FB cell.

Test set-up efficiency

Total losses, and therefore converter efficiency, are defined according to the semiconductor, the cell capacitor, and the iron-core losses in the arm inductors. The transformer, cables and any other collateral equipment such as relays are not considered when calculating converter efficiency.

The total semiconductor losses can be calculated according to the total cell losses as described in Chapter 3. The measured equivalent resistance of the arm inductors is 0.2 Ω, while the ESR of each aluminium electrolytic cell capacitor is calculated to be 0.101 Ω at 100 Hz. For 4 kW operation at unity power factor (see Table 6.1), Table 6.3 shows the losses and the efficiency of the converter operating in MMC mode.

Table 6.3: Efficiency and losses of converter ($\cos\phi = 1$, 4 kW).

Description	Value
Total semiconductor losses	412.8 W (59.7%)
Total cell capacitors losses	185.9 W (26.9%)
Total arm inductor losses	92.9 W (13.4%)
Total losses	691.6 W
Efficiency	82.71%

From Table 6.3 it can be concluded that the semiconductor constitutes a significant proportion of the power converter losses due to the high on-state voltage drop V_{CE} during conduction, and due to the FB topology where two semicon-

ductors always conduct in each cell. Semiconductor losses may be reduced by incorporating more efficient low-voltage semiconductors such as MOSFETs.

The cell capacitor losses are high due to the relative high ESR, and it could be reduced by parallel connection of capacitors. The high inductor losses are due to the use of an iron core. Inductor losses could be reduced by using an air-core inductor but this would be at the expense of increased footprint. In general, passive components contribute significantly to the total efficiency of the converter, but to reduce passive component losses would require additional components at additional capital cost, and increased space. These are not constraints in the development of the reduced scale test-rig.

6.3 Controller execution time and sequence

The converter control system consists of three layers of control: the dSpace unit (master and upper level controllers), the PSoC (low level controller), and the local cell logic (dead-time, and inhibitory logic), as shown in Fig. 6.5. The control system is designed to be a non-centralised asynchronous distributed architecture, in order to reduce computational effort, complexity and cost of the controller equipment. According to the control structure in Chapter 3, the outer controller settling time is 100 ms while the inner current controller settling time is 10 ms. The dSpace system, which includes the whole upper level control structure, samples every 100 μs (10 kHz). The PSoC interrupt timer is set at 400 μs (2.5kHz)

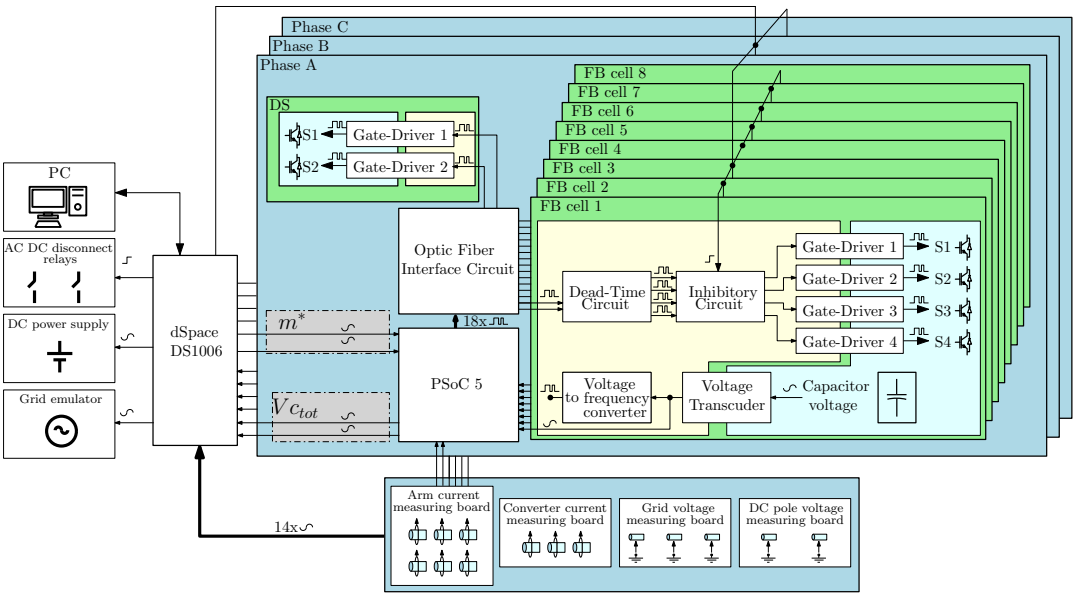


Figure 6.5: Reduced scale test-rig controller architecture.

which defines the switching frequency of each cell. The complete lower level control algorithm is executed in 100 μs (10 kHz). The propagation delay between the input to the dead-time circuit and the IGBT gate is 75 ns.

6.3.1 Low level control optimisation

For each phase of an FB-MMC that consists of 4 cells in each arm, 4608 unique converter states exist, which are defined by current direction, cell voltage output, sorted cell voltage index, and modulation index. The action of the auxiliary circuit which generates four outputs from two inputs, as shown in Fig. 6.2, reduces this to 2304 unique states. To represent these states still requires at least a 12 bit operator (4096). The physical logic required to realise this is significant but almost 50% of its capability would remain redundant, making this a very inefficient solution. In addition, the PSoC 5 used in the test-rig is not capable of representing the required number of states in addition to performing its other functions.

By combining operations which requires similar functions, the number of states may be optimise and reduced from 2304 to 192. Instead of requiring a substantial state machine which includes all inputs and outputs, each required function is split in smaller state machines which require fewer unique states. For example, a cell is sorted as the 2nd highest voltage cell, with positive current, and is required to produce positive voltage when 3 cells need to be inserted. This converter state is defined by four properties. In order to produce a new state, rather than redefining all four properties from the beginning, just one of the properties can be rearranged while the rest are kept the same. Fig. 6.6 shows the state machine architecture required to represent the reduced number of converter states. The main loop processes the required converter properties at frequency of 10 kHz and generates the state machine output required to achieve the corresponding converter operation.

6.3.2 Controller interface

The main controller (dSpace) implements the upper level controls defined in Chapter 3, and provides the modulation indices to the Lower level controller (PSoC 5) through analogue signals. The dSpace and PSoC 5 systems are not synchronised using a common digital clock, ensuring system compatibility regardless the communication protocol. However the analogue signals are exposed to EMI and increased noise.

The interface between the dSpace and PSoC 5 is defined according to Fig. 6.7.

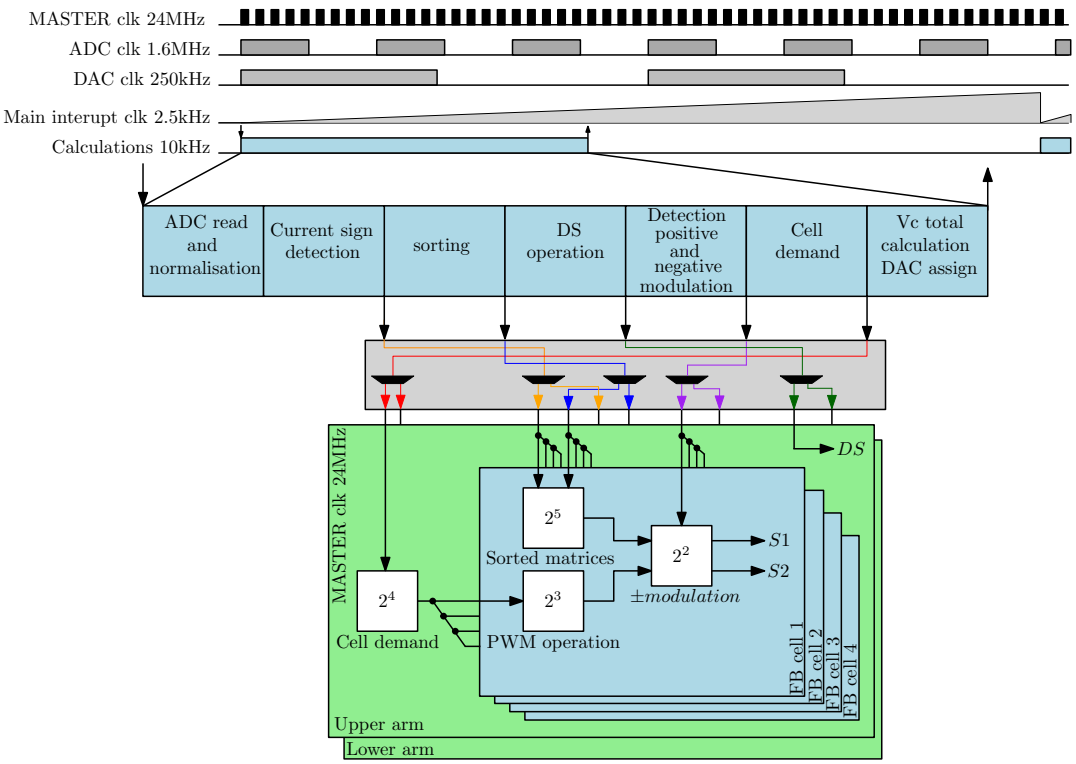


Figure 6.6: State machine with reduced number of converter states.

dSpace 'Controller output' modulation indices are in the range of -1 to 1, which are they converted to a 'dSpace DAC output' in the range 0-4 V. The quantisation error introduced by the 12 bit DAC results in a very small voltage error of 0.092 V at the specified RSTR DC voltage, as defined in Table 6.1. Internally, the PSoC 5 reads the 0-4 V analogue input through a 12 bit ADC with refresh rate of 1.6 MHz. The decimal equivalent 'PSoC ADC input' of the 12bit number is then linearly scaled to the 'PSoC nominalised reference' in the range 0-20000. This process increases accuracy, reduces noise and replaced floating point constants with integers.

The overall controller design is equivalent to the one that was used in off-line simulations and is described in Appendix A.

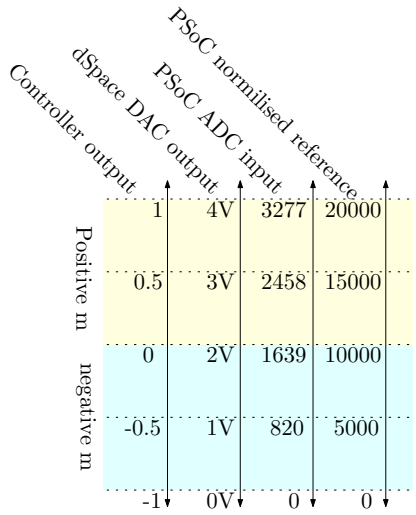


Figure 6.7: Reduced scale test-rig controller architecture.

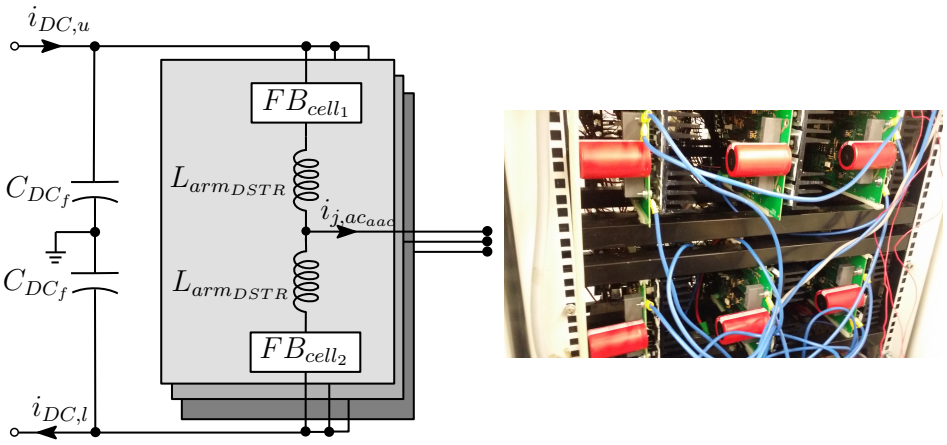
6.4 Hardware implementation of a quasi modular multilevel converter based on the average model

Chapter 3 describes the operation of multilevel converter average models where the cell capacitors are combined into one lumped total capacitance, as shown in Fig. 6.8. Each arm voltage is defined based on the assumption that cell capacitor voltages are perfectly balanced. For some experimental studies which consider the converter's physical stored energy (e.g. power flow, multi-terminal operation, AC transient operation) the complexity of the MMC and AAC described in Section 6.2 is not necessary. Instead an average may be implemented, which meets the needs of these studies, at reduced cost and complexity. This quasi modular multilevel converter (qMMC) includes only one cell per arm with a lumped cell capacitance, similar to average model.

6.4.1 qMMC design and operation

The specification for the reduced-scale qMMC test-rig are similar to those in Table 6.1. However, each arm contains only one cell, and the cell voltage must be rated at the full DC voltage. In addition the cell capacitor $C_{cell_{qMMC}}$ is sized according to (6.6).

$$C_{cell_{qMMC}} = \frac{C_{cell_{DSTR}}}{N_{DSTR}} \tag{6.6}$$



(a) Scematic (b) Photograph

Figure 6.8: qMMC.

where $C_{cell_{DSTR}}$ and N_{DSTR} is the cell capacitance and number of cells of the DSTR respectively. Due to the fact that the qMMC has only a single cell per arm, no CBA is required. As a result, PWM is applied to each cell according to the upper level (dSpace) controller, which is similar to that used in the MMC described earlier, as shown in Fig. 6.9.

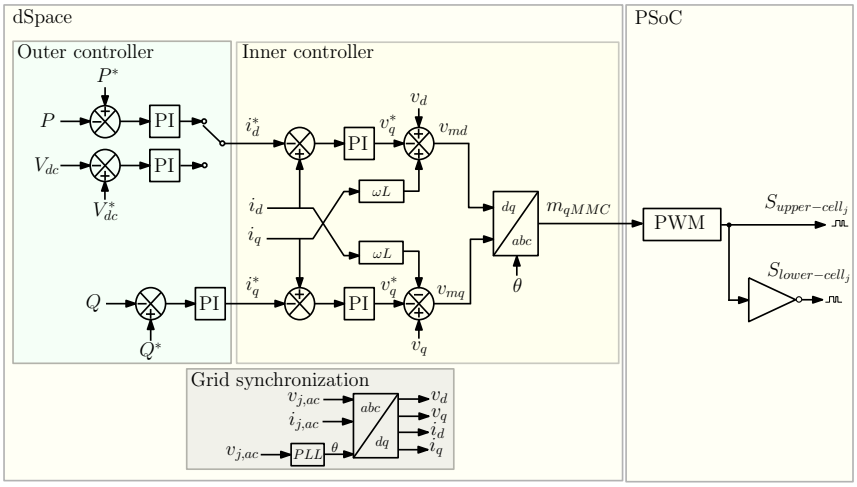


Figure 6.9: qMMC controller design.

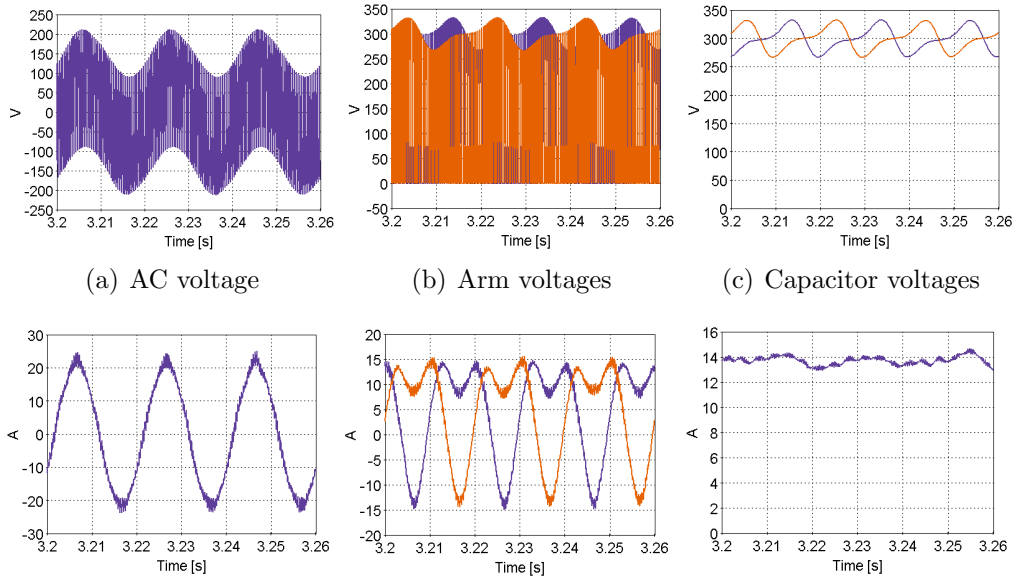
Normally in an MMC each arm is controlled independently in order to control the circulating currents. However such an operation introduces arm voltage mismatch errors of magnitude $\frac{V_{DC}}{N}$. For high numbers of cells the effects of this error are small and can be suppressed by the arm inductors. In the case of the single cell per arm qMMC the arm voltage mismatch error has a magnitude equal to V_{DC}, which synthesises a DC voltage with error ranging between 0 and $2V_{DC}$

that exceeds the voltage limits of the system and which may cause equipment failure. Therefore, each phase arm is modulated from a single reference in a complementary manner. In comparison with the MMC this operation introduces two significant limitations:

- Due to the non-independent operation of each arm it is not possible to suppress the circulating current; thus, the magnitudes of arm current and cell voltage ripple are high.
- Due to only two are voltage states, 0 and V_{DC}, the DC voltage lacks resolution unlike that available from the conventional MMC as shown in Chapter 4.

6.4.2 qMMC verification

Fig. 6.10 shows simulated qMMC performance with the controller specified in Fig. 6.9. The simulation shows well balanced cell voltages, with the arm currents containing 2^{nd} order harmonics. The AC voltage fluctuates according to the arm voltage profile, due to the cell capacitor voltage ripple. The simulation results verify the basic operation of the qMMC.



(a) AC voltage (b) Arm voltages (c) Capacitor voltages

(d) AC current (e) Arm currents (f) DC current

Figure 6.10: qMMC simulation results.

6.5 Experimental Results

The reduced scale test-rig is used to validate controller operation and to provide evidence of the functionality demonstrated by the off-line simulations. In particular, selected operating scenarios such as dynamic operation (PQ capabilities) and AC unbalanced operation of the MMC and AAC, as simulated in Chapters 4 and 5, are investigated experimentally. Also, for these operating scenarios, performance of the MMC and qMMC are compared to validate the concept of the average model hardware implementation. Finally, MMC operation at reduced DC voltage is also investigated. The test-rig set up is shown in Fig. 6.11. The AC and DC relays allow both converters to operate simultaneously or independently. The power flow is from the DC power supply towards to the grid emulator, and all converters operate in active power control mode. The grid emulator is a programmable 15 kW four-quadrant AC to AC power supply which also emulated AC unbalanced operation. The wye-delta transformers are rated at 400 V/230 V and 10 kW. A DC filter is included in each converter in order to create the mid-point DC voltage reference. Finally, the unidirectional DC power supply specification is 600 V and 10 kW.

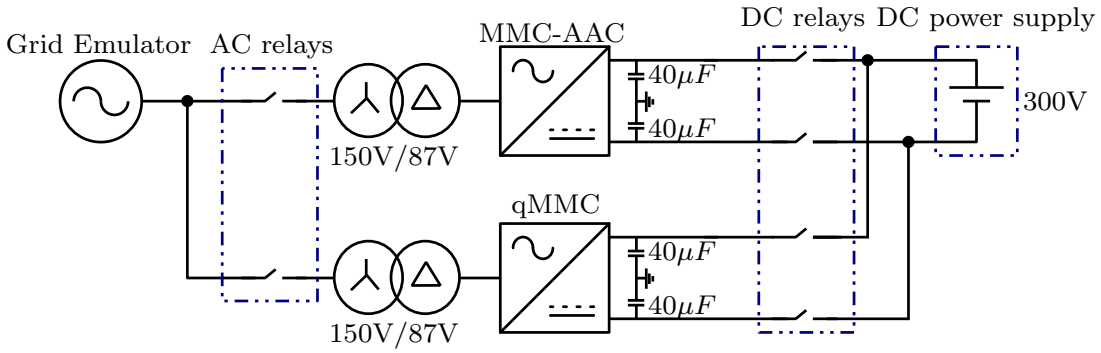
6.5.1 Steady-state operation

This section demonstrates the PQ capabilities of MMC, AAC and qMMC in inverter mode under active power control. The three operation set points are the following:

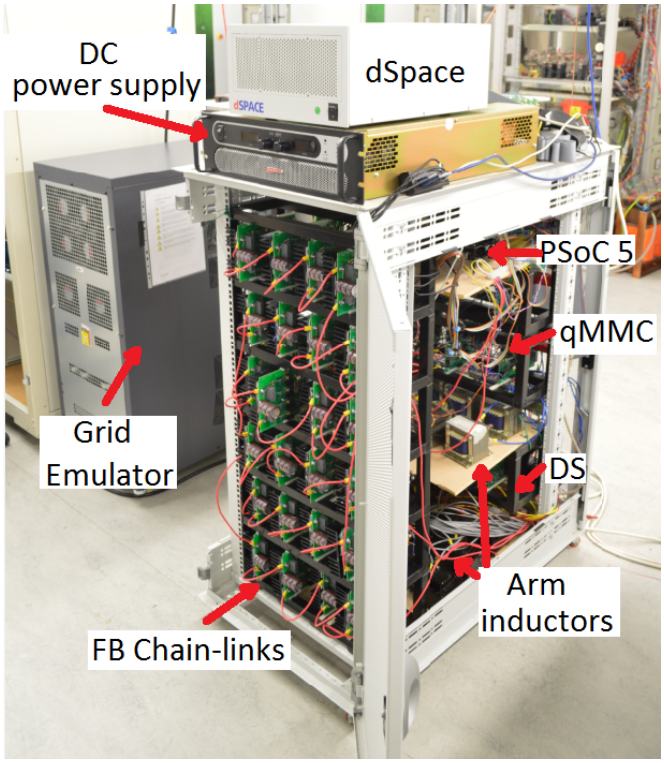
- Unity power factor with $P = 4000$ W, $Q = 0$ VAr,
- STATCOM operation with $P = 0$ W and $Q = \pm 1500$ VAr
- Cos$\phi = 0.9363$ with $P = 4000$ W and $Q = \pm 1500$ VAr

MMC

The full PQ MMC inverter operation is demonstrated in Fig.6.12. The converter successfully operate for a variate of operational set-points with active and reactive power ramp rates of 2 $\frac{p.u.}{s}$. The stiff DC power supply contain a high value capacitor resulting in limited development of the DC voltage phenomena, as shown in Fig. 6.12(b). Due to the reduced number of cells the DC current has a high magnitude ripple. However, by installing a 2.8 mH DC reactor the ripple is reduced, as shown in Fig. 6.12(c).

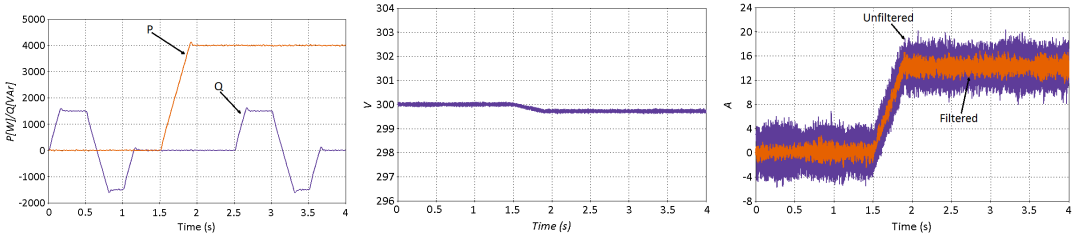


(a) Line diagram



(b) Test rig enclosure

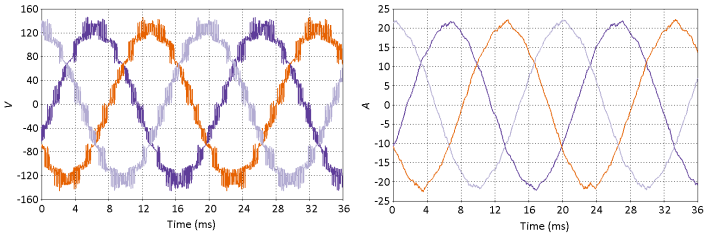
Figure 6.11: Reduced scale test-rig configuration.



(a) MMC (b) DC voltage (c) DC currents

Figure 6.12: Experimental results of MMC dynamic operation

Fig. 6.13 show a sample of the converter AC voltages and currents during unity power factor operation. The AC voltages contain the 2.5 kHz component of the PWM and eight distinguished voltage levels. Due to the reduced total AC inductance the AC currents exhibit a mild distortion.



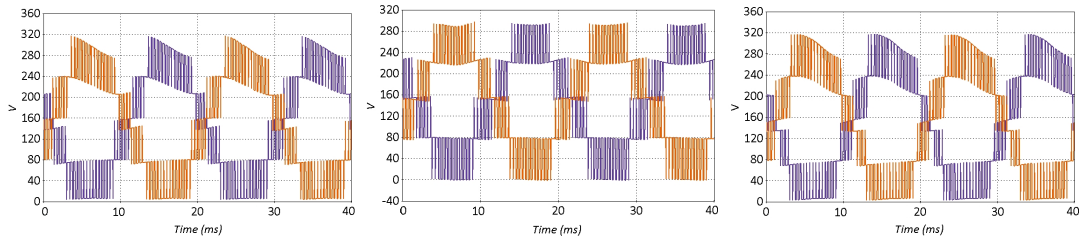
(a) AC converter voltages (b) AC converter currents

Figure 6.13: Experimental results of AC MMC voltages and currents during steady-state

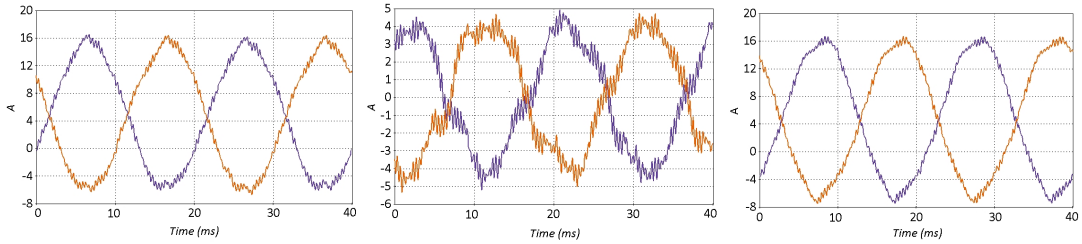
The full PQ MMC inverter operation of the MMC during unity power factor is shown in the left column of Fig. 6.14. Arm voltages operate in 2.5 kHz and there are four distinct voltage levels, while on the upper voltage level there is a slight voltage variation due to the cell capacitor ripple. The arm currents exhibit a high frequency distortion due to the low number of cells per arm and the high frequency operation of the arm voltages. In addition, the low number of cells and the switching frequency of 2.5 kHz are insufficient to enable effective employment of the circulating current suppressing controller which results in the appearance of low magnitude low frequency harmonics. The total cell capacitor voltage exhibits a 2nd order harmonic during unity power factor operation and reduced voltage ripple of $\pm 8\%$.

The inverter operation of the MMC during STATCOM operation is shown in the middle column of Fig. 6.14. The arm voltages do not appear to contain a voltage gradient, due to the fact that the cell capacitor voltages do not contain a second order harmonic. Due to the reduced current flowing through the arms, compared to the unity power factor case, the high and low frequency components have relatively higher amplitude. The total cell capacitor voltage appears to contain only the fundamental 50 Hz frequency component while the cell capacitor voltage ripple appears to be in the range of $\pm 5\%$ due to the reduced apparent power.

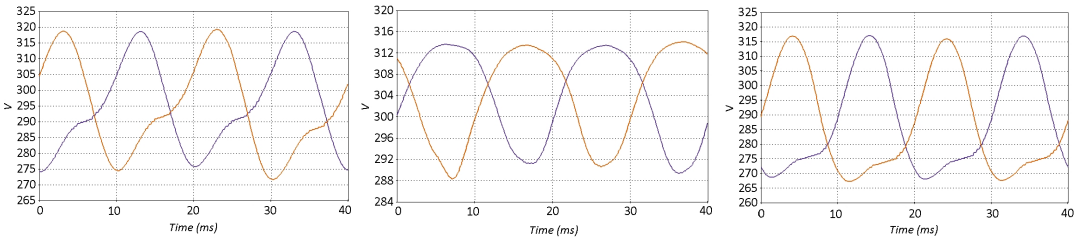
The inverter operation of the MMC during power factor $\cos\phi$=0.9363 operation is shown in the right column of Fig. 6.14. The arm voltages and current profiles are similar to the unity power factor operation case. The total cell capacitor voltages have increased voltage ripple with embedded 1st and 2nd order



(a) Arm voltages (b) Arm voltages (c) Arm voltages



(d) Arm currents (e) Arm currents (f) Arm currents



(g) Total cell capacitor voltages (h) Total cell capacitor voltages (i) Total cell capacitor voltages

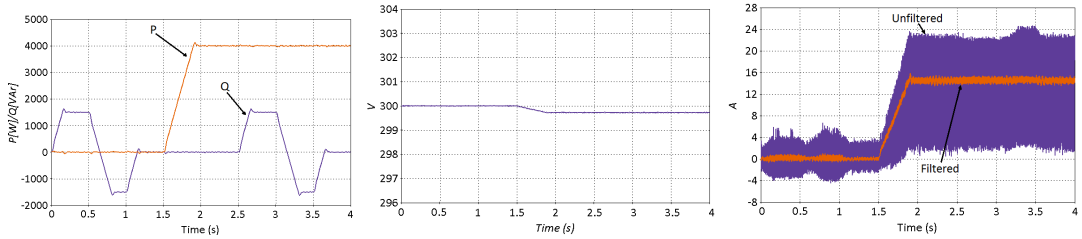
Figure 6.14: MMC steady-state experimental results: cosϕ = 1 (left column), STATCOM (middle column), cosϕ = 0.9363 (right column).

harmonics.

The experimental results show good agreement with the off-line simulation results shown in Chapter 3, thereby validating the off-line models.

AAC

The full PQ AAC inverter operation is demonstrated in Fig.6.15(a).

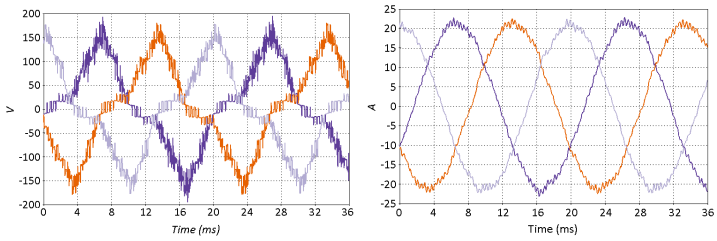


(a) MMC (b) DC voltage (c) DC currents

Figure 6.15: Experimental results of AAC dynamic operation

The converter successfully operates for a range of operational set-points with active and reactive power ramp rates of 2 $\frac{p.u.}{s}$ similar to MMC. The effect of the AAC filter($L = 2.8$ mH) is shown in Fig. 6.15(c).

Fig. 6.16 shows a sample of the converter AC voltages and currents during unity power factor operation. The AC voltages contain the 2.5 kHz component of the PWM, eight distinguished voltage levels and the 3^{rd} harmonic injection.

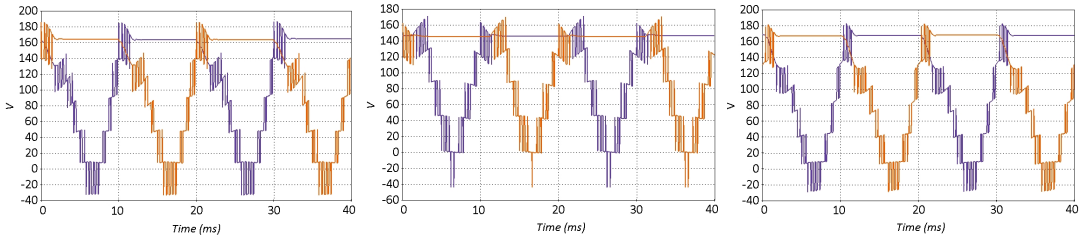


(a) AC converter voltages (b) AC converter currents

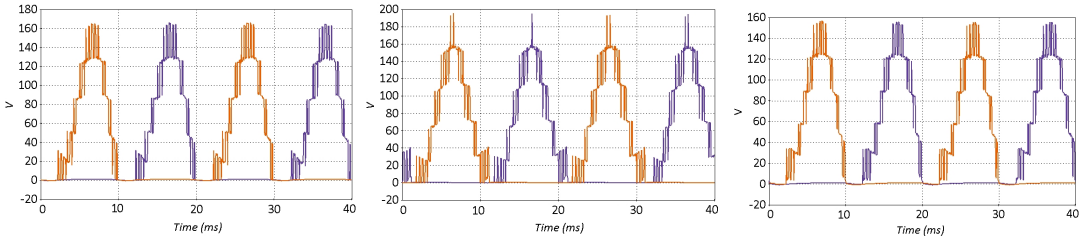
Figure 6.16: Experimental results of AC AAC voltages and currents during steady-state

The value of the AC total inductance is even smaller compared to the MMC which results in AC currents distortion increase.

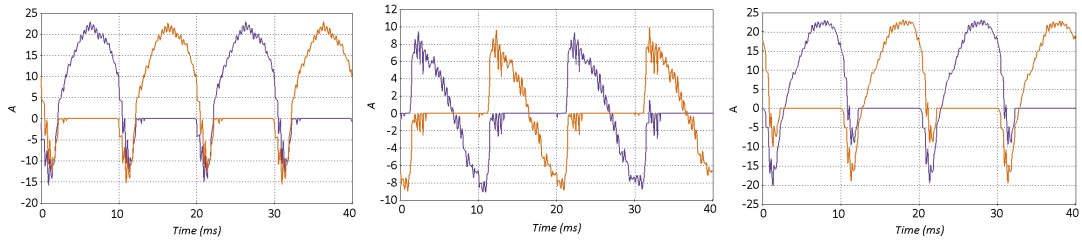
The inverter operation of the AAC during unity power factor is shown in the left column of Fig. 6.17. Arm voltages operate at 2.5 kHz, have positive arm magnitude of approximately $V_{DC}/2$, and can be over-modulated to produce negative voltage.



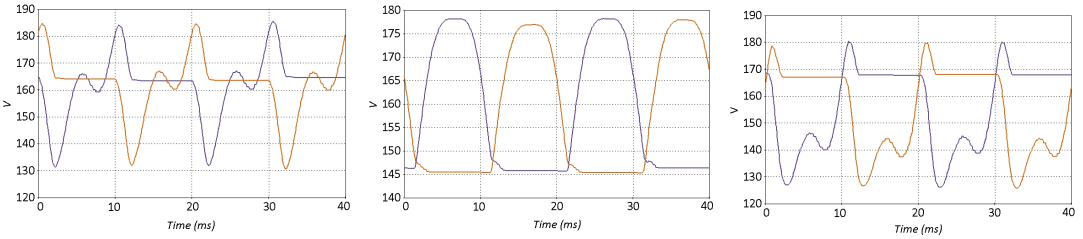
(a) Chain-link voltages (b) Chain-link voltages (c) Chain-link voltages



(d) DS voltages (e) DS voltages (f) DS voltages



(g) Arm currents (h) Arm currents (i) Arm currents



(j) Total cell capacitor voltages (k) Total cell capacitor voltages (l) Total cell capacitor voltages

Figure 6.17: AAC steady-state experimental results: cosϕ = 1 (left column), STATCOM (middle column), cosϕ = 0.9363 (right column).

The experimental test-rig requires larger inductors due to the reduced number of cells and limited switching frequency. This inductance value is larger than that used in simulation studies which represents a realistic fully-rated AAC. The effect of these larger arm inductors can be seen in the chain-link voltages of Fig. 6.17 where, although the DS voltage magnitude is agreement with the chain-link voltage, an asymmetry is introduced. The arm currents exhibit high frequency

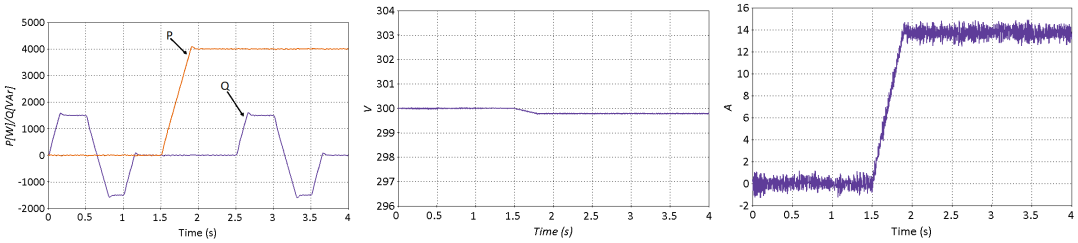
components while the peak values are higher than those seen in a MMC. The total capacitor voltages illustrate the discontinuous current and overlap operation of the converter, as was shown in Chapter 4.

The inverter operation of the AAC during STATCOM operation is shown in the middle column of Fig. 6.17. The arm and DS voltages have similar profiles to those during unity power factor operation. The arm currents are phase shifted with respect to the arm voltage illustrating reactive power flow. The total capacitor voltage ripple is reduced and exhibits a profile which includes a 50Hz component and which illustrates the arm current discontinuity.

The inverter operation of the AAC at power factor cosϕ=0.9363 is shown in the right column of Fig. 6.17. Arm and DS voltages are similar to the unity power case. The arm currents experience higher overshoot during overlap operation. The total cell capacitor voltages, have an increased voltage ripple due to the increase of the apparent power. These results are in a general good agreement with those of the off-line AAC simulation shown in Chapter 4.

qMMC

The full PQ qMMC inverter operation is demonstrated in Fig.6.18(a).

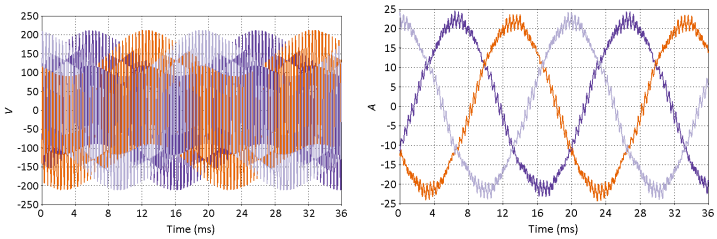


(a) MMC (b) DC voltage (c) DC currents

Figure 6.18: Experimental results of qMMC dynamic operation

The converter successfully operates for a range of operational set-points with active and reactive power ramp rates of 2 $\frac{p.u.}{s}$ similar to MMC and AAC. Due to the complementary operation of the arms the current ripple is reduced and DC filter is not required, as is shown in Fig. 6.18(c).

Fig. 6.19 shows a sample of the converter AC voltages and currents during unity power factor operation.



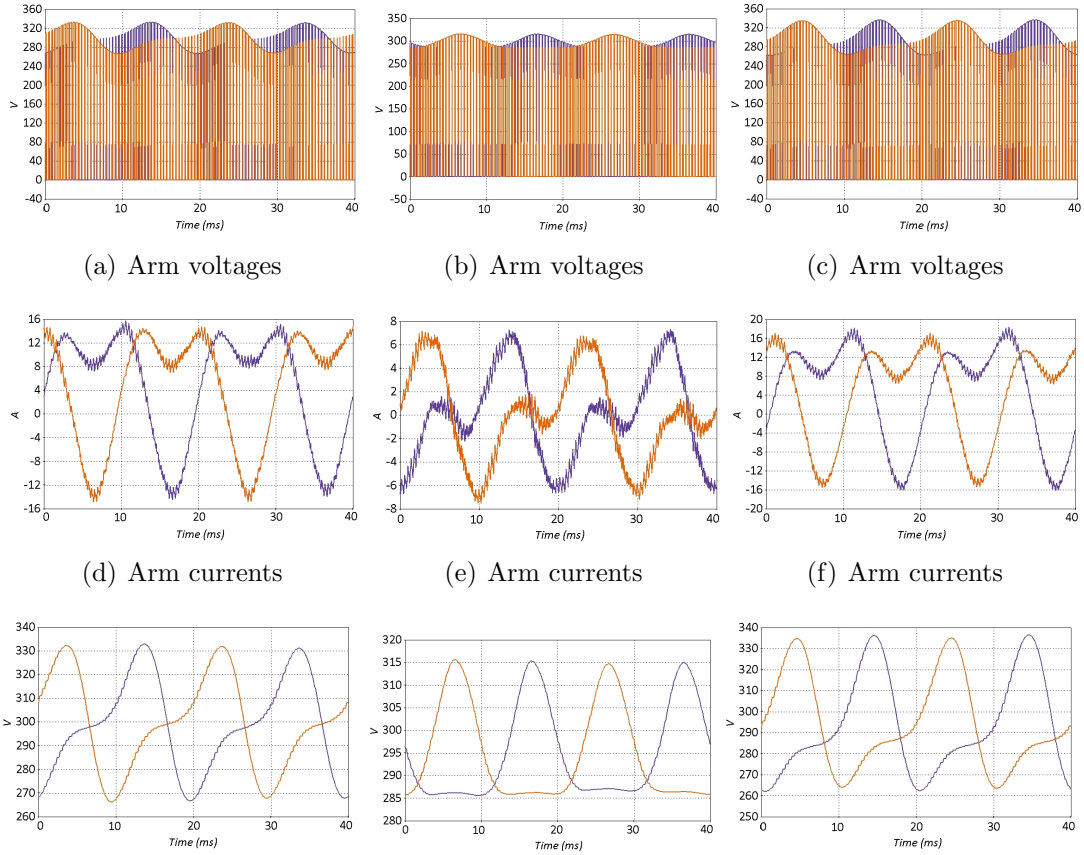
(a) AC converter voltages (b) AC converter currents

Figure 6.19: Experimental results of AC qMMC voltages and currents during steady-state

The AC voltages contain the 2.5 kHz component of PWM, and only two voltage levels exhibiting a voltage fluctuation due to the cell capacitor, as shown in Fig. 6.19(a). Due to the reduced total AC inductance and the two-level AC voltage operation, the AC converter currents exhibit high value distortion.

The inverter operation of the qMMC during unity power factor operation is shown in Fig. 6.20. The arm voltages operate in a two-level voltage manner at a frequency of 2.5 kHz, with a voltage fluctuation due to the cell capacitors. The arm voltages operate in a complementary mode, thus the circulating currents cannot be controlled, where a 2nd harmonic is embedded. In addition, due to the absence of high-frequency passive filters on the AC side of the converter, and the relatively small combined arm and transformer inductance, the AC currents contain high-frequency harmonics. The cell capacitor voltages have a similar profile to those of an MMC, but increased voltage ripple due to the absence of a circulating current controller. The qMMC is able to emulate the operation of an actual MMC, with respect to the internal cell voltage and arm current profile. The hardware results align well with the simulation results.

The inverter operation of the qMMC during STATCOM operation is shown in the middle column of Fig. 6.20. The arm currents include a 2nd order harmonic component and phase shifted relative to the arm voltages, illustrating the generation of reactive power. In addition, the arm currents do not have any DC offset as zero active power is transferred. High-frequency voltage and current components still exist in the AC grid voltages and converter currents.



(a) Arm voltages (b) Arm voltages (c) Arm voltages

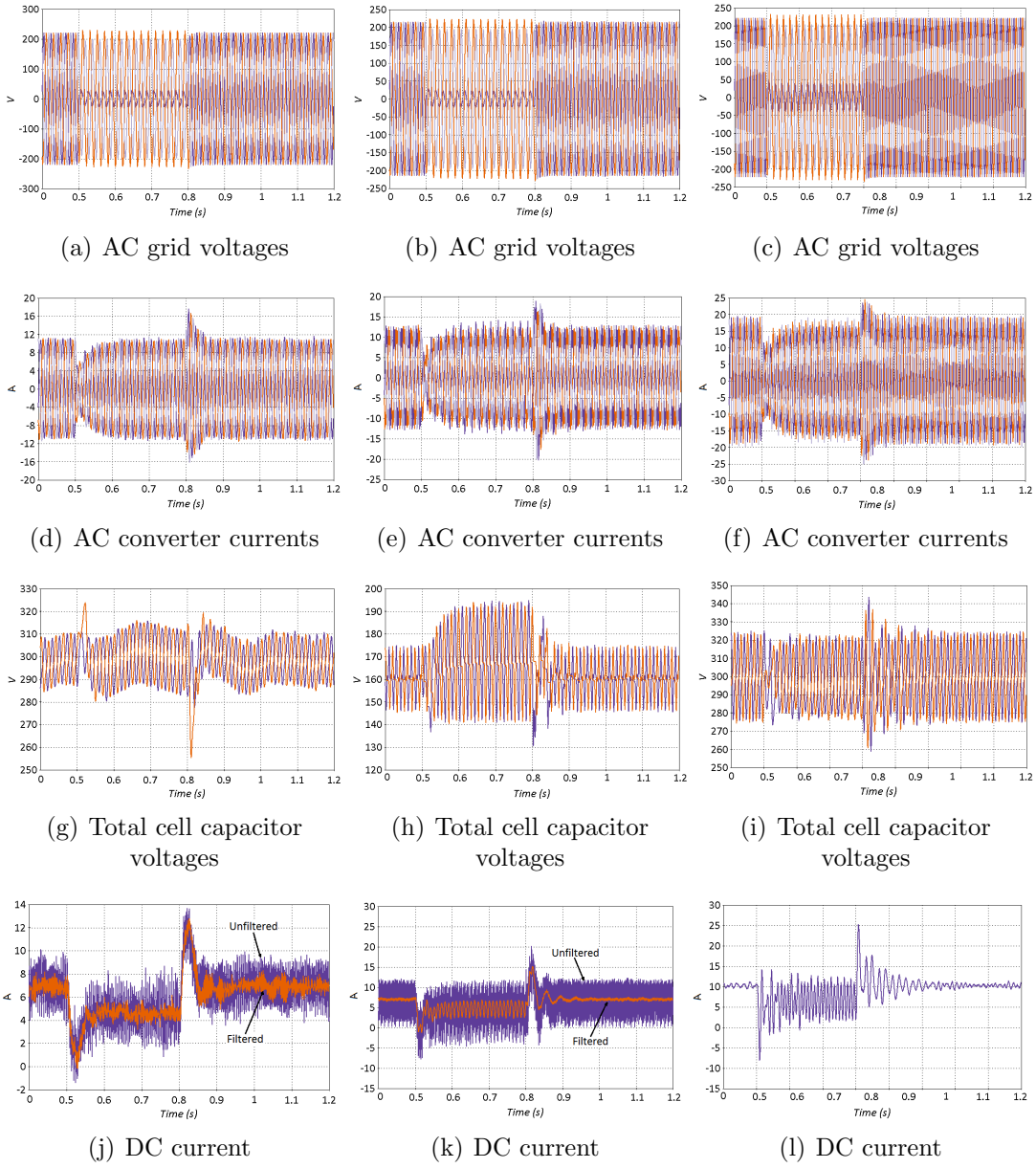
(d) Arm currents (e) Arm currents (f) Arm currents

(g) Total cell capacitor voltages (h) Total cell capacitor voltages (i) Total cell capacitor voltages

Figure 6.20: qMMC steady-state experimental results: $cos\phi$=1 (left column), STATCOM (middle column), $cos\phi$=0.9363 (right column).

6.5.2 AC unbalanced operation

The AC unbalanced operation of MMC, AAC and qMMC is shown in Fig. 6.21, which shows the effects of subjecting each converter to a severe phase-to-ground fault. In each converter, the positive-negative sequence current controller balances the AC currents. During the fault the power reference is actively adjusted in order to reduce the AC currents magnitude to their rated values. When the fault is cleared the power reference is returned to its nominal value. The current undershoot and overshoot are due to the controller delayed reaction. It can be observed that for the MMC and qMMC the total cell capacitor voltage exhibits increased voltage ripple at the beginning of the fault and that it reduces as the power reference is adjusted. However, in the AAC the total cell capacitor voltage ripple is high even with the reduced power reference. The MMC DC



(a) AC grid voltages (b) AC grid voltages (c) AC grid voltages

(d) AC converter currents (e) AC converter currents (f) AC converter currents

(g) Total cell capacitor voltages (h) Total cell capacitor voltages (i) Total cell capacitor voltages

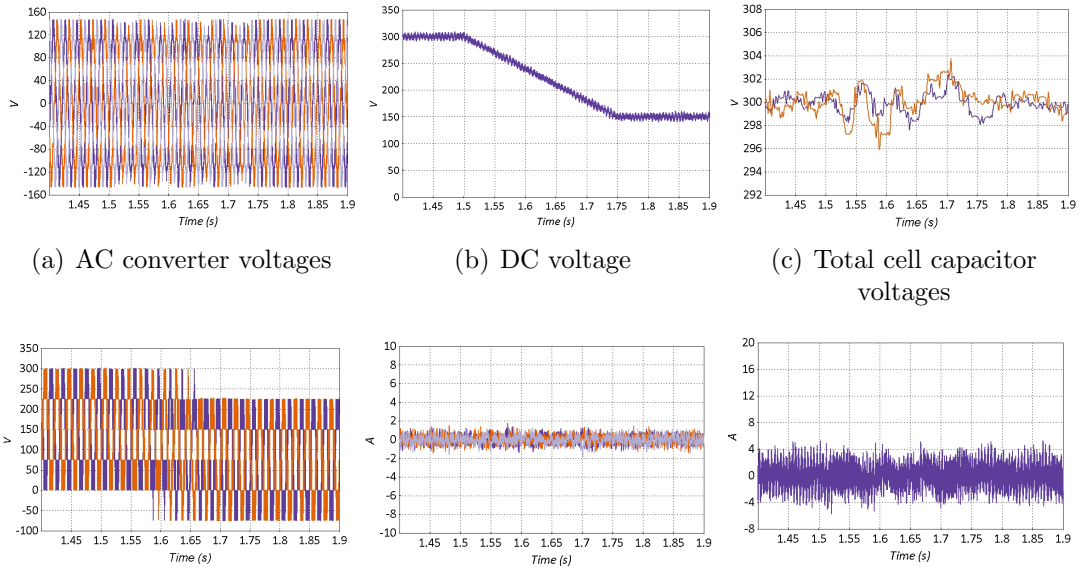
(j) DC current (k) DC current (l) DC current

Figure 6.21: Experimental results on AC unbalanced operation: MMC (left column), AAC (middle column), qMMC (right column).

current maintains the same ripple magnitude throughout the fault, due to the PR circulating current suppressing controller. Due to the absence of a circulating current suppressing controller in the qMMC and AAC, the DC current experience high ripple. These experimental results show good agreement with the off-line simulations presented in Chapter 5.

6.5.3 Reduced DC voltage operation

The inverter operation of the MMC during reduced DC voltage conditions is shown in Fig. 6.22. The DC power supply voltage reference is set to half of the nominal value, and is reduced with a slope of 2 p.u./s. This ramp rate is limited by the capabilities of the DC power supply. The arm voltages, which are initially positive, are modulated to produce both positive and negative voltage levels. The cell capacitor voltages experience only a small fluctuation. The AC and DC currents remain zero, without experiencing any overcurrent during the transition. The AC grid voltages do not experience any overvoltage during reduced DC voltage operation. This aligns well the with the off-line simulations shown in Chapter 4 and 5. Although it was not possible to validate DC fault pole-to-ground faults experimentally due limitations of the hardware, the fact that the experimental converter was shown to be able to operate at reduced DC voltage, which is a fundamental requirement in the management of DC pole-to-ground faults, provides a degree of confidence in the ability of the converter and controller to provide FRT during DC pole-to-ground DC faults.



(a) AC converter voltages (b) DC voltage (c) Total cell capacitor voltages

(d) Arm voltages (e) AC converter currents (f) DC current

Figure 6.22: Experimental results on MMC reduced DC voltage operation.

6.6 Summary

This chapter describes the design, development and implementation of a reduced scale test-rig for multilevel VSC controller and topology validation. Two three-phase 4 kW converters are developed: a four-cell FB-MMC which operates in both MMC and AAC modes, and an experimental qMMC which emulates the operation of an MMC and which is useful for system level studies. The converters are tested in inverter mode under different illustrative PQ demand conditions, and during unbalanced AC faults. In addition, the FB-MMC is tested during reduced DC voltage operation. A key aspect of the experimental system design is the realisation of a multifunctional experimental FB cell which can be operated as FB cell, an HB cell or a DS, and which enables implementation and validation of all the converters described and simulated in Chapter 4, 5 and 7.

Thermal analysis of the FB cell is validated under full-load conditions, by using a thermal imaging camera, which shows acceptable temperatures. The calculated total efficiency of the converter shows that for reduced scale experimental prototype, the passive components make a significant contribution to the total thermal losses. In general, complexity and reliability are traded off against cost and efficiency.

An asynchronous control architecture is incorporated, which is realised using a combination of low-cost microprocessors (PSoC 5) and a controller prototyping platform (dSpace) to distribute the processing effort and reduce the total cost. The dSpace system is responsible for the upper level control of the MMC, AAC and qMMC. Each phase incorporates a dedicated PSoC 5 for handling the lower level control. The asynchronous architecture offers a simple implementation and still enables the experimental test-rig to operate correctly.

The MMC and AAC test-rig results show good agreement with the off-line simulations results shown in Chapters 4 and 5. Experimental tests show that the qMMC can provide acceptable emulation of the MMC and provide a good alternative for system-level hardware studies.

Chapter 7

Enhanced and improved multilevel Converters

7.1 Introduction

This chapter presents two new converters based on MMC and AAC topologies.

The first topology is based on MMC topology which offers a high number of voltage levels with a reduced number of cells when compared to established MMC topologies. The novel MMC exhibits a new unique multiplication feature where the number of voltage levels per arm is approximately equal to the product of the numbers of HB and FB cells, whilst the output voltage step amplitude is equal to that of the FB cell voltage. These characteristics contribute to significant improvement in the quality of the AC and DC side waveforms generated by the proposed MMC. The proposed topology utilises both HB and FB chain-links in its arms, where the HB chain-link is rated for full DC-link voltage. Each HB cell is rated for medium voltage and, therefore, requires series-connected devices. It is used to synthesise an approximation to the fundamental sinusoidal output voltage with large voltage steps. The FB chain-link, with total blocking voltage equivalent to half of that of an HB cell, is used to generate additional voltage levels with small voltage steps to smooth the transitions between the large voltage steps generated by the HB cells so that the MMC provides high-quality sinusoidal output. In this way, the proposed MMC has the potential to eliminate both AC and DC side filters despite having a reduced number of cells. Detailed comparisons with existing MMC topologies show that the proposed MMC offers better design trade-offs in terms of superior AC and DC waveforms with reduced control and power circuit complexity. The validity of the proposed MMC is confirmed using simulation and experimentation.

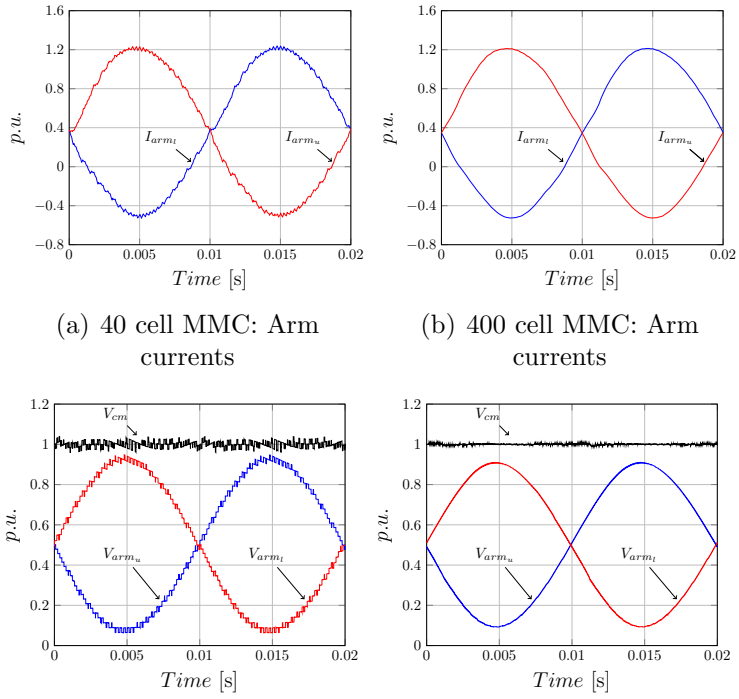
The second topology is based on AAC topology where the DS of the upper and

lower arms of the conventional AAC are rearranged as a conventional two-level converter. The flying capacitor (i.e. the capacitor across the DS) in each phase leg facilitates seamless current commutation between the upper and lower arms, and eliminates the need for the main DC link capacitor across the positive and negative DC rails. The modifications introduced to the power circuit require the proposed converter to adopt a new operating regime that ensures simultaneous conduction of the upper and lower arms of each phase leg as in the MMC. The operating principle, modulation methods of the proposed converter, and sizing of its main components are described in detail, and substantiated by simulations.

7.2 Enhanced multilevel modular converter

7.2.1 Motivation

In general, the MMC synthesises AC voltage by inserting and bypassing cells in the upper and lower arms such that the blocking voltage of the inserted cells in both arms is slightly larger or smaller than the imposed DC link voltage [101]. In MMC with large numbers of cells per arm, where each cell is rated for a small voltage ranging from 1.6-3 kV, the nearest NLC scheme synthesises high quality AC and DC side waveforms. In contrast, in MMC with relatively small numbers of cells per arm, where the rated voltage per cell ranges from 15-20 kV, PWM is widely used to facilitate the accurate synthesis of the output AC and DC voltages. Future advances in SiC devices may allow single IGBTs to be rated up to 12.5 kV [102], and could result in cells with higher rated voltage. The use of series-connected switching devices in the high voltage cells of an MMC with a reduced number of cells (e.g. 40 for a 640 kV HVDC converter) introduces significant errors to the output AC and the cm voltages of the three MMC legs and high-frequency components in the arm currents as shown in Fig. 7.1(a) and 7.1(b).



(a) 40 cell MMC: Arm currents

(b) 400 cell MMC: Arm currents

(c) 40 cell MMC : Common-mode voltage, Arm voltages

(d) 400 cell MMC : Common-mode voltage, Arm voltages

Figure 7.1: Internal voltage and current comparison of 40 and 400 cell MMC (P: 1000 MW, V_{DC}: 640 kV, L_{arm}: 0.05 p.u.).

To satisfy the harmonic requirements specified by the grid code [103], an AC filter is required to reject the high-frequency PWM harmonics. A DC filter is required to remove the voltage mismatch that may cause ripple resulting from transitions between the different voltages, as depicted in Fig. 7.1(c). Under fast-acting current interruption, i.e. DCCBs with operating times in the range 2-5 ms, over-sizing of the arm inductors is unnecessary [104]. Increased voltage error due to the use of large switching voltages increases the magnitudes of the high-frequency currents and voltages to be injected into the DC side. Relatively large arm inductors are therefore required to suppress the high-frequency components of the circulating currents. Thus, an increased number of levels with smaller switching voltages improves the power quality of the AC and DC side waveforms, as well as the arm waveforms, and eliminates or minimises passive filtering requirements.

It should be emphasised that DC fault blocking is not one of the motivations behind the proposed MMC, especially as the maximum negative voltage its FB chain-link produces is negligible and insufficient to facilitate DC fault blocking.

Instead, the proposed MMC is an enhancement to improve the quality of the AC and DC side waveforms, for HB or FB MMCs that employ medium-voltage cells predominantly.

7.2.2 Proposed EMMC

The proposed topology may be considered as an enhancement of the basic MMC since the fundamental operating principle is retained. Each arm of this EMMC as shown in Fig. 7.2, consists of two types of chain-link: the HB chain-link and the FB chain-link.

The total blocking voltage of each of the upper and lower HB chain-links is equal to the full DC voltage. To support this voltage, series-connected IGBTs may be required in the HB cells, as shown in Fig. 7.2. The total blocking voltage of the FB chain-link is equivalent to half the rated voltage of an HB cell. The HB and FB cell voltages are described as:

$$V_{cell-hb} = \frac{V_{DC}}{N_{hb}} \tag{7.1}$$

where $V_{cell-hb}$ is the voltage across an HB cell, N_{hb} is the number of cells in the

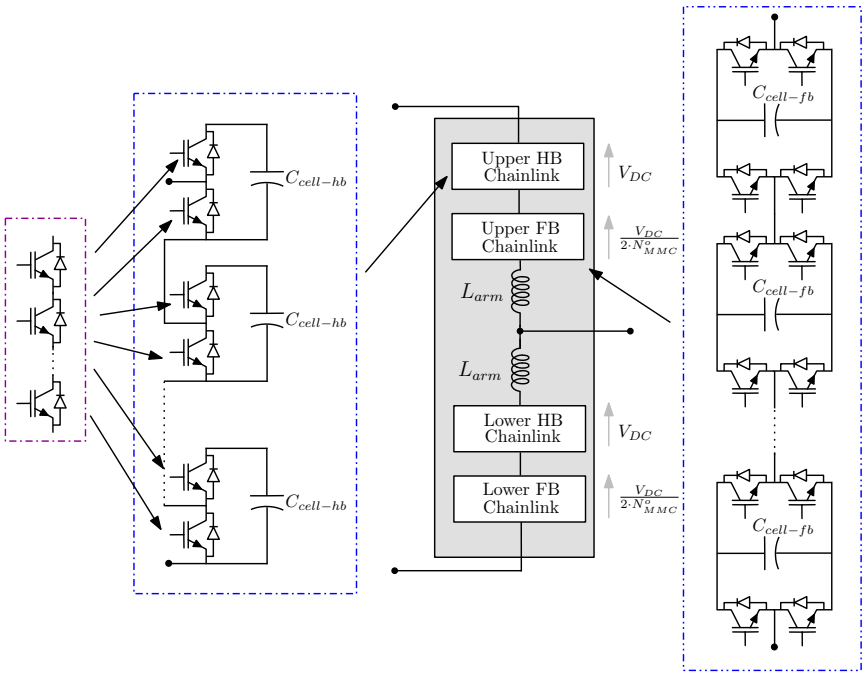


Figure 7.2: Phase representation of EMMC topology.

HB chain-link, and V_{DC} is the pole-to-pole DC voltage, and

$$V_{cell-fb} = \frac{V_{cell-hb}}{2N_{fb}} \tag{7.2}$$

where $V_{cell-fb}$ is the voltage across an FB cell and N_{fb} is the number of cells in the FB chain-link of each arm. Each arm will have a total number of cells N, defined in (7.3).

$$N = N_{hb} + N_{fb} \tag{7.3}$$

When compared to a conventional MMC where the number of levels is given by (7.4), the unique multiplication property of the EMMC offers an increased number of voltage levels given by (7.5), with each converter having the same number of cells as given in (7.3).

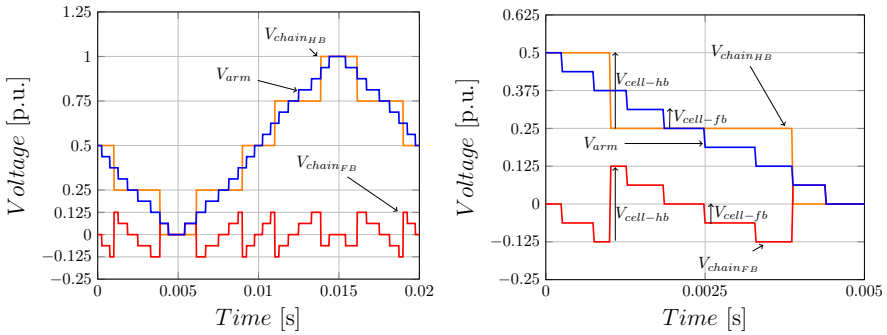
$$N^o_{MMC} = N + 1 \tag{7.4}$$

where N^o_{MMC} and N^o_{EMMC} represent the numbers voltage levels per arm in the conventional MMC and the EMMC respectively.

$$N^o_{EMMC} = 2N_{hb} \cdot N_{fb} + 1 \tag{7.5}$$

Fig. 7.3 depicts the ideal synthesis of the total arm voltage and voltages of the HB and FB chain-links, assuming an illustrative EMMC with 4 HB cells and 2 FB cells per arm, with all voltages being normalized to DC voltage V_{DC}. Fig. 7.3(a) shows that the HB chain-link of each EMMC arm synthesizes a stepped approximation of the sinusoidal fundamental voltage $V_{chain_{hb}}$ with a major voltage step equal to 0.25p.u. ($V_{cell-hb} = \frac{1}{4}V_{DC} = \frac{V_{DC}}{N_{hb}}$), whilst the FB chain-link of each arm synthesizes a bipolar voltage $V_{chain_{fb}}$ with positive and negative peaks of $\pm 0.125 p.u.$ ($\pm\frac{1}{2} \cdot \frac{1}{4}V_{DC} = \pm\frac{1}{8}V_{DC} = \pm\frac{V_{DC}}{2N_{hb}} = \frac{1}{2}V_{cell-hb}$) and minor a voltage step of $\frac{0.125}{2} p.u.$ ($\frac{1}{2} \cdot \frac{1}{8}V_{DC} = \frac{1}{16}V_{DC} = \pm\frac{V_{DC}}{2N_{fb}} \cdot N_{hb} = \frac{V_{cell-hb}}{2N_{fb}}$). Observe that the total arm voltage V_{arm} is the algebraic sum of the voltages $V_{chain_{hb}}$ and $V_{chain_{fb}}$, synthesized by the HB and FB chain-links respectively. The V_{arm} inherent a minor voltage step, equal to a single FB cell ($\frac{V_{dc}}{2N_{hb}N_{fb}} = \frac{V_{cell-hb}}{2N_{fb}}$). The positive and negative peaks of $V_{chain_{fb}}$ in each arm are limited to $\pm\frac{1}{2}V_{cell-hb}$, which suggests that the minimum blocking voltage of the FB chain-link is $\frac{1}{2}V_{cell-hb}$. Based on Fig. 7.3, the illustrative EMMC consisting of 4 HB and 2 FB cells can generate 17 discrete voltage levels in each arm. The arm voltage level genereation can be expressed generically as $2N_{fb}N_{hb} + 1$.

The HB cell capacitance may be expressed in terms of the arm equivalent



(a) Generated voltage waveforms (b) Focused generated voltage waveforms

Figure 7.3: The internal synthesized voltages of EMMC.

capacitance $C_{cell-tot}$ as

$$C_{cell-hb} = C_{arm-tot} \cdot N_{hb} \tag{7.6}$$

where $C_{cell-hb}$ is the cell capacitance for the HB chain-link. Similarly, the cell capacitance $C_{cell-fb}$ for the FB cell is expressed in terms of HB cell capacitance $C_{cell-hb}$ and the number of FB cells N_{fb} as

$$C_{cell-fb} = C_{cell-hb} \cdot \frac{N_{fb}}{2} \tag{7.7}$$

The total capacitance of the FB chain-link is equal to half the total HB cell capacitance. This is achieved by increasing the FB cell capacitance as described by (7.7). In the industry, cell capacitor sizing is based on stored energy criteria and considers volume and capacitor voltage ripple. Values in the range 30-40kJ/MW are commonly considered and (7.6) and (7.7) guarantee that the cell capacitor voltage ripple will not exceed 10%, which is a commonly used design value in conventional MMC [77]. It should be noted that the FB cells in the EMMC are not intended to facilitate DC fault blocking or reduced DC link operation, and that the proposed concept of incorporating FB chain-links with minor voltage steps could be extended to other MMC variants, such as the MC and FB-MMC.

Operating principle

The operating principle of the EMMC is illustrated in Fig. 7.4.

The EMMC uses the HB chain-link rated at full pole-to-pole DC voltage to synthesise the fundamental voltage with major voltage steps, $\frac{V_{DC}}{N_{hb}}$, as shown in Fig. 7.4(a). The FB chain-link, with combined blocking voltage equivalent to half that of an HB cell $V_{cell-hb}$, acts as an active power filter (APF) and

generates a multilevel waveform with minor voltage steps of $\frac{V_{DC}}{2 \cdot N_{hb} \cdot N_{fb}}$. Thus, the FB chain-link a facilitates smooth transition between the major voltage levels through intermediate voltage levels separated by minor voltage steps. Since the HB chain-link synthesises the fundamental component of the arm voltage, the continuous modulating signal m_{hb} is used to estimate the number of HB cells to be inserted and bypassed in each arm on a discrete basis, as shown in Fig. 7.4(a). Equally, the FB chain-link is required to inject voltage harmonics into each arm. Thus the modulating signal of the FB chain-link is extracted as an error between the target fundamental voltage and its switched equivalent, as shown in Fig. 7.4(b). The modulating signals for the HB and FB chain-links are:

$$m_{hb} = M \cdot \cos(\omega t + \delta) \tag{7.8}$$

$$m_{hb_{NLM}} = \text{round}(m_{hb} \cdot N_{hb}) \tag{7.9}$$

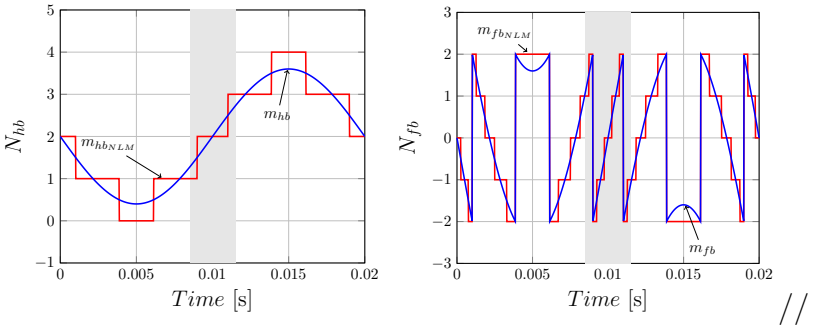
$$m_{fb} = m_{hb} \cdot N_{hb} - m_{hb_{NLM}} \tag{7.10}$$

$$m_{fb_{NLM}} = \text{round}(m_{fb} \cdot N_{fb}) \tag{7.11}$$

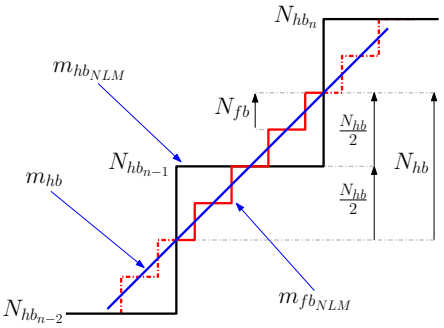
where M represents modulation index amplitude. Equations (7.8)-(7.11) show that the FB and HB cell modulation indices are created from the same reference. Fig. 7.4 shows that the HB chain link in each arm generates a staircase voltage with $N_{hb}+1$ levels, with a pre-defined major voltage step defined in (7.1) between two consecutive voltage levels. In contrast, the FB chain link in each arm generates a bipolar voltage consisting of $2N_{fb}+1$ levels with step voltage of $V_{cell-fb}$ defined in (7.2). The FB cells are switched to produce positive and negative output voltage steps around an artificial zero voltage level that is synchronised with the edges of $m_{hb_{NLM}}$. Fig. 7.4(c) shows the ideal modulating signals of the HB and FB chain-links normalised for the synthesis of the minor voltage levels between two successive major voltage levels. Conventional capacitor voltage balancing techniques, such as the sorting, tolerance band and cell reference modulation methods, can be applied to both EMMC chain-links [105, 106, 107, 108].

Converter analysis

In the following analysis, subscript j defines the phase index (i.e. $j = a, b, c$) and subscript k defines the upper and lower position of the arm (i.e. $k = u$ for the upper arm and $k = l$ for the lower arm). The FB and HB cell capacitor currents



(a) HB chain-link modulation (b) FB chain-link modulation



(c) Combined illustration of arm modulation signals

Figure 7.4: Illustrative EMMC modulation signals with $N_{hb} = 4$ and $N_{fb} = 2$.

can be described in terms of arm currents and their switching functions as

$$m_{hb} \cong \sum_{i=1}^{N_{hb}} \left[S_{cell-hb_{N_{hb},j,k}} \right] \tag{7.12}$$

$$m_{fb} \cong \sum_{i=1}^{N_{fb}} \left[S_{cell-fb_{N_{fb},j,k}} \right] \tag{7.13}$$

$$i_{cell-hb_{N_{hb},j,k}} = s_{cell-hb_{N_{hb},j,k}} \cdot i_{j,k} \tag{7.14}$$

$$i_{cell-fb_{N_{fb},j,k}} = s_{cell-fb_{N_{fb},j,k}} \cdot i_{j,k} \tag{7.15}$$

Each arm voltage $v_{arm_{j,k}}$ is formed by the summation of individual cell voltages $v_{cell-hb_{N_{hb}j,k}}(t)$ and $v_{cell-fb_{N_{fb}j,k}}(t)$ as described in (7.19).

$$v_{cell-hb_{N_{hb},j,k}}(t) = \frac{1}{C_{cell-hb}} \cdot \int \left(i_{cell-hb_{N_{hb},j,k}}(\tau) \right) d\tau \tag{7.16}$$

$$v_{cell-fb_{N_{fb},j,k}}(t) = \frac{1}{C_{cell-fb}} \cdot \int \left(i_{cell-fb_{N_{fb},j,k}}(\tau) \right) d\tau \tag{7.17}$$

$$\begin{aligned} v_{arm_{j,k}} = & \sum_{y=1}^{N_{hb}} \left[s_{cell-hb_{N_{hb},j,k}} \cdot v_{cell-hb_{N_{hb}},j,k} \right] \\ & + \sum_{y=1}^{N_{fb}} \left[s_{cell-fb_{N_{fb},j,k}} \cdot v_{cell-fb_{N_{fb},j,k}} \right] \end{aligned} \tag{7.18}$$

$$v_{arm_{j,k}} = m_{hb} \cdot V_{c_{tot-hb}} + m_{fb} \cdot V_{c_{tot-fb}} \tag{7.19}$$

The instantaneous cm voltage the MMC phase legs present at its DC terminals can be expressed in terms of the instantaneous upper and lower arm voltages ($v_{arm_{j,u}}$,$v_{arm_{j,l}}$) as

$$V_{cm} = v_{arm_{j,u}} + v_{arm_{j,l}} = V_{DC} \pm dV \tag{7.20}$$

where dV represents the DC voltage drops across the internal resistances of the arm reactors and switching devices in the upper and lower arms. Synthesis of the AC voltage, as well as the AC, common-mode and circulating currents, is similar to that in the conventional MMC [101]. Fundamentally, the necessary condition for cell capacitor voltage balancing is that the energy exchange between the cell capacitors of the HB and FB chain-links, and both chain-links with the AC side, must be zero, as described in (7.21) and (7.22).

$$E_{HB_{j,k}} = \int_0^T \left(m_{hb} \cdot i_{arm_{j,k}}(\tau) \right) d\tau = 0 \tag{7.21}$$

$$E_{FB_{j,k}} = \int_0^T \left(m_{fb} \cdot i_{arm_{j,k}}(\tau) \right) d\tau = 0 \tag{7.22}$$

It should be noted that incorporation of the very limited number of FB cells into each arm of the proposed EMMC may affect the magnitudes of the low-order characteristic harmonics and the high-frequency harmonics of the circulating currents. The DC offset of the modulating signal m_{fb} of the FB chain-link is manipulated in order to ensure that the FB chain-link exchanges zero net energy or active power with the FB chain-link and AC side.

Modulation index m_{fb} is adjusted according to the FB cell energy as described in (7.23).

$$W_{fb_{j,k}} = \frac{1}{N_{fb}} \sum_{i=1}^{N_{fb}} \frac{C_{cell-fb} \cdot v^2_{cell-fb_{N_{fb},j,k}}}{2} \tag{7.23}$$

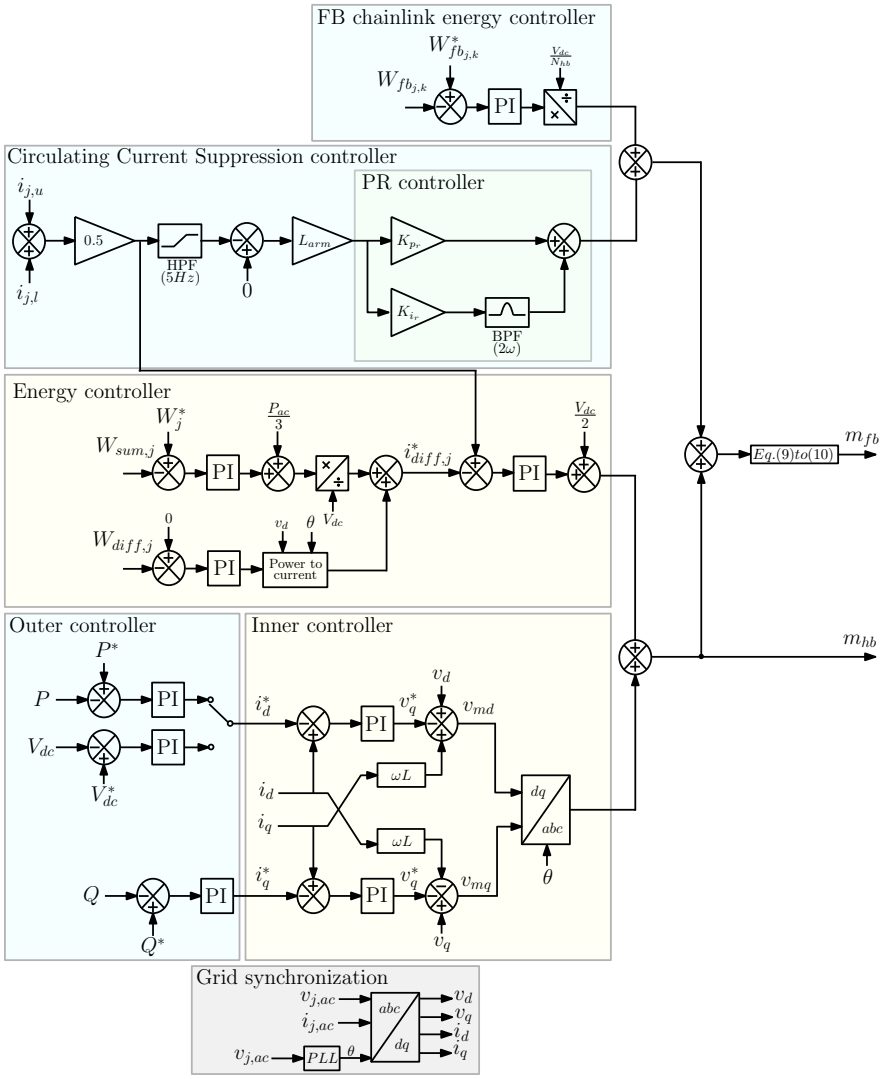


Figure 7.5: EMMC control structure.

Fig. 7.5 shows the overall controller structure of the proposed EMMC. The horizontal and vertical energy balance controllers, and the outer and inner current controllers define the modulation index for the HB chain-link. The vertical (arm balancing) controller is responsible for ensuring that the DC voltages across the upper and lower arms of all three phases are equal (zero differential voltage or energy).

The horizontal (average capacitor voltage or energy) controller is responsible for ensuring that the three phase legs have the same DC voltage to prevent DC circulating currents between the phase legs. The FB chain-link energy controller ensures that the energy stored in the upper and lower arm FB chain-links is balanced. This is achieved by injecting a small DC component into the modulation

index of the FB chain-links. Also, the CCSC modifies the FB chain-link modulation index in order to reduce the switching instances of the HB cells, and hence switching losses.

If HB cells are used in place of FB cells, the NLM algorithm must be modified accordingly, i.e. replacement of the 'round' function in (7.9) and (7.11). Additionally, twice as many HB cells will be required, leading to increased cell capacitance without any additional benefit. Also instead of the previously described DC offset manipulation, distributed capacitor voltage balancing [109] in the FB cells could be used to prevent departure of the cell voltage from its nominal value.

Modulation schemes

Table 7.1 lists a number of hybrid modulation techniques which are applicable for controlling the EMMC HB and FB chain-links. The first scheme is well-suited to the low number of HB and FB cells. Application of PWM to the HB chain-link with major voltage steps permits accurate synthesis of the fundamental voltage over the full modulation index linear range. FB cell balancing is therefore readily achievable over the full modulation range as the FB chain-links will not be forced to produce fundamental voltage (or exchange non-zero active power). This scheme is not however preferred due to the increased complexity of the implementation, difficulty in synchronising two high-frequency modulations, and switching loss concerns. By incorporating SHE, the second scheme in Table 7.1 offers similar attributes to the first scheme for low numbers of HB and FB cells, including operation over the full modulation index range. Its extension to MMC with large numbers of HB cells is, however, problematic with regard to calculation of switching angles and implementation, particularly at high modulation indices where several angles will be inseparable. The third scheme in Table 7.1 inherently has all the features of the second scheme when it is applied to MMC with large numbers of HB cells. When it is applied to MMC with reduced numbers of HB cells, its inability to accurately synthesise the required fundamental voltage during operation at low modulation indices increases the risk of voltage imbalance in the FB cells, as the FB chain-link will be required to contribute fundamental voltage. The fourth scheme is well suited for MMC with large numbers of HB and FB cells. Thus, it is able to operate over the full modulation index and power factor range.

Table 7.1: EMMC modulation schemes.

Scheme	HB Chain-link	FB Chain-link
1	PWM	PWM
2	SHE	PWM
3	NLM	PWM
4	NLM	NLM

Converter power losses

The increased semiconductor losses in the EMMC when compared to the conventional MMC are highly dependent on the relationship between the HB cell voltage and the DC link voltage. Due to FB cell operation, the additional conduction losses are equivalent to those of one HB cell and, as a result, the FB losses will be a small proportion of the total arm losses, as shown in (7.24).

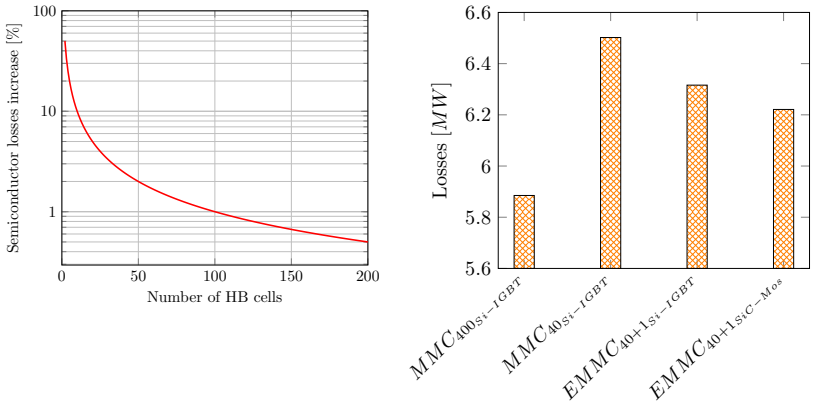
$$P_{EMMC_{cond}} = \frac{N_{hb}+1}{N_{hb}} \cdot P_{MMC_{cond}} \tag{7.24}$$

Fig. 7.6 shows the correlation between the number of HB cells and the increase in total semiconductor losses, but does not consider the potential reduction in switching and passive filter losses. As the number of HB cells increases the incremental semiconductor losses decrease.

Fig. 7.6(b) and Table 7.2 present a semiconductor loss comparison between the conventional MMC implementations (40-cell MMC and 400-cell MMC) and the EMMC. Table 7.2 and Fig. 7.6(b) display semiconductor losses for the 400-cell HB-MMC that uses silicon IGBTs ($MMC_{400_{Si-IGBT}}$), the 40-cell HB-MMC that uses silicon IGBTs ($MMC_{40_{Si-IGBT}}$), the EMMC with 40 HB cells and 5 FB cells, where both HB and FB cells employ silicon IGBTs ($EMMC_{40+1_{Si-IGBT}}$), and the EMMC with 40 HB cells and 5 FB cells, where the HB cells use Silicon IGBTs and the FB cells employ silicon carbide (SiC) MOSFETs ($EMMC_{40+1_{SiC-Mos}}$). The semiconductor losses displayed are computed from a detailed power loss model which accounts for junction temperature, IGBT and diode threshold voltages, on-state resistance, turn-on and turn-off energy, and diode recovery energy.

Fig. 7.6(b) and Table 7.2 show that the EMMC has marginally higher conduction loss compared to conventional the MMC with 40 and 400 cells per arm, when all MMCs being compared employ the same silicon IGBTs. Amongst the silicon IGBT MMCs, the 400-cell MMC exhibits the lowest switching loss, followed by the proposed EMMC, while the conventional 40-cell MMC exhibits the

highest switching loss. As a result, the overall semiconductor loss of the EMMC is slightly lower than that of the conventional 40-cell MMC, with the conventional 400-cell MMC exhibiting the lowest overall semiconductor loss. Additionally, the results in Fig. 7.6(b) and Table 7.2 show further reduction in semiconductor loss of the EMMC is possible by adopting wide-band-gap switching devices such as silicon carbide MOSFETs.



(a) (b)

Figure 7.6: (a) Semiconductor loss increase versus the number of HB cells, (b) Semiconductor loss comparison between conventional MMC and EMMC with Si-IGBTs and SiC-MOSFETs.

Table 7.2: Semiconductor loss comparison between conventional MMC and EMMC

Losses	$MMC_{400_{Si-IGBT}}$	$MMC_{40_{Si-IGBT}}$	$EMMC_{40+1_{Si-IGBT}}$	$EMMC_{40+1_{SiC-Mos}}$
Conduction [MW]	4.75	4.75	4.87	4.87
Switching [MW]	1.14	1.75	1.45	1.35
Total [MW]	5.89	6.50	6.32	6.22

Based on the basic design presented, the EMMC increases semiconductor count by 2.5%, which can be easily offset by other design considerations such as cell redundancy.

7.2.3 Topology validation

Table 7.3 shows the simulation and experimental test-rig parameters used to substantiate the viability of the EMMC. In both simulation and experimentation, the HB chain-link is controlled using NLM, whilst the FB chain-link is controlled

using high frequency PWM with 2.5 kHz level-shifted carriers (one carrier per FB cell). Both chain-links adopt sorting based capacitor voltage balance strategies. The sizing of the HB cell capacitance is derived from a scaled system with inertia of 40 kJ/MVA (equivalent to 40 ms). On a similar basis, the arm inductance is calculated to be 0.2 p.u.

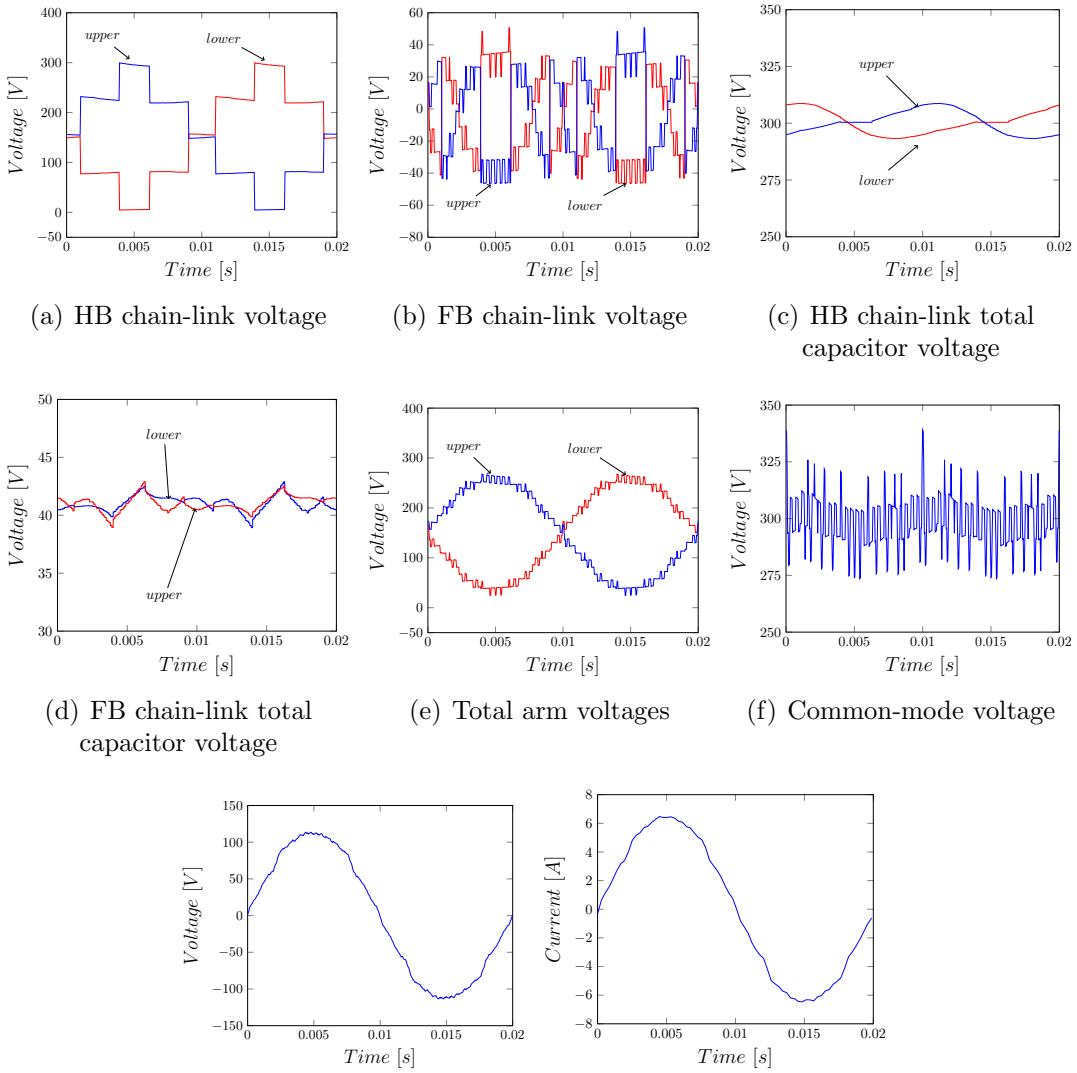
Table 7.3: EMMC specification.

Parameter	Value
V_{DC} [V]	300
R_{LOAD} [Ω]	17
N_{hb} / N_{fb}	4/4
f_S [kHz]	2.5
L_{arm} [mH]	5
C_{hb} / C_{fb} / C_f [mF]	2.2 / 4.4 / 5

Simulations

Simulation results, where one phase of the EMMC operates under open-loop control with a modulation index of 0.85 and a resistive load of 17 Ω, are shown in Fig. 7.7. Fig. 7.7(a) shows the low-frequency modulation of the HB chain-link voltage waveform using NLM, while Fig. 7.7(b) shows the high-frequency modulation of the FB chain-link using PWM as described in Section 6.3.3. It is observed that the synthesised switched voltage, which is a step approximation of a sinusoidal waveform by the FB chain-link, occupies the full DC-link voltage range of V_{DC}, whilst the FB chain-link occupies a voltage range equivalent to half that of an HB cell, and is a small fraction of V_{DC} according to (7.2). Fig. 7.7(a) to 7.7(d) indicate that the voltages across the cell capacitors of the HB and FB chain-links, and consequently the voltages across the switching devices if both chain links, are tightly regulated around the desired steady-state values. Fig. 7.7(e) shows the total upper and lower arm voltages, which are synthesised by HB chain-links comprising four HB cells each and providing large step voltage transitions, and FB chain-links which consist of four FB cells providing small step voltage transitions. It can be seen that the upper and lower arm voltages exhibit a substantial increase in the number of voltage levels, amounting to $2 \cdot N_{hb} \cdot N_{fb} + 1$ as described in Section 6.3.1. Although this illustrative simulation uses only four HB cells and four FB cells, shown in Fig. 7.7, the EMMC arm voltage accurately reflects the modulating signal of a conventional MMC with 32 cells per arm. Fig. 7.7(f) shows that the common-mode voltage (or instantaneous sum of the upper

and lower arm voltages) that the EMMC presents at its DC terminals exhibits some high-frequency content due to switching edge mismatch. Fig. 7.7(g) and Fig. 7.7(h) show that the EMMC produces high-quality sinusoidal output phase voltage and current waveforms even though it is feeding a purely resistive load.



(a) HB chain-link voltage (b) FB chain-link voltage (c) HB chain-link total capacitor voltage

(d) FB chain-link total capacitor voltage (e) Total arm voltages (f) Common-mode voltage

(g) output AC voltage (h) output AC current

Figure 7.7: EMMC simulation results.

Experimental set-up

This section presents experimental results for a prototype single phase of an EMMC, which is based on an existing four cell per arm conventional MMC test-rig that was upgraded to the EMMC topology by the addition of FB chain-links

and the necessary control system, as shown in Fig. 7.3(a). A 50 Hz sinusoidal reference (modulating) signal is generated externally and fed to Cypress Semiconductor 32-bit Arm Cortex-M3 PSoC 5LP low-power microcontroller units MCU 1 and MCU 2. MCU 1 manages NLM and capacitor balancing of the upper and lower HB chain-links, whilst MCU 2 is dedicated to high-frequency level shifted PWM (f_s=2.5 kHz) and capacitor voltage balancing of the upper and lower FB chain-links. This approach ensures that the fundamental voltage components generated by the upper and lower chain-links are synchronised and completely complementary so as to avoid any potential voltage mismatches between the arms which could be reflected in the AC and DC voltages. Moreover, the synchronisation of each arm HB and FB chain-link is achieved from the reference, and does not need internal communication or clock-synchronisation.

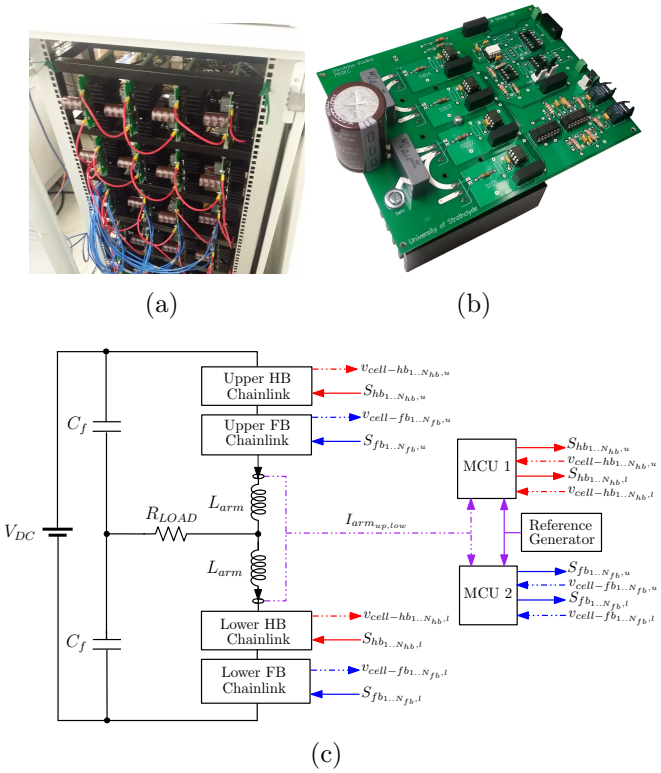


Figure 7.8: Experimental configuration: (a) HB and FB chain-links, (b) converter cell, (c) schematic diagram.

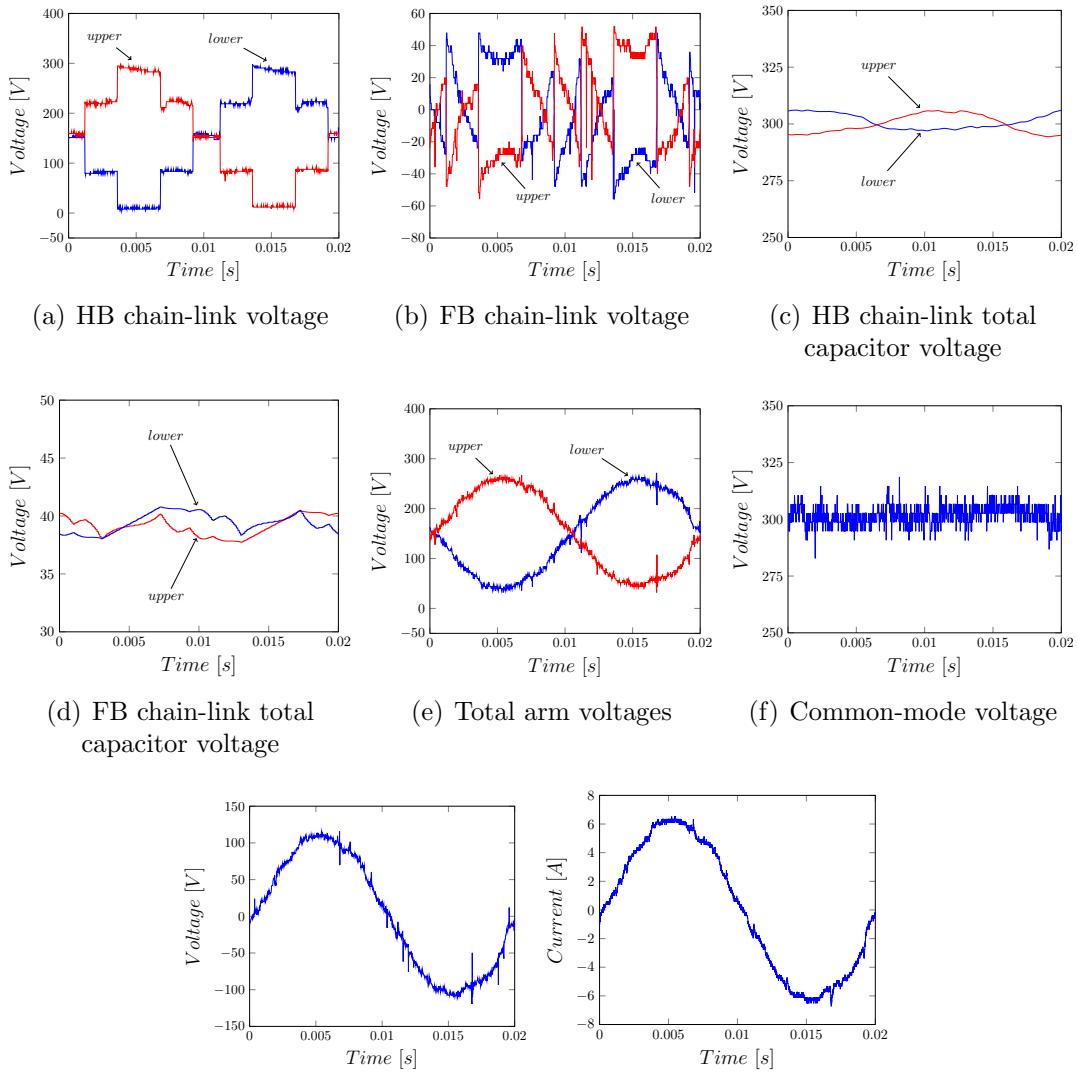
As in the simulation, each HB and FB chain-link consists of four cells, and the capacitances of the HB and FB cells are 2.2 mF and 4.4 mF respectively. Two capacitors (C_f= 5 mF) with split mid-point are connected across the DC power supply, as shown in Fig. 7.3(a), to create a return path for the single-phase arrangement. A 17 Ω resistive load is connected to the converter AC side.

The experimental tests replicate the simulation study to enable direct comparison of the results. Fig. 7.9 shows that the experimental waveforms for the voltages across the HB and FB chain-links of the upper and lower arms, the HB and FB cell capacitor voltages, the upper and lower total arm voltages, the common-mode voltage, and the output phase voltage and current correspond well with the simulation waveforms illustrated in Fig. 7.7. The low-energy, high-frequency voltage and current spikes are due to small switching mismatches introduced by dead-time, differences in the turn-on and turn-off times, rapid reference tracking and EMI. The adverse impact of these factors is amplified in the experimental waveforms in Fig. 7.9 due to the relative size of the minor voltage steps of the FB cells to those of the major voltage steps of the HB cells. In a full-scale system, where the ratio of the minor to major voltage steps will be of the order of 0.1 or less, these current spikes would be expected to be attenuated by the arm inductors.

Detailed quantitative converter comparisons

To complement the simulation and experimental validation presented in Sections 6.4.2 and 6.4.3, this section demonstrates the scalability of EMMC to high-voltage applications, using full-scale models developed in the EMPT simulation environment, and considers a number of implementations and comparisons with conventional MMCs. Details of the various MMC configurations being compared are shown in Table 7.4. In these simulations, the conventional MMC with 40 medium-voltage cells uses PWM and that with 400 cells uses NLC, while the HB and FB chain-links of the EMMC use NLM.

Fig. 7.10 shows simulation waveforms for the conventional MMC with 40 and 400 HB cells, and the EMMC with N_{hb}=40 and N_{fb}=5. The plots for output phase voltages and currents in Fig. 7.10(a) and 7.10(b) show that all converters being compared produce high-quality output voltages. However, the proposed EMMC with 40 medium-voltage HB cells (each rated at 16 kV) and 5 FB cells (each rated at 1.6kV) produces an output phase voltage with similar THD and dv/dt to that of the MMC with 400 HB cells (each rated at 1.6 kV), and which are improved compared to those of the conventional MMC with 40 HB cells. For conventional MMCs with 40 HB cells and 400 HB cells, and the proposed EMMC with 40 HB cells and 5 FB cells, the output voltage THD is 1.47%, 1.32% and 1.28% respectively. The output phase current quality for the three converters being compared is very similar as the arm inductances are sufficiently large to filter the high-frequency switching components from the arm and output phase currents, observed in Figs. 7.10(b) and 7.10(d). The arm voltages shown in Fig. 7.10(c)



(a) HB chain-link voltage (b) FB chain-link voltage (c) HB chain-link total capacitor voltage

(d) FB chain-link total capacitor voltage (e) Total arm voltages (f) Common-mode voltage

(g) Output AC voltage (h) Output AC current

Figure 7.9: EMMC experimental results.

confirm that the EMMC with fewer medium-voltage HB cells is able to match the performance of the conventional MMC with a large number of low-voltage HB cells in terms of waveform quality and dv/dt to affect any AC equipment that will be connected to its AC side. The DC-link currents and common-mode voltages shown in Fig. 7.10(e) and 7.10(f) highlight the injection of significant high-frequency harmonic components into the DC side of the conventional MMC with 40 medium-voltage HB cells when compared to the conventional MMC with 400 HB cells and the proposed EMMC with 40 HB and 5 FB cells, where DC link voltage ripple is 5.18%, 0.22% and 0.25% respectively.

The reason is that the large switching cell voltage of the conventional MMC

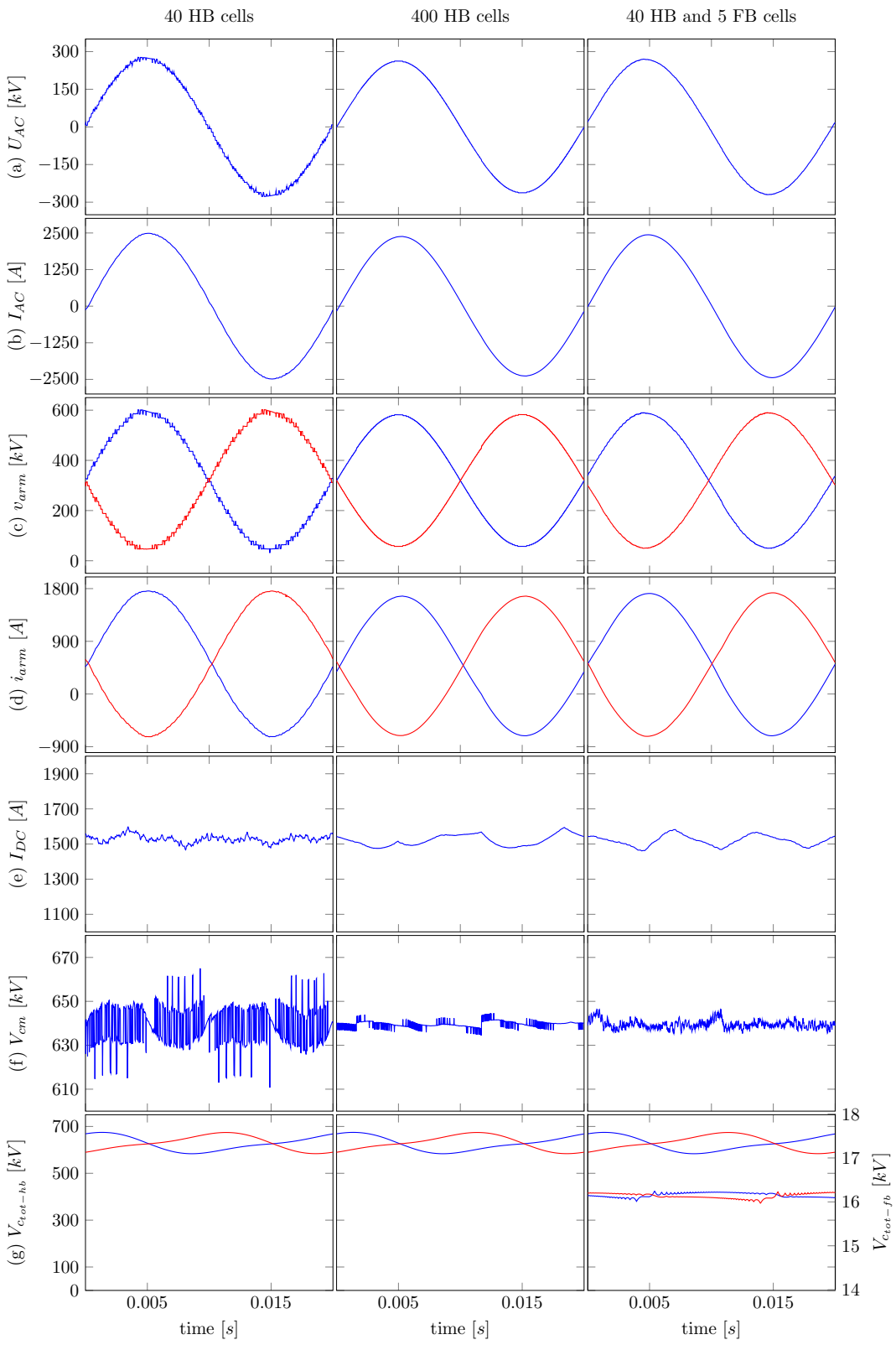


Figure 7.10: Comparison of the HB-MMC with 40 cells (left column), 400 cells (middle column) and EMMC with 40 HB cells and 5 FB cells (right column).

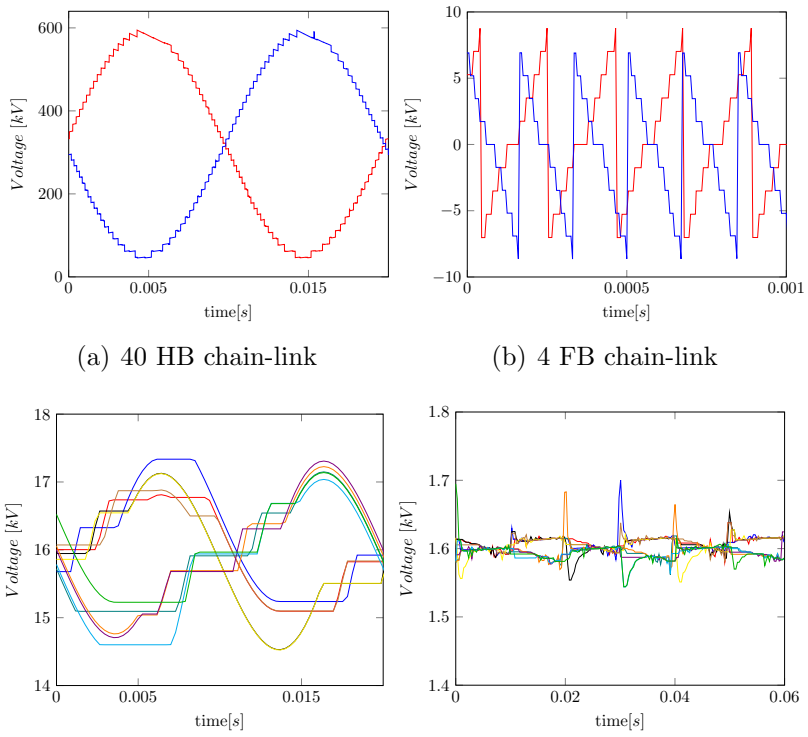
with 40 medium-voltage HB cells ($V_{c_{hb}40}$=16 kV) creates larger errors in the instantaneous magnitudes of the common-mode voltage compared to an MMC with 400 HB cells ($V_{c_{hb}400}$=1.6 kV) and the proposed EMMC. In practice, the DC link voltage ripple would be exacerbated in the MMC with 40 cells due to the dead-times and the significant mismatch between the turn-on and turn off timings of the series-connected IGBTs. The sum of the HB cell capacitor voltages of the conventional MMC with 40 and 400 cells, and of the EMMC with 40 HB and 5 FB cells are displayed in Fig 7.10(g). The total capacitor voltage for the HB cells for all converters shows identical voltage levels, whilst the total FB capacitor voltage of the EMMC is only a small proportion of the total HB cell voltage.

Furthermore, Figs. 7.11(a) and 7.11(b) show that the voltage stresses in the HB and FB cell capacitors and the switching devices of the proposed EMMC are well regulated. Figs. 7.11(c) and 7.11(d) show the voltages synthesised by the EMMC HB and FB chain-links that constitute the total arm voltage shown in the right-hand column of Fig. 7.10(c).

These plots show that the FB chain-link voltage represents a small fraction of the total arm voltage, with a switching pattern and timing that indicate any potential brief loss in synchronisation of the switching instants of the HB and FB chain-links (typically, of the order of few μs) will create low energy voltage spikes (which, in the worst-case, will have a peak value be limited to one half of an HB

Table 7.4: Detailed quantitative converter comparisons specifications.

N^o cells	N_{hb}=40	N_{hb}=400	N_{hb}=40 N_{fb}=5
HB chain-link modulation	PWM	NLM	NLM
FB chain-link modulation	-	-	NLM
HB cell voltage [kV]	16	1.6	16
FB cell voltage [kV]	-	-	0.8
HB cell capacitance [mF]	1.30	13.02	1.30
FB cell capacitance [mF]	-	-	6.51
P [MW]	1000		
V_{DC} [kV]	640		
L_{arm} [p.u.]	0.05		



(a) 40 HB chain-link

(b) 4 FB chain-link

(c) HB capacitor voltages

(d) FB capacitor voltages

Figure 7.11: EMMC internal chain-link and capacitor voltages.

cell voltage) in the arm voltage, which will be absorbed instantly by the upper and lower arm inductances, thus, no distortion will be observed in the output phase voltage. The output voltage spectra shown in Fig. 7.12 confirm the improved harmonic performance of the EMMC compared to that of the conventional HB-MMC with 40 medium-voltage cells.

Fig. 7.13 shows that for a large range of cell numbers, the EMMC can produce the same high-quality output AC voltage (THD, number of voltage levels and dv/dt), DC voltage and current ripple as a conventional MMC with a large number of cells.

7.2.4 Medium-voltage application

In the previous sections, it has been shown that the EMMC can produce a large number of voltage steps with a reduced number of cells per arm. Although the EMMC is intended for HVDC applications, it is possible to apply the same concept for medium-voltage (MV) applications. Usually, the voltage in MV applications does not need series connection of semiconductors, as state-of-the-art IGBTs can support up to a few kV. As a result an MV-EMMC can have exactly

the same circuit as the one that was used in the experimental set-up. One of the best applications for EMMC could be WTs. A WT can benefit from MMC technology as it reduces or even removes the AC passive filter requirements. Moreover, the EMMC can generate high-fidelity AC and DC waveforms with a low number of components (capacitors, semiconductors), which is ideal for installations with reduced space for equipment and voltage clearances, as in WT applications. An EMMC can also operate with an effective switching frequency up to 100 kHz, compared to the 2-3 kHz of the two and three level topologies. As a result, resonances that are created through the cables can be readily attenuated, as these resonant frequency components are significantly higher up in the frequency range than the converter fundamental frequency. The EMMC facilitates a less complex topology for a direct-drive WT, without the need of active filtering or a DC-DC converter. Fig. 7.14 shows the topology of the WT, which consists of a diode rectifier (DR) connected to the permanent-magnet generator (PMG), with an EMMC providing the grid interface.

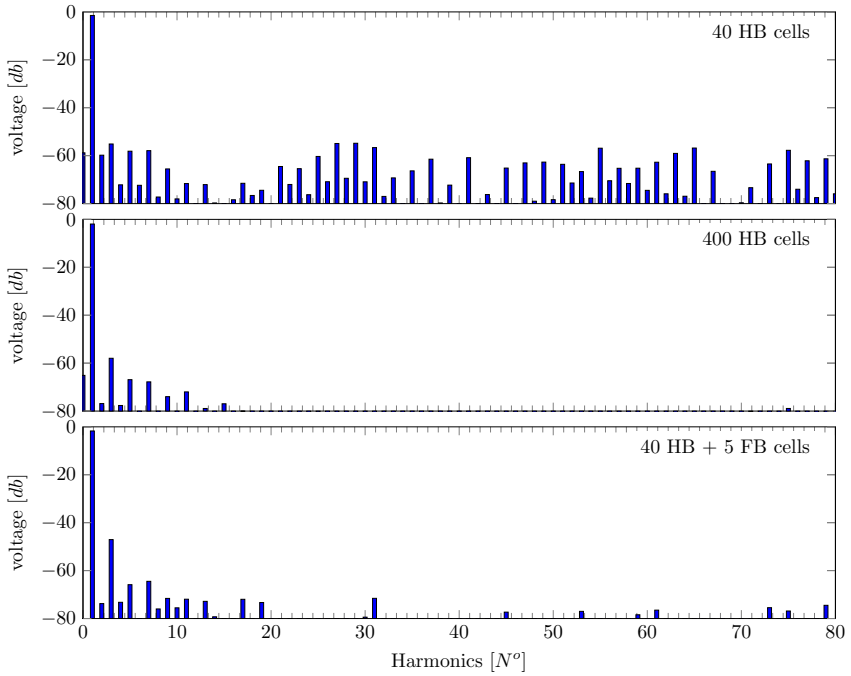
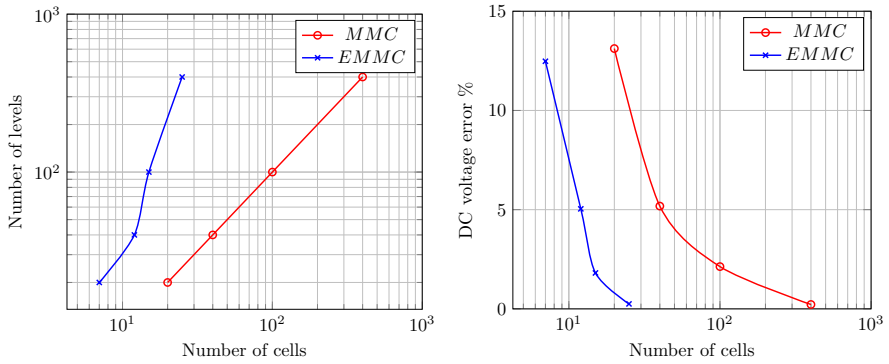
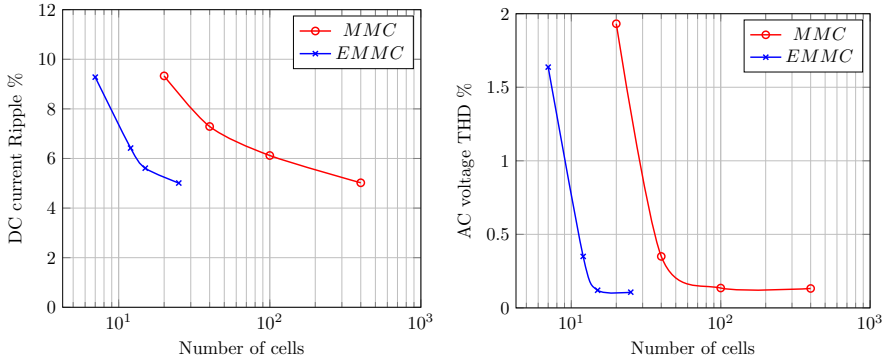


Figure 7.12: Phase voltage spectra, 40 cells, 400 cells and EMMC with 40 HB cells and 5 FB cells



(a) Correlation between number of cells and number of levels produced

(b) Common-mode DC voltage error



(c) DC current ripple

(d) AC phase voltage THD

Figure 7.13: Comparison of EMMC and conventional MMC perfomance for different numbers of cells.

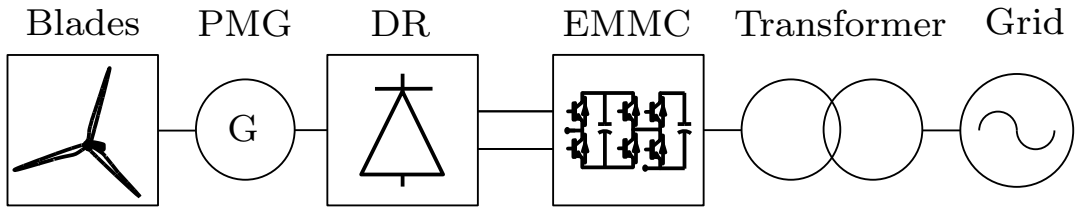


Figure 7.14: Proposed direct-drive WT incorporating EMMC and DR.

Operational concept

In the proposed WT topology, only the EMMC is able to be controlled actively. The DC voltage of the DR $V_{DC_{DR}}$ can be described as

$$V_{DC_{DR}} = \sqrt{2} \cdot V_{LL_{DR}} \cdot \frac{3\sqrt{3}}{\pi} \approx 1.35 \cdot V_{LL_{DR}} \tag{7.25}$$

where $V_{LL_{DR}}$ is the DR AC line-to-line voltage. For a fixed $V_{LL_{DR}}$ across the DR, the DC voltage is also considered to be fixed. Assuming that the EMMC operating in DC voltage control mode can be considered to be a controlled voltage source, the power transfer P_{DR} can be described as a function of the voltage difference between the EMMC and the DR, as shown in (7.26)

$$V^*_{DC_{MMC}} = k_v \frac{P_{DR}}{I_{DC}} = (V_{DC_{DR}} - V_{DC_{MMC}}) \tag{7.26}$$

where k_V regulates the power flow in the system, and is limited by the range of DC voltage control that the MMC allows. This concept is illustrated by the equivalent circuit of Fig. 7.15.

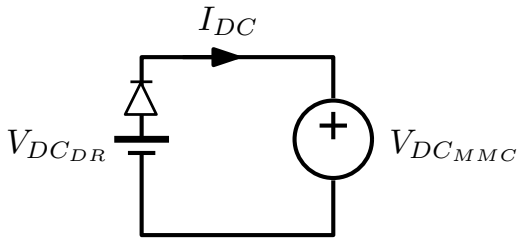


Figure 7.15: Equivalent circuit of DC link.

Equation (7.26) shows that it is possible to control the active power through the difference of DC voltage between the DR and EMMC. As a result, if the EMMC operates in DC voltage control mode, it can have a degree of control over the active power. In such a configuration the EMMC can directly control the power and DC voltage of the WT by adjusting the DC link voltage. Such a feature it is not possible in converters that adapt two and three level topologies, where the DC voltage has to be operate in a stiff fixed mode.

Simulations

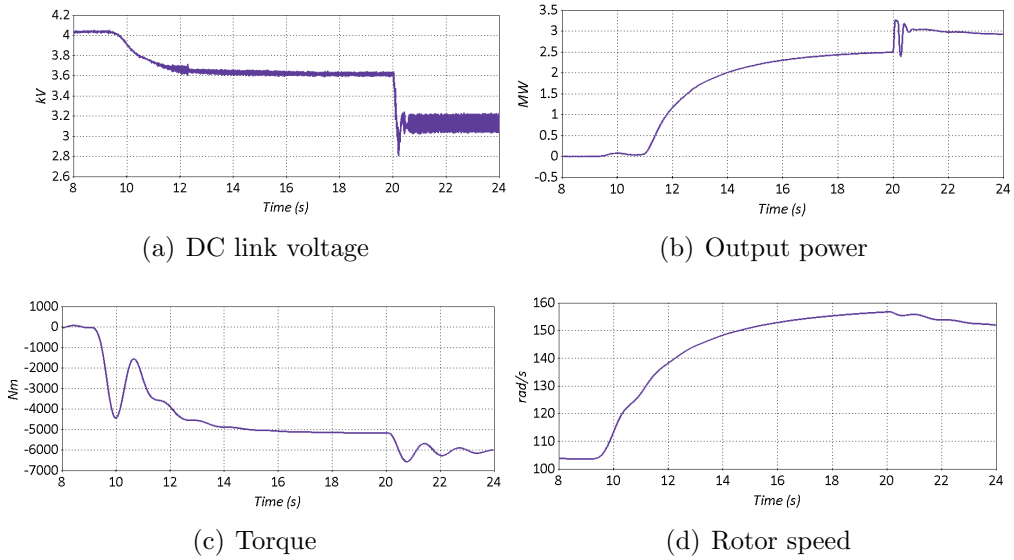
Simulation results in Fig 7.16 and Fig. 7.17 show the operation of the proposed WT system incorporating the EMMC. Table 7.5 shows the specifications of the WT system.

Fig 7.16 illustrates operation for a sudden change in torque at $t = 9$ s. As the rotor speed increases in response, the DC voltage adapts according to (7.26), and power is extracted. An active change in DC reference at $t = 20$ s also leads to increased power extraction as explained in (7.26).

Fig. 7.17 illustrates the operation of the proposed WT system under variable wind speed. The DC voltage adapts according to the mechanical torque which is generated from the wind.

Table 7.5: EMMC and DR WT system specifications.

Parameter	Value
P [MW]	3
V_{DC} [kV]	3.6
$V_{LL_{GRID}}$ [kV]	66
$V_{LL_{DR}}$ [kV]	2.67
EMMC cells	$N_{hb} = 10$
	$N_{fb} = 5$



(a) DC link voltage

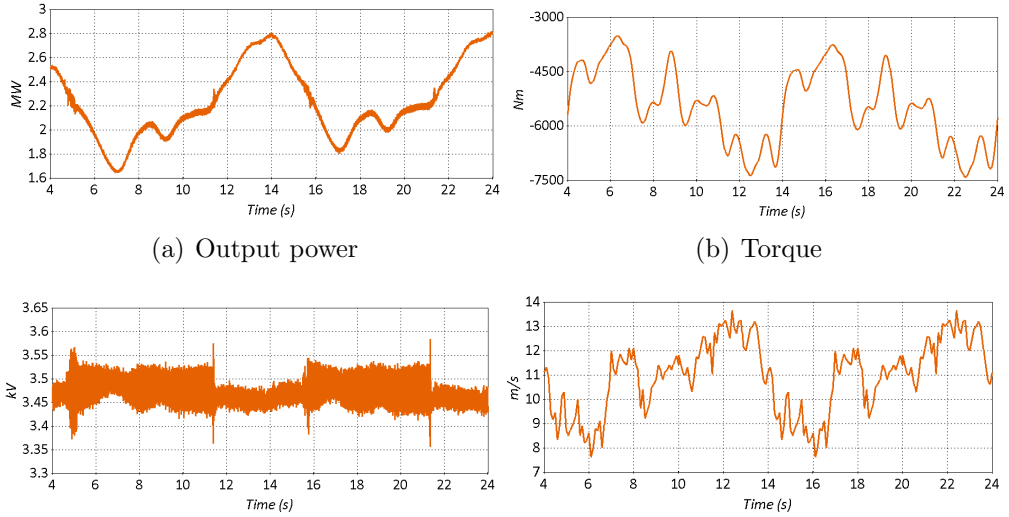
(b) Output power

(c) Torque

(d) Rotor speed

Figure 7.16: Demonstration of active power control through DC voltage.

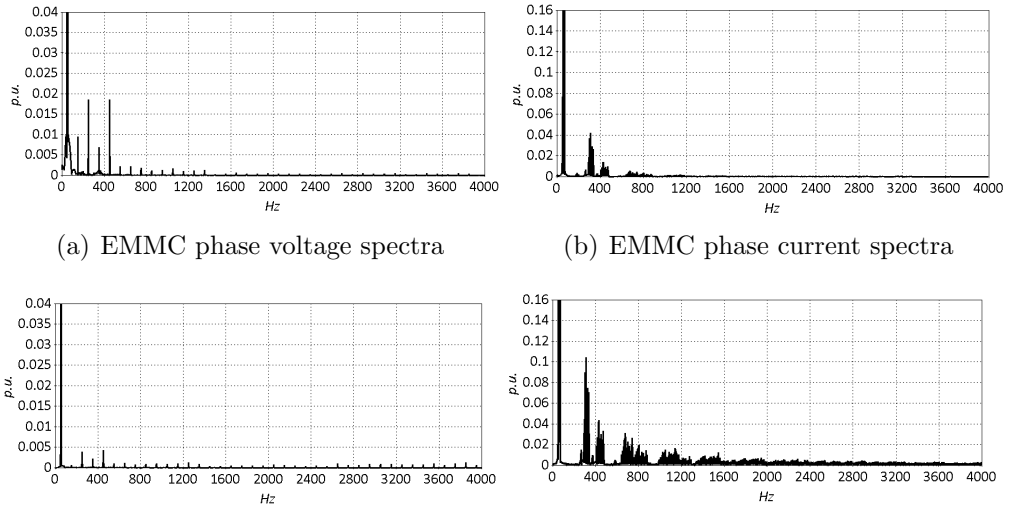
AC voltage and current spectra for the EMMC and the DR are shown in Fig. 7.18. Figs. 7.18(a) and 7.18(b) show that the EMMC produces high fidelity voltage and current without the necessity of passive filtering. The DR voltage and current contain significant 7th harmonic components as shown in Figs. 7.18(c) and 7.18(d) respectively. Whilst this 7th harmonic component may contribute to mechanical wear of the WT it is a positive sequence component and therefore it contributes to power transfer.



(a) Output power (b) Torque

(c) DC link voltage (d) Wind speed

Figure 7.17: Demonstration of operation during variable wind-speed.



(a) EMMC phase voltage spectra (b) EMMC phase current spectra

(c) DR phase voltage spectra (d) DR phase current spectra

Figure 7.18: EMMC and DR AC voltage and current frequency spectra.

7.3 Improved Alternate Arm Converter

7.3.1 Background

At present, there are two competing approaches to the realisation of DC fault blocking converters. The first approach incorporates FB cells into variants of the MMC, and results in the FB-MMC and MC-MMC. This approach is attractive due to its efficiency and power quality, and is well suited for applications with

confined space, such as offshore WFs. The second approach employs hybrid converters, such as the AAC, that combines the basic operation of an MMC or cascaded multilevel converter with a conventional two-level converter. The AAC has, for example, fewer cells than the equivalent MMC, making it suitable for applications with reduced space requirements. However, due to its fundamental operating regime, it has inferior power quality and performance during DC and asymmetric AC faults. Most of these hybrid topologies lack the power quality of an MMC and require filters, thereby making the claim of total converter station footprint reduction debatable.

This chapter presents an IAAC that utilises FB chain-links and a flying capacitor (FC) across the upper and lower arm DS of each phase leg to mimic the fundamental operation of the conventional three-level Flying Capacitor Converter. The FB chain-link in each arm of the IAAC is rated for a fraction of the full DC-link voltage, while the FC and the DS are rated for half of the DC-link voltage. The operating principle, modulation and energy management of the FB chain-links and FC are described in detail. The arm currents of the IAAC do not exhibit abrupt changes, irrespective of load power factor. The consequent low di/dt ensures that converter components are not subject to excessive overvoltages. These characteristics contribute to a significant improvement in the quality of the AC and DC-side waveforms generated by the proposed converter, making the need for AC and DC filtering unnecessary.

7.3.2 Proposed topology

Converter design and operation

Fig. 7.19 shows one phase leg of the IAAC topology. Each arm of the IAAC consist of series-connected FB cells (an FB chain-link) and a DS. An FC is connected across the DS in the upper and lower arms of each phase leg. The FC in each phase leg is rated for half of the DC link voltage V_{DC}. Modulation of the proposed IAAC must therefore utilise the FC in each phase leg to alternately connect directly to the upper and lower arms, principally during the synthesis of voltage levels above $\frac{V_{DC}}{2}$. The FB chain-link in each arm is utilised to synthesise voltage levels below $\frac{V_{DC}}{2}$. To extend the modulation index linear range to 1.27 p.u. as in the conventional AAC, the FB chain-link in each arm of the IAAC must be sized to block $\frac{2}{\pi}V_{DC}$. This design extends the voltage generation capability of the FB chain-link of each arm to $\frac{2}{\pi}V_{DC}$, and offers extra redundancy for voltage synthesis in the voltage range between 0 and $\frac{2}{\pi}V_{DC}$, which could be used to ensure the energy balance of the FC and FB cell capacitors. For over-modulation, the

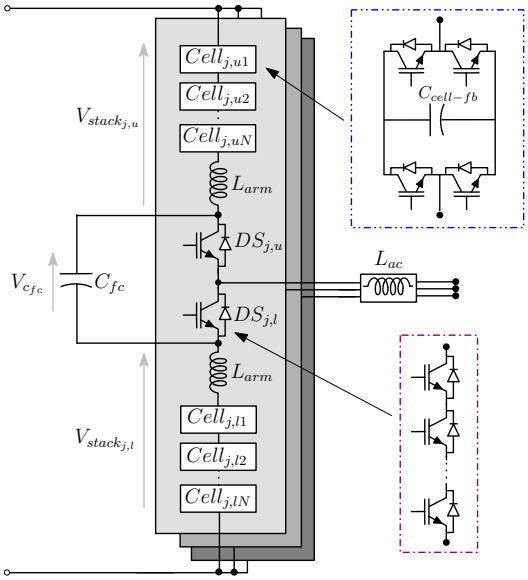


Figure 7.19: IAAC topology.

AC voltage reference m_{ref_j} that originates from the controller has to be modified by the inclusion a $\frac{4}{\pi}$ term as in (7.27).

$$m_{ref_j} = \frac{4}{\pi} M \cos(\omega t + \delta_j) \tag{7.27}$$

Subsequently, the AC reference is normalised for setting the total arm voltages $m_{norm_{j,k}}$ as described in (7.28).

$$m_{norm_{j,k}} = \frac{1 \pm m_{ref_j}}{2} \tag{7.28}$$

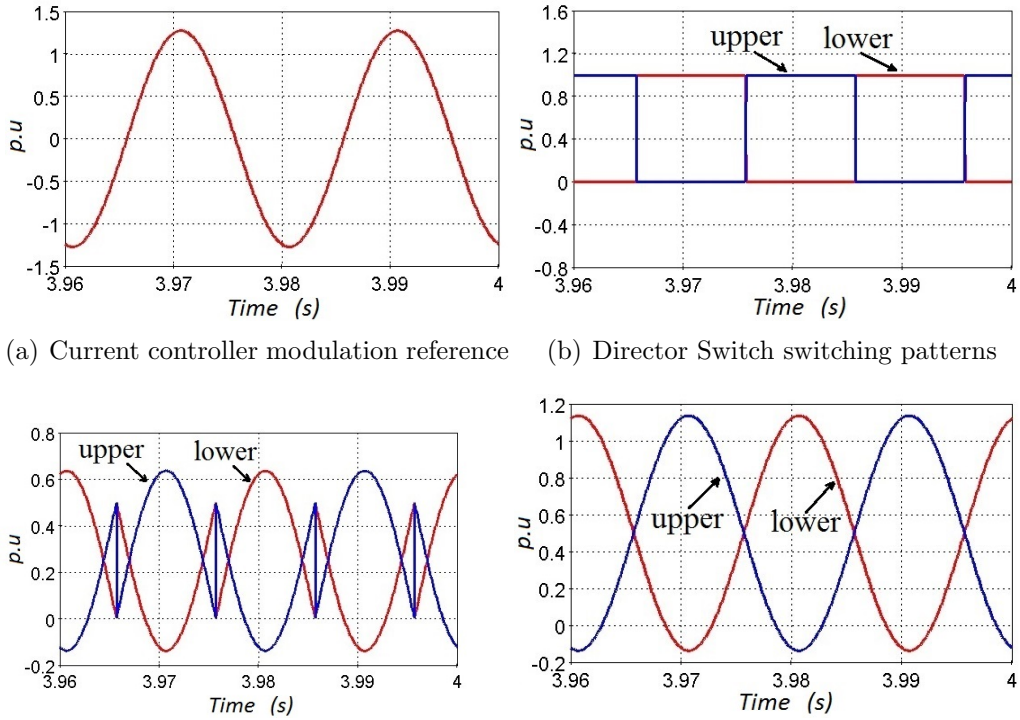
The normalised reference is manipulated for modulating the FB chain-link $m_{chain_{j,k}}$ and for DS operation $S_{DS_{j,k}}$, as described in (7.29) and (7.30).

$$m_{chain_{j,k}} = \begin{cases} m_{norm_{j,k}} - 0.5 & \text{if } m_{norm_{j,k}} \geqslant 0.5 \\ m_{norm_{j,k}} & \text{if } m_{norm_{j,k}} < 0.5 \end{cases} \tag{7.29}$$

$$S_{DS_{j,k}} = \begin{cases} 1 & \text{if } m_{norm_{j,k}} \geqslant 0.5 \\ 0 & \text{if } m_{norm_{j,k}} < 0.5 \end{cases} \tag{7.30}$$

The modulating voltage references are illustrated in Fig. 7.20.

Conventional capacitor voltage balancing techniques such as sorting, tolerance band and cell reference modulation methods can be applied to the chain-links.



(a) Current controller modulation reference

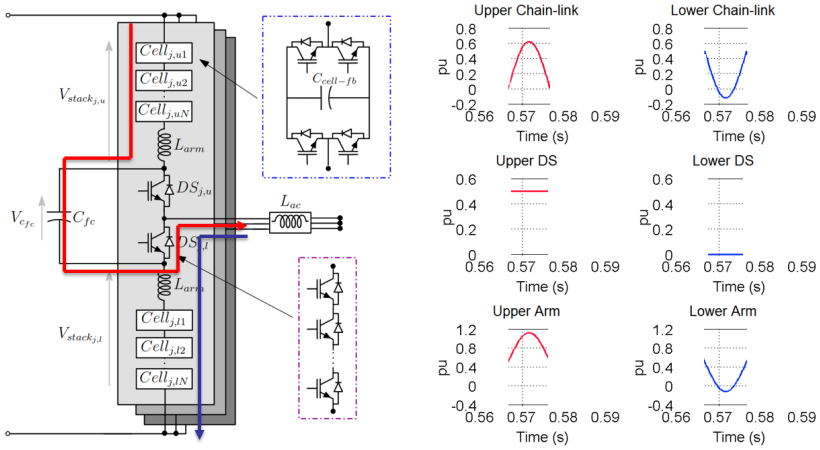
(b) Director Switch switching patterns

(c) Phase upper and lower chain-link reference signals

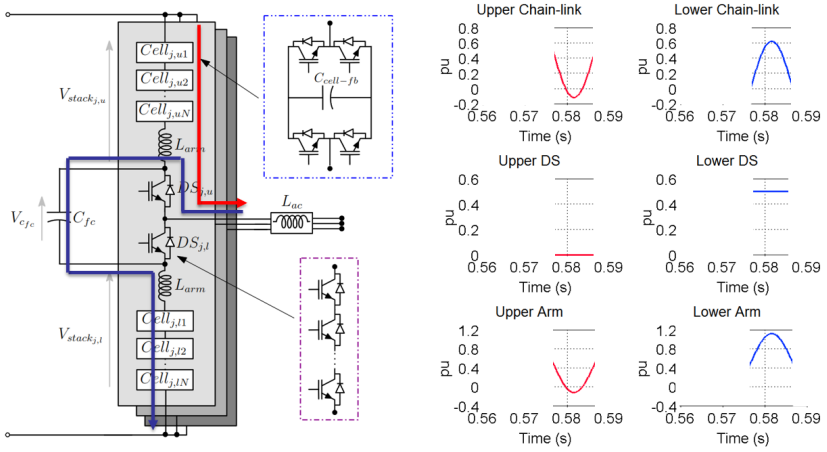
(d) Normalised arm reference voltages

Figure 7.20: IAAC modulation references.

FC voltage balance is achieved by observing the arm current polarity and manipulating the DS, taking into account the voltage magnitude across the FC. Fig. 7.21 shows the conduction paths in the upper and lower arms of the IAAC as it synthesises different output phase voltage levels for positive output phase current (i.e. when output current flows from the converter toward the AC grid). Notice that the two arms of the IAAC conduct simultaneously, and that turning the arm DS on and off bypasses and inserts the FC. The DS in each phase leg operates in a complementary manner, i.e. turning on the upper arm DS precludes the lower arm DS from being turned on. Furthermore, turning on the upper arm DS inserts the FC into the lower arm, and this increases the blocking voltage of the lower arm to $\left(\frac{\frac{4}{\pi}-1}{2}+1\right)\cdot V_{DC}$, whilst the blocking voltage of the upper arm remains at $\frac{2}{\pi}V_{DC}$. This means that with complementary operation of upper and lower arms of the IAAC, as in the MMC case, the entire voltage in the upper arm will be synthesised by the FB chain-link, while the voltage in the lower arm will be synthesised by the combination of the FB chain-link and FC. The opposite is true when the lower arm DS is turned on.



(a) Lower DS conduction



(b) Upper DS conduction

Figure 7.21: IAAC current conduction paths and voltage synthesis.

The total inertia H_{IAAC} of the converter is described as:

$$H_{IAAC} = 3\frac{E_{phase}}{S} \tag{7.31}$$

The energy requirement of each phase E_{phase} is defined as

$$E_{phase} = 2 \cdot E_{chain} + E_{fc} \tag{7.32}$$

where E_{chain} and E_{fc} are the energy stored in chain-link and FC respectively. The stored energy per IAAC is related to the inertia constant H_{IAAC} which is in the range of 30-40 kJ/MW [77]. The total arm capacitance $C_{arm_{req}}$ must be sized to cater for stored energy requirements E_{chain} and E_{fc} and is calculated according to the chain-link and FC equivalent capacitances, C_{chain} and C_{fc} respectively, as

shown in (7.33).

$$C_{arm_{req}} = \frac{C_{chain} \cdot C_{fc}}{C_{chain} + C_{fc}} \tag{7.33}$$

Since the blocking voltage of the FB chain-link is $\frac{2}{\pi}V_{DC}$, the number of FB cells per chain-link N_{FB} is described as:

$$N_{FB} = \frac{2\dot{V}_{DC}}{\pi \cdot V_{cell}} \tag{7.34}$$

where V_{cell} is the voltage across an FB cell.

Converter analysis

The cell capacitor current in each individual cell can be described in terms of arm current $i_{(j,k)}$ and the switching function $v_{cell_{N,j,k}}$ described by:

$$i_{cell-n_{j,k}} = (1 - s_{cell-n_{j,k}}) \cdot i_{j,k} \tag{7.35}$$

The cell voltage can be described as a function of arm current and cell capacitance by:

$$v_{cell-n_{j,k}}(t) = \frac{1}{C_{cell}} \cdot \int_{t-\Delta t}^{t} \left(i_{cell-n_{j,k}}(\tau) \right) d\tau \tag{7.36}$$

where Δt is the time step of the discrete integration. The chain-link voltage is the summation of the cell voltages, described by:

$$v_{chain_{j,k}} = \sum_{i=1}^{N_{cell}} \left[(1 - s_{cell-n_{j,k}}) \cdot v_{cell-n_{j,k}} \right] \tag{7.37}$$

The voltage across the DC link can be expressed in terms of the instantaneous upper and lower arm voltages ($v_{j,u}$,$v_{j,l}$) of the same phase leg, as shown in:

$$v_{arm_{j,k}} = v_{chain_{j,k}} + V_{fc} \cdot (1 - S_{DS_{j,k}}) \cdot dV_{fc} \tag{7.38}$$

where dV_{fc} is the voltage ripple across FC. The voltage V_{DS} across the DS, which determines its sizing, is described as:

$$V_{DS} = \frac{V_{DC}}{2} + dV_{fc} \tag{7.39}$$

Consequently the DC voltage V_{DC} can be defined by:

$$V_{DC} = v_{arm_{j,u}} + v_{arm_{j,l}} \tag{7.40}$$

During upper and lower arm conduction, the converter AC voltage e_j is described respectively as:

$$e_j = -v_{j,u} - \frac{L_{arm}}{2} \cdot \frac{di_{DS_{j,u}}}{dt} + L_{AC} \cdot \frac{di_{j,AC}}{dt} + \frac{V_{DC}}{2} \tag{7.41}$$

$$e_j = v_{j,l} + \frac{L_{arm}}{2} \cdot \frac{di_{DS_{j,u}}}{dt} + L_{AC} \cdot \frac{di_{j,AC}}{dt} - \frac{V_{DC}}{2} \tag{7.42}$$

where L_{arm} and L_{AC} are the arm and AC-side inductances respectively (as shown in Fig. 7.19). The upper and lower chain-link currents $i_{chain_{j,k}}$ in each phase can be expressed, respectively, as:

$$i_{chain_{j,u}} = i_{fc} + i_{DS_{j,u}} \tag{7.43}$$

$$i_{chain_{j,l}} = i_{fc} + i_{DS_{j,l}} \tag{7.44}$$

where i_{fc} and $i_{DS_{j,k}}$ are the FC and DS currents respectively. Phase current $i_{j,ac}$ and DC current i_{DC} can be defined by (7.45) and (7.46) respectively.

$$i_j, AC = i_{DS_{j,l}} - i_{DS_{j,u}} \tag{7.45}$$

$$i_{DC} = \frac{i_{chain_{a,u}} + i_{chain_{a,l}} + i_{chain_{b,u}} + i_{chain_{b,l}} + i_{chain_{c,u}} + i_{chain_{c,l}}}{2} \tag{7.46}$$

It can be seen, therefore, that DC current i_{DC} is synthesised from the DS and FC currents, and contains a low harmonic ripple due to FC voltage ripple from (7.39). In contrast to the AAC, this results in continuous symmetrical arm currents $i_{chain_{j,k}}$ during all IAAC operating modes.

Converter power losses

The semiconductor power losses are calculated using a method previously described in Chapter 3, and are compared in Table 7.6 for several converters. The table also compares the numbers of semiconductor devices in each converter, with reference to the HB-MMC. Observe that the IAAC has reduced conduction losses compared to the AAC, whilst the IAAC switching losses are increased due to hard-switching of the DS. However, the IAAC has lower total losses, primarily due to the reduced number of semiconductors.

7.3.3 Verification using simulation

This section assesses the viability of the IAAC when it is connected to a stiff DC source and a strong AC network, and operates in active and reactive power

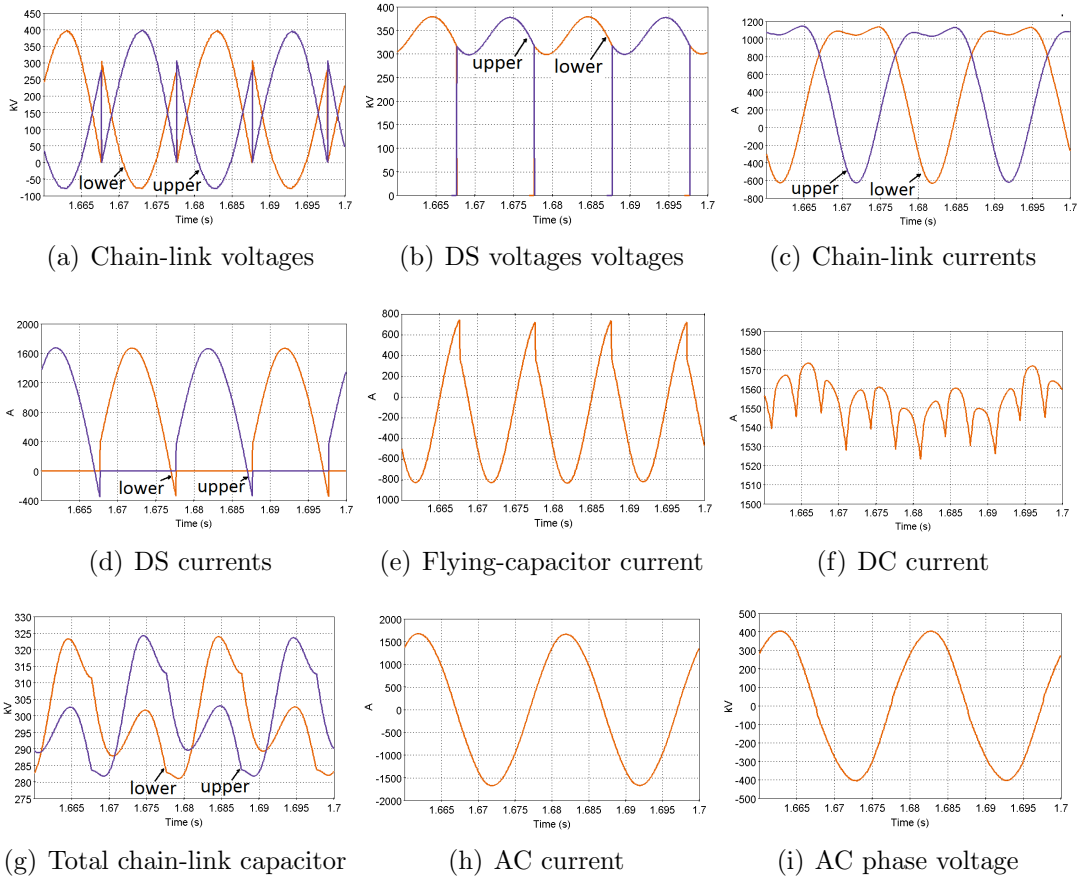
Table 7.6: Comparison of losses and numbers of semiconductors.

Topology	Cond. Losses [kW]	Sw. Losses [kW]	Semiconductors ratio
HB-MMC	4749	1136	1
MC-MMC	8166	1188	1.5
AAC	8535	1686	1.640
IAAC	7324	1973	1.525

control mode with a decoupled dq current controller similar to the controller described in Chapter 3. The simulations are based on the parameters shown in Table 7.7. Fig. 7.22(a) and 7.22(b) show the FB chain-link and DS voltages. The total arm voltages are synthesised from the FB chain-link and DS voltages, using over-modulation operation. The FB chain-link provides voltages to enable arm voltages below zero and above V_{DC}. In contrast to the conventional AAC, the DS voltages of the IAAC exhibit fast and abrupt switching, which indicates hard switching and which necessitates the series connection of IGBTs in the DS. The need for series connection might be considered as a limitation, as the capability to cater for series connection at hundreds of kV is not widely available. The FC capacitor voltage is aligned with the top fluctuation of DS voltage, it settles at $\frac{V_{DC}}{2}$ and exhibit ripple of $\pm 8\%$. The FC capacitor voltage charging and discharging profile is according to the AC current sign. The arm currents in Fig. 7.22(c) do not exhibit high di/dt as a result of the constant continuous current path, which is available under all operating conditions. As can be observed, the DS current in Fig. 7.22(d) is discontinuous, similar to the AAC arm current. Additionally, during the transition between the upper and lower arms, the DS is subjected to a high-energy current spike due to the interruption of the current path, as the

Table 7.7: IAAC specifications.

Parameter	Value
S [MVA] 1045	1045
V_{DC} [kV]	640
V_{chain}/V_{DS} [kV]	388/375
V_{grid}/V_{conv} [kV]	400/500
Arm inductance [%]	15
Transformer reactance[%]	18
Chain-link capacitance [μF]	50
FC capacitance [μF]	50
N	255



(a) Chain-link voltages (b) DS voltages voltages (c) Chain-link currents

(d) DS currents (e) Flying-capacitor current (f) DC current

(g) Total chain-link capacitor (h) AC current (i) AC phase voltage

Figure 7.22: IAAC waveforms during steady-state operation at unity power factor.

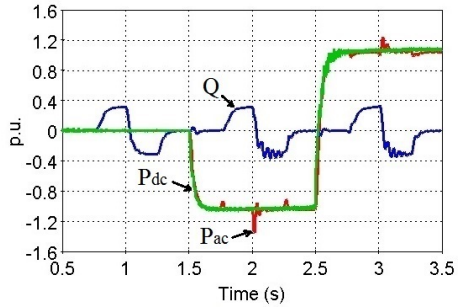
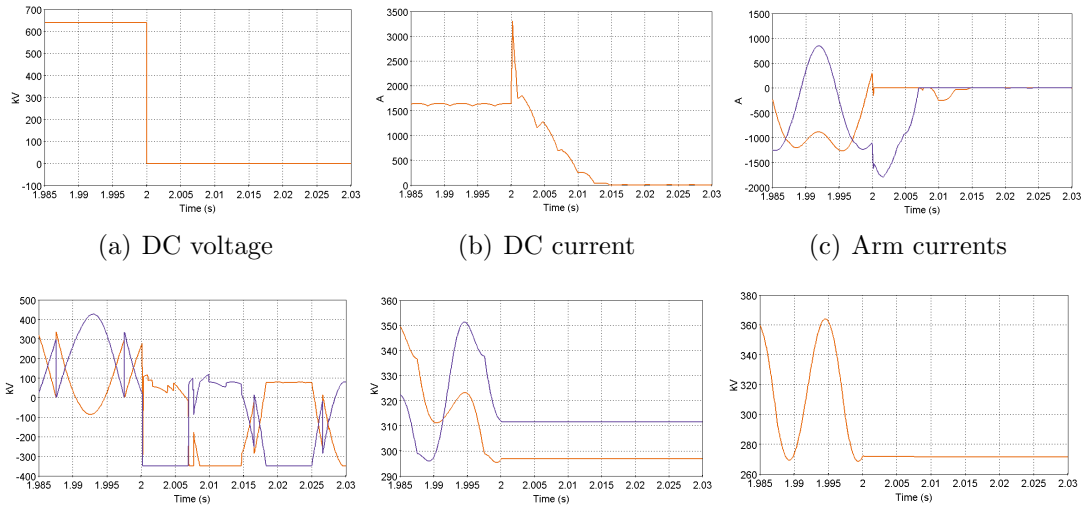


Figure 7.23: IAAC active and reactive power capabilities.

DS switches off. However, due to the continuous current path through the FC, energy equilibrium among the arms is achieved without generation of overvoltage. The FC allows a constant current path to balance the currents during continuous and discontinuous operation of the DS, shown in Fig. 7.22(e). The chain-link currents are always continuous, in contrast to those in AAC, and synthesise the

DC currents in the same way as in an MMC. As a result, DC current in Fig. 7.22(f) does not carry any of the high di/dt components from the DS current path. The high-quality DC current contain only $\pm 1.5\%$ ripple, indicating that no DC filter is required. The 100 Hz harmonic current in each FC appears as a low-magnitude 300 Hz ripple on the DC current. The chain-link capacitor ripple is influenced by the charging and discharging process which depends on arm current sign and the positive/negative voltage insertion of the FB cells, as shown in Fig. 7.22(g). Figs. 7.22(h) and 7.22(i) respectively show high-quality AC phase voltage and line current.

Fig. 7.23 illustrates the PQ capabilities of the IAAC. The converter successfully operates at various operating points following the active and reactive power demands, while there is good match between the AC and DC power transfer. The spikes observed on the active power trace at $t = 2$ s and $t = 3$ s are due to the rapid reactive power reversal demand.

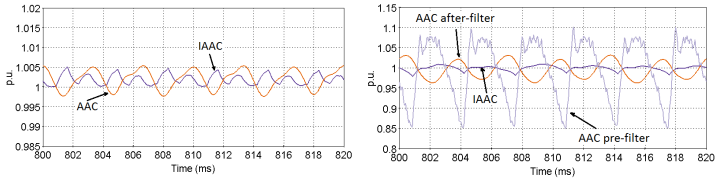


(a) DC voltage (b) DC current (c) Arm currents

(d) Arm voltages (e) Total chain-link cell capacitor voltages (f) FC capacitor voltage

Figure 7.24: IAAC DC fault blocking operation.

Fig. 7.24 demonstrates the DC blocking capability of the IAAC during a pole-to-pole DC fault. The fault is initiated at $t = 2$ s and immediately DC voltage collapses as shown in Fig. 7.24(a), while the DC current rises until arm over-current detection activates the converter's blocking state as shown in Figs. 7.24(b) and 7.24(c) respectively. It should be noted that due to the absence of the capacitive DC filter, the IAAC DC fault current is reduced compared to that of the conventional AAC. The converter's blocked state is illustrated in the arm voltages of Fig. 7.24(d). The chain-link and FC capacitor voltages maintain



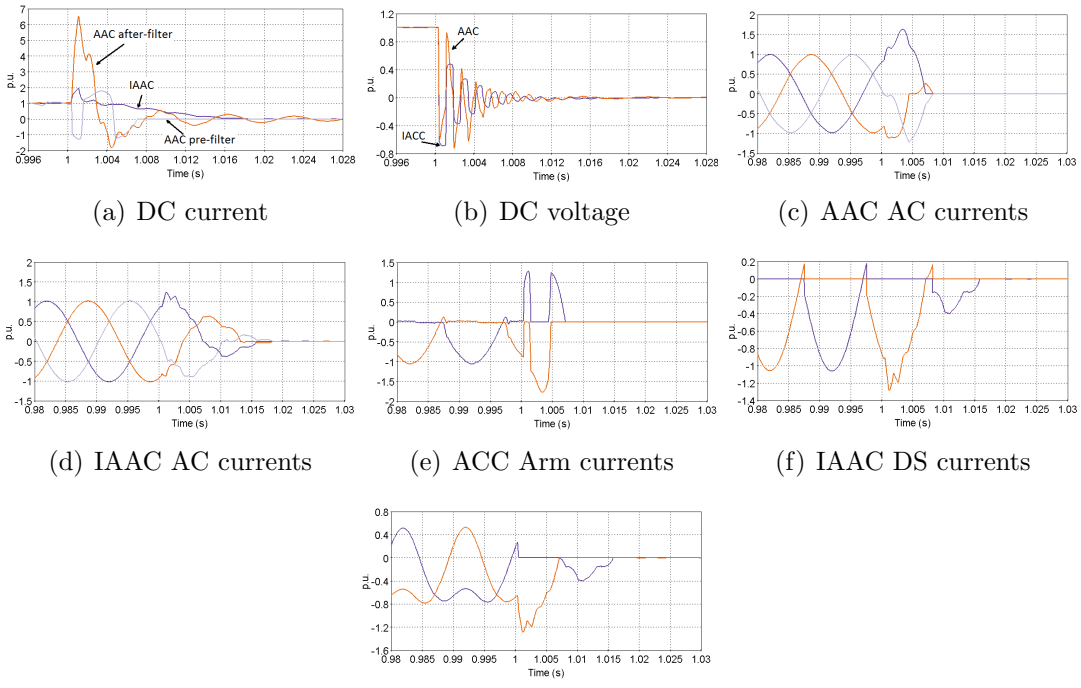
(a) DC voltage (b) DC current

Figure 7.25: AAC and IAAC steady-state DC values.

constant values as arm current flow has been interrupted as shown in Figs. 7.24(e) and 7.24(f) respectively.

Fig. 7.25 shows the steady-state DC voltages and currents of AAC and IAAC. Both topologies achieve an acceptable DC voltage ripple of less than 1%. Fig. 7.25(b) shows the effectiveness of the DC filter on AAC, which reduces the ripple from 25.4 % to 6.8 %, while the IAAC achieves 2.8 % without any DC filter.

Fig. 7.26 shows the comparison between AAC and IAAC during a low resistive permanent pole-to-pole DC fault. The AAC appears to have higher DC fault current value compared to IAAC due to the filter discharge towards to fault, while the contribution of the converter is limited, as shown in Fig. 7.26(a). Moreover, AAC has installed a larger value of inductance, which enforcing the



(a) DC current (b) DC voltage (c) AAC AC currents

(d) IAAC AC currents (e) ACC Arm currents (f) IAAC DS currents

(g) IAAC chain-link currents

Figure 7.26: AAC adn IAAC DC pole-to-pole fault.

DC current to achieve zero in a more slower and oscillatory manner, compare to IAAC. In addition the IAAC has lower magnitude DC voltage oscillations due to the absence of the DC filter, as shown in Fig. 7.26(b). The AC current contribution to the DC fault is lower on the IAAC, as shown through the AC, arm, stack and DS currents of AAC and IAAC in Fig. 7.26.

7.4 Summary

This chapter proposes the development of novel topologies which address some of the shortcomings of the state-of-the-art HVDC converters.

The first topology, the EMMC, is an enhanced MMC topology with a significantly reduced number of cells per arm that generates high-quality AC and DC side waveforms and high numbers of levels in the output voltage to rival the performance of the conventional MMC with hundreds of cells per arm. This is achieved by incorporating low-voltage FB chain-links with blocking voltage equal to half that of an HB cell. The theoretical development, simulations and experimental results confirm that the EMMC offers reduced AC harmonics and DC voltage ripple with a low number of cells per arm when compared to conventional MMC. The main features of the EMMC are:

- Significant improvements in the power quality of the AC and DC side waveforms are achieved without significant increase in the power circuit and control complexity when compared to the conventional MMC.

- In comparison with a conventional MMC with the same number of cells, the EMMC has similar volume but eliminates the need for AC and DC side filters due to significantly increased output power quality. The proposed concept of the low-voltage FB chain-link can be integrated into existing, currently operational, low cell count MMC-based HVDC links with minimum modification, and can be implemented in FB-MMC and other hybrid topologies.

- Gains that are achieved in power quality outweigh the marginal increases in semiconductor losses and area due to integration of the low-voltage FB chain-links. These losses may however be reduced by using state-of-the-art semiconductor devices.

- Possible adaptation for MV applications for higher power quality and controllability compared to conventional VSC, with reduced footprint and increased reliability.

The second topology, the IAAC, offers compact design, high-quality AC and DC side waveforms, and similar semiconductor losses when compared to AAC and MC-MMC topologies. The proposed IAAC replaces the large DC link capacitors required by the conventional short-overlap controller AAC by three flying capacitors (one per phase leg and each rated for half the DC link voltage) that do not discharge during DC faults. The theoretical development is presented, and simulation results show that the proposed IAAC is promising for HVDC applications. The main features of the IAAC are:

- Good efficiency with a reduced number of semiconductors compared to the AAC.
- Continuous arm current operation, which removes the need for DC filters without affecting the efficiency and the complexity of the converter. This is particularly significant since removal of the DC filter capacitors reduces the potential DC fault current levels when compared to the AAC.

Chapter 8

Conclusions and future research

8.1 Conclusions

Multilevel VSC are characterised by their flexibility to allow rapid and accurate energy equilibrium amongst power systems that incorporate HVDC links. However, due to the nature of DC based transmission, future HVDC grids are prone to new challenges which demand solutions which are not straightforward. Following the advent of multilevel converters for HVDC networks, different manufacturers competed to find the best solution for HVDC. Initially, the main challenge was to design an efficient and robust converter topology which could suppress destructive DC pole-to-pole faults. However, it is shown in this thesis that converters must have a variety to additional functionalities to ensure safe operation and to facilitate future network development. The ability to combine these multiple functionalities in a single converter is also attractive due to reduced capital cost and space.

This thesis assesses the key features and operational characteristics of multilevel VSC which are characterised by their ability to block DC pole-to-pole faults. Chapter 1 introduces the thesis, describing the motivation and scope of the research study. Chapter 2 provides a comprehensive literature review of HVDC technologies which are currently the subject of research, and technologies which have been developed sufficiently to the point where they have been installed and are operational. Specifically, the review includes AC-DC power conversion using LCC and VSC technology, a variety of potential DC-DC converter topologies and their design considerations, DC fault current limitation methods, DCCB topologies, and cables structures. The review identifies those HVDC components with the most favourable characteristics to facilitate the development of HVDC grids. Chapter 3 provides analysis and development of time-domain function-switching (FS) VSC models, which are the key tools of this thesis, for determining the oper-

ation and functionality of each converter topology. The models provide a trade-off between complexity and resource efficiency, creating accurate and high-fidelity results. A comprehensive comparison of full detailed and the FS models provides evidence for their accuracy. The FS models include the control architectures which are applicable in real developed hardware. Moreover, the semiconductor thermal profiles are included in the converter operation, where they provide high accuracy thermal loss results according to the exact operation of each converter. The inclusion of the semiconductor losses in the simulation solution of the power circuit provide higher accuracy compared to the analytical method. The actual losses are computed based upon the arbitrary switching pattern of the semiconductors imposed by the CBA. Also, the appearance of the semiconductor losses in the electrical circuit provide a more accurate assessment of the impact of losses on control and protection equipment. Chapter 4 provides a comprehensive comparison of state-of-the-art HB-MMC, MC-MMC, FB-MMC and AAC multilevel converters. The comparison includes the semiconductor losses, AC and DC side power quality, and steady-state and controlled dynamic behaviour for point-to-point HVDC networks that incorporate strong AC grids and WFs. The PQ capabilities of each topology are investigated during active and reactive power reference change, reduced DC voltage, and islanded operation. The investigation reveals:

- For a given DC voltage, a converter with a reduced number of cells has increased switching losses, as the switching voltage is higher compared to a converter with an increased number of cells.
- The converter topology dictates the total semiconductor losses and the loss distribution among the cells. The FB-MMC has more than double the losses of an HB-MMC, while the MC-MMC and AAC have 50% to 60% more losses than an HB-MMC.
- Using Hybrid-Switches, which combine SiC and Si semiconductors, it is possible to reduce the cell switching losses even though semiconductor area is increased.
- The total semiconductor losses differ depending upon whether a converter operating in rectifier or inverter mode. This difference is most apparent in the HB-MMC.
- In an AAC the DC filter capacitor may be reduced in size whilst the filter inductance is correspondingly increased. Hence the potential DC fault current may be reduced.

- For identical specifications, an AAC has reduced capacitive reactive power generation compared to an MMC. Also the AAC cannot operate at reduced DC voltage.

- The AAC appears to stress the snubber and protective equipment of the DS, even during steady state operation. Phase, arm and DS surge arresters may be strained even during normal operation. In addition, the appearance of high dv/dt in the arm voltages, occur on the AC voltage which may further strain the interfacing transformer.

- The HB-MMC can operate over a limited range of reduced DC voltage, whilst the MC-MMC can operate at almost zero DC voltage and the FB-MMC can completely reverse the DC voltage polarity.

In general, the MC-MMC appears to have better performance compared to the AAC due to higher operational range of modulation index. Furthermore, the AAC arms are exposed to high over-voltages due to high di/dt, which results in considerable stress of the protective surge arresters during normal operation within the nominal PQ envelope.

Chapter 5 analyses, demonstrates and compares transient operation of the state-of-the-art converters introduced in Chapter 4. The demonstration includes start-up, DC pole-to-pole faults, DC pole-to-ground faults, AC unbalanced operation, and partial DC voltage loss operation. The demonstration reveals:

- In all the converters studied that include FB-cells, it is necessary the FB cells emulate the operation of HB cells in order to allow a current path between AC to DC sides.

- In order to avoid transient voltages and currents during charging, the master converter has to charge from the AC side and be in DC voltage control mode, while the slope of the DC voltage ramp during charging has to be low in order reduce the voltage overshoots across the cell capacitors and cables.

- Following a DC fault, all of the converters which have DC fault blocking capability are capable of being operated to test for fault clearance as part of the restart process.

- An MC-MMC with a reduced number of FB cells, in combination with DC reactors, is able to control DC fault current trajectory allowing the DCCB design requirements to be relaxed. The total MC-MMC semiconductor losses are reduced, and only one of these converters is required in the HVDC grid to achieve the fault current trajectory control functionality.

- The MC and FB-MMC can continue to operate during a DC pole-to-ground fault, and can transfer power at a reduced level.
- The AAC is not able to protect transformer and cable insulation during DC pole-to-ground faults, without damaging converter's internal components.
- An AC unbalance fault on a converter which controls the DC voltage can be destructive due to the power mismatch with the DC grid. In the case of increased DC voltage the cable insulation might be damaged, while converter control may be lost if DC voltage is decreased. Adjustment of the power reference to the converter which controls active power maintains constant DC voltage as the power delivery meets the demand of the DC grid. This requires communication between the converters and the master controller which rapidly changes the power references.
- All types of MMC can achieve fault ride through under AC unbalanced operation. A simple positive-negative current controller is sufficient to manage the effects of AC unbalance, and a PR circulating current suppression controller suppresses the voltage and current ripples which may appear on the DC side.
- Due to the fact that the AAC does not have a continuously controllable common-mode current, the DC power quality deteriorates during AC unbalanced operation and high-frequency, high-magnitude ripples appear on the DC voltage and current. These ripples may be particularly problematic in multi-terminal grids.

The flexible modulation index of the MC-MMC provides adequate performance for all transient scenarios. Unfortunately, AAC cannot perform acceptably under unbalanced AC and pole-to-ground DC faults, as it has limited independent arm operation and modulation index range. As a result, AAC may be dependent on collateral protection equipment.

Chapter 6 presents the development of a flexible low scale test-rig for experimental laboratory use. A selection of off-line simulations from Chapters 4 and 5 were validated. The chapter includes the design, development and implementation of a reduced scale test-rig for multilevel VSC controller and topology validation. Two three-phase 4kW converters are developed: a four-cell FB-MMC which operates in both MMC and AAC modes, and an experimental qMMC which emulates the operation of an MMC and which is useful for system level studies. The converters are tested in inverter mode under different illustrative PQ demand conditions, and during unbalanced AC faults. In addition, the FB-MMC is tested

during reduced DC voltage operation. The MMC and AAC test-rig results show good agreement with the off-line simulations results shown in Chapters 4 and 5.

An innovative hardware implementation of the average converter model is realised through the qMMC which allows the development and validation of system studies for reduced complexity and cost. The qMMC can emulate the internal stored energy of an MMC by including only one cell per arm. The need for CBA is removed, thus the control complexity of the converter is greatly reduced. However, due to signal latencies and voltage mismatches, each arm of the qMMC must operate in a complimentary mode to avoid large over-voltages on the DC side.

A low-voltage hardware implementation provides good insight into the actual operation and limitations of the converter controller. EMI, signal latency, and synchronisation issues are difficult to include in off-line or real-time simulations, making the hardware implementation a good validation platform.

Chapter 7 presents two new converter topologies. The EMMC offers a high number of voltage levels with a reduced number of cells when compared to established MMC topologies. The novel EMMC exhibits a new, unique multiplication feature where the number of voltage levels per arm is approximately equal to the product of the numbers of HB and FB cells, whilst the output voltage step amplitude is equal to that of the FB cell voltage. The result is high quality AC and DC voltages and currents without the need for filters. Key characteristics of new EMMC topology include:

- Low voltage FB cells are incorporated in combination with medium voltage HB cells.
- The medium voltage HB cells may require series connection of IGBTs.
- Even though FB cells are used, the switching losses are reduced due to the reduced switching voltage, while the HB cells switch less frequently.
- Due to the reduced operating voltage of the FB cells, SiC semiconductors can be incorporated which may reduce the switching losses.
- The concept of EMMC can be used for medium voltage applications such as WTs, where high power quality can be achieved without incorporating passive filtering. Also, by including MMC technology in the WT system, it is possible to reduce the control and interfacing converter complexity by implementing the generator connected converter as a diode rectifier.

The second topology introduces an improved novel AAC topology. The proposed IAAC removes the need for DC filtering, thereby reducing DC fault currents, and can block DC faults. The main characteristic of the IAAC include:

- The chain-link currents are always continuous, compared to the conventional AAC which are discontinuous. The currents find a path through a flying capacitor which allows arm energy balance, thereby removing the need for an overlap controller. This reduces the di/dt which is responsible for harmful overvoltages. Therefore the AC and DC currents and voltages do not experience any voltage or current spikes.
- The IAAC chain-link and DS voltage ratings are reduced compared to the conventional AAC, and it does not require any extra FB cells to operate over the whole PQ range.

8.2 Future research

Based on the research presented in this thesis, several areas for future investigation are proposed:

- Investigation of interoperability among different converter topologies and interaction with other types of HVDC equipment (e.g. DCCB, DC-DC converters, etc.), and on the hardware interactions due to passive component (e.g. cell capacitors, AC and DC filters) deterioration.
- Further system-level exploration of the functionalities of EMMC and IAAC, and their deployment in applications such as DC-DC converters.
- Exploration of the capabilities of the master controller under non-ideal operating conditions (e.g. increased communication delays) and validation using a small (laboratory) scale multi-terminal network based on the qMMC topology.
- Investigation on cell topologies incorporating different types of semiconductor device in order to improve efficiency.
- Investigation of the effects of transients on DC fault blocking VSC when they are under the control of 'grid forming' controllers.
- Further investigation of the IAAC under different AC and DC fault conditions, and validation through experimental hardware.

References

[1] D. Bodansky, "The United Nations framework convention on climate change: a commentary," *Yale J. Int'l l.*, vol. 18, p. 451, 1993.

[2] S. Oberthür and H. E. Ott, *The Kyoto Protocol: international climate policy for the 21st century*. Springer Science & Business Media, 1999.

[3] J. Rogelj, M. Den Elzen, N. Höhne, T. Fransen, H. Fekete, H. Winkler, R. Schaeffer, F. Sha, K. Riahi, and M. Meinshausen, "Paris agreement climate proposals need a boost to keep warming well below 2 c," *Nature*, vol. 534, no. 7609, p. 631, 2016.

[4] W. Winter, K. Kolharkar, L. Fischer, D. Klaar, O. Alonso, H. Vanderbroucke, L. Dale, U. Maarit, T. TENNET, and F. O. NORDEL, "European wind integration study (ewis)-towards a successful integration of wind power into european electricity grids," Technical report, ENTSO-E, Tech. Rep., 2007.

[5] C. Haggett, "Over the sea and far away? a consideration of the planning, politics and public perception of offshore wind farms," *Journal of Environmental Policy & Planning*, vol. 10, no. 3, pp. 289–306, 2008.

[6] T. Tsakiris, "Transmission investment problems in europe: Going beyond standard solutions," August 2014.

[7] A. Aristotelous, "Cyprus' energy systems & pathways to 2020 and 2025," Master's thesis, Department of Mechanical and Aerospace Engineering, 2018.

[8] D. Van Hertem and M. Ghandhari, "Multi-terminal vsc hvdc for the european supergrid: Obstacles," *Renewable and Sustainable Energy Reviews*, vol. 14, no. 9, pp. 3156–3163, 2010.

[9] J. Graham, G. Biledt, and J. Johansson, "Power system interconnections using hvdc links," in *Proceedings of the IX Symposium of Specialists in Electric Operational and Expansion Planning*. Citeseer, 2003.

[10] K. Meah and S. Ula, "Comparative evaluation of HVDC and HVAC transmission systems," in *IEEE Power Engineering Society General Meeting*. IEEE, 2007, pp. 1–5.

[11] P. Buijs, D. Bekaert, S. Cole, D. Van Hertem, and R. Belmans, "Transmission investment problems in europe: Going beyond standard solutions," *Energy Policy*, vol. 39, no. 3, pp. 1794–1801, 2011.

[12] N. Ahmed, A. Haider, D. Van Hertem, L. Zhang, and H.-P. Nee, "Prospects and challenges of future HVDC supergrids with modular multilevel converters," in *European Conference on Power Electronics and Applications*. IEEE, 2011, pp. 1–10.

[13] R. Marquardt, "Modular multilevel converter: An universal concept for HVDC-networks and extended DC-bus-applications," in *International Power Electronics Conference*, June 2010, pp. 502–507.

[14] L. Weimers, "HVDC light: a new technology for a better environment," *IEEE Power Engineering Review*, vol. 18, no. 8, pp. 19–20, 1998.

[15] K. Friedrich, "Modern hvdc plus application of vsc in modular multilevel converter topology," in *2010 IEEE International Symposium on Industrial Electronics*, July 2010, pp. 3807–3810.

[16] C. Barker and N. Kirby, "Reactive power loading of components within a modular multi-level hvdc vsc converter," in *IEEE Electrical Power and Energy Conference*. IEEE, 2011, pp. 86–90.

[17] O. Kuhn, P. Menke, R. Zurowski, T. Christ, S. Seman, G. Giering *et al.*, "2nd generation dc grid access for offshore wind farms: HVDC in an AC fashion," *CIGRE, Paris*, pp. 1–7, 2016.

[18] S. Seman, R. Zurowski, and C. Taratoris, "Interconnection of advanced type 4 wtgs with diode rectifier based hvdc solution and weak ac grids," in *International Workshop on Wind Integration*, 2015, pp. 1–7.

[19] S. Hungsasutra and R. M. Mathur, "Unit connected operator with diode valve rectifier scheme," *IEEE Transactions on Power Systems*, vol. 4, no. 2, pp. 538–543, May 1989.

[20] R. Gou, "Research on 1100kv/5500a ultra-high voltage thyristor valve key technology and its application," *IEEE Transactions on Power Electronics*, pp. 1–1, 2019.

[21] B. Williams, *Principles and Elements of Power Electronics: Devices, Drivers, Applications, and Passive Components*. Barry Williams, 2006.

[22] P. Bakas, L. Harnefors, S. Norrga, A. Nami, K. Ilves, F. Dijkhuizen, and H.-P. Nee, "A review of hybrid topologies combining line-commutated and cascaded full-bridge converters," *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 7435–7448, 2017.

[23] T. Tanaka, M. Nakazato, and S. Funabiki, "A new approach to the capacitor-commutated converter for hvdc-a combined commutation-capacitor of active and passive capacitors," in *Power Engineering Society Winter Meeting, 2001. IEEE*, vol. 2. IEEE, 2001, pp. 968–973.

[24] T. Isobe, D. Shiojima, K. Kato, Y. R. R. Hernandez, and R. Shimada, "Full-bridge reactive power compensator with minimized-equipped capacitor and its application to static var compensator," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 224–234, Jan 2016.

[25] H. Zhou, G. Yang, and J. Wang, "Modeling, analysis, and control for the rectifier of hybrid hvdc systems for dfig-based wind farms," *IEEE Transactions on Energy Conversion*, vol. 26, no. 1, pp. 340–353, March 2011.

[26] T. H. Nguyen, D. Lee, and C. Kim, "A series-connected topology of a diode rectifier and a voltage-source converter for an hvdc transmission system," *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 1579–1584, April 2014.

[27] P. Li, S. J. Finney, and D. Holliday, "Thyristor based modular multilevel converter with active full-bridge chain-link for forced commutation," in *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, June 2016, pp. 1–6.

[28] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, "Vsc-based hvdc power transmission systems: An overview," *IEEE Transactions on power electronics*, vol. 24, no. 3, pp. 592–602, 2009.

[29] B. Jacobson, Y. Jiang-Hafner, P. Rey, G. Asplund, M. Jeroense, A. Gustafsson, and M. Bergkvist, "Hvdc with voltage source converters and extruded cables for up to ±300 kv and 1000 mw," *CIGRE*, pp. 1–8, 2006.

[30] Y. Zhang, G. P. Adam, T. Lim, S. J. Finney, and B. Williams, "Voltage source converter in high voltage applications : multilevel versus two-level converters," in *9th IET International Conference on AC and DC Power Transmission*, Aug 2010, pp. 189–193.

[31] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for hvdc applications: Review on converter cells and functionalities," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 18–36, 2015.

[32] T. B. Soeiro and J. W. Kolar, "Novel 3-level hybrid neutral-point-clamped converter," in *IECON 2011-37th Annual Conference of the IEEE Industrial Electronics Society*. IEEE, 2011, pp. 4457–4462.

[33] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 4–17, Jan 2015.

[34] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 37–53, Jan 2015.

[35] G. P. Adam, I. Abdelsalam, J. E. Fletcher, G. M. Burt, D. Holliday, and S. J. Finney, "New efficient submodule for a modular multilevel converter in multiterminal hvdc networks," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4258–4278, 2017.

[36] G. P. Adam and I. E. Davidson, "Robust and generic control of full-bridge modular multilevel converter high-voltage DC transmission systems," *IEEE Transactions on Power Delivery*, vol. 30, no. 6, pp. 2468–2476, Dec 2015.

[37] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for HVDC applications: Review on converter cells and functionalities," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 18–36, Jan 2015.

[38] M. M. C. Merlin, T. C. Green, P. D. Mitcheson, D. R. Trainer, R. Critchley, W. Crookes, and F. Hassan, "The alternate arm converter: A new hybrid multilevel converter with DC-fault blocking capability," *IEEE Transactions on Power Delivery*, vol. 29, no. 1, pp. 310–317, Feb 2014.

[39] G. P. Adam, K. H. Ahmed, S. J. Finney, K. Bell, and B. W. Williams, "New breed of network fault-tolerant voltage-source-converter hvdc transmission system," *IEEE Transactions on Power Systems*, vol. 28, no. 1, pp. 335–346, Feb 2013.

[40] E. Amankwah, A. Costabeber, A. Watson, D. Trainer, O. Jasim, J. Chivite-Zabalza, and J. Clare, "The series bridge converter (sbc): A hybrid modular multilevel converter for hvdc applications," in *European Conference on Power Electronics and Applications*. IEEE, 2016, pp. 1–9.

[41] P. Li, G. P. Adam, D. Holliday, and B. Williams, "Controlled transition full-bridge hybrid multilevel converter with chain-links of full-bridge cells," *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 23–38, 2017.

[42] G. Adam, *Voltage Source Converter: modulation, modelling, control and applications in power systems*, 2014.

[43] D. Jovcic, D. Van Hertem, K. Linden, J.-P. Taisne, and W. Grieshaber, "Feasibility of dc transmission networks," in *2011 2nd IEEE PES International Conference and Exhibition on Innovative Smart Grid Technologies*. IEEE, 2011, pp. 1–8.

[44] G. P. Adam, I. A. Gowaid, S. J. Finney, D. Holliday, and B. W. Williams, "Review of dc–dc converters for multi-terminal hvdc transmission networks," *IET Power Electronics*, vol. 9, no. 2, pp. 281–296, 2016.

[45] I. A. Gowaid, G. P. Adam, A. M. Massoud, S. Ahmed, D. Holliday, and B. W. Williams, "Quasi two-level operation of modular multilevel converter for use in a high-power dc transformer with dc fault isolation capability," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 108–123, Jan 2015.

[46] D. Jovcic, "Bidirectional, high-power dc transformer," *IEEE Transactions on Power Delivery*, vol. 24, no. 4, pp. 2276–2283, 2009.

[47] J. Yang, Z. He, H. Pang, and G. Tang, "The hybrid-cascaded dc–dc converters suitable for hvdc applications," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5358–5363, 2015.

[48] G. J. Kish and P. W. Lehn, "A modular bidirectional dc power flow controller with fault blocking capability for dc networks," in *Workshop on Control and Modeling for Power Electronics*. IEEE, 2013, pp. 1–7.

[49] S. Wang, J. Guo, C. Li, S. Balasubramaniam, R. Zheng, and J. Liang, "Coordination of dc power flow controllers and ac/dc converters on optimising the delivery of wind power," *IET Renewable Power Generation*, vol. 10, no. 6, pp. 815–823, 2016.

[50] E. Veilleux and B.-T. Ooi, "Multiterminal hvdc with thyristor power-flow controller," *IEEE Transactions on Power Delivery*, vol. 27, no. 3, pp. 1205–1212, 2012.

[51] M. Ranjram and P. W. Lehn, "A multiport power-flow controller for dc transmission grids," *IEEE Transactions on Power Delivery*, vol. 31, no. 1, pp. 389–396, 2016.

[52] S. Balasubramaniam, C. E. Ugalde-Loo, J. Liang, T. Joseph, R. King, and A. Adamczyk, "Experimental validation of dual h-bridge current flow controllers for meshed hvdc grids," *IEEE Transactions on Power Delivery*, vol. 33, no. 1, pp. 381–392, 2018.

[53] J. Sau-Bassols, E. Prieto-Araujo, and O. Gomis-Bellmunt, "Modelling and control of an interline current flow controller for meshed hvdc grids," *IEEE Transactions on Power Delivery*, vol. 32, no. 1, pp. 11–22, 2017.

[54] C. D. Barker and R. S. Whitehouse, "A current flow controller for use in hvdc grids," in *10th IET International Conference on AC and DC Power Transmission (ACDC 2012)*, Dec 2012, pp. 1–5.

[55] W. Chen, X. Zhu, L. Yao, G. Ning, Y. Li, Z. Wang, W. Gu, and X. Qu, "A novel interline dc power-flow controller (idcpfc) for meshed hvdc grids," *IEEE Transactions on Power Delivery*, vol. 31, no. 4, pp. 1719–1727, 2016.

[56] C. M. Franck, "Hvdc circuit breakers: A review identifying future research needs," *IEEE Transactions on Power Delivery*, vol. 26, no. 2, pp. 998–1007, 2011.

[57] C. Meyer, S. Schroder, and R. W. De Doncker, "Solid-state circuit breakers and current limiters for medium-voltage systems having distributed power systems," *IEEE Transactions on Power Electronics*, vol. 19, no. 5, pp. 1333–1340, 2004.

[58] A. Lee, P. Slade, K. Yoon, J. Porter, and J. Vithayathil, "The development of a hvdc sf6 breaker," *IEEE Transactions on Power Apparatus and Systems*, no. 10, pp. 2721–2729, 1985.

[59] K. Tahata, S. Ka, S. Tokoyoda, K. Kamei, K. Kikuchi, D. Yoshida, Y. Kono, R. Yamamoto, and H. Ito, "Hvdc circuit breakers for hvdc grid applications," in *Technical Meeting 2014*. CIGRE, 2014.

[60] L. Ängquist, S. Norrga, and T. Modéer, "A new dc breaker with reduced need for semiconductors," in *European Conference on Power Electronics and Applications*. IEEE, 2016, pp. 1–9.

[61] F. P. Page, "Analysis in circuit breaker performance requirements for high-voltage dc networks," Ph.D. dissertation, University of Strathclyde, 2016.

[62] P. Ruffing, N. Collath, C. Brantl, and A. Schnettler, "Dc fault control and high-speed switch design for an hvdc network protection based on fault blocking converters," *IEEE Transactions on Power Delivery*, pp. 1–1, 2018.

[63] M. Callavik, A. Blomberg, J. Häfner, and B. Jacobson, "The hybrid hvdc breaker," *ABB Grid Systems Technical Paper*, vol. 361, pp. 143–152, 2012.

[64] C. C. Davidson, R. S. Whitehouse, C. D. Barker, J. . Dupraz, and W. Grieshaber, "A new ultra-fast hvdc circuit breaker for meshed dc networks," in *11th IET International Conference on AC and DC Power Transmission*, Feb 2015, pp. 1–7.

[65] W. Zhou, X. Wei, S. Zhang, G. Tang, Z. He, J. Zheng, Y. Dan, and C. Gao, "Development and test of a 200kv full-bridge based hybrid hvdc breaker," in *European Conference on Power Electronics and Applications*. IEEE, 2015, pp. 1–7.

[66] F. Page, S. Finney, D. Holliday, L. Xu, B. Williams, K. Tahata, M. Sato, R. Yamamoto, and H. Ito, "Optimisation of passive system components to minimize dc circuit breaker stresses in multi-terminal systems," in *CIGRE symposium Lund*, vol. 134, 2015.

[67] T. Hoshino, K. M. Salim, M. Nishikawa, I. Muta, and T. Nakamura, "Proposal of saturated dc reactor type superconducting fault current limiter (sfcl)," *Cryogenics*, vol. 41, no. 7, pp. 469–474, 2001.

[68] C. Nentwig, J. Haubrock, R. H. Renner, and D. V. Hertem, "Application of dc choppers in hvdc grids," in *2016 IEEE International Energy Conference (ENERGYCON)*, April 2016, pp. 1–5.

[69] E. F. Vance, *Coupling to shielded cables*. Wiley, 1978.

[70] T. K. Vrana, Y. Yang, D. Jovcic, S. Dennetière, J. Jardini, and H. Saad, "The cigre b4 dc grid test system," *Electra*, vol. 270, no. 1, pp. 10–19, 2013.

[71] R. Wachal, A. Jindal, S. Dennetiere, H. Saad, O. Rui, S. Cole, M. Barnes, L. Zhang, Z. Song, J. Jardini *et al.*, "Guide for the development of models for hvdc converters in a hvdc grid," *CIGRE TB604 (WG B4. 57), Paris, Tech. Rep*, 2014.

[72] H. Saad, S. Dennetiere, J. Mahseredjian, P. Delarue, X. Guillaud, J. Peralta, and S. Nguefeu, "Modular multilevel converter models for electromagnetic transients," *IEEE Transactions on Power Delivery*, vol. 29, no. 3, pp. 1481–1489, June 2014.

[73] H. Saad, S. Dennetière, and J. Mahseredjian, "On modelling of MMC in emt-type program," in *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, June 2016, pp. 1–7.

[74] S. Heinig, K. Ilves, S. Norrga, and H. P. Nee, "On energy storage requirements in alternate arm converters and modular multilevel converters," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Sept 2016, pp. 1–10.

[75] M. M. C. Merlin and T. C. Green, "Cell capacitor sizing in multilevel converters: cases of the modular multilevel converter and alternate arm converter," *IET Power Electronics*, vol. 8, no. 3, pp. 350–360, 2015.

[76] V. Najmi, R. Burgos, and D. Boroyevich, "Design and control of modular multilevel alternate arm converter (aac) with zero current switching of director switches," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2015, pp. 6790–6797.

[77] B. Jacobson, P. Karlsson, G.Asplund, L.Harnnart, and T. Jonsson, "VSC-HVDC transmission with cascaded two-level converters," in *CIGRE*, August 2014.

[78] Dynex, "Dim1500esm33-tl000," November 2016, Single Switch IGBT Module.

[79] F. J. Moreno, M. M. C. Merlin, D. R. Trainer, T. C. Green, and K. J. Dyke, "Zero phase sequence voltage injection for the alternate arm converter," in *11th IET International Conference on AC and DC Power Transmission*, Feb 2015, pp. 1–6.

[80] J. He, T. Zhao, X. Jing, and N. A. Demerdash, "Application of wide bandgap devices in renewable energy systems-benefits and challenges," in *Proceedings of the International Conference on Renewable Energy Research and Application (ICRERA), Milwaukee, WI, USA*, 2014, pp. 19–22.

[81] K. Hamada, S. Hino, N. Miura, H. Watanabe, S. Nakata, E. Suekawa, Y. Ebiike, M. Imaizumi, I. Umezaki, and S. Yamakawa, "3.3 kv/1500 a power modules for the world's first all-sic traction inverter," *Japanese Journal of Applied Physics*, vol. 54, no. 4S, p. 04DP07, 2015.

[82] Cree, "Cas300m17bm2," 2014, Half-Bridge Module.

[83] L. Paulsson, B. Ekehov, S. Halen, T. Larsson, L. Palmqvist, A. A. Edris, D. Kidd, A. J. F. Keri, and B. Mehraban, "High-frequency impacts in a converter-based back-to-back tie; the eagle pass installation," *IEEE Transactions on Power Delivery*, vol. 18, no. 4, pp. 1410–1415, Oct 2003.

[84] M. Marzinotto and G. Mazzanti, "The statistical enlargement law for HVDC cable lines part 1: theory and application to the enlargement in length," *IEEE Transactions on Dielectrics and Electrical Insulation*, vol. 22, no. 1, pp. 192–201, Feb 2015.

[85] O. Despouys, A. Petit, P. Rault, T. Larsson, K. Hämynen, M. Zeller, A. Rentschler, S.Finney, D. Vozikis, J. Freytes, X. Guillaud, S. Gao, J. Rimez, A. Burgos, L. Coronado, and C. Longás, "First recommendations to enhance interoperability in hvdc-vsc multivendor schemes," http://www.bestpaths-project.eu, October 2016.

[86] E. M. Farr, R. Feldman, J. C. Clare, A. J. Watson, and P. W. Wheeler, "The alternate arm converter (aac) - short-overlap mode operation - analysis and design parameter selection," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1–1, 2017.

[87] M. M. C. Merlin, D. S. Sanchez, P. D. Judge, G. Chaffey, P. Clemow, T. C. Green, D. R. Trainer, and K. J. Dyke, "The extended overlap alternate arm converter: A voltage source converter with dc fault ride-through capability and a compact design," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1–1, 2017.

[88] U. Karaagac, J. Mahseredjian, L. Cai, and H. Saad, "Offshore wind farm modeling accuracy and efficiency in mmc-based multiterminal hvdc connec-

tion," *IEEE Transactions on Power Delivery*, vol. 32, no. 2, pp. 617–627, 2017.

[89] S. Dennetière, S. Nguefeu, H. Saad, and J. Mahseredjian, "Modeling of modular multilevel converters for the france-spain link," *Star*, vol. 2, no. 3, p. 4, 2013.

[90] M. Fu, L. A. Dissado, G. Chen, and J. C. Fothergill, "Space charge formation and its modified electric field under applied voltage reversal and temperature gradient in xlpe cable," *IEEE Transactions on Dielectrics and Electrical Insulation*, vol. 15, no. 3, pp. 851–860, 2008.

[91] A. Morched, B. Gustavsen, and M. Tartibi, "A universal model for accurate calculation of electromagnetic transients on overhead lines and underground cables," *IEEE Transactions on Power Delivery*, vol. 14, no. 3, pp. 1032–1038, July 1999.

[92] X. Shi, B. Liu, Z. Wang, Y. Li, L. M. Tolbert, and F. Wang, "Modeling, control design, and analysis of a startup scheme for modular multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 11, pp. 7009–7024, Nov 2015.

[93] J. Hu, K. Xu, L. Lin, and R. Zeng, "Analysis and enhanced control of hybrid-mmc-based hvdc systems during asymmetrical dc voltage faults," *IEEE Transactions Power Deliv*, vol. 32, no. 3, pp. 1394–1403, 2017.

[94] J. Li, G. Konstantinou, H. R. Wickramasinghe, and J. Pou, "Operation and control methods of modular multilevel converters in unbalanced ac grids: A review," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2018.

[95] S. Wang, G. P. Adam, A. M. Massoud, D. Holliday, and B. W. Williams, "Analysis and assessment of modular multilevel converter internal control schemes," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2019.

[96] H. Saad, T. Ould-Bachir, J. Mahseredjian, C. Dufour, S. Dennetière, and S. Nguefeu, "Real-time simulation of mmcs using cpu and fpga," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 259–267, Jan 2015.

[97] S. D'Arco, R. Torres, K. Ljøkelsøy, G. Guidi, T. Reigstad, and G. Bergna, "Detailed specification of the demonstrator," http://www.bestpaths-project.eu, December 2016.

[98] K. Ilves, A. Antonopoulos, S. Norrga, and H.-P. Nee, "Steady-state analysis of interaction between harmonic components of arm and line quantities of modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 27, no. 1, pp. 57–68, Jan 2012.

[99] T. Williams, *EMC for product designers*. Newnes, 2016.

[100] Infineon, "Ikw40n120h3," November 2014, Single Switch IGBT Module.

[101] L. Harnefors, A. Antonopoulos, S. Norrga, L. Angquist, and H. P. Nee, "Dynamic analysis of modular multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 7, pp. 2526–2537, July 2013.

[102] S.-H. Ryu, C. Capell, C. Jonas, L. Cheng, M. O'Loughlin, A. Burk, A. Agarwal, J. Palmour, and A. Hefner, "Ultra high voltage (> 12 kV), high performance 4h-sic igbts," in *Power Semiconductor Devices and ICs (ISPSD), 2012 24th International Symposium on*. IEEE, 2012, pp. 257–260.

[103] M. Tsili and S. Papathanassiou, "A review of grid code technical requirements for wind farms," *IET Renewable power generation*, vol. 3, no. 3, pp. 308–332, 2009.

[104] N. Ahmed, L. Angquist, S. Mahmood, A. Antonopoulos, L. Harnefors, S. Norrga, and H. P. Nee, "Efficient modeling of an MMC-based multiterminal DC system employing hybrid HVDC breakers," *IEEE Transactions on Power Delivery*, vol. 30, no. 4, pp. 1792–1801, Aug 2015.

[105] F. Deng and Z. Chen, "Voltage-balancing method for modular multilevel converters under phase-shifted carrier-based pulsewidth modulation," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 7, pp. 4158–4169, July 2015.

[106] J. Mei, K. Shen, B. Xiao, L. M. Tolbert, and J. Zheng, "A new selective loop bias mapping phase disposition pwm with dynamic voltage balance capability for modular multilevel converter," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 2, pp. 798–807, Feb 2014.

[107] K. Wang, Y. Deng, H. Peng, G. Chen, G. Li, and X. He, "An improved cps-pwm scheme based voltage balancing strategy for mmc with fundamental frequency sorting algorithm," *IEEE Transactions on Industrial Electronics*, vol. PP, no. 99, pp. 1–1, 2018.

[108] K. Wang, Y. Li, Z. Zheng, and L. Xu, "Voltage balancing and fluctuation-suppression methods of floating capacitors in a new modular multilevel converter," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 5, pp. 1943–1954, May 2013.

[109] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 24, no. 7, pp. 1737–1746, July 2009.

[110] Z. Ali, N. Christofides, L. Hadjidemetriou, E. Kyriakides, Y. Yang, and F. Blaabjerg, "Three-phase phase-locked loop synchronization algorithms for grid-connected renewable energy systems: A review," *Renewable and Sustainable Energy Reviews*, vol. 90, pp. 434–452, 2018.

[111] L. Cai, U. Karaagac, and J. Mahseredjian, "Simulation of startup sequence of an offshore wind farm with MMC-HVDC grid connection," *IEEE Transactions on Power Delivery*, vol. 32, no. 2, pp. 638–646, 2017.

[112] R. Li, J. E. Fletcher, and B. W. Williams, "Influence of third harmonic injection on modular multilevel converter -based high-voltage direct current transmission systems," *IET Generation, Transmission and Distribution*, vol. 10, no. 11, pp. 2764–2770, 2016.

[113] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Transactions on Power Delivery*, vol. 26, no. 3, pp. 2009–2017, July 2011.

[114] S. Li, X. Wang, Z. Yao, T. Li, and Z. Peng, "Circulating current suppressing strategy for MMC-HVDC based on nonideal proportional resonant controllers under unbalanced grid conditions," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 387–397, Jan 2015.

[115] S. Samimi, F. Gruson, P. Delarue, F. Colas, M. M. Belhaouane, and X. Guillaud, "MMC stored energy participation to the DC bus voltage control in an HVDC link," *IEEE Transactions on Power Delivery*, vol. 31, no. 4, pp. 1710–1718, Aug 2016.

[116] E. Farr, R. Feldman, A. Watson, J. Clare, and P. Wheeler, "A sub-module capacitor voltage balancing scheme for the alternate arm converter (aac)," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, Sept 2013, pp. 1–10.

[117] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," *IEEE Transactions on Power Delivery*, vol. 25, no. 4, pp. 2903–2912, Oct 2010.

[118] F. Yu, W. Lin, X. Wang, and D. Xie, "Fast voltage-balancing control and fast numerical simulation model for the modular multilevel converter," *IEEE Transactions on Power Delivery*, vol. 30, no. 1, pp. 220–228, Feb 2015.

Appendix A

Controller

This Appendix presents and describes the various controller structures that are used for the off-line simulations and the hardware test-rig.

A.1 Master controller

The master controller is responsible for managing the whole AC/DC transmission system and adjusts power flow according to the system's power demand, ensuring swift DC grid response to power requirements. The master controller can compensate for various uncertainties that occur in the DC grid, such as:

- Error in the wind forecast which results in unexpected power extraction from the WF.
- Unavailability of WFs due to weather conditions, faults and scheduled maintenance.
- Unexpected power bottlenecks in AC grids.
- Unexpected unavailability of onshore power stations due to faults or scheduled maintenance.

The master controller manages and coordinates all the converters in the network to achieve the desired operation. To achieve this, it must be able to:

- Share the wind power forecast error with several onshore converter stations.
- Share the power deviation due to unavailability of one converter station.
- Limit wind power injection if onshore converter stations cannot accept more power.

- Coordinate AC and DC protection actions during AC and DC fault ride-through, benefiting from diversity of capabilities that different converter topologies offer.
- Coordinate converter operation during faults with their respective AC grids, including execution of DC network reconfiguration.
- Dictate WF operation according to extreme weather conditions and regulate the power exchange among the onshore and offshore converter stations.

As a result, the general operation of the master controller is to define the control mode of each converter, while adjusting the active/reactive power, and DC voltage references. It sets the signals that are responsible for the energisation of the system, the protection system, and additionally signals that are needed to operate or start in non-normal modes such as black start and islanding mode.

A.2 Outer controller

The outer controller sets the reference values for the inner controller by measuring the AC and DC voltages and currents in order to sustain desirable converter operation regarding active and reactive power, and DC voltage. Moreover, it sets the operation during unbalanced operation. The measurements are filtered through an antialiasing low-pass filter in order to reject high-frequency switching components. In the case of multilevel converters the minimum effective switching frequency which determines the resolution of the produced AC voltage is given by A.1

$$f_{eff} \geq 4 \cdot N \cdot f \tag{A.1}$$

where N is the number of levels in each arm and f is the fundamental frequency.

A.2.1 Positive sequence current controller references

The reference set-points for the positive dq sequence current controller is determined from the set of outer controllers. The reference for the d component of the current controller can be set according to the real power extraction, the DC voltage set value, or the output of a droop controller. In general, there are two variants of the droop controller: one which sets the active power according to the DC voltage and another which sets the DC voltage according to active power. The q component reference can be set according to reactive power or the AC voltage set value.

The DC voltage controller is implemented as a PI controller. The DC-side voltage deviation V_{DC}^*-V_{DC} is a measure of the power mismatch on the DC side. To achieve proper power balancing, at least one voltage controlling element is required on the DC side. Integral action in (A.2) will bring the voltage back to its reference V_{DC}^* and thereby restore the power balance.

$$i_d^{*+} = k_p(V_{DC}^* - V_{DC}) + \int (V_{DC}^* - V_{DC})dt \tag{A.2}$$

The active power controller is implemented as a feed-forward scheme. If more accurate tracking is required, a combined feed-forward and feedback control scheme could be applied.

$$i_d^{*+} = \frac{P^*}{\frac{3}{2}V_d} \tag{A.3}$$

$$i_d^{*+} = k_p(P^* - P) + k_i \int (P^* - P)dt \tag{A.4}$$

Also, as well as fixed reference current control, droop controller can regulate DC voltage or active power.

$$i_d^{*+} = \frac{P^*}{\frac{3}{2}V_d} + dV_{DC} \tag{A.5}$$

$$\begin{aligned} i_d^{*+} &= k_p\big(P^* - P) + \beta_p(V_{DC}^* - V_{DC})\big) + \\ &+ \int \big((P^* - P) + \beta_p(V_{DC}^* - V_{DC})\big)dt \end{aligned} \tag{A.6}$$

where β_P is the droop value for the power controller according to DC voltage threshold dV_{DC}. The overall structure of the i_d^{*+} controller is shown in Fig. A.1.

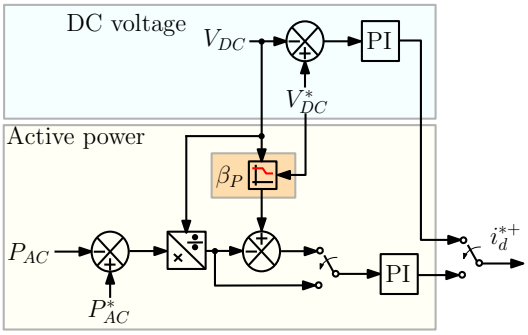


Figure A.1: Active component reference controller.

The reactive power controller is implemented in the same way as the active power controller.

$$i_q^{*+} = \frac{Q^*}{\frac{3}{2}V_q} \tag{A.7}$$

$$i_q^{*+} = k_p(Q^* - Q) + k_i \int (Q^* - Q)dt \tag{A.8}$$

By measuring the AC-Grid voltage and comparing it to a reference value, the VSC is also able to control the AC-side voltage directly or by using a droop controller as shown in (3.31)

$$\begin{aligned} i_q^{*+} &= k_p\big((U_{AC}^* - U_{AC}) + \beta_Q(Q^* - Q)\big) + \\ &+ \int \big((U_{AC}^* - U_{AC}) + \beta_Q(Q^* - Q)\big)dt \end{aligned} \tag{A.9}$$

where β_Q is the droop value for the AC voltage controller. The overall structure of the i_q^{*+} controller is shown in Fig. A.2.

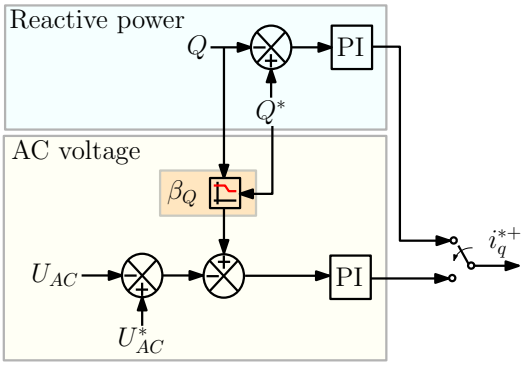


Figure A.2: Reactive component reference controller.

A.2.2 Negative sequence current controller references

The reference set-points for the negative dq sequence current controller can vary according to the scheme or the operator requirement. Setting the reference of the negative sequence current controller can vary according to the operational objective, which may be to

- Balance the AC converter currents.
- Balance the internal converter currents.
- Balance the internal energy stored.
- Extract constant active power.
- Extract constant reactive power.

The converter is able to withstand the various internal imbalances, as the sizing of either voltage or currents during AC unbalance in covered by the current thermal limits and voltage insulation thresholds. As a result, the scheme followed is to balance the AC-side converter currents where is crucial for the safety of the AC grid. As a result both components of the negative sequence current are suppressed to zero with i_d^{*-}=0 and i_q^{*-}=0, and active/reactive power and DC voltages are set by positive sequence currents.

A.2.3 Current limiter

In order to reduce the any potential overloading, the current references are limited, as shown in Fig. A.3. The limited current reference is compared to the calculated current reference. The scheme of limiting the reference current depends on the application. For example, if the converter is connected to a strong network, the positive sequence d current reference i_d^{*+} will have priority in order to produce as much power as possible when the current limit is exceeded. If the converter is connected to a weak network the converter has to give priority to the positive sequence q current reference i_q^{*+} in order to support the AC voltage when the current is limited.

$$i^*_{d_{lim}} = \begin{cases} i_{d_{lim}} = \sqrt{i^2_{lim} - i^{*2}_d} & \text{Priority in active power} \\ 1.1 p.u. & \text{Priority in reactive power} \end{cases} \tag{A.10}$$

$$i^*_{q_{lim}} = \begin{cases} i_{q_{lim}} = \sqrt{i^2_{lim} - i^{*2}_q} & \text{Priority in active power} \\ 1.1 p.u. & \text{Priority in reactive power} \end{cases} \tag{A.11}$$

A.3 Inner controller

The current controller considers the positive and negative sequence voltages and currents, suitable for balanced and unbalanced grid operation. During unbalance operation only the negative sequence components are transferred through the transformer whilst any zero sequence currents do not have any path due to high impedance grounding.

The frequency and phase must be detected at the connection point in order to synchronise the conversion and control system with the grid. This action is performed by the phase locked loop (PPL). The PLL will provide the phase angle that will be used to transform the abc reference system into dq [110]. The positive

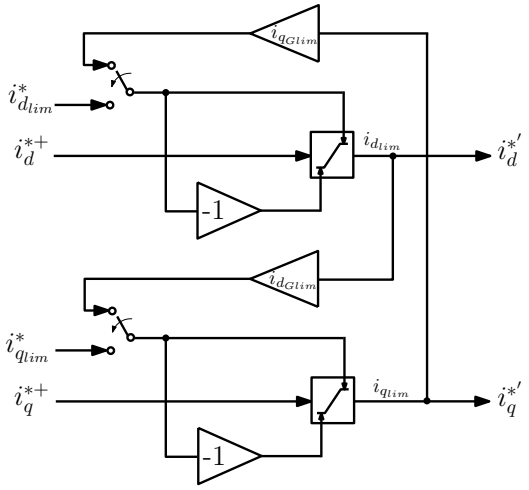


Figure A.3: Current limiter.

and negative sequence components are extracted through *abc* to *dq* transformation, fed with the sign of the angle from the PLL as shown in Fig. A.4.

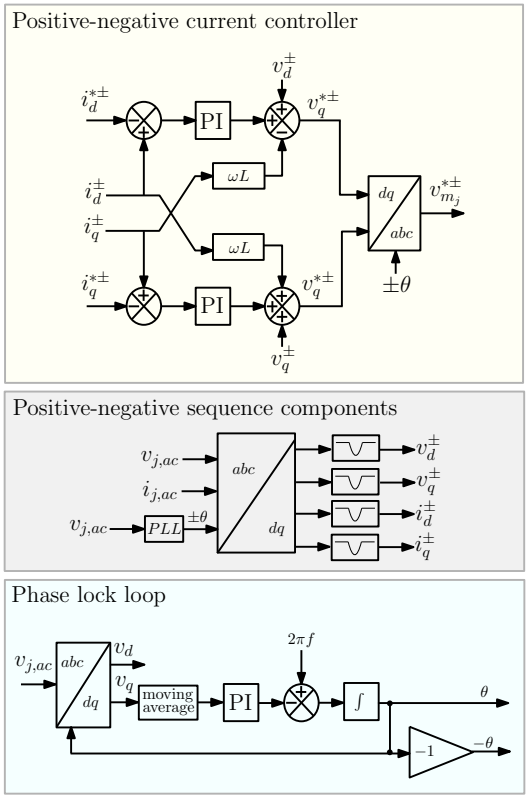


Figure A.4: Positive and negative inner current controller with the generated components.

The two reference current $i^{*\pm}_d$ and $i^{*\pm}_q$ are input to the current controller.

This stage produces the reference d and q voltages $v_d^{*\pm}$ and $v_q^{*\pm}$ which are transformed into abc components and sent to the lower level controllers. The current controllers are identical for both positive and negative sequences.

From (3.11) therefore, the positive and negative dq state equations are:

$$e_q - V_{AC_d} = \left(\frac{L_{arm}}{2} + L_{AC}\right) \cdot \frac{di_d}{dt} + \left(\frac{R_{arm}}{2} + R_{AC}\right) i_d - i_q \left(\frac{L_{arm}}{2} + L_{AC}\right) \omega \quad \text{(A.12)}$$

$$e_d - V_{AC_q} = \left(\frac{L_{arm}}{2} + L_{AC}\right) \cdot \frac{di_q}{dt} + \left(\frac{R_{arm}}{2} + R_{AC}\right) i_d + i_d \left(\frac{L_{arm}}{2} + L_{AC}\right) \omega \quad \text{(A.13)}$$

The dq positive and negative voltage references $v_d^{*\pm}$ and $v_q^{*\pm}$ are shown (A.14) and (A.14).

$$v_d^{*\pm} = \left(k_p(i_d^{*\pm} - i_d^{\pm}) + k_i \int (i_d^{*\pm} - i_d^{\pm}) dt\right) + e_d^{\pm} - i_q^{\pm} \left(\frac{L_{arm}}{2} + L_{AC}\right) \omega \quad \text{(A.14)}$$

$$v_q^{*\pm} = \left(k_p(i_q^{*\pm} - i_q^{\pm}) + k_i \int (i_q^{*\pm} - i_q^{\pm}) dt\right) + e_q^{\pm} - i_d^{\pm} \left(\frac{L_{arm}}{2} + L_{AC}\right) \omega \quad \text{(A.15)}$$

By composing the negative sequence dq transformation through the opposite sign of the angle from the PLL a double fundamental frequency occurs (100 Hz). Therefore, a band-stop filter tuned to double the fundamental frequency is employed. Moreover, such a filter is beneficial for the positive sequence current control as it rejects grid disturbances and also allows operation in medium strength and weak networks.

A.4 Islanding mode

One of the advantages of the VSC technology is that it is possible to connect very low inertia systems, such as an islanded system or a WF, or even perform temporary islanding scenarios, such as black start of a system. The VSC can produce its own AC voltage waveform independent of the AC system. The converter can be connected to an AC system with passive load or with asynchronous generation (e.g. WF). Islanding operation dictates the angle reference from a fixed value, and not a PLL which is used in non-islanded applications, as shown in Fig. A.5. In the islanded case the converter directly controls the AC voltage magnitude according to a fixed frequency, without being able to control the active power extraction or the DC voltage [111].

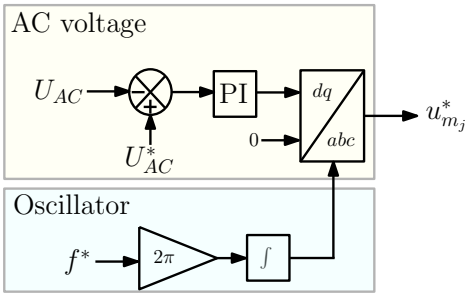


Figure A.5: Non-PLL frequency reference (V/f) controller for islanded mode.

A.5 Valve balance controller

The valve balance controller manages converter valve energy, in order to enhance the converter controllability or to increase the efficiency of the converter by minimising the circulating currents in the converter. This layer of the control is not critical for converter operation and can be disabled at any time if it creates instabilities in the control system.

A.5.1 MMC

In the MMC the valve balance controller ensures the vertical and horizontal stability of the converter's internal dynamic energy imbalances. The vertical controller ensures energy balance among the internal phases of the converter while the horizontal controller ensures energy balance between the arms of each phase of the converter. These dynamic imbalances are mainly due to the tolerances of installed passive and active components, such as arm inductances and cell capacitors. In MMC this may lead to a fluctuation of energy in each phase which, in turn, will generate circulating currents.

A.5.2 Third harmonic injection in MMC

Traditionally, the third harmonic injection (THI) technique is used to extend the modulation index linear range and improve DC link utilisation in order to improve converter PQ capability [112]. The third harmonic voltage injected into the modulated signals is described by (A.16).

$$v_{THI} = \frac{\min(v_a^*, v_b^*, v_c^*) + \max(v_a^*, v_b^*, v_c^*)}{2} \tag{A.16}$$

THI permits MMC to operate with a higher range of converter AC voltages, which is beneficial in terms of potential reduction in transformer and arm currents for

the same power transfer. Equation (A.17) describes the implementation of THI in an MMC.

$$m_{j_{MMC}} = v_{m_j} - v_{THI} \tag{A.17}$$

A.5.3 Circulating current controller

There are various methods for active suppression of the circulating currents, which mainly affect the magnitude of the arm current, cell voltage ripple and the semiconductor losses. However due to the nature of the circulating current, PI control is not appropriate for sinusoidal quantities [113]. An alternative implementation is a PR controller which theoretical has infinite gain at the tuned frequencies [114].

From (3.14) the circulating current which is driven from the common-mode voltage can be describes as

$$dV_j = 2R_{arm} \cdot i_{j,cc} + 2L_{arm} \cdot \frac{i_{j,cc}}{dt} \tag{A.18}$$

The circulating current controller, implemented using the non-ideal PR technique is

$$dV_j = K_{p,cc} \cdot i_{j,cc} + K_{r,cc} \cdot \frac{2\zeta\omega_r s}{s^2 + 2\zeta\omega_r s + \omega_r^2} \tag{A.19}$$

where ζ the damping is factor and ω_r is the desired frequency to suppress, in radians per second. Other frequencies, such as the 1st, 3rd and 4th order harmonics, can be suppressed by employing parallel controllers tuned at these frequencies. The characteristics of the PR controller are $K_{p,cc} = 439.823$, $K_{r,cc} =$

In order to have a more effective controller, the DC component from the common-mode current is rejected using a high-pass filter. The overall structure of the PR circulating current suppressing controller (CCSC) is shown in Fig. A.6.

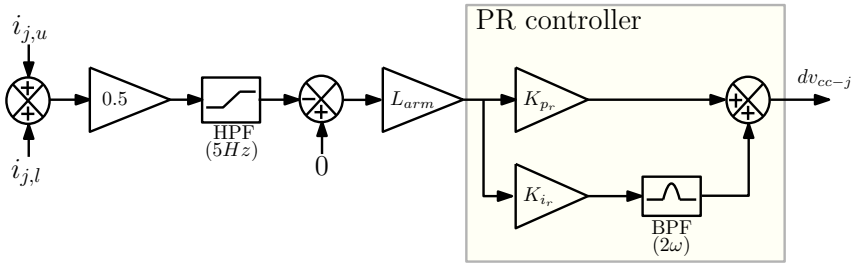


Figure A.6: PR circulating current suppressing controller.

A.5.4 Energy controller

The energy controller is employed to ensure energy balance between the upper and lower arms in each phase. It also decouples cell capacitor voltage regulation, and hence the AC voltage, from the DC link. In this manner, the energy stored in the cell capacitors can be manipulated to adjust DC components of the modulation signals[115]. There are two main approaches to valve energy control. The first calculates energy according to measured voltage and installed capacitance. The second implies energy based only on voltage measurement. The first method may be subject to error due to capacitor tolerances. This error is avoided by the second method which does not rely upon knowledge of the capacitor values.

The horizontal energy control is based on controlling the total energy between the upper and lower arms in each phase, which allows regulated energy exchanged between the AC and DC sides. A PI controller regulates the total energy $W_{sum,j}$, defined in (A.20), according to a reference which may be either user defined or based on DC voltage measurement which reflects the energy stored in the DC grid. The latter approach means that the capacitor voltages are set according to the energy stored in the DC grid, hence providing better response to DC voltage dynamics.

$$W_{sum,j} = C_{arm}\frac{d(v^2_{Ctot_{j,u}} + v^2_{Ctot_{j,l}})}{dt} = \frac{1}{2}(m_{DC_{j,k}} - 1)i_{j,DC} \tag{A.20}$$

The right-hand term of equation (A.21) is considered to be the energy exchange between the AC and DC sides for each phase.

$$m_{DC,E_j} = \frac{1}{2}(m_{DC_{j,k}} - 1) \cdot i_{j,_{DC}} = P_{AC_j} - P_{DC_j} \tag{A.21}$$

The m_{DC,E_j} component regulates the total phase capacitor voltage through a PI controller. The purpose of the horizontal energy controller is to regulate the DC component of the common-mode current, therefore a band-stop filter is employed to reject the 2ω frequency components that appear through the summation of the total arm capacitor voltages in a given phase. Moreover, a feedforward AC power component is applied for improved dynamics.

Vertical energy control is based on controlling the energy among the internal phases of the converter and minimising any potential energy mismatches between the arms. The differential energy of each phase is defined by (A.22).

$$C_{arm}\frac{d(v^2_{Ctot_{j,u}} - v^2_{Ctot_{j,l}})}{dt} = \frac{1}{2}m_{DC_{j,k}} \cdot i_{j,AC} - \frac{1}{2}m_j \cdot i_{j,cm} \tag{A.22}$$

The right-hand term of the equation (A.22) is considered to be the energy balance between the upper and lower arms of each phase.

$$m_{AC,E_j} = \frac{1}{2}\left(\left(m_{DC_{j,k}} \cdot i_{j,AC}\right) - i_{j,cm}\right) \tag{A.23}$$

The purpose of the vertical energy controller is to equalise the upper and lower arm energies, suppressing any DC component difference between the arms. Hence the reference value for the differential energy $W_{diff,j}$ is set to zero.

Fig. A.7 illustrates the architecture of the vertical and horizontal energy controller, and the total energy current correction dv_{W-j}. In general, the MMC valve

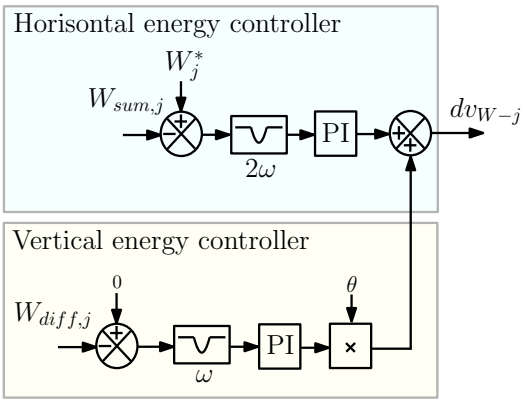


Figure A.7: MMC horizontal and vertical energy controllers.

balance control is considered to be an enhancement rather than a control requirement. The circulating current controller increase the efficiency of the converter by reducing the root mean square (RMS) value of the arm currents by suppressing the second harmonic currents. The vertical and horizontal energy controllers allow improved DC voltage dynamics. However, it has been noticed that in case of system instability, the valve balance controllers may be disabled to provide safe operation without jeopardising the continuous operation of the converter.

A.5.5 AAC

In AAC the valve balance control ensures the accurate and safe transfer of energy between the upper and lower arms during the overlap period. Also it improves the output power quality for a large range of modulation indices and power factors.

A.5.6 Third harmonic injection in AAC

THI extends the period where the AAC operates as an MMC by modifying the voltage profile in the region of zero voltage crossover [79]. This results in a more efficient operation during the overlap period, and allows better dynamics during the energy equilibrium between the upper and lower arms regardless of the overlap period. In AAC, THI removes the necessity for current injection from a star-connected transformer, and reduces the DC filtering requirements. Equation (A.14) describes the implementation of THI in an AAC.

$$m_{j_{AAC}} = v_{m_j} + v_{THI} \tag{A.24}$$

A.5.7 Overlap angle controller (AAC)

This type of controller exists only in AAC converters, and regulates the period during which both arms conduct simultaneously [76, 116]. During unity power factor operation, the arm currents are in phase with the arm voltages and therefore the DS can operate in soft-switching mode. However during reactive power injection the arm currents are phase shifted with respect to the arm voltages, hence the DS start to operate in hard-switching mode. Even with the incorporation of third harmonic injection the current has still a high value as the load is mainly inductive and the arm current has a sinusoidal profile. As a result, a more sophisticated overlap angle controller is used, in order to actively regulate and operate the DS according to the energy stored in the chain-links and the arm current magnitude. The overlap angle controller, defined in (A.25), operates in a similar manner as the horizontal energy controller of an MMC.

$$C_{arm}\frac{d(v^2_{Ctot_{j,u}} + v^2_{Ctot_{j,l}})}{dt} = m_{DC_{j,k}} \cdot i_{j,DC} \tag{A.25}$$

The right-hand term of equation (A.26) is considered to be the energy exchange between the AC and DC sides for each phase.

$$m_{DC,E_j} = m_{DC_{j,k}} \cdot i_{j,DC} = P_{AC_j} - P_{DC_j} \tag{A.26}$$

The target is to equalise the energy among the phases, dictating the operation of DS. Fig. A.8 illustrates the structure of the overlap controller.

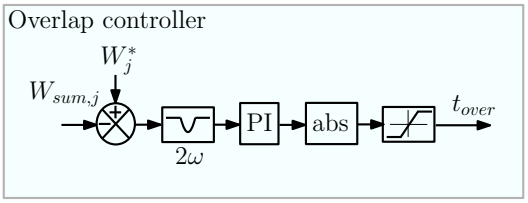
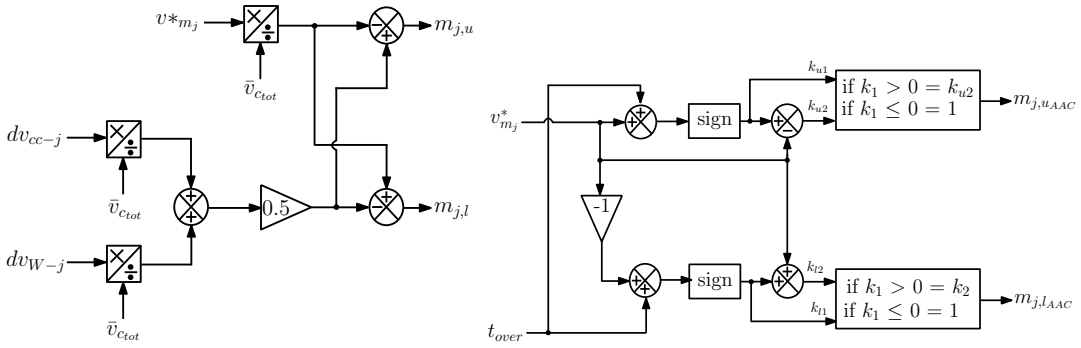


Figure A.8: AAC overlap controller.

A.6 Normalisation

Normalisation creates the final reference for the lower level controller for each arm of the converter. The normalised controllers must be combined in such a way as to ensure that the modulation indices generated for each arm will not attempt to exceed the capabilities of the converter. Fig. A.9 illustrates the normalisation of the controllers for the MMC and AAC topologies.



(a) MMC (b) AAC

Figure A.9: Signal normalisation.

A.7 Controller tuning

The transfer function for the PI controller is described as:

$$G(s) = \frac{1 + K_p + T_i s}{T_i s^2 + K_p T_i s + 1} \tag{A.27}$$

where k is the tunable parameter of the system (e.g. inductance or capacitance).

The gains K_p and T_i are calculated according to the second-order transfer function T^{2nd} characterisation as:

$$T^{2nd} = \frac{1}{\omega_n^2} s^2 + \frac{2\zeta}{\omega_n} + 1 \tag{A.28}$$

where ζ is the damping ration and $\omega_n = 2\pi f$ is the natural frequency of the system response. The gains K_p and T_i are chosen as:

$$K_p = 2\zeta\omega_n k \tag{A.29}$$

$$T_i = \frac{1}{\omega_n^2 k} \tag{A.30}$$

For an over-damped system with $\zeta = 0.7$, the response time τ_r can be related with the ω_n as described as:

$$\omega_n = \frac{3}{\tau_r} \tag{A.31}$$

The overall system control parameters are shown in Table A.1.

Table A.1: System control parameters.

Controllers	**Control Parameters**	
	K_p	T_i
Outer controller		
Active power controller	0	14
Reactive power controller	0	14
AC voltage controller	0	14
V_{DC} controller	9.6	293.878
V/f controller	0	30
Inner controller		
Positive and negative sequence current controller	0.487	149.086
Auxiallary controllers		
Circulating current suppressing controller	439	25132.74
Vertical energy controller	3	0.006
Horisontal energy controller	3	0.006
AAC overlap controller	3	0.006

A.8 Lower level controller

Arm balance control is used for both MMC and AAC, to achieve equal cell voltage.

A.8.1 Modulation techniques

Various modulation techniques have been introduced for modular converters, such as multicarrier pulse width modulation (PWM), nearest level control (NLC),

selective harmonic elimination (SHE) and space vector modulation (SVM). As the number of levels increases techniques such as SHE and SVM become quite complex and difficult to implement. As a result, techniques such as NLC and PWM, which are simple and easy to apply, are preferred.

A.8.2 PWM

In the multicarrier PWM modulation strategy, triangular carrier waveforms are compared with the reference voltage. Each carrier represents a voltage stage level. There are different approaches to the multicarrier PWM modulation strategy, such as phase disposition (PD), phase opposition disposition (POD), and alternative phase opposition disposition (APOS). However, PD carriers are preferred because they produce output voltage with better harmonic distribution and lower THD. Selecting the frequency for the carrier is crucial. High carrier frequency might increase converter switching losses, and create EMI during high-voltage switching. One advantage of the MMC is that can operate in lower switching frequency (<2 kHz) and produce high quality output.

A.8.3 Nearest Level Control

When a modular multilevel converter has a sufficiently large number of cells per arm, an alternative approach to PWM called NLC may be used. This approach determines the voltage levels that must be synthesised and selects the number of cells that are required for a given voltage level, by tracking the reference voltage waveform. NLC determines how many cells are included according to the discretisation function of the modulation signal. The benefit of NLC is reduced complexity of implementation compared to PWM.

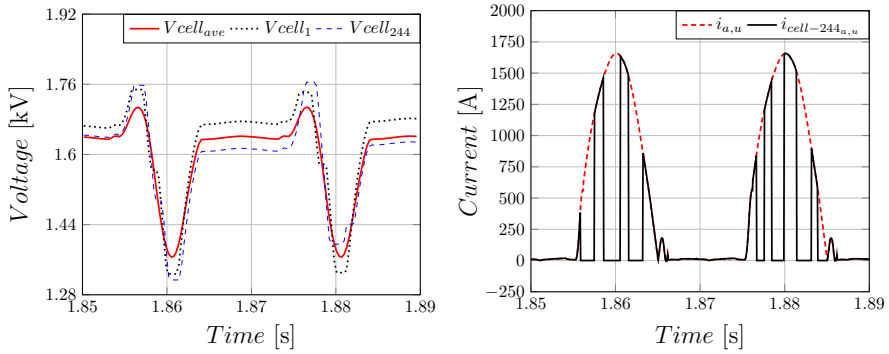
A.8.4 Chain-link controller

The Chain-link controller combines the capacitor voltage balancing and modulation schemes. This particular controller converts the output from the Upper level controller into gate control pulses which drive the semiconductors in the converter. This control layer balances the capacitor voltages, and also influences efficiency as a result of the modulation scheme that is applied.

The CBA scheme is designed to manage the capacitor voltages in each cell, so that equal average energy rating of each capacitor is achieved. Otherwise cell voltages will diverge rapidly and will result in the unstable operation of the converter. The capacitor balancing algorithm decides which cells will take part

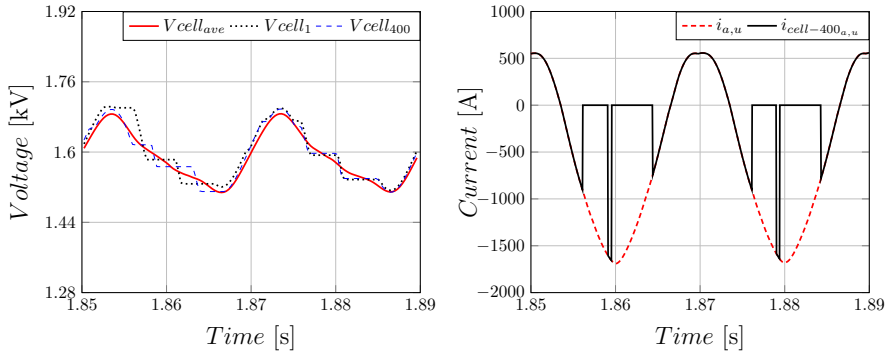
in converter operation. To achieve this the algorithm needs to know how many sub modules are needed to be ON and OFF, and the capacitor states, in order to create a balanced state among the capacitor voltages. There is a compromise between achieving capacitor voltage balance and maintaining a low cell switching frequency. A more frequent execution of the CBA gives better capacitor voltage balancing but increases the switching losses. The CBA operates simultaneously with the modulation techniques as it determines the number of cells that are needed at any given operating condition.

Three main CBA techniques exist: sorting algorithm, distributed control and



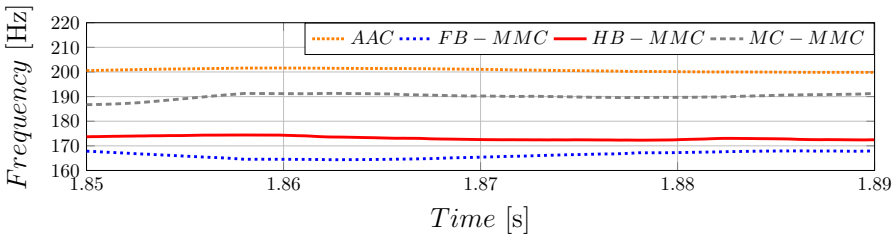
(a) AAC capacitor voltages

(b) AAC arm and cell currents



(c) MMC capacitor voltages

(d) MMC arm and cell currents



(e) Converter average switching frequency

Figure A.10: The effect of tolerance band CBA for $N_{MMC} = 400$ and $N_{AAC} = 244$.

tolerance band. The techniques trade off computational effort, complexity and flexibility, and are described as follows:

1. **Sorting algorithm**. In every state, the CBA sorts the capacitor voltages and, according to the direction of arm current flow, inserts or bypasses the cells that are needed [117]. The cells are sorted from lowest to highest (or highest to lowest) voltage every time the control algorithm requires a cell to be inserted or bypassed. The computational burden of the voltage sorting algorithm is very large for increased numbers of cells. Moreover, it is not possible to regulate actively the cell switching frequency as the frequency with which the algorithm is updated is bound to the number of cells. This type of CBA has an easier implementation in low number of cells converters, hence is used in the experimental set-up.

2. **Distributed control**. This approach uses phase shifted carriers [109]. Each cell has a dedicated carrier which is generated according to the error between the actual cell capacitor voltage and the capacitor voltage reference. It is possible to regulate the cell switching frequency by regulating the capacitor voltage reference. The benefit of this technique is that the distributed operation reduces the process demand as each cell is self-regulated. However, the dedicated carriers have to be synchronised and must be able to cater for cell failure.

3. **Tolerance band**. This technique allows robust control operation, as it does not rely upon a complex sorting function and minimises computational effort as only the voltages that exceed the defined tolerance band need to be considered. The computational effort remains the same regardless of the number of cells, and it is possible to adjust the cell switching frequency by setting the tolerance band accordingly. In this research the tolerance band technique is used [118], and the implementation is described in Appendix B. Its effects are illustrated in Fig. A.10.

Appendix B

Capacitor balancing algorithms

This section shows the Simulink implementation of sorting and tolerance band CBA which are used in the EMTP-RV simulations. A DLL file was generated from the Simulink model and was implemented in EMTP, where the two types of CBA were available.

B.1 Sorting CBA

Universal sorting CBA applicable in HB-MMC, MC-MMC, FB-MMC and AAC, for defined a number of cells.

```
function [VC_US,VC_FB]= PWM_FCN(Vc_sm) %Sortling loop

N_FB=20; % Number of Full-Bridge cells - change for different ratio of FB-HB cells.
num=length(Vc_sm);
numFB=length(Vc_sm(1:N_FB));
VC_UG=Vc_sm;
VC_UG_FB=Vc_sm(1:N_FB);

VC_US=linspace(1,num,num);
for i=1:num-1
    for j=1:num-i
        if(VC_UG(j)>VC_UG(j+1))
            tep=VC_UG(j);
            VC_UG(j)=VC_UG(j+1);
            VC_UG(j+1)=tep;
            tep=VC_US(j);
            VC_US(j)=VC_US(j+1);
            VC_US(j+1)=tep;
        end
    end
end

VC_FB=linspace(1,numFB,numFB);
for iFB=1:numFB-1
    for jFB=1:numFB-iFB
        if(VC_UG_FB(jFB)>VC_UG_FB(jFB+1))
            tepFB=VC_UG_FB(jFB);
            VC_UG_FB(jFB)=VC_UG_FB(jFB+1);
            VC_UG_FB(jFB+1)=tepFB;
            tepFB=VC_FB(jFB);
            VC_FB(jFB)=VC_FB(jFB+1);
            VC_FB(jFB+1)=tepFB;
        end
    end
```

```
end
```

```
function Ka = PSS_CBA(Vref,Vc,VcFb,Vc2,VcFb2,Yota) %Balancing loop, Vref can be PWM or NLC
% Va=Vref;
Ia=Yota;
N=length(Vc);
Ka=zeros(1,N);

%% Modulation
if Vref>=0 && Vref<=N
    Va=Vref;
    for I=1:(Va)
        if Ia<=0
            for II=1:(N+1)
                if (II==Vc2(I))
                    Ka(Vc2(I))=0;
                else
                    Ka(Vc2(I))=1;
                end
            end
        else
            for II=1:(N+1)
                if (II==Vc(I))
                    Ka(Vc(I))=0;
                else
                    Ka(Vc(I))=1;
                end
            end
        end
    end
%% Negative overmodulation
elseif Vref<0 && Vref>=-N
    Vl=-Vref;
    for I2=1:(Vl)
        if Ia<=0
            for II2=1:(N+1)
                if (II2==VcFb(I2))
                    Ka(VcFb(I2))=0;
                else
                    Ka(VcFb(I2))=-1;
                end
            end
        else
            for II2=1:(N+1)
                if (II2==VcFb2(I2))
                    Ka(VcFb2(I2))=0;
                else
                    Ka(VcFb2(I2))=-1;
                end
            end
        end
    end
%% Negative limits
elseif Vref<-N
    for II2=1:(N)
        Ka(Vc(II2))=-1;
    end
%% Positive limits
elseif Vref>N
    for II2=1:(N)
        Ka(Vc(II2))=1;
    end
end
```

B.2 Tolerance band CBA

Universal tolerance band CBA applicable in HB-MMC, MC-MMC, FB-MMC and AAC, for a defined number of cells.

```
function [Gc,idx2]=balancing(Gc_p,Vc_sm,Yota,Vnlc,Vnlc_p,idx,dVc_max,dVc_sort)

M=length(Vc_sm);
NonC=Vnlc;
NonP=Vnlc_p;
Iarm=Yota;
Vc=Vc_sm;
Gp=Gc_p;

if(NonC>=M)
   Gc=ones(M,1);
   idx2=idx;
elseif (NonC==0)
   Gc=zeros(M,1);
   idx2=idx;
elseif (NonC<=-M)
   Gc=-1*ones(M,1);
   idx2=idx;
elseif (NonC<0&&NonC>-M)
   F=0;Vc_avg=sum(Vc)/M;
   NonC_neg=-NonC;
   for i=1:M
      if (abs(Vc(i)-Vc_avg)>dVc_max)
         F=1;
      end
   end
   if(NonC==NonP&&F==0)
      Gc=Gp;
      idx2=idx;
   else
      if(Iarm==0)
         Gc=Gp;
         idx2=idx;
      elseif (Iarm>0)
         j=1;idx2=zeros(M,1);Gc=ones(M,1);
         for i=1:M
            if(Vc(idx(i))>=Vc_avg-dVc_sort)
               idx2(j)=idx(i);
               j=j+1;
            else
               idx2(M-i+j)=idx(i);
            end
         end
         for i=1:NonC_neg
            Gc(idx2(i))=-1;
         end
         for i=NonC_neg+1:1:M
            Gc(idx2(i))=0;
         end
      else
         j=1;idx2=zeros(M,1);Gc=ones(M,1);
         for i=1:M
            if(Vc(idx(i))<=Vc_avg+dVc_sort)
               idx2(j)=idx(i);
               j=j+1;
            else
               idx2(M-i+j)=idx(i);
            end
         end
         for i=1:NonC_neg
            Gc(idx2(i))=-1;
         end
         for i=NonC_neg+1:1:M
            Gc(idx2(i))=0;
         end
      end
   end
else
   F=0;Vc_avg=sum(Vc)/M;
   for i=1:M
      if (abs(Vc(i)-Vc_avg)>dVc_max)
         F=1;
      end
   end
   if(NonC==NonP&&F==0)
      Gc=Gp;
      idx2=idx;
```

```
    else
        if (Iarm==0)
            Gc=Gp;
            idx2=idx;
        elseif (Iarm>0)
            j=1;idx2=zeros(M,1);Gc=ones(M,1);
            for  i=1:M
                if (Vc(idx(i))<=Vc_avg+dVc_sort)
                    idx2(j)=idx(i);
                    j=j+1;
                else
                    idx2(M-i+j)=idx(i);
                end
            end
            for  i=1:NonC
                Gc(idx2(i))=1;
            end
            for  i=NonC+1:1:M
                Gc(idx2(i))=0;
            end
        else
            j=1;idx2=zeros(M,1);Gc=ones(M,1);
            for  i=1:M
                if (Vc(idx(i))>=Vc_avg-dVc_sort)
                    idx2(j)=idx(i);
                    j=j+1;
                else
                    idx2(M-i+j)=idx(i);
                end
            end
            for  i=1:NonC
                Gc(idx2(i))=1;
            end
            for  i=NonC+1:1:M
                Gc(idx2(i))=0;
            end
        end
    end
end
```

Appendix C

Wind farm model

This appendix presents the WF model that was used in Chapter 4. The WF model is an aggregated model of 167 type 4 WTs, rated at 6 MW, with representation of only the grid side converter (GSC), as shown in Fig. C.1. The WF model is assuming constant wind speed, with ascending and descending power ramp of 0.2 $\frac{\text{p.u.}}{\text{s}}$ and 5 $\frac{\text{p.u.}}{\text{s}}$ respectively, to emulate the pitch control capabilities. The control structure is similar to that which was described in Appendix A.

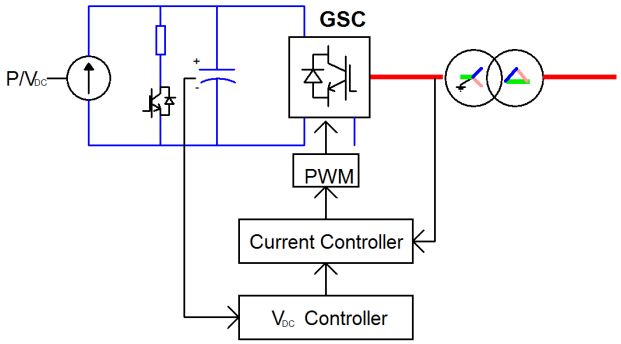


Figure C.1: Schematic diagram of Type 4 WT.

Table C.1 provides the controller parameters of the aggregated WF model.

Table C.1: WF control parameters.

Controllers	K_p	T_i
Outer controller		
AC voltage controller	1	30
V_{DC} controller	6.4	130.612
Inner controller		
Current controller GSC	0.537	67.143