# University of Strathclyde <br> Department of Electronic and Electrical Engineering 

# Current Source DC-DC and DC-AC Converters with Continuous Energy Flow 

by

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A thesis presented in fulfilment of the requirements for the degree of Doctor of Philosophy

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## Dedication

To my father, my mother, my brother, my wife, and my son


#### Abstract

This work considers current sourced power electronic converters. The thesis classifies and presents several new single-phase and three-phase differential-mode current source inverters that evolve from the basic dc-dc converter topologies. The switched, large-signal, and small-signal models of these converters are presented, and used to develop control strategies for the proposed differential-mode inverters, considering their inversion and rectification modes. The viability of each differential mode inverter/rectifier is validated using simulations and experimentation. The performances of different proposed buck, boost, and buck-boost current source inverters are discussed and compared in terms of efficiency, total harmonic distortion, input current ripple, capacitor stresses, and control complexity. Some of the proposed current source inverters offer buck-boost capability (can operate with output voltage less or greater than the input dc voltage), which is suited for gridconnected operation of single-stage three-phase buck-boost inverters. Phase variables and synchronous frame controllers are used to provide satisfactory inverter operation in inversion and rectification modes. The inherent low-order harmonic currents in the input and output of the proposed converters (predominantly, negative sequence $2^{\text {nd }}$ order harmonic) are supressed using PI and PR controllers. Also, interleaved carriers are used to reduce the input current ripple of the three-phase inverters. The proposed converters can operate over a full control range from 0 to unity power factor, with power flow in both directions (unlike the conventional six-pulse current inverter). Additionally, a nonlinear control strategy, sliding mode control, is implemented with to achieve faster dynamic inverter response during faults as well as elimination of dccurrent injection into ac grid. This is necessary during unbalanced operation. Operation of single-phase differential-mode buck-boost inverters is presented, including suppression of the $2^{\text {nd }}$ order harmonic in the input dc current by two methods. In the first, active suppression of the $2^{\text {nd }}$ harmonic uses a power electronic circuit. The second method manipulates the modulating signal in combination with a relatively large capacitor to trap the oscillating power that causes the $2^{\text {nd }}$ order harmonic to appear input dc link current. The two single-phase harmonic suppression approaches are compared.


High-frequency transformer isolated versions of some considered single-phase and three-phase inverters are assessed and compared with their non-isolated counterparts. The isolated versions provide important features such as noise mitigation, voltage compatibility, and galvanic isolation for safety reasons. New isolated single-phase and three-phase inverters with reduced switches number are proposed and assessed.

## List of symbols

| C | Filter Capacitor (F) |
| :---: | :---: |
| $C_{H C}$ | Harmonic compensator output capacitance (F) |
| $C_{o}$ | Output filter capacitance (F) |
| D | Converter's duty ratio |
| $D_{e}$ | Equilibrium duty ratio |
| $f_{b}$ | Band-pass filter base frequency ( Hz ) |
| $f_{s}$ | Switching Frequency (Hz) |
| $h_{a}, h_{b}$ and $h_{c}$ | Instantaneous voltage conversion ratios |
| $H_{d c}$ and $H_{a c}$ | DC and AC voltage conversion ratios |
| $I_{d}, I_{q}$, and $I_{o}$ | Direct, quadrature and dc currents (A) |
| $i_{\text {in }}$ | Input current (A) |
| $I_{L}$ | Series inductor current (A) |
| $I_{m}$ | Output current peak value |
| $i_{o}$ | Output current (A) |
| $i_{o a}, i_{o b}$, and $i_{o c}$ | Instantaneous output currents (A) |
| $I_{r m s}$ | rms switch current (A) |
| $i_{s}$ | Total inverter input current (A) |
| $K_{p}, K_{i}$, and $K_{r}$ | Proportional, integral and resonant controllers parameters |
| $L$ | Filter Inductance (H) |
| M | Modulation index |
| $N_{1}, N_{2}$ | Primary and secondary turns |
| $P$ | Active power (W) |
| $Q$ | Reactive power (VAr) |
| $R$ | Output resistance ( $\Omega$ ) |
| $r_{1}$, and $r_{2}$ | Input and output parasitic resistances |
| $R_{\text {on }}$ | Switch on resistance ( $\Omega$ ) |
| $S$ | Apparent power (VA) |
| $t_{\text {off }}$ | OFF time (s) |
| $t_{o n}$ | ON time (s) |
| $t_{s}$ | Switching period (s) |
| $V_{2}$ | Second harmonic voltage peak value (V) |
| $v_{a}, v_{b}$, and $v_{c}$ | Instantaneous converters output voltages (V) |


| $V_{c}$ | Intermediate capacitor voltage (V) |
| :--- | :--- |
| $V_{d}, V_{q}$, and $V_{o}$ | Direct, quadrature and dc voltages (V) |
| $V_{i n}$ | Input voltage (V) |
| $V_{m}$ | Output voltage peak value |
| $V_{o}$ | Output voltage (V) |
| $\nu_{o o b}, \nu_{o b}$, and $v_{o c}$ | Instantaneous load voltages (V) |
| $Z$ | Output impedance ( $\Omega$ ) |
| $\gamma$ | Output current phase-shift angle ( ${ }^{\circ}$ ) |
| $\delta$ | Small-signal duty ratio |
| $\delta_{H C}$ | Harmonic compensator duty ratio |
| $\Delta I_{i n}$ and $\Delta I_{o}$ | Input and output ripple currents (A) |
| $\delta_{\text {min }}$ and $\delta_{m a x}$ | Minimum and maximum duty ratios |
| $\theta$ | Output voltage phase-shift angle ( ${ }^{\circ}$ ) |
| $\Phi$ | Core flux (wb) |
| $\Phi$ | Core maximum flux (wb) |
| $\Phi_{m}$ | Second harmonic voltage phase-shift $\left({ }^{\circ}\right)$ |
| $\psi_{2}$ | Fundamental angular frequency (rad/s) |
| $\omega$ | PR controller resonant angular frequency (rad/s) |
| $\omega_{o}$ |  |

## List of abbreviations

| AC | Alternating Current |
| :---: | :---: |
| BP | Band Pass |
| CCM | Continuous Conduction Mode |
| CSI | Current Source Inverter |
| DC | Direct Current |
| DCM | Discontinuous Conduction Mode |
| DFIG | Double-fed Induction Generator |
| EMI | Electromagnetic Interference |
| EU | European Community |
| EWEA | European Wind Energy Association |
| HC | Harmonic Compensator |
| HFL | High Frequency Link |
| IGBT | Insulated Gate Bipolar Transistor |
| LCOE | Levelized cost of electricity |
| MMC | Modular Multilevel Converter |
| MPPT | Maximum Power Point Tracking |
| NPC | Neutral Point Clamped |
| PCC | Point of Common Coupling |
| PI | Proportional Integral |
| PID | Proportional Integral Derivative |
| PR | Proportional Resonant |
| PV | Photovoltaic module |
| PWM | Pulse Width Modulation |
| RMS | Root Mean Square |
| SMC | Sliding Mode Control |
| SMPS | Switched Mode Power Supply |
| SVM | Space Vector Modulation |
| THD | Total Harmonic Distortion |
| UPS | Uninterruptible Power Supply |
| VSC | Variable Structure Control |
| VSI | Voltage Source Inverter |
| WTG | Wind Turbine Generator |

## Preface

There is mounting international proclivity to reduce the cost and improve the efficiency of energy conversion systems through improving modular structured renewable/distributed systems. Therefore, the need for reducing converter size and the values of passive components is become more pressing. Moreover, the cost of renewable energy systems, such as photovoltaic (PV), fuel cells, wind turbines, and solar systems are affected considerably by installation and maintenance cost. Inverter initial and running cost may reach half the total initial PV system cost. For dc-ac conversion, the voltage source inverter (VSI) is the most common topology where the output ac voltage peak is always less than the input dc voltage. To interface a renewable energy system to the grid, a voltage boosting stage is needed between the inverter and the point of common coupling. This stage can be dc/dc, dc/ac converters or, a line frequency transformer. If the VSI can be replaced by inverters having a flexible voltage range, above or below the grid voltage, the total system efficiency may increase dramatically. Inverters with continuous input and/or continuous output currents can increase system reliability, efficiency and reduce the total volume and weight. The goal of the thesis is to assess the different families of current sourced inverters with small passive element values, propose new topologies which are not within the literature, and propose beneficial methods for proper control and reliable operation. The first three chapters present the background of power electronic converters and their control methodologies.

Chapter two presents a methodical process to derive different power electronic converters with desirable features. The chapter provides detailed analysis of the instantaneous voltages and currents in each converter. The ability for the converters to be isolated with a high frequency transformer is discussed.

Chapter three proposes methods for modelling the power electronic converters describing average or instantaneous operation. The chapter presents classical controllers based on the stationary and synchronous frame as well as variable structure systems controllers such as sliding mode controllers.

Chapter four presents the modelling, control and operation of the three power electronic converter families, viz., voltage buck, boost, and buck-boost, having
continuous input and/or continuous output energy flow. The chapter presents singlephase and three-phase inverters derived from the dc-dc converters used as building blocks. The chapter provides a comparison between the converters and inverters in each family. Simulation and practical results confirm the performance and control of the different power converters.

Chapter five presents and discusses the grid interfacing operation of several buckboost single-stage, single-phase and three-phase inverters. The chapter presents novel control methodologies to eliminate undesirable low and high frequency voltage and current components in the buck-boost three-phase inverters. The chapter also presents the operation and control of the single-phase inverters and provides novel techniques for the elimination of the $2^{\text {nd }}$ order harmonic current components found in single-phase inverters.
Chapter six is concerned with high-frequency transformer isolated single-phase and three-phase inverters. New inverter topologies with reduced semiconductor switch number are proposed.

Finally, chapter seven presents the thesis general conclusion, the author's contribution, and suggestions for future research.

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## Chapter 1

## Introduction

To discuss the effect of the global warming, the United Nations called a series of meetings, which resulted in the International Agreement called the Kyoto Protocol [1.1]. The agreement states that some countries must reduce their $\mathrm{CO}_{2}$ emissions by certain percentages. This resulted in increased investment in the area of renewable energy. Reference [1.2] suggests that combinations of renewable energy resources such as hydro, wind and solar, and storage systems can provide all the world's energy needs. This would mitigate the global warming problem. Power electronics continue to play an important role in renewable energy generation and in modern high-efficiency energy systems that aim to improve the quality of the power generated from weather dependent renewable energy resources, such as wind and solar. With continuous research and development, power electronics costs have decreased and its efficiency has increased to about $97-98 \%$ in recent years. Moreover, the size is decreasing, reliability has increased, and lifetime is longer. There are two promising renewable and clean energy resources; both predominantly depend on the use of power electronics. The first is electricity generation from solar energy, where the photovoltaic (PV) panels are employed. The second is the use of wind turbine generators (WTG) to converter the kinetic energy of the wind into electricity. It has been estimated that just $10 \%$ of the available wind energy can supply the world's electric energy demand [1.1]. Currently, PV costs three-times more than WTS for the same rated power. However, with continuous research in order to reduce the size and increase efficiency, the cost of PV systems is expected to fall to a level comparable with that of wind. Continuous advancement of power electronics technologies is necessary for increased and efficient exploitation of renewable energy sources and can save $20 \%$ of the world's energy demand [1.1]. The European Community (EU) targets $20 \%$ growth in renewable energy sources by 2020. Countries in Asia have $35 \%$ of the total world's energy share and hence, investments in the renewable energy field will be more significant.

### 1.1 Background and development of wind energy

For thousands years, humans have used wind energy to propel sailboats and ships. Persians built the first windmill, in about 900 AD [1.3] in the region of Seistan, (eastern Iran now) with a vertical axis rotor. The first known reference in the history is from Hero of Alexandria, Egypt, in his work Pneumatics, which describes a simple energy conversion system from wind to other organs. Wind systems appeared for the first time in Europe in the $11^{\text {th }}$ century. These windmills were used mainly for grain grinding and water pumping and remained the most important energy source until the industrial revolution. In the $19^{\text {th }}$ century, wind power was used for the first time to generate electricity. However, wind power systems were not attractive due to their characteristics and because of the lack of advanced generation techniques. In the late $20^{\text {th }}$ century, the world became aware of the importance and attraction of wind systems. Nowadays, there is fast development and high penetration of grid-connected wind systems. The cumulative installed wind power worldwide is shown in Figure 1.1. The biggest market for wind power is in China, $37 \%$ [1.4].


Figure 1.1. Global cumulative installed wind power [1.4].
The total amount of wind energy produced annually (TWh) divided by the gross electricity demand (TWh) is defined as wind energy penetration (\%). The European Wind Energy Association (EWEA) stated that Europe wind penetration was 3.8\% in 2008. The highest penetration level in Europe is $21 \%$ in Denmark, then, Spain and Portugal where the wind penetration rate is $12 \%$ while in Ireland it is $9 \%$ and Germany is 7\% [1.4].

### 1.1.1 Economics of wind energy

$75 \%$ of the total cost of WTS is related to turbine, foundation, and equipment costs [1.1]. For a typical 2 MW wind turbine system, the total cost per kW range is $5-10 \mathrm{c} €$ with an average of $7 \mathrm{c} €$. The WTS costs decrease at sites with higher average wind
speed. During the last two decades, continuous research and development in Europe has led to a rapid decrease in WTS costs. For a 2 MW turbine, the cost has decreased from 21c€ in 1987 to $7 \mathrm{c} €$ in 2009. Generally, the costs of wind energy systems are cheaper than other renewable sources such as photovoltaic systems for the same power levels. Most existing wind systems in the world are currently installed onshore. North European countries are the pioneers in developing offshore wind energy systems as more than 20 projects were installed by 2008 with approximately 1.5 GW. Although onshore wind energy systems cost is $2 / 3$ that of offshore systems, offshore systems are gaining more attention. This comes from the fact that in offshore systems, higher wind speeds are found. Consequently, higher total electrical power can be generated because of the high wind speeds. Generally, conventional electric generator costs are determined by: (1) fuel cost, (2) cost of $\mathrm{CO}_{2}$ emission (as given by ETS organization), (3) operation and maintenance (O\&M) costs and (4) capital costs. Fuel oil prices have changed rapidly during recent months because of political issues. However, if the real prices are used in the comparison (which is about $100 € /$ barrel $)$, and assuming that two conventional power plants are online, the cost of wind energy systems and conventional electric systems are as shown in Figure 1.2. Concluding, even if wind power systems are more expensive than conventional sources, it might share a significant part of the total power demand, since they evade $\mathrm{CO}_{2}$ and fuel un-expected price rises [1.5].


Figure 1.2. Generated power costs comparing conventional plants to wind power [1.5].

### 1.1.2 Wind energy applications

There are two methods for operating wind energy systems. The first is standalone operation, where the system is not connected to the electric grid. The second mode is
grid-connected, where the turbine's generator is connected and injecting power into the grid [1.4, 1.5].

## a) Stand-alone operation

Isolated WTS can be used to supply passive loads or connected together to form a micro-grid. The range of their power may vary between a few kilowatts to a few megawatts. Stand-alone importance comes from the fact that 2 billion people in the world do not have access to the electric grid; therefore, energy sources must be installed in their regions [1.4]. Thus, wind energy systems with proper storage systems, or may be combined with photovoltaic systems, are attractive solutions for these areas. Cost wise, combining a wind system with a diesel system, forming a hybrid wind-diesel system, is much cheaper than a stand-alone diesel system [1.6]. Because these systems supply loads with a fluctuating nature, the main problems of stand-alone systems arise from frequency deviation and voltage control. For this reason, energy storage and load control with the cooperation of the local community is necessary.

## b) Grid-connected operation

Most medium and large scale wind energy systems are connected to local grids. Many wind turbines are connected together to inject active and reactive power into the grid. Wind farms can be grid-connected onshore or offshore. Onshore wind farms are presently preferred than offshore farms because they are cheaper and easier to maintain. However, offshore wind farms have gained more attention recently. This comes from the fact that the lifetime of offshore wind farms are higher than onshore farms as well as being exposed to higher wind speeds which means higher power levels. In addition, the lower noise and visual impact of large wind turbines are preferred merits of this configuration [1.7]-[1.9].

### 1.1.3 Power electronic converters in wind energy systems

A typical wind energy system consists of a turbine, a drive train and an electric generator. The turbine is responsible for capturing the wind energy and converts it to mechanical energy. A gearbox is used to effectively increase the rotational speed of the turbine shaft to the level suitable for a $50 \mathrm{~Hz} / 60 \mathrm{~Hz}$ generator. The generator converts the mechanical rotational energy into electrical energy [1.10]. Usually, a
power electronic converters stage is used after the electric generator to meet the grid requirements. The location of the power electronic stage depends on the type of the electric generator. Figure 1.3 shows the most common topologies of power electronic converters used in wind energy systems. Figure $1.3 \mathrm{a}, \mathrm{b}$ and c show the full power converter structure for a wind energy system. Figure 1.3d and e show multi-cell full power converter structures [1.11].


(a)

(c)


(d)

(e)

Figure 1.3. Wind power system structures: (a) induction generator with gearbox, (b) doubly fed induction generator, (c) multi-pole synchronous generator, (d) parallel connection and interleaved on the grid side, and (e) n-leg diode bridge producing a shared high DC voltage [1.11].

Types of machines used in wind generation:

- Squirrel cage induction generator (fixed speed systems).
- Wound rotor induction generator with fractionally rated back-to-back topology such as in the DFIG
- Electrically excited or permanent magnet synchronous generator with fully rated back-to-back converter.

Until recently, the DFIG structure was the most popular wind energy systems as the power electronic stage handles about $25 \%$ of the total power systems [1.12]. Several studies have discussed the methods of increasing efficiency of the power electronic stage of wind energy systems as well as reducing their cost. The overall cost of power electronics is about 7\% of the wind turbine-generator [1.9]. Recently, multilevel converters have proven to have the lowest commutation demands and so, the switching frequency can be lowered to $25 \%$, resulting in higher efficiency [1.13][1.15].

A back-to-back configuration, shown in Figure 1.4, is the conventional power electronic arrangement for wind systems. This arrangement allows active and reactive power control of the wind system with reduced output current harmonic content. There are many recent studies on multi-level converters for wind energy applications [1.13]-[1.15]. Multi-level topologies have reduced commutations, thus, leading to the switching frequency to be lower to $25 \%$ [1.9]. Reducing the converter's switching frequency increasing the overall efficiency even though the conducting losses are higher[1.12]. Recently, there has been increased desire to reduce the passive components in the DC link of existing rectifier-inverter based systems [1.16], led by much research in this area.


Figure 1.4. Fully controlled back-to-back converter.

### 1.2 Background and development of photovoltaic systems

In 1839, a French experimental physicist, named Edmund Becquerel, did experiments with a two metal electrodes electrolytic cell which led him to discover
the photovoltaic effect. In 1873, photoconductivity of selenium was discovered by Willoughby Smith. The first solar cells were proposed by Charles Fritts in the USA in 1883. Many developments followed these discoveries until 1954 when Bell Labs researchers Pearson, Chapin, and Fuller discovered 4.5\% efficient silicon solar cells which were soon raised to $6 \%$. Much research has been conducted on PV systems, and currently they are the most important energy source in satellite systems [1.17]. The increase of annual PV power installed in the recent years is shown in Figure 1.5 [1.18]. More than 6.5 GW was installed in 2010, which is roughly $20 \%$ of the installed wind power in the world. In 2014, the IEA reported that over 134 GW of PV are now installed worldwide, which is close to the wind power installed in 2008. There are several countries such as Spain, Germany, and Portugal which have several solar parks larger than 40 MW . Although PV penetration is not so high in the world now, the EPIA forecasts that it will be more than 330 GW in 2020.


Figure 1.5. Global cumulative installed PV power [1.4].

### 1.2.1 Economics of photovoltaic energy

The cost of PV modules has decreased dramatically in the past few decades. For a typical PV module, the average price per kW decreased from $10 \$ / \mathrm{W}$ in 1980 to 2 \$/W in 2010 [1.19]. The fast cost reductions of the PV modules led to a significant increase of the PV systems competitiveness [1.20]. However, there is confusion about calculating the economics of PV systems because the absence of a unified standard [1.20]. Three ways are used to calculate the prices and costs of PV systems,
namely: the price-per-watt (peak) capital cost of PV modules (expressed as \$/W), the levelized cost of electricity (LCOE) (expressed as $\$ / \mathrm{kWh}$ ), and the concept of 'grid parity'. Although the price-per-watt method is simple and requires less data, the calculated cost cannot be translated directly into full installed system costs. LCOE and 'grid parity' require a lot of assumptions, however, they are more beneficial for government decision-takers.

The Chinese c-Si module is considered to be the cheapest PV module. Figure 1.6 shows the dramatic decrease of Chinese c-Si module price-per-watt curve between 2006 and 2011. The rapid change in PV technology costs causes important consequences for decision makers and network designers. Finally, the main challenge is how to satisfy a smooth development for the PV systems from being a promising and expensive energy source to a real competitive energy source for electricity.


Figure 1.6. Chinese c-Si PV module prices (\$/W).

### 1.2.2 Power electronics in PV systems

Conventionally, the module-integrated PV topology has one converter for each PV module with centralized measurements for the system states. However, this topology has lower efficiency for higher power levels [1.12]. Currently, string inverters [1.9], see Figure 1.7, are gaining more attraction because of their higher efficiency.


Figure 1.7. Multi-string converter with a single-phase inverter stage [1.9].

Better PV system performance can be achieved if the inverters can voltage buck as well as boost. This enables the maximum power point tracking (MPPT) controller to correctly function and extract the maximum available energy from the power system. Moreover, the energy can be stored at higher limits [1.12]. PV systems can be classified into two major topologies: PV inverters with a DC/DC converter (twostage inverters) and PV inverters without a DC/DC converter (single-stage inverters). Both topologies can operate with or without an isolation transformer. The transformer can be inserted on the grid side and work at the line frequency (LF) or can be within the inverter and operate at high frequency (HF). Although PV inverters without an isolation transformers are cheaper, smaller and lighter, isolation may be important for safety issues and reduces EMI production [1.9]. PV inverters without transformers have higher efficiency, lower cost, and smaller size. Figure 1.8 shows the most common transformer-less inverter topologies used for PV systems, namely: H-bridge, H5-bridge, HERIC, neutral point clamped (NPC), and Coenergy NPC [1.11]. Due to the variation of sun irradiation and temperature, the output power of PV panels fluctuates continuously. As a solution for smoothing the output current which is injected into the grid, an energy storage system can be installed. The simplest storage system is a battery connected to the system by DC/DC converter on the DC side or by a $\mathrm{DC} / \mathrm{AC}$ converter on the AC side.


Figure 1. 8. Converter PV system topologies [1.11]: (a) H-bridge, (b) H5-bridge, (c) HERIC, (d) NPC, and (e) T-type inverter.

### 1.2.3 Grid requirements for $\mathbf{P V}$

The power level of grid-connected PV systems is from a few kilowatts to several megawatts. To ensure system safety and sustainable energy transfer to the distributed grid, the PV systems must comply with specified standards or national grid codes [1.4]. The most important international standards for grid requirements are from the IEEE (Institute of Electrical and Electronic Engineers) and the IEC (International Electro-technical Commission). Examples of IEEE standards for PV are [1.4]:

- IEEE 1547: deals with interconnection of distributed generation. It addresses the interconnected PV types from 100W to 10MW and unifies the requirements and recommendations for testing.
- IEC 61727: specifies the requirements and desired characteristics of utility interface, published in 2004. It is related to the utility-interconnected PV power systems which operate in parallel with solid-state non-islanding inverters for DC/AC conversion.

Table 1.1 summarizes IEEE-1547 and IEC-61727.
Table 1.1. Summary of IEEE-1574 and IEC-61727 standards

| Issue | IEEE 1574 |  | IEC 61727 |  |
| :---: | :---: | :---: | :---: | :---: |
| Rated power | 30 kW |  | 10 kW |  |
| Disconnection time for voltage (RMS) variations (measured at the point of utility connection) | Voltage range (\%) | $\begin{gathered} \hline \text { Disconnecting } \\ \text { Time (s) } \end{gathered}$ | Voltage range (\%) | $\begin{gathered} \hline \text { Disconnecting } \\ \text { Time (s) } \end{gathered}$ |
|  | $V<50$ | 0.16 | $V<50$ | 0.10 |
|  | $50 \leq V<88$ | 2.00 | $50 \leq V<85$ | 2.00 |
|  | $110 \leq V<120$ | 1.00 | $110 \leq V<135$ | 2.00 |
|  | $V \geq 120$ | 0.16 | $V \geq 135$ | 0.05 |
| Disconnection time for frequency variations | Frequency range (Hz) | $\begin{aligned} & \hline \text { Disconnecting } \\ & \text { Time (s) } \\ & \hline \end{aligned}$ | Frequency range $(\mathrm{Hz})$ | $\begin{aligned} & \text { Disconnecting } \\ & \text { Time (s) } \\ & \hline \end{aligned}$ |
|  | $59.3<f<60.5$ | 0.16 | $47.5<f<50.2$ | 0.2 |
| Reconnection after trip | $\begin{gathered} 88<V<110(\%) \\ \text { AND } \\ 59.3<f<60.5(\mathrm{~Hz}) \end{gathered}$ |  | $\begin{gathered} 85<V<110(\%) \\ \text { AND } \\ \mathrm{n}-1<f<f \mathrm{n}+1(\mathrm{~Hz}) \\ \text { AND } \end{gathered}$ <br> inimum delay of 3 min . |  |
| DC current injection limitation | $I_{\mathrm{DC}}<0.5(\%)$ <br> of the rated RMS current |  | $I_{\mathrm{DC}}<1(\%)$ <br> of the rated RMS current |  |
| Maximum current harmonics | $\begin{gathered} \text { Individual } \\ \text { harmonic order } h \end{gathered}$ | Maximum limit <br> (\%) | $\begin{gathered} \text { Individual } \\ \text { harmonic order } h \end{gathered}$ | Maximum limit <br> (\%) |
|  | $h<11$ | 4.0 | $h<11$ | 4.0 |
|  | $11 \leq h<17$ | 2.0 | $11 \leq h<17$ | 2.0 |
|  | $17 \leq h<23$ | 0.6 | $17 \leq h<23$ | 0.6 |
|  | $23 \leq h<35$ | 0.6 | $23 \leq h<35$ | 0.6 |
|  | $h \geq 35$ | 0.3 | $h \geq 35$ | 0.3 |
|  | THD | 5.0 | THD | 5.0 |
| Average power factor | $\square$ |  | PV inverter must have an average lagging power factor greater than 0.9 when the output is greater than $50 \%$. |  |

### 1.2.4 Photovoltaic power systems in the UK

Although it is surmised that PV systems are not viable in the UK because of the lack of significant sunlight energy, the UK is an important partner in the PV market of

Europe [1.21] as modern PV systems can work effectively without exposure to high intensity solar energy [1.21]. The UK Government identifies PV systems to be one of the promising energy sources in the UK and believes that these systems can contribute $15 \%$ of the total energy consumption by 2020 [1.21]. The UK government is committed to increase and develop PV systems across the country. Solar PV panels can be installed in different locations such as residential roofs, commercial buildings, industrial foundations, and in Greenfield sites. The solar PV systems industry can contribute to the country's economic growth because of its flourishing installation sector which is translated into long-term jobs and future investments. Three major PV energy markets exist in the UK at the moment: domestic, building mounted, and ground mounted.

The domestic PV systems are suitable for supplying power to large number of homes in UK in range of 4 kW . The building mounted systems can be installed in offices, schools, hotels, etc. and vary between 4 kW to 100 kW . The ground mounted systems supply power at the grid distributed level with output power higher than 1 MW . Between December 2012 and June 2013, solar PV generation in UK reached 1380 GWh (England: 1201 GWh, Wales: 89 GWh, Soctland: 83 GWh, and North-Ireland: 7 GWh) [1.21].

### 1.2.5 Motivation and Objectives

Weather dependent renewable energy resources such as wind turbines, photovoltaic arrays, fuel cells, and batteries require sophisticated control schemes to maximize power utilization. This increases the need for dc/dc and/or dc/ac converters with continuous input energy flow. Therefore, the output current and voltage of these renewable sources are preferred to be continuous for maximum power extraction. Traditionally, converter input current (renewable source output current) is maintained continuous by means of a large LC filter. This large filter increases the cost, size, resonance and decreases the reliability of the overall system. The filter's capacitor lifetime is halved for every $10^{\circ}$ increase in the temperature. Consequently, this capacitor is main source of unreliability especially in hot countries.

In this research, power electronic converters with inherent continuous input currents and voltages (thus do not need a large input C or LC filter) are proposed, classified,
and discussed. They can be used in many modern and renewable energy systems. The operation of these power converters in dc/ac mode is presented. Some of them are never studied before in dc/ac mode. Possible configurations and attributes of the proposed power converters are presented, as well as their detailed modelling and control methods. The thesis main objectives are:

- To present methodical classification of power electronic converters starting from the dc-dc single-switch single-diode converters using well defined performance indicators.
- To provide a systematic approach for the generation dc/ac single-phase and three-phase converters with continuous input current. They are seventeen power converters in total (four voltage buck, eight voltage boost and five voltage buck-boost converters). Many of these inverters are not studied or presented in the literature. Moreover insightful comparisons between these converters are presented.
- To present detailed models of the proposed converters and their control methods.
- To suggest the necessary modification to facilitate high-frequency isolation of some of the proposed converters, with small size and light weight transformers for safety, voltage boosting and EMI issues.
- To propose solutions for input side low frequency oscillation problems in single-phase inverters when they are connected to the local ac grid.
- To study the high-frequency isolated versions of the dc/ac single-phase and three-phase power inverters and investigate their effect on the total efficiency.
- To propose new topologies for dc/ac single-phase and three-phase inverters with reduced switch numbers.


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## Chapter 2

## Converter Topologies and their Classification

Switched mode power supplies (SMPS) or dc-to-dc converters, are widely used in domestic and industrial applications [2.1-2.3]. Some of these applications are small and medium scale renewable power generation from solar and wind, household apparatus, lighting, transportation vehicles, and many others [2.4]. SMPS efficiency depends on the circuit topology and control strategy employed [2.2]. Generally, SMPSs can be categorized as voltage or current sourced converters, and they use semiconductor switches and passive elements to manipulate their input voltage or current sources to achieve several desirable objectives such as precise output voltage or current control [2.5]. SMPS applications such as electrical drives, power systems, interfacing of power generated from renewable energy resources, are required to have higher efficiency and must meet much strict power quality regulations [2.6]. From this perspective, the design, analysis and control of SMPSs are becoming increasingly important and complex. The SMPS appeared for the first time more than 50 years ago, for which time; much research and development have been conducted [2.7-2.11]. The spread and discussion of their conceptions in text books is still limited to the simplest and most fundamental types of converters such as: buck, boost, and buck-boost converters as well as fourth-order converters such as Ćuk, SEPIC and zeta converters [2.2]. This chapter provides a structural study of possible configurations of single-switch single-diode power converters and explores the converter topologies by means of fundamental circuit theory.

### 2.1 Configurable Switching Structures

Normally, SPMSs are used intensively in power conversion systems to perform voltage and current conversions. In voltage conversion, the SMPS uses controlled semiconductor devices to vary its output voltage level (step-up/step-down). In current conversion, the SMPS converts between two different current levels. The basic operation of an ideal voltage or current type SMPS can be performed with continuous or discontinuous connection of the source to the energy storage devices such as inductor or a capacitor by turning semiconductor switches on and off [2.12]. Consequently, the energy is transferred between the input and output sides at the
required voltage or current levels. The converter's circuit design must ensure that any voltage source is not connected in parallel with a switched capacitor or any current source is not connected in series with a switched inductor [2.5]. The simplest types of converters should consist of at least one inductor and one capacitor establishing a second-order power converter. Second-order power converters have two poles in the frequency domain [2.13]. Installing an additional passive element in the converter topology, results in a higher-order converter. Increasing the converter's order is necessary sometimes for achieving additional features such as bidirectional power flow or having continuous input or output current; however, it increases complexity of the power circuit and control system [2.14].

### 2.1.1 Second-order power converters

There are two fundamental configurable switching structures (canonical cells) that can be used to derive all second-order power converters [2.2]:

- The star-connected two-switch inductor cell; and
- The delta-connected two-switch capacitor cell.

The first configuration is suitable for voltage source converters and sinks, while the second is suitable for current source converters and sinks. These cells represent the minimum possible configurable switching structures for the known power electronic converters [2.2, 2.4].

### 2.1.1.1 The switching-inductor cell (Cell A)

The two-port (assuming a common zero reference ground) switching-inductor cell consists of one inductor for intermediate energy storage and two star-connected switches as shown in Figure 2.1. The two switches are installed in positions that ensure the current through the inductor is not forced to zero instantly. The two switches should not operate simultaneously, but such that the inductor current always finds a continuous path to flow. The switching-inductor cell is rotated so that terminals (a), (b), and (c) can be connected to terminals (1), (2), and (3-4), resulting in six possible configurations. However, due to the circuit symmetry, there are three repeated configurations. Therefore, the three distinct possible converter configurations resulting from terminal rotation are shown in Figure 2.2. The two
switches (initially assumed ideal switches) must operate in a complimentary manner; otherwise a short circuit is created across either the input, the output, or between the input and output. A practical output load, shown in Figure 2.3a, consists of voltage converting capacitor-resistor sink. The capacitor is necessary for filtering the output load current (by averaging the switched output voltage from the cell). Considering the power flow direction, the ideal switches are replaced by an active switch (such as IGBT, MOSFET, etc.) and a diode resulting in three different practical voltage type converters, namely: buck, boost, and buck-boost converters, see Figure 2.3 (b-d). For identifying the cells and converters, each converter will be labelled according to its type and the cell which it evolves from. For example, the structure in Figure 2.3b is labelled as (b1A). 'b' represents a voltage buck property and the following number ' 1 ' means that it is the first buck-type converter in the cell and the letter ' $A$ ' represents Cell A. In the same way, Structure 2 in Figure 2.3c is labelled as (B1A), where ' $B$ ' means that it is a boost-type converter. Structure 3 in Figure 2.3d is labelled as (bB1A), where ' $b B$ ' means that it is a buck-boost converter. For other cells, yet to be discussed, more than one converter with the same type may descent from a given cell.


Figure 2.1. SMPS using the switching-inductor cell (A).

During the on time $\left(t_{o n}\right)$, the switch $S_{l}$ conducts current while the diode $D_{2}$ is in a reverse voltage mode. And during the off time $\left(t_{o f f}\right)$, the diode $D_{2}$ is forward biased and conducting current, while $S_{l}$ is off. The ratio between $t_{o n}$ and the total time ( $t_{o n}+$ $t_{o f f}$, refer to as switching period $t_{s}$ ) is defined as the duty ratio of the converter $(D)$. The relation between the input and output voltages is determined according to each converter voltage conversion ratio $M$ as $V_{d} / V_{i n}=M(D)$. The voltage conversion ratios
of the converters are calculated from the mathematical equations of the switch on and off circuit configurations.


Figure 2.2. The three possible configurations of the switching-inductor cell (A): (a) Structure 1, (b) Structure 2, and (c) Structure 3.

For example, the equations of the b1A converter are expressed as:

$$
\left.\begin{array}{ll}
V_{\text {in }}=L \frac{d i_{L}}{d t}+V_{o} & 0<t<t_{\text {on }}  \tag{2.1}\\
0=L \frac{d i_{L}}{d t}+V_{o} & t_{o n}<t<t_{s}
\end{array}\right\}
$$

Equation ((2.1) can be averaged along the switching time $t_{s}$ as:

$$
\begin{align*}
& D V_{\text {in }}=L \frac{d i_{L}}{d t}+V_{o}  \tag{2.2}\\
& \text { where } D=\frac{t_{o n}}{t_{s}}
\end{align*}
$$

In the steady-state operation (assuming a continuous inductor conduction mode, CCM), the values of the state derivatives are equal to zero. Consequently, the voltage (and by energy conservation, current) conversion ratio is calculated as:

$$
\begin{equation*}
D=\frac{V_{o}}{V_{i n}}\left(=\frac{I_{i n}}{I_{o}}\right) \tag{2.3}
\end{equation*}
$$

The voltage conversion ratio for all the converters in unidirectional Cell A can be expressed as:

$$
\begin{equation*}
M(D)=\frac{V_{o}}{V_{i n}}=D \text { for voltage buck converters } \tag{2.4}
\end{equation*}
$$

$$
\begin{gather*}
M(D)=\frac{V_{o}}{V_{\text {in }}}=\frac{1}{1-D} \text { for voltage boost converters }  \tag{2.5}\\
M(D)=\frac{V_{o}}{V_{\text {in }}}=-\frac{D}{1-D} \text { for voltage buck-boost converters }  \tag{2.6}\\
0<D<1
\end{gather*}
$$


(a)

(c) B 1 A

(b) b1A

(d) bB 1 A

Figure 2.3. Practical load and the three fundamental DC-DC voltage converters: (a) resistor-capacitor output sink (b) buck, (c) boost, and (d) buck-boost.

The output voltage of buck-boost converter 'bB1A' has an opposite polarity with respect to the input voltage. This voltage inverting property will be repeated in most of buck-boost converters, as will be discussed later.

### 2.1.1.2 The switching-capacitor cell (Cell B)

The switching-capacitor cell (Cell B), shown in Figure 2.4, consists of energy storage capacitor and two switches connected in a delta configuration. The switches operate so as to ensure that the voltage across the storage capacitor is never forced to zero instantaneously. Similar to Cell A, terminals (a), (b), and (c) can be connected to terminals (1), (2), and (3-4), resulting in three different configurations, which are current type buck, boost, and buck-boost converters. The resultant converter structures are shown in Figure 2.5. Considering the current and voltage directions, the ideal switches are replaced by an active switch and diode as shown in Figure 2.6. The relation between the input and output currents is determined according to each
converter voltage transfer function $M$ as $I_{o} / I_{\text {in }}=M(\mathrm{D})$. The current conversion ratios (assuming a continuous capacitor voltage mode) for the converters can be written as:

$$
\begin{gather*}
M(D)=\frac{I_{o}}{I_{i n}}=1-D \text { for current buck converters }  \tag{2.7}\\
M(D)=\frac{I_{o}}{I_{\text {in }}}=\frac{1}{D} \text { for current boost converters }  \tag{2.8}\\
M(D)=\frac{I_{o}}{I_{\text {in }}}=-\frac{1-D}{D} \text { for current buck-boost converters }  \tag{2.9}\\
0<D<1
\end{gather*}
$$



Figure 2.4. SMPS using the switching-capacitor cell (B).
The three fundamental current converters in Figure 2.6 can be obtained from the dual counterparts of the voltage converters in Figure 2.3. This is obtained by changing the connection of each element from being connected in series to parallel and vice versa and replacing the inductor with a capacitor. Although the current converters are theoretically viable, current sources and sinks are not practical and do not exist in reality. For this reason, replacing the current sources and sinks with their equivalent circuits consisting of voltage sources and sinks will transform the current converters into more practical converters. This will result in higher order converters, which will be discussed in the subsequent sections.

### 2.1.2 High-order converters

Some high-order converters were presented in the 1980's such as the Ćuk, SEPIC and zeta converters. They have been classified as high-order converters (third and fourth) because each converter consists of more than two passive elements. The third-order Ćuk converter consists of two inductors, one capacitor and two switches (voltage to current conversion), while the fourth-order Ćuk converter (voltage to voltage conversion) consists of two inductors, two capacitors and two switches. The

SEPIC converter is a fourth-order converter, which comprises two inductors, two capacitors and two switches.


Figure 2.5. Three possible configurations of the switching-capacitor cell (B): (a) Structure 1, (b) Structure 2, and (c) Structure 3.

(c) bB1B

Figure 2.6. Three fundamental DC-DC current converters: (a) buck, (b) boost, and (c) buck-boost.

High-order converters have more storage elements than the fundamental converters and hence, are more complicated from the topological analysis and control perspective. However, fourth-order converters present interesting features that make them superior in certain applications over the second-order converters [2.2, 2.7].

### 2.1.2.1 Modified switching-capacitor cell - Cell C

As mentioned in section 2.1.1.2, current sources and sinks generally do not exist in practice. For this reason, the Cell B input and output are modified with two inductors as shown in Figure 2.7 resulting in a new cell (Cell C) where, current sources and sinks are transformed to practical voltage sources and sinks. Because Cell C is symmetrical when viewed from terminals $a-c$ and $b-c$, only three unique unidirectional converters, voltage type buck, boost, and buck-boost, will be synthesized from rotation of terminals a , b and c ; see Figure 2.8. For the three converters (b1C, B1C and bB1C), $C_{o}$ is optional as the output current $I_{o}$ is actually continuous. Inserting $C_{o}$ (converts the output current source to a voltage source) decreases the output voltage ripple, which is necessary for some applications. However, it increases the converter order from three to four, consequently increasing control complexity. The same voltage conversion ratios for the voltage buck, boost, and buck-boost converters illustrated in equations (2.4) to (2.6) apply. The converter states, as input current $\left(I_{i n}\right)$, output current $\left(I_{o}\right)$, switch and diode currents ( $I_{s l}$ and $I_{D 2}$ ), transfer capacitor voltage $\left(V_{C}\right)$, switch and diode reverse voltages are expressed in terms of the converter's duty ratio $(D)$. Figure 2.9 to Figure 2.11 show the different waveforms. Idealized models are used to generate the illustrating waveforms for all circuit. As the switching time is selected relatively low in compare with the circuit time constants, the voltages across the capacitors and the currents through inductors are considered to be linear waveforms. For converter b1C as an example, the current and voltage waveforms can be calculated from the two circuit configurations of the power converter during $t_{\text {on }}$ and $t_{\text {off }}$ shown in Figure 2.12. The average state space model of the converter is:

$$
\left[\begin{array}{l}
\dot{I}_{L 1}  \tag{2.10}\\
\dot{V}_{c} \\
\dot{I}_{L 2}
\end{array}\right]=\left[\begin{array}{ccc}
\frac{-R}{L_{1}} & -\frac{(1-D)}{L_{1}} & -\frac{R}{L_{1}} \\
\frac{(1-D)}{C} & 0 & \frac{-D}{C} \\
-\frac{R}{L_{2}} & \frac{D}{L_{2}} & \frac{-R}{L_{2}}
\end{array}\right]\left[\begin{array}{l}
I_{L 1} \\
V_{c} \\
I_{L 2}
\end{array}\right]+\left[\begin{array}{c}
\frac{1}{L_{1}} \\
0 \\
0
\end{array}\right]\left[V_{\text {in }}\right]
$$

The average values of the states $I_{L l}, V_{c}$ and $I_{L 2}$ can be calculated by setting their derivatives to zero and solving the resultant three equations:

$$
\begin{align*}
& 0=\frac{-R}{L_{1}} I_{L 1}-\frac{(1-D)}{L_{l}} V_{c}-\frac{R}{L_{1}} I_{L 2}+\frac{1}{L_{1}} V_{i n} \\
& 0=\frac{(1-D)}{C} I_{L 1}-\frac{D}{C} I_{L 2}  \tag{2.11}\\
& 0=-\frac{R}{L_{2}} I_{L 1}+\frac{D}{L_{2}} V_{c}-\frac{R}{L_{2}} I_{L 2}
\end{align*}
$$

Solving (2.11) leads to:

$$
\begin{align*}
& \bar{I}_{i n}=\bar{I}_{L 1}=D I_{o} \\
& \bar{I}_{L 2}=(1-D) I_{o}  \tag{2.12}\\
& \overline{V_{c}}=V_{i n}
\end{align*}
$$

Because the average voltage across the any inductor is zero over the complete cycle (during $t_{s}$ ), the current ripple components $\left(\Delta I_{L 1}\right)$ and $\left(\Delta I_{L 2}\right)$ can be calculated from the circuit configuration during on and off periods. $\Delta I_{L 1}$ is calculated during $t_{o n}$ from the voltage across $L_{l}$ as:

$$
\begin{align*}
& L_{l} \frac{\Delta I_{L 1}}{\Delta t}=V_{i n}-V_{o}  \tag{2.13}\\
& \Delta I_{L 1}=\frac{D(1-D) V_{i n}}{L_{l}} t_{s}
\end{align*}
$$

And $\Delta I_{L 2}$ is calculated during $t_{o f f}$ from the voltage across $L_{2}$ as:

$$
\begin{align*}
& L_{2} \frac{\Delta I_{L 2}}{\Delta t}=V_{o}  \tag{2.14}\\
& \Delta I_{L 2}=\frac{D(1-D) V_{i n}}{L_{2}} t_{s}
\end{align*}
$$

Similarly, the average current through the capacitor $C$ is equal to zero over the complete cycle and the voltage ripple $\left(\Delta V_{c}\right)$ is calculated from either $t_{o n}$ or $t_{o f f}$. Calculating it from $t_{\text {off: }}$


Figure 2.7. SMPS using the switching-capacitor Cell C

(a) Terminals: (a-1), (b-3,4), (c-2),
b1C

(b) Terminals: (a-2), (b-3,4), (c-1)

(c) Terminals: (a-1), (b-2), (c-3,4) bB1C
Figure 2.8. Three DC-DC current converters from Cell C: (a) buck, (b) boost, and (c) buck-boost (Ćuk).


(a) Input current $I_{i n}$

$\Delta t_{0}$
$=D(1-D) t_{s} V_{\ln }\left(\frac{1}{L_{1}}+\frac{1}{L_{2}}\right)$
(c) Output current $I_{o}$

(e) Switch $S_{l}$ current

(g) Switch $S_{l}$ forward voltage
(b) Inductor $L_{2}$ current


$$
\bar{V}_{c}=V_{i n}
$$

$$
\Delta V_{c}=D(1-D) \frac{I_{o} t_{s}}{C}
$$

(d) Capacitor $C$ voltage

(f) Diode $D_{2}$ current

(h) Diode $D_{2}$ reverse voltage

Figure 2.9. b1C components voltages and currents.

(a) Input current $I_{i n}$

(c) Output current $I_{o}$

(e) Switch $S_{I}$ current

(g) Switch $S_{l}$ forward voltage

$$
\begin{array}{c:cc}
\Delta V & \bar{V}_{c}=\frac{1}{(1-D)} V_{i n} \\
\hdashline{\underset{D}{D}}_{c} & \Delta V_{c}=D \frac{\bar{I}_{o} t_{s}}{C}
\end{array}
$$

(d) Capacitor $C$ voltage


$$
\hat{I}_{D 2}=\frac{\bar{I}_{o}}{(1-D)}
$$

(f) Diode $D_{2}$ current

(h) Diode $D_{2}$ reverse voltage Figure 2.10. B1C components voltages and currents

(a) Input current $I_{\text {in }}$

(c) Capacitor $C$ voltage

(e) Diode $D_{2}$ current

$$
\hat{I}_{D 2}=\frac{\bar{I}_{o}}{(1-D)}
$$



$$
\hat{V}_{D 2}=\frac{1}{(1-D)} V_{i n}
$$

(g) Diode $D_{2}$ reverse voltage

Figure 2.11 bB 1 C ' $C$ uk' components voltages and currents.


Figure 2.12. Two configurations of b1C converter: (a) $t_{o n}$ and (b) $t_{\text {off }}$

The waveforms of all other converters can be calculated by the same approach. For all the converters emerging from Cell C , the input current $I_{i n}$ and the output current $I_{o}$ are continuous. This is an important feature of the power converters and will be discussed in the next chapters.

### 2.1.2.2 Modified switching-capacitor cell - Cell D

Figure 2.13 shows another cell, Cell $D$, that can be obtained from interchanging the capacitor with one of the two switches. Unlike the previous cells, the Cell D is not symmetric if viewed from the two ports and hence, six distinct different converters are generated from rotating terminals a-b-c relative to $1-2-3$. The resultant six converters are: two voltage-type buck, two voltage-type boost and two voltage-type buck-boost, converters, as shown in Figure 2.14. The voltage conversion ratios for the Cell $D$ are the same as equations (2.4) to (2.6). Because the cell has input and output inductors, the output shunt capacitor $C_{o}$ is not mandatory. The relations between voltages and currents of the converters and the duty ratio can be found in Appendix B.


Figure 2.13. SMPS using the switching-capacitor Cell D.


Figure 2.14. Six voltage converters from Cell D: (a),(b) buck, (c),(d) boost, and (e),(f) buck-boost.

### 2.1.2.3 Switching-inductor-capacitor cell - Cell E

Cell E consists of two inductors, one capacitor and two switches. The cell configuration is shown in Figure 2.15 as one inductor, one switch and the capacitor are delta-connected while the remaining inductor and switch are placed in the input and output ports. Again, rotating the terminals $\mathrm{a}, \mathrm{b}$, and c with respect to terminals 1, 2 and $(3,4)$ results in six converters, shown in Figure 2.16. Because the cell has an inductor in only one port, the output shunt capacitor $C_{o}$ is mandatory for the converters that do not have an inductor in the output side. The relations between voltages and currents of the converters and the duty ratio are illustrated in Appendix B.


Figure 2.15. SMPS using the switching-inductor-capacitor Cell E.


Figure 2.16. Six voltage converters from Cell E: (a),(b) buck, (c),(d) boost, and (e),(f) buckboost.

### 2.1.2.4 Switching-inductor-capacitor cell - Cell $\boldsymbol{F}$

Cell $F$, shown in Figure 2.17, results from interchanging the positions of the switch and inductor in the delta-connected circuit in Cell E. The six resultant converters are, two voltage-type buck (b1F and b2F), two voltage-type boost (B1F and B2F), and two voltage-type buck-boost (bB1F and bB2F), see Figure 2.18. The relations between voltages and currents of the converters and the duty ratio are shown in Appendix B. Converters b1F, b2F, B1F and bB1F must have an output capacitor $C_{o}$ to filter the output current, while this capacitor is optional for converters B2F and bB2F, since the output is filtered by an inductor.


Figure 2.17. SMPS using the switching-inductor-capacitor Cell F.


Figure 2.18. Six voltage converters from Cell F: (a),(b) buck, (c),(d) boost, and (e),(f) buck-

### 2.1.2.5 Switching-inductor-capacitor cell - Cell $\boldsymbol{G}$

Cell G, shown in Figure 2.19, has six converters: two voltage-type buck (b1G and b2G), two voltage-type boost (B1G and B2G), and two voltage-type buck-boost (bB1G and bB2G), see Figure 2.20. Cell G is different to all of the previous cells in its voltage conversion ratios. The voltage ratios for Cell $G$ are shown in equations (2.16) to (2.18). The duty ratios of these converters have discontinuity and defined by the following inequalities: $0<\mathrm{D}<0.5$ and $0.5<\mathrm{D}<1$. The relations between voltages and currents of the converters and the duty ratio are shown in Appendix B.


Figure 2.19. SMPS using the switching-inductor-capacitor Cell G.


Figure 2.20. Six voltage converters from Cell G: (a),(b) buck, (c),(d) boost, and

Converters b1G, B1G, B2G and bB1G must have an output capacitor $C_{o}$ to filter the output current, while this capacitor is optional for converters b2G and bB2G, because of the output inductor. According to the voltage ratios of the first four converters, the output voltage polarity can be positive or negative when the duty ratio is higher or lower than 0.5 . This means that if an anti-parallel diode is inserted with the switch $S_{I}$ and an anti-parallel switch $S_{2}$ is inserted with the diode $D_{2}$, these four converters can give output voltages with both polarities. This feature is unique in this group of converters and will be discussed in the subsequent chapters.

$$
\begin{align*}
& M(D)=\frac{V_{o}}{V_{\text {in }}}=\frac{2 D-1}{D} \text { for b1G and b2G }  \tag{2.16}\\
& M(D)=\frac{V_{o}}{V_{\text {in }}}=\frac{1-D}{1-2 D} \text { for B1G and B2G } \\
& M(D)=\frac{V_{o}}{V_{\text {in }}}=\frac{D}{1-D} \text { for bB1G and bB2G } \tag{2.17}
\end{align*}
$$

### 2.1.2.6 Inductor-capacitor cell - Cell P

Cell $P$ is shown in Figure 2.21 where the capacitor and the two inductors form a delta-connection. This cell has not been presented or discussed in the literature before. Since the average voltage across each inductor is zero, and hence the average voltage across the capacitor is zero, the power is transferred through the ripple capacitor voltage. Because the Cell $P$ is symmetrical when viewed from both ports, three unique converters are generated from rotation of terminals $\mathrm{a}, \mathrm{b}$ and c . These three converters are: voltage buck (b1P), voltage boost (B1P), and voltage buck-boost (bB1P); see Figure 2.22. The transfer functions for Cell P are the same as equations (2.4) to (2.6). The relations between voltages and currents of the converters and the duty ratio are shown in Figure 2.23 to Figure 2.25 .


Figure 2.21. SMPS using the switching-inductor-capacitor Cell $P$.


Figure 2.22. Three DC-DC current converters from Cell P: (a) buck, (b) boost, and
$\overline{I_{i n}} \underset{\sim}{\square}$
(a) Input current $I_{\text {in }}$

$\bar{I}_{L 2}=(1-D) \bar{I}_{o}$ $\Delta I_{L 2}=\frac{(1-D) D t_{s} V_{i n}}{L_{2}}$
(c) Inductor $L_{2}$ current

(e) Output current $I_{o}$

(g) Switch $S_{l}$ forward voltage


$$
\bar{I}_{L 1}=D \bar{I}_{o}
$$

$$
\Delta I_{L 1}=\frac{(1-D) D t_{s} V_{i n}}{L_{1}}
$$

(b) Inductor $L_{l}$ current

(d) Capacitor $C$ voltage

(f) Diode $D_{2}$ current

(h) Diode $D_{2}$ reverse voltage

$$
\hat{I}_{D 2}=\bar{I}_{o}
$$

Figure 2.23. b1P components voltages and currents.


$$
\begin{gathered}
\bar{I}_{i n}=\frac{\bar{I}_{o}}{(1-D)} \\
\Delta I_{i n}=D t_{s} V_{i n}\left(\frac{1}{L_{1}}+\frac{1}{L_{2}}\right)
\end{gathered}
$$



$$
\begin{gathered}
\bar{L}_{L 1}=\frac{D}{(1-D)} \bar{I}_{o} \\
\Delta I_{L 1}=D \frac{t_{s} V_{i n}}{L_{1}}
\end{gathered}
$$

(a) Input current $I_{i n}$


$$
\begin{gathered}
\bar{I}_{L 2}=\bar{I}_{o} \\
\Delta I_{L 2}=D \frac{t_{s} V_{i n}}{L_{2}}
\end{gathered}
$$

(c) Inductor $L_{2}$ current
$\overline{\bar{v}}_{c}=0$
(e) Capacitor $C$ voltage

(g) Diode $D_{2}$ current

$$
\hat{I}_{D 2}=\frac{\bar{I}_{o}}{(1-D)}
$$

(b) Inductor $L_{l}$ current
$\Delta V_{o}=D \frac{\bar{I}_{o} t_{s}}{C_{o}}$

$$
\Delta I_{o}=\frac{D(1-D) t_{s} \bar{I}_{o}^{2}}{C_{o} V_{i n}}
$$

(d) Output current $I_{o}$

(f) Switch $S_{l}$ current

(h) Switch $S_{l}$ forward voltage

Figure 2.24. B1P components voltages and currents.


$$
\begin{gathered}
\bar{I}_{i n}=\frac{D}{(1-D)} \bar{I}_{o} \\
\hat{I}_{i n}=\frac{\bar{I}_{o}}{(1-D)}
\end{gathered}
$$

(a) Input current $I_{i n}$

(e) Output current $I_{o}$

(g) $\mathrm{Sw} S_{l}$ forward voltage

$\bar{L}_{L 1}=\frac{D}{(1-D)} \bar{I}_{o}$

$$
\Delta \Delta_{L 1}=\frac{D t_{s} V_{i n}}{L_{1}}
$$

(b) Inductor $L_{l}$ current

$\bar{V}_{c}=0$
$\Delta V_{c}=D \frac{\bar{I}_{o} t_{s}}{C}$
(d) Capacitor $C$ voltage


$$
\hat{I}_{D 2}=\frac{\bar{I}_{o}}{(1-D)}
$$

(f) Diode $D_{2}$ current


$$
\hat{V}_{D 2}=\frac{1}{(1-D)} V_{i n}
$$

(h) Diode $D_{2}$ reverse voltage

Figure 2.25. bB1P components voltages and currents.

### 2.2 Isolated Converters

In general practice, power converters are required to provide energy to loads which are connected at different potentials [2.16]. Moreover, the regulations for some applications stipulate that the output side should be isolated from the input side for the safety of equipment or people who are handling the equipment [2.17]. Consequently, there needs to be isolation between the source and load sides, created by an electro-magnetic barrier or coupling. These converters are called Galvanicallyisolated power converters [2.18]. Figure 2.26 shows the basic structure for an isolated power converter. $N_{l}, V_{l}$ and $I_{l}$ represent the turn's ratio, voltage and current of the transformer primary side while $N_{2}, V_{2}$ and $I_{2}$ are the turn's ratio, voltage and current of the transformer secondary side.


Figure 2.26. Isolated power converter.

From Faraday's law, the relation between the core flux $\Phi$ and transformer voltages can be represented as [2.19]:

$$
\begin{equation*}
V_{1}=N_{1} \frac{d \phi}{d t} \text { and } V_{2}=N_{2} \frac{d \phi}{d t} \tag{2.19}
\end{equation*}
$$

For ideal transformers, where the flux $\Phi$ is assumed to be fully linked, the VI relations are:

$$
\begin{equation*}
\frac{N_{1}}{N_{2}}=\frac{V_{1}}{V_{2}}=\frac{I_{2}}{I_{1}} \tag{2.20}
\end{equation*}
$$

From equation (2.19), the time domain function can be expressed as:

$$
\begin{equation*}
\phi=\frac{1}{N_{1}} \int V_{1} d t=\frac{1}{N_{2}} \int V_{2} d t \tag{2.21}
\end{equation*}
$$

The main constraint for any converter to be transformer-isolated is that the average of the voltages $V_{l}$ and $V_{2}$, or their integration over a complete switching period, should be zero [2.20]. Otherwise, the flux $\Phi$ increases continuously until reaching the core saturation limit. In Figure 2.27a, the positive and negative areas of volt x time are equal, hence the flux $\Phi$ has finite peak below the transformer saturation limit. While in Figure 2.27b, the positive area is greater than the negative area and the flux is accumulated until the core saturates.

(a) No core saturation

(b) core saturation

Figure 2.27. Transformer primary voltage and core flux.
An example of power converters which are viable for transformer isolation is the bB1C 'Ćuk' converter, shown in Figure 2.28.


Figure 2.28. Transformer-isolated Ćuk converter.

The transfer function of the isolated Cuk converter can be re-written as:

$$
\begin{equation*}
V_{o}=\frac{N_{2}}{N_{1}} \cdot \frac{D}{1-D} \cdot V_{\text {in }} \tag{2.22}
\end{equation*}
$$

Figure 2.29 shows the time domain waveform of transformer voltages and core flux


Figure 2.29. Transformer voltages and core flux.
Since the SEPIC, Zeta, and bB1P transfer power solely through the cell capacitor, they too can be transformer coupled like the Ćuk converter in Figure 2.28. The isolated buck boost converter is isolated by coupled circuit energy storage, not transformer action; hence core volume is proportional to stored energy. Tables 2.1 and 2.2 summarize the main features of the power converters families.

### 2.3 Summary

The main single-switch single-diode switched mode power converter topologies were introduced in this chapter. Different converters were generated from their fundamental cells according to a systematic procedure of derivation. Most of these power converters have not been discussed when used in dc/ac mode before. The relationships between the converters device voltages and currents were introduced when they operate in a current continuous mode. Different applications require power converters with different features, such as: continuous input current, continuous output current, voltage bucking or boosting, etc. Hence, analysing all the converters, considering the features they offer is necessary. Moreover, this chapter has introduced a family of galvanic isolated power converters that exploit highfrequency transformers that reduce their size and cost. Finally, a brief comparison between different power converters properties was presented.

Table 2.1. Summary of different topologies main features

| $\begin{aligned} & 60 \\ & \frac{0}{60} \\ & \frac{0}{0} \\ & 0 \\ & 0 \end{aligned}$ |  | Voltage Conversion Ratio | $\stackrel{V_{o}}{\text { Polarity }}$ | Continuous $I_{i n}$ (capacitor unnecessary) | Continuous $I_{o}$ (capacitor unnecessary) | high- <br> frequency isolation | $\begin{aligned} & \boldsymbol{I}_{\text {in }} \boldsymbol{r i p p l e} \\ & \text { (if } \\ & \text { continuous) } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { n } \\ & 0 \\ & 0.0 \\ & 0 \\ & 0 \\ & 0 \end{aligned}$ | b1A | D | + | No | Yes | No |  |
|  | b1C | D | + | Yes | Yes | No | High |
|  | b1D | D | + | Yes | Yes | No | High |
|  | b2D | D | + | Yes | Yes | No | Low |
|  | b1E | D | + | No | Yes | No |  |
|  | b2E | D | + | No | Yes | No |  |
|  | b1F | D | + | No | No | No |  |
|  | b2F | D | + | Yes | No | No | Low |
|  | b1G | $\frac{2 D-1}{D}$ | $\pm$ | No | No | No |  |
|  | b2G | $\frac{2 D-1}{D}$ | $\pm$ | No | Yes | No |  |
|  | b1P | D | + | No | Yes | No |  |
|  | B1A | $\frac{1}{1-D}$ | + | Yes | No | No | High |
|  | B1C | $\frac{1}{1-D}$ | + | Yes | Yes | No | High |
|  | B1D | $\frac{1}{1-D}$ | + | Yes | Yes | No | High |
|  | B2D | $\frac{1}{1-D}$ | + | Yes | Yes | No | High |
|  | B1E | $\frac{1}{1-D}$ | + | Yes | No | No | Low |
|  | B2E | $\frac{1}{1-D}$ | + | Yes | No | No | Low |
|  | B1F | $\frac{1}{1-D}$ | + | No | No | No |  |
|  | B2F | $\frac{1}{1-D}$ | + | No | Yes | No |  |
|  | B1G | $\frac{1-D}{1-2 D}$ | $\pm$ | No | No | No |  |
|  | B2G | $\frac{l-D}{l-2 D}$ | $\pm$ | Yes | No | No | High |
|  | B1P | $\frac{1}{1-D}$ | + | Yes | No | No | High |

Table 2. 2. Summary of different topologies main features (Continued)

|  | $\begin{aligned} & 30 \\ & 0 \\ & 0 \\ & 0 \\ & 0 \end{aligned}$ | Voltage Conversion Ratio | $V_{o}$ <br> Polarity | Continuous $\boldsymbol{I}_{\text {in }}$ (capacitor unnecessary) | Continuous $I_{o}$ (capacitor unnecessary) | high- <br> frequency isolation | $\begin{gathered} \boldsymbol{I}_{\text {in }} \text { ripple } \\ \text { (if } \\ \text { continuous) } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 00.000000000$\vdots$000 | bB1A | $\frac{D}{1-D}$ | - | No | No | No |  |
|  | bB1C | $\frac{D}{1-D}$ | - | Yes | Yes | Yes | High |
|  | bB1D | $\frac{D}{1-D}$ | - | Yes | Yes | Yes | Low |
|  | bB2D | $\frac{D}{1-D}$ | - | Yes | Yes | Yes | High |
|  | bB1E | $\frac{D}{1-D}$ | - | No | No | No |  |
|  | bB2E | $\frac{D}{1-D}$ | - | No | No | No |  |
|  | bB1F | $\frac{D}{1-D}$ | - | Yes | No | Yes | Low |
|  | bB2F | $\frac{D}{1-D}$ | - | No | Yes | Yes |  |
|  | bB1G | $\frac{D}{1-D}$ | + | Yes | No | Yes | High |
|  | bB2G | $\frac{D}{1-D}$ | + | No | Yes | Yes |  |
|  | bB1P | $\frac{D}{1-D}$ | - | No | No | Yes |  |

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## Chapter 3

## Modelling and Control of Power Electronic Converters

This chapter presents a discussion of the main modelling methods that can be used to describe power electronic converters, including the theoretical basis that supports each modelling method, and its attributes, with the aid of illustrative simulations. The models developed are then used to explain the main control approaches for power converters used in subsequent chapters. The major findings and observations drawn from this chapter will be relied upon in the subsequent chapters so as to avoid repetition.

### 3.1 Model types

In general, there are two major modelling methodologies for the types of systems that will be investigated in this thesis:

- Black-box model is based on the information of the process performance of the modelled system and its response to the input signals [3.1].
- Gray-box model, which is used in non-physical systems or mixed systems of physical, biological, or economic systems [3.1].

Modelling of power converters depends on knowledge of the physical behaviour of the systems under investigation; this means that it must be described mathematically using black-box models. For such systems, state variables are used to describe the system energy-time variation [3.1]. For a power converter, all the mathematical equations used to model the systems stem from Kirchhoff's and Ohm's laws. Normally, some assumptions are made to simplify the modelling process, without significantly affecting the validity of the models being developed. Some of these assumptions are:

1- Switches are assumed to be ideal with two states, zero ohm resistance during conduction (turned on) period and open circuit (infinite ohm resistance) during the turned off period.
2- Voltage and current sources are considered perfect sources. This means that they have no internal power dissipation, that is, no resistance. However,
series equivalent resistance may be incorporated to increase the accuracy of the power converter model.

3- Energy storage inductors and capacitors of the power converters are assumed to be linear and time-invariant. This means inductance and capacitance values are independent of current flow through the inductor and voltage across the capacitor.

### 3.2 Detail switched model

Power converters have several circuit configurations during single switching period $t_{s .}$ These configurations can be represented as different circuits consisting of power sources, sinks and energy storage elements. Such power circuits are usually described by piecewise differential equations, with each differential equation describing a specific part of the switching period. The switched model can describe the electromagnet transient of power converters, with sufficient accuracy [3.2]. The switched model provides an initial point for the derivation of other types of important models, which are necessary for control design, such as averaged large-signal, smallsignal, and generalized models. Tymerski et al. [3.3] established the generic power electronic converter, which has $N$ different configurations. This general converter model can be interpreted by the following differential equation:

$$
\begin{align*}
& \frac{d}{d t} x(t)=A_{i} \cdot x(t)+B_{i} \cdot e(t), \quad t_{i} \leq t \leq t_{i+1} \\
& \text { where }  \tag{3.1}\\
& \sum_{i=1}^{N}\left(t_{i}-t_{i-1}\right)=t_{s}
\end{align*}
$$

where, $x(t)$ defines the column vector with $n$ states and $e(t)$ is the $p$-length vector of the system power sources. The state variables in $x$ are chosen to describe the energy increase or decrease in the passive elements. This energy is measured in the inductors current and/or capacitor voltages. If the number of the non-parallel capacitors in the power converter is $n_{C}$ and the number of non-series inductors is $n_{L}$, the system order $n$ can be calculated as $n=n_{C}+n_{L} . t_{i}$ defines the switching instants between the $N$ configurations corresponding to configuration $i, A_{i}(n \times n)$ and $B_{i}(n \times$ $p$ ) are the state and input matrices [3.2]. For a single-switch single-diode power converter such as depicted in Figure 3.1, there are two possible circuit configurations, so $N=2$ and equation (3.1) can be re-written as:

$$
\begin{equation*}
\frac{d}{d t} x(t)=\sum_{i=1}^{2}\left(A_{i} \cdot x(t)+B_{i} \cdot e(t)\right) \cdot u_{i}, \tag{3.2}
\end{equation*}
$$

where $u(t)$ is the time variant switching function that describes the power converter circuit configurations and takes a value of 1 or 0 , depending on which configuration is active.


Figure 3.1. Basic single-switch single-diode power electronics converters.

However, in the power converters to be studied in this chapter and throughout the thesis, only the first type of switching function will be used because the converters operate in a current continuous mode and no thyristor type switches, which functionality wise depend on the state $x$.

### 3.2.1 Description of the modelling process

Intuitive information about power converter operation is necessary to obtain the switched model. A complete knowledge of the following aspects is indispensable:

- The circuit configuration that describes each switching time interval (switch state).
- Differential equations that describe each circuit configuration

For the single-switch single-diode power converters in Figure 3.1, the two circuit configurations are complementary. The modelling process can be summarized as:

1- The state variables $x$ are selected as capacitor voltages and inductor currents.
2- The mathematical expression of the transistor voltage and diode current are written during the ON and OFF periods.

3- Kirchhoff's voltage law expresses the derivatives of the inductor currents and Kirchhoff's current law is used to obtain the derivatives of the capacitor voltages.
4- The switched variables are written in terms of the switching function $u$.
5- The switched variables are replaced with controlled voltage and current sources in the state-space equations of step 3.

### 3.2.2 Illustrative examples

The converter b1A, shown in Figure 2.3a, can be used to explain the modelling process for a simple $1^{\text {st }}$ order power converter. The switch $S_{I}$ is driven by the switching time function $u(t)$ shown in Figure 3.2. The switching function $u(t)$ can be expressed as:

$$
u(t)= \begin{cases}1, & 0 \leq t<D t_{s}  \tag{3.3}\\ 0, & D t_{s} \leq t<t_{s}\end{cases}
$$



Figure 3.2. b1A in ON and OFF states.
The converter duty ratio $D$ is equal to the average value of the switching function $u(t)$. The converter equations during the ON and OFF periods are written as:

$$
\left\{\begin{array}{lc}
V_{i n}=L \frac{d i_{L}}{d t}+R i_{L}, & 0 \leq t<D t_{s}  \tag{3.4}\\
0=L \frac{d i_{L}}{d t}+R i_{L}, & D t_{s} \leq t<t_{s}
\end{array}\right.
$$

Equation (3.4) may be re-written in generic form that describes both the switching intervals as:

$$
\begin{gather*}
V_{i n} \cdot u(t)=L \frac{d i_{L}}{d t}+R i_{L} \\
\frac{d i_{L}}{d t}=-R / L_{A}^{i_{L}}+\underbrace{1 / V_{i n}}_{B} \cdot u(t), \quad i_{L}=x \tag{3.5}
\end{gather*}
$$

The differential equation (3.5) describes the equivalent behaviour of the power converter and leads to the exact equivalent circuit shown in Figure 3.3. The exact waveform of the inductor current $I_{L}$ is shown in Figure 3.4. By solving the differential equation (3.5) in time domain, the current at each sample time, $I_{L}\left(t_{s}\right)$, $I_{L}\left(2 t_{s}\right)$, and so on, can be evaluated as:

$$
\begin{equation*}
I_{L}\left([k+1] t_{s}\right)=\left(I_{L}\left(k t_{s}\right)-\frac{V_{i n}}{R}\right) e^{-\frac{R}{L} t_{s}}+\frac{V_{i n}}{R} e^{-\frac{R}{L}(1-D) t_{s}} \tag{3.6}
\end{equation*}
$$



Figure 3.3. Exact equivalent circuit of b1A.


Figure 3.4. $I_{L}$ Exact waveform of b1A.
Equation (3.6) represents what is called the Sampled-data model.
bB1C 'Ćuk' converter, where inductors $L_{1}$ and $L_{2}$ are not coupled, is an example of modelling a higher order power converter. Figure 3.5 shows the converter in two states $u=1$ when switch $S_{I}$ is turn on and the diode $D_{2}$ is reverse biased and $u=0$ when switch $S_{l}$ is off and diode $D_{2}$ is forward biased.


Figure 3.5. The two possible configurations of the Ćuk converter.

There are two inductors and one capacitor so $n=3$ and $p=1$ because there is a single switching function. As stated, the differential equations are derived using Kirchhoff's laws. The equations of the first configuration when $u=1$ is:

$$
\begin{align*}
& V_{i n}=L_{l} d i_{L 1} / d t \\
& C^{d v_{c}} / d t=i_{L 2}  \tag{3.7}\\
& v_{o}=v_{c}-L_{2} d i_{L 2} / d t=R i_{L 2}
\end{align*}
$$

Using the same approach, the differential equations of the configuration when $u=0$ are:

$$
\begin{align*}
& V_{i n}=v_{c}-L_{l} d i_{L 1} / d t \\
& C^{d v_{c}} / d t=i_{L 1}  \tag{3.8}\\
& v_{o}=-L_{2}{ }^{d i_{L 2}} / d t=R i_{L 2}
\end{align*}
$$

The two sets of equations, (3.7) and (3.8), are multiplied by $u$ and (1-u) respectively, leading to:

$$
\begin{align*}
& \dot{i_{L 1}}=-\frac{(1-u)}{L_{l}} v_{c}+\frac{l}{L_{1}} V_{i n} \\
& \dot{V_{c}}=\frac{(1-u)}{C} i_{L 1}+\frac{u}{C} i_{L 2}  \tag{3.9}\\
& \dot{i}_{L 2}=-\frac{u}{L_{2}} v_{c}-\frac{R}{L_{2}} i_{L 2}
\end{align*}
$$

By defining $x=\left[\begin{array}{lll}I_{L 1} & V_{C} & I_{L 2}\end{array}\right]^{\mathrm{T}}$, the state vector of the power converter, the differential equations can be put into matrix form as:

$$
\dot{x}=\left[\begin{array}{ccc}
0 & -1 / L_{l} & 0  \tag{3.10}\\
1 / C & 0 & 0 \\
0 & 0 & 0
\end{array}\right] x+\left[\begin{array}{c}
u v_{c} / L_{l} \\
u i_{L I} / C+u i_{L I} / C \\
-u v_{c} / L_{l}
\end{array}\right] x+\left[\begin{array}{c}
V_{i n} / L_{l} \\
0 \\
0
\end{array}\right]
$$

Re-arranging equation (3.9) in the form of equation (3.2) gives:

$$
\begin{gather*}
\dot{x}=A x+B x u+d \\
A=\left[\begin{array}{ccc}
0 & -l / L_{l} & 0 \\
1 / C & 0 & 0 \\
0 & 0 & 0
\end{array}\right], \quad B=\left[\begin{array}{ccc}
0 & l / L_{l} & 0 \\
1 / C & 0 & 1 / C \\
0 & -1 / L_{2} & 0
\end{array}\right], \quad d=\left[\begin{array}{c}
V_{i n} / L_{l} \\
0 \\
0
\end{array}\right] \tag{3.11}
\end{gather*}
$$

The switched model, shown in Figure 3.6, is obtained from equation (3.9). In the first equation, the dependent voltage source in the first circuit is a function of the inductor in the second circuit. In the same way, the second circuit is obtained from the second equation and the third circuit is obtained from the third equation.


Figure 3.6. Equivalent circuit of switched model of Ćuk converter

Figure 3.7 shows simulation results of Ćuk converter with the switched model using MATLAB ${ }^{\circledR}$-Simulink ${ }^{\circledR}$ 。


Figure 3.7 Dynamic behaviour of the switched model of the ideal bB1C (Ćuk) converter $\left(V_{\text {in }}=100, L_{1}=L_{2}=1 \mathrm{mH}, C=10 \mu \mathrm{~F}\right.$, ts $=50 \mathrm{kHz}$, and $\left.\mathrm{R}=20 \Omega\right)$.

### 3.3 Average model

The average models imitate the average behaviour of the states in the power converter. The states average, changes during system operation when excited with different duty ratios. Because the switching period $t_{s}$ window is small compared with converter dynamics, the average state values are assumed to be constant during each switching period. The time window of the average model is considered as if it is sliding on the time axis and therefore will be defined as the sliding (moving) average. For example, if the state under consideration is an inductor current $I_{L}$, the average current can be approximated as:

$$
\begin{equation*}
\left\langle I_{L}\right\rangle_{O}(t)=\frac{1}{t_{s}} \int_{t-t_{s}}^{t} i_{L} d \tau \tag{3.12}
\end{equation*}
$$

Because the average model provides information about the state at each sample time, and unlike the switched model, fails to give the information between two successive sample points, it is considered to be less accurate than the switched model. Averaged models focus on observing the low-frequency behaviour of power electronic converters and do not sense the converter switching and its high-frequency variations. To some extent, this is acceptable in the control design of power
converters as filters are used in most converters to limit the high-frequency voltages and currents (ripple) [3.4] Consequently, a continuous-time model, which is convenient for classical control strategies, is employed [3.5].

### 3.3.1 Large-signal average model

Generally, power converters are non-linear systems [3.6]. This means that the converter dynamics may change with the operating point; with the converter's duty ratio $D$ [3.7]. However, it is necessary to obtain linear models around the converter's equilibrium operating point [3.1]. This is because the designer needs to transform the power converter's discontinuous model (exact model) into a time invariant model and a continuous model, which is required for certain control laws. These types of models were introduced in the early 1970's [3.2].

### 3.3.1.1 Principles and definitions

To derive the average model of a power electronic converter, some fundamental definitions and principles need explaining and unifying.
a) Sliding average

Sliding average (or local average), illustrated in Figure 3.8, defines the average of a certain function $f(t)$ over a time span $t_{s}$. This can be expressed as:

$$
\begin{equation*}
\langle f(t)\rangle_{o}(t)=\frac{1}{t_{s}} \int_{t-t_{s}}^{t} f(\tau) d \tau \tag{3.13}
\end{equation*}
$$

The difference between the classical average of function $f(t)$ and the moving average $\langle f(t)\rangle_{o}$ is that the latter is time-dependent because time span $t_{s}$ continuously changes its position with respect to the time axis [3.2]. However, they become identical when $f(t)$ reaches the steady state point.


Figure 3.8. Moving average illustration.

Intuitively, because the time derivation and the sliding averaging operation are commutative, the time derivative of any function sliding average is equal to the sliding average of the function time derivative [3.8]:

$$
\begin{equation*}
\frac{d}{d t}\langle f(t)\rangle_{o}(t)=\left\langle\frac{d}{d t} f(t)\right\rangle_{o}(t)=\frac{1}{t_{s}}\left(f(t)-f\left(t-t_{s}\right)\right) \tag{3.14}
\end{equation*}
$$

b) Power converter circuit average

The circuit average describes the average behaviour of the power electronic circuit provided it has linear passive elements [3.9]. This means that the inductor, capacitor and resistor values remain constant during operation. To obtain the average model of a power electronic circuit, the state variables are replaced by their averages and the products of the state variables are replaced by the product of the averages. For example, in the presented Ćuk converter switched model in Figure 3.5, the state variables $I_{L 1}, I_{L 2}, V_{c}$, and $u$ are replaced by their averages $\left\langle I_{L 1}\right\rangle_{0},\left\langle I_{L 2}\right\rangle_{0},\left\langle V_{c}\right\rangle_{0}$, and $D$. So, the state products can be calculated by their approximated values [3.9]:

$$
\begin{align*}
& \left\langle(1-u) \cdot v_{c}\right\rangle_{O} \approx\left\langle V_{c}\right\rangle_{O}(1-D) \\
& \left\langle(1-u) \cdot i_{L 1}\right\rangle_{0} \approx\left\langle I_{L 1}\right\rangle_{O}(1-D)  \tag{3.15}\\
& \left\langle u \cdot i_{L 2}\right\rangle_{O} \approx\left\langle I_{L 2}\right\rangle_{O} D
\end{align*}
$$

### 3.3.1.2 Analytical average approach

As mentioned, power electronic circuit dynamics can be expressed as:

$$
\begin{equation*}
\frac{d}{d t} x=\sum_{i=1}^{2}\left(A_{i} \cdot x+B_{i} \cdot e\right) \cdot u_{i} \tag{3.16}
\end{equation*}
$$

where $A_{i}$ and $B_{i}$ are state and input matrices related to the state space model for the circuit configuration $i, u_{i}$ is the switching function status, and the vector e shows the converter independent sources. The circuit average can be obtained from:

$$
\begin{equation*}
\frac{d}{d t}\langle x\rangle_{0}=\left\langle\sum_{i=1}^{2}\left(A_{i} \cdot x+B_{i} \cdot e\right) \cdot u_{i}\right\rangle_{0}, \tag{3.17}
\end{equation*}
$$

Considering the linear feature of the converter and the averaging operation, equation (3.17) can be re-written as:

$$
\begin{align*}
\frac{d}{d t}\langle x\rangle_{0} & =\left\langle\sum_{i=1}^{2}\left(A_{i} \cdot u_{i}\right) x+\sum_{i=1}^{2}\left(B_{i} \cdot u_{i}\right) \cdot e\right\rangle_{0}  \tag{3.18}\\
& \approx\left\langle\sum_{i=1}^{2}\left(A_{i} \cdot u_{i}\right)\right\rangle_{0}\langle x\rangle_{0}+\left\langle\sum_{i=1}^{2}\left(B_{i} \cdot u_{i}\right)\right\rangle_{0}\langle e\rangle_{0}
\end{align*}
$$

By introducing the averaged matrices $A_{m}$ and $B_{m}$ :

$$
\begin{equation*}
A_{m}=\left\langle\sum_{i=1}^{2}\left(A_{i} \cdot u_{i}\right)\right\rangle_{0}, B_{m}\left\langle\sum_{i=1}^{2}\left(B_{i}, u_{i}\right)\right\rangle_{0} \tag{3.19}
\end{equation*}
$$

The average model of the power electronic converter can be written as:

$$
\begin{equation*}
\frac{d}{d t}\langle x\rangle_{0}=A_{m}\langle x\rangle_{0}+B_{m}\langle e\rangle_{0} \tag{3.20}
\end{equation*}
$$

Matrices $A_{m}$ and $B_{m}$ are functions of initial values of the state variables and the duty cycle, which does not appear independently in equation (3.20).

### 3.3.1.3 An example

The average model of the B1A converter, in Figure 2.3a, is studied as an example. The two possible converter configurations are shown in Figure 3.9 and their differential equations can be written as:

$$
\left.\left.\begin{array}{c}
\dot{I}_{L}=\frac{1}{L} V_{i n}  \tag{3.21}\\
\dot{V_{c}}=\frac{-1}{R C} V_{c}
\end{array}\right\} u=1, \quad \begin{array}{c}
\dot{I}_{L}=\frac{1}{L} V_{i n}-\frac{1}{L} V_{c} \\
\dot{V_{c}}=\frac{1}{L} I_{L} \frac{-1}{R C} V_{c}
\end{array}\right\} u=0
$$



Figure 3.9. The two possible configurations of the B1A converter.
The equations can be expressed in state space representation as:

$$
\begin{align*}
& {\left[\begin{array}{l}
\dot{i}_{L} \\
\dot{v}_{c}
\end{array}\right]=\underbrace{\left[\begin{array}{cc}
0 & 0 \\
0 & -1 / R C_{o}
\end{array}\right]}_{A_{1}}\left[\begin{array}{c}
i_{L} \\
v_{c}
\end{array}\right]+\left[\begin{array}{c}
1 / L \\
0
\end{array}\right] V_{i n} \quad, u=1}  \tag{3.22}\\
& \dot{x} \\
& {\left[\begin{array}{c}
\dot{i_{L}} \\
\dot{v_{c}}
\end{array}\right]=\underbrace{\left[\begin{array}{cc}
0 & -1 / L \\
1 / C_{o} & -1 / R C_{o}
\end{array}\right]}_{A_{1}}\left[\begin{array}{c}
i_{L} \\
v_{c}
\end{array}\right]+\left[\begin{array}{c}
1 / L \\
0
\end{array}\right] V_{V_{2}} \quad, u=0}
\end{align*}
$$

To evaluate the average values of the state variables, $A_{m}$ and $B_{m}$ can be approximated as:

$$
\begin{align*}
& A_{m}=A_{1} D+A_{2}(1-D)=\left[\begin{array}{cc}
0 & \frac{-(1-D)}{L} \\
\frac{(1-D)}{C_{o}} & -1 / R C_{o}
\end{array}\right]  \tag{3.23}\\
& B_{m}=B_{1} D+B_{2}(1-D)=\left[\begin{array}{c}
1 / L \\
0
\end{array}\right]
\end{align*}
$$

The relation between the switched converter model and its average equivalent can be visualized in Figure 3.10. By discarding a small dc offset error between the two models, the average model is able to describe the states of the typical converter being studied using a constant duty ratio.


Figure 3.10. B1A capacitor voltage $V_{c}\left(V_{i n}=100 \mathrm{~V}, C_{o}=150 \mu \mathrm{~F}, R=20 \Omega\right.$ and $D=$ 0.5 ): ( - ) Switched model and ( ---- ) Large-signal average model.

However, this error increases when the duty ratio or input voltages are time variant. For illustration of the case when both input voltage and duty cycle vary with time, see Figure 3.11. The accuracy of the large-signal average model is significantly affected when the converter has one or more AC stages and the average value of the derivative terms are not zero. Moreover, from equations in (3.23), the duty ratio $D$ is implicit in the system matrices $A_{m}$ and $B_{m}$. This creates a difficulty for applying the common control strategies that require the system matrices to be time independent and the control inputs ( $D$ and $V_{i n}$ ) appear separately in the control signals vector. This led to the development of the so-called small-signal model which is discussed in the next section.

### 3.3.2 Small-signal model

When linear control strategies are used, it is necessary to build linear models for the power electronic converter around a specified operating point [3.9]. The resultant linearized models are valid for small deviations about the operating point, which is usually dependent on the converter's duty ratio.


Figure 3.11. B1A capacitor voltage $V_{c}$ with varying duty ratio ( $V_{i n}=100 \mathrm{~V}, C_{o}=150$ $\mu \mathrm{F}, R=20 \Omega$ and $D=0.2 \rightarrow 0.65$ ): ( - ) Switched model and ( ---- ) Large-signal

For this reason, they are called small-signal models [3.8]. The relation between the large-signal and the small-signal models is shown in Figure 3.12.


Figure 3.12. Illustration of Relation between large-signal model and small-signal

The superscript $(\sim)$ refers to the small signal deviation of the state $x$ and $x_{e}$ is the state equilibrium point.

### 3.3.2.1 Mathematical modelling

A general nonlinear system can be expressed as:

$$
\left\{\begin{array}{c}
\frac{d}{d t} x=f(x(t), u(t),  \tag{3.24}\\
y=h(x(t), u(t)
\end{array}\right.
$$

where $x, u$ and $y$ are the state, input and output vectors respectively. The steady-state locus of the equilibrium points can be found by setting the derivative terms to zero. The desired small-signal converter model is of the form of the state-space representation, which is suitable for linear control strategies as:

$$
\left\{\begin{array}{c}
\dot{\tilde{x}}=A \tilde{x}+B \tilde{u},  \tag{3.25}\\
\tilde{y}=C \tilde{x}+D \tilde{u}
\end{array}\right.
$$

There are two methods to obtain the small-signal model for a power electronic converter. The first method uses multi-variable Taylor series relations as shown in equation (3.26) [3.1]

$$
\left\{\begin{array}{l}
A=\left(\frac{\partial f(x, u)}{\partial x}\right)_{x_{e}, u_{e}} B=\left(\frac{\partial f(x, u)}{\partial u}\right)_{x_{e}, u_{e}}  \tag{3.26}\\
C=\left(\frac{\partial h(x, u)}{\partial x}\right)_{x_{e}, u_{e}}, D=\left(\frac{\partial h(x, u)}{\partial u}\right)_{x_{e}, u_{e}}
\end{array}\right.
$$

To give an illustrating example of this method, consider the system in (3.27):

$$
\left\{\begin{array}{l}
\dot{x_{1}}=x_{1} x_{2}-x_{2} u  \tag{3.27}\\
\dot{x_{2}}=x_{1}+x_{2} \\
y=3 x_{1}+x_{2}+u
\end{array}\right.
$$

The equilibrium points of the states ( $x_{1 e}$ and $x_{2 e}$ ) and of the output ( $y_{e}$ ) when $u=u_{e}$ are found by equating the time derivatives of the states to zero. This leads to two solutions. The first is $x_{1 e}=x_{2 e}=0$ which is trivial. The second solution is $\left(x_{1 e}=u_{e}\right.$ and $x_{2 e}=-u_{e}$ ) and the output $y_{e}=3 u_{e}$. The system matrices can be calculated from relation (3.26) as:

$$
\begin{align*}
& A=\left[\begin{array}{ll}
\frac{\partial f_{1}(x, u)}{\partial x_{I}} & \frac{\partial f_{1}(x, u)}{\partial x_{2}} \\
\frac{\partial f_{2}(x, u)}{\partial x_{1}} & \frac{\partial f_{2}(x, u)}{\partial x_{2}}
\end{array}\right]_{x_{1 e}, x_{2 e}, u_{e}}=\left[\begin{array}{cc}
x_{2} & x_{1}-u \\
1 & 1
\end{array}\right]_{x_{l e}, x_{2 e}, u_{e}}  \tag{3.28}\\
& =\left[\begin{array}{cc}
-u_{e} & 0 \\
1 & 1
\end{array}\right] \\
& B=\left[\begin{array}{l}
\frac{\partial f_{l}(x, u)}{\partial u} \\
\frac{\partial f_{2}(x, u)}{\partial u}
\end{array}\right]_{x_{1 e}, x_{2 e}, u_{e}}=\left[\begin{array}{c}
-x_{2} \\
0
\end{array}\right]_{x_{l_{e}, x_{2 e}, u_{e}}}=\left[\begin{array}{c}
u_{e} \\
0
\end{array}\right]  \tag{3.29}\\
& C=\left[\begin{array}{ll}
\frac{\partial h(x, u)}{\partial x_{1}} & \frac{\partial h(x, u)}{\partial x_{2}}
\end{array}\right]_{x_{1 e}, x_{2 e}, u_{e}}=\left[\begin{array}{ll}
3 & 1
\end{array}\right], D=\left[\frac{\partial h(x, u)}{\partial u}\right]=1
\end{align*}
$$

The second method for obtaining the small-signal model is by using the perturbed deviations of the states and input as follow [3.10]:

$$
\left\{\begin{array}{l}
\tilde{x}=x-x_{e}  \tag{3.30}\\
\tilde{u}=u-u_{e} \\
\tilde{y}=y-y_{e}
\end{array}\right.
$$

Substituting in the equation set (3.27) leads to:

$$
\left\{\begin{array}{c}
\dot{\tilde{x}}_{1}+\dot{x}_{1 e}=\left(\tilde{x}_{1}+x_{1 e}\right)\left(\tilde{x}_{2}+x_{2 e}\right)-\left(\tilde{x}_{2}+x_{2 e}\right)\left(\tilde{u}+u_{e}\right)  \tag{3.31}\\
\dot{\tilde{x}}_{2}+\dot{x}_{2 e}=\left(\tilde{x}_{1}+x_{1 e}\right)+\left(\tilde{x}_{2}+x_{2 e}\right) \\
\tilde{y}+y_{e}=3\left(\tilde{x}_{1}+x_{1 e}\right)+\left(\tilde{x}_{2}+x_{2 e}\right)+\left(\tilde{u}+u_{e}\right)
\end{array}\right.
$$

Knowing that at equilibrium $\dot{x}_{1 e}=\dot{x}_{2 e}=0$ and by neglecting the product of any two small variations and higher order terms, equation (3.31) can be reduced to:

$$
\left\{\begin{array}{l}
\dot{\tilde{x}}_{1}=-u_{e} \tilde{x}_{1}+u_{e} \tilde{u}  \tag{3.32}\\
\tilde{x}_{2}=\tilde{x}_{1}+\tilde{x}_{2} \\
\tilde{y}=3 \tilde{x}_{1}+\tilde{x}_{2}+\tilde{u}
\end{array}\right.
$$

which is the same as in (3.28) and (3.29)
The difference between the large-signal and the small-signal models are, that in the latter, the control input $u$ is not multiplied by any state from the vector $x$. This means that the model is linearized around operation point $u_{e}$. The small-signal model is useful as it allows power converters to be represented as a transfer function in the sdomain and frequency domain as:

$$
\begin{equation*}
H(s)=\frac{\tilde{Y}(s)}{\tilde{U}(s)}=C(s I-A)^{-1} B+D \tag{3.33}
\end{equation*}
$$

where $\tilde{Y}(s)$ and $\tilde{U}(s)$ are the Laplace transforms of the time-domain functions $\tilde{y}$ and $\tilde{u}$. For the system model in (3.28), the output can be represented as:

$$
\begin{equation*}
\tilde{Y}(s)=\frac{s^{2}+s\left(4 u_{e}-1\right)-3 u_{e}}{s^{2}+s\left(u_{e}-1\right)-u_{e}} . \tilde{U}(s) \tag{3.34}
\end{equation*}
$$

### 3.3.2.2 An Example

For the B1A converter and its configurations in Figure 3.9, the average small-signal model can be obtained from its large-signal model in the equation set (3.23). The converter state equations in (3.23) can be re-written as:

$$
\left\{\begin{array}{l}
\dot{I}_{L}=\underbrace{\underbrace{\frac{-(1-D)}{L} V_{c}+\frac{l}{L} V_{i n}}_{f_{2}}}_{f_{1}}  \tag{3.35}\\
\dot{V}_{c}=\underbrace{}_{\substack{(1-D) \\
C_{o} \\
L_{L}} \frac{1}{R C_{o}} V_{c}} \\
y=V_{c}
\end{array}\right.
$$

The equilibrium points of the states $I_{L}, V_{c}$ and the output $y$ at equilibrium input $D_{e}$ are calculated as $I_{L e}, V_{c e}$ and $y_{e}$ by setting the derivative terms in (3.29) to zero, yielding:

$$
\left\{\begin{array}{l}
V_{c e}=\frac{1}{1-D_{e}} V_{\text {in }}  \tag{3.36}\\
I_{L e}=\frac{V_{i n}}{R\left(1-D_{e}\right)^{2}} \\
y_{e}=\frac{1}{1-D_{e}} V_{i n}
\end{array}\right.
$$

Considering the input voltage $V_{i n}$ is constant, the small-signal matrices can be obtained from:

$$
\begin{align*}
& A=\left[\begin{array}{ll}
\frac{\partial f_{l}\left(I_{L}, V_{c}, D\right)}{\partial I_{L}} & \frac{\partial f_{l}\left(I_{L}, V_{c}, D\right)}{\partial V_{c}} \\
\frac{\partial f_{2}\left(I_{L}, V_{c}, D\right)}{\partial I_{L}} & \frac{\partial f_{2}\left(I_{L}, V_{c}, D\right)}{\partial V_{c}}
\end{array}\right]_{I_{L e}, V_{c e}, D_{e}}=\left[\begin{array}{cc}
0 & \frac{-\left(1-D_{e}\right)}{L} \\
\frac{\left(1-D_{e}\right)}{C_{o}} & \frac{-1}{R C_{o}}
\end{array}\right] \\
& B=\left[\begin{array}{c}
\frac{\partial f_{l}\left(I_{L}, V_{c}, D\right)}{\partial D} \\
\frac{\partial f_{2}\left(I_{L}, V_{c}, D\right)}{\partial D}
\end{array}\right]_{I_{L e}, V_{c e}, D_{e}}\left[\begin{array}{c}
\frac{V_{i n}}{\left(1-D_{e}\right) L} \\
\frac{-V_{i n}}{R C_{o}\left(1-D_{e}\right)^{2}}
\end{array}\right]  \tag{3.37}\\
& C=\left[\begin{array}{ll}
\frac{\partial h\left(I_{L}, V_{c}, D\right)}{\partial I_{L}} & \frac{\partial h\left(I_{L}, V_{c}, D\right)}{\partial V_{c}}
\end{array}\right]_{I_{e}, V_{c e}, D_{e}}=\left[\begin{array}{ll}
0 & 1
\end{array}\right]
\end{align*}
$$

Finally, the system equations are expressed in relation (3.38) where $\delta$ is the smallsignal deviation of the duty ratio $D$ where: $\delta=D-D_{e}$.

$$
\begin{align*}
& {\left[\begin{array}{c}
\dot{I}_{L} \\
\dot{V}_{c}
\end{array}\right]=\left[\begin{array}{cc}
0 & \frac{-\left(1-D_{e}\right)}{L} \\
\frac{\left(1-D_{e}\right)}{C_{o}} & \frac{-1}{R C_{o}}
\end{array}\right]\left[\begin{array}{c}
\tilde{I}_{L} \\
\tilde{V}_{c}
\end{array}\right]+\left[\begin{array}{c}
\frac{V_{i n}}{\left(1-D_{e}\right) L} \\
\frac{-V_{i n}}{R C_{o}\left(1-D_{e}\right)^{2}}
\end{array}\right][\delta]}  \tag{3.38}\\
& {[\tilde{y}]=\left[\begin{array}{ll}
0 & 1
\end{array}\right]\left[\begin{array}{c}
\tilde{I}_{L} \\
V_{c}
\end{array}\right]}
\end{align*}
$$

The transfer function between the small-signal duty ratio $\delta$ and output voltage $\tilde{V}_{c}$ is calculated from relations (3.33) and (3.38) as:

$$
\begin{gather*}
G(s)=\frac{\tilde{V}_{c}(s)}{\delta(s)}=\frac{V_{i n}(R M-L s)}{M\left(C_{o} L R s^{2}+L s+R M\right)}  \tag{3.39}\\
\text { where } M=\left(D_{e}^{2}-2 D_{e}+1\right)
\end{gather*}
$$

The transfer function in equation (3.39) is suitable for linear control strategies as it facilitates ready plotting of classical frequency domain Bode plots and root locus. Figure 3.13 shows the Bode plots of the B 1 A converter with various duty ratios, while Figure 3.14 shows the converter's root-locus. For validation of the presented mathematical analysis, the response of transfer function $\mathrm{G}(\mathrm{s})$ in (3.39) is compared with the converter switched model at different duty ratios. To a certain extent, the small-signal transfer functions give good prediction of the converter's behaviour. For
example, the Bode plots in Figure 3.13 show that the converter's bandwidth (the point where the magnitude is $-3 \mathrm{db}[\mathrm{dB}]$ ), increases with duty ratio.


Figure 3.13 Bode plots for different operating points of BT1A converter.


Figure 3.14. Root-locus for different operating points of BT1A converter.

Moreover, the root-locus in Figure 3.14 shows high damping of the poles (closer to the real-axis) with increasing duty ratio. This means less overshoot with higher duty ratio values, which can also be viewed in Figure 3.15.

### 3.3.2.3 Operation with Time-varying Duty Ratio

In several applications, power electronic circuits operate with time-variant duty ratios (cycles). Because most power converters are non-linear systems, their input-to-output transfer functions tend to depend on the operating point. Equation (3.39) shows the transfer function of the B1A converter depends on its equilibrium duty ratio. To explain this, consider converter B1A that has its output voltage $y=V_{c}$ which consists of two components, a DC component $V_{d c}$ and an AC component with magnitude $V_{m}$ and fundamental frequency $\omega$.

(a) $D_{e}=0.3$

(c) $D_{e}=0.5$

(b) $D_{e}=0.4$

(d) $D_{e}=0.6$

(e) $D_{e}=0.7$

Figure 3.15. Comparison between the exact model ( - ) and small-signal model ( .... ). The reference output voltage $V_{c}^{\text {ref }}$ can be expressed as:

$$
\begin{equation*}
V_{c}^{r e f}=V_{d c}+V_{m} \sin \omega t \tag{3.40}
\end{equation*}
$$

Recall the steady-state converter ratio transfer function of the B1A in equation (2.5); the duty ratio can be expressed as:

$$
\begin{align*}
& V_{c}^{\text {ref }}=\frac{1}{1-D} V_{\text {in }} \\
& 1-D=\frac{V_{\text {in }}}{V_{c}^{r e f}}  \tag{3.41}\\
& D=1-\frac{V_{\text {in }}}{V_{c}^{r e f}}=1-\frac{V_{\text {in }}}{V_{d c}+V_{m} \sin (\omega t)}
\end{align*}
$$

However, depending on the converter's steady-state transfer function, the reference and actual output voltages of the converter may deviate as shown in Figure 3.16. The
root-locus in Figure 3.14 shows the converter dynamics vary with duty ratio; thus, as do the locations of the open and closed loop poles. This means that the transition between any two successive points on the $V_{c}$ waveform depends on the instantaneous operating point. This can be understood from the fact that: a part of the energy absorbed from the sources is stored in the passive elements.


Figure 3.16. B1A with time-varying duty ratio: $V_{c}(-), V_{c}^{\text {ref }}(\ldots .$.$) and V_{i n}=100 \mathrm{~V}$.
The value of this energy is directly proportional to the passive element values. For further illustration of this concept, two different passive element combinations, viz., $L=1 \mathrm{mH}$ and $C_{o}=10 \mu \mathrm{~F}$, and $L=2.5 \mathrm{mH}$ and $C_{o}=150 \mu \mathrm{~F}$, are used in B1A converter. The root-locus plots for each set are shown in Figure 3.17. The small passive elements have poles with higher frequencies with larger passive elements both are distant from the fundamental frequency 50 Hz . This means that small passive elements charge and discharge faster at all duty cycles (ratios); thus resulting in lower in the output voltage $V_{c}$ distortion. This is verified from the converter waveforms depicted in Figure 3.18 where the increased passive element energy storage leads to more output voltage and current deviation from the desired values.


Figure 3.17. Root-locus of B1A with two passive element set: (a) $L=1 \mathrm{mH}, C_{o}=10$ $\mu \mathrm{F}$ and (b) $L=2.5 \mathrm{mH}$ and $C_{o}=150 \mu \mathrm{~F}$.


Figure 3.18. Matlab simulations of B1A switched (exact) models with two passive element set: (a) $L=1 \mathrm{mH}, C_{o}=10 \mu \mathrm{~F}$ and (b) $L=2.5 \mathrm{mH}$ and $C_{o}=150 \mu \mathrm{~F}$. $V_{c}(-)$,

Figure 3.18 b shows that the deviation from the desired settling point is exacerbated at higher duty ratios, where the poles correspond with lower frequencies (Figure 3.17b). This situation physically occurs when the stored energy in the converter is high.

### 3.4 Advantages and Limitations of the Averaged Model

Average models are useful for digital control design as they can be transformed into discrete-time averaged models [3.8]. Also, the averaged models provide good converter approximation when the state variables vary within a narrow range. Generally, power converter models are used for:

- control design;
- study of system behaviour using time and frequency domain simulations; and
- Sizing (optimization of passive elements), taking into account their dynamic performance.

Figure 3.19 describes the relations between control strategies, which will be discussed in the next sections, and models types.


Figure 3.19. Relations between models and control laws

### 3.5 Control Objectives in Power Electronic Converters

Generally, power converter operation requires a proper control system for accomplishing specific operational objectives as well as satisfying safety conditions. The control strategy may vary according to the specific role of the converter. For example, a power electronic converter working in a DC-DC mode, feeding variable loads, requires a proper controller for the duty ratio to maintain a constant output voltage. For DC-AC operation of grid-connected converters, the controller is required to provide sinusoidal output current with a specific magnitude, frequency, and phase-shift angle. Figure 3.20 shows a generic control system for power electronic converters. The power converter controller task is to provide an efficient, stable and high-performance power transfer from the input to output ports.


Figure 3.20 Generic controller for power electronic converters.

The major difference between linear control techniques and variable-structure control (VSC), such as sliding mode control (SMC), is that the linear controllers provide the averaged duty ratio which is required to be modulated, while VSC provides modulated control signals $u$ directly to the converter [3.11].

### 3.5.1 Control Issues Related to Power Converters

Generally, power electronic converters are variable-structure systems operating with fast dynamics [3.12]. Consequently, in order to provide high power quality, the control systems should have high bandwidth and a fast time response. Moreover, robust and stable operation of power converters requires high gain and phase margins to make the controller resilient as the system gain changes with duty cycles, as expected in typical nonlinear systems. For digital implementation of controllers on a
digital signal processor (DSP), the controller must operate with a low computing time and high sampling frequencies ( $1-100 \mathrm{kHz}$ ). Usually, a power electronic converter controller regulates the output voltage or current, softens the converter's variable dynamics, and constrains variables to acceptable values. Typically, integral control loops are required for power electronic converters to provide zero steadystate error of the controlled quantities. In general, the control system is concerned with the low-frequency behaviour of the power converter [3.8]. Consequently, the converter average model becomes an important tool for control design, where the frequency range of interest is much less than the switching frequency. Power converter controllers can be classified into constant-switching-frequency and variable-switching-frequency controllers [3.2]. As stated, power electronic converter models are expressed using coupled voltage and current sources which are controlled with the converter duty ratio as a common control input. The multiplication of two states of the converter variables or multiplication of any variable and the control input introduce nonlinearities into the models [3.8]. This nonlinearity means that the converter dynamic behaviour becomes dependent on the duty ratio [3.8]. There are many current and voltage controllers for power converters in the literature [3.13, 1416]; however, two major controller types will be discussed and used in this thesis. The first is the linear controller that employs classical proportional-integral (PI) control or proportional-integral-derivative (PID) control. The gains of these standard controllers are constant; hence their transfer functions do not change with time. These controllers require a duty cycle modulation stage such as pulse width modulation (PWM) or a sigma-delta modulator [3.8]. The second type is a sliding mode controller where the non-linear nature of the power converter is considered in the control system, where signal modulators are not necessary [3.17].

### 3.5.2 Linear Controllers for Power Converters

Usually, a linear controller is used for power electronic converters operating in a continuous-conduction mode [3.18]. It controls the converter averaged lowfrequency variables using feedback control. As explained in Section 3.3.2, the averaged small-signal models offer good behaviour prediction of the converter under investigation. The main disadvantage of this approach is the fact that the controlled systems are naturally non-linear and linearized around an operating point [3.9]. For
this reason, non-linear systems with linear controllers may suffer from stability problems if the control design does account for the potential impact of converter nonlinearity [3.9]. Although the control objectives vary according to the converter application, the objectives generally include tracking a reference voltage and/or current waveforms. Often, these objectives include the converter's desired dynamics, safety regulations, internal variable limitations and ranges. For second order power electronic converters, or those that have second-order dominant poles, classical time-domain analysis is useful in the control process [3.2]. In addition, socalled loop shaping techniques are useful when the converter's stability is the matter of interest. Pole-placement techniques are used when the converter's closed-loop poles are required to be driven to specific locations to achieve a certain behaviour and dynamics [3.2].

### 3.5.2.1 PI (Proportional-Integral) Controller

The transfer function of the PI controller is shown in equation (3.42) [3.19]. The existence of a pole at zero rad/s (dc quantities) provides an infinite gain as shown in Figure 3.21. Consequently, as the product of zero and infinity can be a finite quantity, the PI controller transfer function can have zero input and finite output. For this reason, the PI controller is placed between the error signal and the power converter, as shown in Figure 3.22, to force the error signal to zero while the duty ratio has a finite non-zero value [3.19]. In this way, the controlled dc output tracks the reference exactly.

$$
\begin{equation*}
G_{p i}=K_{p}+\frac{K_{i}}{s} \tag{3.42}
\end{equation*}
$$

where $K_{p}$ and $K_{i}$ are the proportional and integral gains of the controller
For the B1A converter with the small-signal transfer function in equation (3.39), the open-loop transfer function of the overall system can be expressed by the product of $G_{p i}(s)$ and $G(s)$. From Figure 3.21, the PI controller introduces a $-90^{\circ}$ phase shift into the frequency domain Bode plot at dc quantities. This affects system stability and hence, the control design must ensure that the system is not driven into the unstable region.


Figure 3.21 PI controller Bode plots.


Figure 3.22 A simple PI controlled system.

Figure 3.23 shows the Bode plots for transfer functions of the controller and the converter, as well as their product. Some beneficial information can be obtained from these plots. The first is that the system is stable. This is because, for the total transfer function ( $G . G_{p i}$ ), the phase shift is $+90^{\circ}$ when the magnitude is $0[\mathrm{~dB}]$, which is far from the stability limit of $-180^{\circ}$. The second is that the system is fast as it has a relatively large bandwidth. The third fact is that certain resonance oscillations are expected at the magnitude plot peak, which corresponds 200 Hz . The resonance frequency and time will be denoted as $f_{\text {res }}$ and $t_{\text {res }}$. The MATLAB ${ }^{\circledR}$-Simulink ${ }^{\circledR}$ simulations in Figure 3.24 verify the initial guess. However the controller gains are selected arbitrary and gave acceptable performance; the control design procedures become more difficult for more complicated power converters than B1A.


Figure 3.23 Bode plots of control system for converter B1A.


Figure 3.24 Simulation of PI controlled B1A converter.
$L=1 \mathrm{mH}, C_{o}=150 \mu \mathrm{~F}, V_{i n}=100 \mathrm{~V}$, Reference for $V_{c}=200 \mathrm{~V}, R=20, K_{p}=1$ and $K_{i}=$

### 3.5.2.2 PR (Proportional-Resonant) Controller

If the power electronic converter is required to operate in an AC mode or $\mathrm{AC}+\mathrm{DC}$ mode, control of the sinusoidal current and voltage waveforms becomes necessary. There are two options for the control designer. The first is to use the explained PI control but after transforming all the waveforms from the stationary frame to the $d q$ synchronous frame where all the waveforms are viewed as dc values and consequently, the PI controller can be used, and another $d q$ to stationary frame transformation is applied. The second option is to use PR control [3.20]. The resonant part of the controller provides infinite gain at any desired frequency $\omega_{o}$ which is tuned at the frequency of interest and hence, selected waveforms can be controlled with zero steady-state error. No transformation between the different frames is necessary. The transfer functions of the PR controller is expressed as [3.20]:

$$
\begin{gather*}
G_{p r}=K_{p}+\frac{K_{r} s}{s^{2}+\omega_{o}^{2}}  \tag{3.43a}\\
G_{p r}=K_{p}+\frac{K_{r} s}{s^{2}+k_{b} s+\omega_{o}^{2}} \tag{3.43b}
\end{gather*}
$$

where $K_{p}$ and $K_{r}$ are the proportional and resonant gains of the controller.
The Bode plots of the PR controllers in equation (3.43a) are shown in Figure 3.25. Increasing $K_{p}$ shifts the magnitude plot up, increasing the bandwidth of the controlled system and reducing the settling time. But increasing $K_{r}$ increases the amplification band around $\omega_{o}$ which is beneficial for systems with a slightly changing frequency (like the frequency of a real grid voltage). For the non-ideal PR controller in equation (3.43a), the constant $K_{b}$ introduces a wider band where the controller gives its high gain. This band is beneficial when the controlled waveform frequency changes slightly around certain point. As an example of PR controlled converters, the conventional single-phase DC/AC voltage source inverter (VSI), shown in Figure 3.26, can be modelled as two b1A bidirectional converters shown in Figure 2.3b. A bidirectional converter is obtained by inserting anti-parallel diode and switch pairs. From the previous discussion, the small-signal model of this DC/AC converter can be written as:

$$
\begin{align*}
& {\left[\begin{array}{c}
\dot{I_{L}} \\
\dot{\hat{V}_{c}}
\end{array}\right]=\left[\begin{array}{cc}
0 & \frac{-1}{L} \\
\frac{1}{C_{o}} & \frac{-1}{R C_{o}}
\end{array}\right]\left[\begin{array}{c}
\tilde{I}_{L} \\
\tilde{V_{c}}
\end{array}\right]+\left[\begin{array}{c}
\frac{V_{i n}}{L} \\
0
\end{array}\right][\delta]}  \tag{3.44}\\
& {[\tilde{y}]=\left[\begin{array}{ll}
0 & 1
\end{array}\right]\left[\begin{array}{c}
\tilde{I}_{L} \\
\tilde{V_{c}}
\end{array}\right]}
\end{align*}
$$


(a) Ideal

(b) Non-ideal

Figure 3.25 PR controller Bode plots.


Figure 3.26. Single-phase DC/AC converter consisting of two bidirectional b1A

Then, the transfer function between the duty ratio function (usually called the modulating signal in AC systems) and the output voltage can be expressed as:

$$
\begin{equation*}
G(s)=\frac{\tilde{y}(s)}{\delta(s)}=\frac{\tilde{V}_{c}(s)}{\delta(s)}=\frac{V_{i n}}{C_{o} L s^{2}+L / R s+1} \tag{3.45}
\end{equation*}
$$

The closed-loop control system is shown in Figure 3.27. A typical DC/AC converter with $L=10 \mathrm{mH} C_{o}=50 \mu \mathrm{~F}, R=10 \Omega$ and $V_{i n}=100 \mathrm{~V}$ is studied. The ideal PR controller values are selected as $K_{p}=1$ and $K_{r}=10$ to give a phase margin of $90^{\circ}$ and more than 1 kHz bandwidth. The Bode plots of the transfer functions $G_{p r}, G$ and their product are shown in Figure 3.28. The controlled system appears to have fast dynamics, because it has a relatively large bandwidth. The simulations results of this system are shown in Figure 3.29 where the controller is able to reach $97.5 \%$ of the reference in one fundamental cycle.


Figure 3.27. Block diagram of PR controlled DC/AC converter in Figure 3.25.

The converter in Figure 3.26 is considered as a simple system from the control complexity viewpoint. This comes from the fact that it is a second-order single-stage system with a linear transfer function. However, in more complex DC/AC converters with high-order output filters, additional loops maybe necessary to obtain good converter performance in terms of stability, dynamics and disturbance rejection.


Figure 3.28 Open-loop Bode plots of PR controlled system in Figure 3.26

(a) $V_{o}(-), V_{o}^{\text {ref }}(\ldots$.

(b) E

(c) $\delta$

Figure 3.29. Simulations of PR controlled single-phase VSI: (a) reference and actual voltages, (b) Error signal, and (c) duty ratio.

### 3.5.3 Non-linear Controllers

As explained, power electronic converters are non-linear variable structure systems where their topology changes between numerous configurations. The non-linear behaviour increases with the high orders. Non-linear controllers provide control laws which can vary through the control process according to the sliding functions of
system's internal state variables [3.9]. This feature may be beneficial for non-linear high-order power converters as their poles change continuously with time and duty ratio [3.9]. Sliding mode control (SMC) is a non-linear control method and is used extensively in power converter applications [3.21]. The SMC is attractive for lower rated power converters for several reasons. Such power converters operate with high switching frequency to reduce the variables limits and this imposes limitations on the controller computational time [3.21]. The SMC computational time is less than the required time for linear control techniques [3.22]. Another reason is that SMC accounts for converter moving poles and can reduce the problems of their nonlinearity [3.17]. This guarantees satisfactory stability boundaries and robustness against large variations of the converter's internal state variables and external disturbances. SMC uses a discontinuous function as a control input to force specific internal state variables to move on a specific plan, called the sliding surface $S(x)$, throughout a defined duration. The existence of a control function that can maintain the state variables on the sliding surface is determined by fulfilling the existence condition [3.17]. The existence condition is verified by applying Lyaponov's theory, which can be briefed stated as follows: "If there is a positive definite function $V=$ $f(S)$, and its derivative is negative definite or semi definite $\frac{d V}{d t}<0$, then there is a discontinuous function $u(x)$ which can drive the states $x$ on the surface $S(x)=0$ ". To give an intuitive example of SMC, the B1A converter in Figure 3.9 is studied. If it is required to control the inductor current $I_{L}$, the sliding surface can be identified as [3.9]:

$$
\begin{equation*}
S(x)=I_{L}^{*}-I_{L} \tag{3.46}
\end{equation*}
$$

If the Lyaponov's function is selected as $V=\frac{1}{2} S^{2}(x)$, the existence condition for the sliding surface is established if the switching function $u(x)$ is identified as:

$$
u(x)= \begin{cases}1 & S(x)>0  \tag{3.47}\\ 0 & S(x)<0\end{cases}
$$

Figure 3.30 shows simulations for the SM-controlled B1A converter. However, for many applications, control the output voltage $V_{c}$ (or current $I_{o}$ ) is required rather than the input inductor current $I_{L}$. Unfortunately, any function $V(x)$ does not fulfil the existence condition if the sliding surface is chosen as $S(x)=V_{c}{ }^{*}-V_{c}$.

(a)

(c) $I_{L}(-), I_{L}{ }^{*}(\ldots)$

(b)

Figure 3.30 Simulations of B1A with SMC. (a) SMC block diagram, (b) sliding surface $S(x)$ and (c) input current reference and actual values.


Figure 3.31 Simulations of B1A with SMC. (a) SMC block diagram, (b) sliding surface $S(x)$ and (c) input current reference and actual values.

This can be predicted as the switch $S_{l}$ can directly control $I_{L}$ while it has no direct control on $V_{c}$. For this reason, if output voltage $V_{c}$ control is desired, it must be
achieved as an indirect function of $I_{L}$ as shown in Figure 3.31a, 3.31b and 3.31c show the simulation results for the B1A converter with indirectly SMC.

### 3.6 Summary

Generally, power electronic converters are nonlinear time-variant systems. This system nonlinearity makes for complex control design. The modelling process is an important stage before the control design procedures. Several methodologies for modelling power converters can be applied depending on the different control techniques. These control techniques tend to have a similar objective: to achieve lowfrequency power electronic converter performance. The complexity of this objective depends on the structure and order of the converter. Averaged models describe the converter behaviour along specified switching periods. The main drawback of averaged models is that the converter's duty ratio does not appear explicitly in the transfer function, and hence, classical control strategies, such as proportional-integral (PI) or proportional-resonant (PR) control, cannot be implemented directly. Smallsignal linearized averaged models can be used to ease the use of classical controllers. However, these models are accurate within a specified band of operation. Unlike classical controllers, sliding mode control can deal with the instantaneous converter voltages and currents and can reduce the effect of converter non-linear behaviour. This chapter presented the modelling procedures to obtain exact models (suitable for sliding mode control) and averaged models (suitable for classical control strategies) and introduced the main converters control methodologies and defines the main control challenges. In the following chapters, proper models and controllers will be selected for each converter according to its topological nature and desired operation.

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## Chapter 4

## DC/DC and DC/AC Converters with Continuous Input Current

Universally, there is increasing tendency to reduce costs and improve efficiency of energy conversion systems through modular structured renewable/distributed systems [4.1-4.5]. Therefore, the need for small converters that use small passive components becomes increasingly important. Moreover, the cost of renewable energy systems is affected considerably by installation and maintenance costs [4.64.8] Inverter initial and running costs are estimated to be about half of the PV system initial cost [4.9]. Most dc-ac converters installed in renewable energy systems require large input and/or output filtering capacitance, typically, of electrolytic type. Replacing this electrolytic capacitor with a plastic type increases reliability significantly, by at least thirty times, for the same capacitance and operating voltage [4.9]. At rated operating conditions, the lifetime of this filter capacitor is short compared with the other inverter components [4.10]. Thus, this capacitor is a barrier for increasing overall system reliability. Capacitor lifetime is halved for every $10^{\circ} \mathrm{C}$ increase in the operating temperature [4.10]. Modern low-cost renewable energy applications need galvanic isolation; hence, high-frequency-link (HFL) converters are promising possibilities [4.11-4.13]. This chapter classifies and proposes the possible configurations of continuous-input dc-dc and dc-ac converters, which do not require installation of a large and unreliable electrolytic capacitor. In addition, it discusses the ability of these converters to be isolated with HFL transformers in an attempt to improve switching device utilization and for safety reasons.

### 4.1 Buck Converters

The traditional full bridge single-phase buck dc-ac converter is shown in Figure 3.26. Although this inverter type cannot produce an output voltage greater than the input voltage, its control design is simple and well-studied for a range of renewable energy applications. This inverter can be viewed as two b1A converters, as shown in Figure 2.3b. The average voltage and current stresses are equal to the input voltage and output current respectively, which are less than boost and buck-boost types; hence, better efficiency can be obtained. However, a step-up line frequency transformer
maybe required for some applications, and this may increase the overall system cost and reduce the efficiency. From Table 2.1 in Chapter 2, it was established that there are four buck converters that have the property of providing continuous input current; therefore, do not need large input electrolytic capacitors. These converters are $\mathrm{b} 1 \mathrm{C}, \mathrm{b} 1 \mathrm{D}, \mathrm{b} 2 \mathrm{D}$, and b 2 F . The modelling and performance of the resultant $\mathrm{dc} / \mathrm{dc}$, single-phase dc/ac and three-phase dc/ac converters will be presented and compared.

### 4.1.1 b1C

b1C dc/dc converter is shown in Figure 2.8a. Practically, the inductors $L_{1}$ and $L_{2}$ have equivalent resistances which can be considered as series resistances as shown in Figure 4.1. As concluded in Chapter 2, b1C has both continuous input and output currents. Therefore, the shunt output capacitor $C_{o}$ is optional. For this reason $C_{o}$ results in a L.H.S pole which is relatively far from the other three poles of $L_{1}, L_{2}$ and $C$ and hence, it is acceptable to be eliminated from the state-space models and the converter can be considered as three-order system for simplification.


Figure 4.1. Two configurations of b1C converter: (a) $t_{o n}$ and (b) $t_{o f f}$
As explained in Chapter 3, the averaged large-signal and model of b1C converter can be expressed as:

$$
\left[\begin{array}{l}
\dot{I}_{L 1}  \tag{4.1}\\
\dot{V}_{c} \\
\dot{I}_{L 2}
\end{array}\right]=\left[\begin{array}{ccc}
\frac{-\left(R+r_{1}\right)}{L_{l}} & -\frac{(1-D)}{L_{l}} & -\frac{R}{L_{1}} \\
\frac{(1-D)}{C} & 0 & \frac{-D}{C} \\
-\frac{R}{L_{2}} & \frac{D}{L_{2}} & \frac{-\left(R+r_{2}\right)}{L_{2}}
\end{array}\right]\left[\begin{array}{l}
I_{L 1} \\
V_{c} \\
I_{L 2}
\end{array}\right]+\left[\begin{array}{l}
\frac{1}{L_{l}} \\
0 \\
0
\end{array}\right]\left[V_{i n}\right]
$$

If the input voltage $V_{i n}$ is considered to be constant for a long period, the small-signal model can be expressed as:

$$
\left[\begin{array}{c}
\dot{\tilde{I}}_{L 1}  \tag{4.2}\\
\dot{\dot{V}_{c}} \\
\dot{\tilde{I}}_{L 2}
\end{array}\right]=\left[\begin{array}{ccc}
\frac{-\left(R+r_{1}\right)}{L_{l}} & -\frac{\left(1-D_{e}\right)}{L_{l}} & -\frac{R}{L_{l}} \\
\frac{\left(1-D_{e}\right)}{C} & 0 & \frac{-D_{e}}{C} \\
-\frac{R}{L_{2}} & \frac{D_{e}}{L_{2}} & \frac{-\left(R+r_{2}\right)}{L_{2}}
\end{array}\right]\left[\begin{array}{c}
\tilde{I}_{L 1} \\
\tilde{V_{c}} \\
\tilde{I}_{L 2}
\end{array}\right]+\left[\begin{array}{c}
\frac{V_{i n}}{L_{1}} \\
\frac{D_{e} V_{i n}}{R C} \\
\frac{V_{i n}}{L_{2}}
\end{array}\right][\delta]
$$

The transfer function between $V_{o}$ and $\delta$ can be expressed as:

$$
\begin{align*}
& \quad G(s)=\frac{\tilde{V_{o}}(s)}{\delta(s)}=\frac{a_{2} s^{2}+a_{1} s+a_{0}}{b_{3} s^{3}+b_{2} s^{2}+b_{1} s+b_{0}} \\
& a_{2}=R C V_{i n}\left(L_{1}+L_{2}\right) \\
& a_{1}=V_{i n}\left(D_{e} L_{2}-D_{e}^{2}\left(L_{1}+L_{2}\right)+C R\left(r_{1}+r_{2}\right)\right) \\
& a_{0}=V_{i n}\left(D_{e} r_{2}-D_{e}^{2}\left(r_{1}+r_{2}\right)+R\right)  \tag{4.3}\\
& b_{3}=C L_{1} L_{2} \\
& b_{2}=C R\left(L_{1}+L_{2}\right)+C\left(L_{1} r_{2}+L_{2} r_{1}\right) \\
& b_{1}=L_{2}+D_{e}{ }^{2}\left(L_{1}+L_{2}\right)-2 D_{e} L_{2}+C\left(R\left(r_{1}+r_{2}\right)+r_{1} r_{2}\right) \\
& b_{0}=R+r_{2}-2 D_{e} r_{2}+D_{e}^{2}\left(r_{1}+r_{2}\right)
\end{align*}
$$

## a) $d c / d c$ mode

A PI controlled system similar to that in Figure 3.22 is used to examine the operation of the converter b1C in the dc/dc mode in Figure $4.2\left(V_{\text {in }}=200 \mathrm{~V}, L_{l}=L_{2}=1 \mathrm{mH}, \mathrm{C}\right.$ $=50 \mu \mathrm{~F}, f_{s}=30 \mathrm{kHz}$ and $\mathrm{R}=22 \Omega$ ). The capacitor voltage $V_{c}$ always equals $V_{i n}$. Figure 4.2 b shows the continuous input current at $D=0.8$. In Figure 4.2c, a square wave reference voltage is chosen to show controller response.

## b) dc/ac single-phase inverter

Two b1C converters can be connected to form a single-phase dc/ac inverter as shown in Figure 4.3. For dc/ac operation, the converters should support bidirectional power flow by using switch - antiparallel diode pairs. The PR controller is a candidate to control the single-phase ac inverter in Figure 4.3 as it can directly control the output voltage $V_{o}$ or current $I_{o}$, without the need for additional transformations. The control system is shown in Figure 3.27 with arbitrary selected controller gain values. Figure 4.4 shows single-phase inverter operation when controlled to give $V_{o}=80 \sin \omega t$.

## a) dc/ac three-phase inverter

The three-phase buck inverter based on the bidirectional b1C converter is shown in Figure 4.5. The two possible linear controllers are shown in Figure 4.6. In the first, the output three-phase voltage (or current) is transformed to the rotating synchronous
frame. Then, the dc values (dqo) are controlled by PI controllers. In the second method, the three-phase output quantities are directly negative fed-back to three PR controllers. The experimental operation of the b1C three-phase inverter is shown in Figure 4.7 when controlled by the PR controllers.


Figure 4.2. Performance of b1C in dc/dc mode at $V_{i n}=200 \mathrm{~V}$ : (a) $V_{c}$ at $\mathrm{D}=0.8$, (b) $I_{\text {in }}$ at $\mathrm{D}=0.8$, (c) Output voltage $V_{o}$ when controlled with PI controller to follow a square wave reference voltage in ( $K_{p}=0.1$ and $K_{i}=0.5$ ) and (d) Bode plot at $\mathrm{D}=$


Figure 4.3. Single-phase dc/ac inverter using two b1C converters.


Figure 4.4. Performance of closed loop PR controlled b1C in dc/ac mode at $V_{i n}=$ 200 V and $V_{o}^{\text {ref }}=160 \sin \omega t$ : (a) $I_{L l}-I_{L 2}$, (b) $V_{c l}-V_{c 2}$, (c) Output voltage $V_{o}$ and (d) Bode plot at ( $K_{p}=0.1$ and $K_{r}=0.5$ ).

### 4.1.2 b1D

The second converter with continuous input current is the b1D converter, which is shown in Figure 2.14a. As with the b1C, b1D has both continuous input and output currents and shunt output capacitor $C_{o}$ is also optional. Figure 4.8 shows the two operational modes of the b1D converter.

The large-signal and small-signal average models can be expressed as in equations (4.4) and (4.5) respectively. The transfer function between the output voltage $V_{o}$ and the input voltage $V_{\text {in }}$ is shown in equation set (4.6).

## a) dc/dc mode

A PI controlled system similar to that in Figure 3.22 is used to show the operation of the converter b1D in the dc/dc mode in Figure $4.9\left(V_{\text {in }}=200 \mathrm{~V}, L_{1}=L_{2}=1 \mathrm{mH}, \mathrm{C}=\right.$ $50 \mu \mathrm{~F}, f_{s}=30 \mathrm{kHz}$ and $\mathrm{R}=22 \Omega$ ). Figure 4.9 b shows the continuous input current at $D=0.8$. In Figure 4.9 c , a square wave reference voltage shows the response of the controller.


Figure 4.5. Three-phase buck inverter based on b1C.

In comparison with b1C in a dc/dc mode, the output high-frequency ripple is expected to be lower in b1D as shown in Figures 2.9c and 2.14c. Moreover, the input current ripple depends inversely on $L_{1}$ in b1C while depend inversely on $L_{2}$ in b1D.

(a)

(b)

Figure 4.6. Possible linear controllers for three-phase inverter.

$$
\begin{align*}
& {\left[\begin{array}{c}
\dot{I}_{L 1} \\
\dot{V_{c}} \\
\dot{I}_{L 2}
\end{array}\right]=\left[\begin{array}{ccc}
\frac{-r_{1}}{L_{1}} & \frac{1}{L_{1}} & 0 \\
\frac{-1}{C} & 0 & \frac{1-D}{C} \\
0 & \frac{-(1-D)}{L_{2}} & \frac{-\left(R+r_{2}\right)}{L_{2}}
\end{array}\right]\left[\begin{array}{l}
I_{L 1} \\
V_{c} \\
I_{L 2}
\end{array}\right]+\left[\begin{array}{c}
-\frac{1}{L_{l}} \\
0 \\
\frac{1}{L_{2}}
\end{array}\right]\left[V_{i n}\right]}  \tag{4.4}\\
& {\left[\begin{array}{l}
\dot{I}_{L 1} \\
\dot{\hat{V}_{c}} \\
\dot{\tilde{I}_{L 2}}
\end{array}\right]=\left[\begin{array}{ccc}
\frac{-r_{1}}{L_{1}} & \frac{1}{L_{1}} & 0 \\
\frac{-1}{C} & 0 & \frac{\left(1-D_{e}\right)}{C} \\
0 & \frac{-\left(1-D_{e}\right)}{L_{2}} & \frac{-\left(R+r_{2}\right)}{L_{2}}
\end{array}\right]\left[\begin{array}{c}
\tilde{I}_{L 1} \\
\tilde{V_{c}} \\
\tilde{I}_{L 2}
\end{array}\right]+\left[\begin{array}{c}
0 \\
\frac{D_{e} V_{i n}}{R C} \\
\frac{V_{i n}}{L_{2}}
\end{array}\right][\delta]} \tag{4.5}
\end{align*}
$$



$40 \mathrm{~V} / \mathrm{div}-5 \mathrm{~ms} / \mathrm{div}$
(c)

Figure 4.7 Performance of closed loop PR controlled three-phase b1C in dc/ac mode at $\mathrm{V}_{\mathrm{in}}=200 \mathrm{~V}$ and $V_{o}^{\text {ref }}=80 \sin \omega t$ : (a) $\mathrm{I}_{\mathrm{in}}$, (b) $\mathrm{V}_{\mathrm{ca}}-\mathrm{V}_{\mathrm{cb}}-\mathrm{V}_{\mathrm{cc}}$ and (c) three-phase Output voltage $\mathrm{V}_{\mathrm{o}}$.


Figure 4.8. Two configurations of b1D converter: (a) $t_{o n}$ and (b) $t_{o f f}$

$$
\begin{align*}
& \quad G(s)=\frac{\tilde{V_{o}}(s)}{\delta(s)}=\frac{a_{2} s^{2}+a_{l} s+a_{0}}{b_{3} s^{3}+b_{2} s^{2}+b_{1} s+b_{0}} \\
& a_{2}=R C L_{l} V_{i n} \\
& a_{1}=V_{i n}\left(D_{e} L_{l}-D^{2}{ }_{e} L_{l}+C R r_{l}\right) \\
& a_{0}=V_{i n}\left(D_{e} r_{l}-D_{e}^{2}{ }_{e} r_{l}+R\right)  \tag{4.6}\\
& b_{3}=C L_{l} L_{2} \\
& b_{2}=C\left(R L_{l}+L_{l} r_{2}+L_{2} r_{l}\right) \\
& b_{1}=\left(L_{l}+L_{2}\right)+D_{e}^{2} L_{l}-2 D_{e} L_{l}+C\left(R r_{1}+r_{1} r_{2}\right) \\
& b_{0}=\left(R+r_{1}+r_{2}\right)-2 D_{e} r_{1}+D_{e}^{2} r_{l}
\end{align*}
$$

## b) dc/ac single-phase inverter

Two bidirectional b1D converters are connected to form a single-phase dc/ac inverter as shown in Figure 4.10. In Figure 4.11, the resultant single-phase inverter is controlled with a PR controller to produced sinusoidal output voltage.


Figure 4.9. Performance of b1D in dc/dc mode at $V_{i n}=200 \mathrm{~V}$ : (a) $V_{c}$ at $\mathrm{D}=0.8$, (b) $I_{i n}$ at $\mathrm{D}=0.8$, (c) output voltage $V_{o}$ when controlled with PI controller to follow a square wave reference voltage in ( $K_{p}=0.1$ and $K_{i}=0.5$ ) and (d) Bode plot at $\mathrm{D}=$


Figure 4.10. Single-phase dc/ac inverter using two b1D converters.


Figure 4.11. Performance of closed loop PR controlled single-phase b1D inverter at $V_{i n}=200 \mathrm{~V}$ and $V_{o}^{\text {ref }}=160 \sin \omega t$ : (a) $I_{L l}-I_{L 2}$, (b) $V_{c l}-V_{c 2}$, (c) output voltage $V_{o}$ and (d) Bode plot at ( $K_{p}=0.1$ and $K_{r}=0.5$ ).

## c) dc/ac three-phase inverter

The three-phase buck inverter based on bidirectional b1D converter is shown in Figure 4.12. The experimental operation of the b1D three-phase inverter is shown in Figure 4.13 when controlled by the PR controllers.


Figure 4.12. Three-phase buck inverter based on b1D.


Figure 4.13 Performance of closed loop PR controlled three-phase b1D inverter at $V_{\text {in }}$ $=200 \mathrm{~V}$ and $V_{o}^{\text {ref }}=80 \sin \omega t$ : (a) $I_{i n}$, (b) $V_{c a}-V_{c b}-V_{c c}$; and (c) three-phase output voltage $V_{o}$

### 4.1.3 b2D

The b2D converter is shown in Figure 2.14b with both continuous input and output currents. Figure 4.14 shows the two operational modes of the b2D converter while the large-signal and small-signal models are in equations sets (4.7), (4.8) and (4.9) respectively.

## a) dc/dc mode

b2D performance in the dc/dc mode when controlled by a PI controller is shown in Figure 4.15 with ( $V_{i n}=200 \mathrm{~V}, L_{l}=L_{2}=1 \mathrm{mH}, \mathrm{C}=80 \mu \mathrm{~F}, f_{s}=30 \mathrm{kHz}$ and $\mathrm{R}=22 \Omega$ ).

Figure 4.15 b shows the continuous input current at $D=0.8$. In Figure 4.15 c, a square wave reference voltage is chosen to show controller response. From Figure 2.15a, the input current ripple in b 2 D is small in comparison with b1C and b1D


Figure 4.14. Two configurations of b2D converter: (a) $t_{o n}$ and (b) $t_{o f f}$

$$
\begin{align*}
& {\left[\begin{array}{l}
\dot{I}_{i n} \\
\dot{V}_{c} \\
\dot{I}_{o}
\end{array}\right]=\left[\begin{array}{ccc}
\frac{-r_{1}}{L_{l}} & -\frac{1}{L_{l}} & 0 \\
\frac{1}{C} & 0 & \frac{-D}{C} \\
0 & \frac{D}{L_{2}} & \frac{-\left(R+r_{2}\right)}{L_{2}}
\end{array}\right]\left[\begin{array}{l}
I_{i n} \\
V_{c} \\
I_{o}
\end{array}\right]+\left[\begin{array}{c}
\frac{1}{L_{l}} \\
0 \\
0
\end{array}\right]\left[V_{\text {in }}\right]}  \tag{4.7}\\
& {\left[\begin{array}{c}
\dot{\tilde{I}}_{i n} \\
\dot{\hat{V}}_{c} \\
\dot{\tilde{I}}_{o}
\end{array}\right]=\left[\begin{array}{ccc}
\frac{-r_{1}}{L_{1}} & -\frac{1}{L_{l}} & 0 \\
\frac{1}{C} & 0 & \frac{-D_{e}}{C} \\
0 & \frac{D_{e}}{L_{2}} & \frac{-\left(R+r_{2}\right)}{L_{2}}
\end{array}\right]\left[\begin{array}{c}
\tilde{I}_{i n} \\
\tilde{V}_{c} \\
\tilde{I}_{o}
\end{array}\right]+\left[\begin{array}{c}
0 \\
\frac{D_{e} V_{\text {in }}}{R C} \\
\frac{V_{\text {in }}}{L_{2}}
\end{array}\right][\delta]} \tag{4.8}
\end{align*}
$$

The small-signal transfer function can be expressed as:

$$
\begin{align*}
& \quad G(s)=\frac{\tilde{V_{o}}(s)}{\delta(s)}=\frac{a_{2} s^{2}+a_{1} s+a_{0}}{b_{3} s^{3}+b_{2} s^{2}+b_{1} s+b_{0}} \\
& a_{2}=R C L_{l} V_{i n} \\
& a_{1}=V_{i n}\left(-D^{2}{ }_{e} L_{1}+C R r_{1}\right) \\
& a_{0}=V_{i n}\left(R-D_{e}^{2} r_{1}\right)  \tag{4.9}\\
& b_{3}=C L_{1} L_{2} \\
& b_{2}=C\left(L_{1}\left(R+r_{2}\right)+L_{2} r_{1}\right) \\
& b_{1}=L_{2}+D_{e}{ }^{2} L_{1}+C\left(R r_{l}+r_{1} r_{2}\right) \\
& b_{0}=\left(R+r_{2}\right)+D_{e}{ }^{2} r_{1}
\end{align*}
$$

Figure 4.15 d shows that the gain margin is small and the stability limits of the controller are restricted in comparison with b1C and b1D. This increases control design complexity, and represents a drawback of this group of converters.


Figure 4.15. Performance of b2D in dc/dc mode at $V_{\text {in }}=200 \mathrm{~V}$ : (a) $V_{c}$ at $\mathrm{D}=0.8$, (b) $I_{i n}$ at $\mathrm{D}=0.8$, (c) output voltage $V_{o}$ when controlled with PI controller to follow a square wave reference voltage in ( $K_{p}=0.05$ and $K_{i}=0.5$ ), and (d) Bode plot at $\mathrm{D}=$

## b) dc/ac single-phase inverter

Two bidirectional b2D converters are connected to form a single-phase dc/ac inverter as shown in Figure 4.16. In Figure 4.17, the resultant single-phase inverter is controlled with PR controller to produced sinusoidal output voltage waveform.


Figure 4.16. Single-phase dc/ac inverter using two b2D converters.


Figure 4.17. Performance of closed loop PR controlled single-phase b2D inverter at $V_{\text {in }}=200 \mathrm{~V}$ and $V_{o}^{r e f}=160 \sin \omega t$ : (a) $I_{L 1}-I_{L 2}$, (b) $V_{c 1^{-}} V_{c 2}$, (c) output voltage $V_{o}$, and (d) Bode plot at $\left(K_{p}=0.05\right.$ and $\left.K_{r}=0.1\right)$.

## c) dc/ac three-phase inverter

The three-phase buck inverter based on bidirectional b2D converters is shown in Figure 4.18. Its experimental operation in a three-phase inverter is shown in Figure 4.19 when controlled by the PR controllers.


Figure 4.18. Three-phase buck inverter based on b2D.


Figure 4.19 Performance of closed loop PR controlled three-phase b2D inverter at $V_{\text {in }}$ $=200 \mathrm{~V}$ and $V_{o}^{\text {ref }}=80 \sin \omega t$ : (a) $I_{i n}$, (b) $V_{c a}-V_{c b}-V_{c c}$, and (c) three-phase output voltage $V_{o}$.

### 4.1.4 b2F

The b2F converter shown in Figure 2.29b has continuous input current. Here, the output capacitor $C_{o}$ is necessary as the output current is discontinuous. Figure 4.20 shows two operation modes of the b2D converter. The large and small-signal models and the transfer function of this converter are presented in (4.10), (4.11) and (4.12) respectively.


Figure 4.20. Two configurations of b2F converter: (a) $t_{o n}$ and (b) $t_{\text {off }}$

## a) $d c / d c$ mode

Similar to the previous converters, the dc/dc operation of the b2F is shown in Figure 4.21 with $\left(V_{i n}=200 \mathrm{~V}, L_{l}=L_{2}=1 \mathrm{mH}, C=25 \mu \mathrm{~F}, f_{s}=30 \mathrm{kHz}, C_{o}=25 \mu \mathrm{~F}\right.$, and $\mathrm{R}=$
$22 \Omega$ ). There are two main differences between this converter and the previous three buck converters. The first is the average voltage across the energy transfer capacitor $C$, as for $\mathrm{b} 1 \mathrm{C}, \mathrm{b} 1 \mathrm{D}$ and b 2 D , is independent of the duty ratio and equal the input voltage $V_{i n}$. For b2F, as in Figure 2.31d, this voltage equals $V_{i n}-V_{o}=(1-D) V_{i n}$. The second difference is that because the output shunt capacitor $C_{o}$ is required to be a larger value, the system's order is increased and becomes unstable as shown in Figure 4.21a.

$$
\begin{align*}
& {\left[\begin{array}{l}
\dot{I_{i n}} \\
\dot{V_{c}} \\
\dot{I_{L 2}} \\
\dot{V_{o}}
\end{array}\right]=\left[\begin{array}{cccc}
\frac{-r_{l}}{L_{l}} & -\frac{l}{L_{l}} & 0 & -\frac{l}{L_{l}} \\
\frac{l-D}{C} & 0 & \frac{-D}{C} & 0 \\
0 & \frac{D}{L_{2}} & \frac{-r_{2}}{L_{2}} & \frac{-(l-D)}{L_{2}} \\
\frac{1}{C_{o}} & 0 & \frac{l-D}{C_{o}} & \frac{-1}{R C_{o}}
\end{array}\right]\left[\begin{array}{l}
I_{i n} \\
V_{c} \\
I_{L 2} \\
V_{o}
\end{array}\right]+\left[\begin{array}{l}
\frac{1}{L_{l}} \\
0 \\
0 \\
0
\end{array}\right]\left[V_{V_{n}}\right]}  \tag{4.10}\\
& {\left[\begin{array}{c}
\dot{\tilde{I}}_{i n} \\
\dot{V_{c}} \\
\dot{\tilde{I}_{L 2}} \\
\dot{V_{o}}
\end{array}\right]=\left[\begin{array}{cccc}
\frac{-r_{1}}{L_{l}} & -\frac{1}{L_{1}} & 0 & -\frac{1}{L_{1}} \\
\frac{1-D_{e}}{C} & 0 & \frac{-D_{e}}{C} & 0 \\
0 & \frac{D_{e}}{L_{2}} & \frac{-r_{2}}{L_{2}} & \frac{-\left(1-D_{e}\right)}{L_{2}} \\
\frac{1}{C_{o}} & 0 & \frac{1-D_{e}}{C_{o}} & \frac{-1}{R C_{o}}
\end{array}\right]\left[\begin{array}{c}
\tilde{I}_{i n} \\
\tilde{V_{c}} \\
\tilde{I}_{L 2} \\
\tilde{V_{o}}
\end{array}\right]+\left[\begin{array}{c}
0 \\
\frac{D_{e} V_{\text {in }}\left(1+D_{e}\right)}{R C} \\
\frac{V_{\text {in }}}{L_{2}} \\
\frac{D_{e} V_{i n}}{R C_{o}}
\end{array}\right][\delta]} \\
& G(s)=\frac{\tilde{V_{o}}(s)}{\delta(s)}=\frac{a_{3} s^{3}+a_{2} s^{2}+a_{1} s+a_{0}}{b_{4} s^{4}+b_{3} s^{3}+b_{2} s^{2}+b_{1} s+b_{0}} \\
& a_{3}=C D_{e} L_{1} L_{2} V_{\text {in }} \\
& a_{2}=C V_{i n}\left(L_{1} R\left(1-D_{e}\right)+D_{e}\left(L_{1} r_{2}+L_{2} r_{1}\right)\right) \\
& a_{I}=V_{i n}\left(2 D_{e} L_{2}-D^{2}{ }_{e} L_{I}+D_{e}{ }^{3} L_{I}+D_{e}{ }^{4} L_{I}+C R r_{l}-C D_{e} R r_{I}+C D_{e} r_{1} r_{2}\right) \\
& a_{0}=V_{i n}\left(R\left(1-D_{e}\right)+2 D_{e} r_{2}+D_{e}{ }^{2}(R-r l)+r_{I}\left(D_{e}{ }^{3}+D_{e}{ }^{4}\right)\right) \\
& b_{4}=C C_{o} L_{1} L_{2} R \\
& b_{3}=C L_{1} L_{2}+C C_{o} R\left(L_{1} r_{2}+L_{2} r_{1}\right) \\
& b_{2}=C R\left(L_{1}+L_{2}\right)+C_{o} L_{2} R+C\left(L_{1} r_{2}+L_{2} r_{1}\right)-2 C D L_{1} R- \\
& C_{o} D L_{2} R+D_{e}{ }^{2} L_{1} R\left(C+C_{o}\right)+C C_{o} R r_{1} r_{2} \\
& b_{1}=L_{2}\left(l-D_{e}\right)+D_{e}{ }^{2} L_{1}+C R\left(r_{1}+r_{2}\right)+C_{o} R r_{2}+C r_{1} r_{2} \\
& +D_{e}{ }^{2} R r_{1}\left(C+C_{o}\right)-D_{e} R\left(2 C r_{1}+C_{o} r_{2}\right) \\
& b_{0}=R\left(1-D_{e}+D_{e}{ }^{2}\right)+r_{2}\left(1-D_{e}\right)+D_{e}{ }^{2} r_{I}
\end{align*}
$$

Therefore, the system will need more complex control. Hence, a two loop controller is mandatory for a stable operation as shown in Figure 4.21b. The poles loci for single and two loop versions are shown in Figure 4.22.

(a)

(c) $G_{p i} * G_{c l}$


2A/div-5ms/div
(e)

(b)

(d)


20V/div - $5 \mathrm{~ms} / \mathrm{div}$

$$
-V_{o},-I_{o}{ }^{r e f} \cdot R
$$

(f)

Figure 4.21. Operation of b2F in dc/dc mode at $V_{i n}=200 \mathrm{~V}$ : (a) Bode plot of G, (b) two-loops controller for b2F, (c) Bode plot of the overall controller shown in (b) with $K_{p}=2, K_{i}=1$ and $K=1$, (d) $V_{c}$ at $\mathrm{D}=0.8$, (e) $I_{i n}$ at $\mathrm{D}=0.8$, and (f) output voltage $V_{o}$


Figure 4.22. Poles loci of single loop control (blue) and two loop controller (green)

## b) dc/ac single-phase inverter

Two bidirectional b2F converters are connected to form a single-phase dc/ac inverter as shown in Figure 4.23. In Figure 4.24, the resultant single-phase inverter is controlled with a two-loop PR controller to produced sinusoidal output voltage.


Figure 4.23. Single-phase dc/ac inverter using two b2F converters.

## c) dc/ac three-phase inverter

The three-phase buck inverter based on a bidirectional b2F converter is shown in Figure 4.25. The experimental operation of the b2F three-phase inverter is shown in Figure 4.26 when controlled by PR controllers.


Figure 4.24. Operation of single-phase b2F inverter at $V_{i n}=200 \mathrm{~V}$ and $I_{o}^{\text {ref }}=\frac{160}{R}$ $\sin \omega t$ : (a) two-loops PR controller for b2F, (b) Bode plot of the overall controller shown in (a) with $K_{p}=2, K_{r}=5$ and $K=1$, (c) $I_{1}$ and $I_{2}$, (d) $V_{c 1}$ and $V_{c 2}$, and (e) $V_{o}$ at $\mathrm{D}=0.8$, (f) output voltage $V_{o}$.


Figure 4.25 Three-phase buck inverter based on b2F.


Figure 4.26 Performance of closed loop PR controlled three-phase b2F in dc/ac mode at $V_{i n}=200 \mathrm{~V}$ and $V_{o}^{\text {ref }}=80 \sin \omega t$ : (a) $I_{i n}$, (b) $V_{c a}-V_{c b}-V_{c c}$, and (c) three-phase output voltage $V_{o}$.

### 4.1.5 Notes and discussion on buck converters

According to the previous discussions and experimental results, the four converters families can be compared with each other's in terms of efficiency, output voltage Total Harmonic Distortion (THD), input current ripple, and control complexity. The comparisons are carried out under the same operational conditions and passive elements values

## a) Efficiency

Figure 4.27 shows the efficiency comparisons of single-phase and three-phase inverters presented in this chapter. There are two sources of losses in the power converters. The first source is the power loss through the active switches and forward diode current conduction. From Chapter 2, all four buck converters have the same switch and diode currents waveforms at a given duty ratio. This means that all converters have the same semiconductor power losses. The second source that decreases the efficiency is the loss in inductor equivalent resistance ( $r_{1}$ and $r_{2}$ ). These losses depend on their current: $I_{L 1}{ }^{2} r_{1}$ and $I_{L 2}{ }^{2} r_{2}$. Table 4.1 shows the currents through $L_{1}$ and $L_{2}$. At duty ratios larger than 0.5 , which is the typical operation for buck
inverters, the power loss in b1C is the least. This explains why the b1C inverters have the best efficiency. b1D have higher power loss than b1C because the current through $L_{2}$ is higher. b2D and b2F have the same inductors currents and hence have equal power losses.

Table 4.1. Inductor currents

| Topology | $\boldsymbol{L}_{\boldsymbol{1}}$ | $\boldsymbol{L}_{\boldsymbol{2}}$ |
| :---: | :---: | :---: |
| b1C | $D I_{o}$ | $(1-D) I_{o}$ |
| b1D | $(1-D) I_{o}$ | $I_{o}$ |
| b2D | $D I_{o}$ | $I_{o}$ |
| b2F | $D I_{o}$ | $I_{o}$ |

b) $T H D$

Comparison between output voltage THD for the different inverters is shown in Figure 4.28, where b2F always has the lower THD while b1C has the highest. b1D and b2D have similar THD, between that of b1C and b2F. The distortion in the converter output voltage and current occurs due to low and high frequency components. The low frequency voltage and current components can be reduced with proper control schemes; as will be discussed in Chapter 5. However, the high frequency components can be decreased by two methods. The first is to change the employed PWM technique in order to cancel certain voltage and current components from different phases. The second method is to use passive elements with higher values. Although this method is much simpler than the first, it adds to the size, cost, and reliability of the converter. Figure 4.29 shows the calculated high frequency ripple current at different input voltages and load powers.


Figure 4.27. Efficiencies of buck inverters: (a) single-phase and (b) three-phase.


Figure 4.28. $V_{o}$ THD of buck inverters: (a) single-phase and (b) three-phase.


Figure 4.29. Calculated output ripple current at different input voltages and load

## c) Control Complexity

As mentioned, the b2F converter is the most difficult for control processing. This is because it provides high gain at $180^{\circ}$ phase which increase the system's instability. Therefore, controlling with a single loop is difficult. b2D provides lower gain at $180^{\circ}$ and can be controlled with a single loop controller if the controller gain values are selected carefully. A 7.28 dB gain margin is obtained in Figure 4.17d for b2D. Because they do not have an $180^{\circ}$ phase shift in their Bode plots, b1C and b1D are readily controlled, as shown in the experimental work.

## d) Input current ripple

Renewable energy applications, especially PV application, has a specified curve between the source current and voltage to guarantee maximum extraction power from the renewable source [4.14]-[4.16]. Losses of the renewable source energy during miss-tracking, which are different from transformer copper, core and devices losses, are affected by the input current ripple [4.10]. When the converter has high
input current ripple, its operating point oscillates around this maximum power point and hence, the average obtained power is decreased. Comparing the different converters in terms of input current ripple, b1C and b1D have relatively higher input ripple than b2D and b2F. This appears in Figures 2.9a, 2.14a, 2.15a and 2.31a.

### 4.2 Boost Converters

Grid connected renewable energy systems inject power into the ac grid [4.16]. With aforementioned buck converters, a line frequency transformer is required to match converter output voltage to that of the ac grid. An alternative is to connect many renewable sources in series in order to have a higher input dc voltage. In some applications like PV systems, this may create undesirable characteristics such as during partial shading, etc. [4.17]. For some applications where galvanic isolation is not mandatory, boost inverters allow grid connection, without using line transformers; thus, higher overall system efficiency can be achieved. In [4.18, 4.19] topologies without line transformers have better efficiency, smaller size and lower cost than systems with line transformers. Therefore, a typical transformer-less renewable system, consists of renewable energy generator, dc stage for decoupling and phase interfacing reactor plus shunt filter capacitors to enable power control and injection of high quality voltage and current into ac grid. This provides attractive modularity which permits scaling up of the renewable energy system. The output power of PV arrays is affected significantly by partial shading [4.17]. This effect increases if the PV modules are connected in series as the same current passes through all the modules. A modular PV system allows each PV array to be controlled separately; hence, the total harvested energy is increased [4.18]. Moreover, modularity allows mass production of the inverters, and this decreases production costs [4.18]. Increasing the efficiency, ensuring operational reliability, and lifetime are of paramount important for renewable energy system design [4.20]. However, grounding currents and EMI problems are the main concerns of these systems [4.21]. In this context, there are eight converters which provide continuous input current and three of them provide continuous input and output currents (all are shown in Figure 4.30). The traditional single-phase and three-phase current source inverters (CSI) with continuous input currents were presented in [4.21], [4.22] and shown in Figure 4.31. These inverters can be viewed as extensions of the B1A converter (shown in

Figure 4.30a). The main advantages of these inverters are summarized in the following points [4.23]:

1) A ripple free continuous input dc current is preferable for many renewable energy systems because it allow the global maximum power point to be tracked; thus, the true maximum power can be extracted.
2) Boosting capability allows grid connection, without line-frequency transformers.
3) No dc-link electrolytic capacitor is required, which increases system reliability and reduces overall system size and weight.

This section presents boost converter configurations with continuous-input and/or continuous-output currents when operated in dc/dc, dc/ac single-phase, and dc/ac three-phase modes. Finally, a discussion of their main characteristics is provided.

### 4.2.1 B1C

The B1C converter is shown in Figure 4.30b. The two circuits during ON and OFF durations are shown in Figure 4.32. The converter models and its transfer function are stated in (4.13) and (4.14). The single-phase and three-phase inverters emerging from the B1C converter are shown in Figure 4.33 and Figure 4.34 respectively.

$$
\begin{align*}
& {\left[\begin{array}{c}
\dot{I}_{L 1} \\
\dot{V}_{c} \\
\dot{I}_{o}
\end{array}\right]=\left[\begin{array}{ccc}
\frac{-r_{1}}{L_{1}} & \frac{D-1}{L_{1}} & 0 \\
\frac{1-D}{C} & 0 & \frac{-D}{C} \\
0 & \frac{D}{L_{2}} & \frac{-\left(R+r_{2}\right)}{L_{2}}
\end{array}\right]\left[\begin{array}{c}
I_{L 1} \\
V_{c} \\
I_{o}
\end{array}\right]+\left[\begin{array}{c}
\frac{1}{L_{1}} \\
0 \\
0
\end{array}\right]\left[\begin{array}{l}
\left.V_{i n}\right]
\end{array}\right.}  \tag{4.13}\\
& {\left[\begin{array}{c}
\dot{\tilde{I}}_{L 1} \\
\dot{\tilde{V}_{c}} \\
\dot{\tilde{I}_{o}}
\end{array}\right]=\left[\begin{array}{ccc}
\frac{-r_{1}}{L_{1}} & \frac{D_{e}-1}{L_{1}} & 0 \\
\frac{1-D_{e}}{C} & 0 & \frac{-D_{e}}{C} \\
0 & \frac{D_{e}}{L_{2}} & \frac{-\left(R+r_{2}\right)}{L_{2}}
\end{array}\right]\left[\begin{array}{c}
\tilde{I}_{L 1} \\
\tilde{V_{c}} \\
\tilde{I}_{o}
\end{array}\right]+\left[\begin{array}{c}
\frac{V_{i n}}{L_{1}\left(1-D_{e}\right)} \\
\frac{-V_{i n}}{R C\left(1-D_{e}\right)^{2}} \\
\frac{V_{i n}}{L_{2}\left(1-D_{e}\right)}
\end{array}\right][\delta]} \tag{4.14}
\end{align*}
$$



Figure 4.30. Switched-mode power supplies with continuous input and/or continuous output currents.


Figure 4.31. Traditional current source inverters: (a) single-phase inverter and (b) three-phase inverter.


Figure 4.32. Two configurations of B1C converter: (a) $t_{o n}$ and (b) $t_{o f f}$


Figure 4.33. B1C single-phase inverter.


Figure 4.34. B1C three-phase inverter.
The operation of the dc converter and dc/ac inverters are shown in Figure 4.35, Figure 4.36, and Figure 4.37 respectively.


Figure 4.35. Operation of B1C in dc/dc mode at $V_{i n}=50 \mathrm{~V}$ : (a) control structure, (b) PI-Controlled system Bode plot (c) $V_{c}$ at $\mathrm{D}=0.5$, (d) $I_{i n}$ at $\mathrm{D}=0.5$, and (e) output voltage $V_{o}$ with square wave reference. $\left(C=10 \mu \mathrm{~F}, L_{1}=L_{2}=1 \mathrm{mH}\right.$, and $\mathrm{R}=22 \Omega$ ).

(a)

Figure 4.36. Operation of B1C in dc/ac mode (single-phase) at $V_{i n}=50 \mathrm{~V}$ and ( $I_{o}^{\text {ref }} . R$ $=100 \sin \omega t$ : (a) control structure, (b) PR-Controlled system Bode plot (c) $I_{1}$ and $I_{2}$, (d) capacitor voltage $V_{c l}$, and (e) output voltage $\left.V_{o}\right)$. $\left(C=5 \mu \mathrm{~F}, L_{l}=L_{2}=1 \mathrm{mH}\right.$, and R

(c)

Figure 4.37. Operation of B1C in dc/ac mode (three-phase) at $V_{i n}=50 \mathrm{~V}, V_{m}=100$ : (a) $I_{i n}$, (b) capacitors voltages $V_{c 1}-V_{c 2}-V_{c 3}$, and (c) load voltages $\left(V_{o 1}-V_{o 2}-V_{o 3}\right)$.

### 4.2.2 B1E

The bidirectional B1E converter is shown in Figure 4.30e. Because of the discontinuous nature of the output current $i_{o}$, an output capacitor $C_{o}$ is unavoidable. Unlike the converters with continuous output currents, the value of $C_{o}$ cannot be negligible in respect to the energy transfer capacitor $C$. Consequently, the emerging pole from $C_{o}$ is close to the converter's dominant poles. This raises the order of the converter to four and complicates control design. The two circuit configurations during ON and OFF states are shown in Figure 4.38. The converter models and its transfer function are given in (4.15), (4.16), and (4.17). The single-phase and threephase inverters emerging from B1E converter are shown in Figure 4.39 and Figure 4.40 respectively. Operation of the dc converter and dc/ac inverters are shown in Figure 4.41, Figure 4.42, and Figure 4.43 respectively. In general for high order converters, sufficient stability margins cannot be obtained with controller large bandwidth. This affects converter response to time varying voltage and current waveforms and creates undesirable distortion and harmonics which need additional control effort. This will be discussed for specific converters in Chapter 5.


Figure 4.38. Two configurations of B1E converter: (a) $t_{o n}$ and (b) $t_{o f f}$.


Figure 4.39. B1E single-phase inverter.


Figure 4.40. B1E three-phase inverter.

$$
\begin{align*}
& {\left[\begin{array}{l}
\dot{I}_{i n} \\
\dot{V_{c}} \\
\dot{I_{L 2}} \\
\dot{V_{o}}
\end{array}\right]=\left[\begin{array}{cccc}
\frac{-r_{1}}{L_{1}} & \frac{1}{L_{1}} & 0 & -\frac{1}{L_{l}} \\
\frac{-1}{C} & 0 & \frac{1}{C} & 0 \\
0 & \frac{-1}{L_{2}} & \frac{-r_{2}}{L_{2}} & 0 \\
\frac{1}{C_{o}} & 0 & \frac{-D}{C_{o}} & \frac{-1}{R C_{o}}
\end{array}\right]\left[\begin{array}{l}
I_{i n} \\
V_{c} \\
I_{L 2} \\
V_{o}
\end{array}\right]+\left[\begin{array}{c}
\frac{1}{L_{1}} \\
0 \\
0 \\
0
\end{array}\right]\left[\begin{array}{l}
\left.V_{i n}\right] \\
\\
\hline
\end{array}\right.}  \tag{4.15}\\
& {\left[\begin{array}{c}
\dot{\tilde{I}}_{i n} \\
\dot{\tilde{V}}_{c} \\
\dot{\tilde{I}}_{L 2} \\
\dot{\tilde{V}_{o}}
\end{array}\right]=\left[\begin{array}{cccc}
\frac{-r_{1}}{L_{l}} & \frac{1}{L_{1}} & 0 & -\frac{1}{L_{1}} \\
\frac{-1}{C} & 0 & \frac{1}{C} & 0 \\
0 & \frac{-1}{L_{2}} & \frac{-r_{2}}{L_{2}} & 0 \\
\frac{1}{C_{o}} & 0 & \frac{-D_{e}}{C_{o}} & \frac{-1}{R C_{o}}
\end{array}\right]\left[\begin{array}{c}
\tilde{I}_{i n} \\
\tilde{V}_{c} \\
\tilde{I}_{L 2} \\
\tilde{V}_{o}
\end{array}\right]+\left[\begin{array}{c}
0 \\
\frac{V_{i n}}{\left(1-D_{e}\right) L_{2}} \\
-\frac{V_{\text {in }}}{\left(1-D_{e}\right)^{2} R C}
\end{array}\right][\delta]} \tag{4.16}
\end{align*}
$$

$$
\begin{align*}
& G(s)=\frac{\tilde{V_{o}}(s)}{\delta(s)}=\frac{a_{3} s^{3}+a_{2} s^{2}+a_{1} s+a_{0}}{b_{4} s^{4}+b_{3} s^{3}+b_{2} s^{2}+b_{1} s+b_{0}} \\
& a_{3}=-C C_{o} L_{1} L_{2} V_{\text {in }} \\
& a_{2}=-C V_{i n}\left(C L_{1} R\left(1-D_{e}\right)^{2}+C_{o}\left(L_{1} r_{2}+L_{2} r_{1}\right)\right) \\
& a_{l}=-V_{i n}\left[C^{2} \operatorname{Rr}_{l} D_{e}\left(1-D_{e}\right)+C_{o} C r_{1} r_{2}+C_{o}\left(L_{l}+L_{2}\right)\right] \\
& a_{0}=V_{\text {in }}\left[C R\left(1-D_{e}\right)^{2}-C_{o}\left(r_{1}+r_{2}\right)\right] \\
& b_{4}=C^{2} C_{o} L_{1} L_{2} R\left(1-D_{e}\right)^{2}  \tag{4.17}\\
& b_{3}=C^{2}\left(1-D_{e}\right)^{2}\left[L_{1} L_{2}+C_{o} R\left(L_{1} r_{2}+L_{2} r_{1}\right)\right] \\
& b_{2}=\left(1-D_{e}\right)^{2}\left[C L_{1} R D_{e}{ }^{2}+C L_{2}\left(r_{1}+R\right)+C_{o} R\left(L_{1}+L_{2}\right)+\right. \\
& C L_{1} r_{2}+C C_{o} R r_{1} r_{2} \\
& b_{1}=C\left(1-D_{e}\right)^{2}\left[C r_{1} R D_{e}{ }^{2}+C_{o} R\left(r_{1}+r_{2}\right)+\left(L_{1}+L_{2}\right)+C r_{2}\left(R+r_{1}\right)\right] \\
& b_{0}=C\left(1-D_{e}\right)^{2}\left[R\left(1-D_{e}\right)^{2}+\left(r_{1}+r_{2}\right)\right] \\
& \text { (a) } G_{p i}{ }^{*} G_{c l}\left(K_{p}=1, K_{i}=40 \text { and } K=5\right) \\
& 25 \mathrm{~V} / \mathrm{div}-20 \mathrm{~ms} / \mathrm{div} \\
& \text { (c) } \\
& \text { 3A/div-20ms/div } \\
& \text { (b) } \\
& 25 \mathrm{~V} / \mathrm{div}-5 \mathrm{~ms} / \text { div } \\
& -V_{o},-I_{o}{ }^{\text {ref }} \cdot R \\
& \text { (f) }
\end{align*}
$$

Figure 4.41. Operation of B1E in dc/dc mode at $V_{i n}=50 \mathrm{~V}$ : (a) PI-Controlled system Bode plot (c) $V_{c}$ at $\mathrm{D}=0.5$, (d) $I_{i n}$ at $\mathrm{D}=0.5$, and (e) output voltage $V_{o}$ with square wave reference. $\left(C=C_{o}=5 \mu \mathrm{~F}, L_{1}=L_{2}=1 \mathrm{mH}\right.$, and $\mathrm{R}=22 \Omega$ ).


Figure 4.42. Operation of B1E in dc/ac mode (single-phase) at $V_{i n}=50 \mathrm{~V}$ and ( $I_{o}{ }^{r e f} . R$ $=100$ sinct: (a) control structure, (b) PR-Controlled system Bode plot (c) $I_{1}$ and $I_{2}$, (d) capacitor voltage $V_{c l}$, and (e) output voltage $\left.V_{o}\right) .\left(C=C_{o}=5 \mu \mathrm{~F}, L_{1}=L_{2}=1 \mathrm{mH}\right.$,

(a)

$50 \mathrm{~V} / \mathrm{div}-5 \mathrm{~ms} / \mathrm{div}$
(b)

$50 \mathrm{~V} / \mathrm{div}-5 \mathrm{~ms} / \mathrm{div}$
(c)

Figure 4.43. Operation of B1E in dc/ac mode (three-phase) at $V_{i n}=50 \mathrm{~V}, V_{m}=100$ : (a) $I_{i n}$, (b) Capacitors voltages $V_{c 1}-V_{c 2}-V_{c 3}$, and (c) load voltages ( $V_{o 1}-V_{o 2}-V_{o 3}$ ).

### 4.2.3 Other Converters

The same approach and analysis are repeated for the remaining converters, B1D, B2D, B2E, B2G, and B1P. To avoid prolongation, the emerging single-phase and three-phase inverters are described with their experimental operation, will be found in Appendix C.

### 4.2.4 Notes and discussion on boost converters

The boost inverter topologies can be compared with the traditional CSI, as previously introduced in terms of efficiency, output voltage Total Harmonic Distortion (THD), input current ripple and control complexity. Such a comparison carried out, under the same operating conditions and passive elements values.

## a) Efficiency

Table 4.2 shows the inductor and switch currents of the different boost topologies. The components currents of B1C and B1P are identical; hence, they have similar losses and efficiencies. Both B1E and B2E have similar current components. Figure 4.44 shows the efficiencies of the different inverters with identical passive components ( $L_{1}=L_{2}$ and $r_{1}=r_{2}$ ). B1C and B1P have better overall efficiency than the conventional CSI. B2G has the worst efficiency because of the higher inductor and switch currents. For Cell D inverters, B1D has better efficiency than B2D for D $<0.5$ while B2D has better efficiency for D>0.5. B1E and B2E have comparable efficiency.


Figure 4.44. Efficiency comparison of boost inverters.

Table 4.2. Inductors and devices currents of boost converters

| Topology | $L_{1}$ | $L_{2}$ | $I_{S I}$ | $I_{S 2}$ |
| :---: | :---: | :---: | :---: | :---: |
| B1C | $\frac{D}{1-D} I_{o}$ | $I_{o}$ | $\frac{1}{1-D} I_{o}$ | $\frac{1}{1-D} I_{o}$ |
| B1D | $\frac{1}{1-D} I_{o}$ | $\frac{D}{1-D} I_{o}$ | $\frac{1}{1-D} I_{o}$ | $\frac{1}{1-D} I_{o}$ |
| B2D | $\frac{1}{1-D} I_{o}$ | $I_{o}$ | $\frac{1}{1-D} I_{o}$ | $\frac{1}{1-D} I_{o}$ |
| B1E | $\frac{1}{1-D} I_{o}$ | $\frac{1}{1-D} I_{o}$ | $\frac{1}{1-D} I_{o}$ | $\frac{1}{1-D} I_{o}$ |
| B2E | $\frac{1}{1-D} I_{o}$ | $\frac{1}{1-D} I_{o}$ | $\frac{1}{1-D} I_{o}$ | $\frac{1}{1-D} I_{o}$ |
| B2G | $\frac{l-D}{1-2 D} I_{o}$ | $\frac{D}{1-2 D} I_{o}$ | $\frac{1}{1-2 D} I_{o}$ | $\frac{1}{1-2 D} I_{o}$ |
| B1P | $\frac{D}{l-D} I_{o}$ | $I_{o}$ | $\frac{1}{1-D} I_{o}$ | $\frac{1}{1-D} I_{o}$ |

## b) THD

Comparison between output voltages THD for the different inverters is shown in Figure 4.45, where if the same inductors and capacitors values are used, inverters from B2D and B2E have the lowest THD in the output voltage and current waveforms, while inverters from B1C, B1D and B1P have the highest THD, followed by B2G.


Figure 4.45. Output voltages THD of boost inverters.


Figure 4.46. Root loci of boost converters.

## c) Control Complexity

The aforementioned boost converters are difficult to control with single-loop classical PI or PR controllers. This is seen in the converter root loci in Figure 4.46 where all converters have their dominant poles close to the imaginary axis with zeros in the right hand side. Small proportional gains are sufficient to drive these poles towards their zeros in the right hand side. For this reason, multiple control loops are necessary to control these converters types to achieve acceptable dynamic performance and sufficient stability margin.

## d) Input currents ripple

Comparison of the experimental results of different converters in terms of input current ripple show that the inverters from cell E ( B 1 E and B 2 E ) have the lowest input current ripple, while B2G and B1P have the highest input current ripple.

### 4.3 Buck-boost Converters

Buck-boost converters have numerous advantages over buck and boost types, which can be summarised as follows:

- A buck-boost converter can cover all the operating voltage range of buck and boost converters, that is, it can generate output voltage magnitude lower or higher than the input voltage. For example, the conventional VSI is buck type because its peak output ac voltage is always lower than the input dc voltage [4.24]; while the conventional CSI is considered boost type because its peak output ac voltage is always higher than the input dc voltage [4.25].
- Many buck-boost converters can be isolated with high-frequency transformers. This feature is beneficial from the point of view of safety, compatibility, noise, size and voltage boosting.

Many applications such as battery chargers, electrical vehicles, fuel cells, solar cells, and wind systems may require electrical isolation. The basic traditional buck-boost converter is shown in Figure 2.3d, as bB1A. The emerging single-phase and threephase inverters from bB1A are shown in Figure 4.47. However, these inverter topologies have discontinuous input current, which necessitates a large input dc-link capacitor. In 2003[4.26], the Z-source buck-boost inverter type, shown in Figure
4.48, appeared. By the means of an energy transfer LC circuit, the output voltage can be either higher or lower than the input dc voltage. The main advantage of this topology comes from the fact that there is no risk of shoot-through (simultaneous operation of upper and lower devices) of any phase leg by electromagnetic interference (EMI) noise, which is a major cause for converter reliability deterioration. However, the input diode ( $D_{i n}$ ) results in discontinuous input current From Table 2.2, there are five converters which have buck-boost transfer functions as well as provide continuous input current. These converters are bB1C (Ćuk), bB1D, $\mathrm{bB} 2 \mathrm{D}, \mathrm{bB} 1 \mathrm{~F}$ and bB1G (SEPIC) and all are suitable for transformer isolation.


Figure 4.47. Buck-boost inverters: (a) single-phase and (b) three-phase.


Figure 4.48. Z-source inverter topology.

### 4.3.1 bB1C (Ćuk) Converter

The basic Ćuk converter is shown in Figure 2.8c in the single-switch single-diode configuration. The bidirectional Ćuk converter requires two anti-parallel diode and switch combination. The Ćuk converter has an inductor at the input and the output ports, hence has continuous input and output currents. The two modes of the Cuk converter are shown in Figure 4.49 and the converter's models are illustrated in equations sets (4.18) and (4.19). The small-signal transfer function is shown in equation (4.20).


Figure 4.49. Two modes of bB1C (Ćuk) converter: (a) $t_{o n}$ and (b) $t_{o f f}$.

$$
\begin{align*}
& {\left[\begin{array}{l}
\dot{I}_{i n} \\
\dot{V}_{c} \\
\dot{I}_{o}
\end{array}\right]=\left[\begin{array}{ccc}
\frac{-r_{1}}{L_{l}} & -\frac{l-D}{L_{l}} & 0 \\
\frac{1-D}{C} & 0 & \frac{-D}{C} \\
0 & \frac{D}{L_{2}} & \frac{-\left(R+r_{2}\right)}{L_{2}}
\end{array}\right]\left[\begin{array}{l}
I_{i n} \\
V_{c} \\
I_{o}
\end{array}\right]+\left[\begin{array}{c}
\frac{1}{L_{1}} \\
0 \\
0
\end{array}\right]\left[\begin{array}{l}
\left.V_{i n}\right]
\end{array}\right.}  \tag{4.18}\\
& {\left[\begin{array}{c}
\dot{\tilde{I}}_{i n} \\
\dot{\tilde{V}_{c}} \\
\dot{\tilde{I}}_{o}
\end{array}\right]=\left[\begin{array}{ccc}
\frac{-r_{l}}{L_{l}} & \frac{D_{e}-1}{L_{l}} & 0 \\
\frac{1-D_{e}}{C} & 0 & \frac{-D_{e}}{C} \\
0 & \frac{D_{e}}{L_{2}} & \frac{-\left(R+r_{2}\right)}{L_{2}}
\end{array}\right]\left[\begin{array}{c}
\tilde{I}_{i n} \\
\tilde{V_{c}} \\
\tilde{I}_{o}
\end{array}\right]+\left[\begin{array}{c}
\frac{V_{i n}}{\left(1-D_{e}\right) L_{l}} \\
-\frac{D_{e} V_{i n}}{\left(1-D_{e}\right)^{2} R C} \\
\frac{V_{i n}}{\left(1-D_{e}\right) L_{2}}
\end{array}\right][\delta]} \tag{4.19}
\end{align*}
$$

$a_{2}=C R\left(1-D_{e}\right) L_{l} V_{\text {in }}$
$a_{1}=V_{i n}\left(-L_{l} D_{e}{ }^{2}+C R r_{1}\left(1-D_{e}\right)\right)$
$a_{0}=V_{\text {in }}\left(R\left(1-D_{e}\right)^{2}-D_{e}{ }^{2} r_{1}\right)$
$b_{3}=C L_{1} L_{2}\left(1-D_{e}\right)^{2}$
$b_{2}=C L_{l}\left(R+r_{2}+D_{e}{ }^{2} r_{2}-2 D_{e}\left(R+r_{2}\right)+D_{e}{ }^{2} R\right)+$
$C L_{2} r_{l}\left(1-D_{e}\right)^{2}$
$b_{1}=L_{1}\left(D_{e}{ }^{2}-2 D_{e}{ }^{3}+D_{e}{ }^{4}\right)+L_{2}\left(1+6 D_{e}{ }^{2}-4 D_{e}{ }^{3}+D_{e}{ }^{4}-4 D_{e}\right)+$
$C R r_{1}\left(1+D_{e}{ }^{2}\right)+C r_{1} r_{2}\left(1+D_{e}{ }^{2}\right)-2 C D_{e} r_{1}\left(R+r_{2}\right)$
$b_{0}=R\left(1-D_{e}\right)^{4}+r_{1} D_{e}{ }^{2}\left(1-D_{e}\right)^{2}+r_{2}\left(1-D_{e}\right)^{4}$

## a) dc/dc mode

Ćuk converter operation in dc/dc mode is shown in Figure 4.50 with ( $V_{i n}=200 \mathrm{~V}, L_{l}$ $=L_{2}=1 \mathrm{mH}, C=20 \mu \mathrm{~F}, f_{s}=30 \mathrm{kHz}, \mathrm{D}=0.5$, and $\mathrm{R}=22 \Omega$ ). Its control structure for the dc/dc mode is shown in Figure 4.50a and the correspondence Bode plot is shown in Figure 4.50b, with satisfactory gain and phase margins (gain margin $>10$ and phase margin $>90^{\circ}$ ). The input current $I_{i n}$ and middle capacitor voltage $V_{c}$ at $\mathrm{D}=0.5$ are shown in Figure 4.50c and d. In Figure 4.50e, the output voltage $V_{o}$ follows a reference square voltage and operate in both buck and boost modes.

(c)

$$
-V_{o},-I_{o}^{r e f} \cdot R
$$

(e)

Figure 4.50. Operation of $\dot{C} u k$ converter (bB1C) in dc/dc mode: (a) control structure, (b) Bode plot of $G^{*} G_{p i}$, with $K_{p}=2, K_{i}=1$ and $K=2$, (c) $I_{i n}$ at $\mathrm{D}=0.5$, (d) $V_{c}$ at $\mathrm{D}=$ 0.5 , (e) output voltage $V_{o}$ with square wave reference voltage.

## b) dc/ac single-phase inverter

The Ćuk converter configuration has two dc/ac single-phase inverter configurations, shown in Figure 4.51. For the first topology in Figure 4.51a, four switches and two capacitors are required. The second topology in Figure 4.51b needs one capacitor and five switches. The devices voltage stresses in the both topologies are the same. However, the device current stresses of the second topology are equal to the load current ( $I_{o}$ ) while they are equal to the sum of the load and input currents in first topology. There are major differences between the open-loop operation and the PWM signals of the two topologies. In the first, the inverter can be viewed as two separate Ćuk converters. The controller builds two output voltages $V_{o 1}$ and $V_{o 2}$ and hence, o/p voltage $V_{o}$, as shown in Figure 4.52a and Figure 4.52b. Each converter, with its device pairs $\left(S_{1}-D_{1}, S_{2}-D_{2}\right)$ or ( $S_{3}-D_{3}, S_{4}-D_{4}$ ), is operate separately with separate gate drive signals. The duty ratios of the two converters $\delta_{1}$ and $\delta_{2}$ can be calculated from the equation set (4.21). The second inverter can be viewed as two cascaded converters. The first is a boost converter while the second is buck converters and together they form a buck-boost inverter.


Figure 4.51. Two configurations of single-phase inverters based on Ćuk converter: (a) four-switch inverter and (b) five-switch inverter.


Figure 4.52. Output voltages: (a) converters voltages $V_{o 1}-V_{o 2}$ and (b) load voltage $V_{o}$.

$$
\begin{gather*}
V_{o 1}=1 / 2 V_{m} \sin \omega t+1 / 2 V_{m}, \quad V_{o 2}=1 / 2 V_{m} \sin (\omega t-\pi)+1 / 2 V_{m} \\
V_{o}=V_{m} \sin \omega t  \tag{4.21}\\
\delta_{1}=\frac{V_{o 1}}{V_{o 1}+V_{i n}} \quad \text { and } \quad \delta_{2}=\frac{V_{o 2}}{V_{o 2}+V_{i n}}
\end{gather*}
$$

The five-switch Ćuk inverter topology has four different operational modes, shown in Figure 4.53 , based on the overall inverter duty ratio $\delta_{o v}$ and the polarity of the output voltage $V_{o}$. The duty ratio $\delta_{o v}$ can be evaluated as:

$$
\begin{equation*}
\delta_{o v}=\frac{\left|V_{o}\right|}{\left|V_{o}\right|+V_{i n}} \tag{4.22}
\end{equation*}
$$



Figure 4.53. Operation modes of the single-phase inverter topology in Figure 4.51b.

Because the two topologies have identical transfer functions, they can be controlled by the control structure shown in Figure 4.54a. For the four-switch topology, the
input currents are shown in Figure 4.54c. The transfer capacitor voltages $V_{c 1}$ and $V_{c 2}$ are shown in Figure 4.54d. The load voltage $V_{o}$ is shown in Figure 4.54e. The same results for the five-switch topology are shown in Figure 4.55.


Figure 4.54. Operation of four-switch single-phase Ćuk inverter at $V_{i n}=200 \mathrm{~V}$ and $I_{o}{ }^{\text {ref }}=\frac{200}{R} \sin \omega t$ : (a) two-loops PR controller, (b) Bode plot of the overall controller shown in (a) with $K_{p}=2, K_{r}=5$ and $K=1$, (c) $I_{l}$ and $I_{2}$, (d) $V_{c l}$ and $V_{c 2}$, and (e) output voltage $V_{o}$.


Figure 4.55. Operation of five-switch single-phase $\dot{C} u k$ inverter at $V_{i n}=200 \mathrm{~V}$ and $I_{o}^{r e f}=\frac{200}{R} \sin \omega t$ : (a) $I_{i n}$ and (b) $V_{c}$, and (c) output voltage $V_{o}$

## c) dc/ac three-phase inverter

As with the single-phase inverters, the Ćuk converter has two three-phase dc/ac inverters, as shown in Figure 4.56. For the first topology in Figure 4.56a, six switches, three capacitors and six inductors are required. The second topology in Figure 4.56 b needs seven switches, one capacitor and four inductors. The devices voltage stresses in the both topologies are the same.
The six-switch topology consists of three Ćuk converters, where each converter represents one leg of the inverter, which operates separately. The open-loop operation is acquired by producing three separate converters voltages ( $V_{\text {cuk }}, V_{\text {cuk2 }}$, and $V_{c u k 3}$ ) as shown in Figure 4.57a. The three-phase load voltages ( $V_{o l}, V_{o 2}$, and $V_{o 3}$ ) in Figure 4.57 b result from the voltage difference between the three separate converters output voltages. The duty ratio of the three converters $\delta_{1,} \delta_{2}$ and $\delta_{3}$ are calculated from:

$$
\begin{gather*}
V_{1}=1 / 2 V_{m} \sin \omega t+1 / 2 V_{m} \\
V_{2}=1 / 2 V_{m} \sin (\omega t-2 / 3 \pi)+1 / 2 V_{m}  \tag{4.23}\\
V_{3}=1 / 2 V_{m} \sin (\omega t+2 / 3 \pi)+1 / 2 V_{m}
\end{gather*}
$$

$\delta_{1}=\frac{V_{1}}{V_{1}+V_{\text {in }}}$

$$
\begin{equation*}
\delta_{2}=\frac{V_{2}}{V_{2}+V_{i n}} \tag{4.24}
\end{equation*}
$$

$$
\delta_{3}=\frac{V_{3}}{V_{3}+V_{i n}}
$$


(a)

(b)

Figure 4.56. Two configurations of three-phase inverters based on Ćuk converter: (a) six-switch inverter and (b) seven-switch inverter.


Figure 4.57. Output voltages of six-switch Ćuk-based three-phase inverter: (a) converters voltages $V_{1}-V_{2}-V_{3}$ and (b) load voltages $V_{o 1}-V_{o 2}-V_{o 3}$.


Figure 4.58. Gate signals of seven-switch Ćuk inverter switches.

The seven-switch topology can be viewed as two cascaded converters. The first is a boost converter followed by a buck VSI. The overall duty ratio of the inverter is calculated from:

$$
\begin{equation*}
\delta_{o v}=\frac{V_{m}}{V_{m}+1 / 2 V_{i n}} \tag{4.25}
\end{equation*}
$$

where $V_{m}$ is the peak of the output three-phase voltage

The three legs of the VSI $\left(S_{1}, S_{2}\right)$, $\left(S_{3}, S_{4}\right)$, and ( $S_{5}, S_{6}$ ) operate with the three modulating signals $M_{1}, M_{2}$, and $M_{3}$ respectively:

$$
\begin{align*}
& M_{1}=\frac{2}{\sqrt{3}} \delta_{o v} \sin \omega t \\
& M_{2}=\frac{2}{\sqrt{3}} \delta_{o v} \sin (\omega t-2 / 3 \pi)  \tag{4.26}\\
& M_{3}=\frac{2}{\sqrt{3}} \delta_{o v} \sin (\omega t+2 / 3 \pi)
\end{align*}
$$



Figure 4.59 Performance of closed loop PR controlled six-switch three-phase Ćuk inverter at $V_{i n}=100 \mathrm{~V}$ and $V_{o}^{r e f}=100 \sin \omega t$ : (a) $I_{i n}$, (b) $V_{c a}-V_{c b}-V_{c c}$, and (c) threephase output voltage $V_{o}$.

The PWM gate signals of the seven switches are shown in Figure 4.58. During the active states of the buck inverter ( $S_{I}$ to $S_{6}$ ), the switch S is ON and the input inductor is energising by $I_{i n}$ and the capacitor is discharging into the three-phase load. During the zero states of the inverter $\left(S_{z 1}\right.$ or $\left.S_{z 2}\right)$, the switch $S$ is OFF and the stored energy flows from the inductor to the capacitor. Figure 4.59 shows the operation of a sixswitch Ćuk based three-phase inverter while Figure 4.60 shows the operation of the seven-switch inverter.


Figure 4.60 Performance of closed loop PR controlled seven-switch three-phase Ćuk inverter at $V_{i n}=100 \mathrm{~V}$ and $V_{o}^{r e f}=100 \sin \omega t$ : (a) $I_{i n}$, (b) $V_{c a}-V_{c b}-V_{c c}$, and (c) threephase output voltage $V_{o}$.

### 4.3.2 bB1G (SEPIC) Converter

The dc/dc bB1G (SEPIC) converter is shown in Figure 2.20d in a single-switch single-diode configuration. Like the bB1F, theSEPIC converter has continuous input and discontinuous output currents and hence, an output capacitor $C_{o}$ is mandatory. The two modes of this converter are shown in Figure 4.61 and the models are
illustrated in equations sets (4.27) and (4.28). The small-signal transfer function is mentioned in equation (4.29).


Figure 4.61. Two modes of bB1G (SEPIC) converter: (a) $t_{o n}$ and (b) $t_{o f f}$.

$$
\begin{align*}
& {\left[\begin{array}{l}
\dot{I}_{i n} \\
\dot{V}_{c} \\
\dot{I}_{L 2} \\
\dot{V_{o}}
\end{array}\right]=\left[\begin{array}{cccc}
\frac{-r_{1}}{L_{1}} & -\frac{(1-D)}{L_{l}} & 0 & -\frac{(1-D)}{L_{1}} \\
\frac{1-D}{C} & 0 & \frac{-D}{C} & 0 \\
0 & 0 & \frac{-r_{2}}{L_{2}} & 0 \\
\frac{1-D}{C_{o}} & 0 & \frac{1-D}{C_{o}} & \frac{-1}{R C_{o}}
\end{array}\right]\left[\begin{array}{l}
I_{i n} \\
V_{c} \\
I_{L 2} \\
V_{o}
\end{array}\right]+\left[\begin{array}{c}
\frac{1}{L_{1}} \\
0 \\
0 \\
0
\end{array}\right]\left[\begin{array}{l}
\left.V_{i n}\right]
\end{array}\right.}  \tag{4.27}\\
& {\left[\begin{array}{c}
\dot{\tilde{I}}_{i n} \\
\dot{\tilde{V}_{c}} \\
\dot{\tilde{I}}_{L 2} \\
\dot{V_{o}}
\end{array}\right]=\left[\begin{array}{cccc}
\frac{-r_{l}}{L_{l}} & -\frac{\left(1-D_{e}\right)}{L_{l}} & 0 & -\frac{\left(1-D_{e}\right)}{L_{l}} \\
\frac{1-D_{e}}{C} & 0 & \frac{-D_{e}}{C} & 0 \\
0 & 0 & \frac{-r_{2}}{L_{2}} & 0 \\
\frac{1-D_{e}}{C_{o}} & 0 & \frac{1-D_{e}}{C_{o}} & \frac{-1}{R C_{o}}
\end{array}\right]\left[\begin{array}{c}
\tilde{I}_{\text {in }} \\
\tilde{V}_{c} \\
\tilde{I}_{L 2} \\
\tilde{V}_{o}
\end{array}\right]+\left[\begin{array}{c}
\frac{V_{\text {in }}}{\left(1-D_{e}\right) L_{l}} \\
\frac{-D_{e} V_{i n}}{\left(1-D_{e}\right)^{2} R C} \\
\frac{V_{i n}}{\left(1-D_{e}\right) L_{2}} \\
\frac{-D_{e} V_{i n}}{\left(1-D_{e}\right)^{2} R C_{o}}
\end{array}\right][\delta]} \tag{4.28}
\end{align*}
$$

## a) $d c / d c$ mode

SEPIC converter operation in dc/dc mode is shown in Figure 4.62 with ( $V_{i n}=200 \mathrm{~V}$, $L_{l}=L_{2}=1 \mathrm{mH}, C=20 \mu \mathrm{~F}, C_{o}=20 \mu \mathrm{~F}, f_{s}=30 \mathrm{kHz}, \mathrm{D}=0.5$, and $\mathrm{R}=22 \Omega$ ). Being a fourth-order system, both stability margins and large bandwidth, which ensures fast dynamic response, are difficult to be achieved together in the SEPIC converter control design.

$$
\begin{align*}
& G(s)=\frac{\tilde{V_{o}}(s)}{\delta(s)}=\frac{a_{3} s^{3}+a_{2} s^{2}+a_{1} s+a_{0}}{b_{3} s^{3}+b_{2} s^{2}+b_{1} s+b_{0}} \\
& a_{3}=-C D_{e} L_{1} L_{2} V_{\text {in }} \\
& a_{2}=C R V_{i n}\left(1-D_{e}\right)^{2}\left(L_{1}+L_{2}\right) \\
& a_{l}=C R V_{\text {in }}\left(1-D_{e}\right)^{2}\left(r_{I}+r_{2}\right)-C D_{e} V_{i n} r_{1} r_{2}-D_{e}{ }^{2} L_{l} V_{\text {in }} \\
& a_{0}=R V_{\text {in }}\left(1-D_{e}\right)^{2}-D_{e}{ }^{2} V_{\text {in }} r_{I} \\
& b_{4}=C C_{o} L_{1} L_{2} R\left(1-D_{e}\right)^{2}  \tag{4.29}\\
& b_{3}=C L_{1} L_{2}\left(1-D_{e}\right)^{2}+C C_{o} R\left(1-D_{e}\right)^{2}\left[r_{1} L_{2}+r_{2} L_{1}\right] \\
& b_{2}=C R\left(1-D_{e}\right)^{4}\left(L_{1}+L_{2}\right)+C_{o} L_{2} R\left(1-D_{e}\right) 4+C_{o} L_{1} R D_{e}{ }^{2}\left(1-D_{e}\right)^{2}+ \\
& C\left(1-D_{e}\right)^{2}\left(L_{1} r_{2}+L_{2} r_{1}\right)+C C_{o} R r_{1} r_{2}\left(1-D_{e}\right) 2 \\
& b_{1}=L_{2}\left(1-D_{e}\right)^{4}+L_{1} D_{e}{ }^{2}\left(1-D_{e}\right) 2+C R\left(r_{1}+r_{2}\right)+ \\
& C_{o}\left(1-D_{e}\right)^{2}\left[\left(1-D_{e}\right)^{2}+R r_{1}\right]+C R\left(1-D_{e}\right)^{4}\left[r_{1}+r_{2}\right]+C r_{1} r_{2}\left(1-D_{e}\right)^{2} \\
& b_{0}=\left(1-D_{e}\right)^{4}\left(R+r_{2}\right)+r_{1} D_{e}{ }^{2}\left(1-D_{e}\right)^{2}
\end{align*}
$$





(c)

div - $5 \mathrm{~ms} / \mathrm{div}$

$$
-V_{o},-I_{o}^{\text {ref }} \cdot R
$$

(e)
(f)

Figure 4.62. Operation of SEPIC (bB1G) converter in dc/dc mode: (a) control structure, (b) Bode plot of $G^{*} G_{p i}$, (c) $I_{i n}$, (d) $V_{c}$, and (e) output voltage $V_{o}$ with square

## b) dc/ac single-phase inverter

As with the Cúk and bB1F converters, bB1G (SEPIC) converter has two dc/ac single-phase inverter configurations, shown in Figure 4.63. For the topology in Figure 4.63b, four switches, four capacitors and four inductors are required. The second topology, in Figure 4.63b, requires five switches, two capacitors and two inductors.

For the second topology, the four operational modes are shown in Figure 4.64. Operations of the two inverters are shown in Figure 4.65 and Figure 4.66.

(a)

(b)

Figure 4.63. Two configurations of single-phase inverters based on bBlG (SEPIC) converter: (a) four-switch inverter and (b) five-switch inverter.

## c) dc/ac three-phase inverter

The two three-phase inverter configurations based on the SEPIC converter are shown in Figure 4.67. The open-loop PWM signals of the two topologies are shown in Figure 4.68. The operation of the six-witch topology is shown in Figure 4.69 while that for the seven-switch topology is shown in Figure 4.70.


Figure 4.64 Operation modes of the single-phase inverter topology in Figure 4.63b.


Figure 4.65 . Operation of four-switch single-phase SEPIC inverter at $V_{i n}=200 \mathrm{~V}$ and $I_{o}^{\text {ref }}=\frac{200}{R} \sin \omega t$ : (a) two-loops PR controller, (b) Bode plot of the overall controller shown in (a), (c) $I_{1}$ and $I_{2}$, (d) $V_{c l}$ and $V_{c 2}$, and (e) output voltage $V_{o}$.


$50 \mathrm{~V} / \mathrm{div}-5 \mathrm{~ms} / \mathrm{div}$
(b)

Figure 4.66. Operation of five-switch single-phase SEPIC inverter at $V_{\text {in }}=200 \mathrm{~V}$ and $I_{o}^{r e f}=\frac{200}{R} \sin \omega t$ : (a) $I_{i n}$, (b) $V_{c}$, and (c) output voltage $V_{o}$.


Figure 4.67. Two configurations of three-phase inverters based on bBlG (SEPIC) converter: (a) six-switch inverter and (b) seven-switch inverter.


Figure 4.68. Gate signals of seven-switch bB1G inverter switches.


Figure 4.69 Performance of closed loop PR controlled six-switch three-phase $b B 1 G$ (SEPIC) inverter at $V_{i n}=100 \mathrm{~V}$ and $V_{o}^{\text {ref }}=100 \sin \omega t$ : (a) $I_{i n}$, (b) $V_{c a}-V_{c b}-V_{c c}$ and (c) three-phase output voltage $V_{o}$.


Figure 4.70 Performance of closed loop PR controlled seven-switch three-phase $b B 1 G$ (SEPIC) inverter at $V_{i n}=100 \mathrm{~V}$ and $V_{o}^{\text {ref }}=100 \sin \omega t$ : (a) $I_{i n}$, (b) $V_{c a}-V_{c b}-V_{c c}$, and (c) three-phase output voltage $V_{o}$.

### 4.3.3 Other buck-boost inverters

The same analysis is repeated for the remaining buck-boost converters, bB1D, bB2D, and bB1F. To avoid prolongation, the emerging single-phase and three-phase inverters are described with their experimental operation are shown in Appendix C.

### 4.3.4 Notes and discussion on the buck-boost converters

Using the same operation conditions and passive elements values, the voltage buckboost inverter topologies are compared in terms of efficiency, output voltage, Total Harmonic Distortion (THD), input current ripple, and capacitor voltage stresses.

## a) Efficiency

Table 4.3 shows the inductor and switch currents of the different topologies. The components currents of bB1C and bB1G are identical. Hence, they have similar core losses and efficiencies. Both bB1D and bB1F have similar current components. Figure 4.71 shows the efficiencies of the different inverters with identical passive components ( $L_{1}=L_{2}$ and $r_{1}=r_{2}$ ). Generally, bB 1 C and bB1G have better overall efficiency than the other three inverters. bB1D and bB1F have comparable efficiency. Comparing bB2D with both bB1D and bB1F, bB2D has a better efficiency for higher load power while bB1D and bB1F inverters have better efficiency in the low power region

Table 4.3. Inductors and devices currents of buck-boost converters

| Topology | $\boldsymbol{L}_{\boldsymbol{I}}$ | $\boldsymbol{L}_{\mathbf{2}}$ | $\boldsymbol{I}_{\mathbf{S} 1}$ | $\boldsymbol{I}_{\mathbf{S} 2}$ |
| :---: | :---: | :---: | :---: | :---: |
| bB1C | $\frac{D}{1-D} I_{o}$ | $I_{o}$ | $\frac{l}{1-D} I_{o}$ | $\frac{1}{1-D} I_{o}$ |
| bB1D | $\frac{D}{1-D} I_{o}$ | $\frac{1}{1-D} I_{o}$ | $\frac{1}{1-D} I_{o}$ | $\frac{1}{1-D} I_{o}$ |
| bB2D | $\frac{1}{1-D} I_{o}$ | $I_{o}$ | $\frac{1}{1-D} I_{o}$ | $\frac{1}{1-D} I_{o}$ |
| bB1F | $\frac{D}{1-D} I_{o}$ | $\frac{1}{1-D} I_{o}$ | $\frac{1}{1-D} I_{o}$ | $\frac{1}{1-D} I_{o}$ |
| bB1G | $\frac{D}{1-D} I_{o}$ | $I_{o}$ | $\frac{l}{1-D} I_{o}$ | $\frac{l}{1-D} I_{o}$ |

## b) $T H D$

Comparison between output voltages THD for the different inverters is shown in
Figure 4.72, where, if the same inductors and capacitors values are used, inverters from bB2D have the lowest THD in the output voltage and current waveforms while inverters from bB1C, bB1D have the highest THD, followed by bB1G and bB1F.


Figure 4.71. Efficiencies of buck-boost inverters


Figure 4.72. Output voltages THD of boost inverters.

## c) Control Complexity

As for the boost converters, buck-boost converters are difficult to control with singleloop classical PI or PR controllers as they are non-minimum phase systems with zeros in the right hand plane. Multiple control loops are necessary to control these converters types to achieve acceptable dynamic performance and sufficient stability margins.

## d) Input current ripple

Comparing the experimental results of different converters in terms of input current ripple, inverters from bB1D and bB1F have low input current ripple which forms an attractive point for PV applications [4.10].

## e) Capacitor voltage stresses

Transfer capacitor $C$ voltage stress knowledge is important for its proper selection. For some inverters, the voltage across $C$ consists of a dc-bias plus sinusoidal voltage component while for other converters, the voltage across $C$ is only dc. Inverters from bB1F and bB1G have lower capacitor voltages stresses than bB1C, bB1D and bB2D. Table 4.4 summarize the voltages stresses for each converter.

Table 4.4. Voltage stresses across capacitor $C$

| Topology | $\boldsymbol{d c}$-bias | Sinusoidal voltage | Peak Voltage |
| :---: | :---: | :---: | :---: |
| Ćuk | $V_{\text {in }}+1 / 2 V_{o}$ | $1 / 2 V_{o} \sin \omega t$ | $V_{\text {in }}+V_{o}$ |
| bB 1 | $V_{\text {in }}+1 / 2 V_{o}$ | $1 / 2 V_{o} \sin \omega t$ | $V_{\text {in }}+V_{o}$ |
| bB 2 | $V_{\text {in }}+1 / 2 V_{o}$ | $1 / 2 / V_{o} \sin \omega t$ | $V_{\text {in }}+V_{o}$ |
| bB 3 | $V_{\text {in }}$ | 0 | $V_{\text {in }}$ |
| SEPIC | $V_{\text {in }}$ | 0 | $V_{\text {in }}$ |

### 4.4 Summary

The chapter studied the buck, boost and buck-boost converter families with continuous input and/or continuous output currents where the need for large input filtering electrolytic capacitors is not necessary. Single-phase and three-phase inverters derived from each converter where compared. The comparison features include the efficiency and input high frequency ripple. Inverters with high efficiency are attractive for renewable energy applications, such as PV and fuel cells applications, to ensure maximum power harvesting. However, inverter high efficiency alone does not ensure best total system efficiency. Total system efficiency depends on other parameters such as input ripple, which degrades the output power from a renewable energy source. Other important features such as total harmonic distortion, which requires passive elements with higher values, size and weight, control complexity and capacitor stresses, were discussed.

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## Chapter 5

## Grid-connected buck-boost Inverters with Continuous Input Current

For renewable energy sources with output powers less than 2 kW , their output voltage is usually lower than the ac-grid voltage. In order to interface the renewable source to the ac-grid, an additional boost stage or line-frequency transformer is required to match the inverter output voltage to that of the grid; thus, allow power injection into the grid [5.1]-[5.9]. Line frequency transformers are expensive and heavy. Research has been conducted to establish new designs without heavy line-frequency transformers [5.10]-[5.12]. Reducing the cost, size and increasing reliability are of paramount importance from the renewable energy market prospective. Up to half the overall system cost, if the panels cost is excluded, is related to the inverter cost. [5.13]. In addition, the power inverters are the causes of $2 / 3$ the failures in renewable energy systems [5.13]. Low-cost grid-connected inverter topologies are reviewed in [5.14]-[5.16]. Generally, the inverter topology selection for renewable energy systems depends on several factors such as power loss, total cost, weight, efficiency, and voltage flexibility. The inverter's flexibility means the ability to provide output voltage which is higher or lower than the input voltage [5.17]. This flexibility is preferable for maximum power point tracking (MPPT) controllers which are responsible for extracting the highest available power from the renewable energy source. As explained in Chapter 4, five buck-boost inverters are suitable for providing flexible output voltage without the need of large electrolytic capacitors. In this chapter, the grid-connected operation of these inverters will be discussed as well as their control structures and major challenges. The problems of single-phase inverter topologies, such as second order harmonics in the input dc link, and negative-sequence voltage and current in three-phase topologies during unbalanced operation will be discussed, including their ac fault-ride through. The implementation of high-frequency transformer-isolated versions of these buck-boost inverters, to reduce the EMI effect and common mode leakage currents, are presented.

### 5.1 Three-phase differential mode buck-boost inverter

The basic structure of a three-phase differential mode buck-boost inverter is shown in Figure 5.1.


Figure 5.1. Basic structure of a grid-connected three-phase differential buck-boost Assume the grid phase voltages $v_{o a}, v_{o b}$ and $v_{o c}$ are expressed as:

$$
\begin{align*}
& v_{o 1}(t)=V_{m} \sin \omega t \\
& v_{o 2}(t)=V_{m} \sin (\omega t-2 / 3 \pi)  \tag{5.1}\\
& v_{o 3}(t)=V_{m} \sin (\omega t+2 / 3 \pi)
\end{align*}
$$

Each buck-boost converter produces an output phase voltage comprised of a sinusoid plus a dc component. Due to the differential connection of the converters output voltages, the dc components in the output voltages will be decoupled from the inverter load, which is the three-phase grid voltage in this case. The converter voltages $v_{a}, v_{b}$ and $v_{c}$ are expressed as follows:

$$
\begin{align*}
& v_{a}(t)=h_{a} V_{i n} \\
& h_{a}=H_{d c}+H_{a c} \sin (\omega t+\theta)  \tag{5.2}\\
& v_{b}(t)=h_{b} \cdot V_{i n} \\
& h_{b}(t)=H_{d c}+H_{a c} \sin (\omega t-2 / 3 \pi+\theta)  \tag{5.3}\\
& v_{c}(t)=h_{c} \cdot V_{i n} \\
& h_{c}(t)=H_{d c}+H_{a c} \sin (\omega t+2 / 3 \pi+\theta) \tag{5.4}
\end{align*}
$$

where $h$ is the conversion ratio, $\theta$ is the voltage arbitrary phase-shift and $H_{d c}$ and $H_{a c}$ are constants. It has been established in Chapter 4 that all the buck-boost converters under investigation have voltage conversion ratios of the form:

$$
\begin{align*}
& h_{a}=\frac{v_{a}}{V_{\text {in }}}=\frac{\delta_{a}}{1-\delta_{a}}, \\
& h_{b}=\frac{v_{b}}{V_{\text {in }}}=\frac{\delta_{b}}{1-\delta_{b}},  \tag{5.5}\\
& h_{c}=\frac{v_{c}}{V_{\text {in }}}=\frac{\delta_{c}}{1-\delta_{c}},
\end{align*}
$$

The duty ratios can be calculated as

$$
\begin{align*}
& \delta_{a}=\frac{h_{a}}{1+h_{a}}, \\
& \delta_{b}=\frac{h_{b}}{1+h_{b}},  \tag{5.6}\\
& \delta_{c}=\frac{h_{c}}{1+h_{c}},
\end{align*}
$$

The output currents $i_{o a}, i_{o b}$, and $i_{o c}$ are expressed as:

$$
\begin{gather*}
i_{o a}(t)=I_{m} \sin (\omega t+\gamma) \\
i_{o b}(t)=I_{m} \sin (\omega t-2 / 3 \pi+\gamma)  \tag{5.7}\\
i_{o c}(t)=I_{m} \sin (\omega t+2 / 3 \pi+\gamma)
\end{gather*}
$$

Figure 5.2 shows the ideal plots of grid voltages ( $v_{o l}, v_{o 2}$, and $v_{o 3}$ ), conversion ratios ( $h_{a}, h_{b}$, and $h_{c}$ ), converters output voltages ( $v_{a}, v_{b}$, and $v_{c}$ ) and converters duty ratios $\left(\delta_{a}, \delta_{b}\right.$, and $\left.\delta_{c}\right)$.

### 5.1.1 Ćuk based three-phase differential mode buck-boost inverter

As explained in Chapter 4, the inverters derived from the Ćuk converter have the highest efficiency of the inverters with buck-boost voltage transfer functions.


Figure 5.2. Ideal converter operation.


Figure 5.3. Phase A equivalent circuit of grid-connected Ćuk inverter

$$
\begin{gather*}
{\left[\begin{array}{c}
\dot{i_{i n}} \\
\dot{v_{c}} \\
\dot{i_{o}}
\end{array}\right]=\left[\begin{array}{ccc}
\frac{-r_{l}}{L_{l}} & -\frac{l-D}{L_{l}} & 0 \\
\frac{1-D}{C} & 0 & \frac{-D}{C} \\
0 & \frac{D}{L_{2}} & \frac{-r_{2}}{L_{2}}
\end{array}\right]\left[\begin{array}{l}
i_{i n} \\
v_{c} \\
i_{o}
\end{array}\right]+\left[\begin{array}{cc}
\frac{1}{L_{1}} & 0 \\
0 & 0 \\
0 & \frac{-1}{L_{2}}
\end{array}\right]\left[\begin{array}{l}
V_{i n} \\
V_{o}
\end{array}\right]}  \tag{5.8}\\
{\left[\begin{array}{c}
\dot{i_{i n}} \\
\dot{\hat{V}_{c}} \\
\dot{\hat{i}_{o}}
\end{array}\right]=\left[\begin{array}{lll}
\frac{-r_{1}}{L_{l}} & \frac{D_{e}-1}{L_{l}} & 0 \\
\frac{1-D_{e}}{C} & 0 & \frac{-D_{e}}{C} \\
0 & \frac{D_{e}}{L_{2}} & \frac{-r_{2}}{L_{2}}
\end{array}\right]\left[\begin{array}{l}
\tilde{i_{i n}} \\
\tilde{v_{c}} \\
\tilde{i_{o}}
\end{array}\right]+\left[\begin{array}{c}
\frac{V_{\text {in }}}{\left(1-D_{e}\right) L_{l}} \\
\frac{1}{C}\left(I_{o}+I_{i n}\right) \\
\frac{V_{\text {in }}}{\left(1-D_{e}\right) L_{2}}
\end{array}\right][\delta]} \tag{5.9}
\end{gather*}
$$

By replacing the buck-boost converters in Figure 5.1 with bidirectional Ćuk converters, the per-phase circuit of the resultant inverter, shown in Figure 5.3, can be expressed in state-state form as in equations (5.8) and (5.9). In normal balanced operation of the three phase inverter being considered, the dc offset of each phase voltage ( $v_{a}, v_{b}$ and $v_{c}$ ) measured relative to ground will be cancelled in the phase voltages $v_{a o}, v_{b o}$ and $v_{c o}$; thus, the three-phase grid is exposed to pure sinusoidal currents as illustrated by (5.7).

The operation of each Ćuk converter for each sampling period $t_{s}$ is shown in Figure 5.4. Assuming the switching frequency is much higher than the fundamental frequency ( $t_{s} \ll 1 / \mathrm{f}$ ); the relationship between the input and output current ripple ( $\Delta \dot{i}_{\text {in }}$ and $\Delta i_{0}$ ) with $L_{l}$ and $L_{2}$ when $S_{1}$ is on, can be approximated by:

$$
\begin{align*}
V_{\text {in }} & =L_{1} \frac{\Delta I_{\text {in }}}{\Delta t} \\
L_{1} & =\frac{V_{\text {in }} \delta}{\Delta I_{\text {in }} f_{s}} \\
V_{o} & =L_{2} \frac{\Delta I_{o}}{\Delta t}  \tag{5.10}\\
L_{2} & =\frac{V_{o} \delta}{\Delta I_{o} f_{s}}
\end{align*}
$$

Using the same approach and neglecting the small change in $I_{o}$, the ripple of $C$ can be calculated when $S_{2}$ is on, as:

$$
\begin{gather*}
\bar{I}_{o}=C \frac{\Delta V_{c}}{\Delta t^{\prime}}  \tag{5.11}\\
C=\frac{(1-\delta)}{\Delta V_{c} f_{s}} \bar{I}_{o}
\end{gather*}
$$



Figure 5.4. Ćuk converter operation.
where $\bar{I}_{o}$ in (5.11) is the average output current over the sampling period $t_{s}$. From the previous analysis, the highest $\Delta I_{i n}, \Delta I_{o}$ and $\Delta V_{c}$ occur at the largest $\delta$ of each converter. The values of $L_{1}, L_{2}$ and $C$ can be determined for acceptable input and output current ripple, as well as the peak values of the converter rated currents and voltages. Here, $L_{1}=L_{2}=1 \mathrm{mH}$ and $C_{1}=10 \mu \mathrm{~F}$ are chosen based on the rated values in Table 5.1 as well as equations (5.10) and (5.11).

Table 5.1. Rated values of $\dot{C} u k$ inverter

| Parameter | Value |
| :---: | :---: |
| $V_{\text {in }}$ | 50 Vdc |
| $I_{s}$ | 50 A |
| $V_{m}$ | 50 V |
| $I_{L 2}($ peak $)$ | 33.33 A |
| $r_{1}, r_{2}$ | $0.1 \Omega$ |
| $\delta_{\min }$ and $\delta_{\max }$ | 0 and 0.667 |
| $f_{s}$ | 50 kHz |
| $\Delta I_{\text {in }}$ | 0.667 A |
| $\Delta I_{o}$ | 0.667 A |
| $\Delta V_{c}$ | 20 V |

Figure 5.5 shows the MATLAB simulation of the three-phase differential mode Ćuk inverter with the parameters in Table 5.1 and 10 nF optional output shunt capacitors. The expected output voltages at output poles relative to ground ( $V_{a}, V_{b}$ and $V_{c}$ ) are
sinusoidal voltages of magnitude 50 V peak on a 50 V dc bias. The duty ratios of the three $\dot{C} u k$ converters, $\delta_{a}, \delta_{b}$ and $\delta_{c}$ are calculated from $h_{a}, h_{b}$ and $h_{c}$ as explained in equation (5.5) and are shown in Figure 5.5a and b, respectively. However, the output voltages in Figure 5.5c exhibit distortion. From the output currents in Figure 5.5d and their components in the $d-q$ synchronous rotating frame in Figure 5.5e there is a negative sequence $2^{\text {nd }}$ harmonic component, which is equivalent to the $3^{\text {rd }}$ when transformed to the $d-q$ frame, which appears because of the Ćuk non-linear nature.


Figure 5.5. Operation of three-phase differential Cuk inverter.
For the parameters shown in Table 5.1, the poles and zeros of the system are derived from equation (5.9) and plotted in Figure 5.6a in order to study the dynamic
behaviour. The duty ratio is varied from 0.1 to 0.85 . As the duty ratio increases, the non-oscillatory dominant poles along the real axis move toward the origin; thus, the system dynamics become slower. This is verified from the step response in Figure 5.6 b as the system gets slower with increasing duty ratio. Figure 5.6 a shows that at lower duty cycle, typically below $10 \%$, the dominant poles movement towards the imaginary axis, leads to oscillation. To show the meaning of this analysis, a MATLAB simulation is used when the duty ratio is varied to draw a sinusoidal output voltage with a dc offset. The input voltage is set to 50 V . Figure 5.6 c shows the difference between the reference and the actual output voltages because of the variation of dynamics with duty ratio value.

### 5.1.2 Control Design

A control strategy is proposed to deal with the nonlinearity, control the desired output current, and eliminate the predefined distortion. The control structure is shown in Figure 5.7.


(c) Ćuk voltage with time varying duty ratio

Figure 5.6. Frequency and time analysis of Cuk converter.
$V_{d,}, V_{q}$ and $V_{d c}$ are the direct, quadrature, and dc offset components of the output voltage at $V_{a}, V_{b}$ and $V_{c}$. The subscript ${ }^{{ }^{*},}$ refers to a reference value. $K_{p}$ and $K_{i}$ are the proportional and integral gains of the PI controller.


Figure 5.7. Control structure.
In order to simplify the control design, a point at the middle of the trajectory in Figure 5.6 a , where $d=0.5$, is chosen to be an intermediate operating point. Guided by Routh Hurwitz criterion, the poles loci of the closed loop system are plotted in two different ways. In Figure 5.8a, $K_{i}$ is held constant at 0.7 and $K_{p}$ is varied in the range [0.1:0.8]. Similarly, Figure 5.8 b shows $K_{p}$ held constant and $K_{i}$ varied from [0.1:0.8]. From Figure 5.8a, increasing the proportional gain drives the poles toward the right hand side. From Figure 5.8b, the imaginary poles are locked in their loci while the real poles move away from the origin to the left hand side. The gain values are selected by compromising between these two cases. From Figure 5.8a and Figure 5.8b, selecting $K_{p}=0.3$ and $K_{i}=0.4$ provides preliminary acceptable dynamic performance and stability margin from the imaginary axis. The differential threephase Cuk inverter is simulated firstly using MATLAB/SIMULINK with the selected parameters and gain values. Figure 5.9 shows the results for the voltage response. The reference values are set to produce three-phase output voltages of 100 V peak-to-peak with 50 V dc-offset. $V_{d}, V_{q}$ and $V_{o}$ are set to $50 \mathrm{~V}, 0 \mathrm{~V}$ and 50 V respectively, to fulfill the rated values of Table 5.1.

(a) Pole-zero map when $K_{i}$ is held constant at ( 0.7 ) and $K_{p}$ is varied in [0.1:0.8].

(b) Pole-zero map when $K_{p}$ is held constant at (0.1) and $K_{i}$ is varied in [0.1:0.8].

Figure 5.8 Root loci for a fixed $K_{i}$ and a range of $K_{p}$ or vice versa.
The input dc current and its 50 kHz ripple are shown in Figure 5.9e. By decreasing the Ćuk converter parameters ( $L_{1}, L_{2}$ and $C$ ), the trajectory of the poles in Figure 5.6a becomes shorter. Hence, the effect of $\dot{C} u k$ nonlinearity decreases and the $2^{\text {nd }}$ order harmonic decreases in the output currents and voltages. However, the voltage and current ripple and hence, output voltage and current THD increasing. But increasing the converter parameters will affect the size, cost, losses, and system nonlinearity, and will add to control complexity. A solution is proposed in Figure 5.10 where the controller is modified with a band pass filter tuned at the $2{ }^{\text {nd }}$ harmonic, $3^{\text {rd }}$ harmonic within the $d q$ frame, to extract its components in the output voltage. The filter's transfer function is stated in equation (5.12) where $f_{b}$ is the center frequency and $a$ is selected to adjust the filter's band width to cater for a $\pm 1 \%$ frequency variation. The

Bode plot of the band-pass filter is shown in Figure 5.11. A proportional-resonant (PR) controller is inserted to force this component to zero. The values for the PR controller are chosen to be small so as not to affect the main PI loop. Figure 5.12 shows the minor impact of the new PR-controller on the main control loop with gain values $K_{p r}=0.1$ and $K_{r r}=40$.

$$
\begin{equation*}
G_{b p}=\frac{a s}{\frac{1}{\left(2 \pi f_{b}\right)^{2}} s^{2}+a s+1} \tag{5.12}
\end{equation*}
$$


(a) Output voltages at $v_{a}, v_{b}$ and $v_{c}$ and corresponding $d q$ components

(b) Output voltage dc offset

(d) $2^{\text {nd }}$ order harmonic components of three-phase output current

(c) Three-phase output current

(e) Total input current $\mathrm{I}_{\mathrm{s}}$

Figure 5.9. Three-phase differential inverter under PI control in Figure 5.7.


Figure 5.10. Control structure for eliminating the $3^{\text {rd }}$ harmonic in the $d q$ frame $\left(2^{\text {nd }}\right.$ in the stationary frame).


Figure 5.11. Bode plot of band-pass filter with $\mathrm{a}=0.001$ and $f_{b}=150 \mathrm{~Hz}$.
The results are shown in Figure 5.13 where the PR controller is able to suppress the $2^{\text {nd }}$ harmonic components from the voltages and currents. The new voltage conversion ratios $h_{a, b \text { and } c}$ shown in Figure 5.13e are responsible for eliminating the $2^{\text {nd }}$ order harmonic current in Figure 5.13d.


Figure 5.12. Impact of the additional control loop.

(a) Output voltages at $v_{a}, v_{b}$ and $v_{c}$ and corresponding $d q$ components

(b) Output voltage dc offset

(d) $2^{\text {nd }}$ order harmonic components of three-phase output current

(c) Three-phase output current

(e) Total Input current $I_{s}$

Figure 5.13. Three-phase differential inverter under PI+PR control in Figure 5.9.

In order to suppress the input current ripple, the three PWM carrier signals are displaced by $120^{\circ}$ as shown in Figure 5.14a. In this way, the converters input currents, shown in Fig.14b, charge and discharge in different time periods, instead of all being charged and discharged simultaneously. Hence, the high frequency ripple in total input current $I_{s}$ is reduced to $0.6 \%$ peak-to-peak compared with the symmetric PWM signals shown in Figure 5.9e (6\% peak-to-peak). This reduction may alleviate the need for PV output capacitive filtering.


Figure 5.14. Reduced high frequency ripple.

Figure 5.15 shows the prototype of the three-phase differential Ć $u k$ converters and parameters are listed in Table 5.1. In this demonstration, the control and modulation of the Ćuk inverter being assessed is programmed using a Texas Instrument DSP TMS320F280335.The practical results are used to validate the presented Ćuk inverter and the mathematical analysis presented. The passive parameters of the Ćuk inverter are: $\mathrm{L}_{1}=1.014 \mathrm{mH}, \mathrm{L}_{2}=1.037 \mathrm{mH}$, and $\mathrm{C}=10.4 \mu \mathrm{~F}$. The switches $\mathrm{S}_{1}$ and $\mathrm{S}_{2}$ are realized by two IGBs, type IRGP4062DPBF (with built-in freewheel diodes $D_{1}$ and $\mathrm{D}_{2}$ ). Figure 5.16 shows the proposed system operation when the system is controlled in closed loop as in Figure 5.7. The references are set to constitute three-
phase output voltages of 100 V peak-to-peak with a 50 V dc-offset. $V_{d}, V_{q}$ and $V_{o}$ are set to $50 \mathrm{~V}, 0 \mathrm{~V}$ and 50 V respectively.


Figure 5.15. Experimental prototype
As mentioned, the Ć $u k$ three-phase voltage and load three-phase current in Figure 5.16a, b appear distorted. The input currents $i_{\text {ina }}, i_{i n b}$ and $i_{\text {inc }}$ are shown in Figure 5.16 c with current ripple restricted to acceptable limits, in Table 5.1. The $2^{\text {nd }}$ order harmonic current components are measured with the DSP and plotted in Figure 5.16e. The corresponding duty ratios are shown in Figure 5.16e and the results are in line with the simulations in Figure 5.9.
The additional PR control loop, to eliminate the $2^{\text {nd }}$ order components in the output currents, is inserted and its effect is shown in Figure 5.17 where the Cuk three-phase voltage $2^{\text {nd }}$ order distortion is reduced. Figure 5.17 c shows a significant reduction of the $2^{\text {nd }}$ order output current component because of the additional control loop. The modified duty ratios are shown in Figure 5.17d. The presented experimental results verify the simulations in Figure 5.13. In order to reduce the input current $\left(I_{s}\right)$ ripple, the displaced carrier signals described in Figure 5.14a are generated within the DSP, instead of symmetrical PWM. The effect on the input current ripple is shown in Figure 5.18 , where the high frequency ripple is reduced by $90 \%$. Then, Figure 5.19
shows the output voltage with respect to the output current of phase ' $a$ ' when the system is connected to the grid via a 1:5 step-up transformer and operated at unity power factor $(\gamma=0)$. Figure 5.20 shows the operation at 0.95 lagging power factor.
 of three-phase output current

Figure 5.16. Proposed system under PI control in Figure 5.7.


Figure 5.17. Proposed system under the PI+PR control in Figure 5.10.


5A/div-5ms/div
Figure 5.18. Total input dc current $\left(i_{s}\right)$.

$25 \mathrm{~V} / \mathrm{div}-10 \mathrm{~A} / \mathrm{div}-5 \mathrm{~ms} /$ div
Figure 5.19. Grid voltage and current (unity power factor).

$25 \mathrm{~V} / \mathrm{div}-10 \mathrm{~A} / \mathrm{div}-5 \mathrm{~ms} /$ div
Figure 5.20. Grid voltage and current ( 0.95 power factor).

### 5.1.3 Unbalanced and dc currents compensation

Inverter dc current injection can cause saturation problems in the line transformer. This problem is not so significant if the inverter is connected to the grid through lowfrequency isolation transformers. However, for the single-stage transformer-less dc/ac inverters, this issue should be considered. As mentioned in Chapter 2, IEC 61727 and IEEE 1574 restrict the dc current injection to $1 \%$ of the RMS current. There is no maximum trip time condition as long as the specified limit is not exceeded. For this case, the controller in Figure 5.21 is implemented in order to eliminate the dc component from the output phase currents (the output currents may contain a dc component if the dc offsets of the three-phase output voltages generated by the inverter are not identical, as with unbalanced operation). $I_{o a}, I_{o b}$, and $I_{o c}$ are the dc components in the output currents $i_{o a}, i_{o b}$, and $i_{o c}$. The band pass filters are tuned at the fundamental frequency ( 50 Hz ) to supress the sinusoidal three-phase current values. The remaining dc components are fed to PI controllers with zero reference current. The new converters duty ratios $\delta_{a_{-} n e w,} \delta_{b_{-} n e w,}$ and $\delta_{c_{-} n e w}$ replace the duty ratios from the main controller in Figure 5.10.

The PI controller values are chosen small so as not to affect the main control loop in Figure 5.10. Figure 5.22 shows the ability for the Ćuk differential three-phase inverter to compensate the output dc currents which appear due to sudden unbalance in circuit conditions ( $80 \%$ voltage dip in grid voltages occurring at $t_{f}$ ).


Figure 5.21. Control structure with eliminating the dc output current components.

(a) Output currents $i_{o c}, i_{o b}$ and $i_{o c}$

(b) FFT showing the THD and DC component of the output current $i_{o a}$ in steady Figure 5.22. Performance of three-phase differential Cuk inverter under load

### 5.1.4 Supplying Reactive Power to the Grid

The three-phase inverter can supply reactive power to the grid by varying the phase angle between the phase current $i_{o a}$ and the grid voltage $v_{o a}$ from 0 to $90^{\circ}$. Figure 5.23 shows the inverter voltages and currents when phase angle $\phi$ is approaching $90^{\circ}$. In this case, the inverter supplies nearly pure reactive power of 1.5 kVAr to the grid, plus total active power of 150 W , including inverter semiconductor loss .


Figure 5.23. Grid voltage and current (supplying reactive power).

### 5.1.5 Sliding Mode Controlled three-phase differential Ćuk inverter

For some applications, the differential-mode buck boost inverters may require a robust, efficient and fast control method. But because each phase converter produces ac voltage superimposed on dc bias, the deviation of the output dc voltage component may cause output dc current components which are undesirable in the inverter systems. Because the proposed systems are the high order, Variable Structure Control [5.18] (VSR) is an attractive solution. Sliding Mode Control (SMC) [5.18], which belongs to a family of VSR techniques, will be applied to the differential-mode buck-boost inverters. The mathematical analysis will be presented for the Cuk based system. Based on this approach, the final block diagrams and control equations will be stated for the other inverter types. SMC forces the system
states to track predefined trajectories which lie on the desired reference values [5.18]. SMC fast dynamics and robustness to system parameters and states variations are important features. The control structure aims to drive the inverter's output currents $i_{o l,} i_{o 2}$, and $i_{o 3}$ on specified surfaces. It is reported in [5.19] that the Cuk converter is not able to be controlled directly from the output current and only the input current can be directly controlled. This can be understood from the effect of the two switches $S_{1}$ and $S_{2}$ on the converters currents. For Ćuk, bB1D, bB2D, bB1F, and SEPIC converters, $S_{I}$ affects the input current $i_{i n}$ directly while $S_{2}$ has no direct effect on $i_{o}$. For this reason, the reference value of the converter output current has to be written in terms of $i_{i n}$. The sliding surface ' $S$ ' is chosen as a linear combination of the errors as:

$$
\begin{gather*}
S=\alpha_{1} e_{1}+\alpha_{2} e_{2}+\alpha_{3} e_{3}  \tag{5.13}\\
\dot{S}=\alpha_{1} \dot{e}_{1}+\alpha_{2} \dot{e}_{2}+\alpha_{3} \dot{e}_{3}=0 \tag{5.14}
\end{gather*}
$$

where $\alpha_{1}, \alpha_{2}$ and $\alpha_{3}$ are constants and $e_{1}, e_{2}$ and $e_{3}$ are the controller error signals described by:

$$
\begin{gather*}
e_{1}=i_{i n}^{*}-i_{i n} \\
e_{2}=i_{o}^{*}-i_{o}  \tag{5.15}\\
e_{3}=\int\left(e_{1}+e_{2}\right) d t \\
\dot{e}_{1}=\frac{d i_{i n}^{*}}{d t}-\frac{d i_{i n}}{d t} \\
\dot{e}_{2}=\frac{d i_{o}^{*}}{d t}-\frac{d i_{o}}{d t}  \tag{5.16}\\
\dot{e}_{3}=e_{1}+e_{2}
\end{gather*}
$$

For the pre-stated controllability issues, the reference input current $i^{*}$ in is re-written as:

$$
\begin{equation*}
i_{i n}^{*}=K\left(i_{o}^{*}-i_{o}\right) \tag{5.17}
\end{equation*}
$$

where, $K$ is a control constant. If the frequency of $i^{*}{ }_{o}$ is assumed to be small compared to the switching frequency, $i^{*}{ }_{o}$ can be considered constant during one switching period and its derivative can be considered as zero. Substituting (5.8) and (5.17) into (5.16), yields:

$$
\begin{gather*}
\dot{e}_{1}=\frac{-l}{L_{1}} V_{i n}+i_{i n} \frac{r_{i n}}{L_{1}}+v_{c}\left(-\frac{K \delta}{L_{2}}+\frac{(l-\delta)}{L_{i l}}\right)+i_{o} \frac{K r_{2}}{L_{2}}+v_{o} \frac{K}{L_{2}} \\
\dot{e}_{2}=-\frac{\delta}{L_{2}} v_{c}+i_{o} \frac{r_{o}}{L_{2}}+v_{o} \frac{l}{L_{2}}  \tag{5.18}\\
\dot{e}_{3}=(K+1)\left(i_{o}^{*}-i_{o}\right)-i_{i n}
\end{gather*}
$$

Substituting (5.18) into (5.14) and solving for $\delta$ gives:

$$
\begin{gather*}
u_{e q}=\delta=\frac{-V_{i n}+i_{i n}\left(r_{1}-K_{1}\right)+v_{c}+i_{o}\left(K_{2} r_{2}\right)+v_{o} K_{2}+K_{3}\left(i_{o}^{*}-i_{o}\right)}{v_{c}\left(1+K_{2}\right)} \\
K_{1}=\frac{\alpha_{3}}{\alpha_{1}} L_{1}, \quad K_{2}=\frac{K \alpha_{1}+\alpha_{2}}{L_{2} \alpha_{1}} L_{i n}, \quad \text { and } K_{3}=\frac{(K+1) \alpha_{3}}{\alpha_{1}} L_{1} \tag{5.19}
\end{gather*}
$$

The resultant sliding mode controller from (5.19) is shown in Figure 5.24.


Figure 5.24. Sliding mode controller for the Cuk converter.
The controller gains $K_{1}, K_{2}$ and $K_{3}$ are responsible for steady state regulation, oscillation and settling time. The designer has three degrees of freedom to choose the values of gains. However, it must be confirmed that these values will ensure tracking the predefined trajectory. This is confirmed by fulfilling two existence conditions [20]:

Condition 1 (Lyapunov): when $S>0$ then $\dot{S}<0$ and $u=1$
From (5.19):
$-V_{\text {in }}+i_{\text {in }}\left(r_{1}-K_{1}\right)+v_{c}+i_{o}\left(K_{2} r_{2}\right)+v_{o} K_{2}+K_{3}\left(i^{*}{ }_{o}-i_{o}\right)<v_{c}\left(K_{2}+1\right)$
This implies that:

$$
\begin{align*}
& -V_{\text {in }}(\min )+r_{1} i_{\text {in }}(\max )-K_{1} i_{\text {in }}(\min )-v_{c}(\min ) K_{2}+ \\
& K_{2} r_{2} i_{o}(\max )+K_{2} v_{o}(\max )+K_{3}\left(i^{*}{ }_{o}-i_{o}\right)<0 \tag{5.21}
\end{align*}
$$

Condition 2: when $S<0$ then $\dot{S}>0$ and $u=0$
From (5.19):

$$
\begin{equation*}
-V_{i n}+i_{i n}\left(r_{1}-K_{l}\right)+v_{c}+i_{o}\left(K_{2} r_{2}\right)+v_{o} K_{2}+K_{3}\left(i_{o}^{*}-i_{o}\right)>0 \tag{5.22}
\end{equation*}
$$

This implies that:

$$
\begin{align*}
& -V_{i n}(\max )+r_{1} i_{\text {in }}(\min )-K_{1} i_{\text {in }}(\max )+v_{c}(\min )+K_{2} r_{2} i_{o}(\min )+ \\
& K_{2} v_{o}(\min )+K_{3}\left(i_{o}^{*}-i_{o}\right)>0 \tag{5.23}
\end{align*}
$$

Equations (5.22) and (5.23) are referred to as existence equations. The sliding mode controllers for the other inverters can be similarly obtained. Their control equations as well as block diagrams and existence equations are listed in Figure 5.25 and Table 5.2. The control parameters in Table 5.1 and Table 5.2 are used MATLAB simulations, where the results obtained from different inverters are displayed in Figure 5.26.

Because of the fast dynamics of sliding mode controllers, it is expected that they have better performance against the unbalance conditions, than the linear control strategies discussed previously. Figure 5.27 shows the experimental results of unbalance conditions for the grid connected differential mode three-phase Ćuk inverter. These results show that the controller is able to reproduce the desire output currents much faster than with PR controller in Figure 5.22.
The same control scheme can be used to reverse the energy direction to flow from the ac side (ac grid) to dc side (passive load or active dc source as in a dc micro-grid) for rectifier operation, see Figure 5.28. This system may be beneficial to electrical vehicle (EV) systems without the necessity of a large electrolytic output capacitor. Figure 5.29 shows the rectifier voltages and currents with an output impedance of 14 $\Omega$.


Figure 5.25. Block diagrams of sliding mode controllers for different buck-boost

Table 5.2 Control and Existence equations

| bB1D | $\begin{aligned} u_{e q}= & \frac{V_{i n}\left(K_{2}-1\right)+i_{i n}\left(r_{1}-K_{1}\right)-v_{c}\left(K_{2}-1\right)+i_{o}\left(K_{2} r_{2}\right)+v_{o} K_{2}+K_{3}\left(i_{o}^{*}-i_{o}\right)}{v_{c}} \\ & K_{2} V_{\text {in }}(\min )-V_{\text {in }}(\max )+r_{1} i_{i n}(\min )-K_{1} i_{\text {in }}(\max )- \\ & K_{2} v_{c}(\max )+v_{c}(\min )+K_{2} r_{2} i_{o}(\min )+K_{2} v_{o}(\min )+K_{3}\left(i_{o}^{*}-i_{o}\right)>0 \\ & K_{2} V_{\text {in }}(\max )-V_{i n}(\min )+r_{1} i_{\text {in }}(\max )-K_{l} i_{\text {in }}(\min )- \\ & K_{2} v_{c}(\min )+K_{2} r_{2} i_{o}(\max )+K_{2} v_{o}(\max )+K_{3}\left(i^{*}-i_{o}\right)<0 \end{aligned}$ |
| :---: | :---: |
| bB2D | $\begin{aligned} &\left.u_{\text {eq }}=\frac{V_{i n}( }{} K_{2}-1\right)+i_{i n}\left(r_{\text {in }}+r_{o}-K_{1}\right)-v_{c}\left(K_{2}-1\right)+i_{o}\left(K_{2} r_{o}\right)+v_{o} K_{2}+K_{3}\left(i_{o}^{*}-i_{o}\right) \\ & v_{c}+v_{o} \\ & K_{2} V_{\text {in }}(\min )-V_{\text {in }}(\max )+\left(r_{1}+r_{2}\right) i_{\text {in }}(\min )-K_{l} i_{\text {in }}(\max ) \\ &-K_{2} v_{c}(\max )+v_{c}(\min )+K_{2} r_{2} i_{o}(\min ) \\ &+K_{2} v_{o}(\min )+K_{3}\left(i^{*}{ }_{o}-i_{o}\right)>0 \\ & K_{2} V_{\text {in }}(\max )-V_{\text {in }}(\min )+\left(r_{1}+r_{2}\right) i_{i n}(\max )-K_{l} i_{\text {in }}(\min ) \\ &-K_{2} v_{c}(\min )+K_{2} r_{2} i_{o}(\max )+ \\ & K_{2} v_{o}(\max )-v_{o}(\min )+K_{3}\left(i^{*}{ }_{o}-i_{o}\right)<0 \end{aligned}$ |
| bB1F | $\begin{aligned} & u_{e q}=\frac{-V_{i n}+i_{i n}\left(r_{1}-K_{1}\right)+v_{c}+i_{o}\left(K_{2} r_{2}\right)+v_{o} K_{2}+K_{3}\left(i_{o}^{*}-i_{o}\right)}{K_{2}\left(v_{c}+v_{o}\right)} \\ & \quad-V_{\text {in }}(\max )+r_{1} i_{i n}(\min )-K_{1} i_{i_{i n}}(\max )+v_{c}(\min ) \\ & \quad+K_{2} r_{2} i_{o}(\min )+K_{2} v_{o}(\min )+K_{3}\left(i_{o}^{*}-i_{o}\right)>0 \\ & \quad-V_{\text {in }}(\min )+r_{1} i_{\text {in }}(\max )-K_{l} i_{i n}(\min )-K_{2} v_{c}(\min )-v_{c}(\max ) \\ & \\ & \quad+K_{2} r_{2} i_{o}(\max )+K_{3}\left(i_{o}^{*}-i_{o}\right)<0 \end{aligned}$ |
| SEPIC | $\begin{gathered} u_{e q}=\frac{-V_{\text {in }}+i_{\text {in }}\left(r_{1}-K_{1}\right)+v_{c}-i_{o}\left(K_{2} r_{2}\right)+v_{o}+K_{3}\left(i_{o}^{*}-i_{o}\right)}{v_{c}+v_{o}} \\ -V_{\text {in }}(\max )+r_{l} i_{\text {in }}(\min )-K_{l} i_{\text {Lin }}(\max )+v_{c}(\min ) \\ -K_{2} r_{2} i_{o}(\max )+v_{o}(\min )+K_{3}\left(i_{o}^{*}-i_{o}\right)>0 \\ -V_{\text {in }}(\text { min })+r_{1} i_{\text {in }}(\max )-K_{l} i_{\text {in }}(\text { min }) \\ -K_{2} r_{2} i_{o}(\text { min })+K_{3}\left(i_{o}^{*}-i_{o}\right)<0 \end{gathered}$ |



Figure 5.26. MATLAB simulations of the five differential-mode three-phase


Figure 5.27. Performance of three-phase differential Ćuk inverter under load unbalance (SMC).


Figure 5.28. Basic structure of grid-connected three-phase differential buck-boost


Figure 5.29. Ćuk based three-phase differential rectifier.

### 5.2 Single-phase differential-mode buck-boost inverters

Single-stage inverters have gained attention. In [5.21], a comparison between different single-stage PV inverter topologies is presented. However, grid-connected single-phase buck-boost inverters with continuous input current are not considered in the literature. The basic structure of the single-phase buck-boost inverter is shown in Figure 5.30.

### 5.2.1 Operation Analysis

The input voltage dc source is connected to two bidirectional buck-boost converters. Most of the buck-boost converters produce an output voltage which has different polarity to the input voltage. Each converter produces unipolar voltage as:

$$
\begin{align*}
& v_{o a}(t)=-h_{a} V_{i n} \\
& h_{a}=H_{d c}+H_{a c} \sin \omega t  \tag{5.24}\\
& v_{o a}(t)=-\left[1 / 2 V_{o}+1 / 2 V_{o} \sin (\omega t)\right]
\end{align*}
$$

$$
\begin{gathered}
v_{o b}(t)=-h_{b} \cdot V_{i n} \\
h_{b}(t)=H_{d c}+H_{a c} \sin (\omega t-\pi) \\
v_{o b}(t)=-\left[1 / 2 V_{o}+1 / 2 V_{o} \sin (\omega t-\pi)\right]
\end{gathered}
$$

The output voltage $v_{\text {out }}$ and current $i_{\text {out }}$ are:

$$
\begin{align*}
& v_{\text {out }}(t)=v_{o b}-v_{o a}=V_{o} \sin \omega t \\
& i_{\text {out }}(t)=I_{o} \sin (\omega t+\gamma) \tag{5.25}
\end{align*}
$$



Figure 5.30. Basic structure of a differential-mode buck-boost inverter.
The duty ratio of the converters $\delta$ is:

$$
\begin{equation*}
\delta=\frac{t_{o n}}{t_{s}} \tag{5.26}
\end{equation*}
$$

The transfer function between the output and the input voltages is:

$$
\begin{gather*}
h=\frac{v_{o}}{V_{\text {in }}}=\frac{\delta}{1-\delta}=\frac{i_{\text {in }}}{i_{o}}  \tag{5.27}\\
\delta_{a}(t)=\frac{h_{a}}{h_{a}+1} \text { and } \delta_{b}(t)=\frac{h_{b}}{h_{b}+1} \tag{5.28}
\end{gather*}
$$

The same control schemes mentioned previously can be used for the single-phase buck-boost inverters. Figure 5.31 shows the simulation results of the five singlephase inverters with the sliding mode controllers in Figure 5.25.


Figure 5.31. MATLAB simulations of the five differential-mode inverters.

All buck-boost converters suffer from high voltage stresses, which must be analysed. The five possible differential-mode buck-boost inverters are discussed and compared in terms of: 1) overall efficiency, 2) input current ripple and 3) switch and diode currents and voltages. To avoid prolongation, the mathematical analysis for only the Cuk converter will be presented in detail, while the final conclusions for the remaining converters will be mentioned briefly.

### 5.2.1.1 Losses and Efficiency

Two loss sources will be considered. The first is the copper $\left(I^{2} R\right)$ loss in the input and output inductors and the second is switches losses. Consequently, the values of the root mean square (rms) currents in the inductors as well as the average current in the diodes are derived. If the Cuk converter is used in the configuration in Figure 5.30, the instantaneous input current $\left(i_{\text {ina }}\right)$ can be written as:

$$
\begin{gather*}
\frac{i_{\text {ina }}(t)}{i_{\text {out }}(t)}=\frac{v_{o}}{V_{\text {in }}}=\frac{\delta}{1-\delta} \\
i_{\text {ina }}(t)=\frac{\delta}{1-\delta} i_{\text {out }} \\
i_{\text {ina }}(t)=1 / 2\left[\frac{V_{o}}{V_{\text {in }}}+\frac{V_{o}}{V_{\text {in }}} \sin \omega t\right] I_{o} \sin (\omega t+\gamma)  \tag{5.29}\\
i_{\text {ina }}(t)=\frac{V_{o} I_{o}}{2 V_{\text {in }}}\{1 / 2 \cos \gamma+1 / 2 \cos (2 \omega t+\gamma+\pi)+\sin (\omega t+\gamma)\}
\end{gather*}
$$

The input current consists of dc, fundamental and $2^{\text {nd }}$ order components.

$$
\begin{align*}
& i_{\text {ina }}(t)=I_{\text {in_dc }}+I_{\text {in_fund }} \sin (\omega \mathrm{t}+\gamma)+I_{\text {in_ } 2 n d} \cos (2 \omega \mathrm{t}+\gamma+\pi) \\
& I_{\text {in_ } d c}=1 / 4 \frac{V_{o} I_{o}}{V_{\text {in }}} \cos \gamma \\
& I_{\text {in } n_{-} \text {fund }}=1 / 2 \frac{V_{o} I_{o}}{V_{\text {in }}}  \tag{5.30}\\
& I_{\text {in } n_{-} 2 n d}=1 / 4 \frac{V_{o} I_{o}}{V_{\text {in }}}
\end{align*}
$$

If the parasitic resistances of the inductors ( $L_{1}$ and $L_{2}$ ) are assumed as $r_{1}$ and $r_{2}$, the copper losses are:

$$
\begin{align*}
& \left.P_{\text {loss_in }=\left(I_{\text {in_ }} d c^{2}+1 / 2 I_{\text {in_fund }}{ }^{2}+1 / 2 I_{\text {in_2 }}\right. \text { nd }}{ }^{2}\right) r_{2} \\
& P_{\text {loss_out }}=1 / 2 I_{o}^{2} r_{2} \tag{5.31}
\end{align*}
$$

To calculate the average currents through the devices, the on and off states are shown in Figure 5.32. During the + ve half cycle of the output current, diode $D_{2}$ is reverse bias during $t_{o n}$ and the sum of the input and output currents passes through $S_{1}$. During $t_{o f f}$, the sum of the currents passes through $D_{2}$. The operation is reversed during the ve half cycle of the output current. This means that during $t_{o n}$ the sum of the currents passes through $D_{l}$ while passing through $S_{2}$ during $t_{\text {off }}$.

(a) Converter currents during $t_{o n}(+v e$ half cycle)

(c) Converter currents during $t_{o n}$ (-ve half cycle)

(b) currents during $t_{\text {off }}(+v e$ half cycle $)$

(d) currents during $t_{\text {off }}$ (-ve half cycle)

Figure 5.32 Cuk converter during $t_{o n}$ and $t_{\text {off }}$ periods.
Accordingly, during the positive half cycle, the average current through $D_{2}$ is:

$$
\begin{align*}
& i_{D 2}=(1-\delta)\left[i_{\text {in }}+i_{\text {out }}\right] \\
& i_{D 2}=(1-\delta)\left[\frac{\delta}{1-\delta} i_{\text {out }}+i_{\text {out }}\right] \\
& \bar{i}_{D 2}=\bar{i}_{\text {out }}  \tag{5.32}\\
& \bar{i}_{D 2}=\frac{I_{o}}{\pi}
\end{align*}
$$

Similarly, the average current through $D_{l}$ during the negative half cycle is:

$$
\begin{align*}
& i_{D 1}=\delta\left[i_{\text {in }}+i_{\text {out }}\right] \\
& i_{D 1}=\delta\left[\frac{\delta}{1-\delta} i_{\text {out }}+i_{\text {out }}\right]=\frac{\delta}{1-\delta} i_{\text {out }}  \tag{5.33}\\
& \bar{i}_{D 1}=\bar{i}_{\text {in }}
\end{align*}
$$

As illustrated in (5.30), the input current consists of dc, fundamental and $2^{\text {nd }}$ order harmonic components. Calculating over one half cycle of the fundamental current, the average of the $2^{\text {nd }}$ order current is zero and the average current $\bar{i}_{i n}$ can be written as:

$$
\begin{equation*}
\bar{i}_{D 1}=\frac{I_{\text {in_fund }}}{\pi}-1 / 2 I_{i n_{-} d c} \tag{5.34}
\end{equation*}
$$

Switches power losses in a single Ćuk converter over one complete cycle can be approximated as:

$$
P_{D}=V_{D F} \bar{i}_{D 1}+R_{o n} I_{r m s}^{2}
$$

where

$$
\begin{equation*}
I_{r m s}=\sqrt{\frac{3 \delta_{a v} I_{o}^{2}}{2}\left(\frac{H_{d c}^{2}}{4}+\frac{3 H_{a c}^{2}}{16}\right)}, \quad \delta_{a v}=\frac{1.3 H_{d c}}{H_{d c}+H_{a c}+1} \tag{5.35}
\end{equation*}
$$

where $V_{D F}$ is the diode threshold voltage drop and $R_{o n}$ is the internal resistance of the device.

The total power loss of the inverter is:

$$
\begin{equation*}
P_{\text {total }}=2\left[P_{\text {loss_in }^{2}}+P_{\text {loss_out }}+P_{D}\right] \tag{5.36}
\end{equation*}
$$

The efficiency of the inverter is:

$$
\begin{equation*}
\eta=\frac{V_{o} I_{o}}{V_{o} I_{o}+P_{\text {total }}} \times 100 \tag{5.37}
\end{equation*}
$$

Using the same approach, the main loss equations for the five inverters are shown in Table 5.4. Figure 5.33 shows the efficiency plot for the five inverters at different operating points. This plot shows that the Ćuk and SEPIC inverters have the highest efficiency; while, bB1D and bB1F have better efficiency than bB2D when the input voltage is high. bB 2 D is better than bB 1 D and bB 1 F when the input voltage is low. Generally, the efficiency of all inverters drops as the input voltage decreases.

Table 5.3. Parasitic Component Values and circuit conditions

| Parameter | Value |
| :---: | :---: |
| $P_{\text {rated }}$ | 2.5 kW |
| $f_{s}=1 / t_{s}$ | 50 kHz |
| $L_{l}$ | $1 \mathrm{mH}, 25 \mathrm{~A}$ |
| $r_{l}$ | $80 \mathrm{~m} \Omega$ |
| $r_{2}$ | $80 \mathrm{~m} \Omega$ |
| $V_{i n}$ | 100 V |
| $V_{o}$ | 200 V |
| $\gamma$ | $0^{\circ}$ |
| $V_{D F}$ | 2 V |
| $C$ | $20 \mu \mathrm{~F}$ |
| $C$ (for SEPIC and $b$ B1F $)$ | $20 \mu \mathrm{~F}$ |



Figure 5.33 Inverter efficiency versus output current for different input dc voltages

$$
\left(\mathrm{V}_{\mathrm{o}}=200 \mathrm{~V}\right)
$$

### 5.2.1.2 Input current ripple

Input current ripple is the maximum change of the instantaneous current around its average value. For PV and fuel cell applications, the input current ripple can lead to suboptimal operation due to harmonics and power loss (due to missing the global maximum power point on the PV optimal curve); thus, the ripple has to be reduced. Generally, the ripple is inversely proportional to the size of the passive elements in the inverters. However, using large passive devices is not desirable, because of the cost, weight and size issues. The input current ripple is not constant and changes along the current cycle. The maximum ripple current is calculated at the average current peak values, which generally occur at the peak of the converter's duty ratio.

Table 5.4. Core losses in different topologies

| Topology | Copper losses (xr) |  |
| :---: | :---: | :---: |
|  | $L_{I}$ | $L_{2}$ |
| Cuk | $\frac{3 V_{o}^{2} I_{o}^{2}}{16 V_{i n}^{2}}$ | $\frac{I_{o}^{2}}{2}$ |
| bB1D | $\frac{3 V_{o}^{2} I_{o}^{2}}{16 V_{i n}^{2}}$ | $\frac{I_{o}^{2}}{2}$ |
| bB2D | $\frac{3 V_{o}^{2} I_{o}^{2}}{16 V_{i n}^{2}}$ | $\frac{V_{o}^{2} I_{o}^{2}}{8 V_{i n}^{2}}+I_{o}^{2}\left(\frac{V_{o}}{2 V_{i n}}+1\right)$ |
| bB1F | $\frac{V_{o}^{2} I_{o}^{2}}{8 V_{i n}^{2}}+I_{o}^{2}\left(\frac{V_{o}}{2 V_{i n}}+1\right)$ | $\frac{I_{o}^{2}}{2}$ |
| SEPIC | $\frac{3 V_{o}^{2} I_{o}^{2}}{16 V_{i n}^{2}}$ | $\frac{I_{o}^{2}}{2}$ |

For the Cuk converter as an example, the maximum input ripple current can be calculated as:

$$
\begin{align*}
& V_{o}=\frac{\delta_{\max }}{1-\delta_{\max }} V_{\text {in }} \\
& \delta_{\max }=\frac{V_{o}}{V_{o}+V_{i n}}  \tag{5.38}\\
& \Delta I_{\text {in }}(\max )=\left(\frac{V_{o} V_{i n}}{V_{o}+V_{i n}}\right) \frac{t_{s}}{L_{i n}}
\end{align*}
$$

Figure 5.34. Cuk converter instantaneous operation.

Table 5.5 summarize the maximum ripple current for the five inverters. To compare the different inverters, the input current ripple is simulated and shown in Figure 5.35 using the parameters in Table 5.3. The Cuk, SEPIC and bB2D converters have the same input current ripple versus input and output voltages. Both bB1D and bB1F have the same input current ripple versus output currents and voltage. An important advantage is the ripple contents in bB1D and bB1F are much better than the Cuk, SEPIC and bB2D.

Table 5.5. Maximum current ripple

| Topology | Max Input Current ripple |
| :---: | :---: |
| Cuk | $\frac{V_{o} V_{i n} t_{s}}{L_{i n}\left(V_{o}+V_{i n}\right)}$ |
| bB1D | $\frac{V_{o} V_{i n} t_{s}}{L_{i n}\left(V_{o}+V_{i n}\right)}$ |
| bB2D | $\frac{I_{o} t_{s}^{2}}{L_{i n} C}\left(\frac{V_{o} V_{i n}\left(V_{o}+V_{i n}-V_{o} V_{i n}\right)^{2}}{\left(V_{o}+V_{i n}\right)^{3}}\right.$ |
| bB1F | $\frac{V_{o} V_{i n} t_{s}}{L_{i n}\left(V_{o}+V_{i n}\right)}$ |
| SEPIC | $\frac{I_{o} t_{s}^{2}}{L_{i n} C}\left(\frac{V_{o} V_{i n}\left(V_{o}+V_{i n}-V_{o} V_{i n}\right)^{2}}{\left(V_{o}+V_{i n}\right)^{3}}\right.$ |



Figure $5.35 \Delta I_{\text {in }}$ in: (a) Cuk, SEPIC, bB2D and (b) bB1D, bB1F.

### 5.2.1.3 Device average voltages and currents

Device average voltage can be calculated from the converter on and off periods. For the Cuk converter as an example, device average voltage can be deduced from Figure 5.32 as follows:
i. During $t_{o n}$

$$
\begin{align*}
& v_{D 2}(\mathrm{t})=\delta^{*} v_{c}(t) \\
& v_{c}(t)=\frac{1}{1-\delta} V_{i n} \\
& v_{D 2}(\mathrm{t})=\frac{\delta}{1-\delta} * V_{i n}=v_{o}(t)  \tag{5.39}\\
& \overline{V_{D 2}}=\frac{2 V_{o}}{\pi} \\
& i_{S 1}(\mathrm{t})=\delta^{*}\left(i_{i n}(t)+i_{o}(t)\right) \\
& i_{S 1}(\mathrm{t})=\delta^{*}\left(\frac{\delta}{1-\delta} i_{o}(t)+i_{o}(t)\right) \\
& i_{S 1}(\mathrm{t})=i_{i n}(t)  \tag{5.40}\\
& \overline{I_{S 1}}=\frac{V_{o} I_{o}}{2 \pi V_{i n}}-\frac{V_{o} I_{o}}{8 V_{i n}}
\end{align*}
$$

ii. During $t_{o f f}$

$$
\begin{gather*}
\overline{v_{D 1}(\mathrm{t})}=(1-\delta) * v_{c}(t) \\
V_{D 1}=V_{\text {in }}  \tag{5.41}\\
i_{S 2}(\mathrm{t})=(1-\delta) *\left(i_{i n}(t)+i_{o}(t)\right) \\
i_{S 2}(\mathrm{t})=(1-\delta) *\left(\frac{\delta}{1-\delta} i_{o}(t)+i_{o}(t)\right) \\
i_{S 2}(\mathrm{t})=i_{o}(t)  \tag{5.4}\\
\overline{I_{S 2}}=\frac{I_{o}}{\pi}
\end{gather*}
$$

Table 5.6 shows the average voltages and currents for the other converters. From the devices ratings perspective, there is no point comparing the different buck-boost topologies, as they all have the same performance.

Table 5.6. Switches Average voltages and current

| Topology | $S_{1}$ and $D_{1}$ Average |  | $S_{2}$ and $D_{2}$ Average |  |
| :---: | :---: | :---: | :---: | :---: |
|  | Voltage | Current | Voltage | Current |
| Cuk |  |  |  |  |
| bB1D |  |  |  |  |
| bB2D | $V_{\text {in }}$ | $\frac{V_{o} I_{o}}{2 \pi V_{i n}}-\frac{V_{o} I_{o}}{8 V_{i n}}$ | $\frac{2 V_{o}}{\pi}$ | $\frac{I_{o}}{\pi}$ |
| bB1F |  |  |  |  |
| SEPIC |  |  |  |  |

### 5.2.2 DC side Harmonic Filtering

As stated previously, differentially-mode inverters have non-linear transfer functions and draw oscillating power, with the second-order current harmonic (superimposed on an average dc current) in the dc link (the dc side), independent of the power flow direction.

The conventional VSI and CSI use low pass filtering on the dc side to attenuate the second order component and its sidebands. The cut off frequency of a suitable filter has to be well below $100 / 120 \mathrm{~Hz}$, necessitating large valued and sized passive components. In low power applications like small-scale PV systems for micro-grids, filtering is required at the dc side because the harmonic current components will significantly affect PV MPPT operation. DC-side harmonic elimination for deferentially connected buck-boost single-phase inverters can be categorized as either passive or active elimination methods.

### 5.2.2.1 Passive LC 100/120 Hz filtering

In the differential-mode inverters, only the second-order harmonic appears on the dc side, independent of power flow direction, so notch (in series) or band-pass (in shunt) filtering at that frequency can be used. The necessary notch filter components are smaller and cheaper than its equivalent band-pass filtering approach.

A conventional solution for second-order component $(100 / 120 \mathrm{~Hz})$ attenuation, is a second order LC series notch filter, consisting a parallel inductor $L_{d}$ and capacitor $C_{d}$ inserted in series between the dc-side terminals and the converter [5.22]. The $L_{d}$ and $C_{d}$ are selected in order to suppress the $2^{\text {nd }}$ order voltages in a CSI and currents in a VSI, by presenting high impedance to $2^{\text {nd }}$ harmonic voltage. However, this LC solution has practical limitations.


Figure 5.36. Passive LC filter for 100 Hz elimination.

Firstly, the required $C_{d}$ and $L_{d}$ to block the $100 / 120 \mathrm{~Hz}$ component is large. In addition, any change in filter parameters with time leads to mistuning and drift from the targeted frequency. The energy in the proposed system is transferred and inverted through the inverters passive components, consequently, the series filter may interact with the energy transfer process.
Figure 5.36 shows that the LC filter requires bulky passive elements with high values if it is required to remove $90 \%$ of the $2^{\text {nd }}$ order harmonic currents and voltages.

### 5.2.2.2 Power electronic based active shunt 100/120 Hz filtering

A two-switch two-diode reversible boost converter or voltage buck-boost can actively eliminate the second order harmonic component from the input dc currents. As shown in Figure 5.37, the harmonic compensator (HC) has an input inductor so as not to interact with the control system of the main power stage. The $H C$ reference output current $i_{H C}{ }^{*}$ is controlled at double the grid frequency, with a $180^{\circ}$ phase shift, and magnitude equal to $i_{L}$ (the sum of $i_{\text {ina }}$ and $i_{\text {inb }}$ ). The reversible boost (reverse is buck) converter is shown in Fig. 12b. During the positive half cycle of $i_{H C}$, energy is transferred from the dc input and stored in $C_{H C}$, then in the negative half cycle, this energy is returned back to the dc input. Capacitor $C_{H C}$ stores (and deliver) energy. Equation (5.43), which assumes minimal residual capacitor stored energy, exposes why an active approach may be viable. Firstly, being a boost converter, B1A in Figure $5.38 \mathrm{a}, v_{H C}$ may be well in excess of the dc side voltage, and energy being related to the square of voltage, means $C_{H C}$ can be relatively small. A plastic dc link type capacitor would be viable and to obtain a high voltage gain, (as in a PV system), a tapped inductor approach may be required. Secondly, the boost input inductance is related inversely to the switching frequency, although its current rating before saturation is $i_{s}$. At a modest HC switching frequency, at typical single-phase domestic ac power levels ( $<3 \mathrm{~kW}$ ), $L_{H C}$ can be relatively small.

$$
\begin{equation*}
W_{H C}=\frac{V_{i n} I_{i n}}{1 / 2 f}=1 / 2 C_{H C} V_{H C}^{2} \tag{5.43}
\end{equation*}
$$

The instantaneous power equation of the differential buck-boost inverter with an HC can be written as in (5.44a). The energy ( $P_{H C .} d t$ ) flows from the input side and is stored in the output capacitor $C_{H C}$ in the positive half cycle of $i_{H C}$ and $v_{H C}(t)$ increases from $V_{H C}(i)$ to $V_{H C}(f)$.


Figure 5.37. Differential-mode buck-boost inverter with HC

(b) Shunt elimination of the second order harmonic dc side current component

Figure 5.38. Active harmonic compensation

$$
\begin{gather*}
P_{i n}(t)=P_{H C}(t)+P_{o}(t) \\
V_{i n} I_{s}=i_{H C}(t) V_{i n}+v_{o}(t) i_{o}(t) \\
I_{s}=\frac{V_{o} I_{o}}{2 V_{i n}}  \tag{5.44a}\\
i_{H C}(t)=I_{s}-\frac{v_{o}(t) i_{o}(t)}{V_{i n}}  \tag{5.44b}\\
i_{H C}=\frac{V_{o} I_{o}}{2 V_{i n}} \cos 2 \omega t \\
I_{H C}^{\text {peak }}=\frac{V_{o} I_{o}}{2 V_{i n}} \tag{5.44c}
\end{gather*}
$$

In the negative half cycle of $i_{H C}$, the energy flows from $C_{H C}$ back to the dc supply with $v_{H C}(t)$ decreasing from $V_{H C}(f)$ to $V_{H C}(i)$. This can be expressed as:

$$
\begin{align*}
& V_{i n} \int_{0}^{t_{H C}^{\prime} / 2} i_{H C}(t) \mathrm{dt}=\frac{1}{2} C_{H C}\left[v_{H C}^{2}(f)-v_{H C}^{2}(i)\right] \\
& \text { where } t_{H C}=1 / 2 f \text { and } v_{H C}(i)=V_{i n} \\
& v_{H C}^{2}(f)=V_{i n}^{2}+\frac{2 V_{i n}\left(\frac{V_{o} I_{o}}{2 V_{i n}}\right)}{2 \pi f C_{H C}}  \tag{5.45}\\
& v_{H C}(f)=\sqrt{v^{2}{ }_{i n}+\frac{V_{o} I_{o}}{2 \pi f C_{H C}}}
\end{align*}
$$

In the boost converter, like one in Figure 5.38a, the relation between the input and output voltages is related to the converters duty ratio $\delta_{H C}$ :

$$
\begin{align*}
& \frac{v_{H C}}{V_{\text {in }}}=\frac{1}{1-\delta_{H C}} \\
& \delta_{H C}=\frac{t_{H C}(o n)}{t_{s}} \tag{5.46}
\end{align*}
$$

$t_{H C}(\mathrm{on})$ is the period when $S_{H C I}$ is on.

$$
\begin{align*}
& \delta_{H C}=1-\frac{V_{i n}}{v_{H C}} \\
& \delta_{H C}=1-\frac{V_{i n}}{\sqrt{2 \frac{V_{i n}}{C_{H C}} \int_{0}^{t} i_{H C}(t) \mathrm{dt}+V_{i n}^{2}}} \tag{5.47}
\end{align*}
$$

The average duty ratio can be approximated as:

$$
\begin{align*}
& \bar{\delta}_{H C}=1-\frac{V_{i n}}{\bar{v}_{H C}} \\
& \bar{v}_{H C}=\frac{V_{i n}+V_{H C}(f)}{2}  \tag{5.48}\\
& \bar{\delta}_{H C}=1-\frac{2 V_{i n}}{V_{i n}+V_{H C}(f)}=1-\frac{2 V_{i n}}{V_{i n}+\sqrt{v_{i n}^{2}+\frac{V_{o} I_{o}}{2 \pi f C_{H C}}}}
\end{align*}
$$

Figure 5.39 shows MATLAB simulation results for a single-phase Ćuk inverter with active harmonic compensation

(a) Inverter operation

(b) Rectifier operation

Figure 5.39. Differential-mode Ćuk inverter with HC.
A. Power loss of HC

From Figure 5.40a, averaging along the positive half cycle of $i_{H C}$, the average current $\bar{I}_{D H C} 2$ can be calculated as:

$$
\begin{align*}
& \bar{I}_{D H C 2}=\left(1-\bar{\delta}_{H C}\right) \bar{I}_{H C} \\
& \bar{I}_{D H C 2}=\left(1-\bar{\delta}_{H C}\right) \frac{V_{o} I_{o}}{2 \pi V_{i n}} \tag{5.49}
\end{align*}
$$

From Figure 5.40b, averaging along the negative half cycle of $i_{H C}$, the average current $\bar{I}_{D H C 1}$ is:

$$
\begin{align*}
& \bar{I}_{D H C 1}=\left(1-\bar{\delta}_{H C}\right) \bar{I}_{H C} \\
& \bar{I}_{D H C 1}=\bar{\delta}_{H C} \frac{V_{o} I_{o}}{2 \pi V_{i n}} \tag{5.50}
\end{align*}
$$

If $r_{H C}$ is the parasitic resistance of the inductor $L_{H C}$ and $V_{D F}$ is the forward voltage of the diodes, the total power losses of the converter is:

$$
\begin{equation*}
P_{\text {loss_HC }}=1 / 2 I_{H C}^{\text {peak } 2} \quad r_{H C}+\left(\bar{I}_{D H C 1}+\bar{I}_{D H C 2}\right) V_{D F}+R_{o n} I_{r m s}^{2} \tag{5.51}
\end{equation*}
$$



Figure 5.40. Operation of reversible boost converter (B1A).

## B. HC input ripple

The instantaneous input current and output voltage during one sample period can be written as:
i) During $t_{H C}($ on $)$

$$
\begin{gather*}
L_{H C} \frac{d i_{H C}}{d t}=V_{i n} \\
V_{i n}=L_{H C} \frac{\Delta I_{H C}}{\Delta t} \\
\Delta I_{H C}=V_{i n} \frac{\Delta t}{L_{H C}}  \tag{5.52}\\
\Delta I_{H C}=V_{i n} \frac{\delta_{H C} t_{s}}{L_{H C}}
\end{gather*}
$$

ii) During $t_{H C}($ off $)$

$$
\begin{align*}
\frac{d i_{H C}}{d t} & =\frac{1}{L_{H C}} V_{i n}-\frac{1}{L_{i n}} v_{H C} \\
\Delta I_{H C} & =V_{i n} \frac{\Delta t}{L_{H C}}-v_{H C} \frac{\Delta t}{L_{H C}}  \tag{5.53}\\
\Delta I_{H C} & =V_{i n} \frac{\left(1-\delta_{H C}\right) t_{s}}{L_{H C}}-v_{H C} \frac{\left(1-\delta_{H C}\right) t_{s}}{L_{H C}}
\end{align*}
$$

The maximum ripple in the input current $i_{H C}$ occur at the peak of the duty ratio $\delta^{\max }{ }_{H C}$. From equations (5.45) and (5.46):

$$
\begin{gather*}
\delta_{H C}^{\max }=1-\frac{V_{i n}}{\sqrt{v^{2}{ }_{i n}+\frac{V_{o} I_{o}}{2 \pi f C_{H C}}}}  \tag{5.54}\\
\Delta I_{H C}=V_{i n} \frac{\delta^{\max }{ }_{H C} t_{s}}{L_{H C}}
\end{gather*}
$$

## C. Devices voltages and currents

From Figure 5.38, the average device voltages are:

$$
\begin{gather*}
\bar{V}_{D H C 1}=\left(1-\bar{\delta}_{H C}\right) \bar{V}_{H C} \\
\bar{V}_{D H C 1}=V_{i n}  \tag{5.55}\\
\bar{V}_{D H C 2}=\bar{\delta}_{H C} \bar{V}_{H C} \\
\bar{V}_{D H C 2}=\bar{\delta}_{H C}\left(\frac{V_{i n}+V_{H C}(f)}{2}\right) \tag{5.56}
\end{gather*}
$$

The average switches currents can be calculated as:

$$
\begin{gather*}
\bar{I}_{S H C 1}=\bar{\delta}_{H C} \bar{I}_{H C} \\
\bar{I}_{S H C 1}=\bar{\delta}_{H C} \frac{V_{o} I_{o}}{2 \pi V_{i n}}  \tag{5.57}\\
\bar{I}_{S H C 2}=\left(1-\bar{\delta}_{H C}\right) \bar{I}_{H C} \\
\bar{I}_{S H C 2}=\left(1-\bar{\delta}_{H C}\right) \frac{V_{o} I_{o}}{2 \pi V_{i n}} \tag{5.58}
\end{gather*}
$$

The RMS value of the switch current is:

$$
\begin{equation*}
I_{r m s}=\sqrt{\frac{3 \bar{\delta}_{H C} I_{o}^{2}}{2}\left(\frac{H_{d c}^{2}}{4}+\frac{3 H_{a c}^{2}}{16}\right)} \tag{5.59}
\end{equation*}
$$

## D. Other HC topologies

There are 8 other converter topologies with continuous input current suitable as a HC, as shown in Figure 5.41. Figure 5.42 shows compares their performance at different circuit conditions at $L_{H C}=4 \mathrm{mH}$ (with $r_{L H C}=70 \mathrm{~m} \Omega$ ) and $C_{H C}=50 \mu \mathrm{~F}$. With the boost converter B1A as a reference, B1P and B1C have the highest efficiency
while B1E, B2E and B2G have the lowest maximum input ripple current. In terms of the device rated voltages and currents, they are all rated the same.


Figure 5.41. Possible HC configurations.

(a) Efficiency versus input voltage and output current (at $V_{o}=200 \mathrm{~V}$ and $r_{H C}=70$ $\mathrm{m} \Omega$ )

(b) Maximum input ripple current versus input voltage and output current (at $V_{o}$ $=200 \mathrm{~V}$ and $L_{H C}=4 m H$ and $\left.C_{H C}=50 \mu F\right)$

Figure 5.42. Performance of HC topologies in Figure 5.41.

### 5.2.2.3 Active 100/120 Hz filtering without additional power electronics

The double-frequency input current ripple of the buck-boost inverter can be decoupled by additional control. The controller forces the energy to be stored instantaneously in the output capacitors (which are necessary for bB1F and SEPIC
inverters and optional for bB1C, bB1D and bB2D inverters). The controller must ensure that this stored energy does not affect the output voltages and currents, as shown in Figure 5.43. Without decoupling the double-frequency power, the output instantaneous power is:

$$
\begin{equation*}
p(t)=\underbrace{S \cos \gamma}_{P}-\underbrace{S \cos (2 \omega t-\gamma)}_{Q} \tag{5.60}
\end{equation*}
$$

where, $S=\frac{1}{2} V_{o} I_{o}$


Figure 5.43. Buck-boost inverter with decoupling capacitors
The converter output voltages, $v_{a}$ and $v_{b}$ shown in Figure 5.43, can be expressed as:

$$
\begin{align*}
& \left.v_{a}(t)=1 / 2 V_{o}+1 / 2 V_{o} \sin \omega\right)+V_{2} \sin \left(2 \omega t+\psi_{2}\right) \\
& v_{b}(t)=1 / 2 V_{o}+1 / 2 V_{o} \sin (\omega t+\pi)+V_{2} \sin \left(2 \omega t+\psi_{2}\right) \tag{5.61}
\end{align*}
$$

$V_{2}$ and $\psi_{2}$ are the peak and phase-shift of the $2^{\text {nd }}$ order harmonic output voltages respectively. The dc and double-frequency voltages components cancel leaving the fundamental component across the load. The currents through the output capacitors can be written as:

$$
\begin{align*}
& i_{a}(t)=C_{o}\left[1 / 2 V_{o} \omega \cos \omega t+2 \omega V_{2} \cos \left(2 \omega t+\psi_{2}\right)\right] \\
& i_{b}(t)=C_{o}\left[1 / 2 V_{o} \omega \cos (\omega t+\pi)+2 \omega V_{2} \cos \left(2 \omega t+\psi_{2}\right)\right] \tag{5.62}
\end{align*}
$$

The stored energy within the output capacitors is:

$$
\begin{gather*}
Q_{c}(t)=L_{1}\left(\frac{d i_{\text {ina }}}{d t} i_{i n a}+\frac{d i_{\text {inb }}}{d t} i_{i n b}\right)+2 L_{2} \frac{d i_{o}}{d t} i_{o}+ \\
C\left(\frac{d v_{c a}}{d t} v_{c a}+\frac{d v_{c b}}{d t} v_{c b}\right)+C_{o}\left(\frac{d v_{a}}{d t} v_{a}+\frac{d v_{b}}{d t} v_{b}\right)  \tag{5.63}\\
Q_{c}(t)=C_{o}\left[4 \omega V_{o} V_{2} \cos \left(2 \omega t+\psi_{2}\right)+\omega V_{o}^{2} \sin 2 \omega t+4 \omega V_{2}^{2} \sin \left(4 \omega t+2 \psi_{2}\right)\right]
\end{gather*}
$$

Equating $Q_{c}$ to $Q$ in equation (5.60), neglecting the $4^{\text {th }}$ order components, and solving for $V_{2}$ and $\psi$ leads to:

$$
\begin{align*}
& \psi_{2}=\tan ^{-1}\left(\frac{\omega C_{d} V_{o}^{2}}{4 S \cos \gamma}\right) \\
& V_{2}=\frac{S \cos \gamma}{2 \omega C_{o} V_{o} \cos \left(\psi_{2}\right)}  \tag{5.64}\\
& \quad \text { where } C_{d}=C+C_{o}
\end{align*}
$$

The $2^{\text {nd }}$ order harmonic component can be eliminated from the total input current by proper selection of $V_{2}$ and $\psi$. Figure 5.44 shows MATLAB simulation results for the single-phase SEPIC inverter with $V_{i n}=100, V_{o}=100 \mathrm{~V}$ and $I_{o}=12 \mathrm{~A}$. The $4^{\text {th }}$ order harmonic component in the input current $i_{s}$ (see Figure 5.44a) appears because it is neglected in equation (5.63) in order to ease calculation.


Figure 5.44. Simulation of single-phase SEPIC inverter with decoupling capacitors ( $\mathrm{C}_{\mathrm{o}}=100 \mu \mathrm{~F}$ ).

This also leads to the deviation between $Q$ and $Q_{c}$ as shown in Figure 5.44c. A simple controller, shown in Figure 5.45, is implemented in order to ensure suppression of the $2^{\text {nd }}$ and $4^{\text {th }}$ order harmonics from the input current.

Equ (5.64)


Figure 5.45. Control scheme for system in Figure 5.43.


Figure 5.46. Total input current of SEPIC single-phase inverter using controller in Figure 5.45.

As the controller's fast dynamics are not important, the gain values of the controller can be selected to be much lower than the main loop values in order to avoid its interaction. Figure 5.46 shows MATLAB simulation results for the SEPIC inverter with the controller in Figure 5.45 is used to eliminate the $2^{\text {nd }}$ and $4^{\text {th }}$ order harmonic components in the input current $i_{s}$.
Figure 5.47 shows the voltage stress across the decoupling capacitors ( $C_{H C}$ and $C_{o}$ ) for the two active methods, with and without power electronic devices, at different output current and capacitors values. It is obvious that using additional power electronic based method results in lower stress on the capacitor $C_{H C}$ than on $C_{o}$ in the second method. However, Figure 5.48 shows that the efficiency of the second method is higher as power losses in the devices of the additional power electronic converter are eliminated.


Figure 5.47. Voltage stress across the decoupling capacitor ( $C_{o}$ or $C_{H C}$ ) for active elimination methods at different load current and capacitor values.


Figure 5.48. Differential-mode Cuk inverter efficiency with $2^{\text {nd }}$ order harmonic currents active elimination techniques

### 5.2.3 Experimental Results

In order to substantiate the previous discussion, analysis and simulations, a 2.5 kW differential mode single-phase inverter using two Cuk converters is practically assessed, with the parameters in Table 5.3 and controlled with TMS320F280335 DSP, see Figure 5.49. Inverter close loop operation when supplying 16A (rms) to a $5 \Omega$ resistive load is shown in Figure 5.50. Figure 5.51 shows the inverter operation when connected to the grid $\left(V_{o}=200 \mathrm{~V}\right)$ at unity power factor $(\gamma=0)$. The grid voltage and output current are shown in Figure 5.51a, while the input current is shown in Figure 5.51 b . Figure 5.52 repeats the operation when the inverter operates in the
buck mode with $V_{o}=50 \mathrm{~V}$. The boost converter (B1A) is used as a harmonic compensator to remove the $2^{\text {nd }}$ order harmonic current and the results are shown in Figure 5.53.


Figure 5.49. Experimental single-phase Ć $u k$ inverter.


Figure 5.50. Differential single phase inverter with a $5 \Omega$ resistive load.


Figure 5.51. Grid-connected differential single phase inverter: (a) output voltage and current and (b) input current ( $V_{o}=200 \mathrm{~V}$ and $V_{i n}=100 \mathrm{~V}$ ).


Figure 5.52 Grid-connected differential single phase inverter in voltage buck mode: (a) output voltage and current and (b) input current ( $V_{o}=50 \mathrm{~V}$ and $V_{i n}=100 \mathrm{~V}$ ).


5ms/div-20A/div
Figure 5.53. Differential inverter input current with harmonic elimination using B1A.

Figure 5.54 shows the efficiency of the overall system versus the output current when $V_{o}=200 \mathrm{~V}$ and $\gamma=0$.


Figure 5.54 Differential-mode Cuk inverter efficiency.

Because the differential configuration supports bidirectional power flow, the power can be reversed to flow from the grid to the dc side, converting the system to operate as a boost-buck rectifier. Figure 5.55 shows the results when the dc terminals are connected to a $7 \Omega$ resistive load. Figure 5.56 shows inverter operation when the even order harmonic input current components are reduced with the control scheme in Figure 5.45. (without power electronic converter, $\mathrm{C}_{0}=100 \mu \mathrm{~F}$ )

(a) dc side currents


5ms/div-50V/div-10A/div
(b) Grid voltage and current

Figure 5.55. Buck-boost differential rectifier with a $7 \Omega$ resistive load: (a) dc side currents and (b) grid side voltage and current.

### 5.3 Summary

This chapter discussed the grid interfacing operation of several buck-boost converters with an inherent current source nature, which is attractive for small-scale renewable energy systems like PV and EV applications. This attractiveness comes from the fact that their continuous input currents are preferable for PV system MPPT techniques, in addition to easy of paralleling several dc-ac converters for scaling up the output power. Considered a disadvantage, the buck-boost converters belong to the family of non-linear converters where the dynamics depend on the operation point and duty ratio. The converter high order transfer function hampers easy control design. For three-phase grid-connected buck-boost inverters, the chapter discussed operation, control design and elimination techniques for the undesirable voltage and current harmonic components which appear because of the converters non-linearity.

Operation and control of derived single-phase differential mode buck-boost inverters controlled by sliding mode controllers was presented.


Figure 5.56. Differential inverters with decoupled even harmonics as in Figure 5.44.

Grid-connection of these inverters has been investigated with their numerous advantages when embedded in renewable energy generation systems. Finally, two methods were proposed, with and without additional power electronic devices, for eliminating the $2^{\text {nd }}$ order current component which appears in the input side. The main advantage of the first method is that the total dc side ripple current can be low, without recourse to electrolytic capacitor filtering. This increases system reliability, as plastic capacitors are thirty times more reliable than electrolytic types under identical operating conditions. The second method requires no additional power electronic switches as the oscillating power is stored in the output capacitors. As a result, this eases the required control and reduces semiconductor power losses. A drawback of this method is the voltage stresses across the output capacitors are increased.

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## Chapter 6

## Isolated Buck-Boost Inverters

### 6.1 Introduction

For reasons related to noise mitigation, electromagnetic compatibility and isolation, galvanic isolation between the input and output of a power converter is necessary in many applications [6.1]. Many small and medium scale power converters with buckboost capability can be modified to offer transformer coupling and isolation [6.2][6.5]. The traditional buck-boost converter can be isolated using a coupled magnetic circuit [6.6]. Generally, there are two main methods of power converter transformer coupling. In the first, a magnetic core temporarily stores the energy and then releases it to the output [6.6]. However, the maximum transferred energy is limited by core volume, viz., $1 / 2 B H \times$ Volume. The second method does not require temporarily energy storage; hence, the core need not be exposed to dc magnetizing current bias. In the later method, the magnetic energy is transferred through instantaneous transformer action instead of being temporary stored in an intermediate magnetic circuit and then released. Thus, a relatively small core volume can be used. Figure 6.1 presents the differences between the two methods, in the case of a typical SEPIC converter. In Figure 6.1a, the energy is temporarily stored in the magnetic isolation transformer. Although the average voltage across the transformer is zero in the SEPIC converter in Figure 6.1b; the transformer core is exposed to a dc bias current and flux because of the stored energy; thus, the core volume is increased. Such dc current bias would increase the core power loss and decrease its maximum current utilization. But with the series energy transfer intermediate capacitor split into two and placed each side of the isolation transformer as shown in Figure 6.1c, the energy transfer from the input to the output is achieved instantaneously, without being stored in the transformer core. In the two methods, the average voltage across the transformer is zero. If the turns ratio $N_{2} / N_{1}$ is greater than 1 , the converter voltage output $V_{o}$ can be increased to offer higher voltages. From Table 2.2, seven buck-boost converters are identified that can be isolated using a high frequency transformer, three have continuous input current, viz., bB1C (Ćuk), bB1F, and bB1G (SEPIC) converters, see Table 6.1.

(a)

(b)

(c)

Figure 6.1. SEPIC converter: (a) non-isolated converter, (b) magnetic storage coupling, (c) instantaneous transformer coupling.

Table 6.1. Transformer-isolated buck-boost converters with continuous input current

|  |  |  |  |
| :---: | :---: | :---: | :---: |
|  | Ćuk | SEPIC | BB1F |
|  | Instantaneous energy transfer | Instantaneous energy transfer | Temporarily stored energy |
|  | 0 | 0 | $I_{\text {in }}$ |
|  | $V_{c l}=V_{i n}, V_{c 2}=V_{o}$ | $V_{c l}=V_{i n}, V_{c 2}=0$ | na |

### 6.2 Isolated Ćuk converter

The dc-dc operation of the isolated Ćuk converter in Table 6.1 is shown in Figure 6.2 , showing its instantaneous voltages and currents. As with non-isolated Ćuk inverters, isolated Ćuk converter outputs can be connected differentially as shown in Figure 6.3. The ac operation of the isolated single-phase Cuk inverter is shown in Figure 6.4.


Figure 6.2. Voltages and currents of isolated Cúk converter.


Figure 6.3. Single-phase isolated Cúk inverter.
The isolated three-phase buck-boost inverter based on Ćuk converters is shown in Figure 6.5. The inverter voltages and currents are shown in Figure 6.6. The experimental comparison between the efficiencies of non-isolated and isolated threephase inverters is shown in Figure 6.7. Because of the core losses in the isolated version, it has lower efficiency than the non-isolated version.


Figure 6.4. Voltages and currents of isolated single-phase Cúk inverter.


Figure 6.5. Three-phase isolated Cúk inverter.


Figure 6.6. Voltages and currents of isolated three-phase Cúk inverter.


Figure 6.7. Efficiency of non-isolated and isolated three-phase grid-connected Ćuk inverter (Experimental, $V_{o}=200 \mathrm{~V}$ ).

### 6.3 Isolated SEPIC converter

The voltages and currents of the dc-dc isolated SEPIC converter are same as with Cuk converters except for the secondary capacitor $\left(C_{s}\right)$ voltage $V_{c 2}$. This voltage is shown in Figure 6.8


Figure 6.8. Voltage $\left(V_{c 2}\right)$ across secondary capacitor $\left(C_{s}\right)$ in isolated SEPIC

As with the non-isolated SEPIC inverters, the isolated converters can be connected differentially as shown in Figure 6.9. The ac operation of the isolated single-phase SEPIC inverter is the same as Ćuk single-phase inverter except that voltages $V_{c 2 a}$ and $V_{c 2 b}$ do not have the dc bias ( $V_{i n}$ ). The isolated three-phase buck-boost inverter based on the SEPIC converter is shown in Figure 6.10. The experimental comparison between the efficiencies of the non-isolated and isolated three-phase inverters is shown in Figure 6.11.


Figure 6.9. Single-phase isolated SEPIC inverter.


Figure 6.10. Three-phase isolated SEPIC inverter.


Figure 6.11. Efficiency of three-phase grid-connected SEPIC inverter (Experimental,

### 6.4 Novel Isolated Buck-Boost Inverters with Reduced Switches

New and interesting isolated three-phase inverter can be obtained as a result of the previous discussion. From Table 2.1, four converters were identified that can generate bi-pole output voltage. These converters are b1G, b2G, B1G, and B2G, and their voltage conversion ratios are shown in Figure 6.12. B1G and B2G have a discontinuous voltage ratio over the full operating range and are unable to generate zero output voltage ( $V_{o}=0$ ). However, b1G and b2G have continuous voltage $\left(V_{o} / V_{i n}\right)$ and duty $D$ ratios.


Figure 6.12. Voltage conversion ratios of converters with positive and negative These converters can be combined with a SEPIC (or Ćuk) converter to derive reduced switch count converters as shown in Figure 6.13. The output voltage relative to ground in these inverters can be expressed as:

$$
\begin{align*}
& v_{o a}(t)=M \cdot V_{o} \sin \omega t \\
& v_{o b}(t)=0  \tag{6.1}\\
& v_{o c}(t)=M \cdot V_{o} \sin (\omega t-1 / 3 \pi)
\end{align*}
$$



Figure 6.13. New isolated three-phase inverter with five switches and diodes.

With the output voltages $v_{o a}, v_{o b}$ and $v_{o c}$, typical three-phase currents $i_{o a}, i_{o b}$ and $i_{o c}$ are generated when the load is symmetrical balanced as:

$$
\begin{align*}
& i_{o a}(t)=I_{o} \sin \omega t \\
& i_{o b}(t)=I_{o} \sin (\omega t-2 / 3 \pi)  \tag{6.2}\\
& i_{o c}(t)=I_{o} \sin (\omega t+2 / 3 \pi)
\end{align*}
$$



Figure 6.14. Open loop operation of three-phase buck-boost inverter in Figure
On this assumption and the current polarities in Figure 6.13, the neutral-point voltage relative to ground ( $V_{o n}$ ) is $V_{o n}=\frac{1}{3}\left(v_{o a}+v_{o c}\right)=\frac{1}{\sqrt{3}} M V_{o} \sin \left(\omega t-\frac{1}{6} \pi\right)$; thus, the three-phase voltages relative to the neutral-point, which are responsible for driving the threephase currents are : $v_{a n}=v_{o a}-v_{o n}=\frac{1}{\sqrt{3}} M V_{o} \sin \left(\omega t+\frac{1}{6} \pi\right) ; v_{b n}=0-v_{o n}=\frac{1}{\sqrt{3}} M V_{o} \sin \left(\omega t+\frac{5}{6} \pi\right)$ and $v_{c n}=v_{o c}-v_{o n}=\frac{1}{\sqrt{3}} M V_{o} \sin \left(\omega t+\frac{3}{2} \pi\right)$. The phase voltages $v_{a n}, v_{b n}$ and $v_{c n}$ are displaced by $120^{\circ}$ in space as expected in a three-phase system.

Figure 6.14 shows the open loop simulation for the inverter in Figure 6.13. The same concept can be used for the three-switch single-phase inverter in Figure 6.15 with SEPIC or Ćuk converters. Besides requiring three-switches and diodes instead of four, this topology can decouple the $2^{\text {nd }}$ order harmonic from the input side. Because of independent control between the Ćuk (or SEPIC) and the b1G or (b2G) energy can be stored in capacitor $C_{s}$ capacitor for the $\dot{C} u k$ converter and in $L_{2}$ for the SEPIC converter. Figure 6.16 shows the open loop simulation of this system.


Figure 6.15. New isolated three-phase inverter with five switches and diodes.


Figure 6.16. Simulation of new three-switch isolated buck-boost single-phase inverter ( $V_{\text {in }}=100 \mathrm{~V}$,

### 6.5 Isolated bB1F converter

As described in the previous chapter, the bB1F converter has the lowest input current ripple among all buck-boost converters. The main difference between the isolated BB1F converter and the Ćuk or SEPIC converters is that the average core flux in the former has a finite value.This occurs because the average current though the core is not zero. The core flux is shown in Figure 6.17. The average flux $\bar{\Phi}$ necessitates larger core volume than the $\dot{C} u k$ and SEPIC converters. The single-phase and three-
phase isolated versions of bB1F converter are shown in Figure 6.18 and Figure 6.19 respctively.


Figure 6.17. Core flux of bB1F.
A comparison between the efficiencies of non-isolated and isolated three-phase inverters is shown in Figure 6.20. The effect of increasing the load current on reducing total efficiency is higher than the Cuk and SEPIC base three-phase inverter cases because of the dc-bias current and average net core flux in bB1F.


Figure 6.18. Single-phase isolated $b B 1 F$ inverter.


Figure 6.19. Three-phase isolated $b B 1 F$ inverter.


Figure 6.20. Efficiency of three-phase grid-connected SEPIC inverter $\left(V_{o}=200 \mathrm{~V}\right)$

### 6.6 Summary

The chapter investigated methods of high-frequency transformer isolation for differential-mode buck-boost single-phase and three-phase inverters. In the first method, the inverter is isolated by small-size cores and the energy is transferred between the input and output sides instantaneously by transformer action. In the second method, part of the energy is stored in the couipling circuit core which
requires using larger cores. The generated topologies and their operation as isolated inverters were illustrated. A comparison between the efficiency of the isolated and non-isolated versions was conducted, were the coupled version suffer core losses which decrease their efficiency. The chapter has proposed new isolated inverter topologies with reduced active switch numbers.

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## Chapter 7

## Conclusion

### 7.1 General Conclusion

Modern energy sources, such as wind, photovoltaic, solar and fuel cells, became important energy sources in the international electricity market. Increasing the efficiency, reducing size, weight and cost of the renewable sources power electronic converters are important issues in the system design. The efficiency of a renewable source inverter depends on the total power loss in the passive and active elements as well as in other ripple components, which may be difficult to comprehend. Because most of the electrical output renewable sources have relationships between the output voltage, current, and maximum output power, the inverter input ripple (renewable source output) affects the maximum energy extracted from the renewable source. This energy extraction process is improved dramatically when the output energy flow of the renewable source is ripple free and continuous. Starting from basic singleswitch two-state dc-to-dc converters with continuous energy flow as building blocks, several single-phase and three-phase inverters can be implemented. Chapter two explained a generic method for the generation of dc-dc converters from basic singleswitch topologies such as buck, boost and buck-boost converters, and categorizes these generated converters into groups according to their features.

Chapter three discussed the switched model, large and small signal averaged models of the power converters presented in Chapter two, as well as their control using linear and variable structure nonlinear control techniques.

From a number of converters developed in Chapter two, Chapter four identified three groups of converters with continuous input and/or continuous output currents (continuous energy flow); which are suitable for renewable energy systems. A large electrolytic capacitor, which is an unreliable element, is avoided. The chapter presented, discussed and compared between the different emerging converters of each family in terms of element power losses and input current ripple, as these both affect the overall inverter efficiency. Also, output high frequency current and voltage
ripple of these converters are compared because they influence the size and weight of the required passive elements for a given inverter.

Chapter five proposed a number of new single-stage single and three phase buckboost grid-connected inverters, which are suitable for grid integration of renewable energy such as small-scale PV systems. The chapter proposed a novel control strategy in the stationary reference frame for the three-phase grid-connected inverter that removed the negative sequence current and voltage components, resulting from the non-linearity of some of the new inverters identified in Chapter four. Also, the use of sliding mode control for a number of the proposed grid-connected inverters was examined in order to improve their dynamic performance during faults and to prevent dc injection into ac side in differential mode topologies that have inherent dc bias in their pre-filter phase voltage at converter terminal. Moreover, chapter five examined the operation of single-phase grid-connected inverters with variable output voltage over a wide range (ac output voltage higher and lower than the input dc voltage, both boost and buck modes). Most of the topologies discussed in this chapter are validated using simulation and experimentation. Finally, this chapter presented two methods for elimination of the $2^{\text {nd }}$ harmonic from the input dc current of singlephase inverters and some of the three-phase inverters. The first method is active elimination, where the second order oscillating energy component is stored in a capacitor using an auxiliary converter with two semiconductor switches. The second method is passive elimination, where the oscillating energy is trapped in the main converter filtering circuit, without the need of an auxiliary converter. A comparison between the two methods showed that the second method is more efficient and has lower power losses, but it has higher voltage stresses across the output capacitors.

Chapter Six has proposed several high-frequency-isolated versions of the converters discussed in previous chapters. These converters use small sized nano-crystalline magnetic cores to achieve galvanic isolation for applications with an isolation safety requirement, and require a higher boosting ratio and noise immunity. As well as comparing different isolation mechanisms, this chapter proposed several dc-ac inverters isolated by a high frequency transformer. Additionally, a number of new attractive dc-ac inverters, with reduced number of switches were proposed. Amongst reduced switch count dc-ac inverters developed in this chapter, was a single-phase isolated dc-ac inverter requiring only three switches (two switches is sufficient for
the non-isolated version), while some three-phase isolated dc-ac inverters require only five switches (four switches for non-isolation). In addition, the proposed isolated single-phase inverters are able to supress the $2^{\text {nd }}$ order harmonic current in the dc link, without the need for an auxiliary converter.

### 7.2 Author's contribution

This thesis has explored the generation of simple and complex dc-dc and dc-ac converters (inverter and rectifier) from basic dc-dc converters topologies, including their modelling, control and implementation, with emphasis on current source versions for their suitability in grid integration of many renewable and modern energy systems with relatively low output dc voltage. The main contributions of this thesis are summarized as follows:

- Presented comprehensive analysis of the basic single-switch single-diode power converters and methodology for generation of complex dc-dc and dc-ac converters from these basic topologies. Important device aspects for each of the generated converters were considered, such as the possibility for high-frequency isolation, estimation of voltage and current stresses in the passive and active components, input current ripple estimation, and identification of the converter topologies that offer continuous input and output currents to be used for renewable energy applications, without the need for large filtering capacitors.
- A number of new single-stage single and three phase dc/ac grid-connected inverters capable of operating with variable output ac voltage over wide range (output ac voltage higher and lower than the input dc voltages were proposed. Also, it presented a proper control method for each converter that allows the fundamental voltage and current to be fully regulated, including the elimination of low order harmonic distortion, resulting from any inverter non-linearity.
- Sliding mode controllers were presented for some of the promising dc/ac inverters to provide faster dynamic response during system faults and prevent dc injection into ac side during unbalanced operation.
- A modified method to reduce the input current ripple for renewable energy application was investigated to reduce the required inductance of the current source (supported by simulation and experimentation).
- Due to large number of converters generated in this thesis, bidirectional capability of some of the proposed differential-mode single-stage single and three-phase grid-connected dc/ac inverters was demonstrated using simulation and experimentation, and this was achieved without large electrolytic capacitors.
- Two methods were proposed for eliminating the $2^{\text {nd }}$ order harmonic current from the input dc link current in single-phase grid-connected buck-boost inverters (with and without auxiliary power electronic converters). The validity of these methods was confirmed using simulation and experimentation.
- High-frequency-isolated versions of the single-phase and three-phase buck-boost inverters developed in Chapter five were developed, and compared with their non-isolated counterparts. All the isolated converters presented in this thesis are validated using simulation and experimentation, where nanocrystalline cores with small-size and high permeability are used.
- Several new single-phase and three-phase inverters with reduced switch number were presented. These converters offer buck-boost capabilities, and low order harmonics compensation can be achieved with additional converters.


### 7.3 Suggestion for future research

The research carried out in this thesis is concerned with the implementation, operation, and control of different families of current sourced converters with smaller passive elements, which can be used in many renewable and modern energy systems. Suggestions for future research are:

- Extension of the proposed inverters to form current source multilevel buck-boost inverters. As an indication, the proposed Ćuk three-phase inverter can be extended to a multilevel Ćuk inverter.
- Investigation of the issues that arise from parallel connection of the proposed inverters, such as circulating currents and response to network faults.
- Performance evaluation of the proposed inverters when detailed models of PV and fuel cells are incorporated. The effect of high frequency current ripple over 50 Hz (or 100 Hz components) and their effect on the PV or fuel cells power curves should be investigated in detail.
- Investigate alternative methods for $2^{\text {nd }}$ order harmonic current elimination in single-phase inverters.
- Investigation of the proposed inverters in islanding mode.
- Implementation of multiport PV current source buck-boost inverters with energy storage systems.
- Investigation of the proposed three-phase bidirectional current source inverters for use with wind turbine generators.
- Effect of different PWM techniques on the power losses of the proposed inverters' active switches.


## Appendix A

## Test Rig Structure

In this section, details about hardware elements and simulation software are presented. A description about the measurement devices, control, and power circuits is given. The preparation for interfacing the different converters to the distributed grid is presented.

## A.1Hardware structure

A photograph of the hardware setup is shown in Figure A.1. The overall system consists of:

- DSP: 32-bit TMS320F28335 150MHz floating point controller;
- Current and voltage measurement devices;
- Gate drive circuits;
- Universal power converters;
- DC power supply;
- Auto transformers;
- Variable loads;
- Air core inductors;
- Isolation transformer;
- DC current measurements.


Figure A. 1. Experimental test rig photograph

## A.1.1 Digital Signal Processor (DSP)

The DSP is responsible for reading the actual voltage and current waveforms from the measurement devices. Then, the DSP controls the overall operation according to the loaded program in its flash memory. Accordingly, the controller must have some features as fast calculating processor, sufficient storage memory, compatible and fast analogue to digital converters, and easy programming packages. For these reasons, Texas Instrument (TI) TMS320F28335 floating point DSP is used. The main task of the floating point DSP is to generate the PWM signal for the gate drive circuits which operate the active switches of the different power converters. The output port of the DSP is compatible with the gate drive input voltages and currents and hence, TMS320F28335 DSP does not require additional interfacing circuits. The measurement transducers are designed to have voltages and currents within the read range of the DSP. TMS320F28335 DSP support real-time monitoring and control by sending the data to addressed memory in the RAM and display it by Code Composer Studio V.3.3 software. One of the most important features of the TMS320F28335 DSP, that it can be programmed either by C, C++ coding or MATLAB SIMULINK. This eases the programming process when high level programming is required. Moreover, the DSP support CAN protocol and hence, can be interfaced with CANalayzer boxes. All the variables inside the running $C$ code can be transferred with CANalyzer Vector-XL to the host PC via CAN communication protocol. CANalyzer enables real time monitoring, controlling the system variables and provides also data logging excel sheets for more than 32 different signals all running in the background without affecting the processor's main tasks. In this thesis, two TMS320F28335 DSPs are used in parallel to control the different inverters. A photograph for the controller is shown in Figure A.2.


Figure A. 2. Texas Instrument TMS320F28335 DSP

## Features

- High-Performance Static CMOS Technology
- High-Performance 32-Bit CPU
- IEEE-754 Single-Precision Floating-Point Unit (FPU)
- Harvard Bus Architecture
- 150 MHz (6.67-ns Cycle Time)
- Code-Efficient (in C/C++ and Assembly)
- Fast Interrupt Response and Processing
- Memory
- Over 2M x 16 Address Reach
- 256 K data flash
- 34K on-Chip SARAM
- 8 K x 16 Boot ROM
- 16 K instruction cache
- Clock and System Control
- Dynamic PLL Ratio Changes Supported
- On-Chip Oscillator
- Watchdog Timer Module
- Peripheral Interrupt Expansion (PIE) Block That Supports 58 Peripheral Interrupts
- 128-Bit Security Key/Lock
- Protects Flash/OTP/RAM Blocks
- Prevents Firmware Reverse Engineering
- Enhanced Control Peripherals
- Up to 18 PWM Outputs
- Up to 6 HRPWM Outputs With 150 ps MEP Resolution
- Up to 6 Event Capture Inputs
- Up to 2 Quadrature Encoder Interfaces
- Up to 8 32-Bit Timers (6 for eCAPs and 2 for eQEPs)
- Three 32-Bit CPU Timers
- Serial Port Peripherals
- Up to 2 CAN Modules
- Up to 3 SCI (UART) Modules
- Up to 2 McBSP Modules (Configurable as SPI)
- One SPI Module
- One Inter-Integrated-Circuit (I2C) Bus
- Analogue to Digital Converters (ADC)
- 12-Bit ADC, 16 Channels
- 80-ns Conversion Rate
- $2 \times 8$ Channel Input Multiplexer
- Two Sample-and-Hold
- Single/Simultaneous Conversions
- Internal or External Reference
- Digital Inputs and Outputs
- Up to 88 Individually Programmable, Multiplexed GPIO Pins With Input Filtering
- Emulation Features
- Analysis and Breakpoint Functions
- Real-Time Debug via Hardware
- Development Support Includes
- ANSI C/C++ Compiler/Assembler/Linker
- Code Composer Studio IDE
- DSP/BIOS
- Digital Motor Control and Digital Power Software Libraries
- Temperature Options:
- $-40^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$


## A.1.2 Current and voltage measurements

As described in the previous chapters, the current through the inductors should be measured in order to provide the proper control task. In addition, the voltages of the capacitors as well as the grid voltages should be measured to ensure the proper grid interfacing process.
i. Voltage Measurements

The different voltages of the power converters and local grid are connected to the voltage transducers board shown in Figure A.3.


Figure A. 3. Voltage measurement board


Figure A. 4. Voltage measurement board schematic

The board in turns scales the input voltage and adds a dc-bias to make the output voltage compatible for the ADC of the DSP. The LEM25-P uses the Hall-effect to measure ac and dc signals. The LEM25-P sensor can measure up to 500 V with high frequency bandwidth. The circuit schematic is shown in Figure A.4.

## ii. Current Measurements

The proposed inverters output currents are measured and sent to the DSP for feedback control. In this work, Hall effect current sensing devices LEM LA-55p have been used to build the current sensing boards shown in Figure A.5. These
sensing devices isolate the sensed signals from the real currents waveform completely. They have wide measurement range from 0A to 50 A with accuracy bandwidth of 200 kHz . The schematic of the current sensing boards is shown in Figure A. 6.


## Voltage Transducer LV 25-P

For the electronic measurement of currents: DC, AC, pulsed... with galvanic isolation between the primary circuit and the secondary circuit.


## Electrical data



Note: ${ }^{1)} \mathbf{R}_{1}=25 \mathrm{k} \Omega$ (L/R constant, produced by the resistance and inductance of the primary circuit)

$$
\begin{aligned}
& \mathrm{I}_{\mathrm{PN}}=10 \mathrm{~mA} \\
& \mathrm{~V}_{P N}=10 . .500 \mathrm{~V}
\end{aligned}
$$



## Features

- Closed loop (compensated) current transducer using the Hall effect
- Isolated plastic case recognized according to UL 94-V0.

Principle of use

- For voltage measurements, a current proportional to the measured voltage must be passed through an external resistor $\mathbf{R}_{1}$ which is selected by the user and installed in series with the primary circuit of the transducer.


## Advantages

- Excellent accuracy
- Very good linearity
- Low thermal drift
- Low response time
- High bandwidth
- High immunity to external interference
- Low disturbance in common mode.

Applications

- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Power supplies for welding applications.

Application domain

- Industrial.

|  |  | Page $1 / 3$ |
| :--- | :--- | :--- |
| 20November2012/version 18 | LEM reserves the right to carry out modifications on its transducers, in order to improve them, without prior notice | www.lem.com |



Figure A. 5. Current measurement board


Figure A. 6. Current measurement board schematic

## A.1.3 Gate drive circuits

The gate drive circuits, shown in Figure A.7, are used to buffer the switching PWM of the switches from the DSP. This is necessary as the DSP can inject up to several milli-amperes current which is not sufficient to turn on the IGBT switch. The gate drive amplifies the output current of the DSP to reach the IGBT gate current. The gate drive circuit has suitable high-speed optical isolation which is necessary for
galvanic isolation between the DSP ground and the common points of the IGBTs.
This optical isolation allows short duration pulses to be transmitted to the switch. The parameters of the gate drive circuit are shown in Table A.1.


## Current Transducer LA 55-P

For the electronic measurement of currents: DC, AC, pulsed.. with galvanic isolation between the primary circuit (high power) and the secondary circuit (electronic circuit).


## Accuracy - Dynamic performance data

| X | Accuracy @ $\mathrm{I}_{\mathrm{PN}}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} @ \pm 15 \mathrm{~V}( \pm 5 \%)$ <br> @ $\pm 12$.. 15 V ( $\pm 5 \%)$ | $\pm 0.65$ |  | \% |
| :---: | :---: | :---: | :---: | :---: |
|  |  | $\pm 0.90$ |  | \% |
| $\varepsilon_{\mathrm{L}}$ | Linearity error | < 0.15 |  | \% |
|  |  | Typ | Max |  |
| $I_{0}$ | Offset current @ $\mathrm{I}_{\mathrm{P}}=0, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | $\pm 0.2$ | mA |
| $\mathrm{I}_{\text {OM }}$ | Magnetic offset current ${ }^{3)}$ @ $I_{P}=0$ and specified $R_{M}$, after an overload of $3 \times \mathrm{I}_{\mathrm{PN}}$ |  | $\pm 0.3$ | mA |
| $\mathrm{I}_{\text {OT }}$ | Temperature variation of $\mathrm{I}_{\mathrm{O}}$ | $\pm 0.1$ | $\pm 0.6$ | mA |
|  |  | $\pm 0.2$ | $\pm 1.0$ | mA |
| $\mathrm{t}_{\text {ra }}$ | Reaction time to $10 \%$ of $\mathrm{I}_{\text {PN }}$ step | < 500 |  | ns |
| $\mathrm{t}_{\mathrm{r}}$ | Response time to $90 \%$ of $\mathrm{I}_{\mathrm{PN}}$ step | < 1 |  | $\mu \mathrm{s}$ |
| di/dt | di/dt accurately followed | > 200 |  | A/ $/ \mathrm{s}$ |
| BW | Frequency bandwidth (-1 dB) | DC.. |  | kHz |

## General data

| $\mathbf{T}_{\mathrm{A}}$ | Ambient operating temperature |  | $-40 . .+85$ | ${ }^{\circ} \mathrm{C}$ |
| :--- | :--- | :--- | :--- | :--- |
| $\mathbf{T}_{\mathrm{S}}$ | Ambient storage temperature |  | $-40 . .+90$ | ${ }^{\circ} \mathrm{C}$ |
| $\mathbf{R}_{\mathrm{S}}$ | Secondary coil resistance | $@ \mathrm{~T}_{\mathrm{A}}=70^{\circ} \mathrm{C}$ | 80 | $\Omega$ |
|  |  | $@ \mathrm{~T}_{\mathrm{A}}=85^{\circ} \mathrm{C}$ | 85 | $\Omega$ |
| $\boldsymbol{m}$ | Mass |  | 18 | g |
|  | Standards |  | EN 50178: 1997 |  |

[^0]${ }^{\text {2) }}$ Measuring range limited to $\pm 55 \mathrm{~A}_{\text {max }}$
$$
I_{P N}=50 \mathrm{~A}
$$


## Features

- Closed loop (compensated) current transducer using the Hall effect
- Printed circuit board mounting
- Isolated plastic case recognized according to UL 94-VO.


## Advantages

- Excellent accuracy
- Very good linearity
- Low temperature drift
- Optimized response time
- Wide frequency bandwidth
- No insertion losses
- High immunity to external interference
- Current overload capability.


## Applications

- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Switched Mode Power Supplies (SMPS)
- Power supplies for welding applications.

Application domain

- Industrial.

Table A.1. Gate drive circuit parameters.

| Output voltage | 15 V |
| :---: | :---: |
| Output current | $\pm 3 \mathrm{~A}$ |
| Supply voltage (max) | 5 V |
| Measured signal frequency (max) | 75 kHz |
| $t_{\text {don }}$ | 60 ns |
| $t_{\text {doff }}$ | 60 ns |



Figure A. 7. Gate drive circuit

## A.1.4 Power Electronic Converter

3 kW Universal power electronic converters are built to implement and test all the inverters under investigation. The power electronic converters have changeable terminals and can be used to implement several inverters. the schematic of the power electronic converters is shown in Figure A. 8 and a photograph of the power converters is shown in Figure A.9. RC snubbering circuits are implemented across the switches terminals to supress the high voltage and current spikes. The gate drives are implemented inside the converters very near to the IGBT switches the EMI effect. The freewheeling diodes can be implemented in series or in parallel to the IGBTs according to the inverter under investigation. Each IGBT switches pair is connected on a separate heat sink to keep the IGBT temperature in the acceptable range.


Figure A. 8. Converter schematic


Figure A. 9. Power electronic converters

## A.1.5 DC power supply

Sorensen SG A80/65 (80VDC and 65Amperes) and SG A250/20 (250 VDC and 20 Amperes) supplies are used. A photograph for the first is shown in Figure A. 10.


Figure A. 10. DC supply

## A.1.6 Auto-transformer

Buck inverters are connected to the local ac grid through isolated auto transformers. The three-phase auto transformer is shown in Figure A.11. Type: Clairtronic CMV28F3, SR. No. 304/022007, Input $415 \mathrm{~V}, 3-\mathrm{ph}, 50 / 60 \mathrm{~Hz}$, output $0-415 \mathrm{~V}$. Capacity 50 A per line.


Figure A. 11. Three-phase auto-transformer

## A.1.7 Variable loads

1 kW inductive loads are shown in Figure A. 12 consisting of three variable banks. All loads can be step changed to provide transient test. Single-phase pure resistive loads are shown in Figure A. 13 with maximum DC current of 17A.


Figure A. 12. Three-phase auto-transformer


Figure A. 13. Three-phase auto-transformer

## A.1.8 Air core inductors

Air core inductors are used for the different inverter topologies to avoid saturation currents. The parameters of each air core inductor are:

| Diameter | 22 cm |
| :---: | :---: |
| Length | 25 cm |
| Turns | 60 |
| Inductance | 0.5 mH |



Figure A. 14. Three-phase auto-transformer

## A.1.9 Isolation transformer

12 KVA isolation transformer (with a primary to secondary voltage ratio of 60 V 380 V ) line-to-line is used to isolate the test rig from the inverters under investigations. The primary is delta connected where the secondary's all ends are out for series parallel connection.


Figure A. 15. Isolation transformer

The isolating transformer parameters are: $R_{t}=2 \Omega$ and $L_{t}=1 \mathrm{mH}, \mathrm{Rm}=700 \Omega$ and Lm $=1000 \mathrm{mH}$. These values were obtained with open and short circuit tests. The isolation transformer is shown in Figure A.15. It must be noted that the efficiency of the inverters are calculated without considering the power losses in the isolation transformer.

## A.1.10 DC current measurements

Two high performance current transducers (ITN 12-p Ultrastab) are used to measure the dc components in the output ac currents. The sensor gives very high accuracy and excellent linearity as well as high resolution.


Figure A. 16. DC current sensing boards

## High Performance Current Transducer ITN 12-P ULTRASTAB

For the electronic measurement of currents: DC, AC, pulsed..., with galvanic isolation between the primary circuit (high power) and the secondary circuit (electronic circuit).


## Electrical data

| $\mathrm{I}_{\text {PN }}$ | Primary nominal current DC | 12.5 | A |
| :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\text {PN }}$ | Primary nominal current rms | 8.8 | A |
| $\mathrm{I}_{\mathrm{PM}}$ | Primary current, measuring range | $0 . . \pm 12.5$ | A |
| $\hat{i}^{\text {p }}$ | Max overload capability $100 \mathrm{~ms}{ }^{1)}$ | $\pm 62.5$ | A |
| $\mathrm{R}_{\text {M }}$ | Measuring resistance <br> Over operating current, temperature and supply voltage range | $\begin{array}{ll} \mathbf{R}_{\mathrm{M} \text { min }} & \mathbf{R}_{\mathrm{M} \text { max }} \\ 0 & 31 \end{array}$ | $\Omega$ |
| $\mathrm{I}_{\text {S }}$ | Secondary current | 0 .. $\pm 50$ | mA |
| $\mathrm{I}_{\text {SN }}$ | Secondary nominal current rms | 35 | mA |
| $\mathrm{K}_{\text {N }}$ | Conversion ratio | 1:250 |  |
| $\mathrm{V}_{\mathrm{c}}$ | Supply voltage ( $\pm 5$ \%) | $\pm 15$ | V |
| $\mathrm{I}_{\mathrm{c}}$ | Current consumption $\pm 15 \mathrm{~V}$ | $\leq 60+I_{\text {s }}$ | mA |

## Accuracy - Dynamic performance data

$\varepsilon_{\mathrm{L}} \quad$ Linearity error ${ }^{2)} \quad \leq 4 \quad \mathrm{ppm}$

OE Electrical offset current + self magnetization + effect of earth magnetic field @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}{ }^{2)}$ $\Delta \mathrm{I}_{\mathrm{OE}} \quad$ Offset stability (no load) ${ }^{2)}$ Temperature coefficient of $\mathrm{I}_{\mathrm{OE}}\left(10^{\circ} \mathrm{C} . .45^{\circ} \mathrm{C}\right)^{2)}$ Offset vs. power supply stability @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}{ }^{2)}$
< 500 ppm
@ $\mathrm{V}_{\mathrm{c}}= \pm 15 \mathrm{~V} \pm 5 \%$

General data

| $\mathbf{T}_{\mathrm{A}}$ | Ambient operating temperature | $10 . .+45$ | ${ }^{\circ} \mathrm{C}$ |
| :--- | :--- | :--- | ---: |
|  | Humidity (non condensing) | $20-80 \%$ | RH |
| $\mathbf{T}_{\mathrm{S}}$ | Ambient storage temperature | $-20 . .+85$ | ${ }^{\circ} \mathrm{C}$ |
|  | Humidity (non condensing) | $20-80 \%$ | RH |
| $\mathbf{R}_{\mathrm{S}}$ | Secondary coil resistance @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | 90 | $\Omega$ |
| $\boldsymbol{m}$ | Mass | 0.35 | kg |

Notes: ${ }^{1}$ Single pulse only, not AC.
Overload conditions of use as described page 4
${ }^{2}$ ) All ppm figures refer to secondary measuring range 50 mA .
$I_{P M}=0 . .12 .5 \mathrm{~A}$


## Features

- Closed loop (compensated) current transducer using an extremely accurate zero flux detector
- Mountable on to a PCB
- Metal housing for high immunity against external interference


## Advantages

- Very high accuracy
- Excellent linearity
- Extremely low temperature drift
- Wide frequency bandwidth
- High immunity to external electrostatic and magnetic fields interference
- High resolution
- Low noise on output signal
- Low noise feedback to main conductor.


## Applications

- Feed back element in precision current regulated devices (power supplies...)
- Calibration unit
- Precise and high stability inverters
- Energy measurement
- Medical equipment.

Application domain

- Industrial and Medical.


## Appendix B

## Voltage and Current Waveforms of Power Converters in <br> Chapter 2

## B. 1 Cell D

1) b 1 D


Figure B.1.b1D converter


Table B.1. Voltage and current relations of b1D converter

| $V_{0}$ | $D V_{\text {in }}$ |
| :---: | :---: |
| $\bar{I}_{\text {in }}$ | $D \bar{I}_{o}$ |
| $\bar{V}_{c}$ | $V$ in |
| $\Delta V_{c}$ | $D \frac{\bar{I}_{0} t_{s}}{C}$ |
| $\Delta I_{\text {in }}$ | $D(1-D) \frac{t_{s} V_{i n}}{L_{2}}$ |
| $\bar{I}_{L 1}$ | $(1-D) \bar{I}_{o}$ |
| $\Delta I_{L 1}$ | $\frac{(1-D) \Delta V_{c} t_{s}}{4 L_{1}}$ |
| $\Delta I_{o}$ | $D(1-D) \frac{t_{s} V_{i n}}{L_{2}}$ |
| $\hat{I}_{s 1}$ | $\bar{I}_{o}$ |
| $\hat{I}_{\text {D } 2}$ | $\bar{I}_{o}$ |
| $\widehat{V}_{\boldsymbol{s} 1}$ | $V_{\text {in }}$ |
| $\widehat{V}_{D 2}$ | $V_{\text {in }}$ |

2) $b 2 D$


Figure B.3.b2D converter
Table B.2. Voltage and current relations of b2D converter

| $\boldsymbol{V}_{\boldsymbol{o}}$ | $D V_{\text {in }}$ |
| :---: | :---: |
| $\overline{\boldsymbol{V}}_{\boldsymbol{c}}$ | $V_{i n}$ |
| $\boldsymbol{\Delta} \boldsymbol{V}_{\boldsymbol{c}}$ | $D \frac{\bar{I}_{o} t_{s}}{C}$ |
| $\overline{\boldsymbol{I}}_{\boldsymbol{i n}}$ | $D \bar{I}_{o}$ |
| $\boldsymbol{\Delta \boldsymbol { I } _ { \boldsymbol { i n } }}$ | $\frac{(1-D) \Delta V_{c} t_{s}}{4 L_{1}}$ |
| $\boldsymbol{\Delta \boldsymbol { I } _ { \boldsymbol { o } }}$ | $D(1-D) \frac{t_{s} V_{i n}}{L_{2}}$ |
|  | $\bar{I}_{o}$ |
| $\hat{\boldsymbol{I}}_{\boldsymbol{s} \mathbf{1}}$ | $\bar{I}_{o}$ |
| $\hat{\mathbf{I}}_{\boldsymbol{D} \mathbf{2}}$ | $V_{\text {in }}$ |
| $\widehat{\boldsymbol{V}}_{\boldsymbol{s} \mathbf{1}}$ | $V_{\text {in }}$ |
| $\widehat{\boldsymbol{V}}_{\boldsymbol{D} \mathbf{2}}$ |  |



Figure B.4. b1D components voltages and currents.
3) B1D


Figure B.5. B1D converter


Table B.3. Voltage and current relations of B1D converter

| $V_{o}$ | $\frac{1}{(1-D)} V_{i n}$ |
| :---: | :---: |
| $\bar{V}_{c}$ | $V_{\text {in }} /(1-D)$ |
| $\Delta V_{c}$ | $D \frac{\bar{I}_{o} t_{s}}{C}$ |
| $\bar{I}_{\text {in }}$ | $\frac{\bar{I}_{o}}{(1-D)}$ |
| $\Delta I_{\text {in }}$ | $\left(D t_{s} V_{i n}\right) / L_{1}$ |
| $\bar{I}_{L 2}$ | $\frac{D}{(1-D)} \bar{I}_{o}$ |
| $\Delta I_{L 2}$ | $\frac{(1-D) \Delta V_{c} t_{s}}{4 L_{1}}$ |
| $\Delta I_{0}$ | $\left(D t_{s} V_{i n}\right) / L_{1}$ |
| $\hat{I}_{s 1}$ | $\frac{\bar{I}_{o}}{(1-D)}$ |
| $\hat{I}_{\boldsymbol{D} 2}$ | $\frac{\bar{I}_{o}}{(1-D)}$ |
| $\widehat{V}_{s 1}, \widehat{V}_{D 2}$ | $\frac{1}{(1-D)} V_{i n}$ |

4) $B 2 D$


Figure B.7. B2D converter


Figure B.8. B2D components voltages and currents.

Table B.4. Voltage and current relations of B2D converter

| $\boldsymbol{V}_{\boldsymbol{o}}$ | $\frac{1}{(1-D)} V_{\text {in }}$ |
| :---: | :---: |
| $\overline{\boldsymbol{V}}_{\boldsymbol{c}}$ | $V_{\text {in }} /(1-D)$ |
| $\boldsymbol{\Delta} \boldsymbol{V}_{\boldsymbol{c}}$ | $\frac{\bar{I}_{o} t_{s}}{C}$ |
| $\overline{\boldsymbol{I}}_{\boldsymbol{i n}}$ | $\frac{\bar{I}_{o}}{(1-D)}$ |
| $\boldsymbol{\Delta \boldsymbol { I } _ { \boldsymbol { i n } }}$ | $\left(D t_{s} V_{i n}\right) / L_{1}$ |
| $\boldsymbol{\Delta \boldsymbol { I } _ { \boldsymbol { o } }}$ | $\frac{(1-D) \Delta V_{c} t_{s}}{4 L_{2}}$ |
| $\hat{\boldsymbol{I}}_{\boldsymbol{s} \mathbf{1}}, \hat{\boldsymbol{I}}_{\boldsymbol{D} \mathbf{2}}$ | $\frac{\bar{I}_{o}}{(1-D)}$ |
| $\widehat{\boldsymbol{V}}_{\boldsymbol{s} \mathbf{1}}, \widehat{\boldsymbol{V}}_{\boldsymbol{D} \mathbf{2}}$ | $\frac{1}{(1-D)} V_{i n}$ |

5) bB 1 D


Figure B.9. bB1D converter

Table B.5. Voltage and current relations of bB1D converter

| $\boldsymbol{V}_{\boldsymbol{o}}$ | $\frac{D}{(1-D)} V_{i n}$ |
| :---: | :---: |
| $\overline{\boldsymbol{V}}_{\boldsymbol{c}}$ | $V_{i n} /(1-D)$ |
| $\boldsymbol{\Delta} \boldsymbol{V}_{\boldsymbol{c}}$ | $\frac{\bar{I}_{o} t_{s}}{C}$ |
| $\overline{\boldsymbol{I}}_{\boldsymbol{i n}}$ | $\frac{D \bar{I}_{o}}{(1-D)}$ |
| $\boldsymbol{\Delta} \boldsymbol{I}_{\boldsymbol{i n}}$ | $\left(D t_{s} V_{i n}\right) / L_{1}$ |
| $\overline{\boldsymbol{I}}_{\boldsymbol{L} \mathbf{2}}$ | $\frac{\bar{I}_{o}}{(1-D)}$ |
| $\boldsymbol{\Delta} \boldsymbol{I}_{\boldsymbol{L} \mathbf{2}}$ | $\Delta I_{L 2}=\frac{D t_{s} V_{i n}}{L_{2}}$ |
| $\boldsymbol{\Delta \boldsymbol { I } _ { \boldsymbol { o } }}$ | $\left(D t_{s} V_{i n}\right) / L_{2}$ |
| $\hat{\boldsymbol{I}}_{\boldsymbol{s} \mathbf{1}}, \hat{\boldsymbol{I}}_{\boldsymbol{D} \mathbf{2}}$ | $\frac{\bar{I}_{o}}{(1-D)}$ |
| $\widehat{\boldsymbol{V}}_{\boldsymbol{s} \mathbf{1}}, \widehat{\boldsymbol{V}}_{\boldsymbol{D} \mathbf{2}}$ | $\frac{1}{(1-D)} V_{i n}$ |


6) bB 2 D


Figure B.11. bB2D converter
 Figure B.12. bB1D components voltages and currents.

Table B.6. Voltage and current relations of bB2D converter

| $V_{o}$ | $\frac{D}{(1-D)} V_{i n}$ |
| :---: | :---: |
| $\bar{V}_{c}$ | $V_{\text {in }} /(1-D)$ |
| $\Delta V_{c}$ | $D \frac{\bar{I}_{o} t_{s}}{C}$ |
| $\overline{\mathbf{I}}_{\text {in }}$ | $\frac{\breve{I}_{o}}{(1-D)}$ |
| $\Delta I_{\text {in }}$ | $\left(D t_{s} V_{\text {in }}\right) / L_{1}$ |
| $\bar{I}_{L 1}$ | $\frac{\bar{I}_{o}}{(1-D)}$ |
| $\Delta I_{L 1}$ | $\Delta I_{L 2}=\frac{D t_{s} V_{i n}}{L_{1}}$ |
| $\Delta I_{o}$ | $\frac{(1-D) \Delta V_{c} t_{s}}{4 L_{2}}$ |
| $\hat{I}_{s 1}, \hat{I}_{D 2}$ | $\frac{\bar{I}_{o}}{(1-D)}$ |
| $\widehat{V}_{s 1}, \widehat{V}_{D 2}$ | $\frac{1}{(1-D)} V_{i n}$ |

## B. 2 Cell E

1) b1E


Figure B.13. b1E converter


Figure B.14. b1E components voltages and currents.

Table B.7. Voltage and current relations of b1E converter

|  |  |
| :---: | :---: |
| $\bar{I}_{\text {in }}$ | $D \bar{I}_{o}$ |
| $\hat{I}_{\text {in }}$ | $\bar{I}_{o}$ |
| $\overline{\boldsymbol{V}}_{\boldsymbol{c}}$ | $(1-D) V_{\text {in }}$ |
| $\Delta V_{c}$ | $\frac{D \Delta I_{L 1} t_{s}}{8 C}$ |
| $\bar{I}_{L 1}$ | $(1-D) \bar{I}_{o}$ |
| $\Delta I_{L 1}$ | $\underline{(1-D) \Delta V_{c} t_{s}}$ |
|  | $4 L_{1}$ |
| $\Delta I_{o}$ | $\Delta I_{o} \simeq \frac{\Delta I_{L 1} D^{2} t_{s}^{2}}{12 C L_{2}}$ |
| $\hat{I}_{s 1}$ | $\bar{I}_{o}$ |
| $\hat{I}_{\boldsymbol{D} \boldsymbol{L}}$ | $\bar{I}_{o}$ |
| $\widehat{V}_{s 1}$ | $V_{\text {in }}$ |
| $\widehat{V}_{D 2}$ | $V_{\text {in }}$ |

2) $b 2 E$


Figure B.15. b2E converter
Table B.8. Voltage and current relations of b2E converter

| $V_{o}$ | $D V_{\text {in }}$ |
| :---: | :---: |
| $\bar{I}_{\text {in }}$ | $D \bar{I}_{o}$ |
| $\hat{I}_{\text {in }}$ | $\bar{I}_{o}$ |
| $\bar{V}_{\boldsymbol{c}}$ | $D V_{\text {in }}$ |
| $\Delta V_{c}$ | $\frac{D \Delta I_{L 1} t_{s}}{8 C}$ |
| $\bar{I}_{L 1}$ | $\bar{I}_{o}$ |
| $\Delta I_{L 1}$ | $D(1-D) \frac{t_{s} V_{i n}}{L_{1}}$ |
| $\Delta I_{o}$ | $\frac{\Delta I_{11} D^{2} t_{s}{ }^{2}}{24 C L_{2}}$ |
| $\hat{I}_{s 1}, \hat{I}_{D 2}$ | $\bar{I}_{o}$ |
| $\widehat{V}_{s 1}, \widehat{V}_{D 2}$ | $V_{\text {in }}$ |


3) B1E


Figure B.17. B1E converter


Table B.9. Voltage and current relations of B1E converter

| $\boldsymbol{V}_{\boldsymbol{o}}$ | $\frac{1}{(1-D)} V_{i n}$ |
| :---: | :---: |
| $\overline{\boldsymbol{V}}_{\boldsymbol{c}}$ | $D V_{i n} /(1-D)$ |
| $\boldsymbol{\Delta} \boldsymbol{V}_{\boldsymbol{c}}$ | $\frac{D \Delta I_{L 2} t_{s}}{8 C}$ |
| $\overline{\boldsymbol{I}}_{\boldsymbol{i n}}$ | $\frac{\bar{I}_{o}}{(1-D)}$ |
| $\boldsymbol{\Delta} \boldsymbol{I}_{\boldsymbol{i n}}$ | $\frac{\Delta V_{o} D t_{s}}{4 L_{1}}$ |
| $\overline{\boldsymbol{I}}_{\boldsymbol{L} \boldsymbol{2}}$ | $\frac{1}{(1-D)} \bar{I}_{o}$ |
| $\boldsymbol{\Delta} \boldsymbol{I}_{\boldsymbol{L} \mathbf{2}}$ | $\frac{D t_{s} V_{i n}}{L_{2}}$ |
| $\boldsymbol{\Delta I}_{\boldsymbol{o}}$ | $\left(D t_{s} V_{i n}\right) / L_{1}$ |
| $\widehat{\boldsymbol{I}}_{\boldsymbol{s} \mathbf{1}}, \overline{\boldsymbol{I}}_{\boldsymbol{D} \mathbf{2}}$ | $\frac{\bar{I}_{o}}{(1-D)}$ |
| $\widehat{\boldsymbol{V}}_{\boldsymbol{s} \mathbf{1}}, \widehat{\boldsymbol{V}}_{\boldsymbol{D} \mathbf{2}}$ | $\frac{1}{(1-D)} V_{i n}$ |

4) B 2 E


Figure B.19. B2E converter


Figure B.20. B2E components voltages and currents.

Table B.10. Voltage and current relations of B2E converter

| $\boldsymbol{V}_{\boldsymbol{o}}$ | $\frac{1}{(1-D)} V_{i n}$ |
| :---: | :---: |
| $\overline{\boldsymbol{V}}_{\boldsymbol{c}}$ | $\frac{D \Delta I_{L 2} t_{s}}{4 C}$ |
| $\boldsymbol{\Delta} \boldsymbol{V}_{\boldsymbol{c}}$ | $\frac{\bar{I}_{o}}{(1-D)}$ |
| $\overline{\boldsymbol{I}}_{\boldsymbol{i n}}$ | $\frac{\Delta I_{L 1} D^{2} t_{s}{ }^{2}}{12 C L_{2}}$ |
| $\boldsymbol{\Delta \boldsymbol { I } _ { \boldsymbol { i n } }}$ | $\frac{1}{(1-D)} \bar{I}_{o}$ |
| $\overline{\boldsymbol{I}}_{\boldsymbol{L} \mathbf{2}}$ | $\frac{D t_{s} V_{i n}}{L_{2}}$ |
| $\boldsymbol{\Delta \boldsymbol { I } _ { \boldsymbol { L } \mathbf { 2 } }}$ | $\frac{D(1-D) t_{s} \bar{I}_{o}}{C_{o} V_{i n}}$ |
| $\boldsymbol{\Delta \boldsymbol { I } _ { \boldsymbol { o } }}$ | $\frac{\bar{I}_{o}}{(1-D)}$ |
| $\hat{\boldsymbol{I}}_{\boldsymbol{s} \mathbf{1}}, \hat{\boldsymbol{I}}_{\boldsymbol{D} \mathbf{2}}$ | $\frac{1}{(1-D)} V_{i n}$ |
| $\widehat{\boldsymbol{V}}_{\boldsymbol{s} \mathbf{1}}, \widehat{\boldsymbol{V}}_{\boldsymbol{D} \mathbf{2}}$ |  |

5) bB 1 E


Figure B.21. bB1E converter

(a) Input current $I_{\text {in }}$

(c) Output current $I_{o}$

(e) Switch $S_{l}$ current

(g) Switch $S_{l}$ forward voltage

(b) Inductor $L_{l}$ current

(d) Capacitor $C$ voltage

(f) Diode $D_{2}$ current

(h) Diode $D_{2}$ reverse voltage Figure B.22. bB1E components voltages and currents.

Table B.11. Voltage and current relations of bB1E converter

| $V_{o}$ | $\frac{D}{(1-D)} V_{i n}$ |
| :---: | :---: |
| $\bar{V}_{c}$ | $D V_{\text {in }} /(1-D)$ |
| $\Delta V_{c}$ | $\underline{D \Delta I_{L 1} t_{S}}$ |
| $\bar{I}_{\text {in }}$ | $\begin{gathered} \hline 4 \bar{C} \\ \frac{D \bar{I}_{o}}{(1-D)} \end{gathered}$ |
| $\hat{I}_{\text {in }}$ | $\bar{I}_{o} /(1-D)$ |
| $\bar{I}_{L 1}$ | $\frac{\bar{I}_{o}}{(1-D)}$ |
| $\Delta I_{L 1}$ | $\frac{D t_{s} V_{i n}}{L_{1}}$ |
| $\Delta I_{o}$ | $\frac{(1-D) t_{s} \bar{I}_{o}^{2}}{C_{o} V_{i n}}$ |
| $\hat{I}_{s 1}, \hat{I}_{D 2}$ | $\frac{\bar{I}_{o}}{(1-D)}$ |
| $\widehat{V}_{s 1}, \widehat{V}_{D 2}$ | $\frac{1}{(1-D)} V_{i n}$ |

6) bB 2 E


Figure B.23. bB2E converter


Figure B.24. bB2E components voltages and currents.

Table B.12. Voltage and current relations of bB2E converter

| $\boldsymbol{V}_{\boldsymbol{o}}$ | $\frac{D}{(1-D)} V_{i n}$ |
| :---: | :---: |
| $\overline{\boldsymbol{V}}_{\boldsymbol{c}}$ | $\frac{V_{i n}}{\boldsymbol{V}_{\boldsymbol{c}}}$ |
| $\overline{\boldsymbol{I}}_{\boldsymbol{i n}}$ | $\frac{D \Delta I_{L 1} t_{s}}{4 C}$ |
| $\hat{\boldsymbol{I}}_{\boldsymbol{i n}}$ | $\frac{D \bar{I}_{o}}{(1-D)}$ |
| $\overline{\boldsymbol{I}}_{\boldsymbol{L} \mathbf{1}}$ | $\bar{I}_{o} /(1-D)$ |
| $\boldsymbol{\Delta} \boldsymbol{I}_{\boldsymbol{L} \mathbf{1}}$ | $\bar{I}_{o} /(1-D)$ |
| $\boldsymbol{\Delta \boldsymbol { I } _ { \boldsymbol { o } }}$ | $\frac{D t_{s} V_{i n}}{L_{1}}$ |
| $\hat{\boldsymbol{I}}_{\boldsymbol{s} \mathbf{1}}, \hat{\boldsymbol{I}}_{\boldsymbol{D} \mathbf{2}}$ | $\frac{(1-D) t_{s} \bar{I}_{o}^{2}}{C_{o} V_{i n}}$ |
| $\widehat{\boldsymbol{V}}_{\boldsymbol{s} \mathbf{1}}, \widehat{\boldsymbol{V}}_{\boldsymbol{D} \mathbf{2}}$ | $\frac{\bar{I}_{o}}{(1-D)}$ |

## B. 3 Cell F

1) b 1 F


Figure B.25. b1F converter
Table B.13. Voltage and current relations of b1F converter

| $V_{o}$ | $D V_{\text {in }}$ |
| :---: | :---: |
| $\bar{I}_{\text {in }}$ | $D \bar{I}_{o}$ |
| $\hat{I}_{\text {in }}$ | $\bar{I}_{o}$ |
| $\bar{V}_{c}$ | $D V_{\text {in }}$ |
| $\Delta V_{c}$ | $D(1-D) \frac{\bar{I}_{o} t_{s}}{C}$ |
| $\bar{I}_{L 1}$ | $\bar{I}_{o}$ |
| $\Delta I_{L 1}$ | $D(1-D) t_{s} V_{i n} / L_{1}$ |
| $\Delta I_{o}$ | $\underline{(1-D) t_{s} \bar{I}_{o}{ }^{2}}$ |
|  | $C_{o} V_{\text {in }}$ |
| $\hat{I}_{s 1}, \hat{I}_{\text {D }}$ | $\bar{I}_{0}$ |
| $\widehat{V}_{s 1}, \widehat{V}_{D 2}$ | $V_{\text {in }}$ |


(a) Input current $I_{\text {in }}$

(c) Inductor $L_{2}$ current

(b) Inductor $L_{1}$ current

(d) Output current $I_{o}$

(e) Capacitor $C$ voltage

(f) Switch $S_{l}$ current

(h) Switch $S_{l}$ forward voltage

(g) Diode $D_{2}$ current

(i) Diode $D_{2}$ reverse voltage

Figure B.26. b2F components voltages and currents.
2) $b 2 F$


Figure B.27. b2F converter


Figure B.28. b2F components voltages and currents.
Table B.14. Voltage and current relations of b2F converter

| $\boldsymbol{V}_{\boldsymbol{o}}$ | $D V_{i n}$ |
| :---: | :---: |
| $\overline{\boldsymbol{I}}_{\boldsymbol{i n}}$ | $\frac{\left(\bar{I}_{o}\right.}{}$ |
| $\boldsymbol{\Delta \boldsymbol { I } _ { \boldsymbol { i n } }}$ | $\frac{(1-D) \Delta V_{c} t_{s}}{4 L_{1}}$ |
| $\overline{\boldsymbol{V}}_{\boldsymbol{c}}$ | $(1-D) V_{i n}$ |
| $\boldsymbol{\Delta \boldsymbol { V } _ { \boldsymbol { c } }}$ | $D(1-D) \frac{\bar{I}_{o} t_{s}}{C}$ |
| $\overline{\boldsymbol{I}}_{\boldsymbol{L} \boldsymbol{2}}$ | $\bar{I}_{o}$ |
| $\boldsymbol{\Delta \boldsymbol { I } _ { \boldsymbol { L } 2 }}$ | $\frac{D(1-D) t_{s} V_{i n}}{L_{2}}$ |
| $\boldsymbol{\Delta \boldsymbol { I } _ { \boldsymbol { o } }}$ | $\frac{D(1-D) t_{s} \bar{I}_{o}{ }^{2}}{C_{o} V_{i n}}$ |
| $\bar{I}_{o}$ |  |
| $\widehat{\boldsymbol{I}}_{\boldsymbol{s} \mathbf{1}}, \hat{\boldsymbol{I}}_{\boldsymbol{D} \mathbf{2}}$ | $V_{\text {in }}$ |
| $\widehat{\boldsymbol{V}}_{\boldsymbol{s} \mathbf{1}}, \widehat{\boldsymbol{V}}_{\boldsymbol{D} \mathbf{2}}$ |  |

3) B 1 F


Figure B.29. B1F converter


Table B.15. Voltage and current relations of B1F converter

| $V_{o}$ | $\frac{1}{(1-D)} V_{i n}$ |
| :---: | :---: |
| $\bar{V}_{c}$ | $V_{\text {in }}$ |
| $\Delta V_{c}$ | $D \frac{\bar{I}_{o} t_{s}}{C}$ |
| $\bar{I}_{\text {in }}$ | $\frac{\bar{I}_{o}}{(1-D)}$ |
| $\hat{I}_{\text {in }}$ | $\frac{1-D^{2}}{(1-D)^{2}} \bar{I}_{o}$ |
| $\check{I ̇}_{\text {in }}$ | $\frac{D}{(1-D)} \bar{I}_{o}$ |
| $I_{L 1}$ | $\frac{\bar{I}_{o}}{(1-D)}$ |
| $\Delta I_{L 1}$ | $\frac{D t_{s} V_{i n}}{L_{1}}$ |
| $I_{L 2}$ | $\frac{D}{(1-D)} \bar{I}_{o}$ |
| $\Delta I_{L 2}$ | $\frac{D \Delta V_{c} t_{s}}{4 L_{2}}$ |
| $\Delta I_{o}$ | $\frac{D(1-D) t_{s} \bar{I}_{o}^{2}}{C_{o} V_{i n}}$ |
| $\widehat{I}_{s 1}, \widehat{I}_{D 2}$ | $\frac{\bar{I}_{o}}{(1-D)}$ |
| $\widehat{V}_{s 1}, \widehat{V}_{D 2}$ | $\frac{1}{(1-D)} V_{i n}$ |

4) B 2 F


Figure B.31. B2F converter


Figure B.32. B2F components voltages and currents.
Table B.16. Voltage and current relations of B2F converter

| $V_{o}$ | $\frac{1}{(1-D)} V_{i n}$ |
| :---: | :---: |
| $\bar{V}_{\boldsymbol{c}}$ | $\frac{D}{(1-D)} V_{i n}$ |
| $\Delta V_{c}$ | $D \frac{\bar{I}_{o} t_{s}}{C}$ |
| $\widehat{I}_{\text {in }}$ | $\frac{2-D}{1-D} \bar{I}_{o}$ |
| $\check{I ̇}_{\text {in }}$ | $\bar{I}_{0}$ |
| $I_{L 1}$ | $\frac{\bar{I}_{o}}{(1-D)}$ |
| $\Delta I_{L 1}$ | $\frac{D t_{s} V_{i n}}{L_{1}}$ |
| $\Delta I_{o}$ | $\frac{D(1-D) t_{s} \bar{I}_{o}^{2}}{C_{o} V_{i n}}$ |
| $\hat{I}_{s 1}, \hat{I}_{D 2}$ | $\bar{I}_{o} /(1-D)$ |
| $\widehat{V}_{s 1}, \widehat{V}_{D 2}$ | $\frac{1}{(1-D)} V_{i n}$ |

5) bB 1 F


Figure B.33. bB1F converter


Figure B.34. bB1F components voltages and currents.

Table B.17. Voltage and current relations of bB1F converter

| $\boldsymbol{V}_{\boldsymbol{o}}$ | $\frac{D}{(1-D)} V_{i n}$ |
| :---: | :---: |
| $\overline{\boldsymbol{V}}_{\boldsymbol{c}}$ | $\frac{V_{i n}}{\bar{I}_{o} t_{s}}$ |
| $\boldsymbol{\Delta} \boldsymbol{V}_{\boldsymbol{c}}$ | $\frac{D \bar{I}_{o}}{(1-D)}$ |
| $\overline{\boldsymbol{I}}_{\boldsymbol{i n}}$ | $\frac{D \Delta V_{c} t_{s}}{4 L_{1}}$ |
| $\boldsymbol{\Delta} \boldsymbol{I}_{\boldsymbol{i n}}$ | $\bar{I}_{o} /(1-D)$ |
| $\overline{\boldsymbol{I}}_{\boldsymbol{L} \mathbf{2}}$ | $\frac{D t_{s} V_{i n}}{L_{2}}$ |
| $\boldsymbol{\Delta \boldsymbol { I } _ { \boldsymbol { L } \mathbf { 2 } }}$ | $\frac{(1-D) t_{s} \bar{I}_{o}}{C_{o} V_{i n}}$ |
| $\boldsymbol{\Delta \boldsymbol { I } _ { \boldsymbol { o } }}$ | $\frac{\bar{I}_{o}}{(1-D)}$ |
| $\hat{\boldsymbol{I}}_{\boldsymbol{s} \mathbf{1}}, \hat{\boldsymbol{I}}_{\boldsymbol{D} \mathbf{2}}$ | $\frac{1}{(1-D)} V_{i n}$ |
| $\widehat{\boldsymbol{V}}_{\boldsymbol{s} \mathbf{1}}, \widehat{\boldsymbol{V}}_{\boldsymbol{D} \mathbf{2}}$ |  |

6) bB 2 F


Figure B.35. bB2F converter
Table B.18. Voltage and current relations of bB2F converter

| $V_{o}, \bar{V}_{c}$ | $\frac{D}{(1-D)} V_{i n}$ |
| :---: | :---: |
| $\Delta V_{c}$ | $D \frac{\bar{I}_{o} t_{s}}{\underline{C}}$ |
| $\bar{I}_{\text {in }}$ | $\frac{D \breve{I}_{o}}{(1-D)}$ |
| $\hat{I}_{\text {in }}$ | $\bar{I}_{o} /(1-D)$ |
| $\bar{I}_{L 1}$ | $\bar{I}_{o} /(1-D)$ |
| $\Delta I_{L 1}$ | $\frac{D t_{s} V_{i n}}{L_{1}}$ |
| $\Delta I_{o}$ $\hat{I}_{s 1}, \hat{I}_{D 2}$ | $\begin{gathered} \frac{(1-D) \Delta V_{c} t_{s}}{4 L_{2}} \\ \frac{\bar{I}_{o}}{(1-D)} \end{gathered}$ |
| $\widehat{V}_{s 1}, \widehat{V}_{D 2}$ | $\frac{1}{(1-D)} V_{i n}$ |



## B. 4 Cell G

1) b 1 G


Figure B.37. b1G converter


Table B.19. Voltage and current relations of b1G converter

| $V_{o}$ | $\frac{2 D-1}{D} V_{i n}$ |
| :---: | :---: |
| $\bar{V}_{c}$ | $V_{\text {in }}$ |
| $\Delta V_{c}$ | $(1-D) \bar{I}_{o} t_{s} / C$ |
| $\widehat{I}_{\text {in }}$ and ${ }_{\text {In }}^{\text {in }}$ | $\bar{I}_{o}$ and $-(1-D) \bar{I}_{o} / D$ |
| $I_{L 1}$ | $\bar{I}_{o}$ |
| $\Delta I_{L 1}$ | $(1-D) t_{s} V_{i n} / L_{1}$ |
| $\Delta I_{o}$ | $\frac{D(1-D) t_{S} \bar{I}_{o}^{2}}{C_{o} V_{i n}(2 D-1)}$ |
| $\hat{I}_{s 1}, \hat{I}_{D 2}$ | $\bar{I}_{o} / D$ |
| $\widehat{V}_{S 1}, \widehat{V}_{D 2}$ | $V_{\text {in }} / D$ |

2) $b 2 G$


Figure B.39. b2G converter


Figure B.40. b2G components voltages and currents.
Table B.20. Voltage and current relations of b2G converter

| $V_{o}$ | $(2 D-1) / D V_{i n}$ |
| :---: | :---: |
| $\bar{V}_{c}$ | $(1-D) / D V_{i n}$ |
| $\widehat{I}_{\text {in }}$ and ${ }_{\text {In }}^{\text {in }}$ | $\bar{I}_{o}$ and $-(1-D) / D \bar{I}_{o}$ |
| $I_{L 1}$ | $(1-D) / D \bar{I}_{o}$ |
| $\Delta I_{L 1}$ | $(1-D) \frac{t_{s} V_{i n}}{L_{1}}$ |
| $\Delta I_{o}$ | $\Delta I_{o}=(1-D) \frac{t_{s} V_{i n}}{L_{2}}$ |
| $\hat{I}_{s 1}, \hat{I}_{D 2}$ | $\bar{I}_{o} / D$ |
| $\widehat{V}_{s 1}, \widehat{V}_{D 2}$ | $V_{\text {in }} / D$ |

3) B 1 G


Figure B.41. B1G converter

(a) Input current $I_{i n}$

(c) Inductor $L_{2}$ current

(b) Inductor $L_{1}$ current

(d) Output current $I_{o}$

(e) Capacitor $C$ voltage

(f) Switch $S_{l}$ current

(h) Switch $S_{l}$ forward voltage

(g) Diode $D_{2}$ current

(i) Diode $D_{2}$ reverse voltage Figure B.42. B1G components voltages and currents.

Table B.21. Voltage and current relations of B1G converter

| $V_{o}$ | $\frac{1-D}{1-2 D} V_{i n}$ |
| :---: | :---: |
| $\bar{V}_{c}$ | $\frac{(1-D)}{(1-2 D)} V_{i n}$ |
| $\Delta V_{c}$ | $\frac{D(1-D)}{(1-2 D)} \frac{I_{o} t_{s}}{C}$ |
| $\widehat{I}_{\text {in }}$ and ${ }_{\text {In }}^{\text {in }}$ | $\bar{I}_{o}$ and $-(1-D) \bar{I}_{o} / D$ |
| $I_{L 1}$ | $\frac{(1-D)}{(1-2 D)} \bar{I}_{o}$ |
| $\Delta I_{L 1}$ | $\frac{D(1-D)}{(1-2 D)} \frac{t_{s} V_{i n}}{L_{1}}$ |
| $I_{L 2}$ | $\frac{D}{(1-2 D)} \bar{I}_{o}$ |
| $\Delta I_{L 2}$ | $\frac{D(1-D)}{(1-2 D)} \frac{t_{s} V_{i n}}{L_{2}}$ |
| $\Delta I_{0}$ | $\frac{D t_{s} \bar{I}_{o}^{2}}{C_{o} V_{i n}}$ |
| $\hat{I}_{s 1}, \hat{I}_{D 2}$ | $\frac{\bar{I}_{o}}{(1-2 D)}$ |
| $\widehat{V}_{s 1}, \widehat{V}_{D 2}$ | $\frac{V_{i n}}{(1-2 D)}$ |

4) B 2 G


Figure B.43. B2G converter

(a) Input current $I_{i n}$

(c) Output current $I_{o}$

(e) Switch $S_{l}$ current

(g) Switch $S_{l}$ forward voltage

(b) Inductor $L_{2}$ current

(d) Capacitor $C$ voltage

(f) Diode $D_{2}$ current

(h) Diode $D_{2}$ reverse voltage Figure B.44. B2G components voltages and currents.

Table B.22. Voltage and current relations of B2G converter

| $V_{o}$ | $\frac{1-D}{1-2 D} V_{i n}$ |
| :---: | :---: |
| $\bar{V}_{c}$ | $\frac{D}{(1-2 D)} V_{i n}$ |
| $\Delta V_{c}$ | $\frac{D(1-D)}{(1-2 D)} \frac{I_{o} t_{s}}{C}$ |
| $\overline{\mathbf{I}}_{\text {in }}$ and $^{\text {a }}{ }_{\text {in }}$ | $\frac{(1-D)}{(1-2 D)} \bar{I}_{o} \text { and } \frac{D(1-D)}{(1-2 D)} \frac{t_{s} V_{i n}}{L_{1}}$ |
| $I_{L 2}$ | $\frac{D}{(1-2 D)} \bar{I}_{o}$ |
| $\Delta I_{L 1}$ | $\frac{D(1-D)}{(1-2 D)} \frac{t_{s} V_{i n}}{L_{1}}$ |
| $I_{L 2}$ | $\frac{D(1-D)}{(1-2 D)} \frac{t_{s} V_{i n}}{L_{2}}$ |
| $\Delta I_{o}$ $\hat{I}_{s 1}, \hat{I}_{D 2}$ | $\frac{D t_{s} \bar{I}_{o}^{2}}{C_{o} V_{i n}}$ |
| $1_{s 1}, 1_{D 2}$ | $\frac{I_{0}}{(1-2 D)}$ |
| $\widehat{V}_{S 1}, \widehat{V}_{D 2}$ | $\frac{V_{\text {in }}}{(1-2 D)}$ |

5) bB 1 G


Figure B.45. bB1G converter


Figure B.46. bB1F components voltages and currents.

Table B.23. Voltage and current relations of bB1G converter

| $V_{o}$ | $\frac{D}{(1-D)} V_{i n}$ |
| :---: | :---: |
| $\bar{V}_{c}$ | $V_{\text {in }}$ |
| $\Delta V_{c}$ | $D \frac{\bar{I}_{0} t_{s}}{C}$ |
| $\bar{I}_{\text {in }}$ | $\frac{\check{I}_{o}}{(1-D)}$ |
| $\Delta I_{\text {in }}$ | $\frac{D t_{s} V_{i n}}{L_{1}}$ |
| $\bar{I}_{L 2}$ | $\bar{I}_{o}$ |
| $\Delta I_{L 2}$ | $\frac{D t_{s} V_{i n}}{L_{2}}$ |
| $\Delta I_{o}$ | $\frac{D t_{s} \bar{I}_{o}^{2}}{C_{o} V_{i n}}$ |
| $\hat{I}_{s 1}, \hat{I}_{D 2}$ | $\frac{\bar{I}_{o}}{(1-D)}$ |
| $\widehat{V}_{s 1}, \widehat{V}_{D 2}$ | $\frac{1}{(1-D)} V_{i n}$ |

6) bB 2 G


Figure B.47.bB2G converter
Table B.24. Voltage and current relations of bB2G converter

| $\boldsymbol{V}_{\boldsymbol{o}}, \overline{\boldsymbol{V}}_{\boldsymbol{c}}$ | $\frac{D}{(1-D)} V_{\text {in }}$ |
| :---: | :---: |
| $\boldsymbol{\Delta} \boldsymbol{V}_{\boldsymbol{c}}$ | $D \frac{\bar{o}_{o} t_{s}}{C}$ |
| $\overline{\boldsymbol{I}}_{\boldsymbol{i n}}$ | $\frac{D \bar{I}_{o}}{(1-D)}$ |
| $\hat{\boldsymbol{I}}_{\boldsymbol{i n}}$ | $\bar{I}_{o} /(1-D)$ |
| $\overline{\boldsymbol{I}}_{\boldsymbol{L} \mathbf{1}}$ | $D \bar{I}_{o} /(1-D)$ |
| $\boldsymbol{\Delta} \boldsymbol{I}_{\mathbf{L} \mathbf{1}}$ | $\frac{D t_{s} V_{i n}}{L_{1}}$ |
| $\boldsymbol{\Delta \boldsymbol { I } _ { \boldsymbol { o } }}$ | $D t_{s} V_{i n} / L_{2}$ |
| $\widehat{\boldsymbol{I}}_{\boldsymbol{s} \mathbf{1}}, \widehat{\boldsymbol{I}}_{\boldsymbol{D} \mathbf{2}}$ | $\frac{\bar{I}_{o}}{(1-D)}$ |
| $\widehat{\boldsymbol{V}}_{\boldsymbol{s} \mathbf{1}}, \widehat{\boldsymbol{V}}_{\boldsymbol{D} \mathbf{2}}$ | $\frac{1}{(1-D)} V_{i n}$ |


(a) Input current $I_{i n}$

(c) Output current $I_{o}$

(e) Switch $S_{l}$ current

(g) Switch $S_{l}$ forward voltage

(b) Inductor $L_{l}$ current

(d) Capacitor $C$ voltage

(f) Diode $D_{2}$ current

(h) Diode $D_{2}$ reverse voltage

Figure B.48. bB2G components voltages and currents.

## B. 5 Full derivation of b1P converter

1) Average values calculations


Figure B.49. b1P during:(a) $t_{o n}$, and (b) $t_{o f f}$
The circuit configurations of b1P converter during S1 on and off durations are shown in Figure B.49. Applying KCL and KVL to these circuit configurations:
i) during $t_{o n}$

$$
\begin{align*}
& \frac{d i_{L 1}}{d t}=\frac{1}{L_{l}}\left(V_{i n}-V_{o}\right) \\
& \frac{d V_{c}}{d t}=\frac{1}{C} i_{L 2}  \tag{B.1}\\
& \frac{d i_{L 2}}{d t}=\frac{1}{L_{2}}\left(V_{i n}-V_{c}-V_{o}\right) \\
& \frac{d V_{o}}{d t}=\frac{1}{C_{o}}\left(i_{L 1}+i_{L 2}-\frac{V_{o}}{R}\right)
\end{align*}
$$

ii) during $t_{\text {off }}$

$$
\begin{align*}
& \frac{d i_{L 1}}{d t}=\frac{1}{L_{l}}\left(V_{c}-V_{o}\right) \\
& \frac{d V_{c}}{d t}=\frac{-1}{C} i_{L 1}  \tag{B.2}\\
& \frac{d i_{L 2}}{d t}=\frac{-1}{L_{2}} V_{o} \\
& \frac{d V_{o}}{d t}=\frac{1}{C_{o}}\left(i_{L 1}+i_{L 2}-\frac{V_{o}}{R}\right)
\end{align*}
$$

The average state space model is expressed as:

$$
\left[\begin{array}{c}
\dot{I}_{L 1}  \tag{B.3}\\
\dot{V_{c}} \\
\dot{I_{L 2}} \\
\dot{V_{o}}
\end{array}\right]=\left[\begin{array}{cccc}
0 & \frac{1-D}{L_{l}} & 0 & -\frac{1}{L_{l}} \\
\frac{-(1-D)}{C} & 0 & \frac{D}{C} & 0 \\
0 & \frac{-D}{L_{2}} & 0 & \frac{-1}{L_{2}} \\
\frac{1}{C_{o}} & 0 & \frac{1}{C_{o}} & \frac{-1}{R C_{o}}
\end{array}\right]\left[\begin{array}{l}
I_{L 1} \\
V_{c} \\
I_{L 2} \\
V_{o}
\end{array}\right]+\left[\begin{array}{c}
\frac{D}{L_{1}} \\
0 \\
\frac{D}{L_{2}} \\
0
\end{array}\right]\left[\begin{array}{l}
\left.V_{i n}\right]
\end{array}\right.
$$

At the steady state, the derivatives of the states can be set to zero:

$$
\left[\begin{array}{l}
0  \tag{B.4}\\
0 \\
0 \\
0
\end{array}\right]=\left[\begin{array}{cccc}
0 & \frac{1-D}{L_{1}} & 0 & -\frac{1}{L_{1}} \\
\frac{-(1-D)}{C} & 0 & \frac{D}{C} & 0 \\
0 & \frac{-D}{L_{2}} & 0 & \frac{-1}{L_{2}} \\
\frac{1}{C_{o}} & 0 & \frac{1}{C_{o}} & \frac{-1}{R C_{o}}
\end{array}\right]\left[\begin{array}{l}
I_{L 1} \\
V_{c} \\
I_{L 2} \\
V_{o}
\end{array}\right]+\left[\begin{array}{c}
\frac{D}{L_{1}} \\
0 \\
\frac{D}{L_{2}} \\
0
\end{array}\right]\left[\begin{array}{l}
\left.V_{i n}\right]
\end{array}\right]
$$

Solving the row equations in terms of $D, V_{i n}$ and $I_{o}$ leads to:

$$
\begin{gather*}
V_{o}=D V_{i n}  \tag{B.5}\\
\overline{V_{c}}=0  \tag{B.6}\\
\bar{I}_{L 1}=D I_{o}  \tag{B.7}\\
\bar{I}_{L 2}=(1-D) I_{o} \tag{B.8}
\end{gather*}
$$

## 2) Ripples calculations:

The voltage ripple across C capacitor $\left(\Delta V_{c}\right)$ can be calculated during $t_{o n}$ from:

$$
\begin{equation*}
\frac{d V_{c}}{d t}=\frac{1}{C} i_{L 2} \tag{B.9}
\end{equation*}
$$

Assuming $t_{o n}$ is very short duration:

$$
\begin{equation*}
\frac{\Delta V_{c}}{\Delta t}=\frac{1}{C} \bar{I}_{L 2} \tag{B.10}
\end{equation*}
$$

Then,

$$
\begin{equation*}
\Delta V_{c}=\frac{D(1-D) t_{s}}{C} I_{o} \tag{B.11}
\end{equation*}
$$

The current ripple through $L_{l}$ inductor $\left(\Delta I_{L I}\right)$ can be calculated during $t_{o n}$ from:

$$
\begin{align*}
& \frac{d i_{L 1}}{d t}=\frac{1}{L_{l}}\left(V_{i n}-V_{o}\right)  \tag{B.12}\\
& \Delta I_{L 1}=\frac{1}{L_{l}}\left(V_{i n}-V_{o}\right) \tag{B.13}
\end{align*}
$$

Then,

$$
\begin{equation*}
\Delta I_{L l}=\frac{D(1-D) t_{s}}{L_{l}} V_{i n} \tag{B.14}
\end{equation*}
$$

Similarly, the current ripple through $L_{2}$ inductor $\left(\Delta I_{L 2}\right)$ can be calculated during $t_{\text {off }}$ from:

$$
\begin{equation*}
\frac{d i_{L 2}}{d t}=\frac{-1}{L_{2}} V_{o} \tag{B.15}
\end{equation*}
$$

$$
\begin{equation*}
-\Delta I_{L 2}=\frac{-V_{o}}{L_{2}} t_{o f f} \tag{B.16}
\end{equation*}
$$

$$
\begin{equation*}
\Delta I_{L 2}=\frac{D(1-D) t_{s}}{L_{2}} V_{i n} \tag{B.17}
\end{equation*}
$$

## Appendix C

## Analysis and Experimental Results of Several Boost and Buck-boost Converters

## C. 1 B1D

The two circuit configuration during ON and OFF periods are shown in Figure C. 1 The converter models and transfer function are stated in (C.1), (C.2) and (C.3). The single-phase and three-phase inverters emerging from the B1D converter are shown in Figure C. 2 and Figure C.3. Operation of the dc converter and dc/ac inverters are shown in Figure C.4, Figure C. 5 and Figure C. 6 respectively.


Figure C.1. Two configurations of B1D converter: (a) $t_{o n}$ and (b) $t_{o f f}$.


Figure C.2. B1D single-phase inverter.

$$
\begin{align*}
& {\left[\begin{array}{c}
\dot{I}_{i n} \\
\dot{V_{c}} \\
\dot{I}_{L 2}
\end{array}\right]=\left[\begin{array}{ccc}
\frac{-\left(R+r_{l}\right)}{L_{l}} & \frac{D}{L_{l}} & \frac{R}{L_{l}} \\
\frac{-D}{C} & 0 & \frac{1}{C} \\
\frac{R}{L_{2}} & \frac{-1}{L_{2}} & \frac{-\left(R+r_{2}\right)}{L_{2}}
\end{array}\right]\left[\begin{array}{l}
I_{\text {in }} \\
V_{c} \\
I_{L 2}
\end{array}\right]+\left[\begin{array}{l}
\frac{1}{L_{1}} \\
0 \\
0
\end{array}\right]\left[\begin{array}{l}
\left.V_{i n}\right]
\end{array}\right.} \\
& {\left[\begin{array}{c}
\dot{\tilde{I}}_{i n} \\
\dot{\tilde{V}}_{c} \\
\dot{\tilde{I}}_{L 2}
\end{array}\right]=\left[\begin{array}{ccc}
\frac{-\left(R+r_{l}\right)}{L_{l}} & \frac{D_{e}}{L_{l}} & \frac{R}{L_{l}} \\
\frac{-D_{e}}{C} & 0 & \frac{1}{C} \\
\frac{R}{L_{2}} & \frac{-1}{L_{2}} & \frac{-\left(R+r_{2}\right)}{L_{2}}
\end{array}\right]\left[\begin{array}{c}
\tilde{I}_{i n} \\
\tilde{V}_{c} \\
\tilde{I}_{L 2}
\end{array}\right]+\left[\begin{array}{c}
\frac{V_{\text {in }}}{L_{l}\left(1-D_{e}\right)} \\
\frac{-V_{\text {in }}}{R C\left(1-D_{e}\right)^{2}} \\
0
\end{array}\right][\delta]} \\
& G(s)=\frac{\tilde{V_{o}}(s)}{\delta(s)}=\frac{a_{2} s^{2}+a_{1} s+a_{0}}{b_{3} s^{3}+b_{2} s^{2}+b_{1} s+b_{0}} \\
& a_{2}=C L_{2} R V_{i n}\left(1-D_{e}\right) \\
& a_{1}=C R V_{i n} r_{2}\left(1-D_{e}\right)-V_{\text {in }}\left(L_{1}+D_{e} L_{2}\right) \\
& a_{0}=R V_{\text {in }}\left(1-D_{e}\right)^{2}-V_{\text {in }}\left(r_{1}+D_{e} r_{2}\right)  \tag{C.3}\\
& b_{3}=C L_{1} L_{2}\left(1-D_{e}\right)^{2} \\
& b_{2}=C\left(1-D_{e}\right)^{2}\left[\left(L_{1}+L_{2}\right)+L_{1} r_{2}+L_{2} r_{1}\right] \\
& b_{1}=\left(1-D_{e}\right)^{2}\left[L_{1}+L_{2} D_{e}{ }^{2}+C R\left(r_{1}+r_{2}\right)+C r_{1} r_{2}\right] \\
& b_{0}=\left(1-D_{e}\right)^{2}\left[R\left(1-D_{e}\right)^{2}+r_{1}+D_{e}{ }^{2} r_{2}\right]
\end{align*}
$$

Figure C.3. B1D three-phase inverter.
 plot (c) $V_{c}$ at $\mathrm{D}=0.5$, (d) $I_{i n}$ at $\mathrm{D}=0.5$, (e) output voltage $V_{o}$ with square wave reference. ( $C$ $=10 \mu \mathrm{~F}, L_{l}=L_{2}=1 \mathrm{mH}$, and $\mathrm{R}=22 \Omega$ ).


Figure C.5. Operation of B1D in dc/ac mode (single-phase) at $V_{i n}=50 \mathrm{~V}$ and ( $I_{o}^{\text {ref }} R=$ 100sinot: (a) control structure, (b) PR-controlled system Bode plot (c) $I_{1}$ and $I_{2}$, (d) capacitor voltage $V_{c l}$, and (e) output voltage $\left.V_{o}\right) .\left(C=5 \mu \mathrm{~F}, L_{l}=L_{2}=1 \mathrm{mH}\right.$, and $\left.\mathrm{R}=22 \Omega\right)$

(a)

(b)

$50 \mathrm{~V} /$ div $-5 \mathrm{~ms} /$ div
(c)

Figure C.6. Operation of B1D in dc/ac mode (three-phase) at $V_{i n}=50 \mathrm{~V}, V_{m}=100$ : (a) $I_{i n}$, (b) capacitors voltages $V_{c 1}-V_{c 2}-V_{c 3}$ (c) load voltages ( $V_{o 1}-V_{o 2}-V_{o 3}$ ).

## C. 2 B2D

The two circuit configuration during ON and OFF periods are shown in Figure C.7. The converter models and transfer function are stated in equation sets (C.4), (C.5) and (C.6). The single-phase and three-phase inverters emerging from the B1D converter are shown in Figure C. 8 and Figure C.9. The operation of the dc converter and dc/ac inverters are shown in Figure C.10, Figure C. 11 and Figure C. 12 respectively.


Figure C.7. Two configurations of B2D converter: (a) $t_{o n}$ and (b) $t_{o f f}$.

$$
\begin{align*}
& {\left[\begin{array}{l}
\dot{I}_{i n} \\
\dot{V}_{c} \\
\dot{I}_{o}
\end{array}\right]=\left[\begin{array}{ccc}
\frac{-r_{1}}{L_{l}} & \frac{D-1}{L_{l}} & 0 \\
\frac{1-D}{C} & 0 & \frac{-1}{C} \\
0 & \frac{1}{L_{2}} & \frac{-\left(R+r_{2}\right)}{L_{2}}
\end{array}\right]\left[\begin{array}{l}
I_{\text {in }} \\
V_{c} \\
I_{o}
\end{array}\right]+\left[\begin{array}{c}
\frac{1}{L_{l}} \\
0 \\
0
\end{array}\right]\left[V_{\text {in }}\right]} \tag{C.4}
\end{align*}
$$

$$
\begin{align*}
& G(s)=\frac{\tilde{V_{o}}(s)}{\delta(s)}=\frac{a_{l} s+a_{0}}{b_{3} s^{3}+b_{2} s^{2}+b_{l} s+b_{0}} \\
& a_{l}=R V_{\text {in }}\left(1-D_{e}\right)^{2}-r_{I} V_{\text {in }} \\
& a_{0}=R V_{\text {in }}\left(1-D_{e}\right)^{2}-V_{\text {in }}\left(r_{1}+D_{e} r_{2}\right) \\
& b_{3}=C L_{1} L_{2}\left(1-D_{e}\right)^{2}  \tag{C.6}\\
& b_{2}=C\left(1-D_{e}\right)^{2}\left[L_{l}\left(R+r_{2}\right)+L_{1} R\right] \\
& b_{l}=\left(1-D_{e}\right)^{2}\left[L_{2}\left(l-D_{e}\right)^{2}+L_{l}+C R r_{1}+C r_{1} r_{2}\right] \\
& b_{0}=\left(1-D_{e}\right)^{2}\left[R\left(1-D_{e}\right)^{2}+r_{1}+r_{2}\left(1-D_{e}\right)^{2}\right]
\end{align*}
$$

Figure C.8. B2D single-phase inverter.


Figure C.9. B2D three-phase inverter.

(a) $G_{p i}{ }^{*} G_{c l}\left(K_{p}=1, K_{i}=10\right.$ and $\left.K=20\right)$

(c)

(b)

(b)

Figure C.10. Operation of B2D in dc/dc mode at $V_{i n}=50 \mathrm{~V}$ : (a) PI-controlled system Bode plot (c) $V_{c}$ at $\mathrm{D}=0.5$, (d) $I_{i n}$ at $\mathrm{D}=0.5$, (e) output voltage $V_{o}$ with square wave reference. ( $C=10 \mu \mathrm{~F}, L_{1}=L_{2}=1 \mathrm{mH}$, and $\mathrm{R}=22 \Omega$ ).


Figure C.11. Operation of B2D in dc/ac mode (single-phase) at $V_{\text {in }}=50 \mathrm{~V}$ and ( $I_{o}^{\text {ref }} \cdot R=$ 100sin 1 : (a) control structure, (b) PR-controlled system Bode plot (c) $I_{1}$ and $I_{2}$, (d) capacitor voltage $V_{c l}$, and (e) output voltage $\left.V_{o}\right)$. $\left(C=5 \mu \mathrm{~F}, L_{l}=L_{2}=1 \mathrm{mH}\right.$, and $\left.\mathrm{R}=22 \Omega\right)$.


Figure C.12. Operation of B1D in dc/ac mode (three-phase) at $V_{i n}=50 \mathrm{~V}, V_{m}=100$ : (a) $I_{i n}$, (b) Capacitors voltages $V_{c 1}-V_{c 2}-V_{c 3}$, and (c) Load voltages $\left(V_{o 1}-V_{o 2}-V_{o 3}\right)$.

## C. 3 B2E

The two circuit configurations during ON and OFF states are shown in Figure C.13. The converter large and small signal models and transfer function are stated in (C.7), (C.8) and (C.9). The single-phase and three-phase inverters emerging from the B2E converter are shown in Figure C. 14 and Figure C. 15 respectively. The operation of the dc converter and dc/ac inverters are shown in Figure C.16, Figure C. 17 and Figure C. 18 respectively.


Figure C.13. Two configurations of B2E converter: (a) $t_{o n}$ and (b) $t_{o f f}$.


Figure C.14. B2E single-phase inverter.


Figure C.15. B2E three-phase inverter.

$$
\begin{align*}
& {\left[\begin{array}{l}
\dot{I}_{i n} \\
\dot{V_{c}} \\
\dot{I}_{L 2} \\
\dot{V_{o}}
\end{array}\right]=\left[\begin{array}{cccc}
\frac{-r_{l}}{L_{l}} & \frac{-1}{L_{l}} & 0 & 0 \\
\frac{1}{C} & 0 & \frac{-1}{C} & 0 \\
0 & \frac{1}{L_{2}} & \frac{-r_{2}}{L_{2}} & \frac{D-1}{C_{o}} \\
0 & 0 & \frac{1-D}{C_{o}} & \frac{-1}{R C_{o}}
\end{array}\right]\left[\begin{array}{l}
I_{i n} \\
V_{c} \\
I_{L 2} \\
V_{o}
\end{array}\right]+\left[\begin{array}{c}
\frac{1}{L_{l}} \\
0 \\
0 \\
0
\end{array}\right]\left[\begin{array}{l}
\left.V_{\text {in }}\right] \\
\\
0
\end{array}\right.}  \tag{C.7}\\
& {\left[\begin{array}{c}
\dot{\tilde{I}}_{i n} \\
\dot{V}_{c} \\
\dot{\tilde{I}}_{L 2} \\
\dot{\tilde{V}}_{o}
\end{array}\right]=\left[\begin{array}{cccc}
\frac{-r_{1}}{L_{1}} & \frac{-1}{L_{1}} & 0 & 0 \\
\frac{1}{C} & 0 & \frac{-1}{C} & 0 \\
0 & \frac{1}{L_{2}} & \frac{-r_{2}}{L_{2}} & \frac{D_{e}-1}{C_{o}} \\
0 & 0 & \frac{1-D_{e}}{C_{o}} & \frac{-1}{R C_{o}}
\end{array}\right]\left[\begin{array}{c}
\tilde{I}_{i n} \\
\tilde{V}_{c} \\
\tilde{I}_{L 2} \\
\tilde{V_{o}}
\end{array}\right]+\left[\begin{array}{c}
0 \\
0 \\
\frac{V_{\text {in }}}{\left(1-D_{e}\right) L_{2}} \\
-\frac{V_{i n}}{\left(1-D_{e}\right)^{2} R C_{o}}
\end{array}\right][\delta]}  \tag{C.8}\\
& G(s)=\frac{\tilde{V_{o}}(s)}{\delta(s)}=\frac{a_{3} s^{3}+a_{2} s^{2}+a_{1} s+a_{0}}{b_{4} s^{4}+b_{3} s^{3}+b_{2} s^{2}+b_{1} s+b_{0}} \\
& a_{3}=-C L_{1} L_{2} V_{\text {in }} \\
& a_{2}=C V_{i n}\left[L_{1} R\left(1-D_{e}\right)^{2}-\left(L_{1} r_{2}+L_{2} r_{1}\right]\right. \\
& a_{1}=V_{\text {in }}\left[C R r_{1}\left(1-D_{e}\right)-C r_{1} r_{2}-\left(L_{1}+L_{2}\right)\right] \\
& a_{0}=V_{i n}\left[R\left(1-D_{e}\right)^{2}-\left(r_{1}+r_{2}\right)\right] \\
& b_{4}=C C_{o} L_{1} L_{2} R\left(1-D_{e}\right)^{2}  \tag{C.9}\\
& b_{3}=C\left(1-D_{e}\right)^{2}\left[L_{1} L_{2}+C_{o} R\left(L_{1} r_{2}+L_{2} r_{1}\right)\right] \\
& b_{2}=\left(1-D_{e}\right)^{2}\left[C L_{1} R\left(1-D_{e}\right)^{2}+C_{o} R\left(L_{1}+L_{2}\right)\right. \\
& \left.C\left(L_{1} r_{2}+L_{2} r_{1}\right)+C C_{o} R r_{1} r_{2}\right] \\
& b_{1}=\left(1-D_{e}\right)^{2}\left[C r_{1} R+C_{o} R\left(r_{1}+r_{2}\right)+\left(L_{1}+L_{2}\right)+C r_{1} r_{2}\right] \\
& b_{0}=\left(1-D_{e}\right)^{2}\left[R\left(1-D_{e}\right)^{2}+\left(r_{1}+r_{2}\right)\right]
\end{align*}
$$



Figure C.16. Operation of B2E in dc/dc mode at $V_{i n}=50 \mathrm{~V}$ : (a) PI-controlled system Bode plot (c) $V_{c}$ at $\mathrm{D}=0.5$, (d) $I_{i n}$ at $\mathrm{D}=0.5$, and (e) output voltage $V_{o}$ with square wave reference. ( $C=C_{o}=5 \mu \mathrm{~F}, L_{l}=L_{2}=1 \mathrm{mH}$, and $\mathrm{R}=22 \Omega$ ).


Figure C.17. Operation of B2E in dc/ac mode (single-phase) at $V_{i n}=50 \mathrm{~V}$ and ( $I_{o}{ }_{o}^{\text {ref }} . R$ $=100 \sin \omega t$ : (a) control structure, (b) PR-controlled system Bode plot (c) $I_{1}$ and $I_{2}$, (d) capacitor voltage $V_{c l}$, and (e) output voltage $\left.V_{o}\right) .\left(C=5 \mu \mathrm{~F}, L_{1}=L_{2}=1 \mathrm{mH}\right.$, and R


Figure C.18. Operation of B2E in dc/ac mode (three-phase) at $V_{i n}=50 \mathrm{~V}, V_{m}=100$ : (a) $I_{i n}$, (b) capacitors voltages $V_{c 1}-V_{c 2}-V_{c 3}$ (c) load voltages $\left(V_{o 1}-V_{o 2}-V_{o 3}\right)$.

## C. 4 B2G

The two circuit configurations during ON and OFF states are shown in Figure C.19. The converter models and transfer function are stated in (C.10), (C.11) and (C.12). The single-phase and three-phase inverters emerging from the B2G converter are shown in Figure C. 20 and Figure C. 21 respectively. Operation of the dc converter and dc/ac inverters are shown in Figure C.22, Figure C. 23 and Figure C. 24 respectively.


Figure C.19. Two configurations of B2G converter: (a) $t_{o n}$ and (b) $t_{o f f}$.

$$
\begin{align*}
& {\left[\begin{array}{l}
\dot{I}_{\text {in }} \\
\dot{V_{c}} \\
\dot{I}_{L 2} \\
\dot{V_{o}}
\end{array}\right]=\left[\begin{array}{cccc}
\frac{-r_{l}}{L_{l}} & \frac{D}{L_{1}} & 0 & \frac{D-1}{L_{l}} \\
\frac{-D}{C} & 0 & \frac{l-D}{C} & 0 \\
0 & \frac{D-1}{L_{2}} & \frac{-r_{2}}{L_{2}} & \frac{D}{L_{2}} \\
\frac{l-D}{C_{o}} & 0 & \frac{-D}{C_{o}} & \frac{-1}{R C_{o}}
\end{array}\right]\left[\begin{array}{l}
I_{\text {in }} \\
V_{c} \\
I_{L 2} \\
V_{o}
\end{array}\right]+\left[\begin{array}{l}
\frac{1}{L_{l}} \\
0 \\
0 \\
0
\end{array}\right]\left[\begin{array}{l}
\left.V_{\text {in }}\right] \\
\\
\end{array}\right.}  \tag{C.10}\\
& {\left[\begin{array}{l}
\dot{\tilde{I}}_{i n} \\
\dot{\tilde{V}}_{c} \\
\dot{\tilde{I}}_{L 2} \\
\dot{\tilde{V}}_{o}
\end{array}\right]=\left[\begin{array}{cccc}
\frac{-r_{1}}{L_{1}} & \frac{D_{e}}{L_{l}} & 0 & \frac{D_{e}-1}{L_{l}} \\
\frac{-D_{e}}{C} & 0 & \frac{1-D_{e}}{C} & 0 \\
0 & \frac{D_{e}-1}{L_{2}} & \frac{-r_{2}}{L_{2}} & \frac{D_{e}}{L_{2}} \\
\frac{1-D_{e}}{C_{o}} & 0 & \frac{-D_{e}}{C_{o}} & \frac{-1}{R C_{o}}
\end{array}\right]\left[\begin{array}{c}
\tilde{I}_{i n} \\
\tilde{V}_{c} \\
\tilde{I}_{L 2} \\
\tilde{V_{o}}
\end{array}\right]+\left[\begin{array}{c}
\frac{V_{i n}}{\left(1-2 D_{e}\right) L_{l}} \\
\frac{\left(D_{e}-1\right) V_{i n}}{\left(1-2 D_{e}\right)^{2} R C} \\
\frac{V_{i n}}{\left(1-2 D_{e}\right) L_{2}} \\
\frac{\left(D_{e}-1\right) V_{i n}}{\left(1-2 D_{e}\right)^{2} R C_{o}}
\end{array}\right]} \\
& G(s)=\frac{\tilde{V_{o}}(s)}{\delta(s)}=\frac{a_{3} s^{3}+a_{2} s^{2}+a_{1} s+a_{0}}{b_{4} s^{4}+b_{3} s^{3}+b_{2} s^{2}+b_{1} s+b_{0}} \\
& a_{3}=C L_{1} L_{2} V_{\text {in }}\left(D_{e}-1\right) \\
& a_{2}=C V_{i n}\left(D_{e}-1\right)\left[L_{1} R\left(2 D_{e}-1\right)+\left(L_{1} r_{2}+L_{2} r_{1}\right)\right]+ \\
& C V_{\text {in }}\left(2 D_{e}-1\right) \\
& a_{1}=V_{i n}\left(D_{e}-1\right)\left[L_{1}\left(1-D_{e}\right)-D_{e} L_{2}+C R r_{2}\left(1-2 D_{e}\right)+C r_{1} r_{2}\right]+ \\
& C V_{i n} R r_{1} D_{e}\left(1-2 D_{e}\right) \\
& a_{0}=V_{i n}\left[R\left(1-2 D_{e}\right)^{2}-r_{1}\left(1-D_{e}\right)^{2}+r_{2} D_{e}\left(D_{e}-1\right)\right] \\
& b_{4}=C C_{o} L_{1} L_{2} R\left(1-2 D_{e}\right)^{2} \\
& b_{3}=C\left(1-2 D_{e}\right)^{2}\left[L_{1} L_{2}+C_{o} R\left(L_{1} r_{2}+L_{2} r_{1}\right)\right] \\
& b_{2}=\left(1-2 D_{e}\right)^{2}\left[C L_{2} R\left(1-D_{e}\right)^{2}+C_{o} L_{1} R\left(1-D_{e}\right)^{2}+\right. \\
& \left.C\left(L_{1} r_{2}+L_{2} r_{1}\right)+D_{e} R\left(C_{o} L_{2}+C L_{1}\right)+C C_{o} R r_{1} r_{2}\right] \\
& b_{1}=\left(1-2 D_{e}\right)^{2}\left[\left(L_{1}+C R r_{2}+C_{o} R r_{1}\right)\left(1-D_{e}\right)+D_{e} L_{2}+\right. \\
& D_{e}{ }^{2} R\left(C r_{l}+C_{o} r_{2}\right)+C r_{1} r_{2} \\
& b_{0}=\left(1-2 D_{e}\right)^{2}\left[R\left(1-2 D_{e}\right)^{2}+\left(r_{1}\left(1-D_{e}\right)+r_{2} D_{e}{ }^{2}\right)\right]
\end{align*}
$$



Figure C.20. B2G single-phase inverter.


Figure C.21. B2G three-phase inverter.


Figure C.22. Operation of B2G in dc/dc mode at $V_{i n}=50 \mathrm{~V}$ : (a) PI-controlled system Bode plot (b) $V_{c}$ at $\mathrm{D}=0.5$, (d) $I_{i n}$ at $\mathrm{D}=0.5$, and (e) output voltage $V_{o}$ with square wave reference. (C $C=C_{n}=5 \mu \mathrm{~F}, L_{l}=L_{\text {}}=1 \mathrm{mH}$, and $\mathrm{R}=22 \Omega$ ).


Figure C.23. Operation of B2G in dc/ac mode (single-phase) at $V_{i n}=50 \mathrm{~V}$ and ( $I_{o}^{\text {ref }} . R=$ 100sinet: (a) control structure, (b) PR-controlled system Bode plot (c) $I_{1}$ and $I_{2}$, (d) capacitor voltage $V_{c l}$, and (e) output voltage $\left.V_{o}\right)$. ( $C=5 \mu \mathrm{~F}, L_{l}=L_{2}=1 \mathrm{mH}$, and $\left.\mathrm{R}=22 \Omega\right)$.


Figure C.24. Operation of B2G in dc/ac mode (three-phase) at $V_{\text {in }}=50 \mathrm{~V}, V_{m}=100$ :
(a) $I_{i n}$, (b) capacitors voltages $V_{c 1}-V_{c 2}-V_{c 3}$, and (c) load voltages $\left(V_{o 1}-V_{o 2}-V_{o 3}\right)$.

## C. 5 B1P

The two circuit configuration during ON and OFF periods are shown in Figure C.25. The converter models and transfer function are stated in equation sets (4.13), (C.14) and (C.15). The single-phase and three-phase inverters arising from the B2G converter are shown in Figure C. 26 and Figure C. 27 respectively. The operation of the dc converter and dc/ac inverters are shown in Figure C. 28 , Figure C. 29 and Figure C. 30 respectively.

(a)

(b)

Figure C.25. Two configurations of B1P converter: (a) $t_{o n}$ and (b) $t_{o f f}$.

$$
\begin{align*}
& {\left[\begin{array}{l}
\dot{I}_{L 1} \\
\dot{V_{c}} \\
\dot{I}_{L 2} \\
\dot{V_{o}}
\end{array}\right]=\left[\begin{array}{cccc}
\frac{-r_{1}}{L_{1}} & \frac{D-1}{L_{1}} & 0 & \frac{D-1}{L_{1}} \\
\frac{1-D}{C} & 0 & \frac{-D}{C} & 0 \\
0 & \frac{D}{L_{2}} & \frac{-r_{2}}{L_{2}} & \frac{D-1}{L_{2}} \\
\frac{1-D}{C_{o}} & 0 & \frac{1-D}{C_{o}} & \frac{-1}{R C_{o}}
\end{array}\right]\left[\begin{array}{l}
I_{L 1} \\
V_{c} \\
I_{L 2} \\
V_{o}
\end{array}\right]+\left[\begin{array}{c}
\frac{1}{L_{1}} \\
0 \\
0 \\
0
\end{array}\right]\left[\begin{array}{l}
\left.V_{i n}\right] \\
\end{array}\right.}  \tag{C.13}\\
& {\left[\begin{array}{l}
\dot{\tilde{I}}_{i n} \\
\dot{\dot{V}_{c}} \\
\dot{\tilde{I}}_{L 2} \\
\dot{\dot{V}_{o}}
\end{array}\right]=\left[\begin{array}{cccc}
\frac{-r_{1}}{L_{1}} & \frac{D_{e}-1}{L_{l}} & 0 & \frac{D_{e}-1}{L_{l}} \\
\frac{1-D_{e}}{C} & 0 & \frac{-D_{e}}{C} & 0 \\
0 & \frac{D_{e}}{L_{2}} & \frac{-r_{2}}{L_{2}} & \frac{D_{e}-1}{L_{2}} \\
\frac{1-D_{e}}{C_{o}} & 0 & \frac{1-D_{e}}{C_{o}} & \frac{-1}{R C_{o}}
\end{array}\right]\left[\begin{array}{c}
\tilde{I}_{i n} \\
\tilde{V_{c}} \\
\tilde{I}_{L 2} \\
\tilde{V_{o}}
\end{array}\right]+\left[\begin{array}{c}
\frac{V_{\text {in }}}{\left(1-D_{e}\right) L_{l}} \\
\frac{-V_{\text {in }}}{\left(1-D_{e}\right)^{2} R C} \\
\frac{V_{\text {in }}}{\left(1-D_{e}\right) L_{2}} \\
\frac{V_{\text {in }}}{\left(1-D_{e}\right)^{2} R C_{o}}
\end{array}\right][\delta]} \tag{C.14}
\end{align*}
$$

$$
\begin{align*}
& G(s)=\frac{\tilde{V_{o}}(s)}{\delta(s)}=\frac{a_{3} s^{3}+a_{2} s^{2}+a_{1} s+a_{0}}{b_{4} s^{4}+b_{3} s^{3}+b_{2} s^{2}+b_{1} s+b_{0}} \\
& a_{3}=-C L_{1} L_{2} V_{\text {in }} \\
& a_{2}=C V_{\text {in }}\left[L_{1} R\left(1-D_{e}\right)^{2}-\left(L_{1} r_{2}+L_{2} r_{1}\right]\right. \\
& a_{1}=V_{\text {in }}\left[C R r_{1}\left(1-D_{e}\right)-C r_{1} r_{2}-\left(L_{1}+L_{2}\right)\right] \\
& a_{0}=V_{\text {in }}\left[R\left(1-D_{e}\right)^{2}-\left(r_{1}+r_{2}\right)\right] \\
& b_{4}=C C_{o} L_{1} L_{2} R\left(1-D_{e}\right)^{2}  \tag{C.15}\\
& b_{3}=C\left(1-D_{e}\right)^{2}\left[L_{1} L_{2}+C_{o} R\left(L_{1} r_{2}+L_{2} r_{1}\right)\right] \\
& b_{2}=\left(1-D_{e}\right)^{2}\left[C L_{1} R\left(1-D_{e}\right)^{2}+C_{o} R\left(L_{1}+L_{2}\right)\right. \\
& \left.C\left(L_{1} r_{2}+L_{2} r_{I}\right)+C C_{o} R r_{1} r_{2}\right] \\
& b_{1}=\left(1-D_{e}\right)^{2}\left[C r_{1} R+C_{o} R\left(r_{1}+r_{2}\right)+\left(L_{l}+L_{2}\right)+C r_{1} r_{2}\right] \\
& b_{0}=\left(1-D_{e}\right)^{2}\left[R\left(1-D_{e}\right)^{2}+\left(r_{1}+r_{2}\right)\right]
\end{align*}
$$



Figure C.26. B1P single-phase inverter.


Figure C.27. B1P three-phase inverter.

(a) $G_{p i} * G_{c l}\left(K_{p}=0.9, K_{i}=30\right.$ and $\left.K=6\right)$

$25 \mathrm{~V} / \mathrm{div}-20 \mathrm{~ms} /$ div
(c)


3A/div-20ms/div

(e)

Figure C.28. Operation of B1P in dc/dc mode at $V_{i n}=50 \mathrm{~V}$ : (a) PI-controlled system Bode plot (b) $V_{c}$ at $\mathrm{D}=0.5$, (d) $I_{i n}$ at $\mathrm{D}=0.5$, and (e) output voltage $V_{o}$ with square wave reference. ( $C=C_{o}=5 \mu \mathrm{~F}, L_{1}=L_{2}=1 \mathrm{mH}$, and $\mathrm{R}=22 \Omega$ ).


Figure C.29. Operation of B1P in dc/ac mode (single-phase) at $V_{\text {in }}=50 \mathrm{~V}$ and ( $I_{o}{ }^{\text {ref }} . R$ $=100$ sinct: (a) control structure, (b) PR-controlled system Bode plot (c) $I_{1}$ and $I_{2}$, (d) capacitor voltage $V_{c l}$, and (e) oOutput voltage $\left.V_{o}\right)$. $\left(C=5 \mu \mathrm{~F}, L_{l}=L_{2}=1 \mathrm{mH}\right.$, and


Figure C.30. Operation of B1P in dc/ac mode (three-phase) at $V_{i n}=50 \mathrm{~V}, V_{m}=100$ :
(a) $I_{i n}$, (b) Capacitors voltages $V_{c 1}-V_{c 2}-V_{c 3}$, and (c) Load voltages $\left(V_{o 1}-V_{o 2}-V_{o 3}\right)$.

## C. 6 bB1D

The dc/dc bB1D converter is shown in Figure 2.13e in a single-switch single-diode configuration. The bidirectional converter is created by inserting anti-parallel diode and switch pairs. As with the Ćuk converter, bB1D has continuous input and output currents. The two modes of the bB1D converter are shown in Figure C. 31 and the converter's models are illustrated in (C.16) and (C.17). The small-signal transfer function is shown in equation (C.18).


Figure C.31.Two modes of bB1D Converter: (a) $t_{o n}$ and (b) $t_{o f f}$.

$$
\begin{align*}
& {\left[\begin{array}{l}
\dot{I}_{i n} \\
\dot{V}_{c} \\
\dot{I}_{L 2}
\end{array}\right]=\left[\begin{array}{ccc}
\frac{-\left(r_{1}+R\right)}{L_{l}} & -\frac{1}{L_{1}} & \frac{R}{L_{l}} \\
\frac{1}{C} & 0 & \frac{-D}{C} \\
\frac{R}{L_{2}} & \frac{D}{L_{2}} & \frac{-\left(R+r_{2}\right)}{L_{2}}
\end{array}\right]\left[\begin{array}{l}
I_{i n} \\
V_{c} \\
I_{L 2}
\end{array}\right]+\left[\begin{array}{l}
\frac{1}{L_{l}} \\
0 \\
0
\end{array}\right]\left[V_{\text {in }}\right]}  \tag{C.16}\\
& {\left[\begin{array}{c}
\dot{\tilde{I}}_{i n} \\
\dot{\tilde{V}}_{c} \\
\dot{\tilde{I}}_{L 2}
\end{array}\right]=\left[\begin{array}{ccc}
\frac{-\left(r_{1}+R\right)}{L_{l}} & -\frac{1}{L_{l}} & \frac{R}{L_{l}} \\
\frac{1}{C} & 0 & \frac{-D_{e}}{C} \\
\frac{R}{L_{2}} & \frac{D_{e}}{L_{2}} & \frac{-\left(R+r_{2}\right)}{L_{2}}
\end{array}\right]\left[\begin{array}{c}
\tilde{I}_{i n} \\
\tilde{V_{c}} \\
\tilde{I}_{L 2}
\end{array}\right]+\left[\begin{array}{c}
0 \\
-\frac{D_{e} V_{i n}}{R C\left(1-D_{e}\right)^{2}} \\
\frac{V_{\text {in }}}{L_{2}\left(1-D_{e}\right)}
\end{array}\right][\delta]}  \tag{C.17}\\
& G(s)=\frac{\tilde{V_{o}}(s)}{\delta(s)}=\frac{a_{2} s^{2}+a_{1} s+a_{0}}{b_{3} s^{3}+b_{2} s^{2}+b_{1} s+b_{0}} \\
& a_{2}=C R\left(1-D_{e}\right) L_{l} V_{i n} \\
& a_{l}=V_{i n}\left(-D_{e}\left(L_{2}+L_{l} D_{e}\right)+\operatorname{CRr}_{l}\left(1-D_{e}\right)\right) \\
& a_{0}=-R V_{i n}\left(1-D_{e}\right)^{2}-D_{e} V_{\text {in }}\left(r_{2}+r_{1} D_{e}\right)  \tag{C.18}\\
& b_{3}=C L_{1} L_{2}\left(1-D_{e}\right)^{2} \\
& b_{2}=C\left(1-D_{e}\right)^{2}\left[L_{l}\left(R+r_{2}\right)+L_{2}\left(R+r_{1}\right)\right] \\
& b_{1}=\left(1-D_{e}\right)^{2}\left[\left(L_{2}+L_{1} D_{e}{ }^{2}\right)+C R\left(r_{1}+r_{2}\right)+C r_{1} r_{2}\right] \\
& b_{0}=\left(1-D_{e}\right)^{2}\left[R\left(1-D_{e}\right)^{2}+\left(r_{2}+r_{1} D_{e}{ }^{2}\right)\right]
\end{align*}
$$

## a) $d c / d c$ mode

The operation of the $b B 1 D$ converter in a dc/dc mode is shown in Figure C. 32 with ( $V_{\text {in }}=200 \mathrm{~V}, L_{l}=L_{2}=1 \mathrm{mH}, C=20 \mu \mathrm{~F}, f_{s}=30 \mathrm{kHz}, \mathrm{D}=0.5$, and $\mathrm{R}=22 \Omega$ ). The single-loop structure fails to provide satisfactory gain and phase margins. The two-loop control structure for the $b B 1 D$ converter in a dc/dc mode is shown in Figure C.32a and the corresponding Bode plot is shown in Figure C.32b, with satisfactory gain and phase margins. The input current $I_{i n}$ and central capacitor voltage $V_{c}$ at $\mathrm{D}=$
0.5 are shown in Figures C.32c and C.32d. In Figure C.32e, the output voltage $V_{o}$ follows a reference square voltage,with both buck and boost mode of operation.

## b) dc/ac single-phase inverter

Unlike the Ćuk converter, the transfer capacitor $C$ is surrounded by switches and diodes in bB1D converter. For this reason, only one configuration exists for a singlephase bB1D inverter, which is shown in Figure C.33. Figure C. 34 shows the operation of single-phase bB1D inverter.

## c) dc/ac three-phase inverter

The three-phase inverter arising from the bB1D converter is shown in Figure C.35. The duty ratios $\delta_{1}, \delta_{2}$, and $\delta_{3}$ for the three legs $\left(S_{1}, S_{2}\right)$, $\left(S_{3}, S_{4}\right)$ and $\left(S_{5}, S_{6}\right)$ are calculated from equation set (C.19).

The experimental operation of the bB1D three-phase inverter is shown in Figure C. 36 when controlled by the PR controllers.

(a)


2A/div-5ms/div
(c)

$25 \mathrm{~V} / \mathrm{div}-5 \mathrm{~ms} / \mathrm{div}$

$$
-V_{o},-I_{o}{ }^{r e f} \cdot R
$$

(b)

(b) $G_{p i} * G_{c l}$

(a)
(c)

Figure C.32. Operation of bB1D converter in dc/dc mode: (a) control structure, (b) Bode plot of $G^{*} G_{p i}$, with $K_{p}=2, K_{i}=1$ and $K=2$, (c) $I_{i n}$ at $\mathrm{D}=0.5$, (d) $V_{c}$ at $\mathrm{D}=0.5$, and (e) output voltage $V_{o}$ with square wave reference voltage.


Figure C.33. Single-phase dc/ac inverter based on bB1D converter.


Figure C.34. Operation of bB1D single-phase inverter at $V_{i n}=200 \mathrm{~V}$ and $I_{o}{ }^{\text {ref }}=\frac{160}{R}$ $\sin \omega t$ : (a) two-loops PR controller, (b) Bode plot of the overall controller shown in (a) with $K_{p}=2, K_{r}=5$ and $K=1$, (c) $I_{1}$ and $I_{2}$, (d) $V_{c 1}$ and $V_{c 2}$, and (e) output voltage $V_{o}$.


Figure C.35. Three-phase dc/ac inverter based on bB1D converter.

$$
\begin{gather*}
V_{o 1}=1 / 2 V_{m} \sin \omega t+1 / 2 V_{m} \\
V_{o 2}=1 / 2 V_{m} \sin (\omega t-2 / 3 \pi)+1 / 2 V_{m} \\
V_{o 3}=1 / 2 V_{m} \sin (\omega t+2 / 3 \pi)+1 / 2 V_{m} \\
\delta_{1}=\frac{V_{o 1}}{V_{o 1}+V_{i n}}  \tag{C.19}\\
\delta_{2}=\frac{V_{o 2}}{V_{o 2}+V_{i n}} \\
\delta_{3}=\frac{V_{o 3}}{V_{o 3}+V_{\text {in }}}
\end{gather*}
$$


(a)

(b)

$50 \mathrm{~V} / \mathrm{div}-5 \mathrm{~ms} / \mathrm{div}$
(c)

Figure C. 36 Performance of closed loop PR controlled seven-switch three-phase $b B 1 D$ inverter at $V_{\text {in }}$ $=100 \mathrm{~V}$ and $V_{o}^{r e f}=100 \sin \omega t$ : (a) $I_{i n}$, (b) $V_{c a}-V_{c b}-V_{c c}$ and (c) three-phase output voltage $V_{o}$.

## C. 7 bB2D

The dc/dc bB2D converter is shown in Figure 2.13f in a single-switch single-diode configuration. As with the previous converters, the bB2D has continuous input and output currents. The two modes of the bB2D converter are shown in Figure C. 37 and the converter's models are illustrated in equations sets (C.20) and (C.21). The smallsignal transfer function is shown in equation (C.22).

(a)

(b)

Figure C.37. Two modes of bB2D converter: (a) $t_{o n}$ and (b) $t_{o f f}$.

$$
\begin{align*}
& {\left[\begin{array}{l}
\dot{I}_{L I} \\
\dot{V}_{c} \\
\dot{I}_{o}
\end{array}\right]=\left[\begin{array}{ccc}
\frac{-r_{l}}{L_{l}} & -\frac{1-D}{L_{l}} & 0 \\
\frac{l-D}{C} & 0 & \frac{-1}{C} \\
0 & \frac{1}{L_{2}} & \frac{-\left(R+r_{2}\right)}{L_{2}}
\end{array}\right]\left[\begin{array}{l}
I_{L I} \\
V_{c} \\
I_{o}
\end{array}\right]+\left[\begin{array}{c}
\frac{1}{L_{l}} \\
0 \\
\frac{-1}{L_{2}}
\end{array}\right]\left[V_{\left.V_{i n}\right]}\right.}  \tag{C.20}\\
& {\left[\begin{array}{c}
\dot{I}_{L I} \\
\dot{V_{c}} \\
\dot{I}_{o}
\end{array}\right]=\left[\begin{array}{ccc}
\frac{-r_{l}}{L_{l}} & -\frac{1-D_{e}}{L_{l}} & 0 \\
\frac{1-D_{e}}{C} & 0 & \frac{-1}{C} \\
0 & \frac{1}{L_{2}} & \frac{-\left(R+r_{2}\right)}{L_{2}}
\end{array}\right]\left[\begin{array}{c}
\tilde{I}_{L l} \\
\tilde{V_{c}} \\
\tilde{I}_{o}
\end{array}\right]+\left[\begin{array}{c}
\frac{V_{\text {in }}}{L_{l}\left(1-D_{e}\right)} \\
\frac{D_{e} V_{i n}}{R C\left(1-D_{e}\right)^{2}} \\
0
\end{array}\right][\delta]}  \tag{C.21}\\
& G(s)=\frac{\tilde{V_{o}}(s)}{\delta(s)}=\frac{a_{1} s+a_{0}}{b_{3} s^{3}+b_{2} s^{2}+b_{1} s+b_{0}} \\
& a_{l}=-D_{e} V_{i n} L_{1} \\
& a_{0}=V_{\text {in }}\left[R\left(1-D_{e}\right)^{2}-r_{1} D_{e}\right] \\
& b_{3}=C L_{1} L_{2}\left(1-D_{e}\right)^{2}  \tag{C.22}\\
& b_{2}=C\left(1-D_{e}\right)^{2}\left[L_{1}\left(R+r_{2}\right)+L_{2} r_{1}\right] \\
& b_{1}=\left(1-D_{e}\right)^{2}\left[L_{1}+L_{2}\left(1-D_{e}\right)^{2}+C r_{1} r_{2}+C R r_{1}\right] \\
& b_{0}=\left(1-D_{e}\right)^{2}\left[\left(R+r_{2}\right)\left(1-D_{e}\right)^{2}+r_{1}\right]
\end{align*}
$$

## a) $d c / d c$ mode

The operation of the $b B 2 D$ converter in a dc/dc mode is shown in Figure C. 38 with ( $V_{\text {in }}=200 \mathrm{~V}, L_{1}=L_{2}=1 \mathrm{mH}, C=20 \mu \mathrm{~F}, f_{s}=30 \mathrm{kHz}, \mathrm{D}=0.5$, and $\mathrm{R}=22 \Omega$ ). The two-loop control structure for the $b B 2 D$ converter in dc/dc mode is shown in Figure C.38a and the corresponding Bode plot is shown in Figure C.38b with satisfactory gain and phase margins. The input current $I_{i n}$ and central capacitor voltage $V_{c}$ at $\mathrm{D}=0.5$ are shown in Figures C.38c and C.38d. In Figure C.38e, the output voltage $V_{o}$ follows a reference square voltage in both buck and boost modes.


Figure C.38. Operation of bB2D converter in dc/dc mode: (a) control structure, (b) Bode plot of, (c) $I_{i n}$ at $\mathrm{D}=0.5$, (d) $V_{c}$ at $\mathrm{D}=0.5$, (e) output voltage $V_{o}$ with square wave reference voltage.

## b) dc/ac single-phase inverter

The single-phase bB2D inverter is shown in Figure C.39. The inverter's duty ratios are as calculated from equation (4.21).

Figure C. 40 shows operation of the single-phase bB2D inverter when PR controlled.


Figure C.39. Single-phase dc/ac inverter Based on bB2D converter.


Figure C.40. Operation of bB2D single-phase inverter at $V_{i n}=200 \mathrm{~V}$ and $I_{o}{ }^{\text {ref }}=\frac{160}{R}$ $\sin \omega t$ : (a) two-loops PR controller, (b) Bode plot of the overall controller shown in (a) with $K_{p}=5, K_{r}=10$ and $K=5$, (c) $I_{1}$ and $I_{2}$, (d) $V_{c 1}$ and $V_{c 2}$, and (e) output voltage $V_{o}$.

## c) dc/ac three-phase inverter

The three-phase inverter emerging from the bB2D converter is shown in Figure C.41. The duty ratios $\delta_{1}, \delta_{2}$, and $\delta_{3}$ for the three legs $\left(S_{1}, S_{2}\right),\left(S_{3}, S_{4}\right)$ and $\left(S_{5}, S_{6}\right)$ are calculated from equation (4.24). Experimental operation of the bB2D three-phase inverter is shown in Figure C. 42 when controlled by PR controllers.


Figure C.41. Three-phase dc/ac inverter based on bB2D converter.


Figure C.42. Performance of closed loop PR controlled three-phase $b B 2 D$ inverter at $V_{i n}=100 \mathrm{~V}$ and $V_{o}^{\text {ref }}=100 \sin (\omega t)$ : (a) $I_{i n}$, (b) $V_{c a}-V_{c b}-V_{c c}$, and (c) three-phase output voltage $V_{o}$.

## C. 8 bB1F

The dc/dc bB1F converter is shown in Figure 2.29e in single-switch single-diode configuration. The bB1F has continuous input and discontinuous output currents and hence, an output capacitor $C_{o}$ is required. The two modes of the bB1F converter are shown in Figure C. 43 and the converter's models are illustrated in equations sets (C.23) and (C.24). The small-signal transfer function is as in equation (C.25).

## a) $d c / d c$ mode

Operation of the $b B 1 F$ converter in a dc/dc mode is shown in Figure C. 44 with ( $V_{i n}=$ $200 \mathrm{~V}, L_{1}=L_{2}=1 \mathrm{mH}, C=20 \mu \mathrm{~F}, C_{o}=20 \mu \mathrm{~F}, f_{s}=30 \mathrm{kHz}, \mathrm{D}=0.5$, and $\mathrm{R}=22 \Omega$ ). For this converter, it is difficult to attain adequate stability margins with large bandwidth. This is because of the inserted output capacitor $C_{o}$, which is necessary to filter the output current, leads the system to be fourth-order and more difficult to control design.

$$
\begin{align*}
& {\left[\begin{array}{c}
\dot{\tilde{I}_{i n}} \\
\dot{\tilde{V}_{c}} \\
\dot{\tilde{I}}_{L 2} \\
\dot{\tilde{V}_{o}}
\end{array}\right]=\left[\begin{array}{cccc}
\frac{-r_{1}}{L_{l}} & -\frac{1}{L_{1}} & 0 & 0 \\
\frac{1}{C} & 0 & \frac{-D_{e}}{C} & 0 \\
0 & \frac{D_{e}}{L_{2}} & \frac{-r_{2}}{L_{2}} & \frac{-\left(1-D_{e}\right)}{L_{2}} \\
0 & 0 & \frac{1-D_{e}}{C_{o}} & \frac{-1}{R C_{o}}
\end{array}\right]\left[\begin{array}{c}
\tilde{I}_{i n} \\
\tilde{V_{c}} \\
\tilde{I}_{L 2} \\
\tilde{V_{o}}
\end{array}\right]+\left[\begin{array}{c}
0 \\
\frac{-D_{e} V_{i n}}{\left(1-D_{e}\right)^{2} R C} \\
\frac{V_{i n}}{\left(1-D_{e}\right) L_{2}} \\
\frac{-D_{e} V_{i n}}{\left(1-D_{e}\right)^{2} R C_{o}}
\end{array}\right][\delta]} \tag{C.24}
\end{align*}
$$

$$
\begin{align*}
& G(s)=\frac{\tilde{V_{o}}(s)}{\delta(s)}=\frac{a_{3} s^{3}+a_{2} s^{2}+a_{1} s+a_{0}}{b_{3} s^{3}+b_{2} s^{2}+b_{1} s+b_{0}} \\
& a_{3}=C \quad D_{e} L_{1}{ }^{2} L_{2} V_{\text {in }} \\
& a_{2}=-C D_{e} V_{i n}\left[\left(L_{1} r_{2}+L_{2} r_{1}\right)+L_{1} R\left(2-D_{e}\right)\right] \\
& a_{l}=-V_{i n}\left[D_{e} L_{l}\left(D_{e} L_{l}+C r_{1} r_{2}+L_{2}\right)-C L_{2} R r_{1}\left(1-D_{e}\right)^{2}\right] \\
& a_{0}=V_{\text {in }}\left[R\left(1-D_{e}\right)^{2}-D_{e}\left(D_{e} r_{l}+r_{2}\right)\right] \\
& b_{4}=C C_{o} L_{1}{ }^{2} L_{2} R\left(1-D_{e}\right)^{2}  \tag{C.25}\\
& b_{3}=C L_{1}\left(1-D_{e}\right)^{2}\left[L_{1} L_{2}+C_{o} R\left(L_{1} r_{2}+L_{2} r_{1}\right)\right] \\
& b_{2}=L_{l}\left(1-D_{e}\right)^{2}\left[C L_{1} R\left(1-D_{e}\right)^{2}+C\left(L_{1} r_{2}+L_{2} r_{1}\right)+\right. \\
& \left.C_{o}\left(L_{2} R+D_{e}{ }^{2}+C R r_{1} r_{2}\right)\right] \\
& b_{1}=L_{l}\left(1-D_{e}\right)^{2}\left[L_{2}+D_{e}{ }^{2} L_{1}+\operatorname{CRr}_{1}\left(1-D_{e}\right)^{2}+\right. \\
& \left.C_{o} R\left(r_{1} D_{e}{ }^{2}+r_{2}\right)\right] \\
& b_{0}=\left(1-D_{e}\right)^{2}\left[R\left(1-D_{e}\right)^{2}+r_{2}+r_{1} D_{e}{ }^{2}\right] \\
& \text { (a) } \\
& \text { (b) }
\end{align*}
$$

Figure C.43. Two modes of bB1F converter: (a) $t_{o n}$ and (b) $t_{o f f}$.

## b) dc/ac single-phase inverter

The bB1F converter has two dc/ac single-phase inverter configurations, as shown in Figure C.45. For the first topology in Figure C.45a, four switches, four capacitors, and four inductors are required. The second topology, in Figure C.45b, requires five switches, two capacitors and two inductors. The duty ratio calculations of the first topology are the same as in equation set (4.21). Two sinusoidal +dc output voltages $V_{o 1}$ and $V_{o 2}$ are produced differentially across the load to yield sinusoidal load voltage $V_{o}$. For the second topology, the four operational modes are shown in Figure C. 46 where the current $I_{L 2}$ is directed to the load using four switches, $S_{1}$ to $S_{4}$. It is a cascaded inverter of two converters. The first is a current boost converter which
boosts $I_{i n}$ to $I_{L 2}$. The second is a current buck converter which chops the current $I_{L 2}$ to $I_{o}$. The overall system forms a current buck-boost inverter (or voltage boost-buck inverter) with the same duty ratio calculation as in equation (4.25). The operation of the two inverters are shown in Figures C. 47 and C.48.

(a)


2A/div-5ms/div
(c)

$25 \mathrm{~V} / \mathrm{div}-5 \mathrm{~ms} /$ div

$$
-V_{o},-I_{o}{ }^{r e f} \cdot R
$$


(b) $G_{p i} * G_{c l}\left(K_{p}=0.5, K_{i}=1.5\right.$ and $K=2$ )

$25 \mathrm{~V} / \mathrm{div}-5 \mathrm{~ms} / \mathrm{div}$
(g)
(h)
(i)

Figure C.44. Operation of bB 1 F converter in dc/dc mode: (a) control structure, (b) Bode plot of $G^{*} G_{p i}$, (c) $I_{i n}$ (d) $V_{c}$ (e) output voltage $V_{o}$ with square wave reference


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## c) dc/ac three-phase inverter

As with the single-phase inverters, the $b B 1 F$ converter configuration yields two three-phase dc/ac inverters, as shown in Figure C.49. For the first topology in Figure C.49a, six switches, six capacitors and six inductors are required. The second topology in Figure C.49b needs seven switches, four capacitors and two inductors. The device voltage stresses in the both topologies are the same while the current stresses are higher in the first topology. In the six-switch topology, the inverter's duty ratios are calculated from the calculations in equation set (4.24). For the seven-
switch topology, the overall duty ratio $\delta_{o v}$ is calculated from equation (4.25). The three legs of the current-buck $\operatorname{CSI}\left(S_{1}, S_{2}\right),\left(S_{3}, S_{4}\right)$, and ( $S_{5}, S_{6}$ ) are operating with the three modulating signals $M_{1}, M_{2}$, and $M_{3}$ respectively, calculated from equation (4.26). The open-loop PWM signals of this topology are shown in Figure C.50. During the CSI active states, switch S is OFF allowing the current $I_{L 2}$ to be directed to the three-phase load. During the CSI zero state, the switch S is ON allowing the energy stored in the input inductor and capacitor to flow in the output inductor and $I_{L 2}$ increases. The operation of the six-switch topology is shown in Figure C. 51 while that of the seven-switch topology is shown in Figure C.52.


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## Appendix E

Summary of Relevant Published Research by the Author

[1] A. Darwish, D. Holliday, S. Ahmed, A.M. Massoud, B.W. Williams, "A Single- Stage Three-Phase Inverter Based on Ćuk Converters for PV Applications," IEEE Journal of Emerging and Selected Topics in Power Electronics, , vol.2, no.4, pp.797,807, Dec. 2014


#### Abstract

This paper presents a new three-phase inverter based on the Cuk converter. The main feature of the proposed topology is that the energy storage elements, such as inductors and capacitors, can be reduced in order to improve the reliability, and reduce size and total cost. The buck-boost inherent characteristic of the Cuk converter, depending on the time-varying duty ratio, provides flexibility for standalone and grid connected applications when the required output ac voltage is lower or greater than the dc side voltage. This property is not found in the conventional current source inverter when the dc input current is always greater than the ac output or in the conventional voltage source inverter as the output ac voltage is always lower than the dc input. The proposed system allows much smaller, more reliable nonelectrolytic capacitors to be used for energy source filtering. The new three-phase inverter is convenient for photovoltaic applications where continuous input currents are required for maximum power point tracking operation. Average large and small signal models are used to study the Cuk converter's nonlinear operation. The basic structure, control design, and MATLAB/SIMULINK results are presented. Practical results substantiate the design flexibility of the Cuk-based topology controlled by a TMSF280335 DSP.


[2] A. Darwish, D. Holliday, S. Ahmed, A.M. Massoud, B.W. Williams, "Performance Evaluation and Control Design of Single-phase Differential-mode Buck-boost Inverters with Continuous Input Current," IEEE Journal of Emerging and Selected Topics in Power Electronics, , Submitted


#### Abstract

The paper presents the analysis and implementation of differential-mode (unipolar output) single-phase dc-ac bidirectional inverters with continuous input and/or output energy flows. Differential-mode topologies offer merits such as reduced size of passive elements, higher power density, and reduced total cost. Differential-mode single-phase inverters are promising for renewable energy generation. The converter's continuous input current is appropriate for maximum power point tracking operation for photovoltaic and fuel cells applications. Differential-mode inverters can operate in buck and boost modes, both of which are necessary for better operation and higher efficiency of modern renewable energy applications. But the performance and control of such converters have not been discussed in detail. As a drawback, the total dc side input current of a single-phase inverter consists of a desirable dc component and an undesirable ac component. The ac current component frequency is double the output voltage frequency thus affects maximum power point tracking operation resulting in reduced total efficiency. In this paper, five possible differential-mode inverters with continuous input currents are proposed and compared in terms of total losses, maximum ripple currents, Total Harmonic Distortion, devices and passive element ratings. In addition, two possible methods of eliminating the input 2nd harmonic current component are discussed. Furthermore, the ability for isolating the input and output sides of the inverters with a small size high frequency transformers is discussed. A 2.5 kW bidirectional inverter is used to validate the design flexibility of the inverters topologies, when DSP controlled.


[3] A. Darwish, D. Holliday, S. Ahmed, A.M. Massoud, B.W. Williams, "Topologies and Control Design of Three-phase Differential-mode Buck-boost Inverters with Continuous Input Current," IEEE Journal of Power Electronics, Submitted


#### Abstract

In order to interface the renewable source to the ac-grid, an additional boost stage or line-frequency transformer is required to match the inverter output voltage to that of the grid; thus, allow power injection into the grid. Line frequency transformers are expensive and heavy. Reducing the cost, size and increasing reliability are of paramount importance from the renewable energy market prospective. Up to half the


overall system cost, if the panels cost is excluded, is related to the inverter cost. In addition, the power inverters are the causes of $2 / 3$ the failures in renewable energy systems. The inverter's flexibility means the ability to provide output voltage which is higher or lower than the input voltage. This flexibility is preferable for maximum power point tracking (MPPT) controllers which are responsible for extracting the highest available power from the renewable energy source. Five buck-boost inverters are suitable for providing flexible output voltage without the need of large electrolytic capacitors. In this paper, the grid-connected operation of these inverters will be discussed as well as their control structures and major challenges. The problems of low order harmonics in the input dc link, resulting from the inverters non-linear behaviuor and negative-sequence voltage and current in three-phase topologies during unbalanced operation is discussed, including their ac fault-ride through. The implementation of high-frequency transformer-isolated versions of these buck-boost inverters, to reduce the EMI effect and common mode leakage currents, are presented.
[4] A. Darwish, A. Elserougi, A.S Abdel-Khalik, S. Ahmed, A. Massoud, D. Holliday, B.W. Williams "A single-stage three-phase DC/AC inverter based on Cuk converter for PV application," GCC Conference and Exhibition (GCC), 2013 7th IEEE , vol., no., pp.384,389, 17-20 Nov. 2013


#### Abstract

This paper presents a new three-phase dc-ac inverter based on the basic Cuk converter. The main feature of the proposed topology is the fact that the energy storage elements as inductors and capacitors values can be reduced in order to improve the reliability, reduce the size, and the total cost. Moreover, the buckingboosting inherent nature of the Cuk converter, depending on the time-varying duty ratios, provides more flexibility for stand-alone and grid connected applications when the required output AC voltage is lower or greater than the DC side voltage. This property is not found in the conventional current source inverter (CSI) when the DC input current is always greater than the ac output one or in the conventional voltage source inverter (VSI) as the output ac voltage is always lower than the dc input one. Averaged large and small signal models are used to study the Cuk


nonlinear operation. Basic structure, control design, and MATLAB/SIMULINK results are presented in this paper. The new three-phase DC-AC inverter is very convenient for PV applications where continuous average input currents are required for appropriate Maximum power Point Tracking (MPPT) operations.
[5] A. Darwish, D. Holliday, and B.W. Williams "Operation and Control Design of New Three-phase and Single-phase DC/AC inverters with Reduced Number of Switches," International Conference on Renewable Energy Research and Applications (ICRERA), 2015


#### Abstract

Inverters with reduced number of switches have been proposed the capability of cost reduction, total inverters sizes and switching losses of dc/ac inverter topologies. This paper proposes new designs for inverters with reduced number of switches. For three-phase systems, the proposed inverters use four switches instead of six in the traditional three-phase Voltage Source Inverter (VSI). Compared to traditional FSTP inverter, the proposed FSTP SEPIC inverter improves the voltage utilization factor of the input dc supply. Classical controllers as well as sliding mode controller are used to discuss the dynamic response and robustness of the inverters. The paper as well presents new single-phase inverters with two switches instead of four in the traditional VSI. The capability of supressing the $2^{\text {nd }}$ order current harmonic from the input dc side is discussed. Equations explaining the control design, switches ratings, and the operation of the proposed inverters is presented in this paper. The implementation of high-frequency transformer-isolated versions of these inverters, to reduce the EMI effect and common mode leakage currents, are presented. The basic structure, control design, and MATLAB/SIMULINK results are presented. Practical results substantiate the design flexibility of the proposed topologies when controlled by a TMSF280335 DSP.


[6] A. Darwish, A.K. Abdelsalam, A.M. Massoud, S. Ahmed, "Single phase grid connected curent source inverter: Mitigation of oscillating power effect on the grid current," Renewable Power Generation (RPG 2011), IET Conference on , vol., no., pp.1,7, 6-8 Sept. 2011


#### Abstract

Although voltage source inverters (VSIs) are the most common DC-AC grid-tied converters, current source inverters (CSIs) are considered to be promising candidate, thanks to their low THD voltages/currents and inherent short-circuit proof. The natural oscillating power at the DC-link creates the main CSI's single phase application challenge. Hardware based solutions to this problem exhibits additional cost, components and size. Traditional software based solutions detect the oscillating power effect from a second harmonic component in the DC-link current; hence modify the carrier signal to mitigate the oscillation effect on the grid current. Those solutions are characterised mainly by excessive computational burden in addition to poor tracking. In this paper, a Proportional Resonant (PR) controller, tuned at the third harmonic, is utilized to minimize the oscillating power effect from the grid side, and hence acts as a harmonic cancellator (HC). The proposed technique features: (i) simple implementation, (ii) easy tuning, and (iii) superior steady state elimination. In addition to simulation, experimental setup is implemented to validate the proposed technique effectiveness.


[^0]:    Notes: ${ }^{1)}$ Measuring range limited to $\pm 60 \mathrm{~A}_{\text {m }}$

