# Force and temperature sensors based on organic thin-film transistor and ferroelectric co-polymer

By

**STUART HANNAH**

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# Certificate

This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.



Stuart Hannah

Date: June 2017

**This thesis is dedicated to my supervisor, parents, brother and fiancée who have supported me throughout**

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# Author’s declaration

I declare that all the work presented in this thesis has been carried out by me, unless otherwise acknowledged.

STUART HANNAH

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# Abstract

This thesis presents the development of tactile force and temperature sensors formed by coupling an organic thin-film transistor with a ferroelectric polymer-based parallel-plate capacitor. Ferroelectric material polyvinylidene fluoride trifluoroethylene (P(VDF-TrFE)) sandwiched between two metal electrodes in a parallel plate capacitor structure was coupled to the gate electrode of a low-voltage organic thin-film transistor (OTFT) for signal amplification and voltage readout. To ensure low-voltage operation of the sensing circuit, low-voltage transistor operation was necessary. This was enabled through use of an ultra-thin bi-layer gate dielectric comprised of aluminium oxide ($AlO_x$), formed by the UV/ozone oxidation of aluminium, and a self-assembled monolayer (SAM) of phosphonic acid produced by vacuum deposition. The OTFT was optimised with respect to its dielectric and semiconductor; whereby the length of the SAM's alkyl chain and semiconductor deposition conditions on OTFT electrical and structural properties were studied. An air-stable organic semiconductor dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) was implemented to create OTFTs with improved mobility and electrical stability. Furthermore, two commercially available polyethylene naphthalate (PEN) plastic foils were compared for use as flexible substrates for OTFTs. Response of the P(VDF-TrFE)/OTFT sensor to force and temperature was investigated and results show that the sensor has a linear response to applied constant temperature whereas it responds logarithmically to static compressive force, regardless of whether P(VDF-TrFE) is in the ferroelectric or paraelectric state.

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# List of symbols and abbreviations

| | |
|---|---|
| $\mu$ | Mobility (field-effect/hole) |
| $A$ | Area of capacitor |
| AC | Alternating Current |
| $A_{ch}$ | Cross-sectional area of the channel |
| AFM | Atomic Force Microscopy |
| $AlO_x$ | Aluminium Oxide |
| AMOLED | Active-matrix organic light-emitting diode |
| BCTG | Bottom-Contact Top-Gate |
| BGTC | Bottom-Gate Top-Contact |
| $C$ | Capacitance |
| $C_8PA$ | Octylphosphonic acid |
| $C_{10}PA$ | Decylphosphonic acid |
| $C_{12}PA$ | Dodecylphosphonic acid |
| $C_{14}PA$ | Tetradecylphosphonic acid |
| $C_{16}PA$ | Hexadecylphosphonic acid |
| $C_{18}PA$ | Octadecylphosphonic acid |
| CAG | Contact angle goniometry |
| CMOS | Complementary metal-oxide semiconductor |
| $C_nPA$ | Phosphonic acid |
| $d$ | Dielectric thickness |
| $d_{33}$ | Piezoelectric coefficient |
| DC | Direct current |
| DI | Deionised (water) |
| DIM | Diiodomethane |
| DNTT | dinaphtho[2,3-b:2’,3’-f]thieno[3,2-b]thiophene |
| $E$ | Electric field |
| $EA$ | Electron affinity |
| $E_F$ | Fermi energy |
| EG | Ethylene glycol |
| $\varepsilon_0$ | Electrical permittivity in vacuum |
| $\varepsilon_r$ | Relative permittivity |
| $F$ | Force |
| $f$ | Frequency |
| FET | Field-effect transistor |
| FTIR | Fourier-transform infrared spectroscopy |

| | |
|---|---|
| FW | Filtered water |
| FWHM | Full-width half-maximum |
| HOMO | Highest occupied molecular orbital |
| $I_D$ | Drain current |
| $I_G$ | Gate current |
| $I_{OFF}$ | Transistor OFF-current |
| $I_{ON}$ | Transistor ON-current |
| $I_{ON}/I_{OFF}$ | ON/OFF current ratio |
| IP | Ionisation potential |
| $J$ | Current density |
| $k$ | Boltzmann's constant |
| $L$ | Channel length |
| LUMO | Lowest unoccupied molecular orbital |
| MIM | Metal-insulator-metal structure |
| MIS | Metal-insulator-semiconductor structure |
| OCMFET | Organic charge modulated field-effect transistor |
| OLED | Organic light-emitting diode |
| OSC | Organic solar cell |
| OTFT | Organic thin-film transistor |
| $P$ | Polarisation |
| P(VDF-TrFE) | Polyvinylidene fluoride trifluoroethylene |
| PEN | Polyethylene naphthalate |
| PET | Polyethylene terephthalate |
| PID | Proportional-integral-derivative (controller) |
| POSFET | Piezoelectric oxide semiconductor field-effect transistor |
| ppm | Parts per million |
| PTrFE | Poly(trifluoroethylene) |
| PVDF | Polyvinylidene fluoride |
| PZT | Lead zirconate titanate |
| $Q$ | Charge density |
| $q$ | Charge of electron |
| $Q_X$ | Charge at a distance x from the source |
| R2R | Roll-to-roll processing |
| RFID | Radio-frequency identification tag |
| RMS | Root mean square |
| RO | Reverse osmosis (water) |
| $S$ | Subthreshold slope |
| SAM | Self-assembled monolayer |
| $t$ | Accumulation layer (channel) thickness |
| $T$ | Absolute temperature |

| | |
|---|---|
| $T_{CURIE}$ | Curie temperature |
| TFT | Thin-film transistor |
| UV | Ultraviolet |
| $V$ | Voltage |
| $V_{BD}$ | Dielectric breakdown voltage |
| $V_D$ | Drain voltage |
| $V_{DS}$ | Drain-to-source voltage |
| $V_{REF}$ | Reference voltage |
| $V_G$ | Gate voltage |
| $V_{GS}$ | Gate-to-source voltage |
| $V_{IN}$ | Input voltage |
| $V_{OUT}$ | Output voltage |
| $V_{STRESS}$ | Bias stress voltage |
| $V_{WF}$ | Work function difference voltage |
| $V_t$ | Threshold voltage |
| $V_X$ | Voltage at a distance x from the source |
| $W$ | Channel width |
| WF | Work function |
| ZnO | Zinc oxide |
| $\alpha, \beta, \gamma, \delta$ | PVDF/P(VDF-TrFE) crystal structures |
| $\beta$ | Stretching parameter |
| $\theta$ | Contact angle |
| $\rho$ | Hole density |
| $\rho_3$ | Pyroelectric coefficient |
| $\sigma$ | Electrical conductivity |
| $\tau$ | Time constant |

# List of publications

## Journal papers

1. S. Hannah, A. Davidson, I. Glesk, D. Uttamchandani, R. Dahiya and H. Gleskova, "Multifunctional sensor based on organic field-effect transistor and ferroelectric polyvinylidene fluoride trifluoroethylene," *Organic Electronics*, (Under review).
2. S. Hannah, J. Cardona, D. Lamprou, P. Sutta, P. Baran, A. Ruzaiqi, K. Johnston and H. Gleskova, "Interplay between vacuum-grown monolayers of alkylphosphonic acids and the performance of organic transistors based on dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene," *ACS Applied Materials and Interfaces* **8** (2016), pp. 25405 – 25414.
3. S. Gupta, S. Hannah, C. Watson, P. Sutta, R. Pedersen, N. Gadegaard and H. Gleskova, "Ozone oxidation methods for aluminium oxide formation: Application to low-voltage organic transistors," *Organic Electronics* **21** (2015), pp. 132-137.

## Conference papers

1. S. Hannah, D. Uttamchandani, S. Khan, R. Dahiya and H. Gleskova, "Response of P(VDF-TrFE) sensor to force and temperature," *IEEE Prime 2015*, ($29^{th}$ June – $2^{nd}$ July 2015), Glasgow, UK, pp. 369 – 372, DOI: 10.1109/PRIME.2015.7251412.

## Invited talks

1. S. Hannah, "Response of P(VDF-TrFE) sensor to force and temperature," *IEEE Prime 2015*, 29th June – 2nd July 2015, Glasgow, UK.

## Conference posters

1. S. Hannah, D. Uttamchandani, R, Dahiya and H. Gleskova, "Force sensing enabled by P(VDF-TrFE) sensor coupled with organic thin-film transistor," Innovations in Large-Area Electronics Conference (innoLAE) 2016, 1st -2nd February 2016, Robinson College, Cambridge, UK.
2. S. Hannah, D. Uttamchandani, R. Dahiya and H. Gleskova, "Response of P(VDF-TrFE) sensor coupled with organic transistor to static force," 2nd Asian European Symposium on Organic Optoelectronics, 27th – 29th October 2015, Royal Society of Edinburgh, Edinburgh, UK.
3. A. Al-Ruzaiqi, S. Hannah, M. Aghamohammadi, H. Klauk and H. Gleskova, "Effect of alkylphosphonic acid monolayer on the bias stability of low-voltage organic transistors," UK Semiconductors Conference 2015, 1st – 2nd July 2015, Sheffield Hallam University, Sheffield, UK.
4. S. Hannah and H. Gleskova, "Comparison of 2 V organic thin-film transistors fabricated on free-standing commercial PEN foils," Innovations in Large-Area Electronics Conference (innoLAE) 2015, 3rd – 4th February 2015, Downing College, Cambridge, UK.

5. S. Gupta, S. Hannah and H. Gleskova, “Correlation between the structure of the dielectric monolayer and the performance of low-voltage transistors based on pentacene,” Organics, Photonics & Electronics: Faraday Discussion 174, 8th – 10th September 2014, University of Strathclyde, Glasgow, UK.
6. S. Hannah and H. Gleskova, “Aluminium oxide prepared by atomic layer deposition in organic thin-film transistors operating at 2 V: comparison with UV-ozone oxidation,” 56th Electronics Materials Conference (EMC 2014), 25th – 27th June 2014, University of California, Santa Barbara, U.S.
7. S. Hannah and H. Gleskova, “Aluminium oxide prepared by atomic layer deposition in organic thin-film transistors operating at 2 V: comparison with UV-ozone oxidation,” The 10th International Conference on Organic Electronics, 11th – 13th June 2014, San Germiniano Complex, Modena, Italy.

# Chapter 1

# Introduction

## 1.1 Organic electronics

Organic electronics encompasses a range of materials and fabrication steps to create electronic circuit elements using carbon-based organic materials. The term organic electronics is analogous to flexible or printable electronics, which together are generally termed large-area electronics. Large-area refers to potential scalability of organic devices such as organic thin-film transistors (OTFTs), organic light-emitting diodes (OLEDs), sensors, organic solar cells (OSCs) and displays etc. over

large substrate areas. Over the last 35 years or so, organic electronics has attracted significant commercial interest, particularly in the development of lighting technology, as well as for flexible displays for mobile phones and televisions.

Organic devices offer many advantages over conventional inorganic counterparts such as low fabrication temperature, low cost and non-planar form factors. As a result, unlike silicon-based electronics, novel organic devices can be fabricated on a wide range of flexible substrates such as plastic or paper. Commonly used plastic substrates such as polyethylene naphthalate (PEN) and polyethylene terephthalate (PET) are used in flexible OLED displays [1], flexible pressure sensors [2], RFID tags [3] and disposable electronics [4]. Figure 1.1 shows a photograph of a flexible active-matrix OLED (AMOLED) display on a PEN substrate. A photograph showing OTFTs arranged in an active-matrix to create the readout electronics for an electronic artificial skin is presented in Figure 1.2.

The flexibility element of organic devices is crucial for sensing applications where the requirement of stretchable, foldable or bendable sensors over large-areas is imminent.

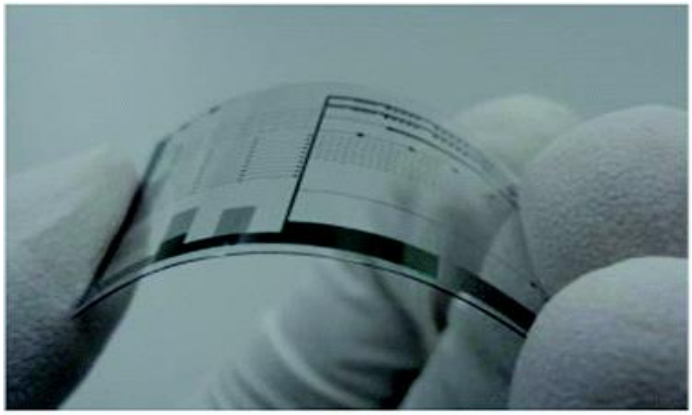


**Figure 1.1:** Flexible AMOLED display on PEN substrate [1].

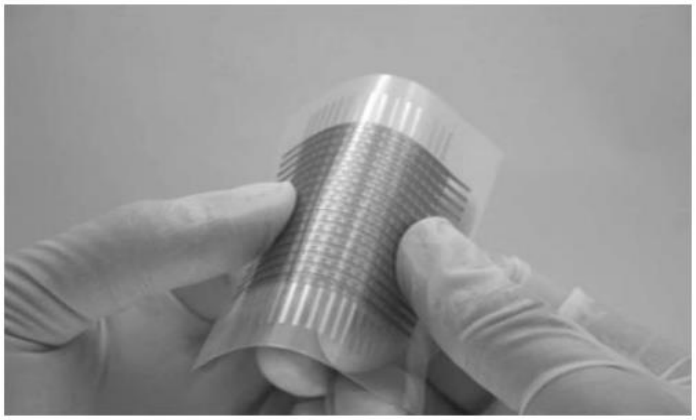


**Figure 1.2:** Flexible active-matrix pressure sensor comprising OTFTs as read-out electronics [2].

## 1.2 Tactile sensing

Tactile sensing refers to the process of detecting and processing a given contact event (such as force or temperature) over a defined area and performing initial processing of the event. Using this definition, a tactile sensor is a device which can measure contact parameters through interaction with the surrounding environment. Tactile sensors are particularly useful within the field of robotics. To enable a humanoid robot to achieve effective human-robot interaction, the robot must be able to interact safely through touching its surroundings in order to cause no harm to the humans or themselves. Robots will be able to learn about their new environments by interacting with everyday objects, and properties of objects such as mechanical compliance can only be assessed via the sense of touch. In addition, for safety reasons, humanoid robots able to detect changes in contact temperature will be at a distinct advantage for applications within the medical or care sectors.

Effective tactile sensing requires two features – sensing and processing. Firstly, the parameter of interest such as force or temperature must be detected. However for this detection to be useful, it must go through some form of processing. This system is analogous to a human's ability to sense and then pass on that information to the central nervous system to pre-process the signals for the brain. By combining multiple sensors and processing units such as OTFTs together on a single flexible substrate, an electronic skin (e-skin) can be developed. Figure 1.3 shows electronic films on flexible substrates creating a large-area e-skin for use on humanoid robots.

Various sensors exist to detect force and temperature. For force, sensors typically exploit capacitive changes [5], the piezoresistive effect [6] and the piezoelectric effect [7] whereas capacitive and pyroelectric effects [8] are used for detecting changes in temperature. Figure 1.4 shows an example of a humanoid robot fitted with capacitive tactile sensors providing touch sensitivity.

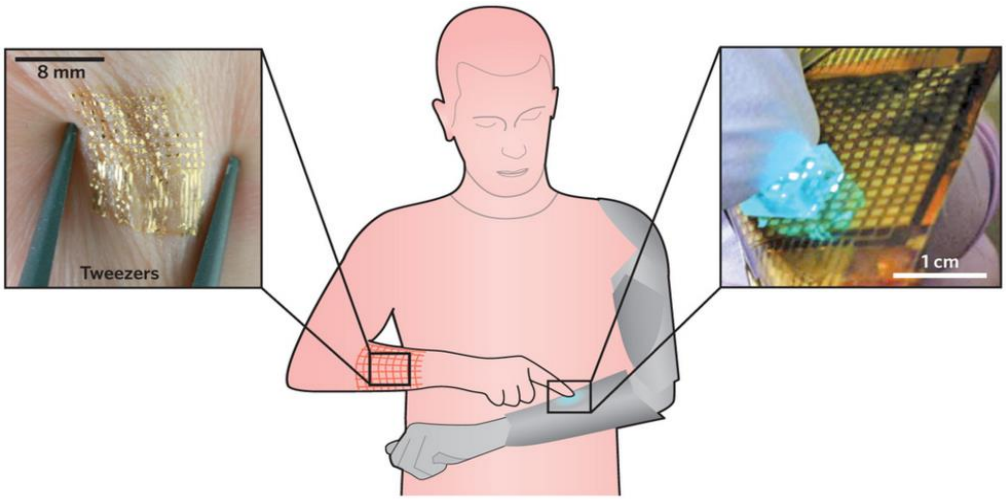



**Figure 1.3:** Humanoid skin made of ultrathin electronics on elastomeric substrates [9].

**Figure 1.4:** Humanoid robot fitted with capacitive tactile sensors for touch detection [10].

## 1.3 Research motivation

An effective tactile skin not only requires sensors for detection of parameters such as force and temperature, but it requires a form of electronics for pre-processing of the sensor output signal. Organic thin-film transistors are excellent candidates to provide signal amplification from a tactile sensor. By careful selection of the substrate, gate dielectric, semiconductor and device contacts, OTFTs can be operated at voltages less than 2 V [11, 12]. Low-voltage operation results in reduced power consumption for electronic circuits such as e-skin. OTFTs have a distinct advantage over inorganic counterparts in terms of their required fabrication temperature, which enable them to be produced on mechanically compliant flexible plastic substrates.

This thesis shows that through careful selection of gate dielectric materials and plastic substrate, low-voltage OTFTs can be produced at low cost on plastic foils for use within a tactile sensing system for force and/or temperature detection.

A useful electronic skin has the ability to sense and process in-situ multiple contact parameters such as force, temperature, humidity etc. To date, many tactile sensors exist capable of sensing compressive force events, but show little or no sensitivity to applied temperature [13, 14]. This thesis shows that by combining a ferroelectric polymer (P(VDF-TrFE)) with a flexible OTFT both force and temperature events can be monitored with almost equivalent sensitivities.

## 1.4 Thesis objectives

This thesis presents tactile force and temperature sensors that combine a low-voltage organic thin-film transistor with a ferroelectric polymer-based parallel-plate capacitor. To reduce the operating voltage of the sensing circuit, low-voltage transistor operation was required. This was achieved by using an ultra-thin bi-layer gate dielectric formed of aluminium oxide ($AlO_x$), prepared by the UV/ozone oxidation of aluminium, and a vacuum-deposited self-assembled monolayer of phosphonic acid ($C_n$PA). Namely, $AlO_x$ preparation method along with an investigation of alkyl phosphonic acids with varied alkyl chain length were employed to produce OTFTs with large gate dielectric capacitance, low-leakage current density, and low threshold voltage. In addition, an air-stable organic semiconductor dinaphtho[2,3-b:2′,3′-*f*]thieno[3,2-*b*]thiophene (DNTT) was implemented to achieve OTFTs with improved field-effect mobility and bias stress stability. Finally, the OTFT fabrication was tested on two flexible plastic substrates to pave the way for future flexible sensors.

Force and temperature sensors have been realised by combining the P(VDF-TrFE) capacitor with an OTFT. Response of such sensors to compressive normal force and temperature are presented in the thesis.

## 1.5 Thesis outline

This thesis is outlined as follows. Chapter 2 describes the background material behind OTFTs and ferroelectric materials. The fabrication procedures adopted to create metal-insulator-metal (MIM) structures, OTFTs and P(VDF-TrFE) sensors are outlined in Chapter 3. The chapter also introduces the various electrical measurements performed on the structures to gain an insight into device performance. Chapter 4 discusses the effect of phosphonic acid alkyl chain length on OTFT performance. Transfer of the OTFT fabrication procedure onto plastic substrates is optimised in Chapter 5. Chapter 6 details the capacitive response of the P(VDF-TrFE) capacitor to compressive force and temperature. Response of the P(VDF-TrFE)/OTFT sensor to force and temperature is presented in Chapter 7. Finally, Chapter 8 concludes the thesis and provides scope for future work.

## 1.6 Thesis contributions

The main contributions of this thesis are:

- Optimisation of the vapour-deposited alkyl phosphonic acid monolayer ($C_nPA$) with respect to the alkyl chain length (n = 8, 10, 12, 14, 16, and 18). The effect of the monolayer on the OTFT short- and long-term performance was also investigated and it has been shown that $C_{18}PA$ provided transistors with the highest field-effect mobility, lowest threshold voltage, and improved bias-stress stability.
- Transfer of the low-voltage OTFT fabrication process onto two plastic (PEN) substrates and optimisation of PEN pre-treatment and DNTT deposition in terms of deposition rate.
- First demonstration of capacitive response of P(VDF-TrFE) capacitor to force and temperature. The results showed that the sensor capacitance increases logarithmically with the applied compressive force, while it increases linearly with the increasing temperature.
- Design and development of P(VDF-TrFE)/OTFT sensor for monitoring normal force and temperature with the emphasis on monitoring the static pressure and temperature. The achieved results constitute the first demonstration that the capacitive properties of the ferroelectric P(VDF-TrFE) co-polymer can be exploited in addition to its piezoelectric and pyroelectric properties.

# Chapter 2

# Research background

The aim of this chapter is to present the organic thin-film transistor (OTFT) and the properties of ferroelectric materials. OTFT structure, operating regimes and the underlying physics pertinent to understanding the OTFT is introduced. Background information on the related metal-insulator-metal (MIM) structure and the field effect transistor are provided in Sections 2.1 and 2.2 respectively. Section 2.3 focusses on charge carrier transport within the organic thin-film transistor. OTFT operation is discussed in Section 2.4, with important OTFT performance parameters highlighted in Section 2.5. The state of the art in low-voltage OTFT operation is

given consideration in Section 2.6. In addition, information related to understanding ferroelectricity and ferroelectric materials is presented. Section 2.7 introduces the concept of electric polarisation and explains the difference between the polarisation of a linear dielectric, paraelectric polarisation and ferroelectric polarisation. Ferroelectricity is described in detail in Section 2.8. Sections 2.9 and 2.10 discuss piezoelectricity and pyroelectricity respectively, with Section 2.11 introducing ferroelectric polymers PVDF and P(VDF-TrFE). Section 2.12 describes the merger of the ferroelectric capacitor with the organic transistor and includes an example of a piezoelectric oxide semiconductor field-effect transistor (POSFET) for illustration. Finally, the chapter is summarised in Section 2.13.

## 2.1 Metal-insulator-metal (MIM) structure

Before discussing the structure of the organic thin-film transistor, it is worth mentioning the metal-insulator-metal (MIM) structure; i.e. a parallel-plate capacitor. A parallel plate capacitor comprises two parallel conducting layers sandwiching a dielectric. The conducting layers are often made of the same metal to reduce fabrication complexity; however, the metals can be different.

An electric field ($E$) is present when a voltage ($V$) is applied across the electrodes. Application of an electric field causes polarisation within the dielectric, i.e. on a microscopic scale the centres of the positive and negative charge separate. This is represented by a relative permittivity ($\varepsilon_r$) that becomes larger than 1. Figure 2.1 depicts a typical MIM structure in the presence of an external electric field.

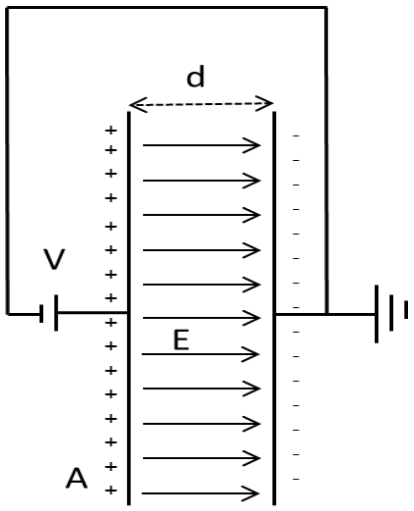



**Figure 2.1:** Metal-insulator-metal (MIM) structure. *A* is the area of each electrode and *d* is the distance between them.

The amount of charge (*Q*) developed on the metal electrodes is a function of the capacitance (*C*) of the dielectric and the applied external voltage (*V*), as expressed in Equation 2.1.

$$Q = CV \tag{2.1}$$

The capacitance is proportional to the area (*A*) of the capacitor and inversely proportional to *d*, the separation between the metal electrodes (thickness of the dielectric), as given in Equation 2.2, where $\varepsilon_o$ is the electrical permittivity of vacuum equal to $8.85\times10^{-12}$ F/m and $\varepsilon_r$ is the relative permittivity of the dielectric material itself. Capacitance has units of Farads (F) and can also be expressed in F/cm$^2$, thereby accounting for the area of the capacitor.

$$C = \frac{\varepsilon_0 \epsilon_r}{d}\cdot A \tag{2.2}$$

The metal-insulator-metal structure is a useful tool for assessing the properties of a dielectric material and is therefore used commonly when investigating the performance of organic thin-film transistors.

## 2.2 Field-effect transistor

A field-effect transistor (FET) is a unipolar transistor requiring a gate-induced electric field to modulate the charge carrier density within the semiconductor material. The essential part of a FET is the metal-insulator-semiconductor (MIS) structure, akin to the MIM structure; in this case one of the metal electrodes is replaced by a semiconductor. The FET terminals are called gate, source and drain. The gate electrode is electrically isolated from the semiconductor layer by the dielectric. The source and drain terminals on the other hand are in direct contact with the semiconductor layer.

A voltage applied to the metal electrode, called the gate, modulates the conductivity in the semiconductor material next to the dielectric/semiconductor interface. Such a transistor is classed as unipolar because it requires only one type of carrier to operate (e.g. electrons in n-type or holes in p-type). FETs feature an active channel, along which electrons or holes flow from the source to the drain.

Flow of current between the source and drain terminals ($I_D$) is controlled by the voltage applied to the gate electrode. The magnitude of the voltage applied to the gate and drain terminals controls the magnitude of the resulting drain current as the

voltages applied affect the size and shape of the conductive channel. The source electrode is typically grounded.

FETs can operate in a number of ways. A common mode of operation is found by using an n-channel enhancement-mode device. In this case, there is no conductive channel initially, and a positive gate-to-source voltage must be applied to form one. The gate voltage attracts free electrons towards the gate, and a channel forms. Through doing so, a depletion region is created. The threshold voltage marks the point where the depletion region begins. By increasing the voltage on the gate, more electrons will be attracted towards the gate and a channel forms between source and drain in a process known as inversion.

FETs are composed of a number of different materials, namely metals, semiconductors and dielectrics. Aluminium (Al) and gold (Au) are the most commonly used metals. Examples of dielectrics include silicon dioxide ($SiO_2$), silicon nitride ($Si_3N_4$), and aluminium oxide ($Al_2O_3$). Various semiconductors have been used to date, with crystalline silicon being the most common due to its well-established fabrication process developed over five decades. In addition to various inorganic semiconductors, organic conjugated polymers also exhibit semiconducting properties which led to the development of organic FETs. Common examples of organic semiconductors include the thiophenes and pentacene.

### 2.2.1 Organic thin-film transistor

In recent years, organic semiconducting materials have been applied to various electronic devices such as field-effect transistors, solar cells, light-emitting diodes, etc., and the performance of these devices is continuously improving. Organic thin-film transistors (OTFTs) are similar to other FETs, the main difference is in the selection of materials; OTFTs always use organic semiconductors such as pentacene or DNTT and sometimes they also feature an organic dielectric. OTFTs are built up layer by layer on a substrate that can be rigid (e.g. glass), or flexible (e.g. plastic or paper) and, therefore, are often called thin-film transistors instead of field-effect transistors.

Organic thin-film transistors (OTFTs) can be produced in different device architectures; bottom-gate top-contact (BGTC) and bottom-contact top-gate (BCTG) being the two most commonly found. A cross-sectional representation of these two architectures is shown in Figure 2.2 (a) and (b) respectively. The bottom-gate top-contact architecture is the one adopted in this thesis.

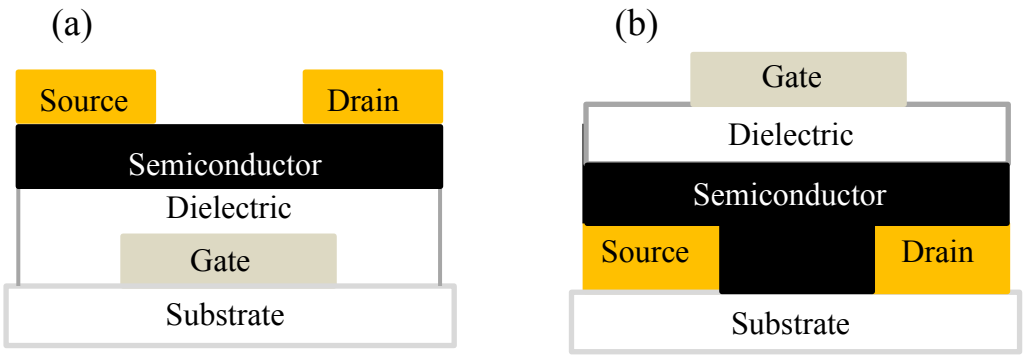



**Figure 2.2:** OTFT cross section: bottom-gate top-contact (a), and bottom-contact top-gate (b).

## 2.3 OTFT carrier transport

In the OTFT, current flow between the source and drain terminals is controlled by the magnitude of the voltage applied to the gate terminal. In a p-type OTFT, negative $V_{GS}$ is required to promote hole accumulation, whereas positive $V_{GS}$ is necessary for electron accumulation in an n-type device.

Let us assume that the applied $V_{GS}$ is high enough to induce charge carrier accumulation and the formation of a conducting channel in the organic semiconductor near the semiconductor/dielectric interface. In a p-type organic thin-film transistor, the channel contains the positive charge and charge transport occurs through the highest occupied molecular orbital (HOMO) levels of the organic semiconductor. In the n-type OTFT, negative charge is accumulated in the transistor channel and charge transport occurs through the lowest unoccupied molecular orbital (LUMO) levels of the organic semiconductor. The HOMO and LUMO bands are an analogy to the valence and conduction bands of inorganic semiconductors. Figure 2.3 illustrates the energy level diagram of the semiconductor/dielectric interface when charge accumulation occurs in p- or n-type OTFTs. Furthermore, Figure 2.4 shows the energy level diagram along the OTFT conducting channel, featuring the source and drain with the semiconductor.

In contrast to semiconductors, metals exhibit no energy gap between their ‘valence’ and ‘conduction’ bands; therefore their Fermi energy ($E_F$) is a useful figure of merit when investigating charge transport between metals and semiconductors. In the context of the OTFT, the energy barrier associated with electron or hole injection

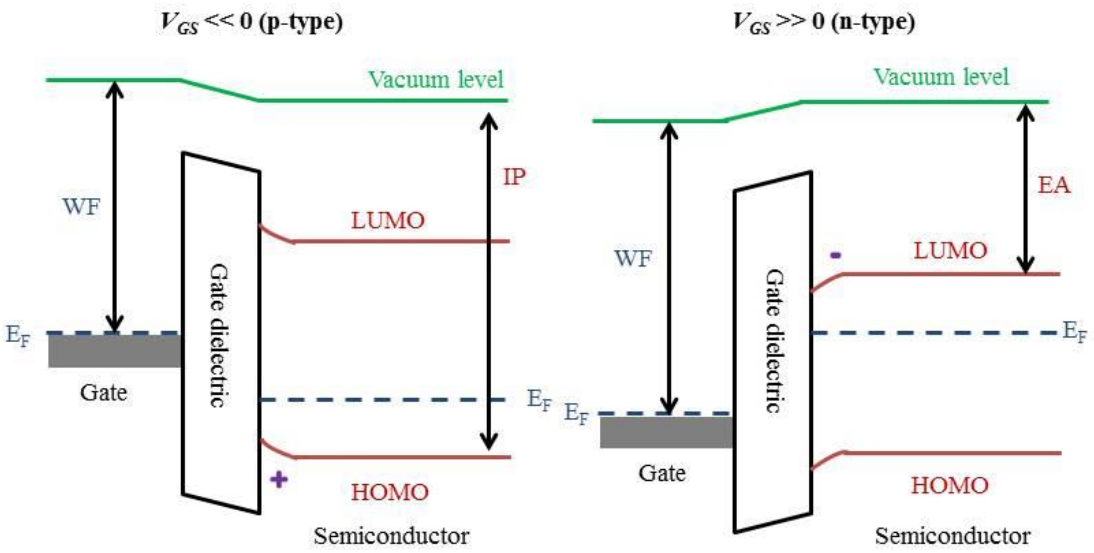



**Figure 2.3:** OTFT dielectric/semiconductor interface energy level diagram. $E_F$ is the Fermi energy, *WF* is the work function of the metal, *IP* is the ionisation potential and *EA* represents the electron affinity.

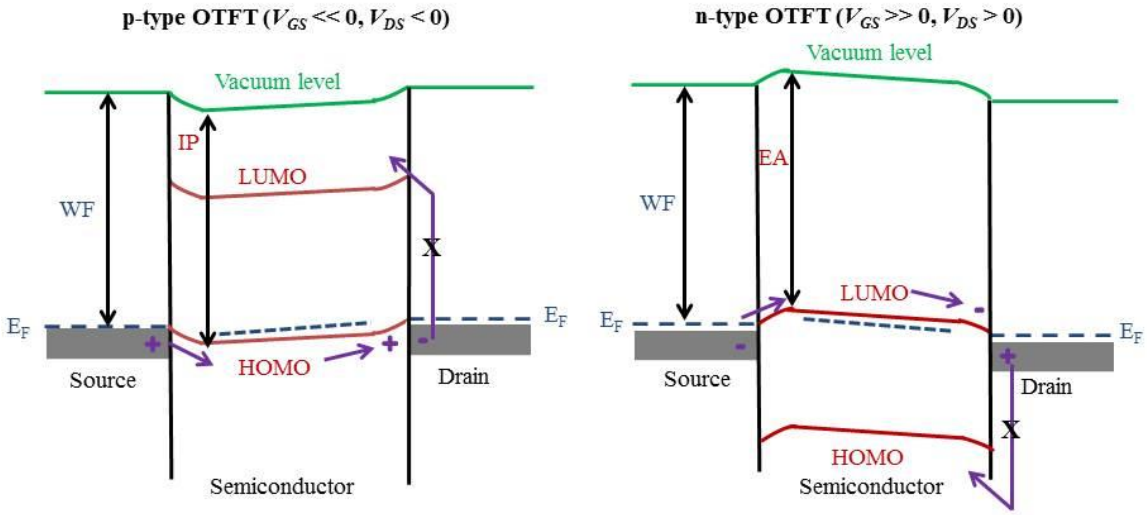



**Figure 2.4:** OTFT energy level diagram along the transistor channel.

from the source contact to the organic semiconductor is the difference between the work function of the metal and the electron affinity of the organic semiconductor or the difference between the work function of the metal and the ionisation potential of the organic semiconductor respectively, as demonstrated in Figure 2.3. For a p-type OTFT, good hole injection can be achieved between the metal and the semiconductor if the work function of the source and the ionisation potential of the organic semiconductor are similar, i.e. there is good alignment between the $E_F$ and the top of HOMO. For the OTFT, choice of semiconductor/electrode materials determines p-type or n-type behaviour. The p-type OTFTs presented in this thesis are composed of organic semiconductor dinaphtho[2,3-b:2′,3′-*f*]thieno[3,2-*b*]thiophene (DNTT) and use gold source/drain contacts.

## 2.4 Organic thin-film transistor operation

When a $V_{GS}$ higher in magnitude, i.e. more negative than the transistor turn-on voltage for a p-type transistor is applied to the gate electrode, channel formation occurs. To complete the OTFT operation a drain-to-source ($V_{DS}$) voltage must also be applied. Upon application of $V_{DS}$, the charge induced in the transistor channel closes the electrical loop and a drain current $I_D$ is measured. For a p-type OTFT, the polarity of the drain-to-source voltage must also be negative. The direction of current flow is from the source to the drain, and this current can be modulated by varying the voltage applied to the transistor gate. Figure 2.5 shows the process of channel formation within a p-type OTFT device.

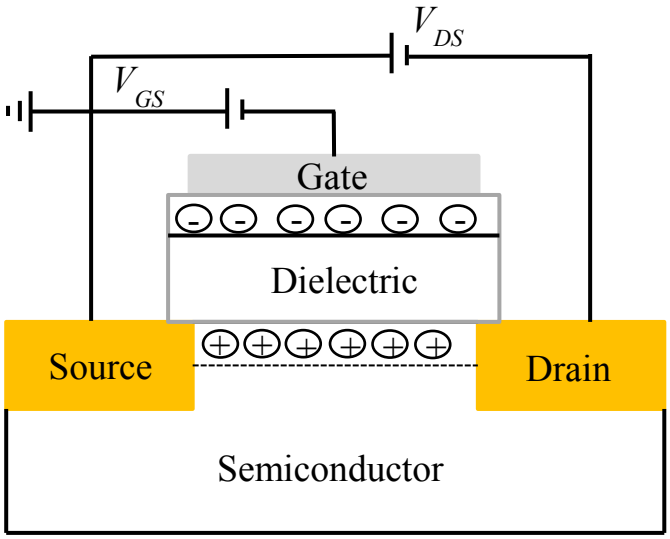



**Figure 2.5:** OTFT channel formation at the semiconductor/dielectric interface.

The magnitude of the drain current depends on the amount of charge ($Q$) induced in the channel. The higher the charge density, the greater the $I_D$. Theoretically, all the developed charge at the semiconductor/dielectric interface should flow along the formed transistor channel. However, in reality, some carriers leak through the gate dielectric to the gate and are measured as a tangible gate current ($I_G$). $I_G$ depends on the gate dielectric layer and in a well-designed transistor it is several orders of magnitude smaller than $I_D$.

Other factors can influence the amount of charge developed at the interface. For example, no transistor behaves completely ideally, and charges can become trapped within the semiconductor itself or near the semiconductor/dielectric interface. Fabrication, exposure to an ambient air or UV light can lead to the additional formation of defects that can be detrimental to OTFT performance.

Trapped charge and defects account for a reduction in the overall charge density at the semiconductor/dielectric interface. Consequently, the charge density is equal to the dielectric capacitance ($C$) multiplied by $V_{GS}$ minus some voltage, known as the transistor threshold voltage ($V_t$) as seen in Equation 2.3.

$$Q = C(V_{GS} - V_t) \tag{2.3}$$

Transistor operation depends on the magnitude of the voltages applied, and an OTFT has three major regimes of operation, namely the linear, saturation and subthreshold regimes. These regimes are described in more detail in the following sub-sections.

### 2.4.1 Linear regime

The first OTFT operating region of interest is the linear regime. In such a case the non-zero drain-to-source voltage is less than the gate-to-source voltage minus the transistor threshold voltage (see Equation 2.4).

$$0 < |V_{DS}| < (|V_{GS} - V_t|) \tag{2.4}$$

Let the x-direction be the direction along the transistor channel from the source to the drain. The charge ($Q_x$) per unit area induced by $V_{GS}$ within the channel for a voltage at a given point along the x-direction ($V_x$) is given by Equation 2.5.

$$Q_x = C(V_{GS} - V_t - V_x) \tag{2.5}$$

The value of $V_x$ varies along the channel from the source to the drain. For example, at the source electrode, $V_x = 0$, whereas $V_x = V_{DS}$ at the drain. The values of $V_x$ at these points set the integration limits when obtaining the expression for $I_D$ (Equation 2.7). Firstly, the channel current is given by Equation 2.6.

$$I_D = \frac{dQ}{dt} = \frac{dQ}{dx}\frac{dx}{dt} \tag{2.6}$$

Drain current ($I_D$) is equal to the current density ($J$) multiplied by the cross-sectional area of the channel ($A_{ch}$). Current density $J$ is by definition a product of electrical conductivity ($\sigma$) and electric field ($E$) along the transistor channel, where the conductivity $\sigma$ is given by Equation 2.7.

$$\sigma = qp\mu \tag{2.7}$$

where $q$ is the charge of an electron, $p$ is hole density and $\mu$ refers to the hole mobility. Knowing that drain current is $J \times A_{ch}$, the following expression for drain current can be derived by substitution (Equation 2.8).

$$I_D = qp\mu A_{ch}\frac{dV_x}{dx} \tag{2.8}$$

where $A_{ch}$ is a product of the channel width ($W$) and the thickness of the accumulation layer ($t$). Taking $qp$ as $Q/t$, Equation 2.9 can be obtained.

$$I_D dx = C(V_{GS} - V_t - V_x)\mu W dV_x \tag{2.9}$$

The final mathematical step required to obtain the expression for OTFT drain current as a function of $V_{GS}$ and $V_{DS}$ is to integrate Equation 2.9 within integration limits of its channel length ($L$). Equation 2.10 shows the integration limits applied to Equation 2.9 which is subsequently solved and revealed in Equation 2.11.

$$\int_0^L I_{\mathrm{D}} dx = C\mu W \int_0^{V_{\mathrm{D}}} (V_{\mathrm{GS}} - V_{\mathrm{t}} - V_{\mathrm{x}}) dV_{\mathrm{x}} \tag{2.10}$$

$$I_{\mathrm{D}} = \mu C \left(\frac{W}{L}\right) V_{\mathrm{DS}} \left[(V_{\mathrm{GS}} - V_{\mathrm{t}}) - \frac{V_{\mathrm{DS}}}{2}\right] \tag{2.11}$$

In the linear operating regime of the OTFT, $|V_{DS}|$ is typically much smaller than $|V_{GS} - V_t|$, therefore Equation 2.11 can be reduced to the expression shown in Equation 2.12. The overall drain current in the linear regime is a function of $V_{DS}$, and is linear in its response to increasing drain-to-source voltage [15].

$$I_{\mathrm{D}} = \mu C \left(\frac{W}{L}\right) (V_{\mathrm{GS}} - V_{\mathrm{t}}) V_{\mathrm{DS}} \tag{2.12}$$

### 2.4.2 Saturation regime

The OTFT operating region known as the saturation regime is characterised by a drain-to-source voltage larger than the gate-to-source voltage minus the transistor threshold voltage (Equation 2.13).

$$|V_{DS}| > |V_{GS} - V_t| \tag{2.13}$$

OTFT drain-to-source voltage plays an important role in OTFT operation. When $|V_{DS}|$ is increased $V_{\mathrm{x}}$ is increased too. This results in a smaller charge density at the drain electrode. When $V_{\mathrm{DS}} = V_{\mathrm{GS}} - V_{\mathrm{t}}$ the induced charge density at the drain is zero and the so-called "pinch-off" point in the transistor operation has been reached. This marks the starting point of the transistor's saturation regime and further increase in $V_{\mathrm{DS}}$ results in a shift of the pinch-off point towards the source. OTFT drain current becomes independent of $V_{\mathrm{DS}}$ and the OTFT is said to be in the saturation regime. In

this regime, only the gate-to-source voltage $V_{GS}$ controls the magnitude of the drain current.

Referring to Equation 2.11, the drain current expression for the saturation regime can be obtained by substituting $V_{DS}$ for $V_{GS} - V_t$ as shown in Equation 2.14 [15].

$$I_D = \mu C \frac{W}{2L}(V_{GS} - V_t)^2 \tag{2.14}$$

Measurement of transistor output and transfer characteristics sheds more light on the current-voltage relationships of the OTFT for the different operating regimes. Figure 2.6 shows the transistor's linear and saturation regimes indicated on a set of output characteristics. Transistor $I_D$ changes linearly for small $V_{DS}$ and remains almost constant for higher $V_{DS}$.

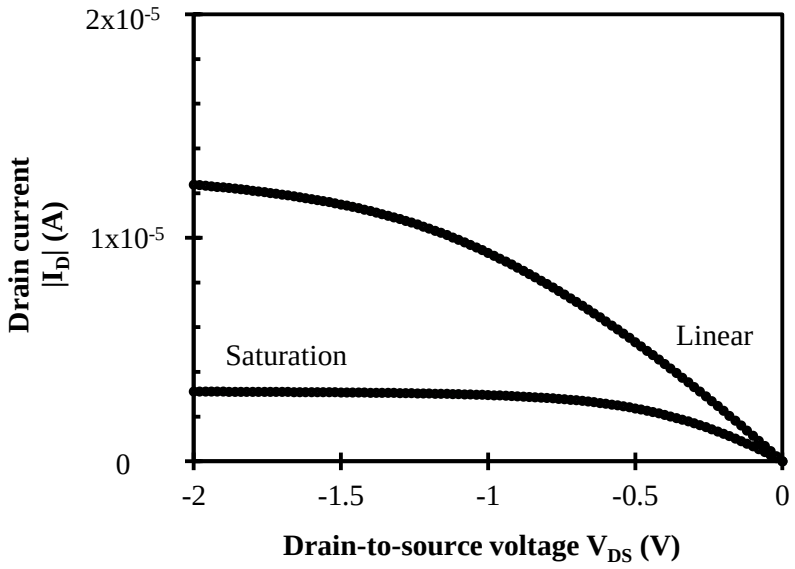



**Figure 2.6:** Drain current as a function of drain-to-source voltage in linear and saturation regimes.

### 2.4.3 Subthreshold regime

The third OTFT operating regime is known as the subthreshold regime. It is characterised by a gate-to-source voltage ($V_{GS}$) smaller than the transistor threshold, or turn-on voltage, $V_t$ as indicated by Equation 2.15.

$$|V_{GS}| < |V_t| \tag{2.15}$$

A common measurement used to assess OTFT electrical performance is evaluating the transistor transfer characteristics by measuring $I_D$ as a function of $V_{GS}$ for a fixed $V_{DS}$. For gate-to-source voltages below threshold, OTFT drain-current increases exponentially as a function of applied $V_{GS}$. This region is normally observed at a few 100's of millivolts below $V_t$, but is of course dependent on the individual transistor. Figure 2.7 shows a saturation regime transfer characteristic ($V_{DS}$ = −2 V), with threshold voltage and subthreshold slope ($S$) indicated.

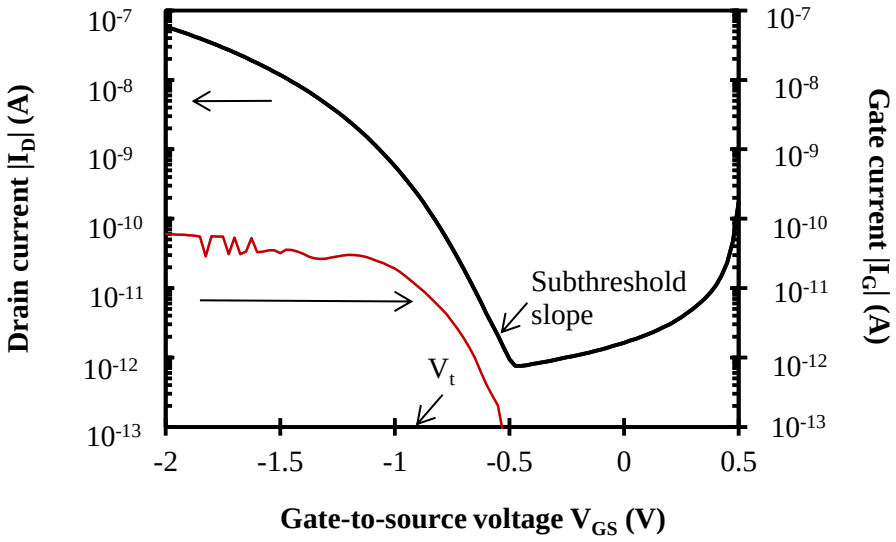



**Figure 2.7:** OTFT transfer characteristic in saturation regime ($V_{DS}$ = –2 V). Threshold voltage and subthreshold slope are shown.

## 2.5 OTFT performance parameters

Two measurements that are typically performed on an OTFT to assess its electrical performance are the output and transfer characteristics, as shown in Figures 2.6 and 2.7. Output characteristics are used to investigate the influence of drain-to-source voltage on the drain current for various fixed values of gate-to-source voltage. Transfer characteristics on the other hand record changes in drain current as a function of sweeping $V_{GS}$ for a fixed $V_{DS}$.

The gate dielectric layer of an OTFT plays a crucial role in determining device performance. Its capacitance determines the transistor drain current, whilst its thickness determines the gate leakage current ($I_G$) and the dielectric breakdown voltage ($V_{BD}$). Higher dielectric capacitance produces greater $I_D$ but requires a thin dielectric. However, a trade-off exists for the dielectric thickness since a thicker layer may be required to reduce $I_G$ and increase $V_{BD}$, thus reducing the capacitance.

OTFT device parameters can be extracted from the transfer characteristics. In addition to threshold voltage and field-effect mobility, the subthreshold slope, ON-current ($I_{ON}$) and OFF-current ($I_{OFF}$) can be obtained. Threshold voltage is the gate-to-source voltage extracted using Equation 2.12 (linear regime) or 2.14 (saturation regime). The field-effect mobility is a reflection of how well charge carriers (holes or electrons) move through the semiconductor. $I_{ON}$ and $I_{OFF}$ are the maximum and minimum drain currents in the saturation regime respectively. Often quoted as a ratio, the ON/OFF current ratio is a useful figure of merit particularly for

logic circuits, where a high ON/OFF current ratio is needed to distinguish between transistor on and off states effectively.

Surface characterisation techniques exist to assess various transistor layer properties. Surface roughness, typically evaluated by atomic force microscopy (AFM), plays an important role for the dielectric and semiconductor layers. AFM allows taking surface images on a nanometre scale and the extraction of the root-mean-square (RMS) surface roughness. Low dielectric surface roughness is important for subsequent organic semiconductor deposition in the bottom-gate top-contact architecture. In addition, Fourier-transform infrared spectroscopy (FTIR) and contact angle goniometry (CAG) can be performed on the samples to provide a greater insight into layer quality and surface properties. FTIR captures the response from different vibrational modes that represent the molecular structure and molecular interactions within the layer under investigation. CAG measurements provide information about the wettability of a particular surface. Surface energies can be calculated from the measured liquid/solid contact angles.

In conclusion, various figures of merit exist to evaluate the organic thin-film transistor. The gate dielectric layer is characterised by its capacitance, leakage current, breakdown voltage and surface roughness. In terms of OTFT performance, the main figures of merit are threshold voltage, field-effect mobility, subthreshold slope, ON-current and the OFF-current. To achieve good OTFT performance, careful selection of the dielectric, semiconductor and contact materials including the associated processing steps must be chosen as the various interfaces between the layers affect parameters such as OTFT contact resistance.

The focus of this thesis is on low-voltage organic thin-film transistors based on air stable organic semiconductor DNTT; optimised in terms of its deposition to provide transistor performance comparable with similar devices reported by others.

## 2.6 OTFT state of the art

The use of organic thin-film transistors in displays [16, 17], inverters [18, 19], amplifiers [20] and NAND or NOR logic gates [21] requires reduction in OTFT operating voltages. Low operating voltage can be achieved through the use of ultra-thin and/or high-k dielectrics. However, to attain high-performing transistors, such dielectrics must also display very low leakage current. Various dielectrics such as HfLao (k ~ 15.3) [22, 23], $Ba_{1.2}Ti_{0.8}O_3$ (k ~ 15.57) [24], $SrTiO_3$ (k ~ 12.1) [25] and polymer dielectrics (k ~ 12.6) [26] have been implemented previously for low-voltage OTFT operation. Another approach to low-voltage operation is through use of thin layer medium-k dielectrics [27] such as aluminium oxide ($AlO_x$) (k ~ 6.2) [28]. Often, the aluminium oxide layer is functionalised with organic monolayers to reduce the leakage current and surface energy [29] or coated with polymer layers [30, 31]. However, such treatment leads to a slight reduction in dielectric capacitance while maintaining low operating voltages. By modifying $AlO_x$ with polymer layers, operating voltages as low as 6 V [30, 31] have been achieved. An improvement in OTFT performance in terms of operating voltage comes from the use of SAMs. For $AlO_x$ dielectrics, the use of SAMs [32, 33] has led to a vast improvement in transistor performance, notably $V_t$ and μ [33]. Of the various SAMs found in the literature, the

alkyl phosphonic acids are the most widely used [34–37]. These have resulted in operating voltages as low as 3 V [35–37].

One way to achieve ongoing improvement in OTFT field-effect mobility is through careful choice of the organic semiconductor material. Recently, flexible pentacene-based organic transistors featuring PMMA/PVP bi-layer gate dielectric showed field effect mobility ~ 1.51 $cm^2/Vs$ [38]. However, due to poor pentacene ambient stability resulting in detrimental OTFT performance [39], many groups are moving towards DNTT [40–42] to benefit from a more air-stable organic semiconductor. To date, OTFTs employing DNTT have achieved field-effect mobility of ~ 2 $cm^2/Vs$ [42].

## 2.7 Electric polarisation

One of the most important concepts fundamental to understanding various dielectric, ferroelectric and piezoelectric materials is how these materials respond to an external electric field. Upon application of an electric field, the position of the electrons is changed and the process of dipole formation follows. This is known as polarisation. If diploes are already present in the material, then the existing diploes will be re-aligned during the polarisation process as a result of the applied electric field.

The total electric polarisation present in a material comes from a contribution of different polarisation sources; electronic polarisation, ionic polarisation and orientation polarisation. The contribution each has towards the total polarisation level

is dependent upon the frequency of the applied electric field. Electronic polarisation typically has the largest effect on the overall polarisation level and refers to the electric dipole moment present. It relates to charge density displacement away from the unit cell centre in the crystalline lattice [43].

In an already polarised material, if an electric field were to be applied in the opposite direction to the polarisation, the polarisation direction can be changed to match the direction of the applied field, in a reversible process known as polarisation switching.

### 2.7.1 Linear dielectrics

A dielectric material is defined as one which is electrically insulating; however application of an external electric field can cause it to become polarised. Furthermore, if the molecular bonding within the particular dielectric is relatively weak, not only does the dielectric become polarised, the molecules may reorient themselves to the direction of the applied electric field.

There are two types of dielectrics: polar and non-polar. Polar dielectrics possess randomly orientated permanent dipole moments in the absence of an electric field, whereas in non-polar dielectrics the dipoles appear upon application of an electric field only.

The practical exploitation of the polarisation is in capacitors. Polarisation leads to an increase in a capacitor's relative permittivity, i.e. the ability of the

capacitor to store charge. Figure 2.8 shows a typical polarisation/electric field (P-E) curve for a dielectric material.

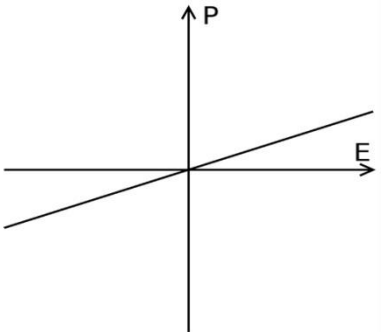



**Figure 2.8:** Typical P-E curve for a linear dielectric material [44].

### 2.7.2 Paraelectric polarisation

Paraelectric materials possess the ability to become polarised under an applied electric field regardless of whether the material features a permanent dipole moment. Paraelectrics display a significant non-linear P-E behaviour and the polarisation within a paraelectric material returns to zero if the electric field is removed.

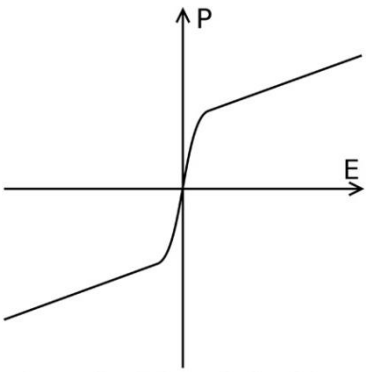



**Figure 2.9:** Typical P-E curve for a paraelectric material [44].

Paraelectricity can occur in the presence of unaligned dipoles which have the ability to align upon application of an external electric field. Figure 2.9 shows a typical P-E curve for a paraelectric material.

### 2.7.3 Ferroelectric polarisation

Ferroelectric materials can display spontaneous polarisation without an electric field being present. Although ferroelectric materials do not require an electric field to become polarised, if a ferroelectric material is subjected to an electric field, the spontaneous polarisation of the dipoles can be swapped to the opposite direction if the electric field is reversed, leading to a typical polarisation-electric field hysteresis loop shown in Figure 2.10.

When a ferroelectric material is heated above its Curie temperature ($T_{CURIE}$), it loses the ability to spontaneously polarise and it becomes a paraelectric material.

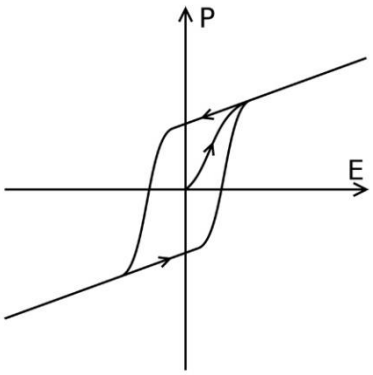



**Figure 2.10:** Typical P-E curve for a ferroelectric material [44].

## 2.8 Ferroelectricity

Ferroelectricity is a property associated with ferroelectric materials. The term ferroelectricity is analogous to ferromagnetism, where the material exhibits a permanent magnetic moment. Referring to Figure 2.10, the polarisation direction within ferroelectrics can be reversed by an electric field resulting in a useful hysteresis loop.

An example of a ferroelectric crystal is lead zirconate titanate (PZT). PZT features regions of uniform polarisation called domains. All dipoles within a particular domain are aligned in the same direction. When grown, a ferroelectric single crystal has several ferroelectric domains [45]. To create a single domain, a high d.c. electric field must be applied to the sample in a process known as poling that would align all domains in the direction of the electric field. In doing so, after removal of the electric field, the material contains remanent polarisation and has the ability to display piezoelectricity [46]. Ferroelectric materials belong to the class of polar piezoelectrics and include materials such as polyvinylidene fluoride (PVDF), polyvinylidene fluoride trifluoroethylene (P(VDF-TrFE) and PZT and as such, all ferroelectric materials are piezoelectric.

Due to the P-E hysteresis associated with ferroelectrics, they are ideal for memory-based applications. Through application of an electric field, the ‘stored’ polarisation of the ferroelectric capacitor can be read. The amount of charge required to switch the cell to the opposite memory state is measured and determines the state

of the cell. For memory-type applications, typically thin films of ferroelectric materials are adopted to reduce the voltage required to switch the polarisation state.

## 2.9 Piezoelectricity

The name piezoelectricity derives from the Greek word “piezo” meaning to press, and can roughly be translated as pressure-electricity. It relates to materials whereby upon application of mechanical stress an electric charge is generated. This charge can be appropriately harnessed to produce a voltage, useful for a whole host of applications from hydrophones [47] and shock transducers [48] to pressure sensors [49, 50].

Piezoelectricity was first discovered in materials such as zincblende and quartz in the late nineteenth century by the Curie brothers, Pierre and Jacques. Historically, the main application of the piezoelectric effect in quartz was for accurate timekeeping, lending a major advantage over the other available methods at the time. The real breakthrough in the field of piezoelectricity came in 1969 by Kawai [51] with the unearthing of a strong piezoelectric response in the polymer polyvinylidene fluoride (PVDF). The discovery of PVDF’s response to mechanical force opened up a variety of new applications where mechanical flexibility was a key requirement, for example for robotic applications and smart sensor-based systems.

A material is defined to be piezoelectric if it can be polarised by both an electric field and through application of mechanical stress. Piezoelectric materials can broadly be split into two distinct categories: polar and non–polar materials. All

ferroelectric materials fall into the polar piezoelectric material category since they possess a net dipole moment even when no external electric field is applied.

Piezoelectric materials display a piezoelectric effect; i.e. the material generates an electric charge as a result of a stress/force applied to its surface. Upon application of mechanical stress to a piezoelectric material, dipoles are created by separating the positive and negative molecular charges and a fixed charge momentarily appears on the surface of the material. Hence, from an application perspective, piezoelectric materials are excellent at sensing changes in force, but are not particularly suitable for static force sensing without additional circuitry to account for the inherent charge leakage effects within the piezoelectric.

The generated surface charge under standard short circuit conditions is proportional to the applied force (Equation 2.16), where $Q$ is the charge developed, $d_{33}$ is the piezoelectric coefficient of the material in C/N and $F$ is the applied force.

$$Q \propto d_{33} \times F \tag{2.16}$$

## 2.10 Pyroelectricity

In general, piezoelectric materials also display pyroelectric properties, i.e. they generate charge/voltage when subjected to a thermal contact or temperature change. The change in temperature affects the position of the atoms within the crystalline structure, modifying the material's polarisation properties. The change in polarisation results in generation of a voltage across the pyroelectric material.

Similarly to the piezoelectric effect, application of a static temperature results in the gradual reduction of the pyroelectric voltage due to charge leakage effects.

By combining the effects of piezo- and pyroelectricity, sensors can be created capable of detecting simultaneously changes in force and temperature. However, a challenge exists in being able to separate the two effects from one another.

Equation 2.17 describes the pyroelectric charge developed under short circuit conditions where $\rho_3$ is the pyroelectric coefficient (material dependent) in C/m$^2$K and $\Delta T$ is the temperature change.

$$Q \propto \rho_3 \times \Delta T \tag{2.17}$$

## 2.11 Ferroelectric polymers

Ferroelectric polymers belong to the class of crystalline polar polymers that exhibit a permanent electric polarisation. This polarisation can be reversed or switched when subjected to an electric field. Ferroelectric polymers are particularly suitable for many applications since they often exhibit high dielectric constants, strong piezoelectric and pyroelectric effects, and low acoustic impedance close to that of water and human skin [52]. Two commonly adopted ferroelectric polymers found in several applications are polyvinylidene fluoride (PVDF) and its copolymer polyvinylidene fluoride trifluoroethylene (P(VDF-TrFE)). Applications using PVDF or the copolymer material include actuators [53, 54], sensors [55, 56] and non-volatile memory [57]. The main advantage of using piezoelectric polymers particularly for sensing applications is their inherent mechanical flexibility, allowing

them to conform to a number of different surfaces and fulfil many unique applications.

### 2.11.1 Polyvinylidene fluoride (PVDF)

Polyvinylidene fluoride (PVDF) is the most commonly used ferroelectric polymer. It is a highly non-reactive semicrystalline fluoropolymer formed by the polymerisation of vinylidene difluoride containing linear chains arranged in a $(CH_2\text{-}CF_2)_n$ sequence. PVDF and its copolymer (P(VDF-TrFE)) are well understood and extremely promising for many applications as a result of being deposited using conventional methods such as spin-coating from solution. PVDF and in particular P(VDF-TrFE) are flexible, have high mechanical strength, display good chemical stability, and show high levels of spontaneous polarisation.

PVDF polymers commonly display four crystal structures (α, β, γ and δ), depending on the phase separation and crystallisation process [58] as well as the evaporation rate of the solvent when PVDF is formed from solution [59]. Figure 2.11 shows the chemical structure of PVDF in the α-phase (left-hand side) and β-phase (right-hand side).

By physically stretching the PVDF polymer, the ~ 50 % crystalline phase can be transformed from the thermodynamically stable α-phase into the β-phase in which the PVDF polymer chains adopt the planar zig-zag structure as shown in Figure 2.11 and are ordered in a quasi-hexagonal lattice [60]. Due to the difference in electronegativity between the fluorine and hydrogen atoms, a large dipole moment

perpendicular to the chain direction occurs. In the initial state, the dipoles are aligned in randomly oriented domains. The planar zig-zag structure and atomic arrangement in the β-phase provides stronger packing density and displays more dipolar alignment resulting in strong piezoelectric properties after poling [61, 62].

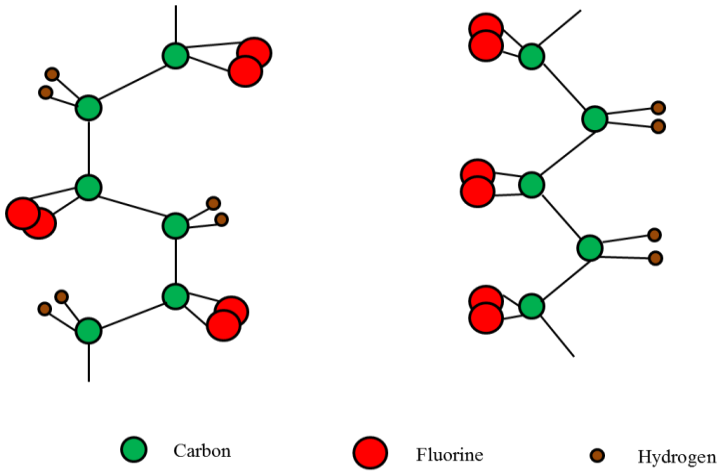



**Figure 2.11:** Structure of PVDF α-phase (LHS) and β-phase (RHS).

Every PVDF chain has a combination of negatively charged fluorine atoms and positively charged hydrogen atoms known as a dipole. The dipoles are strongly bonded to the carbon molecules and the polymer crystal structure controls their orientation. Dipole orientation determines which PVDF structures are piezoelectric. For example, PVDF's β-phase is distinctly polar due to the arrangement of fluorine and hydrogen atoms. The structure shows a net dipole moment due to the well-aligned nature of the dipoles within the carbon backbone and within the crystal itself, resulting in a large spontaneous polarisation [61, 63].

In the virgin β-phase state, the overall net charge is zero as a result of the random dipole arrangement. However, upon application of an external electric field applied across the material, the randomly orientated dipoles align resulting in a net

positive charge in a process known as poling. This process is used to induce piezoelectric and pyroelectric properties within the PVDF film. Figure 2.12 shows the dipole alignment of β-phase PVDF before and after poling.

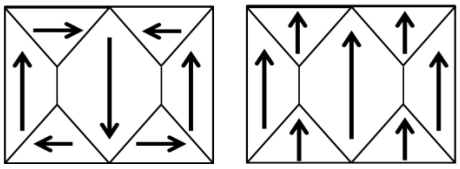


**Figure 2.12:** Alignment of dipoles within β-phase PVDF before (LHS) and after poling (RHS).

To achieve successful poling of PVDF, electric fields ~ 100 V/μm are required often at elevated temperature to convert β-phase PVDF from its non-polar to polar form. Once poled, the β-phase remains stable and polarisation is only removed from the film if heated to a temperature above $T_{CURIE.}$ PVDF displays a relatively high Curie temperature of ~ 195 °C [64] above which, the material loses its polarisation and becomes paraelectric.

In its poled state, PVDF displays remarkable piezoelectric and pyroelectric properties, with a piezoelectric coefficient ($d_{33}$) of ~ –32.5 pC/N [65] and a pyroelectric coefficient ($\rho_3$) ~ 25 C/m$^2$K [66]. The piezoelectric coefficient value quoted for PVDF is significantly lower than the equivalent constant for PZT ($d_{33}$ = 117 pC/N) however PVDF's much lower $\varepsilon_r$ value makes it a far more suitable material for tactile-based devices [67].

## 2.11.2 Polyvinylidene fluoride trifluoroethylene (P(VDF-TrFE))

Polyvinylidene fluoride – trifluoroethylene (P(VDF-TrFE)) is the copolymer formed from PVDF and poly(trifluoroethylene) (PTrFE), examples of homopolymers containing only a single repeating unit in their polymer chains. Similarly to PVDF, P(VDF-TrFE) exhibits four types of crystalline phase, α, β, γ and δ. Among the four phases, the β-phase is the only polar phase exhibiting a large spontaneous polarisation, therefore rendering it the most valuable to investigate the piezoelectric response. Figure 2.13 shows the P(VDF-TrFE) copolymer β-phase crystal structure. One of the main advantages of using P(VDF-TrFE) rather than PVDF is the ability of the copolymer to crystallise directly to the β-phase. PVDF on the other hand often requires an additional mechanical stretching step to change its phase from α to β. If necessary, different processing techniques can be used to alter the crystalline phase of the polymer.

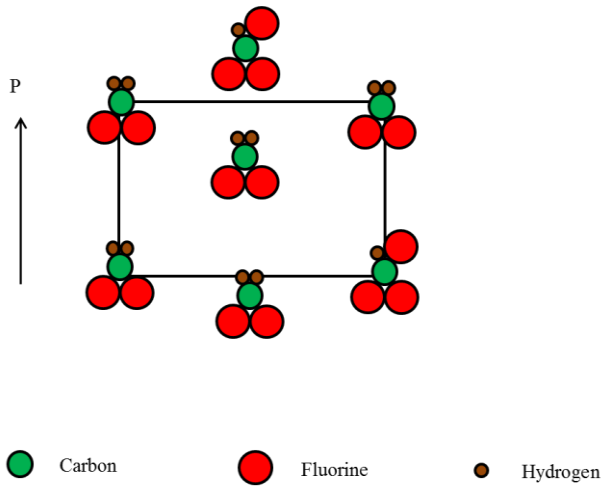



**Figure 2.13:** Schematic of P(VDF-TrFE) β-phase crystal structure.

Similarly to PVDF, P(VDF-TrFE) must be poled using an electric field to induce the piezo/pyro-electric properties within the film. Like PVDF, typical voltages of ~ 100 V/μm applied at elevated temperature would be sufficient to

effectively pole the copolymer material. However, P(VDF-TrFE) displays lower Curie temperature of ~ 110°C [68] compared to ~ 195°C for PVDF.

P(VDF-TrFE) displays a piezoelectric coefficient of –33.5 pC/N [69] which is slightly greater than the equivalent coefficient associated with PVDF (-32.5 pC/N) [65]. The slightly higher piezoelectric coefficient is another advantage of the copolymer material as it provides greater sensitivity for dynamic force sensing.

Figure 2.14 shows typical hysteresis loops for P(VDF-TrFE) produced using three similar poling patterns. The existence of P-E hysteresis leads to a highly non-linear capacitance-voltage dependence (see Figure 2.15), where the capacitance peaks effectively indicate the electric field required to reverse the polarisation, i.e. the coercive voltage.

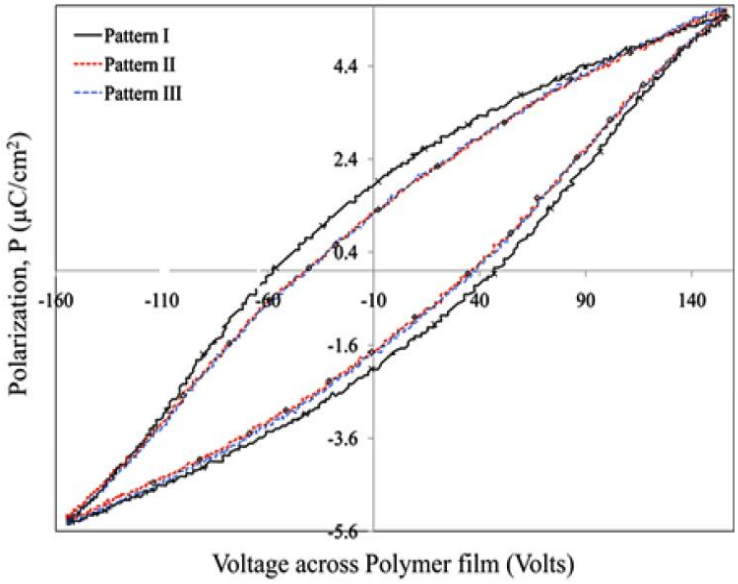



**Figure 2.14:** Typical hysteresis loops for P(VDF-TrFE) [70].

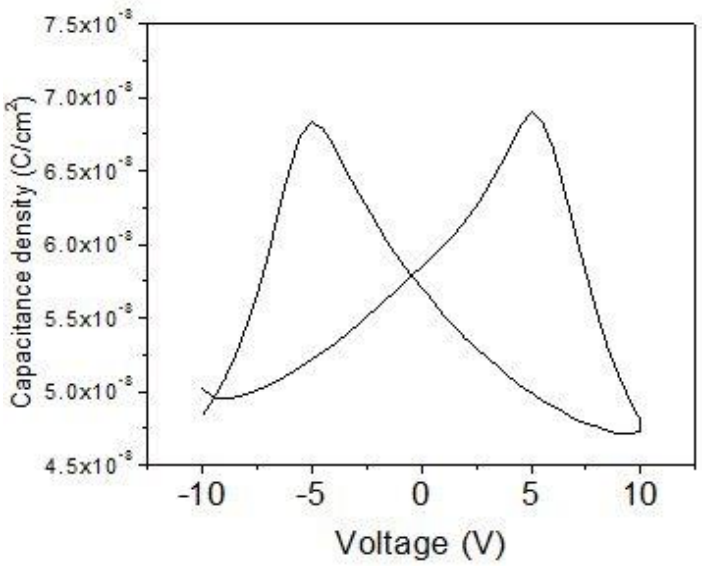



**Figure 2.15:** P(VDF-TrFE) capacitance density as a function of applied voltage [43].

## 2.12 Piezoelectric oxide semiconductor field-effect transistor (POSFET)

So far this chapter introduced the two component parts (OTFT and ferroelectric capacitor) required to create a sensor capable of detecting force or temperature changes through piezoelectricity or pyroelectricity. One method often used to connect a sensor device with a transistor for signal amplification is to use the extended gate approach. Using a contact electrode, a ferroelectric material such as PVDF or its copolymer can be deposited directly onto the metal layer. Through application of force or temperature to the sensor layer and by careful biasing of the transistor, force or temperature changes can be used to control the action of the

transistor. This results in a change in $V_{GS}$ which in turn modulates transistor drain current. Changes in $I_D$ with the stimulus of interest can be evaluated. Formerly, a P(VDF-TrFE)-based pyroelectric sensor has been integrated with a polysilicon thin-film transistor using a multi-foil approach featuring an extended gate to monitor dynamic changes in ambient temperature through the pyroelectric effect [71]. Figure 2.16 shows the approach adopted.

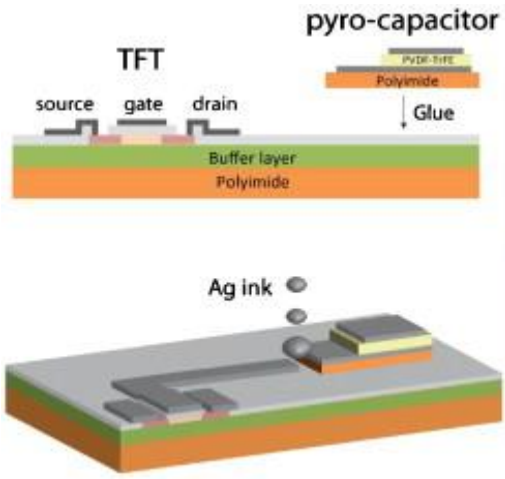



**Figure 2.16:** Scheme of the polyimide platform with the pyroelectric sensor and the polysilicon based readout electronics made using a multi-foil approach. [71].

Previously, a ferroelectric sensor based on polymer P(VDF-TrFE) has been integrated with a CMOS field-effect transistor (FET) to create a device called a piezoelectric oxide semiconductor field-effect transistor (POSFET) [13]. The advantage of the POSFET device over the extended gate approach is the P(VDF-TrFE) layer is directly deposited onto the transistor gate, which in turn modulates transistor $I_D$. By depositing the ferroelectric layer directly onto the metal gate, unwanted cable capacitances can be avoided. The POSFET allows for sensing and processing of pressure signals in-situ at the same site. To date, the POSFET device

has largely been exploited for pressure monitoring. The POSFET relies on the piezoelectric response of P(VDF-TrFE) to modulate transistor drain current, where the charge developed on the transistor gate is proportional to the compressive force applied (Equation 2.17). Figure 2.17 shows the schematic of the POSFET device.

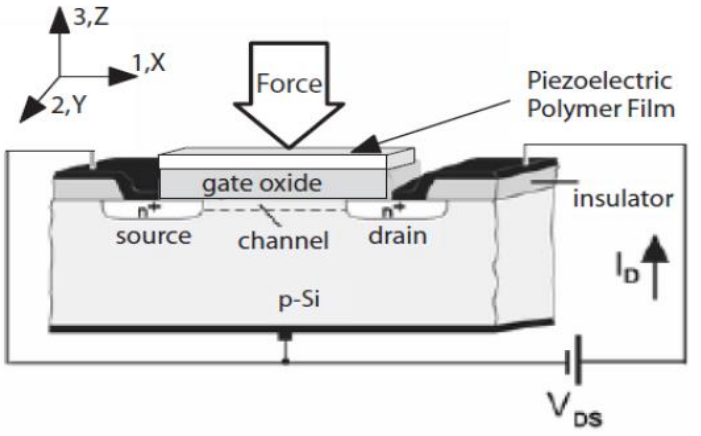



**Figure 2.17:** POSFET touch sensing device [13].

## 2.13 Summary

This chapter presented background information on the organic thin-film transistor (OTFT) and introduced ferroelectric materials including ferroelectric polymers suitable for the development of large-area temperature and force sensors. The focus was on OTFTs because their attributes make them a suitable candidate for future flexible sensors. The aim of this research is to employ low-voltage OTFTs with bi-layer dielectric, consisting of thin aluminium oxide and alkyl phosphonic acid monolayer, and DNTT. Although such bi-layer dielectric has been used previously, further optimisation of the organic monolayer is needed and transistors with DNTT had to be developed. In addition, the OTFT fabrication procedure must

be transferred to plastic foils to take a first step towards future flexible sensors. Furthermore, the marriage of the OTFT with P(VDF-TrFE) provides new opportunities for harvesting the ferroelectric properties of the copolymer and a design of novel force and temperature sensors. The next chapter describes the experimental details of this approach that ultimately led to the development of the P(VDF-TrFE)/OTFT sensor based on the POSFET concept.

# Chapter 3

# Methodology

This chapter introduces the fabrication process used to create the organic thin-film transistor and P(VDF-TrFE) ferroelectric capacitor. Furthermore, it explains the measurements carried out on the devices to evaluate their electrical performance. Section 3.1 describes the fabrication process developed to create OTFT and MIM structures, while section 3.2 introduces the characterisation techniques used to gain an insight into transistor performance. Section 3.3 discusses the measurement protocols used to investigate the performance of metal-insulator-metal (MIM) structures. These latter two sections also explain how various device

parameters were extracted from the measurements. Section 3.4 describes the P(VDF-TrFE) capacitor fabrication protocol. Measurement procedures for the P(VDF-TrFE) capacitor are described in Section 3.5. Finally, Section 3.6 explains the procedure developed to couple the P(VDF-TrFE) capacitor to the OTFT.

## 3.1 Fabrication: OTFT and MIM structures

The OTFT fabrication adopts a previously developed process [72] whereby every single transistor layer, be it a metal or organic material, is deposited by thermal evaporation in vacuum. The only technique performed in ambient environment is the oxidation of aluminium that leads to aluminium oxide formation. This is carried out in an ultraviolet (UV) ozone cleaner enclosed under a Hepa filter to remove any potential contaminants. The ozone system contains a low-pressure quartz mercury lamp that emits UV light at ~ 185 and 254 nm wavelengths, which results in the formation of ozone. Ozone ($O_3$) is a strong oxidiser and the exposure of Al to $O_3$ leads to the formation of aluminium oxide ($AlO_x$) on the surface of Al [73].

The transistor structure is shown in Figure 2.2 (a). All thermal evaporation steps were performed in Mini-Spectros (Kurt J. Lesker) organic thin-film deposition high vacuum system enclosed within a nitrogen-filled glove box (Jacomex) to reduce oxygen and moisture. The base pressure of the Mini-Spectros chamber is ~ $10^{-7}$ mBar and the glovebox ensures $O_2$ and $H_2O$ content is less than 1 particle-per-million (ppm). The system is operated by a computer coupled with a programmable logic controller (PLC) unit, whereby various recipe conditions such as layer

thickness, deposition rate and deposition temperature can be manually adjusted. Metal and organic materials for evaporation in pellet or powder form are loaded into individual crucibles and thermally evaporated. Organic materials were evaporated from 1 $cm^3$-sized crucibles. Each evaporation step makes use of Kapton or steel shadow masks. These are aligned subsequently, and care must be taken throughout the fabrication process to ensure accurate layer-to-layer alignment.

The first step in the OTFT fabrication process is preparation of the chosen substrate. This could be glass, but this discussion focusses on the preparation of PEN plastic film. (Incidentally, the process used to prepare a glass substrate is almost identical.) In order to prepare the PEN substrate, the film is first cut to a size of 7.5 by 7.5 $cm^2$. This is followed by cleaning the plastic by immersing it in sonicated acetone for 25 minutes. Afterwards, the substrate is rinsed in methanol and deionized (DI) water and dried with a nitrogen gun. Some substrates underwent a pre-treatment step involving thermal annealing. The substrate is then loaded into the evaporation chamber pumped down to $1–2x10^{-7}$ mBar.

The first OTFT layer is 30-nm-thick aluminium (Al) (99.999% purity) to create gate lines. This is followed by a 20 nm layer of Al and 20 nm of Au evaporated at one end of each gate line (away from the transistor island) to provide a gate contact during the transistor measurement. This 20 nm of Al followed by 20 nm of Au produces a 40 nm-thick gate contact. During the 40-nm Al/Au evaporation at one end, the rest of the 30 nm-thick Al gate line is shielded to prevent metal deposition. Au is used because it does not oxidise during the oxidation of the Al gate line. Afterwards, the sample is exposed to UV/ozone for 60 minutes to oxidize the Al gate lines (with the exception of the areas covered by Au). This oxidation produces

about 7-nm-thick $AlO_x$ [74]. To increase the oxide thickness, an additional 12 Å of Al is deposited on top of the $AlO_x$ followed by another 60-minute UV/ozone exposure. By increasing the oxide thickness, the dielectric capacitance per unit area is reduced marginally, but the leakage current through the dielectric is suppressed. The total thickness of $AlO_x$ is ~ 9.5 nm. This value has been determined using a spectroscopic ellipsometry technique performed on a number of samples fabricated via an identical process.

$AlO_x$ forms the bottom part of the bi-layer gate dielectric. In the next step the $AlO_x$ is functionalised with a monolayer of phosphonic acid ($C_nPA$), (n = 8, 10, 12, 14, 16 or 18). The $C_nPA$ monolayer is prepared by vacuum evaporation in a two-stage process. Firstly, ~9 monolayers of $C_nPA$ using carefully selected deposition rates and timings are thermally evaporated onto the $AlO_x$ layer. This is followed by a 3-hour anneal at 160°C in vacuum. Annealing removes all physisorbed molecules and improves the structure of the monolayer [72]. This completes the preparation of the $AlO_x/C_nPA$ bi-layer dielectric. In all experiments performed, some gate lines were fully shielded during the $C_nPA$ evaporation to provide a bare-$AlO_x$ dielectric as a reference.

Evaporation of the organic semiconductor layer is the next stage in the fabrication process. A 15 to 20 nm thick dinaphtho[2,3-b:2′,3′-*f*]thieno[3,2-*b*]thiophene (DNTT) layer is deposited at room temperature. DNTT was used as purchased (Sigma Aldrich). The transistors are completed by the thermal evaporation of 50-nm-thick Au (99.99%) source and drain contacts through a shadow mask. Figure 3.1 summarises the OTFT fabrication process flow.

OTFT and metal-insulator-metal (MIM) structures were fabricated side-by-side on a single substrate. The MIM fabrication procedure followed an identical process to the OTFT one, except MIM structures omitted the organic semiconductor layer. The MIM structures were completely masked during the DNTT evaporation.

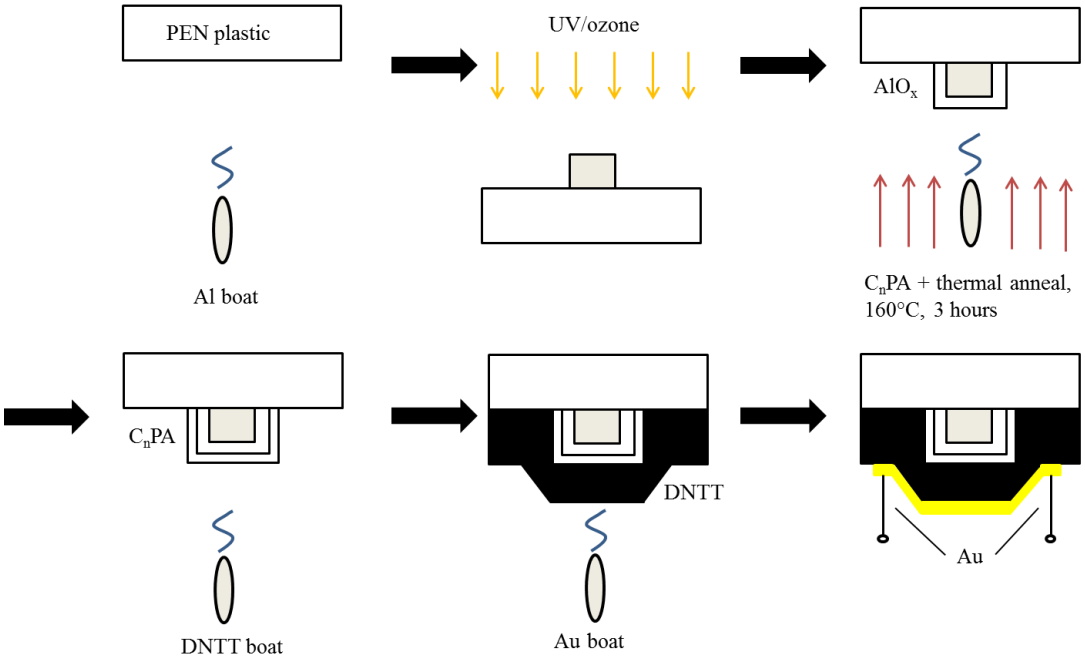



**Figure 3.1:** OTFT fabrication process flow.

## 3.2 Measurement: OTFTs

Measurement of OTFTs was performed using Agilent B1500A semiconductor parameter analyser. A probe station (Signatone) was used to make contact with the samples, and a digital microscope provided high-resolution images of the samples for good probe-to-device contact. The probes are held in place by vacuum and are capable of fine movement adjustment in the x, y and z directions.

Figure 3.2 shows a photograph of the measurement setup, featuring the semiconductor parameter analyser and the attached probe station.

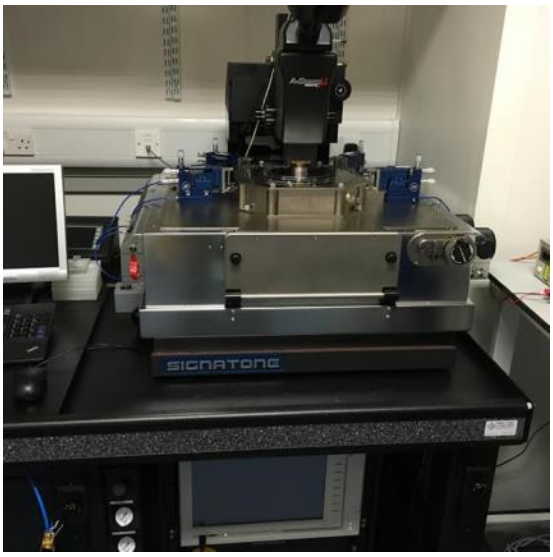



**Figure 3.2:** Device characterisation equipment. Photograph shows Agilent B1500A semiconductor parameter analyser and probe station.

OTFT output and transfer characteristics were measured in a sweep mode and the details are explained in Sections 3.2.1 and 3.2.2. Section 3.2.3 explains the bias stress procedure that allows evaluation of long-term transistor stability. Finally, the OTFT degradation caused by ambient conditions is discussed in Section 3.2.4.

### 3.2.1 Output characteristics

The OTFT output characteristic plots the drain current ($I_D$) against drain-to-source ($V_{DS}$) voltage for fixed gate-to-source ($V_{GS}$) voltages. Each output characteristic depicts the transistor in both the linear and saturation regimes. Figure 3.3 shows an example of output characteristics.

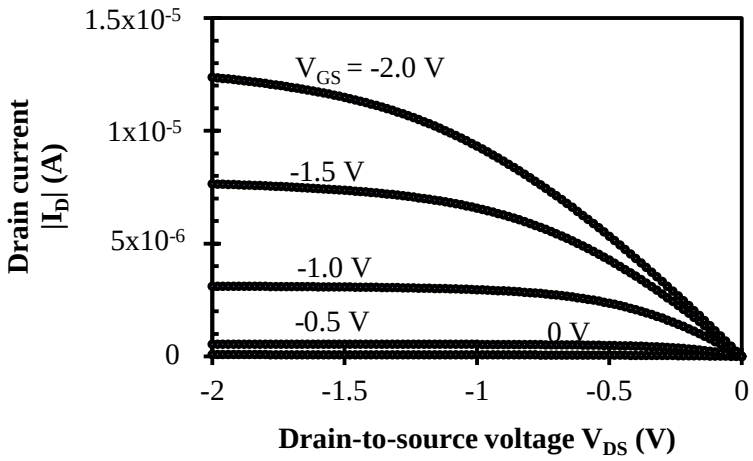



**Figure 3.3:** OTFT output characteristics for $V_{DS}$ of (-) 0, 0.5, 1, 1.5 and 2 V.

## 3.2.2 Transfer characteristics

The transfer characteristics measure the transistor drain current ($I_D$) as a function of the gate-to-source voltage ($V_{GS}$), for a set of drain-to-source voltages ($V_{DS}$). $V_{DS}$ was fixed at –0.1 V and –2 V to capture the transistor behaviour in the linear and saturation regimes respectively. An example of measured OTFT transfer characteristics is shown in Figure 3.4, where $V_{GS}$ is swept from 0.5 to –2 V. On a number of occasions, $V_{GS}$ was initially swept from 0.5 to –2 V and then back again from -2 V to 0.5 V to investigate hysteresis.

Field-effect mobility in the linear regime, ($|V_{DS}|<|V_{GS}-V_t|$), can be obtained by rearranging Equation 2.12 [15]. Equation 3.1 gives the expression for mobility in the linear regime.

$$\mu_{lin} = \left(\frac{\partial I_D}{\partial V_{GS}}\right) . \frac{1}{C\frac{W}{L}V_{DS}} \tag{3.1}$$

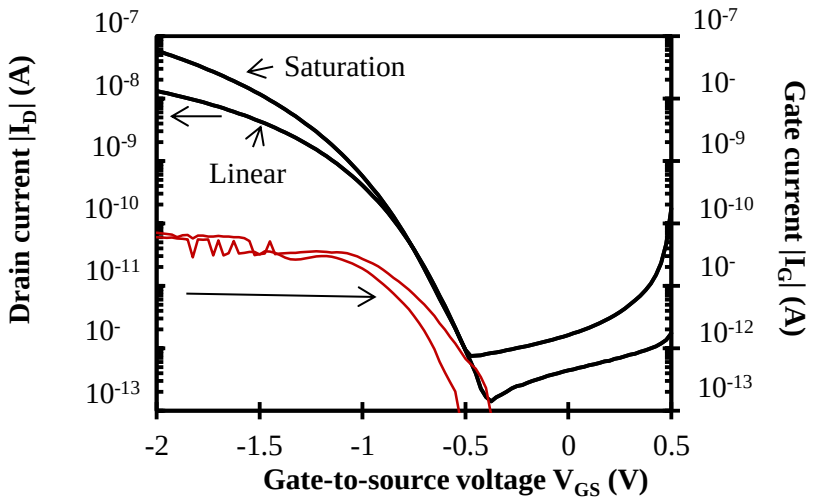



**Figure 3.4:** OTFT transfer characteristics for linear ($V_{DS}$ = –0.1V) and saturation ($V_{DS}$ = –2 V) regimes.

In the saturation regime ($|V_{DS}| > |V_{GS} - V_t|$), the expression for field-effect mobility is found by rearranging Equation 2.14 as follows [15]:

$$\mu_{sat} = \left(\frac{\partial\sqrt{I_D}}{\partial V_{GS}}\right)^2 \cdot \frac{1}{C\left(\frac{W}{2L}\right)} \tag{3.2}$$

where $C$ is dielectric capacitance per unit area in F/cm$^2$, $W$ is transistor channel width and $L$ is transistor channel length. Field-effect mobility ($\mu$) has units of cm$^2$/Vs.

Various OTFT parameters can be extracted from the transfer characteristics. For $V_{DS}$ = –0.1 V the threshold voltage and field-effect mobility in the linear region can be extracted. Furthermore, from the saturation regime ($V_{DS}$ = –2 V), in addition to the threshold voltage ($V_t$) and field-effect mobility ($\mu$), the subthreshold slope ($S$), ON ($I_{ON}$) and OFF ($I_{OFF}$) currents, ON/OFF current ratio ($I_{ON}/I_{OFF}$), and gate leakage current ($I_G$) can be extracted. This chapter will describe how to extract such parameters and explain their significance.

### 3.2.2.1 Threshold voltage and field-effect mobility

The two most important OTFT parameters are the threshold voltage ($V_t$) and the field-effect mobility (μ). In the linear regime the mobility is extracted from the plot of $I_D$ against $V_{GS}$ using Equation 3.1. Conversely, in the saturation regime, the mobility is extracted from the plot of $\sqrt{I_D}$ against $V_{GS}$ using Equation 3.2. Figures 3.5 and 3.6 depict the procedure.

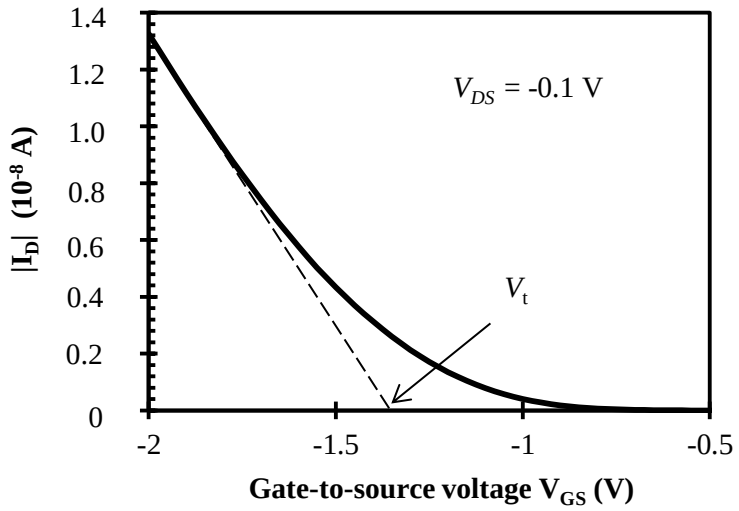



**Figure 3.5:** Extraction of the slope and threshold voltage for linear regime ($V_{DS}$ = –0.1 V).

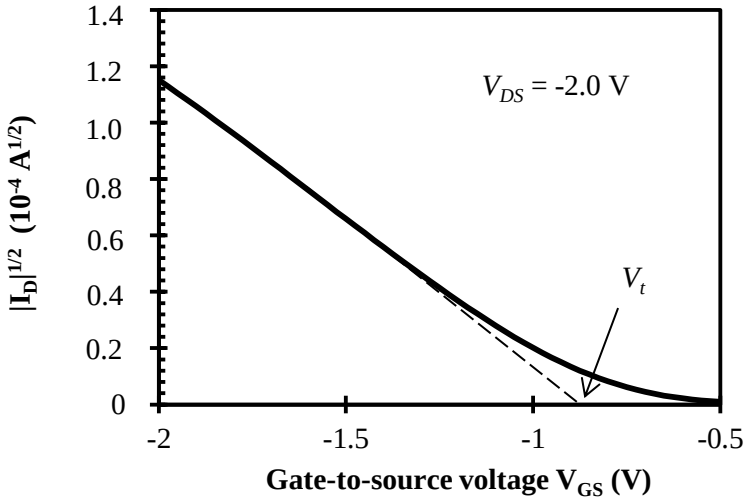



**Figure 3.6:** Extraction of the slope and threshold voltage for saturation regime ($V_{DS}$ = –2.0 V).

After finding the steepest slope on the curve, the intercept of the slope on the x-axis is the threshold voltage, $V_t$.

### 3.2.2.2 Subthreshold slope

The subthreshold slope is found in the subthreshold region on the transfer characteristics curve, and it is the region where the drain-current increases exponentially as a function of the gate-to-source voltage. It is extracted by plotting the logarithm of $I_D$ against $V_{GS}$ in the saturation regime (Figure 3.7), and taking the inverse of the steepest slope. Equation 3.3 describes the subthreshold regime. $S$ typically has units of mV/decade.

$$S = \left[\frac{\partial}{\partial V_{GS}}(\log_{10}|I_D|\right]^{-1} \tag{3.3}$$

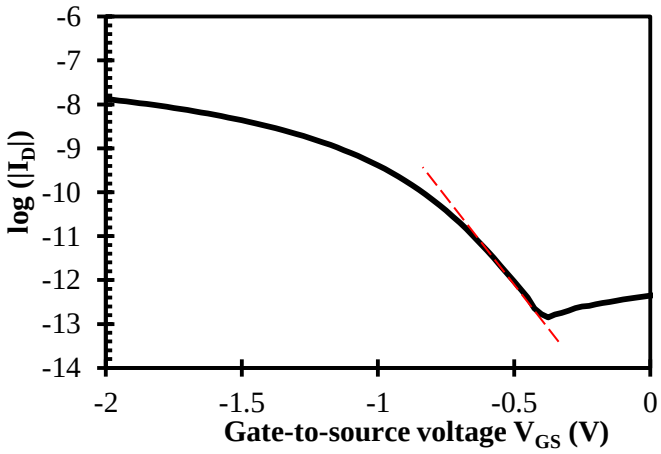



**Figure 3.7:** Extraction of subthreshold slope from the saturation regime transfer characteristic.

### 3.2.2.3 ON and OFF currents

For the saturation region only ($V_{DS}$ = –2 V), the ON and OFF currents are defined as simply the maximum and minimum values of $I_D$ respectively. Normally, the ON and OFF currents are quoted for transistors with similar channel dimensions to provide an accurate comparison. The ON/OFF-current ratio is the ratio taken by dividing the values of $I_{ON}$ and $I_{OFF}$ and is often quoted as a useful figure of merit when analysing OTFT performance, particularly when used in logic circuitry where a high ON/OFF-current ratio is crucial.

### 3.2.2.4 Leakage current

The transistor gate current is often referred to as the leakage current. This thesis quotes the value of gate current ($I_G$) at the maximum gate and drain voltages (e.g. $V_{GS} = V_{DS}$ = –2 V).

## 3.2.3 Bias stress

An established procedure that allows investigation of the long-term electrical stability of the organic thin-film transistor is the bias stress measurement. Bias stress presented in this thesis involves biasing the transistor gate at $V_{GS} = V_{STRESS}$ = –2 V for an extended period of time whilst grounding the source and drain electrodes. Applying bias to the gate electrode introduces charge carriers in the transistor

channel that can be trapped into the existing localised electronic states. Prolonged application of the gate bias leads to changes in transistor performance. The primary effect of the bias stress is an increase in the threshold voltage and the associated decrease in the ON current. However, field-effect mobility and subthreshold slope can also be affected.

The bias stress process is paused at regular time intervals and the OTFT transfer characteristic in the saturation regime ($V_{DS}$ = –2 V) is measured. Each transfer characteristic allows extraction of all OTFT parameters using the procedures described above. Consequently, changes in transistor parameters can be monitored as functions of bias stress time. Changes in OTFT parameters with increasing bias stress time can be fitted with stretched-exponential functions. Equation 3.4 gives an example function for fitting changes in transistor threshold voltage as a function of the bias stress time.

$$\Delta V_t = |V_t(t) - V_t(0)| = |V_t(\infty) - V_t(0)|.\left[1 - e^{-\left(\frac{t}{\tau_{V_t}}\right)^{\beta vt}}\right] \quad (3.4)$$

Here, $\Delta V_t$ is the threshold voltage shift, $V_t$ (t) is the threshold voltage after $t$ seconds of bias stress, $V_t$ (0) is the initial threshold voltage before the application of bias, $V_t$ ($\infty$) is the equilibrium threshold voltage after prolonged application of bias, $\tau_{Vt}$ is a time constant and $\beta_{Vt}$ is the stretching parameter, where ($0 < \beta_{Vt} \leq 1$).

### 3.2.4 Environmental ageing

In addition to investigating the transistor's transfer characteristics and bias stress performance, it can be useful to look at how well the transistor retains its performance with time. OTFT behaviour after residing under varied environmental conditions can be assessed and compared to the as-fabricated devices.

The most widely used organic semiconductor in recent years for use in OTFTs has been pentacene [75-77]. Pentacene can provide OTFTs with field-effect mobility of ~ 0.7 $cm^2$/Vs [77]. However, pentacene is known to degrade in ambient atmosphere, due to the oxidation of its central benzene ring [78]. Transistors with DNTT on the other hand show remarkable ambient stability [79].

## 3.3 Measurement: MIM structures

Measurement of metal-insulator-metal (MIM) structures was carried out using the Agilent B1500A semiconductor parameter analyser. Capacitance as a function of frequency (C-f) and current voltage dependence (I-V) were measured on all MIM structures to assess the dielectric layers. Furthermore, the capacitance data was used to estimate the thickness of the phosphonic acid monolayer.

### 3.3.1 Capacitance

MIM capacitance was measured as a function of a.c. frequency between 1 kHz and 1 MHz by applying a sinusoidal voltage of 100 mV peak-to-peak and a DC bias of –1 V to the Au electrode. Figure 3.8 shows an example of such a

measurement. The frequency range investigated provided a relatively flat capacitance value that started to drop-off for frequencies higher than 300 kHz.

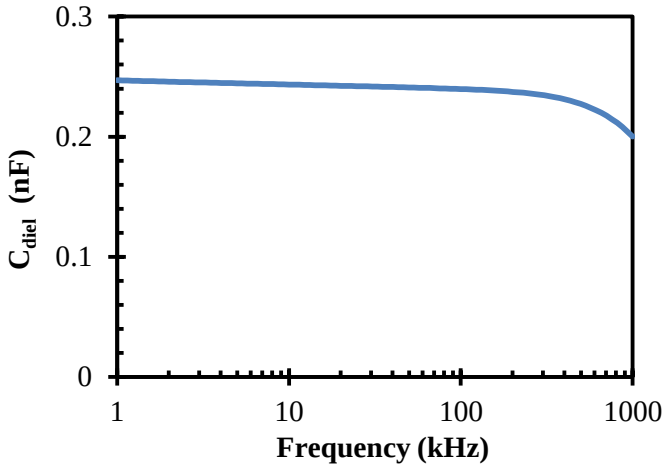



**Figure 3.8:** MIM capacitance as a function of a.c. frequency.

### 3.3.1.1 Dielectric capacitance per unit area

Figure 3.8 displays the capacitance of a typical MIM device. The capacitance per unit area is found by extracting the dielectric capacitance of the MIM structure at a chosen frequency (2 kHz) and dividing it by the contact area. Mean capacitance values and standard deviations are calculated for various MIM structures.

Each transistor sample contains the corresponding MIM structures with bare-$AlO_x$ and $AlO_x/C_nPA$ dielectrics. By obtaining capacitance data for each, the capacitance of the phosphonic acid layer can be established as follows. If the capacitance of the bi-layer is labelled $C_{diel}$, and the bare-$AlO_x$ layer capacitance

$C_{AlOx}$; then $C_{CnPA}$ can be found by rearranging the expression for capacitors in series: $1/C_{diel} = 1/C_{AlOx} + 1/C_{CnPA}$.

### 3.3.1.2 Thickness of alkyl phosphonic acid monolayer

The MIM and OTFT dielectric bi-layer is composed of $AlO_x$ and $C_nPA$ layers that have different thicknesses. The thickness of $C_nPA$ ($d_{CnPA}$) can be found from Equation 3.5 by applying a value of 2.1 [80] for the relative permittivity of $C_nPA$ regardless of alkyl chain length ($\varepsilon_r$). $\varepsilon_o$ is the permittivity of free space and has a value of 8.85 x $10^{-12}$ F/m.

$$d_{CnPA} = \varepsilon_0 \varepsilon_r / C_{CnPA} \tag{3.5}$$

## 3.3.2 Leakage current density

To evaluate the leakage current of the dielectric layer, current-voltage (I-V) measurements are performed on the MIM structures. The chosen voltage range is –3 V to +3 V even though the maximum voltage used in OTFT operation is –2 V. The voltage is swept as indicated in Figure 3.9. To obtain the leakage current density, the measured current is divided by the MIM area. Figure 3.9 shows a typical current-voltage measurement for $AlO_x/C_8PA$ bilayer.

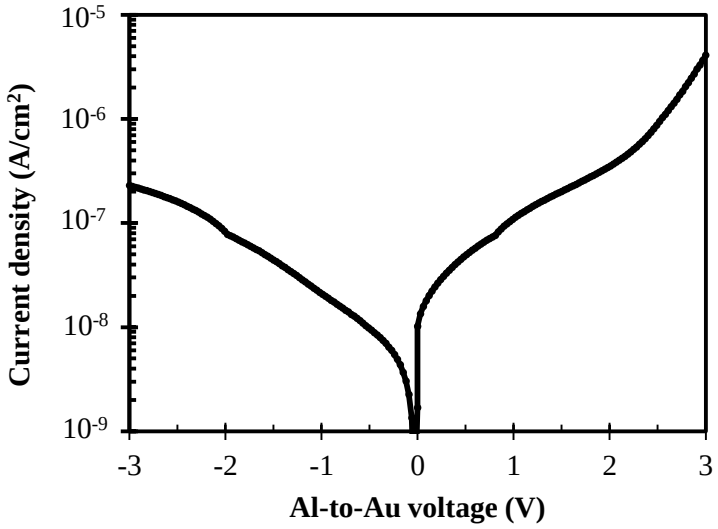



**Figure 3.9:** MIM current density as a function of Al-to-Au voltage.

## 3.4 Fabrication: P(VDF-TrFE) capacitors

Fabrication of P(VDF-TrFE) capacitors involves different fabrication steps that are outlined in this section. The fabrication procedure is outlined in [81].

### 3.4.1 P(VDF-TrFE) deposition

The P(VDF-TrFE) capacitor has the structure of a parallel plate capacitor; where the copolymer layer of P(VDF-TrFE) is sandwiched between two metal electrodes. The metal contacts chosen in this instance are Al and Au for the bottom and top contacts respectively. Both metals are thermally evaporated. The completed capacitor has an active sensing area of 25 $mm^2$, with a P(VDF-TrFE)-layer thickness

of ~ 2.5 µm determined using a Dektak stylus profiler. The capacitors are fabricated on a rigid silicon substrate to be compatible with cleanroom fabrication procedures. The silicon wafer plays no role in the device performance, and future work will exchange the silicon wafer for a PEN foil substrate to achieve the mechanical flexibility required for a useful tactile sensor.

Ferroelectric copolymer P(VDF-TrFE) was deposited by spin-coating. A 10 wt.% solution of P(VDF-TrFE) (70:30) copolymer was used. The solution was prepared by mixing P(VDF-TrFE) in pellet form (Piezotech, France) in RER500 solvent (Fujifilm, Japan) and mixing for 4 hours at 80 °C on a hotplate with magnetic stirrer. The spin-coating was performed on the aluminium bottom contact in three steps. In the first two spin steps, both the spin rate and spin time were low (500 rpm for 2 seconds followed by 600 rpm for 8 seconds) to allow uniform spreading of the solution. The final spinning step was performed at 3000 rpm for 30 seconds. This procedure led to P(VDF-TrFE) thickness of ~ 2.5 µm. Film thickness is predominantly dictated by the spin speed in addition to the molar concentration of P(VDF-TrFE) solution.

### 3.4.2 P(VDF-TrFE) annealing process

The P(VDF-TrFE) layer deposited by spin coating was thermally annealed at 120 °C (temperature above $T_{CURIE}$ ~ 110°C) for three hours to remove any excess solvent from the film and to induce crystallisation of the polymer material. The anneal temperature of 120°C was chosen to lie between the Curie (110°C) and melting temperatures (150°C) of P(VDF-TrFE) [68]. Annealing within this

temperature range greatly improves the opportunity for the film to crystallise in the favourable β-phase thereby enhancing the piezoelectric properties of the P(VDF-TrFE) film [68]. The thermal energy provided via the annealing process enables the P(VDF-TrFE) polymer chains to reorient themselves and form a more favourable crystalline structure upon cooling. After annealing, the Au top contact of the sensor is thermally evaporated to complete the capacitor structure.

### 3.4.3 P(VDF-TrFE) poling procedure

To induce the preferential orientation of the permanent dipoles and the piezoelectric effect, the process of poling is required. Poling is performed by applying a high DC electric field across the material in a specific direction. In order to reduce the electric field required, poling can be carried out at elevated temperature [82]. However, this so called thermal poling requires a temperature lower than Curie temperature, to maintain the piezoelectric properties of P(VDF-TrFE). A temperature of 80°C was chosen for this purpose. At 80°C, an electric field strength of ~ 80 V/μm is adequate to polarise the P(VDF-TrFE) capacitor. Therefore, a maximum voltage of 240 V was chosen for the 2.5 μm-film. To avoid sparking during the poling procedure, the voltage was applied to the sensor in 40 V increments and held for 10 minutes at each stage. Prior to each subsequent voltage application, the device's contacts were shorted for 5 minutes.

The final part of the procedure relates to the contacts chosen for the piezoelectric material's top and bottom electrodes. It can be advantageous to choose a chemically inert metal such as gold (Au) for the top contact since it is less likely to

react with the piezoelectric polymer. On the other hand, metals such as gold can quite easily diffuse into polymer films, which can result in increased leakage current when very thin films of piezoelectric polymer are used in devices and as such a trade-off exists between choice of contact material and polymer layer thickness. Figure 3.10 shows the completed P(VDF-TrFE) capacitor.

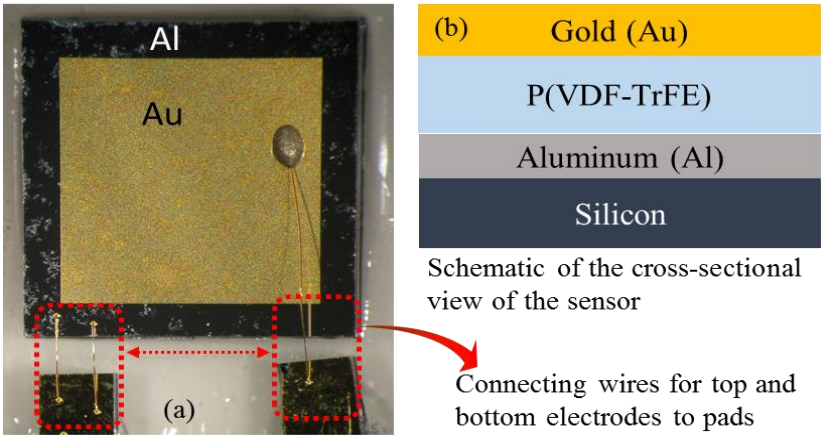



**Figure 3.10:** Fabricated P(VDF-TrFE) capacitor withAl and Au electrodes (a) Capacitor cross-sectional view (b).

## 3.5 Measurement: P(VDF-TrFE) capacitors

### 3.5.1 Current-voltage (I-V)

Leakage current through the capacitor was measured by performing current-voltage (I-V) measurements between 0 to 1 V, and quoting the current value at a voltage of 1 V. Voltage was applied to the top (Au) electrode whilst grounding the Al bottom electrode. Figure 3.11 shows the I-V measurement.

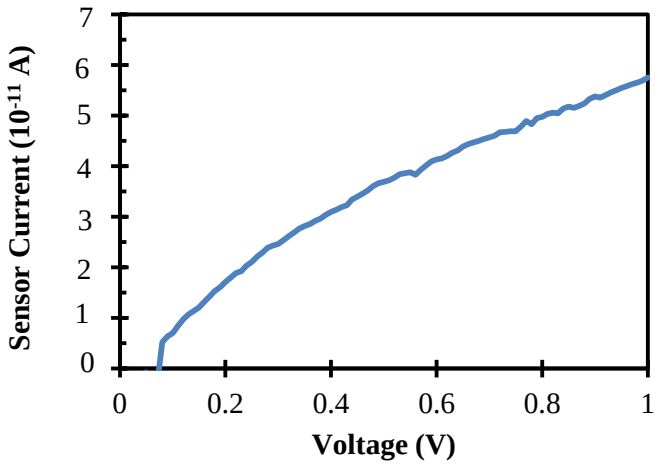



**Figure 3.11:** I-V measurement of P(VDF-TrFE) capacitor.

## 3.5.2 Capacitance-voltage (C-V)

Capacitance-voltage (C-V) measurements were performed between –5 and +5 V at a frequency of 2 kHz in a sweep mode to investigate hysteresis. Figure 3.12 shows a C-V measurement on a fresh P(VDF-TrFE) capacitor.

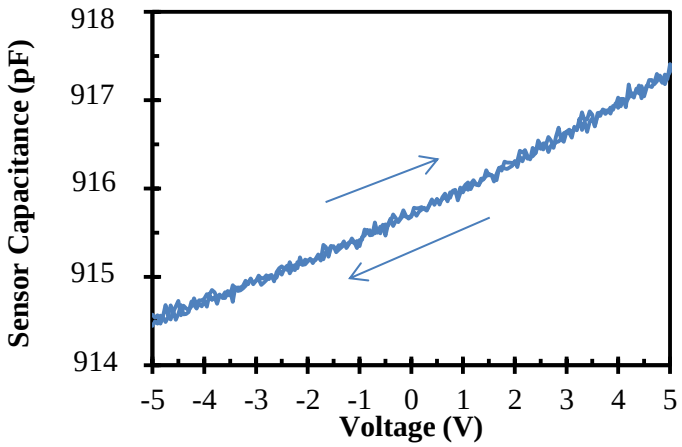



**Figure 3.12:** C-V measurement at 2 kHz of P(VDF-TrFE) capacitor.

### 3.5.3 Static capacitive response

A normal compressive force ranging from a few tenths of Newton to 9 N was applied to the P(VDF-TrFE) capacitor at room temperature using a precision linear stage controlled with a stepper motor (Zaber Technologies). Figure 3.13 shows the capacitor mounted on a glass slide in the linear stage. Force was applied in the direction normal to the surface using a custom-designed Teflon probe. The probe was designed to provide a contact area of 2 mm x 6 mm and was able to compress 40 % of the capacitor's active area.

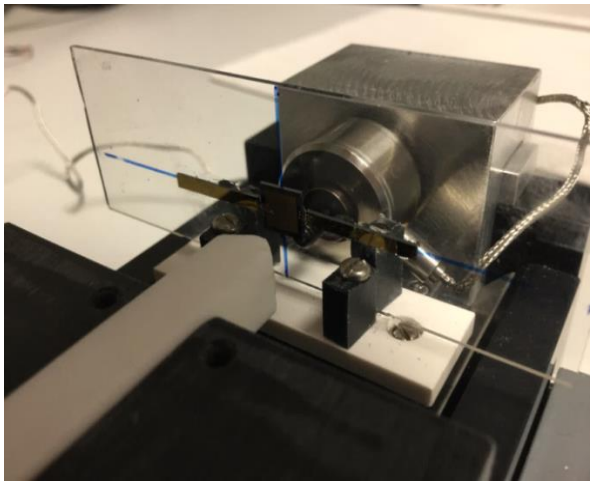


**Figure 3.13** P(VDF-TrFE) capacitor mounted on glass slide for force measurements. Photograph shows linear stage, Teflon probe and load cell setup.

P(VDF-TrFE) capacitance at 2 kHz was measured for a range of compressive forces from 0 N to ~ 9 N, with the exact force application being recorded in real-time by a load cell (Omega). Capacitance was extracted after the force had stabilised.

The response of the P(VDF-TrFE) capacitor to static temperature was assessed by subjecting the sensor to various temperatures for 5 minutes and measuring the capacitance. A Peltier element controlled by a PID (KamVIEW) was used to vary the temperature of the ferroelectric between 15 to 47 °C. Every 2°C, the capacitance was extracted. No force was applied to the P(VDF-TrFE) capacitor during the temperature investigation.

Figure 3.14 shows the P(VDF-TrFE) capacitor mounted on a glass slide on a Peltier element. A thermally conductive paste was used to secure the glass slide to the Peltier surface, and allowed for even distribution of heat.

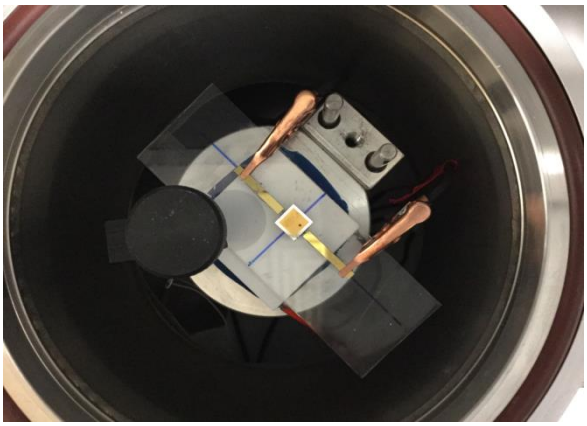


**Figure 3.14** P(VDF-TrFE) capacitor mounted on glass slide for temperature measurements. Photograph shows Peltier element housed within a vacuum chamber.

### 3.5.4 Dynamic piezoelectric and pyroelectric responses

Once poled, the P(VDF-TrFE) capacitor is capable of responding to dynamic pressure and temperature as a result of its inherent piezoelectric and pyroelectric

properties. These events can be monitored in real time using an oscilloscope, where the additional charge generated as a result of the force/temperature change is translated as a voltage at the output. However, the induced piezo/pyroelectric charge decays quickly, and therefore, a charge amplifier must be employed. A charge amplifier built by another PhD student was used in a few instances.

Once connected to an OTFT, the ferroelectric's piezo/pyro-electric response can be measured in terms of a change in transistor output voltage that is monitored with an oscilloscope. One disadvantage of using ferroelectric materials for dynamic force/temperature monitoring is the difficulty to separate the piezoelectric response from the pyroelectric one.

## 3.6 P(VDF-TrFE)/OTFT sensor

The process of coupling the P(VDF-TrFE) capacitor to the organic thin-film transistor to produce the sensor initially adopted a relatively simple approach. In the first instance, the P(VDF-TrFE) capacitor and OTFT were fabricated on separate clean silicon and glass substrates respectively. Furthermore, the completed capacitor was mounted on a glass slide for ease of use and compatibility with the force testing equipment. The glass slide played no role in device operation. After fabricating the two devices, a short piece of gold wire (~ cm's) was used along with highly conductive silver paste (Agar Scientific) to connect one of the sensor electrodes (Al or Au) to the gate of the organic transistor. The length of gold wire was kept to a minimum to reduce its resistance. In this fashion, the force and temperature could be

applied to the P(VDF-TrFE) capacitor only without affecting the transistor. Figure 3.15 shows the schematic of the capacitor's Au electrode connected to the OTFT gate via gold wire.

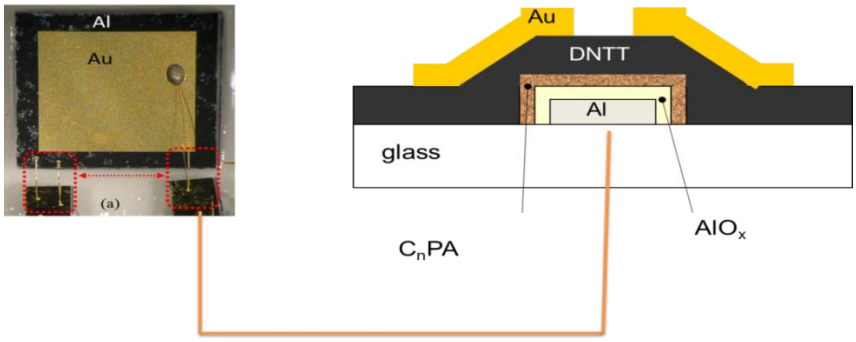



**Figure 3.15** P(VDF-TrFE) capacitor and OTFT connected via gold wire. Circuit shows the sensor Au contact connected to OTFT gate.

# Chapter 4

# Effect of alkyl phosphonic acid length on OTFT performance

This chapter focusses on the organic part ($C_nPA$) of the OTFT's dielectric bi-layer and compares phosphonic acids with different aliphatic tail length with the aim to optimise OTFT performance and improve its long term electrical stability.

The outline of the chapter is as follows. The aim of the work is introduced in Section 4.1, with the experimental procedures described in Section 4.2. Section 4.3 provides results from various measurements performed on different samples for

material and electrical characterisation, as well as organic thin-film transistor parameters for assessing electrical performance and stability. Finally, the chapter is discussed and summarised in Sections 4.4 and 4.5 respectively.

## 4.1 Introduction

To achieve continuous improvement in OTFT properties for applications including wearable or disposable electronics, or sensor systems, low power consumption and low-voltage operation are key device requirements. Low-voltage/power characteristics are particularly crucial for applications requiring batteries or when energy-harvesting devices are used.

A common method adopted to realise low-voltage transistor operation is to increase gate dielectric layer capacitance through choice of thin dielectric layers and/or materials featuring high relative permittivity (high-k dielectrics). The approach demonstrated here integrates a medium-k oxide (aluminium oxide) with a monolayer of alkyl phosphonic acid, which suppresses leakage current through the dielectric layer whist still providing a reasonably high capacitance required for low-voltage operation. The overall OTFT dielectric thickness is ~ 10 nm, with operating voltages as low as –1.5 V.

The performance of low-voltage organic transistors is highly dependent on the individual device layers, and since DNTT is deposited directly onto a very thin monolayer of phosphonic acid in the bottom-gate top-contact transistor architecture, optimisation of the self-assembled monolayer is important to create high-

performance OTFTs. This chapter presents various $AlO_x/C_nPA$ dielectrics incorporated into OTFTs to assess the role that alkyl chain length has on OTFT behaviour. This research was prompted by previous work that studied solution-assembled $C_nPA$ and found better transistor performance when longer-chain phosphonic acid molecules were used. The alkyl phosphonic acids were thermally evaporated in vacuum and incorporated into DNTT-based organic transistors. Metal-insulator-metal and OTFT structures were fully characterised, including transistor bias stress stability. Correlation between phosphonic acid carbon chain length and OTFT performance was sought.

## 4.2 Experimental details

All samples for material characterisation and devices were prepared on Eagle 2000 glass substrates. Six alkyl phosphonic acids featuring different aliphatic tail length ($C_8PA$, $C_{10}PA$, $C_{12}PA$, $C_{14}PA$, $C_{16}PA$ and $C_{18}PA$) were purchased with 97 % purity (Strem Chemicals, USA) and purified in-house by recrystallization from hot hexane or heptane solutions using decolourising charcoal to evaporate any excess solvent.

$AlO_x$ and $AlO_x/C_nPA$ samples for surface and structural characterisation were fabricated by evaporating 30-nm thick aluminium lines at a rate of ~ 2.5 Å/s. Next, ~ 10-nm-thick $AlO_x$ was produced by exposure of aluminium to UV/ozone. Each $C_nPA$ layer was formed under high vacuum conditions. Based on previously optimised n-octyl phosphonic acid ($C_8PA$) [75, 83, 84], each $C_nPA$ deposition rate was adjusted

accordingly to achieve around a "monolayer thickness" in ~ 5.5 seconds, while the as-deposited layer thickness was equal to around 9 monolayers prior to thermal desorption. In all six instances, the substrate was kept at room temperature during $C_nPA$ deposition. For surface characterisation purposes, Fourier-transform infrared spectroscopy (FTIR), atomic force microscopy (AFM) and contact angle goniometry (CAG) measurements were performed on these samples. In addition, two bare-$AlO_x$ samples (as prepared and annealed for 3 hours at ~ 160°C) were prepared for reference.

FTIR spectra were measured using Ge detector in reflection mode with Nicolet 380 spectrometer (Thermo Scientific, USA) in ambient air. The beam diameter was ~ 1.5 mm. PeakFit analysis provided the location of the peaks, their intensity, full width at half maximum (FWHM), and integral area.

Atomic force microscopy images were recorded by scanning 1 x 1 $\mu m^2$ areas of the surface in ambient air using a MultiMode 8 scanning probe microscope (Digital Instruments, USA; Bruker Nanoscope analysis software version 1.40) under the new PeakForce QNM mode. AFM measurements were obtained using ScanAsyst-air probes. AFM images were taken from random spots in at least two areas. The PeakForce QNM mode allows for direct extraction of the nanomechanical properties of the samples without inflicting damage. Upon contact of the AFM tip, the captured force curve is used to calculate DMT modulus, deformation, energy dissipation and force of adhesion.

To investigate liquid-surface interactions with maximum resolution, contact angles (at 22°C) of small drops (4 on each substrate) of diiodomethane (DIM, > 99

%, surface tension $\gamma_l$ = 48.7 mN/m at 18.8°C, ~ 1 μL), 1,2-ethanediol (ethylene glycol, EG, > 99 %, $\gamma_l$ = 47.7 mN/m at 18.8°C, ~ 1 μL), and water (filtered water, FW, $\gamma_l$ = 73.4 mN/m at 18.8°C ~ 2 μL) placed on horizontal surfaces were measured using a goniometer (Kruss DSA30, Germany). The contact angle of a liquid with a solid surface is a result of the interaction between the liquid and solid. Surface energies ($\gamma_s$) of the probed solid surfaces were calculated from the contact angles and the interfacial energies ($\gamma_l$) of the three probe liquids. The total surface energy is the sum of the Lifshitz-van der Waals (also called dispersion or nonpolar) and acid-base (also called polar) contributions. The polar portion can be further subdivided into Lewis acid and Lewis base components.

Six samples were fabricated containing both MIM and OTFT structures which followed identical fabrication procedures up to and including the monolayer of phosphonic acid. Some bare-$AlO_x$ reference samples were also produced. 20-nm-thick DNTT was deposited on OTFT structures at a rate of 0.5 Å/s at room temperature. After DNTT deposition, all devices were completed by evaporating 50-nm-thick Au at a rate of ~ 3 Å/s.

## 4.3 Results

### 4.3.1 Gate Dielectric: Electrical and structural measurements

Capacitance of $AlO_x/C_nPA$ bi-layers along with corresponding phosphonic acid layer thickness is given in Figure 4.1 (a). Additionally, bare-$AlO_x$ capacitance

is also shown which has a mean value of 0.60 µF/cm$^2$. In all cases, $AlO_x/C_nPA$ capacitance is lower than this value, and a general trend of a decrease in capacitance per unit area is seen as the length of aliphatic tail increases. As the length of $C_nPA$ molecules (*n*) rises from 8 to 18, an increase in phosphonic acid thickness is observed, measuring 0.83 nm for $C_8PA$ and 2.49 nm for $C_{18}PA$. The thicknesses were determined by using Equation 3.5 and applying a value of 2.1 [80] for the relative permittivity of $C_nPA$. This value was used for all 6 phosphonic acids.

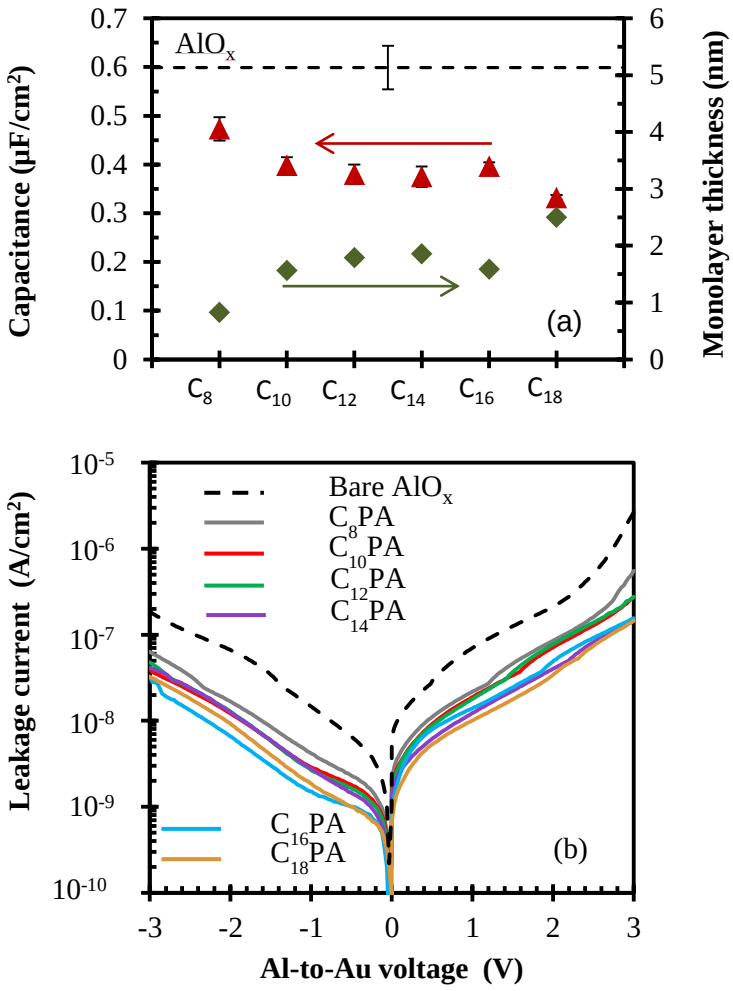



**Figure 4.1** $AlO_x/C_nPA$ capacitance and the extracted $C_nPA$ thickness versus the $C_nPA$ length (a). Current density of $AlO_x/C_nPA$ bi-layers as a function of $C_nPA$ (b). Bare $AlO_x$ is included for comparison.

Figure 4.1 (b) shows $AlO_x$ and $AlO_x/C_nPA$ leakage current densities for each phosphonic acid. The bare-$AlO_x$ dielectric displays a leakage current density at –3 V of ~ $2x10^{-7}$ A/cm$^2$. For the same –3 V, when the $AlO_x$ layer has been functionalised with phosphonic acid, all cases show a reduction in leakage current density with values ranging between ~ $6x10^{-8}$ and ~$3x10^{-8}$ A/cm$^2$. As $C_nPA$ length increases, leakage current density reduces. To summarise, both capacitance and the leakage current measurements confirm that the thickness of $C_nPA$ increases with increasing *n*, while the capacitance measurement proves that in all cases $C_nPA$ thickness corresponds to about a monolayer.

The water contact angles of $AlO_x/C_nPA$ samples as a function of alkyl chain length are displayed in Table 4.1. After the desorption/anneal process, all $AlO_x/C_nPA$ surfaces display hydrophobicity featuring water contact angles greater than 110° regardless of the alkyl chain length. Despite a maximum value of 112.0 ± 1.1° and a minimum value of 110.8 ± 1.3° being obtained for $C_{12}PA$ and $C_{14}PA$ respectively, all contact angles are the same within the error of measurement. For comparison, these contact angles were compared to a non-desorbed $C_{18}PA$ layer of thickness ~ 20 nm (confirmed by atomic force microscopy). The non-desorbed $C_{18}PA$ layer displayed significantly different contact angles for all three probe liquids used.

Every desorbed/annealed $AlO_x/C_nPA$ layer investigated features a low surface energy of ~ 17.5 mJ/m$^2$, with dominating Lifshitz-van der Waals (dispersive) component. There appears to be no correlation between the length of aliphatic chain and the surface properties. The small Lewis acid component and negligible Lewis

**Table 4.1** Advancing contact angles of the probe liquids (filtered water − FW, ethylene glycol − EG and diiodomethane − DIM) on various surfaces.

| Surface | Mean contact angle, $\theta$ (°) | | |
|---|---|---|---|
| | FW | EG | DIM |
| $C_8$PA | 111.1 ± 0.2 | 70.4 ± 2.3 | 85.2 ± 0.8 |
| $C_{10}$PA | 111.5 ± 0.9 | 71.4 ± 1.3 | 86.3 ± 2.6 |
| $C_{12}$PA | 112.0 ± 1.1 | 70.9 ± 5.2 | 87.1 ± 1.9 |
| $C_{14}$PA | 110.8 ± 1.3 | 71.2 ± 4.9 | 83.6 ± 1.6 |
| $C_{16}$PA | 111.3 ± 0.8 | 68.7 ± 1.7 | 84.9 ± 1.1 |
| $C_{18}$PA | 111.3 ± 0.8 | 70.8 ± 3.2 | 86.2 ± 1.0 |
| Non-desorbed $C_{18}$PA (~20 nm thick) | 77.4 ± 3.3 | 82.5 ± 0.4 | 70.7 ± 1.0 |

base component indicates that the surface has electron pair accepting ability. Conversely, the ~ 20-nm-thick non-desorbed $C_{18}$PA sample produced a surface energy ~ 31 mJ/m$^2$. This larger surface energy indicates that some $C_n$PA head groups are found on the surface. For this non-desorbed $C_{18}$PA case, the Lewis base component dominates (the surface has electron pair donating ability), followed by the sizeable Lifshitz-van der Waals energy which is around 50 % greater than that of the desorbed $C_n$PA monolayers. Table 4.2 summarises the results of the surface energy investigation.

**Table 4.2** Surface energies ($\gamma_s$) as calculated from the mean values of advancing contact angles of (a) ($\gamma_s^{LW}$ − Lifshitz-van der Waals, $\gamma_s^+$ − Lewis acid and $\gamma_s^-$ − Lewis base).

| Surface | $\gamma_s^+$ (mJ/m$^2$) | $\gamma_s^-$ (mJ/m$^2$) | $\gamma_s^{LW}$ (mJ/m$^2$) | $\gamma_s$ (mJ/m$^2$) |
|---|---|---|---|---|
| $C_8$PA | 3.22 | 0.56 | 14.91 | 17.61 ± 1.1 |
| $C_{10}$PA | 3.18 | 0.53 | 14.39 | 16.98 ± 1.2 |
| $C_{12}$PA | 3.51 | 0.68 | 14.02 | 17.11 ± 2.2 |
| $C_{14}$PA | 2.73 | 0.44 | 15.69 | 17.89 ± 2.1 |
| $C_{16}$PA | 3.64 | 0.82 | 15.06 | 18.51 ± 1.1 |
| $C_{18}$PA | 3.30 | 0.55 | 14.44 | 17.13 ± 1.2 |
| Non-desorbed $C_{18}$PA (~20 nm thick) | 0.67 | 27.23 | 22.48 | 31.03 ± 1.3 |

Due to the bonding of $C_nPA$ molecules to the underlying $AlO_x$ surface, $C_nPA$ molecules tend to be "standing up" within the monolayers. However, $C_{18}PA$ molecules that form the top surface of a ~ 20-nm-thick layer would be expected to assume random orientations, resulting in the exposure of –OH groups and different surface properties. In comparison to the results obtained for $C_nPA$ assembled in solution, it must be noted that the solution-assembled monolayers produce slightly smaller contact angles for FW and DIM and larger surface energies ranging between 25 and 30 $mJ/m^2$ [85].

Atomic force microscopy was used to investigate the $AlO_x/C_nPA$ surfaces on the nm scale, images of which can be seen in Figure 4.2. A summary of the data extracted from AFM is in Table 4.3. As well as determining the root-mean-square (RMS) surface roughness properties by using the new PeakForce QNM scanning mode, it was possible to directly extract quantitative nano-mechanical information

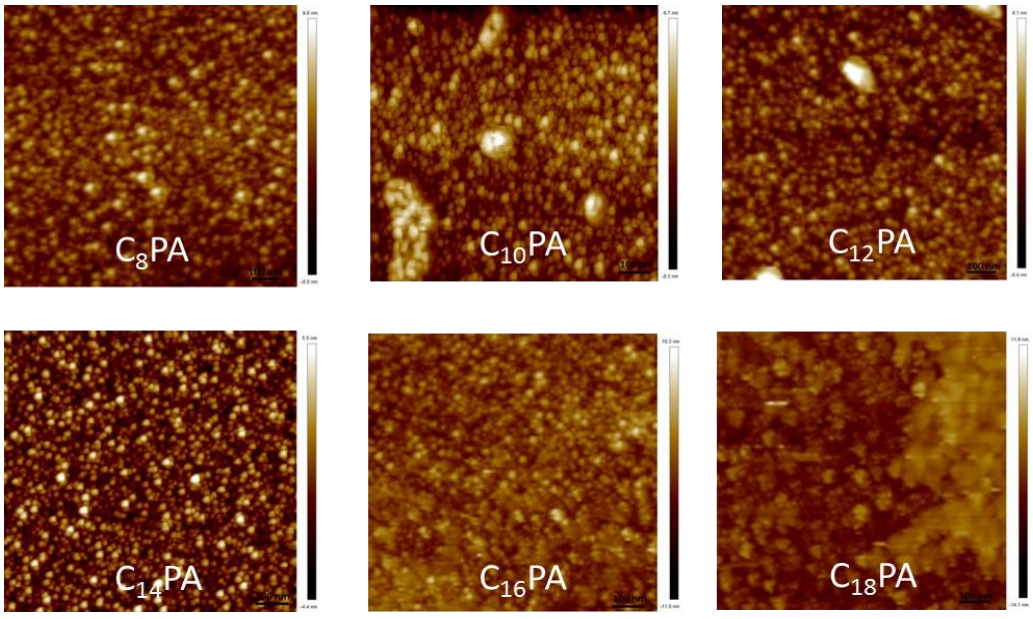



**Figure 4.2** AFM surface topography of $AlO_x/C_nPA$ surfaces for phosphonic acids ranging in chain length from $C_8PA$ to $C_{18}PA$.

such as the force of adhesion, elastic moduli, deformation and dissipation. Referring to Table 4.3, the surface roughness of the ~ 10-nm-thick reference non-annealed $AlO_x$ sample is 1.27 nm. After annealing the same $AlO_x$ sample for 3 hours at 160°C, the surface roughness remains almost unchanged at 1.22 nm. This lack of change in surface roughness of $AlO_x$ after annealing confirms that the $C_nPA$ desorption/annealing step would not lead to an increased overall surface roughness of the bi-layer dielectric due to an increased roughness of the underlying aluminium oxide. The RMS surface roughness of $AlO_x$ functionalised with $C_nPA$ is comparable to the bare-$AlO_x$ case (annealed or non-annealed) or slightly higher, but in all cases is less than 2.35 nm. The non-desorbed $C_{18}PA$ layer features a surface roughness of 2.25 nm. There does not seem to be any correlation between the $AlO_x/C_nPA$ surface roughness and the phosphonic acid chain length. Furthermore, no correlation exists between the $C_nPA$ length and the nano-mechanical properties. The force values lie between ~ 3 and ~ 5 nN, the moduli between 22 and 63 GPa, deformation between ~3 and ~8 nm and dissipation between ~ 200 and 1000 eV.

**Table 4.3** AFM measurements: surface roughness and nano-mechanical properties.

| Surface | Surface Roughness (nm) | Force (nN) | Modulus (GPa) | Deformation (nm) | Dissipation (eV) |
|---|---|---|---|---|---|
| $C_8PA$ | 1.25 | 3.1 ± 0.7 | 63 ± 9 | 2.8 ± 0.6 | 353 |
| $C_{10}PA$ | 1.53 | 3.6 ± 1.1 | 30 ± 9 | 3.2 ± 0.5 | 226 |
| $C_{12}PA$ | 2.34 | 5.3 ± 1.6 | 28 ± 10 | 3.6 ± 0.7 | 1016 |
| $C_{14}PA$ | 1.13 | 5.4 ± 1.5 | 29 ± 8 | 8.6 ± 2.5 | 277 |
| $C_{16}PA$ | 1.82 | 2.8 ± 0.6 | 22 ± 5 | 4.0 ± 0.6 | 219 |
| $C_{18}PA$ | 1.47 | 3.9 ± 1.0 | 37 ± 11 | 3.1 ± 0.1 | 945 |
| Non-desorbed $C_{18}PA$ (~20 nm thick) | 2.25 | 3.3 ± 1.2 | 65 ± 31 | 4.2 ± 1.1 | 566 |
| $AlO_x$ | 1.27 | 4.9 ± 1.3 | 43 ± 10 | 4.4 ± 0.1 | 961 |
| Annealed $AlO_x$ | 1.22 | 4.9 ± 1.1 | 65 ± 50 | 4.5 ± 0.1 | 509 |

In summary, all desorbed/annealed $AlO_x/C_nPA$ surfaces show comparable values of RMS surface roughness. While their mechanical properties on the nanometer scale (AFM tip size of 2 nm) vary by a factor of 2 to 5 (Table 4.3), their macroscopic surface properties (Tables 4.1 and 4.2) are very similar.

FTIR is capable of providing surface structural information on the macroscopic scale (~mm). FTIR was performed on the desorbed/annealed $AlO_x/C_nPA$ surfaces as well as the reference $AlO_x$ surface. Figure 4.3 displays the FTIR results taken.

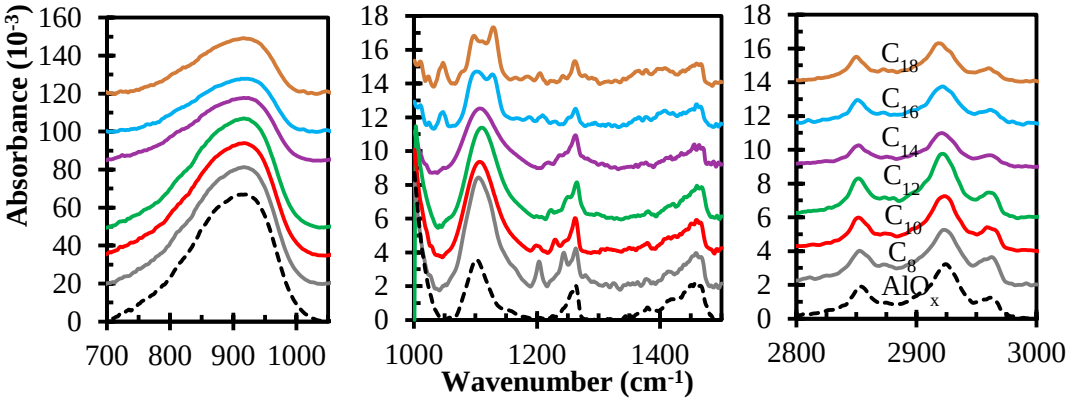



**Figure 4.3** FTIR spectra of $AlO_x/C_nPA$ bi-layers. Bare annealed $AlO_x$ is included for comparison. Individual spectra are offset by a constant value to allow easier viewing.

Referring to the graphs in Figure 4.3, a strong broad absorbance around 900 $cm^{-1}$ is dominated by Al-O vibrations in all samples measured. Weaker vibrations were noticed in the region from 1000 to 1250 $cm^{-1}$, near 1450 $cm^{-1}$ and between 2800 and 3000 $cm^{-1}$. In general, the integral intensity of various peaks is higher for shorter-chain $C_nPA$ and lower for longer chains. As the length of phosphonic acid aliphatic tail is increased, the position of $CH_2$ stretches is shifted to lower

wavenumbers and the associated FWHM is reduced. For the $C_8$PA sample, the peaks are centred at 2853 $cm^{-1}$ (FWHM = 20.7 $cm^{-1}$) and 2924 $cm^{-1}$ (FWHM = 31.9 $cm^{-1}$), while for $C_{18}$PA the peaks are found at 2850 $cm^{-1}$ (FWHM = 17.3 $cm^{-1}$) and 2920 $cm^{-1}$ (FWHM = 28.4 $cm^{-1}$). The position of these peaks is very similar to those reported previously for $C_n$PA monolayers prepared in ethanol on hafnium oxide [85].

Previously, the shift in the peak location was interpreted as an improved molecular order within monolayers, i.e. the increase in $C_n$PA length leads to stronger van der Waals interaction between aliphatic chains and results in a more ordered self-assembly with denser molecular packing [86-88]. However, one may predict that the density of monolayers deposited by vacuum evaporation would be lower than that of solution deposited monolayers as a result of the physical laws governing vapour deposition. This theory is supported by the fact that the integral intensity of the $CH_2$ stretches near 2850 and 2920 $cm^{-1}$ is not increasing with the increasing length of $C_n$PA. As shown in Figure 4.3, the integral intensity of these peaks is comparable for $C_8$, $C_{10}$ and $C_{12}$PA and lower for $C_{14}$, $C_{16}$ and $C_{18}$PA monolayers, suggesting lower molecular coverage for longer phosphonic acids.

To summarise, presence of $CH_2$ stretching vibrations confirm that a degree of order exists within vacuum deposited monolayers, with the molecular order improving for increasing length of alkyl chain. The reduction in the surface energy of vacuum deposited monolayers and the spread in nano-mechanical properties suggest a heterogeneous monolayer structure, such as the presence of ‘domains’ or ‘nanopores’. Previously, molecular dynamic simulations performed on solution assembled $C_n$PA monolayers on aluminium oxide confirmed a change in the morphology from amorphous to quasi-crystalline as a function of increasing length

of $C_nPA$ [89, 90]. In such a case, highly ordered domains with gaps between them exist for long $C_nPA$ molecules.

### 4.3.2 OTFTs: As-fabricated devices

Organic thin-film transistors incorporating $AlO_x/C_nPA$ gate dielectrics were prepared and tested. Figure 4.4 (a) shows the transistor transfer characteristics for the as-fabricated OTFTs with various phosphonic acid monolayers ranging from $C_8PA$ to $C_{18}PA$. Figure 4.4 (b) shows $\sqrt{I_D}$ as a function of $V_{GS}$ for the various phosphonic acids to allow extraction of saturation regime $\mu$ and $V_t$ as described previously in section 3.2.2.1. In addition, the extracted saturation regime transistor parameters are shown in Figure 4.5.

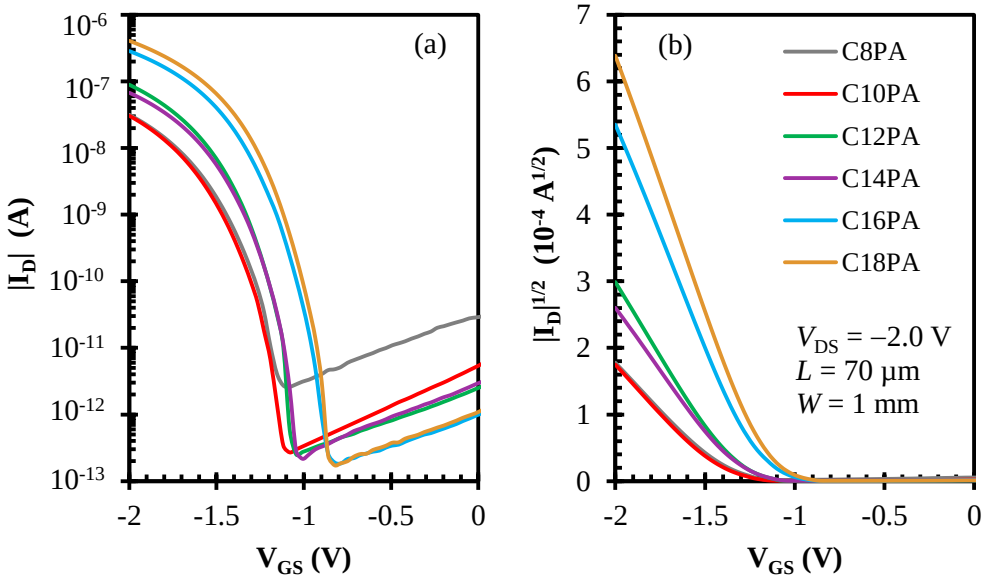



**Figure 4.4** OTFT transfer characteristics (a) and $\sqrt{I_D}$ vs $V_{GS}$ (b) for various $C_nPA$ monolayers.

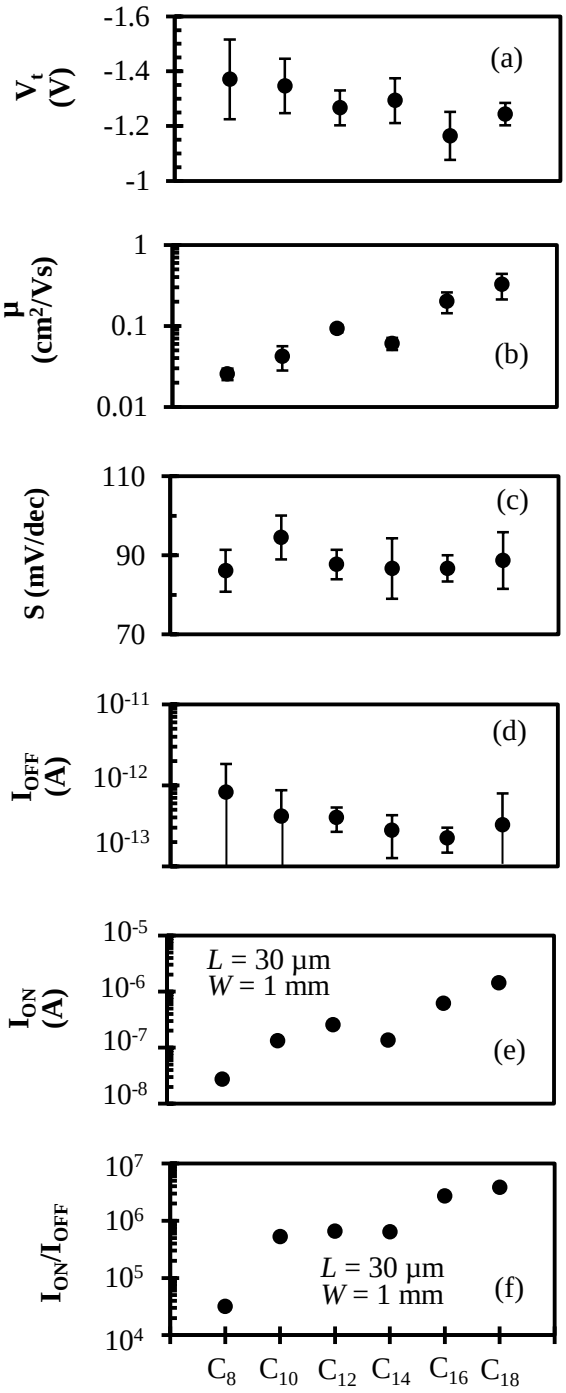



**Figure 4.5** OTFT parameters of the as-fabricated transistors as a function of $C_n$PA. Threshold voltage (a), field-effect mobility (b), subthreshold slope (c), OFF-current (d), ON-current (e) and ON/OFF current ratio (f).

Referring to Figure 4.4, as the length of aliphatic tail increases, transistor threshold voltage and OFF-current decrease. From Figure 4.5 it is clear that going

from $C_8$PA to $C_{18}$PA mean transistor threshold voltage decreases from –1.37 to –1.24 V, field-effect mobility increases from 0.03 to 0.33 $cm^2/Vs$, subthreshold slope remains fairly constant within the error of measurement (~ 90 mV/decade), OFF-current decreases from ~ $8x10^{-13}$ to ~ $3x10^{-13}$ A, and for OTFTs featuring a channel length of 30 μm, ON-current increases from ~ $3x10^{-8}$ to ~ $2x10^{-6}$ A. The ON/OFF-current ratio increases from ~ $3x10^4$ to ~ $4x10^6$.

### 4.3.3 OTFTs: Bias stress results

One transistor from each phosphonic acid sample was subjected to a 1000 second bias stress. The bias stress was performed in the usual manner, with a voltage of –2 V applied to the gate whilst the source and drain electrodes were grounded. Before commencing the bias stress experiment, all transistor samples were stored in dark ambient air for three days. Figure 4.6 (a) shows the evolution of transistor threshold voltage as a function of bias stress time. While the transistors featuring $C_{16}$PA and $C_{18}$PA monolayers display initial $V_t$ similar to that shown in Figure 4.4, the transistors incorporating shorter phosphonic acids show lower initial $|V_t|$, suggesting poorer ambient stability. However, the initial values of field-effect mobility and OFF-current are similar to those shown previously in Figure 4.4.

Application of bias stress results in a more negative threshold voltage for all transistors, however, the rate of degradation decreases as the length of phosphonic acid chain increases, making the transistors with $C_{18}$PA almost a factor of 2 more stable than those with $C_8$PA. Figure 4.6 (b) shows how the various $C_n$PA affect the

degradation in field-effect mobility differently. For both $C_{16}$PA and $C_{18}$PA, the mobility only reduces slightly after 1000 s, reaching ~ 93 % of the initial value. For $C_{12}$PA and $C_{14}$PA the mobility initially increases by ~ 20 % and then decreases to ~ 80 % of the initial value. For the shortest $C_n$PA transistors, the mobility first rises by 30 to 35 % but then decreases to around 60 % of the initial value. Figure 4.6 (c) shows that OTFT OFF-current decreases for all $C_n$PA. For longer chain $C_n$PA, the reduction in $I_{OFF}$ is almost non-existent, however it is much more pronounced for $C_8$PA and $C_{10}$PA. It is worth noting that since all the OTFTs were bias-stressed in the

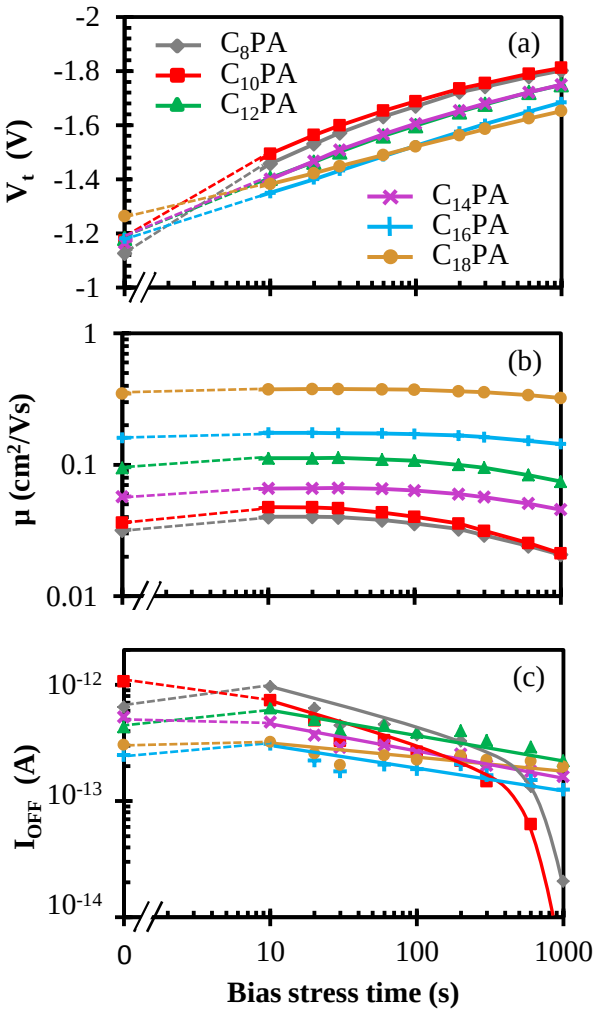



**Figure 4.6** Threshold voltage (a), field-effect mobility (b) and OFF-current (c) as a function of bias stress time for transistors with various $C_n$PA.

same laboratory environment (air ~ 40%RH), any differences in their degradation is ascribed to the transistor structure only. Table 4.4 summarises the initial and final OTFT parameters and their changes from 0 s to 1000 s of bias stress for transistors with different $C_nPA$.

The experimental results confirm a strong correlation between the initial and bias-induced transistor behaviour and the $C_nPA$ monolayer. Overall, the transistors exhibit improved initial parameters and ambient and bias stability when $C_nPA$ length increases. The FTIR vibrations between 2800 and 3000 $cm^{-1}$ indicate a degree of order within the monolayer that improves with increasing $C_nPA$ length.

**Table 4.4** Initial, final and change in bias stress parameters as a function of $C_nPA$ for $V_t$, $\mu$ and $I_{OFF}$.

| OTFT | $C_8PA$ | $C_{10}PA$ | $C_{12}PA$ | $C_{14}PA$ | $C_{16}PA$ | $C_{18}PA$ |
|---|---|---|---|---|---|---|
| $V_t$ (0s) (V) | -1.12 | -1.17 | -1.18 | -1.16 | -1.18 | -1.26 |
| $V_t$ (1000s) (V) | -1.80 | -1.81 | -1.75 | -1.75 | -1.68 | -1.65 |
| $\Delta V_t$ (V) | -0.68 | -0.64 | -0.57 | -0.59 | -0.5 | -0.39 |
| $\mu$ (0s) ($cm^2$/Vs) | 0.032 | 0.036 | 0.095 | 0.057 | 0.160 | 0.347 |
| $\mu$ (1000s) ($cm^2$/Vs) | 0.021 | 0.021 | 0.075 | 0.046 | 0.144 | 0.322 |
| $\Delta\mu$ ($cm^2$/Vs) | -0.011 | -0.015 | -0.020 | -0.011 | -0.016 | -0.025 |
| $\lvert I_{OFF}\rvert$ (0s) (A) | $6.44x10^{-13}$ | $1.07x10^{-12}$ | $4.35x10^{-13}$ | $5.28x10^{-13}$ | $2.08x10^{-13}$ | $3.05x10^{-13}$ |
| $\lvert I_{OFF}\rvert$ (1000s) (A) | $2.01x10^{-14}$ | $1.70x10^{-15}$ | $2.22x10^{-13}$ | $1.63x10^{-13}$ | $1.26x10^{-13}$ | $1.98x10^{-13}$ |
| $\Delta I_{OFF}$ (A) | $-6.42x10^{-12}$ | $-1.07x10^{-12}$ | $-2.13x10^{-13}$ | $-3.65x10^{-13}$ | $-8.2x10^{-14}$ | $-1.07x10^{-13}$ |

## 4.4 Discussion

Overall, as the length of phosphonic acid chain increases, there is a marked improvement in transistor performance. This behaviour is in contrast to transistors

incorporating phosphonic acids assembled from solution. $Si/HfO_2/C_nPA$/pentacene/Au organic transistors show threshold voltage becoming more negative with increasing $C_nPA$ length while the mobility of $C_8PA$ to $C_{14}PA$ exceeded that of $C_{16}PA$ to $C_{18}PA$ [85]. For $Si/AlO_x/C_nPA$/pentacene/Au transistors the threshold voltage did not change significantly and the mobility peaked for $C_{14}PA$ [77]; for $Si/SiO_2/C_nPA$/pentacene/Au devices the lowest threshold voltage occurred for $C_8PA$, the mobility decreased from $C_8PA$ to $C_{18}PA$ and the subthreshold slope was unaffected [91]; for $Al/AlO_x/C_nPA$/pentacene/Au transistors the mobility peaked for $C_{14}PA$ for oxygen-plasma $AlO_x$ and increased with increasing $C_nPA$ length for mild-air-plasma $AlO_x$ [35]; and for $Si/AlO_x/C_nPA$/pentacene/Au devices both the mobility and the threshold voltage increased with increasing $C_nPA$ length [89].

It is worth comparing the performance of the $C_{18}PA$ transistors to recently reported DNTT-based OTFTs incorporating other gate dielectrics. Crosslinked poly(ethylene-*alt*-maleic anhydride) (PEMA) led to a mobility of 0.11 $cm^2/Vs$, while PEMA modified with poly(maleic anhydride-*alt*-1-octadecane) resulted in a mobility of 0.24 $cm^2/Vs$ [92]. Octylamine-treated PEMA gate dielectric produced a mobility of 0.17 $cm^2/Vs$ [93]. DNTT deposited by vapour-jet on polystyrene-buffered poly(tripropyleneglycol diacrylate) dielectric led to a mobility of 0.43 $cm^2/Vs$ [94]. Additionally, field-effect mobilities greater than 1 $cm^2/Vs$ have been reported when gate dielectrics featuring organic monolayers were used [42, 95, 96]. Transistor threshold voltage and subthreshold slope are dependent on gate dielectric thickness and our values are consistent with other figures reported for gate dielectrics of similar thickness. Finally, comparison of the ON/OFF-current ratio is difficult since it is dependent on transistor dimensions in order for a fair comparison to be given.

Previous research on phosphonic acids has shown that phosphonic acids assembled from solution are able to attach strongly to aluminium oxide [97]. The attachment process is enabled by the acid's head group. It has been proposed that during the solution-based self-assembly process of the phosphonic acid monolayer the head group reacts with the surface hydroxyl groups of the aluminium oxide [98]. This reaction proceeds via acid-base condensation mechanisms in stages and can ultimately result in a tridentate binding configuration of the phosphonic acid [99-101]. The first step involves the two P-OH groups of the $C_nPA$ head group reacting with two Al-OH groups on the aluminium oxide surface to form two P-O-Al bonds of a bidentate complex. Next, the P=O group forms the third P-O-Al bond and converts the bidentate complex into a tridentate one.

Regarding the performance of the organic thin-film transistors, specifically their threshold voltage, it is worth noting a few remarks. The presence of Al-OH groups on the surface of $AlO_x$ could result in a fixed negative charge at the $AlO_x/C_nPA$ interface. Since more Al-OH sites would be expected for longer chain phosphonic acids when fewer molecules are attached to aluminium oxide, lower OTFT threshold voltage would be expected for longer $C_nPA$. This is indeed the case for the measured as-fabricated transistors however the presence of Al-OH groups does not explain the changes in OTFT threshold voltage when devices are exposed to ambient air.

We know the choice of $C_nPA$ affects the gate dielectric capacitance (Figure 4.1) and the threshold voltage of the transistors (Figure 4.5). Therefore, one should consider the induced capacitive charge at the beginning of the transistor bias degradation. Since the gate-to-channel voltage is not known, the gate-to-source

voltage $V_{GS}$ is used to approximate the accumulated charge, i.e. $Q = C\,|V_{GS} - V_t|$. This charge is 0.41 μC/cm$^2$ for $C_8$PA, 0.24 μC/cm$^2$ for $C_{18}$PA, and 0.31 – 0.33 μC/cm$^2$ for the remaining $C_n$PA. If transistor bias degradation was solely controlled by the induced charge density, then transistors with $C_{10}$, $C_{12}$, $C_{14}$ and $C_{16}$PA should exhibit similar degradation behaviour. However, the results of Figure 4.6 show degradation that is clearly linked to the length of the phosphonic acid instead of the induced charge density.

## 4.5 Summary

For low-voltage transistor operation, growth which self-limits the thickness of materials for ultra-thin dielectric layers is advantageous. This chapter describes the preparation of monolayers of alkyl phosphonic acids ($C_8$PA to $C_{18}$PA) by vacuum evaporation and their incorporation into organic thin-film transistors based on DNTT.

Various $AlO_x/C_n$PA bi-layer dielectrics were produced ranging in thickness from ~ 11 to 12-nm displaying low leakage current densities between ~ 6x10$^{-8}$ and ~ 3x10$^{-8}$ A/cm$^2$ at –3 V. A decrease in $AlO_x/C_n$PA layer capacitance was observed as a function of increasing phosphonic acid chain length confirming the formation of a monolayer of phosphonic acid on the surface of aluminium oxide in all cases. The total surface energy of desorbed/annealed $AlO_x/C_n$PA surfaces is ~ 17.5 mJ/m$^2$ regardless of $C_n$PA length. In addition, all bi-layer surfaces exhibit similar values of RMS surface roughness. However, while their surface properties on the macroscopic

scale are similar, the mechanical properties on the nanometer scale vary by a factor of 2 to 5. By the same token as solution-assembled phosphonic acid monolayers, the $CH_2$ stretching peaks as observed through FTIR are narrowing and shifting to lower wavenumbers, thereby proving that molecular order improves with increasing length of $C_nPA$. There is also a reduced molecular coverage for longer $C_nPA$ chains. Reduction in the surface energy of vacuum deposited monolayers and the spread in nano-mechanical properties suggest a heterogeneous monolayer structure, such as the presence of 'domains' or 'nanopores'.

$AlO_x/C_nPA$ dielectrics were incorporated into organic thin-film transistors and the electrical performance of the as-fabricated devices is considerably affected by the $C_nPA$ used. Moving from $C_8PA$ to $C_{18}PA$, transistor threshold voltage shifts closer to zero (becomes more positive) by ~ 10%, field-effect mobility increases by an order of magnitude, OFF-current reduces by ~ 50%, and there was no obvious change in the subthreshold slope parameter. Accordingly, OTFT ON-current and the ON/OFF current ratio increased by two orders of magnitude for transistors with $L$ = 30 μm. Transistor parameters significantly improved across the board with increasing length of $C_nPA$. Bias stress was also performed on the transistors and the results confirm that the stress-induced degradation as a function of applied bias stress time is related to $C_nPA$ length. As the molecule length increases, the effect of bias stress on the transistors is less pronounced. Furthermore, the longer $C_nPA$ OTFTs display better air stability.

# Chapter 5

# OTFTs on PEN substrates

This chapter presents the steps taken to transfer the OTFT fabrication onto two polyethylene naphthalate (PEN) foils. It also studies the effect of thermal annealing of the plastic substrates prior to transistor fabrication. Subsequently, MIM and OTFT structures were prepared on each PEN substrate and their electrical characteristics were examined.

The procedure to fabricate devices on PEN foils is outlined in Section 5.1, including the substrate preparation. MIM/OTFT device fabrication is described in

Section 5.2. Results of the substrate annealing, MIM measurements, OTFT performance, and bias stress are provided in Section 5.3. Finally, discussion is provided and the chapter is summarised in Sections 5.4 and 5.5.

## 5.1 Introduction

To achieve flexible organic circuits, device fabrication on thin plastic substrates is required. This chapter adapts the OTFT fabrication procedure introduced in Chapter 3 to flexible PEN plastic substrates. Transistors feature a 10-nm-thick bi-layer dielectric based on aluminium oxide ($AlO_x$) and n-octylphosphonic acid ($C_8PA$) monolayer with DNTT as the organic semiconductor layer.

Two commercially available polyethylene naphthalate (PEN) plastic foils (DuPont Teijin) were used; Teonex Q65FA and Optfine PQA1. Teonex includes an adhesive layer on its bottom (non-device) side to prevent film slippage during R2R processing, while Optfine has a planarisation layer on the top (device) side to provide an ultra-smooth finish. Both PEN substrates were thermally annealed at 160°C to assess their compatibility with the maximum temperature used during the OTFT fabrication process. Low-voltage p-type OTFTs were fabricated on each substrate and their electrical performance was assessed. Finally, a correlation between PEN type and OTFT performance was sought.

## 5.2 Substrate preparation and OTFT fabrication

7.5 cm x 7.5 cm PEN substrates were thoroughly cleaned using acetone and isopropanol. Two substrates from each PEN type were prepared, one for the investigation of the anneal treatment and the other for MIM and OTFT fabrication.

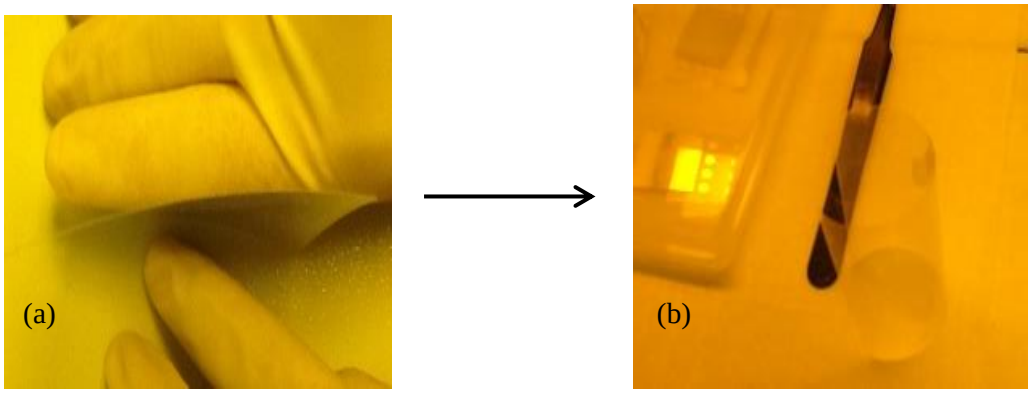
Teonex Q65FA and Optfine PQA1 PEN films were annealed at 160°C for 24 hours. 160°C was chosen to match the maximum temperature used in the transistor fabrication process. Due to the outcome of the anneal treatment on the PEN films, OTFTs were fabricated on non-annealed Optfine and pre-annealed Teonex. OTFT and MIM structures were prepared with $AlO_x/C_8PA$ dielectric as well as bare $AlO_x$ for reference. $C_8PA$ was deposited on the surface of $AlO_x$ at 25°C at a rate of ~ 3 Å/s. For the OTFTs, 15 nm of DNTT was deposited at room temperature at rates of 0.4 Å/s and 0.6 Å/s on Teonex and Optfine respectively. During DNTT evaporation, the MIM structures were fully masked. The devices were completed by evaporating 50-nm-thick gold source and drain contacts. Figure 3.1 in Chapter 3 shows the transistor cross-section. $L$ was 30, 50, 70 or 90 µm and $W$ = 1000 µm.

## 5.3 Results

### 5.3.1 Substrate annealing

Teonex Q65FA was flat prior to the annealing. After the 24-hour anneal it still remained flat (infinite radius of curvature). However, the Optfine PQA1 substrate featuring a planarisation layer on the device side behaved differently. Before annealing, Optfine exhibited a radius of curvature of ~ 17 cm. After the

anneal, the radius of curvature reduced dramatically to ~ 1.5 cm. Figure 5.1 summarises the effect of thermal annealing on the Optfine PQA1 PEN.




Radius of curvature ~ 17 cm

Radius of curvature ~ 1.5 cm

**Figure 5.1:** Radius of curvature of Optfine PQA1 PEN film prior to (a) and after 24 hour anneal at 160°C (b).

## 5.3.2 MIM measurements

Table 5.1 summarises the capacitance and current density of MIM devices on Teonex and Optfine substrates for both $AlO_x$ and $AlO_x/C_8PA$ dielectrics. The capacitance represents the mean capacitance extracted at 10 kHz. The current density was extracted at –2 V.

As expected, the capacitance of bare-$AlO_x$ MIM devices is greater for both PEN films compared to the $AlO_x/C_8PA$ dielectric. In addition, the current density is lower when $AlO_x$ is functionalised with $C_8PA$, for both PEN substrates. There is a larger difference in the capacitance and current density (with and without $C_8PA$) when Optfine PEN is used.

**Table 5.1:** MIM capacitance and current density at –2 V.

| | Teonex Q65FA | | Optfine PQA1 | |
|---|---|---|---|---|
| | $AlO_x$ | $AlO_x/C_8PA$ | $AlO_x$ | $AlO_x/C_8PA$ |
| Capacitance ($\mu F/cm^2$) | 0.74 | 0.66 | 0.86 | 0.43 |
| Current ($A/cm^2$) | $4.42x10^{-7}$ | $2.57x10^{-7}$ | $2.32x10^{-7}$ | $8.39x10^{-8}$ |

### 5.3.3 OTFT measurements

Due to the results of the thermal anneal, $Al/AlO_x/C_8PA/DNTT/Au$ and $Al/AlO_x/DNTT/Au$ organic thin-film transistors were fabricated on non-annealed Optfine and pre-annealed Teonex. Figure 5.2 (a) shows a saturation regime transfer characteristic of an as-fabricated $AlO_x/C_8PA$ transistor on Teonex. The ON-current is ~ 3 x $10^{-7}$ A, while the gate leakage current is ~ $10^{-10}$ A. Figure 5.2 (b) shows $\sqrt{I_D}$ as a function of $V_{GS}$ for the same transistor to explain how mobility and threshold voltage were extracted using the methodology described previously in chapter 3. Figure 5.3 shows the as-fabricated OTFT parameters extracted from transfer characteristics measured at a drain voltage of –2 V.

Referring to Figure 5.3, for both Teonex and Optfine, inclusion of the n-octyl phosphonic acid monolayer leads to an increase in field-effect mobility, ON-current and ON/OFF-current ratio whilst reducing the subthreshold slope and OFF-current.

The two PEN substrates have a mixed effect on OTFT performance. The transistors fabricated on Teonex have a slightly lower subthreshold slope and OFF-current compared to the Optfine devices. However, OTFTs on the planarised Optfine

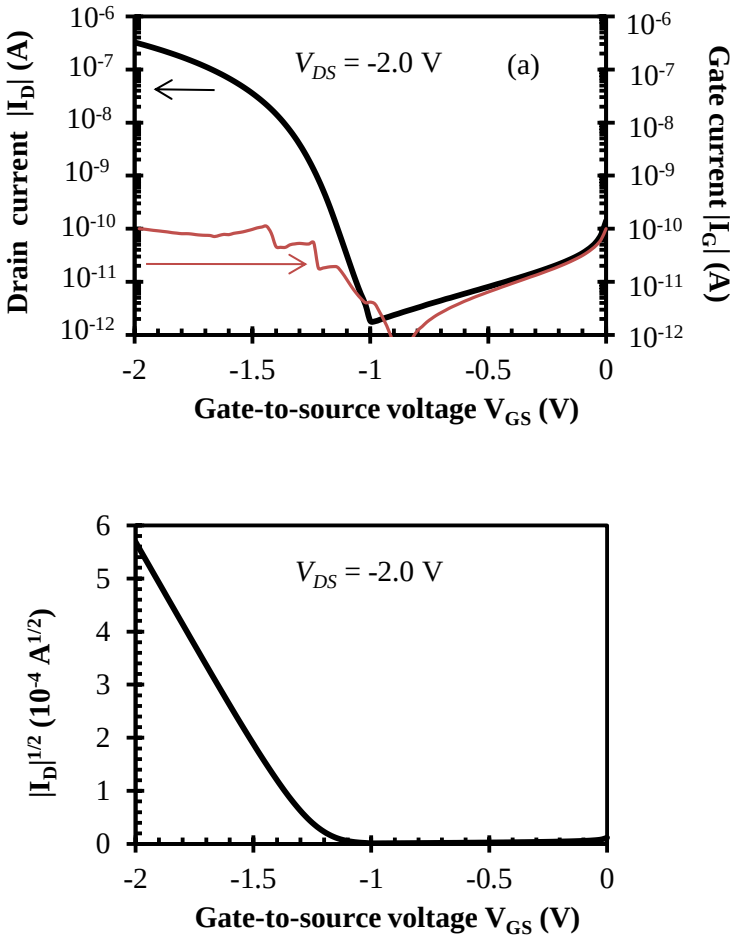



**Figure 5.2:** Transfer characteristics of OTFT with $AlO_x/C_8PA$ gate dielectric in saturation regime (a). $\sqrt{I_D}$ vs $V_{GS}$ in saturation regime (b) OTFT fabricated on Teonex Q65FA PEN substrate. $L$ = 50 µm and $W$ = 1000 µm.

PQA1 substrate exhibit around a factor of three higher field-effect mobility (~ 0.14 $cm^2/Vs$) and around an order of magnitude higher ON-current compared to the Teonex Q65FA case. Transistor threshold voltage remains essentially the same regardless of the PEN film used for the $AlO_x/C_8PA$ OTFTs. On the other hand, OTFTs with bare-$AlO_x$ dielectrics show a few subtle differences in OTFT behaviour, compared with their $AlO_x/C_8PA$ counterparts. OTFT $|V_t|$ is around 0.35 V lower for Optfine OTFTs. Subthreshold slope is around a factor of two smaller for Teonex. The ON-current for the bare-$AlO_x$ OTFTs is marginally higher for Optfine PEN,

however its OFF-current is more than one order of magnitude greater than Teonex. Consequently, the ON/OFF-current ratio for Optfine OTFTs is smaller.

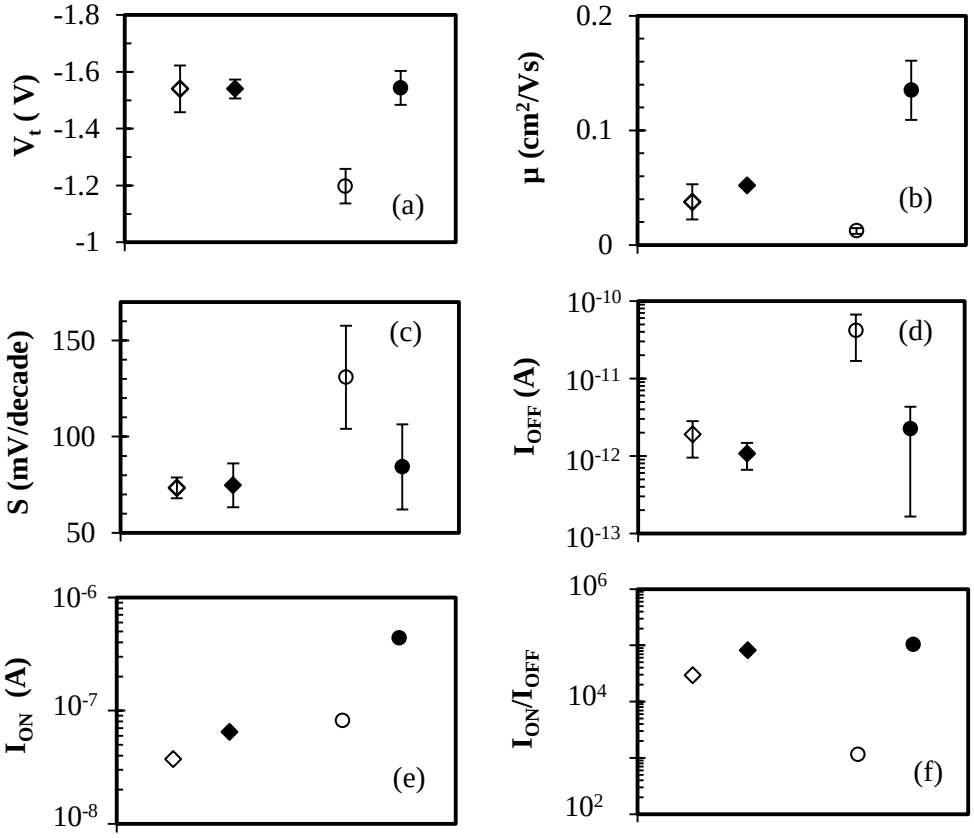



**Figure 5.3:** Threshold voltage (a), field-effect mobility (b), subthreshold slope (c), OFF-current (d), ON-current (e) and ON/OFF ratio (f) for Teonex Q65FA and Optfine PQA1 PEN. Empty and full symbols represent OTFTs with $AlO_x$ and $AlO_x/C_8PA$ dielectrics respectively. ◊♦ = Teonex Q65FA and ○● = Optfine PQA1.

## 5.3.4 Bias stress

To evaluate the long term stability of organic thin-film transistors on Teonex and Optfine PEN foils, bias stress was performed on OTFTs from each substrate, for both $AlO_x$ and $AlO_x/C_8PA$ dielectrics. Bias stress was administered approximately

one week after the initial transfer characteristics were taken. During that time all samples were stored in the dark vacuum conditions, which led to a decrease in $|V_t|$ for all transistors measured. Bias stress was applied for a total of 1000 seconds while the gate was held at –2 V and source and drain were grounded. Figure 5.4 summarises

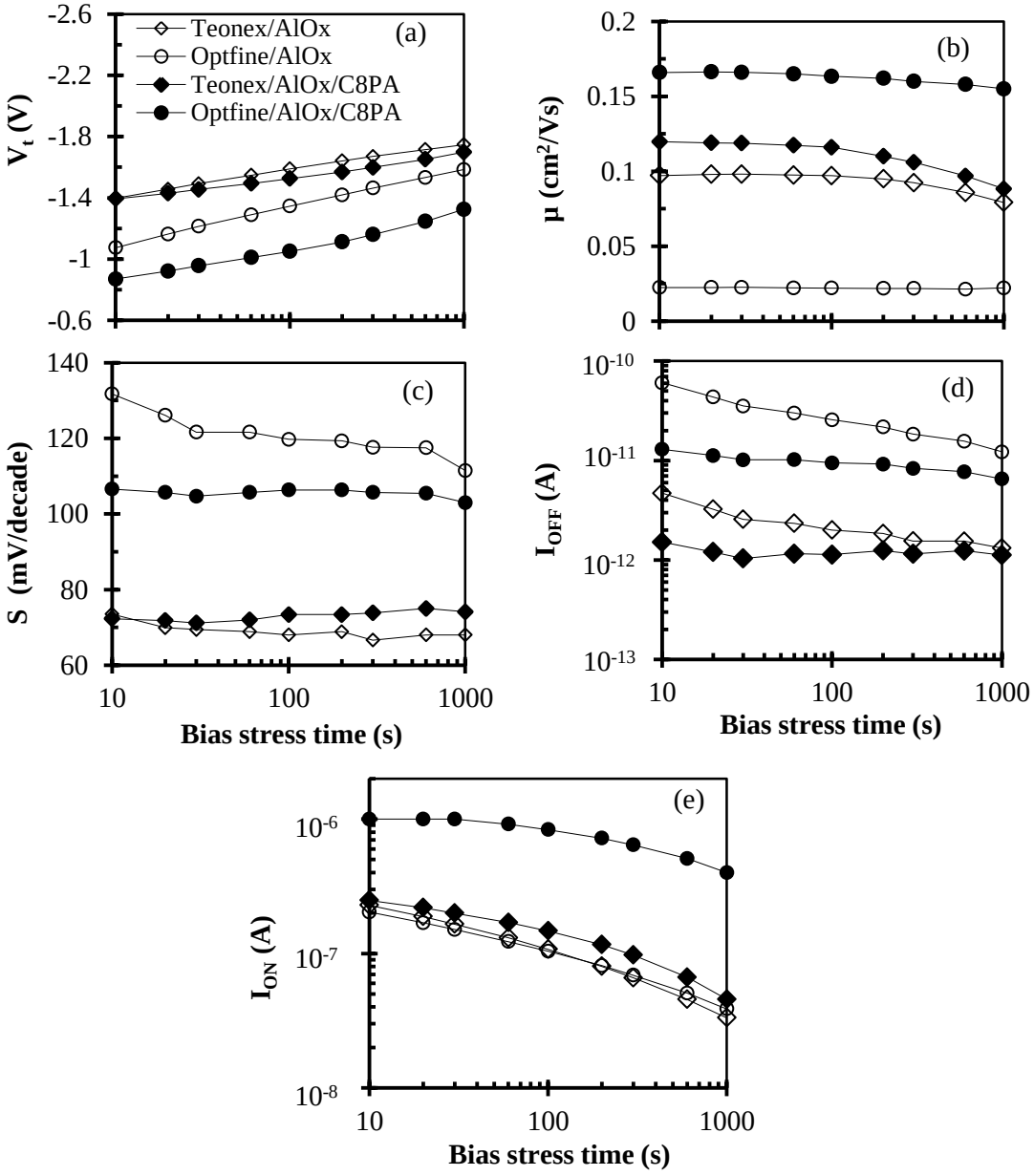



**Figure 5.4:** Effect of bias stress on threshold voltage (a), field-effect mobility (b), subthreshold slope (c), OFF-current (d) and ON-current (e) for Teonex Q65FA and Optfine PQA1 PEN. Empty and full symbols represent OTFTs with AlOx and $AlO_x/C_8PA$ dielectrics respectively. ♦◊ = Teonex Q65FA and ●○ = Optfine PQA1.

the results of the bias stress performed on four OTFTs to investigate the effect of PEN type. Table 5.2 summarises the OTFT parameters extracted at 1000 s and compares them to the initial parameters. Both $AlO_x$ and $AlO_x/C_8PA$ OTFTs on Teonex and Optfine are included in the table.

**Table 5.2:** OTFT parameters for Teonex Q65FA and Optfine PQA1 PEN substrates before and after a 1000-second bias stress.

| | **Teonex Q65FA** | | | | **Optfine PQA1** | | | |
|---|---|---|---|---|---|---|---|---|
| | $AlO_x$ OTFT | | $AlO_x/C_8PA$ OTFT | | $AlO_x$ OTFT | | $AlO_x/C_8PA$ OTFT | |
| | 0s bias | 1000 s bias | 0s bias | 1000 s bias | 0 s bias | 1000 s bias | 0 s bias | 1000 s bias |
| **$V_t$ (V)** | –1.20 | –1.75 | –1.27 | –1.70 | –0.40 | –1.58 | –0.72 | –1.33 |
| **μ ($cm^2/Vs$)** | 0.090 | 0.079 | 0.11 | 0.088 | 0.018 | 0.022 | 0.16 | 0.16 |
| **S(mV/decade)** | 85 | 68 | 78 | 74 | 166 | 111 | 112 | 103 |
| **$\|I_{OFF}\|$ (A)** | $1.4x10^{-11}$ | $1.3x10^{-12}$ | $1.8x10^{-12}$ | $1.1x10^{-12}$ | $2.8x10^{-10}$ | $1.2x10^{-11}$ | $1.7x10^{-11}$ | $6.5x10^{-12}$ |
| **$\|I_{ON}\|$ (A)** | $3.6x10^{-7}$ | $3.3x10^{-8}$ | $3.2x10^{-7}$ | $4.6x10^{-8}$ | $4.0x10^{-7}$ | $3.9x10^{-8}$ | $9.9x10^{-7}$ | $4.0x10^{-7}$ |

There is a clear difference in OTFT performance on Teonex and Optfine as a function of bias stress time. Furthermore, similarly to what was seen previously in the initial OTFT transfer characteristics (Figure 5.3), OTFTs on the same substrate exhibit differences due to incorporation of the phosphonic acid monolayer. Bare-$AlO_x$ transistors on both PEN foils display higher $V_t$ and OFF-current, but lower field-effect mobility and ON-current compared to their $AlO_x/C_8PA$ equivalents. Comparing OTFTs featuring $C_8PA$ on Teonex and Optfine substrates, Teonex OTFTs appear to have ~ 40 mV/decade lower subthreshold slope and around an order of magnitude lower OFF-current compared to the Optfine OTFTs. Conversely, Optfine OTFTs with $C_8PA$ have around 33 % greater field-effect mobility compared to Teonex transistors.

Finally, for both $AlO_x$ and $AlOx/C_8PA$ dielectrics, organic transistors on Optfine PEN are more stable during the 1000 s bias stress in terms of their field-effect mobility when compared with OTFTs on Teonex.

## 5.4 Discussion

The suitability of Teonex Q65FA and Optfine PQA1 PEN substrates was assessed by thermal annealing of both PEN foils prior to device fabrication. The annealing temperature was chosen as 160°C to match the maximum temperature used in the OTFT fabrication process [75]. Dupont Teijin states that a typical PEN film has a melting point around 269°C [102] and therefore, the temperature of 160°C is well below the melting point. Annealing at 160°C for 24 hours in a vacuum oven showed differences between these two substrates. Teonex Q65FA remained completely flat after the heat treatment. Furthermore, there was no noticeable change to the adhesive on the non-device side of the substrate, proving that the adhesive layer engineered to prevent film slippage during roll-to-roll fabrication is able to withstand our OTFT fabrication process, allowing for the process to be transferred to roll-to-roll processing. However, Optfine PQA1 PEN foil curved considerably upon heating, with its radius of curvature changing from ~ 17 cm to 1.5 cm after the anneal, rendering it unsuitable for device fabrication in its annealed state.

A number of differences exist between Teonex and Optfine in terms of OTFT performance. Referring to transistors with $AlO_x/C_8PA$ dielectric, OTFTs on Teonex show a slightly lower subthreshold slope and OFF-current than the Optfine

equivalents. However, OTFTs on Optfine PEN exhibit about an order of magnitude higher ON-current resulting from a factor of three greater field-effect mobility. This may be due to the fact that DNTT was deposited at a higher rate of 0.6 Å/s on the Optfine, as opposed to the lower evaporation rate of 0.4 Å/s on Teonex PEN. Previously, similar OTFTs featuring pentacene as the organic semiconductor showed increasing field-effect mobility as a function of pentacene evaporation rate for transistors with 4x purified pentacene [72]. From AFM images conducted on the pentacene samples, it was shown that although higher pentacene evaporation rates led to a smaller pentacene grain size, the grains showed less sub-grain structure and tighter packing. Similarly, DNTT could show a similar effect when evaporated at higher rates, resulting in improved mobility. Furthermore, OTFTs on planarised Optfine PEN would be likely to benefit from the lower surface roughness [103] provided by the planarisation layer possibly leading to improved OTFT performance than equivalent transistors on non-planarised Teonex Q65FA.

Previously, DNTT-based bottom-gate top-contact OTFTs on 125-μm-thick PEN substrates featuring a cross-linked TPGDA dielectric layer led to mobility ~ 0.46 $cm^2$/Vs with $V_t$ ~ –14 V [40]. Similar OTFTs to those presented in this thesis on Teonex Q65FA featuring $AlO_x/C_{14}PA$ dielectric with vacuum deposited DNTT with $L$ as low as 10 μm achieved mobility as large as 2 $cm^2$/Vs with an impressive ON/OFF-current ratio of ~ $10^8$ [42]. There are a number of reasons why our OTFTs exhibit lower mobility than those presented in [41]. Firstly, their SAM of $C_{14}PA$ dielectric is formed in solution, whereas the transistors presented in this thesis feature vacuum deposited phosphonic acids. Secondly, the DNTT deposition requires further optimisation. DNTT evaporation rate and temperature can both influence field-effect

mobility due to a modification of the interface between the $C_nPA$ and the semiconductor, and further work would need to be done to assess the influence of these parameters on OTFT performance.

By integrating OTFTs onto flexible plastic substrates such as PEN foil, transistors can be used alongside devices such as force/temperature ferroelectric capacitors based on P(VDF-TrFE). Accordingly, OTFTs will require minimum deterioration in their electrical performance. Conducting bias stress experiments can aid with understanding of the electrical stability of transistors. The results show that the OTFTs on Optfine are more stable under the application of bias stress in terms of field-effect mobility, despite their threshold voltage at the beginning of the bias stress test being ~ –0.4 V lower than that of OTFTs fabricated on Teonex.

## 5.5 Summary

Low-voltage organic thin-film transistors fabricated on two free-standing commercial polyethylene naphthalate foils was studied. The investigated PEN foils were Teonex Q65FA featuring an adhesive layer on the non-device side and Optfine PQA1 with a planarisation layer on the device side. Pre-annealing of both substrates at 160°C for 24-hours prior to device fabrication showed that Teonex Q65FA was far easier to handle because it remained flat upon heating. On the contrary, Optfine PQA1 experienced a drastic and permanent reduction in its radius of curvature, rendering it unsuitable for the device fabrication in its annealed state. Regarding $AlO_x/C_8PA$ transistors, devices on Optfine PEN exhibited improved OTFT field-

effect mobility compared to those on Teonex and also remained more stable under the bias stress. This could result from higher DNTT deposition rate compared with that used on Teonex. Overall the curving of Optfine PEN upon prolonged annealing presents a significant challenge if used as a free-standing substrate. On the other hand, the non-annealed Optfine substrate did not present a major problem for layer-to-layer alignment during the transistor fabrication and the resulting transistor performance was better than transistors fabricated on Teonex PEN.

# Chapter 6

# Response of P(VDF-TrFE) capacitor to force and temperature

Previously, Chapter 3 described the fabrication of the ferroelectric P(VDF-TrFE) capacitor. In this chapter, the response of such a capacitor (tactile sensor) to static compressive force and constant temperature is presented. Section 6.1 introduces the concept of tactile sensing and relates it to examples from the literature. A brief outline of the materials used for the P(VDF-TrFE) capacitor fabrication is given in Section 6.2. Section 6.3 presents the electrical properties of the P(VDF-TrFE) capacitor. Results of the capacitor's response to force and temperature are

presented in Sections 6.4 and 6.5 respectively. Section 6.6 discusses the findings from the P(VDF-TrFE) capacitance measurements. Finally, the chapter is summarised in Section 6.7.

## 6.1 Introduction

The field of tactile sensing has been evolving rapidly over recent years; where development of sensors for applications such as touch screen interfaces and electronic skin has received notable interest within the field of mobile devices, robotics or for medical applications. An effective 'electronic skin' should replicate the fundamental features of real skin; from pressure and temperature transduction to having the ability to stretch and conform to non-planar surfaces [104]. Various examples of sensors for force or temperature monitoring exist. For force detection, sensors typically exploit the piezoresistive effect [105, 106], the piezoelectric effect [107, 108] or capacitive changes [109, 110], whereas capacitive [111] and pyroelectric-based sensors [112, 113] are often used for sensing temperature. This chapter focusses on the capacitive response of the P(VDF-TrFE) sensor to detect static force and temperature stimuli.

Tactile sensors using PVDF or its copolymer P(VDF-TrFE) are able to detect dynamic changes in force/temperature through inherent piezoelectric/pyroelectric properties in poled materials [114–116]. However, the piezo/pyroelectric effects are only suitable for detecting changes in force or temperature, i.e. dynamic stimuli, since the charge developed through these phenomena discharges almost instantly in

the absence of additional circuitry such as a charge amplifier [117]. Therefore, the need for such sensors to detect static stimuli, i.e. constant or quasi-constant force or temperature, exists for more realistic e-skin applications. One way to address this is to exploit changes in capacitance of P(VDF-TrFE) parallel-plate capacitors when they are exposed to compressive force or temperature.

This chapter presents the response of a P(VDF-TrFE) ferroelectric capacitor to both static compressive normal force and a constant temperature recorded as a change in its capacitance. Electrical properties of the capacitor are shown first, including I-V and C-V measurements; followed by results of force and temperature experiments to understand how its capacitance responds to these external stimuli.

## 6.2 Experimental details

The ferroelectric capacitor adopts the parallel plate-capacitor structure (see Figure 3.10) where the P(VDF-TrFE) ferroelectric layer is sandwiched between the bottom (Al) and top (Au) metal electrodes. Chapter 3 explains the fabrication process in greater detail. Each fabricated capacitor with an active sensing area of 25 $mm^2$ was mounted on a glass slide to make it compatible with the linear micro stage for force application. The final P(VDF-TrFE) film thickness was ~ 2.5 µm.

## 6.3 Electrical properties of P(VDF-TrFE) capacitor

Current-voltage (I-V) and capacitance-voltage (C-V) measurements were performed on P(VDF-TrFE) capacitors. Sections 6.3.1 and 6.3.2 present the I-V and C-V results on a freshly fabricated P(VDF-TrFE) capacitor that was poled with positive voltage applied to the aluminium electrode.

### 6.3.1 Current-voltage (I-V)

A linear change in current with voltage is observed for the poled P(VDF-TrFE) capacitor (see Figure 3.11) and its leakage current is 57.5 pA at 1 V, making it suitable for our application.

### 6.3.2 Capacitance-voltage (C-V)

Figure 3.12 shows that as the voltage applied to the Al electrode of the capacitor becomes more positive, the capacitance increases by ~ 3 pF between –5 and +5 V. No hysteresis is observed in this voltage range.

## 6.4 Response of P(VDF-TrFE) capacitor to force

Force was applied to the P(VDF-TrFE) capacitor with a Teflon probe using the setup described in section 3.5.3. Figure 6.1 shows the effect of compressive force

applied in the normal direction to a freshly fabricated, poled P(VDF-TrFE) capacitor performed at room temperature. The graph shows the change in capacitance (at 2 kHz) from 0 N to a maximum applied force of 8.85 N across 40 % of the P(VDF-TrFE) active area.

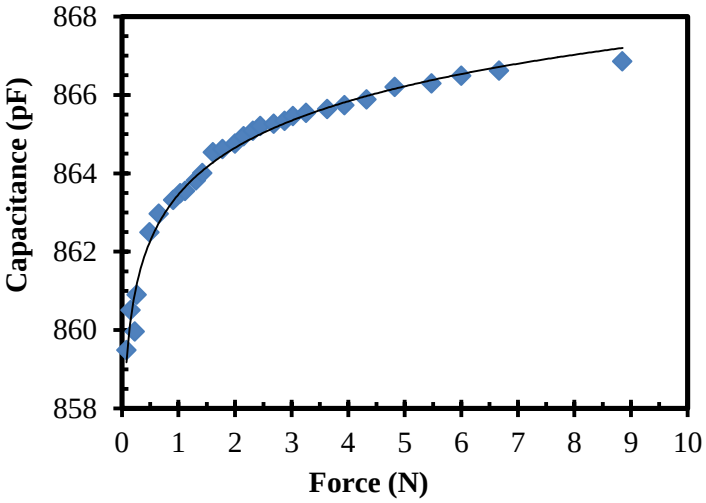



**Figure 6.1:** P(VDF-TrFE) capacitance as a function of applied force. Capacitance is extracted at 2 kHz.

With no force applied, the P(VDF-TrFE) capacitance is 858.59 pF. Upon application of a 8.85 N force, the capacitance has increased to 866.85 pF, an increase of 8.26 pF across the 8.85 N force range. P(VDF-TrFE) capacitance follows a logarithmic dependence on the applied force. Defining sensitivity as the change in capacitance per unit force, sensitivity is far greater at the low end of applied forces. Within the range of forces from 0 N to ~ 0.5 N (Figure 6.2), P(VDF-TrFE) capacitance responds approximately linearly to force, with a sensitivity of ~ 7.1 pF/N.

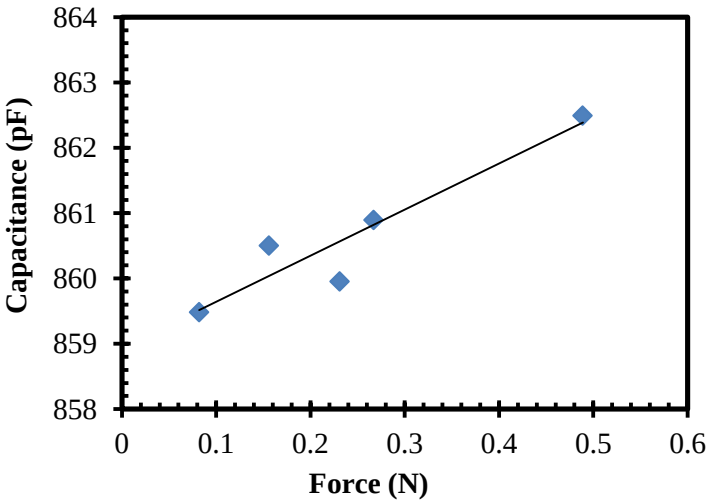



**Figure 6.2:** P(VDF-TrFE) capacitance as a function of applied force for forces between 0 to ~ 0.5 N. Capacitance is extracted at 2 kHz.

## 6.5 Response of P(VDF-TrFE) capacitor to temperature

This section presents how the capacitance of a P(VDF-TrFE) capacitor changes upon application of temperature. No force was applied to the capacitor during this investigation to ensure that capacitance changes were due to temperature effects alone. Temperature experiments were performed using the setup described previously in section 3.5.3.

### 6.5.1 Poled capacitor

To determine whether humidity/moisture was affecting P(VDF-TrFE) capacitance during the measurements, three experiments were devised. The same capacitor was used in all three cases, and the experiments were performed several

days apart to let the capacitor recover back to its room temperature capacitance condition of ~ 875 pF. The following three temperature experiments were conducted:

1. Capacitance of P(VDF-TrFE) measured in vacuum (< $10^{-5}$ mBar) after storing the capacitor in roughing-pump vacuum for three days.
2. Capacitance of P(VDF-TrFE) measured in ambient air after storing the capacitor in roughing-pump vacuum for four days.
3. Capacitance of P(VDF-TrFE) measured in ambient air after storing the capacitor in ambient air for one week.

Figure 6.3 shows the change in capacitance as a function of P(VDF-TrFE) temperature between 15 to 47 °C, with the temperature being ramped up and down. Temperature was recorded using the Peltier element with a precision of +/- 0.1°C. In each case, the capacitor responds approximately linearly as a function of temperature with a small hysteresis present. Sensitivity defined as the change in capacitance per unit of temperature for all three experiments is presented in Table 6.1.

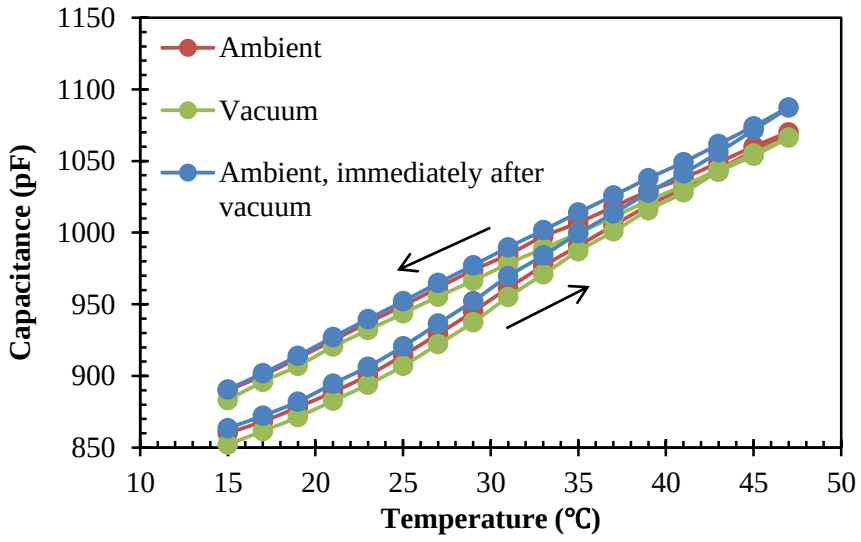



**Figure 6.3:** P(VDF-TrFE) capacitance as a function of ambient capacitor temperature from 15 to 47°C.

**Table 6.1:** Temperature sensitivity of P(VDF-TrFE) capacitor for various measurement conditions.

| Experiment | P(VDF-TrFE) Sensitivity (pF/°C) |
|---|---|
| 1) Vacuum only | 7.04 |
| 2) Ambient after vacuum | 7.22 |
| 3) Ambient only | 6.87 |

## 6.5.2 Depoled capacitor

To verify whether changes in P(VDF-TrFE) capacitance with temperature are affected by polarisation, the P(VDF-TrFE) capacitor presented in Section 6.5.1 was depoled to revert it from the ferroelectric state to a paraelectric one. The capacitor was heated at 125°C for 30 minutes and then connected to a charge amplifier to verify the disappearance of the ferroelectric state.

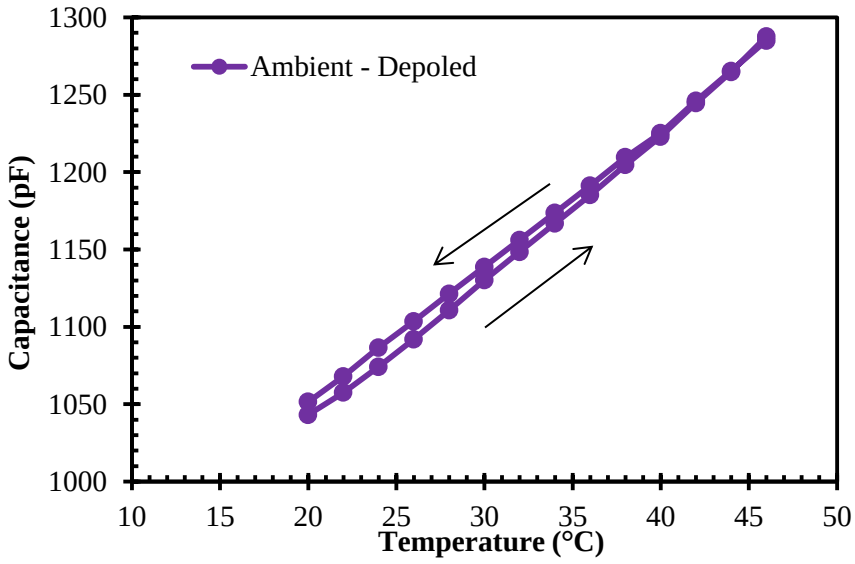



**Figure 6.4:** Capacitance of depoled P(VDF-TrFE) as a function of ambient sensor temperature from 20 to 46°C.

Figure 6.4 shows P(VDF-TrFE) capacitance as a function of applied temperature when conditions of experiment 3 in Section 6.5.1 are used. Temperature was applied to the capacitor in 2°C increments and the capacitance was extracted at 2 kHz after the temperature had stabilised. Again, up and down temperature ramps were recorded.

Similarly to the poled capacitor, the depoled one responds linearly to temperature with a sensitivity of 9.4 pF/°C. This value is higher than the sensitivity of ~ 6.9 pF/°C seen for the poled capacitor (see Table 6.1); however, its room temperature capacitance is also increased from ~ 900 pF to ~1050 pF after depoling.

## 6.6 Discussion

Before evaluating the capacitive response of P(VDF-TrFE) to force and temperature, current-voltage (I-V) and capacitance-voltage (C-V) measurements were performed. The ~2.5-µm-thick P(VDF-TrFE) film exhibited leakage current of 57.5 pA at 1 V. In the range from –5 to +5 V the P(VDF-TrFE) capacitance increased by ~3 pF, confirming that the poled P(VDF-TrFE) was indeed ferroelectric in nature.

P(VDF-TrFE) capacitance displays a logarithmic dependence on applied force over the range 0 N to ~ 9 N. Due to the logarithmic nature of the force dependence, sensitivity is significantly enhanced at the lower end of applied forces (< 0.5 N) compared with higher forces. Forces below 0.5 N show capacitance

sensitivity of ~ 7.1 pF/N, whereas a sensitivity of only ~ 0.26 pF/N can be seen for forces between 3 and 9 N. However, high force sensitivity is a critical feature at the lower range of applied forces since the majority of manipulative activities carried out by a humanoid robot during normal tasks would usually be less than 1 N [13].

On the contrary, ambient temperature causes P(VDF-TrFE) capacitance to vary approximately linearly over the range from 15 to 47°C. Sensitivity of poled P(VDF-TrFE) to temperature is ~7 pF/°C and is independent of measurement condition. The capacitance displays a small temperature-induced hysteresis that seems to depend of the history of P(VDF-TrFE). If the temperature of the capacitor is quickly ramped up and down several times in quick succession, the hysteresis is reduced. The lower hysteresis seen for the depoled P(VDF-TrFE) is likely a result of such ramping. The depoled, paraelectric P(VDF-TrFE) also exhibits higher room-temperature capacitance and a higher temperature sensitivity of 9.4 pF/°C. This may result from the annealing applied to P(VDF-TrFE), thereby changing its $\varepsilon_r$ to a higher value.

The changes in P(VDF-TrFE) capacitance with temperature are predominantly due to changes in relative permittivity $\varepsilon_r$. This is based on an assumption that the thermal expansion of P(VDF-TrFE) can be neglected. Since the P(VDF-TrFE) capacitor is firmly attached to the silicon substrate, it can only expand as much as the silicon. Upon application of temperature, P(VDF-TrFE) would predominantly expand in the *z* direction, since *x* and *y* are constrained by the rigid substrate. This would lead to an increase in the P(VDF-TrFE) thickness *d*. However, an increase in *d* would result in a lowering of capacitance with rising temperature,

contradicting the experimental observation. Consequently, the increase in capacitance with rising temperature must be associated with increasing $\varepsilon_r$.

The changes in P(VDF-TrFE) capacitance with force are more difficult to explain. The elastic compression of P(VDF-TrFE) under the probe and the resulting local reduction in the thickness *d* is negligible compared to the observed changes in the capacitance. Therefore, one would conclude that the material changes its properties under compressive force and this results in a slight increase in $\varepsilon_r$.

Finally, it is likely that the hysteresis in the capacitance with temperature is caused by the 'relaxation' of the polymer, i.e. the polymer structure may undergo minute changes with temperature. This hypothesis was verified by measuring the capacitance of a commercial PZT sensor as a function of temperature since the PZT crystalline lattice would not be prone to structural relaxation seen in polymers. Figure 6.5 shows the capacitance of a PZT parallel-plate capacitor as a function of temperature. No hysteresis is observed in this case.

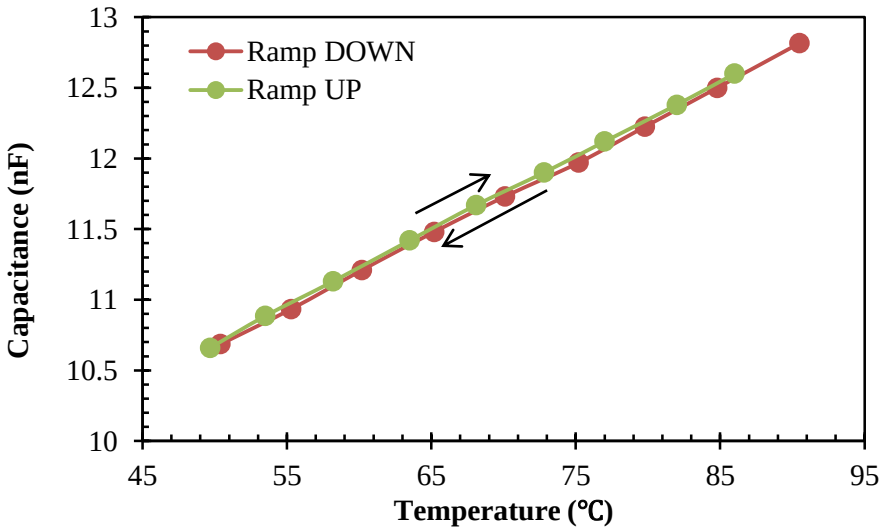



**Figure 6.5:** Capacitance of PZT parallel-plate capacitor as a function of ambient sensor temperature from ~ 50 to 90°C.

## 6.7 Summary

This chapter presents the response of a P(VDF-TrFE) capacitor to static compressive force and constant temperature by monitoring the changes in its capacitance. Compressive force applied in the normal direction to the capacitor led to a logarithmic increase in capacitance as a function of force rising from 0 to ~ 9 N. At the lower end of applied forces (< 0.5 N), the sensitivity is ~ 7.1 pF/N. The P(VDF-TrFE) capacitance was also measured as a function of temperature. To assess the influence of humidity, three experiments were devised using a combination of ambient and vacuum measurement and storage. For all three cases, the capacitor responded approximately linearly with sensitivities of ~ 7 pF/°C. Next, the P(VDF-TrFE) capacitor was thermally depoled to return it to paraelectric state and remove its pyroelectric effect. In this state, the capacitor continued to respond linearly to temperature producing a sensitivity of 9.4 pF/°C.

The change in P(VDF-TrFE) capacitance with temperature and small force is significant enough to allow the coupling of P(VDF-TrFE) capacitor with an organic transistor and thus develop sensors for static pressure and temperature. Such sensors would be compatible with large-area, low-cost manufacturing.

# Chapter 7

# P(VDF-TrFE)/OTFT sensor

Previously, chapter 3 described the methodology for fabricating the ferroelectric P(VDF-TrFE) capacitor and organic thin-film transistor. In this chapter, the P(VDF-TrFE) capacitor is connected to the gate of an OTFT with the aim to create a novel P(VDF-TrFE)/OTFT sensor and the response of such sensor to compressive force and temperature is studied. Section 7.1 introduces the P(VDF-TrFE)/OTFT sensor. The materials and sensor circuit fabrication procedure are briefly reviewed in Section 7.2. Response of the P(VDF-TrFE)/OTFT sensor circuit to force and temperature are shown in Sections 7.3 and 7.4 respectively. Finally, Sections 7.5 and 7.6 present discussion and summary respectively.

## 7.1 Introduction

Chapter 6 presented the response of the P(VDF-TrFE) ferroelectric capacitor to static force and constant temperature. It was shown that the change in sensor capacitance with force and temperature was in the region of pF's. To amplify the response of the sensor and produce a voltage output useful for subsequent interfacing with readout electronics, the ferroelectric capacitor can be connected to an organic thin-film transistor. By changing the capacitance of P(VDF-TrFE) through force or temperature stimuli, OTFT drain current and hence output voltage can be modulated, and this change in $I_D$ or $V_{OUT}$ can be studied as a function of force or temperature.

Previously, P(VDF-TrFE) has been integrated with a CMOS field-effect transistor and by exploiting the piezoelectric effect associated with P(VDF-TrFE), a piezoelectric oxide semiconductor field-effect transistor (POSFET) was created [13]. The POSFET can sense and process pressure signals in-situ. The POSFET is realised by carefully depositing the P(VDF-TrFE) layer directly onto the field-effect transistor gate and any charge developed on P(VDF-TrFE) through piezoelectricity modulates transistor drain current. To date, the POSFET has been primarily explored for monitoring dynamic normal force.

An organic charge modulated FET (OCMFET) featuring a floating gate with a PVDF-based piezoelectric polymer has been also demonstrated [118]. The transistor has a bottom-gate/bottom-contact structure and field effect mobility of ~ 0.028 $cm^2/Vs$. The floating gate of the transistor is connected to either the top or

bottom contact of the PVDF film. The device displays sensitivity ~ 2 mV/N and is able to detect forces as low as 20 mN at 500 Hz.

A wearable wireless pressure sensor based on a ZnO/PVDF hybrid film has been developed for heart rate monitoring [119]. ZnO/PVDF hybrid exhibits greater relative permittivity resulting in an enhanced piezoelectric coefficient for pressure sensing. In addition, Emamian et al [120] created a piezoelectric touch sensing device featuring screen-printed PVDF on a paper substrate. The device shows linear sensitivity of ~ 0.3 V/N over a compressive force range of 0.2 to 1.4 N. However, this device can only sense dynamic forces using the inherent piezoelectric effect within poled PVDF film.

This chapter presents a P(VDF-TrFE)/OTFT sensor in a POSFET-like configuration as shown previously in section 2.12. Such an approach could facilitate the use of organic electronics for large-area fabrication on flexible substrates to achieve the flexibility and potential stretch-ability required for a useful electronic skin, as well as providing the capability to monitor both force and temperature stimuli. The sensor couples the P(VDF-TrFE) capacitor to the gate of a low-voltage organic thin-film transistor. Upon application of static force or constant temperature the capacitance of the ferroelectric capacitor changes, modifying the accumulated charge in the channel of the transistor. This leads to a modulation in OTFT drain current that is converted to an output voltage monitored across a large (1 MΩ) resistor connected to ground.

## 7.2 Experimental details

The ferroelectric P(VDF-TrFE) capacitor and organic thin-film transistor were fabricated following the methodology described in Chapter 3. For testing purposes, the P(VDF-TrFE) capacitor was prepared on silicon wafer, and subsequently mounted onto a glass slide for compatibility with the force testing equipment. Al/$AlO_x$/$C_{18}$PA/DNTT/Au; Al/$AlO_x$/$C_{16}$PA/DNTT/Au and Al/$AlO_x$/DNTT/Au OTFTs were used for static force and constant temperature measurements. For dynamic temperature measurements, Al/$AlO_x$/$C_{14}$PA/DNTT/Au and Al/$AlO_x$/$C_{18}$PA/DNTT/Au transistors were used. All transistors had nominal channel lengths of ~ 30 µm and $W$ = 1000 µm. To complete the sensing circuit, the P(VDF-TrFE) capacitor was connected to the OTFT gate by gold wire. Depending on the experiment performed, the sensor's Al or Au electrode was connected to the gate. Previously, Figure 3.15 showed the schematic adopted for force sensing. Figure 7.1 shows the circuit diagram of the sensing circuit whereby the OTFT drain was biased at –2 V and $V_{IN}$ was chosen between 0 and –3 V. Transistor $V_{OUT}$ was measured in all cases.

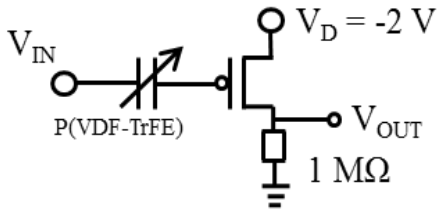



**Figure 7.1** Schematic of P(VDF-TrFE)/OTFT sensor.

## 7.3 Response of P(VDF-TrFE)/OTFT sensor to static force

This section presents results of different force experiments performed on the P(VDF-TrFE)/OTFT sensor circuit. In each instance, force was applied in a normal direction to the sensor's Au electrode which was connected to the OTFT gate. All force experiments were performed at room temperature.

### 7.3.1 Poled P(VDF-TrFE)/OTFT sensor

Force ranging from a few tenths of Newton to ~ 6.5 N was applied to the P(VDF-TrFE)/OTFT sensor using an input voltage of –1.5 V. $V_{OUT}$ was recorded for various forces and referenced to the value of $V_{OUT} = V_{REF}$ with no force applied. $\Delta V_{OUT} = |V_{OUT} - V_{REF}|$ was calculated and plotted as a function of force. Figure 7.2 shows a typical response when a static force of 0.74 N lasting ~ 7 s is repeatedly

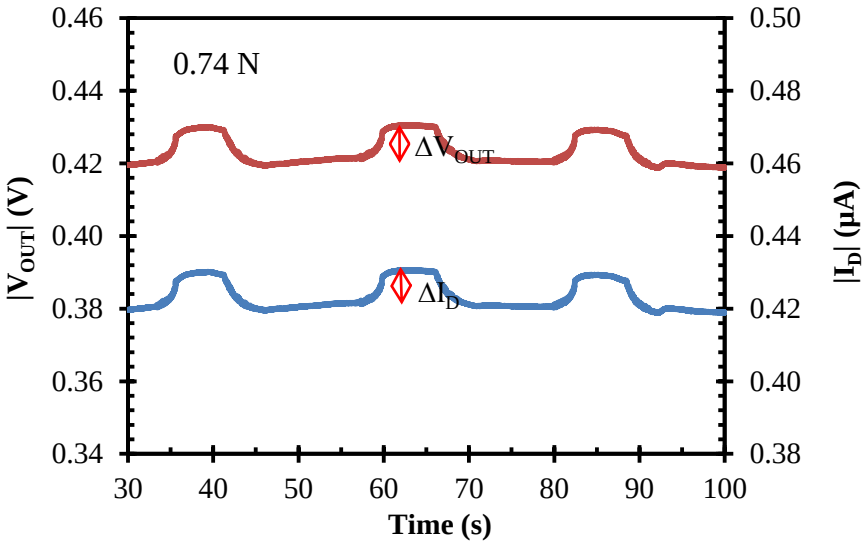



**Figure 7.2** Force of 0.74 N applied repeatedly to P(VDF-TrFE)/OTFT sensor. Graph shows OTFT $I_D$ and corresponding $V_{OUT}$.

applied to P(VDF-TrFE). The static force was applied across 40% of the sensor active area. Application of 0.74 N produces a change in $V_{OUT}$ of ~ 10 mV.

Forces from 0 to 6.5 N were applied to the sensor. For each force, the mean $|\Delta V_{OUT}|$ was extracted. Figure 7.3 shows that as applied force is increased from 0 to 6.5 N, $\Delta V_{OUT}$ increases logarithmically as a function of force. For very low forces, i.e. forces smaller than 0.1 N, the sensitivity of the circuit is high, ~ 66 mV/N. In the range between 0.1 and 1 N the sensitivity is reduced to ~ 3.9 mV/N.

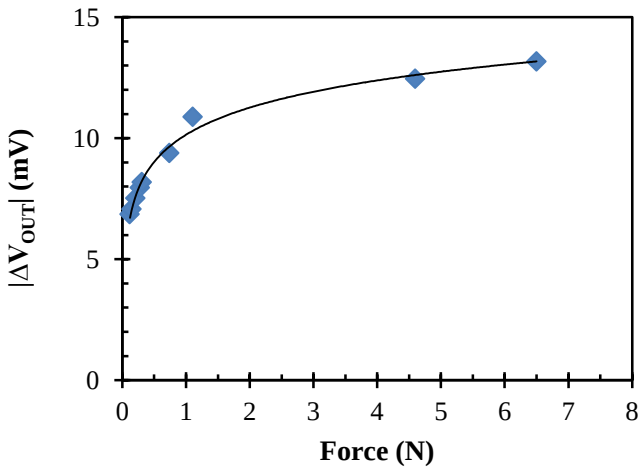



**Figure 7.3** $|V_{OUT}|$ as a function of applied force for P(VDF-TrFE)/OTFT sensor with $V_{IN}$ = –1.5 V. Force was applied to a poled P(VDF-TrFE).

### 7.3.2 Depoled P(VDF-TrFE)/OTFT sensor

To ensure that the effect of static force on the P(VDF-TrFE)/OTFT sensor was a result of capacitive changes alone, the P(VDF-TrFE) capacitor was thermally depoled at 125°C for 30 minutes to change its state from ferroelectric to paraelectric and thus eliminate its piezoelectric properties. The disappearance of the ferroelectric

phase was verified by both use of a charge amplifier and the measurement of a capacitance/voltage curve whereby capacitance did not display a dependence on voltage. A similar experiment to that shown in Figure 7.3 was performed on the depoled P(VDF-TrFE)/OTFT sensor. Compressive force of up to ~ 8 N was applied and $\Delta V_{OUT}$ was extracted and plotted as a function of force.

Figure 7.4 shows that similarly to the poled P(VDF-TrFE) capacitor, $\Delta V_{OUT}$ of the depoled P(VDF-TrFE)/OTFT sensor increases logarithmically as a function of force, confirming that $\Delta V_{OUT}$ does not result from the piezoelectric effect. As seen in Figures 7.3 and 7.4, the logarithmic sensor response means that the sensitivity of the sensor circuit decreases with the increasing force, resulting in high sensitivity for pressures below 0.1 N. Comparing Figures 7.3 and 7.4 one would notice that $\Delta V_{OUT}$ is smaller for the latter. This is caused by using a different transistor for each experiment. Data in Figure 7.4 were obtained with an OTFT that had mobility about 50% smaller than that of the OTFT used in Figure 7.3, resulting in smaller $\Delta V_{OUT}$.

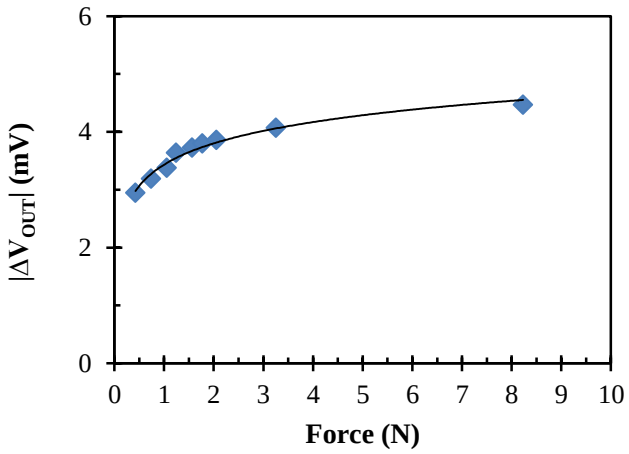



**Figure 7.4** $|V_{OUT}|$ as a function of applied force for P(VDF-TrFE)/OTFT sensor with $V_{IN}$ = –1.5 V. Force was applied to depoled P(VDF-TrFE) in its paraelectric state.

## 7.4 Response of P(VDF-TrFE)/OTFT sensor to static temperature

This section presents results of temperature experiments performed on P(VDF-TrFE)/OTFT sensor. In all cases, the OTFT was held at room temperature.

### 7.4.1 Poled P(VDF-TrFE)/OTFT sensor with DC input voltage

Figure 7.5 presents the effect of static temperature on a poled P(VDF-TrFE)/OTFT sensor. The capacitor's Al electrode was connected to the transistor gate. The temperature of the P(VDF-TrFE) capacitor was varied from 20 to 25°C in 1°C increments. Each temperature was held constant for ~ 1 hour. After waiting for 1 hour at the final temperature (25°C), the temperature was returned to 20°C in one step. Figures 7.5 (a) and (b) show $V_G$ and $|V_{OUT}|$ as a function of time respectively, along with the associated sensor temperature profile.

For the data shown in Figure 7.5, $V_{IN}$ is fixed and $V_G$ represents the voltage at the point where the P(VDF-TrFE) capacitor connects to the gate of the transistor, i.e. the voltage on the gate of the transistor. Figure 7.5 (a) shows that $V_G$ increases with the increasing temperature and remains constant if the temperature does not change. When the temperature set point is changed, it takes about 5 minutes for the temperature to stabilise. The stabilisation of the gate voltage takes longer and the duration depends on the temperature change. Once stabilised, $V_G$ remains constant until the next temperature change occurs.

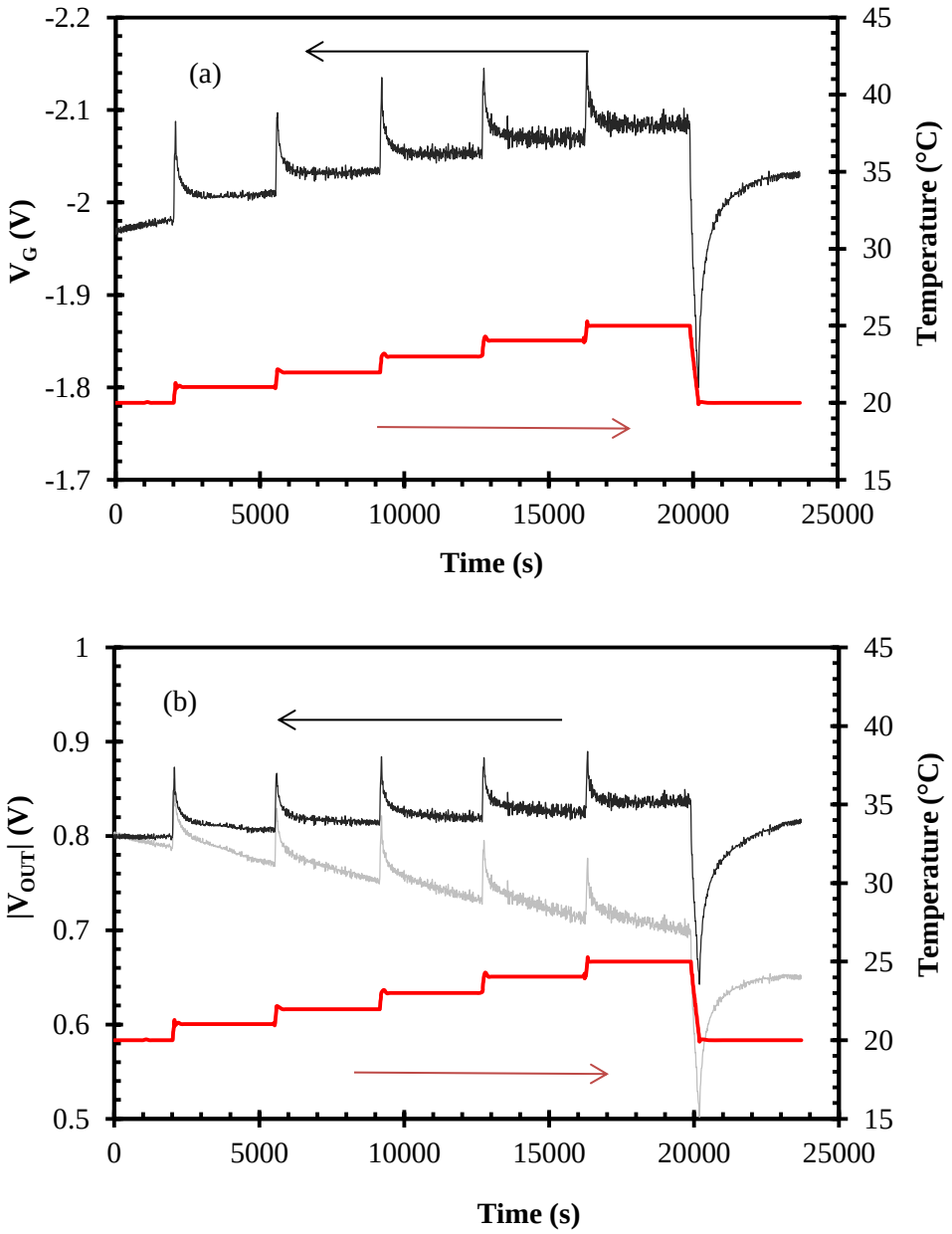



**Figure 7.5** $V_G$ (a) and $|V_{OUT}|$ (b) of P(VDF-TrFE)/OTFT sensor as a function of P(VDF-TrFE) temperature. The grey curve shows the measured $V_{OUT}$ data whereas the black curve shows $V_{OUT}$ compensated for the transistor bias stress effect.

Across the 5°C temperature range, $V_G$ responds linearly to sensor temperature with a sensitivity of ~ 20.5 mV/°C. However, over extended time periods, transistor $I_D$ gradually reduces due to the transistor bias stress effect, leading to a decrease in $|V_{OUT}|$. This can be inferred from the grey curve shown in Figure 7.5 (b). If one

compensates for the bias stress effect, $|V_{OUT}|$ can be levelled (see the black curve in Figure 7.5 (b)) and a change in the output voltage with temperature becomes apparent. This black curve was then used to extract the mean $|V_{OUT}|$ for temperatures between 20 to 25°C and the result is shown in Figure 7.6. A linear dependence between $|V_{OUT}|$ and P(VDF-TrFE) temperature is observed and $|V_{OUT}|$ displays a temperature sensitivity of 6.8 mV/°C. Previously in Chapter 6, an approximately linear dependence between the P(VDF-TrFE) capacitance and temperature was seen.

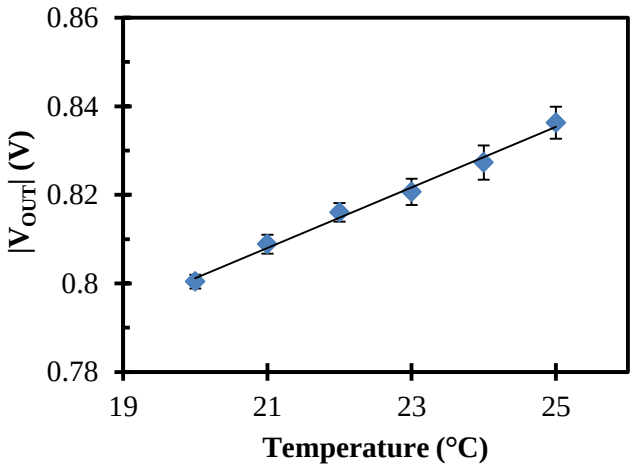



**Figure 7.6** P(VDF-TrFE)/OTFT sensor mean $|V_{OUT}|$ as a function of P(VDF-TrFE) temperature between 20 and 25°C.

Since the bias-stress effect of the organic thin-film transistor affects the output voltage of the P(VDF-TrFE)/OTFT sensor, the next section discusses the performance of the sensor when a pulsed voltage is applied at the input. Since the 'static' temperature is not expected to undergo sudden changes, infrequent sampling with voltage pulses would provide a temperature reading while substantially reducing the bias-stress effect in the organic transistor.

### 7.4.2 Poled P(VDF-TrFE)/OTFT sensor with pulsed input voltage

Using a voltage pulse at the input of the sensor would provide a temperature reading upon request while minimising the bias-stress effect in the organic transistor. A similar experiment to that shown previously in Figure 7.5 was conducted to investigate this approach. As before, the OTFT was held at room temperature whereas the P(VDF-TrFE) capacitor temperature was raised in 1°C increments between 20 to 25°C. Temperature was allowed to stabilise at each set temperature before conducting measurements.

The circuit adopted in Figure 7.1 was used, with $V_D$ = –2 V and $V_{IN}$ an AC pulse from 0 to –3 V with a period of 10 seconds and a 50% duty cycle. The pulse included a –2 V pre-bias for 3 seconds before ramping to –3 V. Figure 7.7 shows the input voltage pulse used. The temperature of the sensor was ramped down from 25 to 20°C and then up again. $|V_{OUT}|$ was extracted at $V_{IN}$ = –3 V for each temperature.

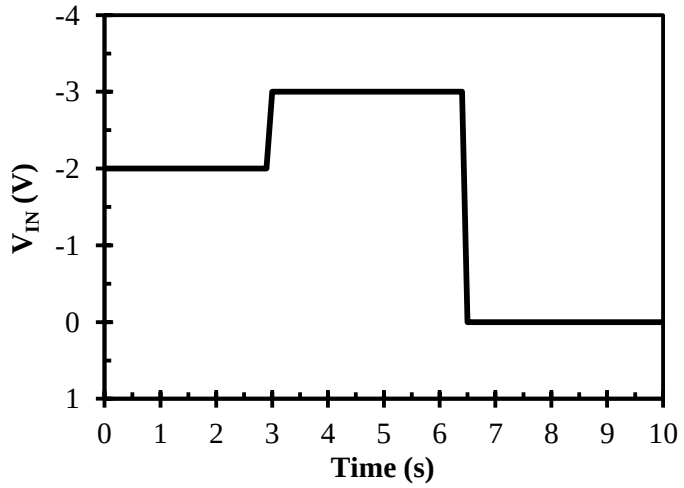



**Figure 7.7** $V_{IN}$ for P(VDF-TrFE)/OTFT sensor with pulsed input voltage.

Figure 7.8 shows the effect of temperature on the P(VDF-TrFE)/OTFT sensor with a pulsed input voltage and temperatures between 25 to 20°C. $|V_{OUT}|$ for the temperature increasing from 20 to 25°C is shown in Figure 7.9 for comparison. $|V_{OUT}|$ was extracted as a function of temperature for both down and up temperature ramps and is shown in Figure 7.10.

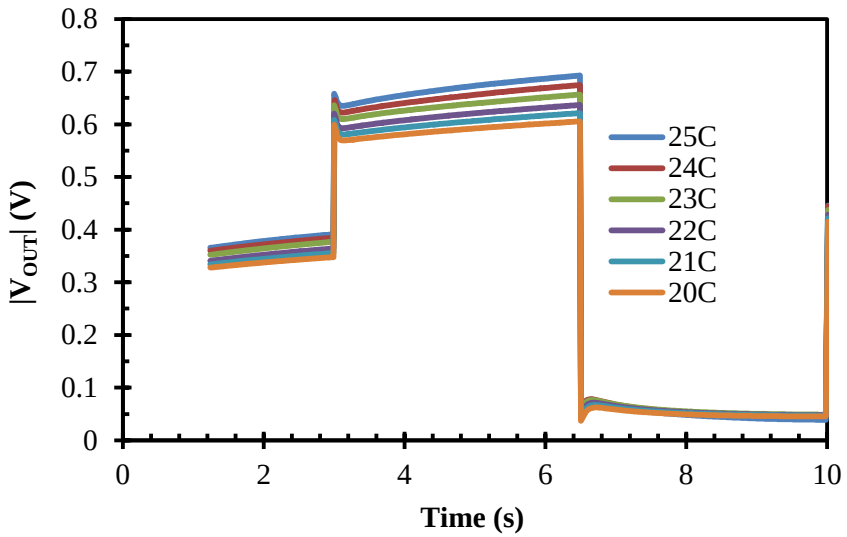



**Figure 7.8** $|V_{OUT}|$ for P(VDF-TrFE)/OTFT sensor as a function of temperature from 25 to 20°C with pulsed $V_{IN}$.

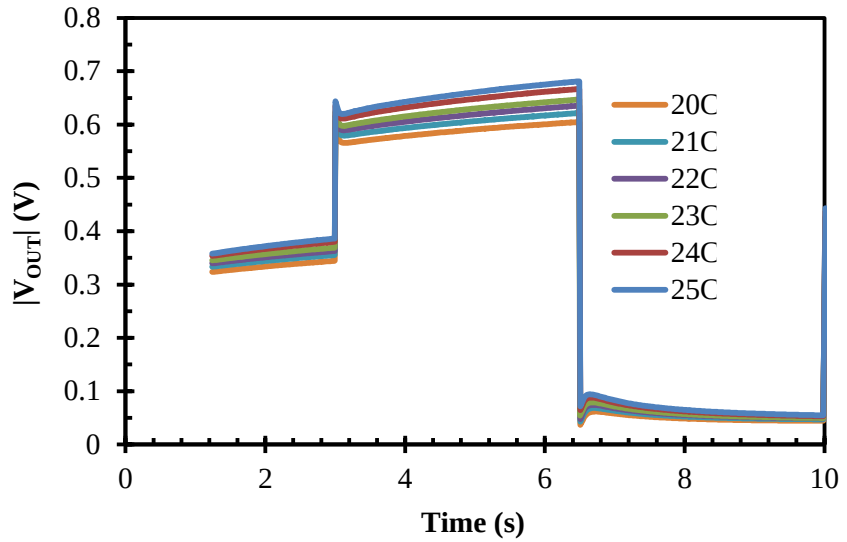



**Figure 7.9** $|V_{OUT}|$ for P(VDF-TrFE)/OTFT sensor as a function of temperature from 20 to 25°C with pulsed $V_{IN}$.

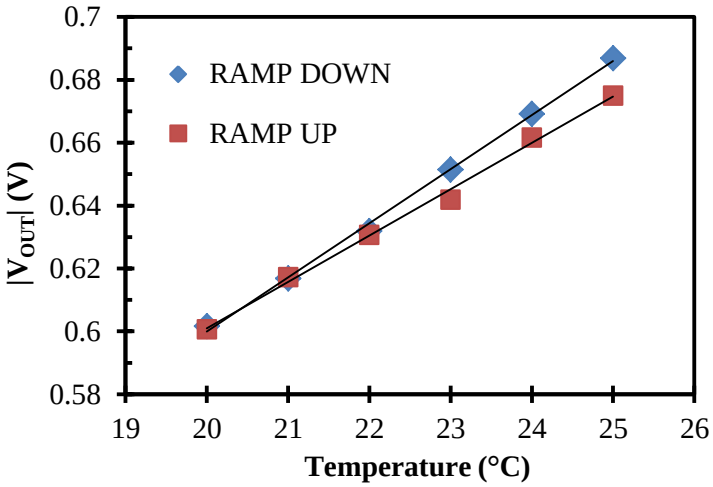



**Figure 7.10** $|V_{OUT}|$ of P(VDF-TrFE)/OTFT sensor as a function of temperature from 20 to 25°C, extracted from Figures 7.8 and 7.9. The temperature was first ramped from 25 to 20°C and then back to 25°C.

$|V_{OUT}|$ increases approximately linearly with temperature between 20 to 25°C. This relationship is in agreement with the results recorded previously for a DC input voltage. $|V_{OUT}|$ displays a sensitivity of ~ 15 mV/°C (20 to 25°C). The small hysteresis is most likely a result of the hysteresis measured for the P(VDF-TrFE) capacitance.

### 7.4.3 Depoled P(VDF-TrFE)/OTFT sensor with DC input voltage

A similar experiment to that shown in Figure 7.5 was conducted on a depoled P(VDF-TrFE)/OTFT sensor. Figures 7.11 and 7.12 present the response of a depoled P(VDF-TrFE)/OTFT sensor to static temperature using a DC input voltage. The P(VDF-TrFE) capacitor was depoled thermally at 125°C for 30 minutes and afterwards connected to a charge amplifier to ensure removal of the ferroelectric

state. The Al electrode of the sensor was connected to the transistor gate. The temperature of the P(VDF-TrFE) capacitor was again varied from 20 to 25°C in 1°C increments. Each temperature was held constant for ~ 1 hour. After waiting for 1 hour at 25°C, the temperature was returned to 20°C in one step. Figure 7.11 (a) and (b) show $V_G$, $|V_{OUT}|$ and temperature as functions of time.

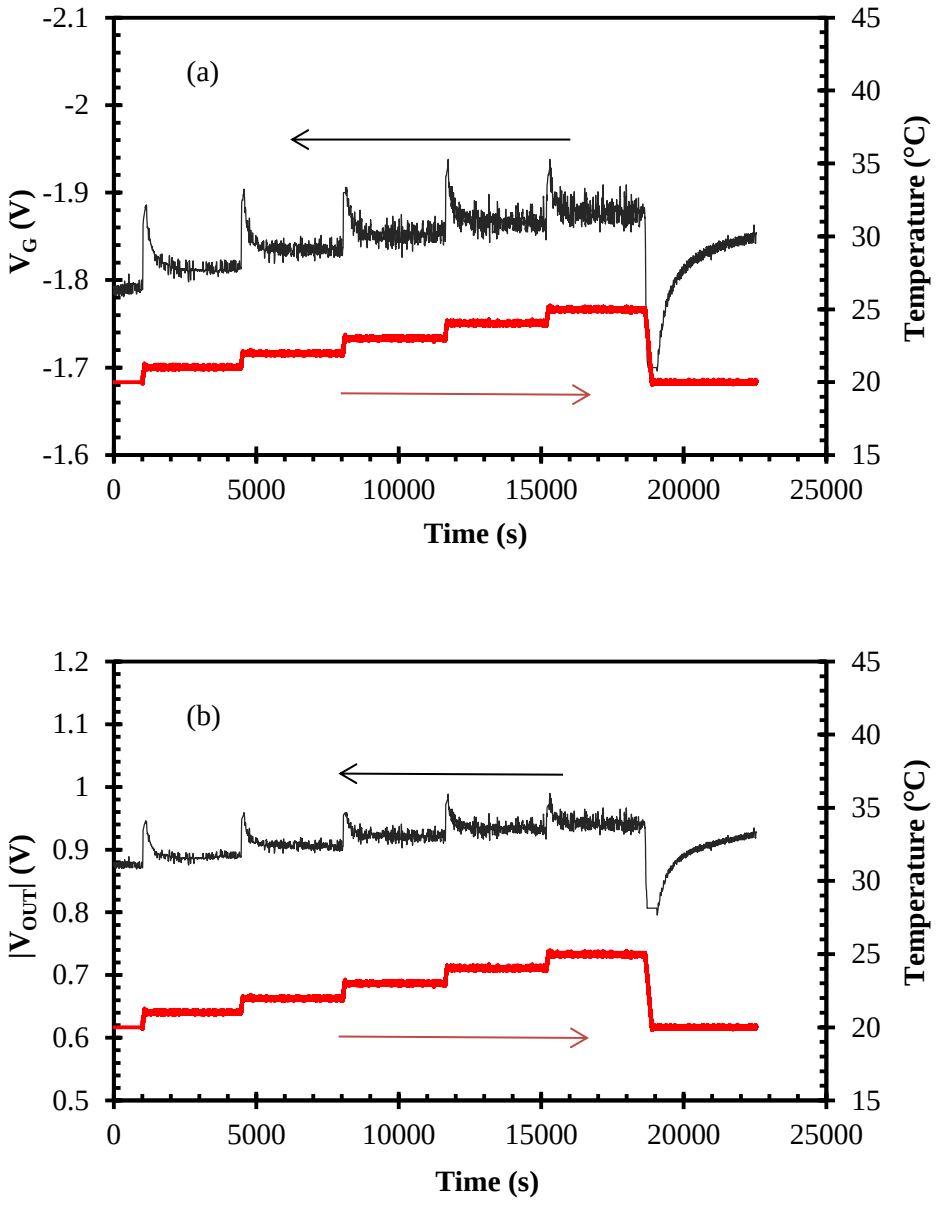



**Figure 7.11** $V_G$ (a) and $|V_{OUT}|$ (b) of depoled P(VDF-TrFE)/OTFT sensor as a function of P(VDF-TrFE) temperature The curve in (b) shows $V_{OUT}$ compensated for the transistor bias stress effect.

Similarly to the poled P(VDF-TrFE), Figure 7.11 shows that $V_G$ increases with the increasing temperature and remains constant if the temperature does not change. Once stabilised, $V_G$ remains constant until the next temperature change occurs. Across the 5°C temperature range, $V_G$ responds linearly to sensor temperature with a sensitivity of ~ 17.3 mV/°C. Figure 11 (b) shows $|V_{OUT}|$ when the OTFT bias stress effect is compensated for. This curve was then used to extract the mean $|V_{OUT}|$ for temperatures between 20 to 25°C and the result is shown in Figure 7.12. $|V_{OUT}|$ displays a linear dependence on P(VDF-TrFE) temperature with a sensitivity of 13.7 mV/°C.

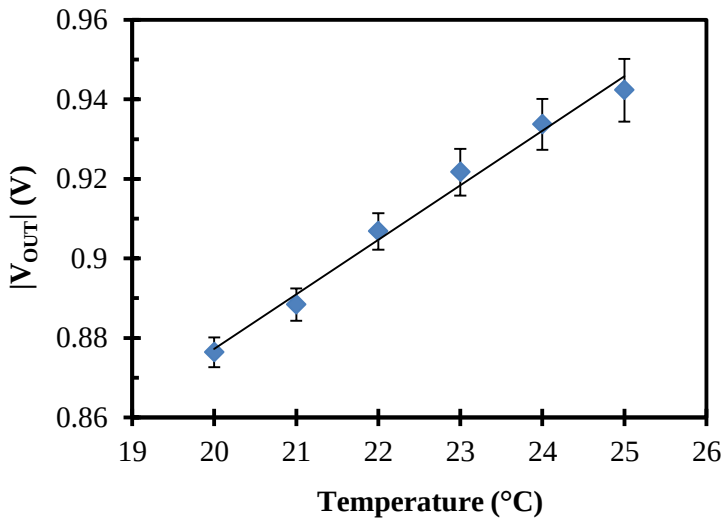



**Figure 7.12** Depoled P(VDF-TrFE)/OTFT sensor mean $|V_{OUT}|$ as a function of P(VDF-TrFE) temperature between 20 and 25°C.

## 7.4.4 Depoled P(VDF-TrFE)/OTFT sensor with pulsed input voltage

To obtain a temperature reading on request and to reduce the organic transistor bias stress effect, a similar experiment to that discussed in Section 7.4.2

was conducted for the depoled P(VDF-TrFE)/OTFT sensor. Figures 7.13 and 7.14 present the response of a depoled P(VDF-TrFE)/OTFT sensor to static temperature using a pulsed input voltage. The P(VDF-TrFE) capacitor was depoled thermally at 125°C for 30 minutes and connected to a charge amplifier to ensure the removal of the ferroelectric state. The Al electrode of the sensor was attached to the transistor gate, with $V_D$ = –2 V and $V_{IN}$ an AC pulse from 0 to –1.5 V with a period of 10 seconds and a 50% duty cycle. The pulse included a –1 V pre-bias for 3 seconds before ramping to –1.5 V. Similarly to the experiment performed on the poled P(VDF-TrFE), the temperature was varied from 20 to 25°C in 1°C increments. $|V_{OUT}|$ was extracted at $V_{IN}$ = –1.5 V for each temperature in the 5°C range, the results of which are shown in Figure 7.15.

$|V_{OUT}|$ shows an approximate linear dependence with temperature between 20 to 25°C. This agrees with results shown previously (Figure 7.10) using P(VDF-TrFE) in its poled condition. $|V_{OUT}|$ displays a sensitivity of ~ 3.8 mV/°C for the temperature ramp from 20 to 25°C.

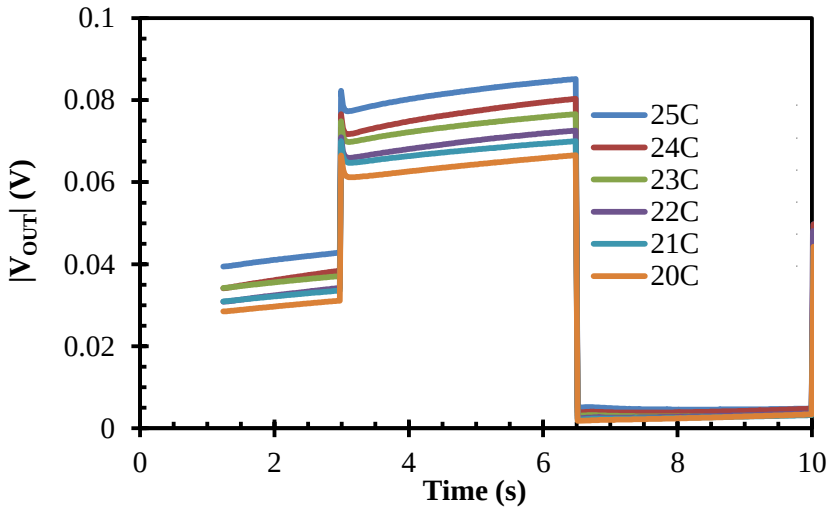



**Figure 7.13** $|V_{OUT}|$ for depoled P(VDF-TrFE)/OTFT sensor as a function of temperature from 25 to 20°C with pulsed $V_{IN}$.

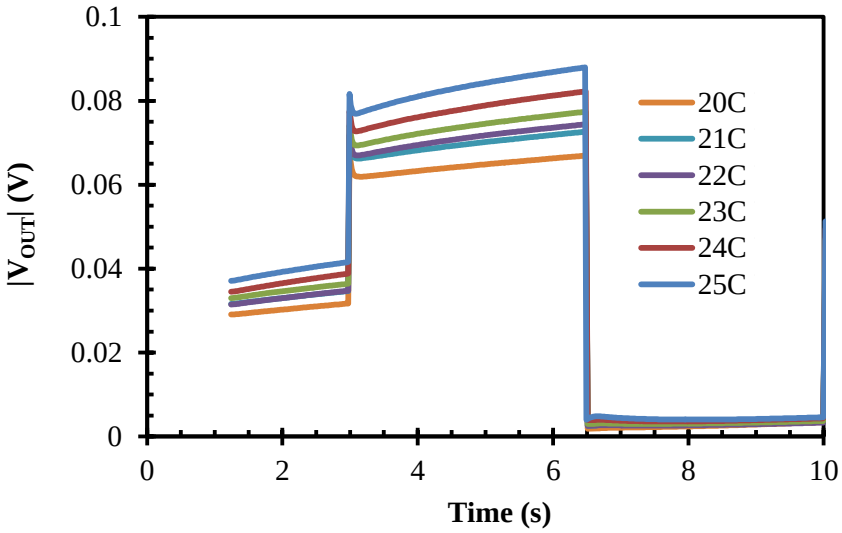



**Figure 7.14** $|V_{OUT}|$ for depoled P(VDF-TrFE)/OTFT sensor as a function of temperature from 20 to 25°C with pulsed $V_{IN}$.

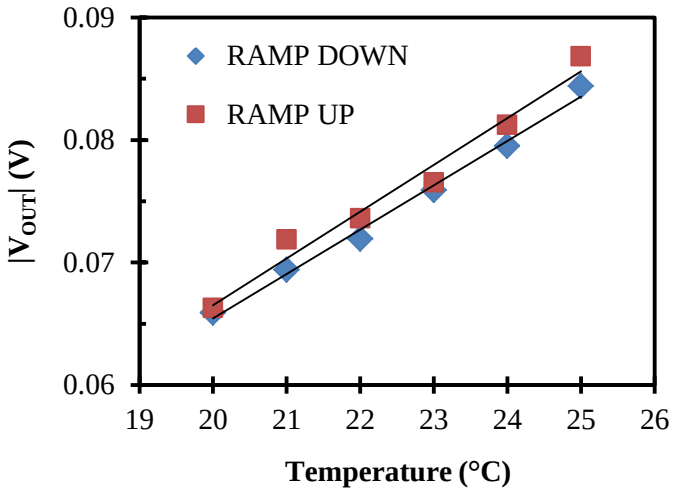



**Figure 7.15** $|V_{OUT}|$ of depoled P(VDF-TrFE)/OTFT sensor as a function of temperature from 20 to 25°C, extracted from Figures 7.13 and 7.14. The temperature was first ramped from 25 to 20°C and then back to 25°C.

### 7.4.5 Response of poled P(VDF-TrFE)/OTFT sensor with DC input voltage to dynamic temperature

This section presents the dynamic temperature response of the P(VDF-TrFE)/OTFT sensor. P(VDF-TrFE) has been poled, i.e. in ferroelectric state, and therefore possessing pyroelectric properties. Similarly to the static temperature investigation, the sensor temperature was varied and $V_{OUT}$ was monitored. Although the sensor temperature was ramped at 0.25°C/s, the PID controller needed about 80 seconds to stabilise the temperature. During that time the temperature was oscillating above and below the upper set value. After the upper temperature value had stabilised, the temperature was ramped down to 20°C. The peak output voltage for each temperature ramp (e.g. 20°C → 25°C → 20°C) was recorded. Here the peak voltage resulted from the combined pyroelectric effect and capacitive changes of P(VDF-TrFE). Five experiments were performed. In each instance, the transistor was kept at room temperature and the temperature of P(VDF-TrFE) was varied from 20 to (20+x)°C and back to 20°C, where x = 2, 3, 4, 5 and 6°C. At each (20+x)°C temperature, the peak transistor output voltage was measured.

Figure 7.16 (a) shows the effect of a 5°C temperature ramp on $|V_{OUT}|$ for both up and down temperature ramps. $|V_{OUT}|$ follows the changes in sensor temperature as set by the controller in real-time. The $|V_{OUT}|$ peak value of ~ 500 mV occurring about 20 seconds after the temperature ramp has started is largely due to the pyroelectric effect. After the temperature has stabilised at 25°C, the voltage magnitude of 385 mV results from the capacitive effect. The opposite behaviour is observed when the temperature is decreased. The graph in Figure 7.16 (b) shows the effect of different temperature increments on $|V_{OUT}|$. $V_{IN}$ was held at –2 V throughout. The sensor responds linearly to P(VDF-TrFE) temperature, with a sensitivity of ~ 34 mV/°C for the peak output voltage.

Figures 7.17 (a) and (b) show a dynamic temperature ramp between 20 to 30°C performed on both a poled and depoled P(VDF-TrFE)/OTFT sensor. The purpose of the experiment was to determine the contribution the pyroelectric effect has to the voltage response, since the depoled sensor does not display pyroelectricity. In each case, sensor temperature was ramped quickly up and down without stabilising. OTFT $|V_{OUT}|$ was monitored in real time for $V_{IN} = V_D = -2$ V.

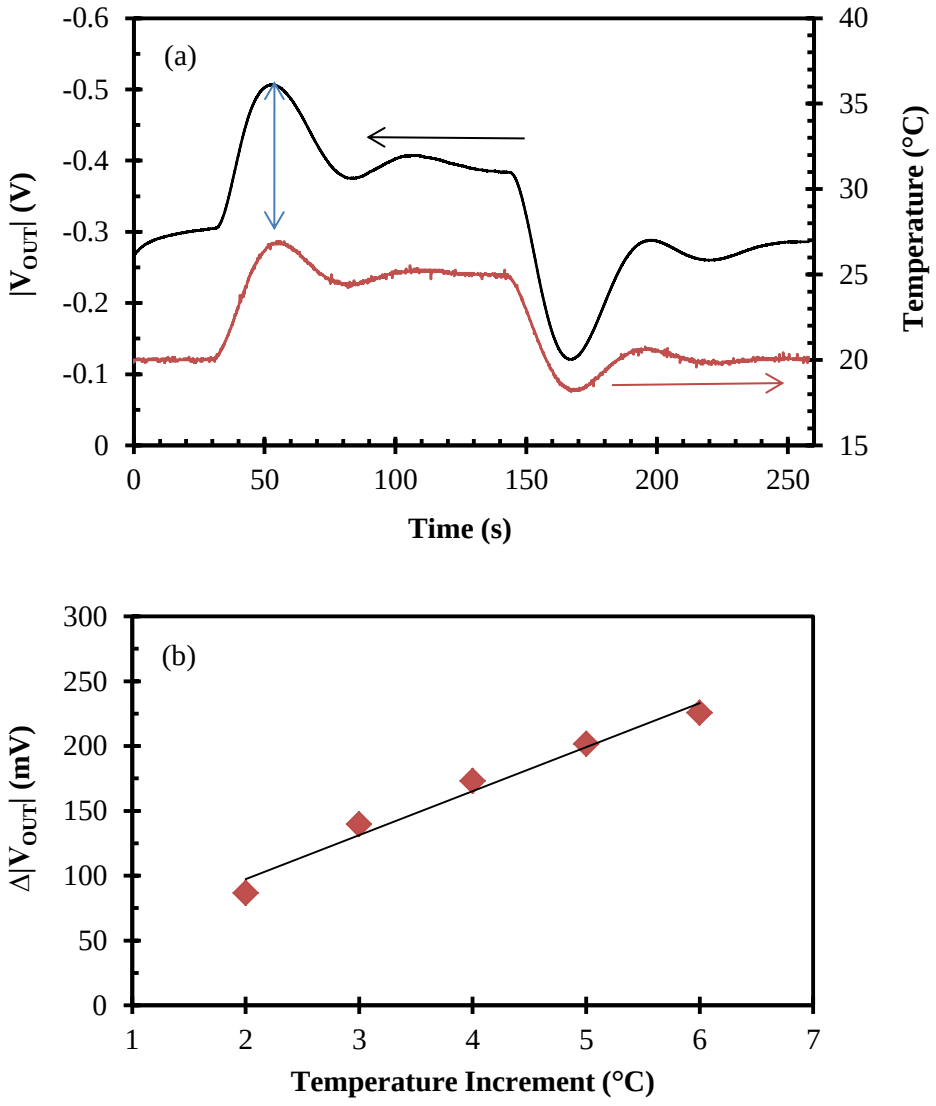



**Figure 7.16** $|V_{OUT}|$ for 20 to 25 to 20°C (a) and $\Delta|V_{OUT}|$ (b) for P(VDF-TrFE)/OTFT sensor as a function of temperature.

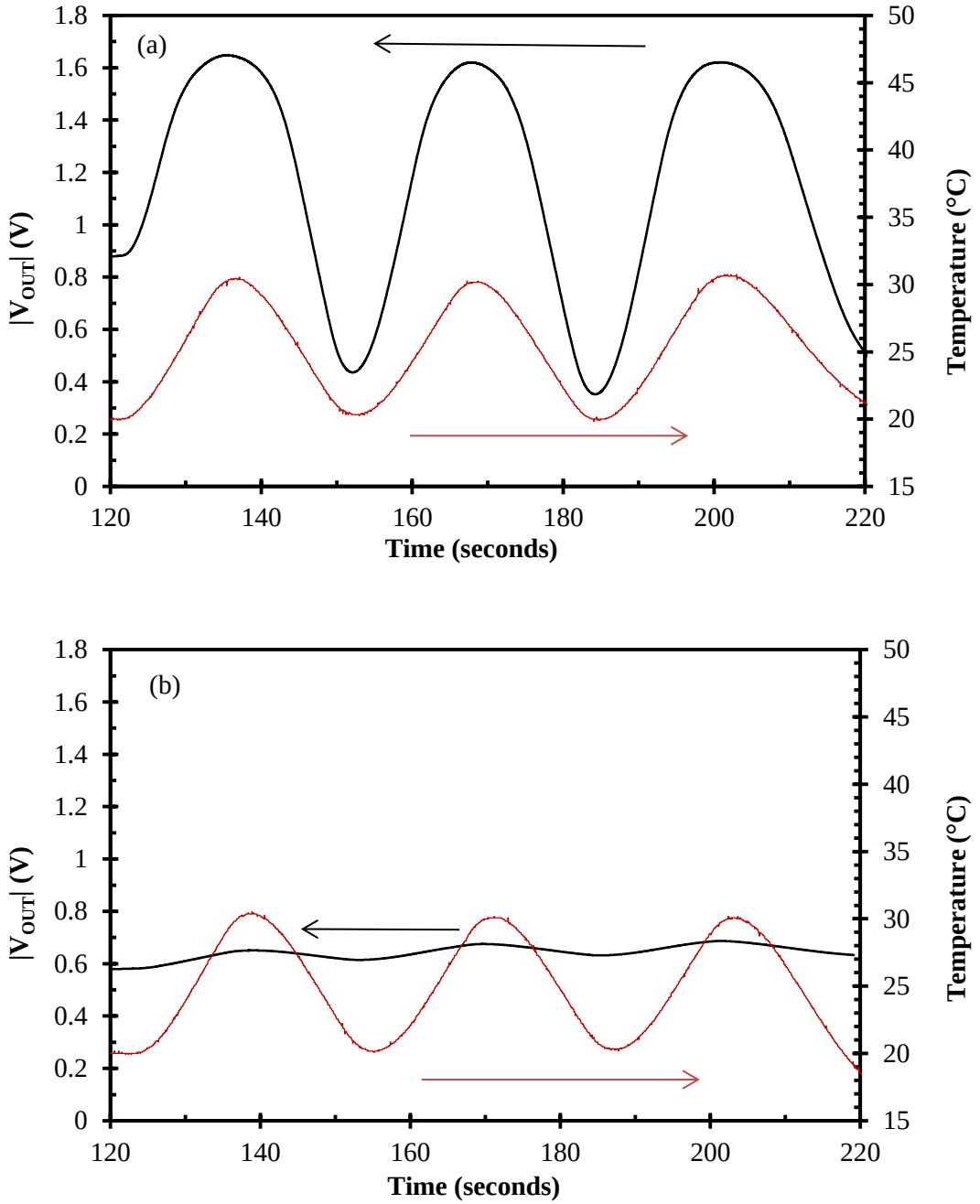



**Figure 7.17** Change in $|V_{OUT}|$ of P(VDF-TrFE)/OTFT sensor for temperature variations between 20 and 30°C for poled (a) and depoled (b) P(VDF-TrFE). $V_{IN} = V_D = -2$ V.

From the graphs in Figure 7.17 it is clear that the response of the poled P(VDF-TrFE) sensor to temperature is much stronger than the one for depoled

P(VDF-TrFE), where only sensor capacitance plays a role in modulating $V_{OUT}$. For the poled P(VDF-TrFE), $|V_{OUT}|$ increases by ~ 1.2 V when the temperature is raised from 20 to 30°C at a rate of 1°C/s, compared with ~ 60 mV increase for the depoled P(VDF-TrFE) when only the capacitive changes have an effect. This 60 mV increase leads to a sensitivity of 6 mV/°C; a value similar to that reported in Section 7.4.3.

## 7.5 Discussion

Figure 7.12 shows a typical response when a force of 0.74 N lasting ~ 7 seconds is applied three times to P(VDF-TrFE). Each time the force is applied, $\Delta V_{OUT}$ from the sensor shows the same change, indicating that the sensor is capable of displaying repeatable behaviour. Due to the nature of the force application, the sensor output voltage follows changes in force in real time. It takes around 2 s for the force to stabilise at 0.74 N from the 0 N steady-state condition due to the speed of the probe impacting the P(VDF-TrFE) capacitor. Similarly, when the probe is retracted, it takes around 2 s to completely pull away from the surface, and this gradual decline in force applied to the capacitor is represented by the fall in output voltage in a ramp-like manner. Referring to Figures 7.3 and 7.4 for the poled and depoled P(VDF-TrFE) respectively, the P(VDF-TrFE)/OTFT sensor displays a logarithmic dependence on applied compressive force (0 to ~ 8 N) regardless of whether P(VDF-TrFE) is in the ferroelectric or paraelectric state. The logarithmic behaviour of $|V_{OUT}|$ as a function of force shows the same dependency as sensor capacitance with force as shown previously in Chapter 6 (see Figure 6.1). Table 7.1 provides a summary of

OTFT parameters such as threshold voltage ($V_t$) and field-effect mobility ($\mu$) measured as part of the two static force experiments. Based on Table 7.1 the response of the sensor to applied force is logarithmic regardless of the initial $V_t$ and $\mu$ of the transistor and the changes they undergo as a result of the bias stress. OTFT stability is greatest in terms of $V_t$ and $\mu$ shift for the OTFT featuring $AlO_x/C_{18}PA$ dielectric which agrees with results previously seen in Chapter 4. In addition, the larger the $|V_{IN}|$, the larger the value of $|V_G|$ which appears on the OTFT gate.

**Table 7.1:** Summary of OTFT characteristics for P(VDF-TrFE)/OTFT sensor static force measurements.

| | **Poled Sensor** | **Depoled Sensor** |
|---|---|---|
| **OTFT** | $AlO_x/C_{18}PA/DNTT/Au$ | $AlO_x/C_{16}PA/DNTT/Au$ |
| **Response to force** | Logarithmic | Logarithmic |
| **$V_t$ initial (V)** | –0.52 | –0.68 |
| **$V_t$ final (V)** | –0.2 | –0.21 |
| **$\mu$ initial ($cm^2/Vs$)** | 0.56 | 0.30 |
| **$\mu$ final ($cm^2/Vs$)** | 0.61 | 0.38 |

Previously, ferroelectret transducers based on polypropylene films have been integrated with amorphous silicon FETs using a lamination technique to capacitively couple the piezoelectric charge produced by the ferroelectret to the transistor gate [121]. In the capacitive-sensing mode, the voltage divider network showed a change in $|V_{OUT}|$ of ~ 20 mV for a static pressure of 16 kPa applied to the ferroelectret.

Despite the logarithmic capacitive response seen as a function of applied force, the P(VDF-TrFE)/OTFT sensor could be improved. This could be achieved through use of a higher-$\mu$ OTFT, so that changes in $I_D$ with force would be amplified.

The change in OTFT $V_G$ and sensor $|V_{OUT}|$ as functions of time for changing P(VDF-TrFE) temperature for poled and depoled P(VDF-TrFE)/OTFT sensors are shown in Figures 7.5 and 7.11 respectively. The experiments were performed on P(VDF-TrFE) in ferroelectric and paraelectric states to confirm that changes in $V_G$ and $V_{OUT}$ as a function of temperature were resulting from P(VDF-TrFE) capacitance.

$V_G$ stabilises at each set temperature and remains stable for the 60-minute period, whereas $|V_{OUT}|$ gradually decreases. This shift in $|V_{OUT}|$ with time is associated with a shift in OTFT characteristics under a prolonged bias. Thin-film transistors are well known to change their performance under the extended application of bias, usually manifesting itself as a change in transistor threshold voltage [122]. An increase in $|V_t|$ for a fixed $V_G$ would lead to a decrease in $I_D$. Consequently, more stable transistors would be desired. However, $I_D$ of our P(VDF-TrFE)/OTFT sensor exhibits a power law decrease with time and the measured data can be compensated for this drift. By doing so, $|V_{OUT}|$ shows a sensitivity of 6.8 mV/°C in the temperature range from 20 to 25°C for the poled P(VDF-TrFE) and 13.7 mV/°C for the depoled P(VDF-TrFE). In this case, the depoled P(VDF-TrFE)/OTFT sensor shows greater temperature sensitivity due to using an OTFT with a marginally higher mobility (see Table 7.2). Similarly to the force experiment, if a higher field-effect mobility transistor were to be used, temperature sensitivity would improve.

Table 7.2 provides a summary of OTFT parameters such as threshold voltage ($V_t$) and field-effect mobility ($\mu$) measured as part of the temperature experiments for both poled and depoled P(VDF-TrFE) using DC and pulsed input voltages.

**Table 7.2:** Summary of OTFT characteristics for P(VDF-TrFE)/OTFT sensor temperature measurements.

| | **Poled P(VDF-TrFE)** | | **Depoled P(VDF-TrFE)** | |
|---|---|---|---|---|
| | DC $V_{IN}$ | Pulsed $V_{IN}$ | DC $V_{IN}$ | Pulsed $V_{IN}$ |
| **OTFT** | $AlO_x/C_{14}PA$/ DNTT/Au | $AlO_x$/DNTT/Au | $AlO_x/C_{18}PA$/ DNTT/Au | $AlO_x/C_{16}PA$/ DNTT/Au |
| **Response to temperature** | Linear | Linear | Linear | Linear |
| **Sensitivity (mV/°C)** | 6.8 | 15.0 | 13.7 | 3.8 |
| **$V_t$ initial (V)** | –0.54 | –0.19 | –0.3 | –0.21 |
| **$V_t$ final (V)** | –0.81 | –0.18 | –0.19 | –0.14 |
| **$\mu$ initial ($cm^2$/Vs)** | 0.37 | 0.14 | 0.50 | 0.02 |
| **$\mu$ final ($cm^2$/Vs)** | 0.20 | 0.13 | 0.67 | 0.03 |

Regarding Table 7.2, the response of the sensor to applied temperature is linear regardless of the initial $V_t$ and $\mu$ of the transistor and their shift under prolonged bias. A linear dependence of $|V_{OUT}|$ as a function of temperature is not unexpected since the capacitance of the sensor alone displays linear behaviour as a function of applied temperature (see Figure 6.2). The differences in $V_t$ and $\mu$ between the transistors account for the differences seen in sensor sensitivity. In addition, the applied $|V_{IN}|$ controls the value of $|V_G|$ which appears on the OTFT gate. One can also notice that the pulsed $V_{IN}$ substantially decreases the transistor bias stress effect and would be preferred in the future.

As seen in section 6.5, the capacitance of P(VDF-TrFE) polymer increases with increasing temperature as a result of rising $\varepsilon_r$. For the data of Figure 7.5, the voltage $V_{DS}$ applied across the drain/source is approximately equal to the voltage $V_{GS}$ applied across gate/source, leading to the transistor operating in saturation regime.

After compensating for the bias stress the increase in $|V_{OUT}|$ with rising temperature results from an increased drain current of the transistor. The primary reason for that is an increase in $|V_G|$ with rising temperature, as seen in Figure 7.5 (a). In addition, Equation 2.14 suggests that a decrease in $|V_t|$ over time would lead to an increased drain current. The latter is unlikely, because the initial value of the threshold voltage was –0.54 V and the final value was higher at –0.81 V. Consequently, this points to the changing $|V_G|$.

Application of a pulsed input voltage to the sensor allowed the sensing of static temperature while minimising the degradation of the OTFT due to prolonged bias. A voltage pulse between 0 to –3 V featuring a –2 V pre-bias step was applied to $V_{IN}$, and $|V_{OUT}|$ was measured for various sensor temperatures between 20 to 25°C. Figures 7.8 and 7.9 show the effect of DOWN and UP temperature ramps on the sensor respectively when P(VDF-TrFE) is in ferroelectric state. As before with a DC $V_{IN}$, $|V_{OUT}|$ increases approximately linearly as a function of sensor temperature, displaying a sensitivity of ~14.8 mV/°C for the 20 to 25°C ramp (Figure 7.10). To confirm the changes seen in $|V_{OUT}|$ as a function of temperature between 20 to 25°C were a result of P(VDF-TrFE) capacitance changes, a similar experiment was carried out on a depoled P(VDF-TrFE)/OTFT sensor, i.e. P(VDF-TrFE) was in paraelectric state. In this case, $V_{IN}$ was a pulse from 0 to –1.5 V, featuring a –1 V pre-bias step. Whether P(VDF-TrFE) is poled or depoled, $|V_{OUT}|$ increases approximately linearly as a function of P(VDF-TrFE) temperature, displaying sensitivities of ~ 14.8 and 3.8 mV/°C for the poled and depoled cases respectively. The difference in sensitivities is due to two main factors. Firstly, the two experiments used different input voltage pulses which would result in smaller changes in output voltage for $V_{IN}$ = –1.5 V

compared to –3 V. Secondly, each experiment used a different transistor with different field-effect mobility. For the depoled P(VDF-TrFE)/OTFT sensor, OTFT mobility was only ~20 % of the value for the poled P(VDF-TrFE)/OTFT sensor, hence the lower output voltage. However, despite the difference in sensitivity, the two experiments confirm that $|V_{OUT}|$ increases linearly as a function of P(VDF-TrFE) temperature and the increase is due to capacitance changes in P(VDF-TrFE).

Finally, the P(VDF-TrFE)/OTFT sensor is able to respond to temperature through changes in P(VDF-TrFE) capacitance as well as through its pyroelectric effect. Due to the short-lived pyroelectric charge, the pyroelectric effect is only suitable for sensing dynamic temperature changes. Figures 7.16 (a) and 7.17 (a) present the sensor's response to temperature. This response combines the capacitive and pyroelectric effects. The PID controller provides fast changes in sensor temperature that are replicated by the sensor and measured as a change in $|V_{OUT}|$. When the temperature becomes constant, the pyroelectric response diminishes and $|V_{OUT}|$ levels out at a higher value that corresponds to the increased capacitance of P(VDF-TrFE). $|V_{OUT}|$ responds linearly across the 20 to 26°C range investigated. The pyroelectric effect leads to a greater voltage response than the voltage response achieved through changes in capacitance; however it is suitable for sensing dynamic temperature only. From Figure 7.17, by changing the temperature rapidly between 20 to 30°C, $|V_{OUT}|$ shows around a factor of 20 greater response for the poled P(VDF-TrFE) compared to the depoled one, indicating much greater sensitivity for sensing dynamic versus static temperature.

The P(VDF-TrFE)/OTFT sensor responds linearly to variations in sensor temperature. $|V_{OUT}|$ shows a linear dependence on temperature, outweighing the

circuit's force sensitivity by at least a factor of two regardless of whether DC or AC $V_{IN}$ is used. Previously, a charge-modulated organic field-effect transistor has been integrated with a pyroelectric element for use as a temperature transducer [123]. In a similar approach, as temperature is increased to the pyroelectric element, transistor $I_D$ increases linearly as a result of pyroelectricity and vice versa. The device shows fully reversible temperature response when temperature is ramped in both UP and DOWN configurations.

$V_G$ can be higher or lower than $V_{IN}$ and its magnitude depends on the orientation of the P(VDF-TrFE) capacitor with respect to the gate electrode of the transistor. Figure 7.18 demonstrates the changes in $V_G$ when either the Al or Au electrode of the P(VDF-TrFE) capacitor is connected to the gate of a transistor and the temperature is kept constant. For this measurement, the schematic of Figure 7.1 was adopted with $V_{IN} = V_D = -2$ V. Referring to Figure 7.18, when the Au electrode

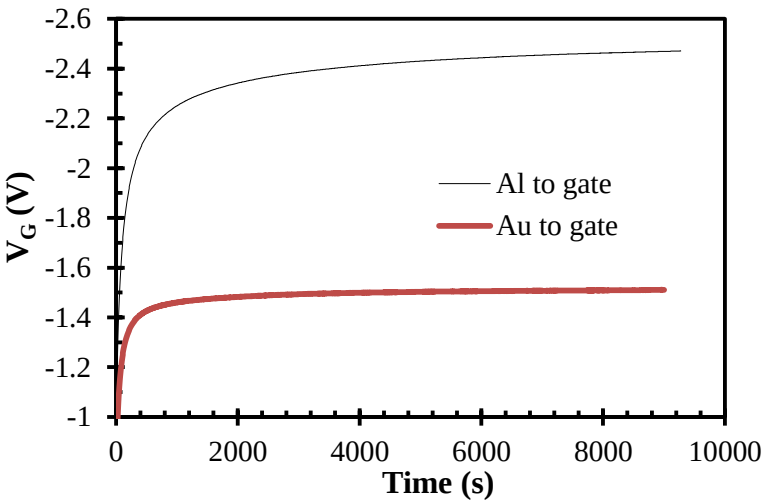



**Figure 7.18** P(VDF-TrFE)/OTFT sensor $V_G$ as a function of time for Al and Au connected to OTFT gate. $V_{IN} = V_D = -2$ V.

of depoled P(VDF-TrFE) is connected to the gate of the transistor, $V_G$ reaches –1.51 V after ~9000 s. On the other hand, when Al is connected to the gate, $V_G$ = –2.47 V after ~9000 s. In this case, the difference in the work functions between Al and Au forces $V_G$ to become more negative than $V_{IN} = V_D$. Fundamentally, this behaviour does not depend on the poling direction of the P(VDF-TrFE) capacitor or whether P(VDF-TrFE) is in ferroelectric or paraelectric state.

At time $t \rightarrow 0$ s, $V_{IN}$ appears across the P(VDF-TrFE) capacitor while there is no voltage across the transistor. For $t > 0$ s, when Au is connected to the gate, the voltage across P(VDF-TrFE) gradually decreases, while the voltage between the gate and source of the transistor increases. Charge accumulation will occur in the transistor when $|V_G| > |V_t|$ and the transistor will turn on.

Let's assume that the Au-side of the P(VDF-TrFE) capacitor is connected to the gate of the transistor and the P(VDF-TrFE) capacitor behaves like any ordinary capacitor. In such a case the voltage on the gate of the transistor (see Figure 7.1) can be written

$$V_G = \frac{C_{PVDF}}{C_{TOT}} \cdot V_{IN} + \frac{C_{GD}}{C_{TOT}} \cdot V_D + \frac{C_{GS}}{C_{TOT}} \cdot V_{OUT} \qquad (7.1)$$

where $C_{PVDF}$ is the capacitance of P(VDF-TrFE), $C_{GD}$ and $C_{GS}$ are the gate/drain and gate/source overlap capacitances of the transistor, respectively, and $C_{TOT} = C_{PVDF} + C_{GD} + C_{SD}$. Based on Equation (7.1), the changing $C_{PVDF}$ would lead to a change in $V_G$; any change in $V_G$ is manifested as a change in the drain current $I_D$ of the transistor, and thus the output voltage $V_{OUT}$ of the sensor. If the P(VDF-TrFE) capacitance changes from $C_{PVDF1}$ to $C_{PVDF2}$ as a result of applied static force or an

exposure to constant temperature, the corresponding change in the gate voltage of the transistor can be approximated by

$$\Delta V_G \cong V_{G2} - V_{G1} = (C_{PVDF2} - C_{PVDF1}) \cdot \frac{C_{GD}(V_{IN}-V_D)+C_{GS}(V_{IN}-V_{OUT})}{(C_{PVDF1}+C_{GD}+C_{GS})\cdot(C_{PVDF2}+C_{GD}+C_{GS})} \quad (7.2)$$

If one assumes that the effect of the second term can be neglected, the change in $V_G$ is proportional to the change in P(VDF-TrFE) capacitance. Therefore, the sensor of Figure 7.1 should respond to static pressure or constant temperature.

To confirm that Equation (7.1) fundamentally describes the behavior of the P(VDF-TrFE)/OFET sensor, the steady-state values of $V_G$ and $V_{OUT}$ of Figure 7.18 were used. Equation (7.1) was used to calculate $V_G$ based on the known values of $V_{OUT}$, $V_{IN}$, $V_D$, $C_{PVDF}$, $C_{GD}$ = $C_{SD}$, and $C_{TOT}$. The calculated value was –1.58 V, a value close to the measured value of –1.51 V. The transistors presented in Figure 7.18 had field-effect mobility of 0.56 $cm^2$/Vs. A similar measurement was performed with a transistor that had field-effect mobility of 0.025 $cm^2$/Vs and Equation (7.1) was again used to calculate $V_G$. The measured steady-state $V_G$ was –1.38V, while the calculated was –1.33 V, leading to a good agreement.

The circuit of Figure 7.1 would also respond to dynamic force or temperature via the inherent piezo- or pyroelectric effect of the ferroelectric P(VDF-TrFE) layer. In such a case, a charge perturbation is induced in the floating gate of the transistor, thus leading to the modulation of the transistor drain current, and Equation (7.1) is modified as follows

$$V_G = \frac{C_{PVDF}}{C_{TOT}} \cdot V_{IN} + \frac{C_{GD}}{C_{TOT}} \cdot V_D + \frac{C_{GS}}{C_{TOT}} \cdot V_{OUT} + \frac{Q}{C_{TOT}} \quad (7.3)$$

where $Q$ is the generated piezo/pyroelectric charge. This behavior is illustrated in Figure 7.17(a) for the poled P(VDF-TrFE)/OFET sensor. The strong response is caused by the induced pyroelectric charge and the corresponding term $\frac{Q}{C_{TOT}}$. In this case the orientation of the P(VDF-TrFE) capacitor (Al electrode connected to the gate) led to an increase (decrease) in $|V_{OUT}|$ with rising (falling) temperature. Swapping the polarity of the sensor (Au electrode connected to the gate) led to an opposite effect, i.e. a decrease (increase) in $|V_{OUT}|$ with rising (falling) temperature. Depoled P(VDF-TrFE) in the paraelectric state cannot respond to changes in temperature via the pyroelectric effect ($\frac{Q}{C_{TOT}} = 0$) and any change in the sensor output voltage results from the change in P(VDF-TrFE) capacitance, as shown in Figure 7.17(b).

## 7.6 Summary

This chapter presents a P(VDF-TrFE)/OTFT sensor where the ferroelectric P(VDF-TrFE) capacitor is connected to the gate of an organic thin-film transistor. The sensor is capable of sensing static force and temperature stimuli through changes in P(VDF-TrFE) capacitance. The circuit responds logarithmically to compressive force between 0 and ~ 8 N for both poled and depoled P(VDF-TrFE). In addition, static temperature can be detected by the sensor and it shows a linear response for DC and pulsed input voltage. Sensitivities for static temperature across the 5°C range are ~ 6.8 and 14.8 mV/°C for DC and pulse input voltages respectively for the poled/ferroelectric P(VDF-TrFE). Similarly, the sensitivities are ~ 13.7 and 3.8

mV/°C for DC and pulsed input voltages respectively for the depoled/paraelectric P(VDF-TrFE). Finally, the circuit is able to respond considerably to dynamic changes in sensor temperature via the inherent pyroelectric effect associated with poled/ferroelectric P(VDF-TrFE).

# Chapter 8

# Conclusion and future work

This chapter concludes all the research contained within this thesis in Section 8.1. Opportunity for future work is presented in Section 8.2.

## 8.1 Conclusion

This thesis presents the development of a force and temperature sensor based on ferroelectric polymer P(VDF-TrFE) integrated with low-voltage organic transistors for signal amplification and readout. The response of the P(VDF-

TrFE)/OTFT sensor to force and temperature was evaluated for potential use as a tactile sensor.

Development of the sensor involved three main areas: (i) low-voltage OTFT optimisation, (ii) study of the ferroelectric capacitor, and (iii) integration of the P(VDF-TrFE) capacitor with OTFT. For OTFT fabrication, the self-assembled monolayer of alkyl phosphonic acid that forms part of the gate dielectric was optimised with respect to the alkyl chain length. MIM structures and OTFTs with different phosphonic acid monolayers were fabricated and compared. WCA, AFM and FTIR were performed on the monolayers. Electrical characterisation of MIM and OTFTs was performed and long-term transistor stability was measured through bias stress experiments.

As the length of phosphonic acid alkyl chain increased, a decrease in $AlO_x/C_nPA$ layer capacitance was observed confirming monolayer formation in all six cases examined. In addition, each $AlO_x/C_nPA$ layer produced a low leakage current density between ~ $6x10^{-8}$ and ~ $3x10^{-8}$ A/cm$^2$. For each desorbed/annealed $AlO_x/C_nPA$ surface, the total surface energy was ~ 17.5 mJ/m$^2$ and independent of chain length. The electrical performance of OTFTs with $AlO_x/C_nPA$ dielectric was significantly affected by choice of $C_nPA$. Going from $C_8PA$ to $C_{18}PA$, OTFT $V_t$ reduces by ~ 10%, field-effect mobility increases by an order of magnitude, and $I_{OFF}$ reduces by almost half. OTFT performance improved across the board as the length of $C_nPA$ increased. Furthermore, bias stress-induced degradation of OTFT samples is related to $C_nPA$ length and longer chains show better air stability.

To achieve flexibility of organic thin-film circuits over large areas by manufacturing processes such as R2R, the integration of devices onto thin plastic substrates is needed. OTFTs based on the organic semiconductor DNTT were fabricated on 125 µm-thick PEN plastic foils. Two PEN substrates were tested for possible use, Teonex Q65FA featuring an adhesive layer on its bottom (non-device) side and Optfine PQA1 with a planarisation layer on the top (device) side. Both substrates were thermally annealed at 160°C to ensure compatibility with the maximum OTFT fabrication process temperature. In addition, DNTT deposition was optimised in terms of deposition rate. MIM and OTFT structures were produced and dielectric and OTFT electrical properties were evaluated, including a 1000-second bias stress.

Pre-annealing of the two PEN substrates prior to device fabrication resulted in Teonex remaining flat, while Optfine underwent a substantial and permanent change to its radius of curvature. $AlO_x/C_8PA$ transistors on Optfine exhibited greater field-effect mobility and remained more stable under bias stress when compared to similar devices on Teonex. This is most likely a result of the increased DNTT deposition rate on the Optfine substrate along with its lower surface roughness resulting from the planarisation.

The capacitive response of a P(VDF-TrFE) ferroelectric capacitor to force and temperature was investigated. The response was assessed via a change in layer capacitance due to static compressive force or constant temperature. Force was applied in the normal direction to the P(VDF-TrFE) capacitor between 0 to ~ 9 N and led to a logarithmic dependence of the capacitance with respect to force. For the lower end of applied forces (< 0.5 N), the capacitance sensitivity was ~ 7.1 pF/N.

Additionally, three distinct temperature ramps were performed on the P(VDF-TrFE) capacitor using changing ambient, vacuum and storage conditions. In each instance, the capacitor responded linearly to temperature between 15 to 47°C with sensitivity of ~ 7 pF/°C. To remove any potential piezoelectric/pyroelectric charge generated by dynamic force and temperature respectively, the sensor was depoled by heating it to above $T_{CURIE}$. In the depoled/paraelectric configuration, the capacitor retained its linear response to temperature displaying sensitivity of 9.4 pF/°C.

To achieve signal amplification and for readout purposes, the ferroelectric P(VDF-TrFE) capacitor was connected to the gate electrode of an organic thin-film transistor. It was shown that the P(VDF-TrFE)/OTFT sensor was capable of responding to static force and temperature events through a change in P(VDF-TrFE) capacitance. Response of the sensor to force and temperature was examined. The P(VDF-TrFE)/OTFT sensor showed a logarithmic dependence of its output voltage as a function of compressive force between 0 and ~ 8 N for both poled and depoled P(VDF-TrFE). Furthermore, a linear response was observed when static temperature changes (20 to 25°C) were applied to the P(VDF-TrFE)/OTFT sensor using both a DC and pulsed $V_{IN}$. Sensitivities of 6.8 and 14.8 mV/°C for poled P(VDF-TrFE) were obtained for DC and pulsed input voltages respectively as a function of static temperature. For depoled P(VDF-TrFE), sensitivities of ~ 13.7 and 3.8 mV/°C were achieved using DC and pulsed input voltages. Finally, the pyroelectric effect was examined using dynamic temperature ramps on both poled and depoled P(VDF-TrFE).

## 8.2 Future work

This thesis has shown the optimisation of OTFTs via the gate dielectric layer, choice of PEN substrate, as well as incorporation of an air stable organic semiconductor dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene. To date, some DNTT growth optimisation with respect to deposition rate has been performed. Further improvement in OTFT performance could be achieved through optimisation of the DNTT deposition temperature. This could lead to transistors with greater field-effect mobility and improved air and bias stability.

The development of ferroelectric P(VDF-TrFE) capacitors able to respond to changes in force and temperature has been shown through changes in P(VDF-TrFE) capacitance. However to date, the capacitors have only been realised on rigid Si wafer. Future work should focus on the fabrication of such ferroelectric capacitors on flexible PEN foil to integrate them with the existing OTFT technology.

Response of the P(VDF-TrFE)/OTFT sensor to compressive static force and temperature stimuli has been thoroughly investigated. Static force has been applied to the sensor in both poled and depoled configurations. Future work would develop a setup whereby dynamic changes in force could be applied to the P(VDF-TrFE) capacitor and the output voltage from the sensor would be a result of capacitive and piezoelectric effects inherent within poled P(VDF-TrFE), leading to an improved sensor sensitivity for dynamic force events.

To support the results found experimentally on the P(VDF-TrFE)/OTFT sensor, a more comprehensive model would need to be developed in the future. The

model would address the force and temperature data separately and form a solid theoretical basis for all further work on the sensor.

Finally, once the P(VDF-TrFE) capacitor and OTFT have been integrated on a shared flexible substrate, response of the entire circuit to force and temperature changes would need to be investigated.

## References


[1] H. Xu, D. Luo, M. Li, M. Xu, J. Zou, H. Tao, L. Lan, L. Wang, J. Peng and Y. Cao "A flexible AMOLED display on the PEN substrate driven by oxide thin-film transistors using anodized aluminium oxide as dielectric," *Journal of Materials Chemistry C* **2** (2014), pp. 1255 – 1259.

[2] T. Someya, T. Sekitani, S. Iba, Y. Kato, H. Kawaguchi and T. Sakurai, "A large-area, flexible pressure sensor matrix with organic field-effect transistors for artificial skin applications," *PNAS* **101** (2004), pp. 9966 – 9970.

[3] V. Fiore, P. Battiato, S. Abdinia, S. Jacobs, I. Chartier, R. Coppard, G. Klink, E. Cantatore, E. Ragonese and G. Palmisano, "An integrated 13.56-MHz RFID tag in a printed organic complementary TFT technology on flexible substrate," *IEEE Transactions on Circuits and Systems-1: Regular Papers* **62** (2015), pp. 1668 – 1677.

[4] C. Lochner, Y. Khan, A. Pierre and A. Arias, "All-organic optoelectronic sensor for pulse oximetry," *Nature Communications* **5** (2014), pp. 1 – 7.

[5] H. Kim, S. Lee and K. Yun, "Capacitive tactile sensor array for touch screen application," *Sensors and Actuators A:Physical* **165** (2011), pp. 2 – 7.

[6] G. Bűscher, R. Koiva, C. Schűrmann, R. Haschke and H. Ritter, "Flexible and stretchable fabric-based tactile sensor," *Robotics and Autonomous Systems* **63** (2015), pp. 244 – 252.

[7] J. Dargahi, "A piezoelectric tactile sensor with three sensing elements for robotic, endoscopic and prosthetic applications," *Sensors and Actuators* **80** (2000), pp. 23 – 30.

[8] S. Pullano, S. Islam and A. Fiorillo, "Pyroelectric sensor for temperature monitoring of biological fluids in microchannel devices, "*IEEE Sensors Journal* **14** (2014), pp. 2725 – 2730.

[9] S. Bauer, "Flexible electronics: Sophisticated skin," *Nature Materials* **12** (2013), pp. 871 – 872.

[10] "NAO humanoid robot tactile sensors", http://www.robotcenter.co.uk/pages/nao-humanoid-robot-tactile- sensors, accessed 2nd November 2016.

[11] Y. Su, W. Xie and J. Xu, "Towards low-voltage organic thin film transistors (OTFTs) with solution-processed high-k dielectric and interface engineering," *AIMS Materials Science* **2** (2015), pp. 510 – 529.

[12] Y. Takeda, K. Hayasaka, R. Shiwaku, K. Yokosawa, T. Shiba, M. Mamada, D. Kumaki, K. Fukuda and S. Tokito, "Fabrication of ultra- thin printed organic TFT CMOS logic circuits optimised for low-voltage wearable sensor applications," *Scientific Reports* **6** (2016), p. 25714.

[13] R. Dahiya, G. Metta and M. Valle, "Piezoelectric polymer oxide semiconductor field effect transistor (POSFET) devices for touch sensing," in *IEDST'09. 2nd International Workshop on Electron Devices and Semiconductor Technology* (2009), pp. 1 – 5.

[14] J. Kim, T. Ng and W. Kim, "Highly sensitive tactile sensors integrated with organic transistors," *Applied Physics Letters* **101** (2012), p. 103308.

[15] S. Sze, "Semiconductor devices physics and technology," John Wiley & Sons Singapore Pte. Limited, 3rd Edition, (2013).

[16] H. Klauk, "Organic thin-film transistors for flexible displays and circuits," in *70th Annual Device Research Conference (DRC)*, University Park, Pennsylvania, USA (2012), pp. 237 – 238.

[17] M. Mizukami, S. Oku, S. Cho, M. Tatetsu, M. Abiko, M. Mamada, T. Sakanoue, Y. Suzuri, J. Kido and S. Tokito, "A solution-processed organic thin-film transistor backplane for flexible multiphoton emission organic light-emitting diode displays," *IEEE Electron Device Letters* **36** (2015), pp. 841 – 843.

[18] R. Shiwaku, Y. Yoshimura, Y. Takeda, K. Fukuda, D. Kumaki and S. Tokito, "Control of threshold voltage in organic thin-film transistors by modifying gate electrode surface with $MoO_x$ aqueous solution and inverter circuit applications," *Applied Physics Letters* **106** (2015), p. 053301.

[19] L. Feng, W. Tang, J. Zhao, Q. Cui, C. Jiang and X. Guo, "All-solution-processed low-voltage organic thin-film transistor inverter on plastic substrate," *IEEE Transactions on Electron Devices* **61** (2014), pp. 1175 – 1180.

[20] G. Maiellaro, E. Ragonese, A. Castorina, S. Jacob, M. Benwadih, R. Coppard, E. Cantatore and G. Palmisano, "High-gain operational transconductance amplifiers in a printed complementary organic TFT technology on flexible foil," *IEEE Transactions on Circuits and Systems-1: Regular Papers* **60** (2013), pp. 3117 – 3125.

[21] D. Taylor, E. Patchett, A. Williams, N. Neto, Z. Ding, H. Assender, J. Morrison and S. Yeates, "Organic digital logic and analog circuits fabricated in a roll-to-roll compatible vacuum-evaporation process," *IEEE Transactions on Electron Devices* **61** (2014), pp. 2950 – 2956.

[22] M. Chang, P. Lee, S. McAlister and A. Chin, "Small-subthreshold-swing and low-voltage flexible organic thin-film transistors which use HfLao as the gate dielectric," *IEEE Electron Device Letters* **30** (2009), pp. 133 – 135.

[23] L. Deng, P. Lai, W. Chen, J. Xu, Y. Liu, H. Choi, and C. Che, "Effects of different annealing gases on pentacene OTFT with HfLao gate dielectric," *IEEE Electron Device Letters* **32** (2011), pp. 93 – 95.

[24] C. Wei, S. Kuo, Y. Hung, W. Huang, F. Adriyanto, and Y. Wang, "High-mobility pentacene-based thin-film transistors with a solution-processed barium titanate insulator," *IEEE Electron Device Letters* **32** (2011), pp. 90 – 92.

[25] H. Yan, H. Hanagata, T. Jo and H. Okuzaki, "Low-voltage organic field-effect transistors fabricated on self-assembled-monolayer-free $SrTiO_3$ insulator," *Japanese Journal of Applied Physics* **50** (2011), p. 01BC05.

[26] S. Kim, S. Yang, K. Shin, H. Jeon, J. Lee, K. Hong and C. Park, "Low-operating-voltage pentacene field-effect transistor with a high-dielectric-constant polymeric gate dielectric," *Applied Physics Letters* **89** (2006), p. 183516.

[27] K. Kim and C. Song, "Low voltage pentacene thin film transistors employing a self-grown metal-oxide as a gate dielectric," *Applied Physics Letters* **88** (2006), p. 233508.

[28] J. Lee, J. Kim and S. Im, "Effects of substrate temperature on the device properties of pentacene-based thin film transistors using $Al_2O_{3+x}$ gate dielectric," *Journal of Applied Physics* **95** (2004), pp. 3733 – 3736.

[29] H. Klauk, U. Zschieschang, J. Pflaum and M. Halik, "Ultralow-power organic complementary circuits," *Nature* **445** (2007), pp. 745 – 748.

[30] J. Choi, D. Hwang, S. Jeong, J. Park, E. Kim, J. Kim and S. Im, "Polymer/$AlO_x$ bilayer dielectrics for low-voltage organic thin-film transistors," *Journal of the Electrochemical Society* **154** (2007), pp. H331 – H335.

[31] H. Yang, C. Yang, S. Kim, M. Jang and C. Park, "Dependence of pentacene crystal growth on dielectric roughness for fabrication of flexible field-effect transistors," *Applied Materials and Interfaces* **2** (2010), pp. 391 – 396.

[32] M. Aghamohammadi, R. Rodel, U. Zschieschang, C. Ocal, H. Boschker, R. Weitz, E. Barrena and H. Klauk, "Threshold-voltage shifts in organic transistors due to self-assembled monolayers at the dielectric: evidence for electronic coupling and dipolar effects," *Applied Materials and Interfaces* **7** (2015), pp. 22775 – 22785.

[33] R. Hofmockel, U. Zschieschang, U. Kraft, R. Rodel, N. Hansen, M. Stolte, F. Wurthner, K. Takimita, K. Kern, J. Pflaum and H. Klauk, "High-mobility organic thin-film transistors based on a small-molecule semiconductor deposited in vacuum and by solution shearing," *Organic Electronics* **14** (2013), pp. 3213 – 3221.

[34] T. Kelley, L. Boardman, T. Dunbar, D. Muyres, M. Pellerite and T. Smith, "High-performance OTFTs using surface-modified alumina dielectrics," *Journal of Physical Chemistry B* **107** (2003), pp. 5877 – 5881.

[35] A. Jedaa, M. Burkhardt, U. Zschieschang, H. Klauk, D. Habich, G. Schmid and M. Halik, "The impact of self-assembled monolayer thickness in hybrid gate dielectrics for organic thin-film transistors," *Organic Electronics* **10** (2009), pp. 1442 – 1447.

[36] H. Ma, O. Acton, G. Ting, J. Ka, H. Yip, N. Tucker, R. Schofield and A. Jen, "Low-voltage organic thin-film transistors with π-σ-phosphonic acid molecular dielectric monolayers," *Applied Physics Letters* **92** (2008), p. 113303.

[37] P. Wöbkenberg, J. Ball, F. Kooistra, J. Hummelen, D. de Leeuw, and D. Bradley, "Low-voltage organic transistors based on solution processed semiconductors and self-assembled monolayer gate dielectrics," *Applied Physics Letters* **93** (2008), p. 013303.

[38] M. Yi, J. Guo, W. Li, L. Xie, Q. Fan and W. Huang, "High-mobility flexible pentacene-based organic field-effect transistors with PMMA/PVP double gate insulator layers and the investigation on their mechanical flexibility and thermal stability," *RSC Advances* **5** (2015), pp. 95273 – 95279.

[39] C. Kagan, A. Afzali and T. Graham, "Operational and environmental stability of pentacene thin-film transistors," *Applied Physics Letters* **86** (2005), p. 193505.

[40] G. Abbas, Z. Ding, H. Assender, J. Morrison, S. Yeates, E. Patchett and D. Taylor, "A high-yielding evaporation-based process for organic transistors based on the semiconductor DNTT," *Organic Electronics* **15** (2014), pp. 1998 – 2006.

[41] Y. Fujisaki, Y. Nakajima, M. Nakata, H. Tsuji and T. Yamamoto," Fabrication of organic thin film transistor arrays on plastic and paper substrate for flexible display application," *MRS Proceedings* **1628** (2014).

[42] U. Zschieschang, F. Ante, D. Kalblein, T. Yamamoto, K. Takimiya, H. Kuwabara, M. Ikeda, T. Sekitani, T. Someya, J. Blochwitz-Nimoth and H. Klauk, "Dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) thin-film transistors with

improved performance and stability," *Organic Electronics* **12** (2011), pp. 1370 – 1375.

[43] D. Mao, B. Gnade and M. Quevedo-Lopez, "Ferroelectric properties and polarisation switching kinetic of poly (vinylidene fluoride – t trifluoroethylene) copolymer", *Ferroelectrics – Physical Effects*, ISBN: 978-953-307-453-5 (2011), DOI: 10.5772/17147.

[44] "Faculty Science – Ferroelectricity", available at http://faculty-.co.uk/, accessed 12th October 2016.

[45] B. Su, "Novel fabrication processing for improved lead zirconate titanate (PZT) ferroelectric ceramic materials," Ph.D dissertation, Fact. Eng. Uni. Birmingham, Birmingham, UK, 1998.

[46] T. Kamel, G. With, "Poling of hard ferroelectric PZT ceramics," *Journal of the European Ceramic Society* **28** (2008), pp. 1827 – 1838.

[47] M. Sung, K. Shin and W. Moon, "A micro-machines hydrophone using piezoelectricity on gate of a field-effect transistor", in *18th Int. Conf. on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, Anchorage, AK, pp. 379-382, June 2015.

[48] W. Zutang, S. Xianzhong, J. Zhuangde, L. Peng, G. Lin and J. Xingdong, "A novel PVDF based high Gn shock accelerometer", *Journal of Physics conference series* **13** (2005), pp.107-110.

[49] S. Rajala, S. Tuukkanen and J. Halttunen, "Characteristics of piezoelectric polymer film sensors with solution-processable graphene-based electrode materials", *IEEE Sensors Journal* **15** (2015), pp. 3102-3109.

[50] S. Khan, W. Dang, L. Lorenzelli and R. Dahiya, "Flexible pressure sensors based on screen-printed P(VDF-TrFE) and P(VDF-TrFE)/MWCNTs", *IEEE Transactions On Semiconductor Manufacturing* **28** (2015), pp. 486-493.

[51] H. Kawai, "The piezoelectricity of PVDF," *Japanese Journal of Applied Physics* **8** (1969), pp.975-976.

[52] F. Foster, K. Harasiewicz and M. Sherar, "A history of medical and biological imaging with polyvinylidene fluoride (PVDF) transducers," *IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control* **47** (2000), pp. 1363 – 1371.

[53] N. Tamjidi, K. Sato, J. Sakurai and S. Hata, "PVDF actuator for high-frequency fatigue test of thin-film metals," *IEEJ Transactions on Electrical and Electronic Engineering* **8** (2013), pp. 199 – 205.

[54] S. Kim and C. Kee, " Electro-active polymer actuator based on PVDF with bacterial cellulose nano-whiskers (BCNW) via electrospinning method," *International Journal of Precision Engineering and Manufacturing* **15** (2014), pp. 315 – 321.

[55] C. Li, P. Wu, S. Lee, A. Gorton, M. Schulz and C. Ahn, "Flexible dome and bump shape piezoelectric tactile sensors using PVDF-TrFE copolymer," *Journal of Microelectromechanical Systems* **17** (2008), pp. 334 – 341.

[56] T. Sharma, K. Aroom, S. Naik, B. Gill and J. Zhang, "Flexible thin-film PVDF-TrFE based pressure sensor for smart catheter applications," *Annals of Biomedical Engineering* **41** (2013), pp. 744 – 751.

[57] S. Hwang, I. Bae, R. Kim and C. Park, "Flexible non-volatile ferroelectric polymer memory with gate-controlled multilevel operation," *Advanced Materials* **24** (2012), pp. 5910 – 5914.

[58] P. Witte, P. Dijkstra, J. Van der Berg and J. Feijen, "Phase separation processes in polymer solutions in relation to membrane formation," *Journal of Membrane Science* **117** (1996), pp. 1 – 31.

[59] R. Magalhães, N. Durães, M. Silva, J. Silva, V. Sencadas, G. Botelho, J. Ribelles and S. Lanceros-Méndez, "The role of solvent evaporation in the microstructure of electroactive β-poly(vinylidene fluoride) membranes obtained by isothermal crystallisation," *Soft Materials* **9** (2011), pp. 1 – 14.

[60] W. Eisenmenger, H. Schmidt and B. Dehlen, "Space charge and dipoles in polyvinylidenefluoride," *Brazilian Journal of Physics* **29** (1999), pp. 295 – 305.

[61] T. Furukawa, "Ferroelectric properties of vinylidene fluoride copolymers," *Phase Transitions* **18** (1989), pp. 143 – 211.

[62] R. Gregorio and E. Ueno, "Effect of crystalline phase, orientation and temperature on the dielectric properties of PVDF," *Journal of Material Science* **34** (1999), pp. 4489 – 4500.

[63] X. Yang, X. Kong, S. Tan, G. Li, W. Ling and E. Zhou, "Spatially-confined crystallisation of poly(vinylidene fluoride)," *Polymer International* **49** (2000), pp. 1525 – 1528.

[64] T. Dargavile, M. Celina and P. Chaplya, "Evaluation of piezoelectric poly(vinylidene fluoride) polymers for use in space environments. I. temperature limitations," *Journal of Polymer Science Part B: Polymer Physics* **43** (2005), pp. 1310 – 1320.

[65] E. Nix, and I. Ward, "The measurement of the shear piezoelectric coefficients of polyvinylidene fluoride," *Ferroelectrics* **67** (1986), pp. 137 – 141.

[66] http://www.piezotech.fr/image/documents/22-31-32-33-piezotech-piezoelectric-films-leaflet.pdf, "Piezoelectric films technical information", accessed 21st October 2016.

[67] A. Lovinger, "Ferroelectric polymers," *Science* **220** (1983), pp. 1115 – 1121.

[68] K. Lau, Y. Liu, H. Chen and R. Withers, "Effect of annealing temperature on the morphology and Piezoresponse characterisation of poly (vinylidene fluoride-trifluoroethylene) films via scanning probe microscopy," *Advances in Condensed Matter Physics* **2013** (2013).

[69] H. Wang, Q. Zhang, L. Cross and A. Sykes, "Piezoelectric, dielectric, and elastic properties of poly(vinylidene fluoride/trifluoroethylene)", *Journal of Applied Physics* **74** (1993), pp. 3394-3398.

[70] R. S. Dahiya and M. Valle, *Robotic tactile sensing: technologies and system*: Springer Science & Business Media (2012), p. 168.

[71] A. Pecora, L. Maiolo, F. Maita and A. Minotti, "Flexible PVDF-TrFE pyroelectric sensor driven by polysilicon thin film transistor fabricated on ultra-thin polyimide substrate," *Sensors and Actuators A: Physical* **185** (2012), pp. 39 – 43.

[72] S. Gupta, "Vacuum growth of N-octylphosphonic acid monolayer for low-voltage organic thin-film transistors," PhD Thesis, Dept. of Electronic and Electrical Engineering, University of Strathclyde, Glasgow, 2013.

[73] K. Chinnam, "Aluminium oxide prepared by UV/ozone exposure for low-voltage organic thin-film transistors," PhD Thesis, Dept. of Electronic and Electrical Engineering, University of Strathclyde, Glasgow, 2014.

[74] S. Gupta, S. Hannah, C. Watson, P. Sutta, R. Pedersen, N. Gadegaard and H. Gleskova, "Ozone oxidation methods for aluminium oxide formation: Application to low-voltage organic transistors," *Organic Electronics* **21** (2015), pp. 132-137.

[75] S. Gupta and H. Gleskova, "Dry growth of n-octylphosphonic acid monolayer for low-voltage organic thin-film transistors," *Organic Electronics* **14** (2013), pp. 354-361.

[76] G. Abbas, Z. Ding, K. Mallik, H. Assender and D. Taylor, "Hysteresis-free vacuum-processed acrylate-pentacene thin-film transistors," *IEEE Electron Device Letters* **34** (2013), pp.268-270.

[77] K. Fukada, T. Hamamoto, T. Yokota, T. Sekitani, U. Zschieschang, H. Klauk and T. Someya, "Effects of the alkyl chain length in phosphonic acid self-assembled monolayer gate dielectrics on the performance and stability of low-voltage organic thin-film transistors," *Applied Physics Letters* **95** (2009), p.203301.

[78] "Organic electronics materials, manufacturing and applications," (Editor H. Klauk), Wiley-VCH, Germany (2006), pp. 124-125.

[79] Z. Ding, G. Abbas, H. Assender, J. Morrison, S. Yeates, E. Patchett and D. Taylor, "Effect of oxygen, moisture and illumination on the stability and reliability of dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) OTFTs during operation and storage," *Applied Materials and Interfaces* **6** (2014), pp. 15224 – 15231.

[80] http://www.engineeringtoolbox.com/relative-permittivity-d_1660.html, accessed 02/12/15.

[81] R. Dahiya, M. Valle, G. Metta, L. Lorenzelli and S. Pedrotti, "Deposition, processing and characterisation of P(VDF-TrFE) thin films for sensing applications," in *2008 IEEE Sensors*, 2008, pp. 490-493.

[82] H. Nalwa, *Ferroelectric Polymers: Chemistry: Physics, and Applications* **28**, CRC Press (1995).

[83] S. Gupta, P. Sutta, D. Lamprou and H. Gleskova, "Effect of substrate temperature on vapour-phase self-assembly of n-octylphosphonic acid monolayer for low-voltage organic thin-film transistors," *Organic Electronics* **14** (2013), pp. 2468 – 2475.

[84] H. Gleskova, S. Gupta and P. Sutta, "Structural changes in vapour-assembled n-octylphosphonic acid monolayer with post-deposition annealing: Correlation with bias-induced transistor instability," *Organic Electronics* **14** (2013), pp. 3000 - 3006.

[85] O. Acton, G. Ting, P. Schamberger, F. Ohuchi, H. Ma and A. Jen, "Dielectric surface-controlled low-voltage organic transistors via n-alkyl phosphonic acid self-assembled monolayers on high-k metal oxide," *Applied Materials and Interfaces* **2** (2010), pp. 511 – 520.

[86] J. Love, L. Estroff, J. Kriebel, R. Nuzzo and G. Whitesides, "Self-assembled monolayers of thiolates on metals as a form of nanotechnology," *Chemical Reviews* **105** (2005), pp. 1103 – 1170.

[87] F. Schreiber, "Structure and growth of self-assembling monolayers," *Progress in Surface Science* **65** (2000), pp. 151 – 256.

[88] R. Nuzzo, L. Dubois and D. Allara, "Fundamental studies of microscopic wetting on surfaces. 1. Formation and structural characterisation of a self-consistent series of polyfunctional organic monolayers," *Journal of American Chemical Society* **112** (1990), pp. 558 – 569.

[89] M. Novak, C. Jager, A. Rumpel, H. Kropp, W. Peukert, T. Clark and M. Halik, "The morphology of integrated self-assembled monolayers and their impact on

devices – A computational and experimental approach," *Organic Electronics* **11** (2010), pp. 1476 – 1482.

[90] C. Zhang, J. Wu, G. Galli and F. Gygi, "Structural and vibrational properties of liquid water from Van der Waals density functionals," *Journal of Chemical Theory and Computation* **7** (2011), pp. 3054 – 3061.

[91] G. Hill, C. Weinert, L. Kreplak and B. Zyl. "Influence of self-assembled monolayer chain length on modified gate dielectric pentacene thin-film transistors," *Applied Physics A* **95** (2009), p. 81.

[92] S. Yoo, M. Yi, Y. Kim and K. Jang, "One-pot surface modification of poly(ethylene-alt-maleic anhydride) gate insulators for low-voltage DNTT thin-film transistors," *Organic Electronics* **33** (2016), pp. 263 – 268.

[93] Y. Choe, M. Yi, J. Kim, Y. Kim and K. Jang, "Surface grafting of octylamine onto poly(ethylene-alt-maleic anhydride) gate insulators for low-voltage DNTT thin-film transistors," *Physical Chemistry Chemical Physics* **18** (2016), pp. 8522 – 8528.

[94] Z. Ding, G. Abbas, H. Assender, J. Morrison, S. Yeates, E. Patchett and D. Taylor, "Vacuum production of OTFTs by vapour jet deposition of dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) on a lauryl acrylate functionalised dielectric surface," *Organic Electronics* **31** (2016), pp. 90 – 97.

[95] H. Chang, Y. Deng, Y. Geng, T. Wang and D. Yan, "Effect of the initial stage of film growth on device performance of organic transistors based on dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT)," *Organic Electronics* **22** (2015), pp. 86 – 91.

[96] Z. Zhang, X. Ren, B. Peng, Z. Wang, X. Wang, K. Pei, B. Shan, Q. Miao and P. Chan, "Direct patterning of self-assembled monolayers by stamp printing method and applications in high performance organic field-effect transistors and complementary inverters," *Advanced Functional Materials* **25** (2015), pp. 6112 – 6121.

[97] E. Hoque, J. DeRose, G. Kulik, P. Hoffmann, H. Mathieu and B. Bhushan, "Alkylphosphonate modified aluminium oxide surfaces," *Journal of Physical Chemistry B* ***110*** (2006), p. 10855.

[98] M. Giza, P. Thissen and G. Grundmeier, "Adsorption kinetics of organophosphonic acids on plasma-modified oxide-covered aluminium surfaces," *Langmuir* **24** (2008), pp. 8688 – 8694.

[99] L. Hector, S. Opalka, G. Nitowski, L. Wieserman, D. Siegel, H. Yu and J. Adams, "Investigation of vinyl phosphonic acid/hydroxylated α-$Al_2O_3$ (0 0 0 1) reaction enthalpies," *Surface Science* **494** (2001), pp. 1-20.

[100] D. Allara and R. Nuzzo, "Spontaneously organised molecular assemblies.1. Formation, dynamics, and physical properties of n-alkanoic acids adsorbed from solution on an oxidised aluminium surface," *Langmuir* **1** (1985), pp. 45 – 52.

[101] I. Maege, E. Jaehne, A. Henke, H. Alder, C. Bram, C. Jung and M. Stratmann, "Self-assembling adhesion promoters for corrosion resistant metal polymer interfaces," *Progress in Organic Coatings* **34** (1998), pp. 1 – 12.

[102] "Teijin Dupont Films: Properties of various high performance films," http://www.teijindupontfilms.jp/english/product/hi_film.html, accessed 29th June 2016.

[103] K. Fukuda, Y. Takeda, Y. Yoshimura, R. Shiwaku, L. Tran, T. Sekine, M. Mizukamo, D. Kumaki and S. Tokito, "Fully-printed high-performance organic thin-film transistors and circuitry on one-micron-thick polymer films, "*Nature Communications***5** (2014), p. 5147.

[104] S. Wagner, S. Lacour, J. Jones, P. Hsu, J. Sturm, T. Li and Z. Suo, "Electronic skin: architecture and components," *Physica E: Low- dimensional Systems and Nanostructures* **25** (2004), pp. 326-334.

[105] J. Park, Y. Lee, S. Lim, Y. Lee, Y. Jung, H. Lim, *et al.*, "Ultrasensitive piezoresistive pressure sensors based on interlocked micropillar arrays," *BioNanoScience* **4** (2014),pp. 349-355.

[106] C. Chang, F. Lee, Y. Lin and Y. Yang, "Tunnelling piezoresistive tactile sensing array for continuous blood pressure monitoring," *29th International Conference on Microelectromechanical Systems* (2016), pp. 169-172, Shanghai.

[107] Y. Wang, J. Zheng, G. Ren, P. Zhang and C. Xu, "A flexible piezoelectric force sensor based on PVDF fabrics," *Journal of Smart Materials and Structures* **20** (2011).

[108] L. Wang, L. Qin and L. Li, "Piezoelectric dynamic pressure sensor," in *Information and Automation (ICIA) 2010 IEEE International conference on* (2010), pp. 906-911.

[109] N. Marsi, B. Majlis, A. Hamzah and F. Mohd-Yasin, "High reliability of MEMS packaged capacitive pressure sensor employing 3C-SiC for high temperature," in *2nd International Conference on Sustainable Energy Engineering and Applications* (2014) , Bandung, Indonesia.

[110] E.G. Bakhoum and M.H. Cheng, "Novel capacitive pressure sensor," *Journal of Microelectromechanical Systems* **19** (2010), pp. 443-450.

[111] Q. Ren, L. Wang, J. Huang, C. Zhang, "A novel capacitive temperature sensor for a lab-on-a-chip system," in *IEEE Sensors 2014 Proceedings* (2014) pp. 436-439, Valencia, Spain.

[112] A. Kimoto and S. Shimada, "A proposal of new multifunctional pressure sensor based on PVDF films," *IEEE Transactions on Instrumentation and Measurement* **62** (2013), pp. 2870-2877.

[113] F. Viola, P. Cosseddu, S. Lai and A. Spanu, "Flexible temperature sensors based on charge modulated organic thin film transistors," in *Ph.D. Research in Microelectronics and Electronics (PRIME) (2015) 11th Int. Conf. on*, pp. 278-281.

[114] T. Sharma, S. Je, B. Gill, J. Zhang, "Patterning piezoelectric thin film PVDF-TrFE based pressure sensor for catheter application," in *Sensors and Actuators A: Physical* (*2012) 24th Int. Conf. on Microelectromechanical Systems* **177** (2012), pp. 87-92.

[115] B. Ploss, F. Shin, H. Chan and C. Choy, "Pyroelectric activity of ferroelectric PT/PVDF-TrFE," *IEEE Transactions on Dielectrics and Electrical Insulation* (2000), pp. 517-522.

[116] J. Anjana, J. Prashanth, S. Jayanth and S. Asheesh, "Typical properties and specific applications of piezoelectric polymer," *International Journal of Materials Science and Engineering* **3** (2015), pp. 327 – 345.

[117] A. Shirinov and W. Schomburg, "Pressure sensor from a PVDF film," in *Sensors and Actuators A: Physical, (2008) 20th European Conference on Solid-State Transducers – Eurosensors* **142** (2008), pp. 48-55.

[118] A. Spanu, L. Pinna, F. Viola, L. Seminara, M. Valle, A. Bonfiglio and P. Cosseddu, "A high-sensitivity tactile sensor based on piezoelectric polymer PVDF coupled to an ultra-low voltage organic transistor," *Organic Electronics* **36** (2016), pp. 57 – 60.

[119] K. Shin, J. Lee and J. Jang, "Highly sensitive, wearable and wireless pressure sensor using free-standing ZnO nanoneedle/PVDF hybrid thin film for heart rate monitoring," *Nano Energy* **22** (2016), pp. 95 – 104.

[120] S. Emamian, B. Narakathu, A. Chlaihawi and M. Atashbar, "Fabrication and characterisation of piezoelectric paper based device for touch and force sensing applications," *Procedia Engineering* **168** (2016), pp. 688 – 691.

[121] I. Graz, M. Kaltenbrunner, C. Keplinger, R. Schodiauer, S. Bauer, S. Lacour and S. Wagner, "Flexible ferroelectret field-effect transistor for large-area sensor skins and microphones," *Applied Physics Letters* **89** (2006), p. 073501.

[122] S. Zilker, C. Detcheverry, E. Cantatore and D. Leeuw, "Bias stress in organic thin-film transistors and logic gates," *Applied Physics Letters* **79** (2001), pp. 1124 – 1126.

[123] P. Cosseddu, F. Viola, S. Lai, L. Raffo and A. Bonfiglio, "A temperature transducer based on a low-voltage organic thin-film transistor detecting pyroelectric effect," *IEEE Electron Device Letters* **35** (2014), pp. 1296 – 1298.