Enhancing Uniformity and Integration Scalability of Photonic Devices Using Selective Transfer-Printing Techniques

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This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

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Abstract

The overall objective of this thesis is to develop and apply high-accuracy transfer-printing techniques for the integration of a wide variety of photonic devices onto heterogeneous photonic integrated circuit (PIC) platforms. These platforms span different material systems as well as a range of structural configurations. By allowing accurate, scalable, and flexible assembly of micro- and nanoscale photonic devices, this approach aims to improve the uniformity, production yield, and device density of next-generation photonic integrated circuits (PICs), and support their use in large-scale applications such as optical communications, sensing, and quantum technologies.

This work began with the design and fabrication of supporting frames made of both photoresist and silica on silicon substrates, which were used to enable high-yield transfer printing of silicon photonic crystal cavity membranes designed to resonate at 1550 nm. The successful, high-accuracy transfer printing of silicon photonic crystal cavity (PhCC) membranes enabled large-scale and wavelength-based regrouping, achieving a yield of 119 out of 120. The reassembled membranes exhibited a significantly improved uniformity, with a mean wavelength shift of ± 0.007 nm and a standard deviation of ± 0.021 nm, in contrast to the ~ 1 nm standard deviation observed in the as-fabricated membranes.

Similar high accuracy transfer-printing techniques were then developed to enable the precise integration of nanoscale light sources into photonic circuits. Specifically, 20 InP semiconductor nanowires were deterministically embedded into 20 polymer (SU-8) optical waveguides fabricated on high-quality glass substrates. A micro-LED-on-CMOS projection system was built and used to optically excite and modulate the InP nanowires via on-off keying at frequencies reaching hundreds of megahertz. The

modulated infrared emission was effectively coupled into the waveguides and collected at the output facets, demonstrating the feasibility of integrating nanowire emitters into scalable photonic platforms. This work represents the first demonstration of nanowire modulation using incoherent visible light sources, although lasing was not achieved due to free-space optical losses. 16 GaN-based micro-LED pixels with dimensions of $100 \times 100\,\mu\text{m}^2$ were transfer-printed onto an optimised chip featuring nanowires (NWs) embedded in polymer waveguides, with a PDMS adhesion layer, to improve scalability and enable an on-chip optical pumping system. 15 out of the 16 pixels were successfully probed and modulated using relatively small-signal excitation at effective frequencies in the tens of megahertz, thereby enabling corresponding modulation of the embedded nanowires. Additionally, the emission of polymer waveguides was shown and analysed.

The high-yield and high-accuracy transfer-printing technique significantly improves the uniformity and scalability in the large-scale fabrication and integration of photonic devices. By enabling precise placement across diverse substrates and material platforms, this approach addresses fabrication non-uniformities and supports the assembly of complex photonic systems. These results highlight the potential of transfer printing as a key enabling technology for next-generation integrated photonics.

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Chapter 0. Acknowledgements

Chapter 1

Introduction

This thesis focuses on the integration of photonic devices, especially arrays of micro/nanoscale optoelectronic devices, onto different substrates through elastomeric micro-transfer-printing for creating scalable photonic integrated circuits (PICs) systems in data processing and communications applications.

This research project can be divided into two main topics: (1) Integration of micro/nanoscale optoelectronics devices onto substrates in different materials (Silica on Silicon and Glass) and additional fabrication processes on these devices to build a complete PIC system; and (2) Optical build of the set-up for the PIC prototype's excitation and manipulation through electrical or optical methods.

As such, Chapter 1 gives a general introduction on the development roadmap of photonic integrated circuits, and their applications in multiple fields, especially in data transmission and communications. Additionally, an overview of heterogenous integration methods applied during the fabrication of optoelectronic devices is given. The physical principle of micro-transfer-printing, and the previous research done by the group are also discussed and summarised. Moreover, a brief introduction of the micro/nanoscale optoelectronic components used for light emitting, transmission and confinement purposes is also given, including Silicon Photonic Crystal cavities (Si PhCCs), Semiconductor Nanowires (NWs) and Gallium Nitride Micro-sized-light-emitting-diodes (GaN micro-LEDs).

Chapter 2 outlines the experimental techniques and systems employed in the fabri-

cation of elastomeric stamps and PICs. The chapter begins by introducing the methods and equipment used in the preparation of various receiver substrates. It then details the fabrication process of elastomeric stamps and explains the underlying mechanism of transfer printing, including the alignment accuracy analysis. Finally, the chapter presents the custom-built systems developed to enable high-precision micro-transfer printing and to facilitate in-situ measurements during the process.

Chapter 3 gives a detailed description of the micro-transfer-printing of Si PhCCs membranes onto receivers with frames in different materials, including photoresist and Silica on Silicon (111) substrate. The chapter begins with an introduction to the customised array of PhCC membranes made in the Massachusetts Institute of Technology (MIT), followed by a detailed discussion on the design considerations of the receiver structures, with an emphasis on minimising their impact on the optical performance of the integrated devices. The process and yield of transfer-printing on two different frames in different materials and with different transfer-printing system is demonstrated and analysed. Furthermore, a critical comparison of the reflectivity spectrum (resonant wavelength) before and after the transfer-printing which is conducted with the advanced customised transfer-printing system with in-situ measurement devices is given.

Chapter 4 describes the high-yield, high-precision fabrication of a prototype PIC chip that embeds semiconductor nanowires into polymer optical waveguides and demonstrates their excitation and modulation via a scalable platform using an individually addressable micro-LED-on-CMOS array. It starts with a brief introduction to the semiconductor NWs fabricated by the Australian National University (ANU) and summarises previous research conducted on these devices. This is followed by a detailed description of the assembly process used to integrate the NWs with polymer optical waveguides. The chapter then introduces the micro-LED-on-CMOS array employed as the optical pumping source for modulating the embedded NWs, the optical components and process of optical set-up design and build to make the optical pumping source projectable are also listed and discussed. Finally, it concludes by demonstrating the optical modulation bandwidth of the prototype chip and discussing its potential applications in high-speed data transmission.

Chapter 5 presents an expanded research project that demonstrates integration of some customised and suspended GaN LED pixels together with the PIC chip introduced in Chapter 4 by transfer-printing with the employment of an additional adhesion layer. This chapter gives an introduction of the suspended GaN LED pixels array prefabricated by Dr. Benoit Jack Eloi Guilhabert, and the workflow and process of the optimised NWs-in-waveguides structures' design, fabrication and integration is coming after. This chapter is summarised and concluded by showing that the embedded NWs can be small signal modulated by the printed LED pixels into a similar frequency range as Chapter 4. This significantly increases the scalability of the whole system by building a system on-chip design for the manipulation of nanowires by an incoherent light source. This thesis concludes with a conclusion and further work chapter, and a list of publications is presented at the end.

1.1 Roadmap of Photonic Integrated Circuits Development

With the development of the internet and the massive growing demand for communication networks that can offer greater bandwidth and calculation capability with low cost [1], especially the massive development of artificial intelligence (AI) [2] and high-performance computing (HPC) [3], the requirement on integrated electronics is also growing explosively. The market needs high performance hardware/processors that can deliver better performance to drive next generation of artificial intelligence, especially those based on generative AI.

As described in the famous Moore's law [4], the number of transistors on a microchip increases rapidly over the years. Some world-leading integrated electronics manufacturers such as Samsung [5] and TSMC [6] are now pushing their semiconductor manufacturing process of the metal-oxide-semiconductor field-effect transistors (MOSFETs) nodes from 3 nm process [7] to 2 nm process [8] for their next generation of commercial integrated electronic circuits. However, the relentless pursuit of better performance and the accompanying demand for greater integration have led to ever-increasing require-

ments for manufacturing processes, such as the need for more advanced lithography systems, at the same time, the defect and cost during the manufacturing are significantly increased. The complexity of shrinking the MOSFETs further, the physical restrictions on fabrication, and the resulting research and manufacturing cost make the manufacturers seek alternative solutions instead of keeping scaling up the numbers of transistors on a single chip.

In traditional integrated circuits, the performance is heavily dependent on and limited by the input/output connections and the power consumption. However, photons can ideally overcome these limitations as they travel at a high speed (light) to carry and process information without significant loss compared to the movement of electrons through conductive materials, which is 60–70% of light speed depending on medium [9]. Furthermore, circuits based on photons exhibit lower energy usage as they encounter less resistance and they are also less influenced by electromagnetic interference leading to the possibility of long-distance data transmission and the multiplexing of signals in a single link [10] [11]. For data/signal communication purposes, communications based on electrical circuits may be initially more efficient in signal generation. However, it suffers from the increased losses over longer distances due to the increased resistance with the length of metal interconnects. Additional re-timers to minimise the bit error rate (BER) are required to compensate the loss and increase the power consumption, the cost to reduce the power consumption will increase rapidly with the increment in data rate and frequency of transmission compared to the cost spent on optical transmission. [12] Therefore, the research and development of PICs can serve as a valuable substitution or a complementary approach to traditional electronics circuits in applications that demand high speed, energy efficiency, and reliable long-distance signal processing as the commercial market is always driven by the cost and profits.

The research of silicon photonics started in 1980s [13] as silicon based photonic devices have characteristics such as low cost (especially compared to indium phosphide-based photonics, which is introduced in this section later), small footprint, and most importantly, complementary-metal-oxide-semiconductor (CMOS) compatibility [14]. Also, silicon can work as low loss waveguides interconnects and can be scaled up to 12-inch

wafers (this is also commonly used for standard CMOS facilities, while indium phosphide is just starting to get to 6-inch) [12]. These factors mean that silicon photonics can be developed rapidly and integrated hybridly with existing electronics integrated circuits technology, this extends the lifetime of current semiconductor's manufacturing technology/facilities, although silicon is a semiconductor material with indirect band gap and it may require additional light source and cooling systems to deal with the heat caused by more extra components and excited carriers inside indirect bandgap materials. [15] Low-loss waveguides in a thick silicon on insulator (SOI) process were demonstrated as some first application of photonic devices in early 1990s. [16] [17]

Subsequently, silicon photonics entered the small-scale integration (SSI) era, characterised by PICs comprising approximately 1 to 10 components on one chip. [18] After that, the silicon-based PICs were then pushed into commercial communication applications, 10 to 500 components (medium-scale integration, MSI) were successfully integrated onto a single PIC chip. Silicon photonics modulators [19] and transceivers [20] demonstrated competitive performance in applications of communications compared to III–V electronics devices [21] [22] [23]. Moreover, in this era, applications of silicon photonics were not limited in communications but expanded into biosensors [24].

In the current era, the integration of silicon photonics is moving into large-scale integration (LSI, 500-10000 components on a single chip) even very-large-scale integration (VLSI, more than 10000 components), and applications are now expanding into very wide domains. [18] [25] Commercial products and prototypes crossing LSI and VLSI silicon photonics PICs include LIDAR [26] [27], photonic switching [28], photonic computing [29] [30] [31], programmable circuits [32] and multiplexed biosensors [33] are demonstrated. In this era, silicon-based PICs always exist together with electronic ICs (EICs) in commercial products, and this may continue in the near future, especially in data communication fields. Usually, EICs serve the system by providing control, (voltage) bias and enabling E/O or O/E conversions of the end-to-end data, while PICs parts play the role of E/O or O/E converters and multiplexer/demultiplexer in these systems [34] and the components are interconnected by either waveguides or fibres [35].

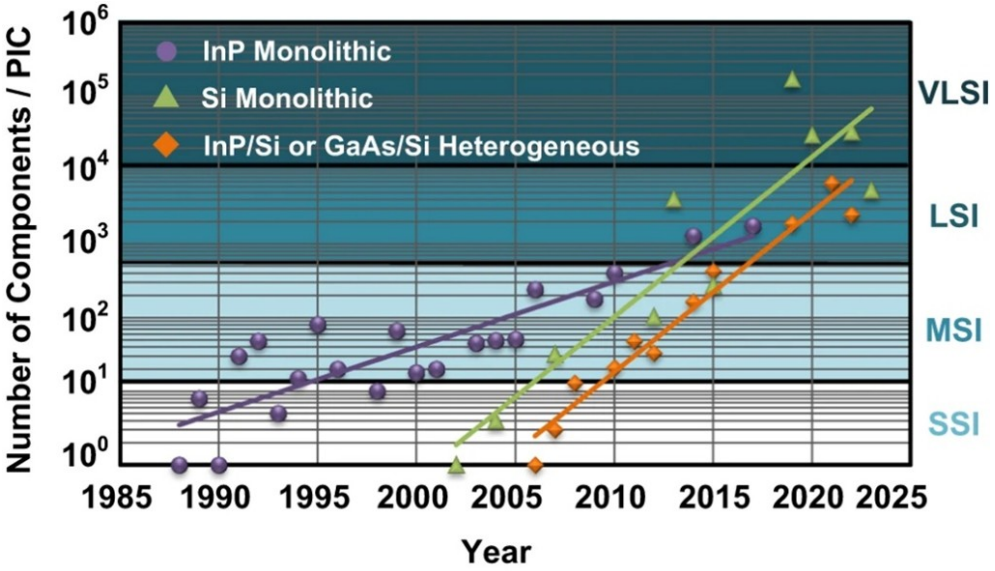

Figure 1.1: Timeline illustrating the evolution in the number of components integrated on silicon PICs across successive generations, including small-scale (SSI), medium-scale (MSI), large-scale (LSI), and very-large-scale integration (VLSI). [18]

In the future, the integration of PICs and EICs would be more common as they have rapidly transferred from device-level research to large-scale circuits on a single chip [36], and the global market of PICs shows robust growth driven by the proliferation of information and communication technology. [10] Also, the PICs will not be limited in silicon-based but also other materials such as gallium arsenide (GaAs) [37], indium phosphide (InP) [38], lithium niobate ($LiNbO_3$) [39] [40], 2D materials [41], polymers [42] and so on will be developed for different platforms and purposes. [43] Figure 1.1 [18] is a diagram indicating the level of the integration process varying with the year.

Notably, InP-based photonic integrated circuits, having been developed prior to silicon photonics, continue to attract significant research interests. [12] [18] [43] Benefits from its direct bandgap (different from silicon), mean it can emit photons while bias is applied, InP-based materials [44] are very good candidates for active components such as Distributed Feedback (DFB) lasers [45], semiconductor optical amplifiers (SOAs) [46], InP-based Mach–Zehnder modulators (MZMs) [47], photodiodes [48] and so on. Moreover, the applications of InP-based material are expanded into in-active components (passive components) like waveguides [49], resonators [50], Distributed

Bragg Reflectors (DBRs) and so on [51]. Additionally, but importantly for this project, InP-based NWs [52] are interesting devices as they could be both active and passive components dependent on the usage and a detailed introduction on NWs is given later in this chapter.

Therefore, InP-based monolithic PICs seem to be the most optimised solution for active optical emitters in the future as it offers the most comprehensive range of photonic functionality. However, the fabrication and integration processes of these devices are challenging and with high cost. The integration of InP-based PICs took around 23 years [44] [53] to reach the same level as Silicon monolithic PICs.

The development of silicon and indium phosphide PICs is complementary, representing two aspects of photonic integration. Silicon based PICs are cheap, easy to fabricate on current 12-inch wafers and compatible with current electronic integrated circuits, but with a lack of light sources and amplifiers. InP-based PICs have complete functionality but with lower manufacturing scale and higher fabrication complexity to integrate active and passive sections monolithically. Therefore, to realise a fully packaged PIC that incorporates both electronic and photonic functionalities, hybrid and heterogeneous integration [54] approaches are essential in the manufacturing of PIC-based systems, including those hybrid integrating PICs with electronic ICs (EICs). Specifically, the integration of InP components onto silicon-based PICs enables the combination of the strengths of both platforms, for example, providing light sources on low loss waveguides platforms. This approach not only makes use of the scalability and CMOS compatibility of silicon photonics but also benefits from the superior active photonic performance of InP, thus paving the way for reduced package size and enhanced functionality in nextgeneration hybrid PICs.

1.2 Hybrid and Heterogeneous Integration

The solution to combine different PICs components together is called integration, and integration processes can be divided into hybrid and heterogeneous integration. [54] These two integration methods are closely related, however, they refer to different methods of combining materials or components.

Hybrid integration refers to the post-fabrication assembly of photonic chips or devices, often from disparate material systems, into a single package. It is commonly used for integrating fully processed III–V semiconductor devices with PICs, especially silicon based, and it usually process at the packaging stage, refer to different integration methods. [54] Integrating an InP laser diode on passive silicon PICs [55] by wire bonds, flip-chip integration of vertical cavity surface emitting lasers (VCSELs) and a silicon PIC [56] and integration of InP NWs with polymer optical waveguides on a mechanically flexible substrate [57] through transfer-printing technology [58] are all examples of hybrid integration's applications. The main advantage of hybrid integration is the ability of testing and characterising each device before the integration. [54] Photonics components fabricated in a large number such as micro-pixelated light emitting diodes [59] and nanowire lasers [60] can be characterised and then selectively picked up from their original fabrication substrates for a high yield and better performance integrated PIC. However, this kind of integration is preferred for devices with relatively large sizes and low-density PICs, as the time consumption of accurate integration is long, which may be only suitable for research level assembly.

Heterogeneous integration may be the potential solution for the fabrication of PICs in industry. It combines different material platforms directly onto a single PIC chip during the early to mid-fabrication process. Integration of unprocessed (usually means un-patterned) III–V thin-films and pre-processed 12-inch silicon wafers [61] or Silicon Nitride PICs [62] are some examples of high-volume applications [63]. This method of integration provides similar performance as monolithic integration [64], but it provides high alignment accuracy, low loss and cost due to economy of scale. The only disadvantages for this method's application in university level of research is the strict

requirement of ultra-clean surface and the difficulty of modular test during the fabrication. However, this challenging point can be satisfied by semiconductor facilities and mature process control in modern semiconductor foundries. Figure 1.2 demonstrate the main difference between hybrid and heterogeneous integration from reference [54].

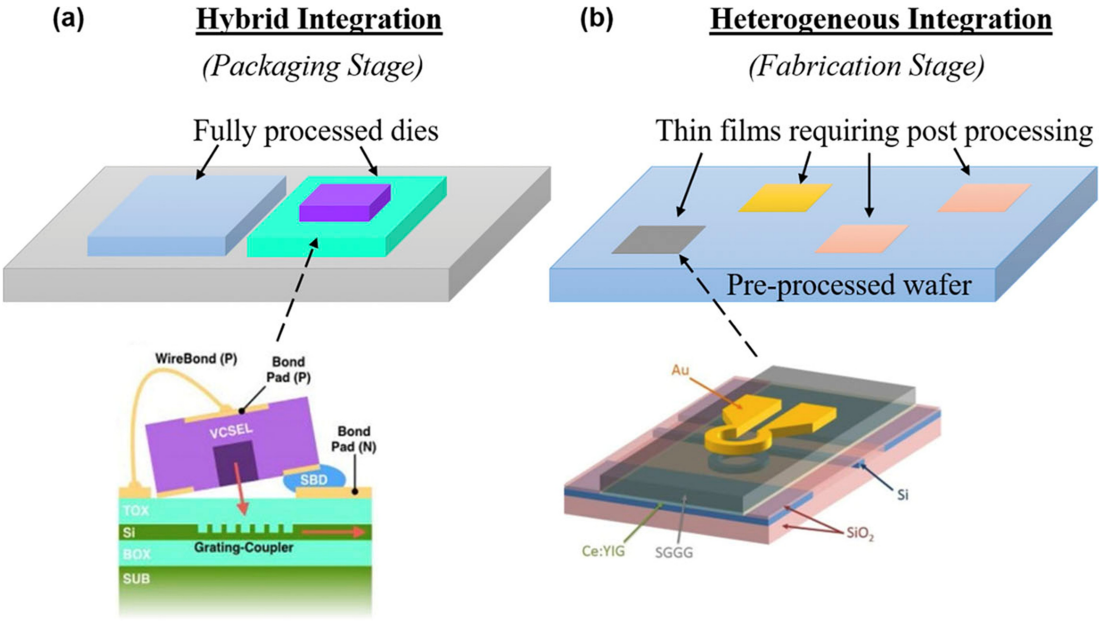

Figure 1.2: Schematic of (a)Hybrid integration of a VCSEL on a silicon on insulator (SOI) PIC [56]. (b) Heterogenous integration of an optical circulator. [65].

1.2.1 Integration Method

There are several different methods of integration depending on the way that optical components can be interfaced between different material platforms (grating coupling, mirror coupling [66], butt coupling [67], adiabatic tapers [68] and so on) and devices alignment. These methods including flip-chip [56], die and wafer bonding [69], direct growth [70], layer deposition [71] and the most important, transfer-printing [72] are briefly introduced in the coming paragraphs.

1.2.1.1 Flip-chip Integration

Flip-chip integration technique was first introduced and developed for the integration of electronic integrated circuits (EICs) with complex architectures and high density [73],

it is a mature packaging technique that connects chip dies to substrates by flipping the chip face-down and bonding it using conductive solder bumps. Flip-chip integration offers advantages [74] such as high integration density, low cost, excellent thermal management [75], low parasitic inductance for high-frequency performance ($\sim$ tens GHz level) [76], and the ability to pre-test dies before assembly [77].

In recent years, this integration method has been attractive for the integration of optical devices/components in PICs due to shorter interconnect length and improved heat dissipation. Not only the previously mentioned VCSEL diode bonded on top of a silicon PIC [56], but also some butt coupling applications like waveguide/fibre-towaveguide/fibre applications [78] and optical-amplifier-to-waveguides/fibres [79] that required precise alignment all benefit from flip-chip integration and result in high packaging scalability and low transmission loss.

1.2.1.2 Die and Wafer Bonding

Die and wafer hybrid bonding are emerging techniques that involve multi-step processes to form a robust and reliable connection between a component die and a substrate wafer [80], which was firstly developed for EICs and Micro-Electro-Mechanical Systems (MEMS). Different from flip-chip, which is using conductive bumps for bonding, it is a process of joining a die/wafer to a target wafer through precise alignment and surface-to-surface bonding at post-fabrication stage, an adhesive layer is optional during this process depending on the material [81] [69]. It provides the benefits of stacking only known-good dies that enhancing overall yield and enabling the bonding of dies with mismatched sizes. [82] This method has been promoted into PICs area since the development of hybrid EICs/PICs.

Both integration methods (with/without adhesive intermediate layers) have demonstrated wide applications of the integration of optical components in the past years. The range of integrated materials/devices on optical components such as waveguides varies from III–V semiconductors [83] to high quality thin films (magneto-optic materials [84] [65], non-optical materials [85] [86] and etc.)

1.2.1.3 Direct Growth and Layer Deposition

Direct growth and layer deposition are both monolithic integration processes. For direct growth, it is an epitaxial process [87] and techniques like metal-organic chemical vapour deposition (MOCVD) [88] and molecular beam epitaxy (MBE) [89] are representative. With these techniques, crystalline layers are grown, and semiconductor materials are integrated in a scalable manner. [54] Electro-optic active devices/components such as optical amplifiers, lasers, detectors and so on usually require this technique for the fabrication of substrates (GaAs on Si, etc.). The challenge of this method is to overcome the structural defects caused by lattice mismatch [90], for example GaAs on Si.

Different from direct growth, layer deposition does not require lattice alignment and is usually applied for the fabrication of passive optical components. Plasma-enhanced chemical vapour deposition (PECVD) [91] is a representative method of layer deposition to integrate materials on target PICs substrates. During this process, the deposited material transitions from a solid at the source into a vapor phase, travels to the target surface, and then transforms back into a solid, forming a thin film. It is easier and cheaper compared to the direct growth, but it cannot be used for crystalline materials. This method is an important heterogenous integration method especially for the fabrication of low loss optical waveguides and resonators, Si_3N_4 waveguides for example [92], on different PICs.

Table 1.1: Features of direct growth and layer deposition

Feature	**Direct Growth**	**Layer Deposition**
Crystal Structure	Crystalined	Amorphous
Cost	High	Low
Devices	Active	Passive, Coatings
Methods	MOCVD, MBE	PECVD, Sputtering

These two integration methods are both heterogenous integration methods, they both integrate thin layers/films of different materials on another target substrate for incoming photonic components fabrication steps, such as pattern definition, further hybrid integration and so on. A summary table is shown as following Table 1.1 to demonstrate the difference of these two integration methods, and a detailed section about the layer deposition (PECVD) is introduced in Chapter 2.

1.2.1.4 Transfer-printing

Transfer printing is a flexible micro-assembly technique widely used to integrate a broad range of materials and devices, including inorganic semiconductors (such as III–V compounds, silicon, and magneto-optic materials) [58] [93], organic materials [94] [95], metals [96], and most importantly, photonic components (LEDs [97], nanowires [98], etc.) Its strong manufacturing versatility makes it particularly well suited for diverse applications, including flexible/stretchable electronics [99] and PICs [100] [101].

Transfer printing is a type of pick-and-place integration, in which devices from one material system are picked-up from their original substrate (donor) and accurately positioned onto a target (receiver) substrate with the help of an elastomeric stamp. [36] Figure 1.3 (a) demonstrates a schematic of the transfer-printing process from left to the right. During both 'pick-up' and 'print' process, the adhesion between the elastomer stamp and the devices and the adhesion between the devices and the receiver substrate are all dominated by van der Waals' interactions [102]. The adhesion strength (energy release rate) is kinetically controlled by the peeling speed of the elastomeric stamp during the 'pick-up' and 'print' process. The detail can be found in reference [103] and the relationship between the adhesion strength (between the stamp and device) and stamp peeling speed is shown as Figure 1.3 (b) and (c) [54] [58]. In simple terms, the adhesion strength between stamp and device should be stronger than the adhesion strength between the device and the donor substrate during the 'pick-up' process. In contrast, during the 'print' process, the adhesion between the device and the target (receiver) substrate must exceed that between the device and the stamp. As shown in Figure 1.3 (b) and (c), the adhesion strength between device and the stamp is strong while the stamp contact with it is fast. Therefore, to pick up device from the donor substrate, quick contact and retrieval are required. To print, the movement of the stamp is slightly complicated, the stamp needs to move fast during the contact stage and then slowly peel back to favour high strength between device and receiver. Additionally, apart from pure kinetic energy control, the suspended structure on donor substrate created by etching during fabrication stage [36] and adhesion coating layer (for example, parylene C) [96] on the receiver substrate can also be applied to make

the transfer-printing process more convenient.

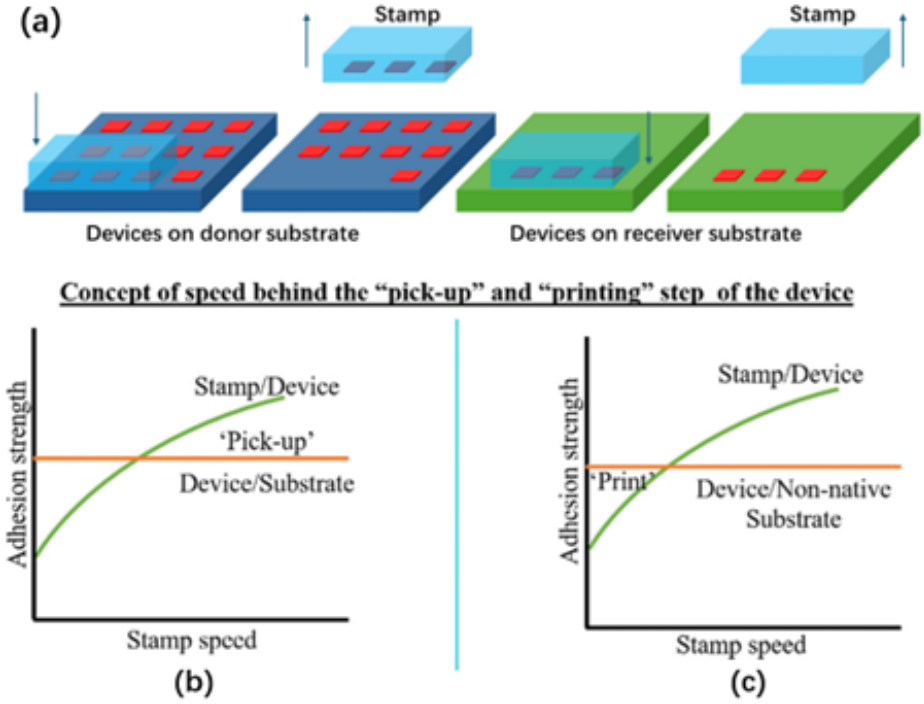

Figure 1.3: (a) Schematic of the full process of transfer-printing. (b) and (c) relationship between adhesion strength and peeling speed of the stamp. [54]

Key features of transfer-printing are the small scale of devices that can be handled (varying from nanometre to micrometre range, therefore, it is also called as μTP) and the high spatial accuracy and density of devices it can realise. To approach this, the fabrication of the stamp is key, and the material of the stamp is usually polydimethylsiloxane (PDMS), it can be easily structured into different shapes in small scale for different photonic components/membranes by moulding which is fabricated through pattern definition on silicon wafer. [104] Moreover, with the help of optical microscopes, computer vision and high-precision translation stages, current transfer-printing, especially within the integrated photonics group, University of Strathclyde, enables both serial and parallel integration of micro/nanoscale photonic devices with $< 350\,\text{nm}$ (3σ) average offset. [105] Many different ranges of active optical components onto passive optical devices layers have been demonstrated as it is more suitable for small elements (lasers on multiplayer silicon membranes [106], photodiodes [107], etc.)

with customised PDMS stamp compared to other integration techniques like flip-chip bonding. A detailed introduction of the fabrication process of PDMS in different forms and the transfer-printing process of different optical/photonic devices for different purposes is given in Chapter 2.

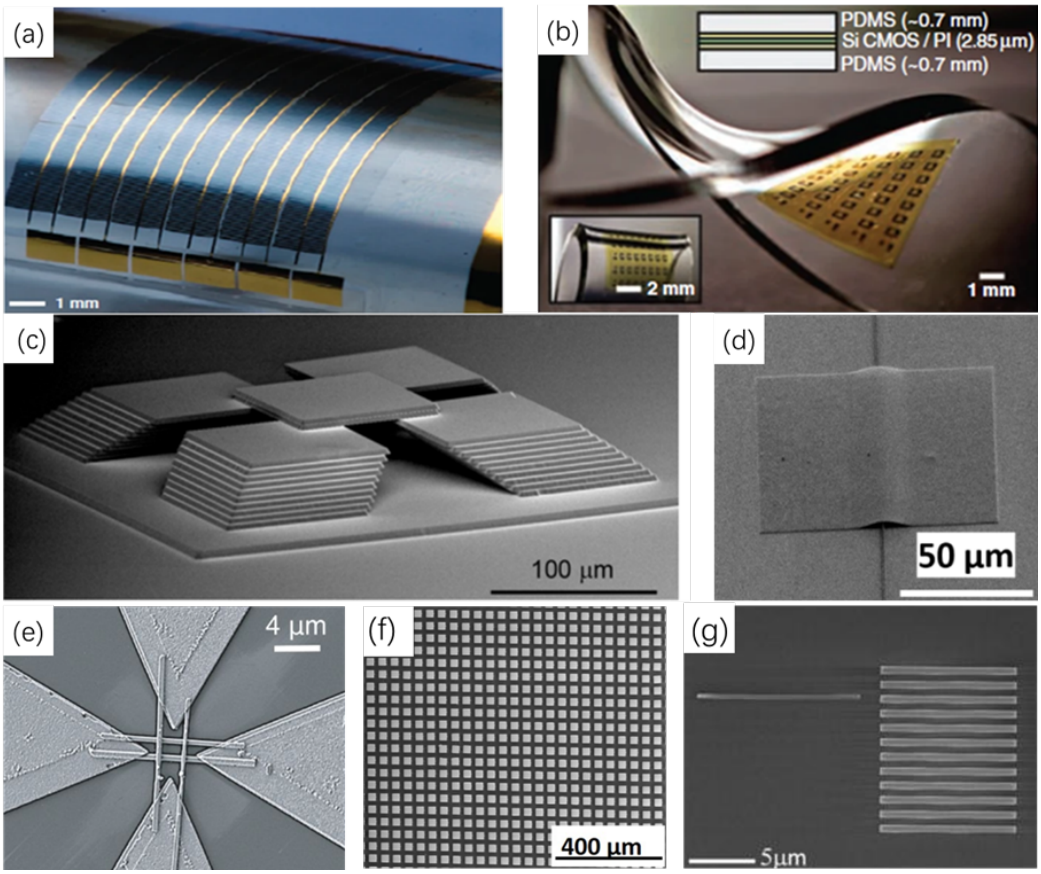

Figure 1.4: (a) A flexible photovoltaic module that utilizes large-scale arrays of silicon solar microcells, fabricated from bulk wafers and arranged in sparse patterns on non-native substrates through transfer printing. [108] (b) A silicon CMOS circuit designed for stretch-ability and foldability, transferred onto a poly PDMS substrate. [109] (c) Stacked flat silicon membranes through transfer-printing technique. [110] (d) A silicon membrane printed on a silicon substrate with SU-8 ridge structure. [111] (e) Terahertz detector with printed semiconductor nanowires. [112] (f) An array of transfer-printed QVGA array. [111] (g) A single nanowire (NW) device, transfer-printed and aligned with a Vernier scale. [105]

While micro-transfer printing technology demonstrates significant promise for enabling large-scale heterogeneous and hybrid integration in PICs, several technical challenges must still be addressed before it can be fully adopted for high-volume manu-

facturing. Key issues include the need for robust automation protocols that ensure consistent and repeatable device placement at the micron or nanoscale, as well as improved selective printing techniques that allow only high-performance or pre-tested devices to be transferred. Additionally, real-time in situ process monitoring remains a critical problem, as it is essential for ensuring yield, reliability, and alignment accuracy during each transfer-printing cycle. Figure 1.4 illustrates a variety of potential applications utilising micro-transfer printing, ranging from flexible and wearable electronics to advanced photonic integrated circuits. These diagrams highlight the versatility of the method in handling diverse material systems and device architectures, which is crucial for next-generation optoelectronic systems.

1.3 Micro/nanoscale Optoelectronic Components

This section presents a detailed overview of the micro- and nanoscale optoelectronic components employed in this PhD project. Emphasis is placed on the fundamental working theory, fabrication techniques, and functional roles of these components within the context of the proposed application. To provide a solid foundation for understanding their relevance and potential, a detailed literature review is conducted, highlighting representative studies and significant advancements in the field. Furthermore, both the advantages and limitations associated with current research involving these components are outlined, which lead to the motivation and aims of this project.

1.3.1 Photonic Crystal Cavity (PhCC)

A photonic crystal is a type of nanostructured material characterised by a periodically varying refractive index, as shown in Figure 1.5 (a). Similar to the electronic bandgap in semiconductor materials, the periodic refractive index modulation creates a photonic bandgap (PBG) which does not allow light propagation over a specific frequency range. As exemplified by a 2-D silicon photonic crystal slab [113], the periodic structure confines the light in the in-plane directions, and the high refractive index contrast between silicon slab and air cladding (~ 3.45 and ~ 1, respectively) traps the light in

the out-of-plane directions (total internal reflection at the interface).

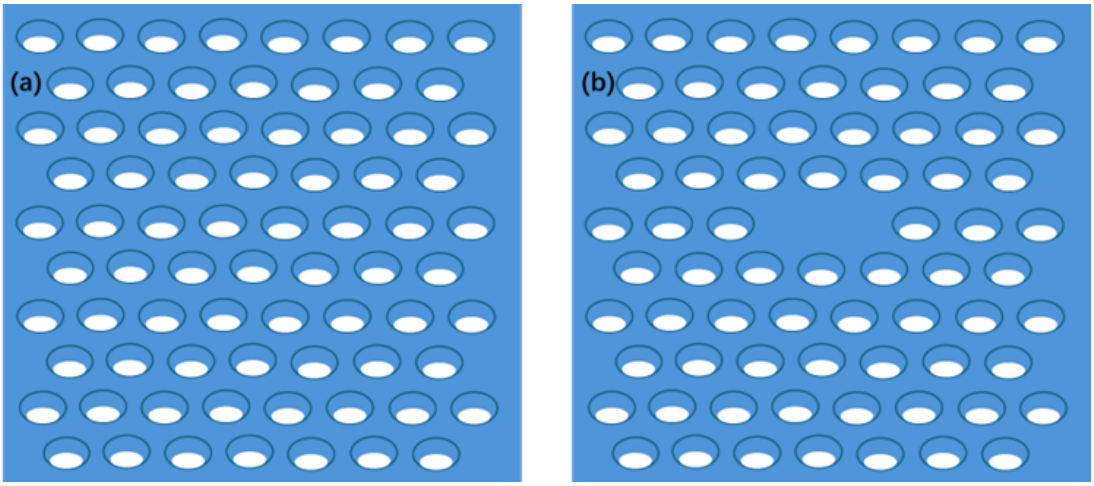

Figure 1.5: Schematics of (a) A 2-D photonic crystal structure. (b) A photonic crystal cavity structure by introducing a point defect.

Different functional structures such as waveguides [114] and optical cavities [115] can be realised within photonic crystals by introducing line defects and point defects, respectively. These defects are created by intentionally breaking the periodicity of the photonic crystal lattice, enabling the control of light propagation and confinement with high precision [113]. A line defect, formed by removing or altering a row of air holes (or dielectric rods), creates a photonic crystal waveguide [114] that allows light to propagate along a designed path, enabling precise dispersion control. In contrast, a point defect is typically created by modifying or removing a single unit cell, forms a cavity [116] [117] that traps light within a very small spatial region. A schematic diagram of a typical two-dimensional photonic crystal cavity is shown in Figure 1.5(b), illustrating the periodic lattice and the central point defect that defines the optical cavity.

Specifically, PhCCs created by point defects are capable of localising and confining electromagnetic energy within an ultra-small mode volume on the order of (or smaller than) a cubic wavelength (see Eq. 1.1).

$$V \sim \left(\frac{\lambda}{n}\right)^3 \tag{1.1}$$

Where, V is the mode volume, λ is the free-space wavelength and n represents the refractive index of the material [115]. This tight spatial confinement results in a high ratio of quality factor (Q) to mode volume (V), often denoted as Q/V, which benefits to applications involving light-matter interaction. A high-Q/V value indicates that the cavity not only stores energy efficiently but also concentrates the optical field in a very small region, conditions ideal for enhancing non-linear optical effects [118] or coupling to quantum emitters [119]. The quality factor (Q) shows the ability that a cavity can store energy, and it can be defined as Eq. 1.2.

$$Q = \omega_0 \cdot \frac{\text{stored energy}}{\text{power loss}} \tag{1.2}$$

Where, ω_0 is the angular resonance frequency of the cavity mode (in radians per second) [115]. Higher Q implies a longer photon lifetime and narrower spectral linewidth, allowing for more selective and sensitive optical responses, which enables a large range of applications like Spatial Light Modulators (SLMs) [120], optical amplifiers [121] [122], biosensors [123] and even in quantum photonics [124].

Currently, the fabrication of PhCCs is mainly based on techniques like deep ultraviolet (DUV) lithography and etching. [125] [126] Additionally, electron beam lithography (EBL) has offered the highest resolution and accuracy, but the sub-micron geometric features required for achieving high Q/V ratios are highly sensitive to fabrication-induced variations. Nanometre-scale deviations can result in shifts in the cavity's resonant wavelength. [127] [128] Therefore, direct fabrication of cavity membranes with identical resonant wavelength is nearly impossible with existing techniques.

To compensate for the fabrication induced wavelength shift, post-fabrication tuning methods such as photo-induced carrier injection and thermal tuning can be employed. [129] [130] However, such approaches become increasingly challenging when applied to densely packed arrays of PhCCs. In these scenarios, the design and usage of customised pumping sources, such as micro-LED arrays [131] that are spatially matched to the layout of the photonic crystal cavity array, may be required to enable individual and localised tuning of each cavity with different shifted resonant wavelength. This technology is technically complex and continues to be the subject of active research.

Alternatively, the array of photonic crystal cavity membranes can be individually characterised, grouped, and selectively integrated (printed) onto a target substrate post-fabrication. This is enabled by a high-precision transfer-printing technique introduced in the previous sections. In this research project, an array of custom-designed silicon photonic crystal cavity membranes with resonant wavelengths around 1550 nm was fabricated by MIT, specifically engineered to function as spatial light modulators (SLMs) within the telecommunication wavelength range. [131]

To enable the characterisation and reconfiguration of PhCC membranes by using transfer-printing and in-situ optical measurement, a suspended membrane structure is required to be designed. Such suspended designs can not only realise the print of the devices but can also enhance out-of-plane optical confinement when combined with a bottom reflector.

In this project, the membranes should be proven that they can be picked up and printed by a PDMS stamp on a designed structure in different materials to make the active area physically suspended. Different transfer-printing set-ups may be applied for different purposes and higher printing yield. A transfer-printing set-up with in-situ measurement can be applied to characterise, selectively pick-up, print and group them based on measured resonant wavelength. A high yield array of PhCC membranes is realised to demonstrate the potential of integration of photonic components of high densities. The complete fabrication, integration process and results are described in Chapter 3. This approach to integrate micro-scale photonic devices offers a promising pathway to overcome fabrication-induced variations, paving the way for high-performance photonic integrated circuits (PICs) with greater flexibility, scalability and uniformity.

1.3.2 Semiconductor Nanowires

Driven by requirements for systems' scalability, smaller optical components are a focus of significant research efforts. Semiconductor-nanowires are quasi-one-dimensioned (1-D) nanostructures with diameters ranging in hundreds of nanometres level and with length up to millimetres-scale. [132] The research of these 'wires' was started in 1964

by growing silicon 'micro-wires' or whiskers using Vaporous Liquid Solid (VLS) process with gold as catalyst to support the requirements of scalability in integrated circuits. [133] [134]

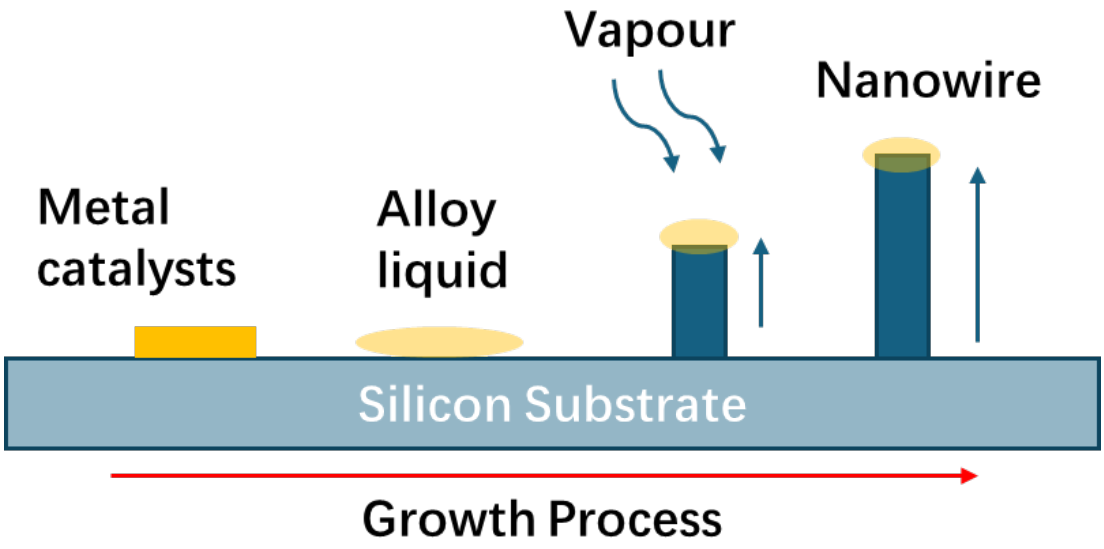

Figure 1.6: Schematic illustration of different stages (from left to right) of the growth process of silicon nanowires with VLS technique. Reproduced based on reference [132].

By the 1990s, advancements in nano-fabrication techniques enabled the miniaturisation of these structures into the nanometre scale, giving rise to what we now classify as semiconductor nanowires or nano-whiskers [135], and the materials are not limited to silicon but are now available in oxides [136], III–V compounds such as GaAs and InP [137] and other elemental semiconductors [138], and the growth of these nanowires in different materials were still heavily inspired by the VLS process. A schematic in Figure 1.6 illustrates the complete growth process of a silicon nanowire using the Vapor-Liquid-Solid (VLS) technique. In this method, metal catalyst nanoparticles, gold, are first deposited onto a silicon substrate. The system is then heated to a temperature sufficient to form Au−Si alloy liquid. Subsequently, a silicon precursor gas (in this case, silane, SiH_4) is introduced into the growth chamber, where it decomposes to release silicon atoms. These atoms dissolve into the liquid alloy droplet. Once the droplet becomes supersaturated with silicon, crystal growth is initiated at the liquid–solid in-

terface, leading to the formation of a silicon nanowire beneath the catalyst droplet [134].

The development of growth technique realises stable fabrication of nanowires and enables a broadband range of applications. Among these, the earliest and most prominent applications have emerged in the field of electronics, like other semiconductor technologies. Notably, the introduction of uniformly doped nanowires has facilitated the development of junction-less transistors, which eliminate the need for complex doping profiles between the source, drain, and channel regions. This simplification of the device architecture not only reduces short-channel effects but also improves overall electrical performance [139] [140]. The optimised transistor design and integration of semiconductor nanowires (Si, Ge, etc.) into field-effect transistors [141] [142] enable better performance CMOS circuits for applications like logic circuits [143], wearable electronics [144], biosensing platforms [142] and non-volatile memory [145].

Nanowire research has since evolved from electronic applications into the fields of optoelectronics and photonics, with growing research interest shifting from purely electronic integrated circuits (EICs) to hybrid electronic-photonic integrated circuits (EICs/PICs), or even fully photonic systems.

The research and applications of nanowires in such areas started with the first demonstration of room-temperature ultraviolet nanowire lasing. [146] During this process, the carrier injection through optical/electrical pumping [147] [148] can generate more electrons in the excited state in the direct bandgap semiconductors, while a photon stimulates one excited electron to recombine with a hole in lower energy level, a second photon which is coherent with the first one is then emitted. In nanowires, the two end facets serve as mirrors and the ultra-small sub-wavelength mode volume that provide optical confinement naturally form a Fabry–Pérot cavity [149], enabling optical feedback without external mirrors, also, the gain media such as multiple quantum wells/dots inside boosts light-matter interaction. These characteristics provide sustained stimulated emission and are necessary for nanowire lasing. [150]

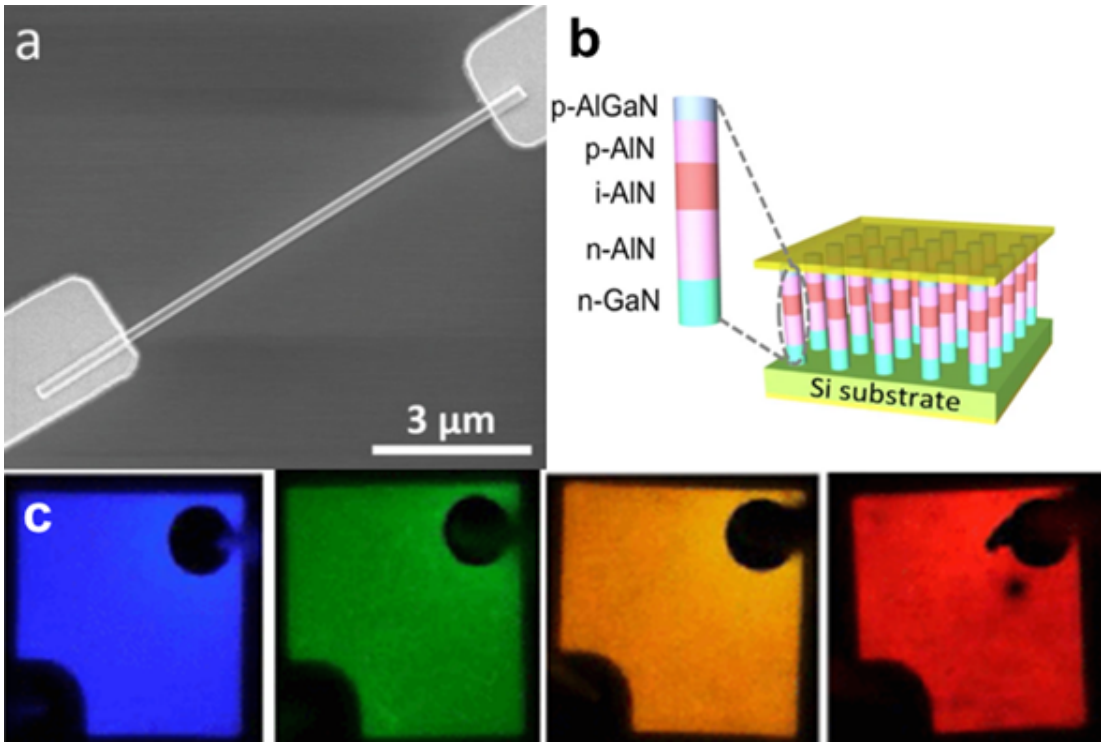

Figure 1.7: (a) A single horizontal nanowire solar cell. [151] (b) A schematic of an Aluminium nitride LED. [152] (c) Nanowire LEDs (emitting area: $250\,\mu\text{m} \times 250\,\mu\text{m}$) with different wavelength. [153]

The capability of room temperature lasing makes semiconductor nanowires (especially III–V materials) potential candidates for on-chip light sources or quantum light sources for PICs. Also, highly efficient semiconductor nanowire-based light-emitting diodes (LEDs) can be realised to push the development of micro-LED displays and on-chip optical communications. [153] [152] Moreover, because of the high refractive index contrast ratio and small volume (leading to high Q/V) makes nanowires attractive to solar cells or as sub-wavelength waveguides for solar panels, on-chip signal processing and ultrafast optics. [154] [151] [155] Figure 1.7 includes some devices and schematic of the devices and design based on nanowires.

With the development in both electronics and photonics, the fabrication processes have also progressed. Depending on the growth direction, these methods can be divided into bottom-up and top-down growth. The first introduced VLS method is a representative bottom-up method. Apart from this, other methods such as vapour-

solid (VS) growth, solution-liquid-solid growth (SLS), [156] chemical vapour deposition, metal-organic chemical vapour deposition (MOCVD) and molecular beam epitaxy (MBE) [157] also enable the fabrication of nanowires across a wide range of materials and temperatures, depending on the specific application requirements.

Within all these new developed methods, both MOCVD and MBE methods are notable, as they can provide atomic-scale control compared to other material deposition methods (either liquid or vapour deposition). Both MOCVD and MBE are well-established in the epitaxial growth of laser diodes and LEDs, and the advantages they offer in thin-film deposition are directly inherited in nanowire fabrication. As a result, these techniques enable the scalable synthesis of high-quality III–V semiconductor nanowires with minimal defects and relatively good uniformity compared to the nanowires fabricated through other methods. However, these techniques have some limitations. For MOVCD, the uniformity is heavily influenced by the precursor flow and temperature (which is very high and can induce thermal mismatch stress), but this can be significantly improved by selective area growth. For MBE, primary problems stop it from large-scale nanowire arrays fabrication is the growth rate (for atomic-scale control) and the requirement of ultra vacuum.

The customised indium phosphide (InP) nanowires (NWs) used in this research project were fabricated via selective-area metal-organic vapour-phase epitaxy (SA-MOVPE, also referred to as SA-MOCVD) at The Australian National University. [52] These InP NWs exhibit high quantum efficiency and are capable of room-temperature lasing. [158] While SA-MOVPE ensures good uniformity in nanowire diameters, variations in nanowire length may occur due to non-uniform precursor flow. These dimensional inconsistencies can affect the lasing characteristics, such as the emission wavelength and threshold power. [159]

To address the issue of length non-uniformity in nanowires, two primary approaches can be employed. The first involves the use of transfer-printing technology to characterise, select, and assemble nanowires that exhibit similar optical and structural performance, and this was previously realised by our research group. [60] Alternatively, top-down fabrication techniques [160] [161] can be applied to achieve greater control

over nanowire length uniformity. In a typical top-down process, a semiconductor layer with a user-defined thickness is first deposited or grown on a substrate. This is followed by laser lithography, which defines the desired spatial pattern on a resist layer that has been spin-coated onto the deposited semiconductor layer. Subsequently, chemical etching can provide precise vertical control and form the nanowire from top surface down to the substrate. However, the overall quality of the resulting nanowires may be affected by the resolution limits of the lithography technique and potential surface defects [162] introduced during the etching process.

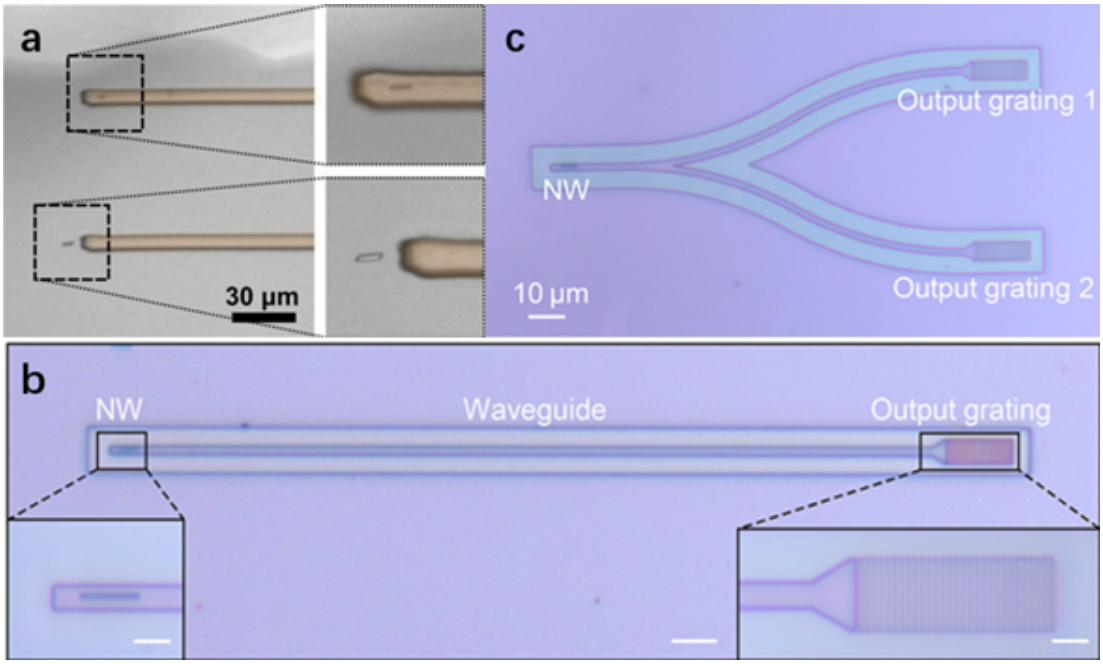

Figure 1.8: (a) Nanowire printed on and next to SU-8 waveguides on flexible glass. [57] (b) A hybrid polymer-SiN waveguide with an InP NW integrated inside. (c) A hybrid polymer-SiN power splitter with an InP NW integrated inside. [163]

Several studies have been conducted both within and outside the research group (shown as Figure 1.8) based on these InP nanowires. In 2017, in the research done within the research group, NWs were placed on or next to the facet of a polymer SU-8 waveguide on flexible glass through transfer-printing technology, then NWs were optically pumped by a pulsed laser (532 nm). [57] In this research, NW lasering were successfully realised and the emission coupled with polymer waveguides. Additionally,

some basic PICs functions are presented, including power splitting and wavelength multiplexing [164]. In 2022, another research represented using a tungsten probe and electron beam lithography (EBL) to embed InP nanowire with polymer waveguides on a SiN slab. [163] The work demonstrated laser coupling, Y-splitter operation, and wavelength-division multiplexing (WDM), where the nanowire laser emission propagating along the hybrid waveguide and could be extracted through output gratings, validating the on-chip coupling and signal transmission capability.

In most cases, the optical excitation and manipulation of nanowires (NWs) rely heavily on the use of pumping lasers. However, this approach presents several challenges, as pumping lasers are typically bulky, consume significant power, and requiring accurate optical alignment. These drawbacks prevent the improvement of scalability and further target applications. Therefore, exciting or modulating coherent light using incoherent light sources (LEDS, etc.) represents a critical step toward achieving low-cost, highly integrated, and flexible photonic applications.

1.3.3 Micro-Light-Emitting-Diodes (μLEDs)

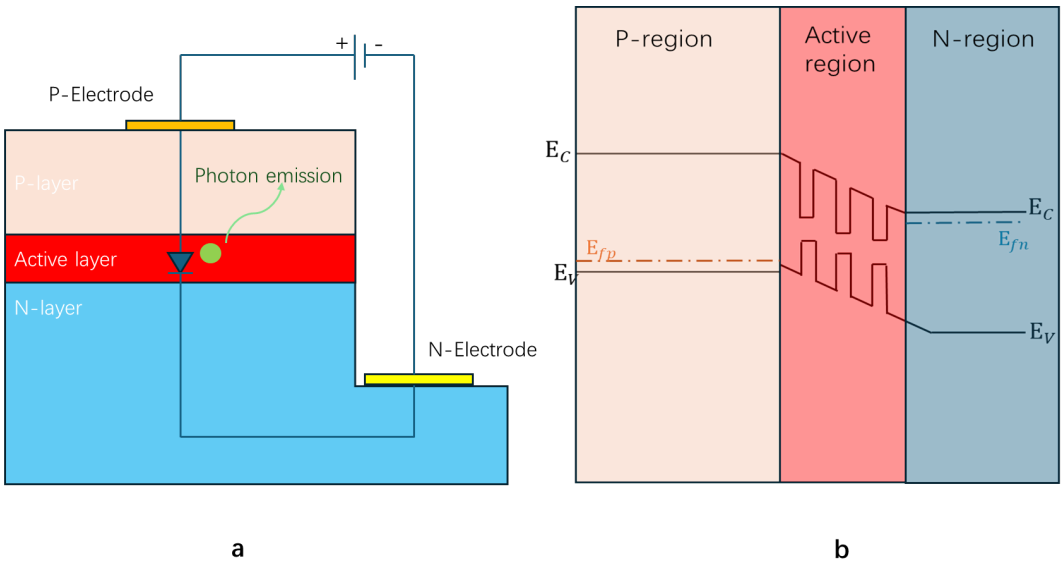

Figure 1.9: Schematic of (a) Micro-LED structure. (b) Energy band of MIcro-LED with MQW active layer under a forward bias.

A light Emitting Diode (LED) is one of the most widely used source of incoherent light. It is a straightforward device based on a p-n junction structure, typically fabricated from direct bandgap semiconductor materials. Within the p and n regions without applied bias voltage, the majority carriers are holes and electrons respectively. Electrons from the n-region move toward the p-region and holes from the p-region move toward the n-region when a bias voltage applied and the diffusion rate of both carriers increased. These carriers meet in the junction region, where electron-hole recombination occurs, resulting in the emission of photons. Elemental semiconductors do not exhibit direct bandgaps, instead, compound semiconductors such as GaAs, GaP, and GaN possess direct bandgaps. The wavelength of the emitted light depends on the bandgap energy of the material, allowing emission to range from ultraviolet to infrared. [165]

The development of LEDs began in the 1960s, starting with the first practical infrared LED demonstrated in 1961 [166], followed by the first visible-spectrum (red) LED in 1962 [167]. Advancements across the spectral range continued, notably with the invention of the blue LED by Isamu Akasaki, Hiroshi Amano, and Shuji Nakamura in the early 1990s [168]. These breakthroughs enabled the creation of white LEDs, achieved either through phosphor conversion [169] [170] or RGB colour mixing [171] [172], which have since become foundational technologies for lighting and display applications.

The innovations in microfabrication, materials science, and integration techniques support the growing demand for compact, efficient, and high-resolution light-emitting devices across industries, from consumer electronics to biomedical optics and quantum photonics. These all requires the scalability of LEDs, therefore, the research of micro-LEDs (μLEDs) has been conducted for the past two decades since the first demonstration in 2000. [173]

Micro-LEDs are light-emitting diodes with an emission area typically smaller than $100\,\mu$m in each dimension. [174] This extra small size enables enhanced pixel per inch (ppi) of modern displays with higher brightness and better contrast. [175] Compared to conventional broad-area LEDs, micro-LEDs offer significantly higher power density and can operate at higher current densities. These advantages are attributed to improved thermal management [176], reduced current crowding [177], and enhanced light

extraction efficiency [178]. Apart from application as next-generation of self-emissive displays, micro-LEDs play an important role in visible light communication (VLC), as the advantages previously mentioned make micro-LED have faster transmission rate. Figure 1.9 (a) is the schematic of a typical micro-LED structure with Multiple Quantum Well (MQW) layers (active layer) [179] under a forward bias. Within the active region, the injected electrons and holes are confined in the lower-bandgap quantum wells, where their increased spatial overlap enhances radiative recombination and leads to efficient photon emission. The corresponding energy band is shown in Figure 1.9(b).

In 2012, researchers in University of Strathclyde developed several Gallium Nitride (GaN) based micro-LED arrays with different emission wavelengths, they have independent CMOS control to provide high modulation speed ($> 400\,\text{MHz}$) for VLC. The prototype device is shown as Figure 1.10 (a). [180] In 2020, a suspended micro-LEDs structure which is designed to be transfer-printed was developed because of the availability of GaN epitaxy on silicon, they demonstrate the capability of integration onto different substrates like diamond, glass and CMOS circuits. [97] [181] The devices diagrams are shown as Figure 1.10 (b) and (c), respectively. This research improved the micro-LEDs in speed, integration methods and scalability.

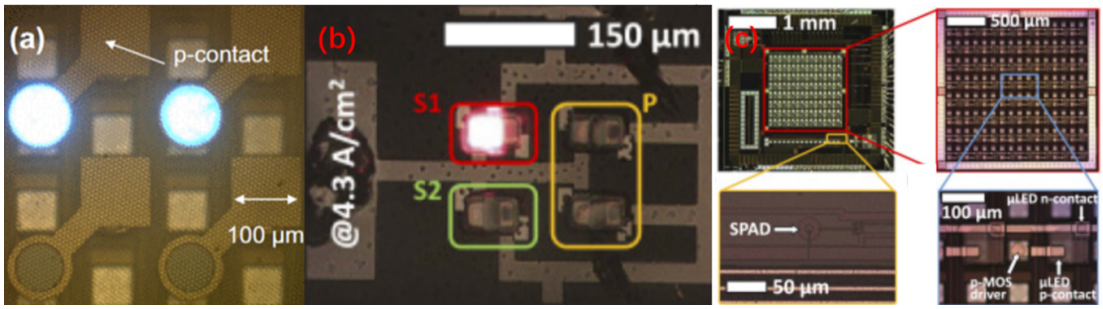

Figure 1.10: (a) Prototype micro-LEDs array of a 450 nm peak emission with CMOS control designed for VLC. [180] (b) A 2×2 micro-LEDs array printed on glass substrate. [181] (c) Diagram of the CMOS chip featuring an 8×8 array of transfer-printed micro-LEDs. [97]

The micro-LED incoherent light sources were applied in this research project, based on a high-speed micro-LED array (405 nm, violet) integrated with CMOS control, to provide individual control on pixels, customised especially for nanowire excitation. [182]

The single pixel with 72 μm diameter from the 16×16 array can demonstrate approximately 245 MHz of modulation bandwidth. If the array demonstrates the ability to excite the InP nanowire mentioned in the previous section, or even make it lasing, it would be the first time that the nanowire laser is pumped and manipulated by an incoherent light source. With the employment of transfer-printing, there is a chance that an array of NWs can be optically excited and modulated following the micro-LED arrays modulation bandwidth. In Chapter 4, the detailed processes including integration, optical pumping, modulation and measurement is described in detail.

There are also suspended micron-scale LEDs pixels structure available. The possibility of the implementation of a full on-chip design containing pumping source (micro-LED pixels), nano-scale emitters (InP NWs), and interconnect optical components (polymer waveguides), is going to be discussed in Chapter 5.

1.3.4 Summarised Motivations and Aims

As the demand for high-performance photonic integrated circuits (PICs) continues to grow, there is an increasing need to integrate different functional components within a compact on-chip system. However, traditional monolithic large-scale fabrication methods are reaching their limits like material incompatibility, complex processing requirements, poor device uniformity, and high production costs. These challenges pose significant barriers to scaling and customising PICs for next-generation, high-density, and multifunctional applications. This drives the pursuit of alternative integration strategies that offer greater flexibility, efficiency, and scalability.

In this project, transfer printing serves as a key solution to address fabrication-induced variations that arise during the large-scale production of microscale photonic devices. It also offers an efficient packaging strategy for integrating micro/nano-scale photonic components onto target PIC platforms, such as CMOS or flexible substrates. By enabling massively parallel assembly and accommodating a wide range of material systems, this technique makes the development of highly functional and scaled integrated photonic systems easier.

1.4 Summary

This chapter has given a brief introduction on the development of photonic integrated circuits and reasons that PICs can enhance electronics integrated circuits in the future. Different integration methods play important role in the fabrication of either single optical components or wafer-scale PICs, especially the micro-transfer-printing technique which is researched and employed widely in University of Strathclyde. The working principle and development of micro/nanoscale optoelectronic components like photonic crystal cavities (PhCC), semiconductor nanowires (NWs) and micro-scale light emitting diodes are reviewed. Key examples and state-of-the-art performance metrics for these technologies were highlighted from the literature. To conclude the main theme of this research project, the technique of micro-transfer-printing provides photonic integrated circuits with more uniformed components and higher scalability.

Chapter 2

Experimental Techniques for Fabrication and Micro-Assembly of Semiconductor Photonic Devices and Photonic Integrated Circuits

In this chapter, the techniques applied for the fabrication of micro-chips used in Photonic Integrated Circuits (PICs) applications as receiver substrates in this specific project are introduced and discussed. There are three main sections in this chapter. In the first section, the detailed techniques of fabrication of a silica-on-silicon platform used for fabricating mechanical supporting structure for the transfer-printing of Photonic Crystal Cavities Silicon (PhCCs Si) devices is presented. The second section contains the fabrication of the passive interconnect photonic devices on glass platforms based on polymer materials. As the micro-assembly and integration technique was applied at different points in both of the fabrication processes, the printing of PhCCs devices (at the end of the first fabrication session) and Nanowires devices (in the middle of the second fabrication session), will be introduced in the final section of this chapter.

2.1 Fabrication Processes of Silica Frames on Silicon Platforms

This section introduces the detailed techniques used in the complete fabrication process of patterned silica frames on a silicon substrate, including cleaning, material deposition, lithography, and etching.

2.1.1 Sample cleaning: Wet and Dry Cleaning

In 1970, the first complete cleaning recipe specifically designed to clear Si surface from particles, metallic, and organic contaminants was proposed based on scientific considerations. [183] [184]

It is hard to keep devices absolutely clean during the fabrication and transition process with particles and metallic contamination are orders of magnitudes smaller than in early years [183], though most of the semiconductor devices or substrates are carefully fabricated inside a clean-room. Different type of contamination will cause different influence on target devices' characteristics. [185]

Also, the more steps involved in the full process, more unwanted pollution may be introduced. To ensure good devices and high yield of fabrication, it is important to offer multiple cleaning options. Effective cleaning processes activate and prepare the surface for subsequent steps, ensuring strong adhesion of resists and deposition layers and resulting in high-quality die. [185] Chips fabricated in this PhD project are mainly for micro-transfer-printing, thus, the surface cleaning level is a key factor influencing the printing quality.

2.1.1.1 Wet Chemical cleaning

In this project, the fabrication started from acetone solvent cleaning. It can dissolve organic impurities, especially oily or greasy contaminants. This step can work with ultrasonic clean to remove most of the contaminants left on the substrate surface. However, the acetone solvent can evaporate rapidly and redeposit the contaminants on the target surface. Hence, Methanol solvent is introduced right after acetone solvent

Figure 2.1: Chemical Benches in the wet process room for wet chemical cleaning. (From left to right, acid bench, developing bench, solvent cleaning bench and photoresist spinning bench)

cleaning to dissolve the acetone's contaminants, and does not evaporate quickly. Then Isopropyl alcohol can be used as a rinse agent to remove both of the methanol and left undissolved acetone contaminants, lift and clean the particle on the chip surface further. Finally, the isopropyl alcohol left is removed by rinsing the sample under the deionised water (D.I. water) and the surface can be dried by applying a nitrogen gun.

Additionally, in some cases, some organic contaminants on the target substrate surface are hard to remove by the cleaning procedure mentioned previously. Piranha solution treatment [186] is introduced to deal with this specific solution. Piranha solution is a high molarity mixture of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2), as a strong oxidizing agent, most organic matter will be decomposed by it. If there are some organic contaminants left on the substrate surface, like polymer or exposed photoresist, the substrate (Si and glass substrate, specifically) can be cleaned by the solution and then rinsed with D.I. water. The surface hydrophilicity [186] of the substrate would also increase after piranha solution treatment, and this can make the

micro-assembly on substrate easier. All these wet chemical cleaning processes are operated on the chemical benches shown as Figure 2.1 depends on the usage of chemical reagents.

2.1.1.2 Dry Cleaning (Oxygen plasma cleaning)

Plasma cleaning is widely used in wafer surface cleaning, for both semiconductors and metal surfaces such as Ge [187], Si [186] [188], Au and PtIr [189]. The dry cleaning will be conducted twice in the fabrication, the first one is after wet chemical cleaning and the second one would be operated after photoresist development to remove unexposed photoresist.

Figure 2.2: Matrix: the plasma asher used for oxygen plasma cleaning in the dry process room.

The oxygen plasma cleaning in this project is operated inside the chamber of a Matrix plasma ashing tool demonstrated as Figure 2.2. The radio frequency (RF) circuits inside Matrix create a high-frequency electromagnetic field, interacting with the oxygen gas inside the chamber to create plasma containing highly reactive oxygen species,

including ions, free radicals and atomic oxygen. These highly reactive oxygen species interact with contaminants on the surface of the sample (contaminants after wet chemical cleaning or undeveloped photo-resist) and break them down into CO_2 and water that can be easily evacuated from the chamber at 150°C. Other particles or oxide layers can also be etched away physically by the energetic ions in the oxygen plasma. The dry cleaning program is set to be 10 minutes inside Matrix. The oxygen plasma cleaning can also increase the surface energy and hydrophilicity significantly compared to other cleaning methods [186], this would improve the adhesion for subsequent procedures.

2.1.2 Pattern Definition

2.1.2.1 Plasma-Enhanced Chemical Vapour Deposition

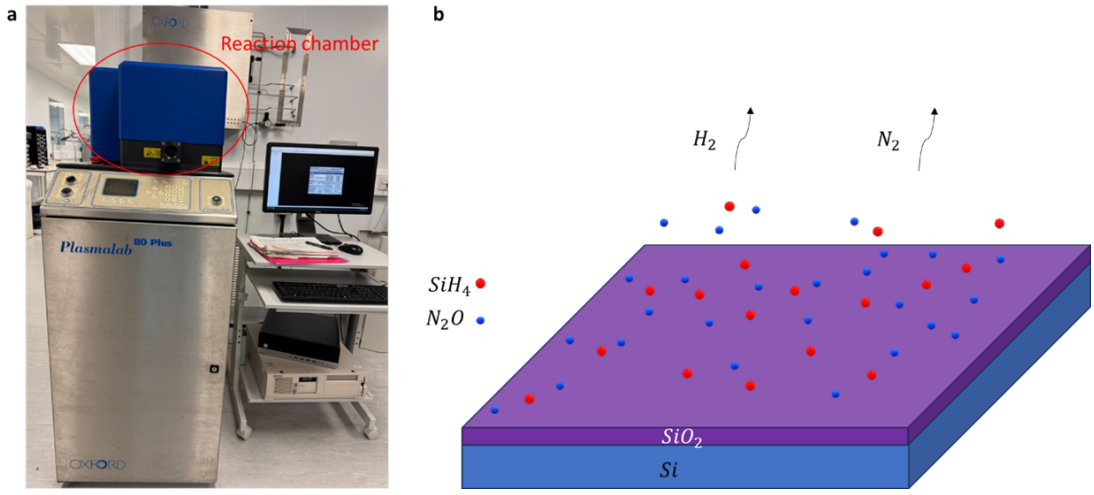

Figure 2.3: (a) Oxford Plasma 80 Plus System used for PECVD. (b) Schematic of the reaction process inside the PECVD machine chamber.

In the project, SiO_2 was chosen to be the material for the mechanical supporting frames as it is both stable and and its thickness is more controllable than photoresist by applying Plasma-Enhanced Chemical Vapour Deposition (PECVD). The deposition in this work was done in an Oxford Plasma 80 Plus System (Figure 2.3, a). PECVD is a hybrid CVD process [91] using plasma energy to drive the reaction between excited species and the substrate rather than using thermal energy only for thin films depo-

sition. The cleaved and cleaned Si substrate would be placed on the heated electrode (300℃) inside the chamber (process pressure: 1 Torr), where the sources gases are activated (by the electromagnetic field created by the RF in 70W), reacted and diffused. The reaction formula of the SiO_2 thin film is:

$$SiH_4 + 2\,N_2O \longrightarrow SiO_2 + 2\,H_2 + 2\,N_2$$

The SiH_4 and N_2O gas flow at 170sccm and 710sccm, respectively. This makes the deposition rate of the silica at $\sim$ 34 nm/min. A layer of silica in $\sim$ 1550 nm was deposited on the silicon substrate at this rate for the subsequent fabrication processes. Figure 2.3 (b) is the schematic of this process.

2.1.2.2 Photoresist Spin Coating

Photoresist is an organic material which is sensitive to UV light, it is used widely in photolithography or laser lithography to form patterns. Also, it can act as a protection layer during etching processes to transfer patterns from photoresist layers into the deposited oxide layer mentioned previously. This process can be found in reference [190].

There are two types of photoresists, positive and negative. Positive photoresist becomes more soluble after UV exposure while negative photoresist becomes extremely difficult to dissolve in development solution after exposure. They can show very different profile after exposure and development. Therefore, they have their own advantages in micro-fabrication. [190]

The photoresist chosen for silica pattern definition is S1805. It is a positive photoresist. In this project, the photoresist was dropped onto the Si sample with Silica deposited through a syringe with a filter (to filter bubbles and keep the photoresist in a unified thickness). The spinner placed on the wet bench (the right one shown in Figure 2.1) spun the sample at $\sim$ 3800 RPM, and the thickness of S1805 was around 500 nm [191] after the spinning. The sample was then placed onto a hot plate (115℃) for one-minute soft baking and prior to the lithography.

2.1.2.3 Photolithograph, Maskless Laser Lithography and Development

Photolithography is using a mask aligner (Karl Suss MA6 mask aligner [192]) to write patterns in coated photoresist mentioned before, which is sensitive to UV light. The exposed area of photoresist would be dissolved in developer (for S1805, the developer would be micro-developer: D.I. water in 1: 1 ratio), and the unexposed area of photoresist would stay on the top of the sample and work as a protection layer during the etching process. The sample can be cleaned by rinsing in D.I. water after development process.

Different from mask-based photolithography, there are no hard chrome glass masks needed in laser lithography, so it is also called maskless lithography. It is a high-precision technique used for semiconductor devices' micro-fabrication [193], it employs a focused laser beam to directly write patterns into photoresist. Compared to photolithography with masks, it might be more time consuming during exposure, but it provides higher resolution and can create more complex patterns. It also allows for fast prototyping and it does not rely on the creation of the mask sets needed by mask aligner photolithography.

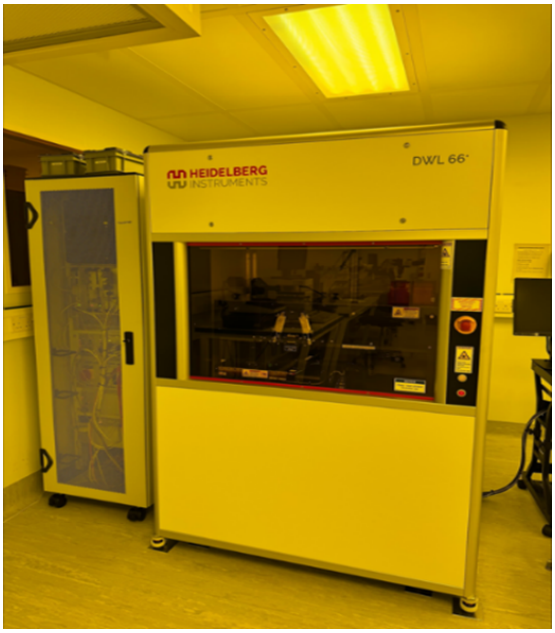

Figure 2.4: Heidelberg DWL66+ laser lithography system placed in wet process room.

The Heidelberg DWL66+ laser lithography system [194] (Figure 2.4) was applied in this project to create patterns of frames (the designed digital mask is shown in **Chapter 3**). There are two lasers embedded inside this system, a 375 nm UV laser for exposure and a red interferometer laser used for scanning and helping with focus process. The system would read the digital masks created through design software like Klayout, align and expose the desired patterns by the UV laser. The exposure parameters such as laser power, intensity and optical focus point are all customisable. Dosage tests are needed before exposure. The development of the exposed sample is exactly same as the conventional UV photolithography.

Figure 2.5 demonstrates the full process of the pattern definition with the laser lithography, designed patterns are transferred onto spin coated photoresist with the help of laser lithography and photoresist development. The undeveloped photoresist would work as a protection layer during the Reactive Ion Etching process to transfer patterns from photoresist onto silicon dioxide materials.

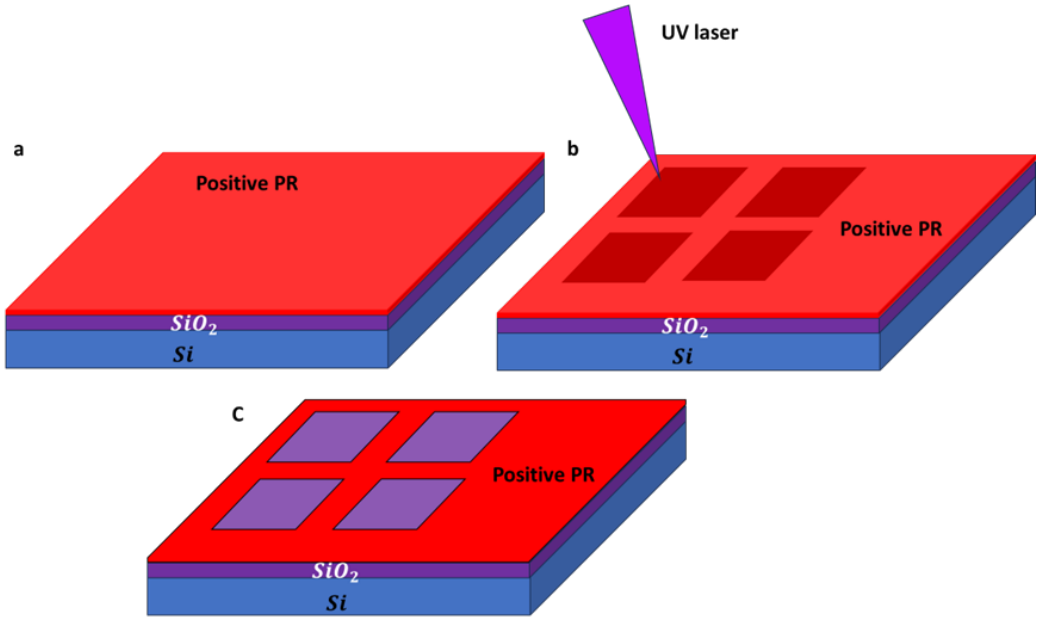

Figure 2.5: schematic of photoresist spinning coating, laser lithography and development. (a) The Si substrate with silica deposited and photoresist S1805 coated. (b) Schematic of laser lithography, darker area are the target area to be exposed by the UV laser. (c) The positive photoresist's solubility increased after laser exposure and developed away by the micro-developer solvent.

2.1.2.4 Dry Etching-Reactive Ion Etching (RIE)

To transfer photoresist patterns faithfully into the deposited silica layers, dry etching is usually applied to etch into the exposed silica. It reacts chemically inside a vacuum chamber and can physically remove material in a selective way. Figure 2.6 (a) is the picture of the Oxford Plasma 80 Plus RIE system used in this project for silica etching. The developed sample was placed on an electrode inside the blue chamber (process pressure: 0.03 Torr). A radio frequency (RF) electric field can be generated inside to interact with the introduced reactive gases, CHF_3 and Ar, produces plasma of ions, radicals, and neutral particles. The gases flowed at 5sccm and 15sccm, respectively. These gases react with the exposed surface materials, silica, and form volatile byproducts. The plasma of ions, radicals and neutral particles sputter the exposed material during the reaction process and enhance the etching rate [190], to around 28 nm/min. The undeveloped photoresist can protect the material underneath, as shown in Figure 2.6 (b).

Another step of oxygen plasma cleaning would be applied after RIE to remove the photoresist and make the sample surface ready for the micro-assembly. The schematic of the oxygen plasma cleaned sample is shown as well in Figure 2.6 (c).

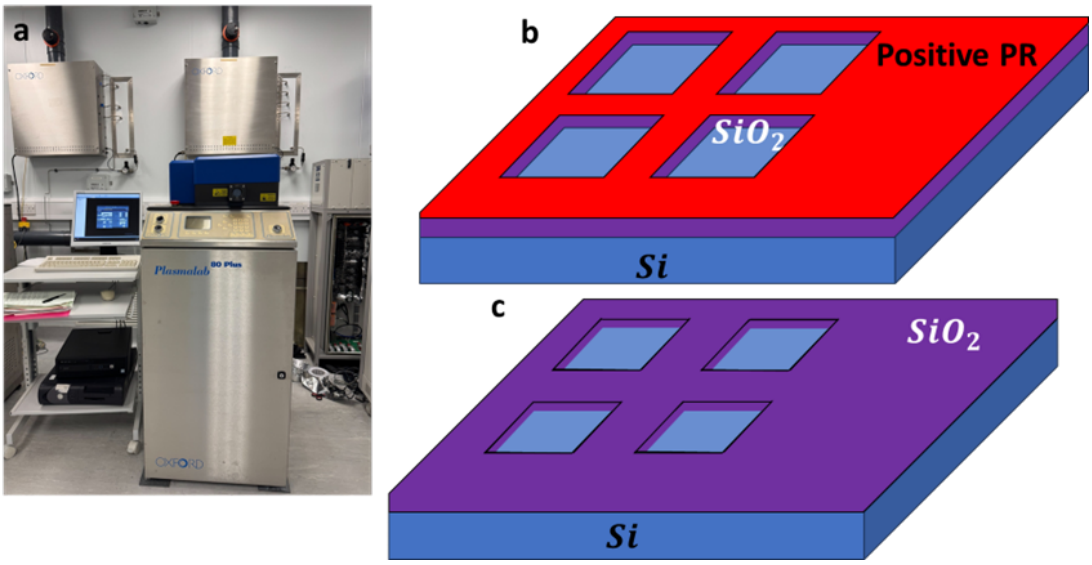

Figure 2.6: (a) Oxford Plasma 80 Plus System used for RIE. (b) Schematic of the sample after reactive ion etching. (c) Schematic of the sample after plasma cleaning to remove the photoresist layer.

2.2 Fabrication Processes of Polymer Waveguides on Glass Substrates

As with the fabrication of the silica frames on silicon substrates, the fabrication of polymer waveguides on glass substrates also started with sample cleaning and the steps are identical. Glass has lower refractive index [195] compared to polymer materials, thus the light emission can be trapped and guided inside the polymer waveguides. The repeated techniques and procedures applied during this fabrication process will only be mentioned briefly below.

2.2.1 Alignment Metal Marker Deposition and Lift-off

The fabrication started with laser lithography of positive photoresist S1818 on the cleaned glass slide sample to transfer the pattern of alignment markers onto the photoresist. Then use electron beam evaporation [71] to cover the sample surface with target metal film. At this point, the metal film would directly deposit on the glass sample surface in the pattern area. In the other area, the metal film deposited onto unexposed photoresist and can be easily removed during the metal lift-off process [196]. The full process is shown as schematic in Figure 2.7, from a to d.

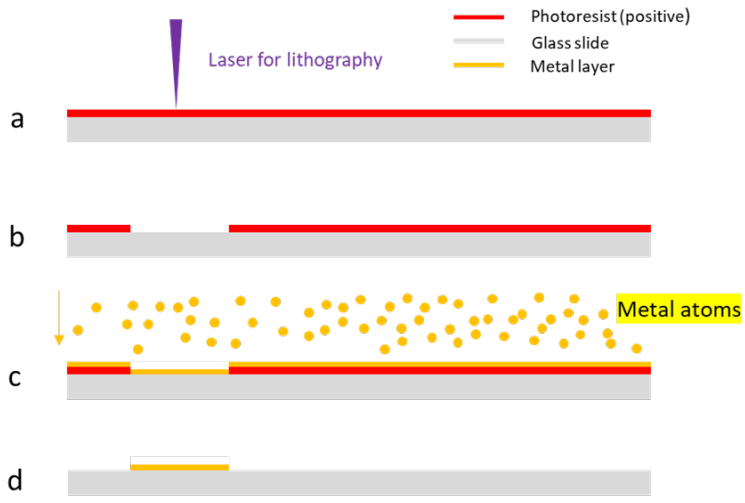

Figure 2.7: Schematic of the process of metal deposition and lift-off

2.2.1.1 Electron Beam (E-beam) Evaporation and Metal Selection

A bilayer of Titanium (Ti) and Gold (Au) was intended to be deposited on the sample. Gold has a bad adhesion with glass substrate and can cause delamination, thus, Ti can work as an additional adhesion layer between glass substrate and gold film layer by forming strong chemical and metallurgical bonding [196].

An electron beam evaporation system (Temescal FC2000) [197] shown as Figure 2.8 (a) was used for the metal deposition procedure. It has a high vacuum system and automated process control which can lead to high-purity thin film deposition in a relatively fast depositing rate.

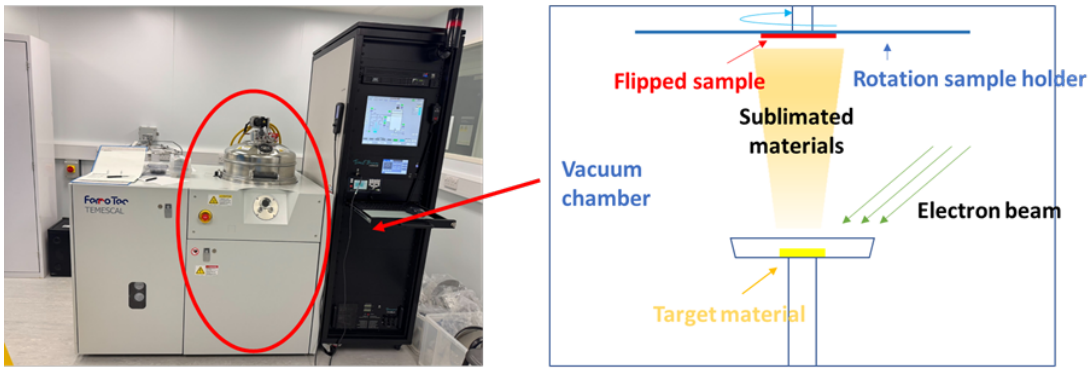

Figure 2.8: (a) Temescal Electron Beam Evaporation system (FC2000). (b) Schematic drawing of the E-beam Evaporation vacuum chamber.

The schematic of the vacuum chamber and the working principle of the E-beam evaporator is shown as Figure 2.8 (b). The sample was flipped and placed on a piece of holding wafer (Si wafer, usually), and the holding wafer was fixed on the rotating sample holder plate to make sure the deposited layer is as even as possible. An electron beam from a high efficiency electron beam gun [197] would bombard the target material (Ti, Pd, Au, etc.) to make it heat up and evaporate into sublimated material gas. These evaporated atoms would travel upwards in a straight line, condense and form a thin film on the samples (glass slides here). In this fabrication process, Ti would be evaporated and deposited first and then Au. The deposition rate inside the chamber was sensed by quartz crystal microbalances (QCM) and controlled by programmable deposition recipes, the deposition rate for both Ti and Au is 10 Å/s. The schematic of the sample

is shown as Figure 2.7 (c), and the metal film layer directly bonded with the glass substrate.

2.2.1.2 MicroStripper Solvent for Metal Lift-off

To remove the metals deposited on unexposed photoresist on the glass substrate, a solvent-based resist stripper 'S1165' made by Kayaku Advanced Materials [198] [199] can be applied, it can dissolve the harden photoresist after metal deposition and the metal film deposited on photoresist area is stripped from the sample while the photoresist is removed. [196]

To conduct the metal lift-off process, the beaker containing S1165 should be placed inside water bath at 80℃. Samples with thin metal film layers should be soaked in S1165 for hours, sometimes overnight. To accelerate this process, ultrasonic agitation is an option. After the metal been lifted off, a standard procedure of wet cleaning (acetone and IPA rinse) and dry oxygen plasma cleaning would be conducted again to remove any possible residues and increase the surface energy and hydrophilicity for transfer-printing of Micro/Nano-emitters (which would be skipped and introduced in section 2.3) and laser lithography of polymer waveguides. The schematic of the sample after metal deposition and lift-off is shown as Figure 2.7 (d).

2.2.2 Polymer Waveguides Fabrication

The polymer material chosen here is Kayaku Advanced Material manufactured SU-8 series [200], SU-8 6005. It is an epoxy-based negative photoresist used widely for high-aspect-ratio and 3D sub-micron lithography [201], and the SU-8 6000 series are enhanced version of the classic SU-8 series. It demonstrates better adhesion and strong chemical resistance compared to classic SU-8 series, also, it is optimised for better development performance.

SU-8 polymer has been developed in micro-electron-mechanical devices fabrication for decades [202] [203] [204] due to its mechanical stability, high aspect ratio, low cost and well-established fabrication process [205], and optical devices have followed more recently [206] [207] [208] [209].

SU-8 polymer's low absorption in both visible and near-infrared (NIR) range exhibits excellent optical transparency from 400 nm to 1500 nm, which makes it have high potential in both visible light communications [210] [211] and telecommunications [212] [213] [214]. Also, SU-8 polymer has a higher refractive index (~ 1.58) [200]than other cladding materials that enable strong optical confinement and guidance in planar photonics structure and this characteristic makes it suitable as single-mode [213] and multimode waveguides [215]. Additionally, but importantly, the optical transmission loss inside SU-8 material (6005 series) waveguides is low [205]. All these features make SU-8 series material suitable for optical devices fabrication, especially working as optical waveguides. Also, this material is compatible with other emitters such as nanowires [57] and it has the potential to increase the scalability of photonic integrated circuits (PIC).

2.2.2.1 SU-8 6005 Spinning Coating, Laser Lithography, Development and Post Treatment

The cleaned glass sample with printed Nanowires would be placed in spinner for SU-8 6005 spinning coating. The spinning process was set at 500 RPM for 5 seconds and 4000 RPM for one minute. A five minutes soft baking on a 95℃ hot plate was applied to enhance resist adhesion, prevent bubbling and reduce thickness variations to improve uniformity. [216]

An extra alignment process was required before the exposure, and it was also conducted in the Heidelberg (Figure 2.4). The metal marker was fabricated by laser lithography and deposition as the design shown in Figure 2.9 (a). The second layer shown as Figure 2.9 (b) was designed to be overlapped with the narrow tail of the metal marker, at where the nanowires were printed. The Heidelberg system can visually scan the whole loaded sample and see the deposited metal markers through the transparent SU-8 6005 layer using a camera system. The Heidelberg can then start the exposure of the waveguides following the overlapped design structure after finding the first metal marker.

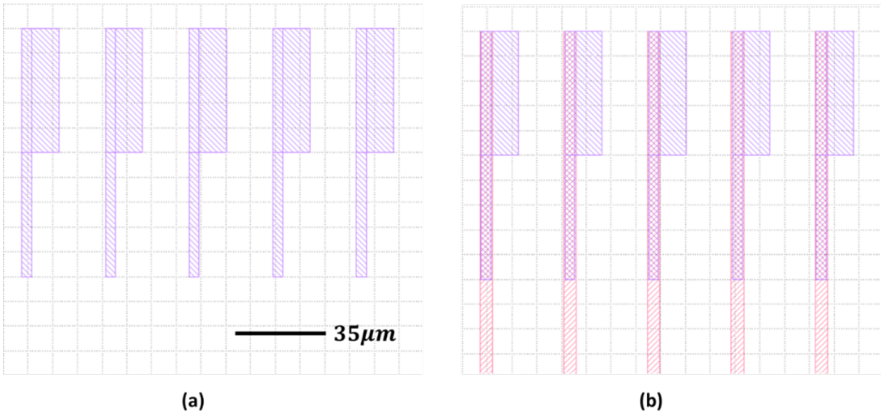

Figure 2.9: (a) Layer 1 of metal marker design. (b) Overlapped design layers of the waveguides structure and metal markers. The scale bar for both diagrams is 35 μm

As introduced previously, the SU-8 6005 polymer is a negative photoresist, thus, the UV laser would expose follow the designed structures and decrease the solubility in developer solvent.

Different from positive photoresist, post exposure baking is required for SU-8 polymer photoresist to create and enhance the cross-link by promoting diffusion of the photoacid and increasing the mobility of the SU-8 monomers. [217] This post exposure baking was also conducted on the hot plate in 95℃ for 2 minutes.

Figure 2.10: Flowchart of SU-8 polymer photoresist development.

To selectively remove the unexposed SU-8 6005 on the sample, Propylene Glycol Methyl Ether Acetate (PGMEA) and Isopropanol (IPA) were applied, and the full development process is shown as the flowchart in Figure 2.10. The sample was then dried with a Nitrogen gun.

To make the exposed SU-8 6005 waveguides become chemically and thermally stable and enhance the mechanical strength [218] for next step treatment, hard bake (final bake after development) was applied. To cure the SU-8 polymer waveguides, the glass sample was placed on a 160℃ hot plate for at least 40 minutes.

2.2.2.2 Sample Cleaving and Characterisation

To enable light coupling to on-chip waveguides, a cleaved facet can provide an interface where light can output (for this specific project) or input. Waveguides facets can be easily created by cleaving the sample from the backside and breaking the waveguide, as SU-8 polymer waveguides were fabricated on a glass sample.

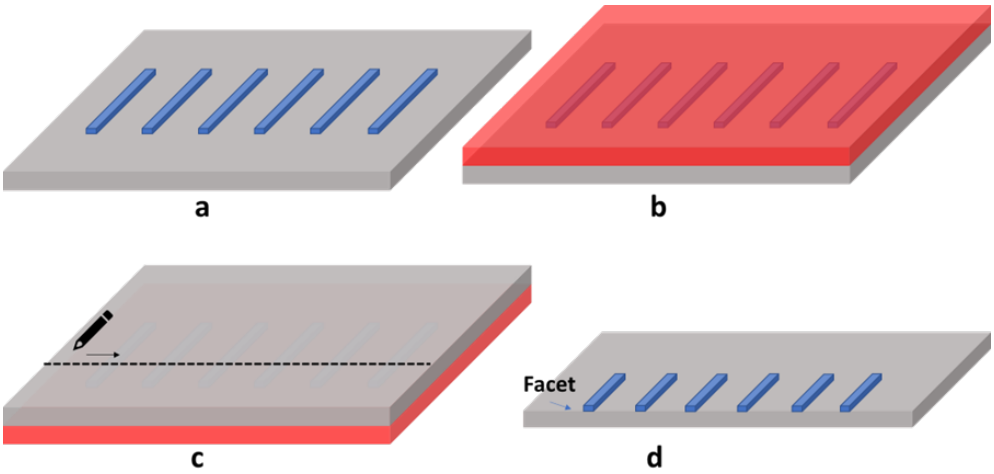

Figure 2.11: schematic of the cleaving process. (a) Harden baked SU-8 polymer waveguides on a piece of glass substrate. (b) SPR 220-7.0 covered sample. (c) Flipped sample with the scribe diamond. (d) Cleaved sample with waveguides facets created for optical output.

As the cleaving step would be done by a diamond scribe on the backside (the side without SU-8 waveguides) of the glass substrate, an additional protection layer was necessary to avoid any damage to the waveguides. The thickness of SU-8 6005 after 4000 RPM spinning should be $\sim 4\,\mu$m. [200] To protect the waveguides during the cleaving process, the MEGAPOSIT SPR 220-7.0 photoresist [219] can be spin-coated at 1000 RPM to cover the whole sample. The thickness of SPR 220-7.0 was $\sim 7\,\mu$m after spinning (1000 RPM) and 90 seconds soft bake (115℃). [219] It can cover the hardened waveguides and protect them from scratching as shown in Figure 2.11 (b). Then a diamond scribe pen was applied to scratch the glass and cleave the sample. The protection layer can be easily removed and cleaned by the wet cleaning process introduced previously (Acetone, Methanol, IPA and D.I. water rinse). The full process of cleaving is shown as the schematic in Figure 2.11.

2.2.2.3 Waveguides Characterisation

To analyse the fabricated SU-8 6005 polymer waveguides' characterization such as 3D topography, thickness and so on and protect the SU-8 waveguides themselves from damage caused by scratching, a non-contact surface measurement tool should be applied.

Figure 2.12: Wyko NT1100 optical profile scanning system.

In this project, the optical profile scanning system applied was Wyko NT1100 system [220] manufactured by Veeco Instruments. This system can precisely do the material characterisation job via white light interferometry (WLI). [221] It is capable of measuring from 0.1 nm to 1 mm in vertical measurement range and this makes it suitable for SU-8 polymer waveguides height analysis, especially in single mode or multimode waveguide fabrication. The optical profile scanning system applied in this step is shown as Figure 2.12.

2.3 Micro-assembly of photonic devices (PhCCs Membranes and Nanoemitters) and Different Substrates in Photonic Integrated Circuits

To advance PICs from device level to large-scale circuits on a chip, different elements and functions such as fiber coupling, electronic ASIC control and copackaging, free-space coupling optics, thermal stabilization modules [222] [223] [224] [55] [225] can ideally be integrated at a carrier level. These elements are all in a variety of geometries and cannot be delivered by single material platforms alone, therefore, hybrid and heterogeneous integration are widely researched and applied in the PICs area. [36]

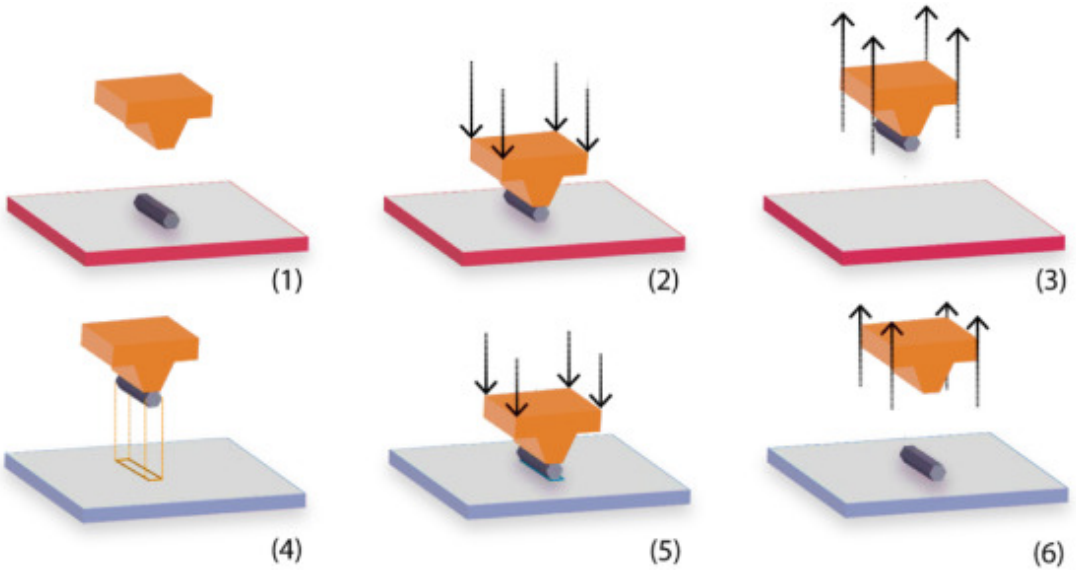

Figure 2.13: Schematic of a NW transfer printing process. (1) Aligning stamps with the target device (NW) on the donor substrate. (2) Contacting stamp with the NW. (3) The NW is released from the donor substrate with a fast peeling speed. (d) Aligning the NW device to its receiver substrate position. (e) Contact the NW with the receiver substrate. (f) The NW is released from the stamp and printed on the receiver. [226]

In this project, to assemble photonic devices by moving them from their own growth substrates to a secondary substrate (usually, they are different materials compared to the original substrate), an accurate technique, micro-transfer-printing, is applied. [227] A stamp made of an elastomer called polydimethylsiloxane (PDMS) is used to pick

up photonic devices from the growth substrate (donor substrate) and release devices slowly on a non-native substrate (silica on silicon, glass slides and polymer waveguides with PDMS adhesion layers in this project).

2.3.1 Micro-transfer-printing Concepts

As shown in Figure 2.13 (1), a soft PDMS stamp is applied to pick up the device from the original fabrication substrate, this 'adhesion force' between the device and the soft PDMS stamp is dominated by van der Waals' interactions, and the adhesion can be kinetically controlled. [227] For the pick-up process, Figure 2.13 (2)-(3), the adhesion between stamp and objects should be stronger than the adhesion between the objects and the donor substrate to break the contact, which requires a very fast retrieval (or picking) velocity in vertical direction. Quite the opposite, the printing process shown as Figure 2.13 (4)-(6) requires stronger adhesion between the objects and the receiver substrate. This printing process will need a very fast contact (to create a strong adhesion) and a very slow releasing velocity. Related research on the relationships between the peeling velocity and the adhesion created by an elastomeric stamp has been well studied and can be found in references [227] and [228]. Figure 2.13 is a schematic of a full transfer-printing process of a semiconductor nanowire, which was previously done by the research group. [226]

2.3.2 Accurate Transfer-printing with NanoInk NLP 2000 System

2.3.2.1 PDMS Stamp Fabrication

The stamp used in this project were pre-fabricated and had been used widely for nanowires printing [226], the contacting area parameters are $30\,\mu\text{m} \times 10\,\mu\text{m}$ (length $\times$ width), which is also very suitable for the PhCCsC membranes ($11\,\mu\text{m} \times 9\,\mu\text{m}$). The microscope image and the side view schematic of the PDMS stamp is shown as Figure 2.14, and the highlighted circle area is the actual contacting area.

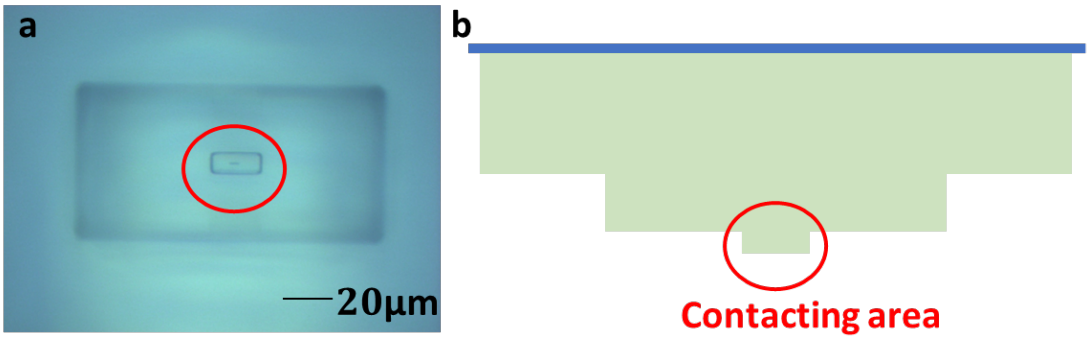

Figure 2.14: (a) Top-view microscope image and (b) Side-view schematic of the pre-fabricated PDMS stamp used for both PhCCs membranes and NWs transfer-printing.

The fabrication process of PDMS stamp can be divided into two parts: the fabrication of the mould and PDMS mixture. The sample mould was fabricated on a silicon wafer and the process is shown in Figure 2.15. The contacting area of the PDMS stamp was formed by deposition and pattern (PECVD, laser lithography and RIE etching applied) of a thin layer of silica and RIE etching applied to the whole wafer (etching rates are different for silica and silicon and this made the trench thickness for the formation of the contacting area to be 6 μm), shown as Figure 2.15 (b) and (c), respectively. Another very thin layer of silica was deposited to cover the wafer and trench surface through the PECVD technique (Figure 2.15 d) to prevent the PDMS sticking in the trench, as polydimethylsiloxane ($CH_3-[Si(CH_3)_2-O]_n-Si(CH_3)_3$) is a kind of silicon-based material. [229] To form the PDMS to the designed form, a layer of SU-8 was spin coated, laser lithography, developed and hard baked to build the mould for the PDMS stamp as shown in Figure 2.15 (e).

The PDMS was mixed at a 10:1 (weight/ weight) ratio of base to curing agent. [230] [231] The mixture was then placed in a beaker for ~40–60 mins for degassing, the bubbles created during the mixture stage would rise and pop during this step. The mixed and degassed PDMS would then be poured into a beaker with the pre-fabricated mould placed and left on a flat stage for $\sim$ 24 hours for curing as shown in Figure 2.15 (f). It can be easily peeled off from the mould and cut into the desired mounting shape to be fixed on stamp holder by wax once cured.

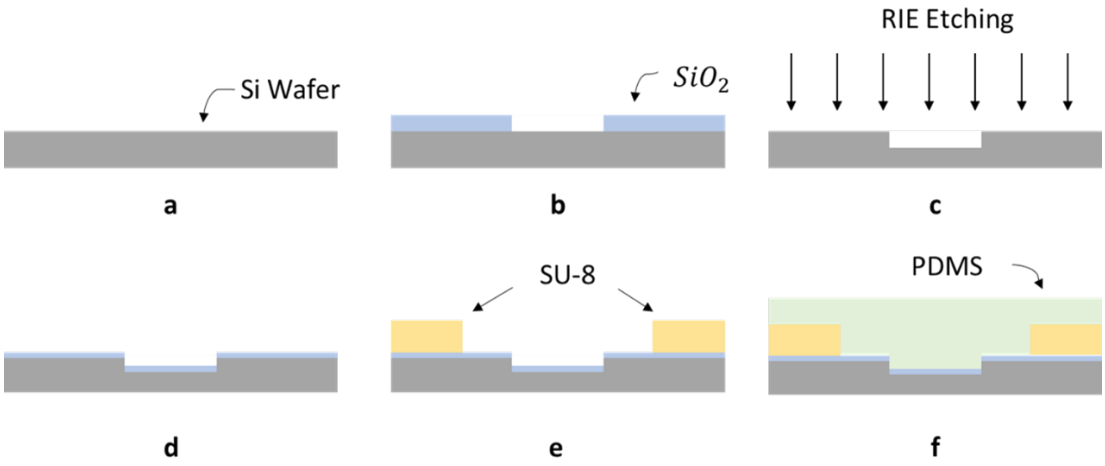

Figure 2.15: Generalised schematic of PDMS stamp fabrication (a) Si Wafer. (b) Patterned Silica on Si wafer. (c) RIE to form the trench on wafer to create the contacting area. (d) Silica deposition. (e) SU-8 patterning. (f) Cured PDMS in the mould. [104]

2.3.2.2 NanoInk NLP 2000 System for Accurate Transfer-printing

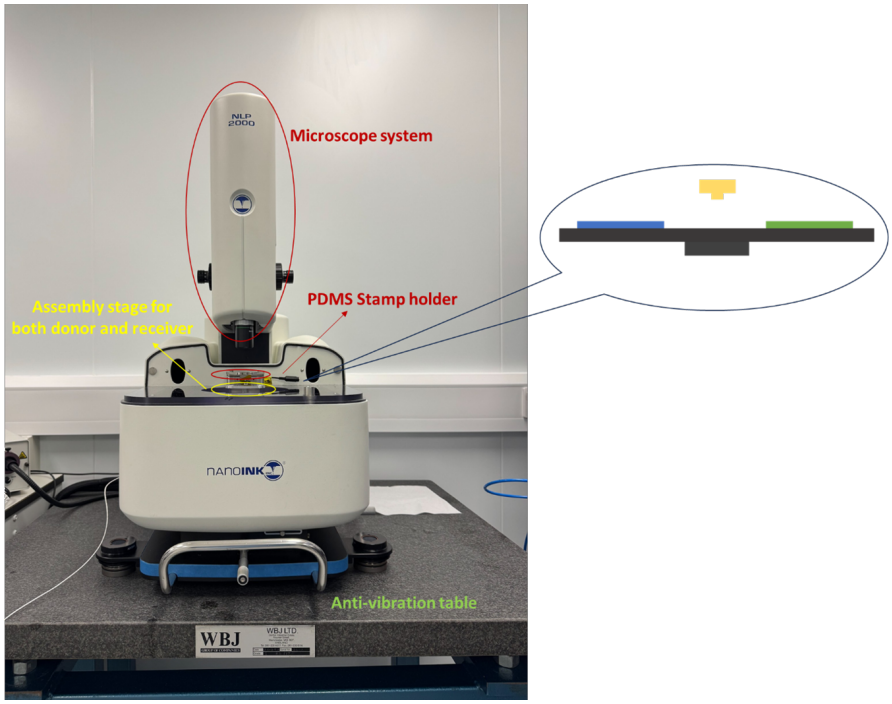

Figure 2.16: Photograph of the NanoInk NLP 2000 system for accurate micro-transfer-printing.

Figure 2.16 demonstrates the photograph of the NanoInk NLP 2000 system used to transfer print photonic devices to target substrates. It is a commercially available nano-fabrication system employing a 5-axis that provides sub-micron accuracy and precision. [232] This system was designed for nanolithography by applying a dip-pen initially, the 'pen' tip was replaced by a PDMS stamp holder for micro-assembly.

During the transfer-printing process, both donor and receiver substrates are fixed on the stage area, and the 5-axis system consisting of 3D piezo-driven linear control and T_x, T_y encoded goniometer control would move the assembly stage (shown as highlighted in Figure 2.16) accurately ($\pm 25\,\text{nm}$ and $\pm 0.000\,25^\circ$) to conduct the picking up and releasing process.

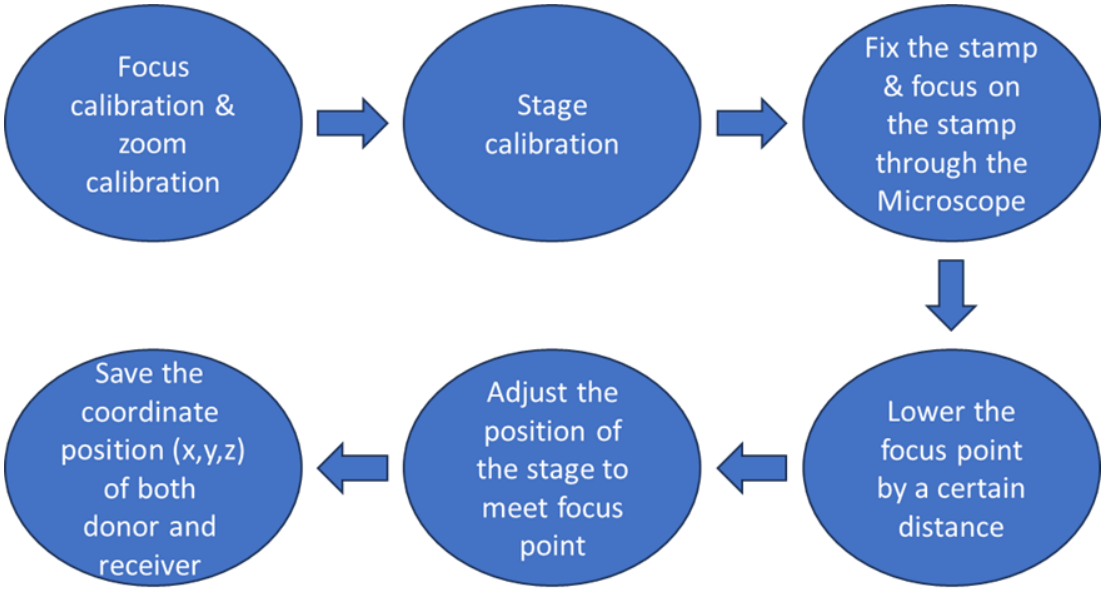

Figure 2.17: Process diagram of the preparation procedure before transfer-printing.

There are several stages preparation of work needed before the start of the transfer-printing process. The first one is the calibration, it contains three parts, microscope focus calibration, zoom calibration and the stage calibration. These calibration functions are all embedded in the controlling software and can be easily accessed. The second step is fixing the PDMS stamp on the stamp holder and change the focus point of the integrated microscope to see the clear image of the contacting area from the camera (a clear PDMS diagram is shown as Figure 2.14) and record it. To avoid the

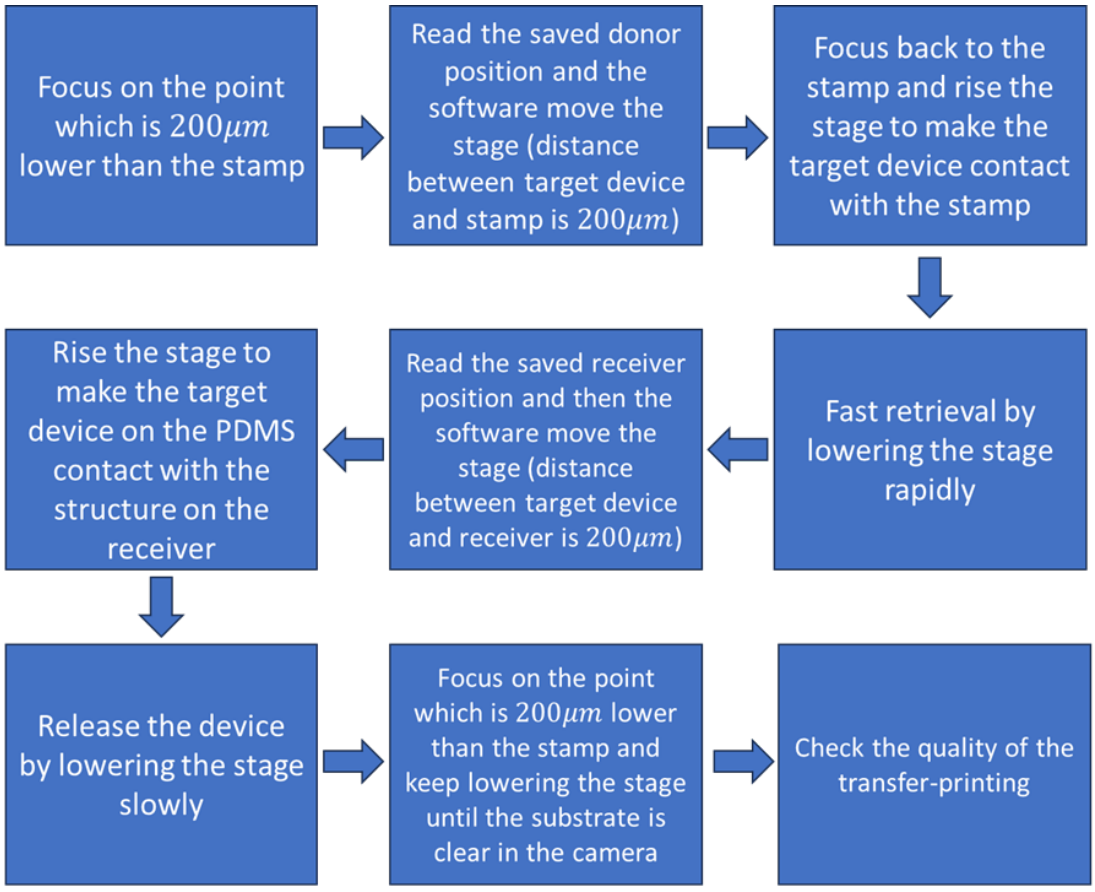

Figure 2.18: Process diagram of the operation process of a single pick-up and releasing process with the NLP 2000 system.

substrate crushing onto the PDMS, it is necessary to lower the pre-recorded focus position, and this can leave a reasonable distance between the stamp and the substrates. For this specific project, a distance of 200 μm is applied, which means the distance between the stamp and the substrate (either donor or receiver) is always 200 μm while the substrate is on focus at this point. This step should be repeated twice to capture and save the positions and rotation angles of both donor and receiver substrates. The software can read and go to the saved position automatically. Finally, the focus point is moved back to the previously saved position of the stamp and the transfer-printing is ready to go by changing the stage position to the recorded donor position. At this point, the distance between the stamp and the donor substrate is 200 μm and the operator can change the distance manually to make a contact and start a pick-up. Figure 2.17

and Figure 2.18 are the process diagrams of the preparation work and the operation process of the NLP 2000 system.

2.3.2.3 Transfer-printing of the Si PhCCs membrane on Supporting Frames

The pre-designed and fabricated Silicon Photonic Cavities (Si PhCCs) membrane with $7 \times 9\,\mu\text{m}^2$ active area [131] was suspended over a silicon substrate at a gap distance of $2\,\mu$m and connected with the original fabrication substrate (the donor) by an anchor, the diagrams of one suspended PhCCs membrane on its original substrate captured by Scanning Electron Microscope (SEM) is shown as Figure 2.19 (a).

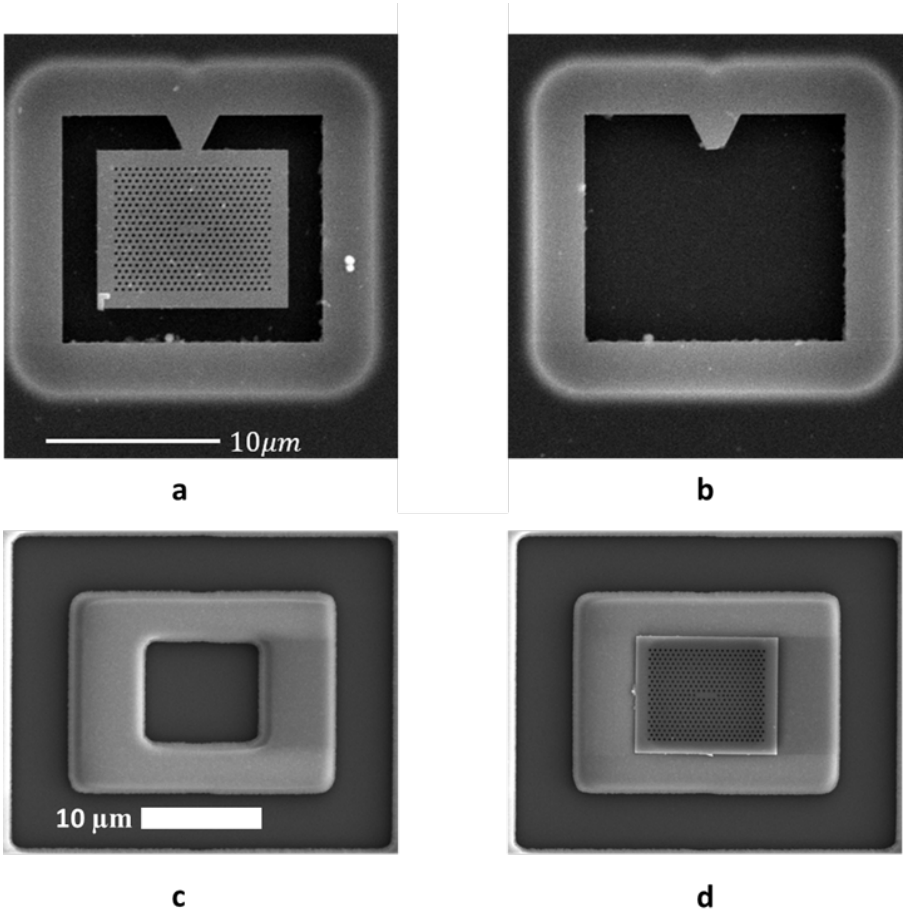

Figure 2.19: SEM captured diagram of (a) Si PhCCs membrane on its original Si substrate. (b) The left void after membrane being picked up. (c) Silica frames on Si substrate. (d) Printed membrane on the frame.

The original Si substrate and the Si substrate with prefabricated silica frames are donor and receiver, respectively. They would be fixed on the assembly stage, and the position of the target device on donor and the target frame on receiver were both checked and saved. During the pick-up step, the stage was raised and the PDMS contacting area would contact the membrane. This contact and the coming fast retrieval (by lowering the stage) could break the anchor and pick the Si PhCCs membrane up, the left anchor is demonstrated as Figure 2.19 (b).

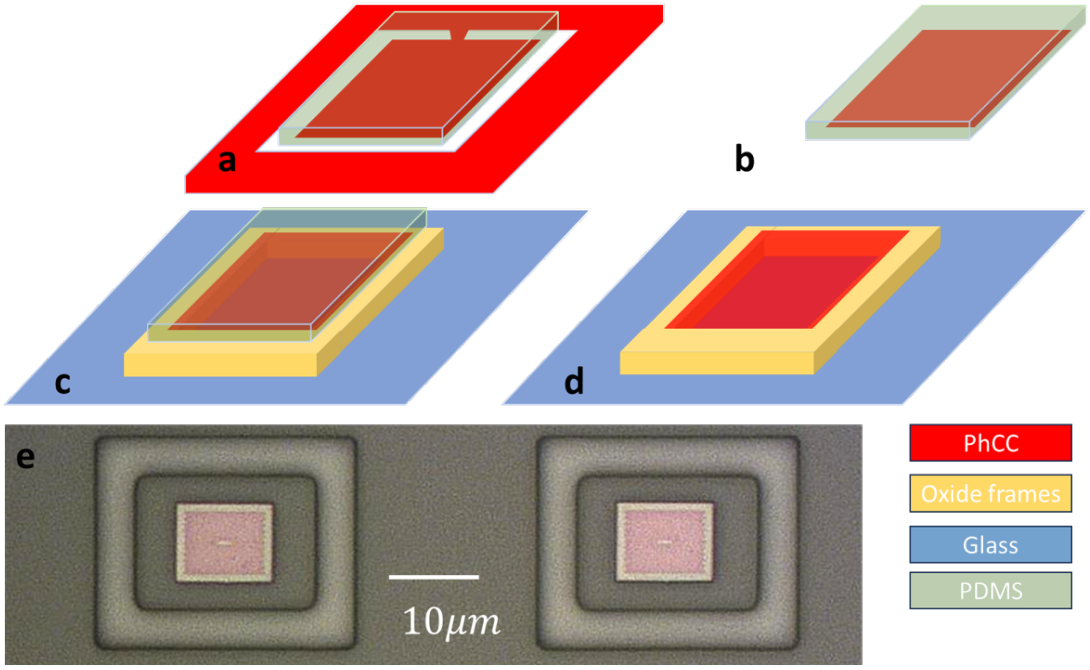

Figure 2.20: Schematic of the transfer-printing process and microscope captured diagram of (a) PDMS contacting with membrane on donor. (b) A PhCCs membrane picked up by the PDMS stamp. (c) Alignment and printing of the membrane. (d) The receiver after releasing. (e) Array of PhCCs-Air-Reflector structures.

In the printing process, the receiver substrate would move to the position which is 200 μm lower than the PDMS stamp first. The alignment and contact could happen by raising the stage, then a very slow releasing process would be applied by lowering the stage at a step of 1 μm. The SEM diagrams of a silica frame and the frame with PhCCs membrane printed are present as Figure 2.19 (c) and (d). The schematic of the transfer-printing process is shown as Figure 2.20 (a) to (d), also diagram (e) shows the microscope image of two printed membranes on silica frame arrays.

2.3.2.4 Transfer-printing of the InP Nanowires on A Glass Substrate

The wurtzite indium phosphide (InP) Nanowires were fabricated by selective-area Epitaxy growth technology on a InP (111) substrate with 30 nm thick silica, the fabrication process of these InP nanowire can be found in reference [52]. The transfer-printing of nanowire was applied after the metal deposition and lift-off step introduced in section 2.2.1, and the printed nanowire should be aligned with the centre point of the tail of the metal marker and would be fully overlapped by the polymer waveguide after the fabrication process introduced in section 2.2.2.

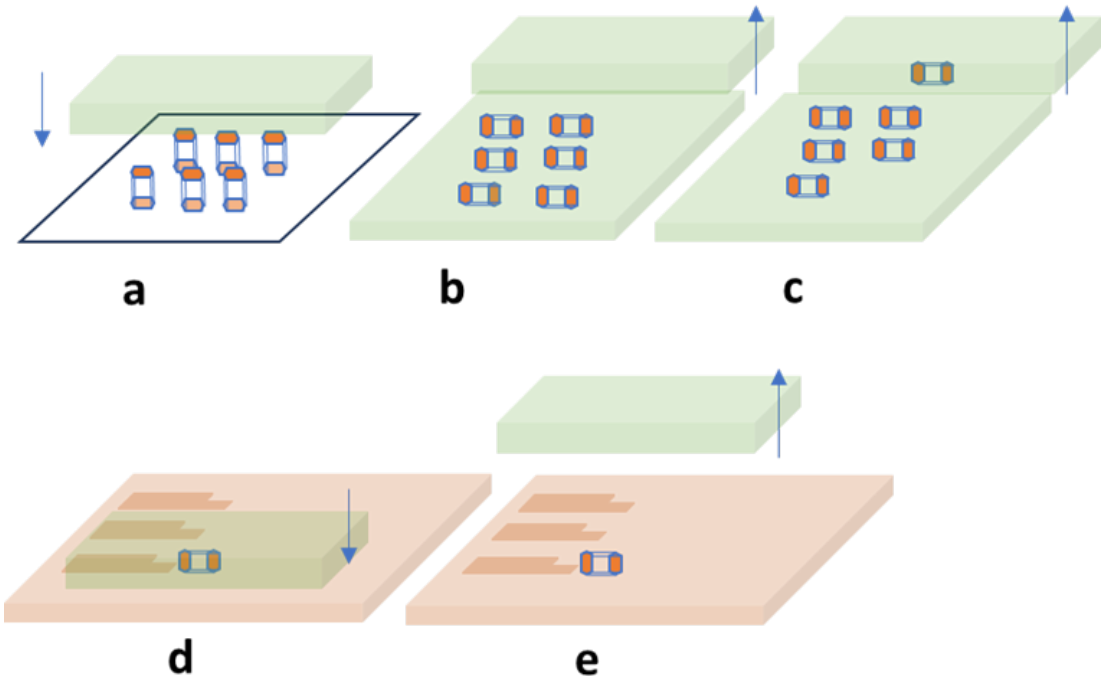

Figure 2.21: Schematic of the transfer-printing process of (a) The contacting process of the PDMS stamp and the InP NWs on their growth substrate. (b) Printed NWs (horizontally) on a flat PDMS stamp. (c) Picking-up process of a single NW from the flat PDMS stamp. (d) Alignment and Printing process of a single NW on the glass substrate. (e) The printed NW and the releasing PDMS stamp.

The nanowires were grown on the original InP (111) substrate vertically and the emission was from two facets, so it need to be printed in a horizontal way. Therefore, an additional transfer-printing was necessary. In the first transfer-printing, the PDMS stamp contacted with a massive number of NWs slightly to pick them up (shown as

Figure 2.21 (a)), and another flat PDMS stamp (without any structure) was used here as a receiver. Then the PDMS stamp with picked NWs made a slight contact with the receiver PDMS stamp and the stage was moved at a step of 1µm to print NWs on the receiver flat PDMS stamp. After this step, the massively printed NWs can be characterised (optional) by a low power HeNe (632.8 nm) laser and re-grouped by the same picking up and printing process. [60]

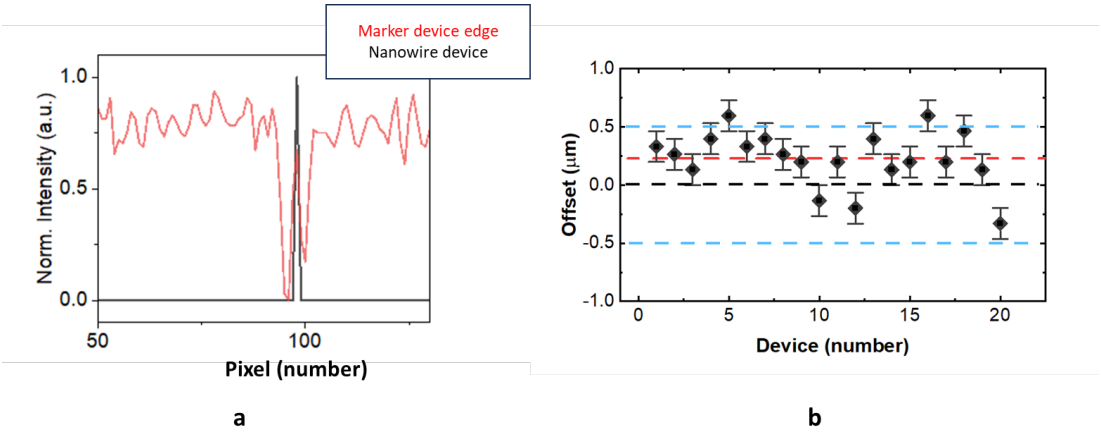

Figure 2.22: (a) A sample diagram of the colour intensity analysis of both metal marker and the nanowire, the comparison of two position is shown and the X-axis is the pixel order. (b) A lateral offset scatter plot of the 20 nanowire-in-waveguide devices.

The secondary transfer-printing was then applied to pick the NW from the flat PDMS and align with the metal marker on the receiver. During this alignment step, a MATLAB script was written to analyse the colour intensity of the edges of the metal marker's tail and generate a 'calculated position' when the marker was clear in the microscope (no contact). The stage was moved to make the picked NW at the roughly centre point and run the script again to see the 'NW position'. The comparison between the 'calculated position' and the 'NW position' can optimise the alignment. A sample diagram of the comparison is shown as Figure 2.22 (a). The stage would be kept moving and adjusting once the two positions difference in a reasonable range or beyond the minimum step of moving. After that, the stage could be raised to make the contact and then slowly release the stamp and print the NW on the glass substrate, this process is shown as Figure 2.21 (c) to (e). In total, 20 NWs were printed.

Additionally, this MATLAB script can also be used after the fabrication of the SU-8 waveguide to analyse the quality of the overlapping of the NW and a single waveguide, the results is shown in Figure 2.22 (b), and the average offset is 228 nm.

2.3.3 Advanced Transfer-printing System Introduction

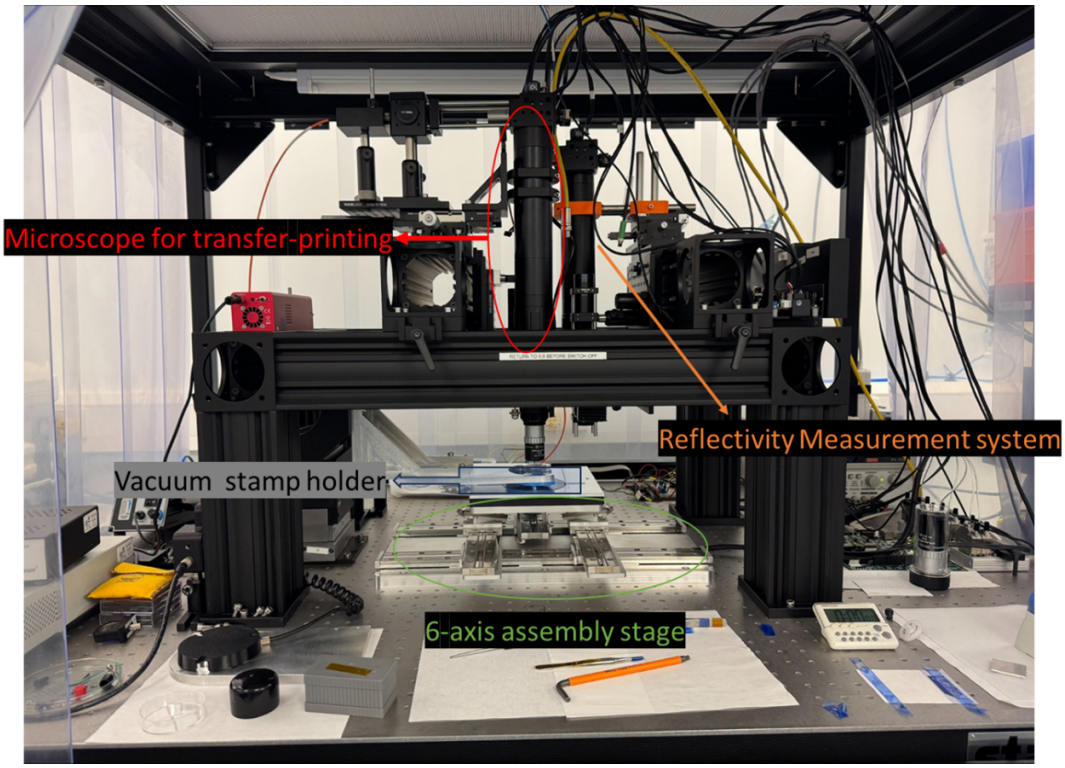

Figure 2.23: The Image of the advanced transfer-printing system with in-situ measurement.

In this project, an advanced transfer-printing system [233] shown as Figure 2.23 was developed to provide better transfer-printing accuracy and in-situ reflectivity spectrum measurement capability to assemble the PhCCs membranes and the frames and measure the performance while the micro-transfer-printing process conducting, detail of this measurement can be found in reference [234] and **Chapter 3**.

In the transfer-printing process, the silica frames sample would be placed on the 6-axis stage together with the PhCCs membranes donor sample. The stamp was fixed on the stamp holder by vacuum (different from NLP system which is fixed by a screw).

The transfer-printing procedure is similar to the procedure with the NLP system but with higher accuracy. The schematic of the advanced transfer-printing instrument and the optical injection column is shown as Figure 2.24. The system can not only monitor the transfer-printing process of a PhCCs membrane but also can optically inject a tuneable laser on it and measure the reflectivity at the same time.

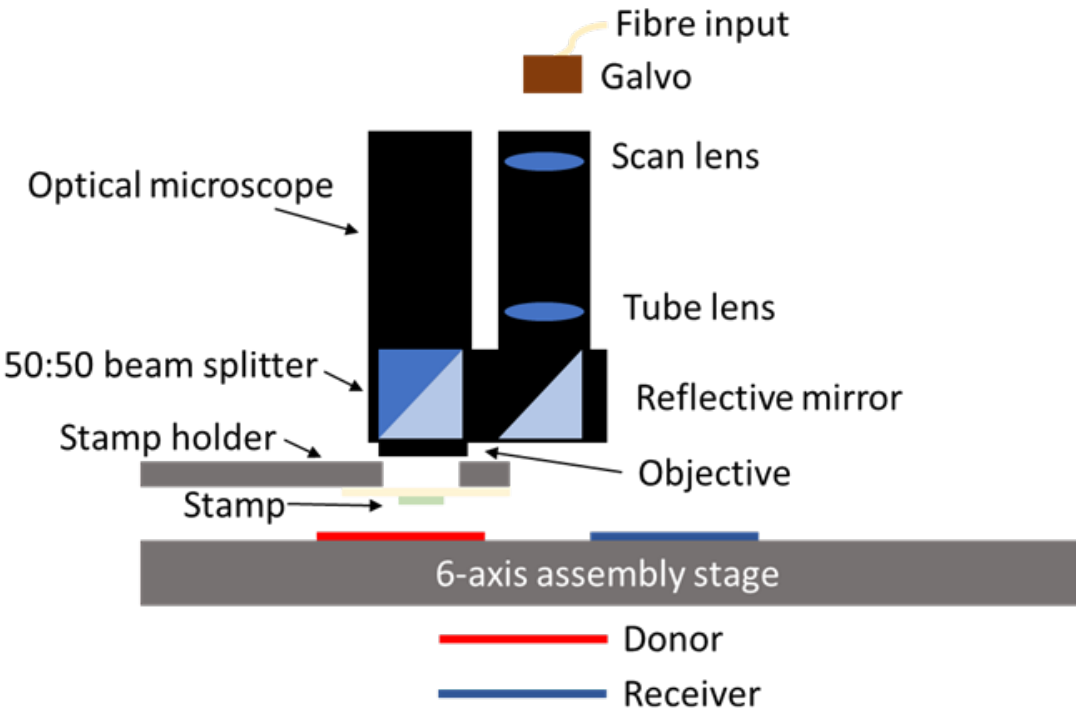

Figure 2.24: Schematic of both the advanced transfer-printing system and the optical injection and measurement system embedded.

2.3.3.1 Micro-assembly of the Waveguide Sample and LED Pixels

After the transfer-printing of InP NWs on the glass substrate, the polymer waveguides array was fabricated and the sample was cleaved as introduced in section 2.2.2. An attractive way to package the pumping source with the PIC chip and increase the scalability is applying transfer-printing technology to directly integrated small LED pixels onto the PIC chip.

The gallium nitride (GaN) LED (emission wavelength: $\sim$ 450 nm) applied here were specifically designed and fabricated for transfer-printing purpose. They are 100 $\times$

$100\,\mu m^2$ and were wet etched, so they were suspended on the original substrate and connected by anchors as shown is Figure 2.25 (a). The PDMS stamp applied here is a square stamp with 5 pyramid tips as the sketch shown in Figure 2.25 (b), this design can pick up the pixel and minimise the contacting area to prevent any possible damage to the LED pixel.

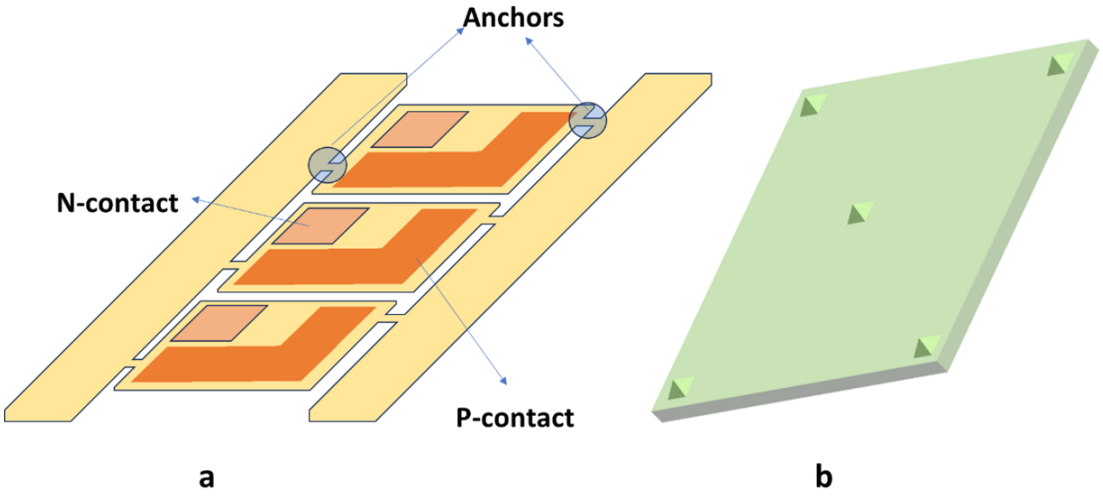

Figure 2.25: Schematic of (a) An array of GaN LED pixels on the fabrication substrate. (b) The PDMS stamp with 5 pyramid tips.

In the transfer-printing process, keeping the receiver substrate surface flat and smooth can maximise the surface energy and make the release process easier. However, for the glass substrate with waveguides fabricated, the surface is rough, the heterogenous integration of hard baked SU-8 waveguides and GaN LED pixel is extremely difficult. Therefore, an adhesion layer was required. As the 10:1 PDMS layer is transparent to 450 nm light, it would not affect the optical performance of the GaN LED. To make the releasing process easier, a layer of 10:1 PDMS was spin-coated on the surface of the glass of substrate with SU-8 waveguides at 5000 RPM. The sample was then placed onto a 80℃ hotplate for one hour to let the PDMS layer curing. During the transfer-printing, both donor and glass substrate were placed on the 6-axis assembly stage, the PDMS stamp with pyramid tips contacted with the pixel and broke the anchors to pick one pixel up. The P-contact would align with the embedded NW area

as the P-contact area is the emitting area.

2.4 Summary

This chapter presented the techniques, equipment and systems applied to fabricated photonic integrated circuits components in different structures, including suspended frames and waveguides. The micro-assembly technique, micro-transfer-printing with different system, either commercial or customised are demonstrated. The fabrication process of elastomeric stamp used for printing is also briefly mentioned. Additionally, some equipment and methods used to characterise the quality of PIC devices are introduced.

Chapter 3

Transfer-printing and Measurement of Silicon Photonic Crystal Cavities (PhCCs) Arrays onto Non-native Substrate

This chapter discusses the development of a micro-transfer-printing (μTP) technique for high resonant quality factors (Q-factor) silicon photonic crystal cavity arrays onto various substrates, including photoresist and silica in a suspended geometry. For this purpose, the fabrication process of the polydimethylsiloxane (PDMS) stamp used to pick up and print objects is described. The chapter also outlines the design and fabrication of microstructures in two different materials: photoresist S1805 and silica, the latter deposited via plasma-enhanced chemical vapour deposition (PECVD). The comparison and analysis of the resonant wavelength of customised silicon photonic crystal cavities (PhCCs) arrays before and after micro-transfer printing (μTP) is presented. This research offers insights into the functionality of μTP in photonic integrated circuits, serving as a foundation for further studies on the transfer printing of PhCCs arrays and in-situ spectral measurement conducted by my colleague Dr. Sean P. Bommer at the Institute of Photonics.

3.1 Introduction

Spatial light modulators (SLMs) are electrically addressed [235] devices that can effectively generate and manipulate structured light, but they are limited by factors such as frame refresh rate, low diffraction efficiency, and pixel density [236] [237]. Photonic Integrated Circuits (PICs) SLMs (optically addressed) [131], using silicon photonics, attract significant research and commercial interests due to their scalability and potential to overcome the mechanical speed limitations of micro-mirror based SLMs [237]. However, PICs based SLMs are still not competitive on the market due to the switching energies caused by combination of waveguides, high-power thermo-optics shifters and vertical grating couplers. [238] [239] Instead of these complex structures, a new design of photonic structure would be an important candidate to improve the development of SLMs.

Researchers from the Englund Group of the Massachusetts Institute of Technology (MIT), USA, designed, modelled and then fabricated inverse designed two-dimensional silicon (Si) photonic crystal micro-cavities arrays [131] with very high Q-factor and small mode-volume. Therefore, the high ratio between Q-factor and mode-volume (Q/V) related to the ultra-high spatial confinement in the silicon layer, can exceed 10^6 [240]. These high Q/V micro-cavity arrays allow for significant enhancement of local light-matter interaction which would be necessary in sensing [241] [242], non-linear optics [243] [244], ultra-compact lasers [245] [246] and coupling with signal photon emitters [247] [248] [249]. Working with incoherent light emitting from complementary-metal-oxide-semiconductor (CMOS) [175] driven micro-LED arrays (wavelength less than 500 nm) [182], strong injection of free-carriers inside micro-cavities can induce a plasma dispersion effect which effectively changes the reflective index, and hence the reflectivity of the device. Then incident coherent light's (IR usually) phase or amplitude can be modulated.

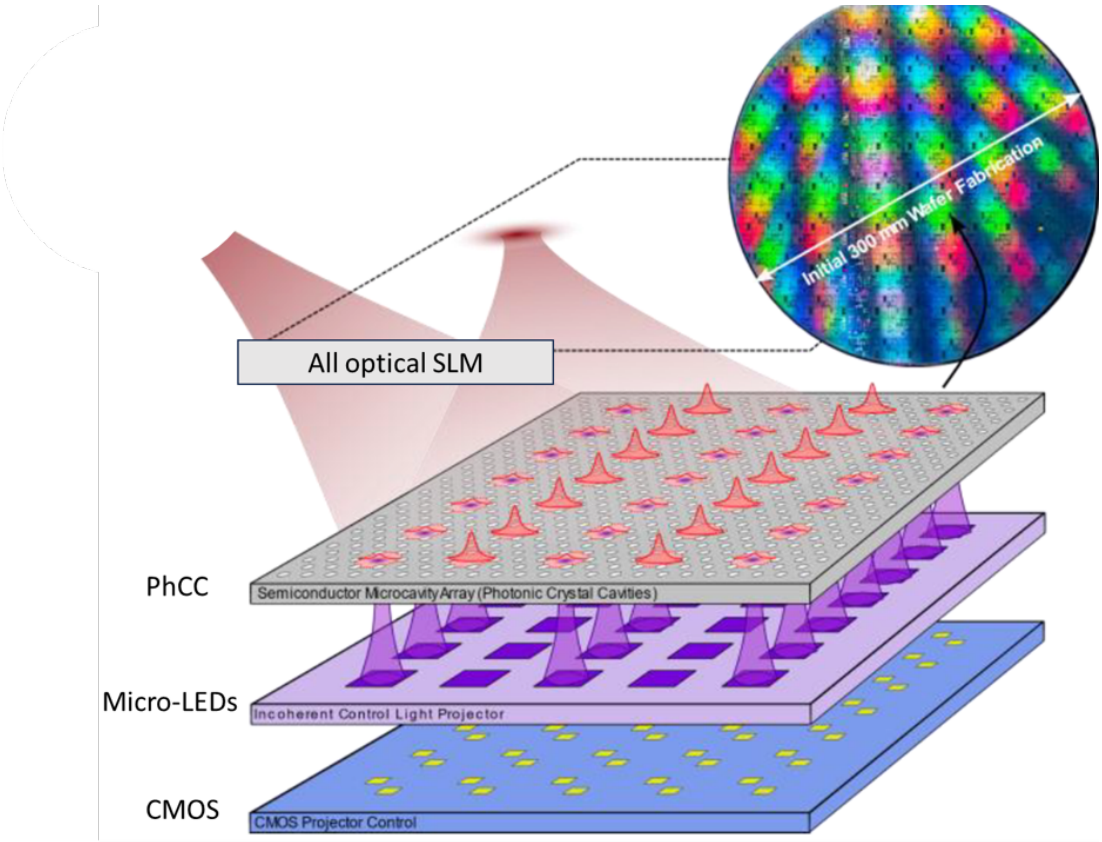

Figure 3.1: Schematic of operation of the new Silicon PhCCs-SLM (reflection mode) [131].

The reflection mode operation of this design is demonstrated in Figure 3.1 provided by MIT [131]. The whole set-up can be divided into three main layers, the first layer is an array of high Q/V silicon PhCC membranes. These cavities spatially localise the incident beam, thereby enhancing local light–matter interaction. In the absence of LED pumping, losses in the silicon layer are negligible. The cavities can be designed to remain off-resonance with the incident beam, enabling direct specular reflection. The second layer (purple in Figure 3.1) is the micro-LED array pumping layer, the emission wavelength is in the range of 405 nm to 450 nm, which can be strongly absorbed by silicon, this can optically create free carriers inside the silicon PhCCs layer region and induce plasma dispersion effects. The induced plasma dispersion effects caused by visible pumping spectrum and the enhanced light matter interaction effectively modulate the reflectivity of the device. The bottom layer is the CMOS layer bonded

to LED pixels to provide both high speed switching (which leads high modulation bandwidth) and greyscale brightness control functionality for shifted wavelength tuning.

As described in Chapter 1, the in-plane mode confinement of silicon PhCCs is realised through the combination of photonic bandgap and induced points defects. [250] Figure 3.2 is the SEM image of a single PhCC membrane, the photonic bandgap is realised through the periodic Silicon-and-air-holes. These air holes were fabricated through deep UV lithography [125] [251] [126] and etching [127] [252] on the order of 150 nm in diameter for resonant wavelength in the telecommunications spectral band on a suspended membrane of 220 nm in thickness, ensuring a single optical mode in the vertical dimension. [234] [131]

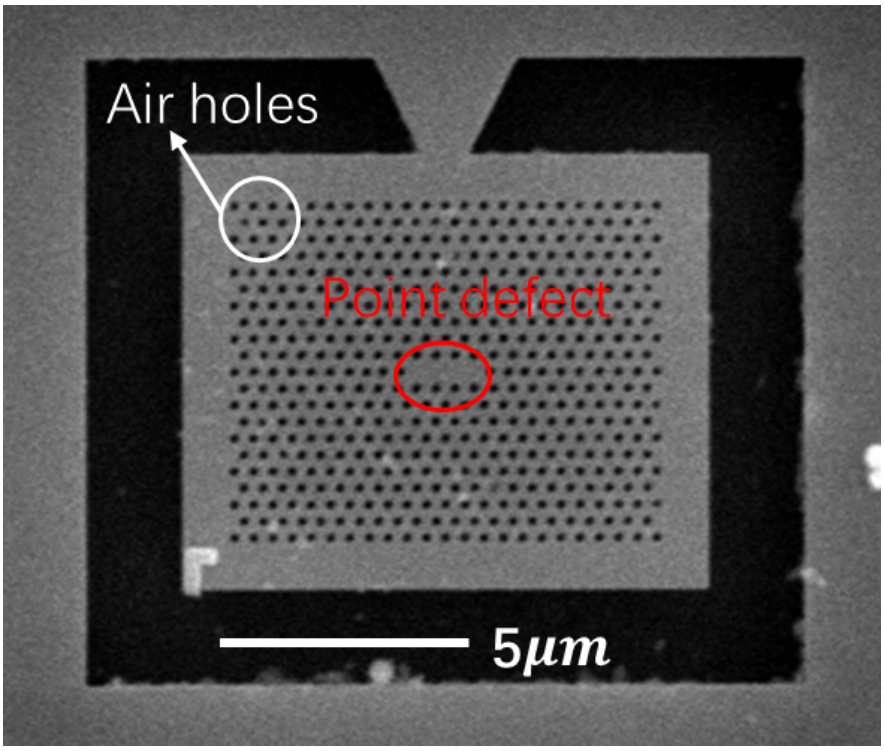

Figure 3.2: SEM image of a Silicon PhCC membrane.

Though these PhCC arrays were fabricated by applying deep UV lithography, the ultra-small fabrication variances during both lithography and etching stages can result in nano-metric variance in the PhCC pattern, preventing the fabrication of identical devices. Therefore, the resonant wavelength of cavities may vary in the few nanome-

tres range, within the 1550 nm spectral region [128] [117]. Post-fabrication tuning of individual PhCC device by selective excitation [131] or active control is challenging.

To overcome fabrication differences within individual PhCC device, a physical transfer method was applied. [253] Different to individual tuning cavities in a fixed spatial arrangement, these fabricated PhCC array membranes can be characterised, selected and re-arranged on a new substrate using this mechanical transfer-printing method. Moreover, with the advanced micro-transfer-printing instrument [233] shown as Figure 3.3, the process of optically characterising the devices could be carried out at the same time within the exact same system. Additionally, detailed diagrams and schematic of the working principle can be found in Chapter 2, Figure 2.23 and 2.24.

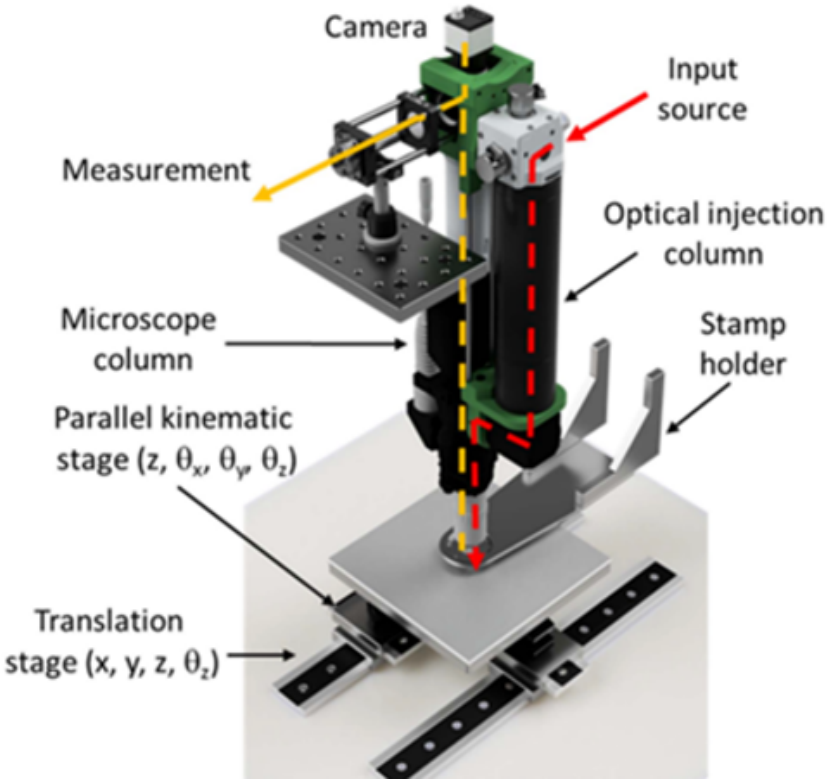

Figure 3.3: Schematic of the customised advanced transfer printing instrument [233].

3.2 Design and Fabrication of Supporting Frames on Silicon Substrates

3.2.1 Design of the Suspended Air-PhCC-Air Structure

To retain the air-clad geometry of the PhCC membrane, a supporting frame is required on the receiver substrate. The dimension of the PhC membrane itself is $9 \times 11\,\mu m^2$, the external planar membrane borders around the active area were limited to be $1\,\mu m$ in width to enable high density integration and minimise the total pixel area, which means the full photonic crystal active area is $7 \times 9\,\mu m^2$. The schematic of the PhCC membrane on its original substrate (also called donor substrate in transfer-printing) is shown as Figure 3.4 (a). Figure 3.4 (b) indicates the membrane connecting to the original substrate with an anchor and the left void after the membrane is picked up, also, the cavity area created by point defect is demonstrated as Figure 3.4 (c).

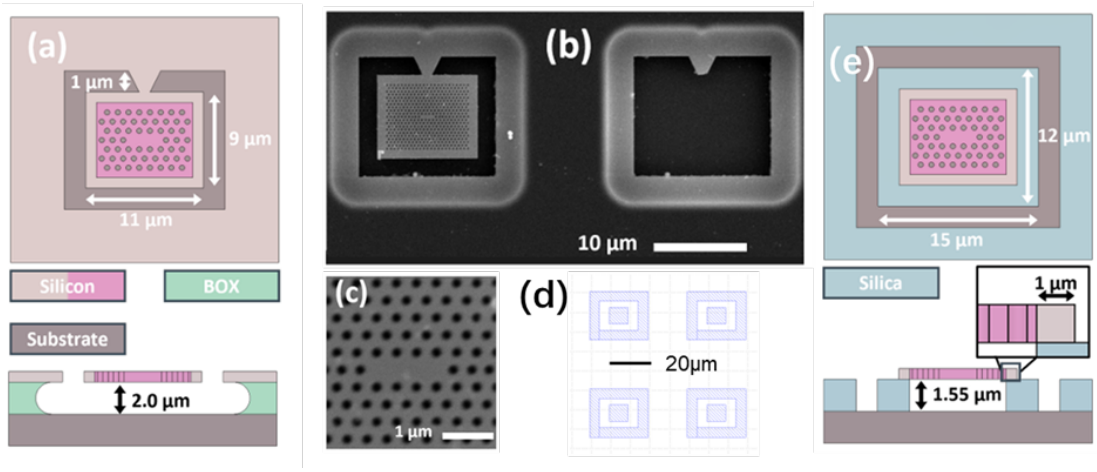

Figure 3.4: (a) Schematic of a single PhCC membrane on its original substrate (donor substrate). (b) Scanning Electron Microscope (SEM) image of a PhCC membrane on the donor substrate and the right-hand pixel has been transferred, leaving a void area with an anchor. (c) High magnification SEM image of the central area of the cavity by inducing point defect (d) GDS design of the supporting frames' structure used for positive photoresist. (e) Schematic of the PhCC membrane on supporting frames (silica or PR, only Silica frames shown) fabricated onto a receiver substrate (silicon). [234]

The core idea behind the design of the suspended Air-PhCC-Air structure is applying supporting frames and making the overlapped area between the supporting rectan-

gular frames and the membrane as small as possible and avoiding contact on the active area. The frames would be fabricated by laser lithography and the GDS map design used for laser lithography is shown as Figure 3.4 (d). The map was designed for positive photoresist and the solid part in the diagram would be exposed, thus a rectangular frame with $8.5 \times 9.5\,\mu\text{m}^2$ void area could be fabricated (the fabrication process will be discussed in next two sections).

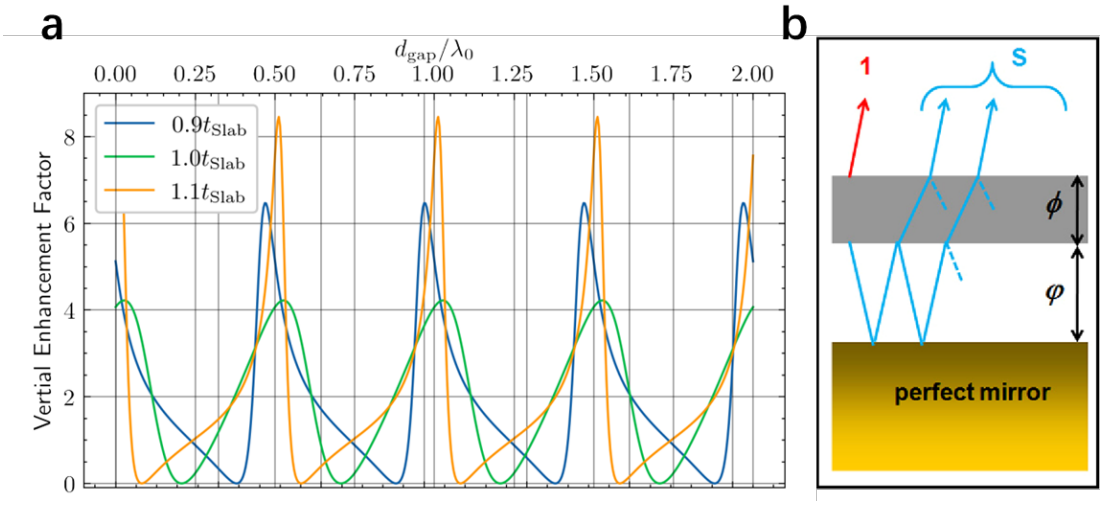

Figure 3.5: Diagram and Schematic of (a) relationship between vertical enhancement and the air -gap length of the Air-PhCC-Air-Reflector with varying PhCC thickness. (b) The membrane place over a perfect mirror [254]

From the simulation conducted by by Prof. Englund's group while they designed the PhCC geometry [131], the vertical enhancement factor varies periodically to the ratio of air-gap length and resonant wavelength while placing the membrane slab over a bottom reflector. The enhancement reaches the peak when the ratio is 1, and this can be found in reference [254]. Also, the enhancement factor curve is sharper when the PhCC slab thickness is thicker as shown in Figure 3.5 (a). Therefore, placing the PhCC membranes suspended over a bottom reflector with a air-gap length of 1550 nm, which is the designed resonant wavelength of the membrane, can efficiently enhance the optical confinement vertically and make the device show optimised performance. The Figure 3.4 (e) shows the ideal cross-section and over-view schematic of the Air-PhCC-Air Structure on silica supporting frames fabricated onto a silicon substrate (used as the

bottom reflector to form Air-PhCC-Air-Reflector structure as shown in Figure 3.5 b) by applying the accurate transfer-printing technique with in-plane positioning accuracy in the 100's of nanometres range.

3.2.2 Fabrication of Frames in Different Materials on Silicon Substrates

Before the assembly of the Air-PhCC-Air-Reflector structure demonstrated as Figure 3.4 (e), the first test was to show that these micro-PhCC membranes could be picked up from their original substrate, as shown and introduced in Figure 3.4 (a) and (b).

3.2.2.1 Fabrication of Photoresist Frames on Silicon Substrates

The photoresist frames in S1805 are easy to fabricate and suitable for printing due to their adhesive surface. The photoresist S1805 is a positive photoresist, which means the exposed area will be removed during development. It was spin-coated on the solvent and plasma cleaned silicon surface after spinning at 3800 RPM for one minute and soft baking on a 115℃ hot plate. The laser lithography machine could read the GDS design mentioned previously in Figure 3.4 (d) and expose the filled part. The frame structures would be clear and ready to receive PhCC membranes after 45 seconds development time in development solvent (micro-developer: DI water= 1: 1), also the thickness of the S1805 supporting frames is around 500 nm. The Figure 3.6 (a) presents the full fabrication process of photoresist S1805 supporting frames and (b) (c) are the microscope images of the supporting frames areas.

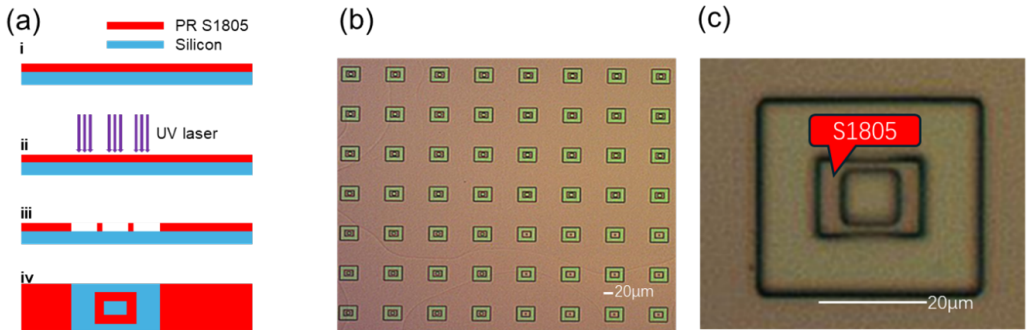

Figure 3.6: (a) Schematic of fabrication process of PR supporting frames and the top of a single frame after solvent development. (b) Microscope image of the photoresist frames array. (c) Microscope image of a single frame in photoresist S1805.

3.2.2.2 Fabrication of Silica (SiO_2) Frames on Silicon Substrate

The thickness of the supporting frames fabricated by PR is relatively difficult to control precisely during the development process. Also, a thicker photoresist is required in the fabrication of an Air-PhCC-Air structure with 1550 nm supporting frames, and most of thick PR is difficult to be spun evenly.

Silica can achieve a relatively controllable thickness by using Plasma-enhanced Chemical Vapour Deposition (PECVD) technique. In this fabrication round, the solvent and Oxygen plasma cleaned silicon sample was placed inside the Oxford instrument PECVD reaction chamber for 1550 nm silica deposition, and the measured silica thickness was 1508nm. The Filmetrics system [255] was used for thickness measurement via spectroscopic reflectometry, where broadband light reflects off the film surfaces and produces interference patterns based on the film's thickness and refractive index. The system fits the measured reflectance spectrum to a theoretical model to accurately determine the film thickness in a fast, non-destructive manner. The photoresist spinning and exposure steps followed the same procedure as described in the fabrication of photoresist frames, but were performed on the silicon substrate with deposited silica. Figure 3.7(a) illustrates the full schematic of the exposure steps.

The dry reactive ion etching (RIE) technique is then applied where the reactive plasma initiated and maintained by the RF field inside. The tool etches the exposed silica vertically at a rate of 28 nm/min with the following recipes: gas flow of 5sccm of

CHF_3 and 15sccm of Ar, 120 W of RF power at a pressure of 0.03 Torr. The unexposed photoresist acts as a protective layer to stop the vertical plasma reacting with unexposed silica, the dry etching process is shown in Figure 3.7 (b). Figure 3.7 (c) and (d) are the microscope captured images of the 1508nm silica supporting frames array on silicon substrate after oxygen plasma cleaning, the oxygen plasma cleaning step removed the unexposed photoresist layer and cleaned the surface of the sample.

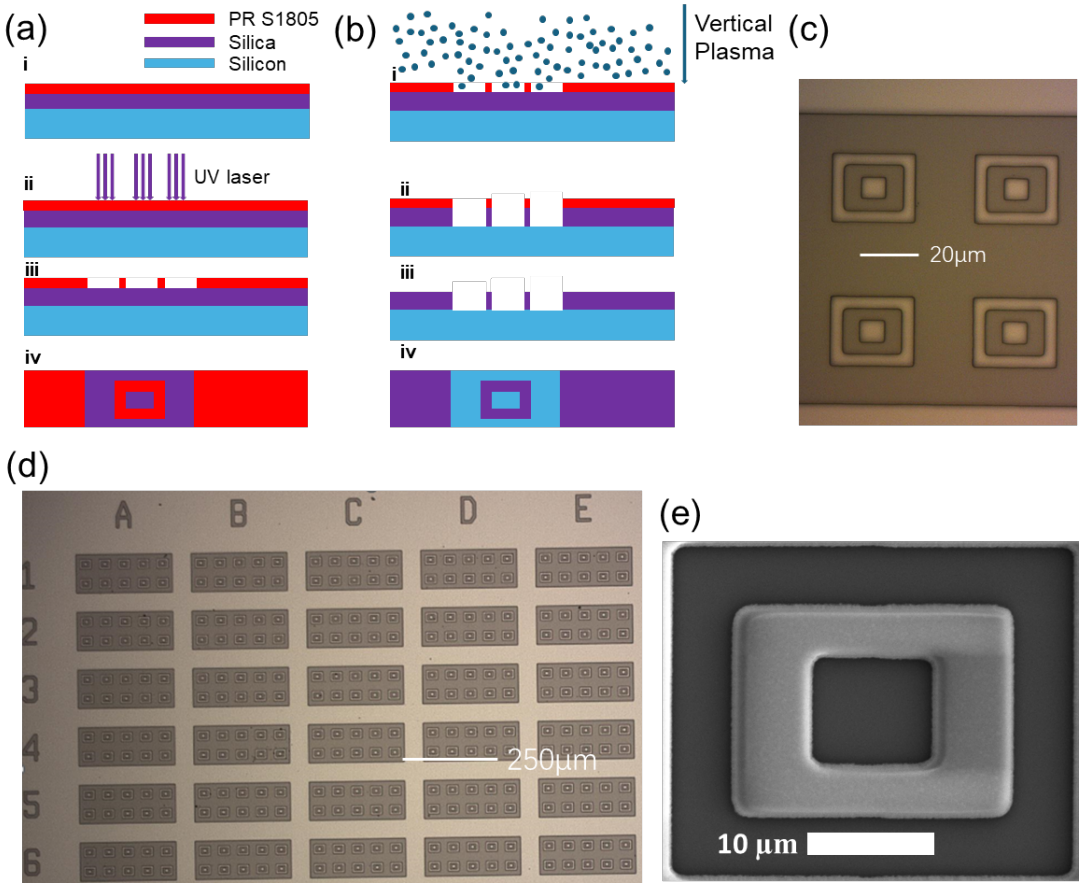

Figure 3.7: Schematic of (a) laser lithography process for silica frames fabrication. (b) Dry etching process to etch exposed silica away. Microscope captured image of (c) silica frames on silicon substrate. (d) the overview of the silica frames array. (e) SEM image of a single silica supporting frame on silicon substrate.

3.3 Transfer-printing (μTP) of Silicon PhCC Membranes onto Photoresist and Silica Supporting Frames

The transfer-printing process uses a soft polymer stamp to pick-up, align and place devices onto a host substrate. The polymer stamp used in this project is the prefabricated stamp used for nanowires transfer [98], and the ratio of the base (RTV615A) to the curing agent (RTV615B) is 10: 1. The adhesion of the stamp at this blending ratio is strong enough to pick up devices but not too strong to release on the receiver substrate. The contacting area of the polymer stamp is $30 \times 10\,\mu m^2$ as shown in Figure 3.8 (a), and matched to the single PhCC membrane's cross-section. The diagrams shown in Figure 3.8 (b) illustrates the complete process of a transfer-printing attempt. First, the stamp is aligned with the micro-device, followed by a quick contact to create strong adhesion between them. The stamp is then rapidly lifted to pick up the device. Next, the stamp and device are aligned with the target substrate, and another quick contact is made. Finally, the stamp is slowly released to print the device onto the new substrate.

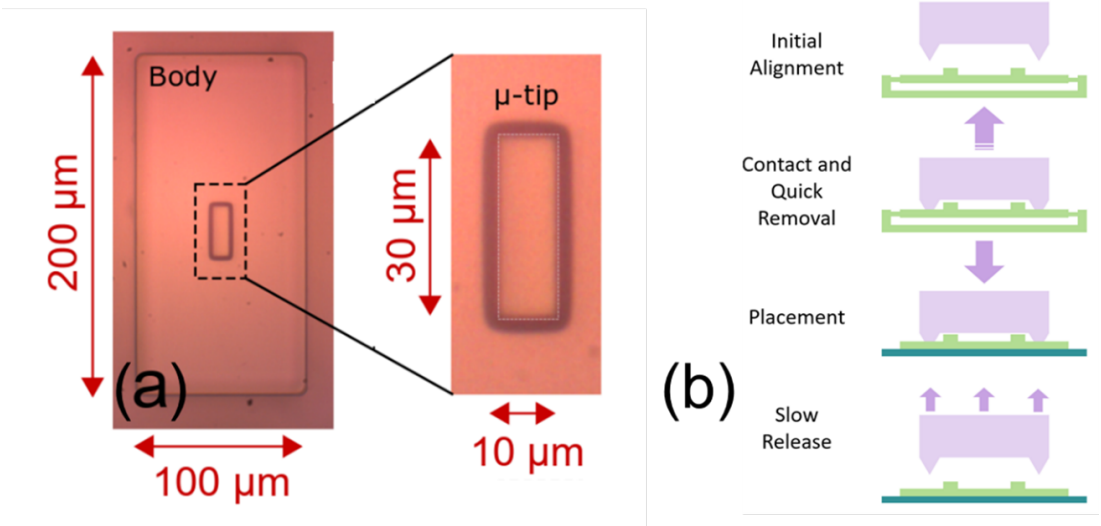

Figure 3.8: (a) Microscope image of the PDMS stamp and the tip (contacting) area. [104] (b) Schematic of a full transfer-printing process of a membrane device.

3.3.1 Attempted Printing of PhCC membranes onto S1805 Frames

During this attempt, the polymer stamp shown as Figure 3.8 (a) was fixed on the Nanoink NLP 2000 system [232] and the whole process could be monitored through a focused microscope lens and imaging system. This system was originally to be a commercially available dip-pen nanolithography instrument which was capable of depositing a wide variety of materials with sub-micron accuracy and precision, the 'pen' was then modified by a stamp holder as the 5-axis system made it suitable for mechanical transfer-printing. [256] Both donor substrate (PhCC membranes arrays on its original silicon substrate) and receiver substrate (PR frames on silicon) were fixed on the 5-axis controllable stage, the picking-up and printing processes were achieved by moving the stage up and down relative to the stamp. Top two diagrams of Figure 3.9 (a) indicate the alignment process through transparent PDMS stamp and the contacting process on silicon PhCC membranes' original substrate. The 5-axis stage moved downward rapidly to break the anchor (shown in Figure 3.4 b) and pick the membrane up after the alignment and contact. To print the membrane onto the target photoresist frame precisely, another alignment was required. Again, a fast contact was made by raising the stage and the membrane was then released on the supporting frame after a slow downwards movement of the stage. The alignment before printing and printed PhCC membranes on photoresist frame captured through the imaging system on NLP 2000 system are shown as two bottom diagrams in Figure 3.9 (a).

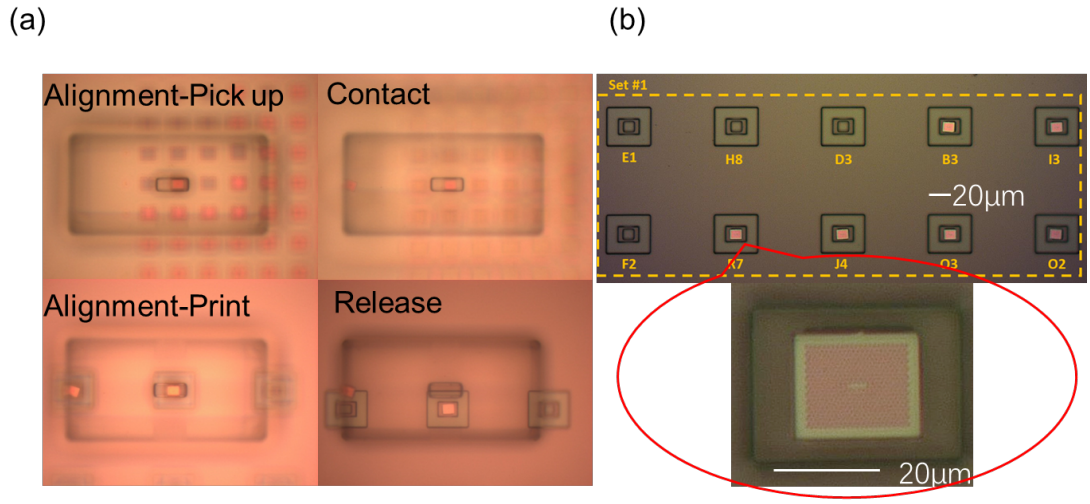

Figure 3.9: (a) Images of the picking up and printing process through the microscope and imaging system of the NLP 2000 system. (b) Microscope image of 6 printed membranes out of 10 attempts, and the high magnification image of R7.

Ten attempts were made to prove that this kind of PhCC membrane is suitable for transfer-printing, and it is possible to create an Air-PhCC-Air-reflector structure. The yield of transfer-printing is 60%. However, this yield is heavily depended on experience of operation and can be easily improved into 100% by practice.

3.3.2 Attempted Printing of PhCC Membranes onto Silica Frames

In the previous paragraph, the silicon PhCC membrane is shown to allow transfer-printing with limited yield. Transfer-printing of PhCC membranes onto 1508nm silica frames were then attempted to create an Air-PhCC-Air structure, and allowing optimised gap to the bottom reflector (silicon) to demonstrate a better optical reflectivity.

The transfer-printing process of PhCC membranes onto silica frames was the same as the previous process but on a different receiver substrate. Four attempts were done in this stage and the transfer-printing yield was 100%, and the microscope image of four printed membranes is shown in Figure 3.10 (a). Also, an image captured by SEM is shown in Figure 3.10 (b) to show an aligned and printed membrane on the silica frame.

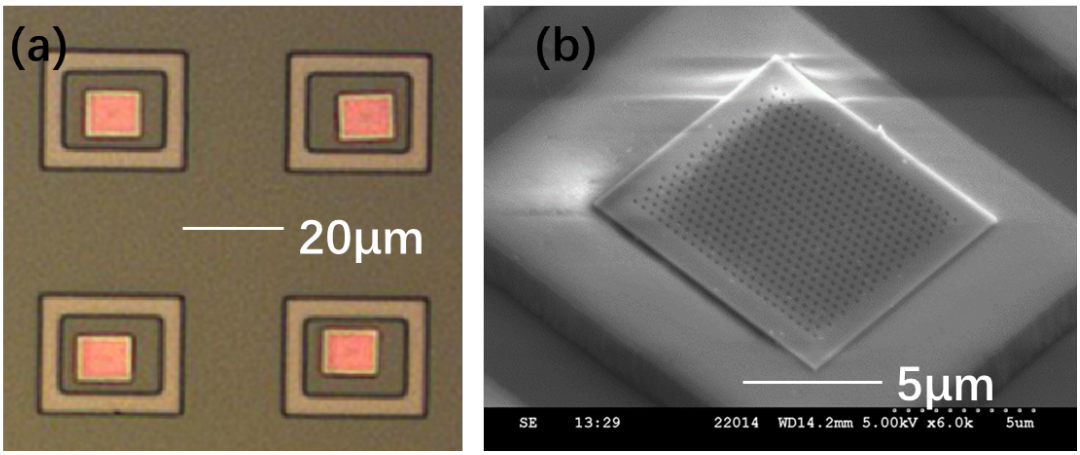

Figure 3.10: (a) Microscope image of four printed membranes on Silica frames. (b) SEM image of the well aligned and printed membrane.

The alignment quality can influence the optical confinement, ideally the active area on PhCC membrane should be well suspended and not overlap with the supporting frames. Therefore, the alignment limitations of the NLP 2000 system were investigated.

Under ideal conditions, the centre of the void area formed by the supporting frames should perfectly align with the centre of the PhCC membrane. To quantify the displacement of the membrane after transfer-printing, a MATLAB script was developed to analyse the colour intensity in both the vertical and horizontal directions. The script generates a graph showing the relationship between colour intensity and pixel position. Figure 3.11 presents an example graph for the top-left printed membrane shown in Figure 3.10 (a), in the vertical direction. From Figure 3.11, the relative pixel positions of the borders of both the printed membranes and the supporting frames are clearly distinguishable, allowing straightforward calculation of the vertical shift in pixels. As the dimensions of both supporting frames and membranes were previously measured and mentioned, one pixel equals to $0.15\,\mu$m. Similar calculations were then conducted to calculated the horizontal shift. The displacement of these four printed membranes are listed in the form of (horizontal, vertical), and they are (0.15μm, 0.75μm), (1.425μm, 0.6μm), (1.275μm, 0.675μm) and (1.125μm, 1.2μm), respectively. The average centre displacement of these 4 attempts is $(0.99 \pm 0.58\,\mu\text{m},\ 0.81 \pm 0.27\,\mu\text{m})$.

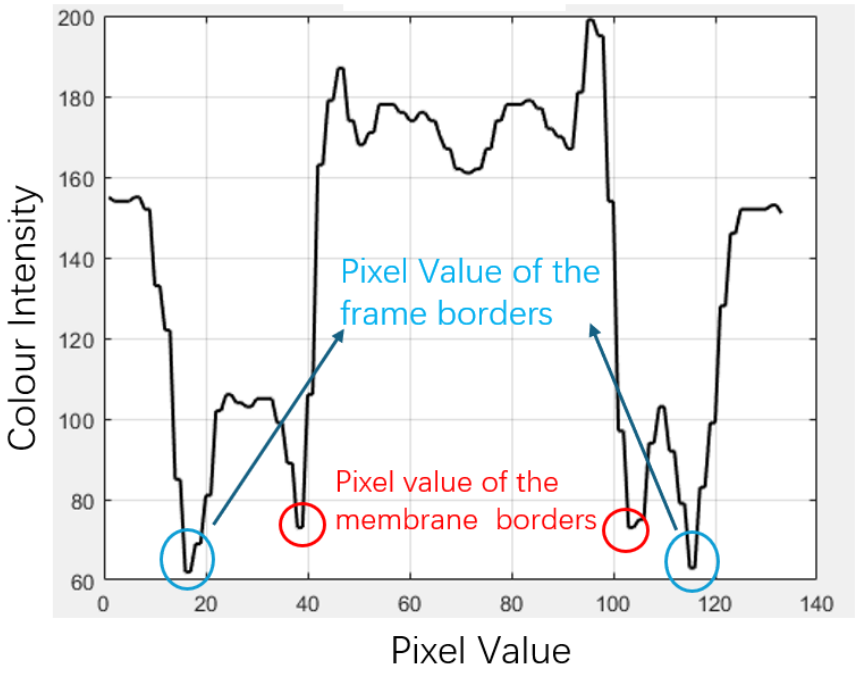

Figure 3.11: Example output graph of colour intensity calculation of the first printed membrane in vertical direction.

This displacement is micrometre level which is worse than the minimum placement error previously achieved by using the NLP 2000 system with the help of cross-correlation markers [105]. Although the SEM image shown in Figure 3.10 (b) indicates that most of the active region was well suspended, the accuracy of the transfer-printing still has high potential to be improved.

3.4 High Accuracy Transfer-printing and Characterisation of PhCC Membranes on Silica Frames Via A Customised Transfer-printing System with Optical Measurement Module

With the NLP 2000 system, the displacement of alignment can be $< 100\,\text{nm}$ [105], both the shearing during the release and the lack of velocity control are the real limitations of this methods. Therefore the advanced high-accuracy 6-axis system [233], as shown

in Figure 3.3, was applied to give precise velocity control during the printing process. Additionally, this system can not only precisely transfer-print the PhCC membrane but it has the ability to provide real-time measurement of resonant wavelength through the customised microscope and imaging system.

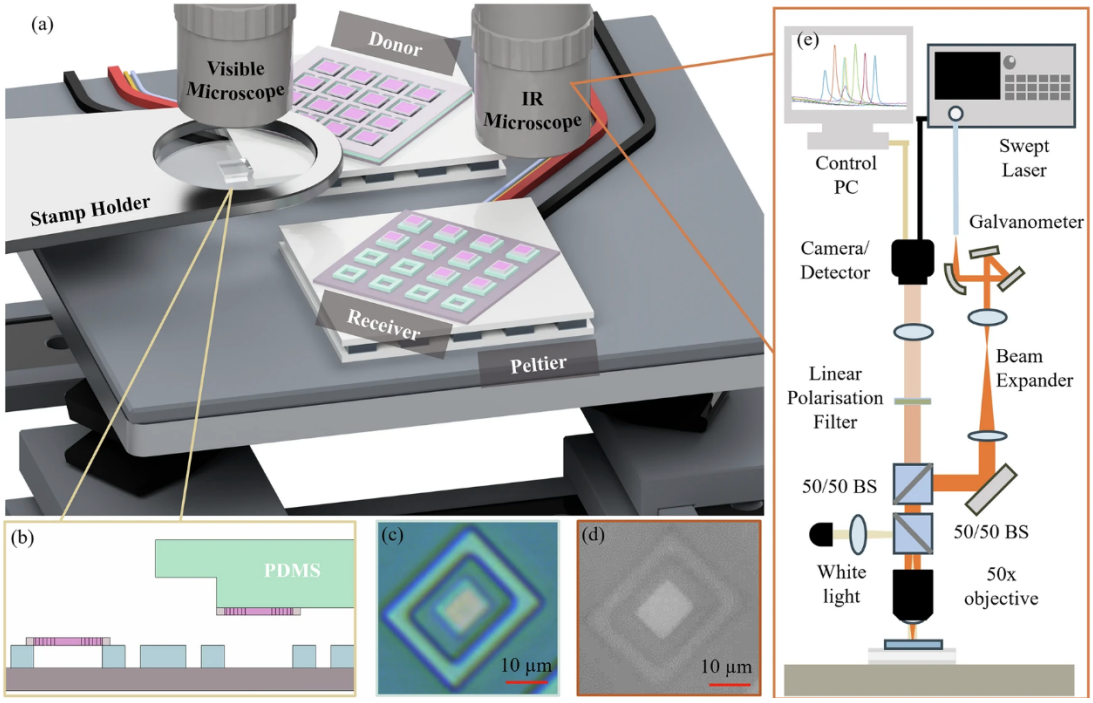

Figure 3.12: (a) Schematic of the advanced transfer-printing system with both donor and receiver mounted on the stage, microscopes for monitoring and spectrum measurement included. (b) Schematic of the pixel TP process. (c),(d) Images captured by monitoring and spectrum measurement microscope, respectively. (e) Schematic of the detail inside the spectrum measurement system embedded. [234]

Apart from the regular microscope and imaging system for the monitoring and alignment during the transfer-printing process, another column of optical devices was embedded in the system. It can inject swept-wavelength tunable laser into the silicon PhCC membrane, the reflected signal from the targeted PhCC membrane is coupled through the microscope objective to the IR camera system, enabling the assessment of the spatial mode and the measurement of the reflectivity spectrum during swept-wavelength operation. This system can not only optimise the alignment but also measure the resonant wavelength of PhCC membrane before and after the transfer-printing,

allowing for selectively pick up and research on the resonant wavelength after mechanical transfer-printing. Figure 3.12 is the schematic of the detail of the system. [234]

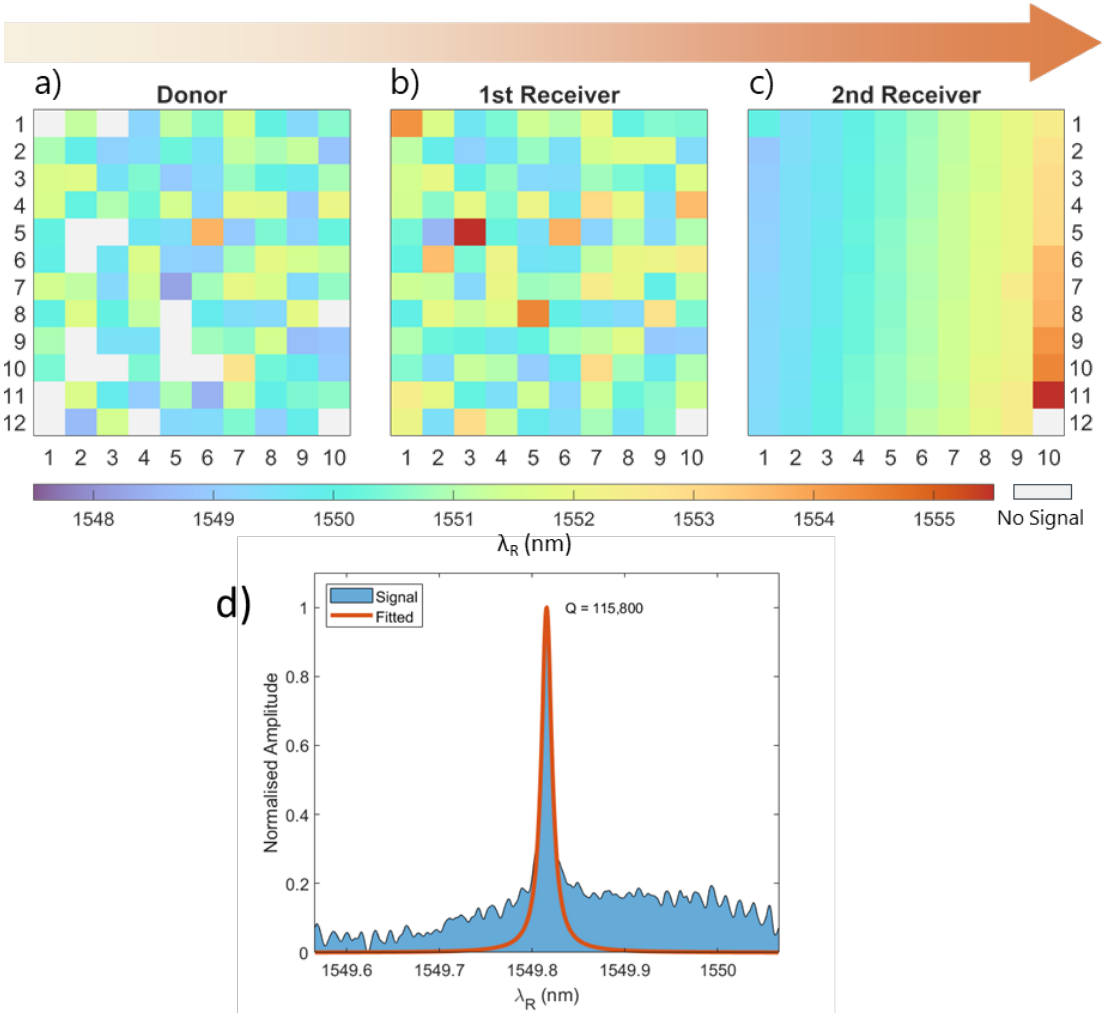

Figure 3.13: Graph of spatially measured resonant wavelength of silicon PhCC membranes array on (a) donor substrate. (b) First receiver substrate with silica frames. (c) Second receiver substrate with silica frames. (d) The reflectivity spectrum of a printed PhCC. [234]

To achieve spatial ordering of an as-fabricated PhCC array as a function of resonant wavelength, λ_R, 120 devices were initially measured on their native substrate. 119 devices out of 120 were successfully printed onto a first receiver with 1.5μm silica supporting frames following the spectral order. A reflectivity spectrum of a printed PhCC membrane is shown as Figure 3.13 (d). Another spectral measurement was con-

ducted onto the receiver after transfer-printing, however, the printed PhC membranes formed a disordered array again and the mean wavelength shift was $\pm 0.426\,\text{nm}$ and the standard deviation across the array is $0.438\,\text{nm}$. It was clear that a plastic shift was induced while the silicon anchor was broken during the picking up process. To overcome this, a second transfer-printing was operated, 119 devices were picked up from the first receiver and printed onto a second receiver with $1.5\mu\text{m}$ silica supporting frames following the spectral measurement order on the first receiver. Repeated spectral measurement was done on the second receiver with PhCC membranes printed and it showed a mean wavelength shift of $\pm 0.025\,\text{nm}$ and standard deviation of $0.139\,\text{nm}$. The mean and standard deviation wavelength shifts were $\pm 0.007\,\text{nm}$ and $0.021\,\text{nm}$, respectively, after two outliers printings were removed from the set. Those were cases where mechanical effects were expected due to accidental contact with the substrate during printing. The spatial ordering of PhCC arrays by the measured resonant wavelength is indicated as Figure 3.13 [234]. This wavelength shift indicates that the application of post-fabrication integration methods including in-situ measurement, selectively picking up and reordering printing of high Q-factor PhC membranes overcome the fabrication tolerance limit with a better uniformity.

3.5 Summary

This chapter mainly focuses on the transfer-printing of prefabricated silicon photonics crystal cavities (PhCC) membranes. In the first section, problems on PhCC membranes' uniformity in resonant wavelength induced during fabrication processes are indicated.

The second section shows design and fabrication of supporting frames in different materials based on the geometry structure of the PhCC membranes. The Air-PhCC-Air-Reflector structure is discussed to obtain a better optical confinement and the most suitable of the air gap length at a specific wavelength, 1550nm, is designed. Two silicon receiver substrates with thin photoresist and silica supporting frames, respectively, are shown in detail.

The third section demonstrates two rounds of transfer-printing of PhCC membranes with the NLP 2000 system. The transfer-printing yields are 60% and 100% on pho-

toresist and silica frames, respectively. The 60% of yield on photoresist frames proves the PhCC membranes are capable of transfer-printing and the yield is deeply affected by the spatial and velocity control of the tool. The successfully transfer-printing on silica frames shows that the NLP 2000 system can limit the misalignment caused during creation of the Air-PhCC-Air structure can be controlled at micro-metre level and it has the potential to be improved further by using cross-correlation design [105].

The final section presents 119 out of 120 high-accuracy transfer-printing of PhCC membranes on silica frames of 1508nm in thickness with an advanced system developed by the integrated photonics group in University of Strathclyde. The transfer-printing was based on two rounds of spectral measurements and applied to selectively pick up and spatially re-arrange the PhCC membranes as a post-fabrication method to beat the limit caused during fabrication. This creative new method replaces individual tuning on PhCC membranes and has the potential to increases the level of integration of future chip systems.

Additionally, the findings of this subproject indicate that the transfer-printing yield is not fundamentally limited by the technique itself. It can be significantly improved through iterative calibration and practical experience, with the achievable yield expected to approach 100% in mature processes.

Chapter 4

Excitation and Modulation of Embedded Semiconductor Nanowires with Micro-LED-on-CMOS Arrays

Within this chapter, the physical characteristics of semiconductor nanowires (NWs) is introduced first. A short literature review on the previous research done by our research group on integrated NW devices is summarised. The motivation of the integration of NWs and waveguides and the micro-assembly process are fully explained. The introduction also contains a short review of the development of micro-LEDs, and the introduction of the specific fourth generation of micro-LEDs arrays on CMOS integrated chips is presented. The applications of these micro-LEDs arrays and the micro-LED set up built for illumination and projection in this project are discussed and explained in detail. A frequency modulation signal was applied to the micro-LEDs arrays controlling panel and optically excited the fabricated PIC. The optical excitation performance including excited spectrum and frequency response is stated and explained, the limitations and optimised methods in the future are also discussed within this chapter.

4.1 Introduction

In the recent decades, light generation and modulation with nanoscale devices have garnered significant research attention, driven by the availability of a broad range of advanced materials and the growing maturity of hybrid and heterogeneous integration techniques [226] [257] [258]. Quasi-one-dimensional geometries, including nanowires (NWs) [259] [260], nanopillars [261], and nanobeam cavities [262], present attractive solutions for on-chip emitters with efficient light coupling to waveguide platforms. These devices have low emission thresholds, high optical confinement, tuneable emission wavelengths, and, especially, the ability to integrate directly with other photonic technologies, such as waveguides, antennas, or grating structures, [263] [264] such nano-scale level emitters are expected to play a crucial role in the next generation of nano-photonics applications.

4.1.1 Semiconductor Nanowires

Within all these quasi-one-dimensional devices, III–V semiconductor NWs are particularly interesting because of their outstanding potential in a wide variety of applications in electronic and optoelectronic fields, not only working as interconnects but also functional devices elements. Attributed to direct bandgap, excellent carrier mobility and low surface recombination rate, various optoelectronic devices, such as LEDs [265] [266], solar cells [267] [268], lasers [269], transistors [270], and photodetectors [271], have been developed using indium phosphide (InP) NWs, specifically. Semiconductor NWs are excellent candidates to realise compact photonic lasers as they provide both a gain medium and a cavity for lasing [163]. The high refractive index combined with their wire-like geometry, allows for strong two-dimensional modes confinement along the NW axis. The end facets of NWs offer optical feedback for these guided modes.

The InP NW used in this project were grown by the Australian National University using selective-area metal-organic vapour-phase epitaxy (MOVPE). The diameters of these stacking-fault-free pure wurtzite InP NWs vary from 80 nm to 660 nm. [52] These NWs also demonstrate room temperature near-infrared (NIR) lasing emission

($\sim$ 840–890 nm) [158] by optical pumping and can be applied in optical communications. These specific NWs were chosen as they have potential to work with pumping sources in visible spectrum range, overlapping with our micro-LED systems.

4.1.2 Previous Research on InP Nanowires

Researchers in our group fabricated a PDMS stamp (introduced previously in Chapter 2 and 3) to apply a micro-transfer-printing technique to manipulate, organise and print InP NWs onto different surfaces precisely, including PDMS, silica, and gold. Apart from that, lasing emissions were achieved after NWs being transfer-printed on various surfaces and excited by a pulsed laser source at room temperature. [57] Moreover, complex spatial patterns, including 1D and 2D, were successfully formed and this proved that NWs could be applied as building blocks within nano-photonic on-chip communication devices. [98]

NWs were used for the realization of coherent optical sources with ultra-small footprint and were capable to be picked up from original surfaces and printed onto various substrates. This means high densities of NWs can be integrated with a large number of photonic devices dependent on applications purposes, therefore, NWs have high potential in the development of photonic integrated circuit.

Our research group transferred NWs from their growth substrate onto a target quartz disk, and randomly spatially distributed them on the surface. A rapid characterization micro-PL set up was applied here by our collaborators at the University of Manchester [159], and repeated measurements were conducted on the NWs' lasing parameters. These randomly placed NWs were selected and sorted as different groups by threshold energy density, and subsequently printed in arrays onto a secondary substrate. [60] This research helped to select NWs with similar characteristics for further on-chip photonics systems' development and can keep the uniformity of chips performance.

The dimension of NWs is very compatible with waveguides in developing on-chip lasers in passive photonic integrated circuits (PICs). The previously mentioned high-accuracy selecting and printing technology can be applied here to play with semi-

conductor NWs and pre-fabricated waveguides to build low power, short haul [272] interconnects in applications such as biosensor systems [273]. This pre-NW-transfer waveguide fabrication route [226] is very attractive for the increase of scalability of PICs.

The relatively high refractive index contrast of semiconductor NWs to low refractive index substrates (silica and polymer materials) or air allows very strong optical confinement inside NWs with very small diameters, which is hundreds of nanometres. Therefore, NWs based waveguides are important for the optical network formation and as interconnections in the next generation of PICs.

Our group hybridly integrated NW lasers with pre-fabricated polymer waveguides on mechanically flexible substrates by using the transfer-printing technique to put NWs at one facet and on top of waveguides. Both integration routes indicate that optical power levels in order of micro-watts can be coupled from NWs lasers into polymer waveguides and collected at the end facet with -21dB and -17dB loss (mainly caused due to mode mismatch between NWs and polymer waveguides). [57]

This mismatch can be improved by embedding emitters (NWs) into waveguides structures. This embedded design is so called post NW transfer waveguide fabrication. During this process, NWs will be transferred onto substrates first, and waveguides are determined later with lithography techniques which is spatially accurate. [226]

4.1.3 Motivation, Challenges and Aims

Based on current research, it is obvious that there are two main challenges that prevent the development of scalability from single device to on-chip systems.

The first challenge is the requirement for a mature technique to integrate multiple emitters with existing chip-scale platforms. As nano-emitters, NWs especially, are grown on their own growth substrate in a large population as mentioned previously in reference [52]. They are required to be transferred onto existing optical structures or onto a receiver substrate that can be used for patterned waveguide circuitry around transferred nano-emitters. There are many optional techniques for hybrid and heterogeneous integrations, including micro-transfer-printing, [98] optical tweezers [274]

and micro-probe-based integration [260] [275]. In our research group, micro-transfer-printing is the main method used for NWs emitters' integration. The micro-transfer-printing technique provides better spatial distribution as it gives better control over NWs placement on the receiver substrate, and it is important for future scaling in PICs.

The second challenge is, to reach NWs lasing, coherent light sources like continuous-wave or pulsed laser are widely used currently. Coherent light sources (typically lasers) are bulky, power-consuming, and require precise alignment. These limitations make it difficult to simultaneously excite multiple nanowires (NWs), which in turn hinders parallel optical excitation and limits scalability. Therefore, specific applications in the future such as wearable devices or biosensors are hard to be realised.

Alternatively, a more compact pumping source with high scalability, high optical output power, and fast switching capability is attractive as a replacement for lasers. Micro-LEDs are promising candidates, as they offer higher optical output power ($\sim$ 1 mW) and faster switching bandwidth ($\sim$ 120 MHz) [182] [180]. Importantly, their compact size and the integration of CMOS driver circuits enable individual pixel-level control. These features make micro-LED arrays on CMOS a strong candidate for serving as a pumping source to excite and modulate multiple semiconductor nanowires at high frequencies to increase the scalability.

So in this chapter, I present the approaches developed to address these two key challenges in nanowire integration and excitation. First, I demonstrate the use of micro-transfer-printing as a scalable and precise method for integrating nanowire emitters onto chip-scale photonic platforms, enabling controlled spatial placement suitable for future large-scale PIC architectures. Second, I introduce a micro-LED-based pumping set-up as an alternative to traditional bulky laser systems, highlighting its advantages in compactness, switching speed, and pixel-level addressability for parallel nanowire excitation. Together, these developments form the foundation for achieving highly scalable nanowire-based photonic devices and integrated systems.

4.2 Chip Fabrication and Photo-luminescence Set-up

4.2.1 Nanowires Transfer-printing

4.2.1.1 Metal marker deposition

The metal marker was deposited at the beginning of the fabrication to indicate the position for NW printing, and they can be used for alignment of waveguides fabrication in the next step to embed NWs accurately in the centre of the waveguide.

The pattern was defined on a glass substrate with photoresist spin-coated (solvent cleaned first, then oxygen plasma cleaned) by a Heidelberg DWL 66+ laser lithography system [194]. The exposed photoresist was developed and removed, leaving behind the unexposed regions, which defined the desired patterns on the glass substrate. A bilayer of titanium and gold (50:200 nm) was deposited onto the sample via electron beam evaporation using a Temescal [197] system. The metal layers adhered directly to the glass substrate in the patterned regions not protected by photoresist. The metal deposited on the regions covered by unexposed positive photoresist was removed using a micro-stripper solvent during the lift-off process, leaving metal only in the exposed pattern areas in the shape defined by the lithographic process. The schematic of this marker fabrication process is shown as Figure 4.1 (a), the detailed process and chemical reagents were introduced in Chapter 2 previously. The metal marker pattern was designed with an asymmetric profile shown in Figure 4.1 (b), and the central axis of the metal marker's tail was designed to be overlapped with the polymer waveguide's central axis.

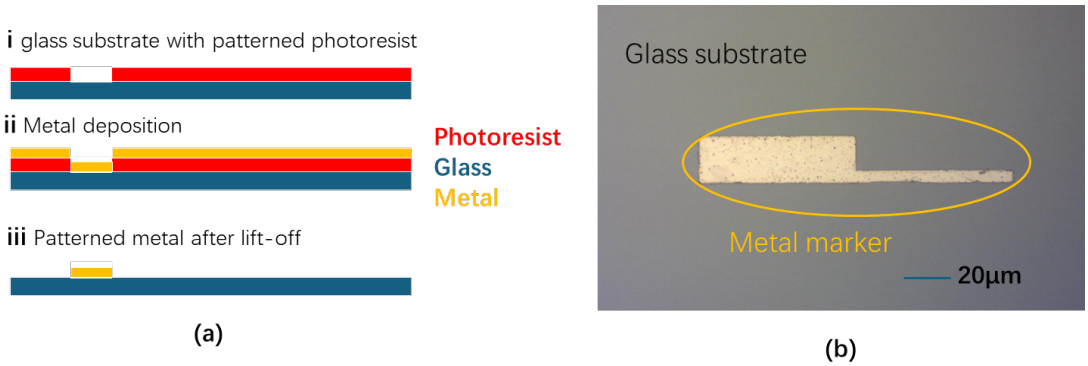

Figure 4.1: (a) Schematic of metal deposition and lift-off. i) Glass substrate with photoresist after laser lithography, photoresist in metal marker pattern area is solvent removed after exposure. ii) Titanium and gold layer deposited on the whole surface of the sample in Temescal chamber. iii) Micro-stripper solvent removed unexposed photoresist, and the metal deposited on photoresist area were lift away at the same time, only metal in exposed pattern left. (b) Microscope captured single metal marker structure.

4.2.1.2 Transfer-printing on Different Substrates and Accurate Alignment

The pre-mentioned PDMS stamp was applied on the NLP 2000 system to transfer NWs from their growth substrate onto another PDMS substrate first. The new PDMS substrate with a large population of printed NWs became the donor substrate for the second stage. A group of InP NWs with different diameters were transfer-printed from the donor onto a Quartz substrate first for spectrum measurement (spectrum measurement is discussed after the set-up section). Figure 4.2 (a) shows the LEICA microscope set-up captured image of printed NWs on a quartz substrate. The information of these InP NWs with different diameters can be found in reference [52]. Figure 4.2 (b) is a SEM image of a single printed NW on a silicon substrate. [276]

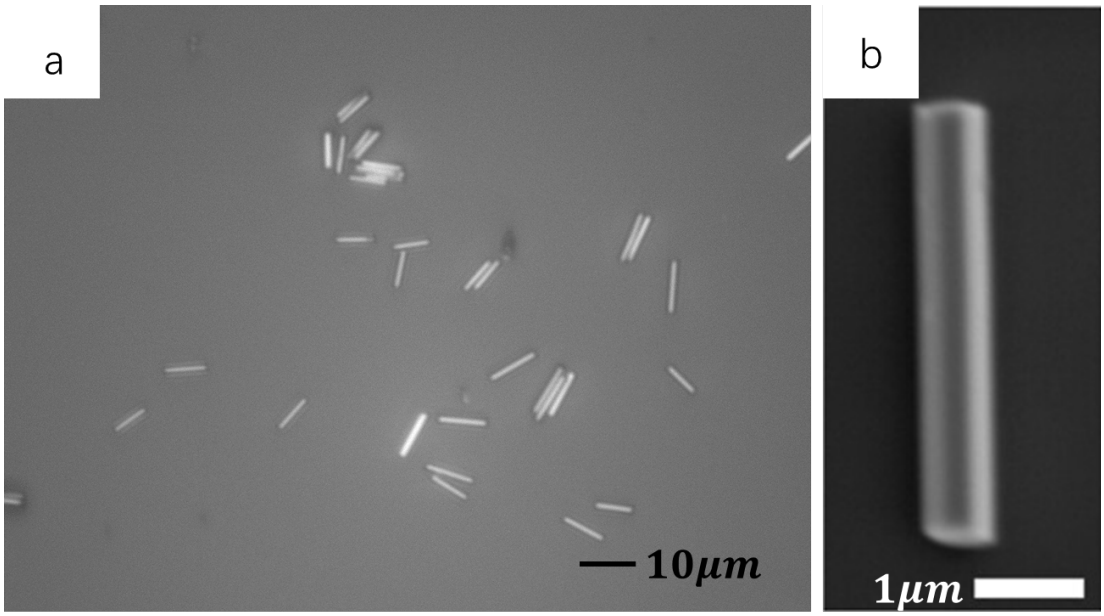

Figure 4.2: (a) Printed NWs on a quartz substrate, captured using LEICA microscope set-up. (b) SEM captured image of a representative InP NW on a silicon substrate [276].

To fully embed the NW inside polymer waveguide, they have to be printed at the middle point of a metal marker which shares the same central axis as the waveguide. This requires high accuracy alignment during the transfer-printing process.

The schematic of micro-transfer-printing process of a single NW was previously shown as Figure 2.13 in Chapter 2. Prior to the printing step, a MATLAB-based colour intensity analysis script (as previously described in Chapter 2) was employed for alignment. This script analyses the colour intensity at the tail end of the metal marker in order to determine the central axis line. It can also detect the position of the nanowire (NW) due to its visual contrast with the stamp material. Diagram (1) in Figure 4.3 (a) shows a nanowire that has been picked up by the stamp. The nanowire (NW) was first manually positioned near the estimated central axis by visual inspection as diagram (2) in Figure 4.3 (a). Following this, the colour intensity analysis script was executed to evaluate the alignment accuracy. Based on the output, the NW position was iteratively adjusted until the intensity profile resembled that shown in Figure 4.3(b), indicating that the NW was well aligned with the central axis and ready for printing. Diagram (3) in Figure 4.3 (a) and figure 4.3 (c) are images of a printed

NW captured by imaging system in the NLP 2000 system and microscope, respectively.

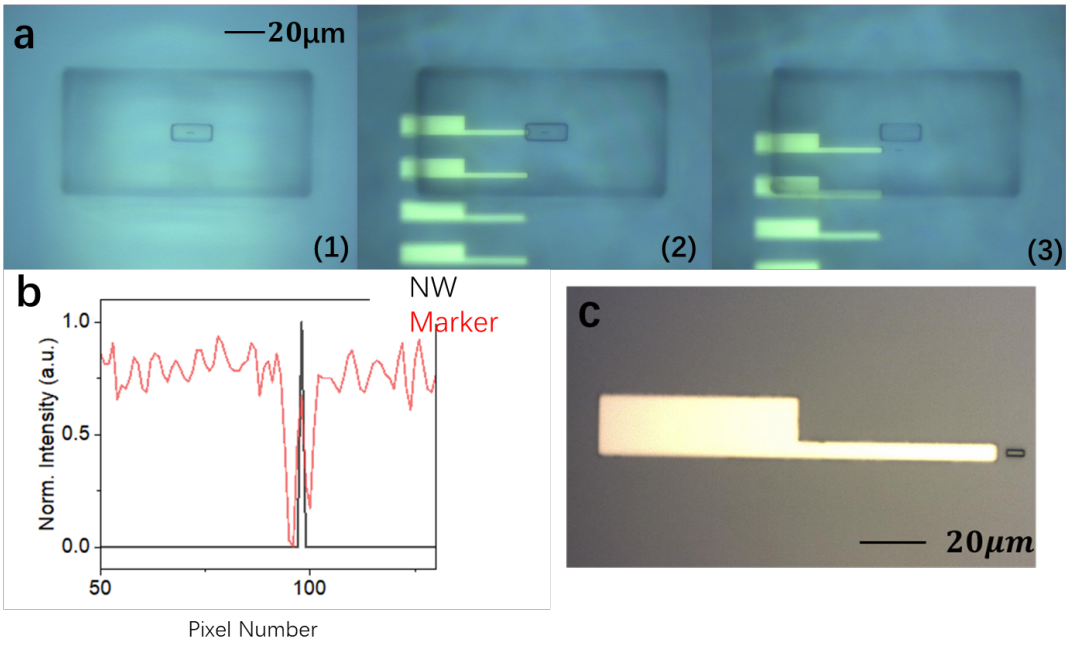

Figure 4.3: (a) Alignment and printing images captured by imaging system on NLP 2000 (b) Colour intensity analysis graph to show that the NW is overlapped with the metal marker central axis. (c) A printed nanowire next to the metal marker captured by the microscope.

In total, 20 NWs were aligned and transfer-printed from the PDMS donor substrate onto the glass substrate with pre-defined markers. After the transfer-printing process, the sample was then solvent cleaned for polymer waveguide fabrication, and all printed nanowires survived. The implementation of the colour intensity analysis during the alignment process enabled the integration displacement to be confined within the sub-micrometre range [104]. An analysis of the integration accuracy will be provided in the subsequent section to assess the quality of nanowire embedding within the polymer waveguides.

4.2.2 Polymer Waveguides Fabrication

SU-8 series polymer photoresist are very good candidates for optical waveguides, as their high refractive index ($\sim$ 1.6) and low absorption across the visible to IR spec-

trum are attractive for low loss optical waveguides. The transmission of SU-8 TF 6000 (0.5–10 μm in thickness after development) is greater than 95% for wavelengths above 400 nm. [200] Other advantages such as excellent adhesion, excellent chemical and thermal resistance, spin coat-able and material compatibility make it good as passive or internal connection devices material in PICs. Also, the characteristics of SU-8 series is sensitive to broadband UV radiations, patterns could be featured after exposure under UV emission. This made it work compatibly with the mask-less laser lithography system, Heidelberg DWL 66+ [194].

The chosen SU-8 TF 6005 resist was spun onto solvent cleaned sample surface at 500 RPM for 5 seconds and 4000 RPM for 1 minute. A step of soft baking on a 95℃ hot plate for 5 minutes was also necessary before laser lithography. The transparent photoresist made metal markers clear for execution of global alignment in the laser lithography tool. The exposure followed the waveguides design shown in Figure 4.4 (a), where the central axis of waveguide was designed to be overlapped with the centrsal axis of tail part of the markers, this alignment was executed by the Heidelberg and the displacement of this alignment was around $\sim 0.5\,\mu$m [194].

A step of 2 minutes post-exposure baking on the same hot plate (95℃) was applied to cure the exposed area of SU-8-6005 polymer before development. Either Propylene glycol methyl ether acetate (PGMEA) or acetone could be used for development. For PGMEA, the process was: PGMEA for 45 seconds, isopropyl alcohol (IPA) for 15 seconds, then put the sample back to PGMEA for 10 seconds and finally cleaning the sample with IPA again. The development process with acetone was easier, requiring the sample in acetone for 2.5 minutes(for this specific exposure dosage parameters, and it would change with the dosage parameters and exposure patterns' feature sizes). The last step before cleaving the sample was hard baking, parameters for this step were 160℃ for at least 40 minutes. This step cured the waveguides further and made it hard enough to survive in the cleaving stage.

Cleaving of waveguides can create facets on the ends for efficient coupling to extend optics. From the datasheet [200], the theoretical thickness of the waveguides after exposure and development should be $\sim 4\,\mu$m. To protect the waveguides during cleav-

ing, another thick layer (thicker than 4 μm) of photoresist (SPR7.0 [219]) was spun over hard baked waveguides as a protection layer. A diamond tipped pen was used to scratch the backside of the sample for cleaving, the detailed cleaving process was introduced in Chapter 2 and the schematic was shown as Figure 2.11. The protection layer could be easily removed with standard solvent cleaning procedure, and Figure 4.4 (b) demonstrates the image of the cleaved facets. The 20 printed nanowires embedded inside polymer waveguides are all shown in Figure 4.4 (c) from images (1) to (5).

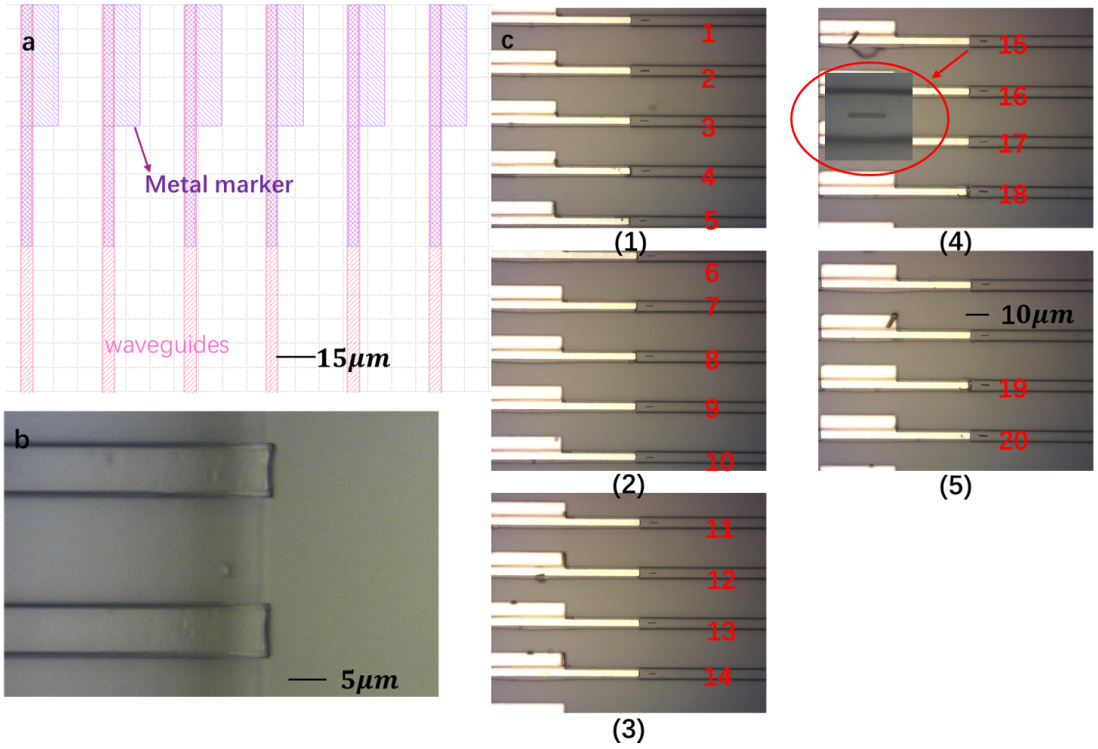

Figure 4.4: (a) Pattern design for DWL 66+ laser lithography system, purple patterns are metal markers, and pink parts are waveguides design. (b) Two facets on the edge of the sample. (c) Microscope captured images (1) to (5) to indicate 20 printed NWs embedded inside the waveguides.

4.2.3 Waveguides Profile Analysis and Overall Alignment Analysis

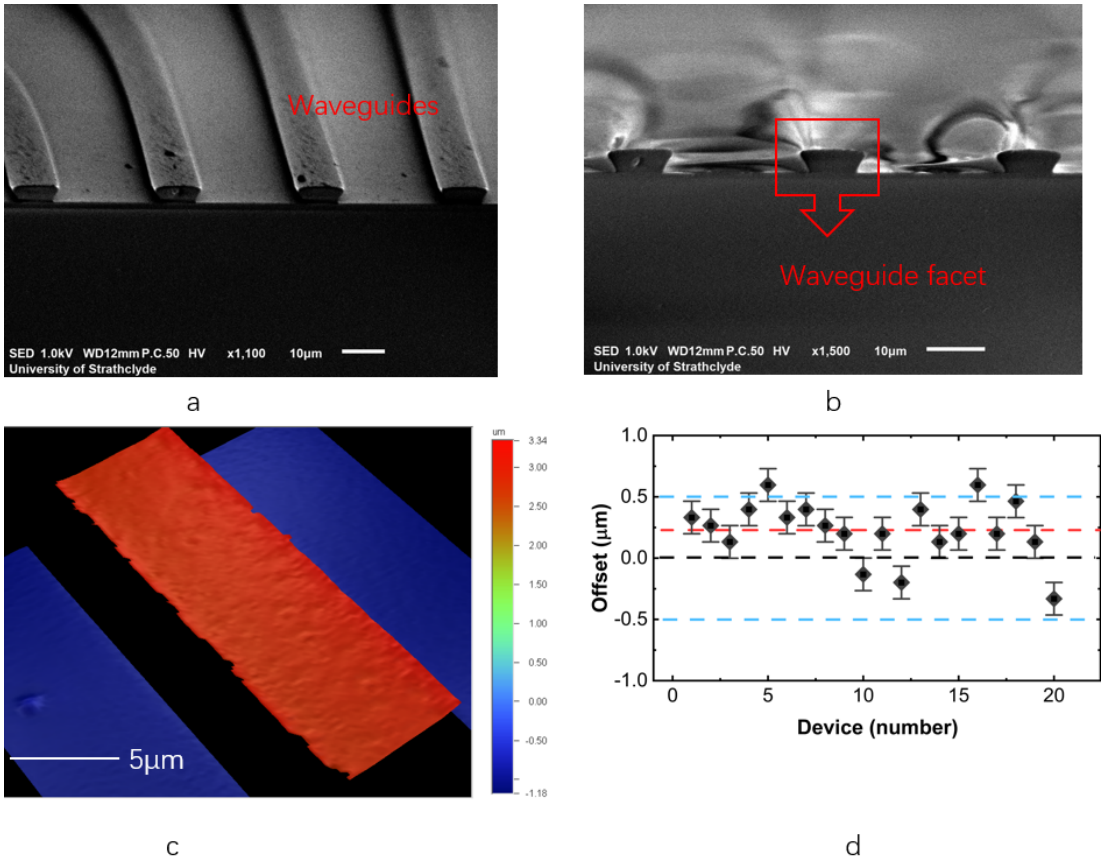

Figure 4.5: (a) SEM image of the waveguide's facet. (b) Cross-section SEM image of the facets. (c) Optical profiler scanner scanned 3D interactive diagram of the waveguide, the measured thickness of waveguide is $\sim 4\,\mu$m. (d) A lateral offset scatter plot of the 20 nanowire-in-waveguide devices is presented, with a red line representing the average offset of 228 nm. [276]

At this stage, several tests and analyses were conducted for device characterisation. The first involved profiling the waveguides and scanning their facets. A scanning electron microscope (SEM) was used to image the waveguide facets, as shown in Figure 4.5(a) and (b). The undercut profile is clearly visible, which is expected given that SU-8 is a negative photoresist [277]. The measured thickness of waveguides was $\sim 3.8\,\mu$m and it matched the result from optical profiler scanning shown as Figure 4.5 (c). The thickness of the waveguide was slightly less than the value specified by KAYAKU Advanced Materials [200], which may be attributed to the optical focus offset parameter used

during the mask-less laser lithography exposure process.

To analyse the positioned accuracy of the 20 NWs embedded inside waveguides, another script written in MATLAB was used. Similarly to the overlay alignment method used for the device fabrication, it could calculate the central axis of the waveguide and compare it with the axis of the printed NW. The average offset of the nanowire major axis from the centre of the waveguides was 228 ± 54 nm. Figure 4.5 (d) demonstrates the scatter plot of all 20 devices. This analysis following the method in reference [105].

4.2.4 Micro-LED-on-CMOS: Driver, Chip and Performance

Micro-LED-on-CMOS has been developed over the last decade in both functionality and scalability. The applications of micro-LED are wide, telecommunications [278], imaging [279] and displays [175] areas all benefit from the development of compact arrays of electronically addressable arrays of LEDs. Our team recently developed a 128×128-pixel micro-LED-on-CMOS display capable of nanosecond pulsing, independent pixel control at frame rates up to 0.5 Mfps with a function of 5-bit brightness adjustment. [280]

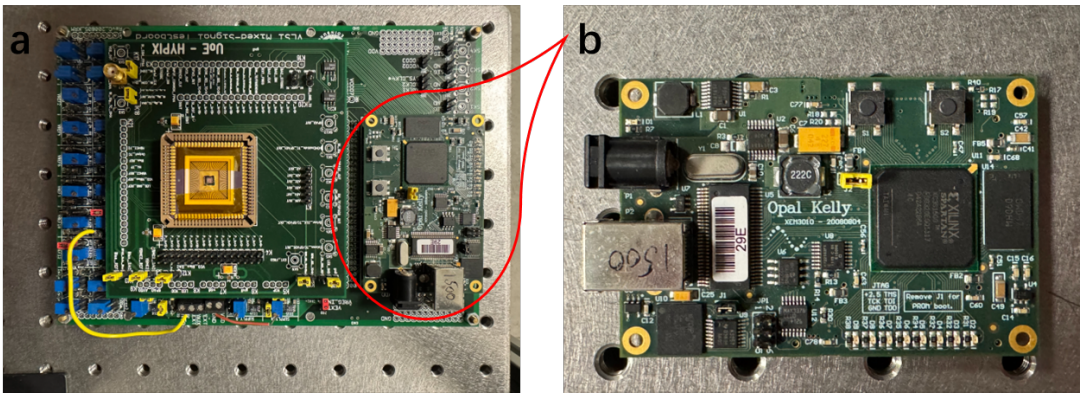

Figure 4.6: Images of (a) CMOS control board. (b) FPGA control module.

With the bonded CMOS driver, the micro-LED chip can demonstrate a range of functions, such as global and rolling shutter and grayscale projection. The particular system used in this work was a 16×16 array, selected for its ability to achieve micrometre-scale pixel-level brightness. The CMOS board and Field-Programmable

Gate Array (FPGA) control module used for driving the micro-LED array are shown in Figure 4.6(a) and (b), respectively. The micro-LED chip on this CMOS driver is swappable, and a GaN based micro-LED emitting at 405 nmwas selected as the optical pumping source. This wavelength can be effectively filtered out using a bandpass filter, thereby preventing interference during the detection of the nanowire emission.

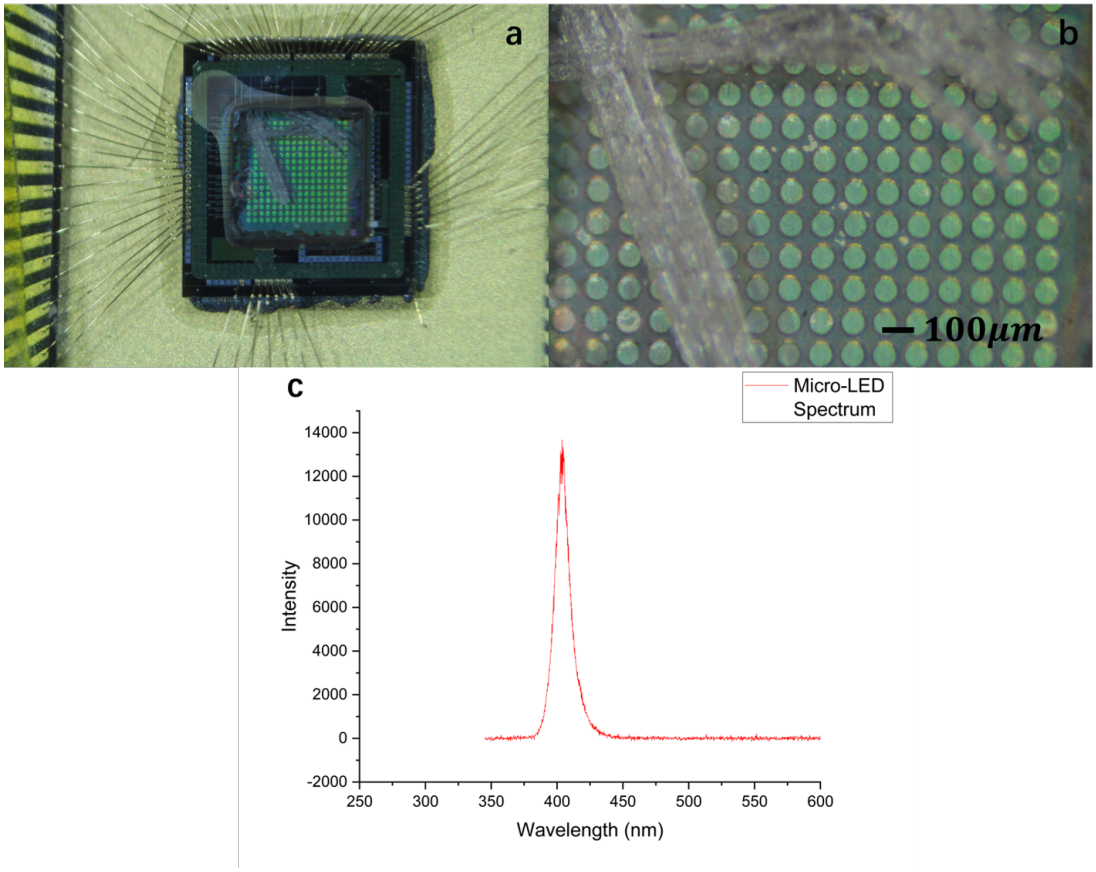

Figure 4.7: Images of (a) Overview of the micro-LED chip. (b) Micro-LED pixels. (c) Spectrum of the emission.

The diameter of the individual circular micro-LED pixels is 72 μm, on a pitch of 100 μm as shown in Figure 4.7 (a) and (b). It was prefabricated by the institution and the optical power of the individual pixel is $\sim$ 1 mW with an emission length of 405 nm. Spectral performance of the LED devices was measured prior to the NW pumping experiments and the spectrum graph is shown in Figure 4.7 (c). From the information in reference [182], it can have modulation bandwidth of up to 100's of MHz,

and the measured cut-off frequency for the full on-off keying of the micro-LEDs pixels was ∼120 MHz, which was limited by the CMOS drive electronics.

4.2.5 Micro-Photoluminescence (μ-PL) Set-up

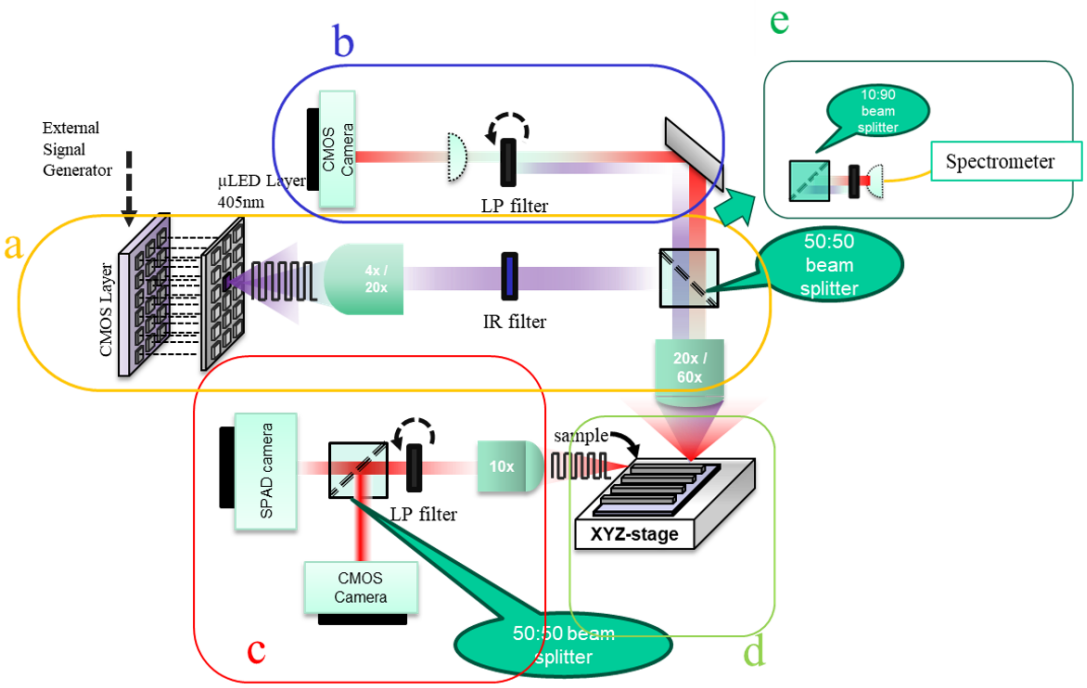

Figure 4.8: Schematic of the micro-Photoluminescence set-up. Blocks of (a) Projection optics. (b) Top imaging system. (c) Edge detector. (e) Stage for samples. (f) A plug in system for NW spectrum measurement.

The micro-LED-on-CMOS array was first mounted on a 3-axis stage to enable alignment with the free-space optical components. A schematic of the experimental setup is shown in Figure 4.8, which can be divided into five functional blocks. Block (a) contains a pair of optical lenses, either 20× and 60× (better projection power), or, 4× and 20× (larger field of view), to provide different magnifications and fields of view, along with a 50:50 beam splitter. This arrangement projects selected pixels from the micro-LED array onto the chip sample mounted on an XYZ-stage, as illustrated in block (d). An infrared (IR) filter is placed between the micro-LED chip and the beam splitter to suppress unwanted IR emission originating from defect-related recombination in the

micro-LED pixels. [281]

A high-quantum-efficiency CMOS camera was positioned above the setup (labelled as block b) to provide real-time visual feedback during the alignment process. With the aid of a mirror and an imaging lens, the camera enabled precise positioning of the projected LED emission onto the embedded nanowire region. To further optimise the imaging of nanowire emission, a long-pass (LP) filter (700 nm) can also be integrated into this optical path. The filter effectively suppresses the visible excitation light from the LED source, allowing for the selective detection of the nanowire emission, which is theoretically expected to occur in the near-infrared (NIR) range.

To collect the NW emission that was coupled into and guided through the waveguide, an edge detection setup, as shown in Figure 4.8 (c), was employed to monitor the optical signal at the waveguide's output facet. A 50:50 beam splitter was introduced in this path to divide the outgoing signal between a CMOS camera, used for alignment, and a single-photon avalanche diode (SPAD) camera (PhotoForce32) [282], which enabled time-domain light modulation measurements. To ensure that only the near-infrared (NIR) emission from the excited nanowire was recorded, a LP filter (700 nm) was placed in the detection path to suppress the visible pumping light coupled into waveguides.

Moreover, to enable spectral characterisation of the NW emission, an additional module, block (e), can be integrated into the optical path from the top. This block comprises a 10:90 beam splitter, a LP filter (700 nm), and a collection lens, which work together to couple most of the nanowire emission into an optical fibre for input into a spectrometer.

4.3 Measurements and Results Analysis

4.3.1 Printed InP Nanowire Excitation and Spectrum Measurement

The very first step of this project is proving that the printed InP nanowire can be optically pumped by the micro-LED's pixel projection. To prove this and characterize printed NWs' emission properties, a quartz disk substrate was used as a receiver

substrate for an array of NWs' transfer-printed as mentioned in section 4.2.1.2. Figure 4.9 (a) shows a top CMOS camera capture image of one micro-LED pixel projecting onto a printed single nanowire device, the 20×/60× pair of lenses were selected for projection with better magnification and output optcal power. The brightest micro-LED pixel projects a total fluence (irradiance) of approximately 280 $\mathrm{mW/mm^2}$ onto a sample, and the output power was measured by placing a power meter detector below the 60X lens. Based on the spatial overlap between the projected micro-LED pixel and the nanowire device, it is estimated that approximately 1% of the pixel's emitted illumination is incident on the single nanowire. The airy disks at the nanowire's facets are clearly visible in Figure 4.9 (b) with the LP filter on, this means that the printed nanowire is emitting, and the wavelength is in the IR range. Therefore, the projected micro-LED pixel is powerful enough to optically excite printed InP nanowire devices.

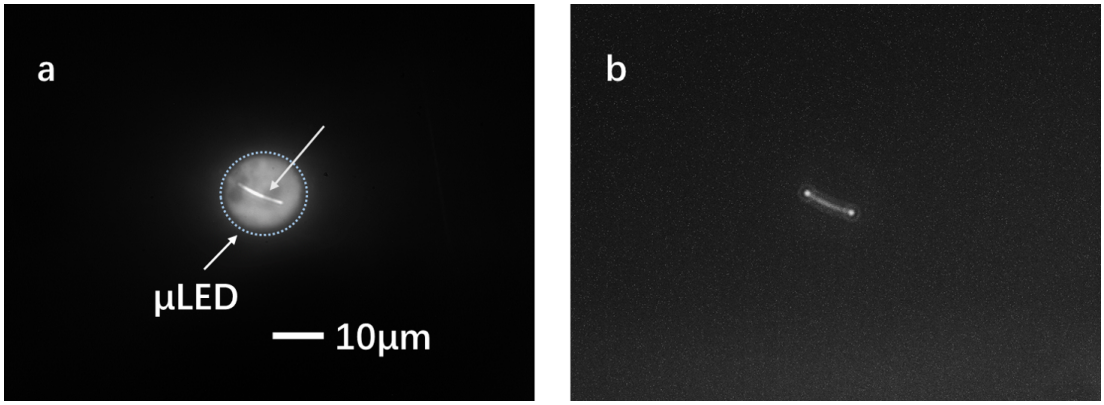

Figure 4.9: (a) Image showing a micro-LED projected onto single InP nanowire emitter device on quartz substrate. (b) Filtered image showing emission patters coming out of the nanowire's facets, excited with the projected microLED.

The measured emission wavelength of the optically excited nanowire device is shown in Figure 4.10, obtained using the spectral characterisation setup illustrated in Figure 4.8 (e). The spectrum exhibits features consistent with the expected spontaneous emission from the nanowire, with a peak wavelength of 860 nm. [52] [276]

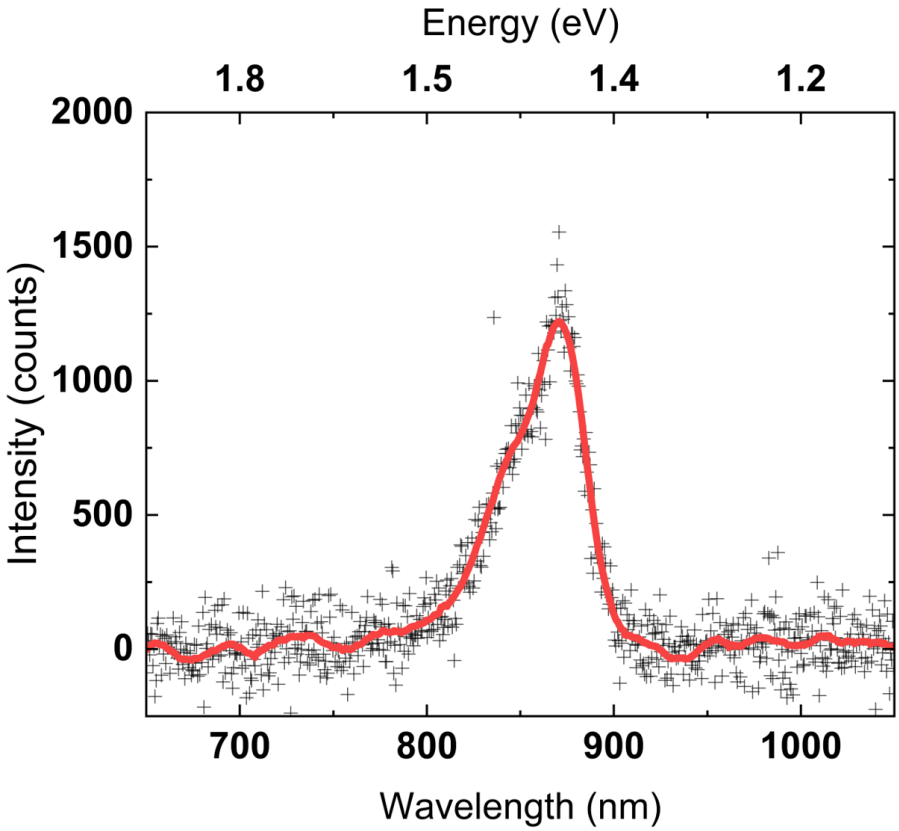

Figure 4.10: Measured spectrum of a printed single InP nanowire on a quartz receiver excited by projected micro-LED pixel.

From the emission and spectral data presented in Figures 4.9 and 4.10, it is evident that the excited nanowire does not exhibit lasing. To further investigate the emission characteristics, an additional measurement was performed to examine the relationship between the nanowire emission intensity and the projected optical power of a micro-LED pixel. In this experiment, the same brightest micro-LED pixel was selected and projected onto the nanowire via a series of neutral density (ND) filters. The pixel output power was measured at each level of optical density (OD). The corresponding nanowire emission intensity was quantified by integrating the signal from images captured by the CMOS camera under consistent exposure conditions. The resulting intensity-power relationship is plotted in Figure 4.11. In typical lasing devices, a distinct threshold point should be observed, marked by a sharp non-linear increase in emission once the pumping power surpasses a critical level. The absence of such a transition here confirms

that the nanowire does not reach the lasing condition under the tested excitation levels.

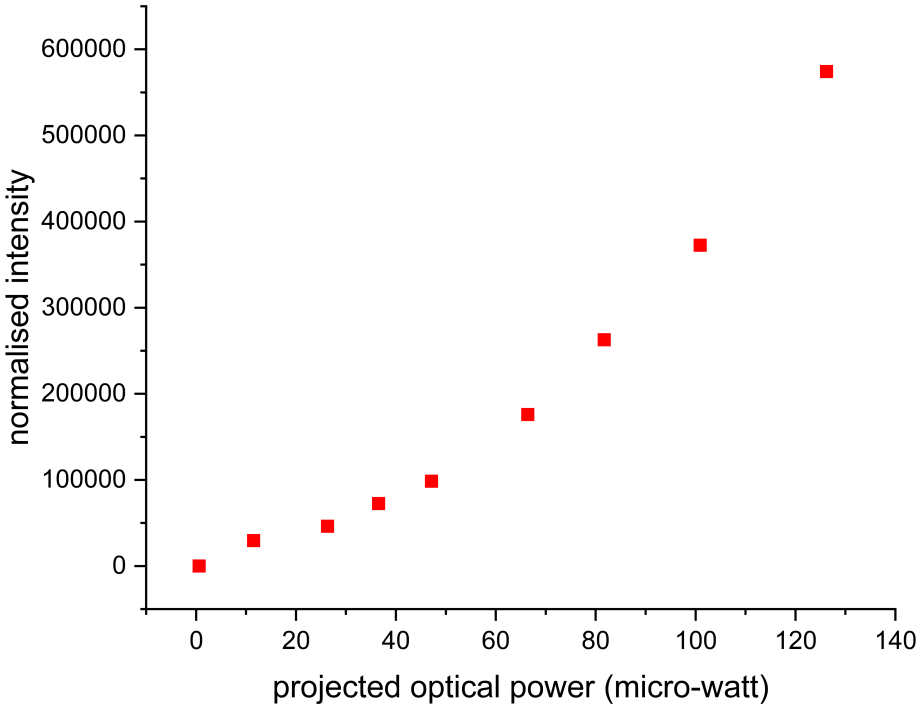

Figure 4.11: Relationship graph of projected power and intensity of nanowire emission.

Furthermore, an array of 3 × 3 InP nanowires devices was transfer-printed onto a glass slide substrate. Each of the nine printed nanowires could be individually excited by a corresponding pixel from the micro-LED array, as illustrated in Figure 4.12. For this multiple-excitation configuration, the projection lens pair was changed to 4× and 20× to provide a larger field of view. Figure 4.12(a) shows the schematic of the micro-LED-on-CMOS panel with nine activated pixels, while Figure 4.12(b) presents an unfiltered image of the 3×3 nanowire array under visible excitation light. The corresponding near-infrared (NIR) image, captured with an LP filter in place to isolate only the nanowire emission, is shown in Figure 4.12(c). As can be seen in Figure 4.12(b), the optical output intensity of the micro-LED pixels is not uniform, resulting in uneven excitation and varied emission intensities among the nanowires, as shown in Figure

4.12(c). Additionally, a pattern of 'X' was created by optically excited nanowires is shown as Figure 4.12 (d).

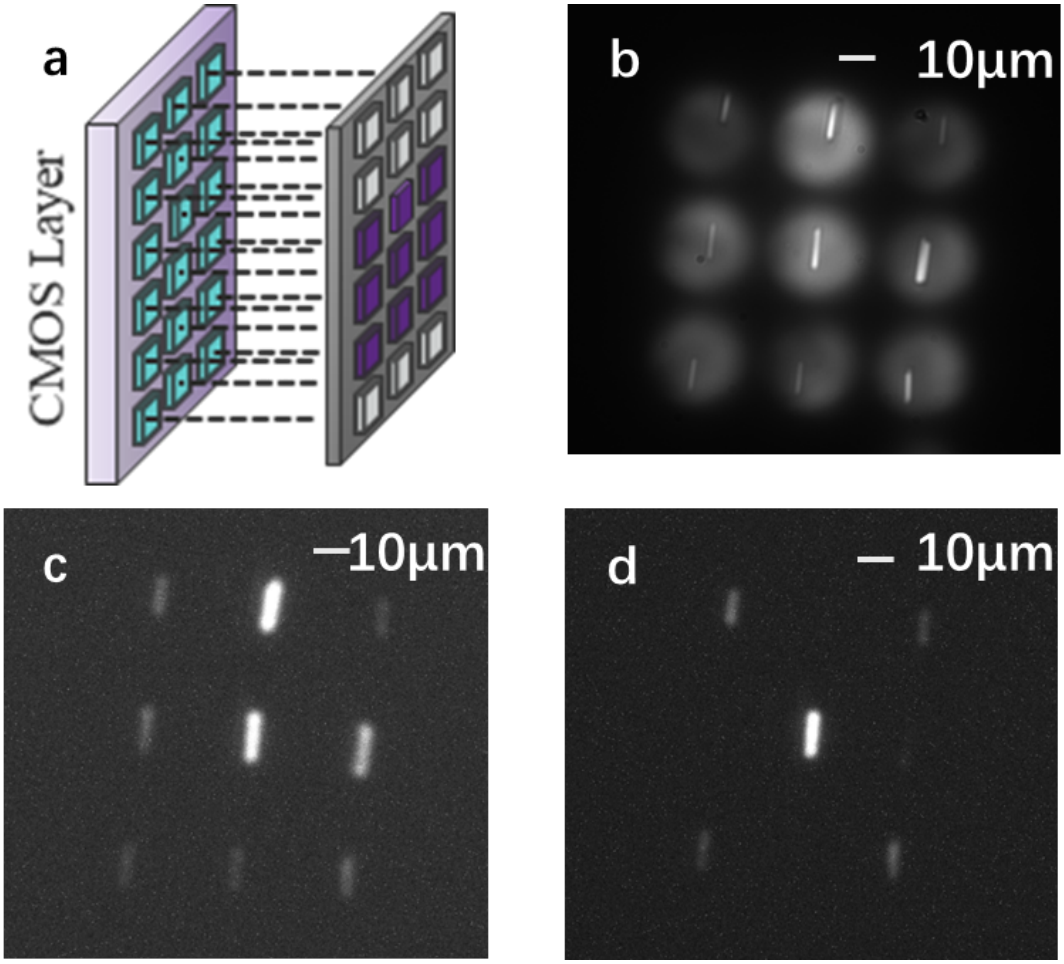

Figure 4.12: (a) Schematic of micro-LED pixels with CMOS control to optically excite printed NWs array. (b) Unfiltered image of 9 printed NWs and corresponding micro-LED pixels projection captured by top CMOS camera. (c) Filtered image of 9 excited NWs. (d) A pattern of 'X' created by optically excited NWs with 4 Micro-LED pixels off.

4.3.2 Optical Excitation of an InP Nanowire Embedded Inside a Polymer Waveguide

As the printed InP NW device is proved can be optically pumped, the next stage was to excite a NW device embedded inside a SU-8 waveguide and collect the coupled optical signal at the waveguide facet.

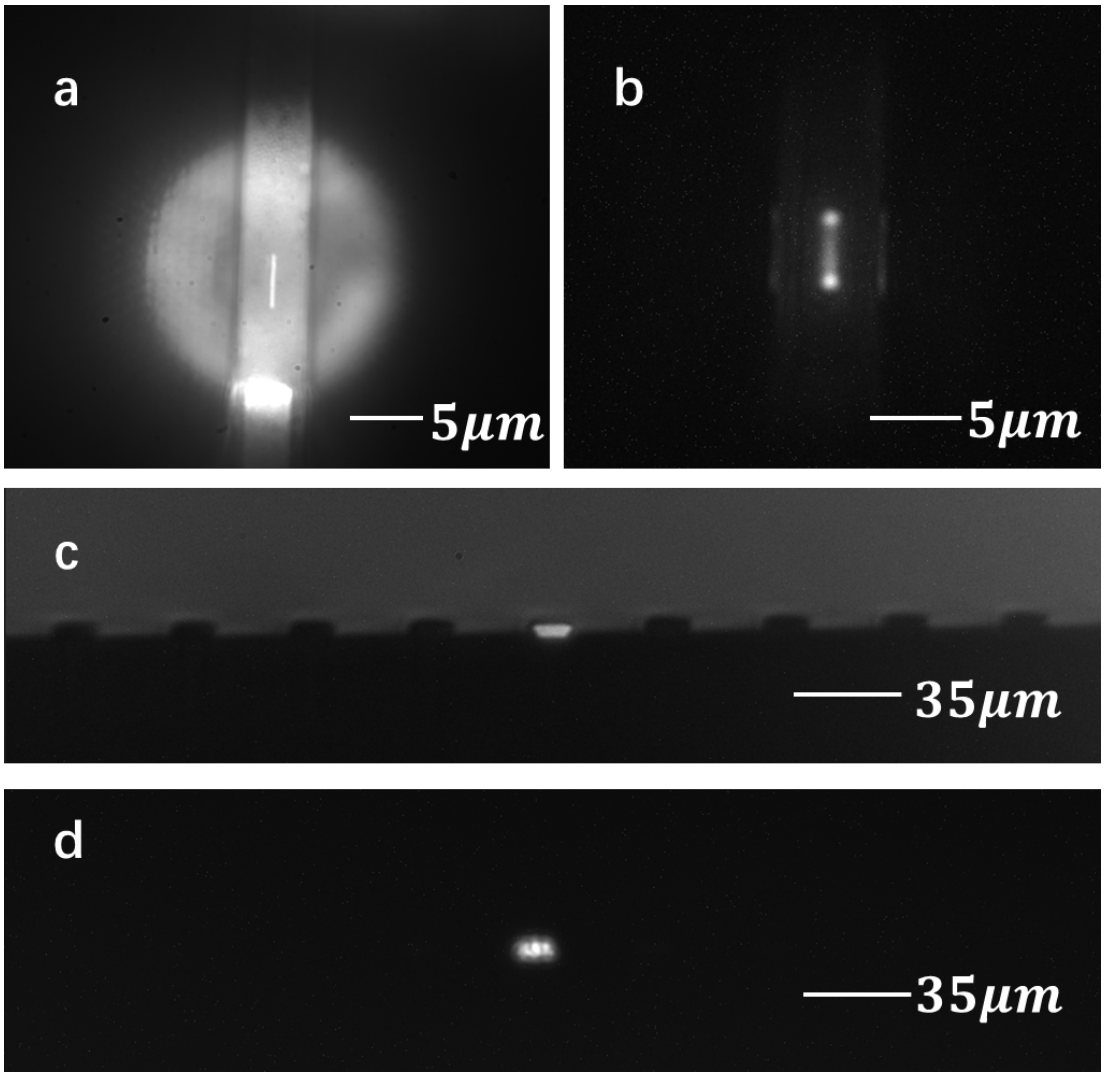

Figure 4.13: (a) Bright field image of a micro-LED pixel projected onto a nanowire device embedded within a polymer waveguide. (b) Filtered image showing the emission from the optically excited nanowire device. (c) CMOS camera image captured at the waveguide facet, showing the output region. (d) Filtered image of the waveguide facet highlighting emission from the nanowire in the near-infrared (NIR) range.

At this stage, the lens pair was changed back to 20× and 60× for optimised output power. The glass sample with 20 NWs embedded inside SU-8 waveguides was placed onto the 3-axis motion control stage, also, the same micro-LED pixel (brightest one of 280 $\mathrm{mW/mm^2}$) was chosen to be projected on the embedded NW as shown in Figure 4.13 (a), which is also captured by the top CMOS camera without LP filter. The top bandpass filter was in place for the observation of nanowire excitation. As shown in

Figure 4.13(b), airy disks are clearly visible at the nanowire facets, along with reflections from the sides of the SU-8 waveguides. This confirms that the embedded nanowires can still be optically excited and emit light via illumination from the projected micro-LED pixels through the polymer waveguides. All 20 devices were characterised in the same way and exhibited similar performance.

The edge detector module and the CMOS camera shown as Figure 4.8 (c) were used to collect coupled optical signal at the waveguides' facets. Figure 4.13 (c) shows the unfiltered image captured by the CMOS camera, and the bright spot is the optical signal coupled through waveguide. It is a mixed signal of visible emission from micro-LED pixel coupled into the waveguide and NIR emission from the excited NW. Additionally, a broadband light source was used to illuminate the facets in this image, so the edge of the sample with 9 waveguides' facets is also indicated clearly. The Figure 4.13 (d) clearly demonstrates the captured coupled optical signal emitted from the embedded NW device which is in NIR region (measured in the previous section) with the bandpass filter in place.

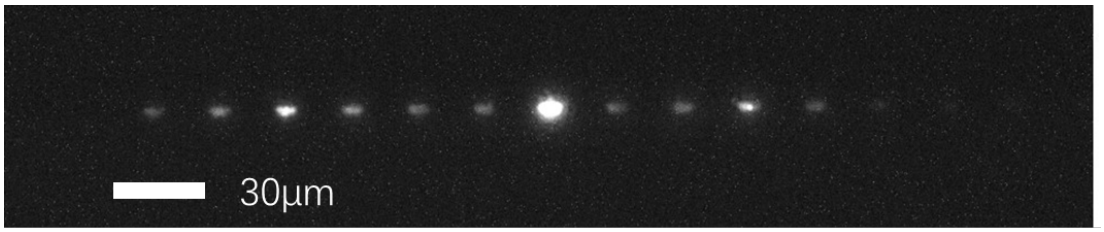

Figure 4.14: Filtered image at the edge of the sample with 12 NWs optically excited.

Excitation of multi-channel NWs was then attempted after single embedded NW excitation. A measurement was done by replacing the lens pair to 4× and 20× to increase the field of view and allow more pixels to be projected onto the sample. The pitch between the waveguides was designed to match the projected pixel pitch of the micro-LED array ($\sim 30\,\mu$m), taking into account the magnification provided by the selected lens pair. With 12 micro-LED pixels (maximised number for this field of view) turned on, each aligned to a nanowire device, the resulting image in Figure 4.14 displays 12 coupled near-infrared signals emitted at the waveguide facets. The variation in emission brightness is primarily because of the non-uniform optical output power of

the individual micro-LED pixels, which results in uneven excitation of the nanowires, and corresponding different intensities of emission.

4.3.3 Optical Modulation of A Single Channel of Nanowire Emitter System

The modulation of the micro-LED pixel was achieved by applying square wave signal from an external frequency generator (Liquid Instruments, Moku: Pro [283]) connected to the CMOS board and controlling the on-off keying of the micro-LED-on-CMOS system. The on-off keying of the micro-LED would also control the on-off status of the embedded nanowire devices. The SPAD camera mentioned before was used to capture the light output from the facet of a nanowire-waveguide coupled device. Frequencies ranging from 20 MHz to 150 MHz were selected due to the acquisition window of the SPAD camera, corresponding to 50 ns to 6.67 ns, respectively. Both the SPAD camera and the micro-LED-on-CMOS board were connected to the Moku:Pro for triggering the data collection to collect Time-Correlated Single Photon Counting (TCSPC) measurements. The triggering signal was set to one quarter of the modulation frequency (80 MHz to 150 MHz) to ensure that the TCSPC histogram covered the full modulation period. When the acquisition window exceeded the temporal range of the SPAD camera, the triggering signal was instead set to the same frequency (20 MHz or 25 MHz) as the modulation frequency, or to half of it (40 MHz), as shown in Table 4.1. TCSPC mode enables precise measurement of photon arrival times, allowing evaluation of the nanowire's temporal response to the micro-LED modulation and confirming whether the emission can follow high-frequency driving signals.

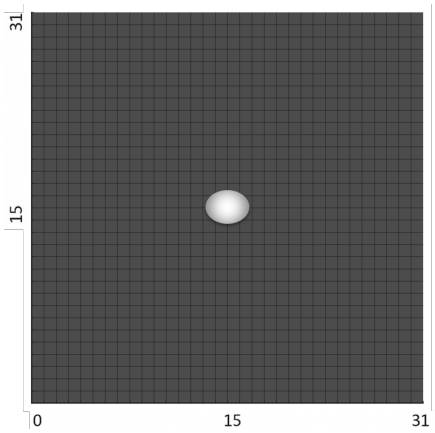

Figure 4.15: Schematic of the SPAD camera sensor user interface in photon count mode, the bright pixels in the middle are the schematic of emitting facet and the axis indicates the pixel number.

Table 4.1: A list of modulation frequencies and corresponding synchronised frequency to trigger the SPAD camera.

Modulation Frequency (MHz)	**Triggering Signal** (MHz)
20	20
25	25
40	20
80	20
100	25
150	37.5

During the measurement process, the SPAD camera was initially operated in photon count mode for alignment. In this mode, the emitting facet of the device was aligned with the sensor's active region and centred on a designated pixel within the array, the schematic of the SPAD camera graphical interface is shown as Figure 4.15. Once alignment was confirmed, the corresponding pixel address was recorded, and the camera was then switched to TCSPC mode to acquire time-resolved emission data for all 20 devices. Figure 4.16 shows a captured optical signal from all 20 nanowire-in-waveguide channels optically modulated at 25MHz. These 20 devices share comparable optical performance and photon counts, and hence coupled optical power in the waveguides. This diagram indicates that the repeatability of the transfer-printing and integration processes was successfully achieved. This result highlights the potential of this hybrid integration

technique for the scalable fabrication of large-scale photonic integrated circuits (PICs).

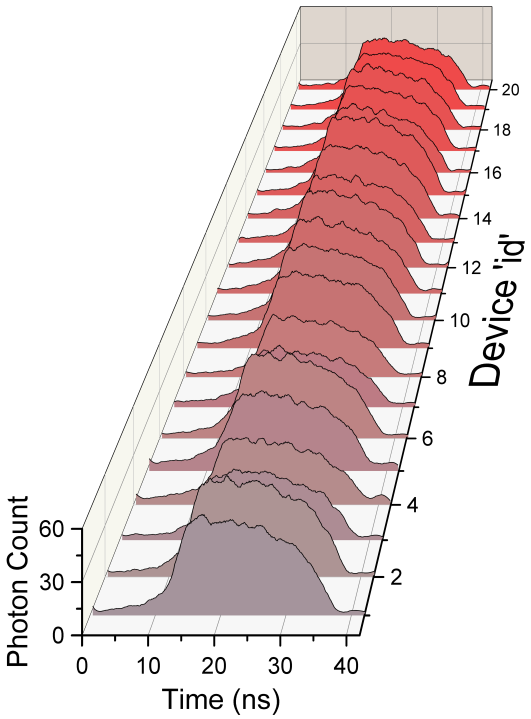

Figure 4.16: Diagram showing time-domain measurements at a modulation frequency of 25 MHz for 20 nanowire emitters integrated into waveguides with the same Micro-LED pixel.

The captured optical signals from NWs at the waveguide facets at different modulation frequencies were then recorded, the data of the corresponding sensor pixel was then signal processed by using Savitzky-Golay digital filter with a third order polynomial and a window size of 53 to reduce high frequency noise. As shown in Figure 4.17 (a), the measured modulation from the waveguide facet for a representative device (nanowire 16) at various frequencies (20, 40, 80, 100 and 150MHz), demonstrating on-off keying (OOK) operation beyond the 3dB cutoff frequency (120MHz [182]) of the micro-LED devices. The measured cut-off frequencies, as shown in Figure 4.17 (b), for both the micro-LED-on-CMOS board and the embedded nanowire-in-waveguide devices (mean values) indicate that the nanowire response closely follows the temporal envelope of the micro-LED emission. This confirms that the modulation speed limitation arises primarily from the micro-LED source, as expected. [276] The modulation

index was defined as $10\log_{10}\left(\frac{P_{\max}-P_{\min}}{P_{\max}+P_{\min}}\right)$, where $P_{\max}$ and $P_{\min}$ are maximum and minimum intensity values, respectively. [275] In this diagram, the nanowire devices exhibit a slightly higher modulation index compared to the micro-LEDs, likely due to their operation under amplified spontaneous emission. This gain mechanism, which scales with optical pump power, enhances the signal-to-noise ratio and contributes to improved modulation performance. [276]

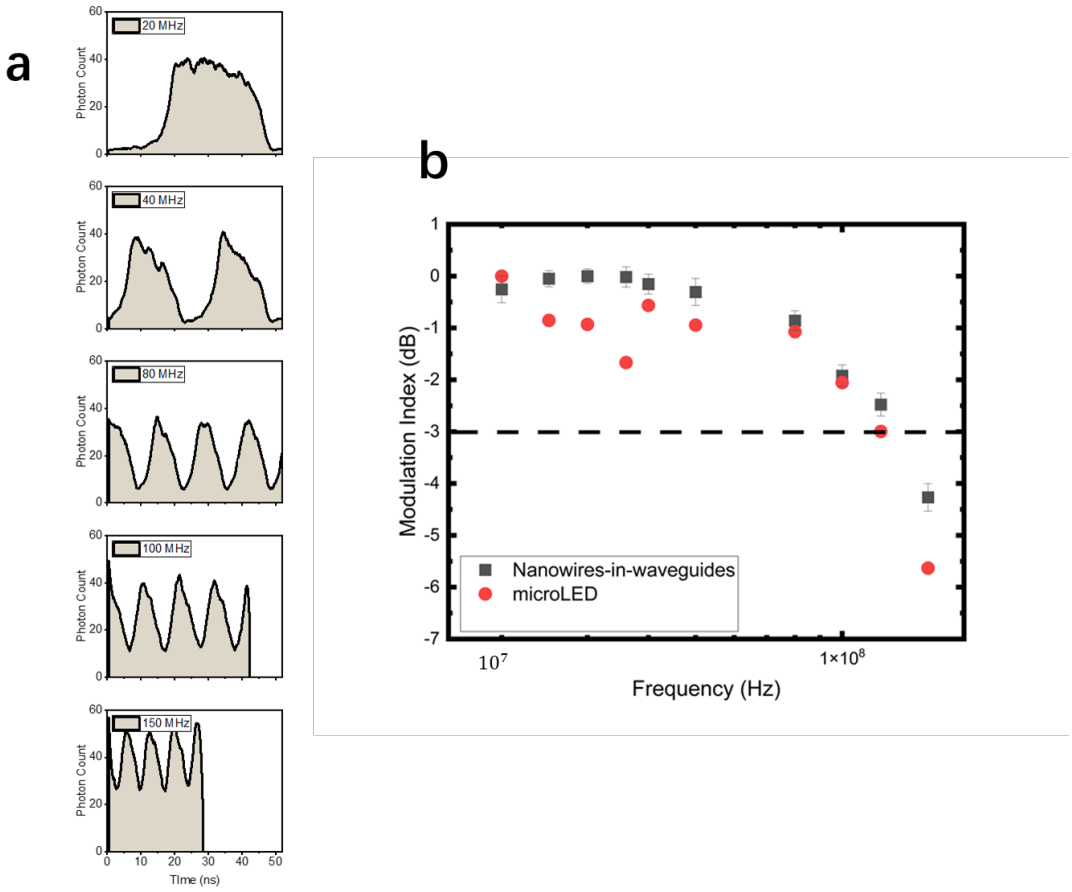

Figure 4.17: (a) Time-domain measurements of Device 16 at modulation frequencies of 20, 40, 80, 100 and 150MHz. (b) Cutoff frequency plot showing the modulation index for both the nanowire-in-waveguide emitters (mean value of 20 devices) and a representative micro-LED pixel.

Furthermore, we projected a micro-LED pixel onto a blank SU-8 waveguide and there was some luminescence captured by the edge detector CMOS camera with the 700 nm LP filter but this significantly reduced using an 800 nm LP filter. It could be

emission from SU-8 waveguides which was also mentioned in reference [284]. However, it was characterized to be ~ 28 times lower than the coupled emission from integrated nanowire under the same optical pump conditions and using the 800 nm LP filter. The images of the waveguides facets with and without nanowire embedded inside are shown as Figure 4.18 (a) and (b), respectively, both images were captured by the CMOS camera in edge detector with 800 nm LP filter on under the same exposure parameters. This means that the filtered optical signal collected at the facets are mainly from embedded nanowires and the influence caused by SU-8 emission is negligible.

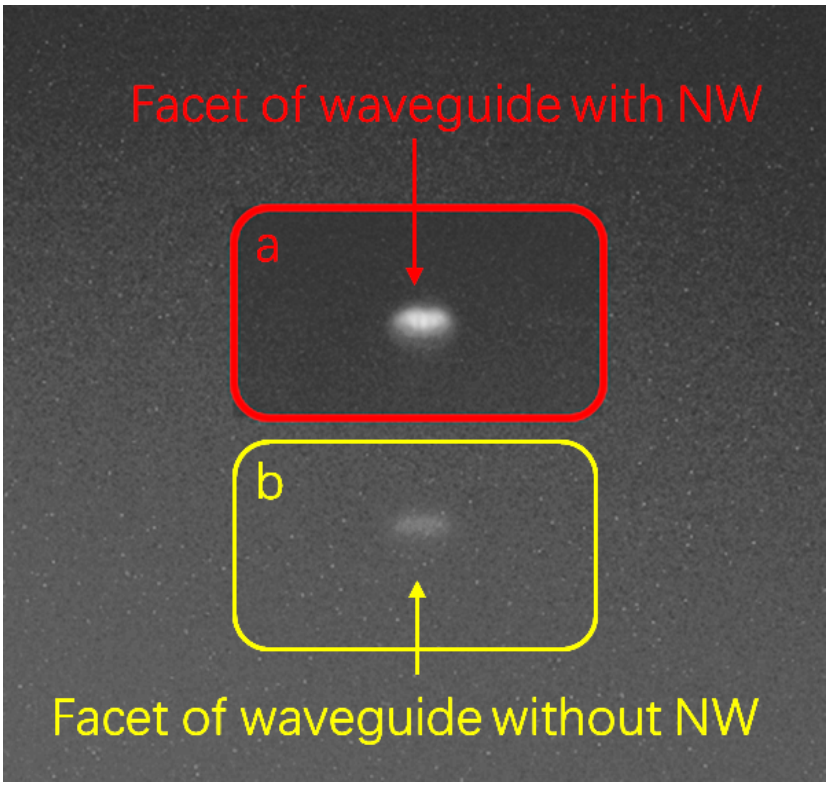

Figure 4.18: (a) Image of waveguide facet (NW embedded) with 800 nm in place. (b) Image of blank waveguide facet with 800 nm in place.

4.3.4 Optical Modulation of Multi-Channels of Nanowire-in-waveguide

As steady state multi-channel excitation was shown previously, the next stage was to demonstrate the ability of multi-channel modulation of waveguide-integrated nanowires emitters in parallel. Considering the trade off between field of view and the output

power of the projection, the 20× and 60× lenses pair was used and a maximum of 3-channel for demonstration without a significant power reduction, compared with the single emitter case.

In this project, three micro-LED pixels in one row were projected onto three embedded nanowires. Three output channels of the Moku: Pro were used to provide different frequencies, f_1, f_2, f_3, to each micro-LED pixel, respectively. The schematic of multi-channel projection is shown as Figure 4.19.

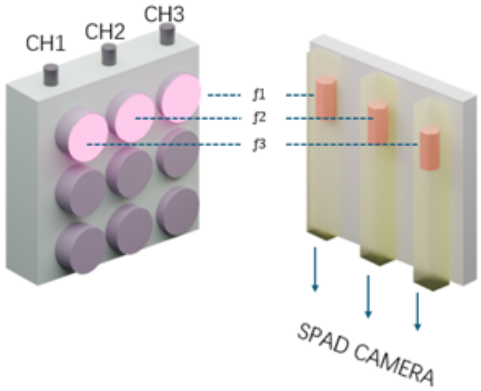

Figure 4.19: A schematic showing three independently modulated pixels projected onto three embedded into waveguide nanowire emitters at various frequencies.

The operation on SPAD camera was similar to single emitter case, but three addresses of pixels were recorded and analysed. Each micro-LED pixel was independently modulated at 20, 40, 80MHz in different configurations. The image of three facets with nanowire embedded, excited and modulated is shown as Figure 4.20 (a), 20, 40, 80MHz modulation frequencies were given to channel 1, 2, and 3, respectively. Figure 4.20 (b) demonstrates the independent frequency modulation of three different nanowire-in-waveguide channels. The comparable signal levels observed from each waveguide confirm uniform device response, and the nanowire emitters clearly follow the modulated on–off keying of the corresponding micro-LED drivers.

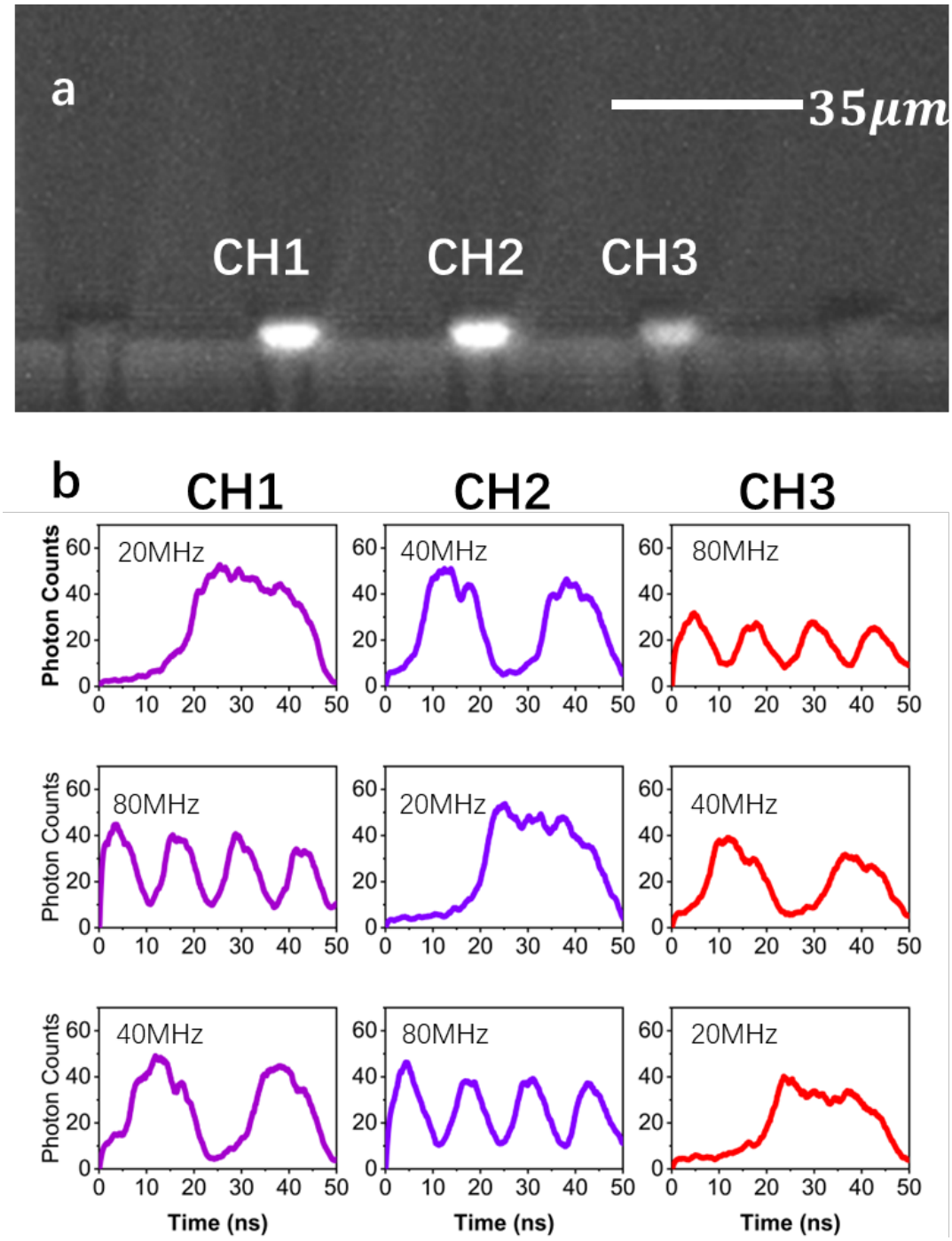

Figure 4.20: (a) Side view of the 3-channel of facets of the waveguide sample showing output NIR emission from the three excited nanowires inside waveguides. (b) Time-domain on–off keying modulation measurements collected simultaneously from three nanowires embedded in separate waveguides, operated at modulation frequencies of 20, 40, 80MHz. Each horizontal panel represents a distinct modulation frequency configuration.

This three-channel modulation shows that each nanowire emitter can be independently excited, modulated and coupled into corresponding polymer waveguide without noticeable crosstalk, indicating effective spatial and optical isolation. Based on this research, large arrays of high speed and high density optoelectronic systems with functionalities like Frequency Division Multiplexing (FDM) [285] can be developed in the future. It is important for the development of scalable photonic integrated circuits.

4.4 Summary

This chapter focuses on the integration and modulation of Nanowires emitters and polymer waveguides through Micro-LED-on-CMOS technology. In the very first section, the background information about the semiconductor Nanowires used in this project is introduced and a short literature review of our group's previous achievement on Nanowires research is given. Also, the challenges in current optical pumping methods on nano-emitters are indicated. Hence, a compact way of integration nano-emitters with passive PICs components and a brand-new method of optical pumping should be researched to increase the scalability of PICs.

In the second section, the fabrication process and integration of NWs and polymer waveguides are discussed in detail. 20 NWs' alignment, transfer-printing and embedding into polymer-waveguides are shown. The Micro-LED-on-CMOS technology is introduced and the information about the Micro-LED devices used for optical projection is indicated. The set-up built for the projection of micro-LED pixel is introduced in detail as well.

The third section starts with single and multiple excitations of printed NWs on a quartz disk with projected micro-LED pixels. The measured spectrum of NW is also shown. The diagrams of top and edge coupled light in this section show the success of excitation on nanowires embedded in polymer waveguides. All 20 embedded devices can be modulated by the micro-LED in the 10s of MHz range, limited in this case by the current CMOS driver chip, the captured TCSPC data through SPAD camera shows not only the successful modulation but also the coupling to waveguides. Finally, the capability of multiple-channels (3-channels) excitation with different frequencies 20, 40

and 80MHz, are demonstrated.

In summary, a chip integrated with 20 transfer-printed NWs and polymer waveguides in a compact pitch ($\sim 30\,\mu$m) is successfully optical excited and modulated up to 10^8Hz level by a micro-LED-on-CMOS system for the first time.

In future work, the emission characteristics and propagation loss of SU-8 waveguides will be investigated. Additionally, transfer-printing techniques will be explored to directly integrate micro-LED pixels with nanowire emitters on-chip, enhancing scalability while eliminating optical losses associated with external projection systems.

Chapter 5

On-chip Design, Integration, Excitation and Modulation of Semiconductor Nanowires with Transfer-printed GaN Micro-LED Pixels

In this chapter, an introduction to Micro-LED technology and its applications in transfer-printing and data communications is given at first. The motivation and aims of integrating Micro-LED pixels and Nanowires-in-waveguides are also discussed in this chapter. The characterisation process of the Gallium Nitride (GaN) based devices is detailed. Secondly, the integration process of Micro-LED pixels and the Nanowires-in-waveguides chip, including the structure design and optimisation, are listed and demonstrated. The small signal modulation results is shown in this chapter as well.

5.1 Introduction

The research and development history of LEDs, especially in the visible wavelength range, is tied closely with the exploration of various compound semiconductor materials. [286] Research on optoelectronic devices based on III–V compound semiconductors has garnered significant worldwide attention since the early 1990s with the successful demonstration of the first blue InGaN LED on sapphire substrates. [287] [288] This achievement promoted research and creations of white LEDs (phosphor conversion) [289] and applications for full-colour LED displays [290] and solid-state lighting. [291] [292] These semiconductor-based LEDs address the key performance requirements for advanced information displays, including high brightness, fast response time (high frame refresh rate), wide colour range and high resolution.

With the increasing demands of information systems, the development of material science and epitaxial growth innovations [293], the research on micro-LED technology has been enabled and is still developing as micro-LEDs have emerging applications beyond illumination, such as high-resolution displays [294], visible light communications (VLC) [295], and optogenetics [296] [297]. Large-scale manufacturers, such as Samsung and Sony have launched their large-area video walls based on micro-LED pixels, 'The Wall' [298] and 'Crystal LED' [299], respectively. These applications benefit from the unique advantages provided by micro-LEDs: high modulation bandwidth [300], the ability of direct integration with CMOS electronics [97], high brightness and power density [301] and very fast response time [302].

The epitaxial growth of GaN on silicon or sapphire substrates has emerged as a promising route for the cost-effective fabrication of GaN-based LEDs. However, the significant lattice and thermal-expansion mismatches between GaN and these substrates can lead to issues such as high defect densities and wafer cracking. [303] In addition, for micro-LED devices operating in the visible spectrum, the emitted light can be strongly absorbed by certain substrate materials (silicon, for example), while sapphire substrates, although transparent, are typically too thick and not suitable for compact or high-performance device integration. Consequently, transfer-printing techniques are

often employed to detach the devices from their growth substrates and place them onto application-specific receiver substrates.

For example, in the fabrication of full-colour displays [304], the application of transfer printing allows for the separate fabrication of red, green, and blue micro-LEDs on their respective native substrates, which are then assembled onto a common target substrate using the transfer-printing technique. Further, the transfer-printing techniques can also be developed into advanced techniques such as mass transfer [93] and roller print [305] to allow for manufacturing scale integration. The transfer-printing of micro-LEDs pixels can also shrink the chip size in VLC applications as a suspended designed micro-LED pixel for transfer-printing is much thinner compared to a GaN-on-Sapphire μLED for VLC. [279]

Research shown in reference [97] [279] and [306] all show that micro-LED arrays have high potential in increase the scalability of the photonics integrated circuits for visible light communications and data transmission purposes as they demonstrate high modulation bandwidth and the capability of integration with different substrates such as CMOS circuits, sapphire and glass substrates.

5.2 Motivations and Aims

The research shown in Chapter 4 and related publication in reference [276] demonstrate the excitation and modulation of the infrared emitters (semiconductor nanowires) embedded in polymer waveguides using individually addressable micro-LED-on-CMOS arrays. The micro-LED arrays used were fabricated from commercially available wafers grown on sapphire substrates and flip-chip bonded onto CMOS circuits to provide individually-addressed functions on each pixel, and the continuous output intensity of single pixel was up to $\sim 0.55\,\mu\mathrm{W}/\mu\mathrm{m}^2$. [179] However, the semiconductor nanowires were excited and modulated by projected micro-LED-on-CMOS pixel through free space optics, and the output power projected on a single embedded nanowire through set-up shown in reference [276] was $\sim 0.28\,\mu\mathrm{W}/\mu\mathrm{m}^2$, which means nearly half of the output optical power had not been delivered onto the embedded nanowire. Apart from the waste of power, the whole set-up applied to optical pump the chip of embedded nanowires in

polymer waveguides is much larger than the chip itself and this went against the concept of increasing the integration level and scalability of photonic integrated circuits.

With the development of suspended micro-LED pixel's structure [279], there is a chance to integrate the suspended ultra-thin micro-LED platelet with pre-fabricated photonics integrated circuits (embedded-nanowires-in-polymer-waveguides structures) using transfer-printing technique. [307]

Therefore, in this project, an optimised waveguide's structure can be designed to fit the dimension of a single micro-LED pixel. The same fabrication procedures can be applied to embedded nano-emitters into polymer waveguides as detailed in Chapter 4. High-accuracy transfer-printing technology would then be applied to pick the pre-fabricated suspended thin micro-LED membranes and integrate them with the waveguide chip, and finally, on-chip probing and excitation of both printed micro-LED pixels and nano-emitters can be conducted. The success of on-chip excitation and modulation (on-off keying or small signal modulation) of the embedded nano-emitter is a milestone for increasing scalability of photonics integrated circuits for data communications applications. The optical signal should couple through the polymer waveguide and be collected from the waveguide facets.

5.3 Transfer-printing of Suspended Micro-LED pixels onto a PDMS Substrate for Characterisations

5.3.1 Introduction of the Pre-fabricated AlInGaN Micro-Light-Emitting-Diodes

The ultra-thin AlInGaN micro-LEDs pixels were fabricated from a commercial GaN-on-silicon LED epistructure, and the suspended format was formed by using potassium hydroxide (KOH) to under etch the silicon substrate. The detailed fabrication procedures including photolithography, metal contact definition and so on can be found in references [97], [279], [307] and [59]. Figure 5.1(a) demonstrates the suspended micro-LED pixels array on the fabrication substrates, the pixel is $100\,\mu$m $\times$ $100\,\mu$m in dimension and it is suspended by anchors in width of $10\,\mu$m. This design would

make the pixel easily picked up by an elastomeric stamp (PDMS stamp, as previously introduced) from the fabrication substrate. [36]

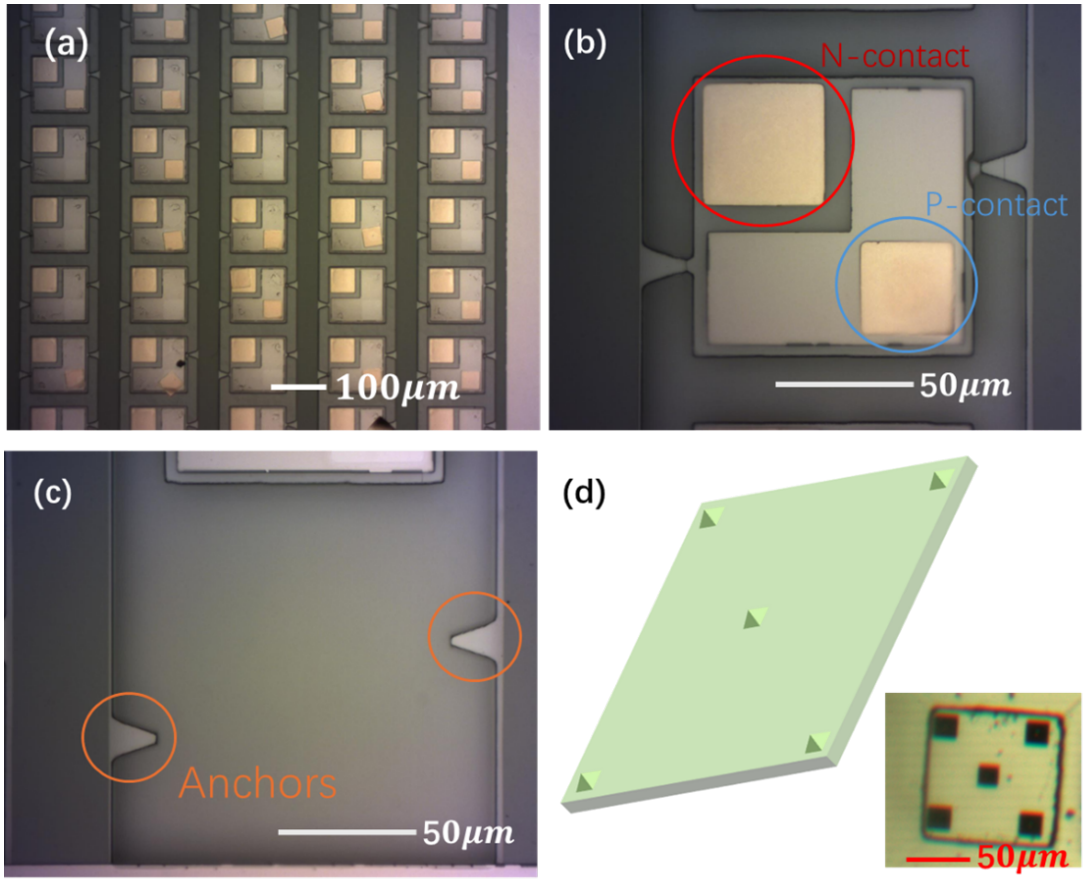

Figure 5.1: (a) Microscope image of the suspended ultra-thin AlInGaN blue micro-LED pixels array on the fabrication substrate. (b) Microscope image of one single suspended micro-LED pixel. (c) Microscope image of both anchors and left void after membranes being picked up. (d) Schematic and Camera captured image of the elastomeric PDMS structure.

5.3.2 Transfer-printing, Probing and Characterisation of a Single Micro-LED Pixel

The first step of this project is to pick-up, print and characterise the fabricated pixel. An elastomeric PDMS stamp ($100\,\mu m \times 100\,\mu m$) with pyramid tips, shown as Figure 5.1 (d), was fixed on the advanced transfer-printing system to break the anchors and pick up a single micro-LED pixel from the fabrication substrate. Figure 5.1 (b) is a

microscope captured image of a single pixel suspended by the anchors on its original substrate, both N and P contacts are indicated for probing. As PDMS is optically transparent in visible spectrum [308], another PDMS stamp without any structure on was applied here as a receiver substrate for further measurement of optical power, I-V performance and modulation. During the transfer-printing process, the 5 pyramid tips contacted with the LED surface and a slight 'press' (movement on vertical axis) was applied to break anchors and pick the thin pixel up. The emitting area of the pixel is the P-region, therefore, the pixel was aligned and printed at the edge of the receiver PDMS substrate with P-region outward facing as shown in Figure 5.2 (a). An array of 6 pixels was printed and the microscope image is demonstrated in Figure 5.2 (b). Figure 5.1 (c) is the left void area and anchors on the original substrate. Printing at the edge of the substrate provided direct access to edge emitted light for measurement of the modulated pixel using the SPAD camera in the edge detector set-up introduced in Figure 4.8 (c), Chapter 4.

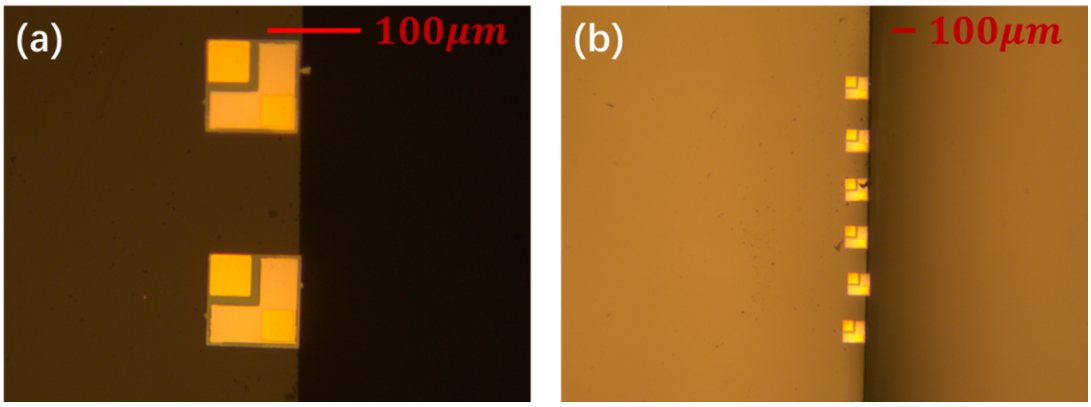

Figure 5.2: Microscope images of (a) Two printed micro-LED pixels on PDMS substrate edge. (b) An array of 6 printed pixels on the PDMS receiver.

A probe stage and a Thorlabs optical power meter [309] were applied to characterise both electrical and optical performance of a printed micro-LED pixel, as shown in Figure 5.3 (a). A DC voltage was applied on the probing tips and increased step by step (automatically controlled by software) to excite the printed pixel, and the I-V performance for the printed micro-LED is shown as Figure 5.3 (b).

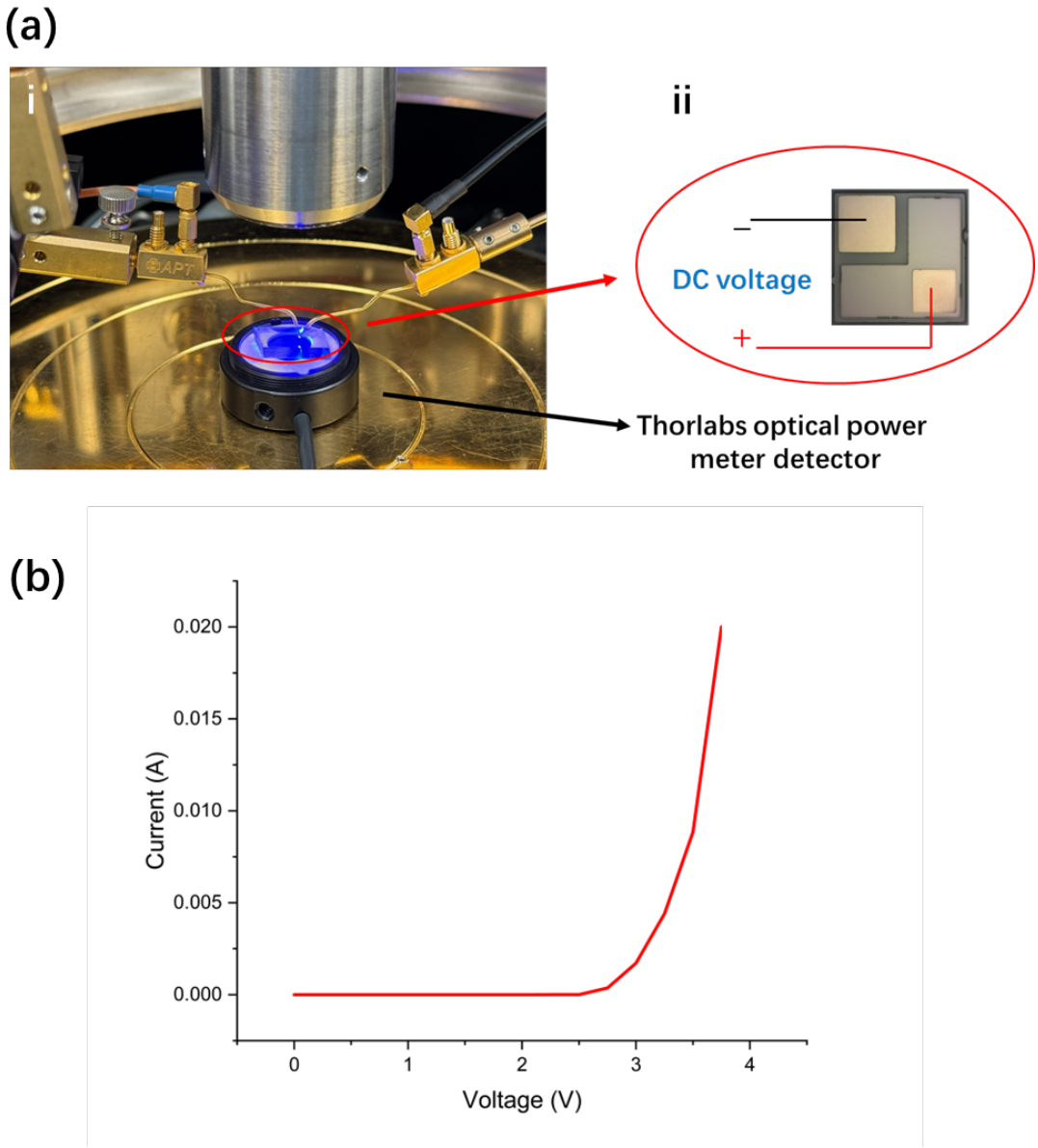

Figure 5.3: (a) Diagram of (i) an emitting printed pixel-on-PDMS on the Thorlabs power meter detector fixed on the probing stage, (ii) a schematic of the equivalent electronic probing. (b) Measured I-V curve of the printed micro-LED pixel.

The PDMS substrate is optically transparent therefore the detector underneath can measure the optical output power at different currents for 450 nm emission wavelength (pre-measured before the transfer-printing). In the further integration of micro-LED pixels and NW-in-waveguides, the micro-LED would be printed on the top of the sample

and the output optical power measured by this method precisely demonstrates the max power density can be delivered on the chip. The relationship between the output optical power and the current is show as Figure 5.4 and the maximum output power is $\sim 470\,\mu$W. The emitting area of the micro-LED pixel is $5200\,\mu\text{m}^2$, therefore, the power density of the printed micro-LED is $\sim 0.09\,\mu\text{W}/\mu\text{m}^2$, which is only $\sim 1/3$ of the output optical power of the projection method in Chapter 4. Since the micro-LED membrane is vertically emitting, this top-integration method suffers from significant optical power loss. As the projection method was already limited to exciting NWs only in the spontaneous emission regime, the even lower power density of the micro-LED membranes approach makes it impossible to reach the lasing threshold. Additionally, there is a roll-off in optical power as highlighted in Figure 5.4 and this was mainly effected by thermal issues, as the pixel membrane was directly integrated on PDMS and it is not a good heat sink compared to substrate like sapphire.

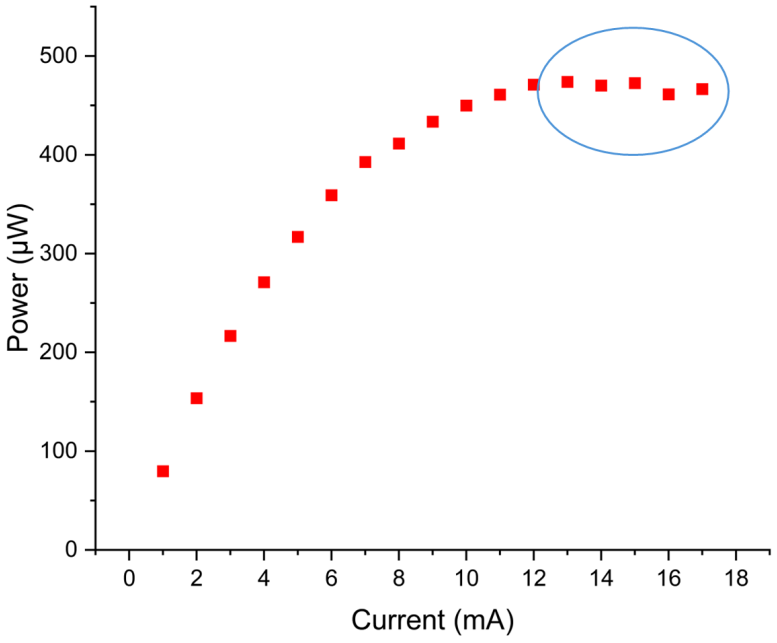

Figure 5.4: The relationship between injecting current and output optical power of the printed micro-LED.

5.4 Modulation of the Printed Blue Micro-LED

The simplest form of modulation on the printed micro-LED is on-off keying modulation as previously carried out and described in Chapter 4. However, different from using micro-LED-on-CMOS, the 'Moku:pro' was used here not only for frequency generation but also applied as power supply. Based on the information provided [283], the device's response was reduced at 30 MHz when the peak-to-peak voltage (V_{pp}) exceeded 1 V. However, this limited voltage was insufficient to effectively drive the printed micro-LED. Therefore,full scale on-off keying modulation on the printed micro-LED is not an ideal modulation method for this project.

5.4.1 Device and Theory of Small Signal Modulation

To modulate the printed micro-LED and excite the nano-emitter in the future, small signal modulation was used. A DC power supply, a bias tee [310] and the 'Moku:pro' were applied here and connected to the probing tips to provide small signal modulations, the schematic of the wire connection is shown as Figure 5.5 (a). A typical bias tee [310] has three ports, two inputs for DC voltage and frequency signals and an output for the combined output signal. For the printed micro-LED, if a 2.5 V DC bias is supplied by the power source and a 1 V ($\mathrm{V_{pp}}$) square wave frequency signal (ranging from 0 V to 1 V) is provided by the signal generator, the output signal from the bias tee varies between 2.5 V and 3.5 V at the same frequency as the input modulation signal. This output signal can be used to perform small-signal modulation of the micro-LED. According to the I-V characteristics, the voltage applied to the printed pixel falls within the highlighted operating range shown in Figure 5.5 (b).

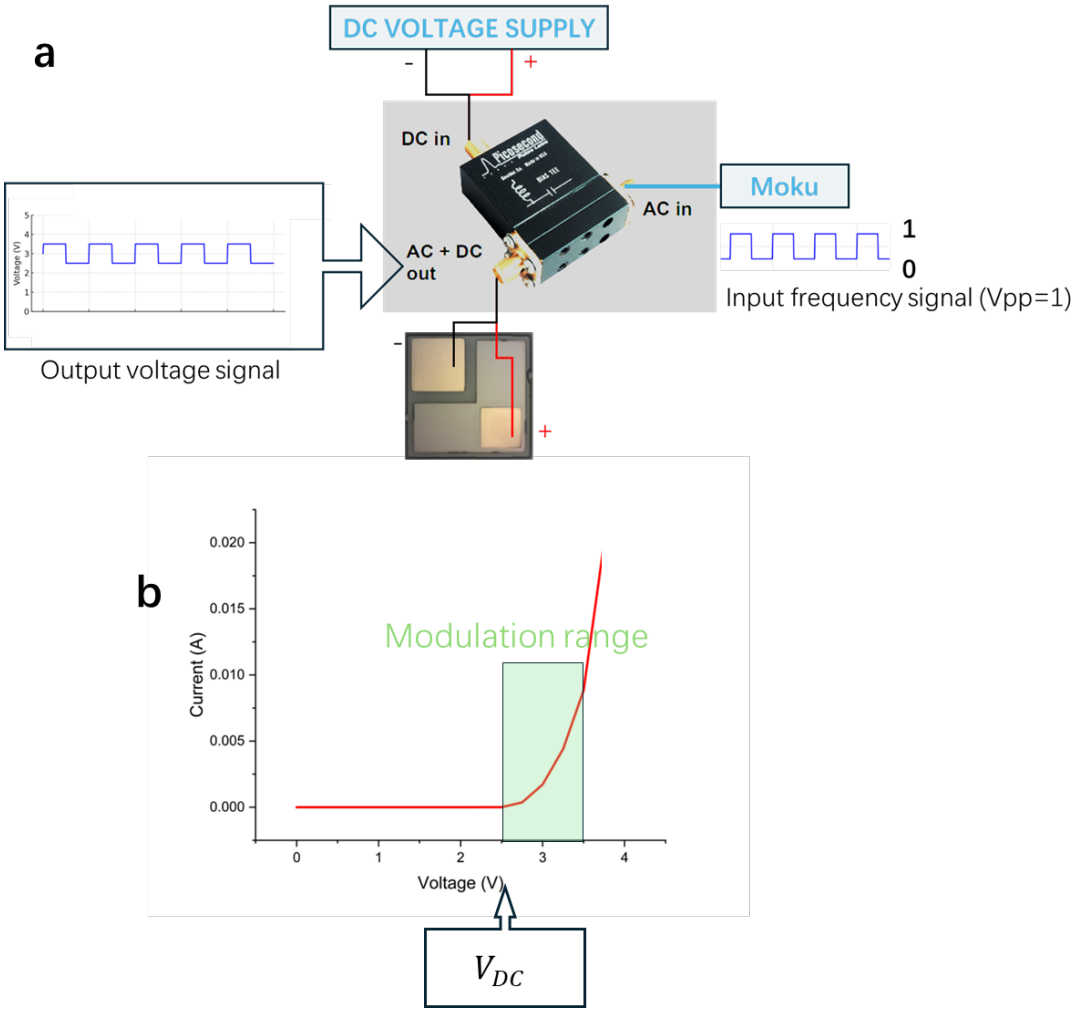

Figure 5.5: (a) Schematic of the wiring configuration for the DC voltage input, frequency input from the Moku:Pro, and small-signal output probing on the printed micro-LED using a bias tee. (b) Modulation range shown on the micro-LED I-V curve.

5.4.2 Set-up for Micro-LED Excitation and Manipulation

The Micro-LED Set-up introduced previously in Chapter 4 for the modulation of embedded-NW-in-polymer waveguides was optimised slightly and used again here. However, the micro-LED-on-CMOS system was applied here with the CMOS camera on the top only for the illumination during the process of probing and it would be turned off during the measurement. Two probing stages were added to deliver the 'small signal modulation' signal from the bias tee's output onto the printed pixel by

making direct contact between the probing tips and metal contacts. The same Single Photon Avalanche Diode (SPAD) camera was used to work in time-correlated single photon counting (TCSPC) mode to measure the signal captured at the edge of the sample. Both modulation frequency signal and trigger signal provided to SPAD camera were generated by the 'Moku:pro'. The LP filter would only be applied while the sample with NWs is mounted for measurement to block the emission in visible spectrum range. Figure 5.6 (a) presents the full schematic of the optimised setup, including the devices used for direct on-chip excitation and small-signal modulation, and Figure 5.6 (b) shows an image of the excited printed micro-LED on a PDMS substrate mounted on the setup.

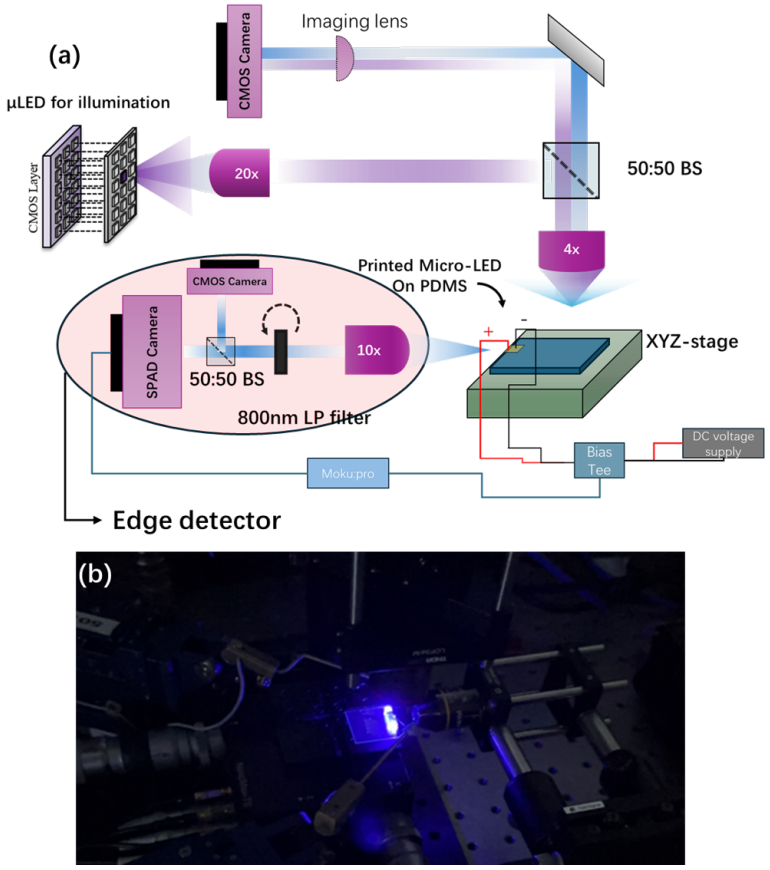

Figure 5.6: (a) Schematic of the Set-up used for illumination, excitation and manipulation both samples with printed micro-LED and further fabricated devices. (b) An image of an excited pixel on the PDMS substrate which is integrated to a piece of glass slide and fixed on a three-dimensions stage.

5.4.3 Results of Modulation and Performance Analysis

The SPAD camera was aligned with the 10× lens to capture the scattered light from the edge of the sample where the micro-LED pixels were printed and probed on the PDMS substrate mounted on the stage. Modulation signal frequencies were selected in the 'Moku:pro' ranging from 20 MHz to 150 MHz (corresponding to 50 ns and 6.67 ns, respectively) based on the acquisition window of the SPAD camera (55 ps to 57 ns). [282] [276] Table 5.1 is the table of both generated modulation signal delivered on micro-LED and the synchronized signal to trigger the data collection. The triggering signal was set to one quarter of the modulation frequency (80 MHz to 150 MHz) to ensure that the TCSPC histogram covered the full modulation period. When the acquisition window exceeded the temporal range of the SPAD camera, the triggering signal was instead set to the same frequency (20 MHz) as, or to half of (40 MHz and 60 MHz), the modulation frequency. During this modulation process, the DC voltage was set at 3.5 V and the voltage of the frequency signal was set to vary from 0 to 1 V to enable high frequency bandwidth in Moku:pro. Therefore, the voltage applied on micro-LED pixel was varying from 3.5 to 4.5 V during the modulation.

Table 5.1: A list of modulation frequencies and corresponding synchronised frequency to trigger the SPAD camera.

Modulation Frequency (MHz)	**Triggering Signal** (MHz)
20	20
40	20
60	30
80	20
100	25
120	30
130	32.5
150	37.5

The collected TCSPC data by the SPAD camera was firstly processed by using a Savitzky-Golay digital filter with a first order of polynomial and a windows size of 53 samples to reduce high frequency noise. Figure 5.7 (a) demonstrated the captured optical modulation signals in different frequencies (20, 40, 60, 80, 100, 120, 130 and 150 MHz). The peak-to-peak photon counts value decreases after approximately

60 MHz. A possible explanation is that the optical output intensity of the micro-LED (shown as photon counts) decreased significantly while the input modulation signal increased to 60 MHz. Therefore, it is important to study the cut-off frequency (−3 dB) of these printed micro-LED devices as they could be unable to excite the nano-emitters at these modulation frequencies in further applications.

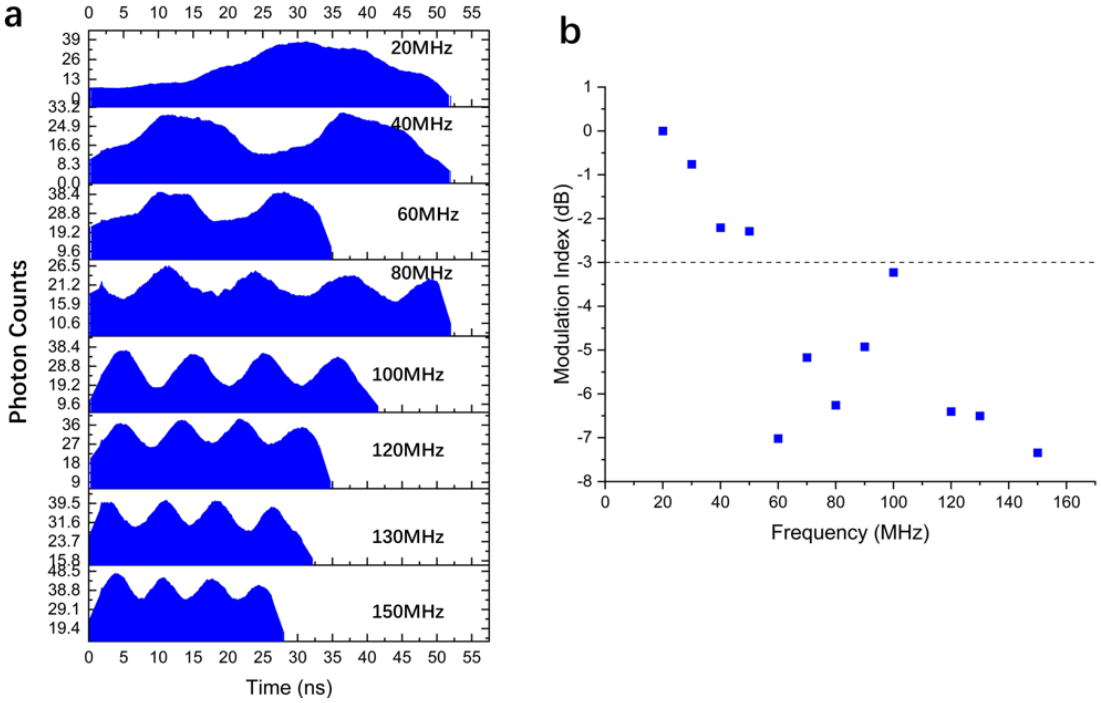

Figure 5.7: (a) Graph of photo counts corresponding to time showing time-domain measurements at modulation frequency of 20, 40, 60, 80, 100, 120, 130 and 150 MHz. (b) Cut-off frequency plot showing the modulation index of printed micro-LED pixel.

As introduced previously, the modulation index is defined as $10\log_{10}\left(\frac{P_{\max}-P_{\min}}{P_{\max}+P_{\min}}\right)$, where $P_{\max}$ and $P_{\min}$ are maximum and minimum intensity values, respectively. [275] The mean values of the peak photon counts were filtered and calculated to get maximum and minimum intensity values for each modulation frequencies. A plot as Figure 5.7 (b) shows that the −3 dB point is between 50 and 60 MHz, which matches the research in reference [279] (where micro-LED pixels were fabricated under identical conditions). This corresponds to a 50% attenuation in output power modulation, reducing the effectiveness of driving the micro-LED pixels. However, it is still a milestone if the printed micro-LED can pump and modulate (small-signal modulation) transfer-printed NWs

directly and transfer the signal through polymer waveguides in the tens of MHz ranges.

5.5 Fabrication and Integration of the Nanowires-Embedded-in Polymer-Waveguides Sample and Micro-LED Pixels for On-chip Excitation and Modulation

5.5.1 Direct Integration of Micro-LED Pixel and First Generation of Sample

The first device iteration was to integrate the NW-in-Waveguides used and introduced in Chapter 4 and the micro-LED pixels together by using the NLP 2000 transfer-printing system. As shown in Figure 5.8, a single pixel was managed to be printed on the sample directly, the pixel moved and rotated a lot during the stamp releasing process even though it was well-aligned during the alignment and printing stages. This poor adhesion quality would not make the pixel survive during the on-chip probing process. Moreover, the pitch between waveguides did not match the micro-LED size. Therefore, both new waveguide design and additional adhesion layer were taken into consideration for a second iteration.

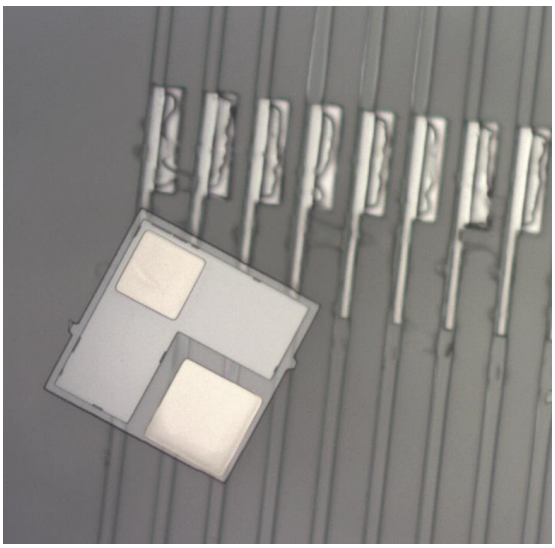

Figure 5.8: Image of a printed Micro-LED on the NWs-Embedded-in-waveguides sample.

5.5.2 New Design and the Fabrication

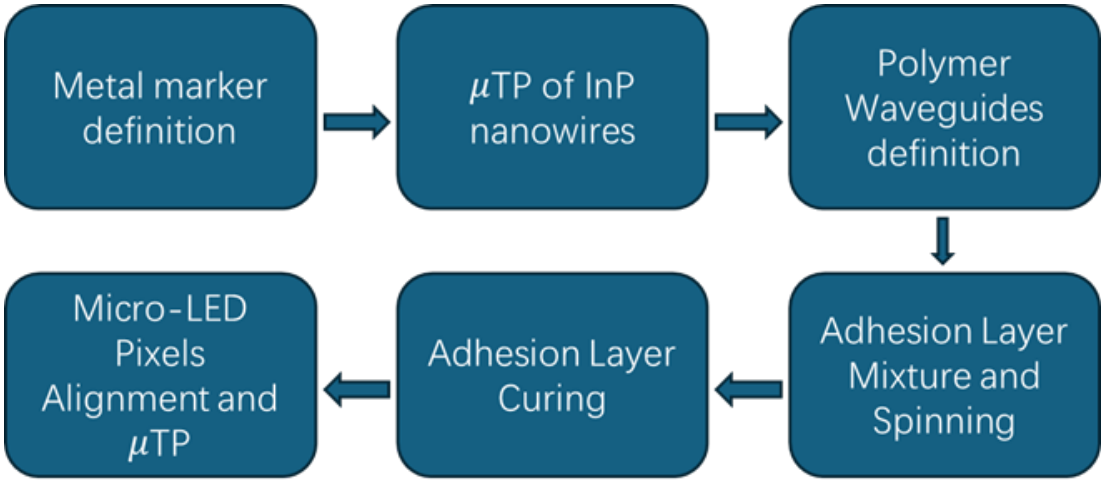

Figure 5.9: Flow process of the chip fabrication.

As the old design was clearly not suitable for as a receiver substrate for micro-LED printing, an optimised design as shown is Figure 5.10 (a) was promoted. In this design, the pitch between waveguides were modified to 127 μm so that each printed NW can be individually excited by one printed micro-LED pixel. Additional blocks in SU-8 were added between waveguides and would be fabricated at the same time while the waveguides were defined. This could made printing area less rough and decreasing the difficulty of releasing during the μTP process.

As shown in the flow chart (Figure 5.9), the fabrication process started with the definition of metal markers. This process included photoresist spinning, laser lithography, development, metal deposition and metal lift-off. All the process were the same as the fabrication process introduced in Chapter 4, but the laser lithography machine 'Heidelberg' read the modified metal layer design shown in Figure 5.10 (a) for global alignment before the definition of waveguides and supporting blocks. By applying the same methods as before, InP nanowires (the same as the Chapter 4) in total were aligned and printed and they all survived the fabrication of polymer waveguides and supporting blocks.

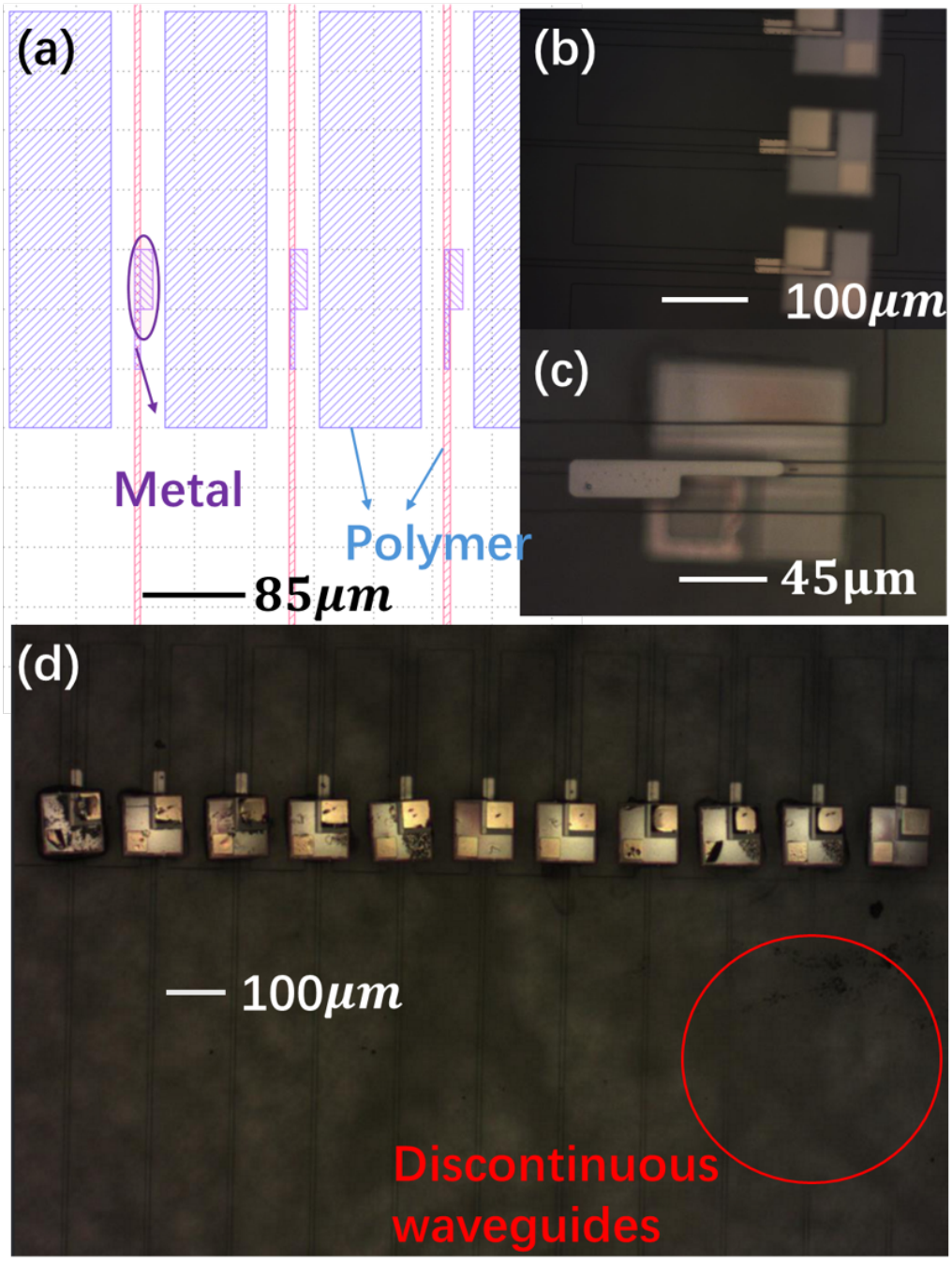

Figure 5.10: (a) Modified design of the new receiver chips including metal markers, waveguides and additional receiver blocks. (b) Microscope captured image of printed pixels on the NW-in-waveguides chip (focus on the waveguide) (c) Microscope captured image (from the chip backside) of a single printed micro-LED, the metal marker, printed NW and polymer waveguides were included. (d) A microscope captured image of 11 printed micro-LED on the chip after probing test.

The edges of the sample were covered by applying low adhesion tapes before the spinning of the adhesion layer. This step could efficiently protect the facets from the adhesion layer to make the possible emission from nanowires collectable at facets. As introduced in previous sections and research [308], PDMS is optically transparent for the visible spectrum and its refractive index is lower than SU-8, so the waveguides still guide. The mixture process of the 10:1 (weight ratio of PDMS base and curing agent) was exactly same as the procedure of PDMS stamp fabrication introduced in Chapter 2. The liquid PDMS mixture was then poured onto the surface of the NWs-in-waveguides sample which was fixed by vacuum on the spinner after 40 minutes of degassing. The spinner would spin the sample at 5000 RPM for at least one minute to make the PDMS as thin as possible. The sample was then left in the university cleanroom overnight to let the thin PDMS layer cure, and ready for the printing of micro-LED pixels.

Same as the printing of micro-LED pixels onto a PDMS stamp, the advanced transfer-printing system was applied. During the alignment and printing process, the P-region (emitting area) of the micro-LED pixel was placed right on the embedded NW area, demonstrated as Figure 5.10 (b). The Figure 5.10 (c) shows the image captured from the backside of the sample, the NW was fully covered and overlapped with the P-region of a pixel and the most part of the pixel was supported by the SU-8 supportive blocks. 21 micro-LED pixels were printed on the sample, 16 of them were used to excite and modulate the NWs underneath and the other 5 pixels printed on bare waveguides were used for probing practice and the analysis of SU-8 fluorescent emission [284] (which was also mentioned in the Chapter 4). Figure 5.10 (d) shows an overview of the sample captured by the microscope after probing and test, only 11 of the printed pixels are included in the image due to the limitations of the field of view. After probing and test, 20 out of 21 devices worked properly.

5.6 On-chip Excitation of Nanowires and Discussion of SU-8 Emissions

5.6.1 Methods of measurement

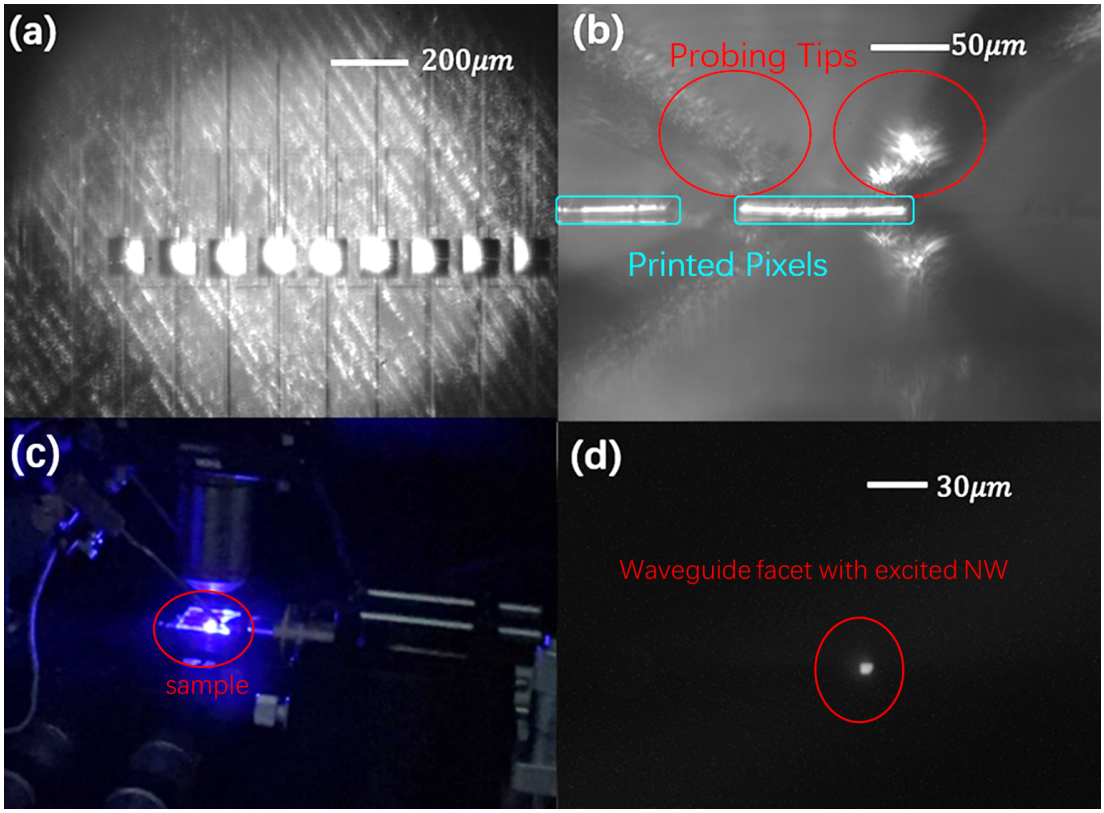

Figure 5.11: (a) Top CMOS camera captured image of the NW-in-waveguides chip with blue micro-LED pixels printed, illuminated by the external 405 nm Micro-LED-on-CMOS projection set-up. (b) CMOS camera in the Set-up edge detector part captured diagram of the printed micro-LED pixel and the probing tips. (c) Image of probed and emitting Micro-LED on the sample with nanowires. (d) Filter image (800 nm LP filter applied) of a waveguide facet with NW embedded while the printed micro-LED is probed.

The probing process at this stage was nearly the same as the previous process of probing micro-LED on PDMS stamp. The chip fixed on the 3-axis stage would be illuminated by the pixels on the 405 nm micro-LED-on-CMOS chip as shown in Figure 5.11 (a). The probing tips were then moved above the metal contact regions and the CMOS camera in the edge detector set-up shown in Figure 5.6 (a) captured a diagram including two

probing tips and a printed Micro-LED pixel, shown as Figure 5.11 (b). The 3-axis stage was then slowly raised to bring the probing tips into contact with the micro-LED pixel. A DC voltage of 3.5 V , supplied by a DC power source (with the small-signal generator turned off), was applied. Under this bias, the printed pixel was successfully excited and exhibited light emission. The active pixel of the micro-LED-on-CMOS for illumination purpose was then turned off, and an overview image of the sample with the emitting printed pixel was captured and is shown in Figure 5.11(c). From the research in Chapter 4, the emission from the SU-8 cannot be fully avoided and could be captured by the CMOS camera if the edge detector set-up while applying a 700 nm LP filter. To optimise the research and minimise the influence of SU-8 emission, an 800 nm LP filter was applied to replace the previous one in the edge detector. Figure 5.11(d) shows the filtered image of the light-emitting waveguide facet, where the corresponding micro-LED was printed and probed. To determine whether this emission collected at the waveguide facet was dominated by the embedded nanowire or SU-8 emission, a comparison and analysis were required.

5.6.2 Analysis of Emission with Different Filters

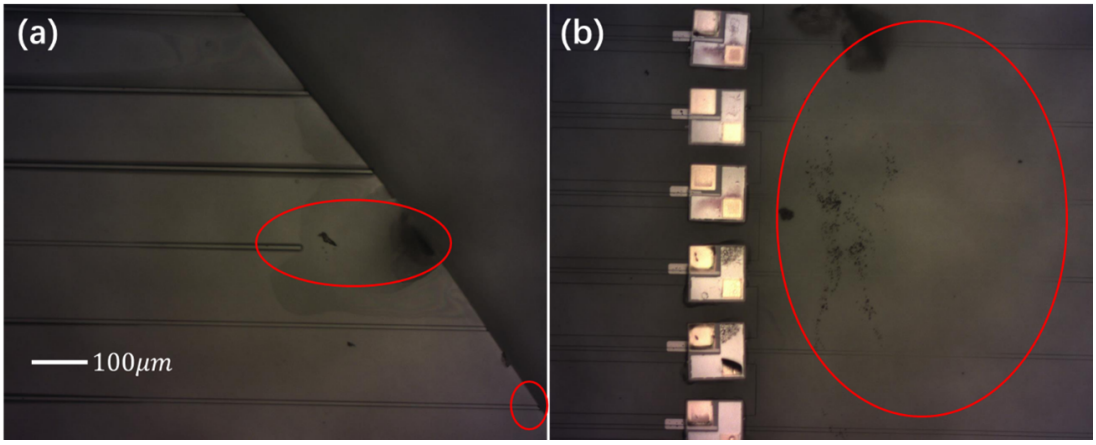

Figure 5.12: Microscope captured image of (a) Damaged waveguide facets. (b) Discontinuous waveguides due to the bubbles during polymer photoresist spinning before laser lithography.

As mentioned before, all 21 printed micro-LED pixels were probed and 20 of them were successfully excited by a DC voltage of 3.5 V, pixel 1 was burnt and cracked by probing tips during the probing. The edge CMOS camera was used to capture all filtered (800 nm LP filter applied) waveguides facets images at the same exposure parameters. However, for the 15 printed pixels on waveguides with NWs buried, only 8 of them delivered usable images. For device 6 and 8, the facets were damaged during the sample cleaving stage and were then covered by PDMS. For devices 9–11, the waveguide fabrication was affected by bubbles in the SU-8 photoresist, resulting in discontinuous waveguides. Figure 5.11 includes two images of the sample captured by microscope during the trouble shooting, and the damaged facets and waveguides are highlighted.

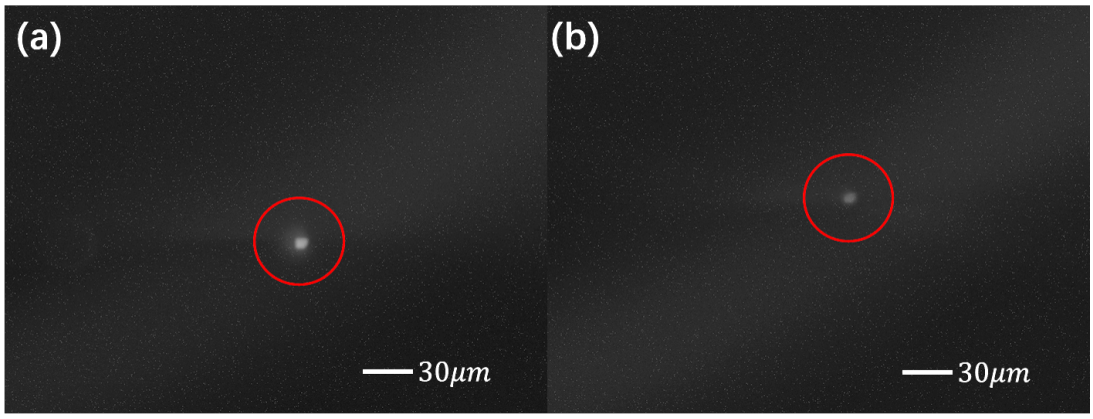

Figure 5.13: CMOS camera captured filtered (800 nm LP) image of (a) the brightest waveguide facet with NW embedded inside. (b) the brightest waveguide facet without NWs.

As the exposure parameter was set to be consistent during the whole measurement, the intensity of the output emission at the facet can be analysed by using a MATLAB script to calculate the integrated brightness of the emitting area. Figure 5.13 shows two images captured by the CMOS camera at the same parameters, diagram (a) is the brightest facet emission (device 3) out of the 8 successfully captured image that NWs were embedded inside waveguides, and diagram (b) is the brightest emission out of the 5 waveguides without NWs inside. The emission in (b) is primarily dominated by SU-8 fluorescent as previously researched in Chapter 4 and reference [284].

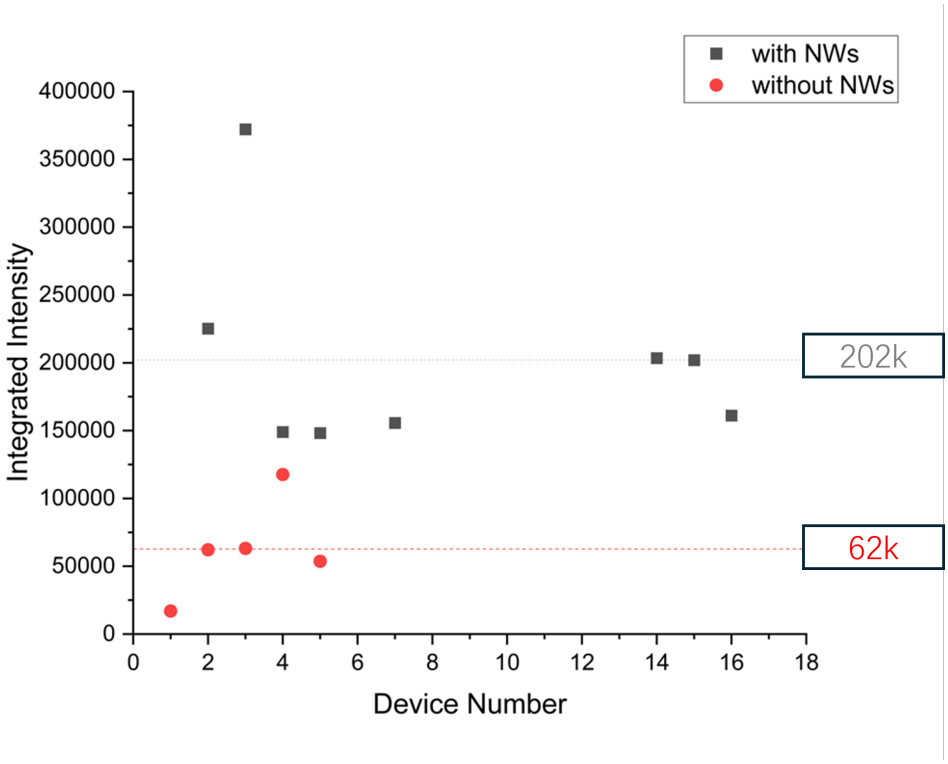

Figure 5.14: Scatter plot of the calculated intensity at each waveguide facet with 800 nm LP filter placed.

The script would generate an editable box first, the output of the manuscript would be the integrated intensity of the selected area. During the diagram processing process, the area of the box was kept the same and the integrated intensity of the waveguide facet would be the integrated intensity value of each facet minus the integrated intensity value of the background (calculated by the same script for each image).

Figure 5.14 indicates the calculated integrated intensity for all 13 devices (8 with NWs and 5 without NWs) at facets. The average intensity of waveguides with NWs is approximately 3.2 times as high as that of waveguides without NWs. For the best-performing device (Device 3), the intensity at the facet is approximately 3.16 times as high as that of the strongest measured SU-8 emission.

For the very sensitive SPAD camera, it required longer integration time during one measurement with the 800 nm LP filter in place, and the signal-to-noise ratio would be relatively lower as more noise would be introduced into measurement. Therefore, it is

meaningful to study the difference between NWs emission and SU-8 fluorescent emission while applying the 700 nm LP filter. The data captured with the 700 nm LP filter can be considered meaningful if the emission intensity contrast between waveguides with and without NWs shows a similarly pronounced difference as observed with the 800 nm LP filter.

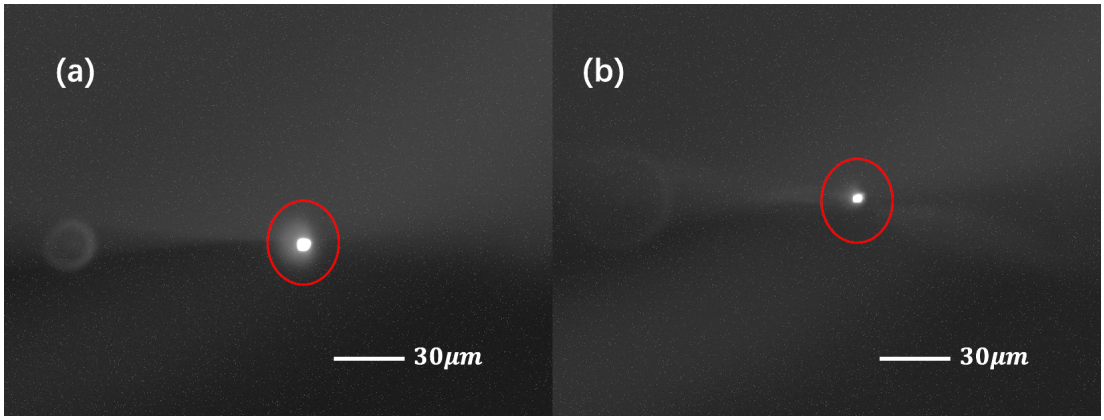

Figure 5.15: CMOS camera captured filtered (700 nm LP) image of (a) the brightest waveguide facet with NW embedded inside. (b) the brightest waveguide facet without NWs.

As shown in Figure 5.15, the CMOS camera captured the brightest waveguide facet with embedded NWs and the strongest emission from bare waveguides with the 700 nm LP filter in place. The scatter diagram of the integrated intensity of all waveguide facets is shown as Figure 5.16. The average intensity at the facets of waveguides containing NWs is approximately 2.6 times that of the average SU-8 emission intensity, while the peak facet intensity with NWs is approximately 3.8 times as much as the strongest measured SU-8 emission intensity.

A one-way ANOVA was performed to compare the emission intensities measured from waveguides with and without integrated nanowires with both 700 nm and 800 nm LP filters. The F (14.88 and 8.26 for 700 nm and 800 nm) and p (0.00266 and 0.015 for 700 nm and 800 nm) value demonstrate that the nanowire contributes substantially to the optical output in both spectral windows, whereas the bare waveguide only exhibits weak background emission. However, the influence of SU-8 waveguide emission, which acts as additive noise in this project, can be significantly reduced by applying the

800 nm long-pass filter.

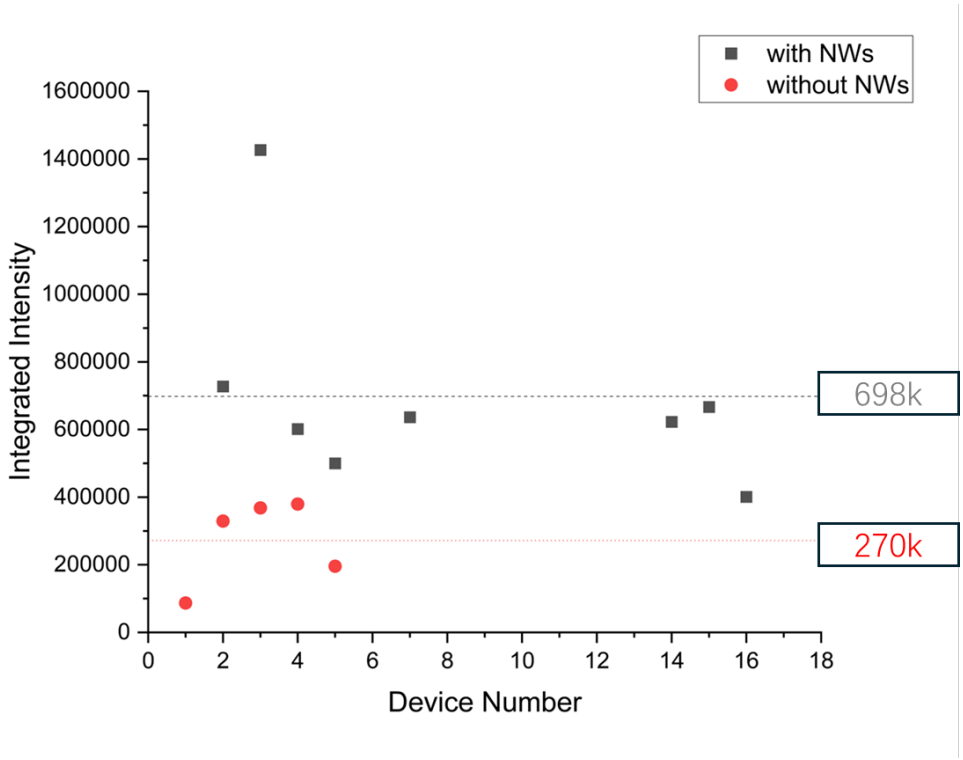

Figure 5.16: Scatter plot of the calculated intensity at each waveguide facet with 700 nm LP filter placed.

5.7 Small Signal Frequency Modulation Results of Printed NWs

The printed micro-LED pixels were excited and modulated electrically (small signal modulation) by the frequency generator 'Moku:pro' through the DC voltage power supply and the additional bias Tee, the operation methods were the same as that previously demonstrated in Section 5.4. The optical emission following the modulation frequency would optically excite and modulate the embedded NWs, and finally the NWs emission would couple with the polymer waveguides and be collectable at the facet as the SU-8 provided higher refractive index than the glass substrate (mentioned in Chapter 2 and 4) and PDMS adhesion layer in this case.

The SPAD camera was aligned using photon count mode, and then switched to

TCSPC mode for modulation results collection. The modulation results of device '2' and '3' (best performance devices) at 20, 40, 60, 80, 100 and 120 MHz were collected and signal processed by using the same method as Section 5.4. Two groups of results were measured with different long pass filters, 700 nm for better signal-to-noise ratio and 800 nm for more accurate NW emission. Based on the analysis and research in Section 5.6.2, the data would be dominated by the excited NW once the SPAD camera was aligned and no matter which filter was used. During this process, the synchronisation signal used for SPAD camera triggering was the same as before and can be found in Table 5.1, also, the DC voltage applied was 3.5 V and the voltage of the modulation signal varied from 0 to 1 V, which was also the same as the condition introduced in previous micro-LED pixel manipulation section.

and the

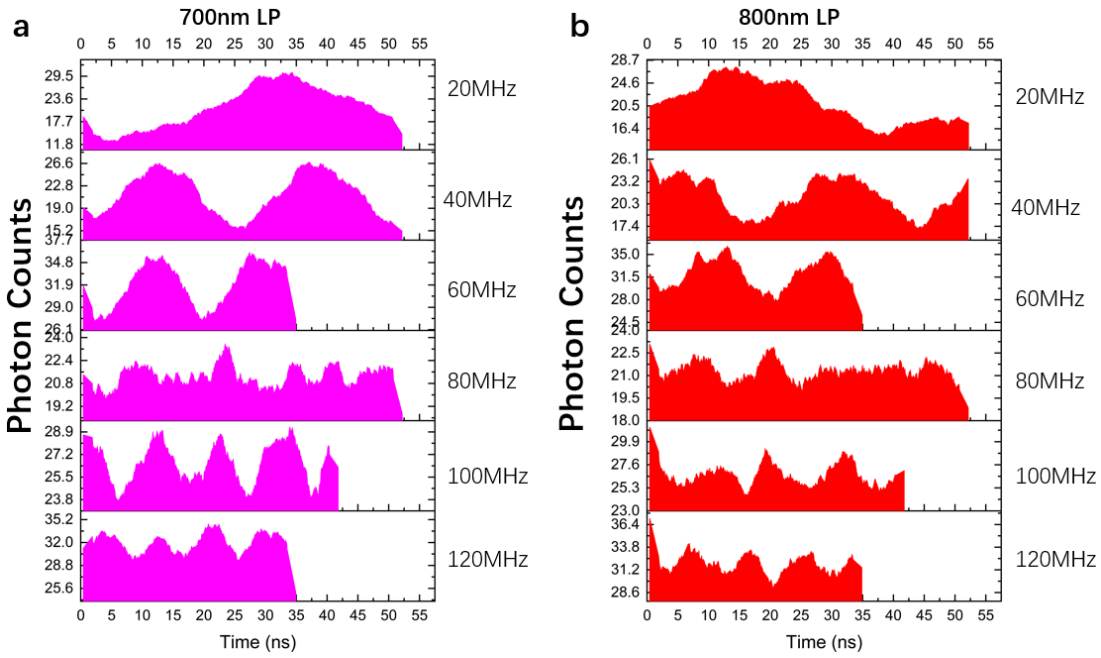

Figure 5.17: Time-domain measurements of device "3" applying (a) 700 nm LP filter (b) 800 nm LP filter at modulation frequencies of 20, 40, 60, 80, 100 and 120 MHz.

Figure 5.17 (a) and (b) show the TCPSC data of device '3', the best performance one, with a 700 nm and 800 nm LP filter attached on the set-up, respectively. For the measurement performed with a 700 nm long-pass filter, the modulation signal is clearly

observed and closely follows the optical modulation frequency of the printed micro-LED at 20, 40, 60, 100 and 120 MHz. The peak-to-peak value which represents the intensity of emission starts to drop significantly from 60 MHz, and this is the previously measured cut-off frequency. The modulation index values of micro-LED and NWs with different filters are shown as Figure 5.18, and it is clear that the NW follows the temporal envelope of the micro-LED emission. In the previous measurement of the micro-LED's cut-off frequency shown in the 5.7 (a) and (b), a 'dip' was shown at 80 MHz, where the optical power significantly dropped. In the modulation of NW, this 'dip' led the optical modulation of NW unmeasurable at this specific frequency and the reason behind this should be researched in future.

For the measurement with an 800 nm LP filter, the modulation results of NWS were still clear for modulation frequency at 20, 40, 60, 100 and 120 MHz but with low signal-to-noise ratio. These results indicate that the nanowires can be optically pumped and modulated by integrated micro-LED pixels in the tens of megahertz (MHz) range, demonstrating optical performance comparable to the previous projection-based approach, but with significantly improved scalability in an on-chip design.

5.8 Summary

This research successfully transfer-printed blue micro-LED pixels from the fabrication substrate onto a PDMS substrate. The characterisation of these micro-LED pixels was measured by direct on-chip probing. The power density of these micro-LED pixels is $\sim 0.09\,\mu W/\mu m^2$ which is substantially lower than the that of the micro-LED-on-CMOS structure. However, it inspired the further integration and increased the scalability by excluding sapphire substrate, controller board and free space optics devices. Additionally, small signal modulation can be applied on these printed devices.

Secondly, a second generation of NW-in-Waveguides chip with optimised pitch was designed and fabricated, 16 InP nanowires were embedded inside into an array of 16 polymer waveguides. With the help of adhesion layer (thin PDMS), this chip was integrated with 21 micro-LED pixels (16 on waveguides with nanowire emitters).

Optical pumping of nanowire emitters and collection of coupled near infrared signal

through polymer waveguides by probing the printed micro-LED pixels (emitting in visible spectrum) with a 3.5 V DC voltage was achieved for the first time. Also, the embedded nanowires were optically modulated (small signal modulation) in the tens of megahertz (MHz) range. Compared to the projection method to optically pump and modulate nanowire emitters, the optical performance is close while the improvement in scalability is enormous.

In the future, the reason behind the power drop of the printed micro-LED at 80 MHz should be researched and analysed. An optimised suspended micro-LED array with higher power density for transfer-printing purpose should be designed and fabricated. Additionally, alternative waveguides and substrate material such as Lithium Niobate or Silicon Nitide on Silicon substrate should be tested and researched to reduce fluorescent noise caused by SU-8.

In summary, this research successfully packaged the optical pump system and nanowire-in-waveguide devices into a single package, created a compact system with high scalability by removing projection optics and shrunk the PIC for data communications applications.

Chapter 6

Conclusion and Future Work

In this Chapter, a short summary is presented first to conclude this thesis and to re-iterate the major outcomes. This research is mainly focused on applying high yield micro-transfer-printing technique to optimise devices with non-uniformity caused during large-scale micro-fabrication and build prototype of functional photonic integrated circuits with high scalability. Both achievements and issues met during the project are listed and analysed in this section. Moreover, based on the issues, future work including proposed advances in process design, applied optical components or experimental methods are also discussed to enhance the scalability or optical performance of the whole system.

6.1 Conclusion

The outcome and results of this PhD research project can be divided into two main parts, the first one is the characterisation, selective pick-up and spatially reorganisation of Silicon Photonic Cavities membranes to substrates with supporting frames in different materials to create suspended structure for enhanced optical performance and uniformity, and the second one is embedding nanowires with optical structures such as polymer waveguides and optical modulation of these nano-emitters through an electrically addressable incoherent pumping source.

In the first results chapter, silicon photonic crystal cavities (PhCCs) membranes

were picked-up and printed using a dip-pen nano-lithography (DPN) micro-transfer-printing system onto thin supportive frames of photoresist and silica on silicon wafers, respectively. The transfer-printing process achieved high yields, 60% for photoresist frames and 100% for silica frames. With the advanced transfer-printing system, 119 out of 120 PhCCs membranes were characterised and then selectively picked up and printed on silica frames on silicon wafers in a high-density array. The re-grouped and printed PhCC membranes exhibited a mean wavelength shift of $\pm 0.007\,\text{nm}$ and a standard deviation of $\pm 0.021\,\text{nm}$, respectively, indicating significantly improved uniformity compared to the original PhCC membranes on their fabrication substrates, which showed a wavelength shift standard deviation of approximately 1 nm.

The developed transfer-printing technique then successfully enabled the precise integration of an array of 20 nanoscale light emitters, specifically, embedding 20 semiconductor nanowires into 20 polymer (SU-8) optical waveguides on high-quality glass slides substrates successfully. A customised optical projection and modulation system, based on a micro-LED-on-CMOS array, was designed to optically excite the embedded nanowires and modulate the resulting infrared emission. This modulation (on-off-keying) followed the frequency bandwidth of the visible incoherent light from the micro-LED array which can be independently controlled through CMOS circuits, reaching into the hundreds of megahertz (MHz) range. The emitting infrared signal was effectively coupled into the polymer waveguides and collected at the output facets, demonstrating the feasibility of integrating nanowire-based light sources into flexible photonic circuits. This work is the first demonstration of optical excitation and modulation of nanowires using incoherent visible light sources. However, lasing was not observed, primarily due to power losses introduced by the free-space optical components in the set-up.

The final chapter explored a promising approach toward realizing lasing and improving scalability by integrating optical pumping sources directly with the nanowire-embedded-in-waveguide structure, with the help of a thin polydimethylsiloxane (PDMS) layer. In this design, suspended GaN -based micro-LED pixels ($100\,\mu\text{m} \times 100\,\mu\text{m}$, 450 nm wavelength) served as the optical pumping sources. A total of 16 successful transfer-printing attempts ensured precise alignment, with each nanowire matched to

a corresponding LED pixel. This integration enabled on-chip excitation and modulation of the nanowires, marking a significant step toward fully integrated photonic systems. However, lasing was not observed, primarily due to the limited optical power delivered by the micro-LED pixel membranes, which was lower than that provided by the previously employed projection set-up. Additionally, the horizontal emission of the printed pixels led to inefficient power coupling into the nanowires. Compared to the Micro-LED-on-CMOS array, the printed pixels also exhibited a reduced cut-off frequency, attributed to the absence of a sapphire substrate (which provides better thermal management). Despite these limitations, the demonstrated configuration significantly enhanced system scalability and successfully achieved direct on-chip modulation (small signal) in the tens of megahertz (MHz) range which is comparable to the performance of earlier projection manipulation methods.

6.2 Improvement and Future Work

In future work, the spatially rearranged silicon photonic crystal cavity (PhCC) membranes, previously demonstrated to exhibit high Q-factors and stable optical performance with minimal emission wavelength shifts, will be further optimised by integrating them onto micro-LED-on-CMOS arrays via transfer-printing. This platform enables precise spatial alignment and offers the potential for scalable, high-speed operation.

The micro-LED-on-CMOS array will be designed to support grayscale illumination [280], enabling dynamic pattern projection. Such functionality can be employed to induce steady-state tuning of the individual PhCC membranes through the plasma dispersion effect [311], thereby aligning their resonant wavelengths and compensating for any fabrication-induced variability.

Moreover, this optically induced plasma dispersion effect can be further applied as a core mechanism in the development of a high-speed spatial light modulator (SLM) [129]. Due to its controllable nature, the plasma dispersion effect provides the ability of modulating the refractive index of the printed silicon PhCC arrays layer, thereby enabling dynamic control over both the phase and amplitude of the incident optical beam. This approach offers a promising pathway toward fully reconfigurable, highspeed

photonic devices suitable for optical computing, and advanced display technologies.

Additionally, a good quality bottom reflector placed under the Silicon PhCCs membrane with a suitable distance can enhance both vertical optical confinement and potentially increase the Q-factor. [254] In this project, bulk silicon was applied as the bottom reflector and its reflectivity of a wavelength of 1550 nm is $\sim 30\%$ [312] and is not ideal, also its strong absorption over visible wavelength prevents the applications like SLMs with optical pumps. Therefore, a distributed Bragg reflector (DBR) [254] can be investigated, it should be transparent at shorter wavelengths allowing for efficient carrier generation in the cavity layer via the plasma dispersion effect and show high reflectivity at the incident beam. This modification could reduce substrate leakage losses and enable more efficient bidirectional operation, particularly in configurations involving reflection-mode spatial light modulation.

For the modulation of semiconductor nanowires, the main limitations of our current systems are the optical power and waveguides emission. In both the projection-based and on-chip integration approaches using micro-LED pixels, the nanowires exhibited only spontaneous emission rather than stimulated emission. A key limitation in both configurations is the insufficient spatial overlap between the nanowires and the light spot (for projection)/emitting area (for printed pixels). This mismatch results in significant optical power loss, with a substantial portion of the pump light failing to couple into the nanowire active region. Instead, much of the light is scattered into the surrounding polymer waveguides and glass substrate, leading to unintended emission from the SU-8 waveguides rather than from the printed nanowires themselves.

A plot to show the relationship between the output intensity of the nanowire emission and the pumping power is drawn as Figure 6.1. To observe the NW lasing, the pumping power must meet the threshold and there are several ways to achieve this. The first one is optimising the design of the printed LED pixels to increase the efficiency and deliver more optical power on the NW. Secondarily, a pulsed pumping laser [57] can be induced to deliver higher pumping power just beyond the threshold, then the pixel on micro-LED-on-CMOS can be projected onto the nanowire and use a small signal modulation within the stimulated emission region shown as Figure 6.1. Therefore, this

will be the first time using an incoherent light to modulate the coherent light signal. However, the giant pumping laser, the micro-LED-on-CMOS array and other free-space optical components are still challenges and not elegant solutions for photonic integrated circuits.

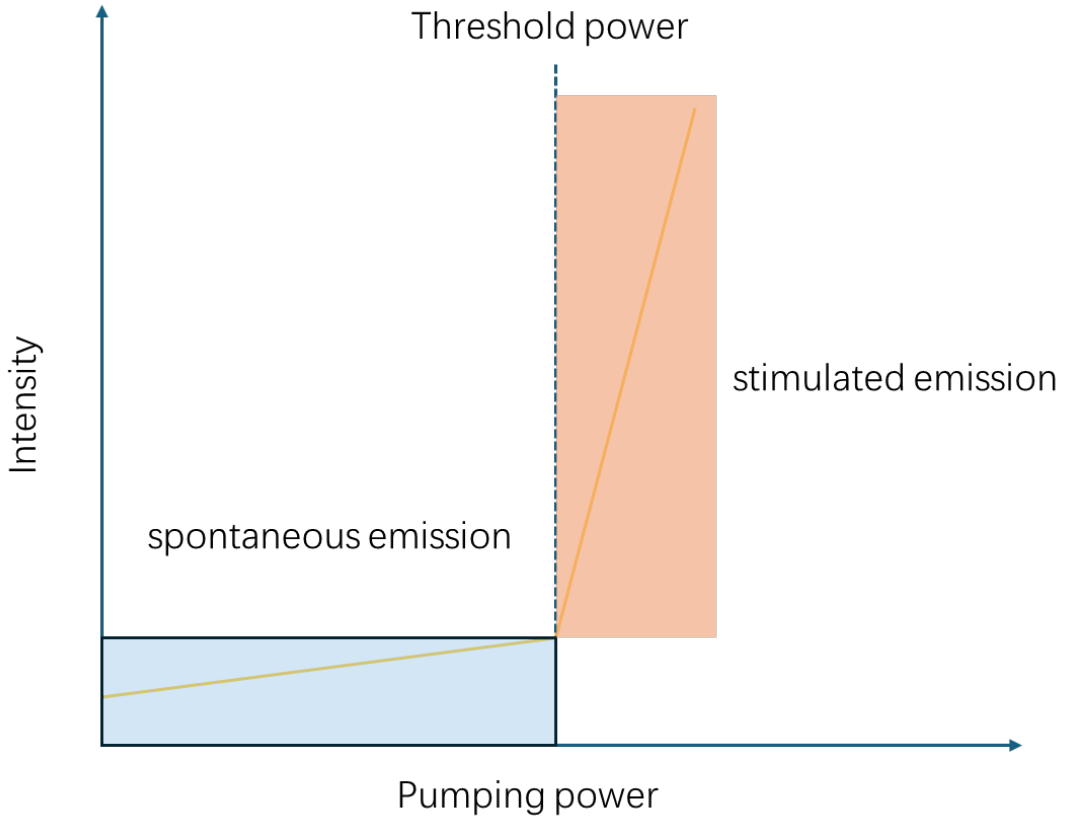

Figure 6.1: Schematic of a plot of nanowire output intensity and pumping power.

One of the reasons for using incoherent light sources is the scalability of the array. However, it is desirable to use an optical component that can provide significantly higher power and scalability at the same time, it can also be integrated to provide on-chip excitation and modulation. The research of vertical-cavity surface-emitting lasers (VCSELs) [313] can make on-chip NW lasing with very high scalability possible. Unlike the pixel integrated in this project, VCSELs can emit from either top or bottom, which can deliver most of the power to excite nanowires and manipulate with on-off keying modulation.

However, current research on VCSELs is more focused on long wavelength (telecommunications wavelengths [314]) and is not the most efficient for optically pumping the NWs. Instead of VCSELS, vertical emitting micro-LEDs [315] are also potential candidate if the optical power can exceed the threshold. These vertically emitting micro-LEDs can achieve output power densities of up to $\sim 0.55\,\mu\mathrm{W}/\mu\mathrm{m}^2$. [179] However, due to their lateral dimensions being on the order of tens of micrometers, the spatial mode overlap with the nanowire regions is significantly limited which can lead to waste of optical power. Also, the high injection current density required for achieving high optical output power can lead to significant thermal issues, which can be worse by the presence of adhesion layers in waveguide-integrated samples. Moreover, the fabrication of these vertically emitting devices is relatively complex. Combined with the additional challenges in their transfer-printing, more mature and robust transfer-printing techniques need to be developed to accommodate these comparatively bulky devices.

In both Chapter 4 and 5, it was clearly demonstrated that the photoluminescence (or fluorescence) from polymer waveguides caused by emitting/scattering light from pumping sources can increase the background noise. Otherwise, waveguides in other materials such as silicon nitride [316] should be researched, other possible structures for higher integration density and scalability are worth investigation.

The work presented in this thesis showed the possibility to build high-density photonic integrated circuits with micro/nano-scale components in good uniformity by applying high yield, accurate transfer-printing techniques. This technique not only overcomes the fabrication and assembly difficulties but also enables the wide application of photonic integrated circuits in fields like data transmission and display.

List of Publications

Journal Papers

1. **Z. Xia**, D. Jevtics, B. J. E. Guilhabert, J. J. D. McKendry, Q. Gao, H. H. Tan, C. Jagadish, M. D. Dawson, M. J. Strain, "Modulation of Nanowire Emitter Arrays Using Micro-LED Technology," *ACS Nano*, vol. 19, no. 16, pp. 15813–15819 (Epub April 16, 2025; published April 29, 2025). DOI: 10.1021/acsnano.5c00474.

2. S. P. Bommer, C. Panuski, B. Guilhabert, **Z. Xia**, J. A. Smith, M. D. Dawson, D. Englund, M. J. Strain, "Transfer printing micro-assembly of silicon photonic crystal cavity arrays: beating the fabrication tolerance limit," *Nature Communications*, vol. 16, Article 5994 (2025; published July 1, 2025). DOI: 10.1038/s41467-025-60957-1.

3. B. Guilhabert, S. P. Bommer, N. K. Wessling, D. Jevtics, J. A. Smith, **Z. Xia**, S. Ghosh, M. Kappers, I. M. Watson, R. A. Oliver, M. D. Dawson, M. J. Strain, "Advanced Transfer Printing With In-Situ Optical Monitoring for the Integration of Micron-Scale Devices," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 29, no. 3, pp. 1–11, May–June 2023. DOI: 10.1109/JSTQE.2022.3227340.

Conference Papers

1. **Z. Xia**, D. Jevtics, B. Guilhabert, J. J. D. McKendry, H. H. Tan, C. Jagadish, M. D. Dawson, M. J. Strain, "Towards scalable on-chip excitation of micro- and nano-photonic emitters," in *Proceedings of CLEO: Applications & Technology 2024 (Optica Publishing Group, Technical Digest Series)*, paper ATu4J.5, CLEO:A&T, Charlotte, NC, USA, May 5–10, 2024.

2. **Z. Xia**, D. Jevtics, B. Guilhabert, J. J. D. McKendry, H. H. Tan, C. Jagadish, M. D. Dawson, M. J. Strain, "Scalable optical excitation and modulation of semiconductor nanowire emitters," in *Proceedings of the British and Irish Conference on Optics and Photonics 2023 (Optica Publishing Group)*, paper Th5B.3, London, UK, December 13–15, 2023. DOI: 10.1364/BICOP.2023.Th5B.3.

3. **Z. Xia**, D. Jevtics, B. Guilhabert, J. J. D. McKendry, H. H. Tan, C. Jagadish, M. D. Dawson, M. J. Strain, "Optical pumping of nanowire emitters embedded in polymeric waveguides using a micro-LED array," in *Proceedings of the 2023 IEEE Photonics Society Summer Topicals Meeting Series (SUM)*, Sicily, Italy, July 17–19, 2023. DOI: 10.1109/SUM57928.2023.10224436.

4. S. P. Bommer, C. L. Panuski, B. Guilhabert, **Z. Xia**, M. D. Dawson, D. R. Englund, M. J. Strain, "Overcoming Nanofabrication Variance in Photonic Crystal Cavities by Transfer Print Integration," in *Proceedings of the 2024 Conference on Lasers and Electro-Optics (CLEO)*, San Jose, CA, USA, May 5–10, 2024, pp. 1–2. ISBN: 2160-8989.

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