Control and Operation of Solid-State Transformer (SST) in Distribution Network

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This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

Signed: Date:

Dedicated to my family

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Abstract

Distribution network has been confronting with many challenges, such as reverse power flow, power quality issue and DC integration due to the increasing penetration of renewable energy. To tackle these issues, solid-state transformer (SST) has recently been considered as a promising solution for the future distribution network. Compared with the line-frequency transformer (LFT), SST can not only feature full controllability of voltage and power in the LV network, but also provide the potential DC connectivity at the middle stage and fault isolation capability between MV and LV networks.

To ensure that SST operates under grid-forming and grid-connected operation without large control mode switch transient, a universal control scheme using a grid forming structure is proposed where SST can operate when the LV side operates either as an isolated network or grid connected to the adjacent network (through the conventional normal opened point (CNOP)). To address the coupling issue between active and reactive power with the grid forming control design when the SST LV side is grid connected, an additional compensation control using active and reactive power feedforward compensation to dq-axis current components of the DC/AC converter is proposed. The active and reactive power fluctuation due to the coupling is significantly reduced without affecting system response. Based on the control scheme above, SST-based distribution network can benefit distributed generation (DG) consumed locally.

To avoid unnecessary converter blocking and increase the reliability of SST, the postfault performance of SST under grid-forming and grid-connected operation is compared with the LFT in different network configurations. The fault current limiting of SST reduces the fault current contribution, and SST can isolate fault current from faulty side to healthy side. In order to prevent SST from unnecessary blocking due to large MVDC voltage fluctuation caused by active power unbalance between MV and LV sides during the fault and improve postfault recovery, an active power limiting control of the SST is proposed where the MVDC voltage variation directly set the d-axis voltage (grid-forming operation)

or the active power output reference (grid-connected operation) of the LV side converter. The MVDC voltage variation can be reduced within 10%, and SST can remain operative during fault, which achieve fast post-fault recovery after fault is cleared.

Finally, considering the topology configuration of SST converter, the AC and DC networks can be co-ordinately operated via the SST. The impact of introducing DC network to SST-based distribution network on the operation and control of the SST is investigated. The types of DC network integration are reviewed and discussed. A coordinated control of the SST and the DC network is proposed for optimising the operation of the SST-based hybrid AC/DC distribution network. With linking MVDC voltage with power output of the DC network, the SST enables the DC network to provide the needed power to ensure the power supply to the load side autonomously. And the adaptive control scheme can regulate the power output of the connected ESD without communication. In addition, the DC fault characterisation and protection requirement of the proposed system are investigated. Fast SSCBs allow the immediate isolation of the faulty DC section without the need for converter (TAB) blocking, which in turn minimizing the disruption for the healthy networks. Meanwhile, the slower DCCBs, e.g., HCBs, will result in fault current contribution from the MV side for a short period, which can affect the operation of the healthy network.

The effectiveness of SST control schemes, including basic control, grid forming control, additional compensation control, coordinated control are all validated in MATLAB/Simulink.

List of Abbreviations

EU	European Union
DERs	Distributed Energy Resources
ESD	Energy Storage Device
CHP	Combined Heat and Power Plant
ANM	Active Network Management
STATCOM	Static Synchronous Compensator
SVC	Static Var Compensator
UPQC	Unified Power Quality Conditioner
DVR	Dynamic Voltage Restorer
SST	Solid State Transformer
LFT	Line Frequency Transformer
HVDC	High Voltage Direct Current
VSC-HVDC	Voltage Source Converter HVDC
MVDC	Medium Voltage Direct Current
CNOP	Conventional Normally Open Point
SNOP	Soft NOP
ZVS	Zero Voltage Switching
MFT	Medium Frequency Transformer
DAB	Dual Active Bridge
CHB	Cascaded H-Bridge
PWM	Pulse Width Modulation
PSM	Phase Shift Modulation
ISOP	Input Series Output Parallel
PLL	Phase Locked Loop
PI	Proportional Integrator
SPS	Single Phase Shift Modulation
EPS	Extended Phase Shift Modulation

DPS	Dual Phase Shift Modulation
TPS	Triple Phase Shift Modulation
B2B	Back to Back Converter
DG	Distributed Generation
RMS	Root Mean Square
PCC	Point of Common Coupling

List of Symbols

$V_{dc,mv}$	MVDC voltage
$i_{g,mv}$	MV grid side current
C_{mv}	MVDC link capacitor
R_{mv}	AC/DC converter output resistance
L_{mv}	AC/DC converter output inductance
ω_{mv}	MVAC network angular frequency
$\theta_{g,mv}$	Phase angle of MVAC network
$v_{c,mv}$	AC/DC converter output voltage
$v_{dc,lv}$	LVDC voltage
$k_{mvdc,p}$	Proportional gain of AC/DC DC voltage control loop
$k_{mvdc,i}$	Integral gain of AC/DC DC voltage control loop
$k_{i,mv,p}$	Proportional gain of AC/DC current control loop
$k_{i,v,i}$	Integral gain of AC/DC current control loop
Subscript d,q	d-axis and q-axis value
Superscript *	Reference of the value
Subscript max	Maximum value
Subscript min	Maximin value
Subscript 0	Initial value
C_{DAB}	DAB LVDC link capacitor
L_{DAB}	DAB Inductance
n	DAB MFT transformer ratio
$i_{L,DAB}$	DAB inductance current

P_{DAB}	Power through DAB
f_s	DAB switching frequency
φ	DAB Phase shift angle
D	DAB Phase shift ratio
v_p	DAB primary side H-bridge voltage
v_s	DAB secondary side H-bridge voltage
P_{in}	DAB instantaneous power output from primary side
i_{sst}	LVAC side inductance current
$v_{f,lv}$	LVAC filter voltage
$i_{g,lv}$	LV grid side current
C_{lv}	LVAC filter capacitor
R_{lv}	DC/AC converter output resistance
L_{lv}	DC/AC converter output inductance
ω_{lv}	LVAC network angular frequency
$v_{c,lv}$	DC/AC converter output voltage
f_{lv}	LVAC network frequency
k_p, k_i	DC/AC voltage controller parameters
P_{sst}	SST active power output
Q_{sst}	SST reactive power output
ω_g	LVAC network angular frequency
θ_g	Phase angle of LVAC
$\omega_{lv,gf}$	LVAC network angular frequency under grid forming operation
$\theta_{lv,gf}$	Phase angle of LVAC under grid forming operation
k_{qp}	Gain of SST reactive power droop control

k_p	Gain of active power and frequency droop control
k_{pp}	Gain of active power droop control
$k_{v,lv,p}$	Proportional gain of DC/AC voltage control loop
$k_{v,lv,i}$	Integral gain of DC/AC voltage control loop
$k_{i,lv,p}$	Proportional gain of DC/AC current control loop
$k_{i,lv,i}$	Integral gain of DC/AC current control loop
$i_{sst,comd}$	Active power compensation control d-axis current reference
$i_{sst,comq}$	Reactive power compensation control d-axis current reference
k_{pid}	Proportional gain of active power compensation control loop
k_{qiq}	Proportional gain of reactive power compensation control loop
k_m	Overload coefficient
$k_{\Delta mv,v}$	Proportional gain of active power limiting control loop under grid forming operation
$k_{\Delta mv,p}$	Proportional gain of active power limiting control loop under grid-connected operation

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Chapter 1 Introduction

1.1 Challenges in distribution network

With the increasing penetration of renewable energy, the integration of distributed renewable energies (DERs) in the distribution network is under consideration, which arises significant technical and economic challenges.

As illustrated in Fig. 1.1, the traditional distribution network is designed to convey electricity unidirectionally from transmission network at higher voltage level to end consumption at lower voltage level. The voltage is operated passively with limited control provided by on-load tap changer in transformers. Load conditions vary with respect to size and time but fairly predictable. Meanwhile, DERs integration in the distribution network needs to be actively managed, planned and maintained due to its nature intermittent and less predictability. Maintaining voltage stability and regulating power flow also become a challenge when dealing with DERs from multiple sources. Also, the massive connection of renewable energy requires the network with bidirectional power flow and thus higher short circuit contribution and fault levels, which will increasing the complexity of power flow control and optimisation. Moreover, increasing DERs integration introduces higher fluctuations creating serious power quality concerns in the distribution network. Power quality issues, like voltage fluctuations, flicker and frequency variations, could lead distribution network operation into converter interaction issues, resonances issues and harmonic instability.

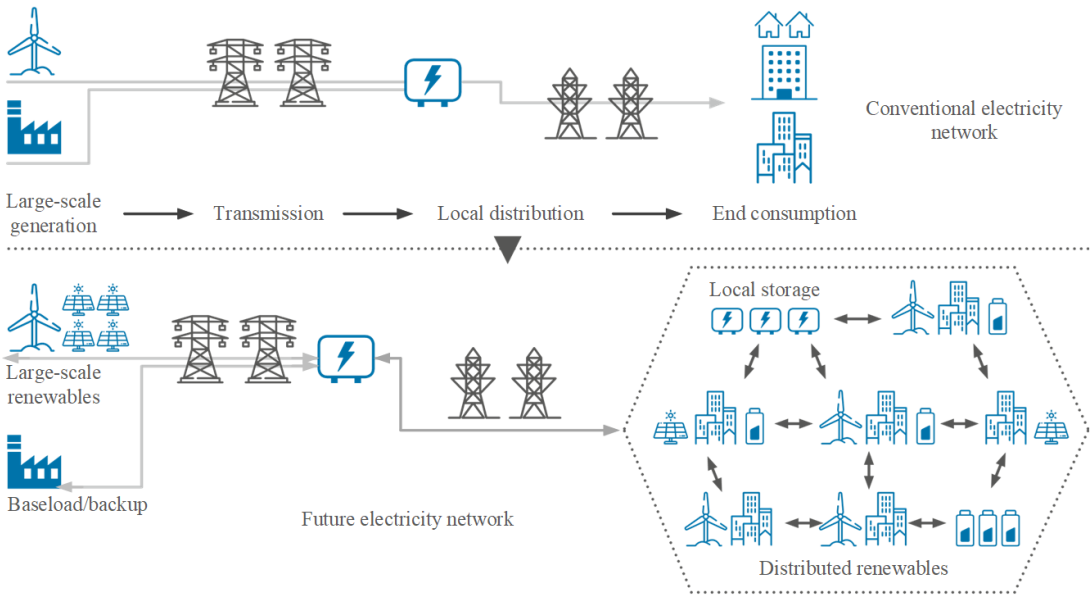


Fig. 1.1 Conventional electricity network versus future electricity network due to growing DERs integration.

Several solutions to tackle the issues have been proposed [1-6]. From the perspective of distribution network level, microgrids [1] and multi carrier energy system [3] are considered to enhance the hosting capability and energy management when considerable amount of DERs are connected. The current congestion and unintentional islanding problems can be alleviated. From view of network control, active network management (ANM) is used to continually monitor the network constraints and allocate the maximum amount of capacity to customers, which can potentially increasing the hosting capacity of the renewable energy in the network without upgrading [7]. From view of network planning, DERs power forecasting can is considered to improve power quality for considerable DERs integration[8]. But it is still under development due to the accuracy and computational efficiency issues.

From the perspective of device level, active filters, such as static synchronous compensator (STATCOM), static var compensator (SVC), unified power quality conditioner (UPQC), have been installed for harmonic filter and voltage regulation under different level of DERs integration [9]. Also, the dynamic voltage restorer (DVR) with

proper control scheme can compensate voltage sags and swells [10]. The two types of active filters can be installed in the existing network to maintain voltage stability and improve power quality[11]. However, advanced proper control is required as generate currents or voltages according to the reference signals with adequate accuracy, especially when it is working under distorted voltage. Also, reducing time delays in computing is highly demanded, especially if high accuracy is required in a wide range of output currents and frequencies. Furthermore, proper sizing and rating of active filters can be challenging. It requires accurate estimation of the harmonic content, reactive power, and load characteristics to determine the appropriate capacity. Undersizing may result in ineffective harmonic mitigation, while oversizing can lead to unnecessary costs [12].

Different from the exiting solutions, which can target one or some specific issues, the solid state transformer (SST) provides a systematic solution to address all the above-mentioned issues at the same time and facilitate management of distribution network. Essentially, SST is a power electronic based converter which can achieve voltage conversion between medium voltage (MV) and low voltage (LV) level. Compared with conventional distribution network, SST-based network provides connection interfaces of AC and DC network, which can potentially increase the hosting capacity for DERs integration and achieve power flow regulation between AC and DC network. Also, various ancillary services can be provided to MV/LV network, which make it possible to increase the reliability of the network. More importantly, these upcoming services with fully controllability enable the SST-based network to more rapidly adjust resources to meet the evolving and unpredictable requirements from utility and customers.

1.2 Concept of SST

The SST, also known as smart transformer, is basically an AC/AC converter complex [13-15]. The basic concept could date back to 1970 [16], in which it named the topology as solid state power converter circuits. In 1971, a half-bridge SST using thyristors was

proposed and its equivalent circuit was provided [17]. For the next few years, although some researchers produced related prototypes, SST remained to be developed [13, 18, 19]. Its development was mainly limited by voltage and current ratings of power electronic devices as well as the lack of high-frequency isolation. In addition, the lack of application needs in distribution systems at that time also reduced SST demand.

With the increasing demand of renewable energy integration and the significant development of power electronics technologies in the past two decades, the potentials and needs to use SST in the electricity network become more abundant. Apart from achieving AC/AC voltage conversion as a replacement of the LFT, SST can provide ancillary services to electricity network, and DC connectivity at both MV and LV voltage levels. As a power electronics equipment, SST is fully controllable to the input and/or output electrical parameters [20]. Also, with the help of the isolated DC/DC converter, SST can provide fault isolation capability. In addition, SST enables the monitoring and coordination of multi-power electronics devices to optimise the operation objectives and higher level controllers [21].

SST was first used in the application of the next generation traction system by ABB due to the reduced weight and volume [22]. In recent decades, several SST related projects, especially in grid applications, have been developed in different countries, such as in China [23, 24], Switzerland [22, 25, 26], Germany[27-30], the United States [31-37] and the UK [14, 38]. The detailed review of the grid application of SST in terms of its functionality will be provided in the following sections.

1.3 Configurations of isolated SST

Many converter configurations that provide isolated AC to AC conversion can potentially suit SST application [13, 14, 35, 36, 39-65]. For ease of documenting the topologies, a classification of the known configurations is presented in Fig. 1.2 [19, 65], where four

SST configurations according to different conversion stages are classified, namely: (a) single-stage; (b) forward two-stage; (c) backward two-stage; and (d) three-stage SST.

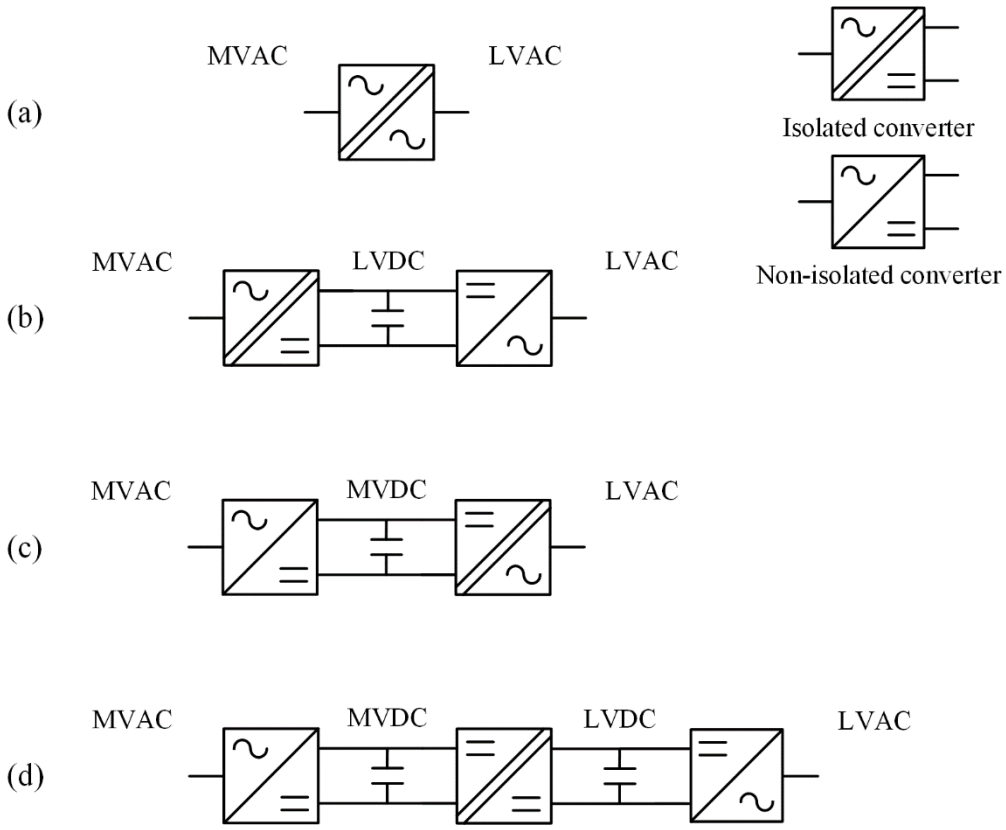


Fig. 1.2 Configuration of isolated SST according to conversion stages: (a) Type A: single-stage; (b) Type B: forward two-stage; (c) Type C: backward two-stage; (d) Type D: three-stage.

For the Type A single-stage configuration shown in Fig. 1.2(a), a direct step-down conversion from medium voltage AC (MVAC) to low voltage AC (LVAC) is achieved with an isolation transformer [43, 46-49, 62, 64, 65]. The SST topologies in Type A potentially achieve the minimum cost, highest efficiency and lightest weight option among all SST topologies because of the simplest structure and fewest conversion stage. A simplified version of Type A converter can be found in [43], and one module for the implementation of this topology is illustrated in Fig. 1.3. Wherein, the low-frequency sinusoidal input voltage is chopped to produce high-frequency wave which is then passed

to the secondary side via medium-frequency transformer (MFT). The high-frequency voltage is converted back into low frequency wave by the secondary side bridge circuit. The phase shift modulation is applied to achieve output voltage regulation. However, Type A configuration usually leads to high switching loss and has limited functionalities compared to the three-stage topologies [65]. The simplified structure may give rise to higher requirement on various components compared with other types. For example, single stage SST must introduce four-quadrant power devices to achieve bidirectional power flow [46, 65]. Meanwhile, the application of this type is under higher restriction due to the lack of DC-link, such as the application of VAR compensation and soft switching [47, 64], and inability for integration of DERs, etc. The lack of DC-link will also increase the size of the filter due to generated large ripple currents. Moreover, Type A SST has no immunity to disturbances, which is the same drawback as a traditional transformer.

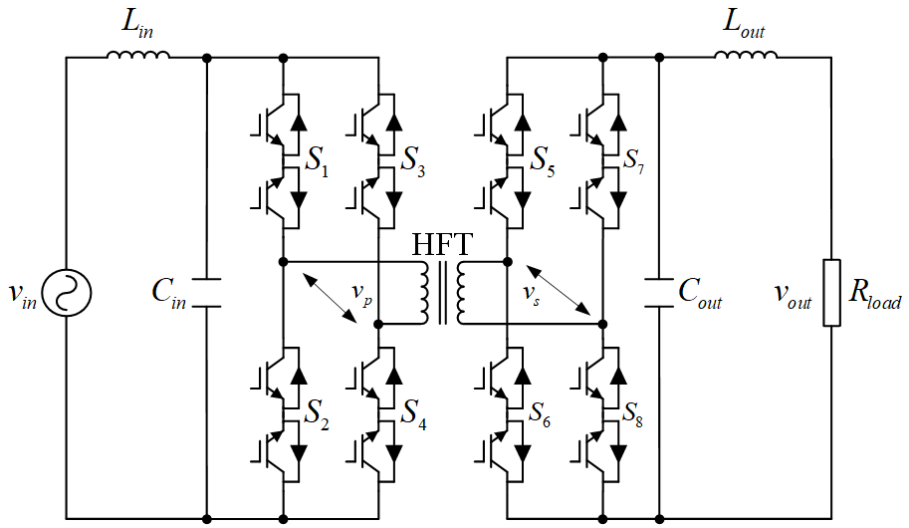


Fig. 1.3 An AC/AC converter for implementation of a single-stage SST topology.

In Type B, there are two conversion stages interconnected with an LVDC link [50, 52-55, 58]. For a Type B SST topology shown in Fig. 1.4, it consists of a single-stage isolated AC/DC converter and a DC/AC converter. The AC voltage at grid side is chopped to produce high-frequency AC voltage with a fixed 50% duty cycle. The chopped voltage is stepped down to high-frequency low AC voltage via HFT and is converted to LVDC by

H-bridge converter. The three-phase four-wire converter then converts the LVDC voltage to the requested AC output for the load side. Known Type B topologies are mainly applied in the traction system [52-55], while the LVDC link provides access to DERs and DC microgrid [66]. Similar to Type B, Type C also consists of two conversion stages. Wherein, an AC/DC converter is connected to MV side to produce a MVDC link, and an isolated single-stage matrix converter convert MVDC to LVAC [51, 57]. Additionally, the topology in [50] can achieve the configurations of both Type B and C due to the adopted two isolation transformers. Compared with Type A SST configuration, introducing a DC link in Type B and Type C enables VAR compensation application under certain topologies. However, the current distortion in the bidirectional single-stage AC/DC matrix converter is high especially with the discontinuous conduction mode (DCM). For that purpose, reference [67] proposes a symmetrical switching to reduce the total harmonic distortion of the phase current, but the soft-switching cannot be guaranteed in all the operation load regions as the instantaneous inductance current of the switching device is not high enough to the ZVS condition, so additional conduction losses are induced. In [68], it describes that the implementation of the single-stage AC/DC matrix converter can result in low efficiency (<88%) due to large circulating current.

In Type D, there are three conversion stages where both MVDC and LVDC links are present [13, 14, 35, 36, 39-42, 44, 45, 56, 59-63]. It can be considered as the most popular configuration since each stage of the SST can be considered independently to optimise the performance [39, 40, 61]. The three-stage SST configuration consists of one AC-DC power conversion stages, one DC/DC conversion stage and one DC/AC conversion stage, with a medium frequency (MF) isolation transformer. The existence of MVDC and LVDC links fill the gap of Type B and C SST configurations. The reduced weight and volume, compared to LFT, provide power conversion in weight/space limited application, such as in traction system [44, 56, 60, 69], nacelles of wind turbine[36], future navy warships and full-electric aircraft system. For application in power grid, Type D can provide full-range control scheme from input to output. The ancillary services, such as VAR compensation and voltage sag compensation, are available and achievable from Type D. Also, the LVDC

link provides a possible interface to low voltage DERs, energy storage system and DC microgrid, etc.

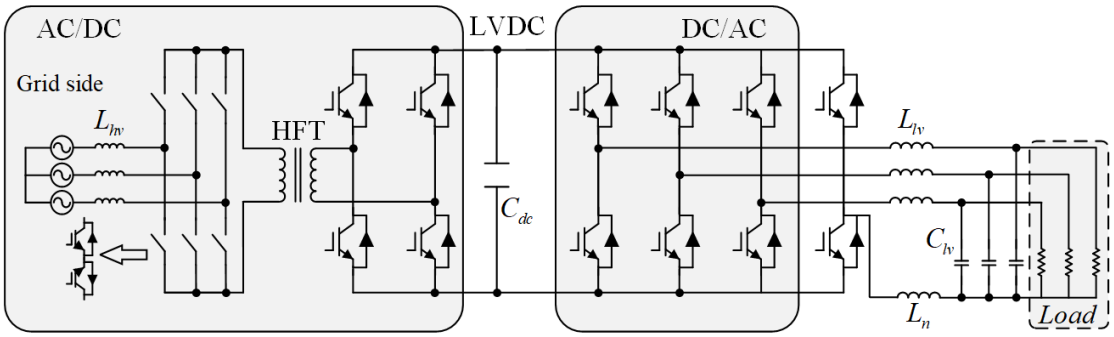


Fig. 1.4 An AC/AC converter for implementation of Type B SST topology.

Reference [65] compares the six types considering different converter topologies (i.e. half-/full- bridge, flyback and dual active bridge (DAB), etc). Wherein, the three-stage DAB based SST is considered as the best-performance topology in the six examined topologies. It is recognized that the limitation of type D SST are:

- The larger numbers of switching devices will increase the switching loss (at least three times higher than an LFT in the same power rating), thus lead to lower efficiency.
- The capital cost of Type D SST will be at least five times of an LFT for the same power rating.

Meanwhile, the level of modularity of SST needs to be considered for medium-power and medium-voltage applications. The three-stage SST configuration is classified as non-modular, partial-modular and full-modular, according to the modularity level, as presented in Fig. 1.5. Wherein, non-modular configuration is the composite of three converter. For partial-modular configuration, one possible configuration is implemented with modular DC/DC converter [70], shown in Fig. 1.5(b.1). In this configuration, the DC/DC converter modules are connected in series on the MVDC side and in parallel in the LVDC side. The

MV side converter may use multilevel converter, e.g., modular multi-level converter (MMC). The other possible configuration is implemented with the module of AC/DC and DC/DC converter [71, 72], shown in Fig. 1.5(b.2). The three-phase MV side is connected with three single-phase modular converters, while the basic module of the single-phase modular converter consists of an AC/DC and a DC/DC stage, where the cascaded H-bridge (CHB) is the preferred choice for the AC/DC stage. The modules are connected in series in the single-phase MV side and in parallel in the LVDC side. It is noted that the MVDC link is not available in the configuration.

For full-modular configurations, the basic module consists of an AC/DC, a DC/DC and a DC/AC stage. The modules can be connected via input series output parallel (ISOP, for input parallel output series will be the same in bidirectional SST application), input parallel output parallel, and input series output series, shown in Fig. 1.5(c). It is necessary to note that the full-modular SST configuration will make intermediate MVDC and LVDC links unavailable.

As the emphasis of the thesis is on control and operation of SST and its performance in distribution network, where Type D SST is selected due to its best-performance topology in terms of functionality. The capital cost and efficiency issue will not be considered in the thesis. To simplify the internal control at each conversion stage, the non-modular configuration is selected in this thesis.

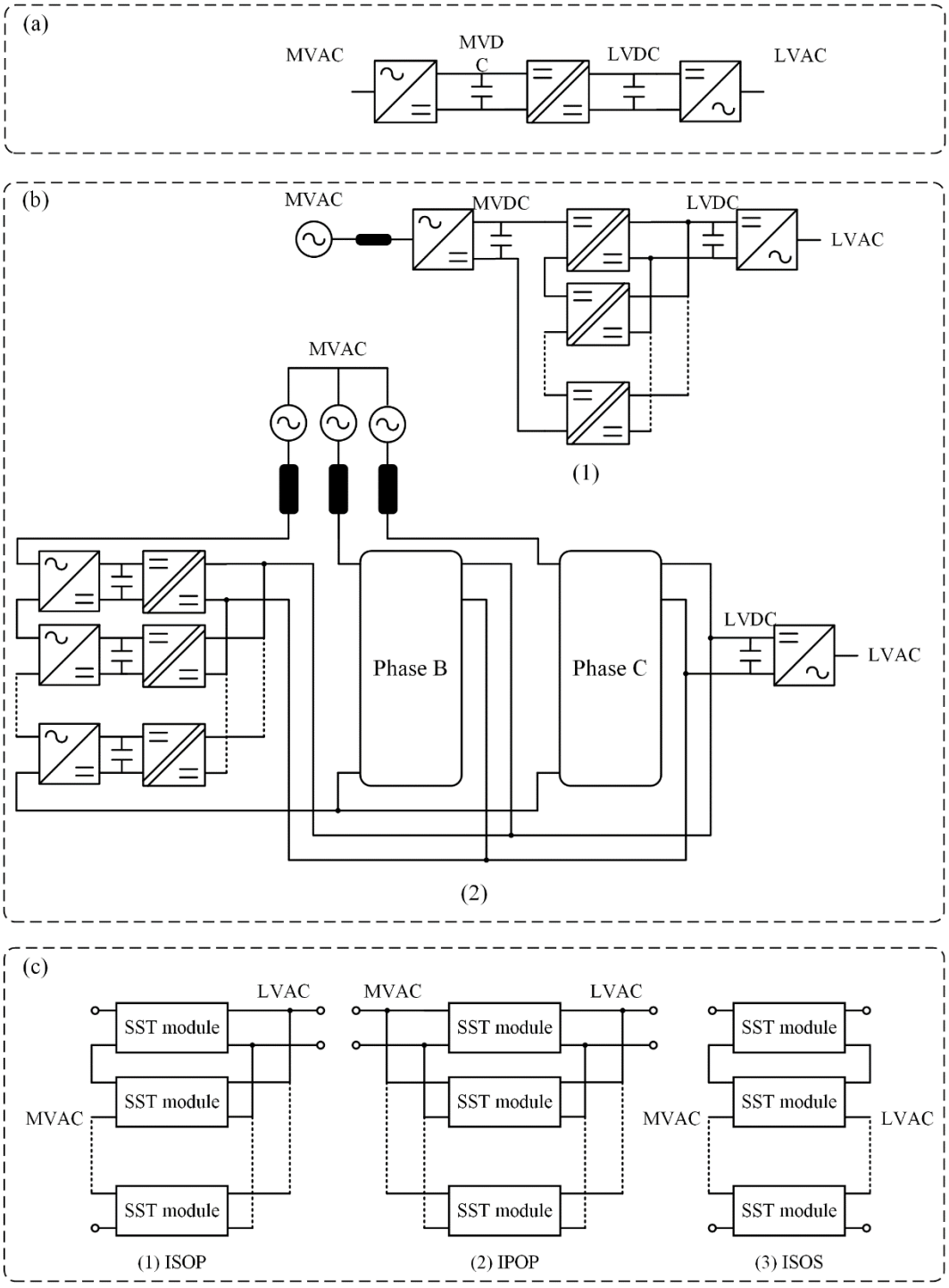


Fig. 1.5 Modularity of three-stage SST: (a) non-modular configuration; (b) partial-modular configuration: (b.1) DC/DC modular configuration; (b.2) AC/DC+DC/DC modular configuration; (c) full-modular configuration: (c.1) ISOP configuration; (c.2) IPOP configuration; (c.3) ISOS configuration.

1.4 Operation of SST in distribution network

The operation scheme of a three-stage SST is investigated in [35] and the control scheme is illustrated in Fig. 1.6. Wherein, the stage 1 converter is controlled to regulate MVDC voltage, while the stage 2 converter regulates the LVDC voltage. As the most commonly used topology of the stage 2 DC-DC converter is DAB, the phase shift modulation is normally chosen. The stage 3 converter operates as the grid-forming converter, where it regulates AC voltage and current to provide a stabilised AC supply to the LVAC load. The scheme can provide bidirectional power flow.

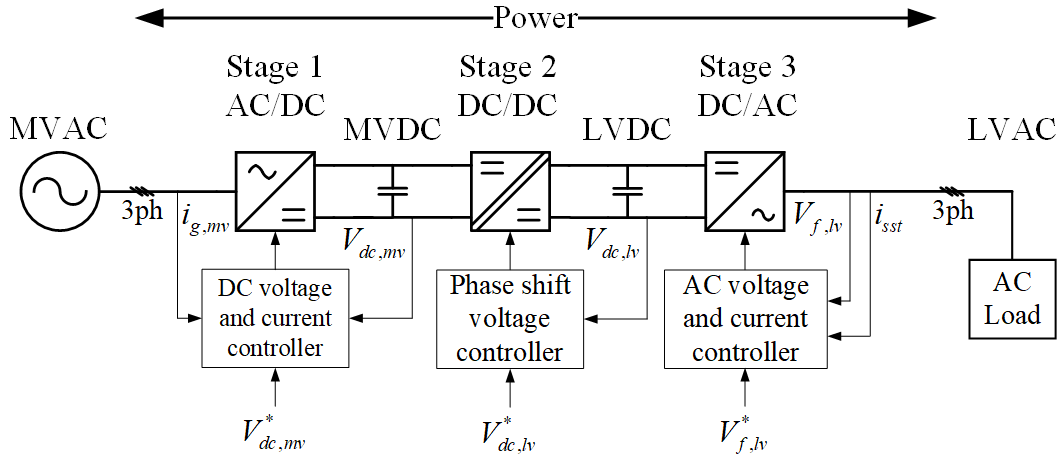


Fig. 1.6 Control scheme of a three-stage SST converter [35].

Considering SST connecting unbalanced loads at local customer side, the three-phase four-wire converter is adopted at Stage 3 converter [73-76]. An additional neutral current control loop is introduced in [73, 75, 76] to reduce the power oscillation, while a dual closed loop of proportional resonant (PR) plus P control is adopted for balanced and unbalanced loads in [74].

In addition to operating as a voltage source to LVAC network, the operation of SST under grid-connected mode is investigated in [77, 78], where SST is designed to connect the adjacent LVAC network with a conventional normally opened point (CNOP). When the

CNOP is closed, the power output is regulated by a direct current loop according to the references, as illustrated in Fig. 1.7(a). In [74] and [79], the $P-V$ and $Q-\omega$ droop control, widely used in microgrid converters, is deployed at the Stage 3 converter to generate power as requested, as illustrated in Fig. 1.7(b), while the control scheme of Stage 1 and 2 converters are the same as that in [35]. In [80], the $P-\omega$ and $Q-V$ droop control is deployed at the outer loop to regulate power output of SST, as shown in Fig. 1.7(c). Meanwhile, a PR controller is used as the inner current loop.

The control scheme can be slightly different with the schemes mentioned above when coordinated with DC integration. In [81], the operation of SST with centralised energy storage device (ESD) integration is investigated. Wherein, the MVDC voltage in SST is controlled at the Stage 1 converter and the LVDC voltage is regulated by the Stage 2 converter when power flow from MV to LV side, as illustrated in Fig. 1.8(a). When power is transmitted from LV to MV side, the MVDC voltage is control by the Stage 2 converter while the LVDC voltage is regulated by the DC/DC converter at the ESD side, as illustrated in Fig. 1.8(b).

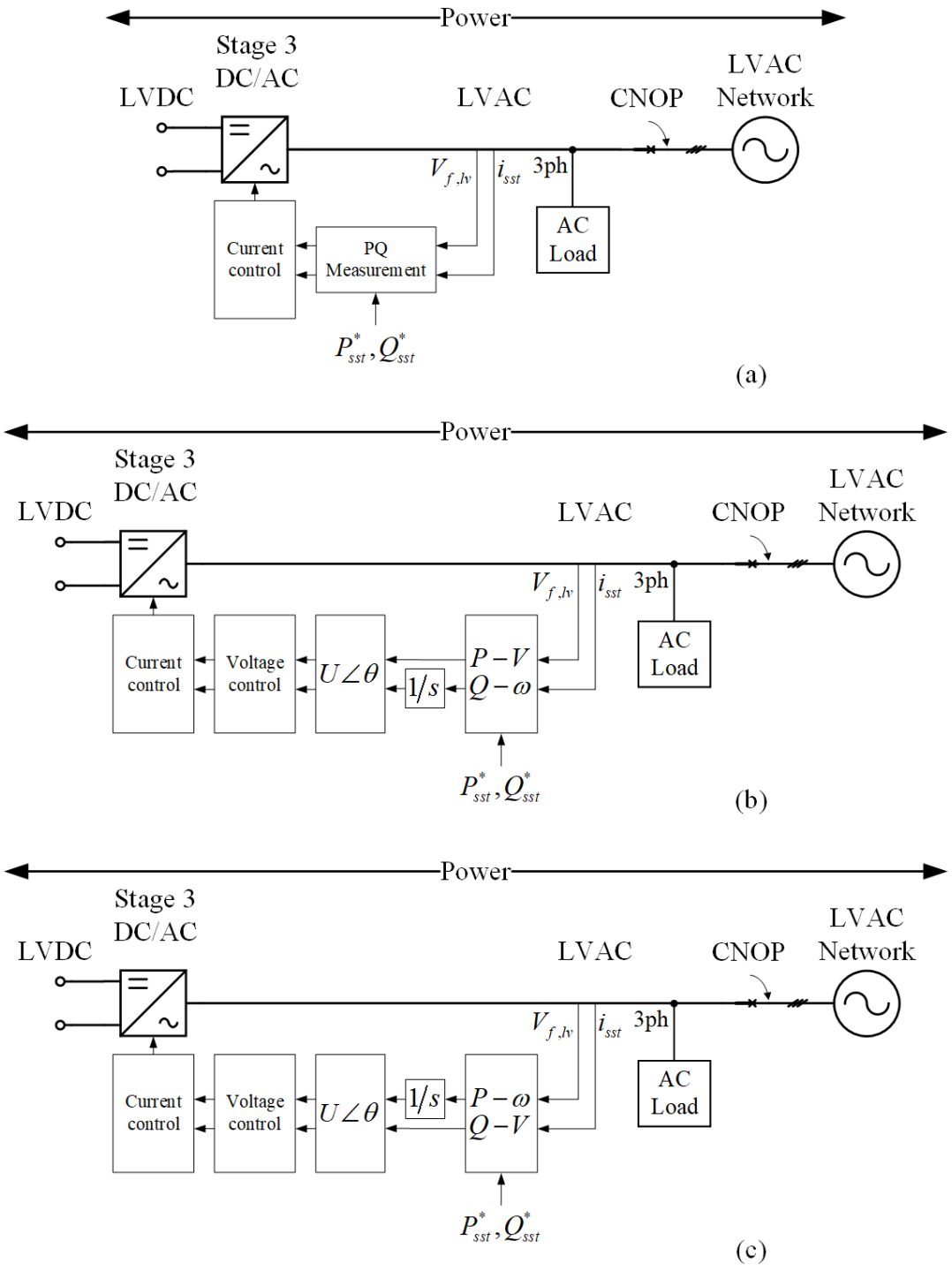


Fig. 1.7 Active and reactive power control scheme of SST under grid-connected operation: (a) Direct current control; (b) $P-V$ and $Q-\omega$ droop control; (c) $P-\omega$ and $Q-V$ droop control.

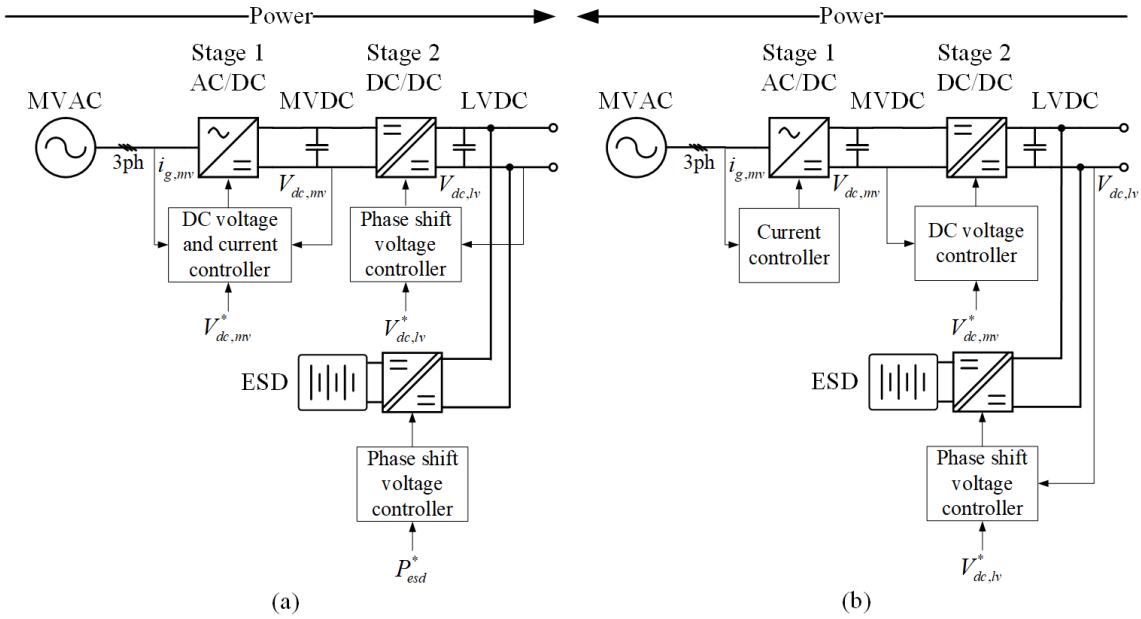


Fig. 1.8 Coordination control scheme of SST with ESD integration for Stage 1 and 2 while the Stage 3 converter is omitted for better readiness: (a) power flow from MV to LV side; (b) power flow from LV to MV side [81].

Furthermore, an SST-based voltage support controller is developed to provide reactive power support for MV side [29], as illustrated in Fig. 1.9. When voltage fluctuation occurs at MV side, a voltage support control strategy is proposed to inject reactive power to MV network to support the voltage. As seen, the MV side voltage is associated with reactive power reference at the MV interfaced converter using a droop controller. Meanwhile, in order to provide more reactive power support to the MV side under the ampacity of the MV converter, the MV side voltage is associated with d-axis voltage reference at LV side converter. The LV side power consumption is reduced by decreasing LV side voltage when considering voltage-dependent load condition. The LV side droop control is implemented by an online load control (OLLC) strategy, which is based on the voltage dependency of the aggregate load power consumption affected by the composition of the aggregated load and the loading conditions, such as weather, season or day-time. It needs to be noted that the range of MV voltage fluctuation in the paper occurs within the safety limit (e.g. ±10%), which means the fault conditions are not included.

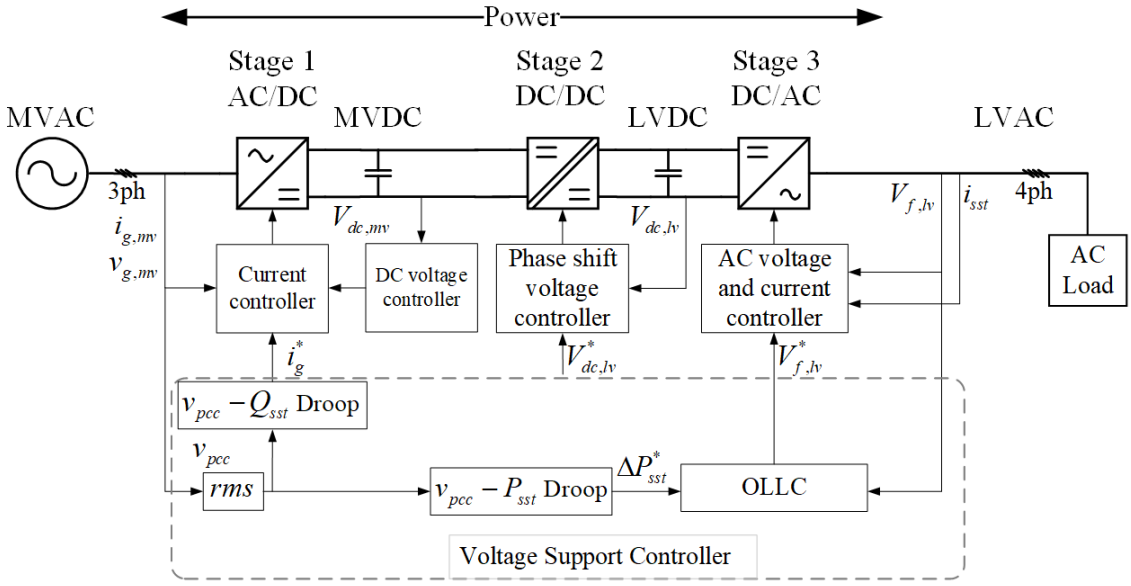


Fig. 1.9 Voltage support controller integration in the control scheme of SST through active power control [29].

In this subsection, the control and operation of each conversion stage of SST is reviewed. For DC/AC converter specifically, grid-forming and grid-connected operation is reviewed. Furthermore, additional coordination control among conversion stages and adjacent ESD are widely reviewed.

1.5 Application of SST in distribution network

SST can not only operate as a LFT to provide voltage change, but also feature a wide range of services, such as reactive power support, DERs integration, power quality improvement and fault isolation[15]. Subsequently, practical application of SST is reviewed to investigate the existing and potential scenarios in distribution network. SST can be considered a solution to meet the increasing demand of advance control and monitoring from the distribution network.

1.5.1 Replacement of a conventional power transformer

The primary SST application is to operate as a MV/LV distribution transformer. With the control scheme of the converter, SST can easily achieve the voltage conversion. Additionally, the DC/AC converter inside of SST can reshape the AC voltage waveform, so the output voltage can be in a near perfect regulation [82]. The output voltage can also be controlled to be free of power frequency harmonics, regardless of the input voltage quality [83]. In [14], a 300 kVA three AC ports SST was developed for interconnecting two 3.3 kV grids and one LV grid, to provide the flexible AC interfaces without requiring large LFT.

The first area for SST to be considered as the replacement of LFT was the traction system. In order to increase space for passengers and operation speed, the traction systems need to provide higher power but reduced weight and volume (higher power density). Meanwhile, the trains are fed by the catenary with different voltage rating from that in electricity network, with the 15 kV/16.7 Hz and 25 kV/50 Hz being the most commonly used railway power supply ratings in Europe [84]. As the power supply are mostly single-phase configuration, the traction system needs to tackle the issues of presence of the inherent 2nd harmonic ripple at DC link voltage [69].

The conventional LFT-based traction system is illustrated in Fig. 1.10(a), which consists of a back-to-back converter and an LFT. In a 15 kV/16.7 Hz locomotive, the LFT occupies about 15% of the whole weight [44]. To optimise the locomotive to maximum power density (2-4kg/kVA) for weight, size and cost reducing, the LFT are operated under heavily load condition and the efficiency is compromised to the range of 90-92% [69].

Meanwhile, the generalised SST-based traction system is illustrated in Fig. 1.10(b), where the LFT is replaced by a medium frequency transformer (MFT) embedded in the DC/DC converter. The MFT operating at a medium frequency which can reduce the weight, volume and cost of the transformer [44, 60]. Traction system suppliers, such as ABB [53,

56, 60, 85-87], Alstom [88, 89], Bombardier [44] and Siemens [55, 90, 91], have all investigated SST-based traction systems. The operating efficiency of SST-based traction system among the projects reach at least 96% [53, 55, 60, 92]. In [53], the proposed SST-based system achieves 50% less of the system weight and 20% less of volume compared to LFT-based solutions.

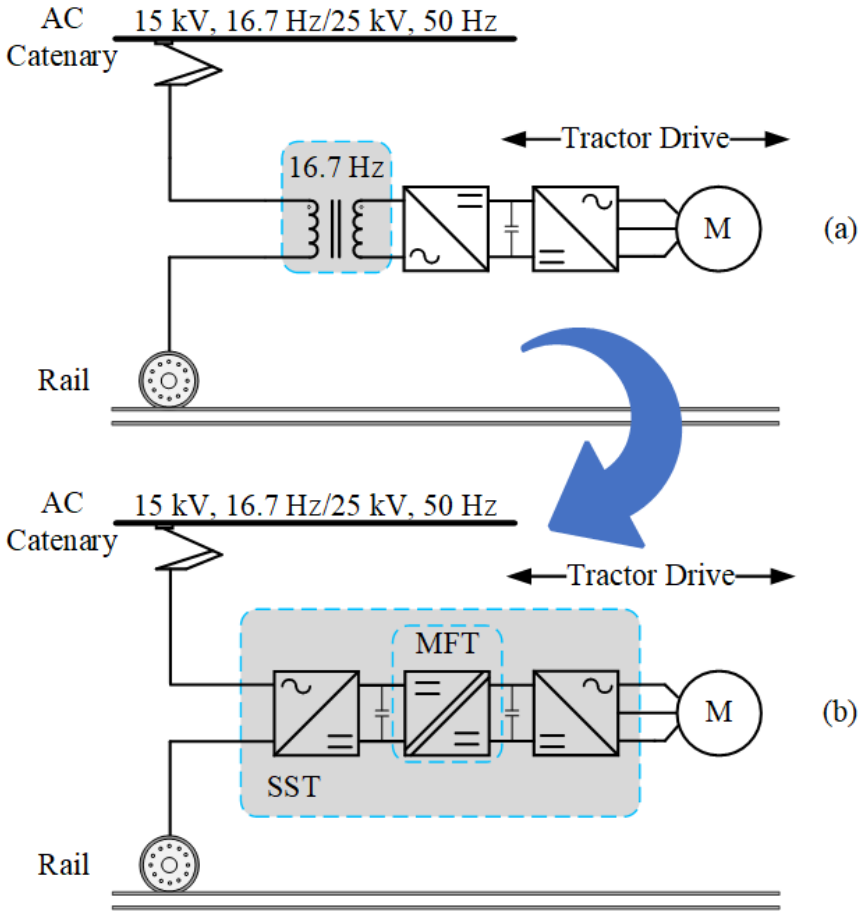


Fig. 1.10 Electrified traction system: (a) Conventional LFT-based traction system; (b) SST-based traction system.

Shipboard system is considered as another potential application for SST to replace the LFT transformer [93]. The application of SST in ship power network to perform MV/LV voltage conversion is considered in [94], though the practical application of SST in shipboard system has not been launched yet. However, it can be observed from [95, 96] that future electric shipboard systems using SST are under research.

Meanwhile, a detailed comparison between a 1 MVA SST and LFT in weight, volume, efficiency and costs are provided in [34]. It shows that at this stage the switching losses of the SST is at least three times higher than an equivalent LFT while the capital cost is over five times more expensive.

1.5.2 Reactive power compensation

Apart from voltage conversion, SST facilitates active and reactive power control (depends on the topology adopted). Reactive power can be compensated as required and the harmonics from the LVAC network can be isolated from the MVAC network by the DC stage [97]. Reference [98] provides case studies of SST application in distribution network on reactive power injection for voltage stabilisation in MV grid, while the detailed control scheme of reactive power support is proposed in [29], as described in Section 2.3. Also, SST can be potentially utilised as the dynamic voltage restorer behaving as an AC/AC controllable converter [99]. Wherein, a three-stage SST is implemented with direct parallel-connection at input stage while the output stage is series connected with the loads and provides demanded compensation voltage according to the DVR control signal. Compared with the conventional back-to-back structure, the input voltage step down transformer and coupling transformer at the output stage can be substituted by MFT, which can improve power density and reduce overall system volume.

1.5.3 DERs integration

With the increasing integration of distributed energy generation and energy storage systems, the various AC/DC and/or DC/AC conversion stages for accessing to the network are increasing. The integration of these AC and DC distributed resources can affect the system efficiency and complicate the system coordination [100]. Meanwhile, SST can provide DC access at the DC link (depends on the topology adopted.), and become energy routers to connect AC and DC sources and loads [15, 35]. The normal operation of an

SST-based hybrid microgrid is investigated in [35]. The DC microgrid is directly connected with the LVDC link while the AC load is considered at the LVAC side. In [27], the SST-based meshed hybrid microgrid architecture is proposed. Compared with DERs integration at LVAC side, an additional pathway between SST-LVDC link and DC bus of DERs is established, forming an outer interconnection loop between LVAC and LVDC. In the study in [15], it is observed that the power through LVDC line in the proposed system only has 22% power losses as that of the LVAC line. The system efficiency is increased by 6% when reverse power flow operation is achieved via the LVDC link connection compared with the connection through the SST DC/AC and DERs interfaced AC/DC converter. In [101], ESD is integrated in SST on either MVDC or LVDC bus by a DC/DC converter. The performance of the SST-based network considering normal and fault conditions are studied, which show that the integrated ESD can contribute to energy management of SST especially when the MVAC network is out of service due to the fault.

1.5.4 Fault isolation and current limiting

Being a power electronics converter, the lack of robustness compared with LFT is a common criticism of SST [102]. However, SST with its active control can potentially limit fault current contribution and isolate the faulty part from the healthy side of SST under normal operation [33]. Meanwhile, a current limiting strategy can be implemented to regulate the behaviour of SST before, during and after symmetrical/asymmetrical fault conditions according to the grid code requirements [103].

1.5.5 Existing pilot SST project

Early SST projects were developed in locomotive industry as SST has an obvious advantage on applications with strict weight and volume limits. Reference [104] reviews the detailed specifications, including topology, control, design parameters and efficiency, of existing locomotive projects from GE [42], Siemens [91], Bombardier [44], Alstom

[89], ABB [60, 105] and ETH [106]. In recent years, SST applications in distribution network have been widely analysed. Several projects, including UNIFLEX-PM [14], FREEDM GEN I-IV [32, 41, 107, 108] and HEART [27] have been proposed and developed according to different features. This section briefly introduces the features of these pilot SST projects and their purposes.

UNIFLEX-PM

The universal and flexible power management (UNIFLEX-PM) was a European funded project led by University of Nottingham, which provides a flexible and modular power electronic interface that is able to connect different kinds of sources and loads including MV electrical networks, RES, and energy storage systems, without requiring line frequency transformers [109]. The configuration of the system is illustrated in Fig. 1.11. Wherein, a three-port, type D full-modular SST is considered, while the rated power of the system is 300 kVA. Port 1 and Port 2 are both rated at 3.3 kV and used for RES integration and MV network interface, while Port 3 is rated at 0.4 kV and used mainly for ESD integration and/or LV network interface. However, as UNIPLEX-PM takes IPOP configuration with cascaded H-bridge for each phase design, a common DC link is not available. The control schemes of the three ports are all under grid-connected mode, which limits its application where SST is needed as the grid forming converter. Moreover, UNIFLEX-PM uses IGBT with 5 kHz operating frequency, and thus the efficiency and power density of the system are not competitive compared with LFT.

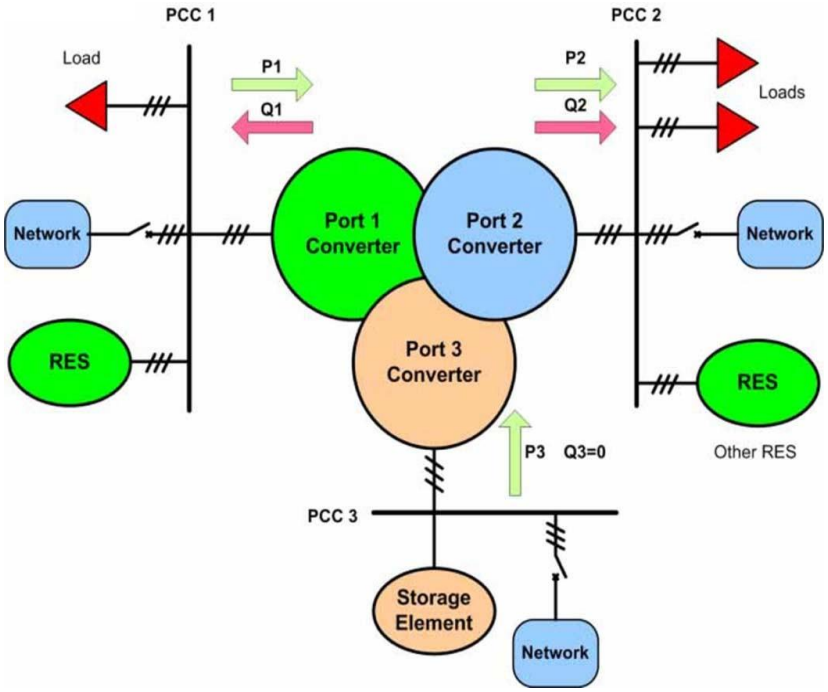


Fig. 1.11 Functional diagram of the UNIFLEX-PM system [109].

FREEDM

Future renewable electric energy delivery and management (FREEDM) system is a NSF-funded ten-year project led by North Carolina State University to renovate existing power system with high DERs integration and ESDs [110]. In the developed system, SST is considered as the key element for the interface between MVAC, LVAC and DERs. The four generations of SST in the FREEDM project all consider Type D, partial-modular configuration, which has been illustrated in Fig. 1.5(b.2), and the detailed topology (per phase) of GEN-I is illustrated in Fig. 1.12 as an example. For the interface of MVAC, the AC/DC and DAB are ISOP connected, and provide one LVDC link. The DC/AC converter then interfaces the LVAC network. The designed GEN-I SST shows fully control of voltage and power among the existing 7.2 kV MVAC distribution system, 240 V LVAC network, 400 V DC microgrid and smart loads [35]. In Fig. 1.13, the four generations of SST in FREEDM are briefly described. GEN-II SST improves the system efficiency from 88% in GEN-I to 96%, though it cannot achieve bidirectional power flow as the MV side uses a diode rectifier. Gen-III uses 15 kV SiC switch connection to produce 7.2 kV AC

and improve the system efficiency further to 97.5%. However, Gen-III SST has no capability to control the power factor of MVAC network, and there is no DC integration due to the single-stage conversion. Moreover, LVAC (240 V) is not controlled in Gen-III SST because of the fixed frequency operation of the resonant converter. Gen-IV SST enables bidirectional power flow, DC microgrid integration and LVAC regulation serving as a smart node in distribution network while maintaining the high efficiency as Gen-III (97.5%).

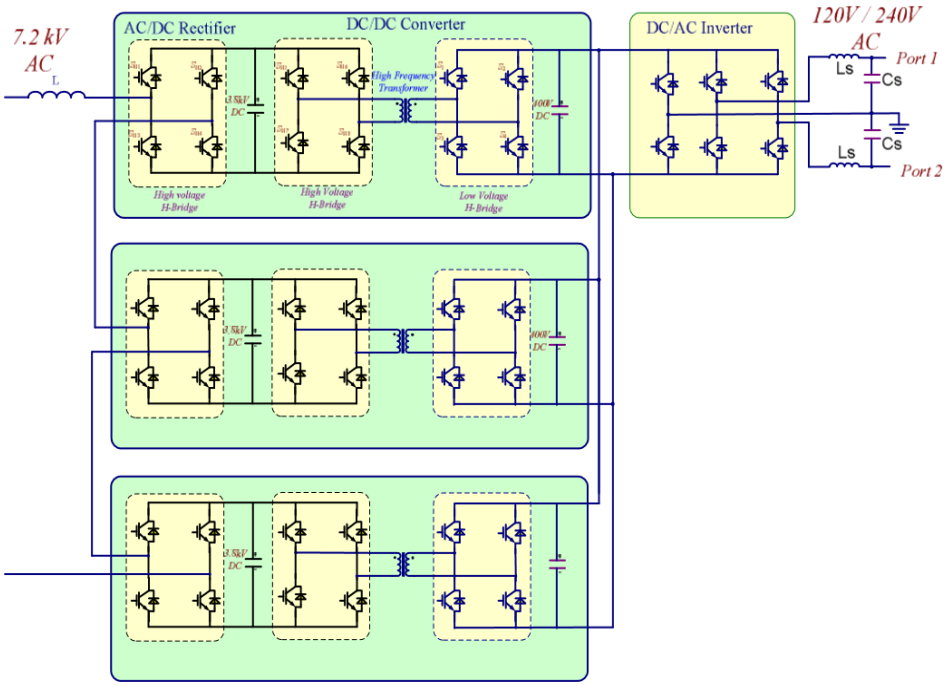


Fig. 1.12 Topology of GEN-I SST in FREEDM project [111].

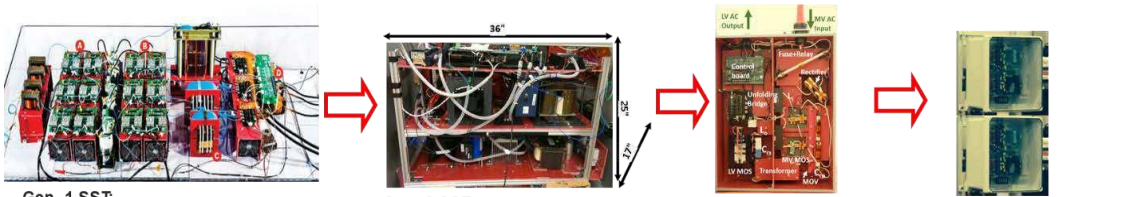


Fig. 1.13 Four generations of SST in FREEDM project [111].

HEART

The highly efficient and reliable smart transformer (HEART) is an European Research Council-funded project led by University of Kiel to investigate the capabilities (power quality enhancement, DC connectivity, ESD integration and fault reclosing coordination) of SST. The topology in HEART uses Type D, non-modular SST, as shown in Fig. 1.5(b.2). Wherein, the AC/DC conversion stage uses MMC converter to provide 10 kV MVDC, while the DC/DC conversion stage considers the quadruple-active-bridge (QAB) for better efficiency and lower cost [112] while providing a 0.8 kV LVDC link. The DC/AC conversion takes a three-phase four-wire converter configuration to connect with LVAC network considering unbalanced load condition [75]. Based on that, the project considers the SST performance when different types of fault occur at the SST-fed LV distribution network [73, 76] and its continuous operation under single-phase fault at the LVAC network [113]. The project also investigates grid services brought by SST, including ESD integration and coordination operation [114], primary frequency regulation [115], MVAC voltage support [29] and reactive power compensation [98].

LV Engine project

The LV Engine project is an innovation industrial project led by ScottishPower to carry out a network trial of SST in the UK. However, the topology demonstrated in the LV Engine project is a 500 kVA back-to-back converter at secondary side of 11/0.4 kV LFT, where a 150 kW, 800/900 V DC/DC converter is parallelly connected to the LVDC link [116, 117]. As the voltage step-down is achieved by an LFT in the LV Engine project, the project has limited relevance to SST. So, the details, including the objectives and case studies of the project will not be included in the section.

In this subsection, application of SST in distribution network is widely reviewed. Wherein, SST can achieve voltage regulation and functionally replace LFT in the reduced weight and volume application, such as traction system. Meanwhile, the capital cost, efficiency and robustness can be challenges compared with LFT. Also, reactive power compensation, DERs integration, fault isolation capability can be potential application

that SST can achieve. Furthermore, existing SST projects in the world is widely reviewed. In the thesis, the replacement of LFT in distribution network, DERs integration and fault isolation capability are the main applications under consideration.

1.6 Existing issues to be solved

Based on the review, some existing issues which have not been well addressed are discussed in this section.

1.6.1 Control issues

Existing control schemes of DC/AC converter in SST are only designed for either grid forming or grid-connected operation [27, 79, 81]. Under grid forming operation, the SST DC/AC converter provides stabilised AC supply to isolated LVAC network with defined voltage and frequency. Under grid-connected operation, the DC/AC converter follows the voltage and frequency from the connected LVAC network and regulates SST's active and reactive power output. On the other hand, the conventional normally open point (CNOP) is widely implemented in distribution network to achieve network reconfiguration between radial and ring topologies. CNOP helps to distribute the load power demand among the feeders and can significantly improve the appliances overload condition and feeder voltage profile [118]. When CNOP reconfigures the network from radial to ring topology with one side supplied by SST, SST should switch its control scheme of its DC/AC converter from grid forming to grid-connected operation. The control mode switch has been widely investigated in microgrid [119-124]. Wherein, a voltage-based droop (VBD) control that is capable of operating in islanded mode and in grid-connected mode was considered in [123]. An additional synchronization procedure is also proposed in the VBD control strategy which is required for the transition to grid-connected operation. The main drawback of the proposed control scheme is the import and export of power from the microgrid cannot be regulated. In [124], two individual control schemes for islanded and grid-connected operation are considered, where current loop only is for

islanded mode while voltage and current loop are for grid-connected mode. Under this case, the synchronisation procedure must be needed. Also, the proposed control can only have control on the total power flow between the converter-connected microgrid and the external grid and not individually for each DG unit. A more specialized control that act separately on the converters would be needed to optimize the power flow inside the microgrid and with the external main grid. In [119], $P-\omega$ with fixed voltage amplitude reference is for islanding mode, while $P-\omega$, $Q-V$ droop are for grid-connected. The major concern that droop-based controller presents is regarding the dynamic performance issue of the controller, such as coupling issue. In general, finding a suitable control scheme for DC/AC converter to accommodate conditions when the LV side operates as an isolated network or grid connected to the adjacent network (through the CNOP) is a challenge.

Furthermore, when considering droop-based controller, most of the control schemes at DC/AC converter under grid-connected operation are $P-Q$ outer loop to regulate power and inner voltage and current control [74, 79, 81]. However, this droop-controlled scheme has active and reactive power coupling issue (i.e., the interaction between the active power loop and the reactive power loop) since the high R/X ratio of line impedance in LV microgrid [125]. As a result, the dynamic performance of the system and the active power delivery capability can be degraded and restricted [126]. In [79], the control schemes of DC/AC converter in SST under grid forming and grid-connected operations are adopted separately, while the $P-V$ and $Q-\omega$ droop controller are adopted outside the dual inner controllers to regulate power output. A 20% variation of the active power output is illustrated in the simulation results when a 0.4 pu change of reactive power output is applied.

In order to deal with the inherent active power coupling issue, a number of improved droop control methods have been proposed, including virtual impedance-based [127-131], virtual power-based [132, 133] and virtual frequency- and voltage-based [134] decoupling methods. The most widely adopted method is the virtual inductor method due to its clear

physical meaning and easy implementation [128]. In the method, a virtual impedance loop is implemented to modify the equivalent output impedance of the inverter to be predominantly inductive. However, it is challenging to design the virtual impedance value without high complexity while maintaining good system dynamics and stability [132]. The virtual power-based control scheme is also widely recognized, which can decouple the power by rotating the power vectors with the impedance angle [132, 133]. The virtual active and reactive power are related to the frequency and voltage amplitude, respectively without coupling to each other. Droop control is then adopted in the virtual frame to ensure the virtual power being shared. However, this method cannot guarantee the sharing of actual power if the distribution line impedance angles of each inverter are different. The virtual frequency- and voltage-based decoupling method is an analogue of the virtual power-based decoupling method [134]. However, reference [134] does not provide a mathematical derivation to prove that the power flows are decoupled in the virtual frequency and voltage frame. In summary, the aforementioned decoupling methods for inverters in are either complicated or not intuitive. Therefore, it is necessary to further study the power decoupling methods and design a power decoupling control applicable for the SST DC/AC converter under grid-connected operation.

1.6.2 Postfault operation issues

The applicability challenge of SST in distribution network in terms of efficiency, compatibility and cost compared with LFT has been investigated in [26]. SST as a power electronics device can typically only withstand about 1.2-1.5 times rated overcurrent within one second, which is much lower than LFT delivering up to 25 times their rated current for at least two seconds [26]. Also, the overvoltage capability of LFT caused by lightning strikes or switching action are much more robust than SST. As a result, if implementing an SST directly in the existing distribution network, the external overcurrent fault could easily reach the overcurrent limit of SST before protection (or even detection) operates, which decreases the reliability of SST and introduces unnecessary power outage to distribution network [102]. Thus, to start with, it is important to

understand the postfault performance of SST and the postfault performance difference between LFT and SST. It will also be beneficial for further improving postfault performance of SST and designing compatible protection scheme for SST.

Meanwhile, the proactive control of SST under postfault operation are yet to be fully explored. Most research works conducted concentrate on how to protect SST from the fault, such as converter blocking and fault-ride through (FRT) strategy, which have been widely considered in converter control [102]. Meanwhile, from the view of replacing LFT, SST need to avoid unnecessary power outage during the fault to fast recover its power supply. the existing FRT are not sufficient to secure the power supply for SST. Also, the existing FRT may not be able to avoid unnecessary power outage of SST. In [78], an FRT strategy of SST is demonstrated to avoid the disconnection with MV network. But SST with the proposed FRT strategy can still activate converter blocking as the overvoltage and undervoltage of the internal MVDC and LVDC links during external faults are not considered. Disconnection is still possible under the case. Thus, it will be a challenge to develop a control scheme to keep SST under operation during external faults while avoiding the activation of converter blocking.

1.6.3 DC integration related issues

One of the benefit SST can bring to distribution network is DC integration via its internal DC terminal. In [21], a concept that the SST is considered as an energy router to connect AC and DC network is proposed, where SST forms a DC microgrid and powers DC loads directly. As PV and ESD can be directly connected to the DC microgrid without additional AC/DC conversion stage, SST-based network can potentially benefit system efficiency. However, most research on DC network integration by SST concentrated on the access providing for both LVAC and LVDC network [35, 81, 101]. The adaptive coordination among SST, LVAC network and LVDC network has yet been investigated. For example, power sources in the LVDC network are able to supply the LVAC network when the

upstream MVAC network via SST has limited power available, and this adaptive power flow transfer can be bidirectionally achieved. Existing coordination control has been found in DC microgrid and multi-terminal HVDC system (MTDC), where the concentration is to limit DC voltage variation. In DC microgrid, the coordination control is aimed to achieve a fast and balanced DC power distribution by multiple dominant stations according to a given slope relationship between DC power and DC voltage [135]. In MTDC system, the DC voltage-AC power droop control at the same HVDC station is developed to allow a smooth transition from the current operating point to a new steady-state operating point when the transmitted power changes or when a converter station is out of service or at fault [136]. The adaptive coordination control scheme for securing AC power supply has not been found. Also, either the different terminals in MTDC system or the generator/storage etc in the LVDC network can locate differently from SST. The response time delay of the existing coordination control is dependent on communication, which can introduce large transient to the network [35, 81]. Further research on coordination control without communication is required.

Meanwhile, introducing additional DC network/connection to SST can introduce DC faults. Most researches consider the LVDC network is directly connected with the LVDC link in the SST [35, 81, 101], while a fault occurred at the LVDC network can cause the DC link voltage to collapse and potentially, power outage spreads to any connected device of the SST, including the LVAC and MVAC sides. Therefore, to improve the reliability of the SST under the DC fault, the configuration of DC integration in SST need to be assessed.

Furthermore, the fault characteristics, protection scheme and postfault operation of SST under DC fault need to be properly addressed. In HVDC systems, it is widely considered to block converters for short period of time while circuit breakers operate to clear the DC fault and resume operation afterwards [137]. This protects semiconductor device from overcurrent maintain DC voltage for fast recovery. However, the coordination between converter blocking strategy with the external protection scheme of SST has yet been

investigated, which is important to prevent SST from unnecessary blocking and consequent power outage due to DC fault. Also, the effectiveness of protection device (i.e. DC circuit breakers) for SST-based hybrid network also requires further assessment for fast DC fault clearance, while further investigations are needed for performance comparison among different types of DC circuit breakers.

1.7 Research scope and contribution

1.7.1 Research motivation and objective

SST is considered as a promising solution to benefit the network management and increase the hosting capacity of renewable energy. It can also provide ancillary services without additional devices. But existing control scheme of SST can only be applicable under certain operation (grid-forming/grid-connected operation). The universal control scheme for various operation is under development, which can increase the flexibility of SST.

Meanwhile, SST is hindered from replacing line-frequency transformers (LFT) in distribution network due to the issues like expensive cost, less efficiency, incompatibility with existing protection scheme and less robustness than LFT [25, 102]. Subject to the power electronic component development, SST has inherent disadvantages as mentioned above since most efforts on SST have been made only in recent few years. On the other hand, potentials of SST have not been fully developed yet. As power electronic device can only withstand limited overvoltage and overcurrent, the fault current contribution of SST can potentially less than that of LFT, which detailed comparison have not been taken yet. Compared with other multi-stage converter (such as HVDC system), SST can achieve almost no-delay communication among each conversion stages, which improves its reliability and flexibility by coordinated control.

Therefore, this thesis will investigate the modelling, control and operation of SST in distribution network, with aiming at maximising proactive control of SST to increase the reliable and flexible operation during both normal and fault conditions. A suitable universal control scheme is thus developed for normal operation and several additional control schemes are developed to increase the reliability of SST under postfault conditions. Also, the control and operation of SST-based hybrid network will also be explored.

1.7.2 Thesis contributions

The main contributions of this thesis are:

- A universal control scheme for SST is proposed for grid-forming and grid-connected operation, which enables SST to operate flexibly in the distribution network. An additional compensation control using active and reactive power feedforward compensation to dq-axis current components of the DC/AC converter is further proposed to reduce the coupling between SST active and reactive powers without affecting overall system response.
- The performance comparison between LFT and SST during network faults are investigated. Fault limiting method of SST during fault conditions is analysed. The additional active power limiting control schemes for SST under both grid-forming and grid-connection operation are proposed. SST can remain normal operation after fault occurrence avoiding unnecessary converter and recover power supply once the fault is cleared.
- An adaptive droop control is proposed for SST to continue supplying the LVAC network during MVAC faults, which balances the power flow between the AC and DC networks dispatched by SST and eliminates the voltage variation. As the integrated ESD may not be at the same place as the SST, a strategy which modifies SST LVDC output voltage according to the variation of MVDC voltage, is

proposed, so as to enable the ESD to control its power output according to the connected LVDC link voltage.

1.7.3 Author's Publications

[1] **T. Zhang** and L. Xu, " Grid forming control for solid-state transformer operating in islanding and grid connected conditions," The 11th International Conference on Power Electronics, Machines and Drives (PEMD), 2022.

Abstract: Solid-state transformer (SST) has recently been considered as one of the key components for future distribution networks with enhanced controllability and operating flexibility. This paper proposes a universal control scheme for SST's low voltage DC/AC converter such that the same grid forming control structure can be used during both islanding operation and grid connected state to the adjacent feeder through the normally open point (NOP). This ensures smooth transition between different operation states without the need for control mode switching. To reduce the coupling between active and reaction power, an additional compensation control using active and reactive power feedforward compensation to dq-axis current components of the DC/AC converter is proposed. Simulation results are provided to confirm the overall SST performance and effectiveness of the proposed control schemes during power reference changes when the SST is operated in grid connected mode through the NOP.

[2] **T. Zhang** and L. Xu, "Enhanced control of solid state transformer with LVDC port and energy storage during network fault for continuous power supply.". (under preparation.)

Abstract: In SST-based hybrid network, the continuity of the power supply is affected by external faults. In the case of network fault at MV side, power imbalance can lead to large deviation of MVDC voltage and the blocking of the SST, which can delay the recovery of

the power supply to the LV side after fault clearance. In order to maintain SST operation and prevent it from unnecessary blocking, this paper proposes an active power limiting control for SST under both grid-forming and grid-connection operation by reducing the LVAC side voltage to curtail the load/generation. A coordination P-V_{dc} droop control is also proposed for a SST-based hybrid AC/DC network containing a LVDC port to ensure continuous power supply during MVAC fault. By regulating the power from the ESD which is connected to the LVDC network based on the variation of either the MVDC or LVDC voltage, the power supply to the LVAC network can be maintained during MVAC faults. Finally, the effectiveness of the proposed scheme is verified in the network model built in MATLAB/Simulink.

1.8 Thesis organisation

This thesis is organised as follows:

Chapter 2 presents the basic control scheme of the three-conversion stage SST under grid-forming operation, including voltage control, current control. MATLAB/Simulink simulations are then carried out to tune the proposed controller and verify the effectiveness of the proposed control scheme.

Chapter 3 proposes a universal control scheme for SST's Stage 3 DC/AC converter, where the control structure is developed under both grid-forming and grid-connected operation. SST is applied in the test distribution network with the co-operation of the conventional normally open points (CNOP). To reduce the coupling issue between active and reaction power, an additional compensation control using active and reactive power feedforward compensation to dq-axis current components of the DC/AC converter is proposed. Simulation results are provided to confirm the overall SST performance and effectiveness of the proposed control schemes.

Chapter 4 investigates the control and performance of SST during the network faults. In order to compare SST and LFT, a series of case studies are considered to investigate fault performance of SST under grid-forming and grid-connected operation in different network configurations. In order to prevent SST from unnecessary blocking during large MVDC voltage fluctuation due to MVAC faults, which can lead to active power unbalance between MV and LV sides of the SST, an active SST power limiting control is proposed where the MVDC voltage variation directly sets the d-axis voltage (during grid-forming operation) or the active power output reference during (grid-connected operation) of the LV side converter. Various case studies are carried out in MATLAB/Simulink to validate the effectiveness of the proposed control and operation during different fault locations and SST operation modes.

Chapter 5 investigates the potential of introducing DC network to SST-based distribution network. A coordinated control of selected the SST and the DC network is proposed for optimising the operation of the SST-based hybrid AC/DC distribution network. With linking MVDC voltage with power output of the DC network, the SST enables the adjacent ESD providing needed power to ensure the power supply to the load side autonomously. Considering the scenario where the ESD is far from SST, the LVDC link voltage connected with DC network is linked with MVDC voltage to achieve adaptive power regulation of the ESD. In addition, the DC fault characterisation and fault clearance requirement of the proposed system is reviewed and analysed. The effectiveness of different fault clearance schemes on SST under DC fault is verified by simulations in MATLAB/Simulink.

Chapter 6 draws the conclusions and provides the future work.

Chapter 2 Control of Solid State Transformer

In this chapter the basic control of SST will be described. A three-conversion stage SST, including an AC/DC converter, DC/DC converter and DC/AC converter, is considered in this thesis. The overall configuration is shown in Fig. 2.1. Wherein, the control scheme of a three-conversion stage SST is under assessment. The details of the basic control strategies are provided in this chapter and the performance of the SST-forming network is assessed in MATLAB/Simulink.

2.1 System control of the SST

The overall control scheme of the SST is shown in Fig. 2.1. For the stage 1 AC/DC converter, it is designed to regulate MVDC voltage and its control is similar to that of a VSC HVDC transmission system [138]. To simplify the internal control loop, two level AC/DC converter is selected to regulate current and MVDC voltage. The stage 2 DC/DC converter is designed to convert DC voltage levels from MV to LV and regulate the DC voltage at the LV side. The stage 3 DC/AC converter is designed to regulate AC voltage and frequency (under grid-forming operation) or the transmitted power (under grid-connected operation) to LVAC network.

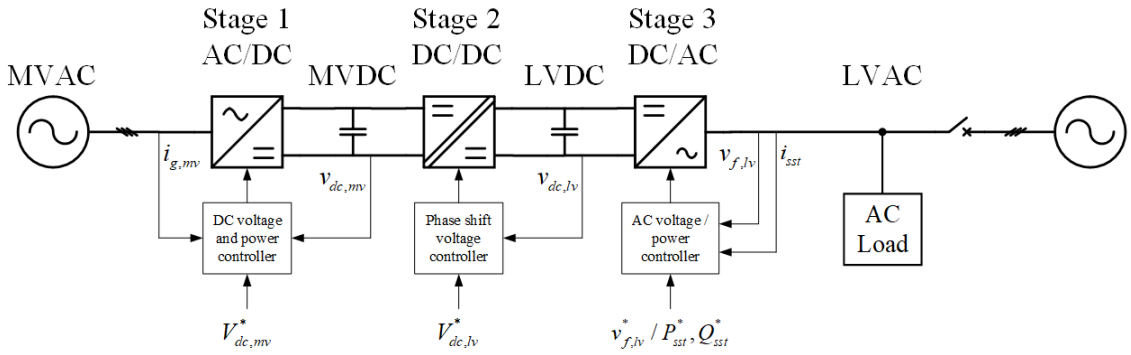


Fig. 2.1 Overall configuration and control scheme of the three-conversion stage SST.

2.1.1 Stage 1 AC/DC converter

For the AC/DC converter which uses the two-level converter in this system considered, its control objective is to regulate the DC voltage on the MV side. A dual-loop control system, including a DC voltage outer loop and a current inner loop is used, as illustrated in Fig. 2.2. The inner current loop which provides fast response and current limiting capability has been widely used for VSC converters [138, 139]. According to Fig. 2.2, the current dynamics under dq frame can be derived as

$$R_{mv} i_{g,mv,d} + L_{mv} \frac{di_{g,mv,d}}{dt} = v_{c,mv,d} - v_{g,mv,d} + \omega_{mv} L_{mv} i_{g,mv,q} \tag{2.1}$$

$$R_{mv} i_{g,mv,q} + L_{mv} \frac{di_{g,mv,q}}{dt} = v_{c,mv,q} - v_{g,mv,q} - \omega_{mv} L_{mv} i_{g,mv,d} \tag{2.2}$$

Where the DC voltage loop can be derived as

$$i^*_{g,mv} = \frac{4C_{mv}}{3 \cdot M_d} \left(-\frac{dv_{dc,mv}}{dt} + \frac{1}{C_{mv}} I_{dc,mv} - \frac{3}{4C_{mv}} M_q i_{g,mv,q} \right) \tag{2.3}$$

Where $M_d = 2v_{c,mv,d} / v_{dc,mv}$ and $M_q = 2v_{c,mv,q} / v_{dc,mv}$. $v_{dc,mv}$ is the measured MVDC voltage. The DC voltage PI control generates the d-axis current reference $i^*_{g,mv,d}$, and the minimum and maximum values of the $i^*_{g,mv}$ are set according to the converter rating. The inner current controller regulates d-axis current $i_{g,mv,d}$ and q-axis current $i_{g,mv,q}$ to regulate active and reactive power consumed (or supplied) by the AC/DC converter. $i^*_{g,mv,q}$ can be set according to the required SST operating power factor.

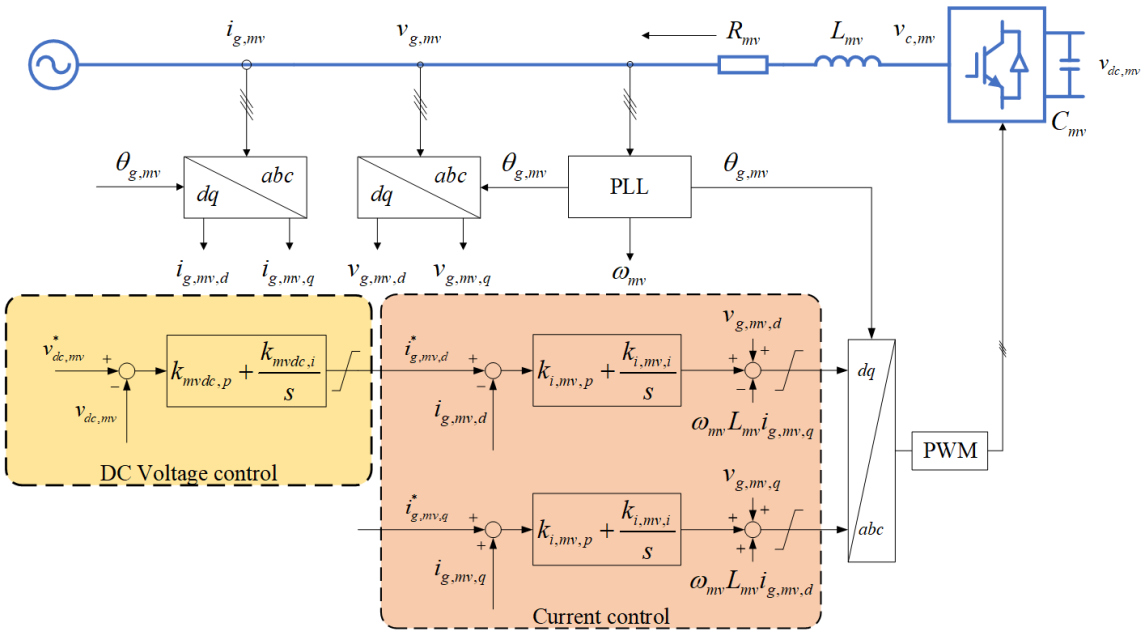


Fig. 2.2 AC/DC converter control strategy.

2.1.2 Stage 2 DC/DC converter

2.1.2.1 DAB isolated bidirectional converter

As per reference [65], DAB topology considered as DC/DC conversion stage due to bidirectional power flow and fully controllability. The DAB topology is shown in Fig. 2.3. The symmetric configuration consists of two capacitors (C_{mv}, C_{DAB}), two H-bridges with a MFT in the middle and an inductor. The inductance L_{DAB} represents the sum of the leakage inductance in the MFT and any additional inductance, which acts as the energy transfer carrier in the circuit. n is the turns ratio of the MFT.

Power flow control of DAB can be considered in a similar way as in a traditional AC power system, shown in Fig. 2.4. The direction and magnitude of the power flow is determined by the phase shift of the sinusoidal waves at both side of the inductor L in

traditional AC power systems (Fig. 2.4(a)). For DAB, the 50 Hz sinusoidal waveforms are changed to medium frequency square waves, which ranges few kHz to <100 kHz [140]. The waveform of the H-bridge voltage at the primary side v_p and secondary side v_s are determined by the conditions of the switches in the two H-bridges. Therefore, the power flow of the DAB can be controlled by controlling the switches of the two H-bridges, using the so-called phase shift modulation (PSM) control. The angle difference between the voltages of the two H-bridges is controlled to generate a voltage potential upon the inductance, thus the power transferred via the inductance between the two H-bridges is controlled. The power transferred by PSM can be derived as[141]:

$$P_{DAB} = \frac{v_{dc,mv} n v_{dc,lv}}{2\pi^2 f_s L_{DAB}} \varphi(\pi - \varphi) \tag{2.4}$$

where f_s is the switching frequency, φ is the phase shift angle between the two voltages. When φ is great than 0, power flows from the primary side to the secondary side (considered as positive direction.), whereas for negative φ, power flows from the secondary side to primary side. The maximum positive power is transferred when $\varphi = 0.5\pi$,which is

$$P_{DAB} = \frac{V_{dc,mv} n V_{dc,lv}}{8 f_s L_{DAB}} \tag{2.5}$$

The control strategies of the DAB and their detailed comparison are analysed in the following subsection.

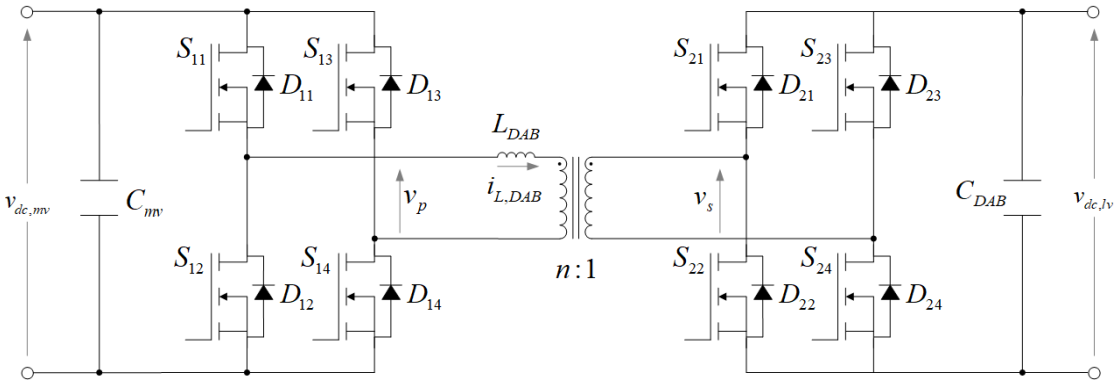


Fig. 2.3 Topology of DAB.

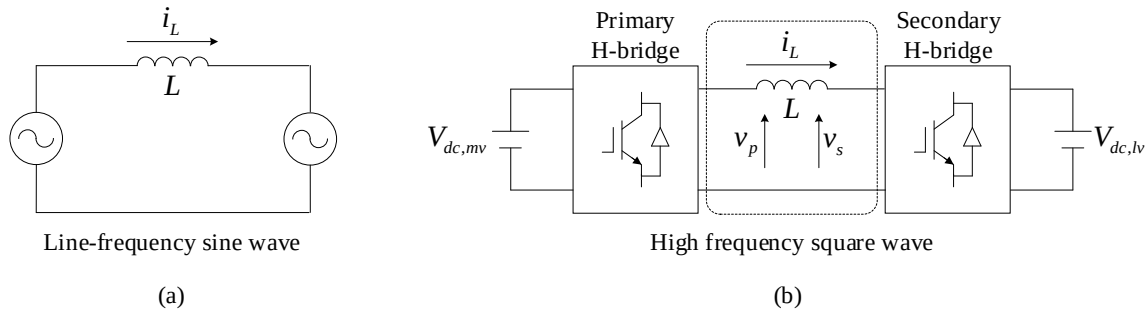


Fig. 2.4 Basic control principle of the DAB.

2.1.2.2 Control schemes of the DAB

Within PSM, the most widely used control scheme for the DAB is the single phase shift (SPS) modulation due to the simplest control [49, 142-144], and the details, including primary side H-bridge voltage v_p, secondary side H-bridge voltage v_s, current through inductance $i_{L,DAB}$ and the instantaneous power output from primary side H-bridge P_{in} during one switching cycle are shown in Fig. 2.5, wherein, all the duty cycle of the switches are 50%. The power flows from primary side to secondary side (i.e., positive), and the initial value of the current $i_{L,DAB,0}$ is assumed to be negative. The voltage waveforms of the two H-bridges present two-level square waves as the H-bridges operate in bipolar switching mode with the same gate signals for the switches at the diagonal position. A typical control scheme under SPS modulation can be achieved by applying a PI controller, shown in Fig. 2.6, where the phase shift ratio D, defined as $D = \varphi/\pi$, is controlled by the PI controller to adjust the voltage potential upon the inductance, thus controlling the direction and magnitude of the power flow. As shown in Fig. 2.5, during $t_0 - t_0^{'}$, a portion of the power shown as the orange part in Fig. 2.5, is sent back to the primary voltage source due to the positive voltage and negative current. This is defined as

circulated reactive power in the DAB control, which will decrease the efficiency of the DAB, thus the whole SST system.

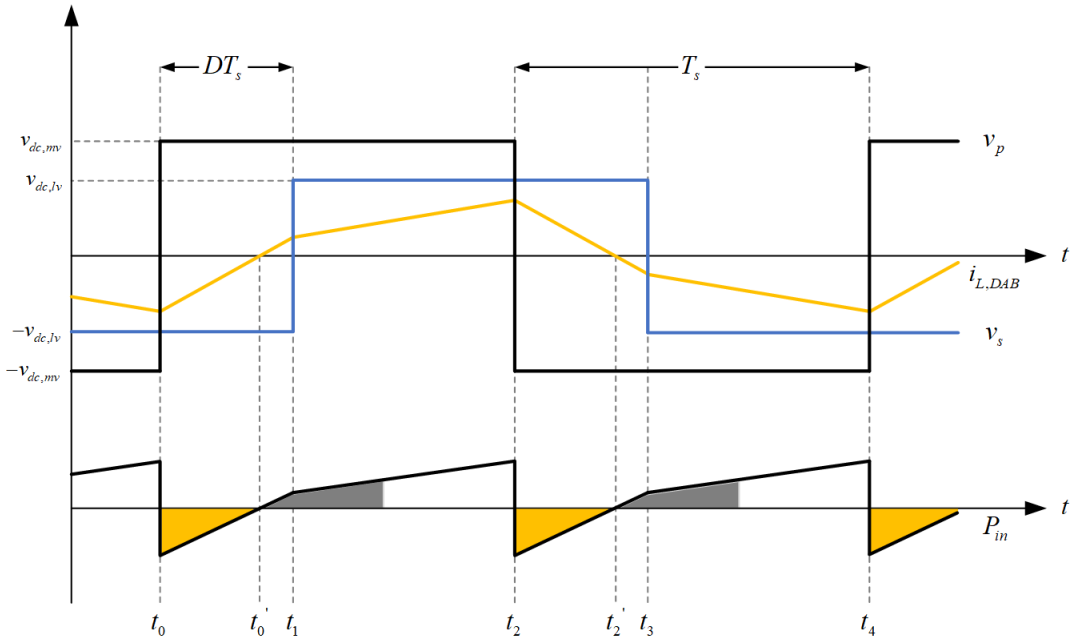


Fig. 2.5 Working principle of the DAB under SPS modulation.

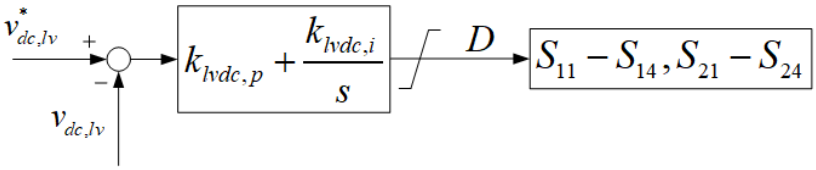


Fig. 2.6 Typical control diagram under SPS modulation.

The extended phase shift modulation (EPS) is introduced in [145-148], and the working principle is shown in Fig. 2.7. With EPS, the primary H-bridges operate in unipolar PWM mode where the switches in the same bridge arm are switched in turn so the converter produces 3-level voltage output. For the secondary H-bridge, its operation is the same as SPS with two-level voltage output. The inner phase shift ratio, D_1 is introduced between the switches on different bridge arms of the primary side H-bridge, while D_2 is the outer phase shift ratio between the two H-bridge (which is the same as the phase shift ratio D under SPS modulation).

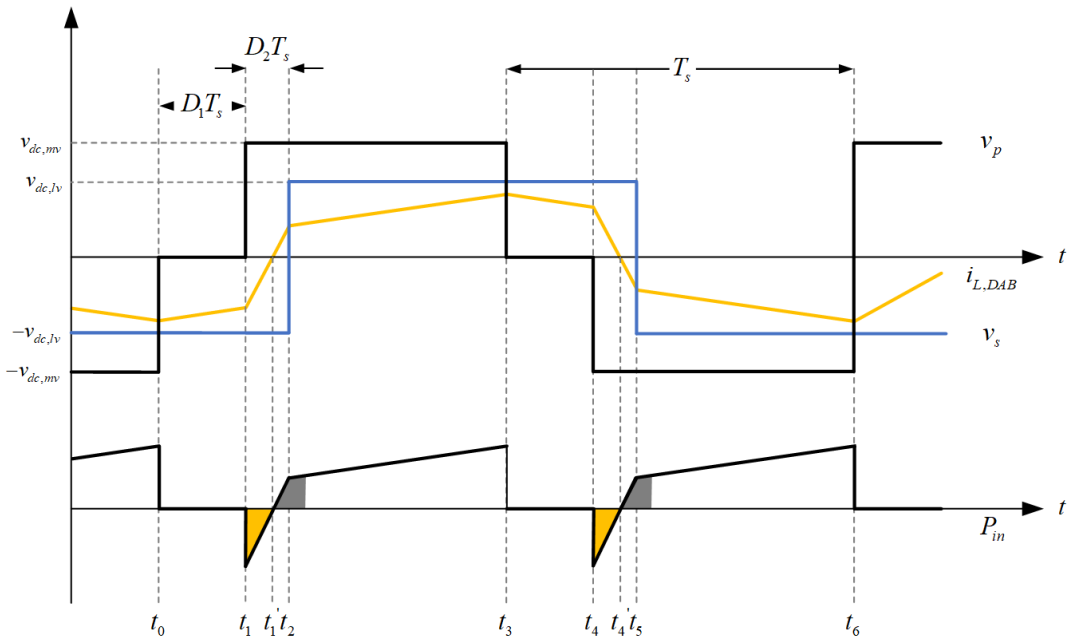


Fig. 2.7 Working principle of the DAB under EPS modulation.

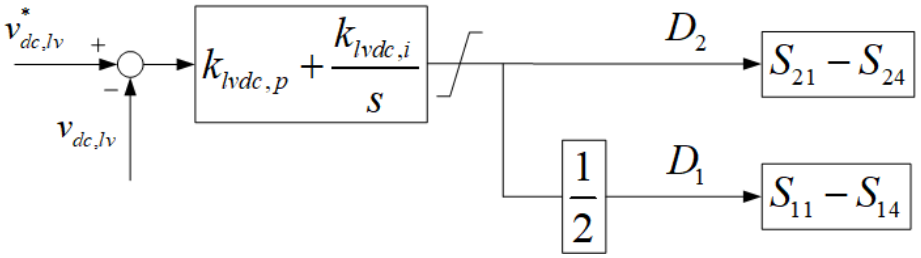


Fig. 2.8 Typical control diagram under EPS modulation.

The phase shift ratios are constrained as $0 \le D_2 \le 1$, $0 \le D_1 + D_2 \le 1$ ($D_1 \ge 0$). The transmitted power under EPS modulation can be derived as [145],

$$P_{DAB,EPS} = \frac{v_{dc,mv} n v_{dc,lv}}{2 f_s L_{DAB}} \left[D_2 (1 - D_2) + \frac{1}{2} D_1 (1 - D_1 - 2D_2) \right] \tag{2.6}$$

D_2 can be regulated by a PI controller in the same way as in SPS modulation. Meanwhile, for minimising the circulated reactive power, D_1 is derived as $1/2\,D_2$, where the detailed

derivation can be found in [145]. A typical control diagram under EPS modulation is shown in Fig. 2.8.

From the typical waveforms shown in Fig. 2.7, it can be seen that the improvement when compared with the SPS modulation is on the primary H-bridge. By introducing the 'zero voltage potential' intervals, the circulated reactive power is reduced to zero during $t_0 - t_1$. However, as the three-level potential is only improved on the primary side, the control scheme is designed asymmetrically in EPS modulation. The operation of the switches on the two H-bridge converters need to be exchanged when power flow direction is reversed.

To further address the issues, the dual phase shift (DPS) modulation is introduced [146], and the working principle is shown in Fig. 2.9. As shown, D_2 is still defined as the phase difference between the primary and secondary side H-bridge converters. However, under DPS modulation, the secondary side of the H-bridge operates with the same inner phase shift ratio as the primary side so both voltages possess three-level characteristic. The adjustable ranges of these two variables are $0 \le D_1 \le D_2 \le 1$ and $0 \le D_1 + D_2 \le 1$. The operation principle, transmission power, current stress, power loss, soft switching and optimisation design methods are discussed in [149-151], and the transmitted power under EPS modulation is given as:

$$P_{DAB,DPS} = \frac{v_{dc,mv} n v_{dc,lv}}{2 f_s L_{DAB}} \left[D_2 \left(1 - D_2\right) - \frac{1}{2} D_1^2 \right] \tag{2.7}$$

To minimise the circulated reactive power, the relationship between D_1 is derived as D_2 or $1 - 2D_2$ when D_2 is less or greater than $1/3$. And the typical control diagram under DPS modulation is shown in Fig. 2.10.

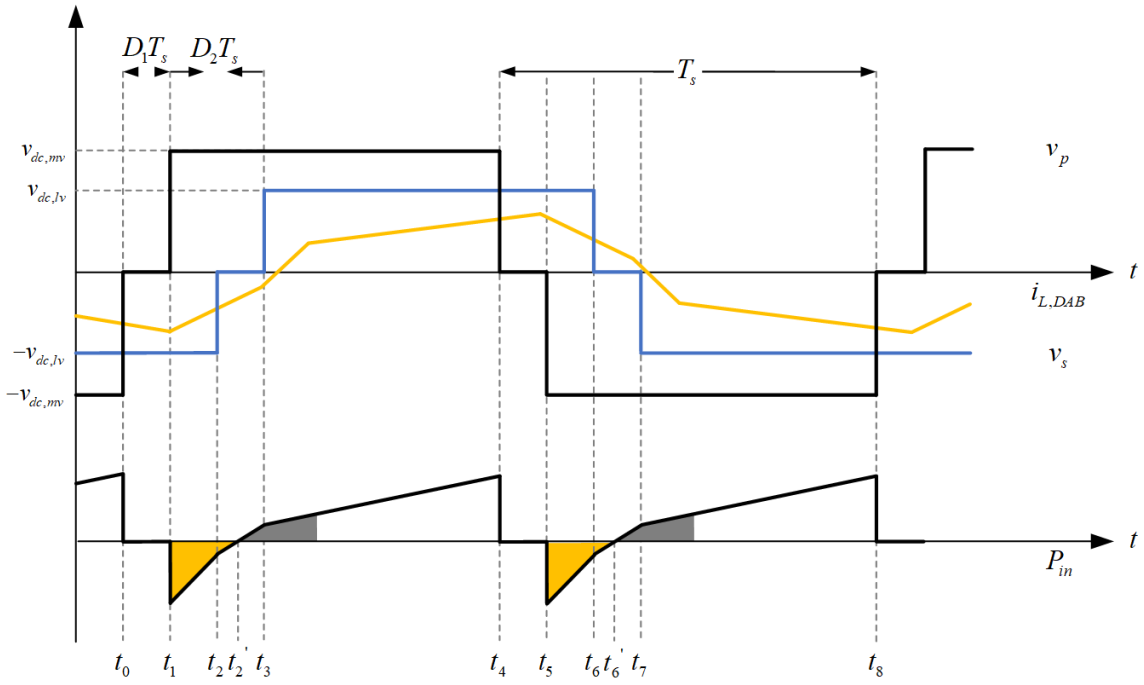


Fig. 2.9 Working principle of the DAB under DPS modulation.

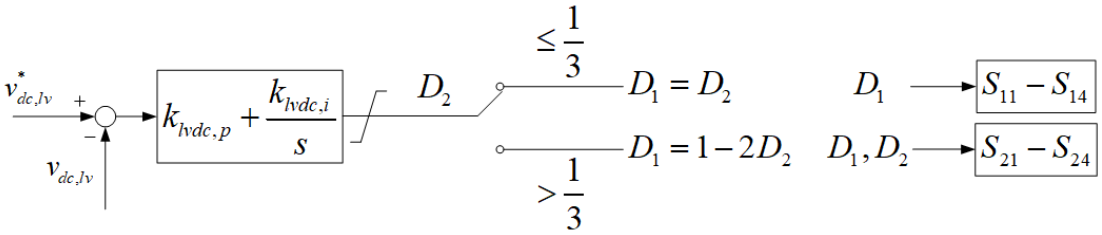


Fig. 2.10 Typical control diagram under DPS modulation.

Compared with the SPS modulation, DPS modulation can decrease current stress and steady-state current. Introducing the zero potential level at secondary side of the H-bridge further improves the efficiency. Comparing with EPS modulation, DPS modulation is more flexible to achieve bidirectional power flow due to its symmetric control structure. Therefore, DPS performs better dynamic behaviour.

To make DPS modulation more flexible, the triple phase shift (TPS) modulation is introduced. The working principle is shown in Fig. 2.11, where the inner phase shift ratio on the secondary H-bridge D_3 can be different to that of the primary side D_1. It is proved

that TPS modulation can minimise the inductor current and power loss compared to other modulation schemes [152].

TPS modulation can be considered as a consolidated version of the phase shift modulation for the DAB, which SPS, EPS, and DPS modulations are as special cases of TPS modulation.

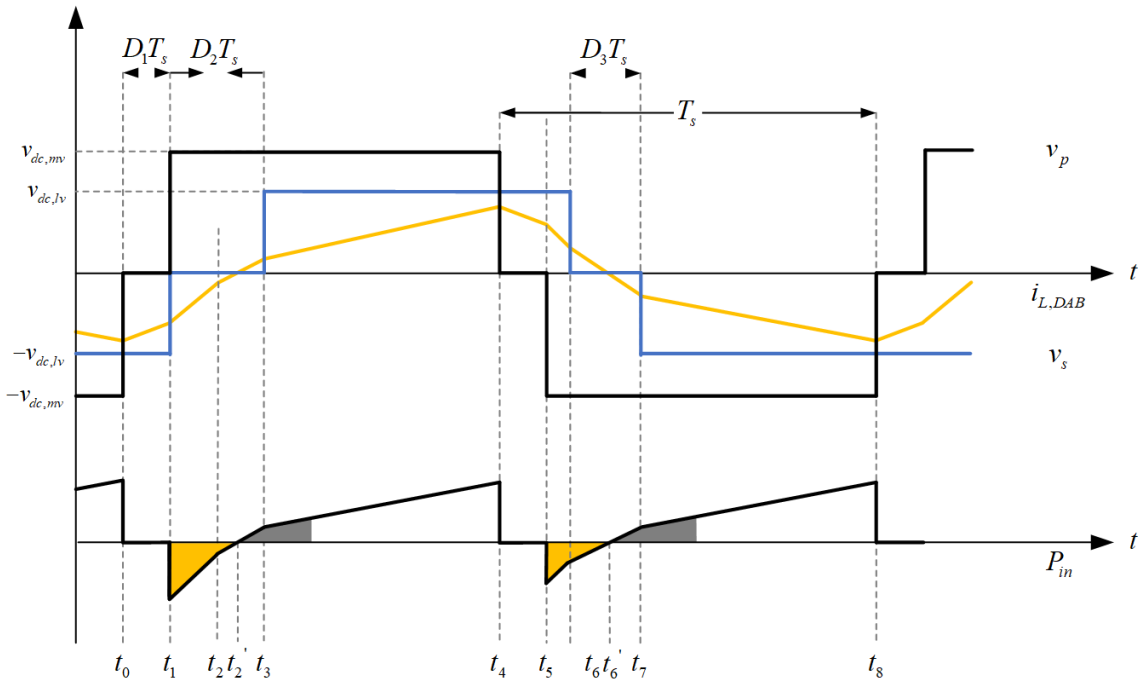


Fig. 2.11 Working principle of the DAB under TPS modulation.

2.1.2.3 Simulation comparison among different phase shift modulation schemes

The operation of the SPS, EPS and TPS modulation schemes are compared in MATLAB/Simulink in this sub-section. It is noted here that DPS scheme results are the same as TPS, so that the DPS results will not be included. The main parameters of the tested DAB model are shown in Table 2.1. As the thesis is planning to demonstrate prototype with Silicon Carbide (SiC) device, the switching frequency here is considered

as 20kHz. Fig. 2.12 (a)-(c) show the voltages on both sides of L_{DAB}, v_p and nv_s (n =12.5), and inductance current $i_{L,DAB}$ under SPS, EPS and TPS modulations, respectively. During a single switching cycle $t = 50\mu s$, the two-level voltages on the primary and secondary sides under SPS modulation are clearly to be seen in Fig. 2.12(a). The peak value of $i_{L,DAB}$ is about 1.537 kA under SPS modulation. The three-level primary side voltage under EPS modulation is seen in Fig. 2.12(b). The peak value of $i_{L,DAB}$ (1.74 kA) shows 13% increase compared to that under SPS modulation, which indicates increased current stress for the power electronic switches. The dual three-level voltages on both primary and secondary sides of the H-bridge converters under TPS modulation are seen in Fig. 2.12(c) and the current stress is slightly reduced (1.49 kA) compared to that under SPS modulation.

Table 2.1 Parameters of the tested DAB converter

Parameters	Values
Rated power (DC/DC)	10 MW
Inductance	52.08 μH
MVDC voltage	10,000 V
LVDC voltage	800 V
Transformer ratio	25:2
LVDC capacitance	18.5 mF
Switching frequency	20 kHz
Load	10 MW at 750 V

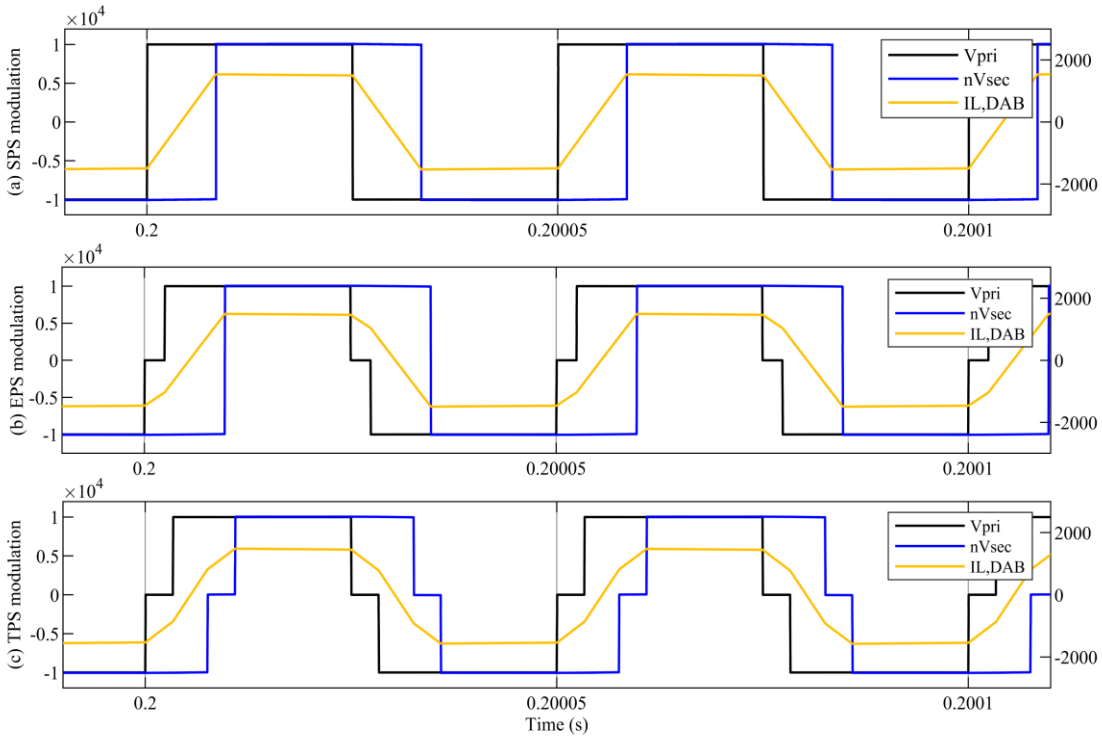


Fig. 2.12 Primary side voltage, secondary side voltage and inductance current waveforms under: a) SPS modulation, b) EPS modulation, c) TPS modulation.

Fig. 2.13 shows the instantaneous power output from primary side H-bridge under the three phase shift modulations.

As shown in Fig. 2.13(a), the backflow reactive power under SPS modulation reaches to -14.38 MW and flows back to zero after $t = 4.088\mu s$. The power output reaches to 15.32 MW in $t = 4.299\mu s$. The backflow energy ratio over single switching cycle is calculated as 11.95%, which is the largest ratio due to the lack of the zero voltage potential.

As shown in Fig. 2.13(b), the backflow reactive power under EPS modulation reaches to -10.71 MW and flows back to zero after $t = 2.966\mu s$,which is reduced compared with that under SPS modulation. The power output reaches to 15.61 MW in $t = 4.344\mu s$. The peak value of the instantaneous power output is slightly higher than SPS modulation since

the current stress under EPS modulation is higher than that under SPS modulation. The backflow energy ratio over single switching cycle is calculated as 6.27%, which is reduced about half of that under SPS modulation.

As shown in Fig. 2.13(c), the backflow reactive power under TPS modulation reaches to -8.304 MW and flows back to zero after $t = 2.071\mu s$, which is further reduced compared with that under EPS modulation. The power output reaches to 14.95 MW in $t = 5.492\mu s$. The backflow energy ratio over single switching cycle is calculated as 3.6%, which is further reduced than that under EPS modulation.

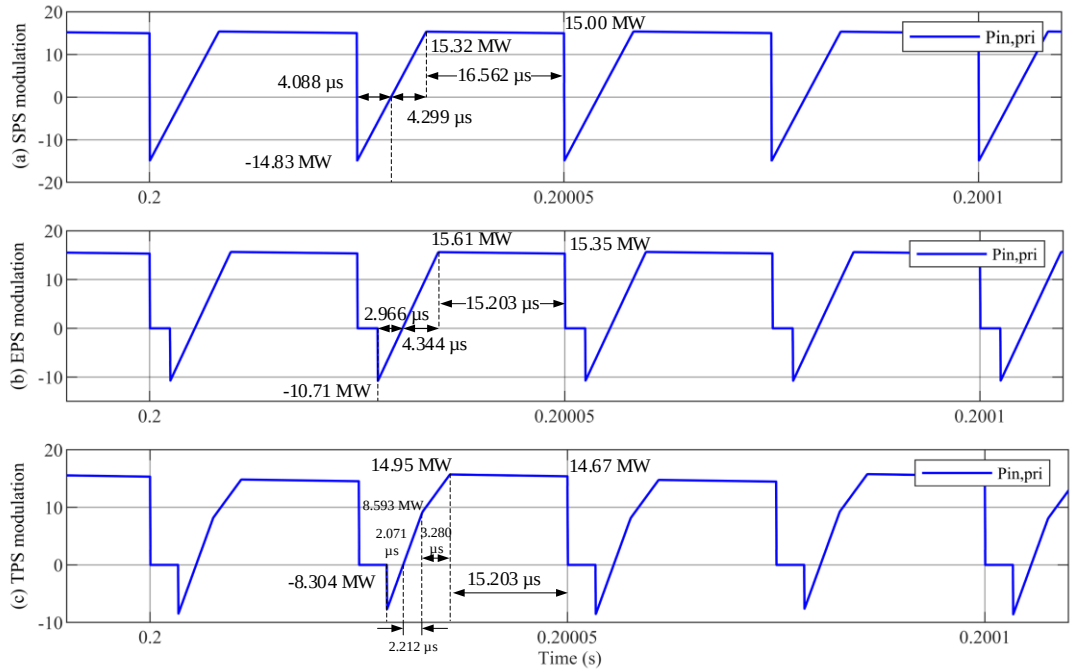


Fig. 2.13 Instantaneous power output from primary side H-bridge under: a) SPS modulation, b) EPS modulation, c) TPS modulation

2.1.3 Stage 3 DC/AC converter

Similar with the stage 1 AC/DC converter, the two-level converter is considered for the DC/AC conversion stage. It is noted that the grid-forming operation is considered only in this chapter and the performance of the DC/AC converter under grid-connected operation is similar to the stage 1 converter control and will be evaluated in Chapter 3.

The main objective of the converter in the SST is to provide stable three-phase sinusoidal voltage with constant amplitude and frequency. To achieve the objective, a dual closed loop, including current control and voltage control is used as shown in Fig. 2.14.

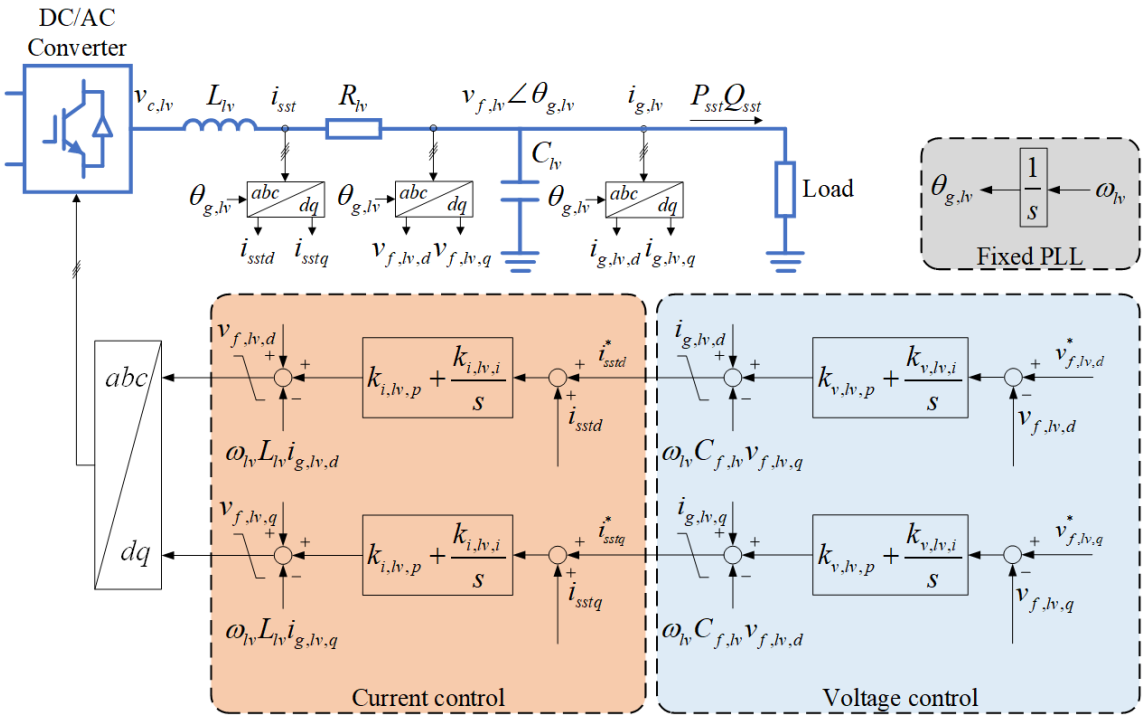


Fig. 2.14 DC/AC converter control strategies

The inner current controller is developed to regulate the AC side current i_{sst}, enabling fast response and current limiting during external AC fault [138]. It can be designed in a similar way as the inner current controller for the stage 1 AC/DC converter shown in

Subsection 3.1.1. By fixing the d-axis to the VSC filter voltage $v_{f,lv}$, the i_{sst} dynamics under *dq* reference frame is

$$R_{lv} i_{g,lv,d} + L_{lv} \frac{di_{g,lv,d}}{dt} = v_{c,lv,d} - v_{g,lv,d} + \omega_{lv} L_{lv} i_{g,lv,q} \tag{2.8}$$

$$R_{lv} i_{g,lv,q} + L_{lv} \frac{di_{g,lv,q}}{dt} = v_{c,lv,q} - v_{g,lv,q} - \omega_{lv} L_{lv} i_{g,lv,d} \tag{2.9}$$

wherein ω_{lv} is angular frequency of the AC voltage at the LV output, which is also the rotating speed of the *dq* reference frame. ω_{lv} is fixed since only the grid forming mode is considered in this chapter. $v_{c,lv}$ is the output voltage of the DC/AC converter. The current control loop is implemented by proportional-integral (PI) controllers, shown in Fig. 2.14. The upper and lower limitation of the *dq* current are set on the basis of the converter current rating, also serving for limiting the fault current.

Similar with current control, $v_{f,lv}$ under *dq* reference frame can be derived as

$$C_{lv} \frac{dv_{f,lv,d}}{dt} = i_{sst,d} - i_{g,lv,d} + \omega_{lv} C_{lv} v_{f,lv,q} \tag{2.10}$$

$$C_{lv} \frac{dv_{f,lv,q}}{dt} = i_{sst,q} - i_{g,lv,q} - \omega_{lv} C_{lv} v_{f,lv,d} \tag{2.11}$$

By regulating the output current of the DC/AC converter, $v_{f,lv}$ can follow its reference with the implemented PI controller, as shown in Fig. 2.14. The upper and lower limitation of the *dq* voltage are set on the basis of the DC/AC converter voltage rating, also serving for limiting the overvoltage.

2.2 Simulation results

In this section, the voltage controller of the DC/AC converter is firstly tested as an example to be used to understand how the control parameters influence on the system

response in MATLAB/Simulink. The control scheme is implemented in a two level converter. Then the performance of the three stage SST as a whole system under grid forming operation is evaluated. The system parameters of the whole system are shown in Table 2.2.

Table 2.2 Parameters of the SST system.

	Parameter	Value
Stage 1 AC/DC converter	Rated power (AC/DC)	10 MW
	Rated MVAC voltage	11 kV
	Rated MVDC voltage	10 kV
	Inductance L_{mv}	0.001 H
	Capacitance $C_{f,mv}$	6.76 mF
	Rated MVAC frequency	50 Hz
Stage 2 DC/DC converter	Rated power (DC/DC)	10 MW
	Inductance L_{DAB}	52.08 μH
	LVDC capacitance C_{DAB}	18.5 mF
	Rated LVDC voltage	750 V
	Switching frequency	20 kHz
Stage 3 DC/AC converter	Rated power (DC/AC)	10 MW
	Rated LVAC voltage	415 V
	Capacitance $C_{f,lv}$	0.185 mF
	Inductance L_{lv}	0.011 mH
	Rated LVAC frequency f_{lv}	50 Hz
	Voltage controller parameters (k_p, k_i)	(172.2, 5.9e4)

2.2.1 Performance of the controller

The performance of the DC/AC converter is evaluated firstly in this subsection. Main parameters of the tested DC/AC converter are shown in Table 2.2. The tested controller tuning can be used to better understand how k_p and k_i influence the system response, where the control parameters are estimated by $2/\omega' C_{f,lv}$ and $8/\left(\omega' C_{f,lv}\right)^2$ according to natural frequency $f' = 7Hz$, which is based on experienced value.

At the beginning, the converter operates with a 6 MW load. At $t = 2s$, a 4 MW load is switched in at the LVAC side. Fig. 2.15 and Fig. 2.16 show the voltage controller (dq-frame) responses to the load change with different control parameters. It can be seen that both k_p and k_i affect the response of the system. Compared with the base value of k_p and k_i (172.2, 5.9e4) in d-axis controller, $2k_p$ has smaller oscillation than k_p and $0.75k_p$ with the same k_i, illustrated in Fig. 2.15(a)(b). For q-axis controller, k_p performance are mainly the same when k_i varies, while $2k_p$ has smaller oscillation than k_p and $0.75k_p$ with the same k_i, illustrated in Fig. 2.16(a)(b). Obviously, the setting of the control parameters also affects system stability so needs to be carefully considered.

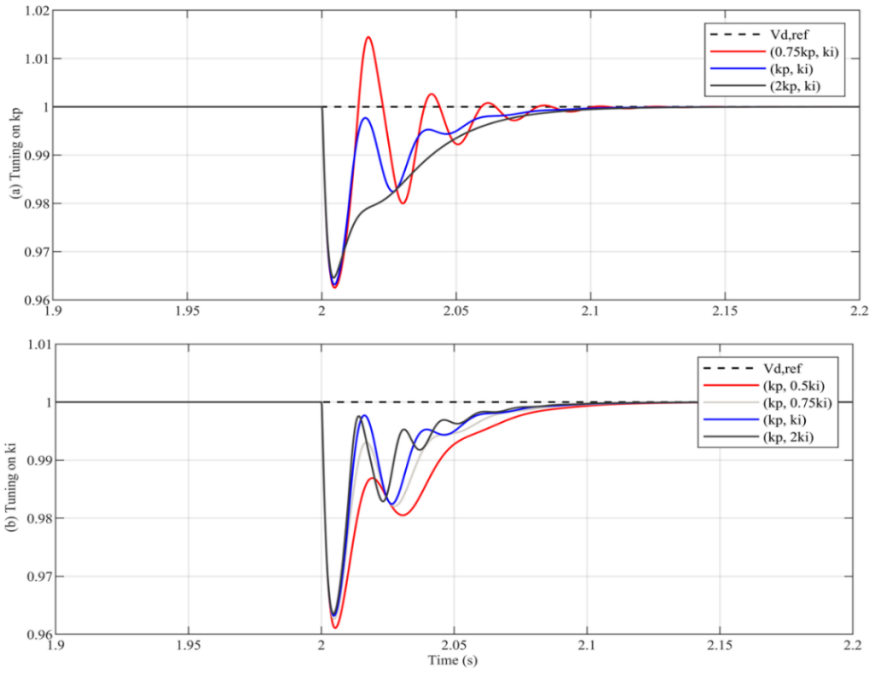


Fig. 2.15 Performance of the d-axis voltage controller in the DC/AC converter under grid-forming operation: a) tuning on k_p; b) tuning on k_i.

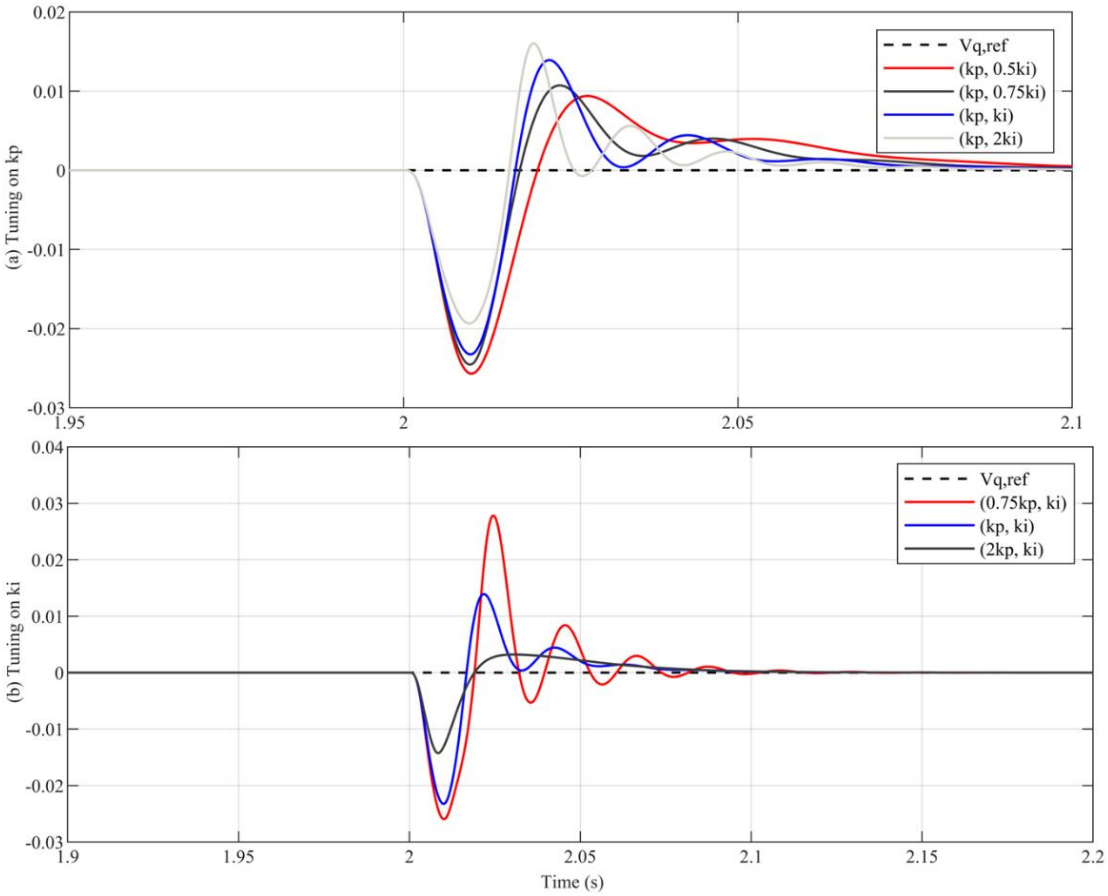


Fig. 2.16 Performance of the q-axis voltage controller in the DC/AC converter under grid-forming operation: a) tuning on k_p; b) tuning on k_i.

2.2.2 Performance of the basic SST under grid-forming operation

The performance of the basic SST control under grid forming operation is assessed in this sub-section. The parameters of the SST can be found in Table 2.1. The tested system is shown in Fig. 2.1, The load conditions during simulation are listed in Table 2.3 and described as in the followings. The simulations results are shown in Fig. 2.17.

Event 1: At the beginning, the MVDC link voltage is established and regulated by the AC/DC converter while the LVDC link voltage is established and regulated by the DC/DC

converter, seen in Fig. 2.17(i)(j). The voltage and current control of the DC/AC converter regulate its output LVAC voltage ($v_{f,lv}$) and current (i_{sst}) under dq frame to 1 pu with LVAC frequency at 50 Hz, as shown in Fig. 2.17(a)-(d). The active power and reactive power output of the SST matches the load of 10 MW, as shown in Fig. 2.17(e)(f), and the three-phase output voltage and current are illustrated in Fig. 2.17 (g) and (h), respectively.

Event 2: At $t = 2s$, a 2 MW load is switched off at the LVAC side. As seen in Fig. 2.17(e)(f), the power output of the SST is quickly changed. while the frequency of the LVAC network has a small fluctuation of 0.09 Hz, shown in Fig. 2.18(a). The MVDC and LVDC appear 2% and 0.1% fluctuation and recovered within 0.15 s respectively, shown in Fig. 2.18(b)(c). For AC voltage, according to the requirement of the rapid voltage change (RVC) under Grid Code Limits, a sudden reduction of the AC voltage is defined to a value of 90% and 10% of the declared voltage, and the duration of the a voltage fluctuation is between 10 ms and 1 min [153]. The AC volage during the load change and the phase A voltage in rms value are shown in Fig. 2.18(d)(f). The fluctuation of the AC voltage is up to 8.6% and recovered in 0.1 s, which meets the requirement of the under Grid Code Limits.

Event 3: At $t = 3s$, another 2 MW load is switched off. The simulation results show similar with Event 2. The fluctuation of the AC voltage is up to 9.6% and AC voltage is back to 1 pu in 0.1 s, shown in Fig. 2.19(a)(b), which meets the requirement of the RVC under Grid Code Limits.

Event 4: At $t = 4s$, a 2 MVar capacitive load is switched in. As seen in Fig. 2.17(e)(f), the power output of the SST is smoothly changed to generate the required active and reactive power. From the detailed waveforms shown in Fig. 2.20, the frequency of the LVAC network has a small fluctuation of 0.08 Hz, while the MVDC and LVDC are largely unaffected, shown in Fig. 2.20(b)(c). The AC voltage fluctuation at load side is around 4.1% and is eliminated within 0.1s, shown in Fig. 2.20(d)-(f).

Event 5: At $t = 5s$, a 2 MVar capacitive load is switched off and the simulation results show similar behaviour as in Event 4. The fluctuation of the AC voltage is up to 1.5% and AC voltage is back to 1 pu in 0.1 s, shown in Fig. 2.21(a)(b), which meets the requirement of the rapid voltage change (RVC) under Grid Code Limits.

Event 6: At $t = 6s$, a 2 MVar inductive load is connected to the LVAC side. As seen in Fig. 2.17(e)(f), the power output of the SST is smoothly changed to meet the required active and reactive power. The frequency of the LVAC network has a fluctuation of 0.14 Hz, where the details are shown in Fig. 2.22(a). The MVDC and LVDC are well controlled as shown in Fig. 2.22 (b)(c). The AC voltage fluctuation at load side is around 4.3% and settles within 0.1s, as shown in Fig. 2.22 (d)-(f).

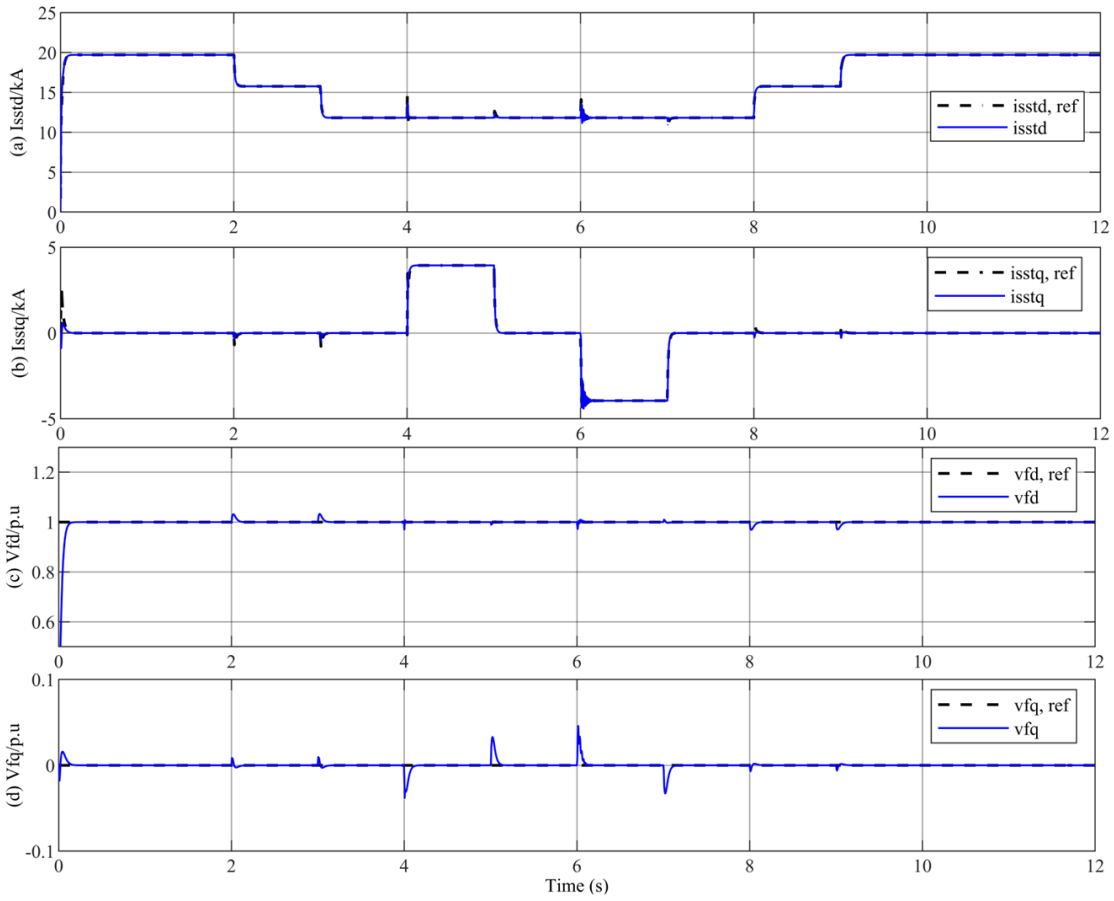
Event 7: At $t = 7s$, the 2 MVar inductive load is disconnected and the simulation results show similar behaviour as with Event 6. The fluctuation of the AC voltage is up to 3.4% and AC voltage is back to 1 pu in 0.1 s, shown in Fig. 2.23(a)(b), which meets the requirement of the rapid voltage change (RVC) under Grid Code Limits.

Event 8 and Event 9: At $t = 8s$, and 9s, two 2 MW resistive loads are connected to the LVAC load side in sequence. As seen in Fig. 2.17, the simulation results are similar to Event 1 and 2, and the operation is very smooth during the load changes. The fluctuation of the AC voltage is up to 5.4% and 5.1% respectively. AC voltages under two events are both back to 1 pu in 0.1 s, shown in Fig. 2.23(a)(b), which meet the requirement of the rapid voltage change (RVC) under Grid Code Limits.

From the performance under the 9 events, the basic control scheme of SST, including all three conversion stages can effectively follow the references under different load conditions. The AC voltages are within RVC under Grid Code limit. Additional control scheme for SST under grid-connected operation and hybrid AC/DC network will be based on the basic control.

Table 2.3 Load condition under grid forming operation.

Event	Time	Active Power (MW)	Reactive Power (MVar)
Event 1	0-2 s	10	0
Event 2	2-3 s	8	0
Event 3	3-4 s	6	0
Event 4	4-5 s	6	2
Event 5	5-6 s	6	0
Event 6	6-7 s	6	-2
Event 7	7-8 s	6	0
Event 8	8-9 s	8	0
Event 9	9-12 s	10	0



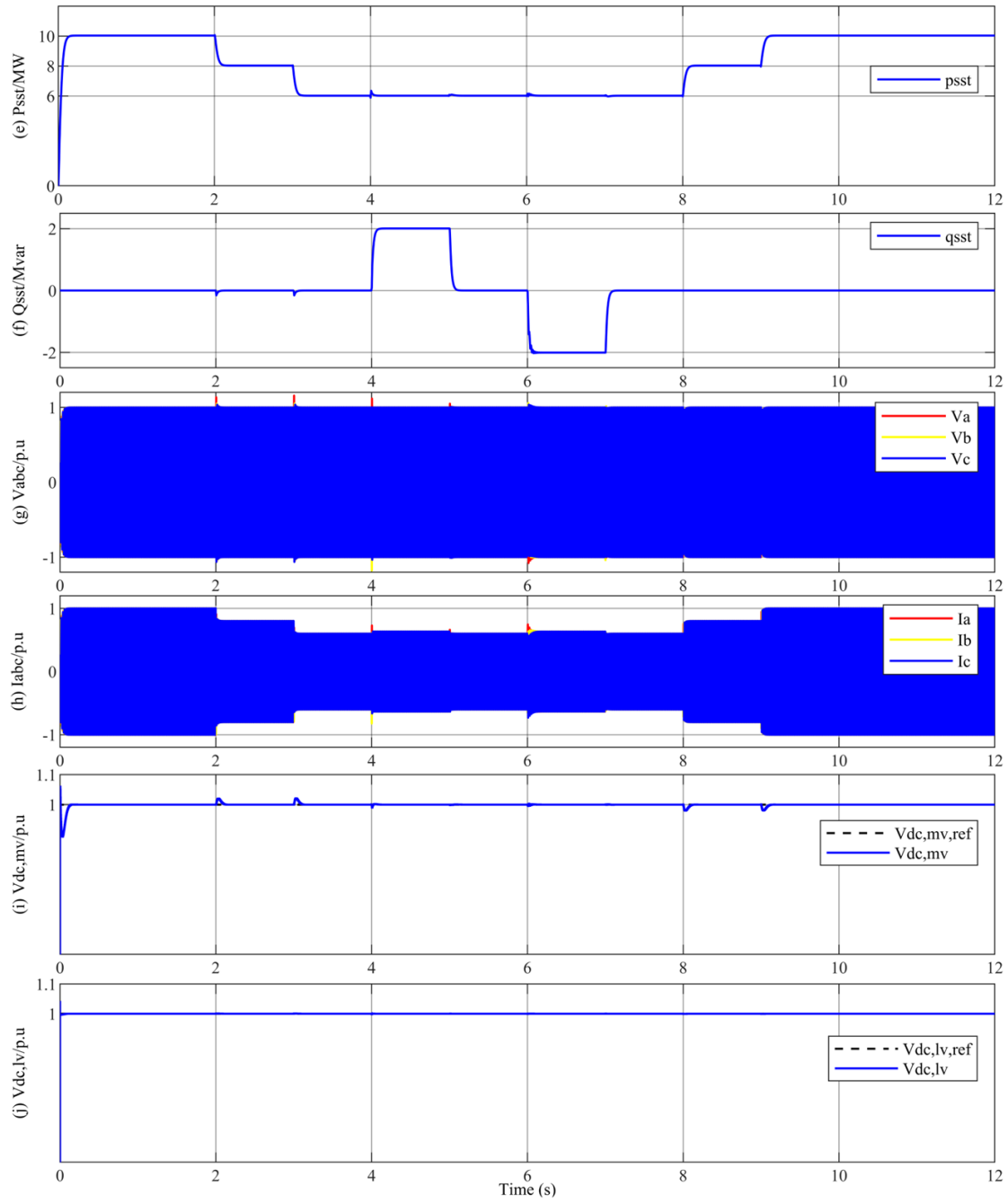


Fig. 2.17 Performance of the SST converter under grid-forming operation: (a) output d-axis current; (b) output q-axis current; (c) output d-axis voltage; (d) output q-axis voltage; (e) converter transmitted active power; (f) converter transmitted reactive power; (g) load voltage (3-ph); (h) load current (3-ph); (i) medium voltage DC; (j) low voltage DC.

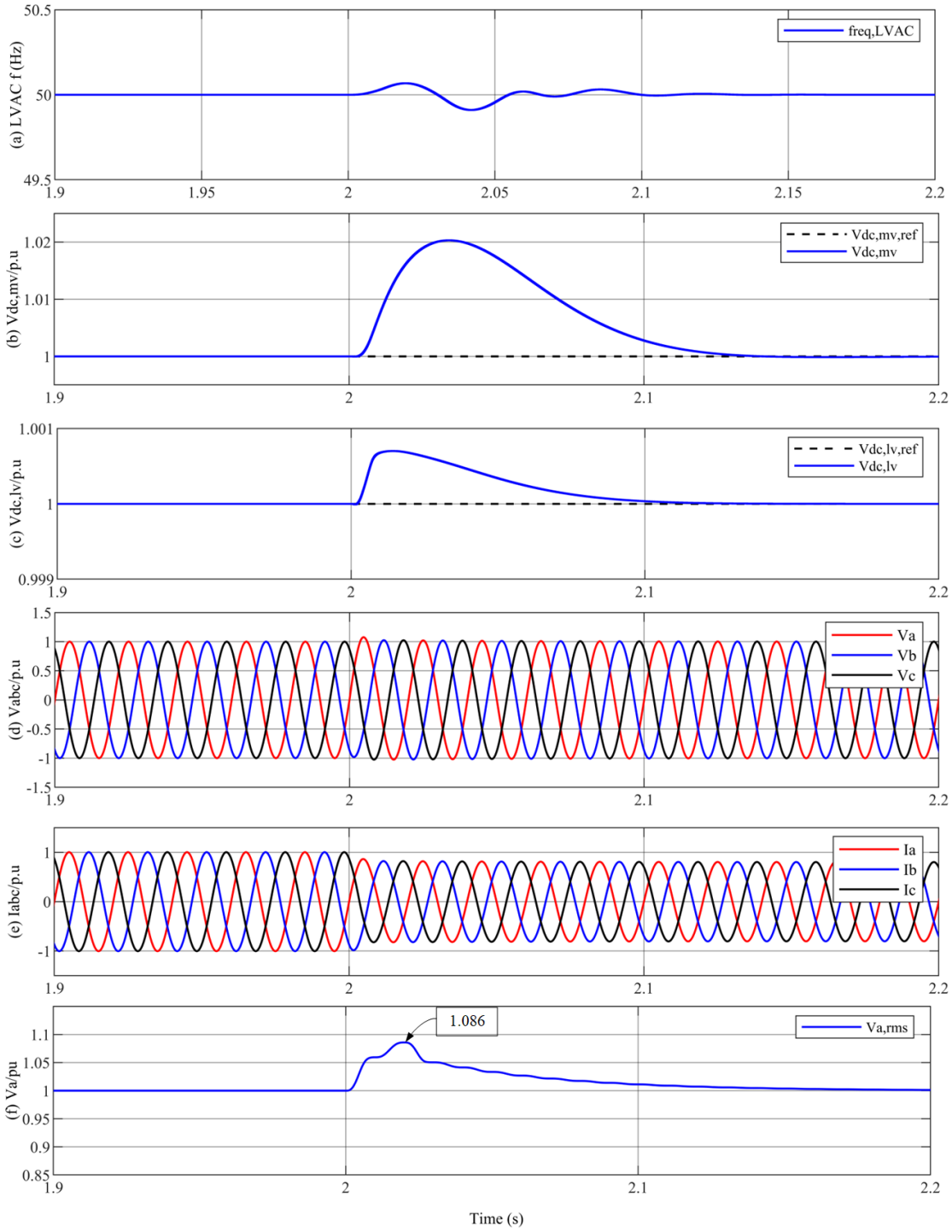


Fig. 2.18 Performance of the DC/AC converter under grid-forming operation during Event 2: a) LVAC frequency; b) MVDC voltage; c) LVDC voltage; d) load voltage (3-ph); (e) load current (3-ph); (f) Phase A load voltage (rms value).

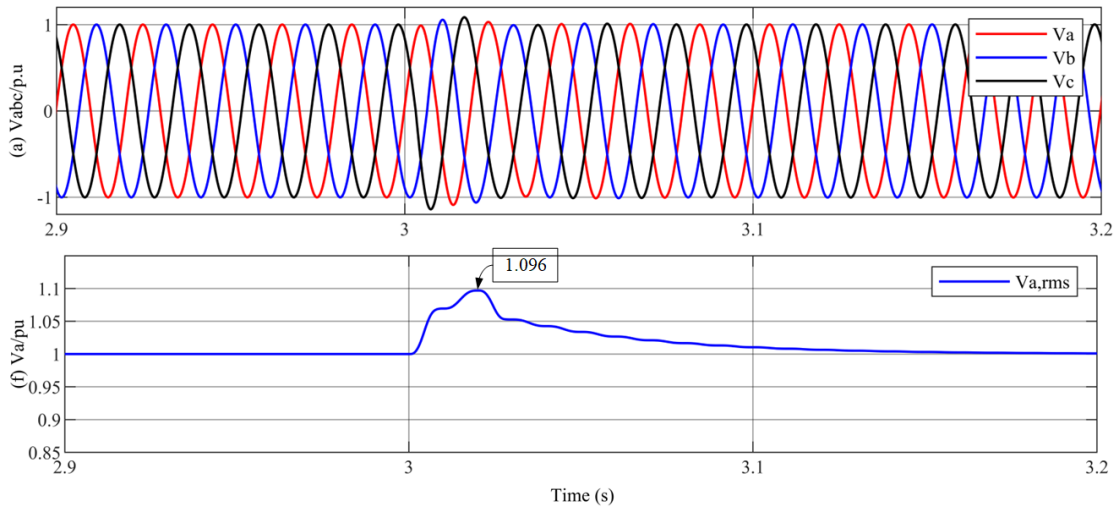
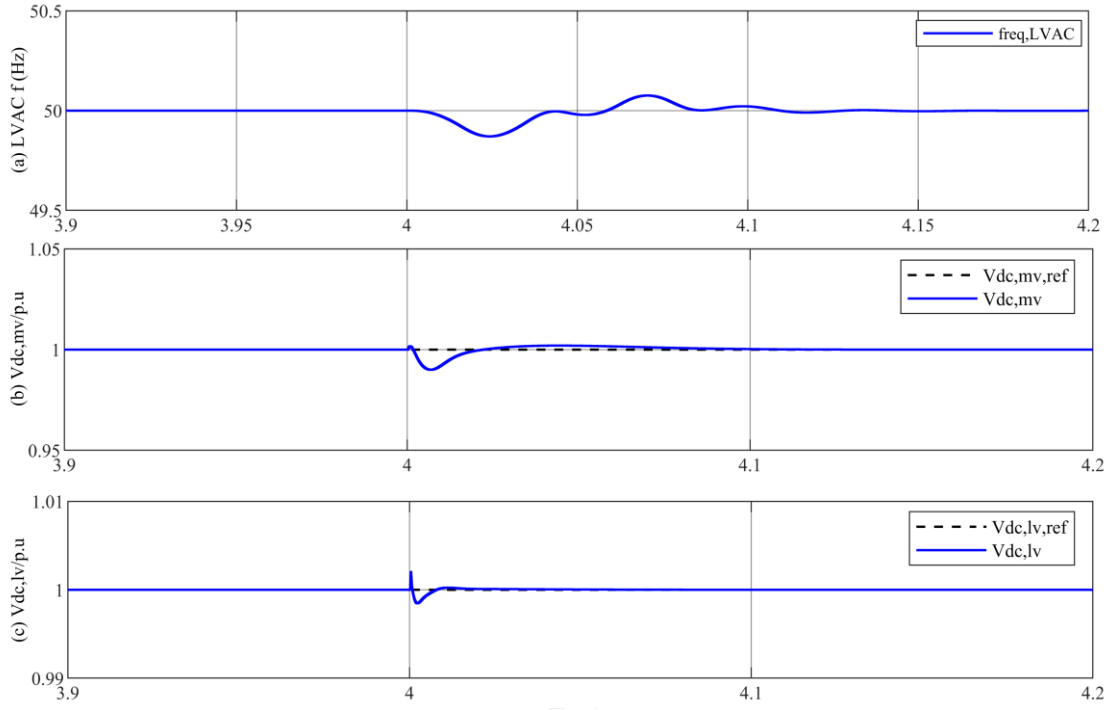


Fig. 2.19 Performance of the DC/AC converter under grid-forming operation during Event 3: a) load voltage (3-ph); b) phase A load voltage (rms value).



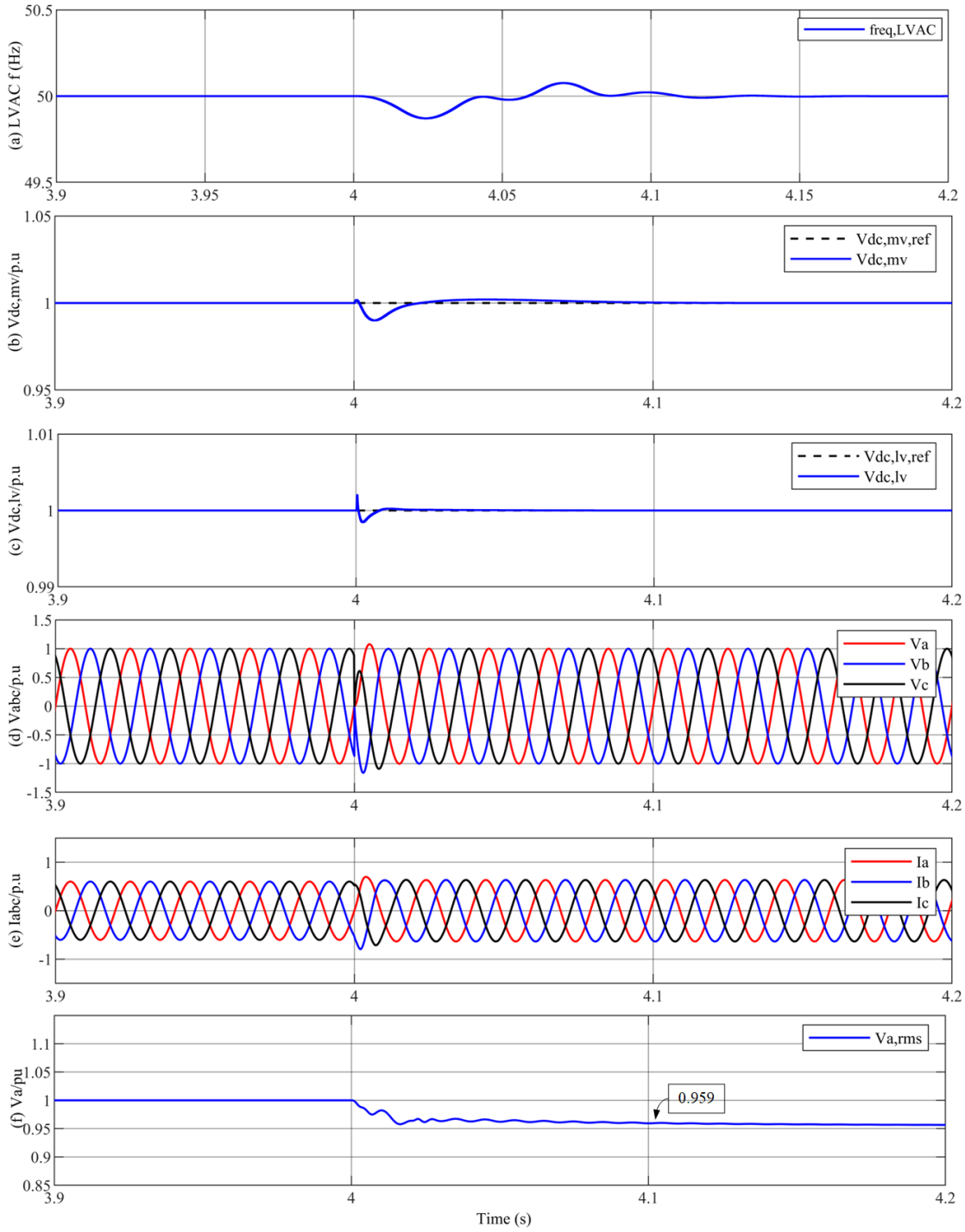


Fig. 2.20 Performance of the DC/AC converter under grid-forming operation during Event 4: a) LVAC frequency; b) MVDC voltage; c) LVDC voltage; d) load voltage (3-ph); (e) load current (3-ph); f) phase A load voltage (rms value).

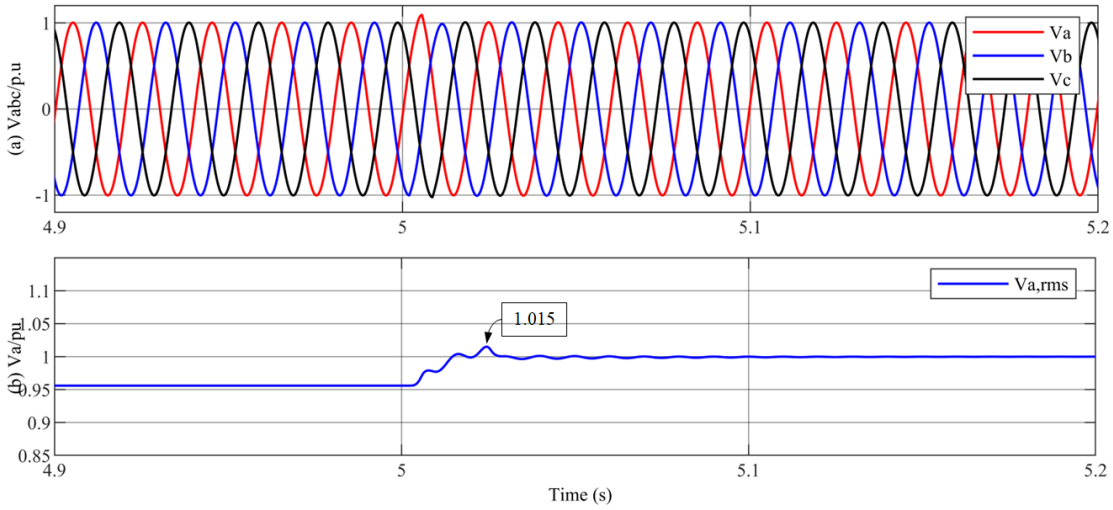


Fig. 2.21 Performance of the DC/AC converter under grid-forming operation during Event 5: a) load voltage (3-ph); b) phase A load voltage (rms value).

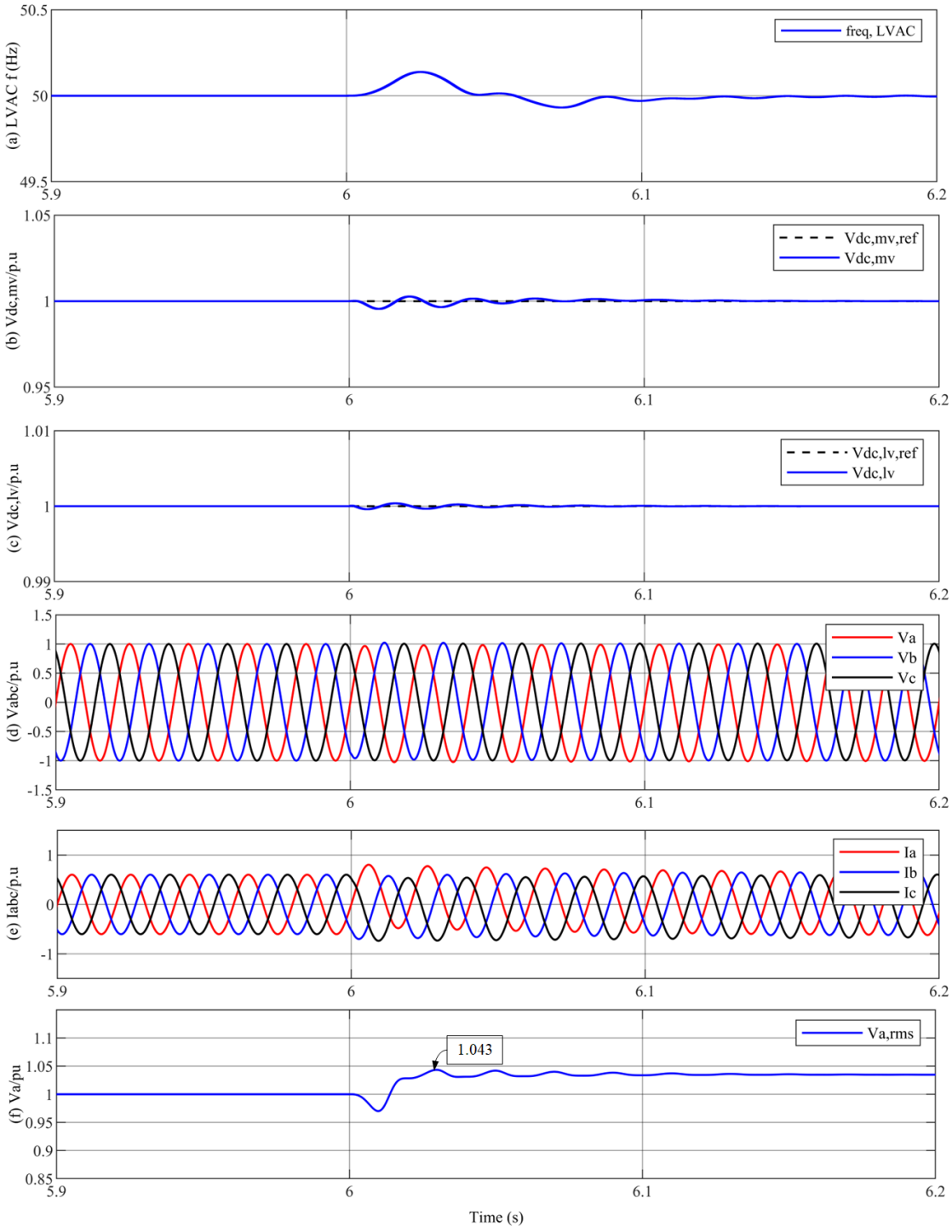


Fig. 2.22 Performance of the DC/AC converter under grid-forming operation during Event 6: a) LVAC frequency; b) MVDC voltage; c) LVDC voltage; d) load voltage (3-ph); (e) load current (3-ph); f) phase A load voltage (rms value).

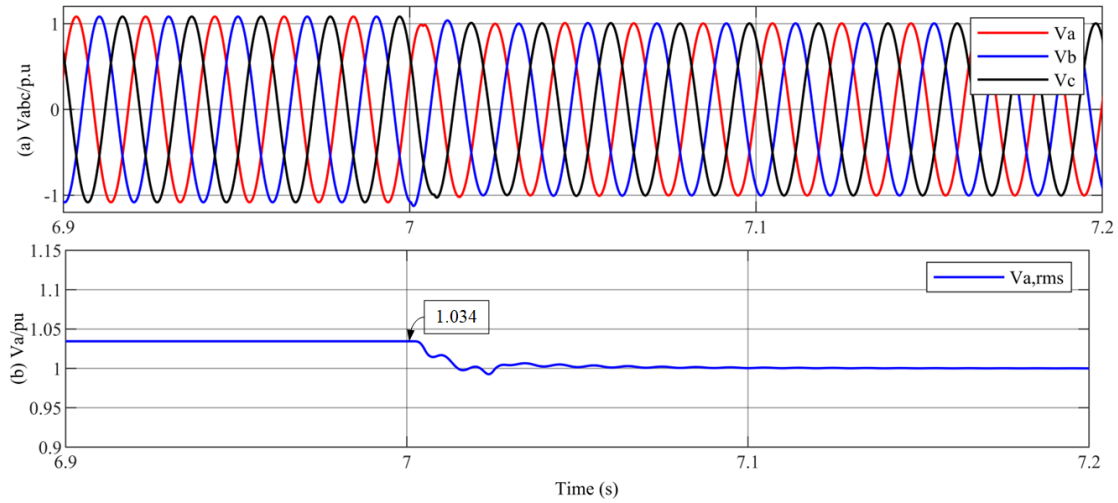


Fig. 2.23 Performance of the DC/AC converter under grid-forming operation during Event 7: a) load voltage (3-ph); b) phase A load voltage (rms value).

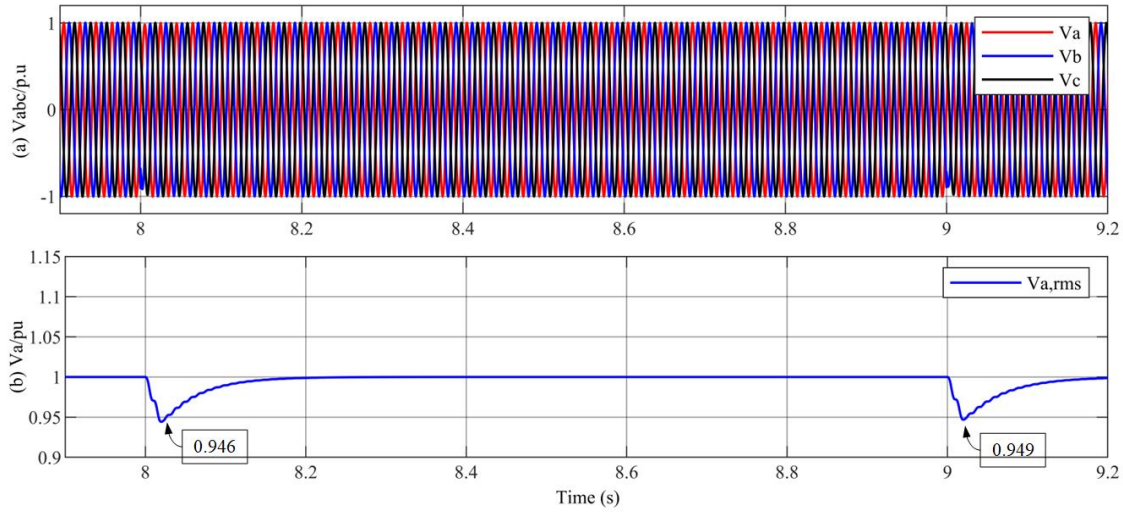


Fig. 2.24 Performance of the DC/AC converter under grid-forming operation during Event 8 and 9: a) load voltage (3-ph); b) phase A load voltage (rms value).

2.3 Summary

The basic control of a SST with three conversion stages under LV grid forming operation is illustrated in this chapter, with the control schemes of the AC/DC converter, DC/DC converter and DC/AC converter described. Wherein, a DC voltage control combined with inner current control is used for the AC/DC converter to regulate the MVDC voltage. For the DAB based DC/DC converter, SPS, EPS, DPS and TPS modulation schemes are reviewed to achieve bidirectional power flow and reduce the circulated reactive power. For the grid forming DC/AC converter, a dual closed loop, including outer AC voltage loop and inner AC current loop is used as the basic control to regulate the LVAC voltage, frequency and current. The system performance of the SST under grid forming operation is demonstrated and is shown that the SST achieves good voltage and current regulation during load step changes. The control and operation of the SST under grid-connected operation will be discussed in the following chapters.

Chapter 3 Optimal Droop Control for SST

The control and operation of SST connected with a LVAC network is under investigation. By cooperating with the CNOP, the SST performance under grid-connected operation is assessed. Wherein, a synchronisation procedure is designed to achieve the SST mode switch from grid forming to grid-connected condition. A universal control scheme for SST's low voltage DC/AC converter such that the same grid forming control structure can be used during both islanding operation and grid connected state through the CNOP. To eliminate the large transient brought by the switch of the controllers, the voltage and current controller remain in the control scheme under grid-connected operation. With adopting a $Q-v_{fd}$ and $P-v_{fq}$ droop control scheme, the active and reactive power of SST become controllable under grid-connected operation. To reduce the coupling between active and reaction power, an additional compensation control using active and reactive power feedforward compensation to dq-axis current components of the DC/AC converter is proposed. Based on the control scheme above, the SST-based distribution network can benefit distributed generation (DG) consumed locally. Simulation results are provided to confirm the overall SST performance and effectiveness of the proposed control schemes.

3.1 Concept of the CNOP

In distribution networks, conventional normally open points (CNOP) are designed for network re-configuration to balance feeders and loads [118]. A CNOP can connect two adjacent feeders to transfer loads from lightly loaded feeder to heavily loaded one, optimising network operation and minimising the loss and fault in the network. However, the power flow through CNOP is non-actively controlled, and the process of activating CNOP can take minutes [154]. Voltages at both ends of the CNOP could have different amplitude and phasor so care must be taken when closing CNOP to prevent large transient

current and the activation of overcurrent protection. It is noted here that the open and close of the CNOP is planned operation after checking voltage phasors.

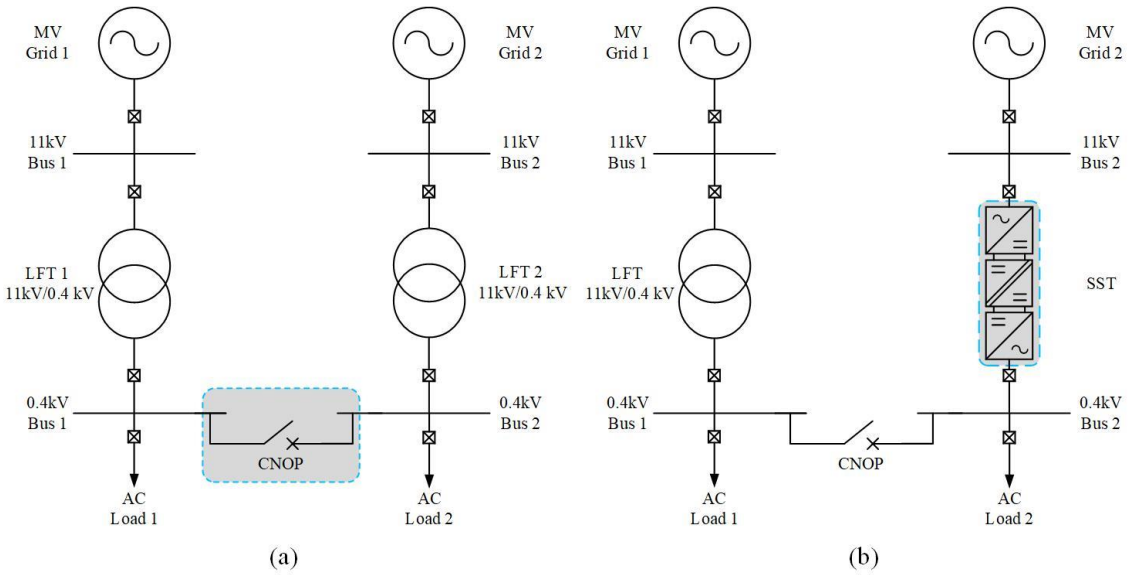


Fig. 3.1 Single line diagram of a simple distribution system. (a) CNOP integration; (b) typical network with SST integration.

Fig. 3.1(a) illustrates an example distribution system with an CNOP. As seen, AC Load 1 and AC Load 2 are connected to the 11 kV grid, MV Grid 1 and MV Grid 2 via two conventional low frequency power transformers, LFT 1 and LFT 2, respectively. The CNOP is installed between the 0.4 kV Bus 1 and 0.4 kV Bus 2. Once the CNOP is closed, depending on the load and network conditions of the two sub-systems, power can be exchanged between them through the CNOP.

In Fig. 3.1(b), an example distribution network where an SST replaces a LFT in one of the feeders and the use of the CNOP for connections at the LV networks is illustrated. As seen, AC Load 1 and AC Load 2 are connected to the 11 kV feeder, via the conventional LFT and SST, respectively. The CNOP is installed between the 0.4 kV Bus 1 and Bus 2. The SST considered contains three stages, including an AC/DC, DC/DC and DC/AC

converter stages. SST can supply AC Load 2 on its own (grid forming) while can also facilitate smooth connection and disconnection of the CNOP. When the CNOP is closed, the power transfer through CNOP can also be actively controlled by SST, thus the power dispatch to AC Load 1 and AC Load 2 can be optimised. The configuration in Fig. 3.1(b) is a good example to allow SST to optimise the power flow at 0.4kV Bus 1 and 2 with ON and OFF of CNOP. However, the basic control schemes of the SST as outlined in Chapter 2 need to be improved so as to automatically switch between grid forming and grid-connected operation.

3.2 Control requirement of the SST DC/AC converter for grid-connected operation

As illustrated in Chapter 2, when the secondary side of the SST supplies a separate network (CNOP is open), it is usually under grid-forming operation and the DC/AC converter generates a constant voltage and frequency output to the 0.4 kV Bus 2. It is likely that the voltage appears differently with that at Bus 1 in terms of the voltage amplitude, phase and frequency. Also, voltage control loop is typical excluded under grid-connected operation. Thus, direct close of the CNOP or switch voltage control loop to power control loop will cause large transient. To ensure seamlessly transients, the voltage amplitude, operation frequency and angle differences between Buses 1 and 2 need to be compensated by SST control before CNOP can be closed [155]. In addition, after the closure of the CNOP, the SST is expected to regulate the power exchange between MV Grid 1 and MV Grid 2.

To ensure the smooth transition and satisfactory operation of the SST under both grid-forming and grid-connected condition, an optimal control scheme for DC/AC converter is proposed, as illustrated in Fig. 3.2. The detailed function of the individual block is described as follows.

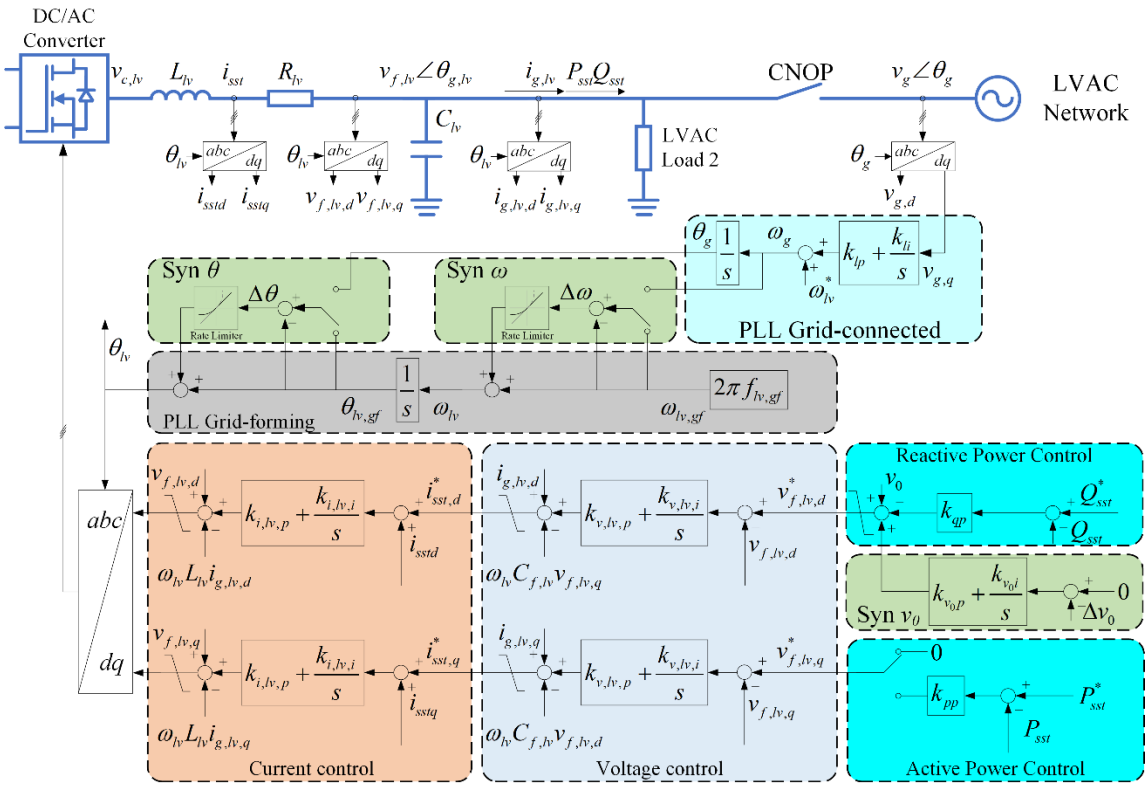


Fig. 3.2 Proposed universal grid forming control scheme for DC/AC converter.

3.2.1 Voltage and current control

To reduce large transients brought by the switch of the control variables, the voltage and current control loops under grid-connected operation remain the same as those under grid-forming operation. As previously described, under grid-forming operation, the voltage amplitude of the LVAC network is determined by the d-axis reference of the VSC filter voltage $v^*_{f,lv,d}$, while the q-axis reference $v^*_{f,lv,q}$ is normally zero [156]. Differently, the dq voltage references, $v^*_{f,lv,d}$ and $v^*_{f,lv,q}$ are generated by secondary control loops in the grid-connected mode, as will be described in the following sections.

3.2.2 Phase Locked Loop (PLL) and grid synchronisation

When the CNOP is open, the DC/AC converter operates as a grid-forming converter and the converter output voltage does not need to be synchronized to any external source. Thus, a fixed frequency can be used to generate the required voltage position angle as described in Chapter 2 and shown in Fig. 3.2. Meanwhile, when the DC/AC converter need to switch its control scheme from grid forming to grid-connected before closing the CNOP. The output voltage is required to be synchronized to the voltage at the other side of the CNOP, where a PLL is needed. The PLL has been widely used for grid synchronisation. In Fig. 3.2, a conventional synchronous reference frame PLL is implemented [157]. By solving $v_{f,lv,q}$ equals to zero, the grid angular frequency ω_g is determined and the phase angle at grid side θ_g is determined after ω_g passes through the integrator.

As the voltage and operation frequency can be different between the SST output and grid side, a smooth transition before closing the CNOP is required to avoid large current transients. Thus, the PLL needs to be modified accordingly, where it consists of the block Syn ω, Syn θ and Syn v_0, illustrated in Fig. 3.2. Wherein, the angular frequency, angle and voltage amplitude difference, $\Delta\omega$, $\Delta\theta$ and Δv_0 are zero under grid forming operation since the references are the same constant value by default. During the grid synchronisation process, ω_g is introduced into Syn ω. To adjust the reference angular frequency from $\omega_{lv,gf}$ to ω_g without triggering the protection system, a rate limiter is introduced for $\Delta\omega$. The compensation of $\Delta\theta$ by switching the reference angle from $\theta_{lv,gf}$ to θ_g is similar with the that of $\Delta\omega$ compensation. For the voltage amplitude difference, Δv_0, is compensated to zero by a PI controller inside of the $Q_{sst} - v_{f,lv,d}$ control, illustrated as Syn v_0 block in Fig. 3.2, leading the voltage amplitude reference v_0 to v_g.

The effect on synchronisation speed according to different chronological order of the $\Delta\omega$, $\Delta\theta$ and Δv_0 compensation will be discussed in Section 3.3.

3.2.3 Active and reactive power control

Active and reactive power control scheme for SST is specifically required when the CNOP is closed and the LV side is grid connected. As previously described, in order to avoid control mode switching during the ON and OFF of CNOP, a universal grid forming approach is adopted for both operation conditions. The droop control is widely applied for active and reactive power control due to its better reliability and avoidance of communication links. The principle of the droop control is to adjust the output voltage and frequency in functions of active and reactive power delivered by the inverter [156]. Considering the inductive line impedance, the active and reactive power can be controlled by angular frequency and voltage magnitude difference between inverter output voltage $v_{f,lv}$ and the grid voltage v_g. Learning from the conventional $P-\omega$ and $Q-v$ droop control to balance any increase in load by reducing the frequency and voltage amplitude of the system according to the droop characteristics, derived as

$$\omega_{lv}^{*} - \omega_{lv} = -k_p \left(P_{sst}^{*} - P_{sst} \right) \tag{3.1}$$

$$v_{f,lv}^{*} - v_{f,lv} = -k_{qp} \left(Q_{sst}^{*} - Q_{sst} \right) \tag{3.2}$$

Wherein, ω_{lv} and ω_{lv}^{*} are the real and rated value of the DC/AC converter angular frequency. $v_{f,lv}$ and $v_{f,lv}^{*}$ are real and rated value of the DC/AC converter output voltage amplitude. P_{sst} and P_{sst}^{*} are real and rated active power of the inverter. Q_{sst} and Q_{sst}^{*} real and rated reactive power of the SST. k_{qp} and k_p are droop coefficients, respectively. The selection of the droop coefficients needs to be designed properly since they make an influence on the network stability. Generally, the droop coefficients can be estimated as

$$k_p = \frac{\Delta\omega}{2P_{\max}} \tag{3.3}$$

$$k_{qp} = \frac{\Delta v}{2Q_{\max}} \tag{3.4}$$

Wherein, $\Delta\omega$ and Δv are maximum allowed angular frequency and voltage amplitude. $P_{\max}$ and $Q_{\max}$ are maximum allowed active power and reactive power of the DC/AC converter. The $P-\omega$ and $Q-v$ droop can be considered to regulate active and reactive power output of SST.

To reduce the possibly large transient brought by switching the control scheme, the voltage and current control loop under grid-connected operation remain the same as that under grid forming operation. This necessitates the implementation of the active and reactive power controller to the existing control scheme.

As the d-axis of the PLL is aligned to the grid voltage, the reactive power control generates the d-axis AC voltage reference $v^*_{f,lv,d}$, as illustrated in the reactive power control block in Fig. 3.2. Meanwhile, with the additional Syn v_0 block, the voltage reference of the reactive power controller can be smoothly moved from $v^*_{f,lv}$ to v_g in grid synchronisation.

Due to the existence of the PLL and inner AC voltage control loop, in the proposed design, the active power control directly generates the q-axis voltage reference $v^*_{f,lv,q}$, as illustrated in the active power control block in Fig. 3.2, as:

$$v^*_{f,lv,q} = k_{pp}\left(P^*_{sst} - P_{sst}\right) \tag{3.5}$$

wherein, k_{pp} is the proportional control coefficient. In such as design, when the active power output of SST needs to change, the q-axis voltage of the converter output will be changed accordingly, which effectively change the phase of the converter output AC voltage. Consequently, the phase shift between the converter output and AC network

changes which leads to the change of the SST active power output. For example, when $P_{sst} < P_{sst}^{*}$ (i.e., P_{sst} needs to be increased and $v_{f,lv,q}^{*} > 0$), the following control actions are taking place:

- The proportional controller produces a positive $v_{f,lv,q}^{*}$ for the voltage control, illustrated in Fig. 3.2.
- As $v_{f,lv,q}$ is zero due to the action of PLL, the AC voltage controller produces a q-axis current order such that a transient positive $v_{f,lv,q}$ is created.
- The positive $v_{f,lv,q}$ will lead the acceleration of the phase of the converter output, resulting in increased SST active power output P_{sst}.
- The action will only stop when $P_{sst} = P_{sst}^{*}$.

Similarly, when $P_{sst} > P_{sst}^{*}$ (i.e., P_{sst} needs to be reduced and $v_{f,lv,q}^{*} < 0$), the proportional controller produces a negative $v_{f,lv,q}^{*}$ and a transient negative $v_{f,lv,q}$. Thus, the decelerated phase of the converter output voltage leads to P_{sst} reduction.

Thus, the decelerated ω_{lv} leads the reducing P_{sst} correspondingly. The performance of the proposed $P_{sst} - v_{f,lv,q}$ droop control will be assessed in section 4.3.

3.3 Simulation performance under grid-connected operation

3.3.1 Simulation performance of the synchronisation procedure

The synchronisation procedure of SST before applying grid connected operation is evaluated in this subsection. The tested two feeder distribution system configuration is

illustrated in Fig. 3.3. Wherein, LVAC Load 1 and Load 2 are connected with MV Grid 1 and MV Grid 2 through LFT and SST (rated power: 10 MW) respectively. An CNOP is located between the two LVAC buses. The key parameters of the tested network are listed in Table 3.1. The detailed parameters of the SST converter can be found in Table 2.2 (Page 48) in Chapter 2.

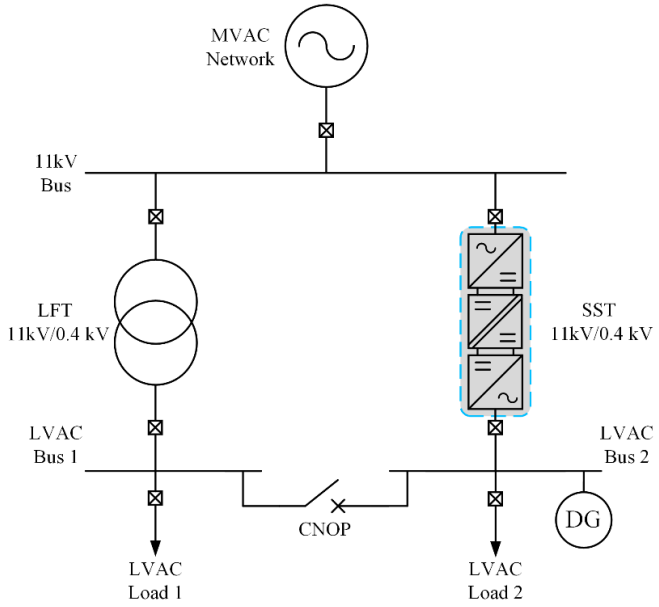


Fig. 3.3 Tested SST-based network.

Table 3.1 Main parameters of the tested network

Parameter	Value
Rated power of SST	10 MW
Rated voltage at LVAC Network 1	0.96 pu
LVAC Load 1	(6 MW, 0 MVar)
LVAC Load 2	(8 MW, 0 MVar)
Power output of DG	(0 MW, 0 MVar)
LVAC Network 1 frequency f_g	49.5 Hz
Grid forming operation frequency f_{lv}	50 Hz

Table 3.2 Synchronisation procedure schedules

Scheme	0-0.5 s	0.5-0.7 s	0.7-0.9 s	0.9-1.1 s	1.1s
1	Grid forming	Syn $\Delta\omega$	Syn $\Delta\theta$	Syn Δv_0	CNOP closed
2	Grid forming	Syn $\Delta\omega$	Syn Δv_0	Syn $\Delta\theta$	CNOP closed
3	Grid forming	Syn Δv_0	Syn $\Delta\omega$	Syn $\Delta\theta$	CNOP closed
4	Grid forming	Syn Δv_0	Syn $\Delta\theta$	Syn $\Delta\omega$	CNOP closed
5	Grid forming	Syn Δv_0	$\Delta\theta+\Delta\omega$		CNOP closed

Five synchronisation procedures according to different compensation order for optimisation and are scheduled in
Table 3.2. The description and analysis of each scheme are shown below.

Scheme 1: The $\Delta\omega$, $\Delta\theta$ and Δv_0 are compensated for $0.2s$ in succession, and the synchronisation is designed to complete in $0.6s$. Phase A voltage at SST output $v_{f,lv}$ and 0.4 kV Bus 1 v_g are compared and illustrated together in Fig. 3.4(a). The RMS voltage of $v_{f,lv}$ and v_g are compared and illustrated together in Fig. 3.4(b).

During 0-0.5 s, the DC/AC converter in the SST operates under grid-forming operation and generates 50 Hz AC voltage output. As the LVAC voltage frequency is assumed to be 49.5 Hz, the phase difference between $v_{f,lv}$ and v_g are not constant due to the 0.5 Hz difference, thus the angle difference between $v_{f,lv}$ and v_g are time-varying, illustrated in Fig. 3.4(d).

From $t=0.5s$, the synchronisation procedure starts, and the compensation of the angular frequency is activated firstly. The frequency of the LVAC network is measured and $\Delta\omega$

in the block Syn ω (illustrated in Fig. 3.2) is switched from 0 to $\omega_g - \omega_{lv,gf}$, which is corresponding frequency of -0.5 Hz. The difference is injected into ω_{lv} through a rate limiter, illustrated in Fig. 3.4(c). Once ω_{lv} is compensated from $\omega_{lv,gf}$ to ω_g, the phase difference between $v_{f,lv}$ and v_g is settled, illustrated in Fig. 3.4(d). The ω compensation is completed in $0.2s$.

From $t = 0.7s$, the synchronisation of angle proceeds, $\Delta\theta$ in the block Syn θ (illustrated in Fig. 3.2) is switched from 0 to $\theta_g - \theta_{lv,gf}$. The difference is injected into θ_{lv} through the rate limiter. A slight fluctuation (~3.3%) occurred at the phase A voltage (RMS value) since the variational angle affects RMS calculation, illustrated in Fig. 3.4(b). Once θ_{lv} is compensated from $\theta_{lv,gf}$ to θ_g, the angle difference between $v_{f,lv}$ and v_g is cleared, illustrated in Fig. 3.4(d). The θ compensation is completed in $0.2s$.

From $t = 0.9s$, the synchronisation of voltage amplitude lastly proceeds. Before that, Δv_0 in the block Syn v_0 (illustrated in Fig. 3.2) equals to zero, where the voltage amplitude compensation controller can be considered dormant. Δv_0 is switched to the difference between $v_{f,lv}$ and v_g. The PI controller in the block Syn v_0 (illustrated in Fig. 3.2) starts to work and amplitude difference is compensated, illustrated in Fig. 3.4(b). Once v_0 is compensated from $v_{f,lv}$ to v_g, the synchronisation process is completed and there is no difference between $v_{f,lv}$ and v_g.

From $t = 1.1s$, the CNOP is closed. As $v_{f,lv}$ and v_g has no difference, the active power output of the SST remains the same as the condition before the CNOP is open, illustrated in Fig. 3.4(e). Meanwhile, there is a slight fluctuation (<1%) of the reactive power output of the SST, illustrated in Fig. 3.4(f).

In Fig. 3.5, the performance of the SST during the synchronisation procedure is illustrated. Wherein, the SST remains normal operation during the compensation of the frequency. Fluctuations in q-axis voltage controller and the corresponding q-axis current controller are assessed, illustrated in Fig. 3.5(b)(d). During the synchronisation of angle, the angle experienced an acceleration when angular difference was injected and a deceleration when the injected angle reached to the fixed angular difference. According to the $\omega_{lv} - v_{f,lv,q}$ relationship, the two-time rate of change of the angle will lead to change of the q-axis voltage, thus the fluctuation of the q-axis current controller. On the other hand, d-axis voltage and the corresponding current controller is not affected, illustrated in Fig. 3.5(a)(c). During the synchronisation of the voltage amplitude, the voltage and current controller in DC/AC converter, LVDC voltage controller in DC/DC converter and the MVDC voltage controller in AC/DC converter appear slight fluctuation and go back to normal operation shortly, illustrated in Fig. 3.5. When the CNOP is closed, all the controllers remain the normal operation.

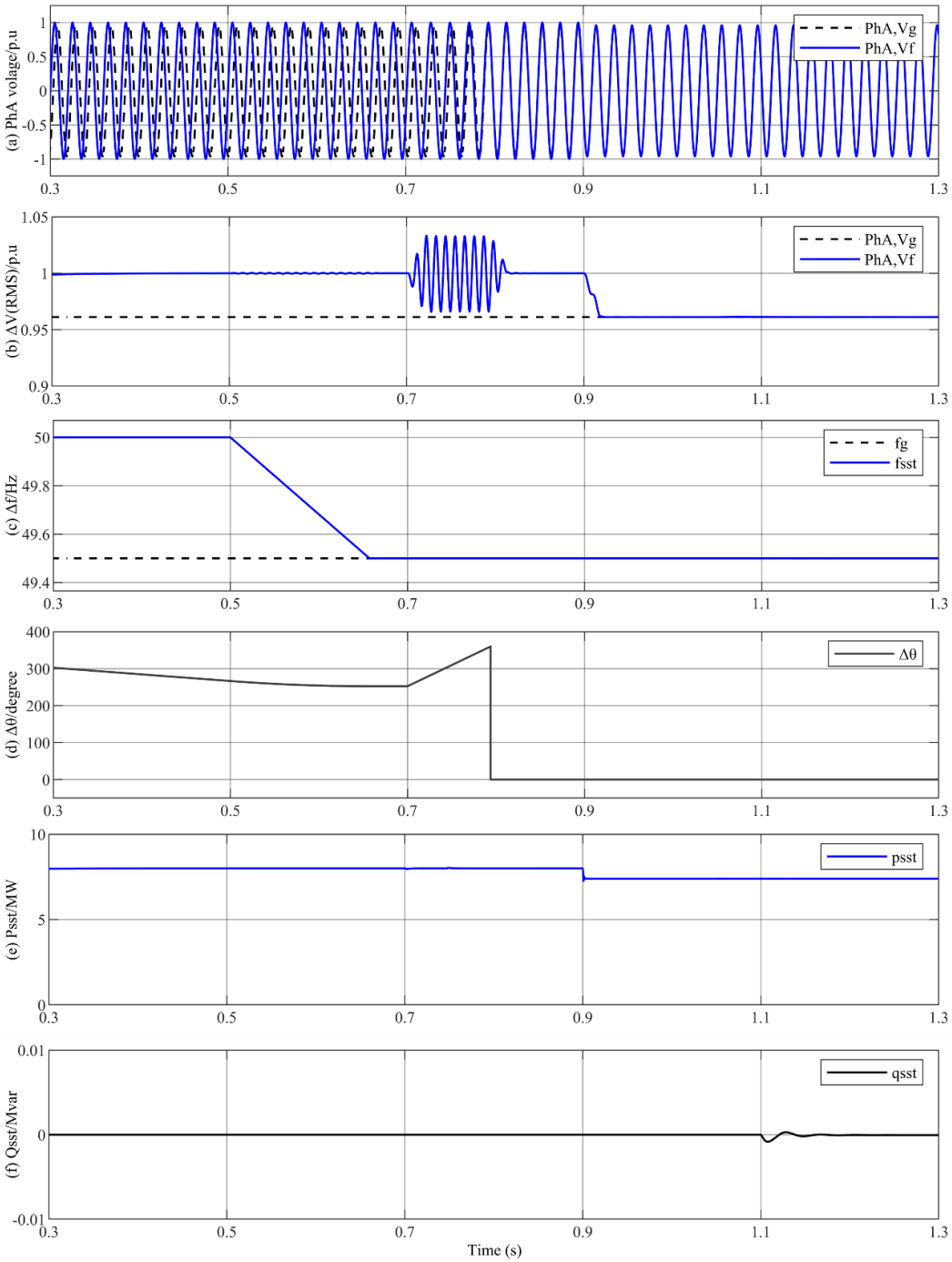


Fig. 3.4 Phase A voltage during synchronisation process under scheme 1: (a) SST output Phase A voltage v_f and 0.4 kV Bus 1 voltage v_g; (b) voltage difference (RMS) between $v_{f,lv}$ and v_g; (c) frequency difference between $v_{f,lv}$ and v_g; (d) angle difference between $v_{f,lv}$ and v_g; (e) SST output active power; (f) SST output reactive power.

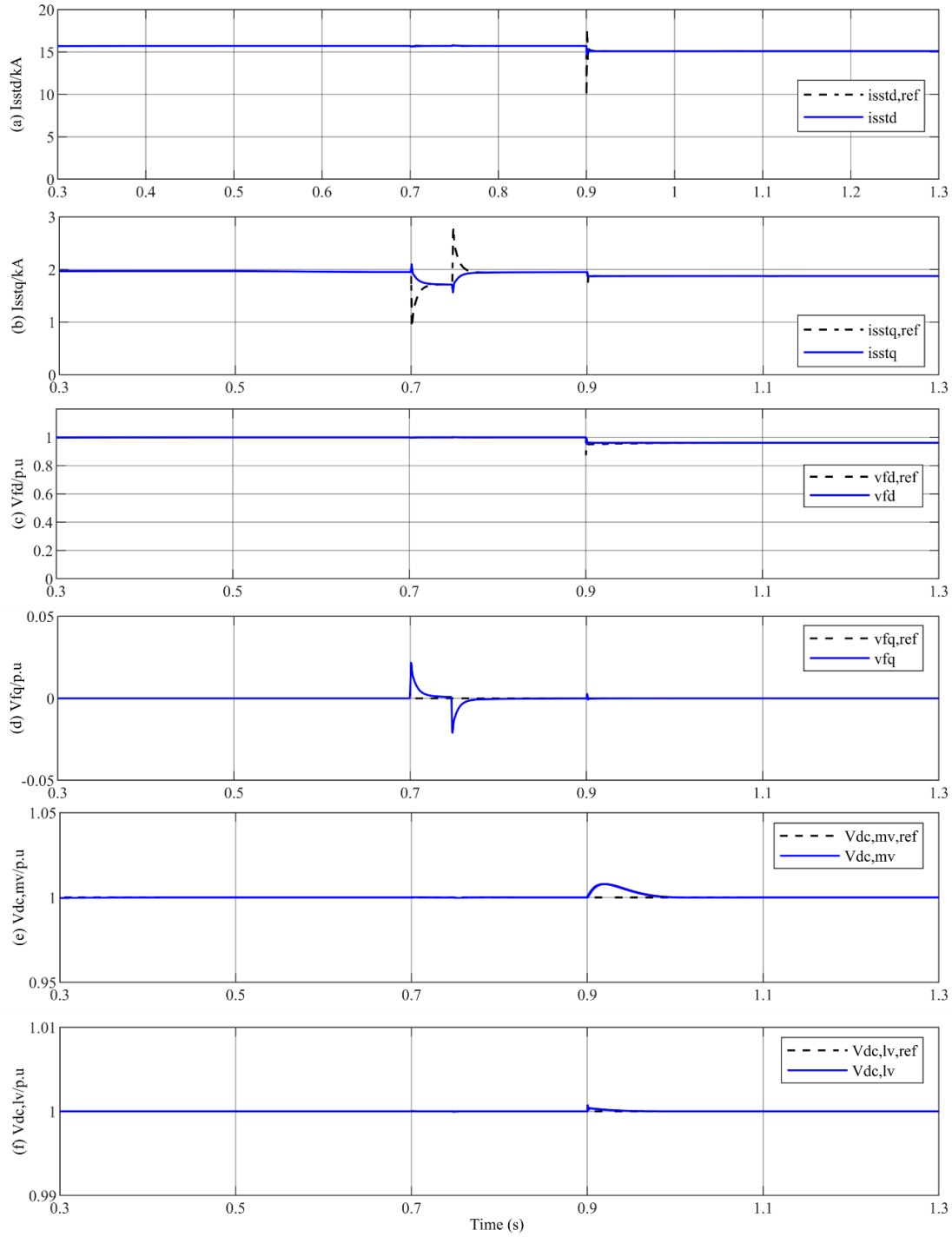


Fig. 3.5 Performance of the SST during synchronisation procedure under scheme 1: (a) DC/AC output d-axis current; (b) DC/AC output q-axis current; (c) DC/AC output d-axis voltage; (d) DC/AC output q-axis voltage; (e) medium voltage DC; (f) low voltage DC.

Scheme 2: The synchronisation order is adjusted to $\Delta\omega$, Δv_0 and $\Delta\theta$ for $0.2s$ in succession. Phase A voltage at SST output $v_{f,lv}$ and 0.4 kV Bus 1 v_g are illustrated in Fig. 3.6(a). The RMS voltage of $v_{f,lv}$ and v_g are compared and illustrated together in Fig. 3.6(b).

During 0-0.5 s, the performance under scheme 2 is similar with that under scheme 1.

From $t = 0.5s$, the synchronisation of $\Delta\omega$ proceeds, illustrated in Fig. 3.6(c). The process of $\Delta\omega$ compensation is similar with the situation under scheme 1. Once ω_{lv} is compensated from $\omega_{lv,gf}$ to ω_g, the phase difference between $v_{f,lv}$ and v_g is settled, illustrated in Fig. 3.6(d).

From $t = 0.7s$, the synchronisation of Δv_0 proceeds. The detailed process is the same as that under scheme 1. Once v_0 is compensated from $v_{f,lv}$ to v_g, the voltage amplitude difference between $v_{f,lv}$ and v_g is cleared, illustrated in Fig. 3.6(b).

From $t = 0.9s$, the synchronisation of $\Delta\theta$ proceeds. The detailed process is the same as that under scheme 1, and the process is illustrated in Fig. 3.6(d). A slight fluctuation (~3.2%) occurred at the phase A voltage (RMS value) since the variational angle affects RMS calculation, illustrated in Fig. 3.6(b). Once θ_{lv} is compensated from $\theta_{lv,gf}$ to θ_g, the synchronisation procedure is completed and there is no difference between $v_{f,lv}$ and v_g, illustrated in Fig. 3.6(a).

From $t = 1.1s$, the CNOP is closed. As $v_{f,lv}$ and v_g has no difference, the active power output of the SST remains the same as the condition before the CNOP is open, illustrated

in Fig. 3.6(e). Meanwhile, there is a slight fluctuation (<1%) of the reactive power output of the SST, illustrated in Fig. 3.6(f).

In Fig. 3.7, the performance of the SST during the synchronisation process is illustrated. Comparing with scheme 1, the synchronisation process of the ω, v_0 and θ is similar with no influence on the transposition between Δv_0 and $\Delta\theta$. For the compensation of the frequency, controllers in SST all remain the normal operation, illustrated in Fig. 3.7. The compensation of the voltage amplitude results the fluctuation of all the controllers, which get recovered in a very short time, illustrated in Fig. 3.7. For the compensation of angle, two-time rate of change of the angle leads to fluctuation of the q-axis voltage, thus the fluctuation of the q-axis current controller, illustrated in Fig. 3.7(b)(d).

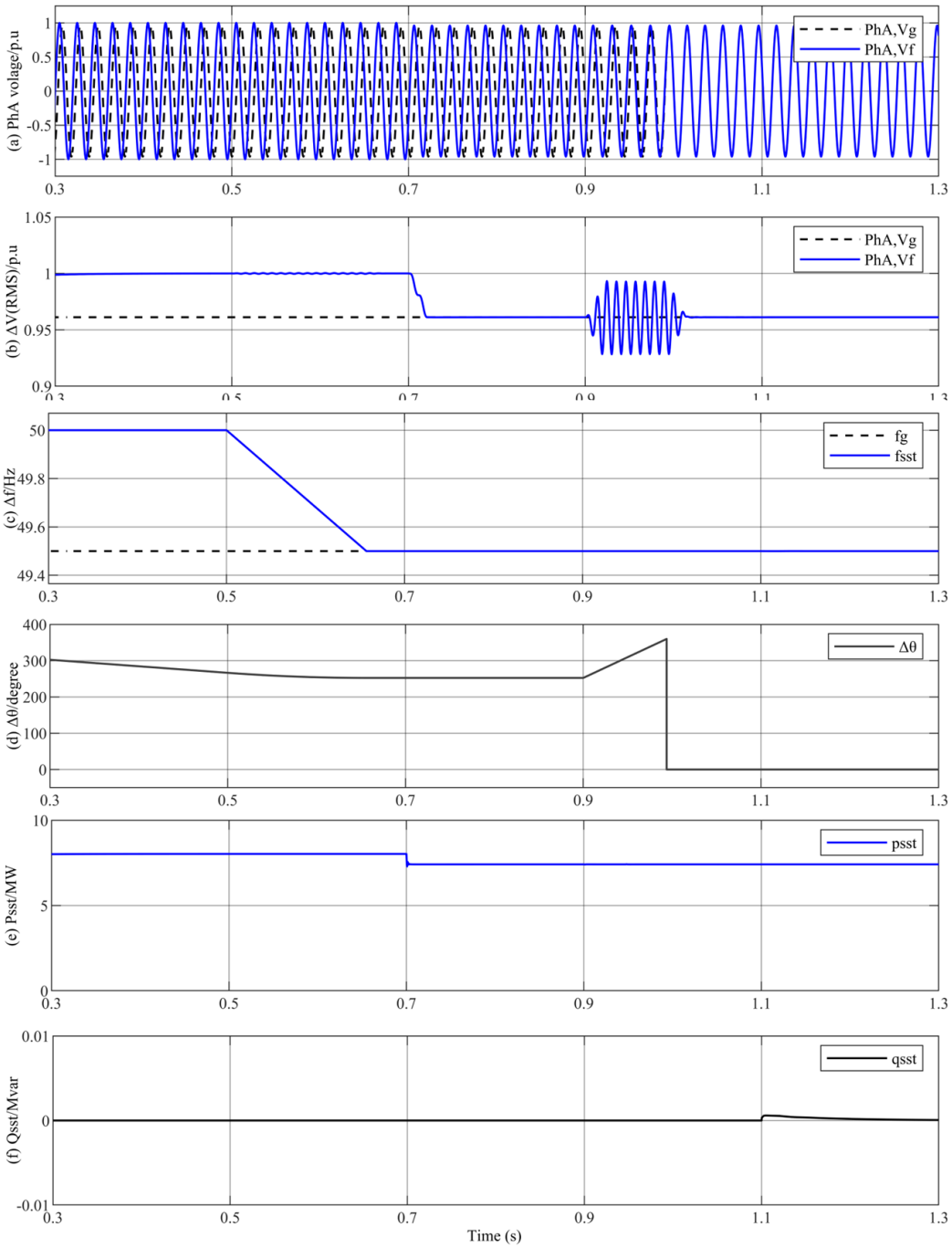


Fig. 3.6 Phase A voltage during synchronisation process under scheme 2: (a) SST output Phase A voltage v_f and 0.4 kV Bus 1 voltage v_g; (b) voltage difference (RMS) between v_f and v_g.(c) frequency difference between $v_{f,lv}$ and v_g; (d) angle difference between $v_{f,lv}$ and v_g; (e) SST output active power; (f) SST output reactive power.

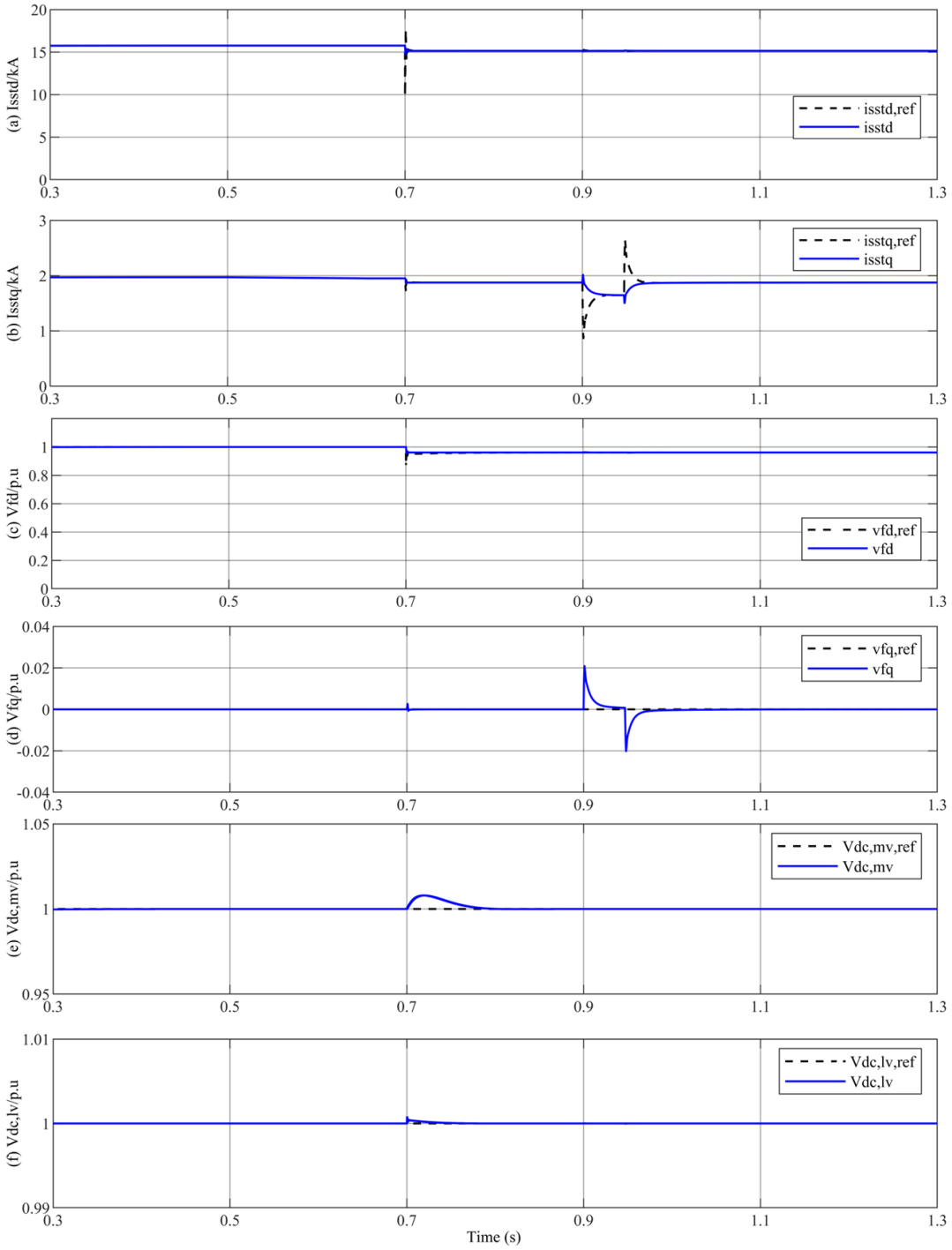


Fig. 3.7 Performance of the SST during synchronisation procedure under scheme 2: (a) DC/AC output d-axis current; (b) DC/AC output q-axis current; (c) DC/AC output d-axis voltage; (d) DC/AC output q-axis voltage; (e) medium voltage DC; (f) low voltage DC.

Scheme 3: The compensation order is adjusted to Δv_0 , $\Delta\omega$ and $\Delta\theta$ for $0.2s$ in succession. Phase A voltage at SST output $v_{f,lv}$ and 0.4 kV Bus 1 v_g are illustrated in Fig. 3.8(a). The RMS voltage of $v_{f,lv}$ and v_g are compared and illustrated together in Fig. 3.8(b).

During 0-0.5 s, the performance under scheme 3 is similar with that under scheme 1.

From $t = 0.5s$, the synchronisation of Δv_0 firstly proceeds. The detailed process is the same as that under scheme 1. Once v_0 is compensated from $v_{f,lv}$ to v_g , the voltage amplitude difference between $v_{f,lv}$ and v_g is cleared, illustrated in Fig. 3.8(b).

From $t = 0.7s$, the synchronisation of $\Delta\omega$ proceeds. The detailed process is illustrated in Fig. 3.8(c), which is similar with the situation under scheme 1. Once ω_{lv} is compensated from $\omega_{lv,gf}$ to ω_g , the angle difference between $v_{f,lv}$ and v_g is settled, illustrated in Fig. 3.8(d).

From $t = 0.9s$, the synchronisation of $\Delta\theta$ proceeds. The detailed process is the same as that under scheme 1, and the process is illustrated in Fig. 3.8(d). A slight fluctuation (~3.3%) occurred at the phase A voltage (RMS value) since the variational angle affects RMS calculation, illustrated in Fig. 3.8(b). Once θ_{lv} is compensated from $\theta_{lv,gf}$ to θ_g , the synchronisation procedure is completed and there is no difference between $v_{f,lv}$ and v_g , illustrated in Fig. 3.8(a).

From $t = 1.1s$, the CNOP is closed. As $v_{f,lv}$ and v_g has no difference, the active power output of the SST remains the same as the condition before the CNOP is open, illustrated

in Fig. 3.8(e). Meanwhile, there is a slight fluctuation (<1%) of the reactive power output of the SST, illustrated in Fig. 3.8(f).

In Fig. 3.9, the performance of the SST during the synchronisation process is illustrated. The synchronisation process of the $\Delta\omega$, Δv_0 and $\Delta\theta$ is similar with scheme 1 with no influence on the transposition of the v_0. During the compensation of $\Delta\omega$, all the controllers in SST remain the normal operation, illustrated in Fig. 3.9(a)-(f). The compensation of Δv_0 results the fluctuation of all the controllers, which get recovered in a very short time, illustrated in Fig. 3.9(a)-(f). During the compensation of $\Delta\theta$, two-time rate of change of the angle leads to fluctuation of the q-axis voltage, thus the fluctuation of the q-axis current controller, illustrated in Fig. 3.9(b)(d).

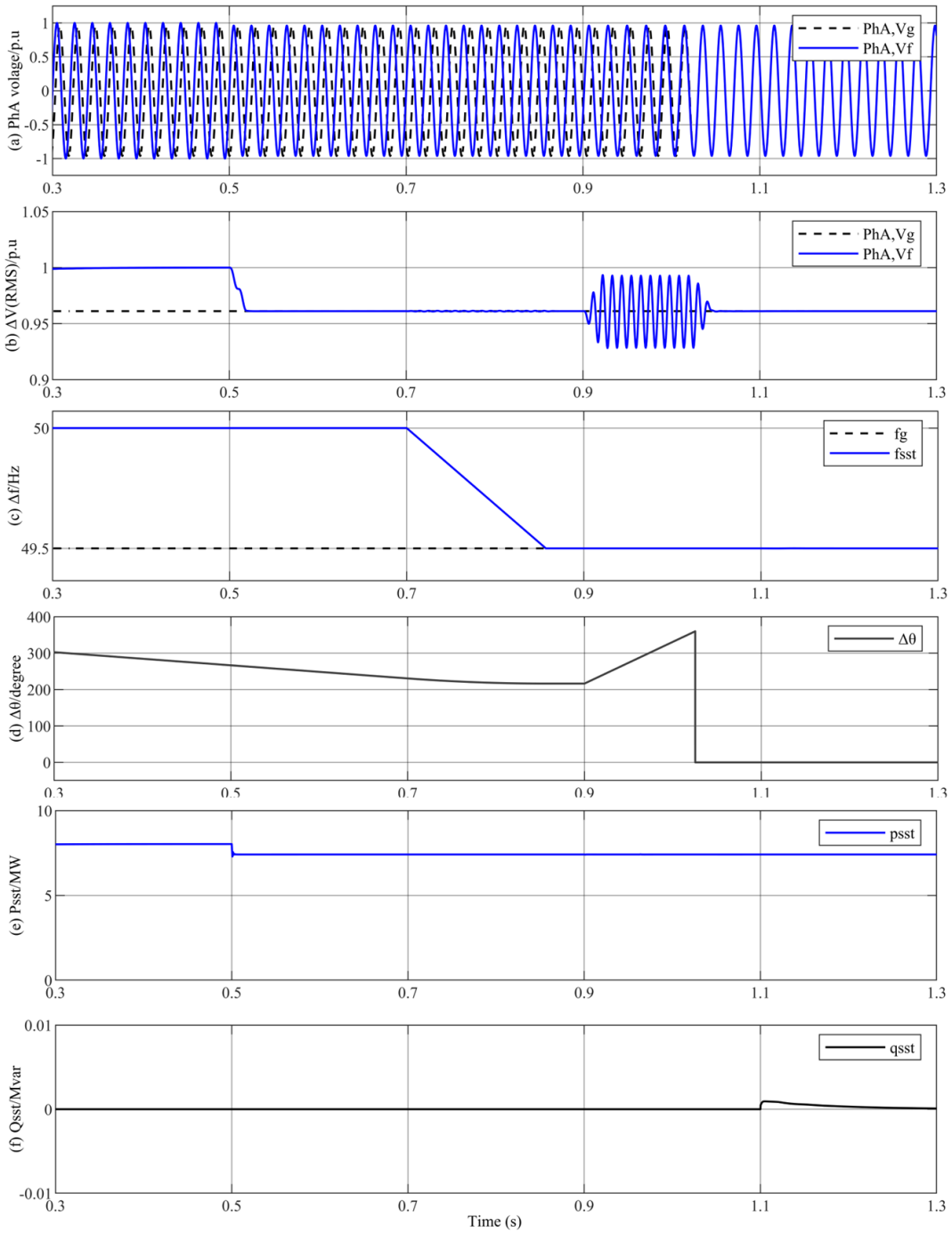


Fig. 3.8 Phase A voltage during synchronisation process under scheme 3: (a) SST output Phase A voltage v_f and 0.4 kV Bus 1 voltage v_g; (b) voltage difference (RMS) between v_f and v_g; (c) frequency difference between $v_{f,lv}$ and v_g; (d) angle difference between $v_{f,lv}$ and v_g; (e) SST output active power; (f) SST output reactive power.

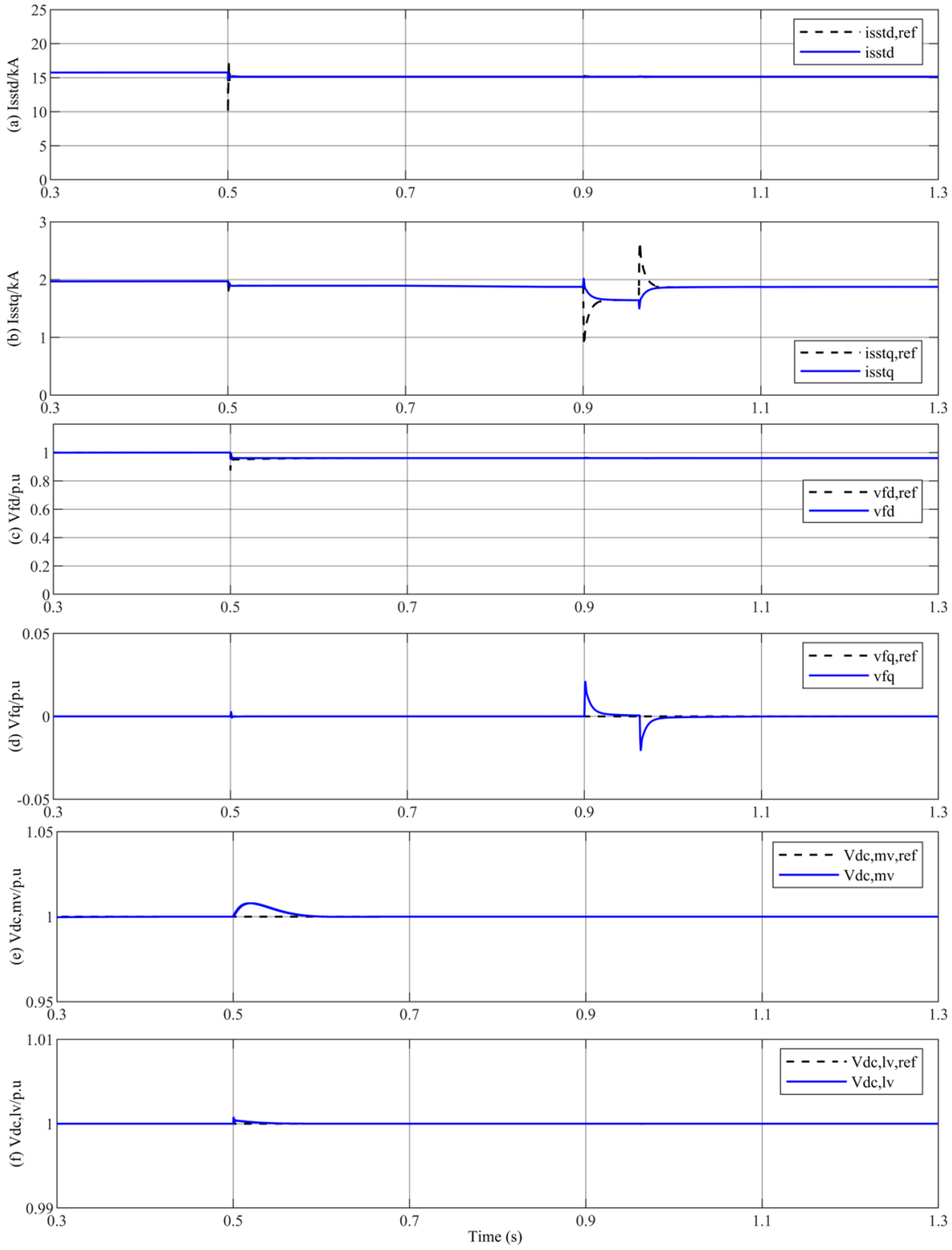


Fig. 3.9 Performance of the SST during synchronisation procedure under scheme 3: (a) DC/AC output d-axis current; (b) DC/AC output q-axis current; (c) DC/AC output d-axis voltage; (d) DC/AC output q-axis voltage; (e) medium voltage DC; (f) low voltage DC.

Scheme 4: The compensation order is adjusted to Δv_0 , $\Delta\theta$ and $\Delta\omega$ for 0.2*s* in succession. Phase A voltage at SST output $v_{f,lv}$ and 0.4 kV Bus 1 v_g are illustrated in Fig. 3.10(a). The RMS voltage of $v_{f,lv}$ and v_g are compared and illustrated together in Fig. 3.10(b).

During 0-0.5 s, the performance under scheme 4 is similar with that under scheme 1.

From $t = 0.5s$, the synchronisation of Δv_0 firstly proceeds. The detailed process is the same as that under scheme 1. Once v_0 is compensated from $v_{f,lv}$ to v_g , the voltage amplitude difference between $v_{f,lv}$ and v_g is cleared, illustrated in Fig. 3.10 (b).

From $t = 0.7s$, the synchronisation of $\Delta\theta$ proceeds. Compared with scheme 3, the angle difference is changed from a constant value to a variation, illustrated in Fig. 3.10(d), since $\Delta\theta$ compensation proceeds in advance of $\Delta\omega$ compensation, As a result, the synchronisation of $\Delta\theta$ does not only compensate the angle difference but also the angular frequency difference. The consistent $v_{f,lv}$ and v_g after $\Delta\theta$ compensation also show the result, illustrated in Fig. 3.10(a). A slight fluctuation (~3.2%) occurred at the phase A voltage (RMS value) since the variational angle affects RMS calculation, illustrated in Fig. 3.10(b). Once $\Delta\theta$ is compensated, there is no difference between $v_{f,lv}$ and v_g , illustrated in Fig. 3.10(a).

From $t = 0.9s$, the synchronisation of the $\Delta\omega$ proceeds. A slight fluctuation (~0.3%) occurred at the phase A voltage (RMS value) since the variational angular frequency affects RMS calculation, illustrated in Fig. 3.10(b). Once the ω_{lv} is changed to ω_g , the synchronisation procedure is completed, illustrated in Fig. 3.10(a).

From $t = 1.1s$, the CNOP is closed. As $v_{f,lv}$ and v_g has no difference, the active power output of the SST remains the same as the condition before the CNOP is open, illustrated

in Fig. 3.10(e). Meanwhile, there is a slight fluctuation (<1%) of the reactive power output of the SST, illustrated in Fig. 3.10(f).

In Fig. 3.11, the performance of the SST during the synchronisation process is illustrated. During the compensation of the voltage amplitude, the resulted fluctuation of all the controllers, which get recovered in a very short time, is similar with that under other schemes, illustrated in Fig. 3.11(a)-(f). During the compensation of the $\Delta\theta$, the similar two-time rate of change of the angle leads to twice fluctuation of the q-axis voltage, thus the fluctuation of the q-axis current controller, illustrated in Fig. 3.11(b)(d). During the compensation of $\Delta\omega$, all the controllers in SST remain the normal operation, illustrated in Fig. 3.11(a)-(f).

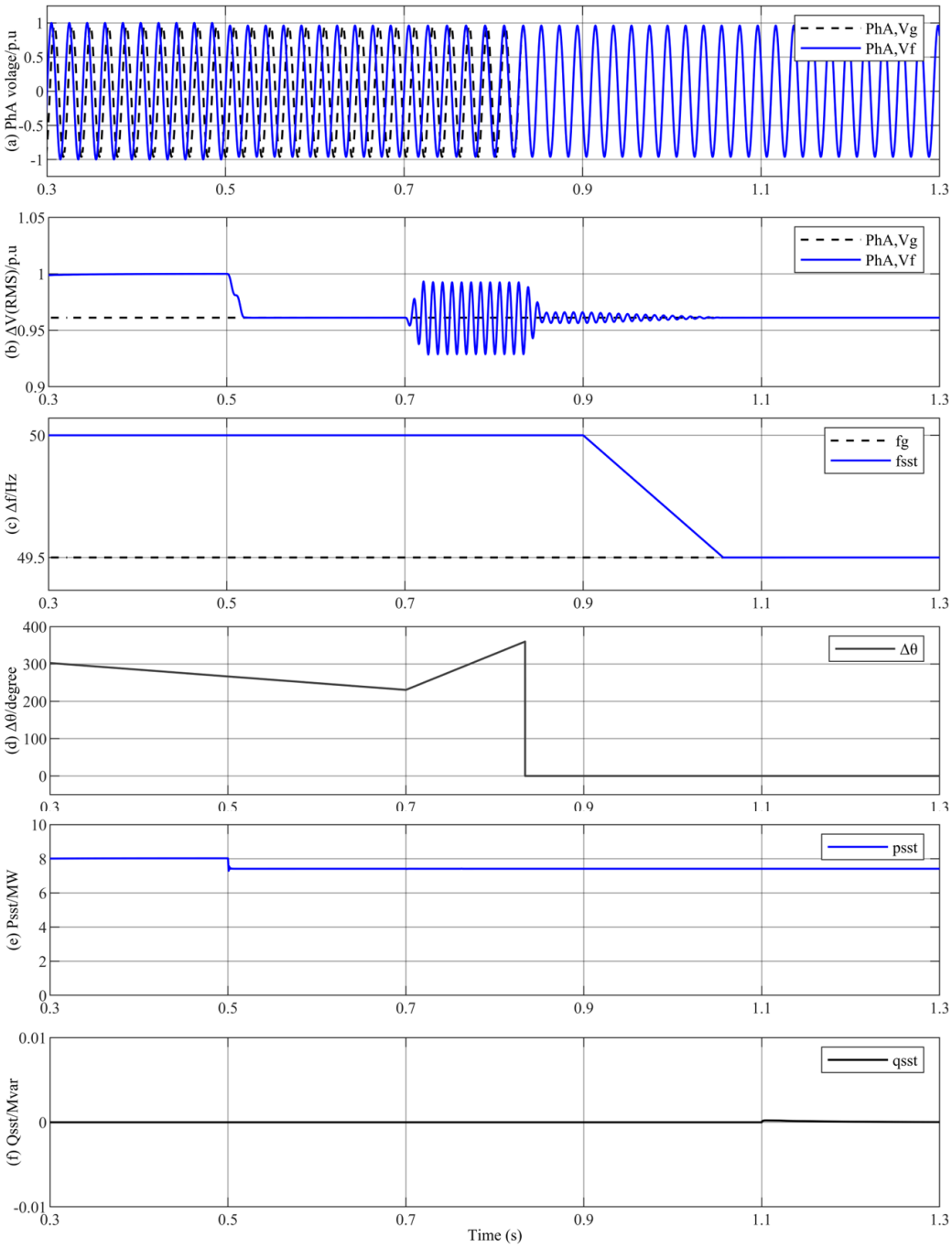


Fig. 3.10 Phase A voltage during synchronisation process under scheme 4: (a) SST output Phase A voltage v_f and 0.4 kV Bus 1 voltage v_g; (b) voltage difference (RMS) between v_f and v_g; (c) frequency difference between $v_{f,lv}$ and v_g; (d) angle difference between $v_{f,lv}$ and v_g; (e) SST output active power; (f) SST output reactive power.

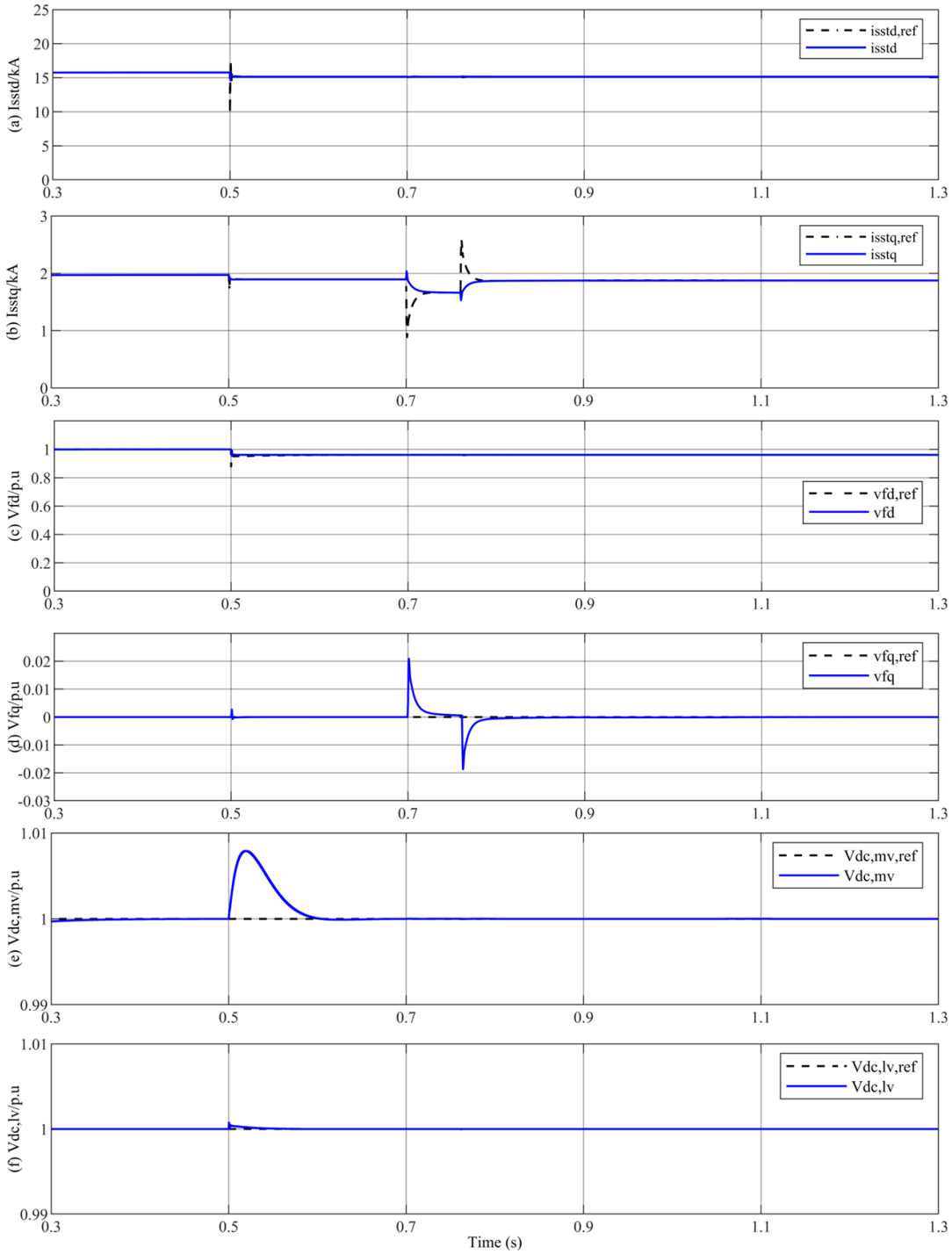


Fig. 3.11 Performance of the SST during synchronisation procedure under scheme 4: (a) DC/AC output d-axis current; (b) DC/AC output q-axis current; (c) DC/AC output d-axis voltage; (d) DC/AC output q-axis voltage; (e) medium voltage DC; (f) low voltage DC.

Scheme 5: The synchronisation of $\Delta\theta$ and $\Delta\omega$ will proceed at the same time with the order of Δv_0, $\Delta\theta+\Delta\omega$ for in succession. Phase A voltage at SST output $v_{f,lv}$ and 0.4 kV Bus 1 v_g are illustrated in Fig. 3.12(a). The RMS voltage of $v_{f,lv}$ and v_g are compared and illustrated together in Fig. 3.12(b).

During 0-0.7 s, the performance under scheme 5 is the same as that under scheme 4.

From $t=0.7s$, the synchronisation of $\Delta\theta$ and $\Delta\omega$ proceed. The detailed process is similar with the synchronisation of $\Delta\theta$ under scheme 4.

The angle difference is changed from a constant value to a variation, which is similar with scheme 4, illustrated in Fig. 3.12(d). A slight fluctuation (~3.3%) occurred at the phase A voltage (RMS value) since the variational angle affects RMS calculation, illustrated in Fig. 3.12(b). Once $\Delta\theta$ and $\Delta\omega$ are compensated, there is no difference between $v_{f,lv}$ and v_g, illustrated in Fig. 3.12(a).

From $t=1.1s$, the CNOP is closed. As $v_{f,lv}$ and v_g has no difference, the active power output of the SST remains the same as the condition before the CNOP is open, illustrated in Fig. 3.12(e). Meanwhile, there is a slight fluctuation (<1%) of the reactive power output of the SST, illustrated in Fig. 3.12(f).

In Fig. 3.13, the performance of the SST during the synchronisation process is illustrated. During the compensation of the voltage amplitude, the resulted fluctuation of all the controllers, which get recovered in a very short time, is similar with that under other schemes, illustrated in Fig. 3.13(a)-(f). During the compensation of the $\Delta\theta$ and $\Delta\omega$, it leads to twice fluctuation of the q-axis voltage, thus the fluctuation of the q-axis current controller, illustrated in Fig. 3.13(b)(d), which is similar with the synchronisation of $\Delta\theta$ under other schemes.

The compensation of the voltage amplitude causes fluctuation of all the controllers in SST, and the fluctuation can be eliminated under regulation. The compensation of $\Delta\theta$ causes fluctuation of q-axis voltage and the corresponding q-axis current controllers. Scheme 3 and Scheme 4 show that the chronological order of $\Delta\theta$ and $\Delta\omega$ compensation has limited effect on the speed of synchronisation. It can be seen in Scheme 5 that the combination of the synchronisation of $\Delta\theta$ and $\Delta\omega$ can simplified the synchronisation procedure to speed up the synchronisation.

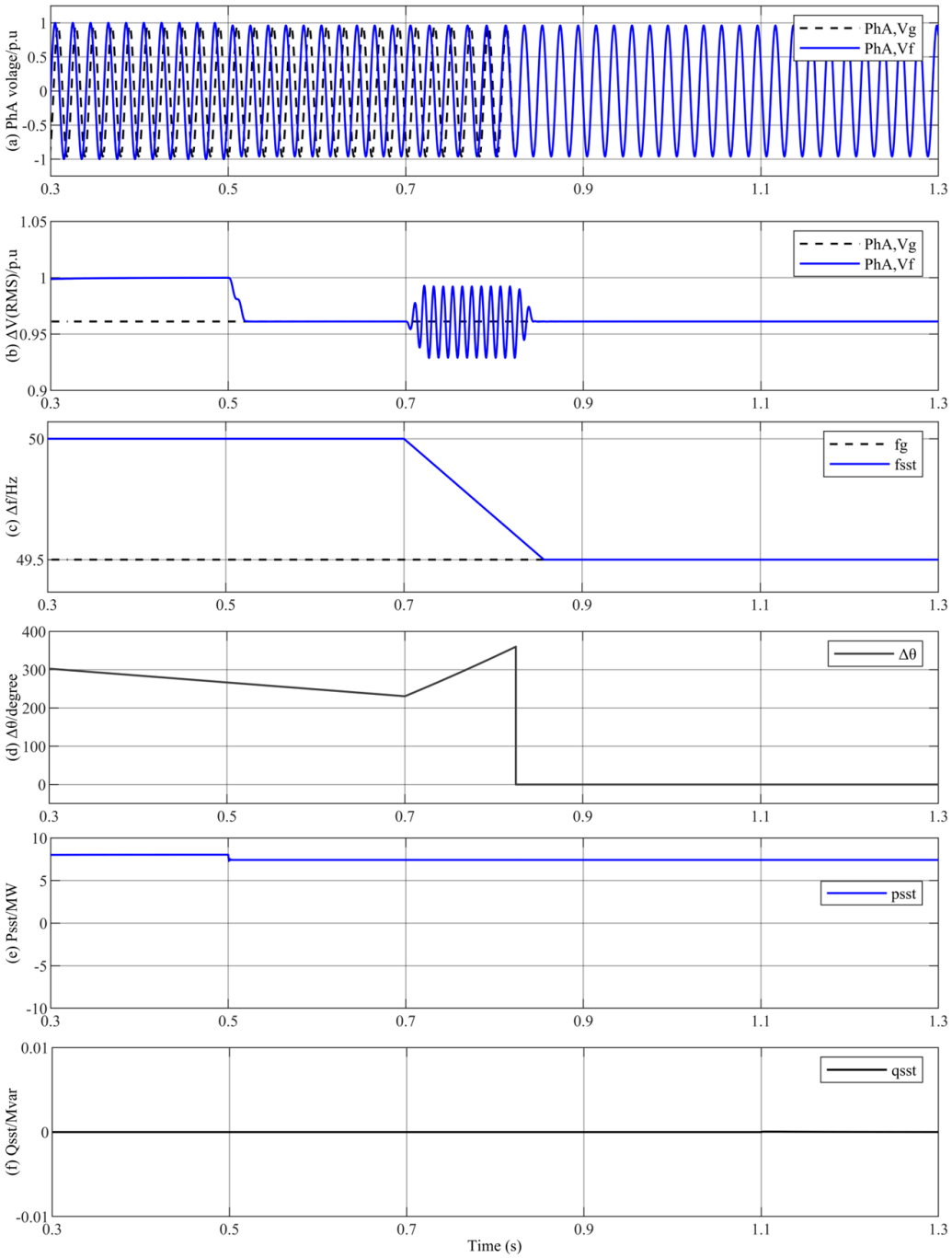


Fig. 3.12 Phase A voltage during synchronisation process under scheme 5: (a) SST output Phase A voltage v_f and 0.4 kV Bus 1 voltage v_g; (b) voltage difference (RMS) between v_f and v_g; (c) frequency difference between $v_{f,lv}$ and v_g; (d) angle difference between $v_{f,lv}$ and v_g; (e) SST output active power; (f) SST output reactive power.

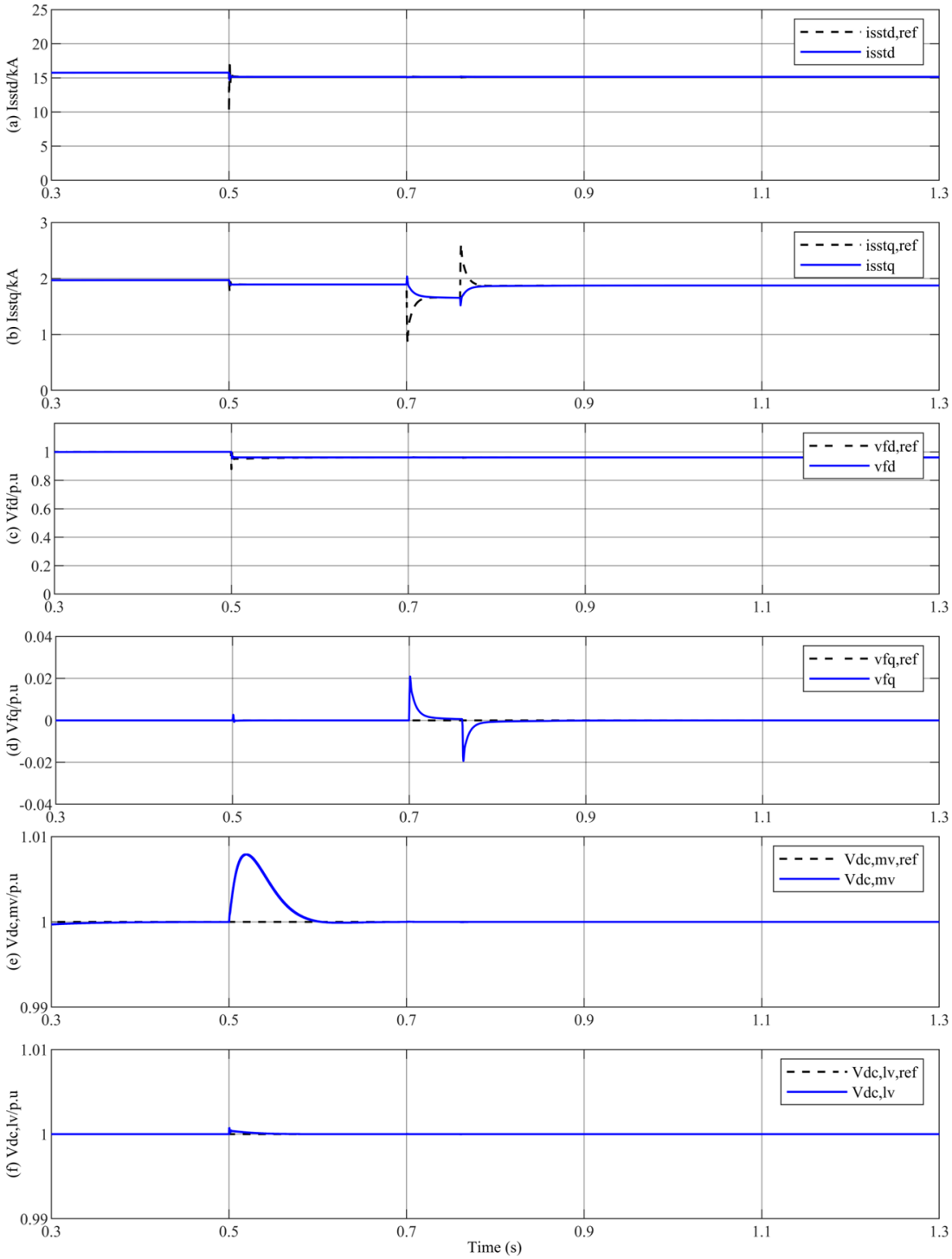


Fig. 3.13 Performance of the SST during synchronisation procedure under scheme 5: (a) DC/AC output d-axis current; (b) DC/AC output q-axis current; (c) DC/AC output d-axis voltage; (d) DC/AC output q-axis voltage; (e) medium voltage DC; (f) low voltage DC.

3.3.2 Simulation performance under grid-connected operation

The performance under grid-connected operation is assessed in this subsection. The tested network configuration is illustrated in Fig. 3.3. The parameters of the configuration are mostly the same as in Table 3.1 except the frequency of LVAC Network 1 is changed to 49.8 Hz. The SST power set points / references are varied, while different loads at LVAC Load 1 and 2 are switched in and out so the total active and reactive power P_1, Q_1 and P_2, Q_2 of LVAC Load 1 and 2 vary from time to time as scheduled in Table 3.3. It is noted that a current flowing from SST into an RL circuit produces a positive P and a positive Q, and the transmitted power from Bus 1 to Bus 2 is considered as positive. The active power and reactive power at SST output, LVAC Load 2, CNOP and 11 kV Bus 1 are illustrated in Fig. 3.14. The performance of the controllers in SST is illustrated in Fig. 3.15. The description and analysis of each event are shown below.

Table 3.3 Scheduled power references and load conditions under grid-connected operation.

Event	Time	Reference (P, Q) (MW, MVar)	Load Condition (P_1, Q_1, P_2, Q_2) (MW, MVar, MW, MVar)
Event 1	0-5 s	(10, 0)	(6, 0, 10, 0)
Event 2	5-10 s	(10, 0)	(6, 0, 4, 0)
Event 3	10-15 s	(10, 0)	(6, 0, 4, 1)
Event 4	15-20 s	(10, 0)	(6, 0, 4, -1)
Event 5	20-25 s	(5, 0)	(6, 0, 4, -1)
Event 6	25-30 s	(5, 2)	(6, 0, 4, -1)
Event 7	30-35 s	(5, 2)	(6, 2, 4, -1)

Event 1: From simulation starts to $t = 2.1s$, the inverter of SST operates under grid-forming operation and synchronisation procedure. the CNOP closed at $t = 1.1s$. During the time, the real power consumed at LVAC Load 2 is lower (0.87 MW, shown in Fig.

3.16(a).) than the rated value. As the power output of SST is determined by the load conditions under the grid forming operation, the difference between the rated voltage and the real value, illustrated in Fig. 3.16(c), results in the active power difference. At $t = 2.1s$, the $P_{sst} - v_{f,lv,q}$ and $Q_{sst} - v_{f,lv,d}$ droop controller are switched in DC/AC converter. The active and reactive power becomes controllable. The active power output starts to track the reference once the control in place. As a result, the active power difference between SST output and LVAC Load 2 flows to LVAC Load 1 via CNOP, illustrated in Fig. 3.14(e)-(h). In addition, a 0.55 MVar fluctuation occurs at reactive power output due to the coupling between the active and reactive power outputs of the SST, illustrated in Fig. 3.16(b). All the other controllers, including MVDC voltage, LVDC voltage DC/AC voltage and DC/AC current controllers are under normal operation, illustrated in Fig. 3.15.

Event 2: At $t = 5s$, a 6 MW load shedding is applied to LVAC Load 2 side while the power output references of the SST remain at 10 MW and 0 MVar. The active power and reactive power outputs of the SST see some disturbances when the load shedding occurs but quick track the references, as illustrated in Fig. 3.14(a) and (b). The 6 MW surplus power by the SST is transmitted through the CNOP to LVAC Load 1, illustrated in Fig. 3.14(e)(f). During Event 2, all the other controllers, including MVDC voltage, LVDC voltage DC/AC voltage and DC/AC current controllers are under normal operation, illustrated in Fig. 3.15.

Event 3: At $t = 10s$, a 1 MVar inductive load is added at LVAC Load 2 side while the power output references of the SST remain at 10 MW and 0 MVar. Similar with Event 2, the power outputs of the SST see some disturbances but quick track the references, as illustrated in Fig. 3.14(a) and (b). As the reactive power reference of SST output is zero, the inductive load is fed by MV Grid 1 through the CNOP. Again, the surplus 6 MW power is transmitted through the CNOP and consumed by LVAC Load 1, as illustrated in Fig. 3.14(e)(f). During Event 3, all the other controllers, including MVDC voltage, LVDC

voltage DC/AC voltage and DC/AC current controllers are under normal operation, illustrated in Fig. 3.15.

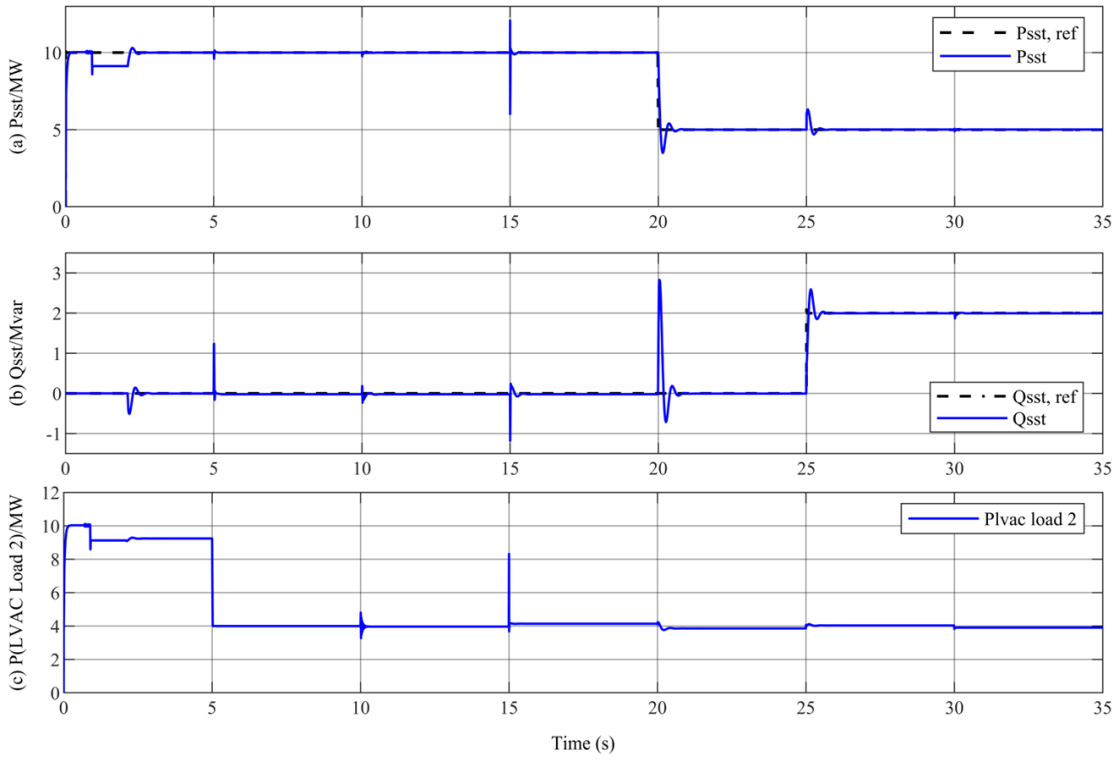
Event 4: At $t = 15s$, the 1 MVar inductive loadshedding is applied and a 1 MVar capacitive load is added at LVAC Load 2 side while the power output references of the SST remain at 10 MW and 0 MVar. The power outputs of the SST see disturbances with considerable overshoot but quick track the references, as illustrated in Fig. 3.14(a) and (b). Again, as the reactive power reference of SST output is zero, the capacitive load is fed by MV Grid 1 through the CNOP. The surplus 6 MW power is transmitted through the CNOP and consumed by LVAC Load 1, as illustrated in Fig. 3.14(e)(f). During Event 4, all the other controllers, including MVDC voltage, LVDC voltage DC/AC voltage and DC/AC current controllers are under normal operation, illustrated in Fig. 3.15.

Event 5: At $t = 20s$, the active power output reference of the SST is changed to 5 MW. The active power output of the SST quickly tracks the reference but with considerable overshoot, as shown in Fig. 3.14(a). In addition, a 2.8 MVar fluctuation occurs at reactive power output due to the coupling between the active and reactive power outputs of the SST, as illustrated in Fig. 3.14(b). This is obviously not desirable and further study to minimize the P and Q coupling will be provided in Section 4.4. The load conditions remain the same as that in Event 4. So the surplus 1 MW power at LVAC Load 2 is transmitted through the CNOP and consumed by LVAC Load 1, the 1 MVar capacitive load is fed by MV Grid 1 through the CNOP, as illustrated in Fig. 3.14(e)-(h). During Event 5, all the other controllers, including MVDC voltage, LVDC voltage DC/AC voltage and DC/AC current controllers are under normal operation, illustrated in Fig. 3.15.

Event 6: At $t = 25s$, the reactive power output reference of the SST is changed to 2 MVar. Similar to Event 5, the reactive power output of the SST quickly tracks the reference, though a 0.63 MW fluctuation occurred at active power output due to the coupling of the active and reactive power output of the SST, as illustrated in Fig. 3.14(a) and (b). The optimisation will also be provided in Section 4.4. The load conditions remain the same as that in Event 4. The surplus 3 MVar reactive power from LVAC Network 2 flows to MV

Grid 1, while the surplus 1 MW power flows to LVAC Load 1, as illustrated in Fig. 3.14(e)-(h). During Event 6, all the other controllers, including MVDC voltage, LVDC voltage DC/AC voltage and DC/AC current controllers are under normal operation, illustrated in Fig. 3.15

Event 7: At $t = 30s$, a 2 MVar inductive load is added at LVAC Load 1 side while the power output references of the SST remain at 5 MW and 2 MVar. The power outputs of the SST only experience small disturbance as illustrated in Fig. 3.14(a) and (b). The 1 MVar capacitive load is fed by MV Grid 1 through the CNOP while the 2 MVar inductive load is fed by SST through the CNOP. The surplus 1 MW active power from LVAC Network 2 is consumed by LVAC Load 1 and MV Grid 1 via the CNOP, as illustrated in Fig. 3.14 (e)-(h). During Event 7, all the other controllers, including MVDC voltage, LVDC voltage DC/AC voltage and DC/AC current controllers are under normal operation, illustrated in Fig. 3.15



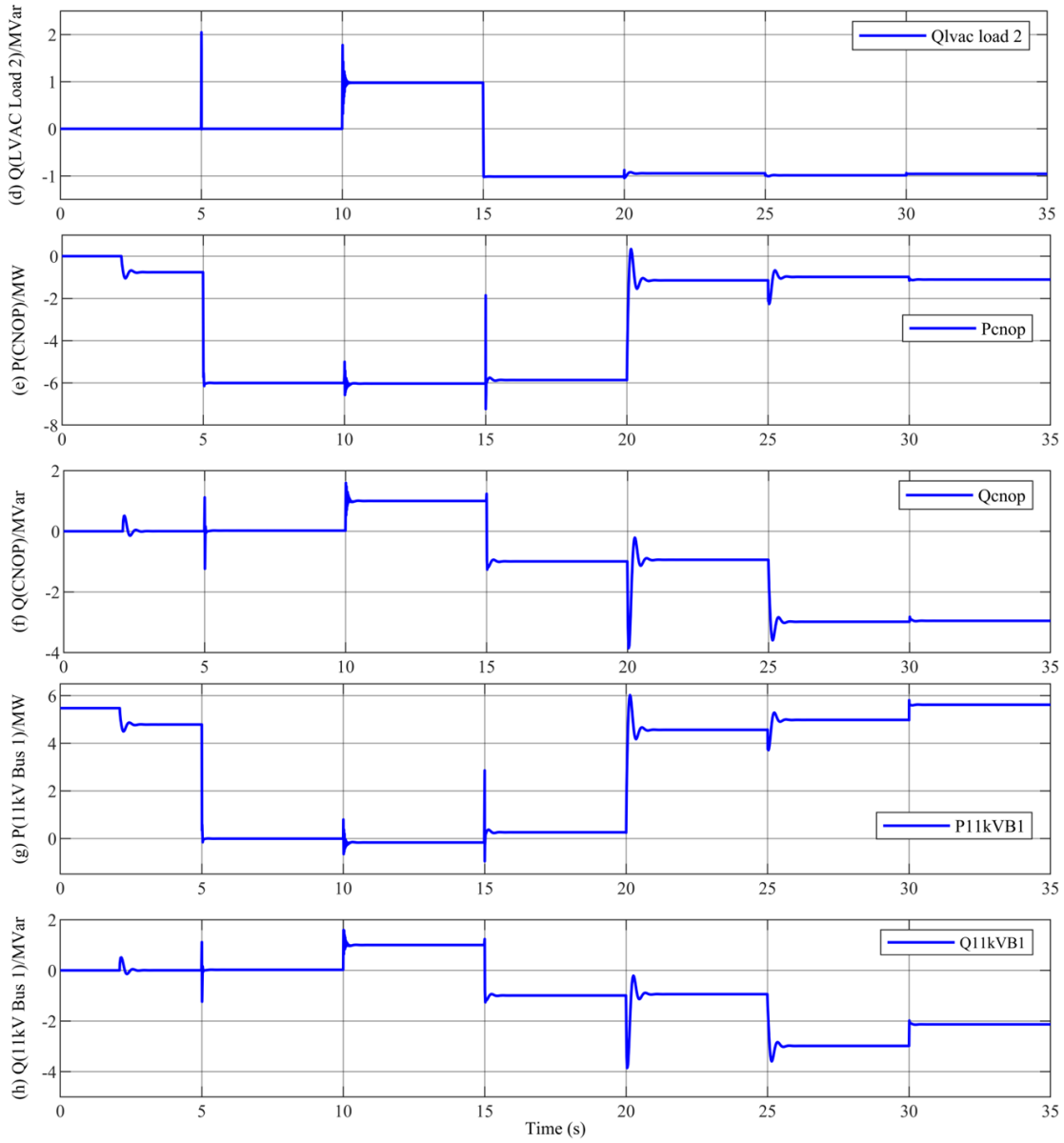


Fig. 3.14 Performance of the SST-based distribution system: (a) SST active power output;(b) SST reactive power output; (c) LVAC Load 2 active power; (d) LVAC Load 2 reactive power;(e) Transmitted active power via the CNOP; (f) Transmitted reactive power via the CNOP; (g) Transmitted active power via 11 kV Bus 1; (h) Transmitted reactive power via 11 kV Bus 1.

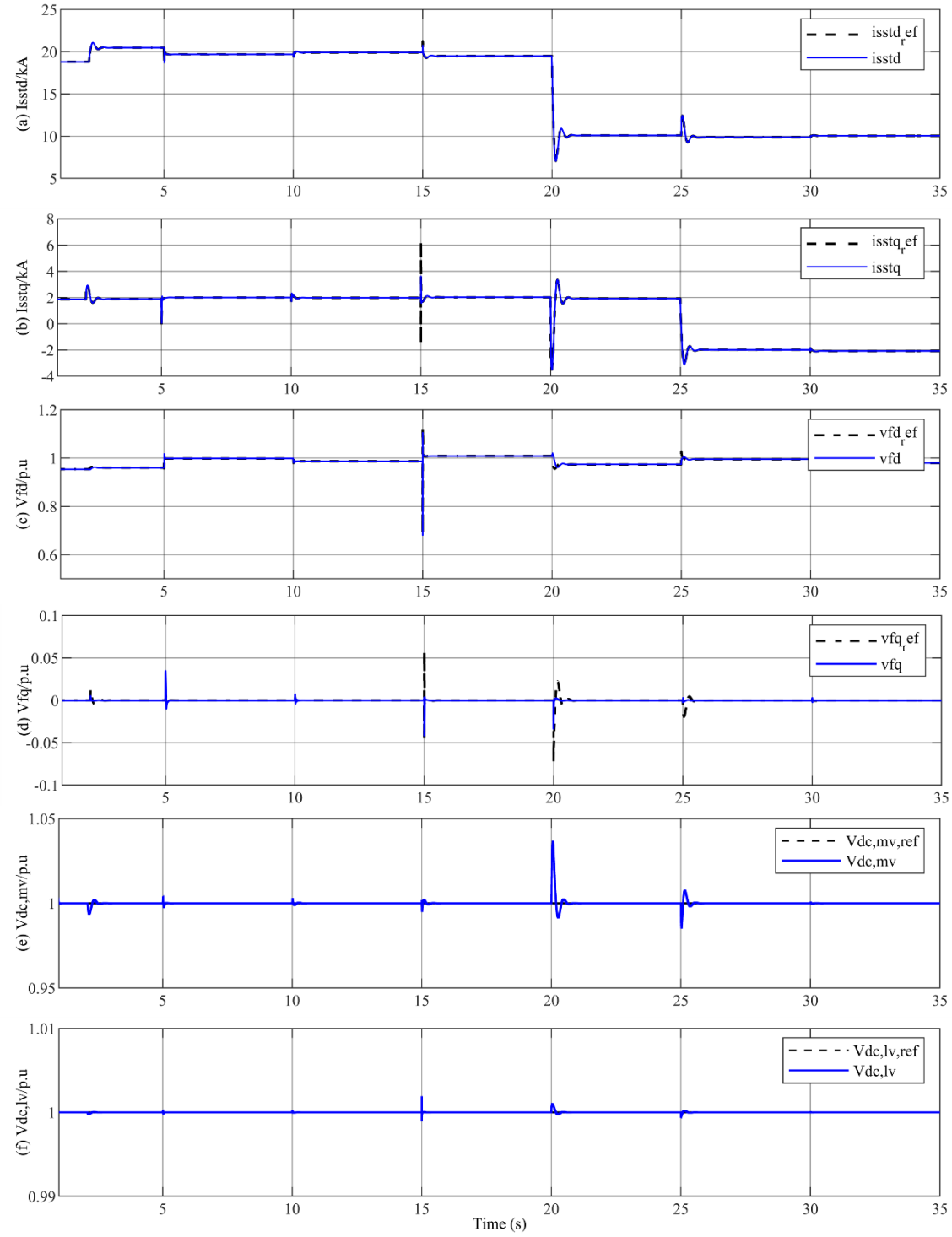


Fig. 3.15 Performance of the SST during grid-connected operation: (a) DC/AC output d-axis current; (b) DC/AC output q-axis current; (c) DC/AC output d-axis voltage; (d) DC/AC output q-axis voltage; (e) medium voltage DC; (f) low voltage DC.

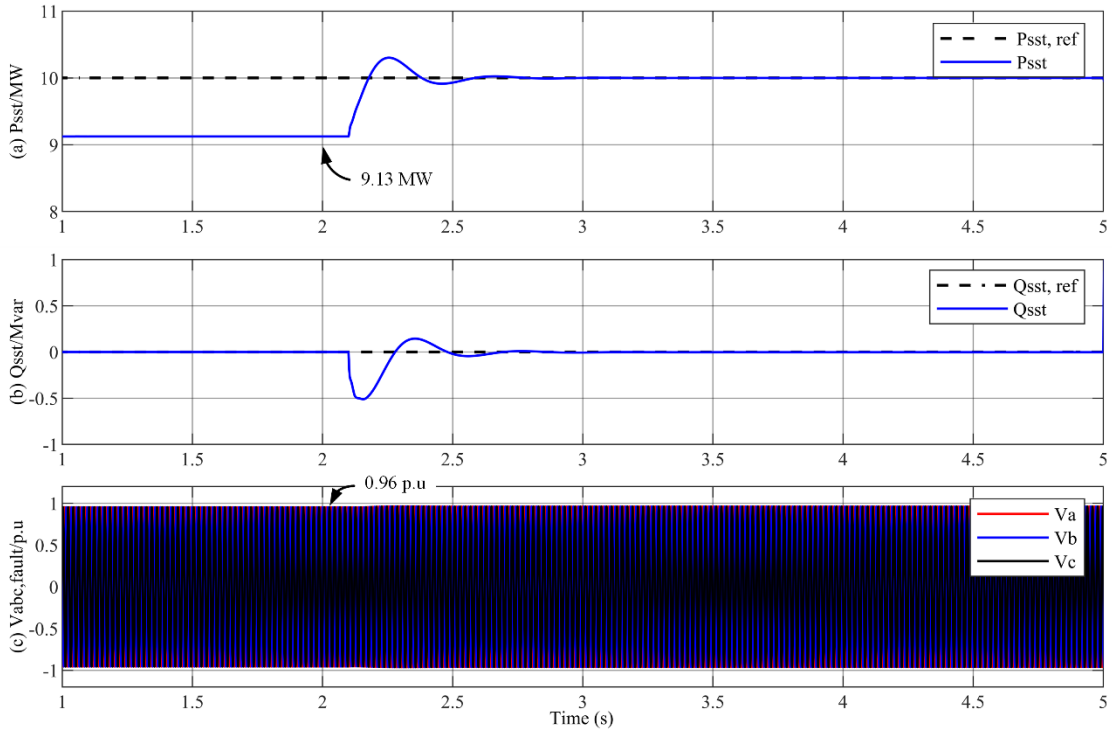


Fig. 3.16 Performance of SST during Event 1: (a) active power controller; (b) reactive power controller; (c) SST output voltage (3ph).

It can be seen that DC/AC converter under grid-connected operation can effectively follow the references under different load conditions. And it can follow the reference during the step load changes. Meanwhile, a large fluctuation at reactive power is observed when active power reference is changed, where active and reactive power loops of DC/AC converter are strongly coupled due to the operation of the $Q_{sst}-v_{f,lv,d}$ and $P_{sst}-v_{f,lv,q}$ droop. The detailed analysis and solution of the coupling issue will be assessed in Section 3.4.

3.3.3 Simulation performance under distributed generation integration

The performance under distributed generation integration is assessed in this subsection. The tested network configuration is illustrated in Fig. 3.3. Compared with the parameters

of the configuration in Table 3.1, the rated power of LVAC Load 2 is changed to 4 MW and the active power reference of SST is changed to 2MW. The DG operates under grid-connected operation at LVAC Bus 2 and its condition is listed in Table 3.4. It is noted that a current flowing from SST into an RL circuit produces a positive P and a positive Q, and the transmitted power from Bus 1 to Bus 2 is considered as positive. The transmitted power from DG to LVAC Bus 2 is considered as positive. The active power and reactive power at SST output, LVAC Load 2, CNOP and 11 kV Bus 1 are illustrated in Fig. 3.17. The performance of the controllers in SST is illustrated in Fig. 3.15. The description and analysis of each event are shown below.

Table 3.4 Scheduled power reference of DG under distributed generation integration.

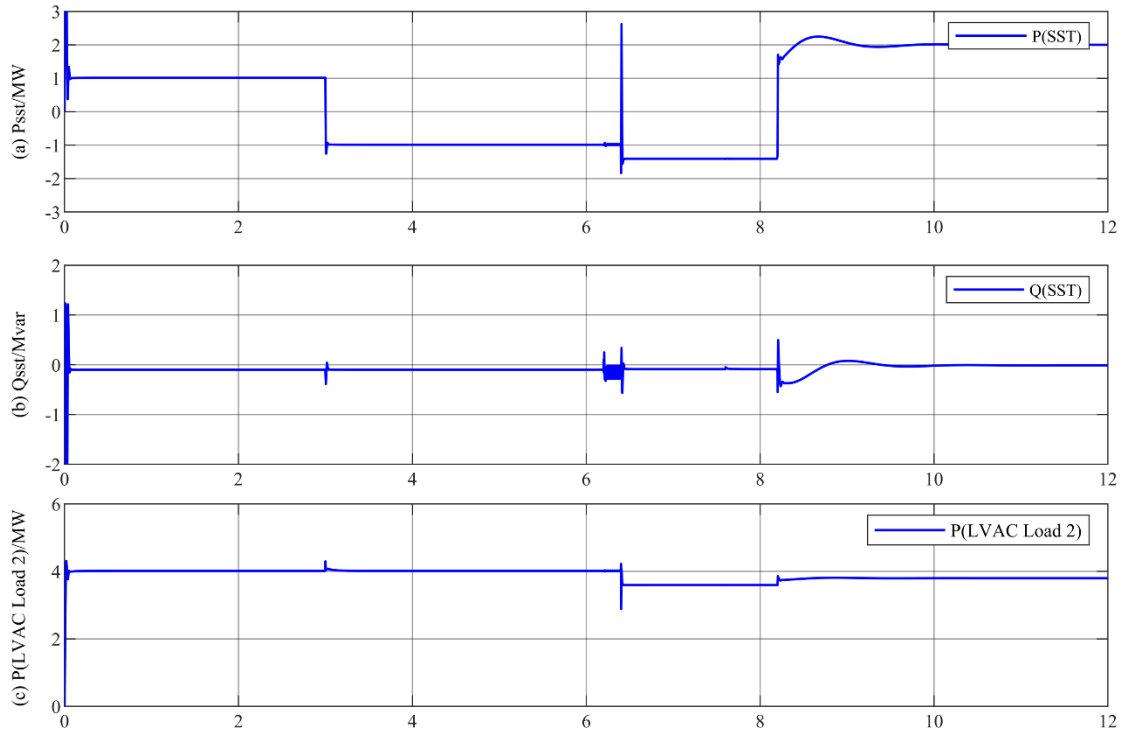
Event	Time	DG (MW, MVar)	SST operation
Event 1	0-3 s	(3, 0)	Grid forming
Event 2	3-6 s	(5, 0)	Grid forming
Event 3	6-12 s	(5, 0)	Syn and Grid-connected

Event 1: From simulation starts to $t = 3s$, the inverter of SST operates under grid-forming operation. As the power output of SST is determined by the load conditions under the grid forming operation, DG supplies 3 MW and SST supplies 1 MW respectively to the real power consumed at LVAC Load 2, illustrated in Fig. 3.17(c)(d). It can be seen that the active power generated by DG can be priorly consumed at LVAC Load 2. All the other controllers, including MVDC voltage, LVDC voltage DC/AC voltage and DC/AC current controllers are under normal operation, illustrated in Fig. 3.18.

Event 2: At $t = 3s$, the active power output of DG is changed to 5 MW. Part of the power output of DG is consumed by LVAC Load 2, illustrated in Fig. 3.17(c)(d). And the surplus 1 MW is transmitted to MVAC network via SST, illustrated in Fig. 3.17(e)(f). Combining with Event 1, it can be seen that the bidirectional power flow capability of SST helps DG consumed locally and transmitted to MVAC network. During the time, all the other

controllers, including MVDC voltage, LVDC voltage DC/AC voltage and DC/AC current controllers are under normal operation, illustrated in Fig. 3.18.

Event 3: At $t = 6s$, the inverter of SST starts synchronisation procedure. the CNOP closed at $t = 8s$. SST starts to operate under grid-connected operation with the active power reference 2 MW, illustrated in Fig. 3.17(a)(b). As the power output of DG is 5 MW, 2 MW of the DG output is consumed by LVAC Load 2 while the rest is consumed by LVAC Load 1 via the CNOP, illustrated in Fig. 3.17(c)-(f). During the time, all the other controllers, including MVDC voltage, LVDC voltage DC/AC voltage and DC/AC current controllers are under normal operation, illustrated in Fig. 3.18.



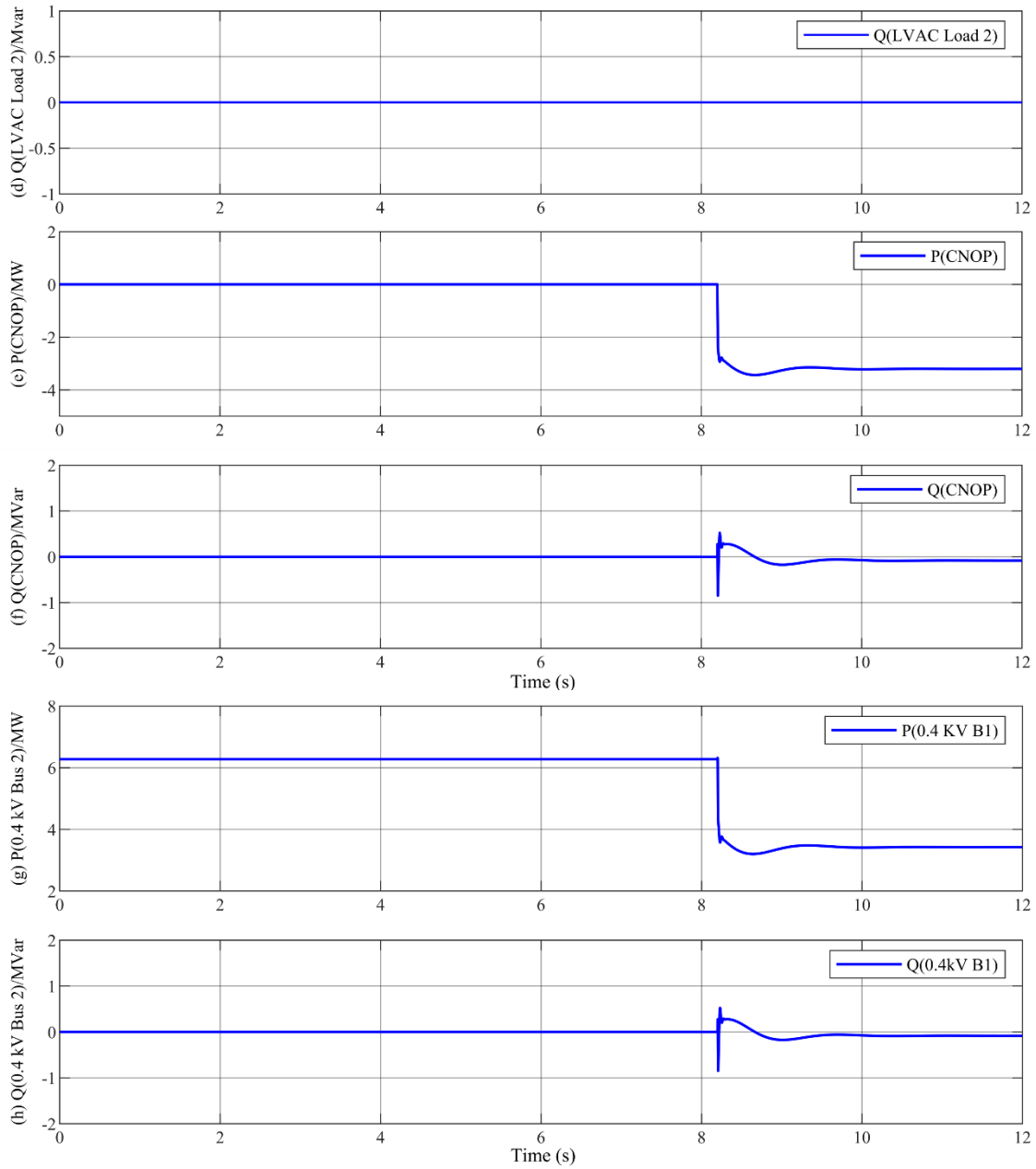


Fig. 3.17 Network performance with DG integration: (a) SST active power output;(b) SST reactive power output; (c) LVAC Load 2 active power; (d) LVAC Load 2 reactive power;(e) Transmitted active power via the CNOP; (f) Transmitted reactive power via the CNOP; (g) Transmitted active power via 0.4 kV Bus 1; (h) Transmitted reactive power via 0.4 kV Bus 1.

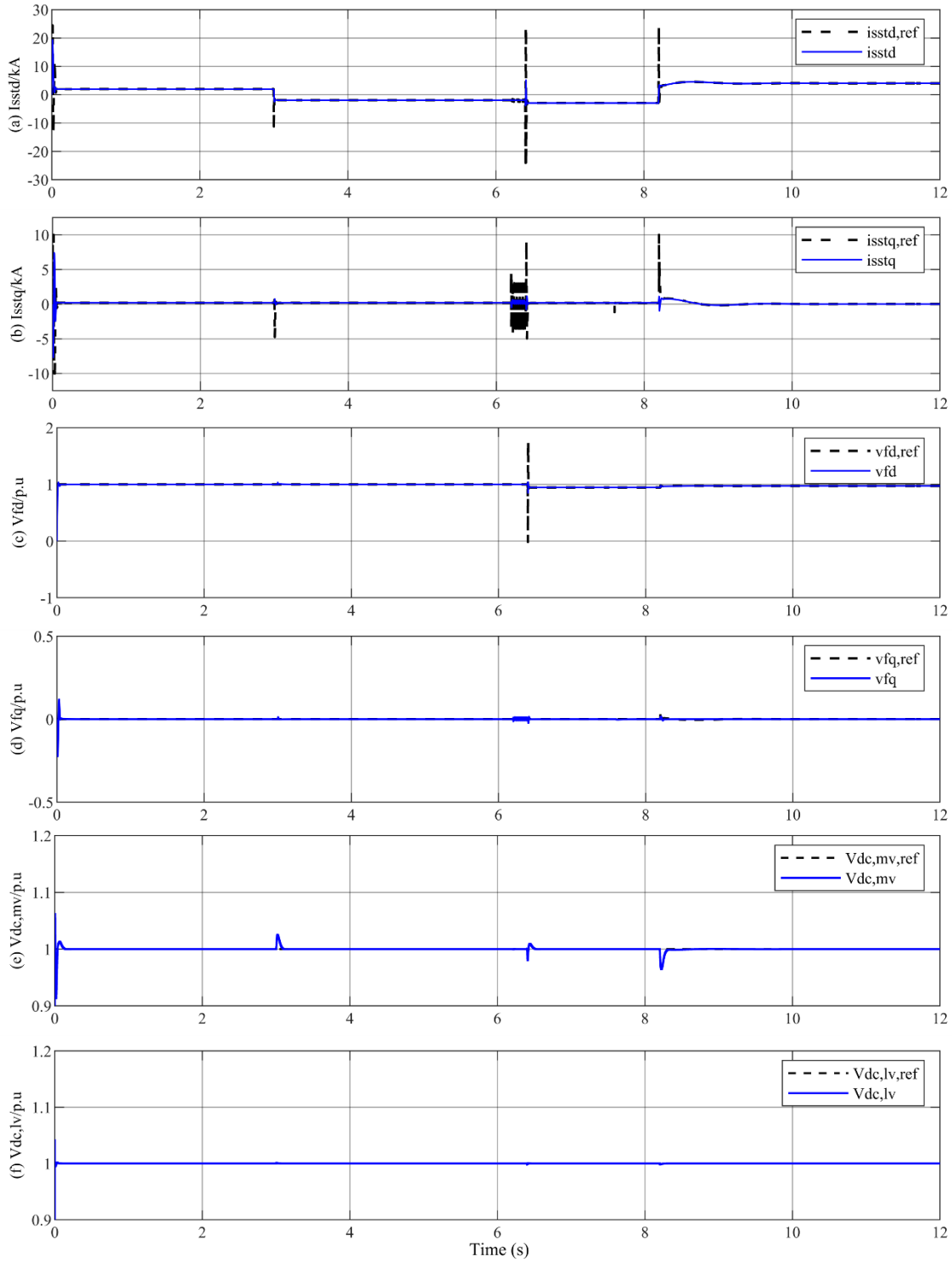


Fig. 3.18 Performance of the SST during DG integration operation: (a) DC/AC output d-axis current; (b) DC/AC output q-axis current; (c) DC/AC output d-axis voltage; (d) DC/AC output q-axis voltage; (e) medium voltage DC; (f) low voltage DC.

It can be seen that active power generated by DG can be priorly consumed near SST locally. The surplus power can either be consumed through the CNOP (Grid-connected operation) or flow to MV network (grid-forming operation). All the controllers in SST are under normal operation.

3.4 Additional compensation control

3.4.1 Additional compensation control principles

The operation of the $Q_{sst}-v_{f,lv,d}$ and $P_{sst}-v_{f,lv,q}$ droop control makes the active and reactive power of SST strongly coupled. This is because the change of reactive power will lead to the change of d-axis voltage and through the AC voltage control loop, d-axis current (active current) will change accordingly which also result in the change of active power. Similarly, the change of active power will eventually lead to the change of q-axis current (reactive current) through the q-axis AC voltage loop and thus affecting the reactive power.

As an example, selected waveforms during step changes of active and reactive power references are shown in Fig. 3.19 and Fig. 3.20, respectively. Considering the case when P_{sst}^{*} is reduced shown in Fig. 3.19, the active power error produces a negative $v_{f,lv,q}^{*}$ through the droop coefficient k_{pp} in the $P_{sst}-v_{f,lv,q}$ droop controller. The negative q-axis voltage reference $v_{f,lv,q}^{*}$ is fed to the q-axis voltage controller and results in a negative q-axis current reference $i_{sst,q}^{*}$ as seen in Fig. 3.19. Considering the high dynamics of the current controller compared to the voltage and power controllers, the q-axis current immediately tracks the reference, which results in the fluctuation of Q_{sst}.

Similarly, as shown in Fig. 3.20, when Q_{sst}^{*} is increased, the reactive power error produces a positive $v_{f,lv,d}^{*}$ which is fed to the d-axis voltage controller. A positive d-axis current reference $i_{sst,d}^{*}$ is produced and considering the high dynamics of the current controller, the d-axis current immediately tracks the reference before, which results in the fluctuation of P_{sst}.

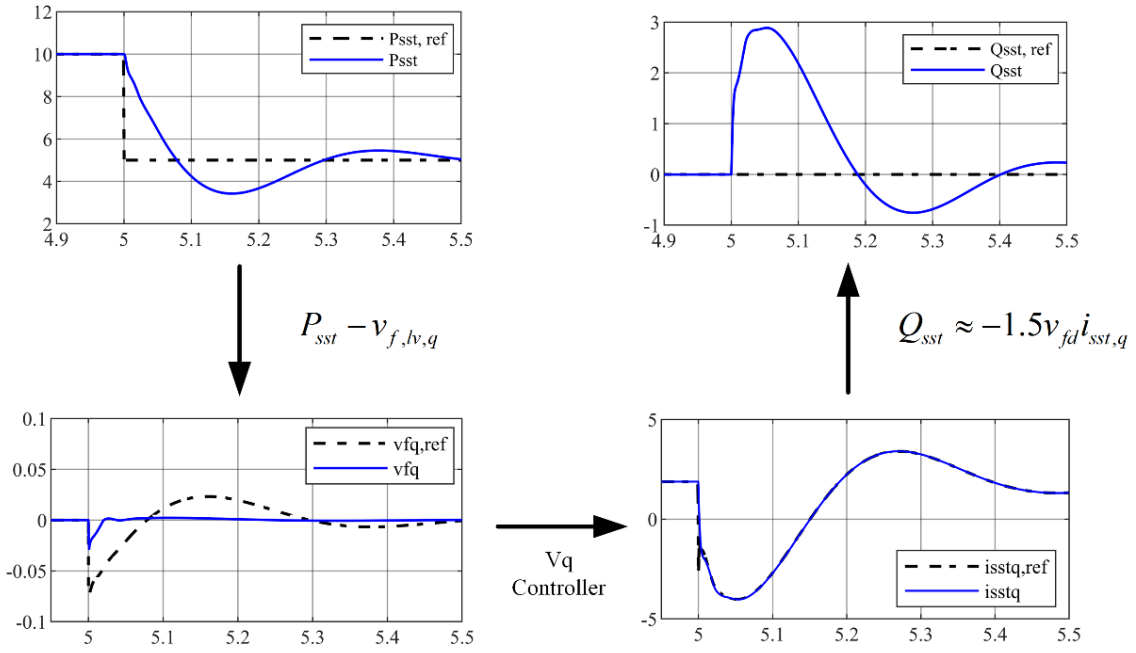


Fig. 3.19 SST active and reactive power coupling when P_{sst}^{*} is reduced.

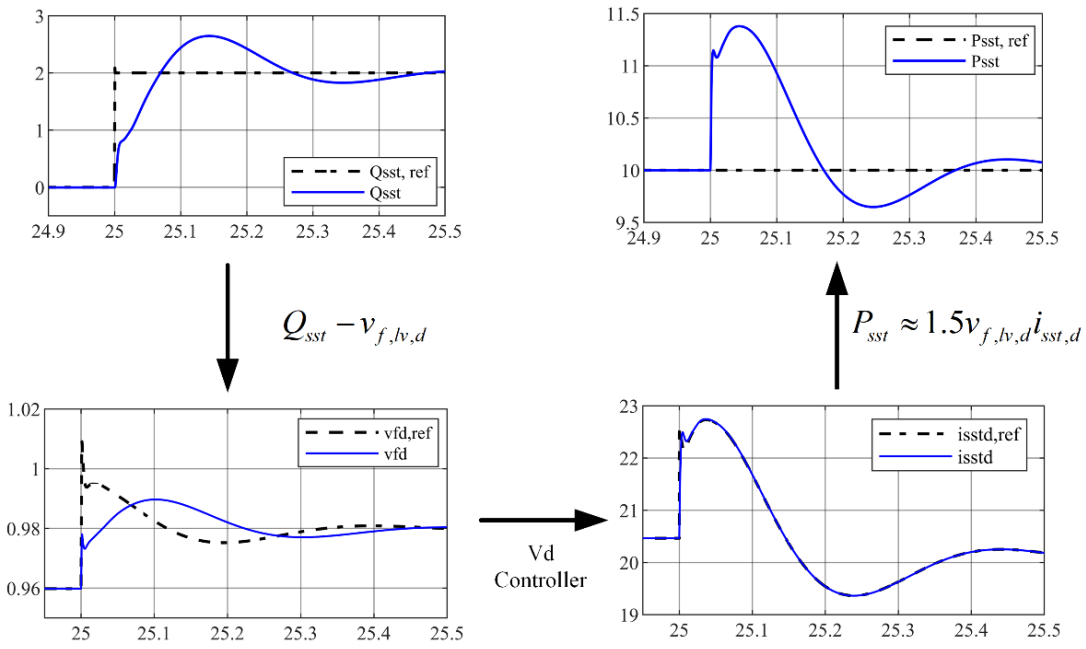


Fig. 3.20 SST active and reactive power coupling when Q_{sst}^{*} is increased.

From the above discussion, the coupling between P_{sst} and Q_{sst} is caused by the need to change q-axis current when P changes while the d-axis current has to be changed when Q changes. To reduce the coupling between P_{sst} and Q_{sst}, a compensation control is proposed, as shown in Fig. 3.21. In essence, active and reactive power feedforward terms are added directly to d- and q-axis current components, such that the coupling link between P and Q as shown in Fig. 3.19 and Fig. 3.20 is weakened. As shown, the active power compensation controller takes the active power error ΔP_{sst} as the input and generates an additional d-axis current reference $i_{sst,comd}$ by a gain k_{pid}, as,

$$i_{sst,comd} = k_{pid} \Delta P_{sst} \tag{3.6}$$

Similarly, the reactive power compensation controller takes the reactive power error ΔQ_{sst} as the input and generates the additional q-axis current reference $i_{sst,comq}$ by a gain k_{qiq}, as,

$$i_{sst,comq} = k_{qiq} \Delta Q_{sst} \tag{3.7}$$

Consequently, when the SST changes active power reference, the active current will be immediately changed in addition to the effect of the normal $P_{sst}-v_{f,lv,q}$ control loop which advances the phase of the converter output through the q-axis voltage. As a result, the reactive power fluctuation is greatly reduced due to the reduced q-axis current demand from the $P_{sst}-v_{f,lv,q}$ controller.

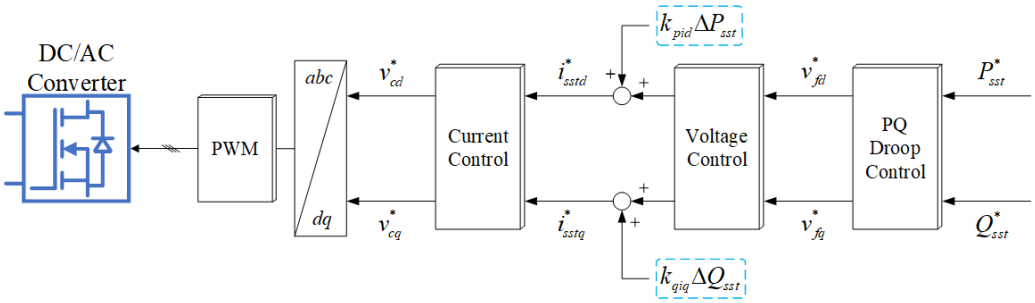


Fig. 3.21 Proposed compensation control scheme.

3.4.2 Simulation result

Fig. 3.22 illustrates the performance of the SST with the conventional control and proposed compensation control. In the study, $k_{pid}=0.008$, and $k_{qiq}=-0.0015$. When simulation starts, the CNOP opens and SST supplies 10 MW to AC Load 2. It then starts synchronisation procedure to prepare CNOP closing. The CNOP closes at $t=2.1s$ and immediately, the active and reactive power controller start to regulate the power output of SST to the active and reactive power references of 10 MW and 0 MVar. When the active power reference of the SST reduces from 10 MW to 5MW at $t=5s$, the active power quickly follows the order but significant reactive power variation is also induced as can be seen in Fig. 3.22. However, with the proposed compensation control, the maximum reactive power variation is reduced from 2.88 MVar (with conventional control) to 0.51 MVar, as illustrated in Fig. 3.22(b). Similar, when the reactive power reference of the SST increases from 0 MVar to 2 MVar at $t=25s$, the maximum active power variation is

reduced from 1.72 MW (with conventional control) to 0.35 MW (with proposed compensation control), as illustrated in Fig. 3.22(a). Similar performance can also be observed at $t = 20\,s$ and 30 s during active and reactive power reference changes. In addition, a 2 MW load shedding is applied to AC Load 2 at $t = 15\,s$ and the 2 MW load is added back to AC Load 2 at $t = 20\,s$. The power outputs of the SST only see some small disturbances but quick track the references, as illustrated in Fig. 3.22(a)(b).

Fig. 3.23 and Fig. 3.24 illustrate the effect of different k_{pid} and k_{qiq} on the compensation control performance. In Fig. 3.23, the reactive power fluctuation at $t = 5\,s$ is illustrated when $P^{*}_{sst,ref}$ decreases from 10 to 5 MW. As can be seen in Fig. 3.23, the reactive power peak value reaches the minimum when k_{qiq} is selected as -0.015, though lower k_{qiq} (more negative) results in slower active power response. Similarly, as seen from Fig. 3.24, $Q^{*}_{sst,ref}$ increases from 0 to 2 MVar at $t = 5\,s$, the active power fluctuation can be reduced by increasing k_{pid}. However, higher k_{pid} leads to slower reactive power response. Thus, $k_{qiq} = -0.0015$ and $k_{pid} = 0.008$ were selected as they provided balanced response for both active and reactive power.

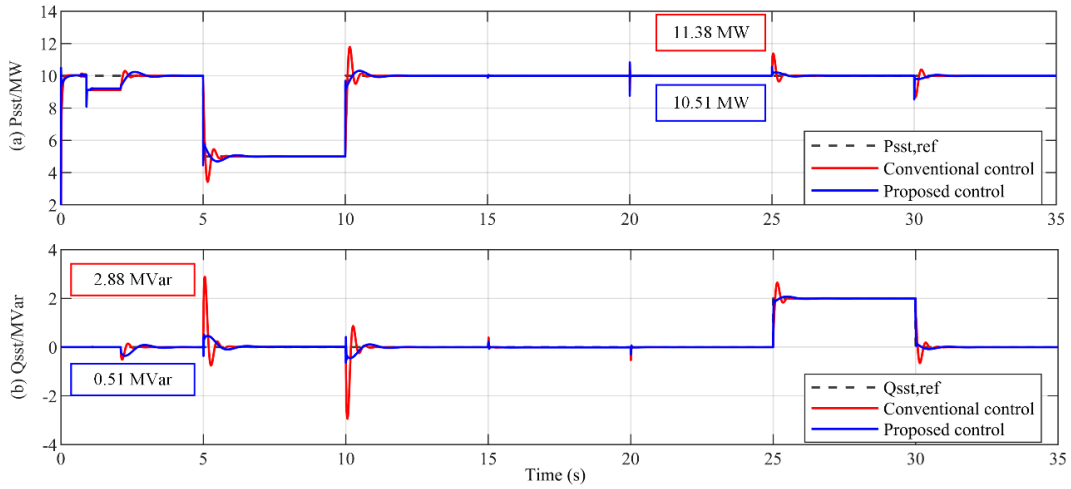


Fig. 3.22 Performance of system with conventional control and proposed compensation control: (a) active power output of the SST; (b) reactive power output of the SST

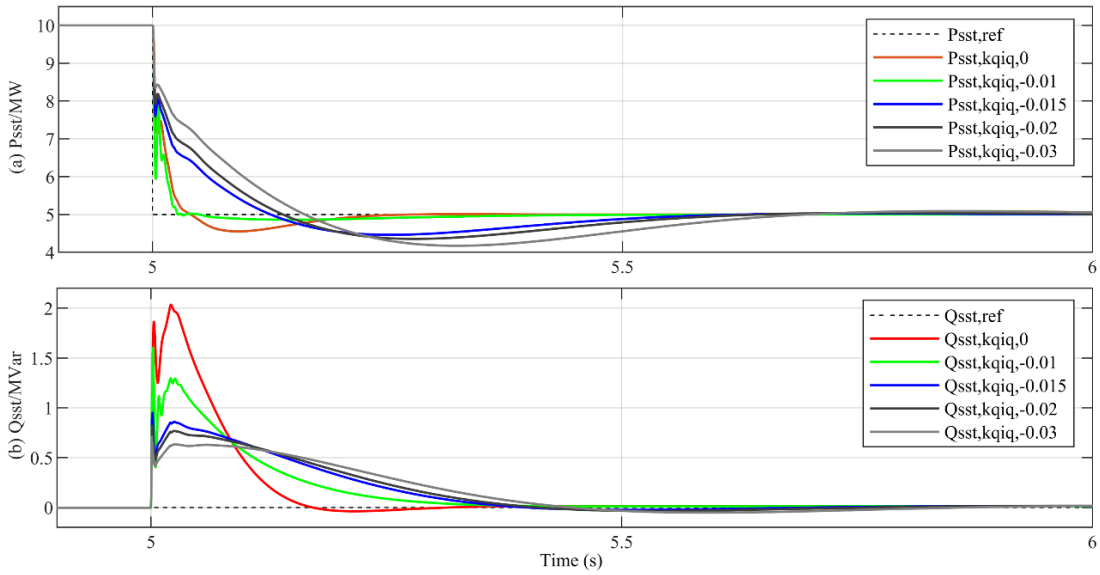


Fig. 3.23 Performance with different compensation control coefficients when active power reference changes: (a) SST output active power; (b) SST output reactive power.

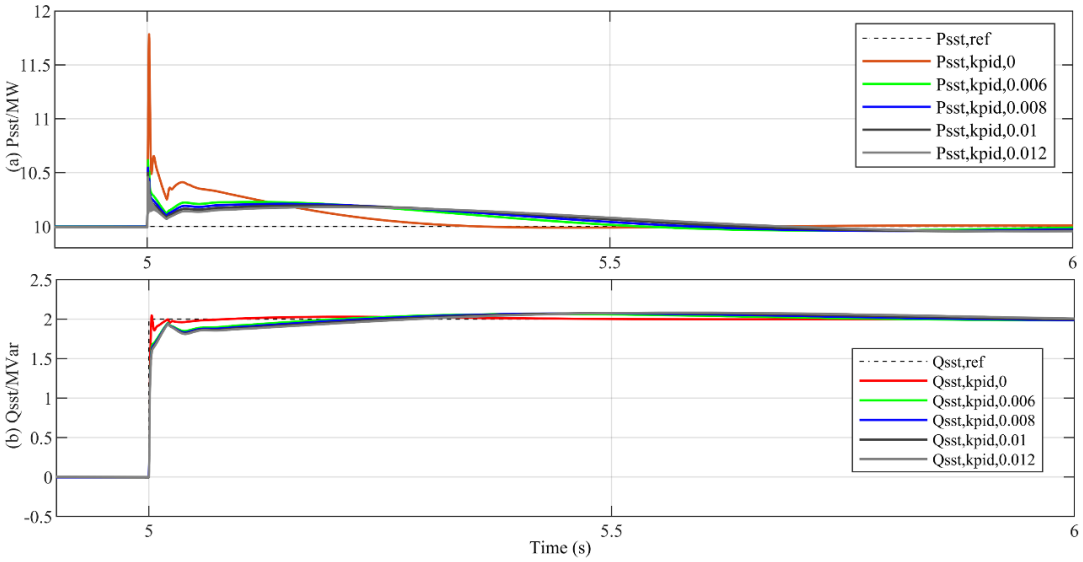


Fig. 3.24 Performance with different compensation control coefficients when reactive power reference changes: (a) SST output active power; (b) SST output reactive power.

3.5 Summary

The control scheme of the DC/AC converter in SST under grid-connected operation has been proposed in this chapter, only the control scheme of the DC/AC converter. By cooperated with the CNOP, the grid-forming SST can be connected with another LVAC network. The proposed control scheme consists of current control, voltage control, synchronisation procedure, active and reactive power control and additional compensation control. In order to eliminate large transient brought by control mode switch, the current and voltage control remain the same as the that under grid-forming operation. The synchronisation procedure is proposed specially for the control mode switch from grid forming operation to grid-connected operation. Wherein, the angular frequency, angle and voltage amplitude are considered as the three impact factors during the synchronisation procedure, and their effect on the controllers in SST and synchronisation speed are under investigation. The controllers in SST remain the normal operation during the synchronisation of angular frequency. The q-axis voltage controller and the corresponding q-axis current controller in DC/AC converter occurs small disturbance during the

synchronisation of angle. The synchronisation of voltage amplitude causes small disturbances in all the controllers in SST. All the disturbances can track back to the references in a very short time. Meanwhile, the synchronisation of angular frequency and angle can proceed at the same time to speed up the procedure. The proposed $P_{sst}-v_{f,lv,q}$ and $Q_{sst}-v_{f,lv,d}$ droop control enable the SST to control its power output to the local load and the connected LVAC network. The proposed additional compensation control weakens the coupling between active power and reactive power output of the SST without affecting the overall system response to reduce the power variation when power output reference is changed. Based on the control scheme, the SST-based network can benefit distributed generation consumed locally and transmit the surplus power from LVAC to MVAC network. Simulation results in MATLAB/Simulink during synchronisation procedure and grid-connected operation verify the voltage and power controllability of the SST with proposed control scheme.

Chapter 4 Control and Performance of SST during Network Faults

The control and performance of SST during network faults is investigated in this chapter. The constraints due to the limited over-current and over-voltage capability of semiconductor devices require specific control and protection measures for SST during network faults, while the potential benefits of SST to the distribution network in terms of fault performance need further study. To address these issues, a series of case studies are considered to investigate fault performance of SST under grid-forming and grid-connected operation in different network configurations. The fault current limiting capability of SST reduces the fault current contribution from SST, while it also provides isolation between the faulty side and healthy side. In order to prevent SST from unnecessary blocking during large MVDC voltage fluctuation due to MV AC faults, which can lead to active power unbalance between MV and LV sides of the SST, an active SST power limiting control is proposed where the MVDC voltage variation directly sets the d-axis voltage (during grid-forming operation) or the active power output reference during (grid-connected operation) of the LV side converter. Various case studies are carried out in MATLAB/Simulink to validate the effectiveness of the proposed control and operation during different fault locations and SST operation modes.

4.1 Considered cases for evaluating SST under network faults

In order to evaluate the performance of SST during and after network faults, a simplified distribution network with different fault locations is developed, illustrated in Fig. 4.1. In the model shown in Fig. 4.1(a), the network is supplied by MV Network. A LFT is used to supply LVAC Load 1, while different configurations using either LFT2 or SST for supplying LVAC Load 2 are considered and the performances are compared. At LVAC Bus 2, a distributed generation (DG) is connected to examine the fault performance of SST under bidirectional power flow. In the model shown in Fig. 4.1(b), the network is

supplied by MV Network 1 and MV Network 2 separately (e.g., from different part of the transmission network), where the CNOP is closed. In order to examine the performance of SST under network faults, four fault locations are selected in the developed network. And five cases studies are developed according to different operation mode of SST along with the state of the CNOP, as:

- Case 1: fault at LVAC Load 1 (F1) with the CNOP open
- Case 2: fault at LVAC Load 2 (F2) with the CNOP open
- Case 3: fault at LVAC Load 1 (F1) with the CNOP closed
- Case 4: fault at MVAC Network (F3) with the CNOP open
- Case 5: fault at MVAC Network 2 (F4) with the CNOP closed

As the thesis concentrates on the operation of SST and improve SST reliability in the network, only the critical fault which could result in outage of SST will be considered. For the asymmetrical fault, the DC/DC converter in the middle can isolate the 2^{nd} ripple DC voltage brought by asymmetrical fault to the healthy part. For the first three case studies, symmetrical three-phase to ground faults are applied at different locations along with different state of the CNOP. The performance during and after fault clearance of the SST and LFT2 are examined and compared in terms of fault current level, voltage level and affected area by the faults.

Both Case 4 and 5 consider symmetrical three-phase to ground faults at the MV grid side. While Case 4 examines the performance of SST under grid-forming operation, Case 5 considers SST under grid-connected operation. The simulation results are shown in Section 4.3.

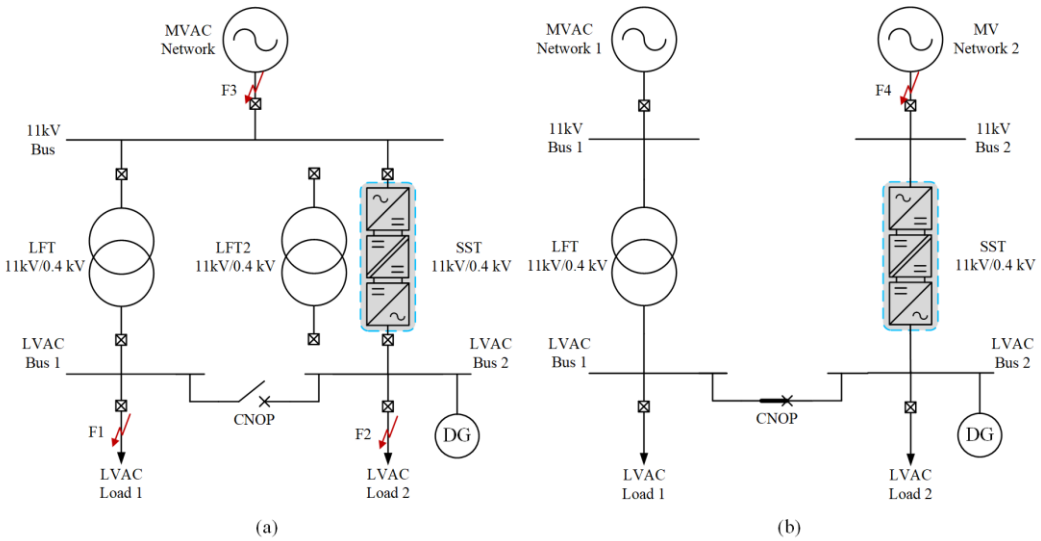


Fig. 4.1 Potential fault locations in the distribution network: (a) fault locations for the Case 1-4; (b) fault locations for the case 5.

4.2 Control requirement of SST during network faults

4.2.1 Fault current limiting of SST

For SST, in order to prevent the SST current from exceeding the maximum value while provide sufficient fault current for fault detection, the maximum and minimum value of the d-axis and q-axis current in the LV DC/AC converter can be set accordingly as

$$\begin{cases} i_{sst,qref,\max} = k_m I_{rated} \\ i_{sst,qref,\min} = -k_m I_{rated} \end{cases} \tag{4.1}$$

$$\begin{cases} i_{sst,dref,\max} = \sqrt{\left(k_m I_{qrated}\right)^2 - \left(I_{sst,qref}\right)^2} \\ i_{sst,dref,\min} = -\sqrt{\left(k_m I_{qrated}\right)^2 - \left(I_{sst,qref}\right)^2} \end{cases} \tag{4.2}$$

where I_{rated} is DC/AC converter's rated current. k_m is the overload coefficient of the DC/AC converter, which is set as 1.2 pu in this chapter. The setting in AC/DC converter is the same as that in DC/AC converter.

4.2.2 Active power limiting of SST during MV grid side AC fault

An active power limiting control is proposed for SST to enhance the fault ride through capability and post-fault recovery in this subsection.

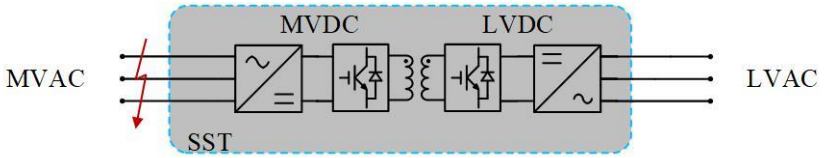


Fig. 4.2 SST under MVAC network fault.

As shown in Fig. 4.2. When an AC fault occurs at MV grid side, the MV side AC voltage drops and thus the power transmission capability of SST between the MVDC and MVAC sides is significantly reduced. If SST continues to try to transmit the assigned power from MV to LV network, power unbalance at the SST converters will occur, which can result in MVDC voltage under- or over-voltage (over -voltage can occur if the LV side converter exports active power to the MV network through the SST). The under-voltage of MVDC voltage will lead to restart of the whole SST converter, while the over-voltage of MVDC voltage will potentially lead to convert blocking. If these situations can be avoided, the system can quickly recover to normal operation to support the load side after MV side fault clearance.

For the considered SST topology, The LV side DC/AC converter regulates AC voltage and current under grid-forming operation as well as the active and reactive power output under grid-connected operation in the SST as discussed in Chapter 3. If the SST detects the abnormal (i.e., rapid decrease/increase) of the MVDC voltage at the initial stage of MV grid side fault, it can reduce AC voltage (grid-forming operation) or the active power output (under grid-connected operation) rapidly, to quickly rebalance the active power of the SST, and consequently, the MVDC voltage can be maintained closely at its nominal value. Therefore, it is necessary to establish a relation between MVDC voltage variation and AC voltage (under grid-forming operation) or active power (under grid-connected

operation) of the SST at the LV side DC/AC converter. Based on the deduction above, an active power limiting control is proposed, shown in Fig. 4.3.

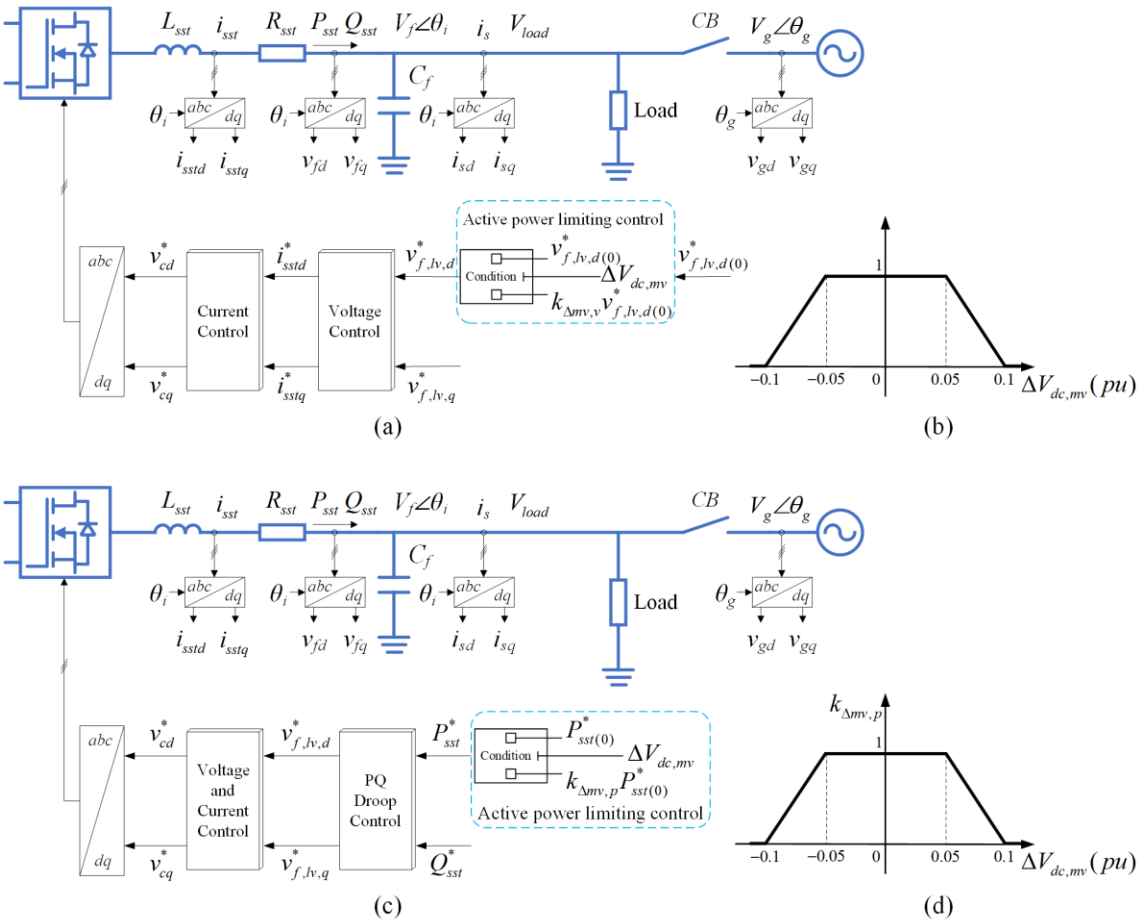


Fig. 4.3 Active power limiting control of SST: (a) control diagram under grid-forming operation; (b) droop parameter curve under grid-forming operation; (c) control diagram under grid-connected operation; (d) droop parameter curve under grid-connected operation.

Under grid-forming operation, as illustrated in Fig. 4.3(a), a droop controller is used to link the variation of MVDC and the d-axis voltage reference at DC/AC converter $v^*_{f,lv,d}$ via the droop parameter $k_{\Delta mv,v}$, given as:

$$
\begin{aligned}
& v_{f,lv,d}^{*} = k_{\Delta mv,v} \cdot v_{f,lv,d(0)}^{*} \\
& k_{\Delta mv,v} = \begin{cases} 1 & \left|\Delta V_{dc,mv}\right| \le 0.05 \\ 1 - k\left(\left|\Delta V_{dc,mv}\right| - 0.05\right) & \left|\Delta V_{dc,mv}\right| > 0.05 \end{cases} \\
& 0 \le k_{\Delta mv,v} \le 1
\end{aligned} \tag{4.3}
$$

where $v_{f,lv,d(0)}^{*}$ $v_{f,lv,d}^{*}$ are the original and actual d-axis voltage orders of the LV DC/AC converter, respectively. $\Delta V_{dc,mv}$ is the normalised per unit value of MVDC voltage error, and *k* is the droop constant. As MVDC variation is expected to control within ±10%. *k* is set to ± 20 in the illustration in Fig. 5.3(b).

During normal operation, $\left|\Delta V_{dc,mv}\right|$ is less than the pre-set threshold of 0.05 pu, which means MVDC voltage variation is less than 5%. Thus, $k_{\Delta mv,p} = 1$ and $v_{f,lv,d}^{*}$ remains to its assigned value of $v_{f,lv,d(0)}^{*}$. When there is a fault at the MV grid side, the unbalance active power will lead to MVDC voltage variation. Once $\left|\Delta V_{dc,mv}\right|$ exceeds the threshold of 0.05 pu, MVDC voltage variation is over 5%. $v_{f,lv,d}^{*}$ will be modified according to the reduced *k* value, as shown Fig. 4.3(b), and thus the active power can be re-balanced. When MVDC voltage variation is over 10%, $k_{\Delta mv,p} = 0$, and $v_{f,lv,d}^{*}$ will reduce to zero accordingly. SST power output will reduce to zero. Consequently, the MVDC voltage is maintained to the corresponding level according to the droop characteristic. Once the fault is cleared, the MVDC will be controlled by the AC/DC converter at the MV side to its reference, and consequently, $v_{f,lv,d}^{*}$ goes back to its normal value of $v_{f,lv,d(0)}^{*}$.

Under grid connected operation, as illustrated in Fig. 4.3(c), a droop controller is used to link the variation of MVDC and the active power reference at DC/AC converter P_{sst}^{*} via the droop parameter $k_{\Delta mv,p}$, given as:

$$
\begin{aligned}
&P_{sst}^{*} = k_{\Delta mv,p} \cdot P_{sst(0)}^{*} \\
&k_{\Delta mv,p} = \begin{cases} 1 & \left|\Delta V_{dc,mv}\right| \le 0.05 \\ 1 - k\left(\left|\Delta V_{dc,mv}\right| - 0.05\right) & \left|\Delta V_{dc,mv}\right| > 0.05 \end{cases} \\
&0 \le k_{\Delta mv,p} \le 1
\end{aligned} \tag{4.4}
$$

where $P_{sst(0)}^{*}$ P_{sst}^{*} are the original and actual active power orders of the LV DC/AC converter, respectively. $\Delta V_{dc,mv}$ is the normalised per unit value of MVDC voltage error, and *k* is the droop constant, which is set to 20 in the illustration in (4.4).

During normal operation, $\left|\Delta V_{dc,mv}\right|$ is less than the pre-set threshold of 0.05 pu, as the MVDC voltage follows the reference as assigned, and thus $k_{\Delta mv,p} = 1$ and P_{sst}^{*} remains to its assigned value of $P_{sst(0)}^{*}$. When there is a fault at the MV grid side, the unbalance active power will lead to MVDC voltage variation. Once $\left|\Delta V_{dc,mv}\right|$ exceeds the threshold of 0.05 pu, P_{sst}^{*} will be modified according to the reduced *k* value, as shown Fig. 4.3(d). Consequently, active power can be re-balanced and the MVDC voltage is maintained to the corresponding level according to the droop characteristic. Once the fault is cleared, the MVDC will be controlled by the AC/DC converter at the MV side to its reference, and consequently, P_{sst}^{*} goes back to its normal value of $P_{sst(0)}^{*}$.

Detailed case studies to investigate the performance of SST under fault conditions will be assessed in Section 4.3.

4.3 Simulation results

The radial distribution network for test Case 1-4 with SST integration is illustrated in Fig. 4.1(a). The LV load sides (F1 and F2) are the two fault locations assessed in the following studies.

In the model shown in Fig. 4.1(a), a LFT is used to supply LVAC Load 1, while different configurations using either LFT2 or SST for supplying LVAC Load 2 are considered and compared. AC Load 1 and AC Load 2 are both 4 MW. The main parameters of the test network are shown in Table 4.1 and the detailed parameters of SST can be found in Chapter 4. Initially, three solid symmetrical three-phase to ground faults are considered:

Table 4.1 Main parameters of the tested network

Parameter	Value
Rated power of LFT	10 MVA
Rated power of SST	10 MVA
Transformer ratio of LFT, LFT2 and SST	11/0.4 kV
Rated power of LFT1	10 MVA
MVAC Network fault level	150 MVA
LVAC Load 1	(4 MW, 0 MVar)
LVAC Load 2	(4 MW, 0 MVar)
Base Power	10 MVA

4.3.1 Case 1: Performance under F1

In Case 1, the comparison of the fault performance between LFT and SST are assessed. Wherein, the CNOP is open, and LFT2 and SST are tested in the network respectively. The network equivalent circuit under F1 is shown in Fig. 4.4. X_{LFT}, X_{LFT2}, X_{mv} and X_{SST} are the equivalent reactance of LFT, LFT2, MV network and SST. The simulation results are shown in Fig. 4.5, where the waveforms in the left column refer to LFT2 and those in the right column refer to SST. The description and analysis of the case study are provided in the followings.

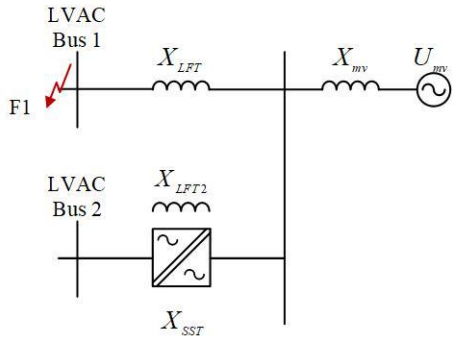
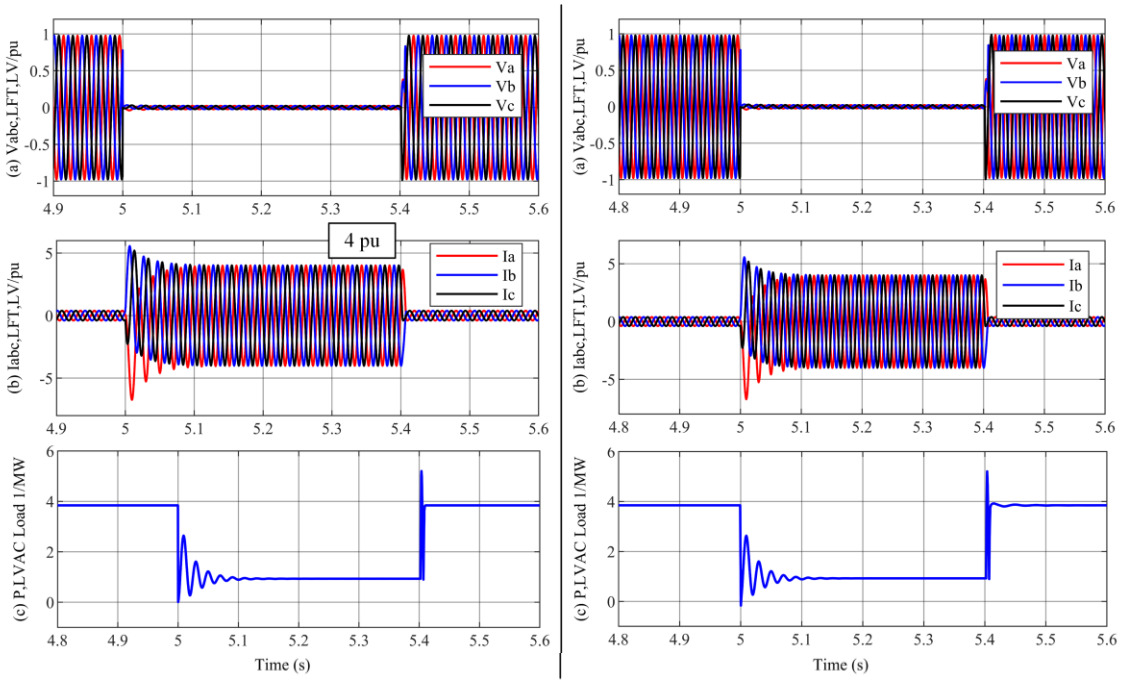


Fig. 4.4 System equivalent circuit under Fault 1.

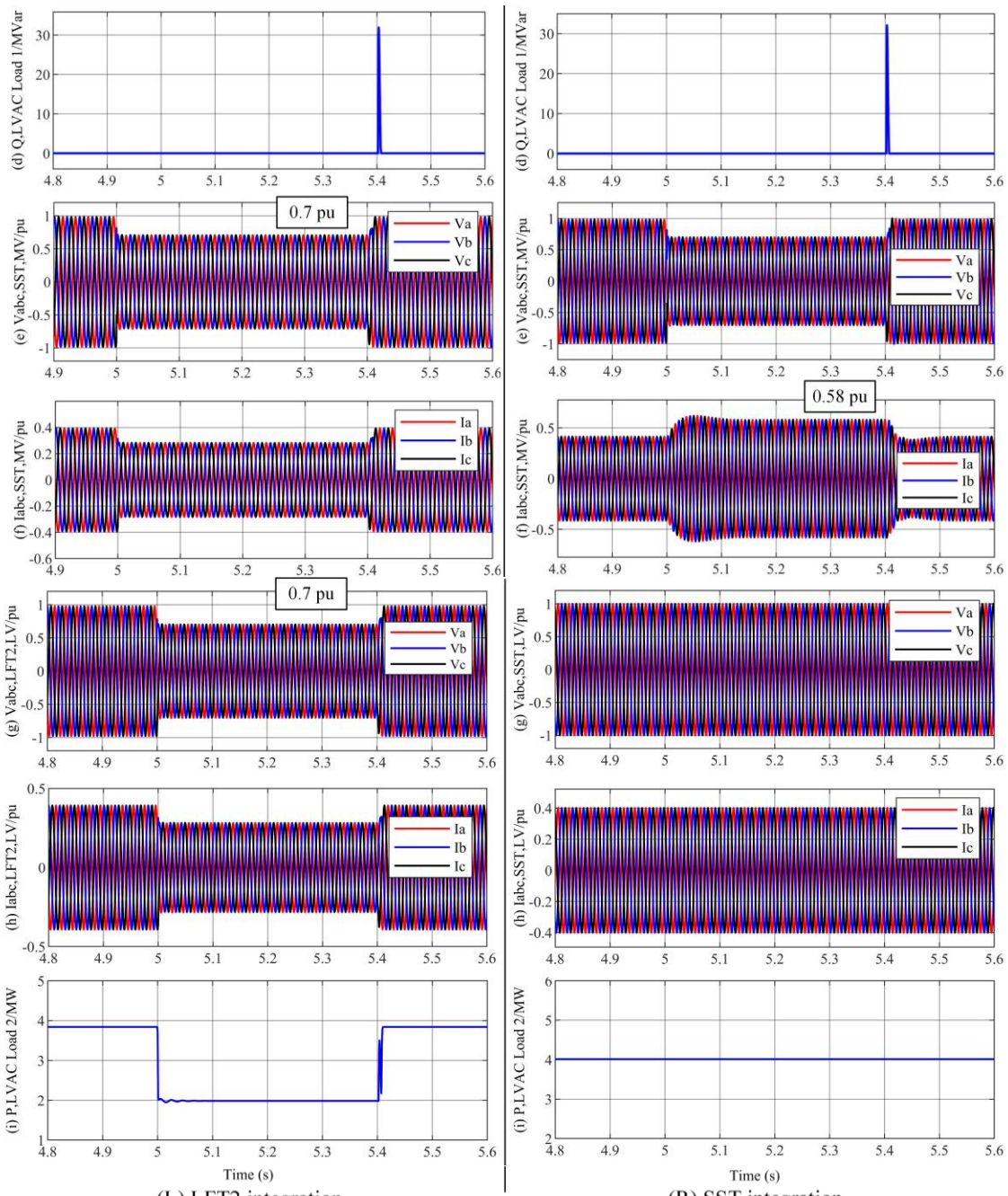
Prior to 5 s, the network is under normal operation, and LFT2/SST supplies 4 MW and 0 MVar to LVAC Load 2. When the fault occurs near LVAC Load 1 at $t = 5s$, the LVAC Load 1 voltage drops to almost zero and the fault current increases and maintain at 4 pu, illustrated in Fig. 4.5 L(a)(b). LVAC Load 1 is out of service as both active and reactive drop to zero, illustrated in Fig. 4.5 L(c)(d). The system performance at 'LFT-LVAC Load 1' side under SST integration is the same as that under LFT2 integration, illustrated in Fig. 4.5 R(a)-(d). Meanwhile, the voltage at MV side under both LFT2 and SST cases decreases to 0.7 p.u due to the fault F1, as seen in Fig. 4.5 L(e) and Fig. 4.5 R(e). With LFT2, the AC voltage at the LVAC Bus 2 and Load 2 is also reduced to around 0.7 pu and consequently, both the primary and second sides of the LFT2 currents are reduced accordingly, as illustrated in Fig. 4.5 L(e)-(j). However, in the case of SST, although the MV AC side voltage is reduced, its LVAC voltage and current remain at the rated value, indicating the supply to LVAC Load 2 is unaffected, as illustrated in Fig. 4.5 R(g)-(j). As a result, the MV side current under SST integration increases to 0.58 pu to match the power needed at LVAC Load 2, as shown in Fig. 4.5 R(f). Under heavy Load 2 condition, the drop of the MV AC voltage may lead to the primary current (MV side) at the SST to reach its limit. Such scenario is similar to Case 4 and power rebalancing will be required, as will be studied late in the section.

At $t = 5.4s$, the fault is cleared and the whole system quickly goes back to normal operation under both LFT2 and SST integrations, as illustrated in Fig. 4.5.

During the fault transients, the MVDC voltage sees small fluctuation but gets back to its rated value in a very short time, while the LVDC voltage is largely undisturbed (through the control of the DC/DC converter), as illustrated Fig. 4.6.



(L) LFT2 integration (R) SST integration



(L) LFT2 integration (R) SST integration

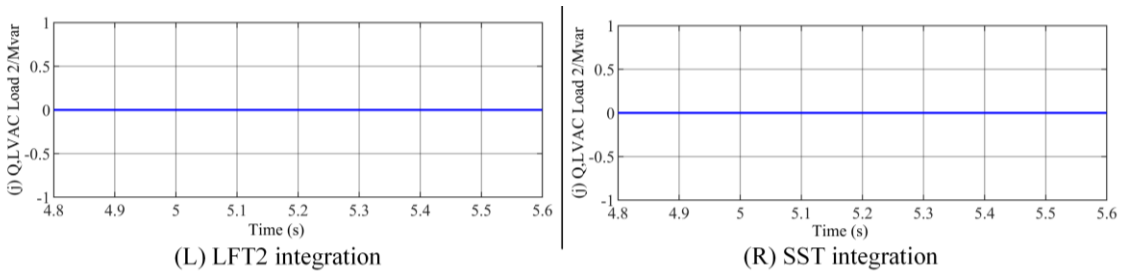


Fig. 4.5 Performance of system in Case 1 with LFT2 (left) and SST (right): (a) fault voltage (3ph); (b) fault current (3ph); (c) LFT transmitted active power; (d) LFT transmitted reactive power; (e) LFT2 MV side voltage (3ph); (f) LFT2 MV side current (3ph); (g) LFT2 LV side voltage (3ph); (h) LFT2 LV side current (3ph); (i) LFT2/SST transmitted active power; (j) LFT2/SST transmitted reactive power.

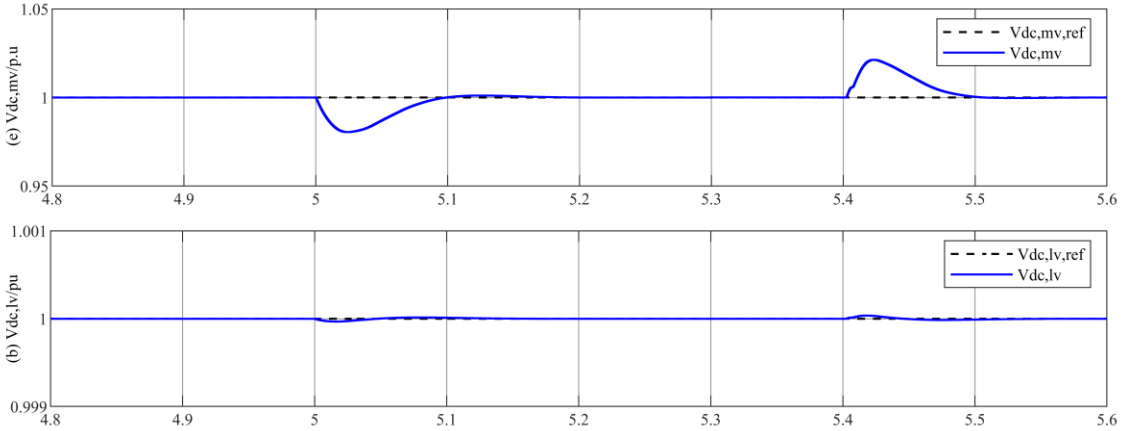


Fig. 4.6 DC controller performance in SST under case study I: (a) MVDC voltage controller; (b) LVDC voltage controller.

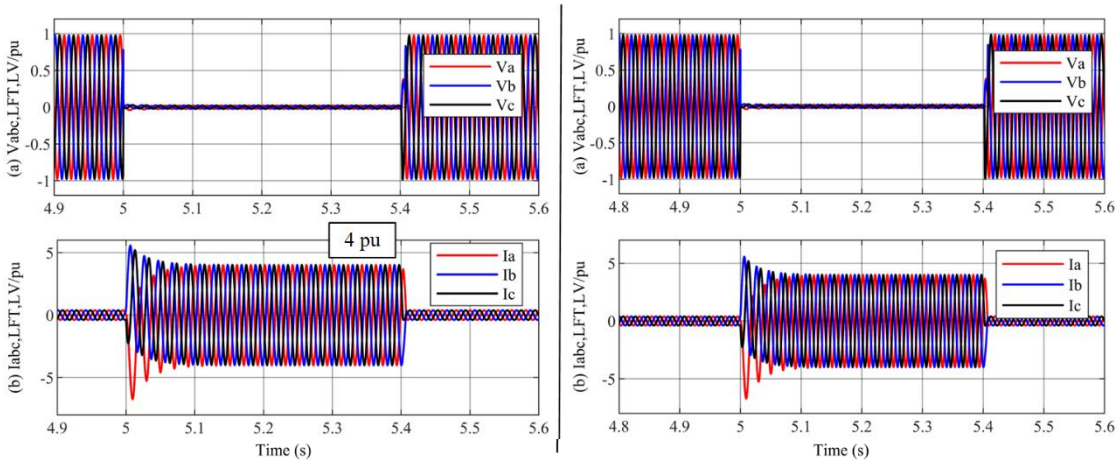
4.3.2 Case 2: Performance under F2

Fig. 4.7 shows the simulation results under F2. Again, the waveforms associated with LFT2 are shown in the left column, while those in the right column refer to SST connection. Prior to 5 s, the network is under normal operation. The CNOP is open and LFT2/SST supplies 4 MW and 0 MVar to LVAC Load 2.

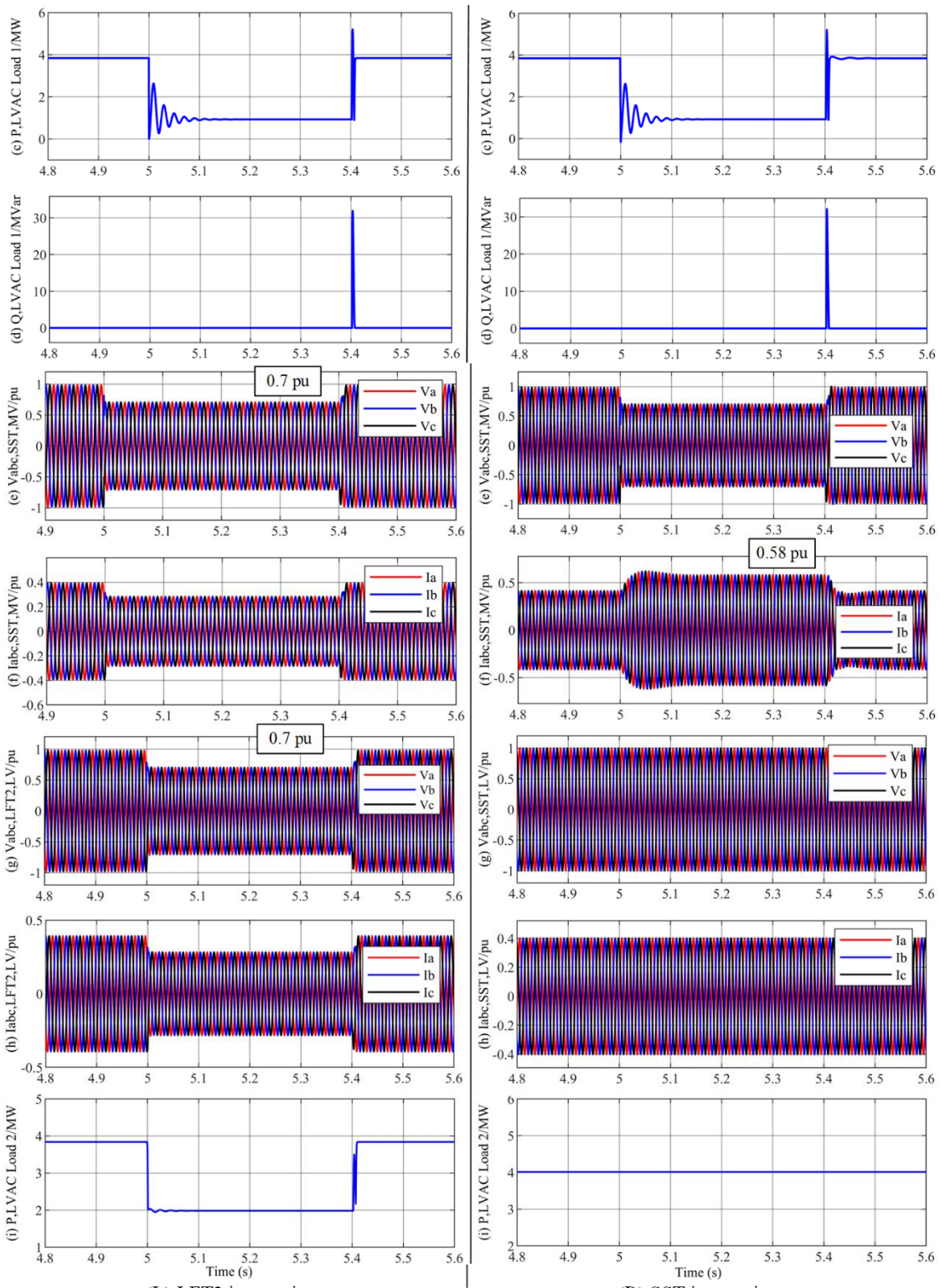
When the three-phase to ground fault occurs near LVAC Load 2 at $t = 5s$, LVAC Load 2 voltage drops to zero and the fault current increases and maintains at around 4 pu with LFT2, as illustrated in Fig. 4.7 L(a)(b). Similar with Case 1, the voltage and current at non-faulted LVAC 1 side are affected under LFT2 integration, illustrated in Fig. 4.7 L(e)(f). The voltage at MV side under LFT2 integration decreases to 0.7 p.u and thus only 2 MW is allocated to LVAC Load 1, as can be seen in Fig. 4.7 L(i)(j). Meanwhile, the system at MV AC and LVAC Load 1 sides under SST integration remains unaffected as the fault at LVAC 2 is not blocked by the SST, as illustrated in Fig. 4.7 R(e)-(j). As seen in Fig. 4.7 R(b), the fault current at the LV side with SST only increases to 1.67 pu, where the increasing fault current indicates the saturation of the controller of LV side converter.

At $t = 5.4s$, the fault is cleared and the whole system backs to normal operation under both LFT2 and SST integrations. During the energy restoration, active power output of SST sees small fluctuation but gets back to normal operation in less than 0.1 s, as can be seen in Fig. 4.7 R(c).

During the fault transients, the MVDC and LVDC voltages in SST fluctuate due to the transient active power unbalance but quickly get back to their rated values, as illustrated Fig. 4.8.



(L) LFT2 integration (R) SST integration



(L) LFT2 integration (R) SST integration

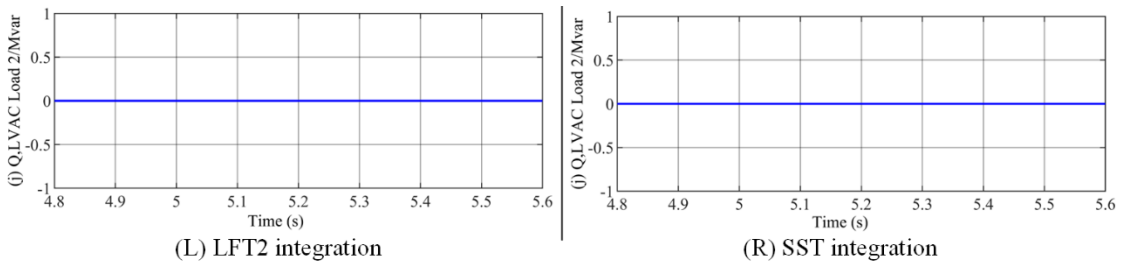


Fig. 4.7 Performance of system in Case 2 with LFT2 (left) and SST (right): (a) LV AC voltage;(b) LFT2/SST LV side AC current; (c) LFT2/SST transmitted active power; (d) LFT2/SST transmitted reactive power; (e) MV side AC voltage; (f) LFT MV side current; (g) LFT LV side voltage; (h) LFT LV side current; (i) LFT transmitted active power; (j) LFT transmitted reactive power.

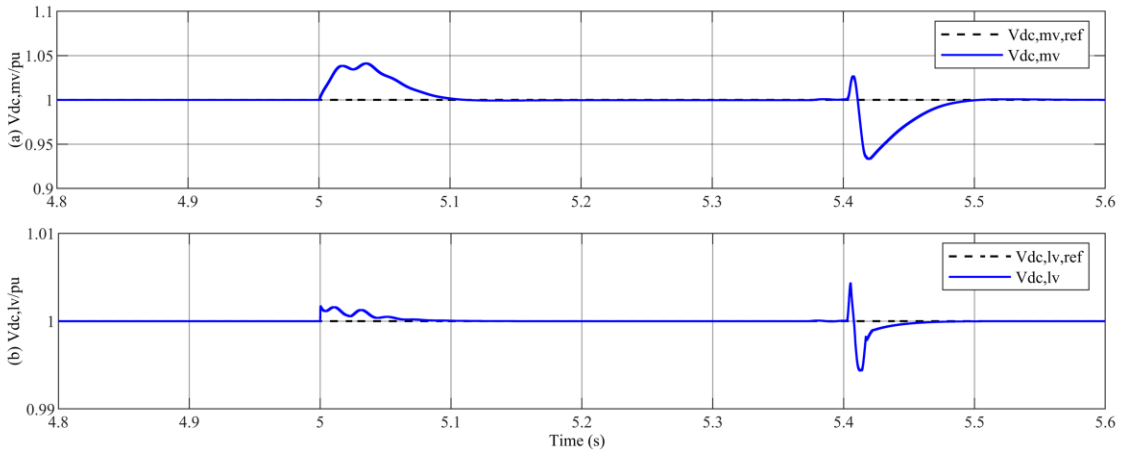


Fig. 4.8 DC controller performance in SST under Case 2: (a) reference and measured MVDC voltages controller; (b) reference and measured LVDC voltages.

4.3.3 Case 3: Performance under F1 with closed CNOP

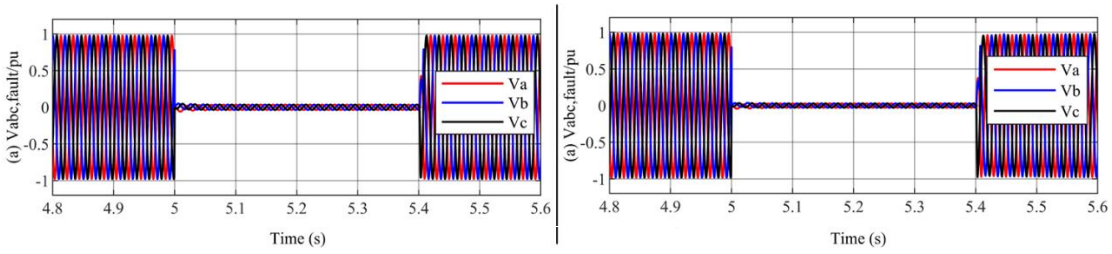
In this case study, the CNOP is closed and fault F1 is considered. Similar to Case 1 and 2, the LFT2 and SST are tested in the network, respectively. The simulation results are shown in Fig. 4.9. Prior to 5 s, the network is under normal operation. The CNOP is closed and power is dispatched naturally/as SST controlled, where LFT2/SST supply 4 MW and 0 MVar to LVAC Load 2.

When the fault occurs near LVAC Load 1 at $t = 5s$, with LFT2 configuration, both LVAC Load 1 and 2 voltages drop to zero due to the closure of CNOP, and the fault current increases maintains at 6.2 pu with LFT and LFT2 each contributing 3.1 pu fault current, as illustrated in Fig. 4.9 L(a)-(f). Meanwhile, the MV side of the network is also affected and the voltage drops to 0.38 pu, as seen in Fig. 4.9 L(g)(h).

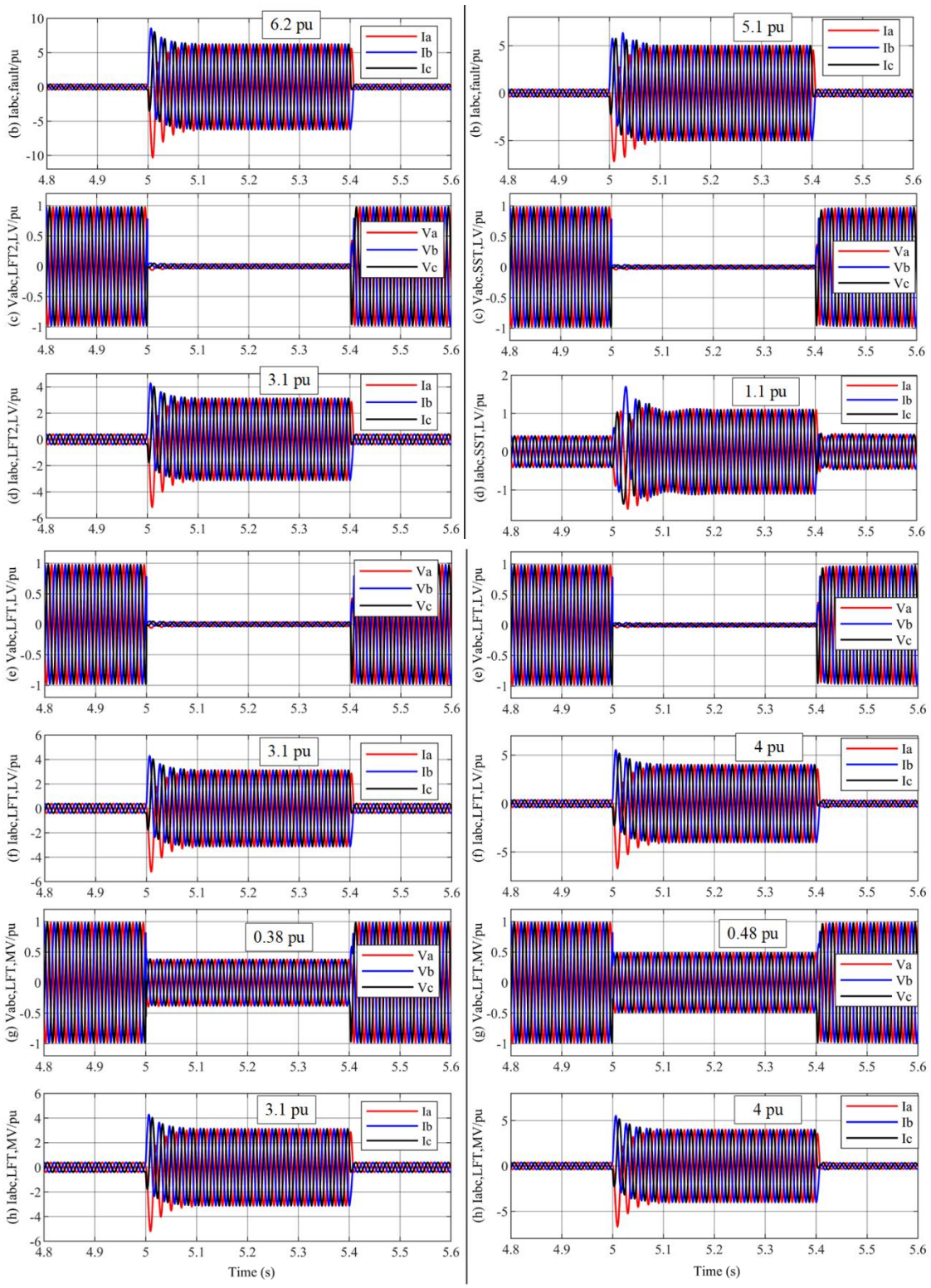
Under the network with SST integration, both voltages at LV side drop to zero when F1 occurs, as shown in Fig. 4.9 R(a)(c)(f). The fault current contribution from LFT is around 4 pu whilst the SST only contributes around 1.1 pu, as can be seen in Fig. 4.9 R(f) and (d), respectively. As a result, the fault current stabilises around 5.1 pu, illustrated in Fig. 4.9 L(b). The equivalent short circuit impedance increases under SST integration (due to its current limiting) when compared to LFT2 configuration, and consequently, the MV side voltage drops to 0.71 pu (compared to 0.38 pu with LFT2 integration), as illustrated in Fig. 4.9 L(g)(i). This also mean the fault current contribution at LFT side (i.e., 4 pu) is higher than LFT2 (3.1 pu).

From $t = 5.4s$, the fault is cleared and the whole system is back to normal operation under both LFT2 and SST integrations. The power output of SST quickly goes back to normal operation, as seen in Fig. 4.10(c)(d).

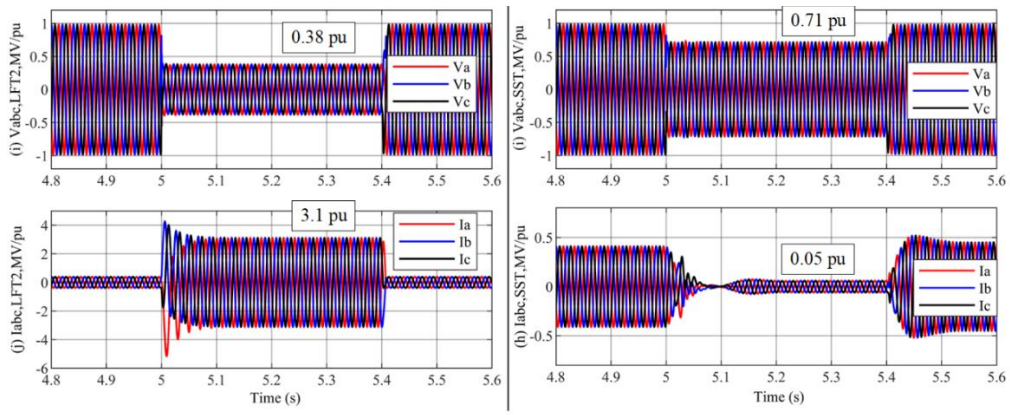
During the fault transients, both MV and LV DC voltages in SST are well controlled with only small fluctuations, and quickly go back to their rated values after short transients, as can be seen in Fig. 4.10(a)(b).



(L) LFT2 integration (R) SST integration



(L) LFT2 integration (R) SST integration



(L) LFT2 integration (R) SST integration

Fig. 4.9 Performance of system in Case 3 with LFT2 (left) and SST (right): (a) fault voltage; (b) fault current; (c) LFT2/SST LV side voltage; (d) LFT2/SST LV side current; (e) LFT LV side voltage; (f) LFT LV side current; (g) LFT MV side voltage; (h) LFT MV side current; (i) LFT2/SST MV side voltage; (j) LFT2/SST LV side voltage.

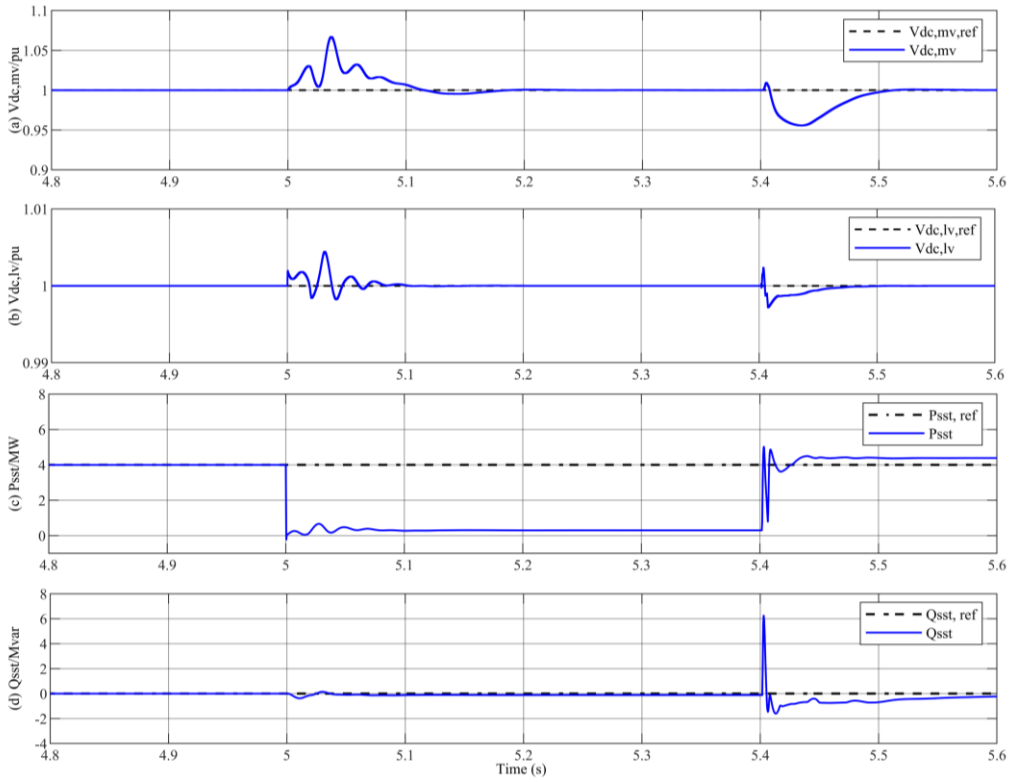


Fig. 4.10 Controller performance in SST under case study III: (a) MVDC voltage controller; (b) LVDC voltage controller; (c) SST output active power controller; (d) SST output reactive power controller.

4.3.4 Case 4: Performance of active power limiting control under grid-forming operation

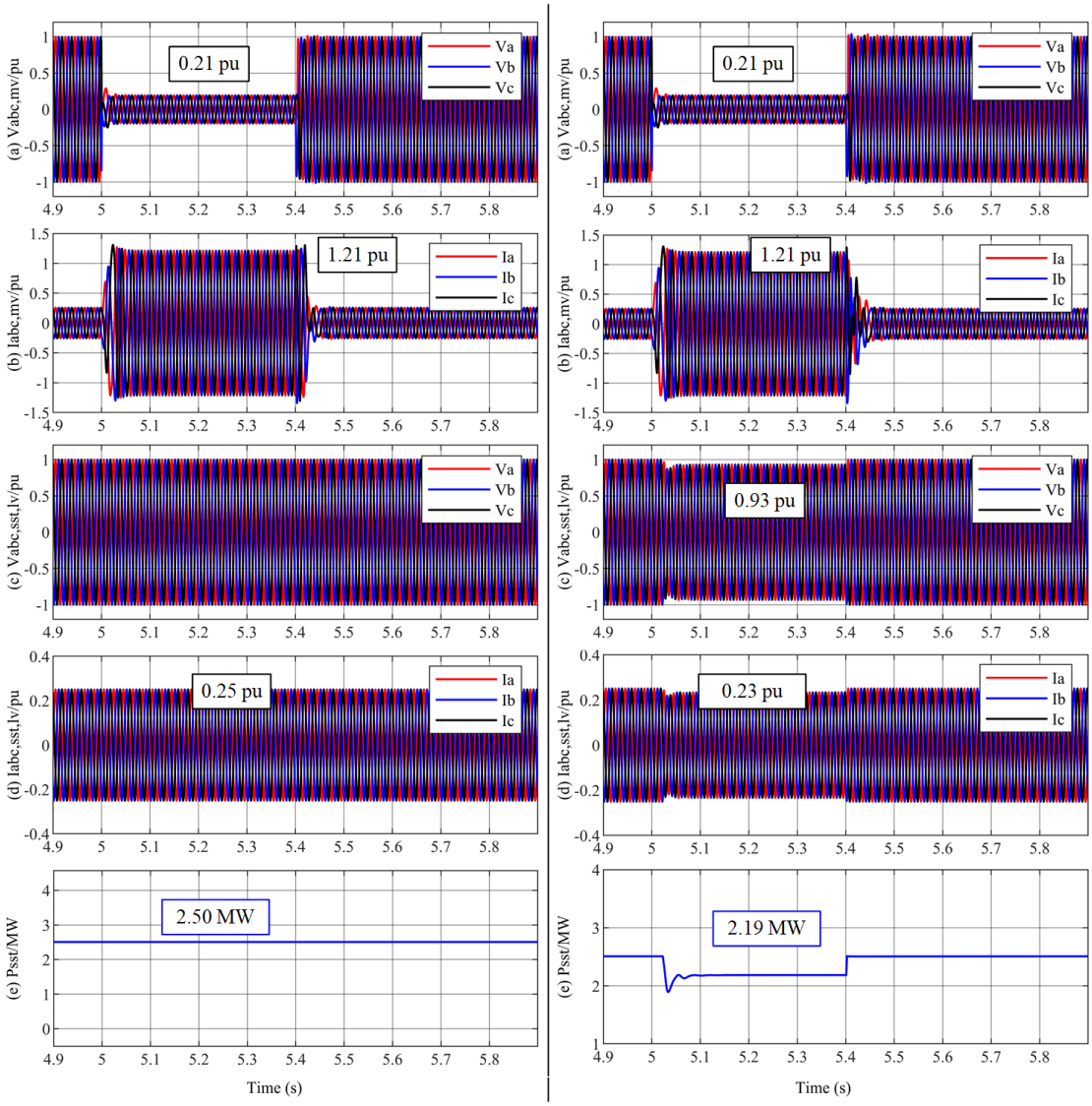
The effectiveness of active power limiting control under grid forming operation for under- and over-voltage cases on the MVDC of the SST is examined. In case 1, it is shown that the LVAC2 voltage drops to 0.7 pu with LFT2 integration while it remains normal value with SST integration. However, when heavy Load 2 condition is considered, the drop of MVAC voltage may lead to the primary current (MV side) at SST reaching its limit and DC voltages in SST will be unbalanced. From view of improving reliability of SST under network faults, active power limiting control will be required, which will be assessed in this study.

As shown in Fig. 4.1(a), a three-phase to ground fault occurs at the MV grid (F3). Wherein, the rated power at LVAC Load 2 is 2.5 MW. The DG in the simulation is disconnected from Bus 2. As the case investigates the performance of the proposed active power limiting control, the operation at LFT side will not be shown. Prior to 5 s, the network is under grid-forming operation. The CNOP is open and the power is dispatched naturally, where SST supplies 2.5 MW to LVAC Load 2.

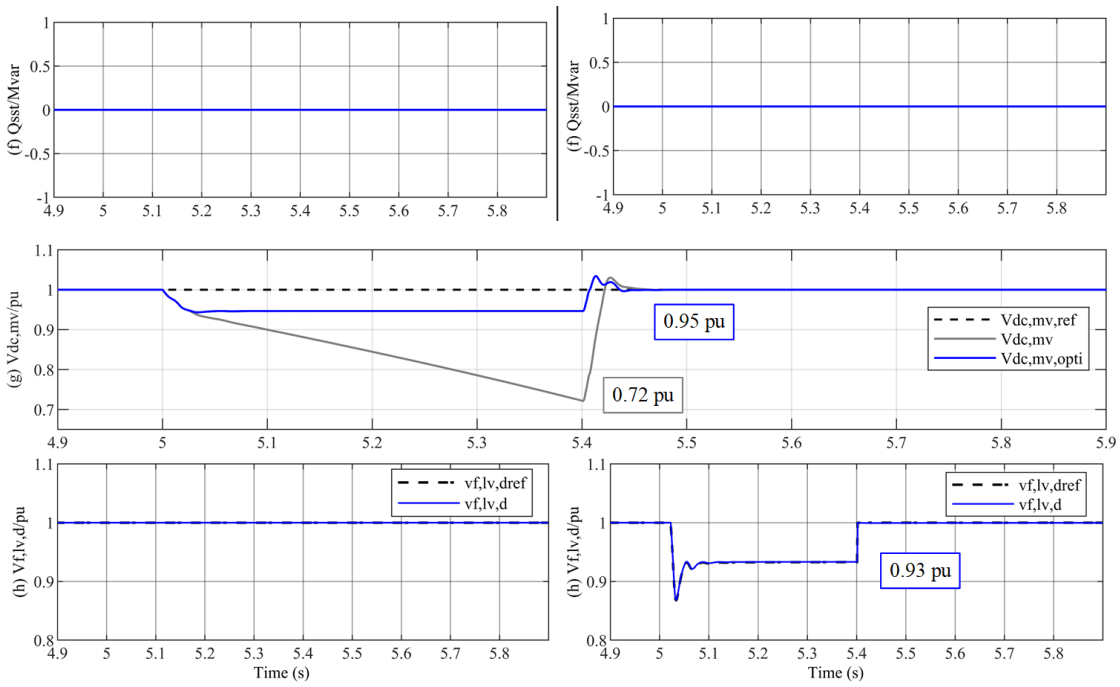
The simulation results are illustrated in Fig. 4.11. Before the fault, the SST operates at normal operation and the voltages and currents are under well controlled. During the fault, it can be observed in Fig. 4.11L(a) that phase voltage at MV grid 2 drops to 0.21 pu for a duration of 400 ms due to the fault. The current reaches the limit of 1.21 pu at MVAC side, illustrated in Fig. 4.11L(b). Consequently, the MV grid can only provide 2.24 MW (calculated according to the Fig. 4.11R(a)(b)) to the load side, which leads to the MVDC voltage drop. As illustrated as the grey line in Fig. 4.11(g), the MVDC voltage continues falling to about 0.72 pu until the fault is clear. LVAC remains normal operation (illustrated in Fig. 4.11L(c)(d)(h)) as LVDC voltage is under control. On the other hand, the SST MV side converter with active power limiting goes into current limiting operation after fault occurs, which is similar with that without the proposed control, illustrated in Fig.

4.11R(a)(b). The MVDC voltage drop is detected by the proposed control and the d-axis voltage reference at the DC/AC converter is thus reduced to 0.93 pu according to the droop characteristic, illustrated in Fig. 4.11R(h). The active power re-balances and the MVDC voltage remains at 0.95 pu, shown as blue line in Fig. 4.11(g). After the fault is cleared, the MV grid recovers to supply the SST and the load sides. As the MVDC voltage recovers to track the reference, the active power output of the SST recovers to the normal operation, shown in Fig. 4.11R(a)-(h).

It is noted here that the case study is designed to show the irrepressible MVDC descent without active power limiting. When the power unbalance becomes larger, the faster descent to MVDC voltage will occur, which will lead to the converter blocking activated (Normally happen when MVDC voltage is less than 0.7 pu.). Consequently, the LVDC and LVAC voltage at SST will collapse, resulting in the power outage of the downstream network. Also, the reduced voltage at LV network will only be considered as the final remedy to avoid a larger scale voltage collapse under voltage load shedding (UVLS).



(L) Normal operation (R) Active power limiting control integration



(L) Normal operation (R) Active power limiting control integration

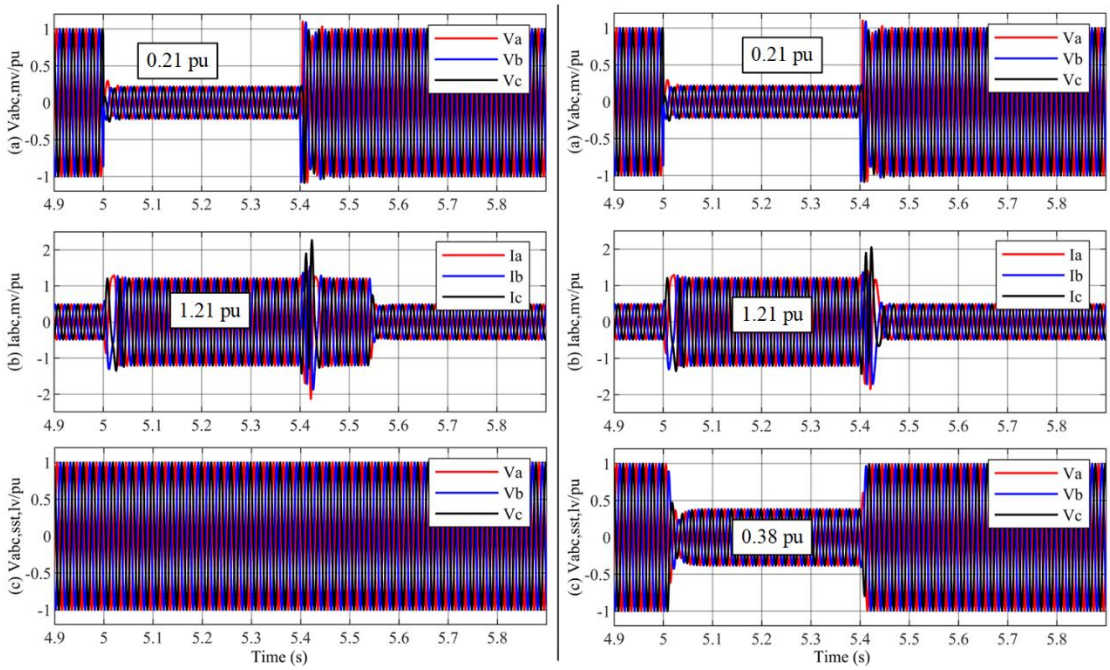
Fig. 4.11 Performance of system under MVDC under-voltage condition in Case 4 without active power limiting control (left) and with active power limiting control (right): (a) SST MV side voltage; (b) SST MV side current; (c) SST LV side voltage; (d) SST LV side current; (e) SST active power output; (f) SST reactive power output; (g) SST MVDC voltage; (h) SST LV side d-axis voltage.

To examine active power limiting control performance during over-voltage condition, the DG in the simulation supplies power locally and transmits surplus power to MV network via SST. The rated power at LVAC Load 2 is 4 MW. Prior to 5 s, the network is under grid-forming operation, the CNOP is open, and DG outputs 9 MW where 4 MW supplies LVAC Load 2 and the surplus 5 MW is transmitted to MV Network via SST.

At $t = 5s$, the MV grid 2 AC voltage drops to 0.21 pu for a duration of 400 ms (20 cycles for 50 Hz). The simulation results are illustrated in Fig. 4.12. During the fault, it can be observed in Fig. 4.12L(a) that phase voltage at MV grid 2 drops to 0.21 pu due to the fault. As the surplus 5 MW is kept transmitting to MV Network 2, shown in Fig. 4.12L(e), the

current at MV Network 2 reaches to the current limit of 1.2 pu, illustrated in Fig. 4.12L(b). The surplus power leads to 1.93 pu MVDC over-voltage, illustrated as the grey line in Fig. 4.12(g). On the other hand, with active power limiting control, the MVDC voltage increase is detected and the d-axis voltage reference at the LV DC/AC converter is thus reduced to 0.38 pu, illustrated in Fig. 4.12R(h). SST MV side converter also goes into current limiting operation, which is similar with that without the proposed control, illustrated in Fig. 4.12R(a)(b). The active power re-balances and the MVDC voltage remains at 1.08 pu, shown as blue line in Fig. 4.12(g). Thus, 2.87 MW can be transmitted to the MV network, illustrated in Fig. 4.12R(e)(f). After the fault is cleared, the MV network recovers, the MVDC voltage recovers to track the reference, and the LV side voltage of the SST recovers to the normal level, shown in Fig. 4.12R(a)-(h).

It is noted here that the case study is designed to show the irrepressible MVDC voltage increase without active power limiting of SST. Considering the sensitivity of power converters, the converter will need to be blocked (Normally blocked when MVDC voltage is over 1.1 pu). Consequently, the LV network will also collapse.



(L) Normal operation (R) Active power limiting control integration

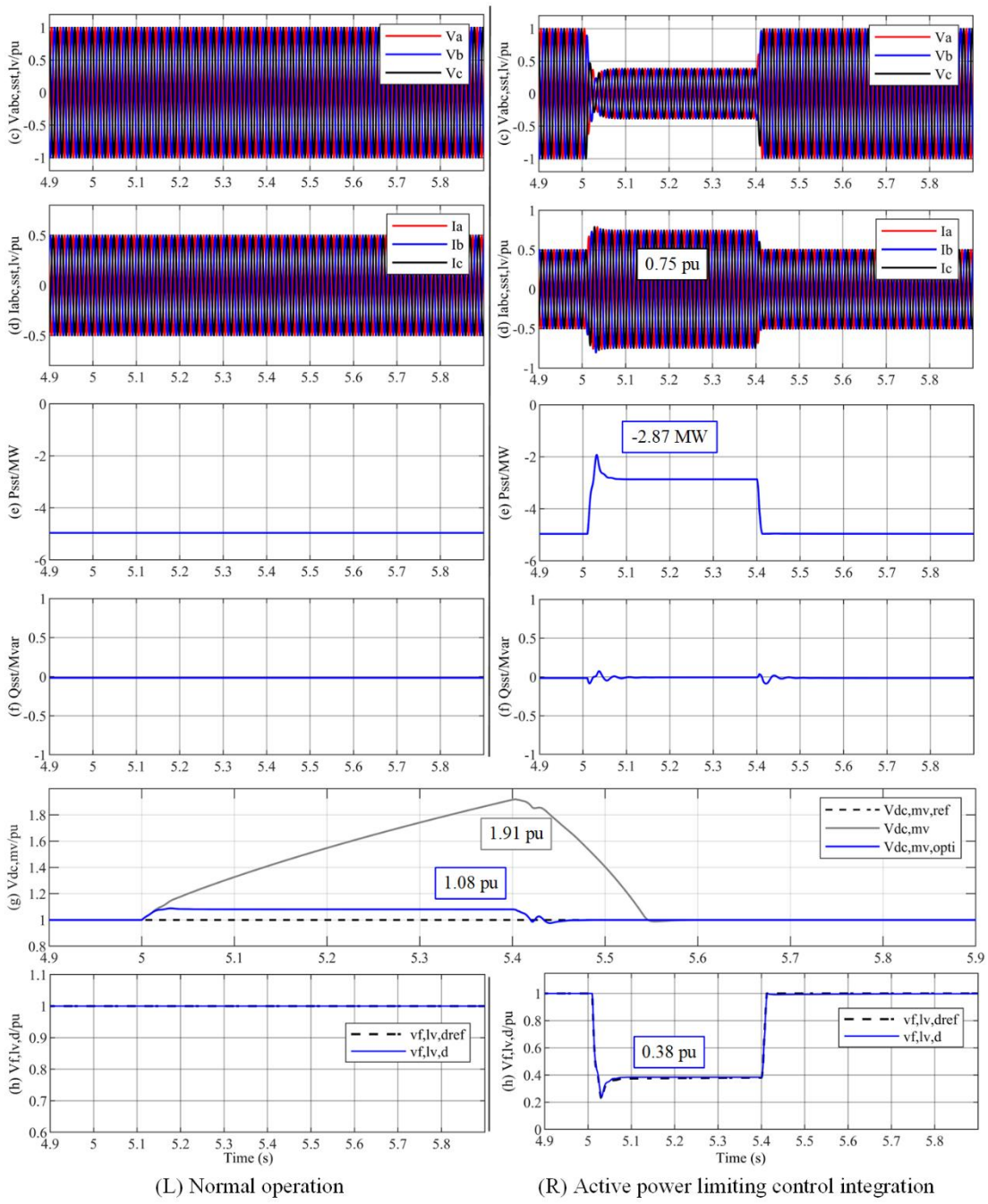


Fig. 4.12 Performance of system under MVDC over-voltage condition in Case 4 without active power limiting control (left) and with active power limiting control (right): (a) SST MV side voltage; (b) SST MV side current; (c) SST LV side voltage; (d) SST LV side current; (e) SST active power output; (f) SST reactive power output; (g) SST MVDC voltage; (h) SST LV side d-axis voltage.

In Fig. 4.13 and Fig. 4.14, the performance of the active power limiting control during grid-forming operation when the fault voltage are 0.2 pu, 0.3 pu, 0.5 pu, 0.7 pu at MV Network 2 illustrated. Wherein, SST transmits 8 MW from MV Network 2 to LVAC Load 2 in Fig. 4.13 while transmits 8 MW from LVAC to MV Network 2 in Fig. 4.14. It can be easily seen the d-axis voltage reference is effectively adjusted to re-balance the power through SST, while MVDC voltage remains 10% over- or under- voltage.

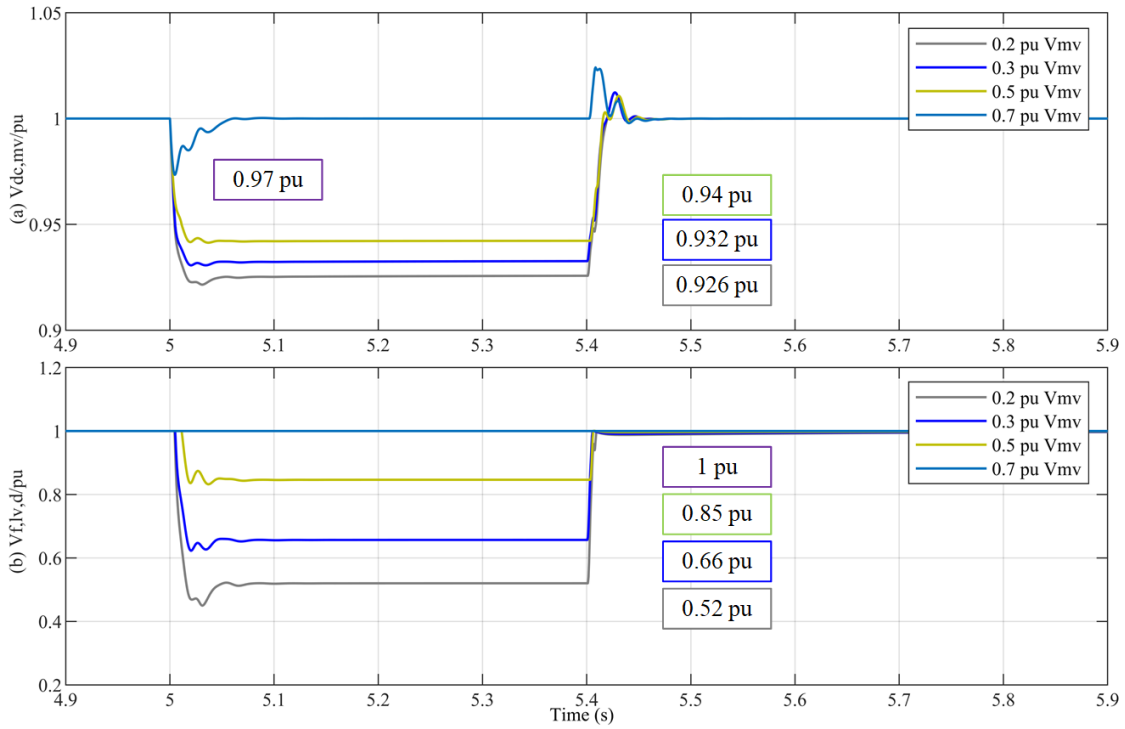


Fig. 4.13 Performance of active power limiting control under under-voltage condition with different MV side fault voltages (0.2 pu; 0.3 pu; 0.5 pu; 0.7 pu) in Case 4: (a) SST MVDC voltage; (b) SST LVAC d-axis voltage.

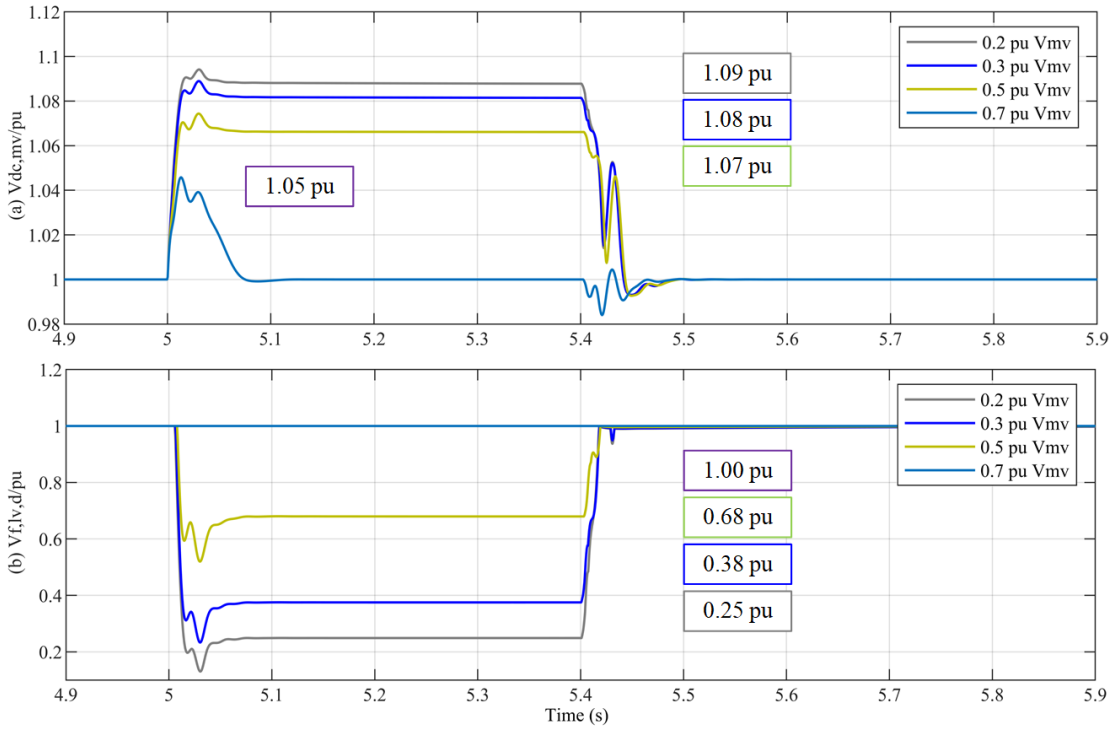


Fig. 4.14 Performance of active power limiting control under over-voltage condition with different MV side fault voltages (0.2 pu; 0.3 pu; 0.5 pu; 0.7 pu) in Case 4: (a) SST MVDC voltage; (b) SST LVAC d-axis voltage.

4.3.5 Case 5: Performance of active power limiting control under grid-connected operation

For Case 5, the test radial distribution network with SST integration is illustrated in Fig. 4.1(b). Compared with the test network illustrated in Fig. 4.1(a). The main differences are that LFT and SST are supplied by MV Network 1 and 2 separately, and in Case 5 the CNOP is closed and the LV SST converter operates under grid-connected mode. The network parameters remain the same as those shown in Table 4.1. To examine active power limiting control performance during under-voltage condition, a three-phase-to-ground fault occurs at the remote side of MV grid 2 (F4), shown in Fig. 4.1(b). The DG is disconnected, and the power reference of SST is 3 MW and 0 MVar, respectively. The CNOP is closed and supplies around 1 MW to LVAC Load2.

At $t = 5s$, a three-phase-to-ground fault occurs at near MV Network 2 side with duration of 400 ms. The simulation results are illustrated in Fig. 4.15L. During the fault, it can be observed in Fig. 4.15L(a) that phase voltage at MV network 2 drops to 0.2 pu due to the fault. The current reaches to the current limit 1.2 pu at MVAC side, illustrated in Fig. 4.15L(b). SST can only receive around 2.4 MW from MV network while the order for the LV side converter is 3 MW to LVAC Load 2. The unbalanced power results in MVDC voltage drops. Without active power limiting control, the MVDC voltage drops to about 0.202 pu, shown as the grey line in Fig. 4.15(g). On the other hand, the proposed active power limiting control observes the MVDC voltage drop and reduces the active power reference at DC/AC converter to 2.32 MW, shown in Fig. 4.15R(c), while the SST MV side converter also goes into current limiting operation, which is similar with that without the proposed control. The active power thus re-balances and the MVDC voltage remains at 0.938 pu, shown as blue line in Fig. 4.15(e). The extra 0.62 MW of LVAC Load 2 is supplied by MV Network 1 via the CNOP, illustrated in Fig. 4.15L(h)(i). After the fault is cleared, the MV Network 2 recovers to supply the SST and the load sides. As the MVDC voltage recovers to track the reference, the active power output of the SST recovers to the nominal value, shown in Fig. 4.15R(a)-(h).

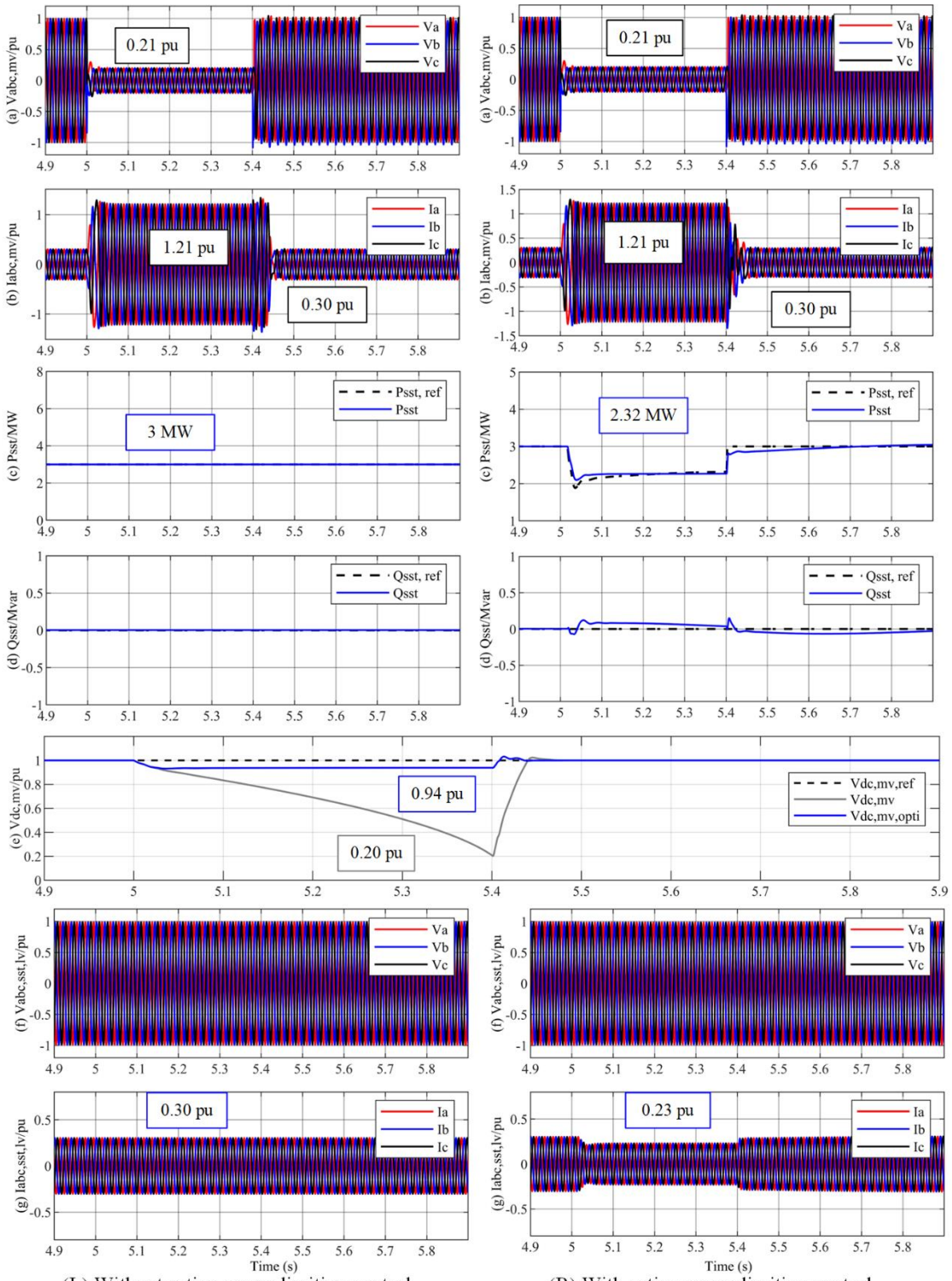
It is noted here that the case study is designed to show the irrepressible MVDC voltage reduction without active power limiting. When the power unbalance becomes larger, the faster descent to MVDC voltage will occur, which will lead to the converter blocking activated (Normally happen when MVDC voltage is less than 0.7 pu.). Consequently, the LVDC and LVAC voltages at SST will collapse, resulting in the power outage of the downstream network.

To examine active power limiting control performance during over-voltage condition, the DG in the simulation is connected at LVAC Bus 2 and a three-phase ground fault occurs at the remote side of MV Network 2 (F4), shown in Fig. 4.1(b). Prior to 5 s, the DG produces 9 MW while the SST transmits 5 MW and 0 MVar to MVAC Network 2. The simulation results are shown in Fig. 4.16.

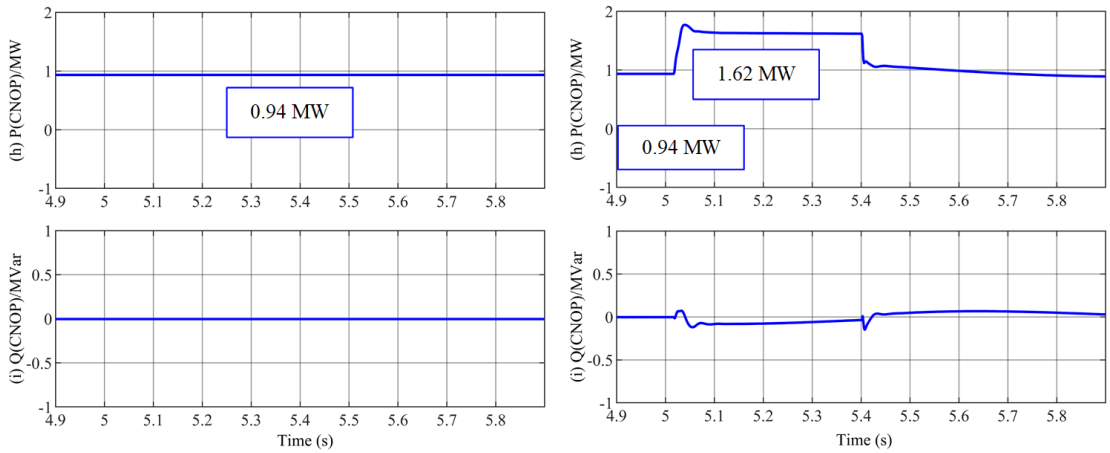
When the fault occurs near MV Network 2 at $t = 5s$, MV Network 2 voltages drop to 0.22 pu, and fault current increases and is held at 1.2 pu due to current limiting in MV converter, as illustrated in Fig. 4.16L(a)(b). The power unbalance in MV converter leads to 1.89 pu over-voltage at MVDC voltage, illustrated as grey line in Fig. 4.16 (e). On the other hand, with active power limiting control, the MVDC voltage increase is detected by the proposed control and active power reference at DC/AC converter is thus changed from -5 MW to -2.91 MW, illustrated in Fig. 4.16R(c). The active power re-balances and the MVDC voltage remains at 1.07 pu, shown as blue line in Fig. 4.16(e). The fluctuation of reactive power in the LV DC/AC converter, illustrated in Fig. 4.16R(d), is due to the small fluctuation of reactive power across the NCOP during the disturbance. After the fault is cleared at $t = 5.4s$, the MV network recovers and the active power output of the SST recovers to the normal setpoint of -5 MW, shown in Fig. 4.16R(a)-(h).

It is noted here that the case study is designed to show the irrepressible MVDC voltage increase without active power limiting of SST. Considering the sensitivity of power converters, the converter will need to be blocked (Normally when MVDC voltage is over 1.1 pu). Consequently, the LV network will also collapse.

In Fig. 4.17 and Fig. 4.18, the performance of the active power limiting control during grid-connected operation when the fault voltage are 0.2 pu, 0.3 pu, 0.5 pu, 0.7 pu at MV Network 2 illustrated. Wherein, SST transmits 8 MW to load side in Fig. 4.17 and 8 MW to MV Network 2 in Fig. 4.18. It can be easily seen the active power reference is effectively adjusted to re-balance the power through SST, while MVDC voltage remains 10% over- or under- voltage.

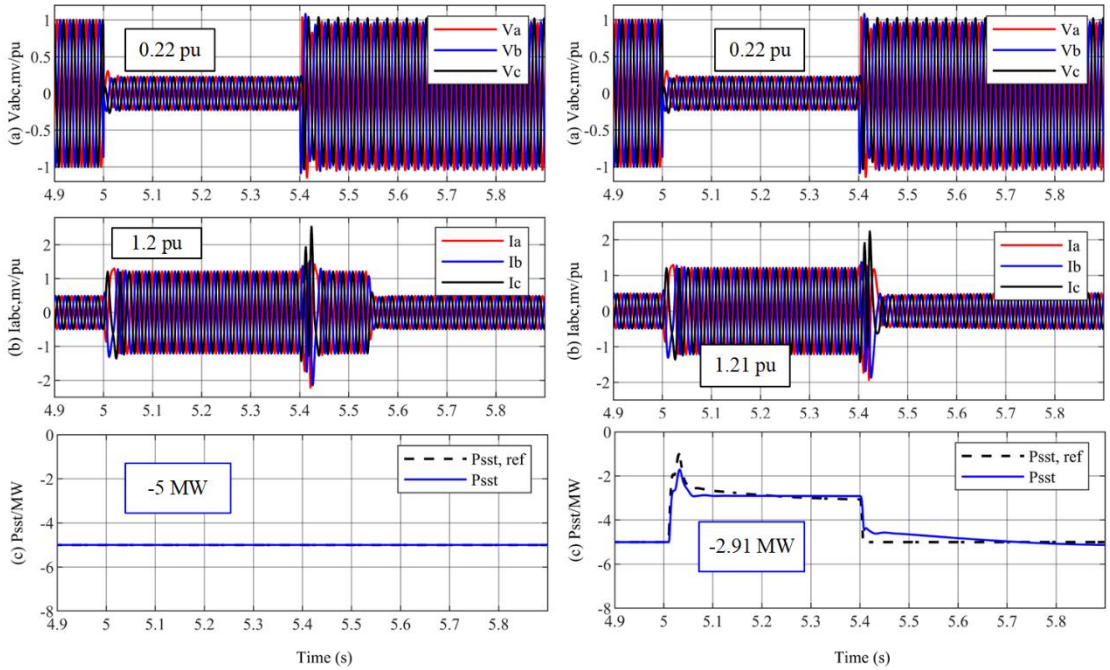


(L) Without active power limiting control (R) With active power limiting control

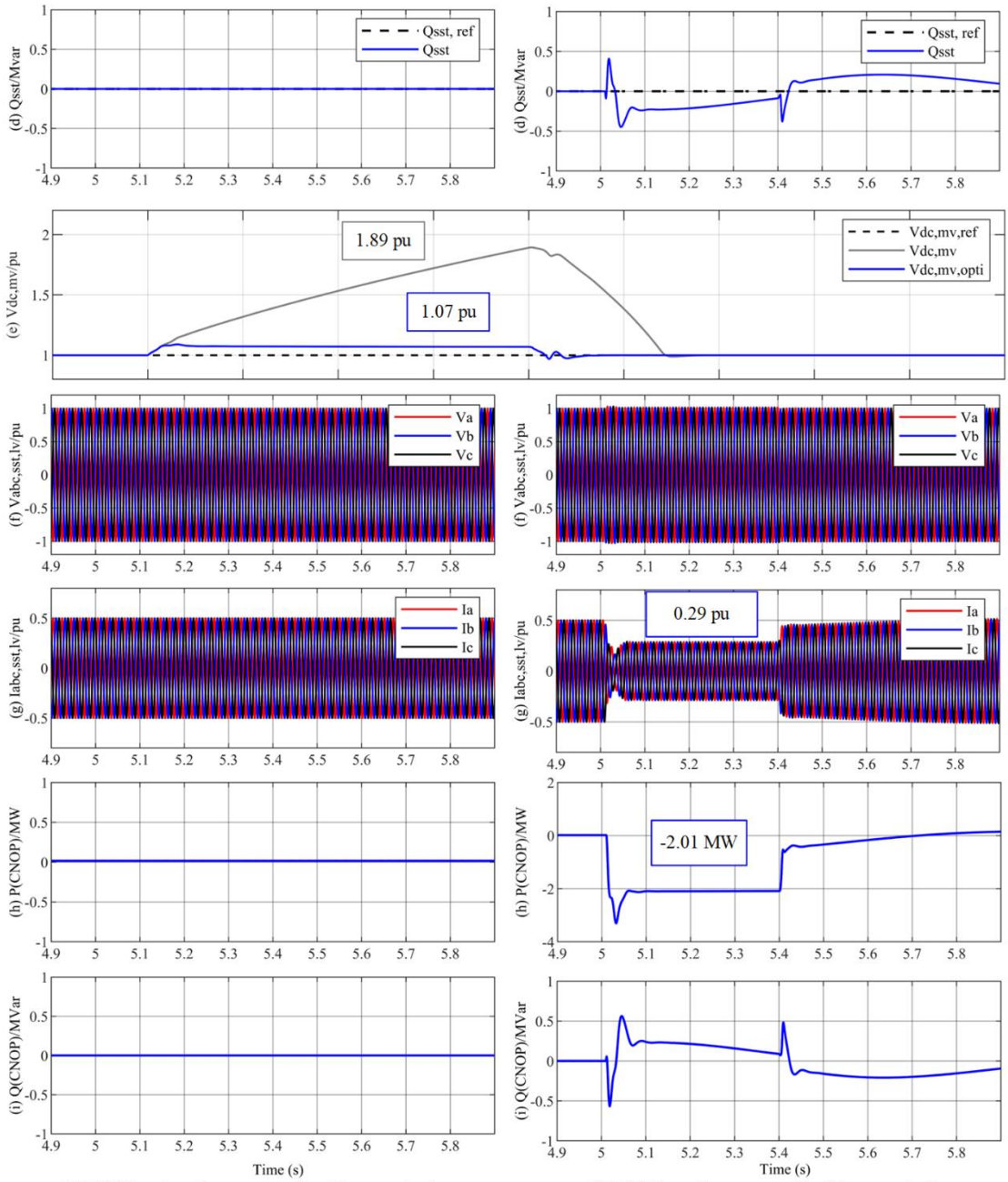


(L) Without active power limiting control (R) With active power limiting control

Fig. 4.15 Performance of system under MVDC under-voltage condition in Case 5 without active power limiting control (left) and with active power limiting control (right): (a) SST MV side voltage; (b) SST MV side current; (c) SST LV side active power output; (d) SST LV side reactive power output; (e) SST MVDC voltage; (f) SST LV side voltage; (g) SST LV side current; (h) CNOP transmitted active power; (i) CNOP transmitted reactive power.



(L) Without active power limiting control (R) With active power limiting control



(L) Without active power limiting control (R) With active power limiting control

Fig. 4.16 Performance of system over-voltage condition in case study in Case 5 without active power limiting control (left) and with active power limiting control (right): (a) SST MV side voltage; (b) SST MV side current; (c) SST LV side active power output; (d) SST LV side reactive power output; (e) SST MVDC voltage; (f) SST LVDC voltage; (g) SST LV side voltage; (h) SST LV side current; (i) CNOP transmitted active power; (j) CNOP transmitted reactive power.

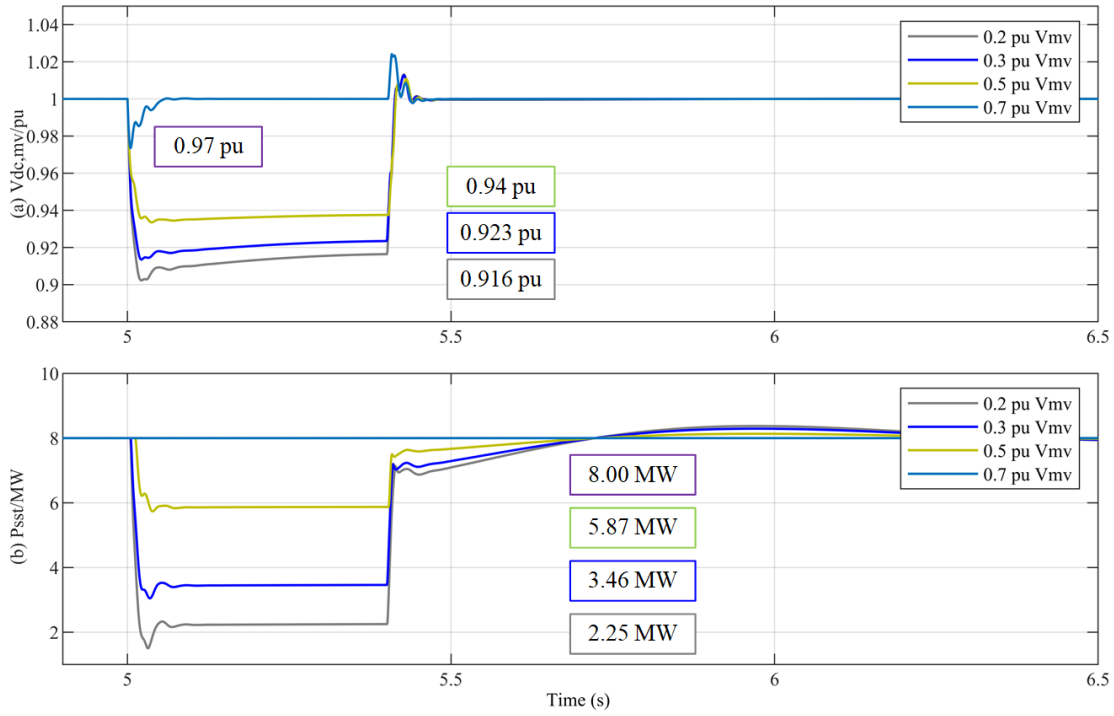
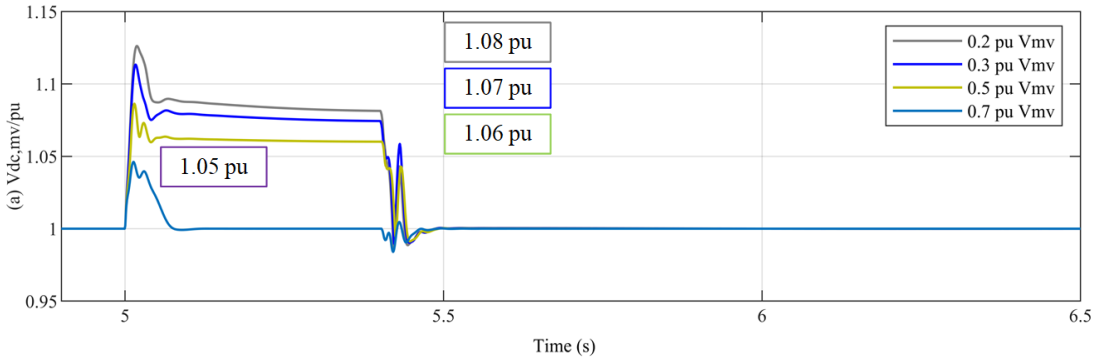


Fig. 4.17 Performance of active power limiting control under under-voltage condition with different MV side fault voltage in Case 5: (a) SST MVDC voltage; (b) SST power output under 0.2 pu MV fault voltage; (c) SST power output under 0.3 pu MV fault voltage; (d) SST power output under 0.5 pu MV fault voltage; (e) SST power output under 0.7 pu MV fault voltage.



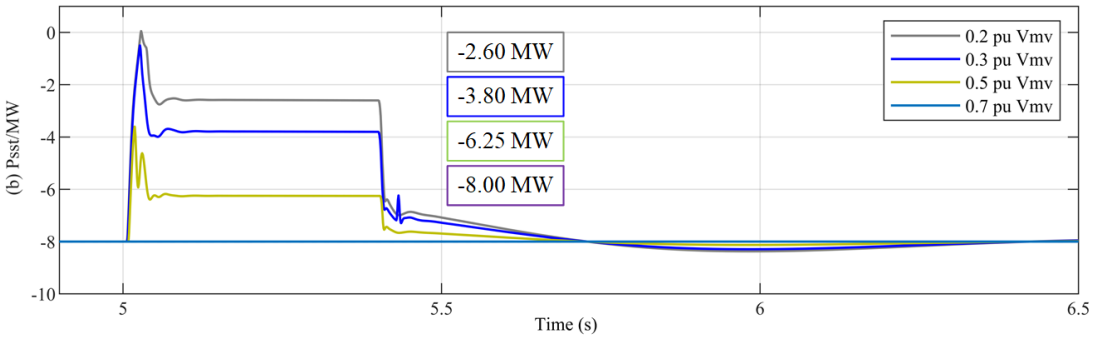


Fig. 4.18 Performance of active power limiting control under over-voltage condition with different MV side fault voltage in Case 5: (a) SST MVDC voltage; (b) SST power output under 0.2 pu MV fault voltage; (c) SST power output under 0.3 pu MV fault voltage; (d) SST power output under 0.5 pu MV fault voltage; (e) SST power output under 0.7 pu MV fault voltage.

4.4 Summary

The fault performance of SST during the network faults is investigated in this chapter. Benefitting from the controllability, SST can isolate fault current from the healthy part of the network and reduce fault current contribution from SST when compared with LFT. The proposed active power limiting control associate MVDC voltage variation and d-axis voltage (grid-forming operation) or active power reference (grid-connected operation) of DC/AC converter to achieve adaptive active power rebalance during the fault. The MVDC voltage thus remains less than 10% fluctuation of rated voltage level until the fault is cleared. The proposed control is validated under both under- and over- voltage condition, which maintains SST operation during fault condition from unnecessary blocking due to the MVDC voltage fluctuation. The benefits brought by the additional control schemes of the SST are verified by case studies in MATLAB/Simulink. The effectiveness of the proposed control on reducing MVDC voltage variation and improving dynamic response is also verified by simulations.

Chapter 5 Coordinated Operation and Protection for Hybrid AC and DC Distribution Networks Interfaced by SST

Within a typical SST, there are a number of intermediate DC stages. For example, for the SST topology studied in this thesis, there are MVDC and LVDC stages. Considering many renewable generations, storages, loads (e.g., EV chargers) are naturally DC, there will be benefits to establish an intermediate DC network within the SST for direct connection of DC generations and loads. This chapter investigates the potential of introducing DC network to SST-based distribution network. In this chapter, the types of DC network integration are reviewed and discussed first. A coordinated control of the SST and DC network is then proposed for optimising the operation of the SST-based hybrid AC/DC distribution network. In addition, the impact of the DC fault on the SST-based distribution network is investigated. DC fault characterisation of the proposed system is assessed. On the basis, DC fault clearance requirement for TAB and their effectiveness are raised and further assessed.

5.1 Interfacing DC network by the SST

A DC network can be accessed to conventional MV/LV AC networks by a direct AC/DC conversion stage, whereas for the SST, the DC network can be established using the DC-link of the SST. In this chapter, only LVDC network is considered while many of the concepts can also be applied to MVDC system using the MVDC link of the SST. For designing an SST-based AC/DC hybrid distribution network, voltage level and configurations are discussed in this section.

5.1.1 Voltage rating of the LVDC network

According to the IEC 60038 Standard [158], the voltage level of LVDC ranges from 120 V to 1500 V. However, from the deployed LVDC projects, the voltage level of the LVDC network has not been well-defined compared to those of medium voltage and high voltage DC systems. Projects in Finland (750V/±750V) [159-161], Netherlands (±350V/±700V) [162], Korea (±750V/380V/±190V) [163], and China (±750V/220V) [164] were designed with different approaches. Meanwhile, the DC voltage level needs to consider the required DC current (power), ease of connection to other AC and DC sources and loads. For simplifying voltage level matching between the SST and LVDC network, the LVDC link voltage of 750 V is considered in this chapter.

5.1.2 Configurations for interfacing the LVDC network

In Fig. 5.1, potential configurations of SST to interface the LVDC network are illustrated. As illustrated in Fig. 5.1(a) and (b), the LVDC network can be integrated to the LVAC side of the SST, through an AC/DC converter (Fig. 5.1(a)) or connected through a LFT and an AC/DC converter (Fig. 5.1(b)), which has been widely used in DC microgrid [165]. Both configurations can provide fault isolation capability, which can prevent DC fault from affecting LVAC side. Both configurations will increase the cost as the additional AC/DC converter is required.

In the configuration illustrated in Fig. 5.1(c)(d), the LVDC network integration at LVDC link of SST. LVDC network is directly connected to LVDC link (Configuration (c)) or parallel connected to the LVDC link by an isolated DC/DC converter. In Configuration (c), the additional interface devices are not needed, which benefits the cost of the LVDC integration. However, the rated voltage of LVDC network is fixed as the same as LVDC link and there is no control strategy available in the configuration. Also, the protection scheme for the LVDC link need to be reorganized to a DC bus level. If a fault occurs in any device on the LVDC link, the LVDC voltage will drop and the operation of SST will

be affected. In Configuration (d), The use of an isolated DC/DC converter connected to the LVDC-link of the converter solves the problem of the fault isolation, selectable LVDC rated voltage in Configuration (c). and it provides independent control strategy for LVDC network, which can regulate either LVDC voltage or power flow between SST and LVDC network. However, the cost of the configuration will increase as a full isolated DC/DC converter is needed. Also, the location of the DC/DC converter may be different from SST, where communication between SST and DC/DC converter are needed for coordination.

In Fig. 5.1(e), the triple active bridge (TAB) is adopted to provide an individual LVDC port as the interface LVDC network. Compared with Configuration (a)-(d), TAB provides fault isolation and control strategy for the LVDC network without implementing a full DC/DC conversion stage. Also, the communication will not be needed as the added active bridge can be considered inside SST. Configuration (e) is then selected to investigate the integration of LVDC network in this chapter. Detailed research will be provided in the following section.

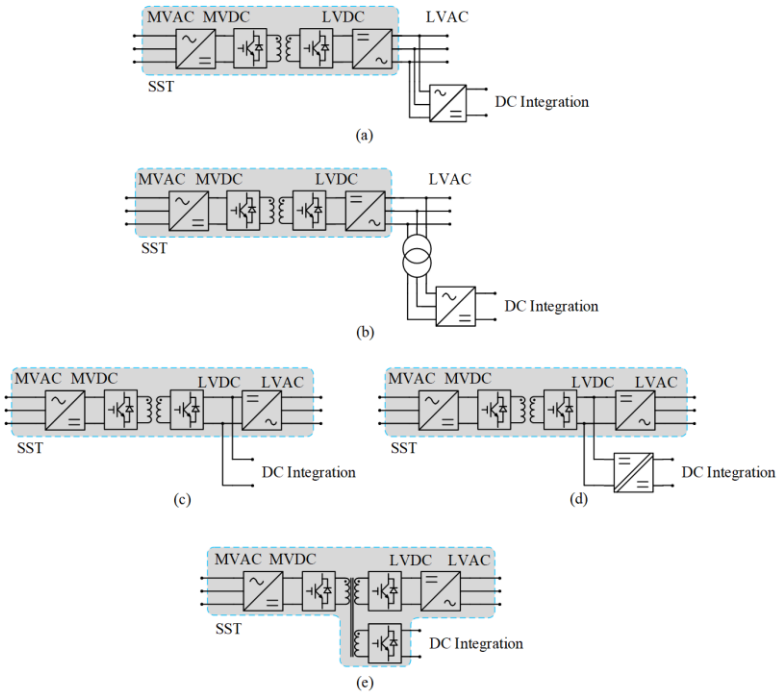


Fig. 5.1 Potential configurations of LVDC network integration for SST.

5.2 Coordinated control and operation of the proposed SST-based hybrid AC/DC distribution network

This section investigates the coordinated operation for the SST-based distribution network. Different operation modes of the hybrid distribution network are defined and studied. A coordinated droop control is developed for achieving self-adaptive power support from the LVDC network to the LVAC network via the integrated ESD. The integrated ESD adjust its power output according to connected LVDC voltage without communication. The LVDC network can operate as a power buffer to maintain the voltage and power under MVAC network outage and LVAC network load shedding.

5.2.1 System structure

Fig. 5.2 shows the layout of the proposed SST-based hybrid AC/DC distribution network. The SST consists of an MV AC/DC converter, a triple-active-bridge (TAB) DC/DC converter and LV DC/AC converter. In the study, the MVDC link is rated at 10 kV, while both the LVDC1 and the LVDC2 links are rated at 750 V. The simplified DC microgrid is connected in parallel with the integrated ESD (3 MW). As the proposed control is around MVDC voltage variation and the ESD control loop. The operation mode of LV DC/AC converter will not affect the performance of the proposed control. And LV DC/AC converter operates at the grid connected mode in this chapter.

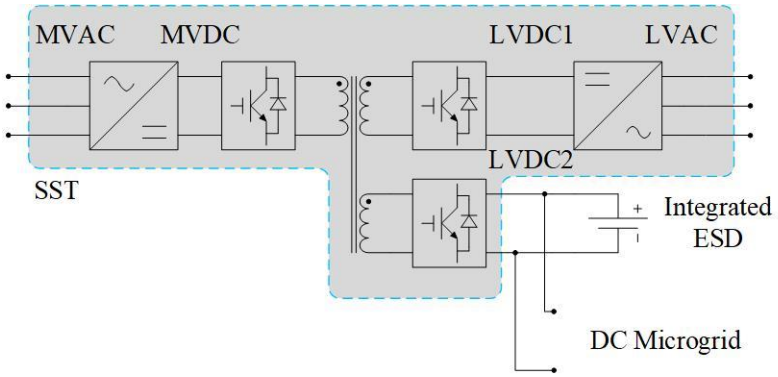


Fig. 5.2 Diagram of SST-based hybrid distribution network using TAB topology.

5.2.2 Control and operation principle of the SST-based AC/DC distribution network

Depending on the power flow direction in the distribution network, the system operation is classified as two operation modes,

- Grid feeding mode: The MVAC network transmits active and reactive power as the main power supplier to the LVAC. The ESD is either charged / discharged or in standby state.
- Grid outage feeding mode: A remote fault occurs at the MVAC network, and the ESD operates as the power balancing device to supply/absorb active power to the SST via the LVDC link.

To ensure adequate operation under different modes, a control scheme of the SST is proposed. The AC/DC rectifier regulated MVDC voltage, active and reactive power, as presented in Chapter 2. The TAB DC/DC converter regulates the LVDC grid voltage and LVDC 2 bus voltage with shared primary H-bridge on the MVDC side. The detailed TPS modulation control for optimised operation has been presented in Chapter 2. The DC/AC converter operates at grid-connected mode to regulate active and reactive power, as presented in Chapter 3.

The DC/DC converters connect the LVDC2 network with the ESD and DC microgrid can be based on any suitable converter configurations, considering the power rating and voltage conversion ratio. In this thesis, the use of DAB is assumed, and the phase shift ratio D_{esd} of the DAB converter can be controlled by regulating the difference between the actual power P and reference value P_{ref} via a PI controller, as show in Fig. 5.3.

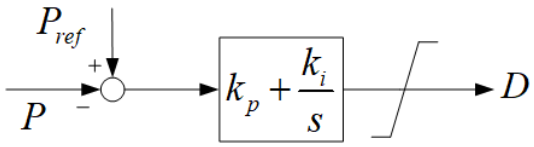


Fig. 5.3 Controller diagram of DAB DC/DC converter

5.2.3 Coordinated control of the SST-based AC/DC distribution network

In the existing control scheme, the MVDC voltage is regulated via the MV AC/DC converter during normal operation [138], so the total active power feeding to the SST, including active power from MVAC, and active power to LVAC and LVDC2 network are balanced. However, in case of MVAC network outage, the active power exchange between the MVAC and MVDC which is likely to be restricted due to the reduced MVAC voltage, may not be able to match those to the LVAC and LVDC2 networks. Consequently, MVDC voltages experience undervoltage or overvoltage conditions due to the unbalanced power flow. To ensure the reliable power supply to the LVAC network, and taking the advantage of ESD connected to the LVDC2 network of the SST, a coordinated active power control in which the integrated ESD can active supply power to feed the load at the LVAC network can be developed.

The main concept of the proposed coordination strategy is to modify the power (charging or discharging) order of the ESD when abnormal MVDC voltage is detected. Considering

positive ESD power referring to ESD being discharged, i.e., flowing from ESD to LVDC2 network, two cases can be envisaged, as:

- If MVDC under-voltage is detected, an additional ESD discharging order (positive P reference) is added to the initial ESD power order, and
- If MVDC over-voltage is detected, an additional ESD charging order (negative P reference) is added to the initial ESD power order.

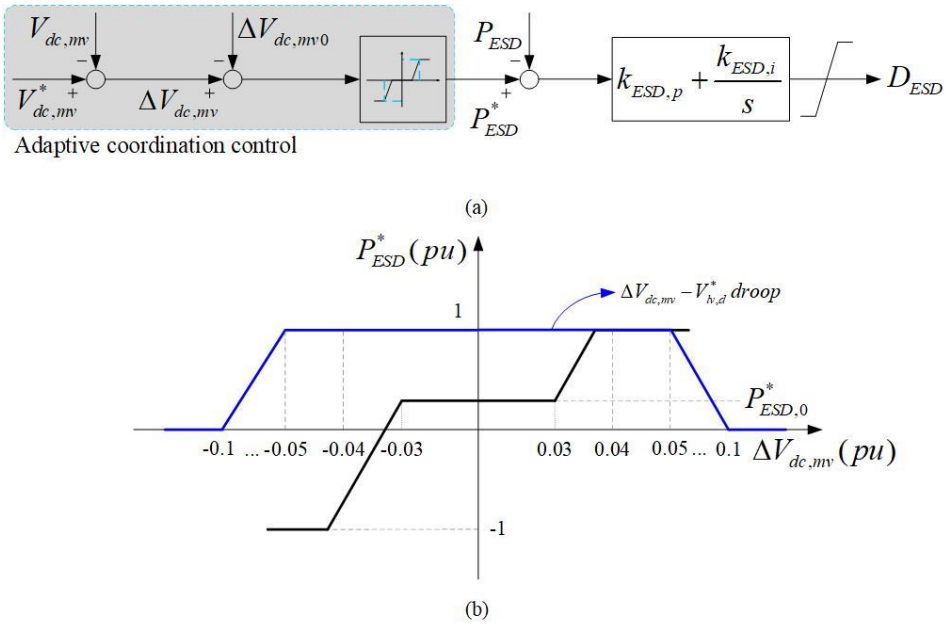


Fig. 5.4 Adaptive power control of the ESD DAB converter: (a) adaptive power control diagram; (b) adaptive power control curve.

This process is illustrated in Fig. 5.4(a). As seen, taking the positive MVDC voltage variation $\Delta V_{dc,mv}$ as an example, a linear relationship between the ESD power output reference $P_{ESD,ref}$ and $\Delta V_{dc,mv}$ is implemented as,

$$P_{ESD,ref} = P_{ESD,ref\,0} + k_{ESD,mvdc}(\Delta V_{dc,mv} - \Delta V_{dc,mv0}) \tag{5.1}$$

where $P_{ESD,ref\,0}$ is the set point of the power output of the ESD under normal operation and $P_{ESD,ref}$ is the coordinated power output of the ESD. $\Delta V_{dc,mv0}$ and $\Delta V_{dc,mv}$ are the normal operation value and actual value of the variation of the MVDC voltage. $\Delta V_{dc,mv0}$ is set to

4% so that the adaptive power control reacts faster than the $P_{sst,ref} - \Delta V_{dc,mv}$ droop. $k_{ESD,mvdc}$ defines the coordination capability of the integrated ESD, which is set at $1/0.01$ in this thesis.

Thus, under normal operation, the power output reference is set as $P_{ESD,ref\,0}$. When the MVDC voltage variation drops over its normal operation value $\Delta V_{dc,mv0}$, 3%, the coordinated control is activated and regulates the ESD discharging power to suppress the $\Delta V_{dc,mv}$. Similarly, when the MVDC voltage variation increases over 3% (excessive active power is fed from LVAC and LVDC2 networks to the SST), the coordinated control is activated and adds additional charging power to the ESD to balance the total active to the SST and suppress $\Delta V_{dc,mv}$.

Considering the power output limiting of the ESD, the $P_{ESD,ref} - \Delta V_{dc,mv}$ droop characteristics are shown in Fig. 5.4(b) and can be expressed as

$$P_{ESD,ref} = \begin{cases} P_{ESD,\max} & P_{ESD,ref} \geq 1 \\ P_{ESD,ref\,0} + k_{esd,mvdc}(\Delta V_{dc,mv} - \Delta V_{dc,mv0}) & \Delta V_{dc,mv} \geq \Delta V_{dc,mv0}, 0 \leq P_{ESD,ref} \leq 1 \\ P_{ESD,ref\,0} & -\Delta V_{dc,mv0} \leq \Delta V_{dc,mv} \leq \Delta V_{dc,mv0} \\ P_{ESD,ref\,0} + k_{esd,mvdc}(\Delta V_{dc,mv} + \Delta V_{dc,mv0}) & \Delta V_{dc,mv} \leq -\Delta V_{dc,mv0}, -1 \leq P_{ESD,ref} \leq 0 \\ -P_{ESD,\max} & P_{ESD,ref} \leq -1 \end{cases} \quad (5.2)$$

One consideration for the above proposed method is that the strategy of ESD requires the information of the MVDC voltage. In reality, the ESD and SST may not be located at the same place which can created practical issues. Ideally, the change of ESD power order should be based on the local DC voltage measurement, i.e., LVDC2 voltage. Once way to address this problem is to close resemble the LVDC2 network voltage according to the MVDC voltage, i.e., the LVDC2 voltage varies when the MVDC voltage changes, which can be derived as

$$V^{*}_{dc,lv2,new} = \frac{V_{dc,mv}}{V^{*}_{dc,mv}} V^{*}_{dc,lv2} \tag{5.3}$$

This can be implemented in the TAB control, with the new LVDC2 voltage reference set $V^{*}_{dc,lv2,new}$ according to the actual MVDC voltage. This also allows other devices connected to the LVDC2 network, e.g., PV generation to participate in the MVDC voltage regulation, in the event of ESD alone not able to bring back the MVDC voltage. For ESD, it monitors its own terminal DC voltage (i.e., the LVDC2 voltage), and when low LVDC2 voltage is detected, its power export to the LVDC network is increased (i.e., by modifying its power order).

5.2.4 Simulation results

In order to verify the operation of the SST-based hybrid AC/DC network under different mode, the test network shown in Fig. 5.2with the main parameters in Table 5.1, are simulated in MATLAB/Simulink. The LV side DC/AC converter of the SST operates under grid connected operation, and the control scheme has been detailed investigated in Chapter 4. The performance of the local ESD coordination during low and heavy load conditions as well as the remote ESD coordination are assessed during faults on the MVAC side.

Table 5.1 Parameters of the tested SST-based hybrid AC/DC network

Component	Parameter	Value
SST converter	SST Power rating	10 MW
	MVAC voltage rating	11 kV
	MVDC voltage rating	10 kV
	LVDC1 and 2 voltage rating	750 V
	LVAC voltage rating	415 V
ESD	ESD Power rating	3 MW
	Control parameters $k_{esd,p}$ $k_{esd,i}$	0.15 mΩ; 0.2 Ω/s;

(a) ESD is sufficient for supplying LVAC load

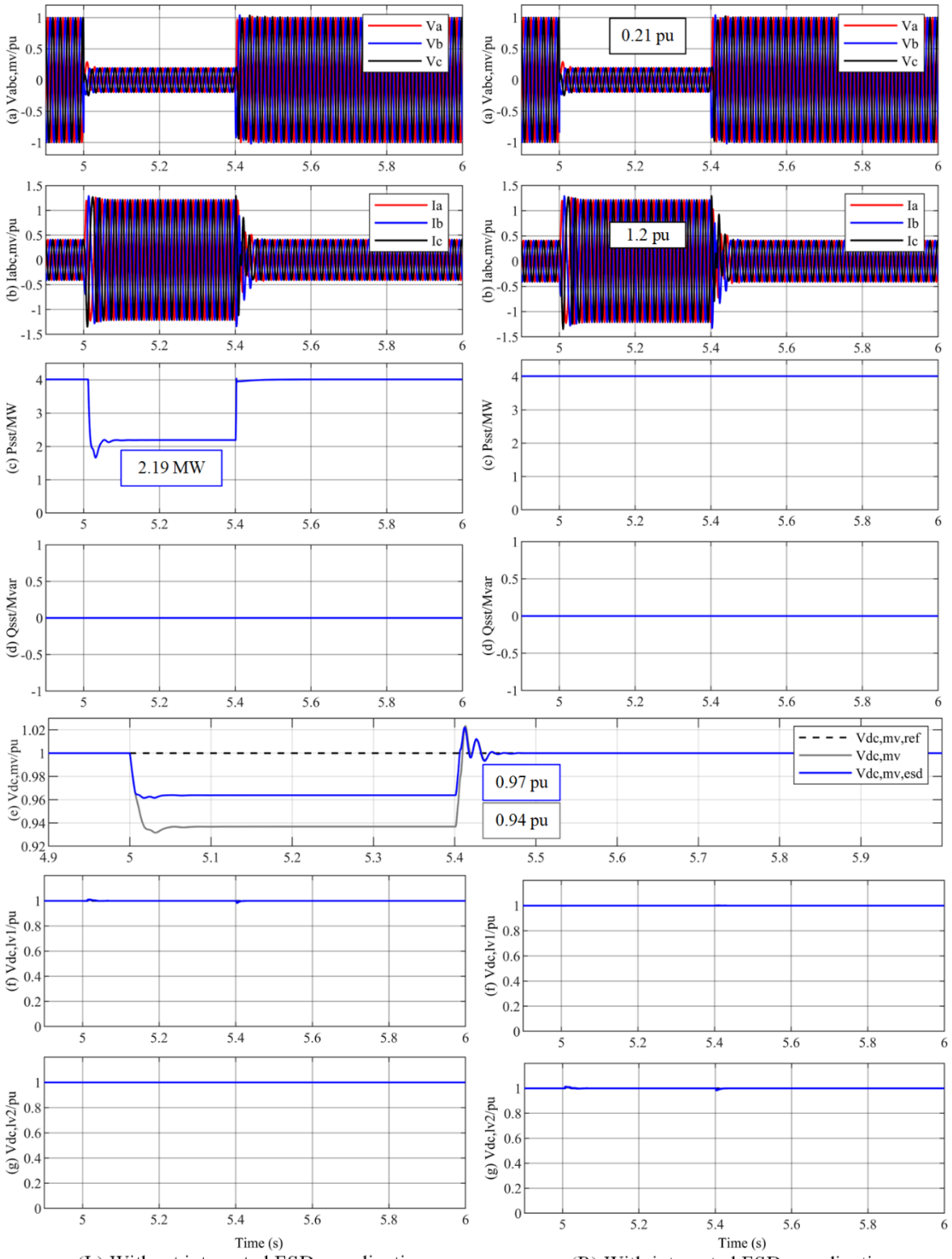
In the first simulation, the performance of the system during low load condition is assessed. The rated power of LVAC load is 4 MW and the locally integrated ESD on the DC network is sufficient to supply the deficit power during the MVAC fault. The simulation results are illustrated in Fig. 5.5.

Prior to 5 s, the LVAC side converter is under grid-forming operation. The CNOP is open and 4 MW active power is dispatched from the MVAC network to the LVAC Load. The ESD is fully charged so its power is zero. The SST operates at normal operation and the voltages and currents are well controlled.

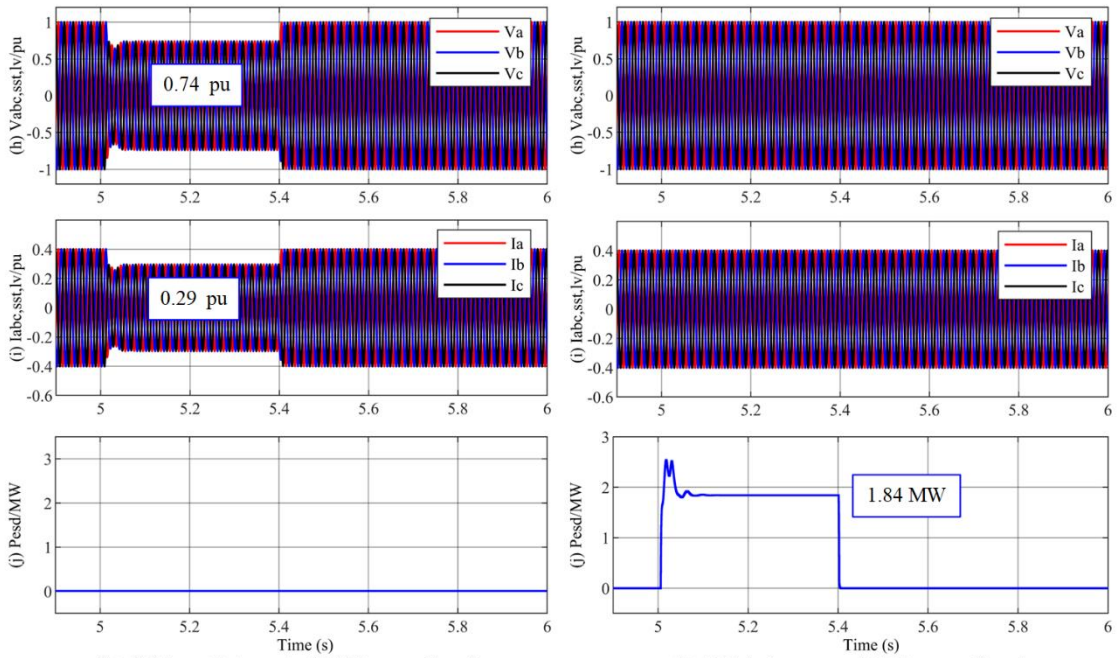
During the fault, it can be observed in Fig. 5.5L(a) that the phase voltage at the MV grid drops to 0.21 pu for a duration of 400 ms. The current reaches the limit of 1.21 pu at MVAC side, illustrated in Fig. 5.5L(b). Consequently, the MV grid can only provide 2.19 MW to the load side, which leads to the MVDC voltage drop. As illustrated as the grey line in Fig. 5.5(e), the MVDC voltage remains at 0.94 pu as the active power limiting control at the DC/AC converter of SST is activated, illustrated in Fig. 5.5L(h)(i). LVAC network voltage drops to 0.74 pu accordingly, which decreases the power required at LVAC side (as the LVAC load is resistance type). The power thus rebalances. Small

fluctuations occur on LVDC1 and LVDC2 link, illustrated in Fig. 5.5L(f)(g). In reality, the voltage sag can cause the disconnection of sensitive loads.

With ESD coordination control, the SST MV side converter also goes into current limiting operation after fault occurs, which is similar with that without the proposed control, illustrated in Fig. 5.5R(a)(b). The MVDC voltage dip is detected by the ESD coordination control so the power output of ESD is increased to 1.84 MW to provide the deficit power, illustrated in Fig. 5.5R(j). The power thus rebalances and SST transmits 4 MW to the LVAC network. The MVDC voltage remains at 0.97 pu, shown as the blue line in Fig. 5.5R(e). Only small fluctuations occur on LVDC1 and LVDC2 link, illustrated in Fig. 5.5R(f)(g). The voltage at the LVAC network remains at the rated value, illustrated in Fig. 5.5R(h)(i). After the fault is cleared, the MV grid recovers and the MVDC voltage recovers to track the reference. The active power output of the SST and ESD also recover to normal operation, shown in Fig. 5.5R(a)-(j).



(L) Without integrated ESD coordination (R) With integrated ESD coordination



(L) Without integrated ESD coordination (R) With integrated ESD coordination

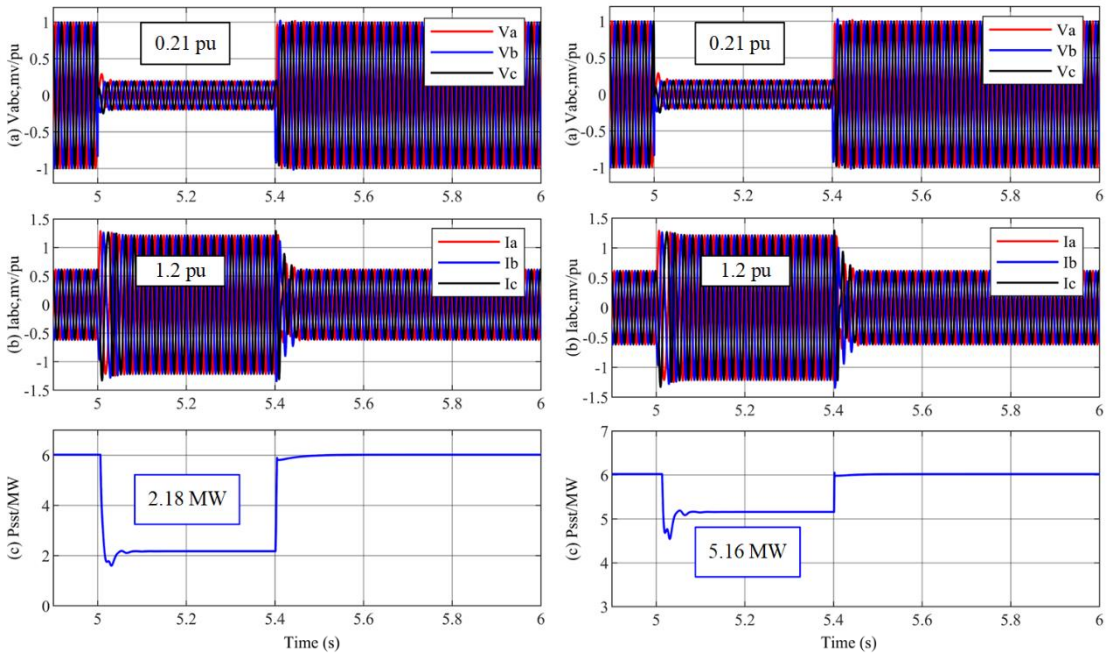
Fig. 5.5 Performance of system under light load condition without ESD integration coordination (left) and with local ESD integration coordination (right): (a) SST MV side voltage; (b) SST MV side current; (c) SST active power output; (d) SST reactive power output; (e) SST MVDC voltage; (f) SST LVDC1 voltage; (g) SST LVDC2 voltage; (h) SST LV side voltage (3ph); (i) SST LV side current (3ph); (j) ESD active power output.

(b) ESD is insufficient for supplying LVAC load

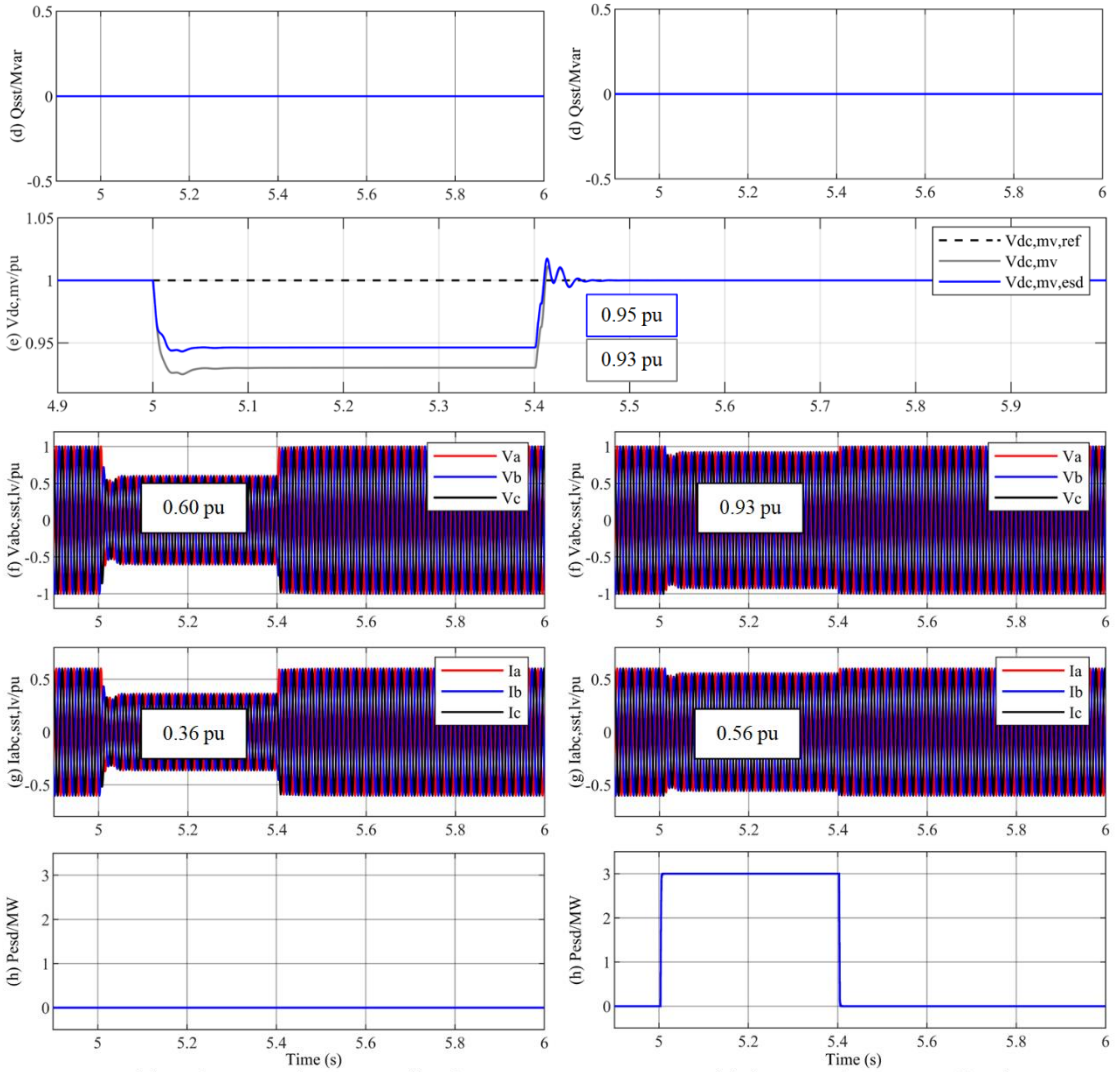
In the second simulation, the performance of the system during heavy load condition is assessed. The rated power of LVAC load is 6 MW and consequently, the integrated ESD is not sufficient to supply the deficit power during the fault. the simulation results are illustrated in Fig. 5.6.

During the fault, it can be observed in Fig. 5.6L(a) that the phase voltage at the MV grid drops to 0.21 pu for a duration of 400 ms due to the fault. The current reaches the limit of 1.21 pu at the MVAC side, illustrated in Fig. 5.6L(b). Thus, the MV grid can only provide 2.24 MW to the load side, which leads to the MVDC voltage drop. As illustrated as the grey line in Fig. 5.6(e), the MVDC voltage remains at 0.93 pu as the active power limiting

control at the DC/AC converter of SST is activated, illustrated in Fig. 5.6L(f)(g). LVAC network voltage drops to 0.60 pu accordingly, which decreases the power required at LVAC side and thus the power rebalances. With ESD coordination control, the SST MV side converter also goes into current limiting operation after fault occurs, similar to that without the proposed control, as illustrated in Fig. 5.6R(a)(b). The MVDC voltage drop is detected by the ESD coordination control so its power output increases to 3 MW to provide the deficit power, as illustrated in Fig. 5.6R(h). As the ESD cannot provide sufficient power for LVAC network, the active power limiting control at the DC/AC converter of SST is still activated, as shown in Fig. 5.6R(f)(g). Thus, the LVAC network voltage drops to 0.93 pu accordingly, which decreases the power required at LVAC side. The power thus rebalances and the total power transmitted to the LVAC side through the SST is 5.16 MW. The MVDC voltage remains at 0.95 pu, shown as the blue line in Fig. 5.6 (e). After the fault is cleared, the system recovers as shown in Fig. 5.6R(a)-(h).



(L) Without integrated ESD coordination (R) With integrated ESD coordination



(L) Without integrated ESD coordination (R) With integrated ESD coordination

Fig. 5.6 Performance of system under heavy load condition without ESD integration coordination (left) and with local ESD integration coordination (right): (a) SST MV side voltage; (b) SST MV side current; (c) SST active power output; (d) SST reactive power output; (e) SST MVDC voltage; (f) SST LV side voltage; (g) SST LV side current; (h) ESD active power output.

(c) SST and ESD at different locations

The last simulation investigates the performance of the system with the proposed method when the ESD is located different place with SST. In this case, the ESD has no access to the MVDC voltage information. Thus, in order to inform the ESD about the power

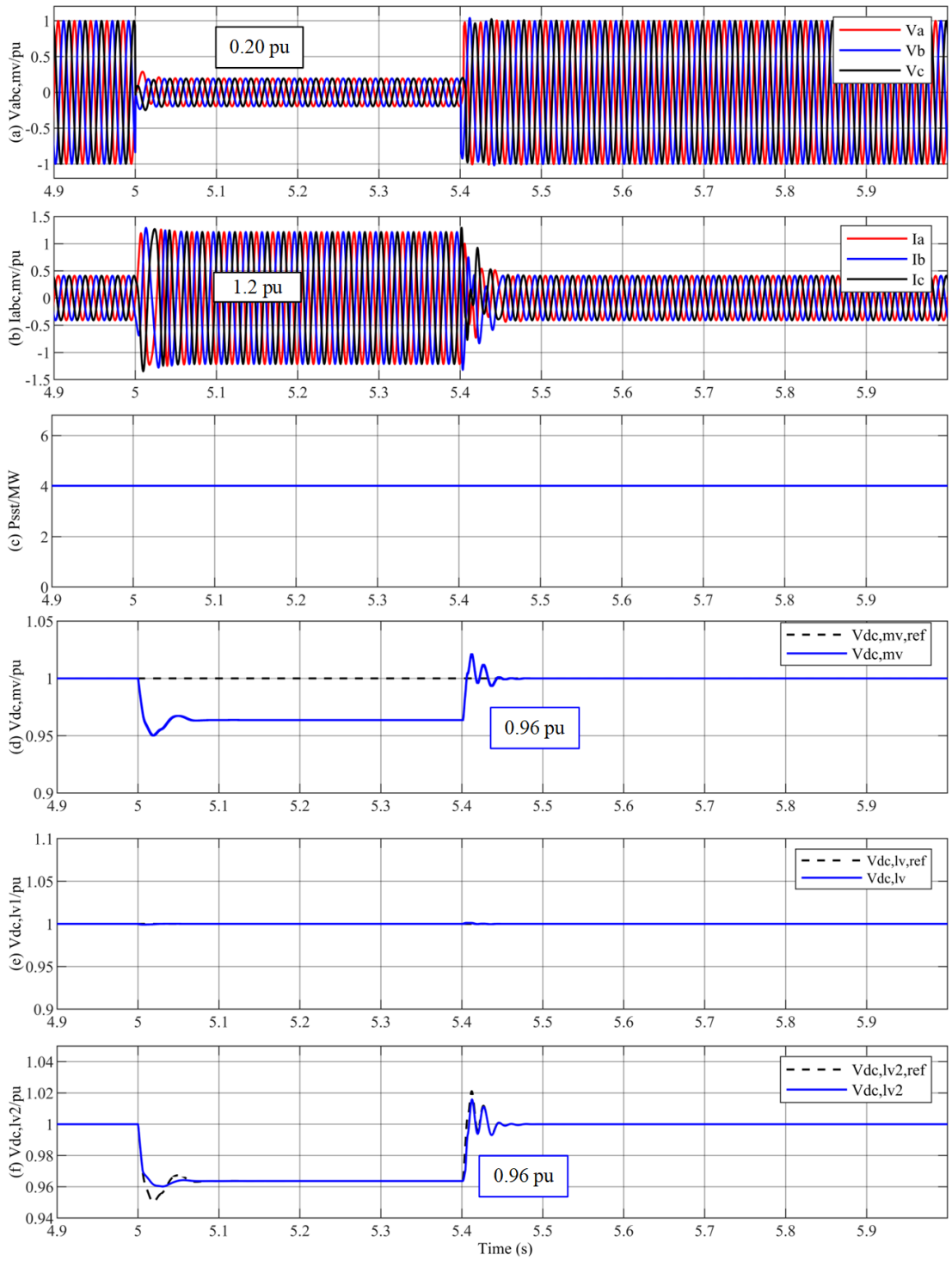
imbalance on the MVAC and LVAC sides, LVDC2 link voltage is modified according to MVDC variation as derived as (5.4). The $P_{ESD,ref} - \Delta V_{dc,mv}$ droop characteristics is then also modified to $P_{ESD,ref} - \Delta V_{dc,lv2}$ droop as:

$$P_{ESD,ref} = \begin{cases} P_{ESD,\max} & P_{ESD,ref} \geq 1 \\ P_{ESD,ref\,0} + k_{esd,mvdc}(\Delta V_{dc,lv2} - \Delta V_{dc,lv2,0}) & \Delta V_{dc,lv2} \geq \Delta V_{dc,lv2,0}, 0 \leq P_{ESD,ref} \leq 1 \\ P_{ESD,ref\,0} & -\Delta V_{dc,lv2,0} \leq \Delta V_{dc,lv2} \leq \Delta V_{dc,lv2,0} \\ P_{ESD,ref\,0} + k_{esd,mvdc}(\Delta V_{dc,lv2} + \Delta V_{dc,lv2,0}) & \Delta V_{dc,lv2} \leq -\Delta V_{dc,lv2,0}, -1 \leq P_{ESD,ref} \leq 0 \\ -P_{ESD,\max} & P_{ESD,ref} \leq -1 \end{cases} \quad (5.4)$$

where $\Delta V_{dc,lv2,0}$ and $\Delta V_{dc,lv2}$ are the normal operation and actual values of the variation of the LVDC2 voltage. And the characteristics of the coordinated control illustrated in Fig. 5.4(b) can be modified accordingly.

For the simulation results illustrated in Fig. 5.7, the rated power of LVAC load is 4 MW so the ESD is sufficient to supply the deficit power during the fault.

Prior to 5 s, the SST operates at the normal operation and it is similar to that in case (a). After the fault occurs, the phase voltage and current at the MV grid behave similar to those in case (a), as illustrated in Fig. 5.7(a)(b). The MVDC voltage drops due to the power unbalance and consequently, LVDC2 voltage is reduced accordingly, as shown in Fig. 5.7(d)(f). The LVDC2 voltage dip is detected by the ESD coordination control and its power output is increased to 1.91 MW, as seen in Fig. 5.7(i). Thus, the power in SST is rebalanced, while the MVDC and LVDC2 voltages remain at 0.96 pu. The LVAC voltage remains at the rated value and SST transmits a total of 4 MW to the LVAC network, as illustrated in Fig. 5.7(g)(h). Only small fluctuation is observed at LVDC1 voltage in Fig. 5.7(e). After the fault is cleared, the MV grid recovers and the whole system goes back to normal operation, as can be seen in Fig. 5.7(a)-(i).


(a) Vabc,mv/pu
0.20 pu
Va
Vb
Vc
(b) Iabc,mv/pu
1.2 pu
Ia
Ib
Ic
(c) Psst/MW
(d) Vdc,mv/pu
Vdc,mv,ref
Vdc,mv
0.96 pu
(e) Vdc,lv1/pu
Vdc,lv,ref
Vdc,lv
(f) Vdc,lv2/pu
Vdc,lv2,ref
Vdc,lv2
0.96 pu
Time (s)

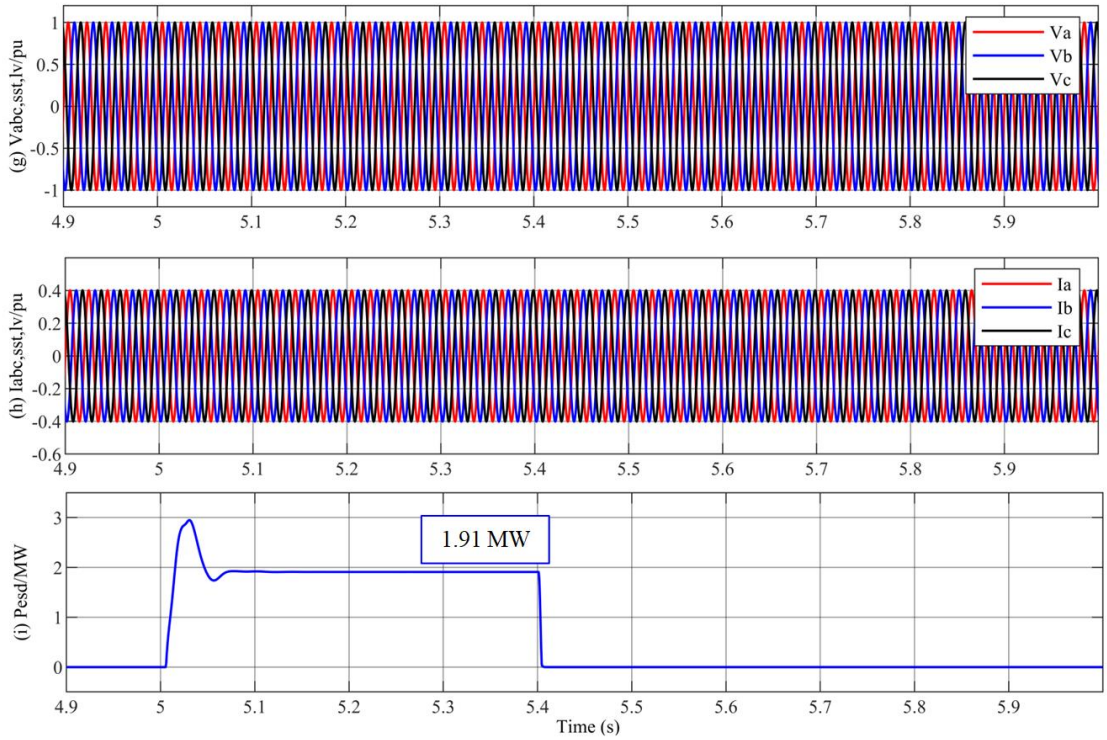


Fig. 5.7 Performance of system with remote ESD integration coordination: (a) SST MV side voltage (3ph); (b) SST MV side current (3ph); (c) SST active power output; (d) SST MVDC voltage; (e) SST LVDC1 link voltage; (f) SST LVDC2 link voltage; (g) SST LV side voltage (3ph); (h) SST LV side current (3ph); (i) ESD active power output.

5.3 Impact of DC fault on SST-based distribution network

The impact of faults on the LVDC network of the SST is investigated in this section. DC fault characteristics are assessed and a DC fault protection scheme for the proposed SST is studied.

5.3.1 DC fault characteristics and the impact on the hybrid AC/DC distribution network

In the considered SST configuration, as illustrated in Fig. 5.2, the TAB converters establish the connection from the MVDC to the LVDC2 network which can connect to the ESD and other DC load/generation etc. Thus, it is necessary to investigate the DC fault characteristic of the TAB converter in the event of faults on the LVDC2 network. In this section, a typical pole-to-pole fault is assessed.

For TAB converters, the behaviour is dependent on the operating and protection of the three active bridges (AB1-3) as shown in Fig. 5.8. Wherein, MVDC, LVDC1 and LVDC2 are the 3 DC terminals. $i_{dc,mv}$, $i_{dc,lv1}$ and $i_{dc,lv2}$ are the respective DC currents. v_{AB1} is the voltage output of AB1, while v_{AB2} and v_{AB3} are the voltage inputs of AB2 and AB3, respectively. At AB1, i_{AB1} and v_{pri} are the AB1 output current and the primary side voltage of the three-winding MFT. At AB3, i_{cd} is the current flow through C_{dc2}. i_{diode} presents the current through diodes at AB3 during fault condition while i_{ac} represents the arm current.

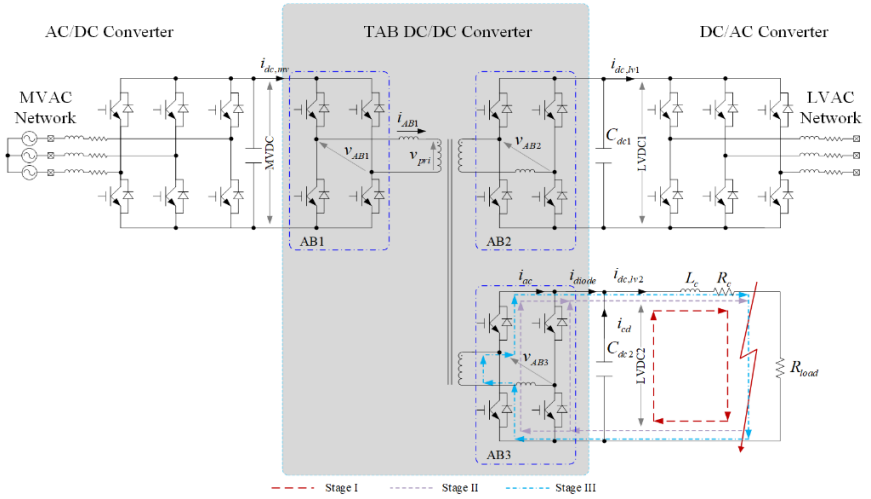


Fig. 5.8 Paths of the fault currents feeding by the SST.

Similar to DC fault analysis of grid connected two-level converters [166, 167], the fault transient can be analysed and progressed in three stages according to the fault current contribution. The corresponding fault current paths in the event of a fault at the LVDC2 network are illustrated in Fig. 5.8. As described, different to conventional grid connected two-level converters, the AC fault current contribution during LVDC2 fault in a TAB can be blocked by turning off the MV side active bridge AB1. Fig. 5.9 illustrates a common approach, whereas blocking will be activated when either the DC current i_{dc} exceeds the overcurrent threshold i_{oc} or the DC voltage v_{dc} falls below the threshold value u_{uv}. Depending on the converter design, the typical overcurrent blocking threshold is around 2 pu, while the undervoltage blocking threshold is normally 0.7-0.8 pu. Once the blocking signal is activated, all the switching devices will be turned off and the corresponding DCCB is disconnected. The analysis here considers the connected DC network as load only, for simplicity. L_c and R_c are the LVDC cable impedance.

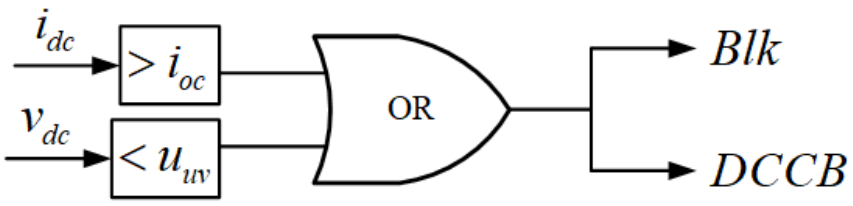


Fig. 5.9 Commonly used converter blocking logic.

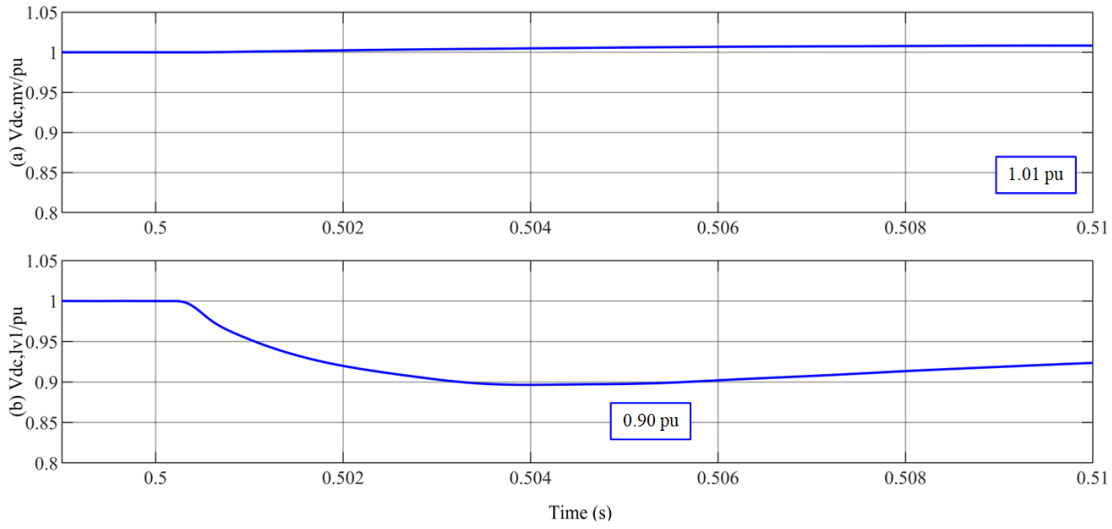
The three different stages of fault current contribution are:

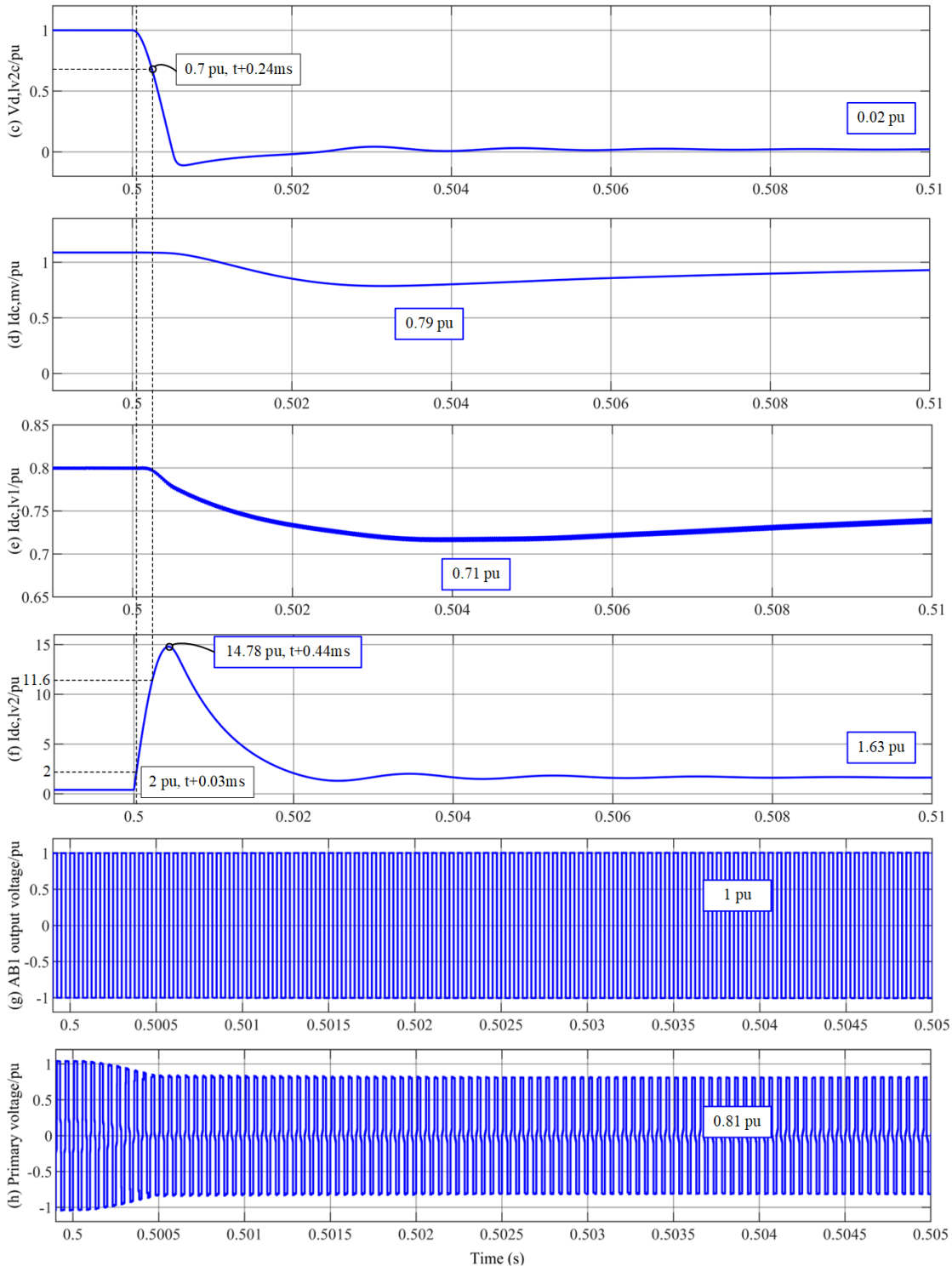
- Stage I: Capacitor discharge. After the occurrence of a pole-to-pole fault at the LVDC side, the discharge of the DC link capacitor C_{dc2} dominates the fault current, shown as the RED dashed line in Fig. 5.8. After the capacitor voltage drops to zero, Stage I completes.
- Stage II: Diode free-wheeling. With the capacitor discharging, the inductance components (such as cable inductance, and any DC inductance that may have) in the

fault current path store a portion of the flowed energy. The stored energy is then released after Stage I through the fault current path provided by the antiparallel diodes (assuming AB3 is blocked immediately after fault detection), shown as the grey dashed line in Fig. 5.8. The diodes experience the highest overcurrent level and it is considered as the most destructive stage for converters [168].

- Stage III: AC fault feeding. The fault current is fed by the MVDC side through the AB1 and AB3 (blocked), though as previously described this stage will be different if AB1 is blocked.

To analyse the fault characteristics of the proposed network under the DC fault condition, simulations are conducted. A solid DC pole-to-pole fault occurs at 0.5 s as shown in Fig. 5.10, while the system parameters of AB1 and AB2 are the same as in Section 5.2, with the rated power of AB3 setting as 5 MW. The u_{uv} and i_{ov} in the blocking logic is set at 0.7 pu and 1.2 pu, respectively. The power needed from LVAC network is 8 MW while R_{load} on LVDC 2 is 2 MW. A 200 m LVDC cable ($R_c = 32.8 m\Omega / km$, $L_c = 0.048 mH / km$) is used to connect the LVDC2 terminal of the SST with the rest of the DC network. The converter blocking at AB3 is applied, while AB1 and AB2 are not blocked in this subsection. DCCB operation will be further considered in Subsection 5.3.3.




(c) Vd,Iv2c/pu
0.7 pu, t+0.24ms
0.02 pu
(d) Idc,mv/pu
0.79 pu
(e) Idc,Iv1/pu
0.71 pu
(f) Idc,Iv2/pu
14.78 pu, t+0.44ms
2 pu, t+0.03ms
1.63 pu
(g) AB1 output voltage/pu
1 pu
(h) Primary voltage/pu
0.81 pu
Time (s)

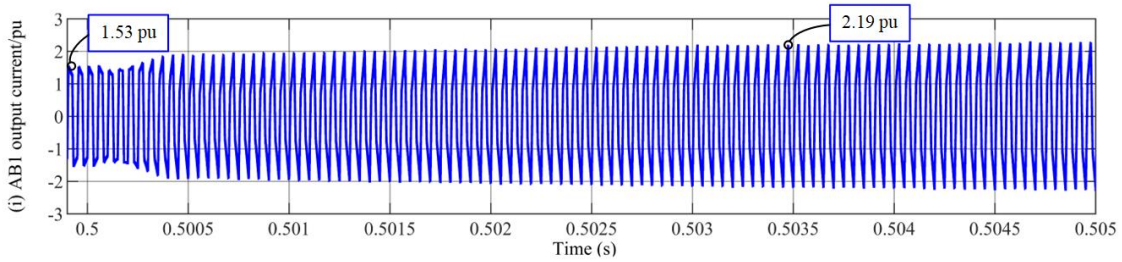


Fig. 5.10 Voltage and current profiles under a DC short circuit, (a) MVDC voltage; (b) LVDC1 voltage; (c) LVDC2 voltage; (d) MVDC input current; (e) LVDC1 current after filter; (f) LVDC2 current after filter; (g) AB1 output voltage; (h) three-winding MFT primary side voltage; (i) AB1 output current.

When simulation starts, TAB supplies 8 MW to LVAC network and 2 MW to LVDC2 link. After the DC fault initiation at $t = 0.5s$, LVDC2 current reaches 2 pu (based on AB3 rated power 5 MW) at $t + 0.03ms$ while LVDC2 voltage drop below 0.7 pu at $t + 0.24ms$, as illustrated in Fig. 5.10(c). AB3 is thus blocked at $t + 0.03ms$. The fault current continues increasing as current can contribute to fault through capacitor discharging, as illustrated in Fig. 5.10(f).

Meanwhile, Due to the increasing transient current from AB1, illustrated in Fig. 5.10(i), voltage upon L_{DAB} becomes larger and the primary side voltage at MFT decreases from 1 pu to 0.81 pu accordingly, illustrated in Fig. 5.10(h). The secondary side voltage v_{ab2} decreases, and consequently LVDC1 link voltage decrease to 0.9 pu, illustrated in Fig. 5.10(b). It is noted here that the LVDC1 current decreases to 0.71 pu according to LVDC1 voltage since DC/AC converter in Fig. 5.10 is simplified as an equivalent load in the simulation.

The total fault current reaches to the peak value 14.78 pu at $t + 0.44ms$, illustrated in Fig. 5.10(f), after the discharge of the capacitor C_{dc2}. The DC fault current gradually comes down and remains at 1.63 pu which is contributed through the freewheeling diodes in AB3. It needs to be noted that the simulation here shows the condition that the AB3 is blocked

without any protective arrangement. For example, the fault current contribution from the TAB could be cut off by blocking AB1 through power supply to LVDC1 and LVAC will cease. Also, if there is an additional DC source connected with LVDC2 side or AC source connected with LVAC network, the additional sources will also contribute to fault current at LVDC2.

From the view of system operation, blocking the whole TAB can isolate DC fault from MVAC and LVAC network, but the normal power transmission of SST to LVAC network will be seriously affected. In order to maintain the reliable power supply to LVAC network while achieving DC fault isolation capability, the requirement for DC protection needs to be studied in the following section.

5.3.2 DC fault clearance requirement of the proposed SST

Apart from converter blocking for protecting switching devices in TAB, fast fault clearance is also needed. As no additional DC network is connected with MVDC and LVDC1 in the proposed SST topology, the protection of MVDC and LVDC1 links will not be considered. Fig. 5.11 illustrates the position for implementing the DCCB for protecting the SST from DC fault occurred at either integrated ESD or DC network. For LVDC2 link, fast fault clearance can not only isolate the fault before the severe transient develops in the network, but also ensure the healthy part of SST remains under normal operation during the DC fault.

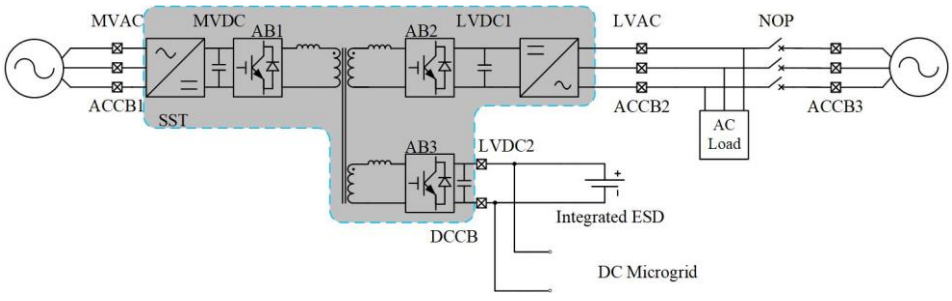


Fig. 5.11 Position for implementing relays and CBs in the SST-interfaced DC network.

DC protection in MV and LV network can be achieved using fuses, Mechanical CBs (MCBs), Solid-State CBs (SSCBs), Hybrid CBs (HCBs). Reference [169] provides a detailed review of the different DC protections mentioned above. For SST application, fuses are the simplest and the most inexpensive choice, and it is applicable especially for integrated ESD when cost and tripping time are considered. But it is not suitable for protecting DC links. The one-off attribute of fuse means that replacement will be needed after operation and it cannot discriminate between a transient and a permanent fault. MCBs are not applicable for DC links due to its slow fault clearance time (30-100 ms).

The SSCBs is the preferred choice for SST due to its fast fault clearance (tens of microseconds level) [169] which ensures the SST to remain normal operation when a DC fault occurs at the DC network connected with the TAB. The disadvantages of SSCBs are mainly high power losses and cost and large (due to the need for heat sinks) [169]. Meanwhile, The HCBs can be the cost-effective option. It combines mechanical switch and semiconductor device in parallel to achieve fast fault clearance with low power loss, which can also be applicable to SST. However, as the operation time of HCBs can be several milliseconds [170, 171], it is uncertain that the fault can be cleared effectively before affecting the healthy part of the TAB. Thus, it is important to investigate the requirement for converter blocking and consequent power outage under HCBs implementation.

5.3.3 Effectiveness of different protection device on SST under DC fault

The simulation here evaluates the effectiveness of different protection schemes on SST under DC fault shown in Subsection 5.3.1. The maximum operating current value is set as 2 pu while undervoltage protection threshold is set as 0.7 pu. A 200 ms pole-to-pole fault is applied at Load 2 at $t = 0.5s$. Four protection schemes are considered here and compared as follows:

- LVDC2 BLKD: After DC fault occurs, TAB detects the fault and blocks the faulty port (LVDC2 link in this case). The healthy port will remain normal operation. The simulation of this case study has been shown in Fig. 5.11, while additional observation will be provided.
- TAB BLKD: After DC fault occurs, TAB detects the fault and blocks all the ports of TAB.
- SSCB: A fast SSCB is applied to disconnect the faulty part connected with TAB. The operation time of the SSCB used here is set as 120 μs.
- SLOW DCCB: slow operation DCCB, i.e., HCBs are used for isolating the faulty port.

For LVDC2 BLKD case study, the enlarged transient current profile in AB3 is illustrated in Fig. 5.12. Wherein, arm current, current through diode and LVDC2 output current are assessed, and the location of them are illustrated in Fig. 5.8. As seen, the DC overcurrent activates converter blocking at $t+0.03ms$, illustrated in Fig. 5.12(c). However, the arm current in AB3 only reaches 2pu at $t+0.27ms$. From view of protecting switching devices, AB1 can be blocked only after the arm current is over 2pu. Thus, fault clearance device and converter blocking can be activated at different times.

Thus, converter blocking and DCCB operation signals are modified in Fig. 5.13. As seen, converter blocking will be activated when either AB3 arm current i_{ac} exceeds the overcurrent threshold i_{oc} or AB3 DC voltage is less than the undervoltage threshold u_{uv}, while the operation logic of DCCB will remain the same by considering the DC current and DC voltage. The i_{oc} is set as 2 pu while u_{uv} is set as 0.7 pu. The corresponding simulation results will be shown in SLOW DCCB case study.

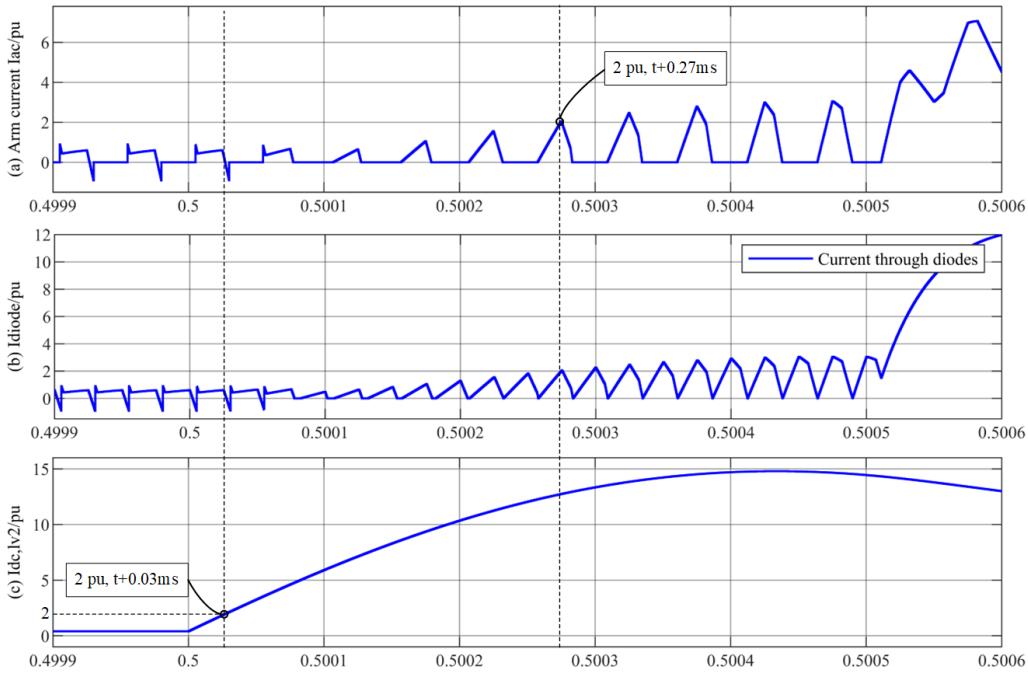


Fig. 5.12 Enlarged current profile for LVDC2 BLKD case study: (a) arm current in AB3; (b) fault current through diodes; (c) DC output current at AB3.

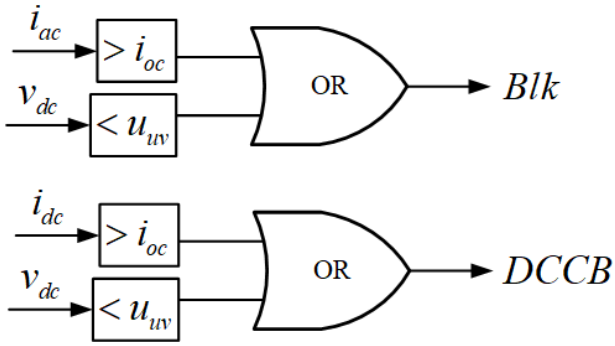
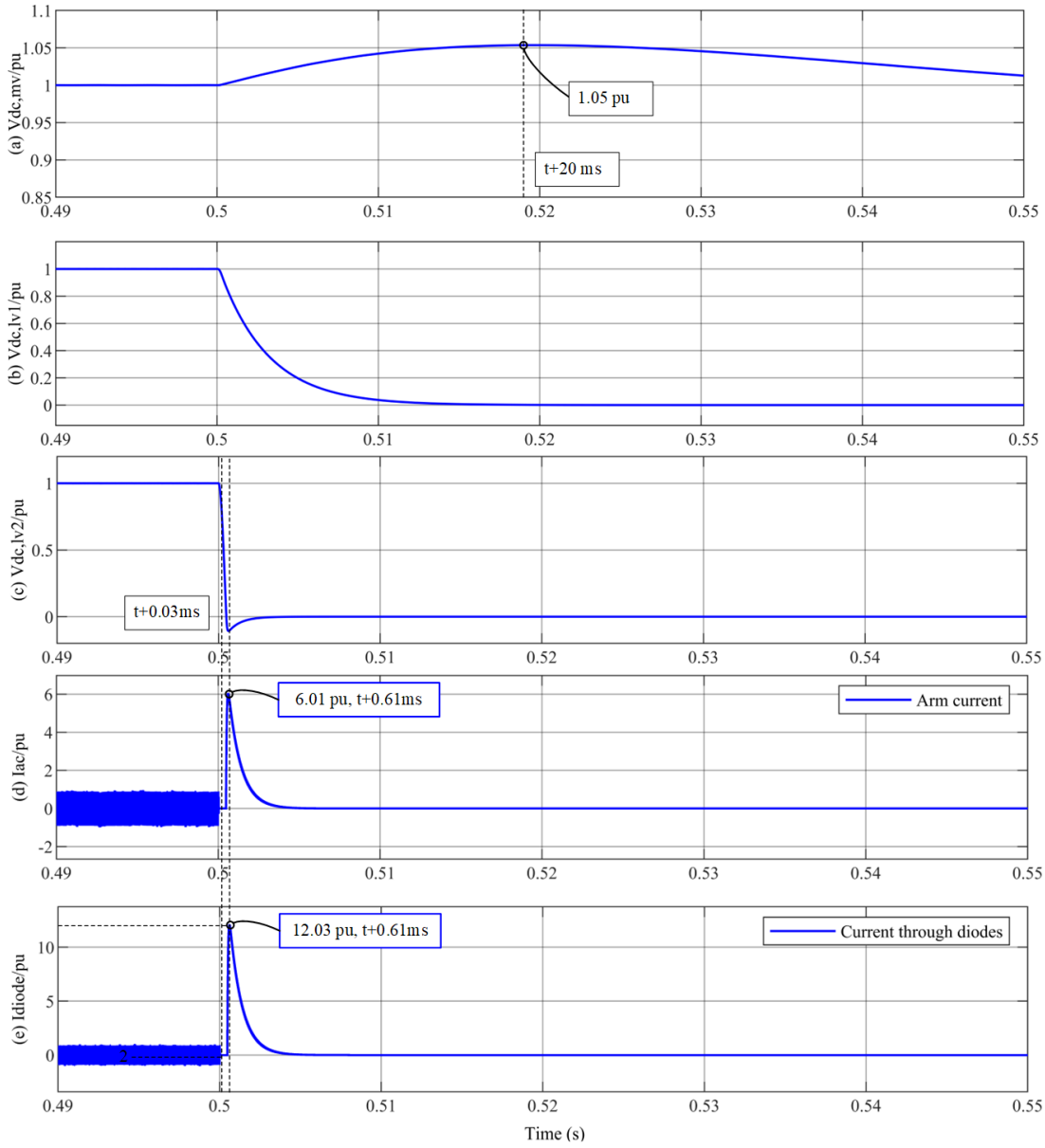


Fig. 5.13 Modified converter blocking and fault detection for TAB.

In TAB BLKD case study, as illustrated in Fig. 5.14(a)-(f), the TAB is blocked at $t+0.03ms$ so neither the MVAC network nor the LVAC network contribute fault current to LVDC2. A 5% fluctuation occurs on MVDC voltage after the DC fault due to the transient power unbalance and it tracks back to the rated value by the MV side AC/DC converter control. The capacitor is discharged on LVDC1 link to the DC/AC converter

and LVDC1 link voltage drops to zero due to the power unbalance at LVDC1 link, illustrated in Fig. 5.14(b). LVDC2 link voltage drops to zero due to the power unbalance and becomes negative value at around $t+1.48ms$ due to the reverse current flow through diode and capacitor, illustrated in Fig. 5.14(c)-(e). With TAB BLKD scheme, the blocked TAB isolates the fault while disables SST can cause the power outage of the LVAC network.



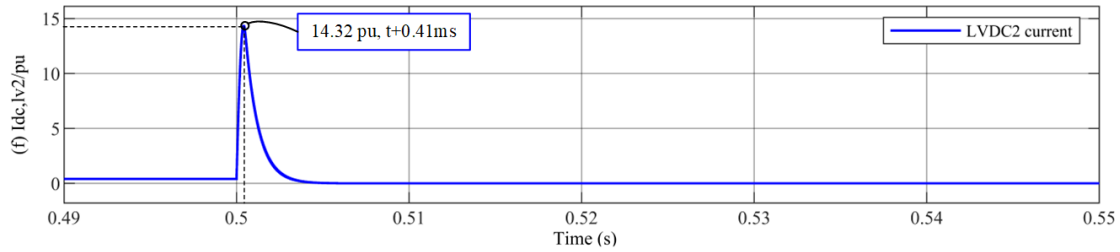


Fig. 5.14 Performance of SST with TAB BLKD case study under the DC fault: (a) MVDC voltage; (b) LVDC1 link voltage; (c) LVDC2 link voltage; (d) arm current in AB3; (e) fault current through diode; (f) DC output current at AB3.

In the SSCB case study, as illustrated in Fig. 5.15(a)-(f), after fault occurs, the SSCB operation signal is activated at $t+0.03ms$ as LVDC2 current goes over the threshold, illustrated in Fig. 5.15(f). It takes 120 μs to open the SSCB, and the maximum LVDC2 current decreases to 8.18 pu and drops to zero after SSCB opening, illustrated in Fig. 5.15(f). LVDC2 voltage then recovers from 0.87 pu to 1.05 pu as SSCB disconnects the faulty part, illustrated in Fig. 5.15(c). Due to the fast action of the SSCB, the arm current at AB3 is less than 2 pu (0.90 pu) while LVDC2 voltage remains 0.99 pu, as illustrated in Fig. 5.15(c)(d). Converter blocking at AB3 is thus not activated. Also, there is only small fluctuation at MVDC and LVDC1 link, illustrated in Fig. 5.15(a)(b). It is noted here that the detailed operation of the SSCB is not considered. The main benefit of the SSCB case shows that the healthy part of TAB can remain normal operation without activating converter blocking.

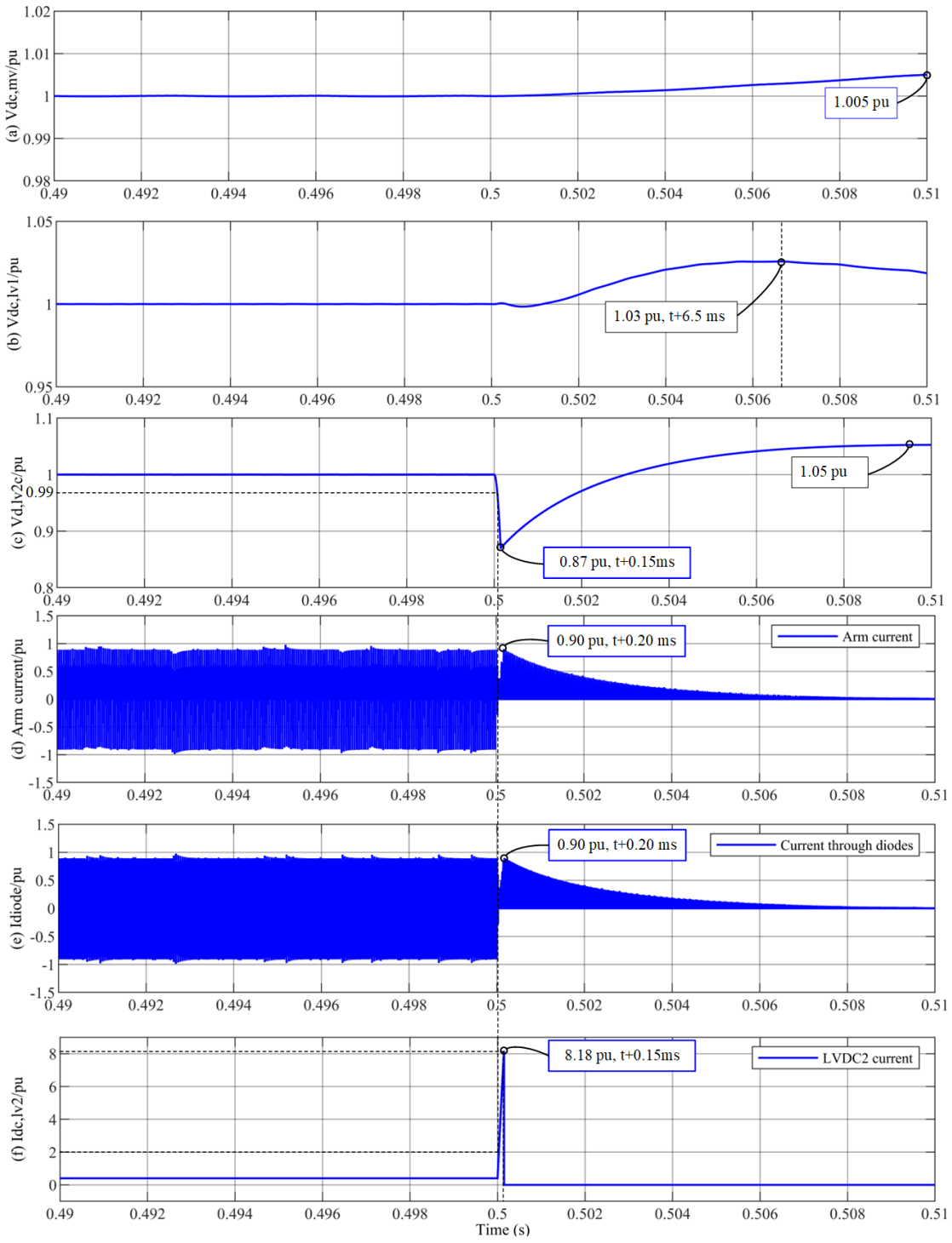


Fig. 5.15 Performance of SST with SSCB case study under the DC fault: (a) MVDC voltage; (b) LVDC1 link voltage; (c) LVDC2 link voltage; (d) arm current in AB3; (e) fault current through diode; (f) DC output current at AB3.

In the SLOW DCCB case study, the DCCB operation signal is activated at $t+0.03ms$ as LVDC2 current precedes LVDC2 voltage reaching the threshold, illustrated as Fig. 5.16 (c)(f). As the DCCB operation time is set as 1 ms in the case study. The fault remains connected with TAB before $t+1.03ms$. LVDC2 voltage drops below 0.7 pu after $t+0.24ms$ while the arm current at AB3 is over 2 pu after $t+0.27ms$. Thus, AB3 converter blocking is activated at $t+0.24ms$, illustrated in Fig. 5.16(c)(d). The DC fault current reaches the maximum value of 14.78 pu at $t+0.44ms$. Similar with LVDC2 BLK case, LVDC1 voltage drops to 0.89 pu due to voltage drops at the MFT terminal. When the DCCB operates at $t+1.03ms$, the fault current through LVDC2 links is cut off, and LVDC2 voltage recovers to the rated value, illustrated in Fig. 5.16(b). After the fault occurrence, a small fluctuation occurs on MVDC voltage, illustrated in Fig. 5.16(a), which returns to the rated value after fault is cleared (not shown).

According to the four case studies assessed, AB1 can contribute to fault current through diodes under LVDC2 BLKD. Meanwhile, it is observed that fault clearance device and converter blocking can be activated at different times to avoid unnecessary converter blocking. For TAB BLKD study, the blocked TAB isolates the fault while disables SST can cause the power outage of the LVAC network. For SSCB study, the fast fault clearance of the SSCB is shown in the case study. The healthy part of TAB can remain normal operation without activating converter blocking. For the SLOW DCCB case study, converter blocking will be needed as the typical HCBs cannot operate before AB3 blocking activated.

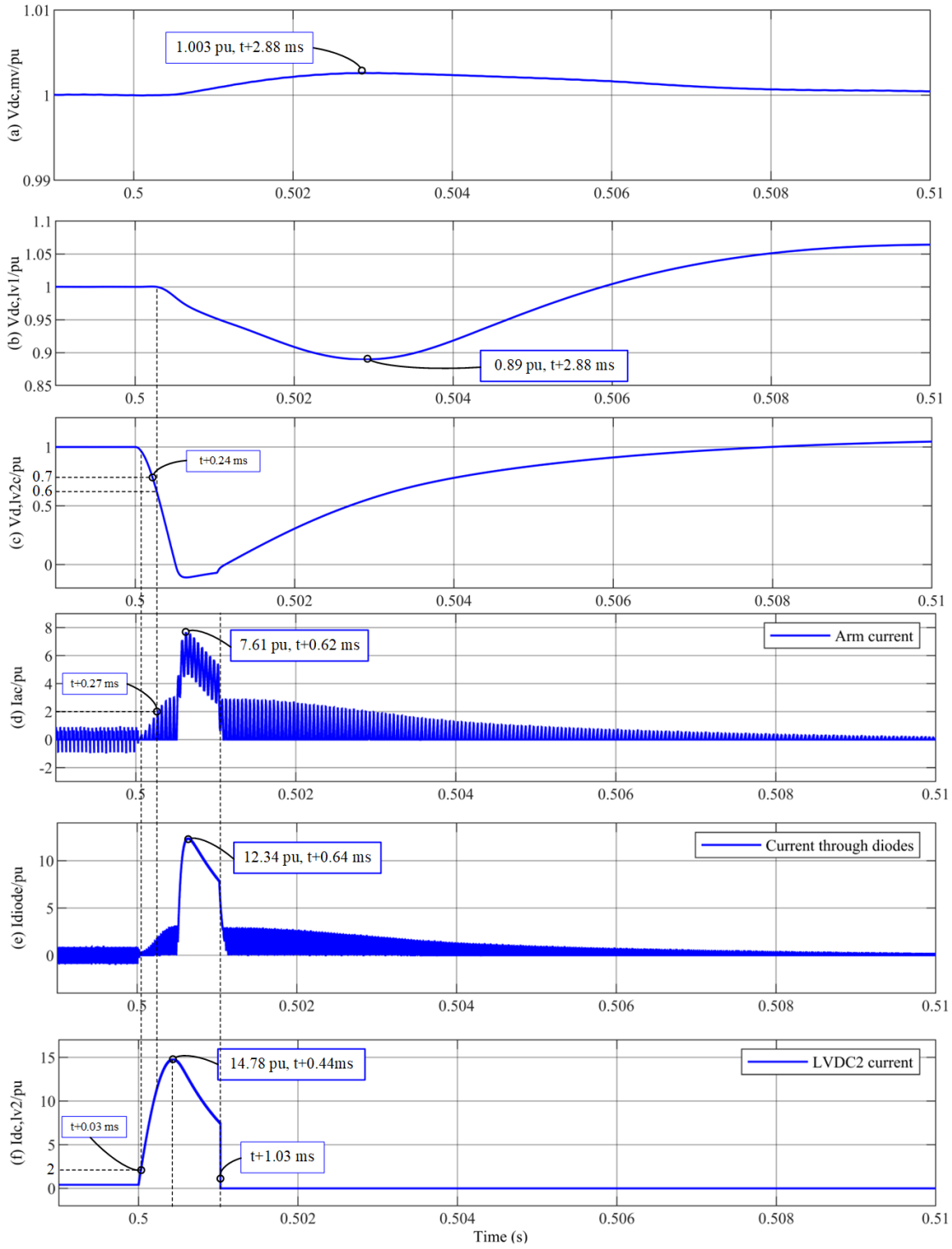


Fig. 5.16 Performance of SST with SLOW DCCB case study under the DC fault: (a) MVDC voltage; (b) LVDC1 link voltage; (c) LVDC2 link voltage; (d) arm current in AB3; (e) fault current through diodes; (f) DC output current at AB3.

5.4 Summary

Coordinated operation and protection for the SST-based hybrid AC/DC network have been investigated in this chapter. Different ways to accessing the LVDC network via SST are considered and discussed. The triple active bridge (TAB) DC/DC converter is investigated due to its decoupling and isolation of the different DC terminals. By cooperating with integrated ESD, an adaptive droop control is proposed for the SST to continue supplying the LVAC network during MVAC faults, which balances the power flow between the AC and DC networks dispatched by SST and eliminates the voltage variation. As the integrated ESD may not be at the same place as the SST, a strategy which modifies SST LVDC output voltage according to the variation of MVDC voltage, is proposed, so as to enable the ESD to control its power output according to the connected LVDC link voltage.

The DC fault characterisation of the SST-based LVDC network is then investigated, and the DC fault protection requirement is assessed. In the event of a pole-to-pole DC fault on the LVDC network, blocking only the active-bridge connected to the faulty LVDC network (AB3 in the studies) is not sufficient as the MV network can continue feeding fault current through the diodes in AB3. On the other hand, blocking the whole TAB can reduce the fault contribution from MV side and isolate the MVAC and LVAC networks from the DC fault. However, the power transmission from MV to LV by the SST will also be blocked. Thus, fast fault clearance devices are needed to ensure power supply to unfaulty network through SST. The effectiveness of different DC fault protection strategy and/or DCCBs is assessed and their impact on overall system operation studied. It is found that fast SSCBs allow the immediate isolation of the faulty DC section without the need for converter (TAB) blocking, which in turn minimizing the disruption for the healthy networks. Meanwhile, the slower DCCBs, e.g., HCBs, will result in fault current contribution from the MV side for a short period, which can affect the operation of the healthy network.

Chapter 6 Conclusion and Future Work

6.1 General conclusions

This thesis focuses on the control and operation of SST in distribution network, where improved SST control schemes are considered to achieve adaptive operation in the hybrid AC/DC network.

In this thesis, SST converters in distribution network are reviewed in terms of concept, configurations, operation and applications. A three conversion stage SST is then selected as the topology for further investigation in the thesis due to its fully controllability. As a promising solution to replace the line frequency transforms (LFT) in distribution network, SST can achieve a variety of functionalities, including voltage regulation, power regulation, renewable energy integrations, fault isolation and current limiting, and black start capability. Considering the cooperation with the conventional normal open point (CNOP) at LV network, existing control scheme cannot allow SST to operate under both grid forming and grid-connected operation. Although the limitations of SST in terms of over-voltage, over-current capability compared with LFT under fault conditions are well acknowledged, the potential benefits during post fault performance, such as fault current limiting and fault ride-through capability have not been investigated in details. Meanwhile, the concept of SST-based hybrid AC/DC network has been proposed in recent researches, but the impact of the DC fault on SST has not been investigated thoroughly. The detailed fault characteristics, protection scheme and post-fault operation of SST under DC fault need to be properly addressed.

Chapter 2 introduces the basic control for the three-conversion stage SST. The control scheme under grid-forming operation in the three conversion stages are implemented. For the DC/DC conversion stage, the operation principle of dual active bridge (DAB) is reviewed and studied. Different phase-shift modulation methods, including the Single

Phase Shift modulation (SPS), Extended Phase Shift modulation (EPS), Double Phase Shift modulation (DPS) and Triple Phase Shift modulation (TPS), are compared and TPS is considered to reduce the circulated reactive power. The basic control scheme is tuned to better understand how control parameters influence the system response. Also, the performance of the basic control scheme is assessed under step load changes, which is shown to achieve good voltage and current regulation.

Chapter 3 proposes a universal grid-forming control scheme for DC/AC converter to enable SST to operate under both grid-forming and grid-connected operation. The conventional $P-\omega$ and $Q-V$ droop control is modified to $P-v_q$ and $Q-v_d$ controllers, which allows active and reactive power controller implemented without changing the voltage and current control scheme under grid-forming operation. The large transient due to the control mode switch can be largely reduced. Also, the coupling issue between active and reactive power control loop is observed when testing the performance of the universal grid-forming control scheme. In order to reduce the P and Q coupling brought by the droop control, an additional compensation control is integrated in the universal grid-forming control by adding active and reactive power feedforward terms to the d- and q-axis current. Simulations studies show that the universal grid forming control scheme can effectively regulate power output of SST without introducing the large transient due to the control mode switch. The proposed compensation control can effectively reduce the coupling between active and reactive power during transients without affecting the overall system response.

Chapter 4 investigates the active power limiting of SST during MV network faults. Performance comparison between LFT and SST during network faults is assessed, which shows that SST provides less fault current contribution and can isolate the fault from healthy side of network. Meanwhile, large fluctuation of the SST MVDC link due to the active power unbalance is found during the MVAC network fault, which can lead to SST blocking. In order to avoid the unnecessary outage of SST, an additional active power

limiting control of SST under both grid-forming and grid-connected operation is proposed. The proposed active power limiting control associate MVDC voltage variation and d-axis voltage (grid-forming operation) or active power reference (grid-connected operation) of the LV side converter to achieve adaptive active power rebalance during the MVAC fault. The MVDC voltage can thus remain regulated during the fault, while the load/generation at the LVAC side is temporary curtailed. The proposed control is validated under both MVDC under- and over- voltage conditions, which prevent SST from unnecessary blocking and enable SST fast power supply recovery right after fault is cleared.

Chapter 5 investigates the potentials and issues for adding a LVDC port/network as part of the SST. Different types of accessing the LVDC network via SST are reviewed and discussed. The TAB converter is considered due to the decoupling LVAC network capability while providing two isolated LVDC links, i.e., LVDC1 for connecting to the DC/AC converter to supply the LVAC network and LVDC2 as a DC network). Considering an integrated energy storage device (ESD) connected with SST via the LVDC2 link, a coordination control is proposed for the ESD to secure continuous power supply to the LVAC network in the event of MVAC network fault. The active power reference of the ESD is linked with MVDC variation, so the ESD can support the LVAC network when abnormal MVDC voltage is detected by providing/absorbing additional power. Meanwhile, considering the ESD location may be different from SST which means the MVDC voltage may not be accessible to the ESD controller, the coordination control is modified to achieve adaptive power regulation. The LVDC2 voltage is linked with MVDC variation, so the ESD output can thus be regulated according to the connected LVDC2 voltage. DC fault characteristics of the SST-based LVDC network are also investigated and DC fault clearance requirement of the proposed system is raised. In order to maintain SST power supply without being affected by LVDC2 network fault, converter blocking and fast fault clearance are needed for the TAB. In addition, the effectiveness of different fault clearance schemes is assessed. It shows that SSCB can achieve fault clearance without activating converter blocking, which allows continuous power supply

to the LVAC network during DC fault. Meanwhile, HCBs can cause the TAB to block due to the slow fault isolation, which can interrupt power supply to the LVAC network.

Extensive simulation in MATLAB/Simulink have demonstrated and validated the effectiveness of the proposed control schemes and operations.

6.2 Author's contributions

The main contributions of this thesis are:

- A universal grid forming control scheme for SST to operate in the distribution network with the additional compensation control is proposed in this thesis. A grid forming control structure is implemented for both islanded and grid connected operation of the SST LV network, such that transients due to the control mode switch can be avoided. The active and reactive power feedforward terms are added directly to the d- and q-axis current components to reduce the coupling between the active and reactive power brought by the droop control without affecting the overall system response.
- The additional post-fault control schemes of SST under grid-forming and grid-connection operation are proposed. The proposed active power limiting control associates the MVDC voltage variation and d-axis voltage (grid-forming operation) or active power reference (grid-connected operation) of the LV side converter to achieve adaptive active power rebalance during faults. The proposed control is validated under both under- and over- voltage conditions, which prevent SST from unnecessary blocking due to large MVDC voltage fluctuation, and improve post-fault recovery.
- Considering an ESD integrated in one of the LVDC links of SST, an adaptive droop control is proposed for SST to continue supplying the LVAC network in the

event of the MVAC fault, which balances the power flow between the AC and DC networks dispatched by SST and eliminates the voltage variation. Considering the integrated ESD may not be at the same place as the SST, which means the proposed coordination control cannot be implemented, a strategy which modifies the output voltage of the ESD-connected LVDC link according to the variation of MVDC voltage, is proposed. This enables the ESD to control its power output according to the connected LVDC link voltage without communication.

6.3 Suggestions for future research

Potential areas for future research include:

- As the proposed control schemes in this thesis are assessed only in simulation. It is necessary to investigate the effectiveness of the control schemes under hardware implementation. Phototype or hardware-in-the-loop model of SST will be further developed to verify SST under various operating conditions.
- As the compensation control scheme is manually tuned, a unified analytical guideline will be provided to investigate the relationship between coupling and controller tuning in different rating of SST.
- The topology of SST in the thesis are only considered as two-level VSC and DAB/TAB for high level assessment. In reality, modular multilevel converter (MMC) and cascaded H-bridge (CHB) will be more applicable options for high-voltage high-power application. Thus, the applicability of the proposed control schemes in these topologies are under investigation. Also, coordination between the proposed control scheme and internal control loop are also under consideration.
- The thesis only considers the condition where there is only one SST in the network. System performance with multiple SST can be further developed to increase integration of renewable energy. The coordination among different SST for application, such as black start and inertia provision, can be assessed.

- Current applications of SST are mainly in conceptional stage, such as in distribution network, wind turbine system. And the application of SST is strictly limited due to higher cost, lower efficiency, less robustness compared with LFT or any other converter with similar functions. Apart from weight and volume-limited application (traction system), it is important to find out the potential application where the SST can bring unique benefits, such as an energy router in a hybrid AC/DC network.

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