Characterisation and design of power electronic converters for superconducting applications

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Abstract

There is a large and growing interest in superconductor applications, as they can offer optimised solutions in different areas, such as all-electric aircraft (superconducting motors), and fusion magnets (superconducting magnet accelerators) and levitation (superconducting Maglev levitation). For these applications, auxiliary circuits (converters, inverters) that utilise power electronics are required. As all superconducting systems require cooling cryostats, it would be better from the engineering point of view to have the entire electrical network inside the cryostat. This, in turn, requires power electronics to operate at lower temperatures. Literature has indicated that characteristics of semiconductor devices at cryogenic temperatures (below 123 K) change; this, in turn, would reflect on a) device selection and b) circuit topologies. Thus, this thesis aims to fill the research gaps in the performance of cryogenic power electronics suitable for superconducting applications mainly a) all-electric aircraft and b) superconducting magnet systems.

For the gap in device selection for superconducting applications, different devices including diodes, MOSFETs and IGBTs were tested. The devices are first characterised at room temperature (300 K) and then tested at Liquid Nitrogen (LN2) temperature (77 K). The characterisation tests included 1) static tests, 2) dynamic tests and 3) paralleling tests. For the dynamic tests, this thesis has proposed a bespoke current sensor that can operate at cryogenic temperature with high bandwidth, as commercial current sensors are not suitable for immersion in cryogenic temperature zones. Based on these tests, circuits were

built to test cryogenic power electronics suitable for the two superconducting applications mentioned earlier.

For the all-electric aircraft, the thesis aimed to fill in two gaps; 1) implementing a cryogenic rectifier integrated with a partial superconducting machine and 2) using different permutations of phase-leg utilising super-junction MOSFETs at cryogenic temperature. At first, the rectifier was immersed in liquid nitrogen and was connected to a superconducting machine where it was shown to have lower losses at that temperature. For the super-junction MOSFET, the thesis has tested for the first time the effect of cryogenic temperature on different permutations of diode deactivation circuits in a phase-leg structure. Based on the test results a phase-leg dc/ac using super-junction MOSFET was built and assessed at room and cryogenic temperature to determine its performance.

As for the superconducting magnet applications, the thesis has developed a tailored cryogenic dc/dc converter that utilises a nano-crystalline core step up the current at lower temperatures. The converter was able to supply current up to 500 A.

In summary, this thesis 1) identifies which devices with a rating of 1200 V are suitable for cryogenic applications 2) develops a bespoke current sensor, 3) tests a rectifier circuit implemented with the superconducting machine, 4) investigates the usage of a cryogenic converter and inverter for superconducting applications.

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Knowledge contribution

The contributions of this thesis can be summarised as follows:

- Testing and understanding the performance of high capacity power semiconductor devices and modules at cryogenic temperature as they have different packaging from the modules tested previously.
- Studying the performance of a cryogenic pulse current transformer tailored for double testing of semiconductor devices at lower temperatures.
- Demonstrated that rectifier circuit could be successfully applied to rectify signal from an HTS axial motor at cryogenic temperatures.
- Studied the effect of a short circuit on the rectifier on an HTS axial flux machine.
- Demonstrated that technique for deactivation for antiparallel diode for superjunction MOSFET could be successfully applied at cryogenic temperatures.
- Validated that the use of cryogenic forward converter to reduce the size of the current leads for a superconducting magnet application.

List of publications

[1] F. Weng, M. Zhang, **A. Elwakeel**, T. Lan, N. McNeill and W. Yuan, "Transient test and ac loss study of a cryogenic propulsion unit for All-Electric Aircraft," *IEEE Access*, vol. 9, pp. 59628-59636, Apr. 2021.

[2] **A. Elwakeel**, Z. Feng, N. McNeill, M. Zhang, B. Williams and W. Yuan, "Study of power devices for use in phase-leg at cryogenic temperature," *IEEE Trans. Appl. Supercond.*, vol. 31, no. 5, pp. 1-5, Aug. 2021.

[3] **A. Elwakeel,** N. McNeill, R. Peña-Alzola, M. Zhang and W. Yuan, "Cryogenic DC/DC converter for superconducting magnet application," *IEEE Trans. Appl. Supercond.*, vol. 32, no. 6, pp. 1-5, Sep. 2022.

[4] **A. Elwakeel**, Z. Feng, N. McNeill, M. Zhang, and W. Yuan, "Comparison of phase-leg circuits for cryogenic operation in the all-electric aircraft", in *Proc., 11th IET Power Electron. Machines Conf.,* Newcastle, UK, pp. 618-624, Jun. 2022,

[5] **A. Elwakeel**, N. McNeill, R. Peña-Alzola, M. Zhang and W. Yuan, "Study of MOSFET and IGBT modules at cryogenic temperatures", **under review**, *ASC conference*, Oct. 2022

Other publications

[6] E. Tsotsopoulou, A. Dyśko, Q. Hong, **A. Elwakeel**, M. Elshiekh, W. Yuan, C. Booth, and D. Tzelepis, "Modelling and fault current characterization of superconducting cable with high temperature superconducting windings and copper stabilizer layer," *Energies*, vol. 13, no. 24, p. 6646, Dec. 2020

[7] M. Elshiekh, **A. Elwakeel**, S. Venuturumilli, H. Alafnan, X. Pei, M. Zhang, W. Yuan, "Utilising SMES-FCL to improve the transient behaviour of a doubly-fed induction generator dc wind system", *Int. Journal of Electrical Power & Energy Systems*, vol. 131, May 2021

Abbreviations

CO_2 – Carbon dioxide

DAQ – Data acquisition card

EU – European Union

EDS – Electrodynamic suspension

ESR – Equivalent series resistance

FAA – Federal Aviation Administration

FRED–Fast Recovery Epitaxial Diode

GaN – Gallium Nitride

GaAs – Gallium Arsenide

HEMT–High electron mobility transistor

HFET – High Field Effect Transistor

HTS – High-Temperature Superconductor

IGBT – Insulated gate bipolar transistor

JFET – Junction gate field effect transistor

LTS – Low-Temperature Superconductor

LN2 – Liquid Nitrogen

LIM – Linear induction motor

LSRM – Linear synchronous motor

Maglev train – Magnetic levitation train

MRI – Magnetic resonance imaging

MOSFET–Metal oxide semiconductor field effect transistor

NASA - National Aeronautics and Space Administration

NPT – Non-punch through

PCB – Printed circuit board

RMSE – Root mean squared error

SBD – Schottky Barrier Diode

Si – Silicon

SiC – Silicon Carbide

SOI – Silicon-on-insulator

SR – Synchronous rectification

SLPM – Standard litre per minute

TI – Tapped inductor

UV – Ultra violet

Symbols

A^{**} – Richardson constant

B_{pk} – peak excursion

B_{sat} – saturation flux density

C^{o} – Celsius

C_{oss} – Output capacitance

D_{ext} – External diode

E_C – critical electric field

Hz – Hertz

H – Henry

I_c – Critical current

i_{out} – Output current

I_{ave} – Average current

i_{peak} – Peak current

i_{LOAD} – Load current

K – Kelvin

k – Boltzmann's constant

L_{in} – Input inductor

L_s – Series inductor

Q_{rr} - Reverse recovery charge

R_{DS} – Drain-source resistance

V_{BR} – Breakdown voltage

$V_{forward}$ –Forward voltage

V_{out} – Output voltage

v_{GS} – Gate source voltage

Greek Symbols

δ – duty cycle

ρ_{HTS}– Resistivity of the HTS

χ_s – Semiconductor electron affinity

ϕ_B– Metal-semiconductor barrier height

Φ_m – Metal work function

μ_n – Carrier mobility

Chapter 1

Introduction

1.1 Overview

This thesis presents an analysis of the performance of power electronics at cryogenic temperature (77 K) for superconducting applications. It includes the study and inspection of different types of semiconductor devices at temperatures between room temperature (300 K) and liquid nitrogen temperature (LN2) (77 K). The study also consists of the design and analysis of power converters for superconducting applications.

1.2 Introduction

This thesis investigates how to utilise power electronics at cryogenic temperature for superconducting applications. The main motivation to research power electronics at cryogenic temperature is for two reasons:

- Some applications, such as all-electric aircraft, fusion magnets and train transportation are expected to rely heavily on superconductors in the future that utilize superconducting machines or work in harsh and cold environments. Other applications, like aerospace applications, require the use of power electronics to supply the necessary power. Usually aerospace applications require power electronics to be thermally insulated and operate at room temperature (300 K) [1], [2]. However, this can complicate the structure of the layout from the mechanical

point of view, mainly as an extra layer of thermal insulation and heaters are required. This in turn increases the weight, volume and cost. Hence, it would be advantageous to use power electronics at cryogenic temperatures.

- The literature has shown that some semiconductor devices have different behaviours at cryogenic temperatures with some of them having lower on-resistances and faster switching speeds [1], [2]. As a result, operating semiconductors at cryogenic temperatures can reduce the power dissipation of the system and increase the overall power density.

1.2.1 Introduction to superconductivity and superconducting applications

Superconductivity was first discovered by a professor of physics at Leiden University, in the Netherlands, Heike Kamerlingh Onnes. Onnes was conducting a series of experiments concerning freezing mercury to temperatures around 4.3 K. When Onnes measured the resistance of Mercury against the decrease of temperature he discovered that the resistance falls till it reaches absolute zero. This discovery was ground-breaking at the time, leading him to win the Nobel prize in 1913 [3]-[6]. Based on Onnes's experiment, two of three restrictions of superconductivity were deduced, 1) the temperature should remain below the critical temperature and 2) the current flowing through the material should remain below the critical current. Following Onnes's discovery, Meissner was able to discover perfect diamagnetism; that superconductors can expel all magnetic fields until a critical field. Based on Meissner's experiment, the third restriction of superconductivity was

identified. The three main restrictions are shown in Fig. 1-1. These must be observed for the material to maintain the superconducting state.

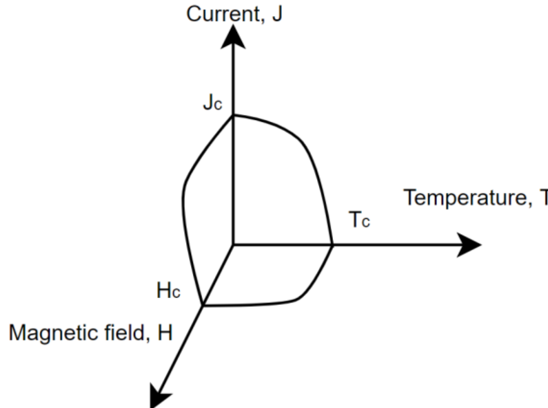


Fig. 1-1 Superconductivity boundaries [6]

Superconductors are usually characterized by a *V-I* curve where the voltage drop along the length of the superconductor is a function of the current passing through. Fig. 1-2 shows a common *V-I* curve. It is commonly accepted that at critical current I_c is the current that produces a voltage of 1μV/cm across the superconductor, as shown in the figure. The *N* value is the characteristics of a given superconductor that describes the relationship between the applied current and the voltage drop across the superconductor. The voltage across the superconductor can be described by Equation (1.1) [7]. *E(I)* is the voltage drop across the superconductor, E_C is the critical electric field at $1\mu V/cm$, *I* is the current in the conductor, I_c is the critical current and *N* is the exponent that is dependent on the superconductor type.

$$E(I) = E_C(\frac{I}{I_c})^N \tag{1.1}$$

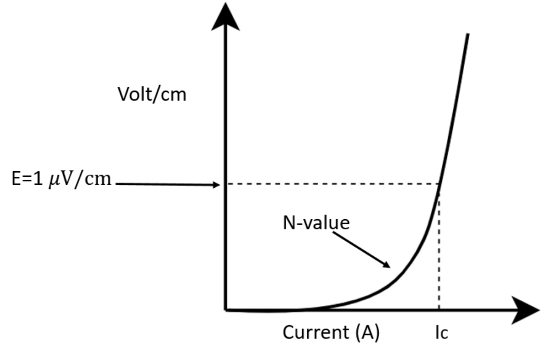


Fig. 1-2 V-I curve for a superconductor[7]

The resistivity of superconductors as shown in Fig. 1-2 can be modelled by Equation (1.2) [7].

$$\rho_{HTS} = \begin{cases} 0, T < T_C, I < I_C \\ \frac{E_c}{I_c(T)}\left(\frac{I}{I_c(T)}\right), T < T_C, I > I_C \end{cases} \tag{1.2}$$

As superconductors have much lower losses than regular conductors, they are expected to be increasingly used in future applications. In Section 1.2.2, these applications are discussed in more detail and how cryogenic power electronics can be integrated into systems is addressed.

1.2.2 Applications of superconductivity and cryogenic power electronics

Superconductor applications are predicted to be implemented in many industries mainly because superconductors have lower losses, are lighter and have a higher power density when compared to copper or aluminium. Thus, this section discusses current and future

applications of superconductivity across different fields and how power electronics can be integrated into the system. The applications discussed are;

a) All-electric aircraft,

b) Maglev (Magnetic levitation) trains and

c) MRI (Magnetic Resonance Imaging)

1.2.2.1 All-electric aircraft

Over the past years, there has been a rapid increase in air traffic which has led to stricter restrictions on the; 1) noise level produced by the aircraft, and 2) the fuel consumption and the carbon footprint of the aircraft [8]-[10]. As a result, governments and organizations around the world are calling for stricter targets on air travel. For example, the UK and the EU are pushing for net-zero carbon emissions by 2050, with aviation objectives to replace conventional aircraft with Hydrogen and All-Electric aircraft [10]-[16]. By setting stricter targets, the EU as well set a goal to reduce the CO_2 emissions by 75%, NO_x by 90% and the overall noise resulting from aircraft by 65% by 2035, pushing for hybrid electric aircraft [10]-[12]. On the other side of the Atlantic, NASA has been seeking the implementation of commercial all-electric aircraft since 2019, publishing a report on the strategy to implement electric propulsion in flights [13]. However, the plan proposed by the Federal Aviation Administration (FAA) for the United States does not yet include electric propulsion [14].

This interest in electrifying aircraft has driven aircraft manufacturers to research electric aircraft. One of the leading manufacturers, Rolls Royce [15], is currently testing Power

Generation System 1 (PGS1) in Bristol, the UK as part of a plan to have net-zero products by 2050. The PGS1 is a demonstrator Rolls-Royce engineers are using to prove new propulsion technology for future hybrid-electric regional aircraft.

Another leading manufacturer, Airbus [16] has set a goal to build an electric aircraft by 2035 using hydrogen as the source of energy. The focus on hydrogen fuel Airbus is mainly due to two reasons, a) it can be used to create e-fuels and b) it can be used for electric propulsion. Based on that, it is predicted that hydrogen can be a disruptive technology to the current aviation sector which is seen in Fig. 1-3 [17].

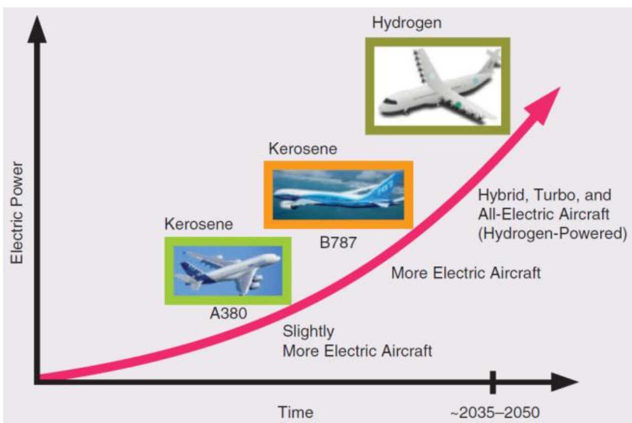


Fig. 1-3: Projected progress of the aviation sector [17]

Fig. 1-3 shows the expected use of hydrogen in the aviation sector, where based on this, commercial aircraft would be more hydrogen focused by the year 2035[17]. In that vision of all-electric aircraft, it would be expected to employ hydrogen as both a) fuel to supply electric energy to propel the aircraft, and b) coolant to cool down the superconducting machines [11], [17]. As most of the powertrain inside the aircraft is designed to operate at a cryogenic temperature, operating power electronics at cryogenic temperature would

reduce the system complexity. In addition, cryogenic power electronics have higher efficiency and higher power density than their room-temperature counterparts [1],[2].

Thus, the architecture of the all-electric aircraft is expected to be as seen in [17], where a liquid hydrogen tank supplies the fuel cell and hydrogen circulation for the aircraft. The system realises ac to dc and dc to ac power conversion in the MVA range.

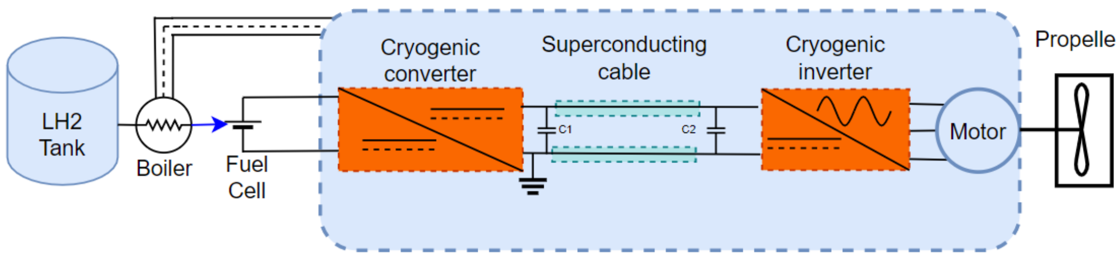


Figure 1-4: The architecture of all-electric aircraft [17]

1.2.2.2 Maglev train

With the rapid increase of population and with cities expanding their horizons and city connections becoming more important than ever, fast inter-city links are required that can offer rapid, reliable and safe transportation. This transportation as well must be environmentally friendly, suitable for mass transportation and low-maintenance. Train transportation offers one of the best solutions [18]. The Maglev is one of the train technologies that can provide very high speeds and has fewer accidents, especially derailing. In the Maglev, the wheels on the trains are replaced by using electromagnetic and levitation technologies, thus there is no contact between the train and the actual rail.

Hermann Kemper first suggested the Maglev train in a patent in 1934 [18]. In 1966, Powell and Danby were the first to work on electrodynamic levitation. In the 1970-1980s more

work was done on levitation development. Linear Induction Motor (LIM) was used for early Maglev trains, and Fig. 1-5 shows the early development of electromagnetic trains [19]. The LIM is known for its simpler construction and more straightforward design when compared to other levitation motors. However, it requires complex control and laminated iron guides to reduce losses [20]-[22]. On the other hand, utilising superconductors in Maglev has opened opportunities to reach record speeds. In 2015 the Japanese Maglev using Low-Temperature Superconductors (LTS) achieved a speed of 603 km/h on Mount Fuji for 10 seconds [23] [24]. All of this is attracting researchers from different fields to improve and expand on this technology.

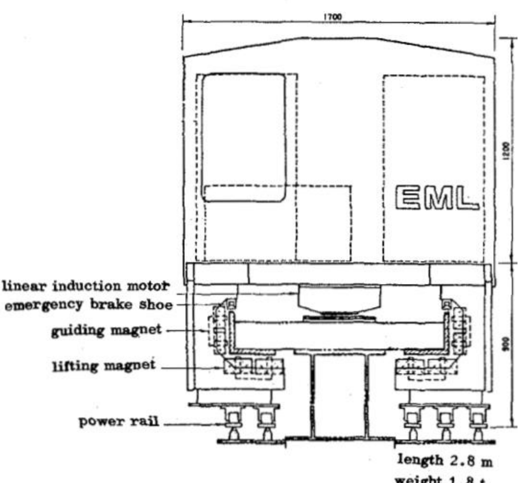


Fig. 1-5: Sectional view of electromagnetic trains developed in the 1970s [19]

Table 1-1 shows a comparison between the motor technologies used for the Maglev train. From the literature, it was shown that employing superconductors in the linear synchronous reluctance motor (LSRM) is encouraged as superconductors are known to reduce losses, increase system efficiency and high power density than regular conductors [19],[22],[24].

Table 1-1 Linear induction motor (LIM) Vs. linear synchronous reluctance motor (LSRM) for Maglev train applications

Propulsion motor type	Advantages	Disadvantages
Linear Induction Motor (LIM) [20]-[22]	• Low-cost guideways (No active parts). • Simple construction. • No dc excitation is required.	• Requires on board energy. • More complex control than the linear reluctance motor. • Must use laminated steel for the guideways to reduce eddy currents and losses.
Linear Synchronous Reluctance Motor (LSRM) [22],[25]-[27]	• Low losses (only Ohmic losses). • Large starting torque similar to the brushed dc-motor. • Change speed by changing frequency.	• Properties change according to the level of magnetic saturation. • The cross-couplings between different phase coils depend on the saturation. • The thrust pulsates due to the slotting. • The LSRM requires a high magnetisation in the air gap, thus the track and vehicle stator are thicker to prevent saturation. Hence, the amount of track iron is required to be laminated twice as much compared with LIM.

The literature in [24] discusses how superconducting coils can be used for implementing electrodynamic suspension (EDS). With superconductor coils, a cryogenic system must be in place, thus with the same case as mentioned in the all-electric aircraft, it would be easier from the engineering point of view to make the entire system operate in the same temperature region. The use of cryogenic semiconductors was first suggested in [28], [29]. The system is seen in Fig. 1-6, where a cryogenic converter is used in the Maglev trains. This configuration reduces the size of the current leads and increases the power density at

which the converters would operate at cryogenic temperature. The cryogenic converter would be mainly a dc/dc converter, which will be addressed in this thesis.

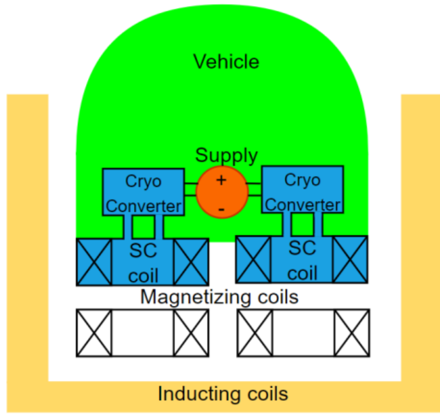


Fig. 1-6: Electrodynamic suspension using superconducting magnets [24]

1.2.2.3 MRI and magnets for particle accelerator applications

Due to their high current density, superconductors can be used to produce large magnetic fields, which is important in applications such as Magnetic resonance imaging (MRI) and fusion reactors. MRIs are one of the important techniques for non-invasive medical diagnosis. The largest commercial application of superconducting magnets is MRI, where over 100 tons of superconducting material are produced each year to meet the demands [30]. Research has always been aimed at increasing the magnetic field density of MRIs to get more clear imaging, as they were able to reach up to 3 T [31], [32].

Fusion reactors also require superconductors [33], [34] where the ITER (International Thermonuclear Experimental Reactor) has been aiming to produce a magnetic field of 11.8 T to be able to successfully maintain the fusion reaction. Fig. 1-7 shows Magnetic

confinement fusion. The reactor utilises superconductor magnets to guide the reactions through the confined space. Research is still ongoing on nuclear fusion to be able to supply constant power, but is outside the scope of this thesis.

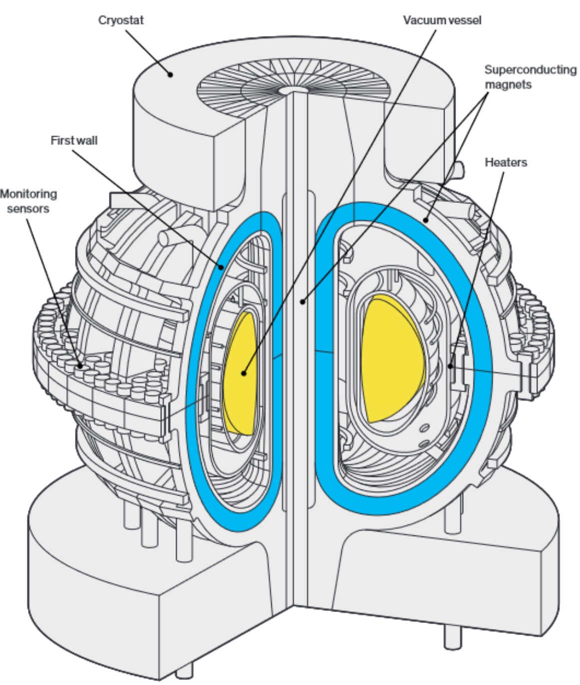


Fig. 1-7: Magnetic confinement fusion from ITER reactor [33]

As both MRIs and Fusion magnets require large magnetic fields, large charging currents are required which increases the I^2R losses in the current leads. Hence [28], [29] have reviewed different ways of reducing the losses and one of them was utilizing power electronics at cryogenic temperature.

1.2.2.4 Summary of superconductor applications

From the review, we can predict that the demand for using superconductors will increase in the future. To control these applications, a converter or inverter needs to be in place.

Hence, in the next section, the advantages of using power electronics at cryogenic temperatures to supply the necessary power shall be discussed.

1.2.3 Advantages of cryogenic power electronics

Cryogenic converters can be built using; a) superconducting switches, or b) semiconductor switches [28],[29]. The superconducting switches were tested in 1979 at the University of Twente, where the circuits were able to produce 9 kA with 50 W losses and 25 kA at 500 W losses. In [28] a superconducting rectifier circuit test rig was built as seen in Fig. 1-8. The circuit consists of the superconducting coil, commutation switch that is controlled by a transformer (solenoid), switching elements (superconducting switches) and diodes to protect the switches. The experimental results showed stable performance of the rectifier circuits at cryogenic temperature, as with the improved design of adding a solenoid to the circuit, the switches were able to be operated at a higher frequency (5 Hz) than previously done (0.1 Hz). However, some disadvantages persisted when using superconducting switches 1) require bulky transformers, 2) the higher the switching frequency the lower the efficiency, 3) no blocking voltage protection and would require some kind of other protection devices in the circuit.

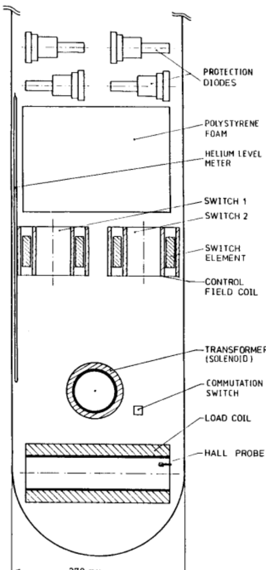


Fig. 1-8: Top view of rectifier circuit utilizing magnetically controlled superconducting switch [28]

Based on this, the authors in [28] decided to use semiconductor devices at cryogenic temperature in [29]. In [29] a power converter was built to charge a superconducting coil, where the results have shown that the losses of the chopper were reduced from 162 W at room temperature to 81.7 W at cryogenic temperature.

In [35] the advantages of using certain semiconductor devices and circuits at cryogenic temperature were summarised as the following:

- **The forward voltage of the devices decreases with the decrease of temperature**: Bulk electron and hole mobilities tend to increase by more than an order of magnitude from 300 K to 77 K. This results in a reduction in the forward on-state voltage drop (and the on-state conduction power loss).
- **Higher switching speeds due to reduced carrier lifetime**: Electron and hole lifetimes are reduced by more than an order of magnitude as the temperature

decreases from 300 K to 77 K. This decay time is mainly associated with the minority carrier device turn-off by a corresponding factor. Hence, with the lower switching losses, devices such as IGBTs and thyristors can be operated at higher frequencies.

- **Increased thermal conductivity**: The size and the weight of the device packages are much more relaxed at lower temperatures mainly due to increased thermal conductivity. Hence, the size, weight and design requirements imposed on device packages are much more relaxed at 77K than at room temperature.
- **Devices are more reliable due to reduced temperature**: Environmental issues such as corrosion and electron migration are temperature dependent. Therefore, the cryogenic environment can act as a shield to prevent these issues.
- **Noise reduction**: MOS gated devices have lower thermal noise which is directly related to the temperature. Operating these devices at lower temperatures reduces that noise.

The disadvantages of using cryogenic power electronics are [35];

- **Bulky cooling equipment**: Even though cryogenic power electronics are smaller in size when compared to room temperature power electronics, they require cooling equipment such as cryostats, insulation and other ancillary setups. This in turn can increase the overall size and cost of the system.
- **Cooling penalty for cryogenic power electronics**: Cryogenic penalty for cooling the circuit can be over 1:8; this can decrease the overall efficiency of the system and can increase the operating cost of the system.

1.2.4 Motivation

Superconductors are expected to be used in a multitude of applications. They are already employed largely by hospitals for MRI and they are expected to have an important impact on transportation as they offer high power densities, thus making all-electric aircraft and ultra-fast trains likely. Superconductors are also anticipated to play a critical role in providing sustainable energy with the current research in nuclear fusion, as they can produce large magnetic fields that can make sustainable fusion reactions. The mentioned superconducting application requires an input power supply. The power supply may be an ac to dc, dc to dc, or dc to ac converter. Since all superconducting applications require a cryogenic system to be in place, it is better from the engineering point of view to make the entire electrical system operate at the same temperature.

The above-mentioned applications of superconductors require power electronic circuits to regulate the required output, which can be either 1) Speed (all-electric aircraft and Maglev) or 2) Magnetic flux density (MRI and fusion reactors). Placing the power electronic circuits at cryogenic temperature would simplify the mechanical structure, as they would be directly integrated with the superconductor. Furthermore, some power electronic devices have higher efficiency at cryogenic temperatures. Thus, this can improve the system's overall efficiency.

An alternative to using semiconductor devices at low temperatures is to utilise a superconducting switch, which can be used to switch from the on-state to the off-state by changing the magnetic field [28],[29], [35]. However, it was found that the breakdown

voltage, switching speed and reverse bias leakage in these devices compared poorly with state-of-the-art semiconductor devices.

Using semiconductor power converters at cryogenic temperature has shown to offer high power density and high efficiency compared to using them at room temperature [1],[2]. In addition to these benefits, an analysis of a cryogenic power converter installed in radar systems has shown a decrease in the losses by 50% and reduced mass and volume, and can yield more than 65% savings in fuel consumption in comparison with the room temperature power system [36].

This thesis is mainly focused on identifying and testing the performance of semiconductor devices at cryogenic temperatures. Due to available cooling restrictions, the tests will not be conducted below 77 K and will be conducted from 77 K to 300 K. Upon finding the most suitable devices for operation at cryogenic temperatures, the thesis directs its focus on designing and building 1) power converter for all-electric aircraft; a cryogenic rectifier and a cryogenic phase leg for both dc/dc and dc/ac conversion and 2) high current cryogenic dc/dc converter for superconducting magnet applications.

1.2.5 Research questions (knowledge gaps)

1) What is the performance of semiconductor devices, with current ratings above 100 A, perform at cryogenic temperature? Which of these devices have the lowest losses at cryogenic temperature?
2) What is the performance of a rectifier connected to a superconducting machine? What is the impact of a fault on the rectifier side on the superconducting machine?

What are the performance of diode deactivation circuits of the silicon superjunction (SJ) MOSFET at cryogenic temperature?

3) Can the current leads for superconducting magnets be reduced in cross-sectional area to decrease the cooling losses to reduce the heat leakage? How to design a cryogenic forward dc/dc converter that allows a decrease in the current leads' cross-sectional areas?

1.3 Thesis Structure

This thesis includes an introduction to superconducting applications, a review of power semiconductor devices at cryogenic temperature, testing semiconductors for cryogenic power electronics and designing and testing of power converter circuits, the layout of the thesis is as follows;

- **Chapter 1** outlines the contained research of the thesis and its structure. The chapter provides a brief introduction to the applications of the superconducting coils, which include all-electric aircraft, Maglev trains and MRI and superconducting magnets.
- **Chapter 2** reviews cryogenic power electronics in literature. The review includes the previous literature on tests and equations on cryogenic power electronics. Also, the chapter includes a review of passive devices' performance at cryogenic temperature.
- **Chapter 3** discusses the setup of the experiment rig for characteristics tests and investigates the performance of semiconductor devices at cryogenic temperature.
- **Chapter 4** investigates the performance and tests setup for cryogenic rectifier and a phase leg for dc/dc converter and dc/ac inverter for use in the all-electric aircraft.

- **Chapter 5** investigates the performance and tests a setup of a cryogenic high current dc/dc converter used to supply current to a superconducting magnet.
- **Chapter 6** presents conclusions, the author's contribution, and suggestions for future research.

Chapter 2

Review of the performance of power converter elements at cryogenic temperature

This chapter presents the groundwork for the following chapters, by surveying previous work done on a) cryogenic power electronics and then b) giving a brief review of the performance of passive elements at cryogenic temperature.

2.1 Introduction

There has been increased interest in cryogenic power converter circuits as they promise higher power density, efficiency and performance than room temperature power electronics. Some special applications such as space vehicles or fusion nuclear reactors require to be operated at cryogenic temperature; in these systems, the power electronics are usually thermally insulated from the rest of the system so they can be operated at room temperature. However, this can overcomplicate the system and increase the cost and the volume. Several benefits have been highlighted for cryogenic power electronics, these include; a) faster switching as the carrier mobility has increased b) lower dissipation losses resulting from enhanced switching with lower switching on surge currents and lower on-state voltage, and the improved efficiency subject to the cooling system [1],[2].

In Sections 2.2 and 2.3, a review is done on the performance 1) of power electronic devices and 2) passive components at cryogenic temperature.

2.2 Performance of semiconductor devices at cryogenic temperature

The characterisation of semiconductor devices is mainly done to understand how a device will behave in a circuit and to predict losses, reliability and switching speed of the device. This section is mainly concerned with two main characteristics; a) static characteristics, b) dynamic characteristics (switching), and c) paralleling test:

- From the static characteristics we can deduce;
    - Forward voltage/ on-resistance; measuring the forward voltage indicates the losses the semiconductor has during the forward conduction period.
    - Breakdown voltage; measuring the breakdown voltage shows the voltage blocking capabilities of the device.
- From the dynamic characteristics we can identify;
    - Switching behaviour of the device, the rise and fall time indicates how much energy is lost in the device during switching.
- Static paralleling test:
    - Gives an indication of how would devices share current if they are paralleled together.

This section shall cover a review of different semiconductor devices' performances at cryogenic temperatures. Mainly five devices are to be reviewed; 1) diodes, 2) Si/SiC MOSFETs, 3) IGBTs, 4) GaN HEMT and HFET and 5) JFET.

2.2.1 Diodes

In [1], [2] a brief review on diode characteristics at cryogenic temperature was given and highlights that the forward voltage increases with the decrease of temperature. This is seen in Fig. 2-1, where different types of diodes, which includes; fast recovery diodes, PiN diodes, and Schottky diodes have been tested for the forward voltage [37]–[40]. The test also included different diode materials such as Silicon Carbide (SiC), Gallium Arsenide (GaAs) and Silicon (Si). In [37] it was highlighted that the forward voltage for the Si diode increases linearly with the decrease of temperature, however, that of the SiC diode increases non-linearly.

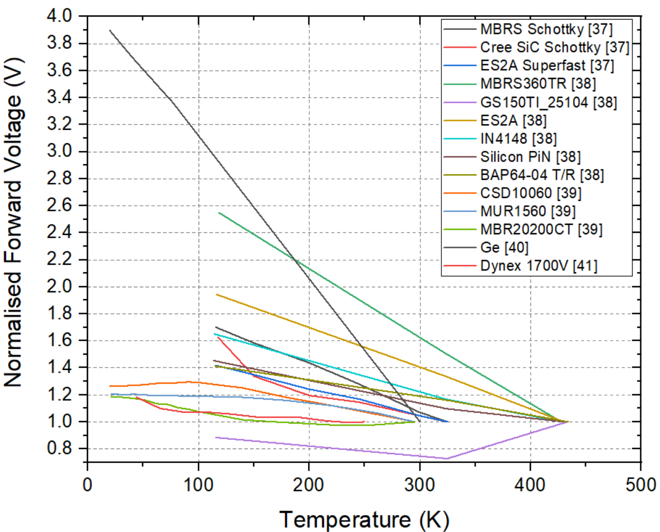


Fig. 2-1: Normalised forward voltage of diodes vs. temperature evaluated in previous literature

In [37], [39], and [40] experiments were done to assess the values of the resistance when the device is in forward conduction. As seen in Fig. 2-2, the Cree SiC, Silicon Schottky, SiC Schottky and Silicon Ultrafast diode have had an increased resistance; this can be due to the structure of the diode, as Schottky diodes have shown a positive temperature

coefficient. The Silicon diode in [40] has shown a rapid decrease for the on-resistance down to 75 K, but its resistance rapidly increases afterwards due to carrier freezout.

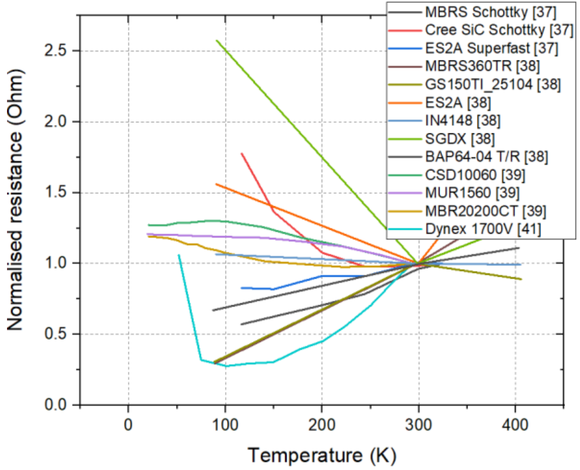


Fig. 2-2: On-resistance vs. temperature evaluated in previous literature

In [37], [41] the breakdown voltage of several types of diodes was tested at cryogenic temperature. It was found, as seen in Fig. 2-3, that the breakdown voltage of SiC Schottky, Cree SiC and ES2A Ultrafast diodes has slightly increased. As for the remaining diodes, the breakdown voltage has decreased by approximately 20%.

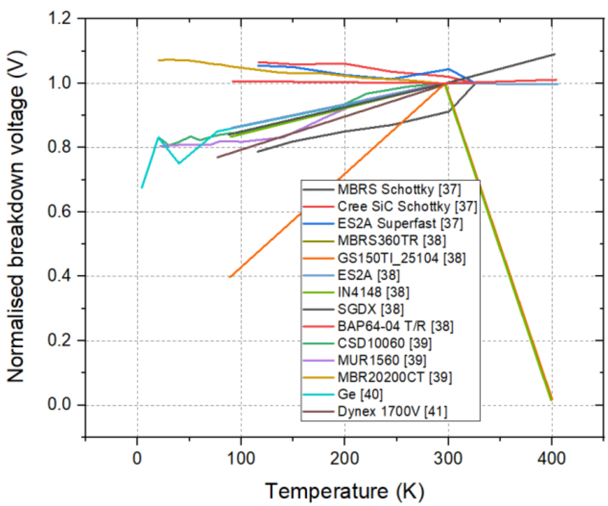


Fig. 2-3: Diode reverse breakdown vs. temperature evaluated in previous literature

The switching performances of two devices tested in [40],[41] are shown in Fig. 2-4. where the results have shown that a decrease in temperature corresponds with a decrease in the switching time due to an electron and hole diffusion coefficient change [35], and hence a reduction of the switching losses.

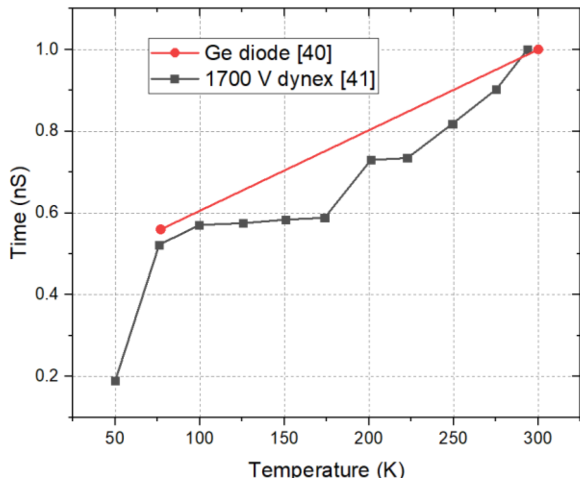


Fig. 2-4: Diode switching characteristics vs. temperature evaluated in previous literature

The test results of the diodes shown in Fig. 2-1, Fig. 2-2, Fig. 2-3 and Fig. 2-4 are summarised in Table 2-1.

Table 2-1 Summary of diode literature review

Device tested	**Rated voltage**	**Rated current**	**Test results**			
			Threshold voltage	On-resistance	Breakdown voltage	Switching losses
MBRS360TR [37], [38] **Si Schottky**	60	4	+70%	-18%	-22%	N/A
ES2A [37], [38] **Si Fast**	50	2	+62%	-18%	0%	N/A
CSD10060 [37] **SiC Schottky**	300	10	+26%	+77%	0%	N/A
GS150TI_25104 [38] **GaAs Schottky**	250	4	-12%	-70%	-60%	N/A
SGDX [38] **SiGe (Not specified)**	450	10	+45%	+150%	-16%	N/A
1N4148 [38] **Si Switching**	100	0.2	+65%	+6%	-17%	N/A
BAP64-04 T/R[38] **PiN diode**	100	0.2	+40%	-33%	0%	N/A
MBR20200CT [39] **Si Schottky**	200	20	+150%	+20%	-17%	N/A
MUR1560 [39] **Si Fast Recovery**	600	15	+20%	+20%	-20%	N/A
CSD10060 [39] **SiC Schottky**	600	10	+26%	+27%	-17%	N/A
Ge diode [40]	Not specified	Not specified	+370%	N/A	-33%	-40%
1700 V Dynex diode (Not specified) [41]	Not specified	Not specified	+18%	5%	-23%	-80%

From the table, it can be concluded that the threshold voltage increases for all of the diodes. For the on-resistance, it can be deduced that the Schottky diodes have increased resistance with the decrease in temperature. The breakdown voltage for all diodes (excluding SiGe and GaAs) decreases. As for measuring the switching time, [40] and [41] have shown that

with the decrease in temperature the switching time decreases, yielding lower switching losses. The reviewed literature can be summarised as seen in Table 2-1, where different diodes had various reactions to the decrease in their operating temperature. Overall, the trend can be seen that the threshold voltage of the diodes increases at a lower temperature. On the other hand, the on-resistance, breakdown and switching losses decrease with the decrease in temperature.

2.2.2 Si MOSFET

In [42]-[47] the literature reviewed the performance of the Si MOSFET at different temperatures. The $R_{DS(on)}$ of a selection of MOSFETs plotted against temperature is shown in Fig. 2-5, where there is a significant dip in the $R_{DS(on)}$ in the region of 50-100 K [42], [43].

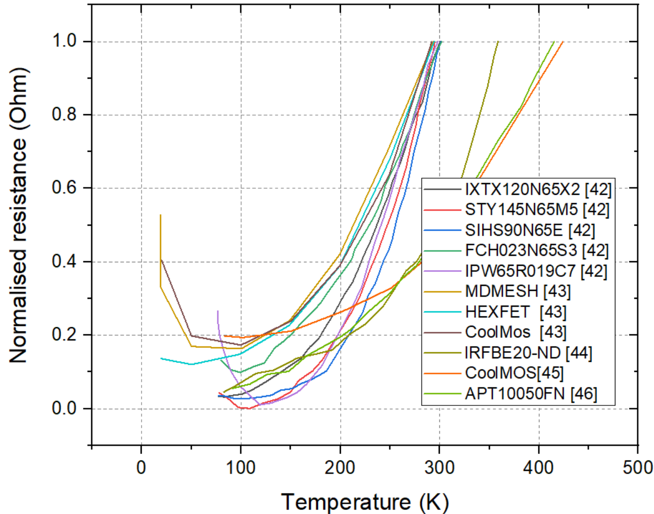


Fig. 2-5 Normalised on-state resistance of MOSFETs vs temperature evaluated in previous literature

The breakdown voltage of the Si MOSFET decreases with the reduction of the temperature by typically 33%. The normalised breakdown voltage of the MOSFET is plotted against temperature in Fig. 2-6 [42]-[45], [47]. This decrease can be primarily attributed to the increase of mean free path and higher impact ionization. Thus, care must be taken when designing a system at a cryogenic temperature to accommodate the decrease in breakdown voltage of the MOSFET, which is at least 20%.

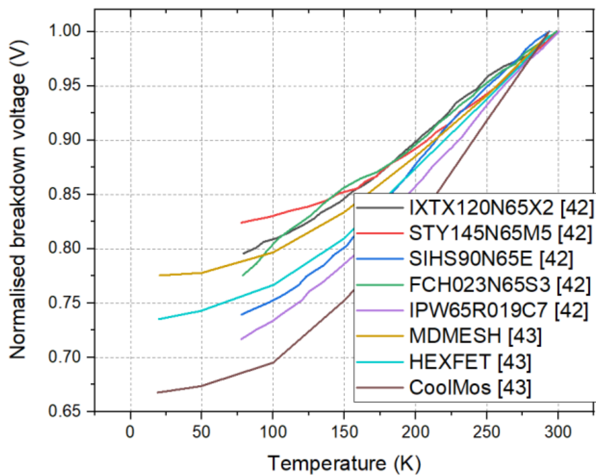


Fig. 2-6: Breakdown voltage of Si MOSFET vs temperature evaluated in previous literature

The gate-source threshold voltage $v_{GS(th)}$ has also been shown to increase with the decrease of temperature as seen in Fig. 2-6. [45], [47]. The relative increase in $v_{GS(th)}$ is caused by the fall in the intrinsic carrier concentration in the p-base region [47]. Below 77 K, carrier freeze-out starts to have a larger effect on the threshold voltage which is mainly due to the low ionisation energies and beginning of carrier freeze-out of doping atoms [45], [47].

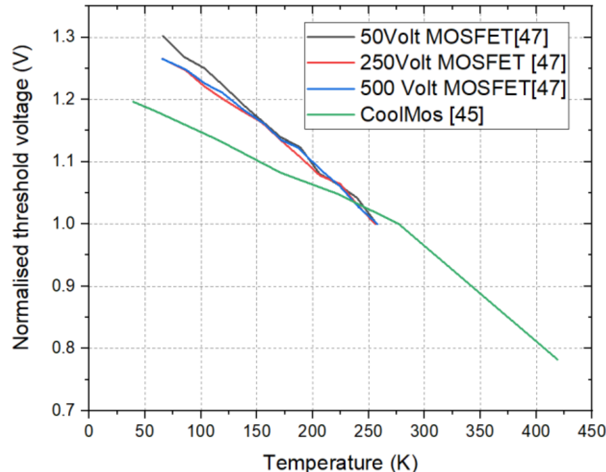


Fig. 2-7: Si MOSFET gate-source threshold voltage vs temperature evaluated in previous literature

The switching time of the MOSFET decreases with temperature as seen in Fig. 2-8 [46]. However, it is noted that an increase in the threshold voltage can increase the switching losses.

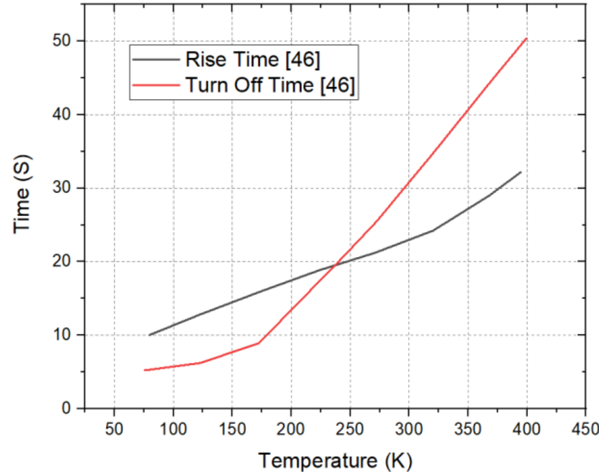


Fig. 2-8: MOSFET rise-time and turn-off time vs temperature evaluated in previous literature

The review of the performance of the Si MOSFET can be summarised as seen in **Error! Not a valid bookmark self-reference.**. From the table it can be seen that the on-resistance

decreases by around 50% to 95%, the breakdown voltage also decreases from 18% to 80%, the switching losses decrease by around 90% and the gate-source threshold voltage increase by 18%-30%.

Table 2-2 Summary of reviewed Si MOSFET devices

Device tested	Rated voltage (V)	Rated current (A)	Test results			
			On-resistance	Breakdown voltage	Switching	Gate – source threshold
IXTX120N65X2 [42]	650	125	-96%	-20%	N/A	N/A
STY145N65M5 [42]	650	138	-95%	-18%	N/A	N/A
SIHS90N65E [42]	650	87	-95%	-23%	N/A	N/A
FCH023N65S3 [42]	650	75	-86%	-22%	N/A	N/A
IPW65R019C7 [42]	650	75	-80%	-29%	N/A	N/A
MDMESH [43]	-	-	-50%	-23%	N/A	N/A
HEXFET [43]	-	-	-87%	-27%	N/A	N/A
CoolMos [43]	-	-	-60%	-33%	N/A	N/A
lRFBE20-ND [44]	-	-	-96%	-80%	N/A	N/A
CoolMos [45]	-	-	-80%	-25%	N/A	18%
APT10050FN [46]	1000	22	-95%	N/A	-90%	N/A
500V MOSFET [47]	500	-	N/A	-20%	-	30%
250V MOSFET [47]	250	-	N/A	-18	-	26%
50V MOSFET [47]	50	-	N/A	-25%	-	20%

2.2.3 SiC MOSFET

The forward voltage and the resistance of different SiC MOSFETs were tested at cryogenic temperature across different references [48]-[51]. Unlike the Si MOSFET, the

SiC MOSFET experiences an increase in its on-resistance with the decrease of temperature. This is plotted in Fig. 2-9. As a result, it is assumed that the SiC MOSFET has higher conduction losses at temperatures below room temperature.

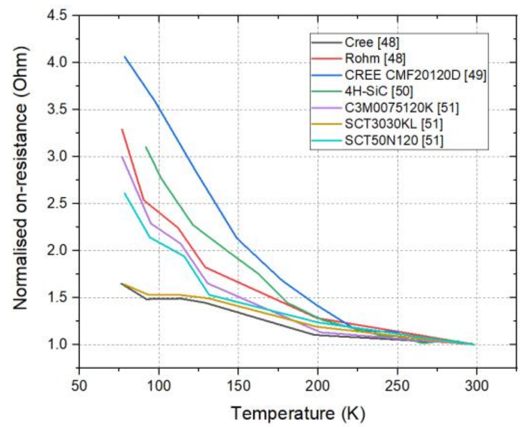


Fig. 2-9: Normalised on-resistance of SiC MOSFET vs temperature evaluated in previous literature

The breakdown voltage of the SiC MOSFET is plotted against temperature in Fig. 2-10 [50],[51]. It is seen that the breakdown voltage at lower temperatures has different behaviour in different types of MOSFET. While some SiC MOSFETs show no change, others show a decrease in the breakdown voltage with the decrease in the temperature.

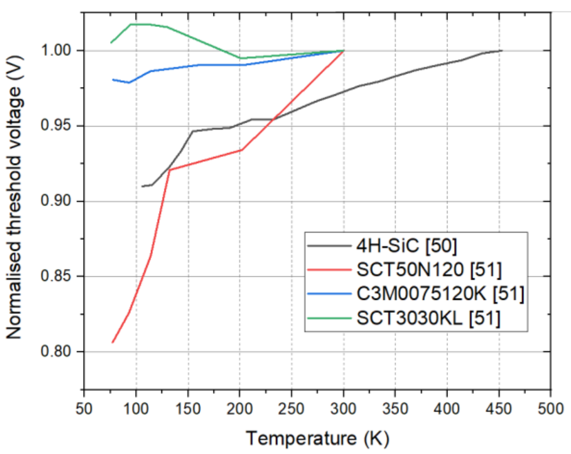


Fig. 2-10: Breakdown voltage of SiC MOSFET vs temperature evaluated in previous literature

At lower temperatures, the switching losses of SiC MOSFET have decreased as seen in Fig. 2-11 similar to the results of Si MOSFETs.

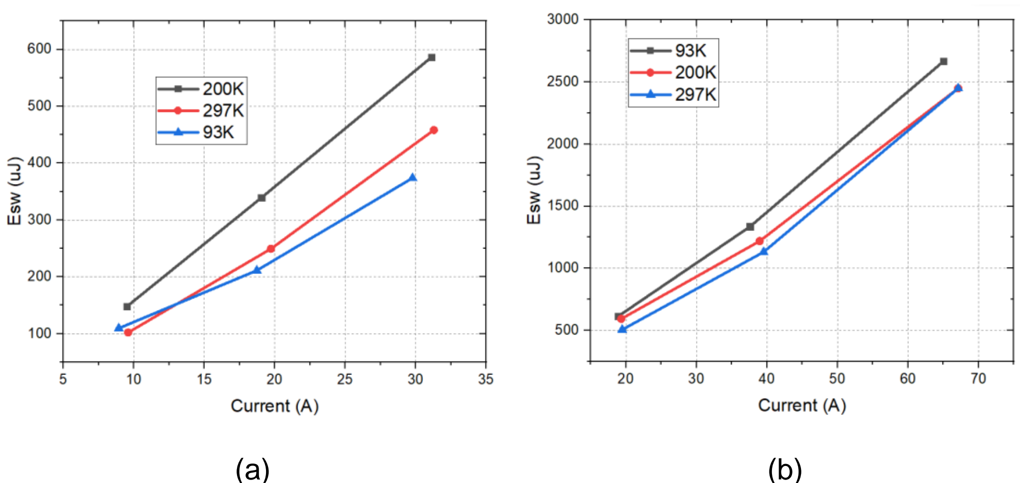


Fig. 2-11: Switching speed against temperature for (a) Wolfspeed Rohm C3M0075120K (b) Rohm SCT3030KL [51]

The gate-source threshold voltage of the SiC MOSFET increases with the decrease of temperature as seen in Fig. 2-12, a similar result to that of the Si MOSFET.

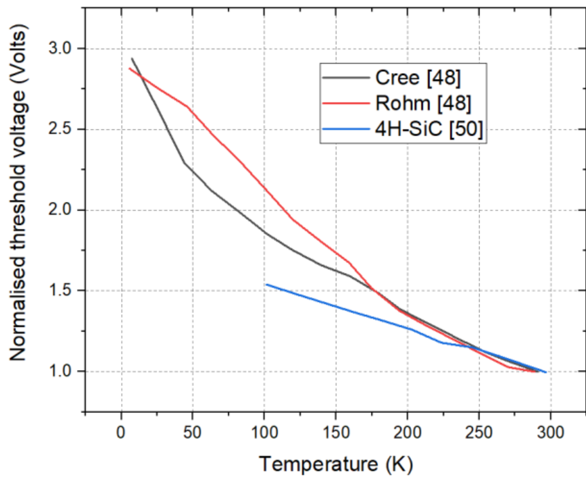


Fig. 2-12: Gate-source threshold voltage vs temperature evaluated in previous literature

The performance of the SiC MOSFET is summarised in Table 2-3, where it is seen that the on-resistance increases by 60% up to 200%, the breakdown voltage decreases at most by 20%, the switching losses increase up to 25% and the gate-source threshold voltage increases in the range of 160%.

Table 2-3 Summary of reviewed performance SiC MOSFET devices

Device tested	**Rated voltage (V)**	**Rated current (A)**	**Test results**			
			On-resistance	Breakdown voltage	Switching losses	Gate – source threshold
Cree [48]	-	-	60%	N/A	N/A	170%
Rohm [48]	-	-	120%	N/A	N/A	N/A
CMF20120D [49]	1200	90	180%	N/A	N/A	N/A
4H-SiC [50]	-	-	200%	-10%	N/A	160%
SCT50N120 [51]	1200	65	200%	-20%	N/A	N/A
C3M0075120K [51]	1200	30	70%	-2%	+10%	N/A
SCT3030KL [51]	1200	72	170%	0%	+25%	N/A

2.2.4 IGBT

The literature in [52]-[55] have tested different IGBTs' performances at cryogenic temperature. The decrease in temperature has been shown to affect the collector-emitter voltage $v_{CE(on)}$ [52], [53]. This is seen in Fig. 2-13 that the IGBT's $v_{CE(on)}$ at a collector current of 100 A has decreased for the 1700-V NPT IGBT 3 in [18], and also for the 600-V IGBT in [19]. The PT IGBT's $v_{CE(on)}$ was found to increase below 100 K [18]. This may be due to the structure of the IGBT.

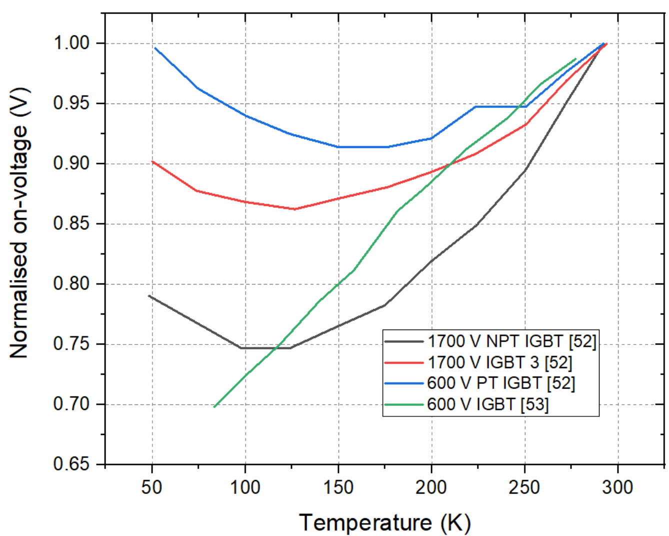


Fig. 2-13: On voltage vs temperature evaluated in previous literature

In terms of the on-resistance of the IGBT, the temperature is directly proportional to the resistance, thus decreasing the operating temperature of the IGBT decreases the resistance; this can be seen in Fig. 2-14.

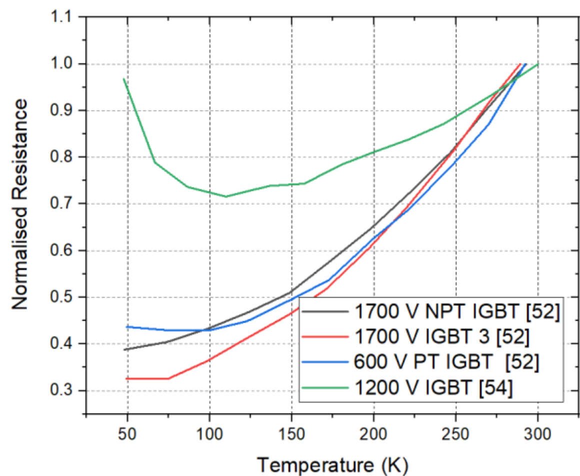


Fig. 2-14: Normalised IGBT resistance vs temperature evaluated in previous literature

The breakdown voltage of the IGBTs seems to decrease with the decrease of temperature, which is shown the Fig. 2-15 as the breakdown decreases to reach 35% of the room temperature value at near 50K for IGBT 3 and between 70-80% for NPT and PT IGBTs.

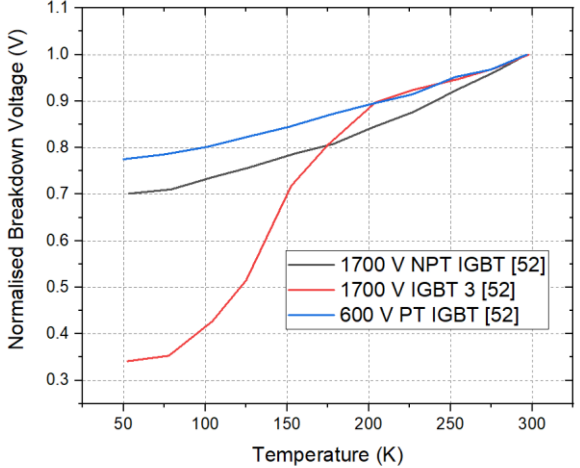


Fig. 2-15: Breakdown voltage of IGBTs vs temperature evaluated in previous literature

The effect of temperature decrease is shown in Fig. 2-16, where the decrease in temperature has resulted in a decrease in the switching losses.

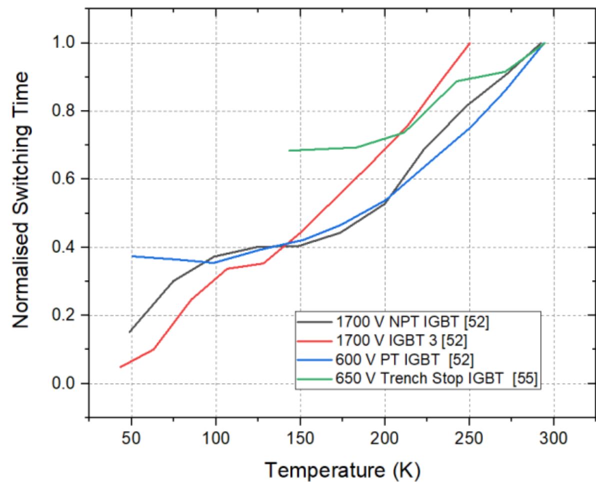


Fig. 2-16: Switching time of IGBTs vs temperature evaluated in previous literature

In [41], the gate resistance of the IGBT was measured at different temperatures, where it was found that with the decrease in temperature the gate resistance decreased as seen in Fig. 2-17. The gate resistance has a great influence on the turn-on transient as it affects both the turn-on delay time and the transit time of the current to rise from zero to full current level are related to the gate resistance. Hence, at values of larger resistances, longer delay time and transit time are required [41]. This can be the reason why the switching time has decreased.

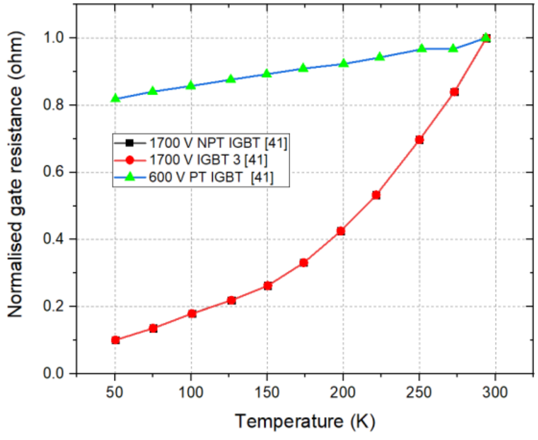


Fig. 2-17: Gate resistance vs temperature evaluated in previous literature

The performance of the IGBT can be summarised as seen in

Table 2-4 where the on-resistance decreases by 20% to 70%, and the breakdown voltage decreases by 20%-60%. Switching losses have shown a significant decrease by decreasing up to 85% and the gate-source resistance decreased by around 90%.

Table 2-4 Summary of reviewed performance of IGBTs

Device tested	**Rated voltage (V)**	**Rated current (A)**	**Test results**			
			On-resistance	Breakdown voltage	Switching losses	Gate – source resistance
1700 V NPT IGBT [41],[52]	1700	-	-60%	-30%	-85%	-90%
1700 V IGBT 3 [41] ,[52]	1700	-	-70%	-60%	-95%	-90%
600 V PT IGBT [41], [52]	600	-	-60%	-20%	-63%	-18%
1200 V IGBT [54]	1200	-	-20%	N/A	N/A	N/A
650 V Trench Stop IGBT [55]	650	-	N/A	N/A	-34%	N/A

2.2.5 GaN HEMT/Vertical

The GaN HEMT is one of the wide bandgap transistors that had attracted interest in research due to its low losses compared to other semiconductors [1]. GaN HEMT is a lateral device architecture that is less well suited to power applications. Vertical structure is optimal for achieving devices with higher breakdown voltage up to 650 V and current

up to 100 A without paralleling and suffer less from thermal management issues associated with thin-film surfaces and yield more die on a wafer[56] -[58]. The device tested in [57] was a vertical junction field transistor. In [56]–[58] the on-state resistance of a GaN HEMT was measured at a lower temperature. As seen in Fig. 2-18, its resistance decreases with temperature.

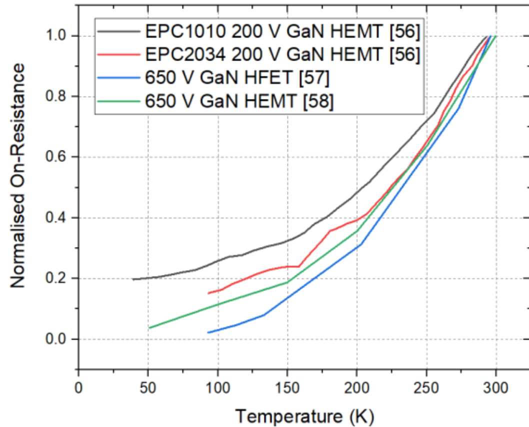


Fig. 2-18: On-resistance of GaN power devices vs temperature evaluated in previous literature

The breakdown voltage of the GaN HEMT has been shown to increase by 10 % with the decrease in temperature as in Fig. 2-19.

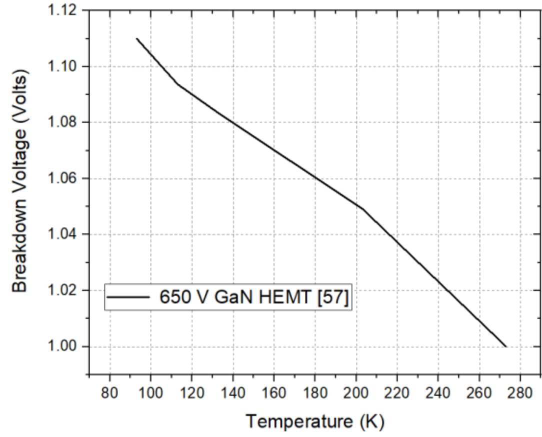


Fig. 2-19: Breakdown voltage of GaN HEMT vs temperature evaluated in previous literature

The switching losses seen in Fig. 2-20 of GaN HEMT have been shown to decrease with the decrease in temperature. There were sparse data when it came to the switching losses on the GaN HFET, and thus it is not mentioned in this review.

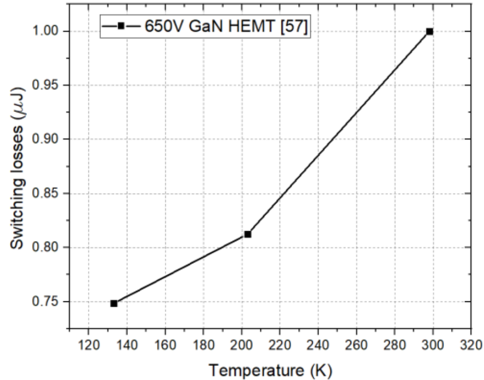


Fig. 2-20: GaN HEMT switching losses vs temperature evaluated in previous literature

The gate threshold voltage had different reactions to the decrease in temperature. This can be seen in . Where EPC2034 device in [56] shows an increase in the gate voltage threshold. However, the 650-V GaN HFET in [57] has been shown to almost stay the same and for the GaN HEMT in [58] the gate threshold voltage decreases.

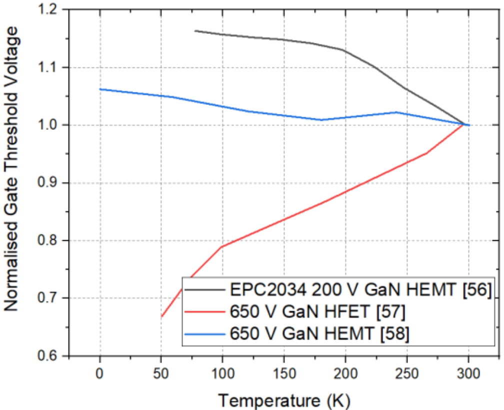
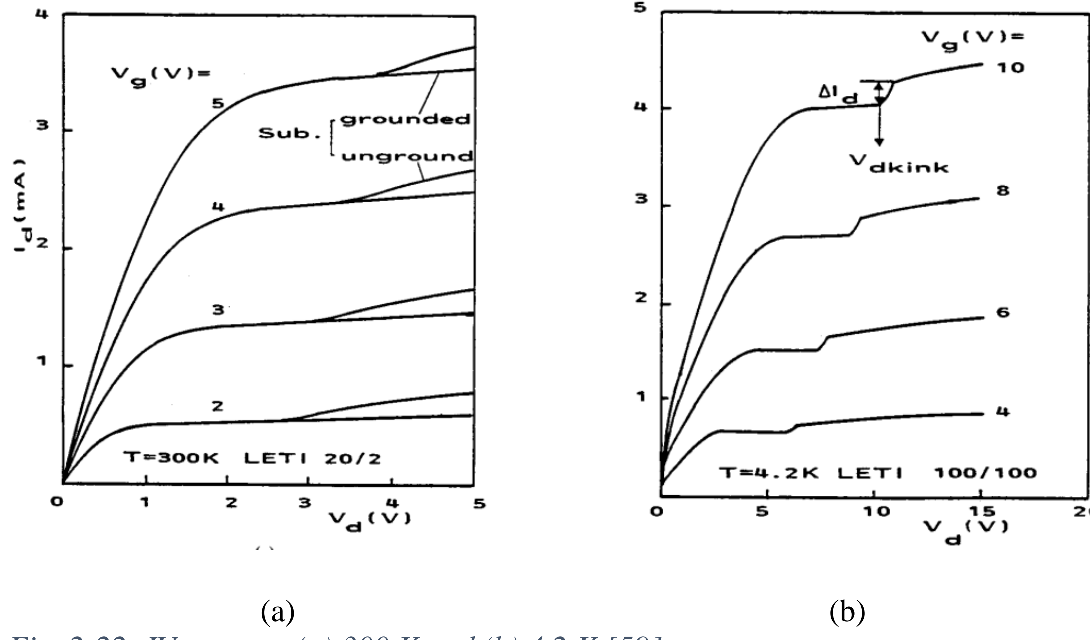


Fig. 2-21: GaN gate-source voltage threshold vs temperature evaluated in previous literature

The GaN shows a very promising switching device at cryogenic temperature, nevertheless, there are several drawbacks to using them. The maximum gate-source voltage to be applied to the device is 7 V, thus an overshoot can damage the device easily. In addition to that [59] mentions that at cryogenic temperature GaN devices suffer from the kink effect; which is a rapid increase in the drain current provoking an increase in the conductance. The kink effect arises from the threshold voltage shift due to the forward biasing of the source-substrate diode caused by substrate impact ionization current flowing from the drain to the source. This also occurs in bulk silicon MOSFETs operating at very low temperatures or when disconnecting the substrate electrode at room temperature, nevertheless, previous literature did not highlight it as a major issue for cryogenic MOSFETs [60]. Fig. 2-22 shows how a typical kink effect can be generated on standard bulk MOSFETs operating at (a) room temperature when the substrate electrode is disconnected from the ground and (b) obtained on bulk MOSFETs operating at liquid helium temperature. In this case, the bulk is so resistive because of the impurity freeze out that the substrate is practically at a floating potential.

The kink effect is known to reduce the lifetime of the device and increase its losses and is particularly in narrow bandgap semiconductors such as SOI MOSFETs or GaN, where impact ionization is more probable. A solution was offered to reduce the kink effect by adding UV lights on the GaN [59].



(a) (b)

Fig. 2-22: IV curve at (a) 300 K and (b) 4.2 K [59]

The performance of GaN devices reviewed in the literature is summarised in Table 2-5. The on-resistance has generally seen a decrease by 80%, the breakdown voltage has seen an increase of around 10%, as for the switching losses it has decreased by 25%, however, the gate-source resistance seen variable performance between increasing by 15% in [56] and decreasing 25% in [57].

Table 2-5 Summary of reviewed performance GaN devices

Device tested	Rated voltage (V)	Rated current (A)	Test results			
			On-resistance	Breakdown voltage	Switching	Gate – source resistance
EPC1010 200 V GaN HEMT [56]	200	12	-80%	-	-	-
EPC2034 200 V GaN HEMT [56]	200	48	-80%	-	-	+15%
650 V GaN HFET [57]	650	-	-93%	+10%	-25%	-25%
650 V GaN HEMT [58]	650	-	-92%			+6%

2.2.6 Si/SiC JFET

In different literature, the characteristic of the JFET has been tested at different temperatures [61]-[63]. Fig. 2-23 shows the on-voltage vs temperature of devices tested in [59],[60], where it can be seen there is around 40% reduction of the forward voltage at cryogenic temperature, hence losses for the JFET would be lower at cryogenic temperature.

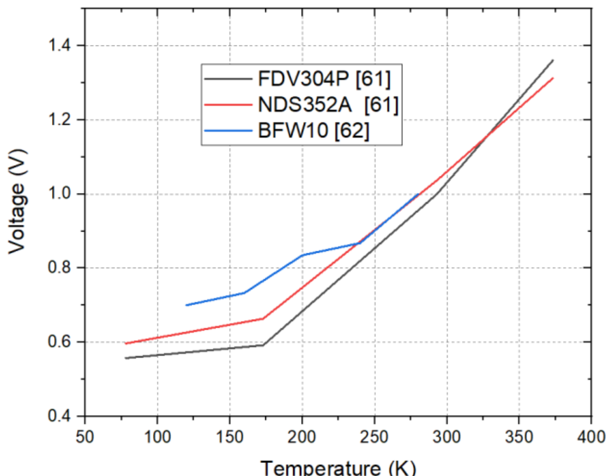


Fig. 2-23:JFET normalised forward voltage vs temperature evaluated in previous literature

The on-resistance of the JFET was tested at different temperatures for two different JFETs; 1) normally-off JFET and 2) normally-on JFET [63]. From Fig. 2-24, it can be deduced that the resistance of the device decreases below 300 K, and starts rising again around 170 K.

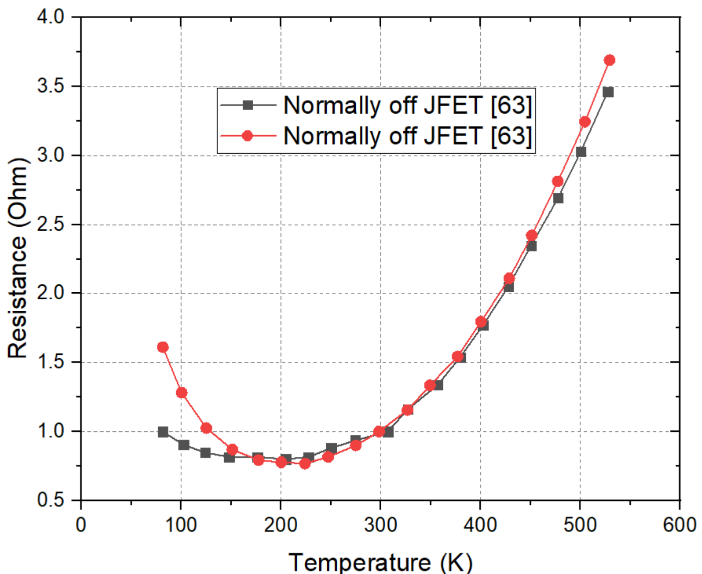


Fig. 2-24: JFET normalised resistance vs temperature evaluated in previous literature

The performance of the reviewed JFET devices can be summarised as seen in Table 2-6 where it can be seen that the on-resistance increases up to 120%. There were very sparse data in the literature in regards to testing the JFETs breakdown voltage, switching characteristic and gate-source threshold voltage at cryogenic temperature.

Table 2-6 Summary of reviewed performance JFET devices

Device tested	**Rated voltage (V)**	**Rated current (A)**	**Test results**				
			Forward voltage	On-resistance	Breakdown voltage	Switching	Gate – source resistance
FDV304P [61]	25	0.46	-60%	N/A	N/A	N/A	N/A
NDS352A [62]	30	1.7	-40%	N/A	N/A	N/A	N/A
BFW10 [63]	30	0.02	-30%	N/A	N/A	N/A	N/A
Normally-off JFET [63]	1700	-	N/A	+3%	N/A	N/A	N/A
Normally-on JFET [63]	1700	-	N/A	+120%	N/A	N/A	N/A

2.2.7 Summary of reviewed semiconductor devices

The summary of the reviewed semiconductor devices is presented in Table 2-7. From the reviewed papers, the semiconductor switches with the least losses are Si diodes, MOSFETs, IGBTs and GaN devices. The breakdown voltage and the switching losses have been shown to decrease across most of the semiconductor switches.

It is noted that most of the devices tested in the literature are not suitable for the large ratings of superconducting applications. Thus in the next chapter semiconductor devices, such as diodes, MOSFETs and IGBTs with power ratings suitable for cryogenic applications will be tested.

Table 2-7 Summary of reviewed performance of semiconductor switches

Device tested	**Test results**			
	On-resistance	Breakdown voltage	Switching losses	Gate–source resistance/ Threshold voltage
Si MOSFET	Decreases by 60%	Decreases by 30 - 80 %	Decreases by 90%	Increases by 18%-30%
SiC MOSFET	Increases by 70%	Decreases by 10%	Increases by 10%	Increases by 160%
IGBT	Decreases by 60%	Decreases by 30-60%	Decreases by 63%-85%	Decreases by 18%-90%
GaN	Decreases by 80%	Increases by 10%	Decreases by 25%	Ranges between +15% to -25%
JFET	Increases by 3%-120%	N/A	N/A	N/A

2.3 Performance of passive components at cryogenic temperature

As the performance of semiconductor devices has been discussed in the previous section, in this section we review passive devices' performance at cryogenic temperature in the literature as they represent an important part of the circuit.

Three main passive components will be discussed in this section; 1) resistors, 2) capacitors and 3) HTS inductors

2.3.1 Resistors

In [37], [38], [60] resistor values were measured at different temperatures. In Table 2-8 [64], most of the values of the resistors remain the same with the decrease in temperature. However, the ceramic and carbon composition resistors values change with the decrease in temperature. In [64], the resistors have undergone five thermal cycles at a rate of 10°C/min. The thermal cycling test results have shown a slight change in the resistance values after cycling.

Table 2-8 Performance of resistors at cryogenic temperatures [64].

2.3.2 Capacitors

Type	Value (Ω)	Resistance (Ω) at 300 K	Resistance (Ω) at 83 K	Change in Resistance (%) at 83 K
Metal film	10	10.00	9.99	0.0
	1K	999.15	1001.86	0.3
Wirewound	10	9.70	9.62	-0.9
	1K	984.80	979.31	-0.6
Thin film	33	33.07	34.32	3.8
	1K	995.41	1007.88	1.3
Thick film	100	99.99	105.42	5.4
	1K	998.70	1003.22	0.5
Carbon film	10	9.96	10.46	5.1
	1K	980.30	1035.83	5.7
Carbon composition	15	14.65	16.34	11.6
	1K	1013.29	1296.54	28.0
Ceramic composition	10	9.49	10.99	15.8
	1K	993.09	1167.51	17.6
Power film	10	10.00	10.48	4.9
	1K	996.20	1037.06	4.1

In [37], [38], [65]–[71] have discussed the effects of cryogenic temperature on the capacitors. In [38] two of the propylene capacitors that underwent tests at lower temperatures have exhibited mechanical failures. In [65] a tantalum capacitor has been tested at cryogenic temperatures where the capacitance was lower at 77 K and decreased even further with the increase of temperature. When placed in a cryogenic environment Aluminium electrolytic capacitors have seen a rapid decrease to almost zero [66], this can be attributed to the freezing of liquid electrolytes and loss of capacitance. Polypropylene,

polycarbonate and MICA types have shown good performance at cryogenic temperature as their capacitance was not affected by the temperature [37], [38], [68], [70]. In [71] the Equivalent Series Resistance (ESR) of different capacitors have been tested at 77 K and 4K. The results show that X7R and Y5V ceramic capacitors have had a significant increase in their ESR. The NPO's ESR remained the same at 1 kHz. Polyphenylene ESR decreased with temperature. Table 2-9 shows the effects of cryogenic temperature on the capacitance of different capacitor types. The dissipation of capacitors at cryogenic temperature is given in Table 2-9. The dissipation factor is defined as the ratio of ESR to capacitance reactance [72].

Table 2-9 Different capacitor types' capacitance at cryogenic temperature

Capacitor Type	**Capacitance at Cryogenic Temperature**
Metalized polypropylene	Increased by 5% [37]
Polypropylene (Film/Foil)	Increased by 5% [37], [38], remained the same [66]
Polyethylene	Decreased by 5% [37], [38], [71]
NPO Ceramic	Slight increase by 1% [37], remained the same [66], [67]
Ceramic (X7R, Y5V)	Different results been recorded for X7R as it decreased by 41% [37], and decreased by 80% [66], [71], Decreased at higher frequency [68], Y5V decreased by 50% [71]
Tantalum (TAJ)	Decreased 10% [38]
Tantalum (T491)	Decreased 10% [38]
Tantalum	Decreased 10% [38], [61], [68], decrease by 20% [66]
Film	Decreased at 50 Hz by 8% [67]
Mica	Remained the same[38]
Polycarbonate	Slight decrease by 5%[66]
Polyphenylene	Remained the same [66], [71]
Z5U	Decreased up to 80% [66]
Al Electrolytic	Became zero [66]
Polyester	Decreased by 80% [71]

2.3.3 Magnetic materials

In the literature different magnetic materials have been tested at a cryogenic temperature [72],[74]. The performance of fifteen different magnetic materials at below room temperatures is shown in Fig. 2-25.

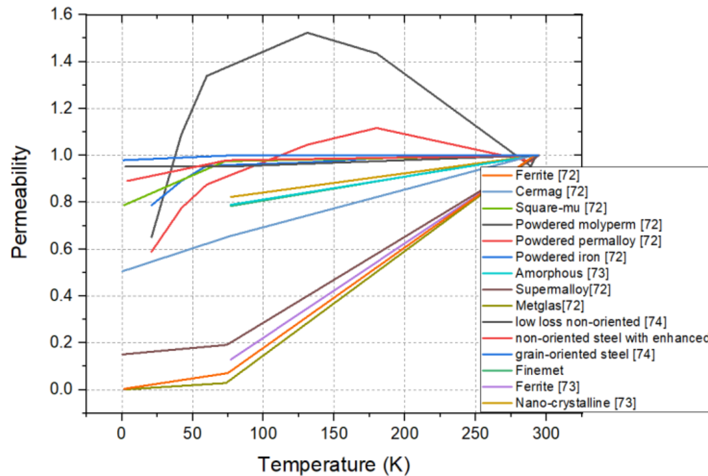


Fig. 2-25: Magnetic material performances vs temperature evaluated in previous literature

Table 2-10 summarises the performance of magnetic materials at cryogenic temperature. It is seen that with ferrites, commonly used for room temperature applications, permeability significantly drops with the decrease of temperature and they are hence not preferred for cryogenic applications. Ferrites have shown a rapid increase in core losses at cryogenic temperature, up to 18 times the room temperature value [73]. On the other hand, materials such as powdered molyperm, powdered permalloy, square-mu, powdered iron and nano-crystalline suffer less than 20% permeability reduction at cryogenic temperature, making them valuable candidates for cryogenic applications. Amorphous, grain-oriented steel and Finemet materials also had good performances at the cryogenic

temperature where their permeability has been reduced by 22% at a lower temperature. The core losses in the nano-crystalline core did not change with the decrease in temperature, however, they increased by 18 % for the amorphous core.

Table 2-10 Performance of magnetic materials at cryogenic temperature

Material	Change of permeability at cryogenic temperature
Supermalloy[72]	-85%
Metglas[72]	-99%
Ferrite [72]	-99%
Cermag [72]	-50%
Square-mu [72]	-20%
Powdered molyperm [72]	-5%
Powdered permalloy [72]	-11%
Powdered iron [72]	-3%
Amorphous [73]	-22%
Nano-crystalline [73]	-18%
Ferrite [73]	-88%
Finemet [74]	-22%
Grain-oriented steel [74]	-22%
Non-oriented steel with enhanced permeability [74]	-42%
Low loss non-oriented [74]	-35%

2.3.4 Inductors

Given that the demand for ultra-low losses technology is increasing and since the power electronic circuit tested would be operating at cryogenic temperature, it is highly

favourable to examine the usage of an HTS inductor as a replacement for the copper inductor.

In [75] a comparison was made between using a copper and an HTS coil as inductors where both were used for high voltage generation in part of the RLC circuit; the HTS coil was made from 37 filaments of Bi-2223/Ag wire consisting of two pancakes each with $r_{inner} = 20\ cm$ and $r_{outer} = 43\ cm$ with a 10-A critical current. It was shown that a 0.12 H HTS coil was able to store more than double the energy of a cryogenically cooled copper coil with a 0.19 H inductance, these results are shown in

Table 2-11.

Table 2-11 Comparison between copper and HTS inductors [75].

	HTS inductor 77K	**Copper inductor 77K**	**Copper inductor 300K**
Voltage Generated (kV)	2.8	1.2	0.2
Resistance (Ω)	-	4.7	36
Energy (J)	93	41	7
Inductance (H)	0.12	0.19	0.19

In [76] a brief efficiency comparison between HTS and copper inductors was made. A 3 mH HTS coil consisted of two 18 turns double pancake coils, an inner diameter of 130 mm, an outer diameter of 133.6 mm and a height of 32 mm. The total loss in the coil was 9 W. If a copper coil at room temperature was used instead with 3 mH inductance the estimated total resistance would be 2.61 $m\Omega$ considering 2 A/mm^2 and the resistivity to be 0.0175 $\Omega \cdot mm^2/m$ then the losses would be 104.37 W at 200 A. Thus, it can be estimated that an HTS inductor would reduce the losses in this case by 90%, similar to the results obtained when comparing an HTS coil to a copper coil at room temperature in [75].

The effect of ripple current on the HTS coil has been discussed in [77]–[79], where the hysteresis losses are dominant. Also, it was shown that the first harmonic was the largest contributor to the ac loss, for that an increase in a 24-pulse ac/dc rectifier would have a higher efficiency than that of a six-pulse ac/dc rectifier. It was calculated that the hysteresis loss could be in the range between 0.30 - 0.45 mW/m for the HTS inductor. In [79] has shown that the ripple current can decrease the critical current of the HTS inductor which can cause the coil to quench at lower operating currents; where the higher the RMS of the ripple current the lower the critical current would be for the coil. In [80] has studied the effect of the ripple current on the thermal stability of the coil. It was shown that a coil with a rating of 68 A, the critical current a 55 A load (80% of the critical current) and a 6 A ripple current (10% of the critical current) would push the coil into thermal instability causing the temperature to exponentially increase.

The literature in [81] and [82] have discussed how the relationship between energy and volume is for the HTS inductors. In [81] it was shown that the coil shape and configuration might affect the critical current by reducing the maximum radial magnetic flux density of the HTS coil. Fig. 2-26 shows (a) the cross-section of a rectangular coil and (b) the cross-section of a step-shaped coil with three different radii. According to the calculations, coil (b) has shown higher energy density. Thus it can be concluded that the main factors affecting the coil design are 1) the critical current 2) configuration and the shape of the coil.

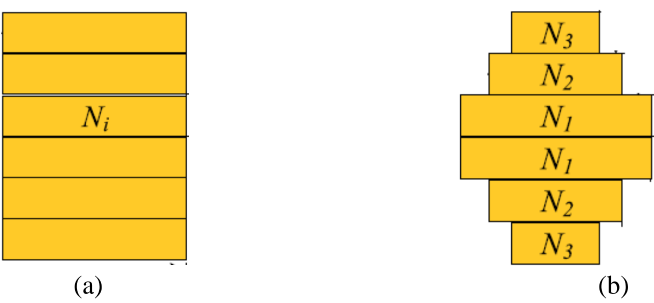


Fig. 2-26: Different coil rectangular cross-section a) rectangular cross-shaped b) inner and out step-shaped

From the review it can be concluded that HTS inductors provide better performance than their copper counterparts; as they reduce the losses by 90% (without considering the cooling losses) [76]. Nevertheless, factors such as high ripple current and the shape of the winding/coil are important to take into consideration as this might affect the amount of energy stored in them and the maximum allowable current that can pass through them.

2.3.5 Summary of reviewed passive components at cryogenic temperature

In this section, the performance of several passive components at cryogenic temperature has been reviewed. Most of the resistors maintained small changes when they were cooled down, except that for the carbon and ceramic composition. As for the capacitors, materials such as ceramic capacitors drop immensely, however polypropylene suffers from a slight decrease at cryogenic temperature. For magnetic cores, ferrites which are widely used in room temperature applications permeability drops immensely, on the other hand, Nano-crystalline and powdered cores have shown slight reduction at a lower temperature. In the

end a review of inductor performances at cryogenic temperature, where it was shown that HTS inductors have higher efficiency and can store more energy than copper inductors. However, it is noted that the critical current of HTS materials drops when it is wound as an inductor and hence the shape and design of the inductor need to be considered.

2.4 Summary

In this chapter, we have discussed the performance of the circuit elements at cryogenic temperature. The literature gives a good indication of which devices are best suited for a low-temperature operation that would allow us to proceed through the next chapters. However, most of the tested devices in the literature have either rated currents below 50 A or rated voltages below 100 V, which presents a research gap that needs to be filled. Over the next paragraphs, a summary is done of the work presented in this chapter.

The chapter starts with analysing semiconductor devices' characteristics. The devices which were considered are diodes, MOSFETs, IGBTs, GaN HEMT/HFET devices and JFET. From the reviewed literature, devices such as diodes, SiC MOSFET and JFET conduction losses increase with the decrease of temperature. Meaning that using these devices at cryogenic temperature would reduce the overall circuit efficiency. However, devices such as Si MOSFETs, IGBTs and GaN HEMT/HFET have shown decreased conduction losses at cryogenic temperature, which in turn would increase the efficiency of the circuit if it were used at cryogenic temperature.

The chapter then reviews passive devices such as resistors, capacitors, magnetic cores and inductors. Most of the resistors are slightly affected by cryogenic temperature with a

decrease of up to 6%, except for carbon and ceramic composition which can suffer a decrease of up 28% in resistance. Similarly, capacitors have shown a slight decrease at cryogenic temperature to 90% of their room temperature capacitance value. Magnetic cores on the other hand have shown various performances at cryogenic temperatures. For example, ferrites have shown a decrease of to become 12% of their room temperature value. Metglas, Nano-crystalline and powdered iron have shown good performances as their value has not dropped with the decrease in temperature. In addition, inductor performance was reviewed at cryogenic temperature, where HTS coils are known to virtually have no resistance and are more power-dense when compared to their copper counterpart.

As mentioned earlier, some devices which were tested had ratings that would not be sufficient to power large applications, thus in the next chapter, a set of devices with suitable current and voltage ratings for superconducting applications are selected and their performance is evaluated at cryogenic temperature. The results are compared with the literature review done in this chapter.

Chapter 3

Testing power electronic devices at cryogenic temperature

This chapter mainly focuses on testing different semiconductor devices at cryogenic temperatures. Diodes, MOSFETs and IGBTs characteristics are tested at both room and cryogenic temperatures. The tests done on these devices are; 1) static, 2) dynamic and 3) paralleling tests. Section 3.1 discusses the research gaps covered in this chapter.

3.1 Research gap on testing semiconductor devices at cryogenic temperature

Chapter 2 has discussed the performance of different semiconductor devices that were tested in the literature at cryogenic temperature. Most of the components previously tested at cryogenic temperature had a current rating of 100 A or lower. Thus, in this chapter, we explore the performance of semiconductor devices that have ratings above 100 A at 77 K as they have different packaging from the devices that have been tested earlier. This will be done by testing different types of semiconductor devices at room and cryogenic temperatures and assessing the performance of these devices based on the results. In addition to that, the double pulse test conducted in the literature has used current measurement outside of liquid nitrogen, thus introducing stray inductance into the circuit.

Accordingly, the research gaps covered in this chapter are;

- Investigating the performance of semiconductor devices with rating above 100A as they have different packaging from what was tested in the literature.
- Studying the performance of a cryogenic pulse current transformer tailored for double testing of semiconductor devices at lower temperatures.

3.2 Introduction

The goal of this chapter is to test the performance of semiconductor devices at cryogenic and room temperatures. Primarily three tests will be used to assess the performance;

a) Static test; this tests the device's static characteristics. This test is mainly divided into 1) forward voltage test; which indicates the conduction losses of the devices, and 2) breakdown voltage test; which indicates the breakdown voltage withstand of the device.
b) Dynamic voltage test (double pulse test); this test is mainly executed to deduce the switching losses at a given voltage and current value.
c) Paralleling test; this test is done to understand the current sharing of devices at cryogenic temperature and whether two or more devices can share current equally.

Based on the review done in the previous chapter; diodes, MOSFETs and IGBTs have shown an improved performance at cryogenic temperature. Thus, devices were selected to be tested at room and cryogenic temperatures.

3.3 Characteristic tests

In this section, the performance of semiconductor devices ae mainly assessed based on two different tests 1) static characteristics test, 2) dynamic characteristics test and 3) paralleling test.

3.3.1 Static characteristics tests

Static characteristic determines the *I-V* curve of the semiconductor device, based on which we can understand the performance of the device at different current and voltage values [83].

Power semiconductor devices can be allocated into three categories based on the degree of their controllability:

- On and off states are controlled by the external power circuit; diodes.
- Latched on by a control signal but must be turned off by the power circuit; thyristors.
- Turned on and off by control signals; controllable switches (e.g. BJT, MOSFET, JFET, GTO thyristor, IGBT, HEMT, HFET).

The *I-V* curves for the diode are represented in Fig. 3-1, Fig. 3-2 and Fig. 3-3 where for forward bias, diodes and IGBTs have a small voltage across them. MOSFETs act as a switch with a resistor and do not exhibit an offset forward voltage. As for the reverse bias, negligible leakage current passes through the diode and IGBTs until reverse breakdown voltage occurs. MOSFETs can conduct in both forward and reverse. For MOSFETs is a

leakage current and voltage breakdown if the device is switched off. The forward and the reverse bias indicate the conduction losses of the device and the max reverse voltage the device can undertake [83].

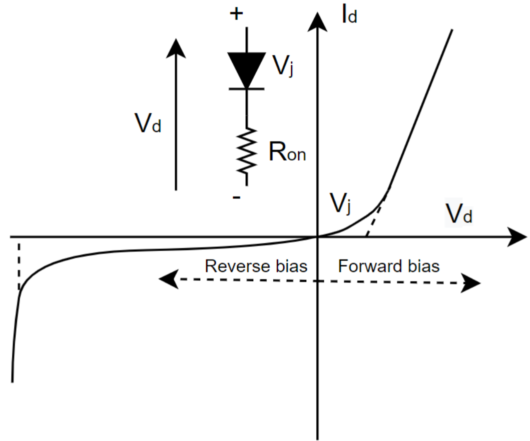


Fig. 3-1:I-V curve for diodes [83]

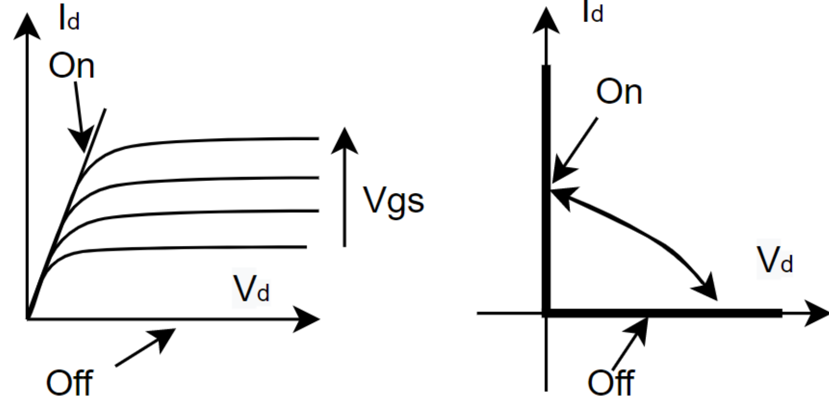


Fig. 3-2: I-V curve for MOSFET [83]

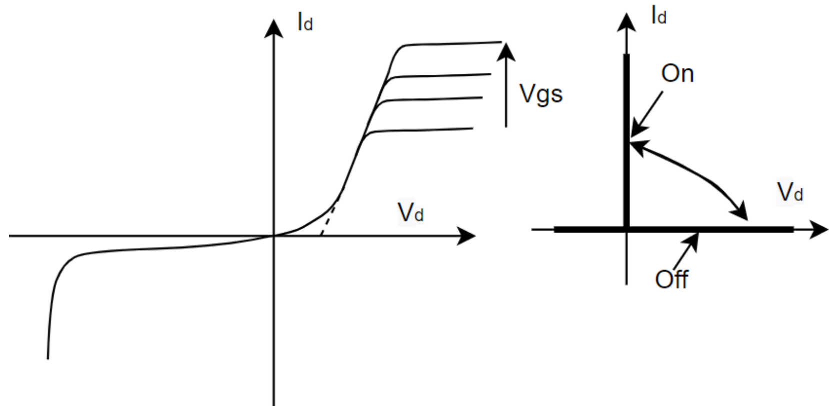


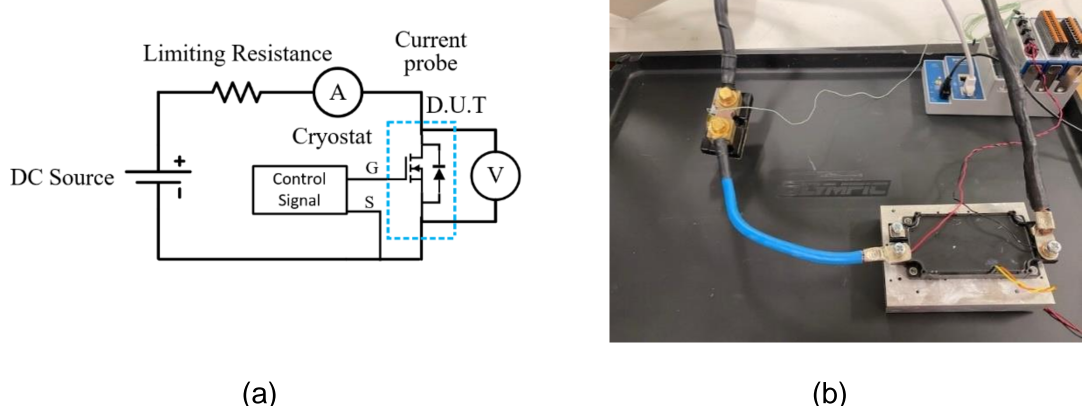
Fig. 3-3: I-V characteristics of IGBT [83]

3.3.1.1 Forward voltage test

The test circuit, as seen in Fig. 3-4 [84] includes the Device Under Test (DUT) and a DC power source set to operate in constant-current mode. In the test, the current level is changed while the voltage level is monitored. In this procedure, it is assumed that the heating produced by the constant current will not produce substantial changes in the junction temperature of the device immersed in liquid Nitrogen especially if the duration is in the range of milliseconds thus preventing temperature rise.

The equipment used in the test includes;

- Isolated Genesys GSP10-1000 dc power supply with current limitation
- cDAQ 9185 with NI 9229 (sampling 25 kHz).
- NI LabVIEW 2018 SP1 to control the Genesys power supply.
- Shunt resistor (current sensor).
- PT100 sensor to measure case temperature.



(a) (b)

Fig. 3-4: Forward voltage testing circuit (a) schematic diagram, (b) experimental setup

A flowchart describing the testing procedure is shown in Fig. 3-5. The tests start with setting the current and the voltage values in the LabVIEW program, which controls the power supply. The LabVIEW program switches on the power supply which pushes the current through the DUT and the reading of the device voltage and the voltage across the shunt resistor are collected in an Excel spreadsheet. Using the voltage readings taken across the shunt resistor, the current passing through the device is calculated. For the forward voltage, the voltage across the device is directly measured through the NI card.

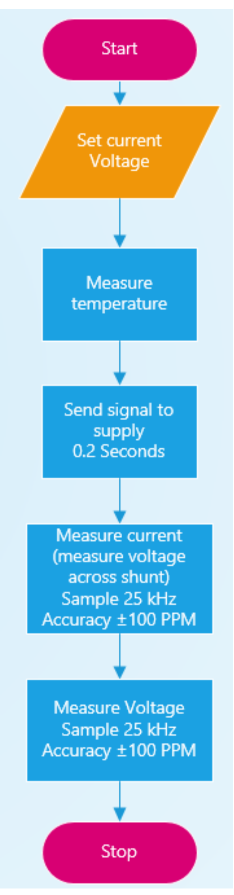


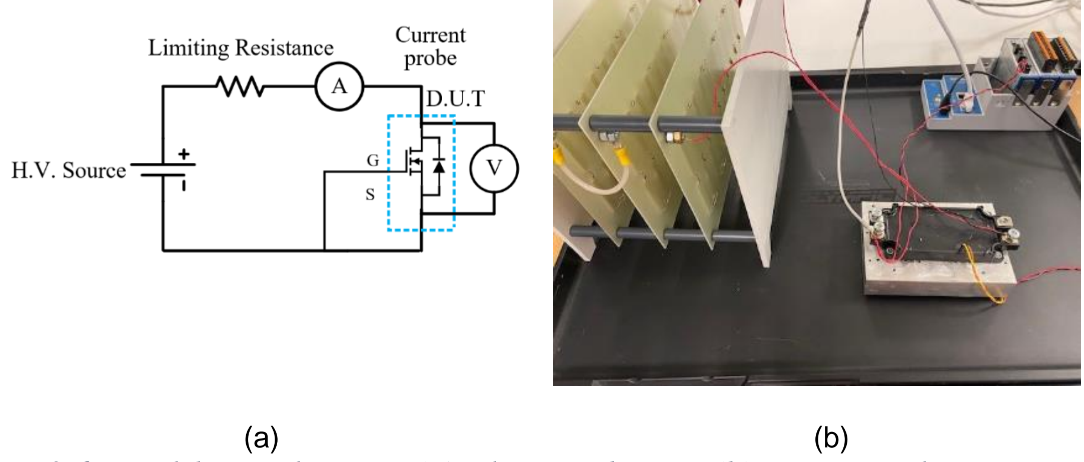
Fig. 3-5: Forward voltage testing procedure

3.3.1.2 Breakdown voltage test

The circuit diagram of the test rig and the experimental setup is shown in Fig. 3-6. The test arrangement consists of a dc power source and a resistance for current limiting or a precision current source. With the DUT reverse biased and its off-state gate-source voltage applied, the test changes the voltage levels while monitoring the current levels. The power supply current limit shall be set to the limit recommended in the datasheet for each device. Fig. 3-6 shows the equipment used in the test, which includes:

- Glassman high voltage EJ (3 kV – 200 mA),

- cDAQ 9185 with NI 9229 (sampling 25 kHz),
- NI LabVIEW 2018 SP1 to control the Genesys power supply,
- Platinum resistance temperature detector PT100 to measure case temperature,
- Measuring voltage directly across the device,
- Measuring current using a shunt resistor.



(a) (b)

Fig. 3-6: Breakdown voltage test (a) schematic diagram (b) experimental setup

The test procedure is illustrated in the flowchart shown in Fig. 3-7. The tests start with setting the current and the voltage values on the power supply. Once the power supply is switched on, the LabVIEW program is run to collect the measurements of the device characteristics. Using the readings from LabVIEW, the current passing through the device is calculated. Based on this, the breakdown voltage of the device under test is determined. This test is repeated multiple times at different temperatures from 77 K to 300 K.

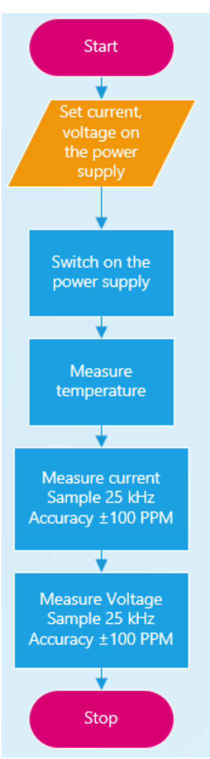
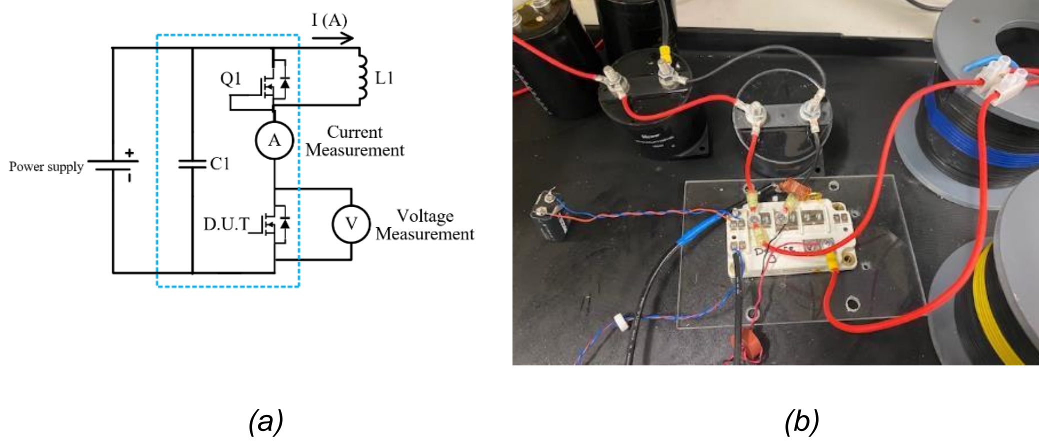


Fig. 3-7: Breakdown voltage testing procedure

3.3.2 Dynamic characteristic test

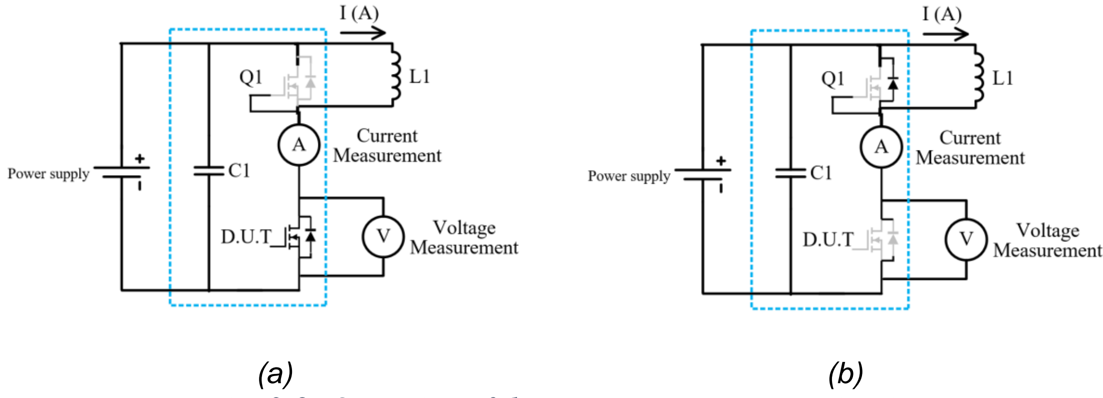
The double pulse test has been explained in [57],[58] and [85]. The test circuit, Fig. 3-8, consists of a dc power source, inductor, capacitor and MOSFET Q1. A supply voltage is used and the transient current during the turn-off of the diode is measured using the double-pulse technique. With this technique, as seen in Fig. 3-9 (a), initially Q1 is turned on to charge the inductor L1. Then, as seen in Fig. 3-9 (b), Q1 is turned off, forcing the inductor current to go through the diode. Finally, after the desired forward current has been established in the diode, Q1 is turned on to force the diode to recover in reverse. The test is done at cryogenic and room temperatures. Fig. 3-10 shows an ideal double pulse;

where the device is switched on and the current rises through the device and based on that the switching losses across the device are calculated.



(a) *(b)*

Fig. 3-8: Double pulse test circuit ((a) schematic diagram (b) experimental setup



(a) *(b)*

Fig. 3-9: Operation of the reverse recovery test circuit

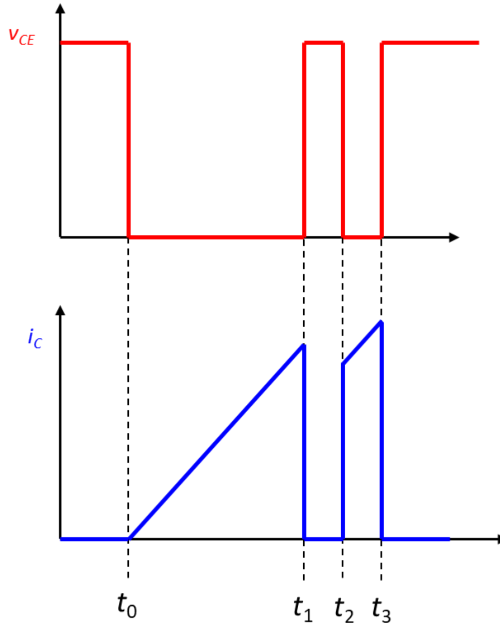


Fig. 3-10: Double pulse test waveforms

3.3.2.1 Energy losses calculation of DPT

To calculate the losses [83] has provided approximate switching waveforms as seen in Fig. 3-11, where based on the fall and rise time we can calculate the switching losses. The switching energy is calculated by integrating the power dissipated during the turn-on and turn-off of a semiconductor. The switching energy can be determined using the equation

$E_{on} = \int_{t_{I_{DS-10\%}}}^{t_{V_{DS-10\%}}} V_{DS} I_{DS} dt$, $E_{off} = \int_{t_{V_{DS-10\%}}}^{t_{I_{DS-10\%}}} V_{DS} I_{DS} dt$

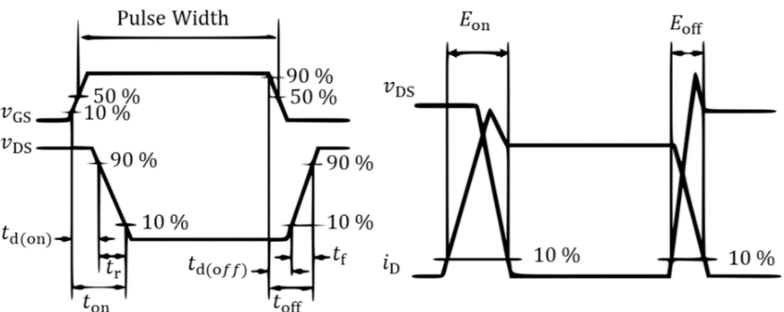


Fig. 3-11: Double pulse test waveform with turn-on and turn-off and switching energies of MOSFETs according to IEC 60747-8 [85]

3.3.2.2 Developing a current sensor for DPT

As current and voltage probes cannot normally operate at cryogenic temperature, wires from the test rig in the cold zone would need to be extended to provide access to probes. Most of the literature has had to use extended wires to measure the current through the device during the DPT at cryogenic temperature [1], [2] and [48]. However, as the length of the wires increases, parasitic inductances are introduced into the circuit [85]. Thus a bespoke arrangement for measuring the current in the DUT has been implemented.

A Tektronix TCP303 current probe was used for initial tests as its bandwidth is 15 MHz. However, some issues are present with this configuration:

- The bulk of the measuring head raises stray inductances in the loop required to accommodate it. This problem is exacerbated if currents in two parallel devices are to be measured;
- It cannot be used in cryogenic temperature zones as the packaging is not designed for that temperature;

- Its capacity is limited to 150 A (RMS). The peak current is limited to 500 A, but this is still too low for the required testing programme;
- There is a propagation delay (typically 53 ns) through the probe and amplifier system.

To address these issues, other current measurement techniques were investigated [86]. Table 3-1 shows a comparison of these techniques when considered for double pulse testing at cryogenic temperatures. From Table 3-1 it was deduced that using a current transformer is the most suitable solution.

Table 3-1 Candidate current measurement techniques.

	Sense resistor	Rogowski coil	Current transformer
Advantages	• Inexpensive to implement • Simple	• High accuracy bandwidth	• No integrator needed • Low sensitivity to stray fields • Low sensitivity to its location around the conductor
Disadvantages	• No inherent isolation • Need for a resistive element with a low-temperature coefficient	• Complicated compensation circuit • Not built for cryogenic temperature	• Requires a desaturation circuit

The equivalent circuit of the transformer is presented in Fig. 3-12. R_L is the load resistance and R_W is the winding resistance. N_1 and N_2 are the number of turns on the primary and the secondary side of the transformer, where N_1 is assumed to be one as the primary conductor is normally passed once through the core's aperture. L_m is the magnetising inductance at the primary side and L_{m2} is the magnetising inductance referred to the secondary side.

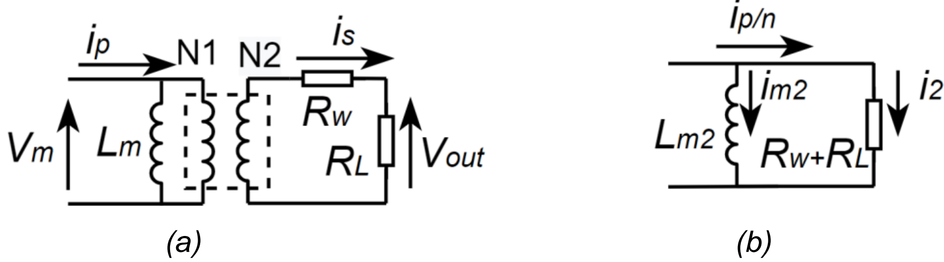


Fig. 3-12: Equivalent circuit of the current transformer, a) parameters of the primary and the secondary of the current transformer, b) equivalent circuit with parameters referred to the secondary side.

For measurements at cryogenic temperature, several requirements must be met:

- The peak magnetising current drawn must not be excessive. This fundamentally defines accuracy. The $i \times t$ product applied consequently applies a voltage-time product $v \times t$ across the CT's secondary winding N_2. $v \times t$ over the triangular current pulse is given by the area under the curve shown in Fig. 3-10 and:

$$vt = \frac{I_{pk}(R_w + R_L)(t_1 - t_0)}{2N_2} \quad (3\text{-}1)$$

The peak magnetizing current $I_{mag2(pk)}$ is given by dividing the $v \times t$ product by L_{m2}:

$$I_{mag2(pk)} = \frac{I_{pk}(R_w + R_L)(t_1 - t_0)}{2nL_{m2}} \quad (3\text{-}2)$$

The CT's secondary-side magnetising inductance L_{m2} is given by:

$$L_{m2} = \frac{\mu_0 \mu_r A_e N_2^2}{l_e} \quad (3\text{-}3)$$

- High bandwidth, ability to withstand $i \times t$ product needed in DPT test, low droop.
- Sufficient saturation flux density B_{sat} is needed to support the $i \times t$ product.

- Needed for low droop are high permeability of core and low secondary winding resistance R_w. Importantly here, the secondary winding resistance R_w falls with temperature. A low R_w is also needed to avoid saturation.
- Finding the peak flux density excursion (must be below B_{sat}) to withstand the required *i*x*t* product without saturation: from Faraday's Law

$$v = N\frac{d\Phi}{dt} \tag{3-4}$$

- *dB* is, therefore, calculated to identify if it is lower than the saturation flux density. Fig. 3-13 shows that B_r needs to be well below B_{sat} to avoid core saturation and measurement inaccuracies. However, some ancillary circuitry can be used to de-saturate the core to ensure correct measurements.

$$dB = \frac{Vt}{N_2 A_e} \tag{3-5}$$

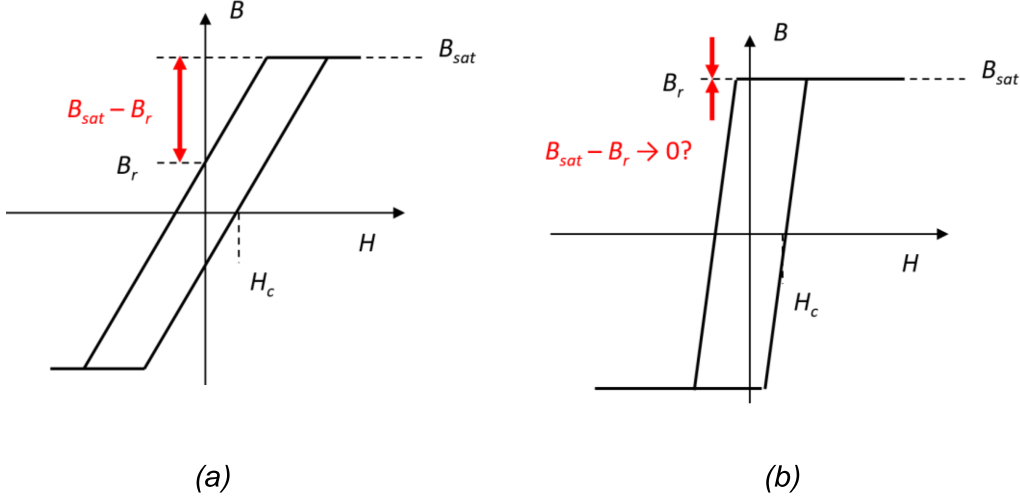


Fig. 3-13: B-H curves for magnetic cores; a) B_{sat} is much lower than B_r, b) B_{sat} is almost equal to B_r

Core material selection criteria are:

- High permeability;
- Sufficient saturation flux density B_{sat};
- Low losses (heating not problematic, but consequent current drawn by the resistive part of the magnetising branch may affect accuracy).

Material options for cryogenic temperature:

- Ferrite: judged to be unfeasible at 77 K from the literature review in Chapter 2.
- Nano-crystalline/ amorphous materials are viable contenders.

Based on a market and literature review, two different cores were found suitable for the cryogenic application, an amorphous and a nano-crystalline one. The comparison between the two cores can be seen in Table 3-2. From the table, it can be concluded that the amorphous core saturates at a lower current than the nano-crystalline. Hence, Nano-crystalline was chosen.

For the Hitachi amorphous core, the magnetising current was calculated using RT values, and with I_{pk} = 600 A, R_L = 1 Ω, and $t = t_1 - t_0$ = 10 µs, then $I_{mag2(\mathrm{pk})}$ = 873 µA. As the nominal secondary current is 6 A, then this represents an inaccuracy of 0.0146%.

For the Vacuumschmelze core the magnetising current was calculated using RT values, and with I_{pk} = 600 A, R_L = 1 Ω, and $t = t_1 - t_0$ = 10 µs, then $I_{mag2(\mathrm{pk})}$ = 393.1 µA. As the nominal secondary current is 6 A, then this represents an inaccuracy of 0.0066%.

Table 3-2: Comparison between available Amorphous and Nano-crystalline core

	Amorphous core	Nano-crystalline
Manufacturer / Part number	Hitachi/ MP1903M4AS	Vacuumschmelze/ T60006L2020W450
Dimensions	Inside Diameter: 11.86 mm Outside Diameter: 21.24 mm Height: 4.7 mm	Width: 22.60 mm Diameter 10.20 mm
Secondary winding resistance and inductance at 300 K	$R_{r/t}$= 611 mΩ $L_{r/t}$= 55.38 mH	$R_{r/t}$=1.284 Ω $L_{r/t}$=174 mH
Secondary winding resistance and inductance at 77 K	$R_{c/t}$=105 mΩ $L_{c/t}$=41.18 mH	$R_{c/t}$=190 mΩ $L_{c/t}$=229 mH
Desaturation	Requires compensation circuit for core resetting at 150 A	Requires compensation circuit for core resetting at 400 A
Inaccuracy	0.0146%.	0.0066%.
Core		

3.3.2.3 Testing current sensor performance

To assess the performance of the developed current transformer, the device was tested by comparing it with Tektronix TCP303 current probe, where the experimental results are shown in Fig. 3-14 where it can be concluded that the current transformer had a matching performance with the Tektronix probe in terms of magnitude. Also from Fig. 3-14, the current transformer is slightly faster than the Tektronix probe in terms of the current measurement, thus higher accuracy would be obtained when calculating the energy dissipated during switching.

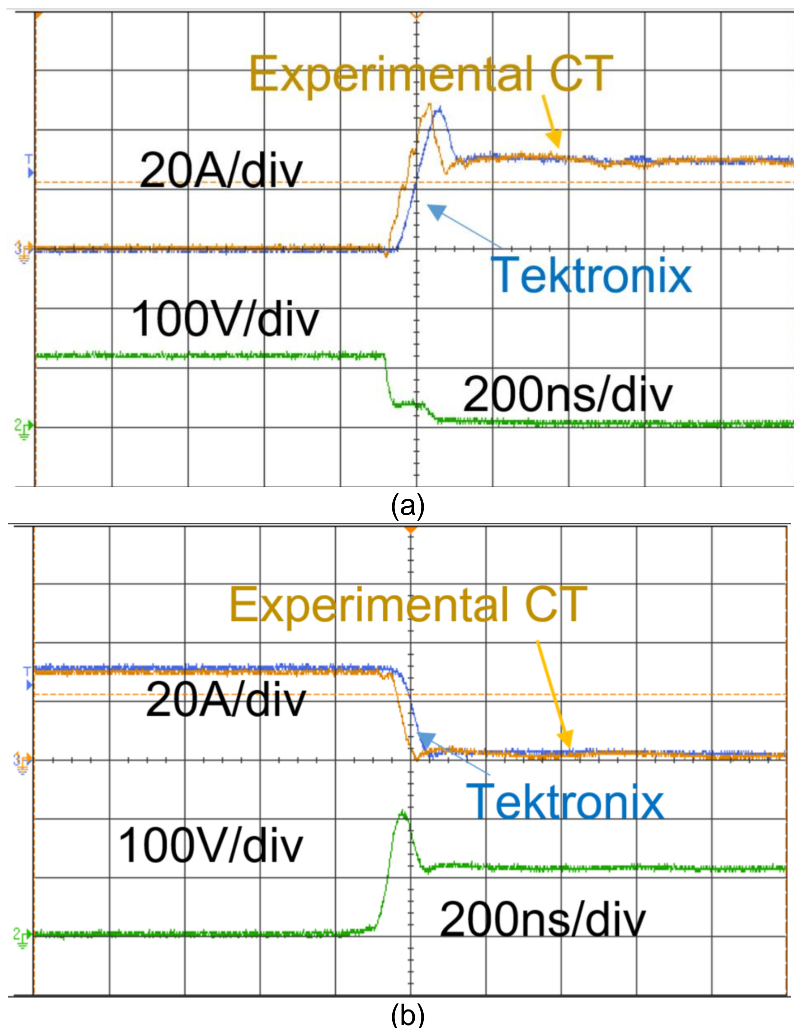


Fig. 3-14: Double pulse test to compare the performance of the developed current transformer and the Tektronix probe.

3.3.2.4 Desaturation circuit of current transformer

To increase the capacity of the current transformer and avoid current saturation, two different circuit configurations were investigated for desaturation, and both are shown in Fig. 3-15. In Fig. 3-15(a), current desaturation is established just by inserting a small bias current in the secondary side of the transformer, this increases the saturation point of the current transformer. Fig. 3-15 (b) shows the second current desaturation technique by

inserting a fast diode rectifier in the circuit [87], the oscillatory action between the current transformer's magnetising inductance and stray capacitance now resets the core flux to less than zero (slightly reverses it).

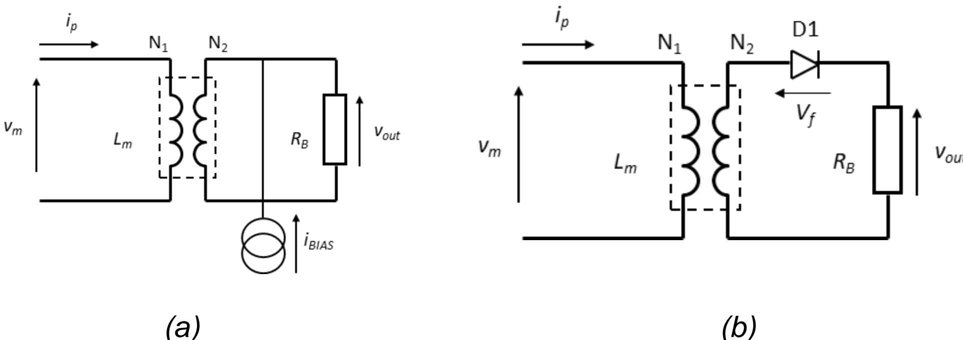


Fig. 3-15: Different desaturation circuits, a) using a resistor on the output, b) by inserting bias current on the secondary, c) by using a diode on the secondary side of the transformer

3.3.2.5 Designing of gate driver for large power modules

Large power modules such as MSCSM120AM02CT6LIAG and VS122PA690M7 require a high current gate driver with a negative gate bias for switching. This ensures that sufficient current can pass through the gate to ensure proper switching on and guarantees that the device is switched off during the switch-off period of the DPT. The design of the gate driver is as seen in Fig. 3-16, where a signal from a controller is applied and is isolated from the circuit using an optocoupler. The output of the optocoupler is then switched on to the gate driver, which can drive the device accordingly.

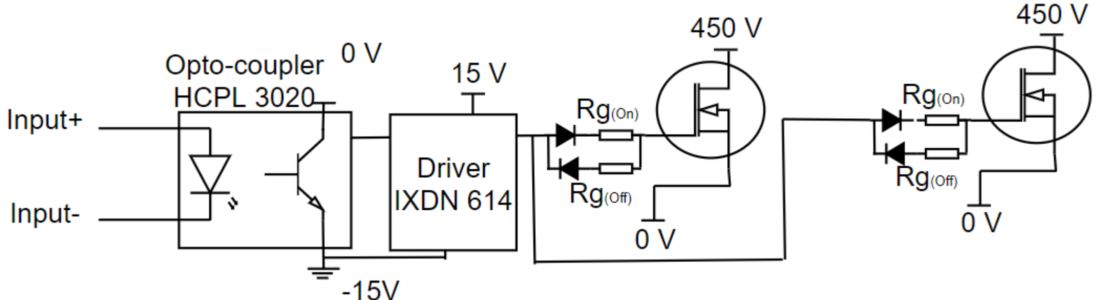


Fig. 3-16: Gate driver for power modules for the DPT circuit

3.3.3 Paralleling test

In this section, the paralleling test of devices is explained, where the test is done statically and no switching is involved. The main objective of this test is to ensure equal current sharing between semiconductors when they are connected in parallel.

Fig. 3-17 shows one set of static paralleling tests where a power supply (Genesys) with current capabilities of up to 1000 A was used to supply current to the load. Fig. 3-18 shows the algorithm of the test. The test is started by setting the current and voltage of the power supply, after which the supply is switched on and the current is measured through the shunt resistor in series with the devices and the voltage is measured straight onto the devices. The equipment used for that test is as follows;

- Isolated Genesys GSP10-1000dc power supply with current limitation,
- cDAQ 9185 with NI 9229 (sampling 25 kHz),
- NI LabVIEW 2018 SP1 to control the Genesys power supply,

- Shunt resistor (current sensor).

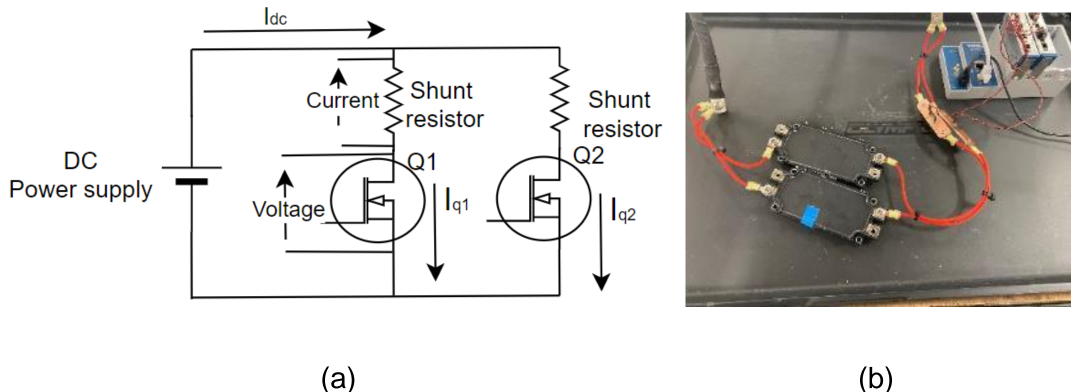


Fig. 3-17: Paralleling circuit a) schematic diagram, b) experimental setup

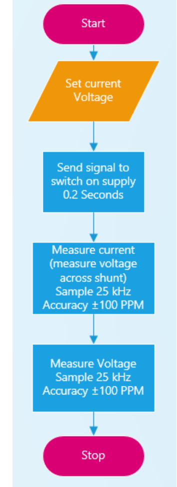


Fig. 3-18: Paralleling algorithm

3.4 Selection of devices

In this chapter two different sets of devices are tested to fulfil the requirements for superconducting applications; 1) a set of diodes with current and voltage ratings of 100 A and 1200 V were tested, and 2) testing MOSFETs and IGBTs of rating 1200V and 900A

at room and cryogenic temperature. These devices shown in Table 3-3 have been tested at room and cryogenic temperatures. Some of the tested devices do not meet the required ratings due to the limitation of current off-shelf technology capabilities. The tests were conducted twice, once at room temperature and a second time at a cryogenic temperature of 77 K. For the cryogenic testing, the DUT is placed in a container filled with liquid nitrogen.

Table 3-3: Selected devices for testing at cryogenic temperature

Device part number	Manufacturer	Technology	Rated voltage (V)	Rated current (A)
GB2X100MPS12-227	GeneSiC	SiC Schottky diode	1200	200
VS-QA250FA20	Vishay	Si Schottky diode	200	250
APT2X101D120J	Microsemi	Si Ultrafast diode	1200	93
VS-HFA220FA120	Vishay	Si Ultrafast diode	1200	110
MUR2X100A12	GeneSiC	Si Superfast diode	1200	200
DIM1500ESM33-TS000	Dynex	Si Superfast diode	3000	3000
IPW60R041C6	Infineon	Si CoolMOS	650	50
IKW75N65ET7XKSA1	Infineon	IGBT Trench/ FieldStop	650	80
AIKQ100N60CTXKSA1	Infineon	IGBT Trench/ FieldStop	600	160
FZ900R12KE4	Infineon	IGBT Trench/ Fieldstop	1200	900
VS122PA690M7	Vincotech	IGBT M7	1200	690
MSCSM120AM02CT6LIAG	Microchip	SiC MOSFET	1200	947

3.5 Characteristic test results

In this section, the characteristic test results are presented. The section will start with presenting the test results for the diodes, then MOSFET and finally the IGBTs. As mentioned earlier, two main characteristic tests are displayed in this section; 1) static tests, 2) dynamic tests and 3) paralleling tests for module packages.

3.5.1 Diodes

In this section, the characteristic tests of eight different diodes are reviewed.

3.5.1.1 Experiment results

a) GB2X100MPS12-227 (Silicon Carbide Schottky Diode):

Fig. 3-19 (a) shows the forward voltage performance of a Silicon Carbide (SiC) Schottky diode at cryogenic and room temperature, whereas seen from Fig. 3-19, the forward voltage has been shifted towards the right-hand side at cryogenic temperature. This shift means that switching losses increase at cryogenic temperatures. Fig. 3-19 (b) shows the breakdown test of the SiC diode at room and cryogenic temperature. It can be seen that the reduced temperature has no major effect on the breakdown voltage of the diode. Fig. 3-19 (b) shows the test result for the SiC type diode. From Fig. 3-19 (b) it can be seen there is a slight reduction in the current overshoot from 28.8 A to 26.6 A, a 5% decrease.

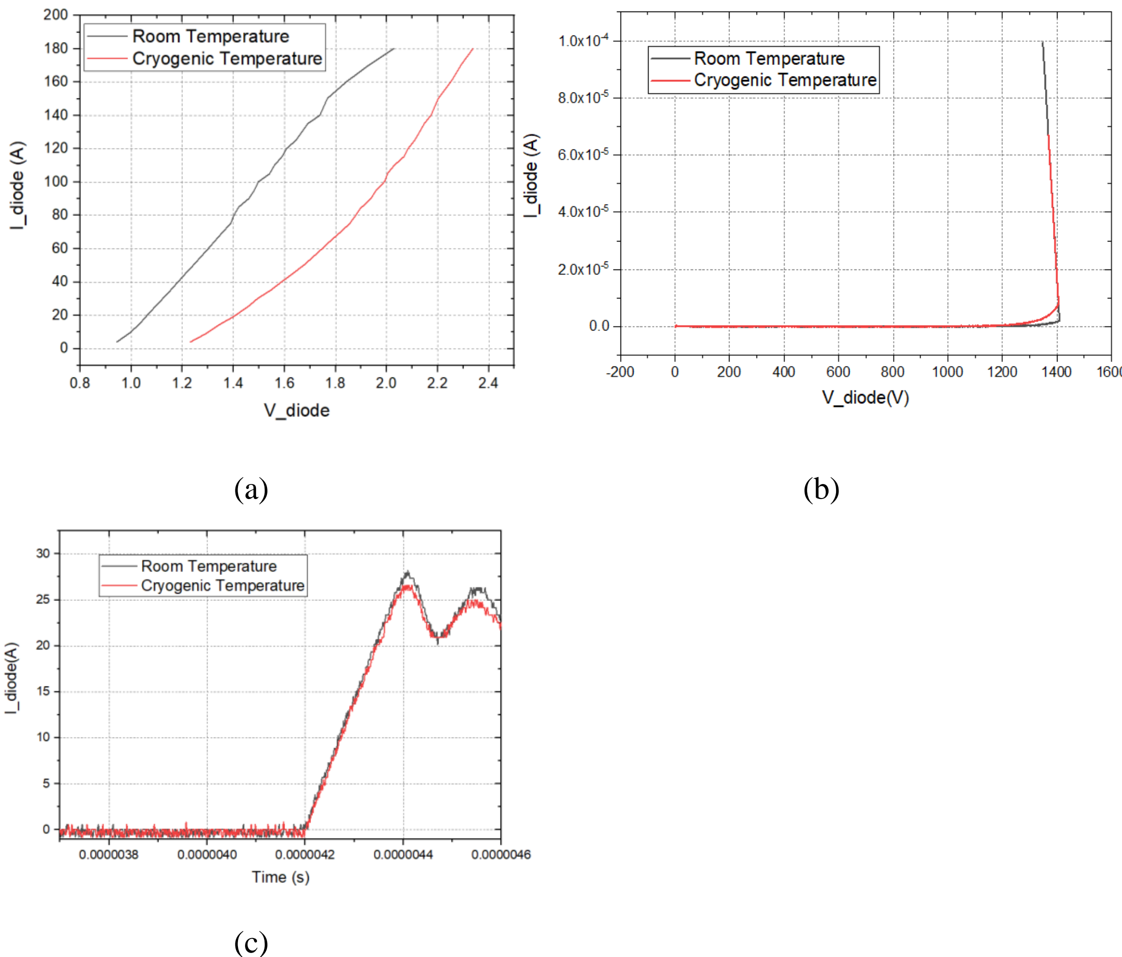


Fig. 3-19: GB2X100MPS12-227 test results at room and cryogenic temperature, a) forward voltage test, b) reverse breakdown test, and c) reverse recovery test.

b) VS-QA250FA20 (Silicon Schottky Diode):

Fig. 3-20 (a) shows the forward voltage performance of the Silicon (Si) Schottky Diode. As seen, the diode reacted similarly to that of the SiC Schottky diode, in that the forward voltage increased with the decrease of temperature. Fig. 3-20 (b) shows the breakdown voltage of a Silicon Schottky Diode. From the figure, the temperature does not have a significant effect on reducing the breakdown. The effect of change of temperature on

Silicon Schottky diode reverse recovery charge has had a minimal effect, shown in Fig. 3-20 (c). The peak reverse recovery current remained at 20.8 A.

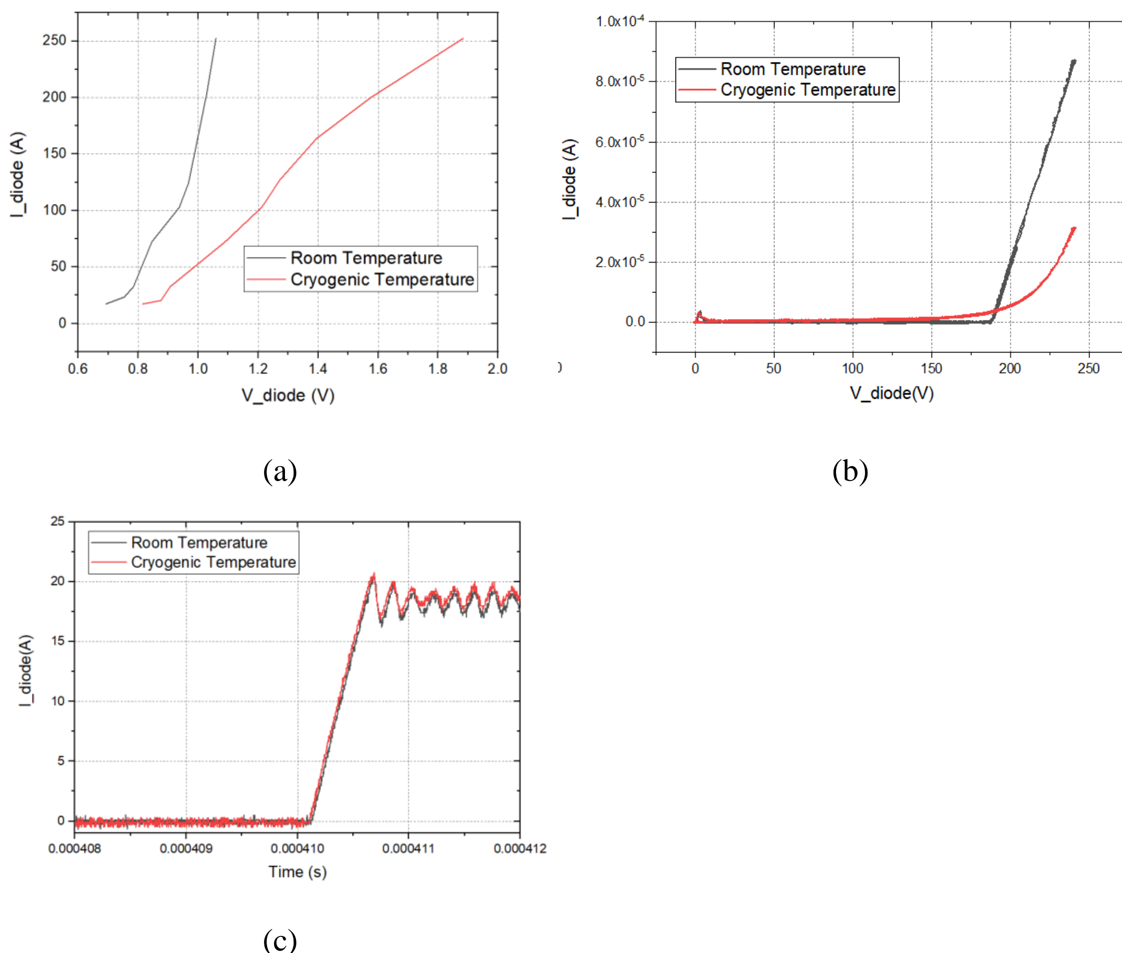


Fig. 3-20: VS-QA250FA20 test results at room and cryogenic temperature, a) forward voltage test, b) reverse breakdown test, and c) reverse recovery test.

c) APT2X101D120J (Silicon Fast Recovery Diode):

Fig. 3-21 shows the forward voltage of the Silicon Ultrafast Diode by Microsemi. It is seen that the forward voltage at cryogenic temperature is larger than the forward voltage at room temperature. However, the forward voltage at cryogenic temperature has a steeper

slope when compared to its room temperature counterpart Fig. 3-21 (a). Fig. 3-21 (b) shows the performance of the APT2X101D120J breakdown test. It can be seen that the breakdown voltage has decreased at cryogenic temperature. Fig. 3-21 (c) shows the performance of the APT2X101D120J Silicon type diode during a reverse recovery test. It can be seen that the current overshoot at the cryogenic temperature has been significantly reduced compared with the room temperature. The peak reverse current has dropped from 29 A to 25.8 A, an 11% decrease.

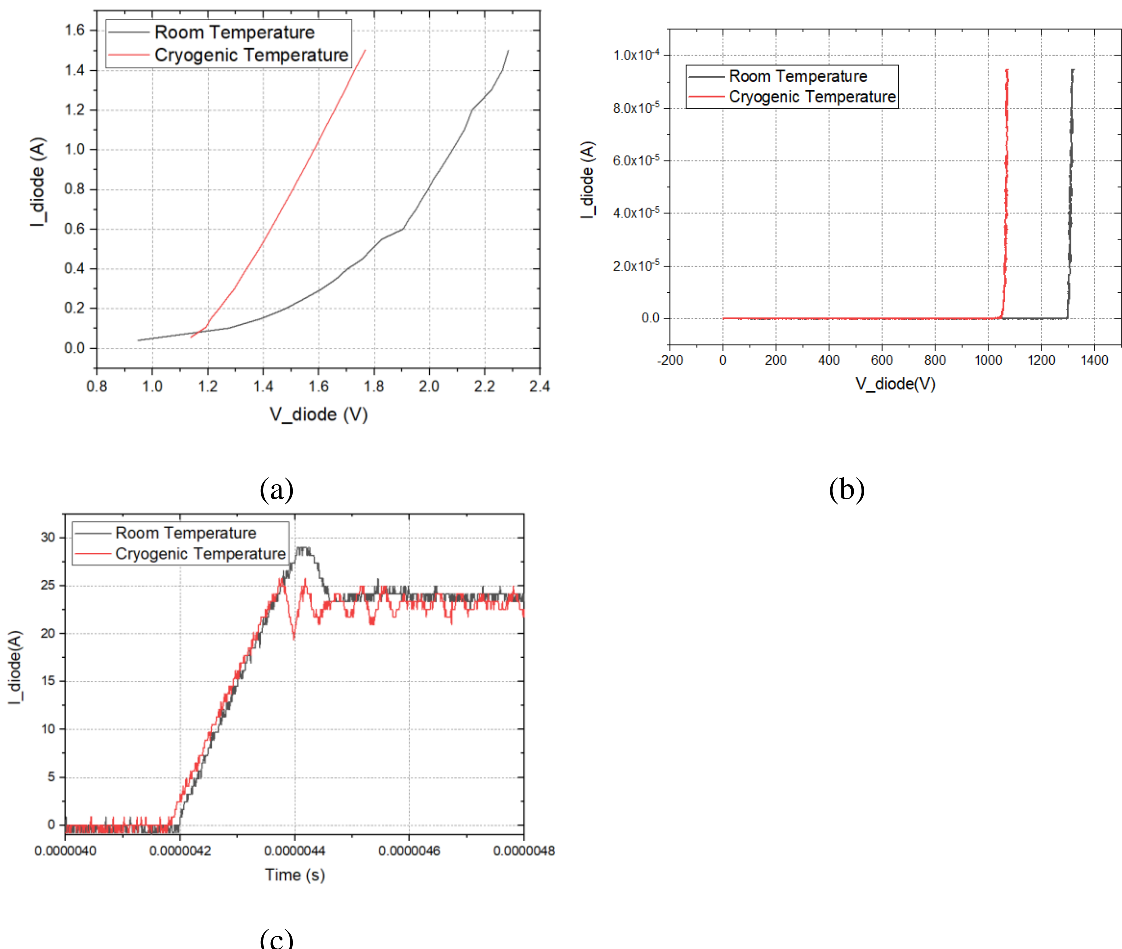


Fig. 3-21: APT2X101D120J test results at room and cryogenic temperature, a) forward voltage test, b) reverse breakdown test, and c) reverse recovery test.

d) VS-HFA220FA120 (Silicon Fast Recovery Diode):

Fig. 3-22 (a) shows the performance of the Vishay VS-HFA220FA120 Silicon Ultrafast Diode. It is seen that the forward voltage drop has decreased with the decrease in temperature. However, the forward voltage curve at cryogenic temperature has a steeper slope than its room temperature counterpart, showing similar results as the APT2X101D120J.

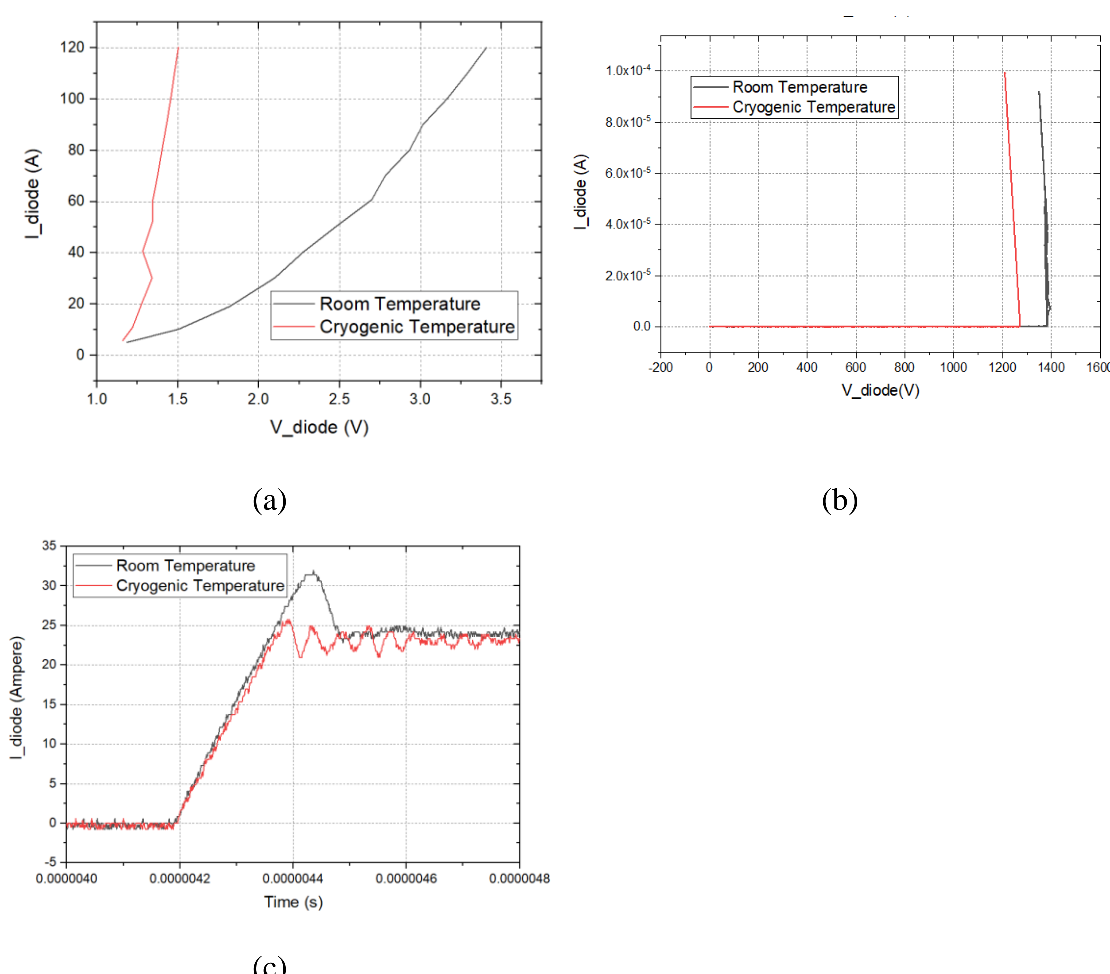


Fig. 3-22: VS-HFA220FA120 test results at room and cryogenic temperature, a) forward voltage test, b) reverse breakdown test, and c) reverse recovery test.

Fig. 3-22 (b) shows the performance of a Silicon Ultrafast Diode. The breakdown voltage at cryogenic temperature has decreased. This is similar to what has happened to the APT2X101D120J type diode discussed previously. Fig. 3-22 (c) shows the performance of the VS-HFA220FA12 diode during the reverse recovery test. There has been a significant reduction in the overshoot current during switching. The peak current has decreased from 32.8 A to 26.1 A, a 20% decrease.

e) MUR2X100A12 (Silicon Fast Recovery Diode)

Fig. 3-23(a) shows the performance of Ultrafast Silicon Diode at both cryogenic and room temperature. It can be seen that there is no major difference in the performance of the diode at the cryogenic and room temperature. Fig. 3-23 (b) shows the performance of MUR2X100A12 where the breakdown voltage has been reduced with the decrease of temperature, shifting the breakdown characteristic curve toward the left. Fig. 3-23 (c) shows the reverse recovery test for the MUR2X100A12. There has been a significant improvement in the performance of the diode in regards to the decrease of the current overshoot. The peak reverse current has decreased from 32.1 A to 25.8 A, a 20 % decrease.

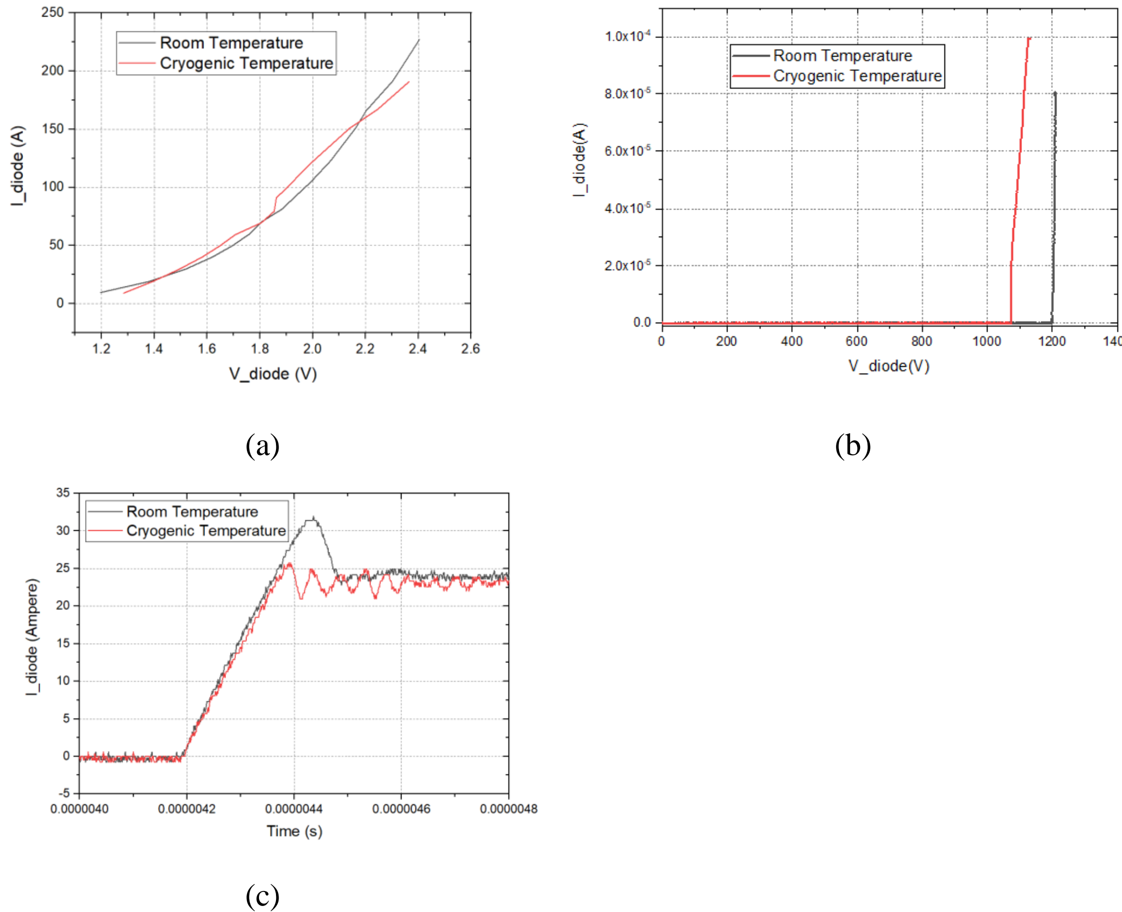


Fig. 3-23: MUR2X100A12 test results at room and cryogenic temperature, a) forward voltage test, b) reverse breakdown test, and c) reverse recovery test.

f) DSEI30-06A (Fast Recovery Epitaxial Diode)

Fig. 3-24 (a) shows the forward voltage test of a FRED diode. It can be seen that the forward voltage increases with the decrease of temperature. A similar effect to that of the Schottky Diode. Fig. 3-24 (b) shows that operating the diode at cryogenic temperature has had little effect on the breakdown voltage of the diode. In Fig. 3-24 (c), the FRED type diode DSEI 30-06A reverse recovery seems not to have been affected by the decrease in temperature. The change of the peak reverse current is too small to measure.

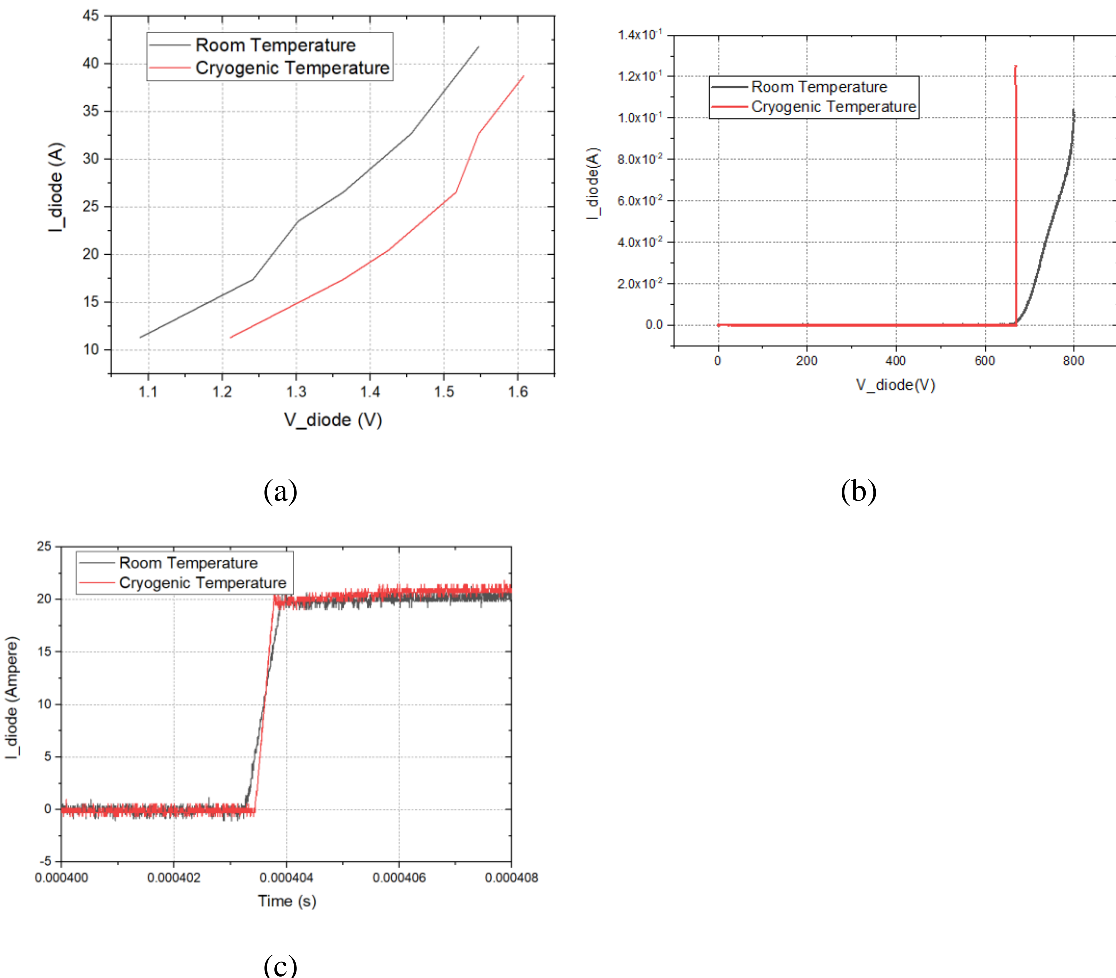
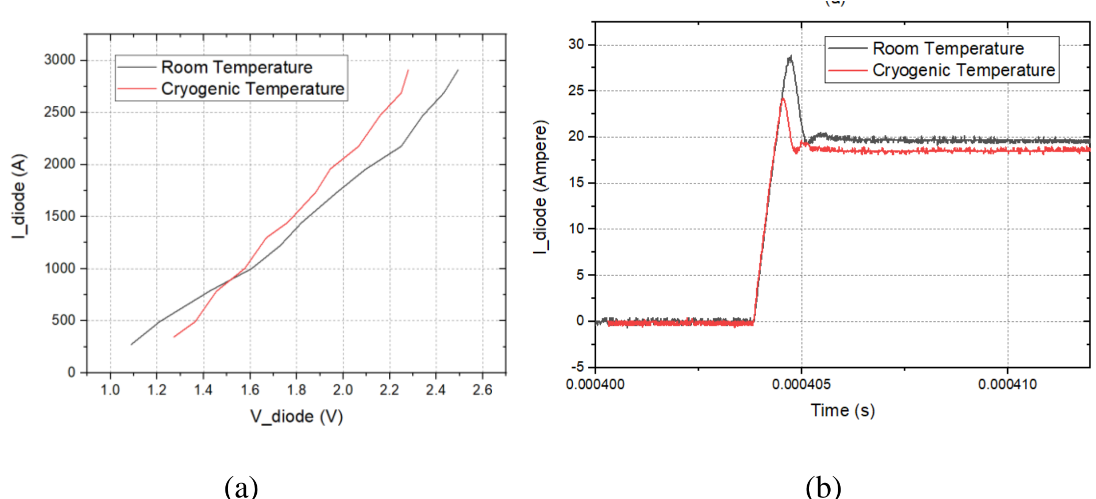


Fig. 3-24: DSEI30-06A test results at room and cryogenic temperature, a) forward voltage test, b) reverse breakdown test, and c) reverse recovery test.

g) DIM1500ESM33-TS000 (Silicon Fast Recovery Diode):

Fig. 3-25 shows the performance of the DIM1500ESM33-TS000 diode. Fig. 3-25 (a) shows the forward voltage where, as seen, there is a breakeven point, where the performance of the diode at cryogenic temperature improves after 1.55 V. This case is similar to the other Silicon Fast Recovery Diode previously discussed. This module was not tested for breakdown voltage due to the limited capability of the current high voltage

supply of 3kV. The peak reverse recovery current of the Dynex DIM1500ESM33-TS000 diode has improved with the decrease of temperature, going down from 29 A to 24 A (17%), as seen in Fig. 3-25(b).



(a) (b)

Fig. 3-25: DIM1500ESM33-TS000 test results at room and cryogenic temperature, a) forward voltage test and b) reverse recovery test.

3.5.1.2 Summary of diode experimental results

As shown in Table 3-4 a comparison has been done between the diodes at cryogenic and room temperature. From the table, Schottky diodes, both SiC and Si, have shown an increase in the forward voltage cryogenic temperature. Hence, Schottky diodes have higher conduction losses at cryogenic temperatures. Si Ultrafast diodes have shown reduced losses at cryogenic temperature since their forward voltage decreases with the decrease of temperature. The results of the table largely agree with the previous results mentioned in the literature review in Chapter 2.

Table 3-4: Comparison of the performance of diode devices at room and cryogenic temperature

	GB2X100MPS12-227 GeneSiC SiC Schottky		**VS-QA250FA20 Vishay Si Schottky**		**APT2X101D120J Microsemi Si Ultrafast**		**HFA220FA-120 Vishay Si Ultrafast**		**MUR2X100A12 GeneSiC Si Superfast**		**DSEI30-06A IXYS FRED diode**		**DIM1500ESM33-TS000 Si Ultrafast**	
Temperature (CT=77K)	RT	CT	RT	CT	RT	CT	RT	CT	RT	CT	RT	CT	RT	CT
$V_{forward}$ **(V)**	1.49	1.99	1	3.16	2.08	1.5	3.16	1.46	1.9	1.8	1.16	1.3	1.8	1.8
% Change	+33%		+60%		-24%		-53%		-5%		+12 %		-2.7%	
[Current used for $V_{forward}$ **test (A)]**	[100]		[200]		[100]		[100]		[100]		[15]		[1500]	
V_{BR} **(V)**	1400	1400	220	240	1300	1000	1400	1300	1200	1080	660		-	-
% Change	0%		+9%		-23%		-7%		10%		0%		-	
Q_{rr} **charge (nC)**	168	112	104	128	28	1.62	102	5.43	192	6.56	-	-	119	507
% Change	-33%		23%		-94%		-94%		-96%		-		-57.38%	
Peak transient current (A)	28.2	26.6	20.8	32.8	25.8	25.8	32.8	26.1	32.1	25.8	-	-	28	25

3.5.1.3 Theoretical analysis of diode forward voltage results

In this section, the theoretical analysis of the experiment results done on diodes is presented. The main purpose is to identify how the different parameters of the diode change with the temperature. To characterise the *I-V* characteristic of PN and Schottky diodes the Shockley equation (3-6) is used [35],[88]. By using curve fitting of the experimental values with the Shockley equation, we can extrapolate the diodes resistance and ideality factor at room and cryogenic temperature. The Shockley Equation is defined as follows;

$$I_{Diode} = I_S(e^{\frac{qV_{Diode} - I_{Diode}*R_S}{nkT}} - 1) \quad (3\text{-}6)$$

- I_{Diode} : is the diode forward current.

- V_{Diode}: is the diode forward voltage.
- I_s : is the diode saturation current, which is equal to the leakage current when the diode is placed into reverse bias.
- R_s : is the diode's resistance.
- n is an ideality factor that measures how much the diode is non-ideal: the higher the n, the less ideal the diode.
- V_T is a constant which is the thermal voltage of the diode. $V_T = \frac{k*T}{q} = 8.265 \times 10^{-5} \times Temp$

Another important characteristic of the Schottky diodes is the barrier height can be calculated through the following equation [88]. Fig. 3-26 shows the barrier height, where the value depends on the semiconductor and the metal types. A Schottky diode consists of a metal element and a semiconductor element. When the metal element is in contact with the semiconductor. As seen in Fig. 3-26 the Fermi levels are plotted; which is the energy level which is occupied by the electron orbital at 0 K temperature in the two materials must be equal at thermal equilibrium. In addition, the vacuum level must also be continuous. These two requirements determine a unique energy band diagram for the contact. The resulting band bending at the interface creates a potential barrier known as the Schottky barrier [89]. The barrier height is shown in Fig. 3-26, Φ_{Bn} is simply the difference between the metal work function, Φ_m, (the energy difference between the metal Fermi level and the vacuum level) and the electron affinity of the semiconductor (the difference between the semiconductor conduction band edge and the vacuum level). E_C, E_V, and E_F denote the conduction band minimum, valence band maximum,

and Fermi level, respectively. Φ_m is the metalwork function, χ_s the semiconductor electron affinity, ω the thickness of the space-charge layer, eV_s the potential barrier, and Φ_B the potential barrier height.

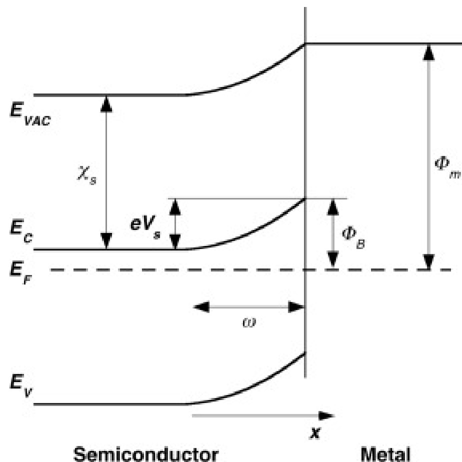


Fig. 3-26: Schematic representation illustrating a Schottky barrier at a metal-semiconductor interface [89].

The barrier height is given by Equation (3-7), where it is directly related to the temperature and inversely related to the breakdown leakage current.

$$\emptyset_{Bn} = \frac{kT}{q} \ln\left(\frac{A^{**}T^2}{I_0}\right) \text{ (Barrier Height)} \qquad (3\text{-}7)$$

- A^{**} is the Richardson constant where, $A^{**} = 110$ for Silicon, 146 for Silicon (Si) Carbide (SiC);
- T is the temperature;
- I_0 is the reverse diode current

From the experimental results, voltages and currents have already been obtained at room and cryogenic temperatures. Therefore the only missing variables in the equation are the n and R_s. Curve fitting has been done for two ultrafast diodes and two Schottky diodes. This is done by a MATLAB program for the initial iteration R_s has been set at an initial value and according to that n is extracted using the Shockley equation by substitution I_{Diode} and V_{Diode} by experimental point, then the data points for the voltages are obtained. In the program, the error from the difference between the V_{Diode} experimental curve and the V_{Diode} expected curve calculated and if the error is still big the iteration is repeated for a different value of R_s. The algorithm of the MATLAB program is as in Fig. 3-27. The root mean squared error (RMSE) is calculated for each step to reach the minimum error possible.

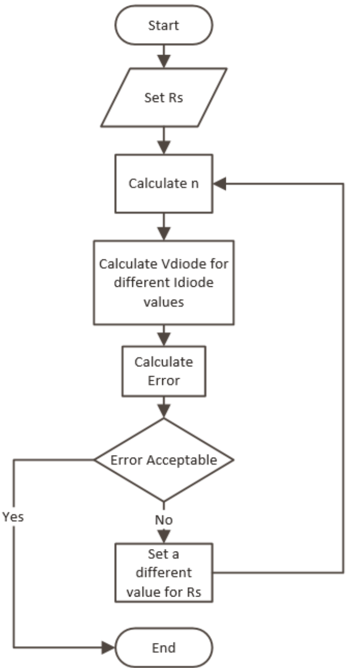


Fig. 3-27: Algorithm for MATLAB code to calculate the best values for R_s and n

a) APT2X101D120J (Si Ultrafast)

To get the best-fit curves as seen in Fig. 3-28, the ideality factor n was determined to be 2.819 at room temperature and 9.19 at cryogenic temperature. As for R_s, the best values were 6.324 mΩ at room temperature and 3 mΩ at cryogenic temperature. Fig. 3-28 shows the plot of RMSE against different values of R_s for (c) at room temperature and (d) at cryogenic temperature.

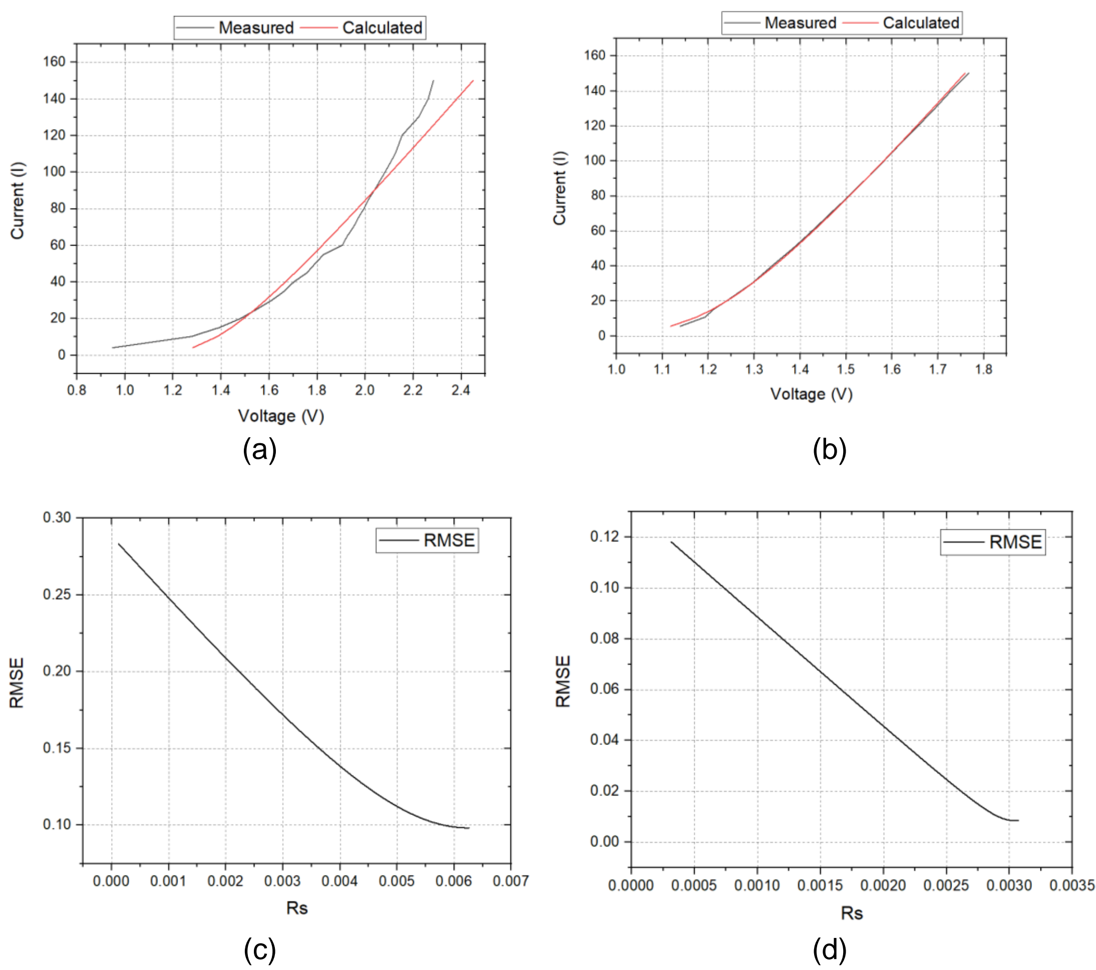


Fig. 3-28 Curve Fitting for APT2X101D120J Ultra-Fast diode at; (a) room temperature (300 K) (b) cryogenic temperature (77 K), RMS error for curve fitting for APT2X101D120J Ultra-Fast diode at; (c) room temperature (300 K) (d) cryogenic temperature (77 K)

b) VS-HFA220FA120 (Si Ultrafast)

The ideality factor n that best matched the curves in Fig. 3-29. The ideality factor calculated was 3.316 for room temperature and 9.092 for cryogenic temperature. As for the diode resistance R_s, the value that best matched was 15.5 mΩ at room temperature and 2.53 mΩ at cryogenic temperature. Fig. 3-29 shows RMSE vs R_s for (c) at room temperature and (d) at cryogenic temperature.

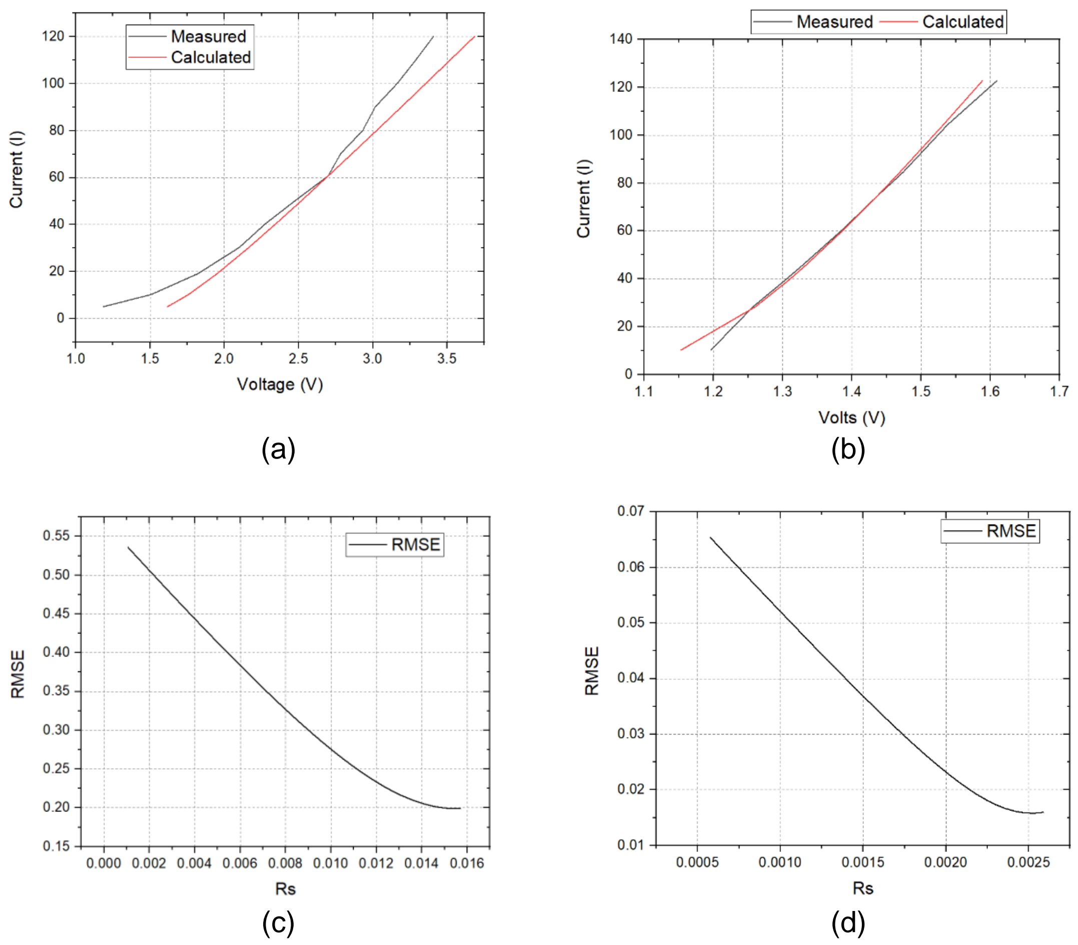
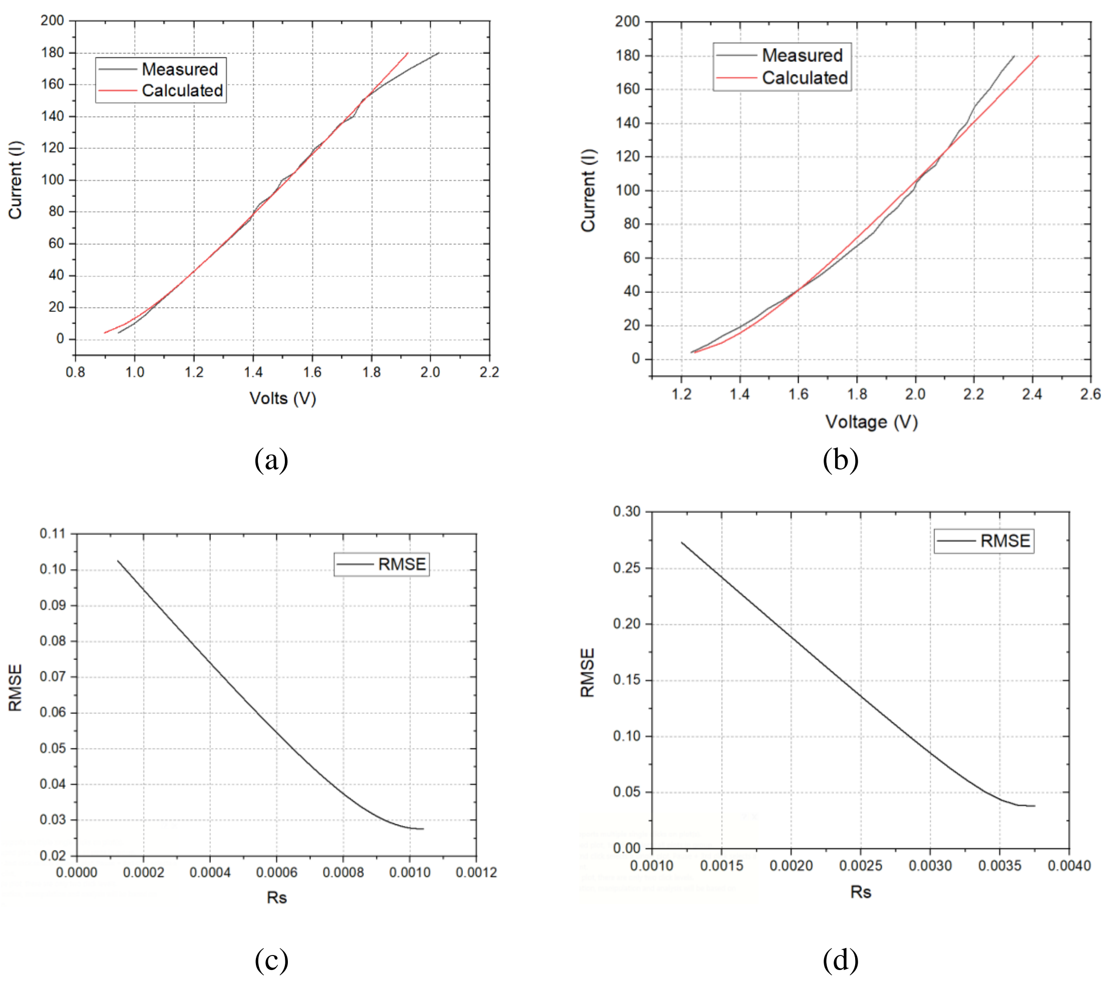


Fig. 3-29: Curve Fitting for VS-HFA220FA120diode at; (a) room temperature (300 K) (b) cryogenic temperature (77 K) and RMS error for the curve fitting for VS-HFA220FA120 diode at; (c) room temperature (300 K) (d) cryogenic temperature (77 K)

c) GB2X100MPS12-227 (SiC Schottky)

It was calculated that the ideality factor n that best fit the curves in Fig. 3-30 was 1.96 for room temperature and 10.7 for cryogenic temperature. The corresponding best values for the diode resistance R_s was $4.74m\Omega$ and $5.15m\Omega$ for room and cryogenic temperature respectively.



(a) (b)

(c) (d)

Fig. 3-30: Curve fitting for GB2X100MPS12-227 Diode at; (a) room temperature (300 K) (b) cryogenic Temperature (77 K), RMS error for curve fitting for GB2X100MPS12-227 diode at; c) room temperature (300 K) d) cryogenic temperature (77 K)

The calculated barrier height $\emptyset_{Bn}$ was 0.834 at room temperature and 0.20502 at cryogenic temperature. Fig. 3-30 shows the RMSE versus R_s for (c) at room temperature and (d) at cryogenic temperature.

d) VS-QA250FA20 (Si Schottky)

The ideality factor n that yields the best fitting curve as seen in Fig. 3-31 was 1.47 for room temperature and 5.97 for cryogenic temperature.

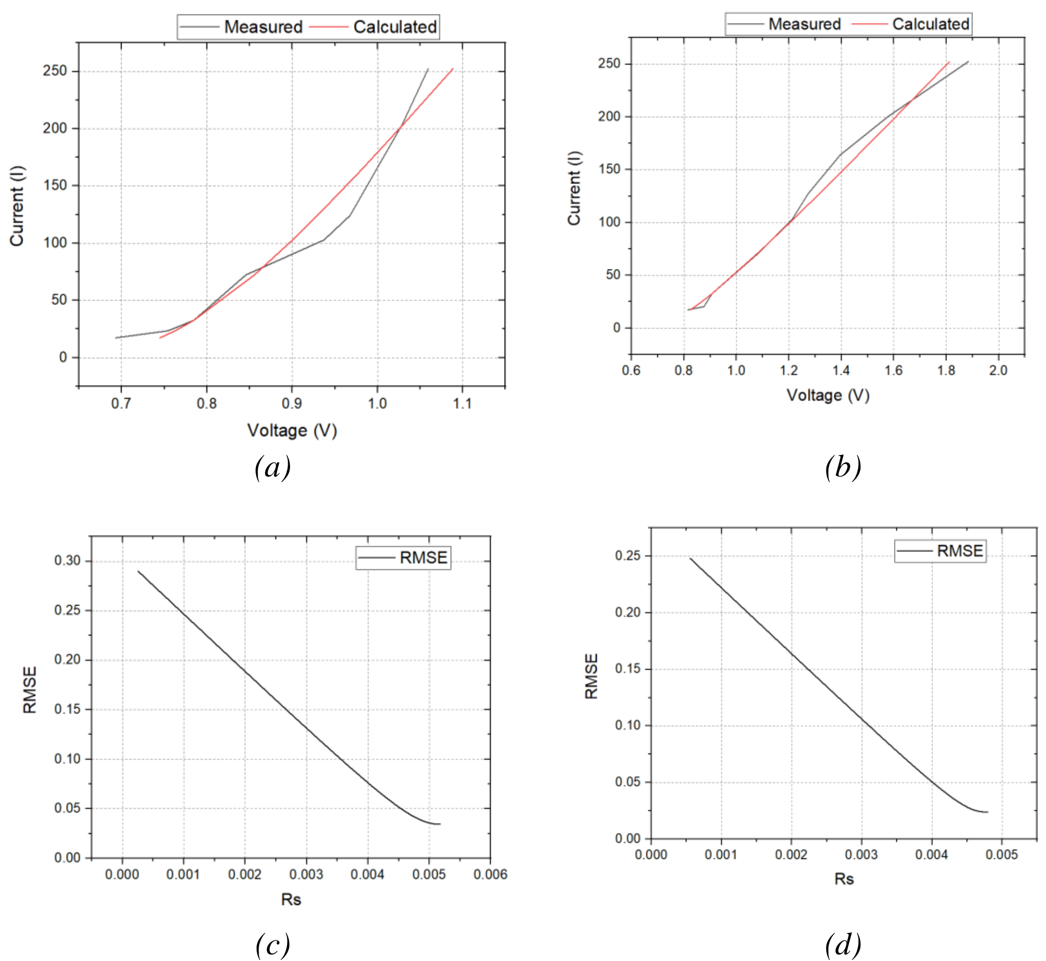


Fig. 3-31: Curve fitting for GB2X100MPS12-227 diode at (a) room temperature (300 K) (b) cryogenic temperature (77 K) RMS error for curve fitting for GB2X100MPS12-227 diode at (c) room temperature (300 K) (d) cryogenic temperature (77 K)

The corresponding diode resistances were 1.03 mΩ and 3.75 mΩ. The calculated barrier height $\emptyset_{Bn}$ was 0.838 at room temperature and 0.197 at cryogenic temperature. Fig. 3-31 shows the RMS error curve drawn against the different values of resistances for (c) at room temperature and (d) at cryogenic temperature.

e) Results summary

In this section, an analysis of the forward voltage experimental results has been done. The analysis was carried out by implementing curve fitting to extract the parameters of different types of diodes. Table 3-5 and Table 3-6 shows the results for Si and SiC Schottky diodes. Where both types of Schottky diodes have shown that their resistances and their ideality factor increase with the decrease in the temperature and their barrier height decreases with the decrease of temperature.

Table 3-5: Curve fitting results for APT2X101D120J and VS-HFA220FA120

	APT2X101D120J		**VS-HFA220FA120**	
Parameter	Room Temp	Cryogenic	Room Temp	Cryogenic
$\boldsymbol{n}$ (Ideality Factor)	2.819	9.19	3.316	9.092
$\boldsymbol{R_s}$ (Diode Resistance)	$6.324 m\Omega$	$3.04 m\Omega$	$15.5 m\Omega$	$2.53 m\Omega$
Number of Iteration	299	90	141	37
Root Mean Square Error (RMSE)	0.1576	0.0084	0.199	0.0158
R squared Error	0.822	0.998	0.99	0.97

This analysis has limitations as it exclusively uses Shockley's equation to extract the parameters and fit the best curve to the experimental values. The major focus of this

analysis is to understand the general trend at which *Rs* and *n* move concerning the decrease in temperature.

Table 3-6 show the curve fitting results. As seen in Table 3-5, the Ultrafast diodes APT2X101D120J and VS-HFA220FA120 have been shown to decrease their resistance with the decrease in temperature. Also, the Ultrafast diodes have shown an increase in ideality factor with the decrease in temperature.

Table 3-6 shows the results for Si and SiC Schottky diodes. Where both types of Schottky diodes have shown that their resistances and their ideality factor increase with the decrease in the temperature and their barrier height decreases with the decrease of temperature.

This analysis has limitations as it exclusively uses Shockley's equation to extract the parameters and fit the best curve to the experimental values. The major focus of this analysis is to understand the general trend at which *Rs* and *n* move concerning the decrease in temperature.

Table 3-6: Curve fitting results for GB2X100MPS12-227 and VS-QA250FA20

	GB2X100MPS12-227 (SiC)		**VS-QA250FA20 (Si)**	
Parameter	Room Temp	Cryogenic	Room Temp	Cryogenic
$\emptyset_{Bn}$ (Barrier Height)	0.834	0.205	0.838	0.197
$\boldsymbol{n}$ (Ideality Factor)	1.96	10.68	1.47	5.97
$\boldsymbol{R_s}$ (Diode Resistance)	$4.74m\Omega$	$5.15m\Omega$	$1.03m\Omega$	$3.75m\Omega$
Number of iterations	79	198	78	24
Root mean square error (RMSE)	0.153	0.03	0.027689	0.07
R squared Error	0.8045	0.99	0.87134	0.96

3.5.2 MOSFET

In this section, two MOSFETs have been tested at room and cryogenic temperatures.

a) IPW60R041C6 (Si CoolMOS MOSFET)

Fig. 3-32 (a) shows that the forward voltage decreases with the decrease of temperature. Fig. 3-32 (b) shows the breakdown voltage at room and cryogenic temperatures. As seen in Fig. 3-32, the breakdown voltage decreased from 640 V to almost 480 V.

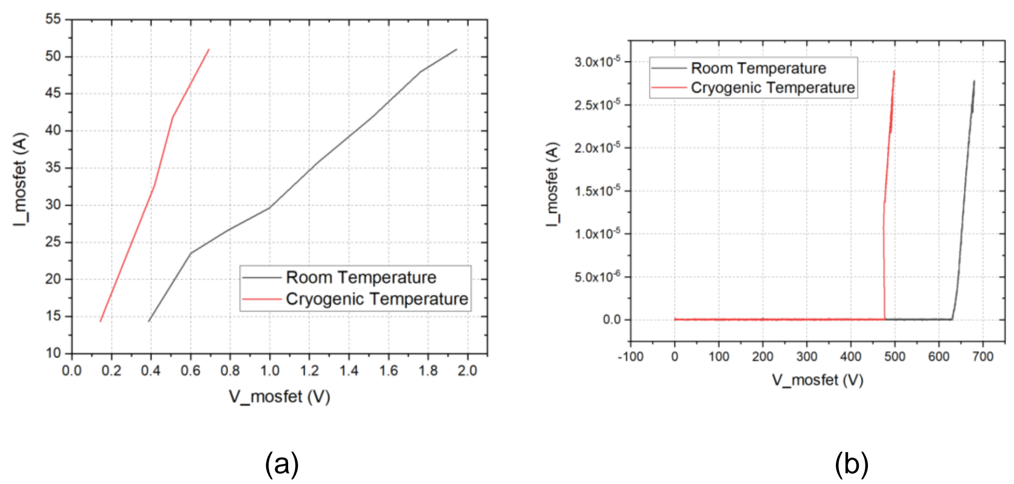


Fig. 3-32: Testing of IPW60R041C6 at room and cryogenic temperature (a) forward voltage test (b) breakdown voltage test

b) MSCSM120AM02CT6LIAG (SiC MOSFET)

Fig. 3-33 (a) shows that the forward voltage decreases with the decrease of temperature. The MOSFET resistance at different temperatures and gate-source voltages is presented in Fig. 3-33 (b). From Fig. 3-33 it can be seen that with the decrease of temperature the on-resistance of the device increases. Fig. 3-33 (c) shows the breakdown voltage of the SiC MOSFET at different temperatures between 300K and 77K. It is seen clearly with the decrease in temperature there is a decrease in the breakdown voltage. Fig. 3-33 (d) shows

the reverse recovery of the SiC MOSFET. From Fig. 3-33 it is seen that the reverse recovery time increased and hence the reverse recovery losses increased with the decrease in temperature.

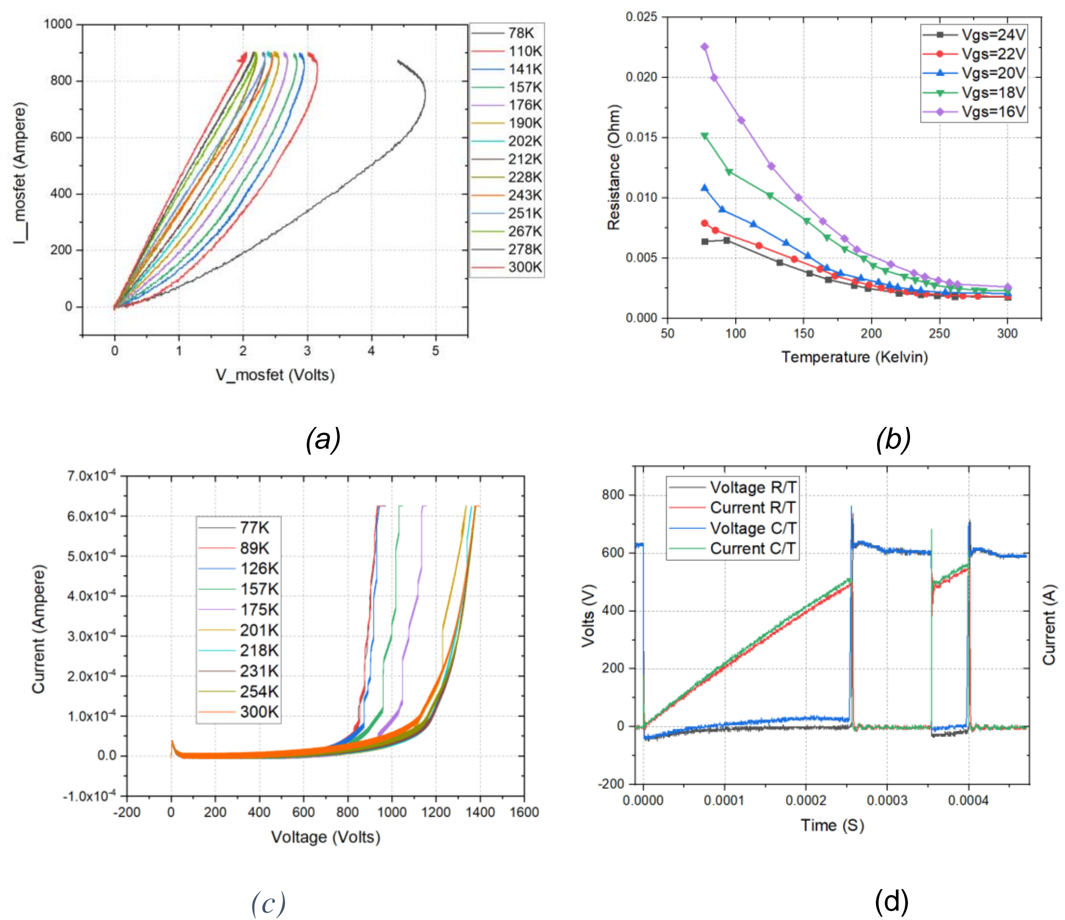


Fig. 3-33: Characteristics tests for MSCSM120AM02CT6LIAG; a) forward voltage, b) on-resistance, c) breakdown voltage, and d) double pulse test

Fig. 3-34 shows the experiment of MSCSM120AM02CT6LIAG at room and cryogenic temperature. From the experiment, it can be seen that the SiC MOSFET device has good current sharing characteristics at room temperature, where both devices carry almost equivalent current. However, at cryogenic temperature, the current sharing of the device

becomes worse, as seen in Fig. 3-34 (c) where one MOSFET carries 30A more than the other device.

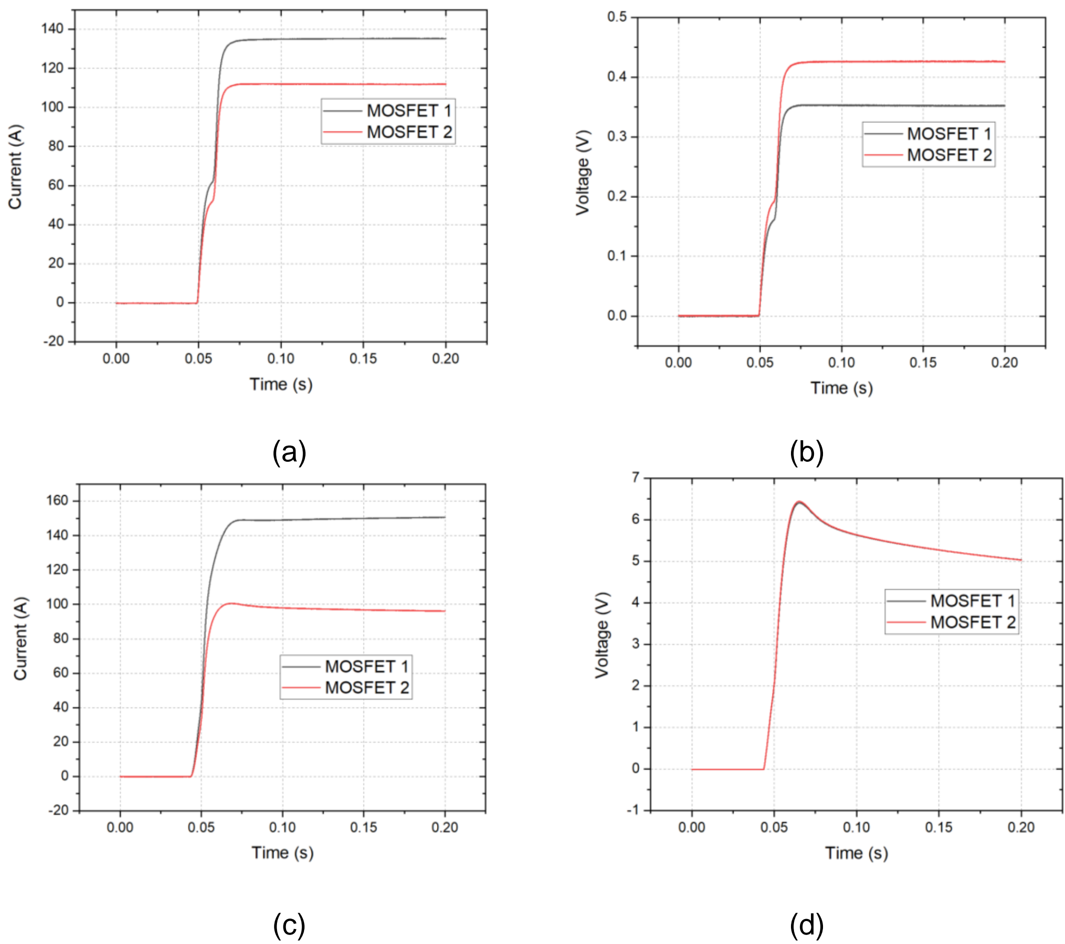


Fig. 3-34: Paralleling test experiment results at room temperature for (a) and (b) and cryogenic temperature for (c) and (d)

Table 3-7 summarises the experimental results for the Infineon IPW60R041C6 and MSCSM120AM02CT6LIAG devices. From the table, it is seen, that with the decrease in temperature the CoolMOS has experienced a decrease in the on-resistance. The breakdown voltage also decreased with the temperature. Microchip MSCSM120AM02CT6LIAG SiC MOSFET has shown an increase with the decrease of

temperature, meaning there are higher losses at cryogenic temperature. The breakdown voltage of the MSCSM120AM02CT6LIAG decreases with the decreased temperature. MSCSM120AM02CT6LIAG has shown an increase in the switching time with the increase in temperature. The results are consistent with the literature

Table 3-7 Summary of experiment results for IPW60R041C6 and MSCSM120AM02CT6LIAG

	IPW60R041C6 **Infineon** **CoolMOS MOSFET**		**MSCSM120A-** **M02CT6LIAG** **Microchip / Microsemi** **SiC MOSFET**	
Temperature (RT = 300 K, CT = 77 K)	Room temperature	Cryogenic temperature	Room temperature	Cryogenic temperature
R_{DS} **(mΩ)**	36.7	13.2	2.1	6.64
% Change	+33%		+216%	
[Current used for $V_{forward}$ test (A)]	[35]		[480]	
V_{BR} **(V)**	650	480	1250	915
% Change	-26%		-26.8%	
Switching off time (ns)	N/A		710	1980
% Change	N/A		+178%	
Switching on time (ns)	N/A		100	158
% Change	N/A		+58%	

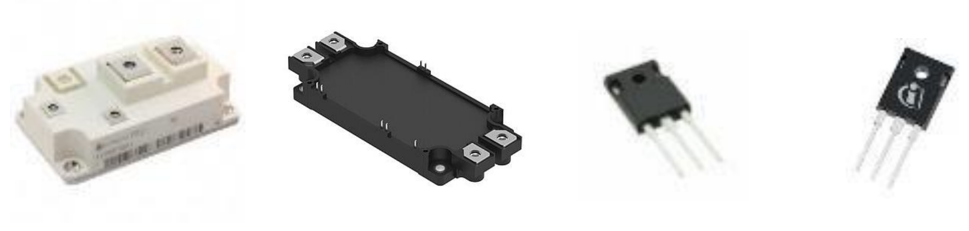
3.5.3 IGBT

Table 3-8 shows the different IGBTs tested at cryogenic and room temperature. FZ900R12KE4 IGBT shown in Fig. 3-35 was tested at room and cryogenic temperatures. After several runs, cracking sounds were heard from the device and the gate current increased indicating the device degradation. Discrete IGBTs were tested IKW75N65ET7XKSA1 and AIKQ100N60CTXKSA1 shown in Fig. 3-35, which did not suffer from the same degradation issues as the FZ900R12KE4 and were able to run multiple cycles without malfunctioning. The results of the forward voltage tests are as

demonstrated in Fig. 3-36. Similarly, VS122PA690M7 was able to withstand the cryogenic temperature without suffering gate failure. Based on that, this section covers the tests done on the VS122PA690M7 at cryogenic and room temperature. The tests would include; 1) forward voltage, 2) double pulse test and 3) paralleling test.

Table 3-8 Ratings of different IGBTs that were tested at room and cryogenic temperature.

Devices	FZ900R12KE4-HOSA1-ND	VS122PA690M7	IKW75N65-ET7XKSA1	AIKQ100N60-CTXKSA1
Max voltage rating (V)	1200	1200	650	600
Max current rating (A)	900	690	80	160
Manufacturer	Infineon	Vincotech	Infineon	Infineon
at 77K based on literature	Decreases [2]			
at 300K	2.1V @ 900A	1.54V @ 690A	1.65 @ 75A	1.5 @100A
Topology	Single switch	Phase-leg	Discrete	Discrete



(a) (b) (c) (d)

Fig. 3-35 Different IGBT devices tested at room and cryogenic temperature (a) FZ900R12KE4, (b) VS122PA690M7, (c) IKW75N65ET7XKSA1 and (d) AIKQ100N60CTXKSA1

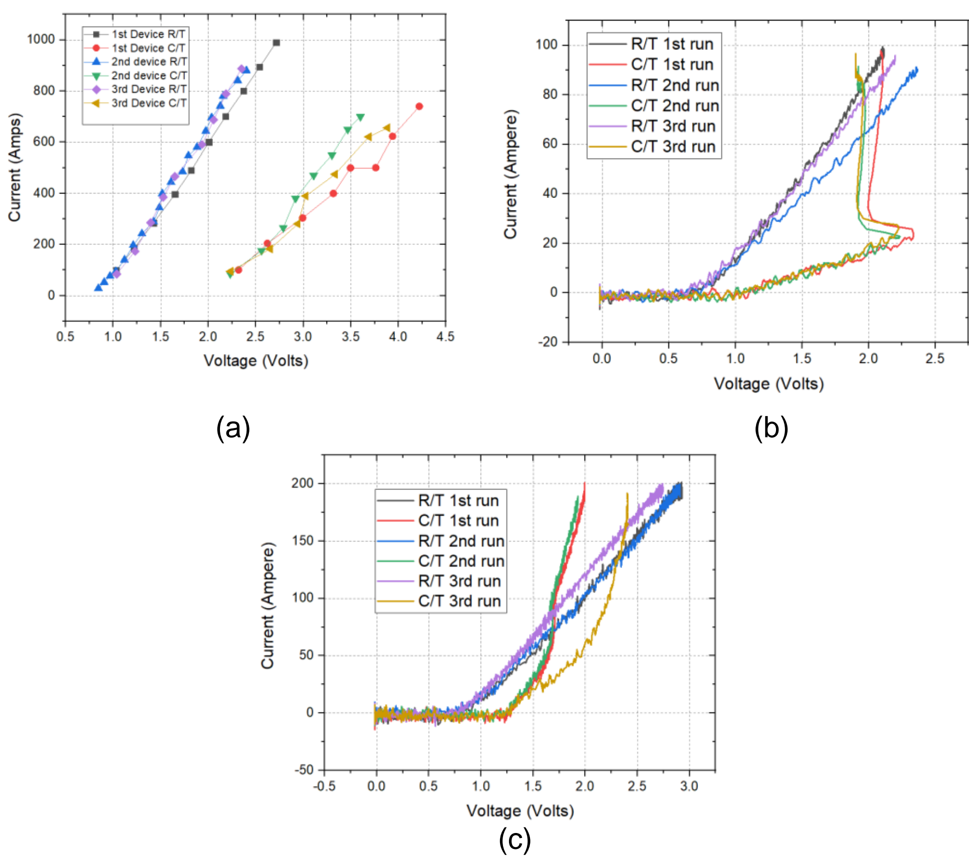


Fig. 3-36 Forward voltage test results for devices (a) FZ900R12KE4, (b) IKW75N65ET7XKSA1 and (c) AIKQ100N60CTXKSA1

3.5.3.1 VS122PA690M7

Fig. 3-37 (a) and (b) show the forward voltage test of VS122PA690M7 at different temperatures. From the figure, it can be seen that with the decrease in temperature the forward voltage of the device has decreased. This agrees with the literature review done in Chapter 2.

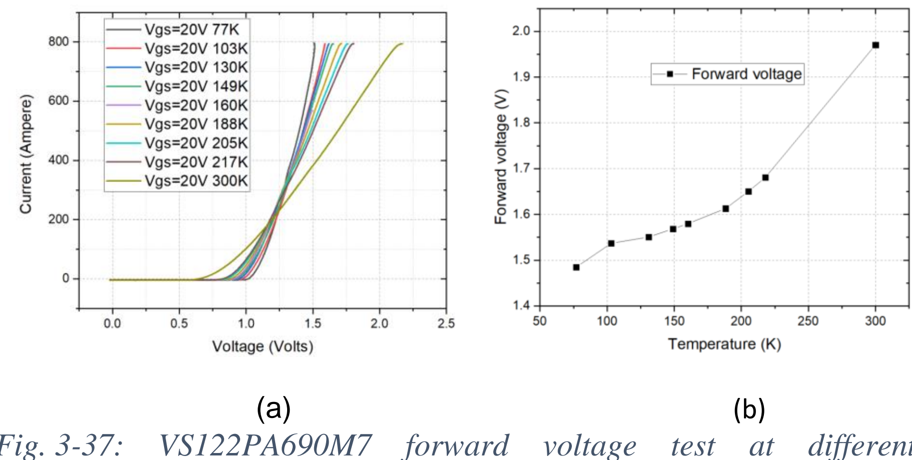


Fig. 3-37: VS122PA690M7 forward voltage test at different temperatures

Fig. 3-38 shows the double pulse test for VS122PA690M7 at room and cryogenic temperature. Fig. 3-38 (a) shows the double pulse test at room temperature and (b) at cryogenic temperature. Table 3-9 shows the switching time of the device at cryogenic temperature. From the figure, it is deduced that at cryogenic temperature the switching time has been reduced, hence the switching losses as seen in Fig. 3-38.

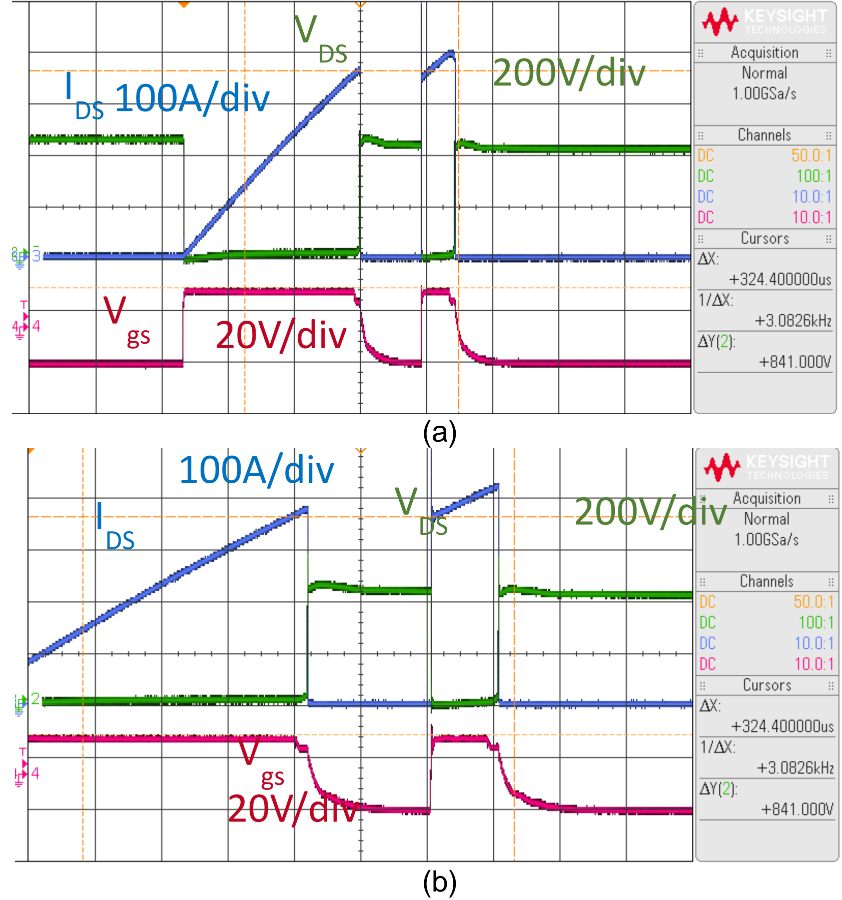


Fig. 3-38: Double pulse test for VS122PA690M7 at (a) room temperature and (b) cryogenic temperature

Fig. 3-39 shows the static paralleling test of VS122PA690M7 at cryogenic and room temperature. Both tests have shown good current sharing at room and cryogenic temperatures.

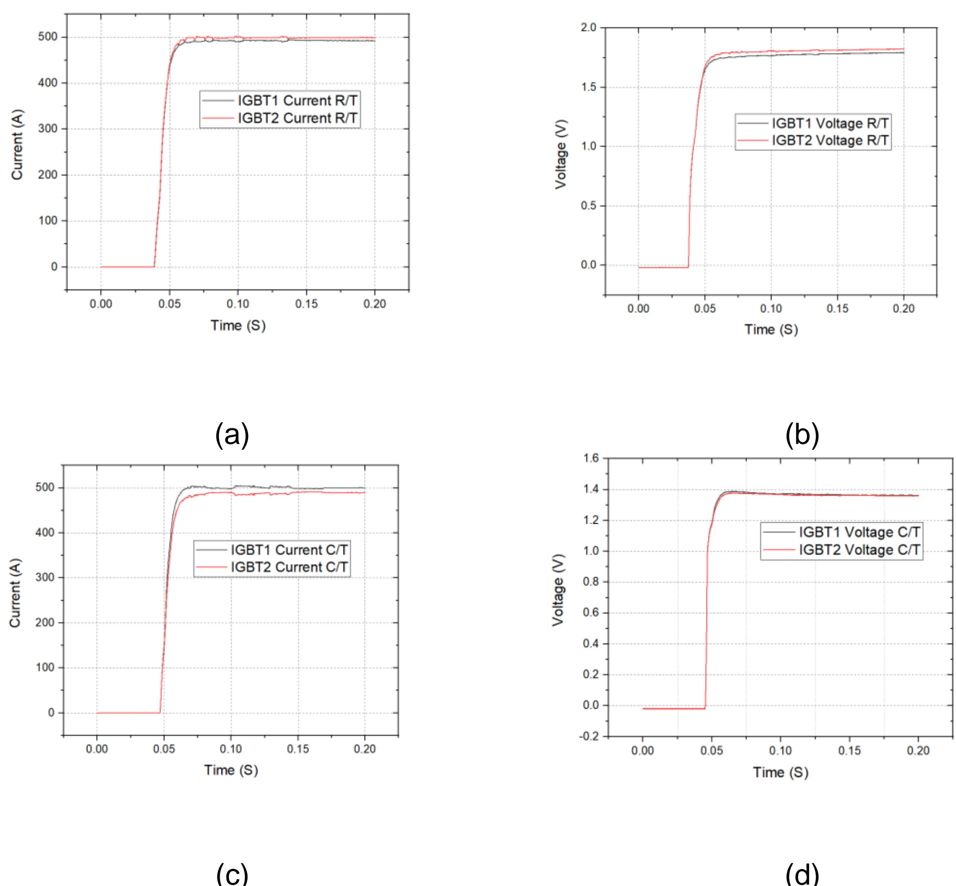


Fig. 3-39: VS122PA690M7 shows the paralleling results

Table 3-9 shows a summary of experiment results done for the IGBT. From the table it can be seen that with the decrease of temperature the forward voltage has decreased with temperature; hence lower conduction losses. Also from the table, it can be seen that the switching time has been significantly reduced at cryogenic temperature; hence, the conduction losses have been reduced.

Table 3-9 Experimental results of VS122PA690M7

	VS122PA690M7 Vincotech	
Temperature (RT = 300 K, CT = 77 K)	Room temperature	Cryogenic temperature
$V_{Forward}$ **(*V*)**	1.97	1.47
% Change	-25%	
[Current used for $V_{forward}$ test (A)]	[690]	
Switching off time (ns)	713	555
% Change	-22%	
Switching on time (ns)	273	134
% Change	-50%	

3.6 Contributions

The main contributions of this chapter can be summarised as follows:

- Investigated the performance of high capacity power semiconductor devices and modules at cryogenic temperature. In the literature, mostly discrete module below 100A were tested at cryogenic temperature. However, semiconductor devices above 100A have a module different structure than the ones below 100A and there are sparse data in the literature about them. Thus in this chapter, semiconductor devices with rating above 100A with were tested at room and cryogenic temperature to measure their performance. From the tests, it was confirmed that IGBT modules with Silicone gel insulation tend to fail at cryogenic temperature, however IGBT modules with epoxy resin insulation were able to function without degradation at that temperature.

- Studying the performance of a cryogenic pulse current transformer tailored for double testing of semiconductor devices at lower temperatures. In the literature, double pulse is difficult to measure at cryogenic temperature, as the commercial probes can not be immersed in LN2. Thus, a current transformer with a Nanocrystalline core was designed for that specific application. The designed current transformer had a bandwidth up to 100 MHz.

3.7 Summary

In this chapter, the testing of power electronic devices at room and cryogenic temperatures has been discussed. This chapter mainly focused on characterising the performance of semiconductor devices using mainly three characteristic tests, 1) static tests, 2) dynamic tests and 3) paralleling tests.

The chapter then went into detail discussing why these characteristic tests are important and how the experimental rig can be set up. The chapter begins with the static characteristic test, which is mainly used to identify the device's *I-V* characteristics. Based on that test we can identify the forward and breakdown voltages of the semiconductor devices at cryogenic and room temperature. The forward voltage can indicate whether the conduction losses increase or decrease with the temperature. As for the breakdown voltage, it gives an indication of which devices are best suitable with which voltage, helping with the circuit design at cryogenic temperature.

The chapter as well as discussed the dynamic test, and how it can be used to identify the switching losses at room and cryogenic temperature. For the dynamic test, a current sensor

is developed to have more accurate results as it can be immersed in liquid nitrogen thus reducing the distance between the source and the devices and avoiding introducing leakage inductances in the loop.

The chapter also addressed the paralleling test of devices. Only module devices have done that test to guarantee that the devices can share the load currents equally at cryogenic temperature.

The chapter then discussed the diodes' performance at cryogenic and room temperature using by assessing the performance using the characteristic tests mentioned earlier. The experimental results have shown that the Schottky diodes perform worse at cryogenic temperature as their forward voltage increased (higher conduction losses) and their switching losses increased as well. The best performing diodes were the Silicon PN diodes, as they have displayed that their conduction and switching losses decrease with temperature.

The chapter then described the experimental results of the MOSFET devices. From these results, the SiC MOSFET (MSCSM120AM02CT6LIAG) was found to have worse performance at cryogenic temperature, in terms of conduction, and switching losses as they both increase at cryogenic temperature. Also, the SiC MOSFET were unable to parallel successfully at cryogenic temperature as one out of the two tested devices carried more than 66% of the load current. The Si SJ MOSFET on the other hand has shown lower conduction losses at cryogenic temperature.

The chapter also investigated the performance of the IGBT devices at cryogenic temperature. The experimental results show that one device module the FZ900R12KE4 kept failing at cryogenic temperature, mainly due to the insulation, which utilises silicone gel. Another device module VS122PA690M7 with a different insulating material (epoxy resin) was able to withstand the low temperature without suffering failures as the previous device. The VS122PA690M7 has shown lower conduction and switching losses at cryogenic temperatures. The VS122PA690M7 also showed good paralleling at cryogenic temperature. Thus, the VS122PA690M7 is a more preferable option over the SiC MOSFET (MSCSM120AM02CT6LIAG) for cryogenic applications, as the SiC MOSFET has a negative temperature coefficient. The results are consistent with the literature.

Chapter 4

Power converter circuits for all-electric and hydrogen-electric aircraft

This chapter primarily focuses on the design of cryogenic power converters for all-electric and hydrogen-electric aircraft. In this chapter, the electrical architecture design of all-electrical aircraft will be investigated, where the ratings of the system and the design requirements for power converter circuits will be investigated. Based on that, two cryogenic power converters will be studied in this chapter; 1) a three-phase rectifier using diodes connected to an axial machine with HTS coils, and 2) a phase-leg using SJ MOSFETs for dc-dc and dc-ac power conversion.

4.1 Introduction

The architecture of all-electric aircraft is shown in Fig. 4-1, where liquid hydrogen would act as both fuel and coolant for the system. As seen in Fig. 4-1, a hydrogen turbine is used as the prime mover for superconducting generators. The superconducting generator provides an ac output power, which is rectified using a cryogenic converter and transmitted over a superconducting cable as it is connected to a cryogenic inverter used to drive the superconducting machine that is connected to the propeller of the aircraft.

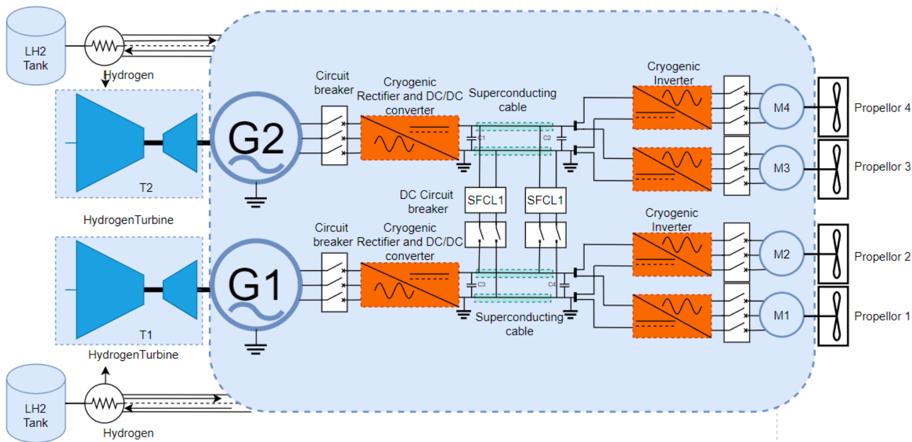


Fig. 4-1: Architecture of all-electric aircraft

For the architecture in Fig. 4-1, it was shown that two main power converter circuits are required for all-electric aircraft; 1) rectifier and dc/dc converter; which consists of a three-phase rectifier and dc/dc converter to regulate the voltage across the bus, and 2) inverter circuit to control the motor speed.

4.2 Design of the system

The purpose of this section is to determine the ratings of the converters and the design requirements for each converter.

To determine the operating voltage of the converter, [90] discussed the benefits of using higher bus voltage levels for conventional aircraft. The study has found that by increasing the voltage from the conventional 115 V_{ac} to 270 V_{dc} system the size of the cables, the mass of the converters and the overall electrical system are reduced by approximately 60 per cent. This reduction leads to an increase in the power density of the electric aircraft and the feasibility of the system. An axial generator with HTS [91] will be used to supply the power to the system in the experiments in the following sections. Based on the voltage

recommendation in [90], and the machine ratings in [91], the system parameters shown in Table 4-1 will be used for power converter design.

Table 4-1 Parameters for all-electric aircrafts

Parameters	Values
Voltage (V)	270
Frequency (Hz)	50-400
Current (A)	100

Fig. 4-2 shows the three main converter circuits to be discussed in this chapter;

1. Three-phase uncontrolled rectifier; this circuit shall be connected to an axial generator, with HTS coils, to see the output. Fault analysis is done as well.
2. Phase-leg operating as a dc-dc converter; this circuit is connected to a bench power supply where it would be used as a step-down converter and a current limiter
3. Phase-leg circuit operating as a dc-ac inverter; this circuit is connected to a bench power supply where it would be used as an inverter circuit which can be extended to be a three-phase inverter.

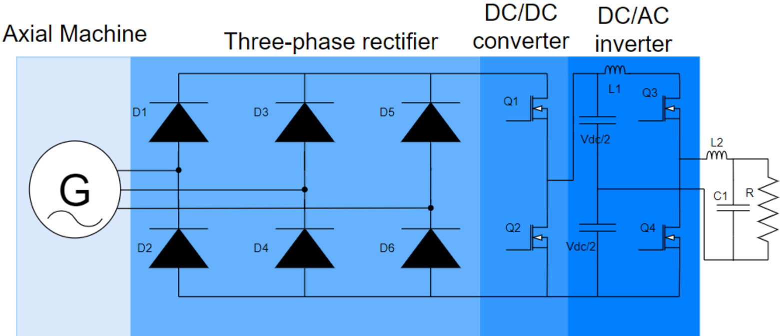


Fig. 4-2: Power converters connected to the axial machine based on the system architecture in the next section

4.3 Three-phase rectifier and fault analysis

In this section, the design, development, and fault analysis of a three-phase rectifier connected to an axial machine with HTS coils is explained. The section shall mainly with the selection of the devices suitable for the three-phase rectifier, setting up the experiment rig, testing the rectifier for single-phase input, testing the rectifier while integrated with the axial machine and fault analysis of the experiment.

4.3.1 Research gap for cryogenic rectifier

In the literature [28], [29] converters and rectifiers have been tested at cryogenic temperatures connected to superconducting coils. However, there has been no previous literature on having a cryogenic rectifier connected with an axial machine that has HTS coils. Thus, the research gaps to be covered in this chapter are the following;

- Designing and testing a cryogenic rectifier suitable for an axial machine with HTS coils.
- Fault analysis on the rectifier side and investigating the HTS coil after the fault.

4.3.2 Selection of devices for the three-phase rectifier

The design criteria for the rectifier is to have a rating voltage of at least 600 V and supply current up to 200 A. The rectifier designed shall be uncontrolled, where diodes shall be used to rectify the ac input to give a dc output. Previously in Chapter 3, different devices have been tested at room and cryogenic temperatures, where some of the tested rectifier diodes have shown that their conduction and switching losses change with the decrease of

temperature. Table 4-2 shows a summary of the important change in characteristics of different rectifier devices at different temperatures. From the table, it can be seen that although SiC Schottky diode breakdown voltage did not change at cryogenic temperature, it has higher switching and conduction losses at that temperature than at room temperature. Conversely, silicon-based devices have shown lower conduction and switching losses. The device that has shown the best performance in Table 4-2 is the APT2X101D120J diode from Microsemi and based on that it was selected as the building block for the three-phase rectifier circuit.

Table 4-2 Test results of rectifier diodes at room and cryogenic temperature

	GB2X100MPS12-227 GeneSiC SiC Schottky		**APT2X101D120J Microsemi Si Ultrafast**		**HFA220FA-120 Vishay Si Ultrafast**		**MUR2X100A12 GeneSiC Si Superfast**	
Temperature (CT = 77 K , RT=300 K)	RT	CT	RT	CT	RT	CT	RT	CT
$V_{forward}$ (V)	1.49	1.99	2.08	1.5	3.16	1.46	1.9	1.8
% Change	+33%		-24%		-53%		-5%	
[Current used for $V_{forward}$ test (A)]	[100]		[100]		[100]		[100]	
V_{BR} (V)	1400	1400	1300	1000	1400	1300	1200	1080
% Change	0%		-23%		-7%		10%	
Q_{rr} charge (nC)	168	112	28	1.62	102	5.43	192	6.56
% Change	-33%		-94%		-94%		-96%	
Peak transient current (A)	28.2	26.6	25.8	25.8	32.8	26.1	32.1	25.8

4.3.3 Setting up the experiment rig

APT2X101D120J was used to build a three-phase rectifier seen in Fig. 4-3. The diodes in the figure are arranged so that there are two modules connected per phase. The circuit is

located in a Styrofoam box where it is going to be filled with LN2. Over the next sections, the rectifier is tested in single-phase and three-phase modes.

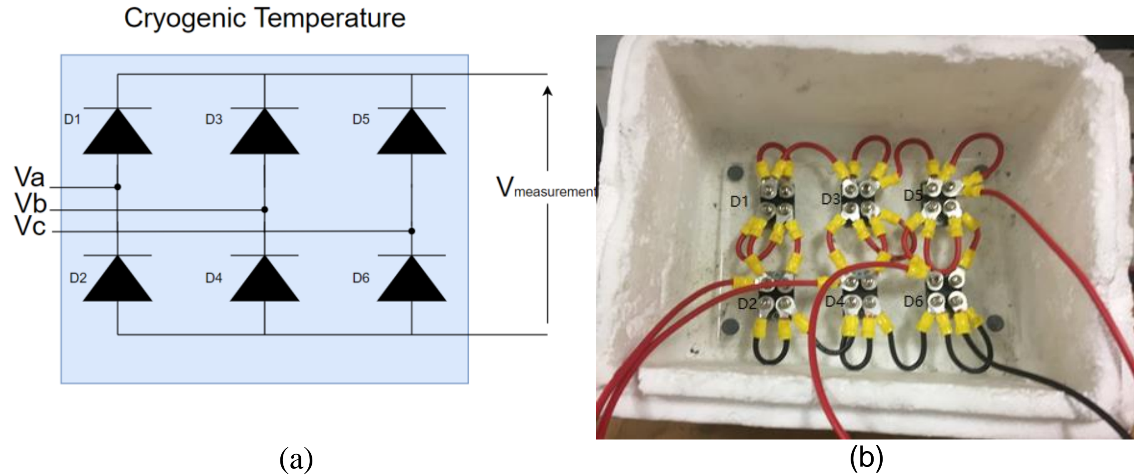


Fig. 4-3 Three-phase rectifier based on APT2X101D120J devices, (a) schematic, (b) the experimental rig setup

4.3.4 Rectifier circuit for single-phase input

The circuit was first run as a full-bridge rectifier for a single-phase at cryogenic and room temperature. The test was performed using the following equipment Fig. 4-4;

1) AE TECHRON 7796 amplifier
2) Arbitrary Waveform Generator
3) Keysight MSO-X 2024A
4) Passive Keysight probe

As seen in Fig. 4-4, a waveform generator is connected to an amplifier (AE TECHRON 7796) that generates the ac waveform required for the experiment. The

circuit is run at room and cryogenic temperature. The input supply is located outside of the Styrofoam box.

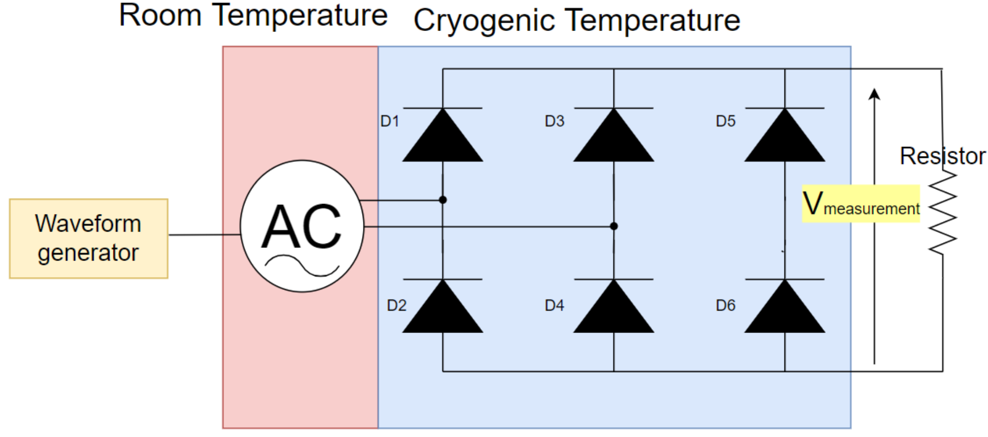


Fig. 4-4: Cryogenic three phase rectifier testing diagram

The input voltage to the circuit was set to V_{rms} =11.5 V. The results are shown in Fig. 4-5. From the figure, it can be seen that the output voltage at cryogenic temperature has increased due to reduced forward on-voltage which also results in lower conduction losses. The average output voltage was calculated at both room and cryogenic temperature where it was found that at room temperature $V_{rms\ (300K)}$ = 7.5 V and cryogenic temperature $V_{rms\ (77K)}$= 8.3 V, thus there is a 10.6 % decrease in the conduction losses if the same current to be supplied, the load is set at R_L=2Ω.

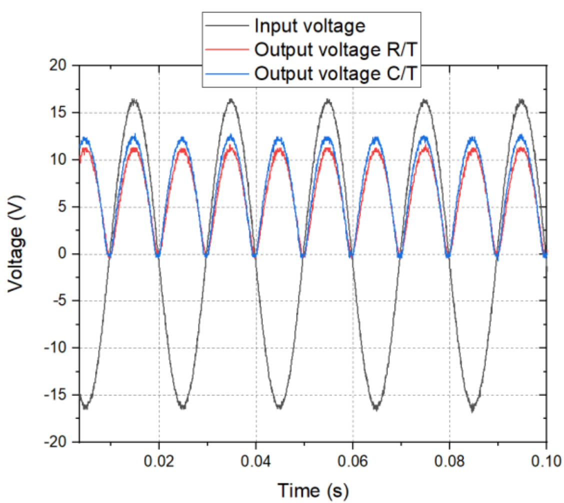


Fig. 4-5: Experimental results for full bridge rectification at cryogenic and room temperature

4.3.5 Three-phase rectifier for an axial generator with HTS coils

This section focuses on testing the three-phase rectifier integrated with the axial machine. Fig. 4-6 shows the internal structure of the machine with the superconducting coils. Based on the improved performance of the device at cryogenic temperature a cryogenic unit testing platform has been set up as seen in Fig. 4-7 (a). Fig. 4-7 (b) shows the schematic, where it can be seen that the dc motor acts as a prime mover as it is used to drive an axial machine that has six rotor coils, two of which are superconducting and the rest are made from copper. The axial motor output is connected to a rectifier circuit that is shown in Fig. 4-8, where current and voltage probes are used to capture the experiment results. The system was operated at 240 RPM in generator mode. Before commencing rotation, the HTS machine and the rectifier were fully cooled down to 77 K by LN2. The speed control of the rotational shaft was implemented via the separately excited dc motor by adjusting the dc power supply input seen in Fig. 4-7.

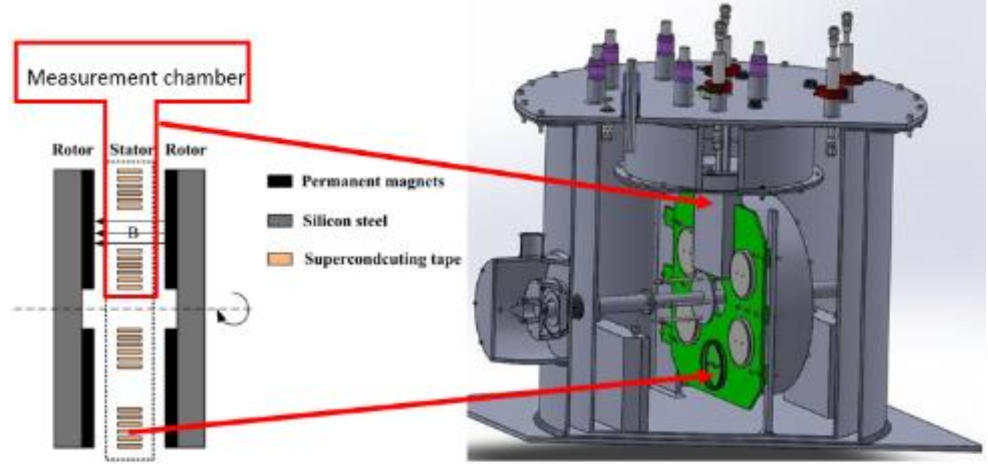


Fig. 4-6: Axial machine with two superconducting coils

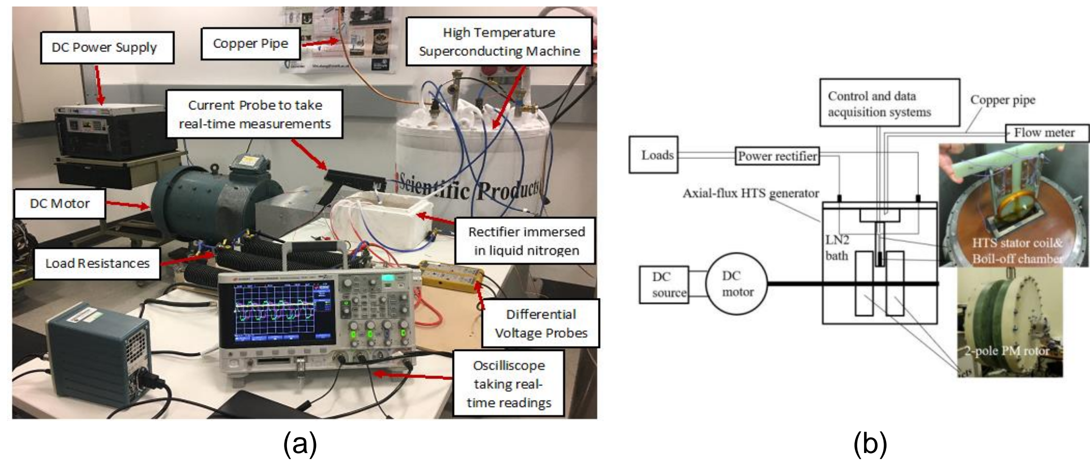


Fig. 4-7: Cryogenic propulsion unit test platform, (a) shows the experimental rig setup and (b) shows the schematic diagram of the experiment

Fig. 4-8 shows the electrical connection of the experiment. From the figure, it can be seen that a dc motor is used as the replacement for hydrogen turbines seen in Fig. 4-1, where it acts as a prime mover for the axial machine generator. By controlling the dc motor, the axial machine speed is changed and accordingly the voltage and current output of that machine changes. The three phases of the axial machine are connected to the rectifier as

seen in the figure, which in turn is connected to a resistor, where voltage and current are measured across the resistor. The control applied in this setup is open-loop control. This setup emulates the effect of all-electric aircraft architecture presented earlier in this chapter.

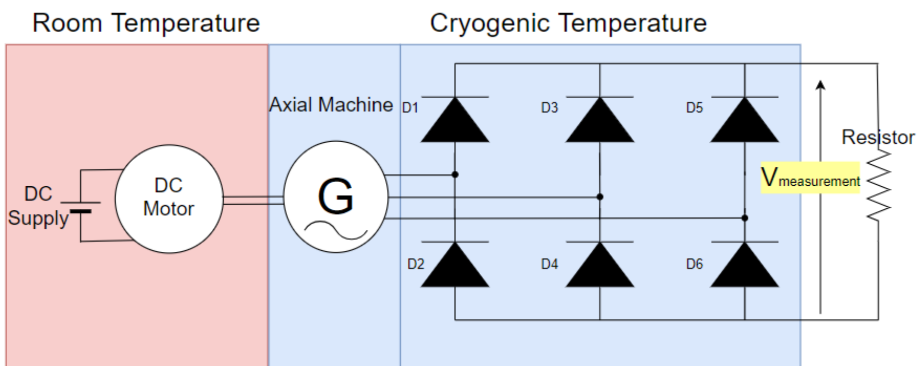


Fig. 4-8: Three-phase rectifier connected to an axial machine with two HTS coils

Fig. 4-9 shows the experimental results of using a three-phase rectifier connected to an axial machine that has two of its cores superconducting. The imbalance in the voltage outputs is due to the impedance mismatch between Phase A (an HTS phase winding is 937.4 μH) and Phases B and C (a copper phase winding is 526.4 μH). It can be noticed from the figure that there are harmonics and disproportionality at the peaks of the waveforms, where this is mainly what was generated on the machine side.

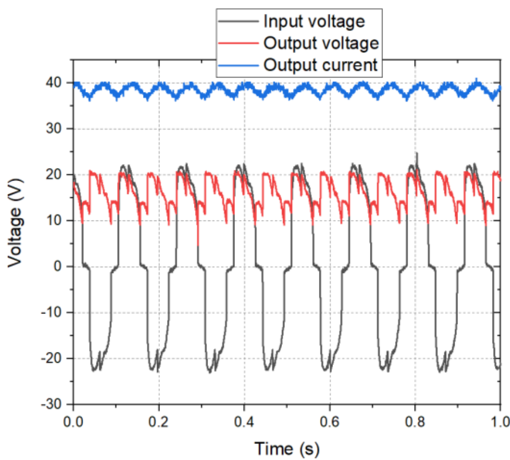


Fig. 4-9: Output results using a rectifier for the axial machine generator

4.3.6 Transient analysis of the propulsion unit

Implementing a sudden short-circuit in a cryogenic propulsion network can have serious impacts on superconducting machines and the whole aircraft's electrical system. It can potentially happen when there is a device or insulation failure in the cryogenic environment, leading to permanent damage to HTS windings and consequently affecting the performance of the whole system. In this section, the effect of a short circuit event at the power electronic side of the propulsion unit, which can be caused by the failure of a diode, is studied both experimentally and numerically.

As shown in Fig. 4-10, a short-circuit was introduced across D4 at approximately 0.5 s. When the short-circuit event occurred, there was a loud sound from the machine, indicating a quench event happening. The nitrogen gas boil-off rate increased dramatically from 1.8 SLPM to more than 7 SLPM, as shown in Fig. 4-11. The HTS coil was inspected physically and electrically afterwards. There was no obvious burning sign of the coil due to the quench induced by the short-circuit. However, the outer layer of the coil has been

deformed slightly due to unbalanced Lorentz forces during the short-circuit. The critical current of the measured HTS coil remains the same, but the ac loss values are 28 times higher than before the short-circuit event. This indicates that weak points have been introduced into the coil, caused potentially by the unbalanced Lorentz forces or the large amount of heat generated during the quench. The quenching of the superconducting coil curtailed the output current leaving the diodes unharmed.

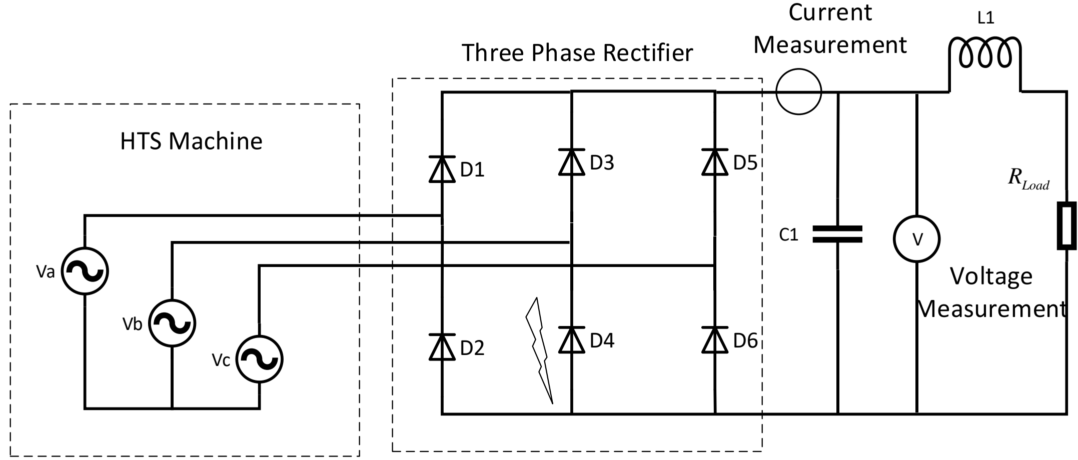


Fig. 4-10: Induced short circuit on diode D4

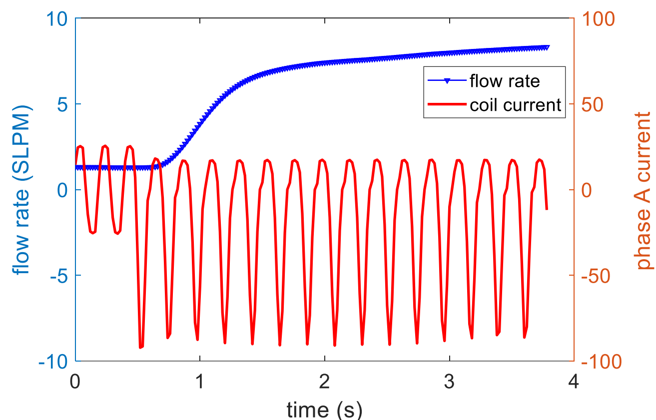


Fig. 4-11: Short circuit current effect on the flow rate and boil off

Fig. 4-12 shows the phase-phase output voltages and the load voltage before and immediately after the short-circuit event. The sample rate is 50 samples/s due to DAQ system limitations. During the experiment, diode D4 was short-circuited as seen in Fig. 4-10, meaning that when V_b is larger than V_a or V_c, there is a short-circuit across line voltage V_{ba} and V_{bc}, which in return would cause a very large current passing through the phases, and eventually causing the superconducting coil in Phase A to quench.

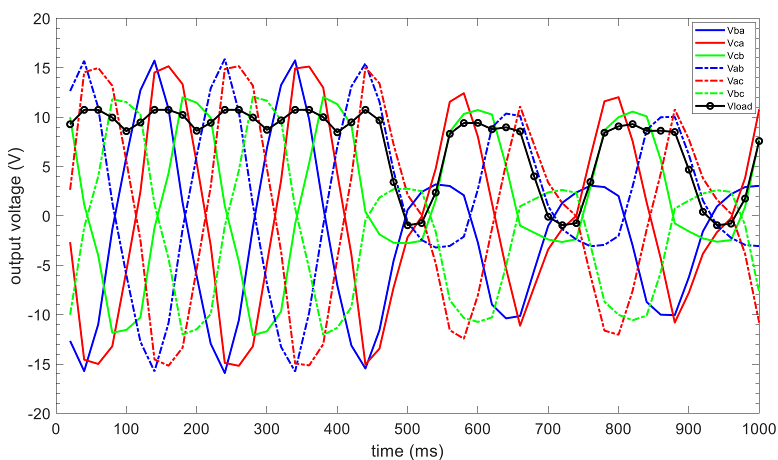


Fig. 4-12: Three-phase output of the axial machine during the fault event

To better understand what happened during the short-circuit event, a MATLAB/SIMULINK. The parameters that were measured directly from the system are listed in Table 4-3. The simulation simplifies the quench progress of HTS windings by ignoring the quench propagation process and uses two resistance values to represent the HTS winding before and after the quench respectively. Good agreements between experiment and simulation have been found as shown in Fig. 4-11 and Fig. 4-12.

Table 4-3: Parameters used in system simulation.

Resistance	Description	Value
$\boldsymbol{R_{Load}}$	Measured resistance for the load resistance bank	0.33 Ω
$\boldsymbol{R_{HTS\ Coil}}$	Measured resistance for the HTS coil joints	$2\ \mu\Omega$
$\boldsymbol{R_{quench}}$	Equivalent resistance after the HTS coil quenches	$60\ m\Omega$
$\boldsymbol{R_{copper\ Coil}}$	Measured resistance for copper coils	$98\ m\Omega$

Fig. 4-13 shows a comparison between the experimental and simulation results for the output voltages. When the short-circuit occurred, V_{ab} reaches -3 V, corresponding to voltage drops from D2 and the copper cables when an overcurrent flowed from Phase B to Phase A. Similarly, the positive half cycles of V_{bc} are approximately 3 V, corresponding to voltage drops from D6 and the copper cables when an overcurrent flowed from Phase B to Phase C. V_{ca} is largely unaffected. The slight voltage drop is the result of the slowing-down of the dc machine from 150 RPM to 136.5 RPM. This results in the peak induced EMF being reduced from 15 V to 12 V. A similar voltage drop is also observed in the positive half cycles of V_{ab} and the negative half cycles of V_{bc}.

Fig. 4-14 shows the comparison between experimental results and simulation for the measured load current and Phase A current. During the pre-fault period, the load current had small oscillations around 25 A. After the fault, the load current has been significantly reduced as seen in Fig. 4-14. The peak Phase A current is approximately -80 A to -90 A for the negative half cycles. This is much higher than the critical current of the HTS coil, which is 53 A under the rotational field conditions. Consequently, the HTS coil has quenched, leading to the large nitrogen boil-off rate as shown in Fig. 4-11. The Phase A

current is asymmetric because the short-circuit only happens when V_b is higher than V_a and V_c. For positive half-cycles, the slight reduction in the Phase A current is the result of EMF reduction.

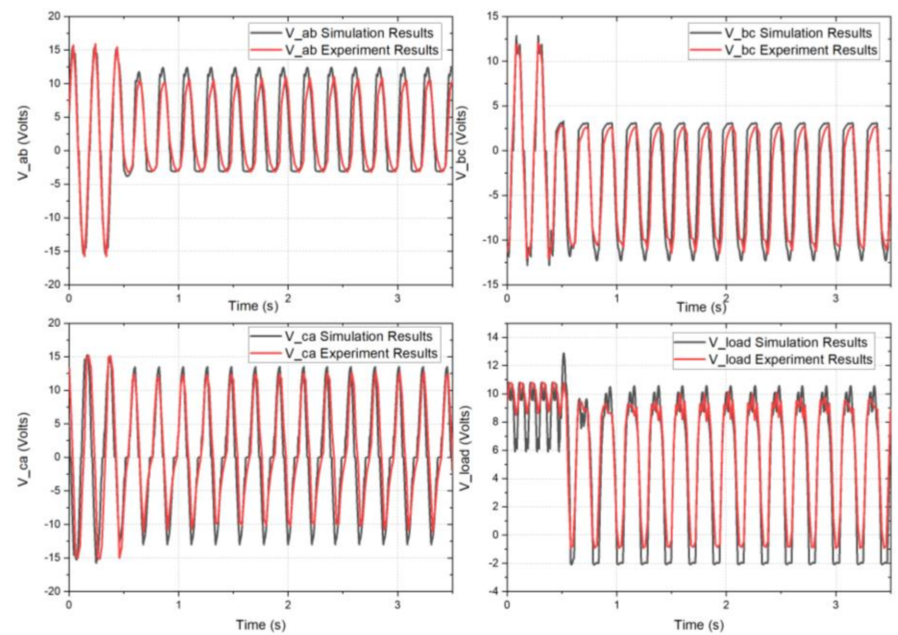


Fig. 4-13: Comparison between experimental and simulation voltages

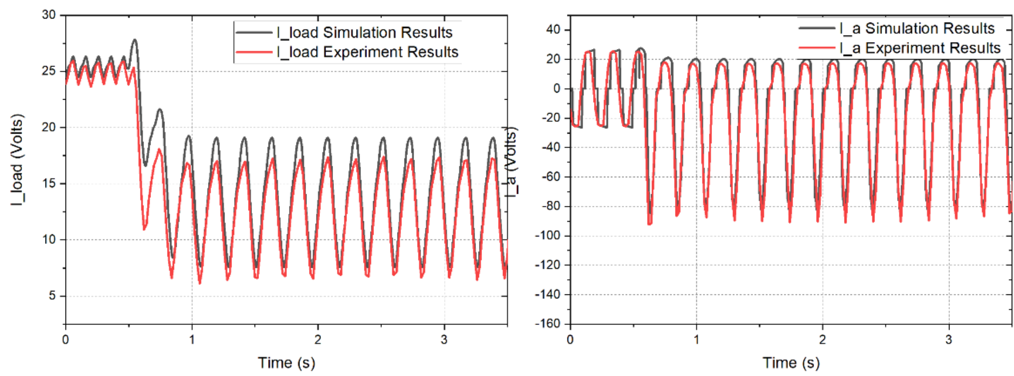


Fig. 4-14: Comparison between simulated and experimental load and phase A currents

4.3.7 Summary of testing cryogenic rectifier

In this section, an assessment has been done on the application of a rectifier circuit for an axial machine with superconductor coils. At first, the down-selection of the devices was made based on the experimental results from chapter 3, where it was deduced that the Si-based rectifier APT2X101D120J has shown superior characteristics at the cryogenic temperature over other diode types.

Based on that deduction an experimental rig was built, where six modules APT2X101D120J were connected to form a three-phase rectifier, a configuration for two modules/phases. After which, a single-phase experiment was run using a bench power supply, where it was shown that at cryogenic temperature the three-phase rectifier has higher efficiency than at cryogenic temperature.

Subsequently, the three-phase rectifier was connected to an axial machine where a rectified waveform has been produced. Afterwards, fault analysis was done to assess the effects of a short circuit on an axial machine with HTS coils. This is done by short-circuiting diode D4 during the experiment and simulation.

4.4 Phase leg application for all-electric aircraft

As part of the implementation of cryogenic semiconductors for all-electric and hybrid-electric aircraft. Previous papers have tested converters at a cryogenic temperature [92], [93] where the converters immersed at cryogenic temperature were found to be more efficient than at room temperature, with cooling losses excluded. This section will mainly

focus on testing a phase-leg circuit at cryogenic and room temperature and comparing the results in terms of efficiency.

4.4.1 Selection of switching device

From the literature review in Chapter 2 where different semiconductor switches have been assessed at room and cryogenic temperature, it was deduced that Si MOSFET devices have the best performances at cryogenic temperature. Based on this, in this thesis, the SJ MOSFET tested in Chapter 3 was used as the building block for the phase-leg seen in Fig. 4-15, where they had proven high efficiency performance in [94]. SJ MOSFETs are known for being superior to standard MOSFETs due to their low on-state resistance [95]. However, their intrinsic diode passes a high reverse recovery charge Q_{rr} where [96] has introduced a circuit to deactivate that diode shown in Fig. 4-15. To address the high reverse recovery charge Q_{rr} drawn by the intrinsic diode, and the non-linear output capacitance C_{oss} of the Si MOSFET, ancillary components and the dual-mode switching technique developed by Feng *et al* will be used in this thesis. As such, this work extends the work carried out by Feng.

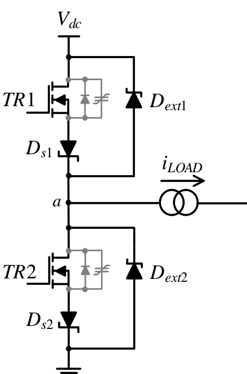


Fig. 4-15: Phase leg configuration using SJ MOSFET with intrinsic diode deactivation circuit

Table 4-4 shows the approximate performance trends of the candidate device types as the temperature is reduced from RT to 77 K. The trends listed are estimated from works including [2],[39], [42], [43], [92], [97]-[101]. It is noted that the trends are generic, and are not the measured trends for the specific devices listed in Table 4-4.

Although it has been decided to use an SJ MOSFET at cryogenic temperatures, the characteristics of this device are also included for completeness in Table 4-4. The far-right column lists the relevant and important trends. The V_{RRM} of the Si diode falls and the forward voltage drop (V_f) rises, but these trends are mitigated by a reduced Q_{rr}. Importantly, the V_f of the SiC Schottky diode rises, with no compensating beneficial effects. The V_f of the Si Schottky diode also rises, again with no mitigating beneficial effects. The $R_{DS(on)}$ of the low-voltage MOSFET falls significantly. The Q_{rr} of the SJ MOSFET's intrinsic diode also falls significantly. However, in the course of addressing the C_{oss} problem, this diode is not activated, and therefore this trend is not deemed a relevant significant trend for the application here.

Table 4-4 Approximate device performance trends as the temperature are reduced from room temperature to 77 K.

Device	Device type	Parameter	Trend as the temperature is reduced to 77 K
Main device location	Si SJ MOSFET [2],[42], [43], [98], [99]	V_{DSS}	-25%
		$R_{DS(on)}$	-80%
		Intrinsic diode Q_{rr}	No change with temperature
		$v_{GS(th)}$	+15%
Anti-parallel device location	Si fast recovery PN diode [2],[100]	V_{RRM}	-20%
		V_f	+25%
		Q_{rr}	Very good
	SiC Schottky diode [102]	V_{RM}	No change
		V_f	+25%
		Q_{rr}	No change
Series device location	Si Schottky diode [39]	V_{RRM}	-20%
		V_f	+20%
		Q_{rr}	No change
	Si low-voltage MOSFET [100]	V_{DSS}	-20%
		$R_{DS(on)}$	-80%
		Intrinsic diode Q_{rr}	Very good

SJ MOSFETs equipped with the intrinsic diode deactivation circuitry in [96] have been used in a cryogenic power converter in [103]. The converter in [98] is a three-level active neutral point clamped (ANPC) topology, and some of the MOSFETs in it are deployed in series. However, the objective of the current thesis is to evaluate the best configuration of circuitry for cryogenic use in a simple two-level converter with one SJ MOSFET in each module. The modules' parameters are listed in Table 4-5.

Table 4-5: Devices used for cryogenic temperature testing of the testing modules and their key parameters

Device	Device specifications	Module schematic
Si super-junction MOSFET (TR1)	IPW60R041P6	
	V_{DSS} = 650 V	
	$R_{DS(on)}$ = 41 mΩ (maximum)	
Si fast recovery FRED diode (Dext in Modules (a))	DSEI30-06A	
	V_{RRM} = 600 V	
SiC Schottky diode (D_{ext} in Modules (b))	SCS220AE	
	V_{RM} = 650 V	
Si low-voltage MOSFET (TR2 in Modules (a) and (b))	IRFB7546PBF	
	V_{DSS} = 60 V	
	$R_{DS(on)}$ = 6.0 mΩ (typical)	

4.4.2 Diode deactivation circuit

Fig. 4-15 shows a VSC phase-leg with SJ MOSFETs and intrinsic diode deactivation circuitry using ancillary power devices based on the circuit patented in [96]. The series diodes D_s prevent reverse current from flowing into the MOSFETs when they would otherwise be carrying a freewheeling current via their intrinsic diodes. The external diodes D_{ext} in anti-parallel, which replace the function of the intrinsic diodes, can be chosen to have a low reverse recovery charge characteristic.

Even if its intrinsic diode behaviour is addressed, the SJ MOSFET's C_{oss} is problematic in a bridge-leg when the MOSFETs are switched complementarily in the normal way. Fig. 4-16 shows the highly non-linear Q-V characteristic of C_{oss}. If, for example, the load current i_{LOAD} is positive and $TR2$ is turned on when $TR1$ is off, then $TR2$ fully self-discharges its C_{oss}. When $TR1$ next turns on, it, therefore, recharges the C_{oss} of $TR2$ from 0 V up to the dc-link voltage V_{dc}. The energy dissipated in $TR1$ due to this action is approximated by the nearly rectangular shaded area representing capacitive co-energy

under the Q-V curve in Fig. 4-16. In practice, the energy dissipated in $TR1$ is greater than this due to the incoming i_{LOAD} being superimposed onto the current charging C_{oss}.

Furthermore, it can be seen that the C_{oss} of $TR2$ is high when the voltage across it is low. When $TR1$ turns on it is therefore sourcing a large transient current into this capacitance. Effects of this current are to produce EMI and an oscillatory over-voltage across $TR2$.

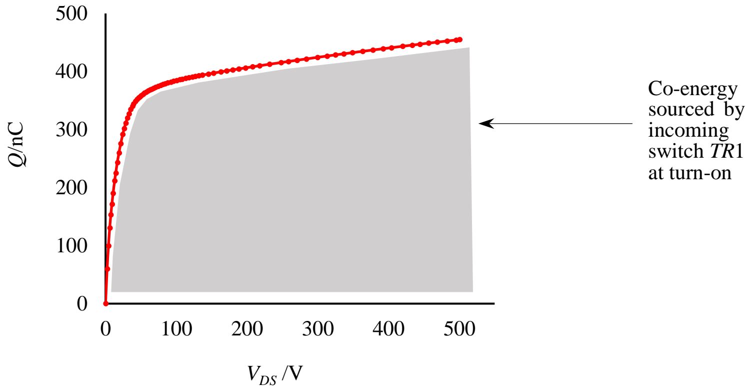


Fig. 4-16: Typical Q-V characteristic of an SJ MOSFET's output capacitance C_{oss}, in this case, that of the IPW60R041P6 device.

To avoid the problems associated with C_{oss}, the phase-leg can be run with unipolar PWM modulation to avoid fully discharging the C_{oss} of $TR2$ when $TR1$ is off. When i_{LOAD} is positive only $TR1$ switches, and $TR2$ is never turned on. As shown in Fig. 4-17 (a), $TR2$'s C_{oss} is now only partially discharged, down to the breakdown voltage V_{BR} of D_{s2}. V_{BR} is typically such that C_{oss} is not discharged to below the 'knee point' of the curve in Fig. 4-17 (b), and the energy dissipation in $TR1$ is now approximated by the smaller shaded area. The gradient of the Q-V curve of C_{oss} is lower at V_{BR} than it is at 0 V. When the incoming device turns on, the complementary device, therefore, presents a lower capacitance, and the incoming device consequently sources a smaller transient current.

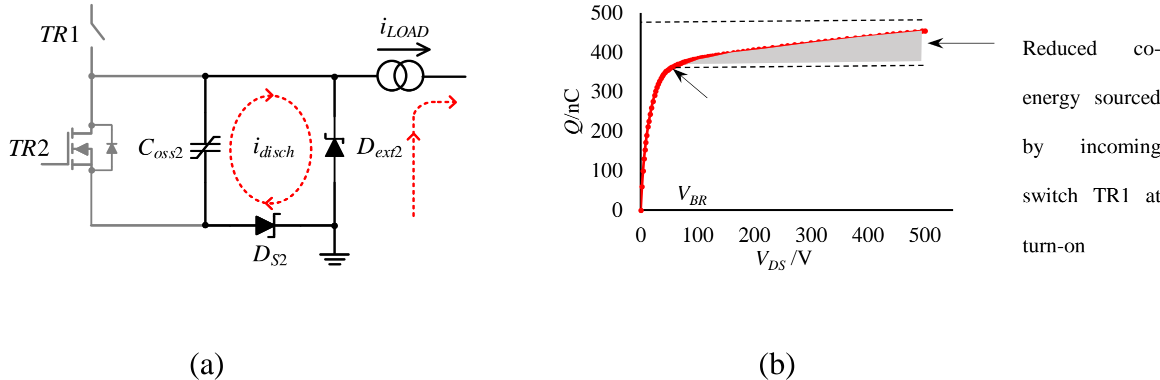


Fig. 4-17: Discharge route for C_{oss} of TR2 when TR1 is off and Dext2 is freewheeling. The circuit is operating with a positive i_{LOAD} and only TR1 is being driven on and off. Provided that TR2 is not turned on during the freewheeling period, its C_{oss} is only discharged down to the Schottky diode's breakdown voltage VBR. (b) Effect of only partially discharging the C_{oss} of the IPW60R041P6 SJ MOSFET [94].

Similarly, when i_{LOAD} is negative, only *TR*2 switches and *TR*1 is never turned on. This is relatively straightforward to arrange in a dc-dc converter [104]. However, a problem arises in dc-ac or ac-dc power conversion when i_{LOAD} is transitioning through zero. Ideally, bipolar switching would be used in this region to avoid distortion in the ac current waveform due to i_{LOAD} becoming discontinuous. With an ac load current such as that in an inverter, the dual-mode gate driver technique in [94] can be applied. In the fast-switching mode, unipolar switching is applied to either *TR*1 or *TR*2 according to the direction of i_{LOAD}. In this mode, the MOSFETs are driven in the normal way with rapid switching transitions for low losses. However, at low i_{LOAD} magnitudes, bipolar PWM modulation is enabled to reduce distortion in the ac waveform. The problem of high peak currents due to supplying high charges into fully-discharged C_{oss} that occurs with bipolar

switching is addressed by turning the SJ MOSFETs on slowly (the "slow-switching mode"), thereby limiting the di/dt in the C_{oss} charging current sourced by the incoming switch.

Fig. 4-18 shows the same Q_{oss} for different I_{LOAD} values and different di/dt. A lower I_{LOAD} and lower di/dt lead to lower I_{peak}, therefore when I_{LOAD2} is lower than I_{LOAD1} in Fig. 4-18, I_{peak2} is lower than I_{peak1}. A key point is that, although the slow-switching mode incurs losses, enabling it only at low i_{LOAD} magnitudes means the aggregate power losses in the converter are low. Slow-switching SJ MOSFETs in a VSC under all conditions to avoid high peak currents reduces efficiency, as described in [102].

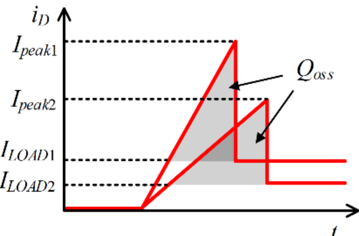


Fig. 4-18: Same Q_{oss} under different load current i_{LOAD} and different di/dt [94].

4.4.3 Dual-Mode control and gate driver circuit

The dual mode technique has been implemented previously in [94]. Dual-mode switching is a combination of both fast switching and slow switching. During the fast-switching unipolar waveform is applied and during slow switching bipolar switching is applied. In the so-called hard switching mode, unipolar PWM modulation is selected for $TR1$ and $TR2$ seen in Fig. 4-15 according to the direction of i_L. During this mode with high i_L magnitudes, the MOSFETs are driven with rapid switching transitions for low losses.

However, in the zones where i_L magnitudes are low, bipolar PWM modulation is applied to diminish distortion as much as possible. By implementing slow switching in the bipolar region the di/dt in the current will be limited. This prevents the problem of high peak currents due to supplying high charges into fully discharged C_{oss} capacitances that occur with bipolar modulation in the normal way.

Fig. 4-19 shows the same Q_{oss} for different i_L values and different current slew rates explained in [94], di/dt, where lower i_L and lower slew rate lead to lower i_{peak}. In the slow switching mode, this becomes an advantage when operating bipolar PWM modulation under low load current. Different gate resistances are used in the turn-on path to control the switching speed.

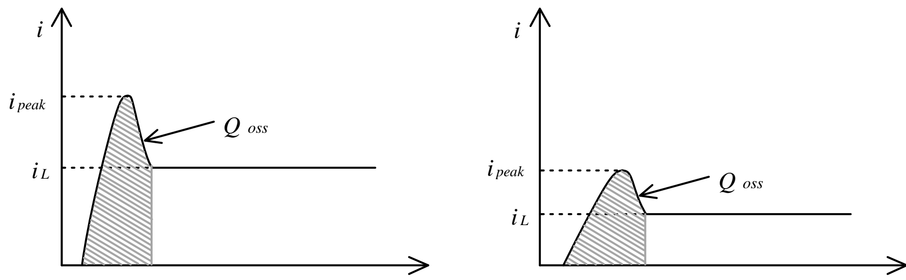


Fig. 4-19: Same Q_{oss} under different I_{load} and different slew rate. [94]

The gate driver circuit from [94] is outlined in Fig. 4-20. Different gate resistances are used in the slow-switching and fast-switching paths to control the switching speed.

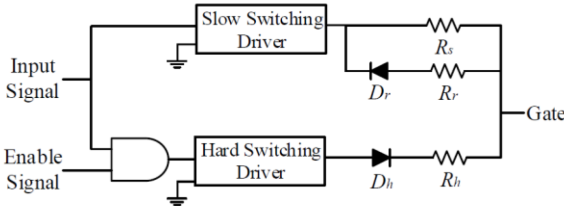


Fig. 4-20 Gate driver circuit arrangement for dual-mode switching from [94].

4.4.4 Research gaps for cryogenic SJ MOSFET converters

In [105] a three-level ANPC inverter using SJ MOSFET has been tested at cryogenic temperature seen in Figure 4-21. The SJ MOSFET had a diode deactivation circuit shown in Table 4-5, however, the paper did not test other deactivation circuits which are to be done in the next sections. The paper has shown that when at CT, the conduction losses have decreased by around 80% compared to those at RT, whereas the switching losses remained almost the same. This thesis takes forward the earlier investigation of Feng [106] into device permutations for SJ MOSFETs and expands it to cryogenic temperature.

Based on the review done, the following knowledge gaps are found when it comes to testing SJ MOSFET at cryogenic temperature;

- Implementing dual-mode control at that temperature.
- Investigation different diode deactivation circuits at that temperature.

Thus the next section shall focus on these gaps.

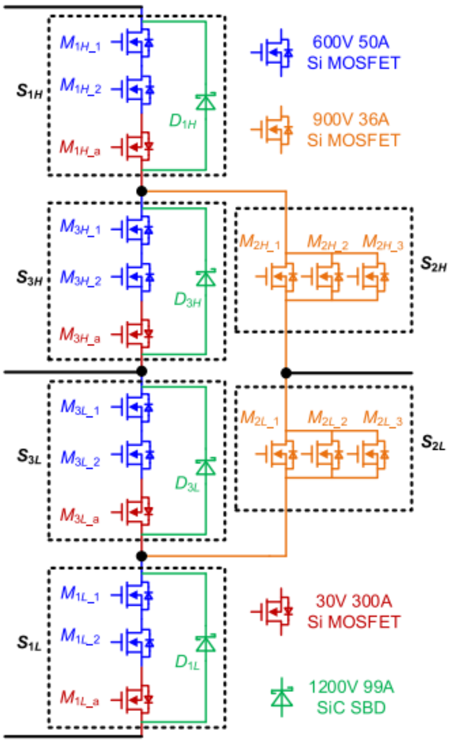


Figure 4-21: Structure of a single-phase three-level ANPC inverter [105]

4.4.5 Phase-leg in converter mode

A phase-leg circuit shown in Fig. 4-22 (a) was constructed. In the circuit, the low-voltage MOSFETs *TS1* and *TS*2 operate in synchronicity with the main MOSFETs *TR1* and *TR2*. The low-voltage MOSFETs prevent freewheeling currents from flowing in the main MOSFETs' intrinsic diodes and incurring high losses attributable to their Q_{rr} charges. Instead, current flows through the external diodes D_{ext1} and D_{ext2}. The problem of capacitive currents still exists, and this is addressed by operating the circuit with the dual-mode control scheme in [94]. The circuit in Fig. 4-22 (a) was connected in the buck configuration in Fig. 4-22 (b), which was run at a duty cycle of 10%. Concerning [100], the circuit is therefore operating in the unipolar mode with a positive output current.

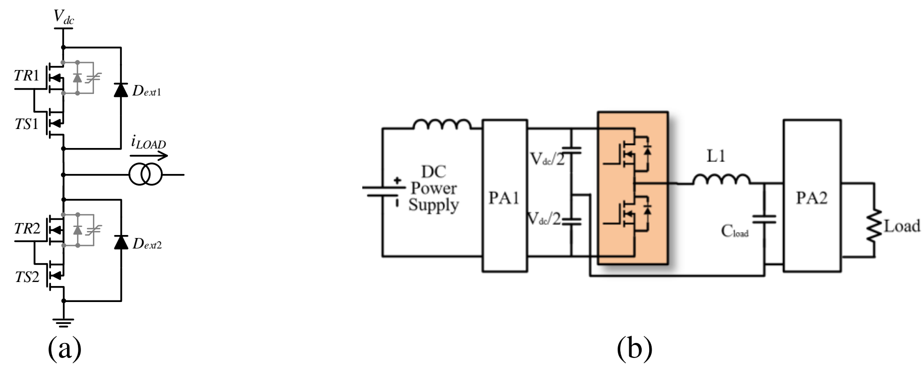


Fig. 4-22: (a) Phase-leg based around MOSFETs with intrinsic diode deactivation circuitry from [96]. (b) Electrical test connections.

Fig. 4-23 shows the physical circuitry used for testing. The gate driver circuit was located remotely and was not submerged in the LN2, hence the lengthy gate driver connections. The output inductance (L_{choke}) and output capacitance were left at room temperature. Applying a tightly-controlled gate-source voltage is challenging due to the stray inductances introduced with this arrangement. However, the gate-source junction of the Si MOSFET is tolerant of a wider voltage range than is the case with SiC or GaN devices. Furthermore, the gate-source threshold voltage of Si MOSFETs rises [97] when the device is cooled from RT to 77 K, yielding improved noise immunity.

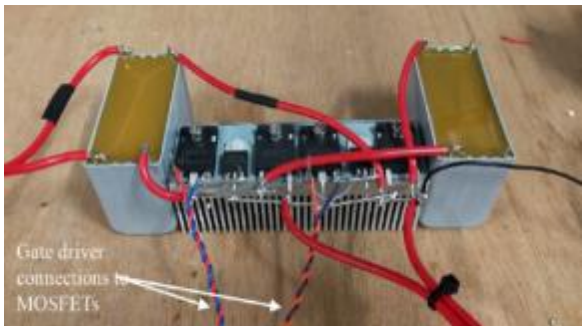


Fig. 4-23: Experimental phase-leg used for testing.

As presented in Fig. 4-22 (b), two PM100 power analysers, PA1 and PA2, were used to measure the input power and output power. Using a low duty cycle is advantageous here as the circuit can be run with a low power throughput, but with full-load current and full-load switching losses. If the losses are inferred from the difference between the measured input power and output power, this enables more accurate loss measurements to be obtained. The inductor L_{in} was included to reduce the high-frequency ripple current drawn from the supply, and thereby enable a more accurate input power measurement to be obtained from PA1.

Initially, the circuit was run at room temperature before immersing it in LN2 for cryogenic testing. Plots of loss against switching frequency with Vdc = 270 V and i_L = 10 A, at both room temperature and 77 K are shown in Fig. 4-24. Losses in the 1-mH output choke (L_{choke}) are included here to obtain higher accuracy reading from the power analyser. The loss in the choke is assumed constant and thus the losses at room and cryogenic temperature are easily comparable. From Fig. 4-24 it can be seen that the losses are lower at cryogenic temperature than at room temperature. This verifies with the work done in Chapter 3 where it was found that the MOSFET on-resistance and switching losses decrease with the decrease of temperature.

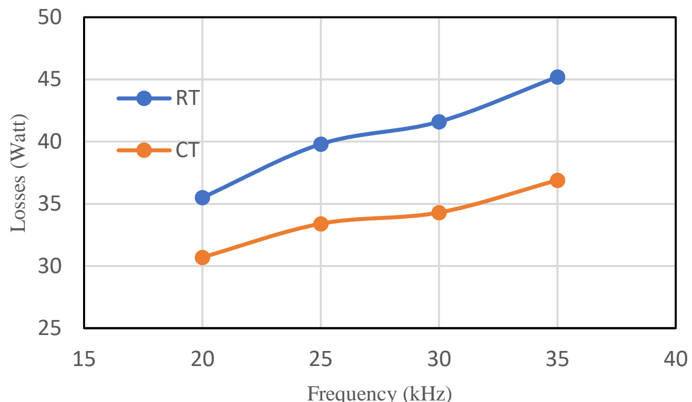


Fig. 4-24: Losses against switching frequency at both RT and 77 K. The circuitry was intentionally run at a low-efficiency operating point to facilitate accurate loss measurements.

Fig. 4-25 shows the efficiency at both room and cryogenic temperatures. The efficiency plotted does not include the cooling losses. From the results shown, it can be seen that cryogenic temperature the efficiency of the phase-leg, when operated in dc/dc mode, has increased. However, they do not include cooling losses, nevertheless, the main purpose is to have an overall system at the same temperature.

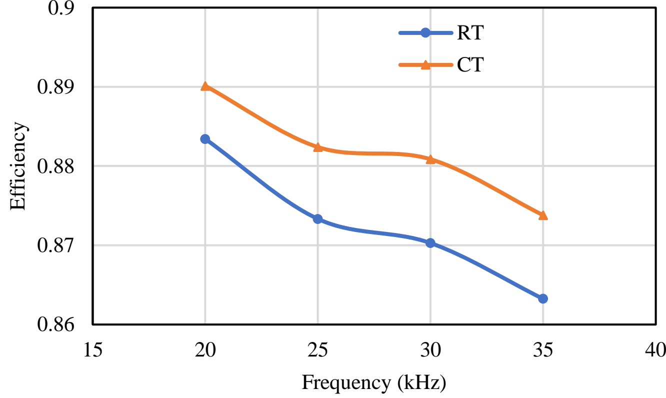


Fig. 4-25: Efficiency against switching frequency at both RT and 77 K. The circuitry was intentionally run at a low-efficiency operating point to facilitate accurate loss measurements

4.4.6 Phase-leg in inverter mode

To understand the performance of the phase-leg in Fig. 4-22 (a) and to use it for dc/ac applications, two different diode deactivation permutations are shown in Fig. 4-26 were assessed to reduce the SJ MOSFET losses. The devices selected for experimentation and their key room temperature parameters are listed in Table 4-4. At first, the performances of these permutations are evaluated in a simulation and after.

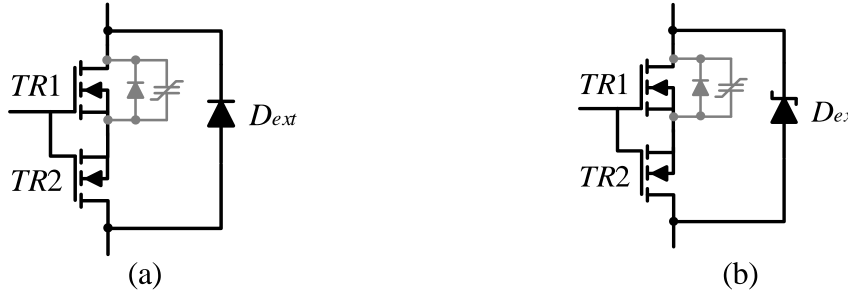


Fig. 4-26:Permutation of diode deactivation circuits for the phase-leg in the next section

Table 4-6 shows different D_{ext} diodes that were experimented with to assess the best performing diode deactivation technique at cryogenic temperature. The diodes were chosen based on the that the SiC Schottky performance is worse at cryogenic temperature, however, the reverse recovery is almost zero, whereas the Fast Recovery Epitaxial Diodes (FRED) diode is Si-based and it was shown in the previous literature that the diodes of the same type have improved performance at cryogenic temperature.

Table 4-6: Different D_{ext} devices used for diode deactivation circuit

Si fast recovery FRED diode (*Dext* in Modules (a))	DSEI30-06A
	V_{RRM} = 600 V
SiC Schottky diode (D_{ext} in Modules (b))	SCS220AE
	V_{RM} = 650 V

4.4.6.1 Simulation of the phase-leg at cryogenic and room temperatures

A simulation was built to estimate the performance of a phase-leg at RT and cryogenic temperature. From Table 4-5. the parameters chosen and set as seen in Table 4-7. As for the diodes DSEI30-06A and SCS220A, their forward voltages were tested at both temperatures. For the MOSFET TR1 the $R_{DS(on)}$ was taken from Table 4-5 the CoolMos MOSFET was tested at room and cryogenic temperature, where the resistance has decreased by 50% at 77 K, as for the $V_{GS(th)}$ extracted from [42] which has shown of an increase by 50% at 77 K.

Table 4-7 Parameters of the devices for simulation.

Device	Room Temperature	Cryogenic temperature
Si super-junction MOSFET (TR1) IPW60R041P6	$R_{DS(on)} = 41m\Omega$	$R_{DS(on)} = 21m\Omega$
	$V_{GS(th)} = 4.5\ V$	$V_{GS(th)} = 6.75volts$
DSEI30-06A Si fast recovery FRED diode (Dext in Modules (a) and (c))	$V_f = 1.5V$	$V_f = 1.65V$
	$Q_{rr} = 1000nC$	$Q_{rr} = 1000nC$
SCS220AE SiC Schottky diode (D_{ext} in Modules (b) and (d))	$V_f = 1.35V$	$V_f = 1.485V$
	$Q_{rr} = 31nC$	$Q_{rr} = 31nC$
IRFB7546PBF Si low-voltage MOSFET (TR2 in Modules (c) and (d))	$R_{DS(on)} = 6m\Omega$	$R_{DS(on)} = 1.2m\Omega$
	$V_{GS(th)} = 3.7\ V$	$V_{GS(th)} = 5.5\ V$

For the D_{ext} DSEI30-06A and SCS220AE diodes, V_f was tested at room and cryogenic temperature shown in Fig. 4-27 (a) and (b) respectively. It should be noted that the

DSEI30-06A diode forward voltage has increased because it is a FRED diode. As for the Q_{rr} the literature has shown no change in it for the fast recovery diodes, thus they have been set to the same value at both temperatures in the simulation.

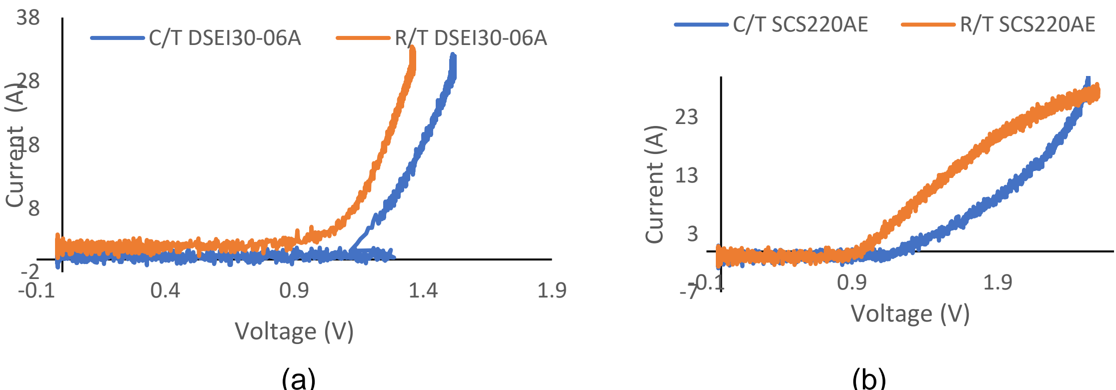


Fig. 4-27 (a) performance of the DSEI30-06A at cryogenic and room temperature (b) performance of the SCS220AE at cryogenic and room temperature

Fig. 4-28 shows the configuration of two phase-leg circuits using the diode deactivation circuits in Fig. 4-27. In Fig. 4-28, a series MOSFET IRFB7546PBF is used with the SJ MOSFET, the only difference is in (a) and Schottky diode SCS220AE is used whereas in (b) a DSEI30-06A Si fast recovery FRED is used as the antiparallel device for both MOSFETs.

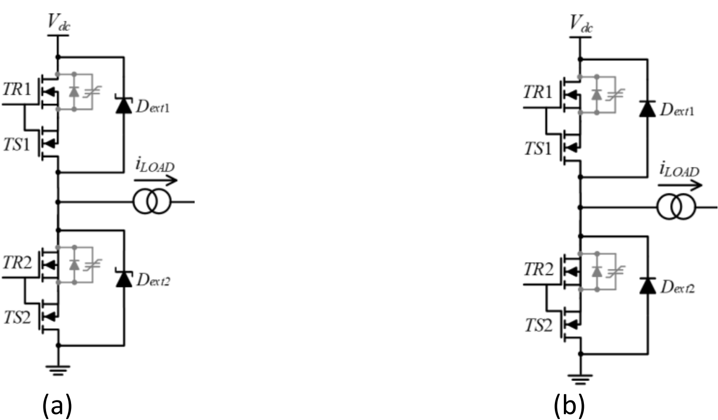


Fig. 4-28 Candidate cryogenic phase leg permutations, (a) using SiC Schottky diode as D_{ext}, (b) using Si diode as D_{ext}.

To simulate the performance of the phase-leg, MATLAB/SIMULINK software was used. For each circuit design in Fig. 4-28 two simulations were run, one for room temperature and one for cryogenic temperature. In all of the simulations, the input and output voltages and currents were measured to calculate the efficiency of the phase at room and cryogenic temperatures. The simulations were run at different power levels: 0.25, 0.5, 0.75, and 1 kW and at different frequencies: 15, 20, 25, 30 and 35 kHz. The simulation results are shown in Fig. 4-29.

Fig. 4-29 shows that the performance of the circuit improves with the decrease of temperature, this can be mainly attributed to the fact that the SJ MOSFET on-resistance has significantly decreased with the decrease of temperature. Even though both antiparallel diodes' forward voltages have increased at cryogenic temperature, the overall efficiency still increased. The difference in the efficiencies between the room and cryogenic temperature is more apparent at larger values of power. In addition, it should

be noted that the SiC diode has shown better performance as it has lower switching losses than the Si diode.

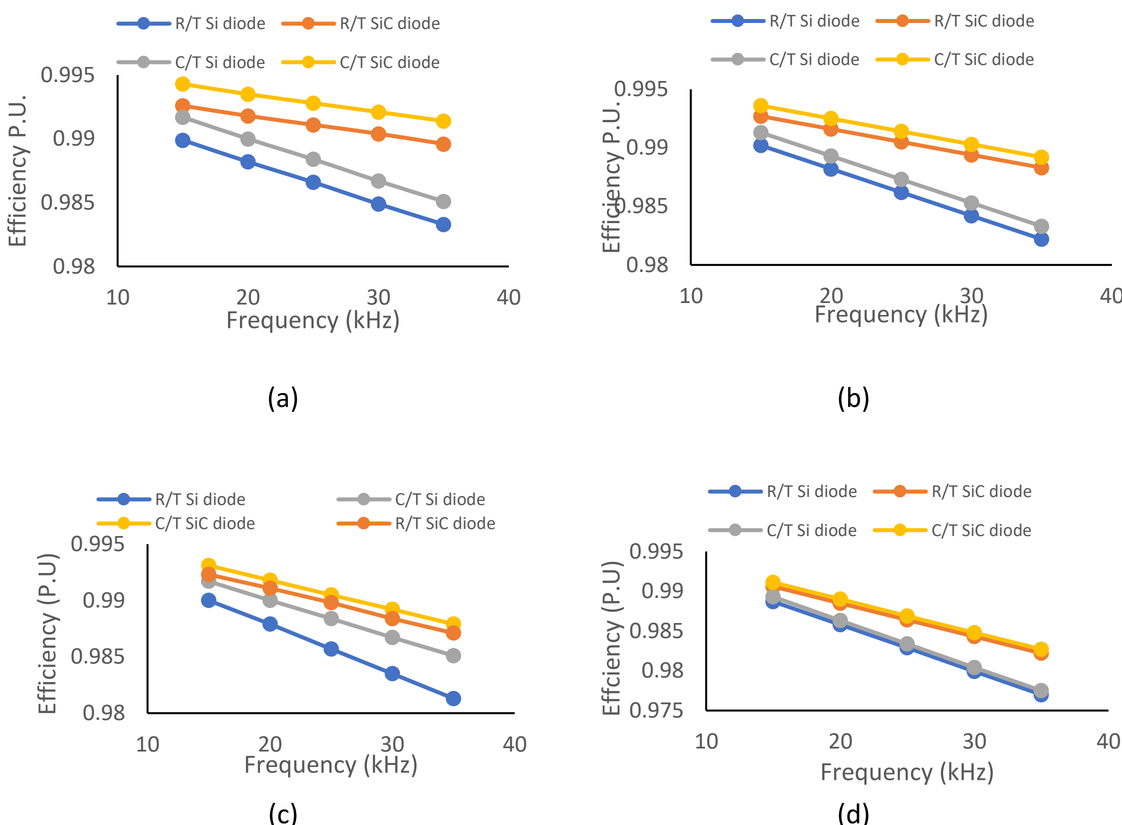


Fig. 4-29 Simulation at different powers (a) 1000 Watts, (b) 750 Watts (c) 500 Watts, (d) 250 Watts at room and cryogenic temperature

4.4.6.2 Cryogenic experimental rig and results

Using the circuit configuration of phase-leg in Fig. 4-28 an experimental rig has been built seen in Fig. 4-23, where it was cryogenically tested by immersing it in liquid nitrogen (LN2). V_{dc} was set to 270 V due to the degradation of the blocking voltages of the SJ MOSFET and the Si fast recovery PN diode when the temperature is reduced to 77 K. Two 50-μF 450-V polypropylene capacitors in parallel were used for local supply voltage decoupling. This capacitor type has shown reliable performance at 77 K, where its

capacitance value does not change significantly [2]. The gate driver circuit was located remotely and was not submerged in the LN2, hence the lengthy gate driver connections. Applying a tightly-controlled gate-source voltage is challenging due to the stray inductances introduced with this arrangement. However, the gate-source junction of the Si MOSFET is tolerant of a wider voltage range than is the case with SiC or GaN devices. Furthermore, whilst not highlighted as significant in Table 4-4., the gate-source threshold voltage $V_{GS(th)}$ of Si MOSFETs typically rises by 15% when the device is cooled from RT to 77 K, yielding higher noise immunity.

The circuit in Fig. 4-23 was connected as shown in Fig. 4-28 and run at a modulation index of 90%. As seen in Fig. 4-23, two PM100 power analysers, PA1 and PA2, were used to measure the input power and output power. The inductor L_{in} was included to reduce the high-frequency ripple current drawn from the supply, and thereby enable a more accurate input power measurement to be obtained from PA1.

Initially, the circuit was run at RT before immersing it in LN2 for cryogenic testing. Plots of efficiency against switching frequency with V_{dc} = 270 V at both RT and 77 K are shown in Fig. 4-30. Losses in the 1-mH output choke (L_{choke}) are included here. The phase-leg was tested at loads of 0.25, 0.5, 0.75, and 1 kW. The performance of the circuit using the Si diode improves at cryogenic temperature. However, the highest efficiencies are attained when a SiC diode is used at cryogenic temperature.

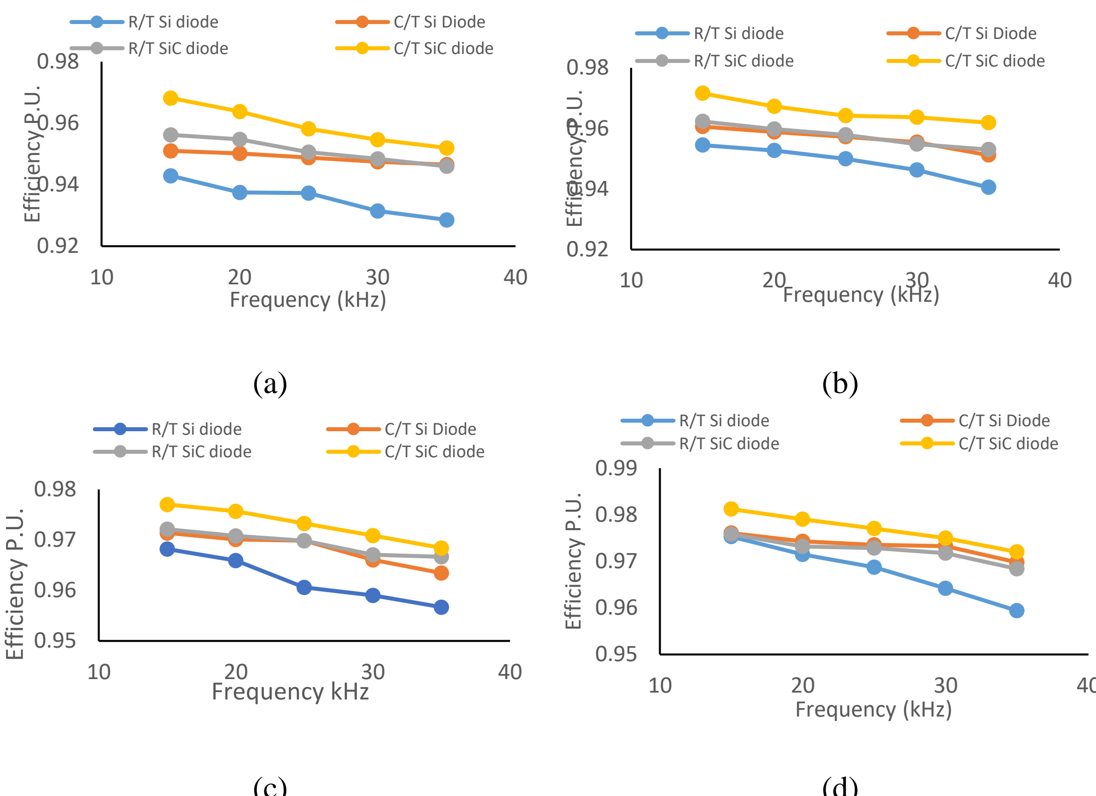


Fig. 4-30 Experimental results at different power outputs (a) 1000 Watts, (b) 750 Watts (c) 500 Watts, (d) 250 Watts

4.4.6.3 Discussion

As expected from the literature, the performance of the phase leg at cryogenic temperature has improved efficiency compared to room temperature. This is mainly attributed to the decrease of the Super-junction MOSFET device on-resistance. The difference in the efficiency between the two temperatures becomes less pronounced at higher loads; mainly due to the larger current emphasising the conduction losses more.

A feature of loss measurement using the power analyser method is that the choke loss is included. For experimental purposes, the devices being tested were in standard TO-247 and TO-220 packages, and appropriate packaging for low temperatures would normally be needed.

The discrepancies between experimental and simulation are displayed in Fig. 4-31 at 1000 W. These can be mainly due to 1) measurement accuracies, 2) interconnection resistances 3) large ripple components in current waveforms, especially at lighter loads and lower frequencies.

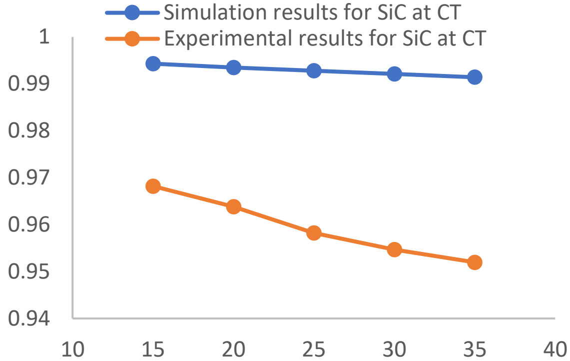


Fig. 4-31: Efficiency against switching frequency at CT showing experimental versus simulation results at cryogenic temperature for 1000 W

4.4.6.4 Summary of phase leg application for all electric aircraft

A two-level voltage source converter phase-leg designed around SJ MOSFETs has been tested at room temperature and a cryogenic temperature of 77 K. To address the problems presented by the SJ MOSFET's intrinsic diode and output capacitance, ancillary power components are used in conjunction with a bespoke control technique. Two permutations were selected for further evaluation at both room temperature and 77 K. Both the simulation and experiment results have shown that the usage of SiC Schottky diode for reverse recovery of the phase-leg exhibits lower losses than using Si diode at cryogenic temperature. The result shows that the SJ MOSFET phase-leg has improved performance

at cryogenic temperature making it suitable to be extended into a full inverter driving the superconducting machine in the all-electric aircraft.

4.5 Contributions

- A three phase rectifier was connected to the machine to verify that the system could applied successfully at such temperature. Diode APT2X101D120J was used to build the rectifier as it has shown that its conduction losses has decreased at cryogenic temperature, thus improving the power density of the system. The rectifier has shown a decrease in losses by 20%.
- Examined the effect of a short circuit on the rectifier on an HTS axial flux machine. Where during the experiment a fault was induced on D4 on the rectifier to assess how would the superconducting be affected and that it would quench and destabilise the performance of the machine and cause large heat dissipation.
- Studied the performance of techniques for deactivation for antiparallel diode for superjunction MOSFET could be successfully applied at cryogenic temperatures. Where two different diode deactivation techniques, one with using SiC Schottky and another using Si diode were tested at room and cryogenic temperature. The experiment results have shown that circuit with SiC Schottky has the highest efficiency at cryogenic temperature.

4.6 Summary

In this chapter, a brief review of the architecture for all-electric aircraft has been done. That review explained the role of cryogenic power electronics in the transmission, where

a generator would be used to supply a cryogenic rectifier that would feed a dc/dc converter that would be used to supply power to the dc/ac inverter. As the main three power converter circuits have been identified, the chapter took on the role of discussing the design and the implementation separately.

The chapter started with assessing the application of the three-phase rectifier for an axial generator with an HTS coil. In this section, the selection of the rectifier diode was done based on the previous experiment that was done in chapter 3. After down-selecting a Si-based device, an experimental rig has been built for testing. The experimental rig was the first to run to rectify a single-phase input to compare the performance of the rectifier circuit at room and cryogenic temperature. The results have shown that the efficiency of the rectifier increases with the decrease of temperature, which was expected as the forward voltage of the rectifier decreases with temperature and hence the conduction losses have decreased with temperature. The three-phase rectifier was placed in liquid nitrogen and was connected to an axial machine with HTS coils where the experiment results have shown good performance at cryogenic temperature. A fault was tested across one of the rectifier modules (D4) to understand the performance of the machine and the rectifier at that temperature during faults and a fault analysis was done. The fault analysis has shown that the HTS coils are very fragile when it comes to faults and require fast protection schemes to prevent their damage.

The chapter later discussed the implementation of a phase-leg using an SJ MOSFET for both dc and ac applications. That section mainly discussed why SJ MOSFET was chosen over other MOSFET types where a quick review was done. This section also discussed

the core problems with SJ MOSFET, which include, 1) the large reverse recovery losses due to the intrinsic diode, which is fixed by adding a diode deactivation circuit and 2) the non-linear capacitance that keeps charging and discharging the capacitor at every cycle, which is addressed by using dual-mode control.

An experimental rig was set up for a dc/dc application, where the experiment was run at 270 V and a comparison between the performances of the phase-leg at cryogenic and the room temperature was made. That comparison had shown that at cryogenic temperature the efficiency is improved, without considering the cooling penalties. However, further studies are needed to understand further the cooling losses of the system to understand the practicality of using a dc/dc converter for all-electric aircraft applications.

The phase-leg was later reconfigured to be set up for use of the dc/ac application. At first different diode deactivation circuits for the dc/ac application were simulated using MATLAB/SIMULINK where the parameters for the simulations were drawn from the literature. The simulation results have shown that the deactivation circuit with SiC Schottky diode performs better than the Si diode one at both room and cryogenic temperatures. This result can be attributed to the fact that SiC Schottky switching losses are almost negligible in comparison with the Si diode and hence that explains these results. Afterwards, an experimental rig of both phase-leg circuits was set up to be tested at room and cryogenic temperature to verify the simulation results. The experiment confirmed the simulation results of identifying that the best circuit for diode deactivation at cryogenic temperature is the one that utilises the SiC Schottky diode.

Chapter 5

dc/dc converters for superconducting magnet applications

As discussed in Chapter 1, several applications including MRIs, Maglev trains and nuclear fusion reactors require the use of large magnets to fulfil the need to provide a large current to reach the target magnetic field. Thus in this chapter, we focus on designing and building a cryogenic dc/dc converter to supply these applications with low ripple.

5.1 Introduction

Superconducting magnets are now found in a variety of applications such as 1) medicine, where they are used in MRIs, 2) accelerator magnets in nuclear fusion, and 3) levitation systems for high-speed tracks and trains [30]. These magnets require currents up to 80 kA [107], and thus bulky current leads are needed, which can reduce the efficiency of the cooling system.

Literature has investigated the use of different current leads for cryogenic applications [107]-[109]. In [107] explained the setup made for current leads with a rating of 80 kA to supply ITER coil. Typically an HTS current lead shown in Fig. 5-1 is needed for the cryostat. The designed current lead consists of three parts; 1) a large copper busbar module in a heat exchanger is connected to 2) an HTS module that is connected to a

superconducting magnet. In that setup, a heat exchanger is required to cool down the large copper busbar. The dimensions of the heat exchanger used in [107] are not shown.

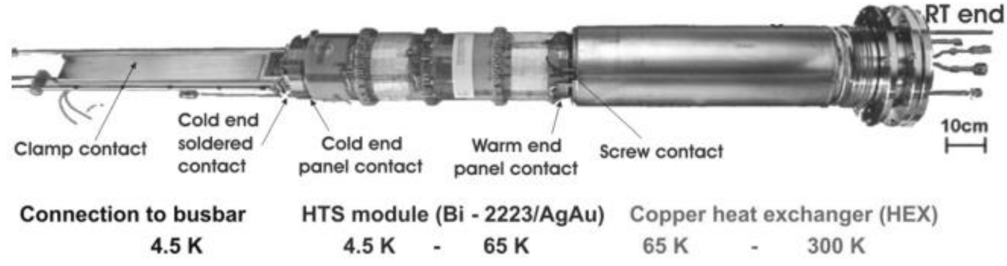


Fig. 5-1: HTS current lead comprises three parts, left-hand side: connection to the busbar, middle part: HTS module, right-hand side: heat exchanger [107]

The size of the heat exchanger is large and the power from the heat leakage of the system are high, thus making the system both complex as seen in Fig. 5-2 to install and costly to run as it requires cooling the large copper bars.

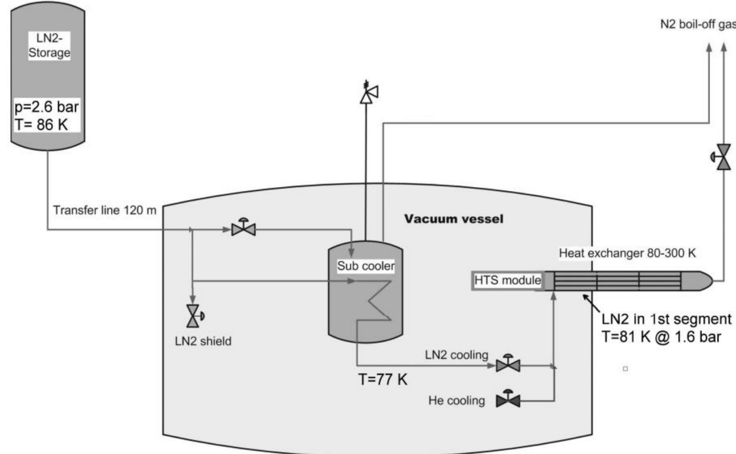


Fig. 5-2: Flow scheme for cooling the current leads [107]

To avoid using large conductors for current transportation, there are other options mentioned in the literature. In [28], [29], HTS superconductor switches have been proposed, where, as explained in Chapter 2, the circuit would be placed at the cryogenic temperature and small size wire leads would be required. However, with using HTS switches, there are several drawbacks which include; slow switching and large harmonics content. Thus in [29], it was recommended to use a MOSFET device over HTS switches.

Fig. 5-3 (a) shows the circuit proposed in [29], where the input is rectified using a three-phase uncontrolled rectifier that lies in the warm region as seen in the figure. The rectifier is then connected to a stepdown asymmetric H-bridge that lies inside the cryostat. By stepping down the voltage inside the cryostat, the input current leads can be smaller, thus reducing the size requirement for the heat exchanger. This setup has much lower complexity and operating cost than seen in the previous literature [106] as shown in Fig. 5-1 and Fig. 5-2.

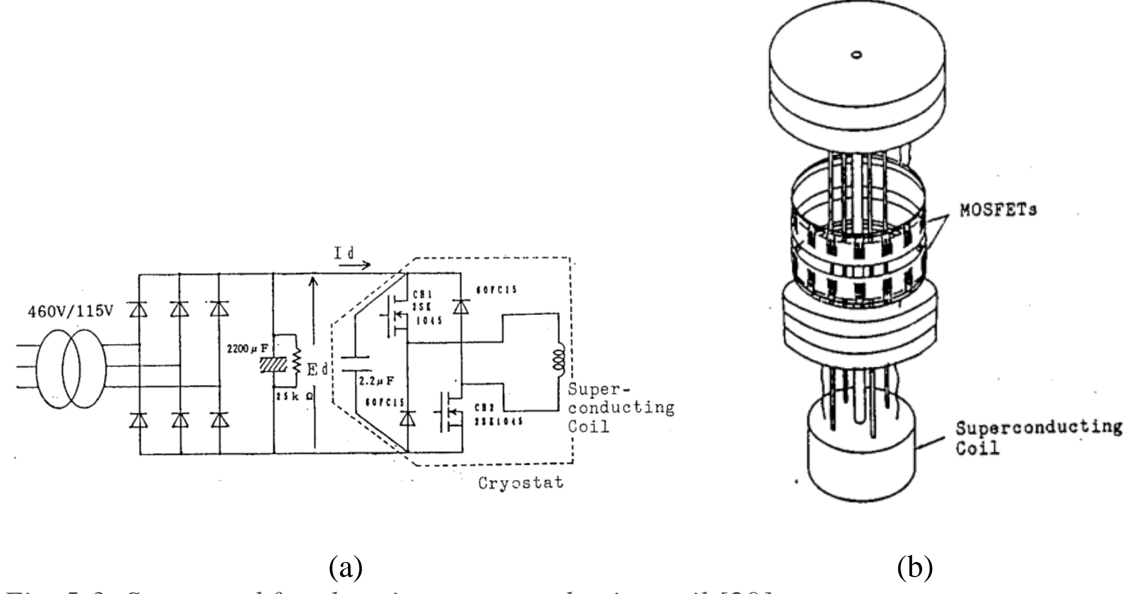


Fig. 5-3: Setup used for charging superconducting coil [29]

The purpose of this thesis is to follow the setup suggested in [29] and design a converter that requires smaller current leads on the warm side and can supply a current up to 500 A on the cryogenic side. The purposed setup is shown in Fig. 5-4. This is done to transfer the power over higher voltage and lower current at the warm temperature and step up the current in the cold zone to reduce the current lead conductor size at the input. Thus, the conductors at the entry point have a relatively much smaller cross-sectional area with a consequently reduced thermal conductance and heat flow into the cold zone [110].

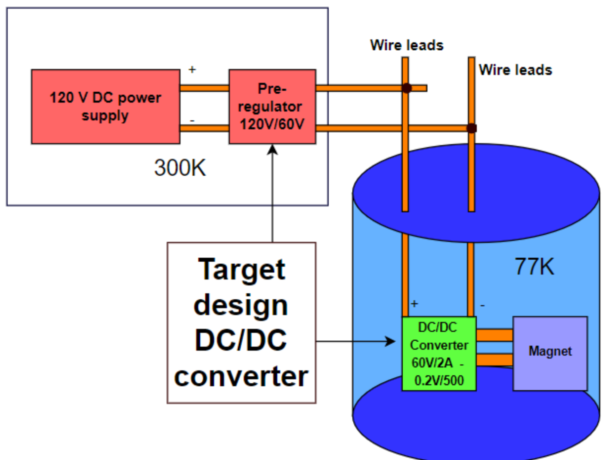


Fig. 5-4: Overview of the system architecture

Conversion to a high current takes place in the cold zone, where the advantage is the lower resistivity of copper or superconductors, and the generally improved parameters of semiconductor devices, such as the reduced on-state resistances of MOSFETs [6]-[8]. As seen in Fig. 5-4, the power converter is physically distributed over the warm (300 K) and cold zones (77 K). Because of reliability concerns in the semiconductor switches and passive elements at cryogenic temperatures, it is desirable to have a minimal number of

components in the cold zone. This thesis describes the development of a converter for supplying 500 A into a superconductor cooled with liquid nitrogen and therefore operating at 77 K. The target load to be driven is represented by a 1-mH inductance in series with a voltage sink. The maximum allowable peak-to-peak current ripple is specified at 5% of the rated value.

5.2 Research gaps in cryogenic converters

The purpose of this section is to review cryogenic converters and the auxiliary circuits, this shall be done by reviewing the following;

1. The efficiency of cryogenic converters.
2. The performance of control circuits at cryogenic temperature.
3. The paralleling of semiconductors at cryogenic temperature.

5.2.1 The efficiency of cryogenic converters

Several papers have discussed the usage of converters at a cryogenic temperature [111]–[116], where the efficiency of various converters was discussed at cryogenic temperature. In [112] the efficiency of the dc/dc buck converter rated at 28 V output and 175 W has been measured at room and liquid nitrogen temperature, the converter utilised IRFP250 Si MOSFET as its switch. The results have shown the efficiency of the converter has increased from 95.8% at room temperature to 97% at liquid nitrogen temperature. In [112], the controller remained operating outside the cold zone at room temperature.

In [112]–[116] the efficiencies of converters are measured at different temperatures as seen in Figure 5-5. The converter specification [111], [112] is for a MOSFET converter

rated at 12 V output, 60 W three-level buck converter. For [113] a GaN HEMT converter rated 45-V output 1000 W, and for [115] MOSFET converters rated 5 V output 10 W. It can be noted that at very low power output the efficiency of the converter decreases at a cryogenic temperature which is similar to the case of operating lighter loads at room temperature. At higher power (higher current); the resistance becomes more dominant in terms of power losses. This has been verified in [112]–[116] where the efficiency of the converter has decreased at cryogenic temperature when operating at low power. This can be seen more clearly in Figure 5-5 that the converter in [116] utilising CMOS, where the converter has lower efficiency when operating at current output of 36 W (0.5 A) than when it is operated at 288 W (4.0 A). In [116], which utilises GaN as the switching device, there is a slight increase in efficiency at cryogenic temperature Figure 5-5.

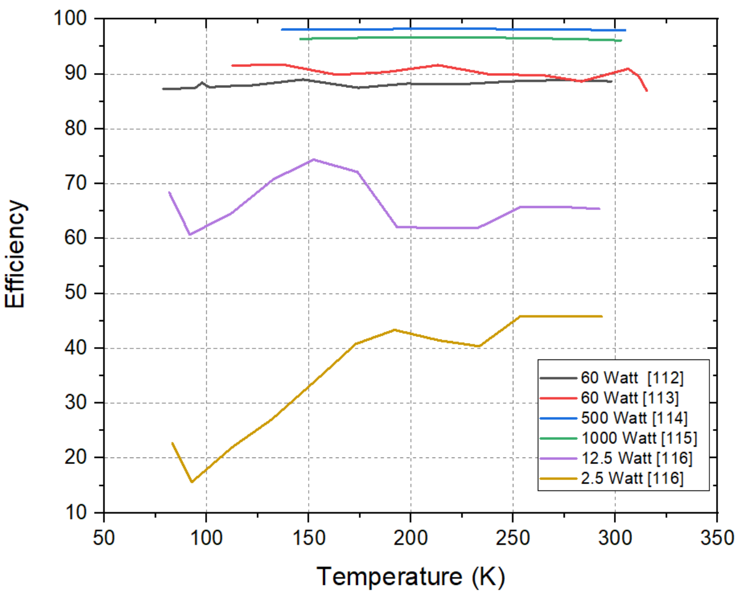


Figure 5-5: Efficiency of the converter vs temperature evaluated in the literature

5.2.2 Performance of control circuits at cryogenic temperature

In [112] the implemented control circuit consisted of two CMOS 556 timer ICs, CMOS logic ICs, and two CMOS high-side driver ICs (IR 2110). In [115] the controller used was the C2000 Texas Instruments TMS320F28069 microcontroller with gate driver Texas Instrument LM5113. The controller circuit in [97] consisted of 8051 microcontrollers and CMOS MOSFET as they have proved their robustness at cryogenic temperature. Two different PWM chip technologies, bipolar and CMOS were tested at a cryogenic temperature [38]. In total, four ICs were tested as seen in Fig. 5-8, where both the bipolar technology chips did not work below 130 K. One BiCMOS chip was able to function below 100 K. The study also showed that the bipolar technology ICs exhibited large noise when operated at cryogenic temperature. The same results were shown in [43] where the bipolar-based IC cease operating when the temperature drops below 163 K. However, these ICs will readily recover and commence working once their temperature rises again. The CMOS based IC tested in [117] were able to operate until 88 K. The following results were deduced from the experimentation, 1) the switching frequency has slightly increased with the decrease of temperature, 2) the supply current has been almost doubled at cryogenic temperature, 3) there is a slight decrease in duty cycle at lower temperatures which can be addressed using closed-loop control.

The cooling energy of the converter has been discussed in [97], [118]. Where in [97] it has been highlighted that the total losses of the converter at 85 A would be just under 5 W. It was mentioned in [118] that the cryocooler's efficiency range from 10-30 %, which will

be attractive at a high power rating, whereas a 1-MW converter with 99.7% efficiency would have an efficiency of 95.5% if the cooling losses are included at an efficiency 8:1.

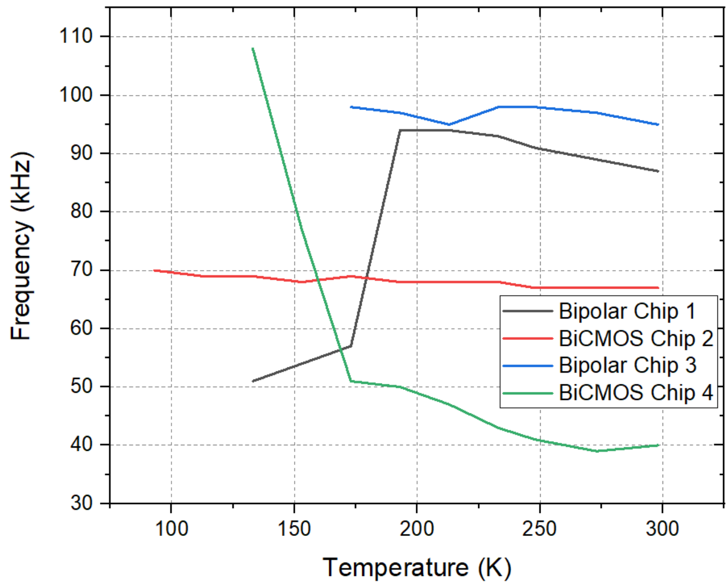


Figure 5-6: PWM ICs operating frequency vs temperature [97]

5.2.3 Paralleling of semiconductors at cryogenic temperature

Literature has placed the switching devices in parallel in the converter to gain improved performance [97], [119],[120]. In [97] an H-Bridge made up of an array of ten MOSFETs connected in parallel was tested at cryogenic temperature as seen in Figure 5-7. The test results have shown a reduced MOSFET resistance, which effectively has reduced the conduction losses. In [120], two power MOSFETs were connected in parallel, to improve the performance of the converter. The experiment results have shown good current sharing, where the current in the negative cycle is shared between the two MOSFETs.

The operation of MOSFET in parallel might cause a current imbalance between them, as any discrepancy between them might be reflected in the MOSFET characteristics such as

on-state drain-to-source resistance, threshold voltage, and input-to-output transconductance, gate-to-drain capacitance. One of the particular issues that arise with MOSFETs in parallel is currently sharing as the on-state resistance has been provided in datasheets with a tolerance of up to 30%, not to mention that the junction temperature has a great effect on that resistance [121]. It is argued that if the resistances are not equal at cryogenic temperature, one MOSFET would heat up, increasing its resistance and causing the current to flow in the other MOSFET till the temperature stabilises. However, still, further research on paralleling cryogenic MOSFETs is essential to test the variation of the characteristics of MOSFETs of the same type at cryogenic temperature.

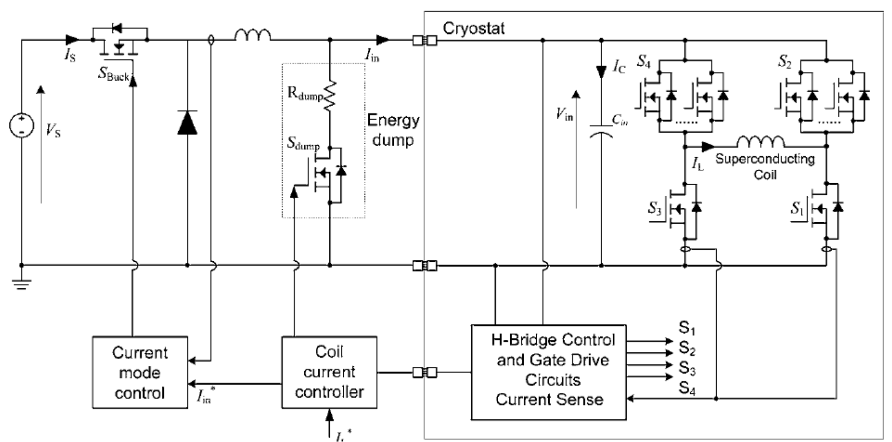


Figure 5-7: H-bridge with paralleled MOSFETs for superconducting coil control [97]

5.2.4 Summary

From that review, it can be deduced that dc/dc converter can function well at cryogenic temperature and that the conduction losses become more dominant at that temperature. It was also found that controllers at lower temperatures do not function effectively and some

ICs tend to shut down at lower temperatures, thus the controller is preferred to be at room temperature. The review has also shown that MOSFETs can be paralleled easily for dc/dc converter applications as they had good current sharing among the paralleled devices.

5.3 Selection of topology

As mentioned in the introduction, the purpose is to have a small current in the warm zone converted into a large current after the system enters the cryogenic zone. The step-up in current is realized with a magnetic component having a large turn ratio, with a minimal number of components in the cold zone is desirable.

A buck converter would normally be used for voltage step-down applications. However, the extremely low duty cycle and high RMS currents are problematic in this application because of reduced efficiency and difficulties with control. Alternative possibilities, shown in Fig. 5-8, considered here are:

- Forward converter
- Flyback converter
- Tapped-inductor (TI) buck converter [122].

These are all simple single-ended circuits. It is noted that, at high load currents, the rectifier diodes in the circuits in Fig. 5-8 will be replaced by MOSFETs acting as synchronous rectifier (SR) elements.

A challenge is to minimize the ripple content in the current i_{out} in the load. The current ripple is defined as the difference between the highest and lowest current values in a

waveform. As shown in Fig. 5-8, the flyback and TI converters have a high output current ripple and the forward converter has the lowest current ripple. Normally, a filter capacitance is connected across V_{out} to remove the bulk of the ripple current from i_{out}, but the difficulty lies in identifying a capacitance type with the required capacitance per unit volume for cryogenic temperatures, and without excessive losses [2]. The next part is mainly focused on making a thorough comparison between the three circuits.

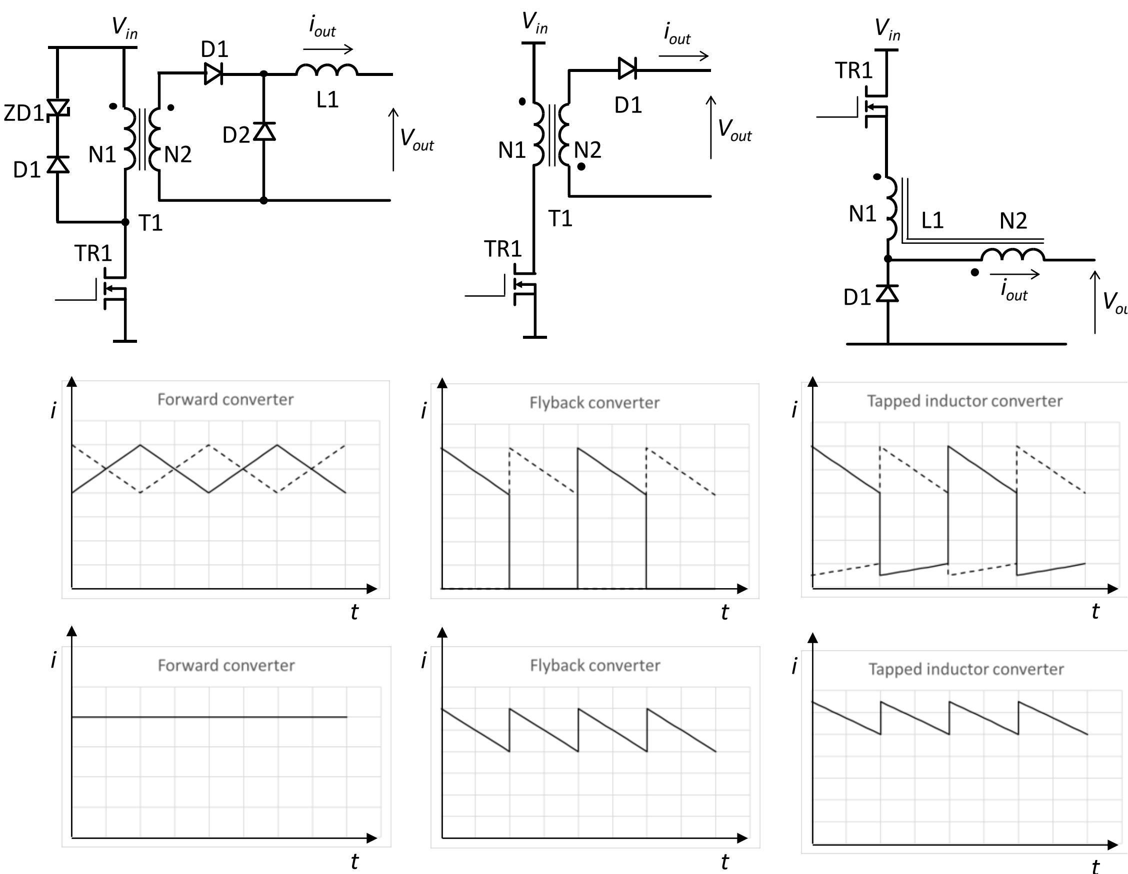


Fig. 5-8: Single-ended converters. Top: Schematic diagrams. Centre: Output current from one unit (solid line) and output current from a second unit switching out of phase (dashed line). Bottom: Total output current from two interleaved units in parallel with each operating at 50% duty cycle.

The following points are considered for identifying the best converter suitable for superconducting magnet applications.

- The forward converter has the lowest output ripple current when compared to the flyback and TI converters. This is mainly due to the effective ripple cancellation seen in Fig. 5-8. Thus using the forward converter at cryogenic temperature would get rid of the requirement of using capacitors at the cryogenic zone, increasing the power density of the circuit.
- Interleaved power converter stages can be used to reduce the output current ripple. With the forward converter in the continuous current mode, the ripple in the aggregate i_{out} can be virtually eliminated by operating units in parallel at a duty cycle of $1/n$ or $1-1/n$ each [123] where n is the number of units. In [124], a pre-regulator buck converter stage varies the input voltage applied to units in parallel. This pre-regulator buck converter allows parallel forward converters to be operated at a fixed duty cycle for zero output current ripple in i_{out}, but with the total i_{out} being controlled by adjusting the input voltage. The forward converters' input voltage, v_1 in Fig. 5-8, is adjusted by the pre-regulator side, which is done by changing the duty cycle of the converter, which in turn controls v_1. The addition of the pre-regulator simplifies the circuit in terms of control and results in a low output current ripple. However, with the flyback and TI converters, complete elimination of the ripple current is not possible in this way. Other interleaved circuits include those such as [125], where resonant converters are used, although complexity is increased.

- The TI buck converter, whilst used in a high-current application in [126]. The circuit was tested to step down the voltage from 48 V to 6 V where large current output was produced. However as seen from Fig. 5-8, the circuit has no inherent input-output isolation, thus in case of faults, the current can be transferred to the supply risking higher damage.
- Feasible core options for chokes or flyback transformers at cryogenic temperatures are iron powder materials, or gapped nanocrystalline materials [2], [127]. For voltage transformers, nanocrystalline materials are suitable.
- Two SR elements are needed for the forward converter, but two SR elements are not necessarily more problematic than one as the silicon utilization is essentially similar. If the average output current I_{ave}, then the total conduction loss W_{cond} only in the MOSFETs is given by;

$$W_{cond} = R_{DS(on)} {I_{ave}}^2 \tag{5-1}$$

  where R_{DS} is the MOSFET on-state resistance in each location. The conduction loss and I_{ave} are frequency independent. For a flyback converter operating at 50% duty cycle, the rectifier has to conduct an RMS current equal to I_{ave} multiplied by √2. The RMS current squared, therefore, rises by a factor of two, and if the same silicon is located in the one rectifier location, the loss is the same.
- Two SR elements need to be driven in the forward converter, but simple circuitry can be used for this [128].

- Although the forward converter needs an output choke, at very low output voltages there is the possibility of using stray inductances to realize this function.
- Ideally, only the forward converter needs a reset circuit, as formed by D1 and ZD1 in Fig. 5-8. However, in practice, similar circuitry is needed in the flyback and TI converters to limit over-voltages due to currents being commutated in their magnetic component's leakage inductances.

Table 5-1 shows a summary of the comparison between the three different types of converters investigated for the dc/dc application. From the table it can be seen that whilst the forward converter appears to need more components in the cold zone, the rectifier requirement is not more onerous, and a discrete output choke may not be needed at low voltages. To achieve ripple current cancellation an interleaved forward converter arrangement was selected.

Table 5-1: Comparison between different types of converters

Parameters	**Forward converter**	**Flyback converter**	**Tapped inductor converter**
Isolation	Yes	Yes	No
Output capacitor required	No	Yes	Yes
Number of semiconductor switches	Two	One	One

5.4 Proposed scheme

TR1 and TR2 in each of the forward converters in Fig. 5-9 operate at a fixed duty cycle of 50%, but 180° out of phase with each other. This gives, ideally, zero output ripple current. The aggregate output current is controlled by using the pre-regulator buck

converter formed by TRin, Din, Lin, and Cin to vary v_1. The core fluxes in T1 and T2 are reset using the paths presented by Dr1 and Dr2, to recover the energy. The circuit is designed so that the full output current can always be obtained with v_1 being less than half of v_{in}. This ensures a complete reset of T1 and T2, as a sufficient reverse volt-second product is always available across their primary windings when TR1 or TR2 are off.

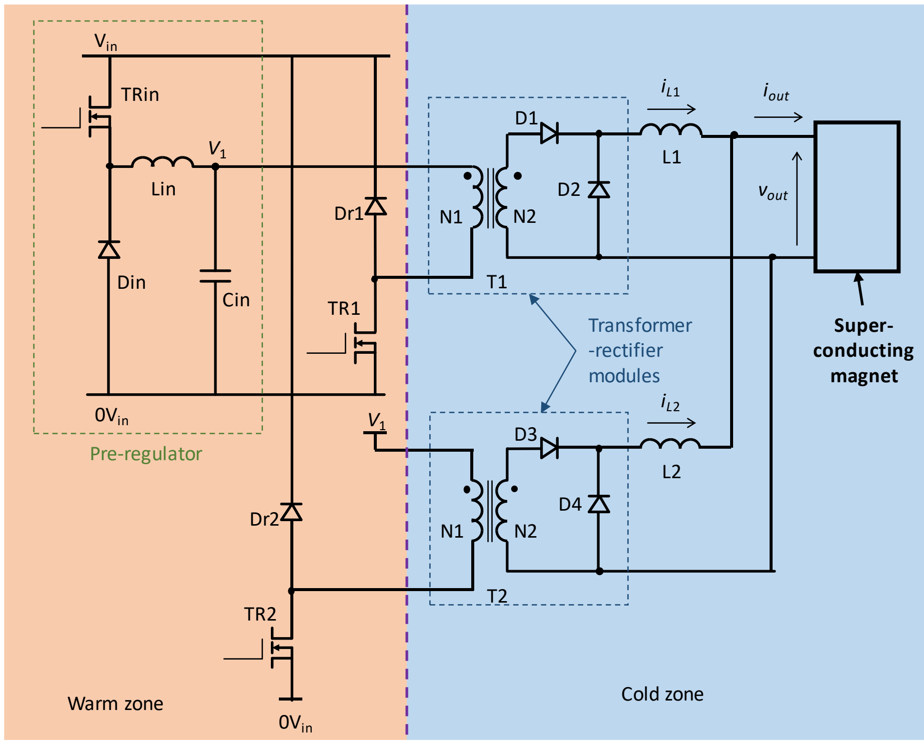


Fig. 5-9: Proposed scheme. For simplicity, D1-4 are depicted as passive diodes without synchronous rectification in this diagram.

For simplicity, the output rectifiers and freewheeling devices are shown as passive diodes in Fig. 5-9. However, synchronous rectification (SR) is mandatory in high-current applications to minimize losses.

5.5 Design of gate-driver circuit

Three main options are available for driving the gates of SR MOSFETs; control-driven, self-driven and current-driven SR. In control-driven SR the MOSFETs are driven with signals from the circuit producing the drive signals for the primary power devices. For self-driven SR [129], the gate is driven by an existing winding, or auxiliary winding, on a magnetic component as seen in Fig. 5-10. A difficulty occurs when voltage variation occurs across the winding due to changes in the converter's input or output voltages. In current-driven SR [130], the MOSFET's drain current is detected through a current transformer, however, this can be physically difficult to implement around high-current conductors.

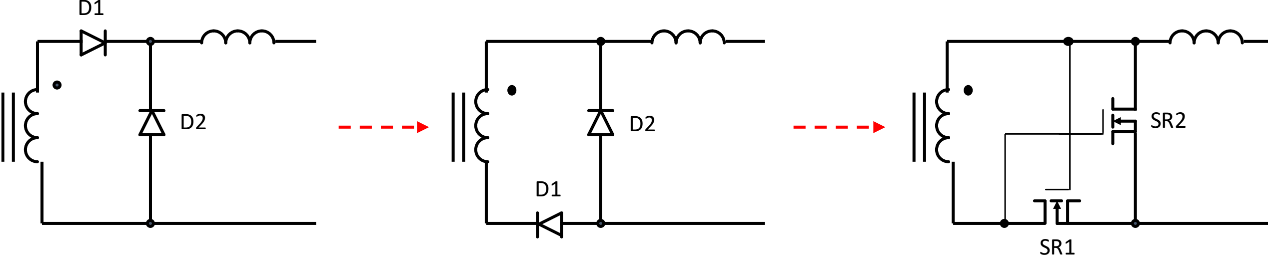


Fig. 5-10: Rectifier arrangements for a forward converter. Left: diodes in common-cathode configuration. Centre: D1 shifted so that the diodes are in a common-anode configuration. Right: D1 and D2 were replaced with SR1 and SR2 respectively to realize a synchronous rectifier circuit.

In this thesis, the SR elements were driven via a transformer-isolated control signal to address the problem of a large voltage range that would be present with self-driven SR. Transformer isolation was used to provide noise immunity.

So that only one secondary winding is needed on the transformer, a secondary-side circuit similar to the single-winding self-driven SR arrangement in [128] was used. Three variants of the driver circuit are shown in Fig. 5-11.

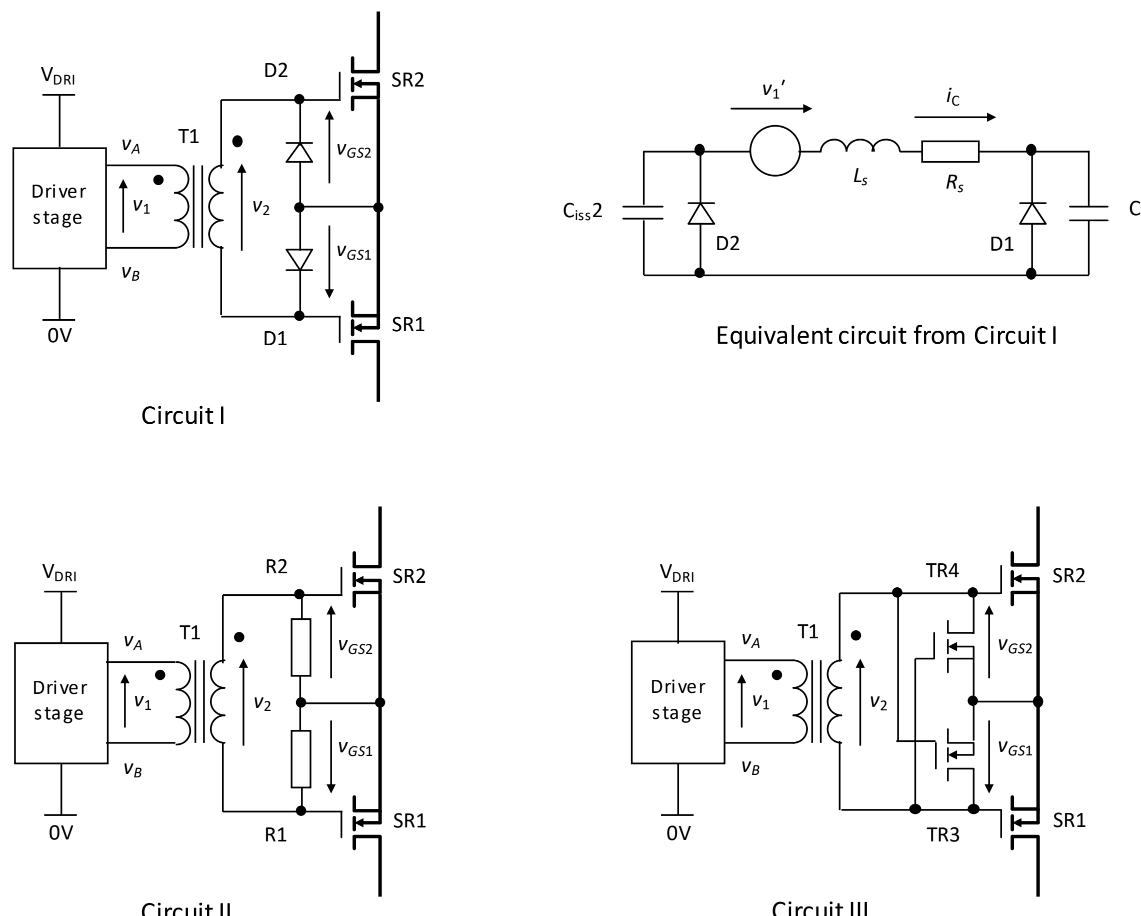


Fig. 5-11: Variants of single-winding self-driven SR arrangement in [128] are considered for driving synchronous rectifier elements as used in the transformer-rectifier modules in Fig. 5-9.

From Fig. 5-11 Circuit I, current flows through R_s when the gate capacitances charge and discharge. R_s represents the resistance of T1's secondary winding in series with the

referred resistance of its primary winding and the driver output impedance. There are stray inductances and transformer leakage inductances, lumped as L_s, between v_1 and the gates being driven. Ideally, the off-state v_{GS} should be zero, but L_s can lead to non-zero v_{GS} [128]. In Circuit II, the off-state v_{GS} is now negative and half of v_2, which is well below the MOSFET's threshold v_{GS}. T1 needs twice the number of secondary turns to obtain the same on-state v_{GS}. In Circuit III the auxiliary signal transistors are used to clamp v_{GS} to zero. This addresses resonances but reduces efficiency.

5.6 Experimental circuit design

A switching frequency f_{sw} of 10 kHz was selected for the forward converters in Fig. 5-9. T60004-L2063-W627 cores in *VITROPERM 500 F* nano-crystalline material [131] were used for T1 and T2. A nano-crystalline material was selected as it has good performance at cryogenic temperatures. Permeability and saturation flux density rise, and losses only increase moderately [2]. N_1 had 100 primary turns and N_2 was formed from one turn. With an output voltage of 50 mV and a duty cycle of 50%, the required voltage V_1 is 10 V.

$$B_{sw} = \frac{V_2(1-\delta)}{N_2 A_e f_{sw}} \qquad 5\text{-}2)$$

Using secondary-side quantities, the peak-to-peak flux density excursion B_{sw} is given by

where A_e is the core's effective magnetic path area which is specified as 94.9 mm^2 in [131]. Putting this and the other data into Equation (5-2) gives B_{sw} = 26.3 mT. In practice, a much higher B_{sw}, and V_1, are expected due to the output voltage needed to overcome the SR MOSFET's on-state resistances, transformer winding resistances, and the resistances of interconnections within the circuit.

Discrete chokes were not used for L1 and L2 in Fig. 5-9. Instead, the circuit's stray inductances were used to realize this function, as discussed earlier.

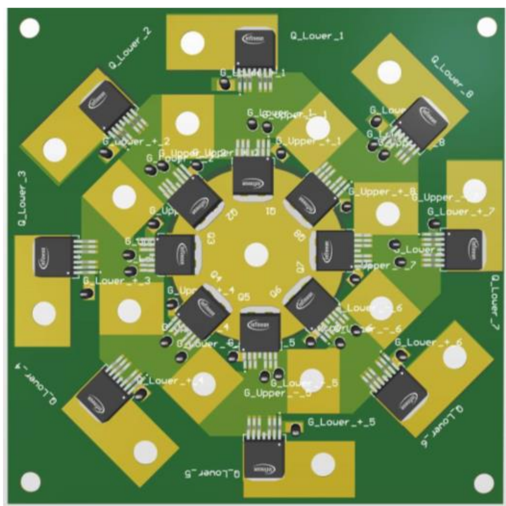
Si MOSFETs and GaN HEMTs show decreased on-resistance of approximately 80% at cryogenic temperature, whereas SiC MOSFETs exhibit increased resistances of approximately 300% [2]. GaN HEMT is known to exhibit the kink effect at a cryogenic temperature, where deeper studies are needed [59]. Also, Si MOSFET has proven reliability in dc/dc converters operating at cryogenic temperatures [132]. The SR devices were selected to be IRL40SC228 MOSFETs, mainly due to the high current requirement and low voltage blocking requirement. These have a typical $R_{DS(on)}$ of 500 μΩ at 25°C. Si MOSFET on-resistance will decrease by 80% [2], $R_{DS(on)}$ of the device is expected to fall to 170 μΩ at 77 K. Eight MOSFETs in parallel were used for each D1-4 in Fig. 2. This gives an effective R_{DS} of 21 μΩ.

For the gate driver, based on the discussion in the previous section, Circuit II in Fig. 5 was selected for driving the SR devices. T1 was constructed with a *Hitachi Metals* MP1903M4AS toroidal core in the 2714A-type *METGLAS®* amorphous alloy [133]. This material has a square-loop, high permeability characteristic, and a saturation flux density B_{sat} of 570 mT. A peak excursion B_{pk} of 400 mT was allowed for, below B_{sat} by a margin of 170 mT. V_{pri} is the voltage applied to N1, which was 12 V. As mentioned in the previous section, the transformer was included for isolation purposes, and not to step a voltage up or down. N2 was therefore made equal to N1. To limit the flux density to B_{pk}, N1 is given by

$$N_1 = \frac{V_{pri}}{4 f_{sw} B_{pk} A_e}. \quad (5\text{-}3)$$

A_e is specified as 8 mm^2 in [133]. Putting this and the other data into Equation (5-3) gives N_1 = 94 turns. N_1 and N_2 were of 0.2-mm diameter copper wire with polyurethane insulation, and the core was found to accommodate 98 turns when both N_1 and N_2 were wound onto it in a single layer, and this number of turns was used. R1 and R2 were both 1-kΩ. Rectangular copper bar conductors measuring 6 mm by 20 mm were used for the load to emulate a superconductor with low resistance.

Fig. 5-12 shows one of the PCBs on which each of the 250-A transformer-rectifier modules is constructed and a built-up module. The sixteen MOSFETs are in a symmetrical layout to enhance current sharing and are physically close to the transformer core to mitigate leakage inductances. Fig. 5-12 also shows a built-up module. The single secondary turn is formed with copper rods and sheets. Wire loops could be arranged around the core and soldered onto the PCB. However, because of breakages due to the expansion and contraction of the wire, the arrangement with mechanical fasteners in Fig. 5-12 was preferred when cycled over a wide temperature range.



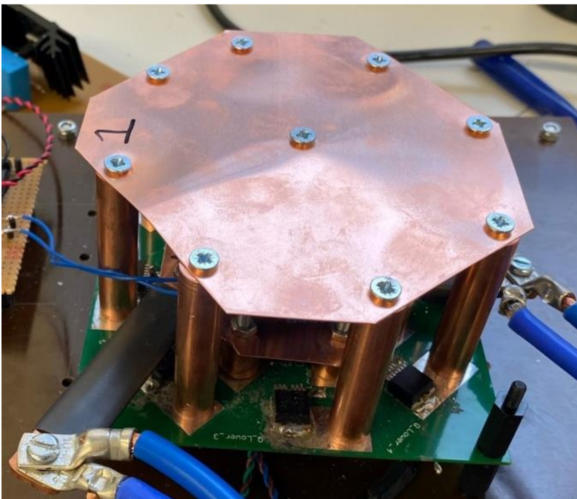


Fig. 5-12: Transformer-rectifier module Left: PCB for accommodating a module. Right: Built-up module.

Fig. 5-13 shows the experimental rig. The control of the system is implemented as an open loop. Function generators were used to provide the three control signals, one for the pre-regulator buck converter, and two for the forward converters. The control signal for the buck converter was set to a value to allow the maximum current output possible from the converter. As for the two control signals output to the forward converter were set to a constant duty cycle of 50 %, and in anti-phase, to obtain successful interleaving.

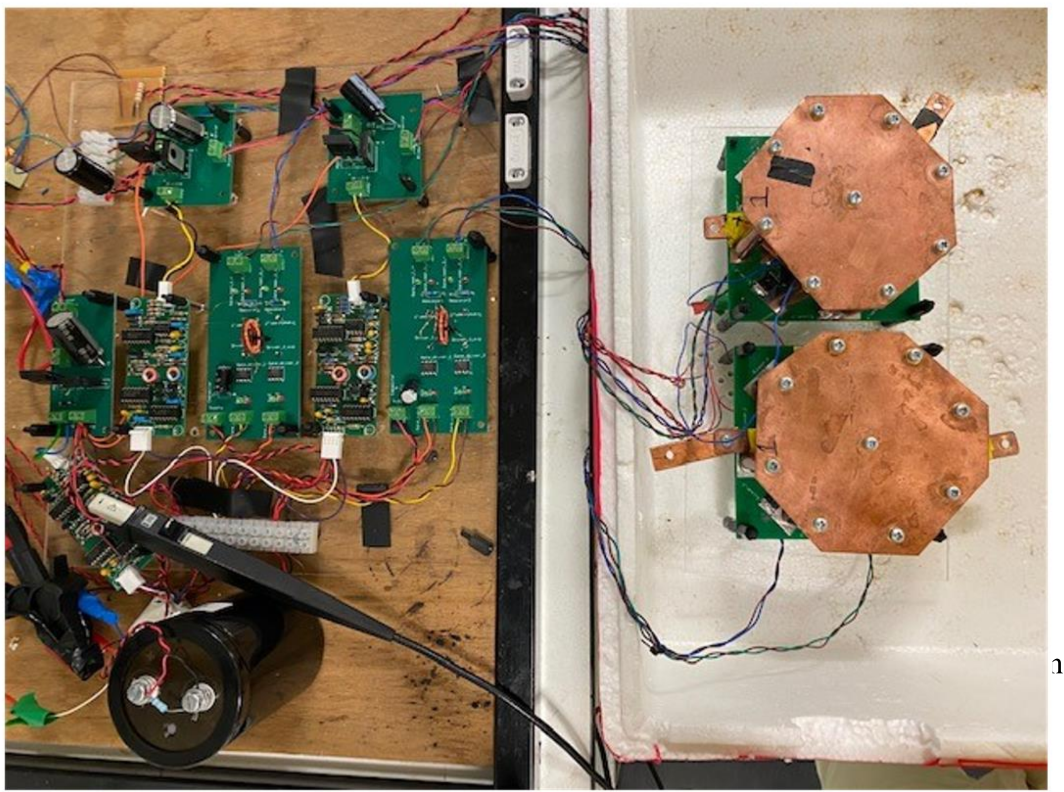


Fig. 5-13: Experimental rig of the dc-dc converter

The connections to the primary windings of TR1 and TR2, which link the circuitry in the warm zone with that in the cold zone, are made with twisted pairs of wire, minimizing stray inductances. Similarly, the connections from each of the gate driver circuits also use twisted pairs. Nonetheless, because of the physical length of these conductors, a higher stray inductance than usual is introduced into L_s seen in Fig. 5-11, with consequent resonances in the gate-source voltage v_{GS} as L_s interacts with the MOSFETs' input capacitances [134]. However, the MOSFETs' v_{GS} is still held well below zero in the off-state. Also, a feature of the silicon MOSFET is that the on-state or off-state v_{GS} does not

have to be as precisely set as that of other devices, such as the SiC MOSFET or GaN HEMT.

5.7 Experimental results

Fig. 5-14 shows key waveforms when the converter is operating with the cold-zone section immersed in liquid nitrogen, and with an average i_{out} of 564 A. For testing purposes, a superconductor was not driven here, but instead, the load was formed with a copper bar connected across the v_{out} terminals. The ripple content is estimated at less than 5% of the dc value. As presented in Fig. 5-8, a forward converter output filter is not required due to low current ripple, thus no capacitor was placed on the output terminals during experimentation. The dead time was set to be larger than the fall time of the MOSFET device of 250 ns, following previous literature [135]. The oscillation frequency at the output corresponds with the switching frequency of the buck converter of 100 kHz.

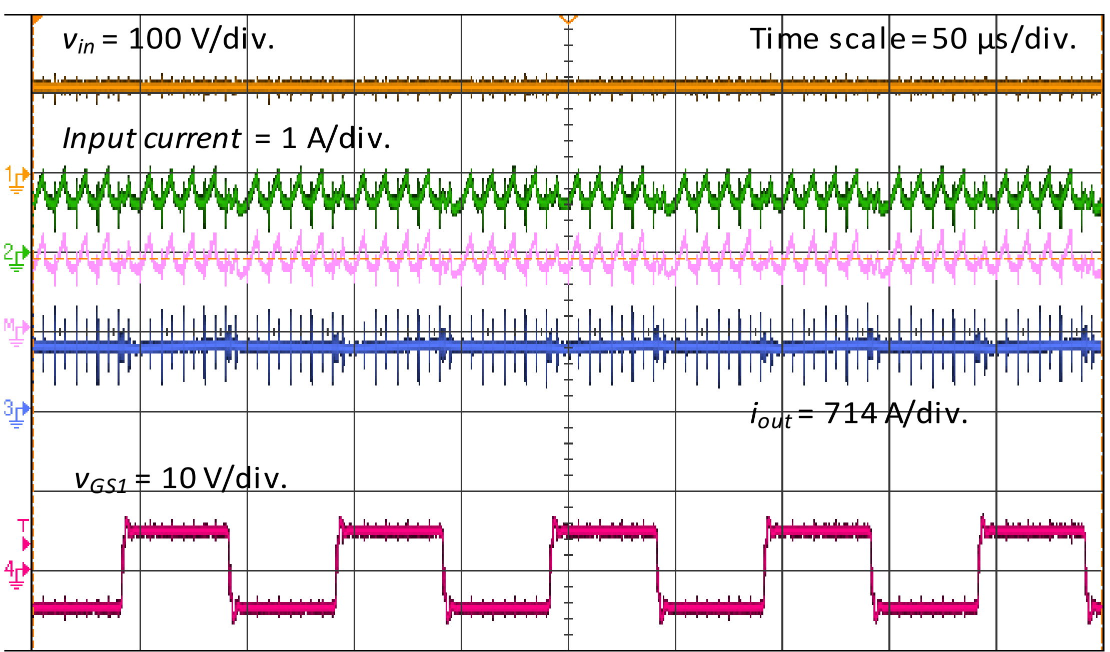


Fig. 5-14: Output waveforms from the experiment

5.8 Contribution

- Examining and analysing the use of cryogenic forward converter to reduce the size of the current leads for a superconducting magnet application. By using a cryogenic converter, the input voltage can be stepped down within the cryostat instead of outside. This in effect would reduce the size of copper leads which always have heat leakage and reduce the system overall efficiency.

5.9 Summary

In this chapter, a brief introduction has been done to discuss the application of a dc/dc for cryogenic magnets. The introduction has shown that utilising a step-down power converter can reduce both the size and the complexity of the current leads.

A literature review on cryogenic converters has been done. The review covered the performance of converters at cryogenic temperature, as it was shown that the efficiency of the converter increases with the decrease of temperature. Also, the review has shown that with the decrease in temperature some control circuits tend to stop working, especially those which are bipolar based chips. In the end, the review covered the performance of paralleling semiconductor switches at cryogenic temperatures.

Different topologies that are most suitable to supply large currents for superconducting magnets were considered mainly focusing on three main converter circuits. Of those three, it was shown that the forward converter has the best features as it offers isolation to the load and at the same does not require filtering capacitors due to ripple cancellation when using two antiphase forward converters. Based on that investigation a forward converter has been selected for further development for the application. After which, different gate-driver circuits have been examined for use with the converter. Single-winding self-driven gate driver was selected as it did not require large winding and at the same time ensured

that the gate of the MOSFET remained switched off by offering a stable negative voltage bias.

In the end of the chapter, an experimental setup was built and was able to produce a current of 500 A. The test circuit was run open-loop, and further investigation will include developing a current sensing and feedback control arrangement and simulating the circuit's dynamic response to changes in current demand.

Chapter 6

Conclusion and Future Work

This chapter summarises the accomplishments and general conclusions acquired by the thesis in addition to the main research contributions. At the end of this chapter, suggestions for conceived future research are highlighted.

6.1 Summary and contribution

The main objective of the thesis is to investigate the use of cryogenic power electronics for superconducting applications. In this section, a quick summary of each chapter is done as follows;

- **Chapter 1** gave an introduction to the thesis by highlighting the importance of cryogenic power electronic superconducting applications. The chapter first explained the theory of superconductivity as it discussed relevant equations and different types of superconductive materials. The chapter then briefly explained the different applications of superconductivity, specifically all-electric aircraft, Maglev, MRIs and Magnet accelerators applications. It was shown in each of the mentioned applications how superconducting material can be integrated and how power electronics are used in the system. Later in the chapter, it was explained how utilising power electronics at cryogenic temperature can improve the system

in terms of the mechanical complexity of the system and increased power density. In the end, a brief layout of the thesis was laid out.

- **Chapter 2** reviewed previous literature on cryogenic power electronics to identify the gaps. The chapter mainly reviewed the characteristics and the performances of different semiconductor devices including diodes, MOSFETs, IGBTs, GaN HEMT/HFET and JFET. The comparison was mainly done to see how each of these devices performs with the decrease in temperature. Mainly two characteristics were reviewed; 1) static characteristics, which identifies the conduction losses and the breakdown of the device and 2) dynamic characteristic, which identifies the switching losses. Based on the review results, it was found that the knowledge gaps were mainly that the ratings of the devices tested were smaller than the requirements of superconducting applications. Thus testing of devices with ratings suitable for superconducting applications is required which is discussed in the next chapter.
- **Chapter 3** discusses the testing of power electronic devices at cryogenic temperatures. The device ratings were decided based on the requirements of the different superconducting applications. Mainly three semiconductor devices were tested; diodes, MOSFETs and IGBTs. Experimental rigs were built for testing different characteristics, including 1) static characteristics, 2) dynamic characteristics and 3) paralleling. For the switching characteristic test, a current transformer suitable for cryogenic applications has been built. Based on the experiment results, the devices with the best performances at cryogenic

temperature were chosen for building cryogenic power converters in Chapters 4 and 5.

- **Chapter 4** discussed cryogenic power converters for all-electric aircraft. In the chapter the overall architecture of the aircraft is explained, where it was shown how the power converter would be integrated with the overall system at cryogenic temperature. The chapter mainly discussed two circuits; 1) three-phase rectifier and 2) phase-leg circuit for dc/dc and dc/ac applications. The three-phase rectifier was integrated with an axial machine, where it was shown that the efficiency of the rectifier increases once it was immersed in liquid nitrogen. A short-circuit across one of the diodes was induced, to evaluate the performance of the system in case of a fault. It was found that the superconducting coils were the most likely to fail in such an event and that the semiconductor devices remained unaffected by this fault. For the phase-leg; an experimental rig was set up to test the circuit. At first, the phase-leg was run in dc/dc mode, where it had shown that its efficiency increases at cryogenic temperature. The circuit was then run again in dc/ac mode, where different diode deactivation devices were tested at room and cryogenic temperatures. The experiment results also had shown that the efficiency increases at lower temperatures.
- **Chapter 5** has discussed the design and experimental set-up for the dc/dc converter used to supply MRIs and magnets. It was explained that using a dc/dc converter at the cryogenic side to step up the current would reduce the size of the wire leads and reduce the losses in the heat exchanger. The chapter then reviews

possible topologies that can be used for those requirements. In the chapter an experimental setup has been built, where it was able to supply the required current at cryogenic temperature, thus reducing the sizes of the current leads.

The contributions of this thesis can be summarised as follows:

- Investigated and analysed the performance of high capacity power semiconductors at cryogenic temperature. There is sparse literature on the testing of semiconductor devices above 100A especially IGBTs with ratings of 1200 V at cryogenic temperature, thus this thesis covered this gap and identified that IGBT modules utilising Silicone gel for insulation tend fail at cryogenic temperature, something not presented in the reviewed literature. On the other hand, IGBT modules that had Epoxy resin for insulation were able withstand such temperature.
- Examined a current transformer to be operated at cryogenic temperature to reduce leakage inductance in the double pulse test. Literature has struggled with accurately measuring double pulse tests at cryogenic temperatures as they used lengthy wires to avoid immersing commercial current probes at that temperature. This issue has been solved in this thesis by building a bespoke pulse current sensor that is capable of measuring current at cryogenic with high bandwidth.
- Verified that a rectifier circuit could be successfully applied to rectify signal from an HTS axial motor at cryogenic temperatures. There are sparse data on the effect of the implementation of a three-phase rectifier in a cryogenic

environment connected to a partially axial superconducting machine. This gap is addressed in this thesis.

- Studied and confirmed that diode deactivation techniques for superjunction MOSFET could be successfully applied at cryogenic temperatures. For verification, two different diode deactivation technique were applied at cryogenic temperature, where it was shown that the circuit with SiC diode as an antiparallel diode is the most efficient at cryogenic temperature.
- Testing and investigating the use of a cryogenic forward converter to reduce the size of the current leads for a superconducting magnet application. This test was done mainly to address the issue of using large copper current leads which have large heat leakage. Based on this test the size of the copper conductor for the cryostat can be reduced from almost 200 times and thus almost eliminating the heat leakage.

6.2 Future work

This thesis has focused on the use of cryogenic power electronics for superconducting applications to have a feasible system and increase the power density. The following includes planned and recommended future research:

- The testing of semiconductor devices at cryogenic temperature should be further extended. The first thing to do is to identify why some IGBTs in Chapter 3 have failed at cryogenic temperature and study which device materials and architecture are best suitable for that temperature. Conduct thermal and mechanical tests on

semiconductor devices at cryogenic temperature, to identify the weaknesses of the devices.

- To investigate building an inverter for superconducting motors for all-electric aircraft. Based on the tests done on different devices in Chapter 3, IGBTs have been found the most suitable device at that temperature that matches the required current rating. In addition, the cooling penalty of the overall system would be studied to make a comparison between using the power converter at room and cryogenic temperature.
- Extend the experimental rig of Chapter 5, where copper conductors are going to be replaced with superconducting coil and closed-loop using DSP and hall effect sensor would be implemented. In addition, the cooling penalty of the overall system would be studied to make a comparison between current leads and using dc/dc converter. Losses to be formally analysed and, including the kink effect, the use of GaN devices for the synchronous rectifiers instead of Si MOSFETs to be investigated.

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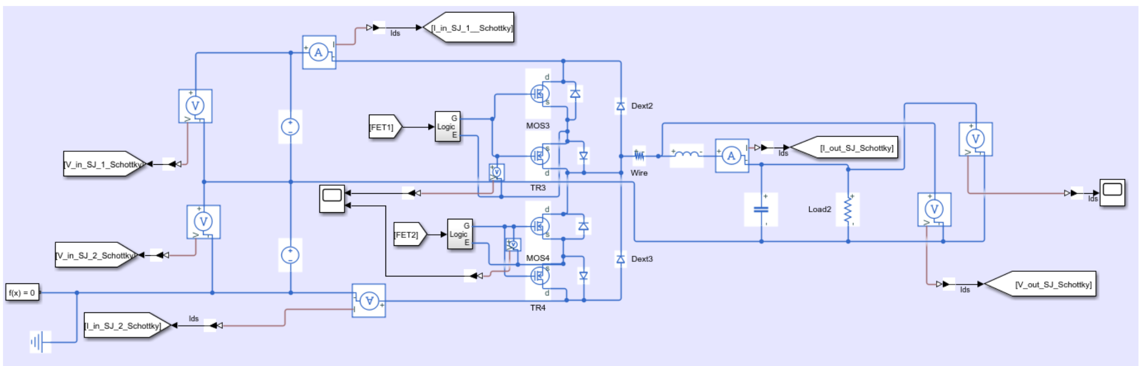
Appendix A: Simulation

A.1 Simulation of the phase-leg at cryogenic and room temperature

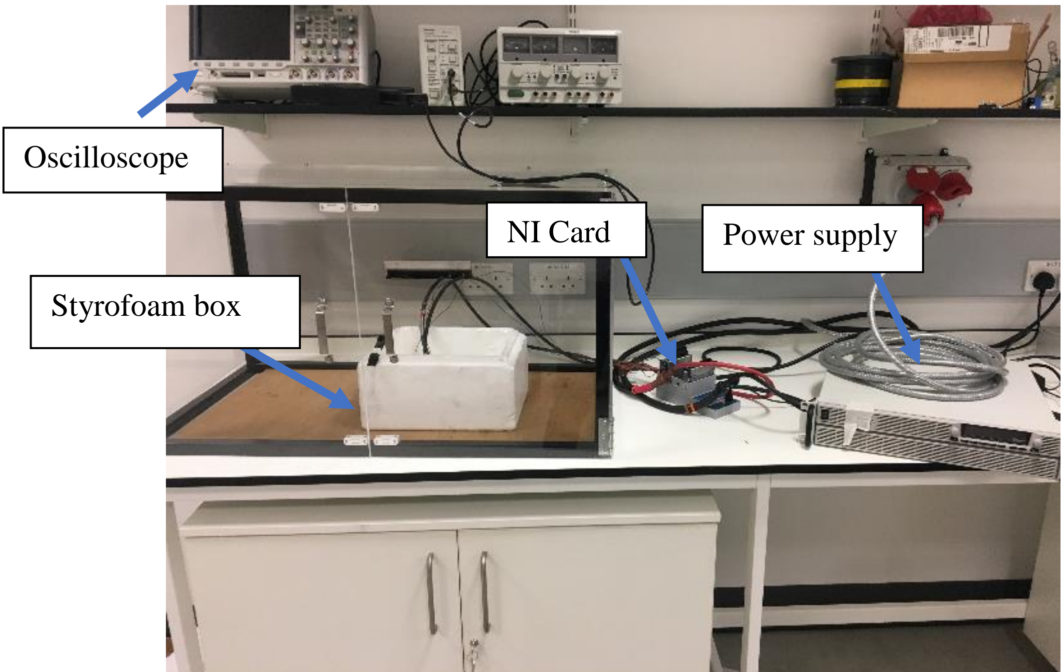
Figure A.1 shows the schematic circuit used in the Simulink to simulate the phase-leg circuit presented in Fig. 4-15. As seen in the figure, the phase-leg is connected to a power supply on the left-hand side and a load on the right-hand side. The parameters input to that simulation are presented in Table 4-7. The simulation is run twice, once at room temperature and another at cryogenic temperature. To calculate the efficiency, the input power from the power supply and the output power on the load are both measured and calculated.



A.1: Circuit Schematic of phase-leg

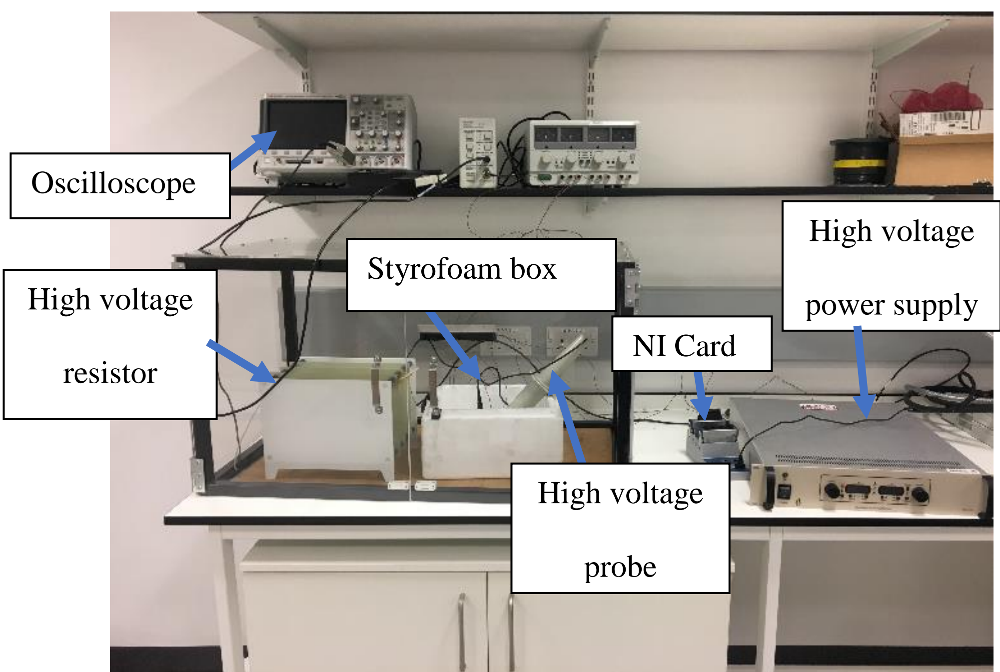
Appendix B: Experimental setup

Figure B.1 shows the experimental setup for the forward voltage test shown in Fig. 3-4. The D.U.T. is located in the Styrofoam as this gives the capability to store LN2 so that the device can be tested at cryogenic temperature. The DUT is connected to a power supply, where it is used to source current through the device. The NI card is used to capture measurements which are then store data on the PC.



B.1: Experimental setup for the forward voltage test

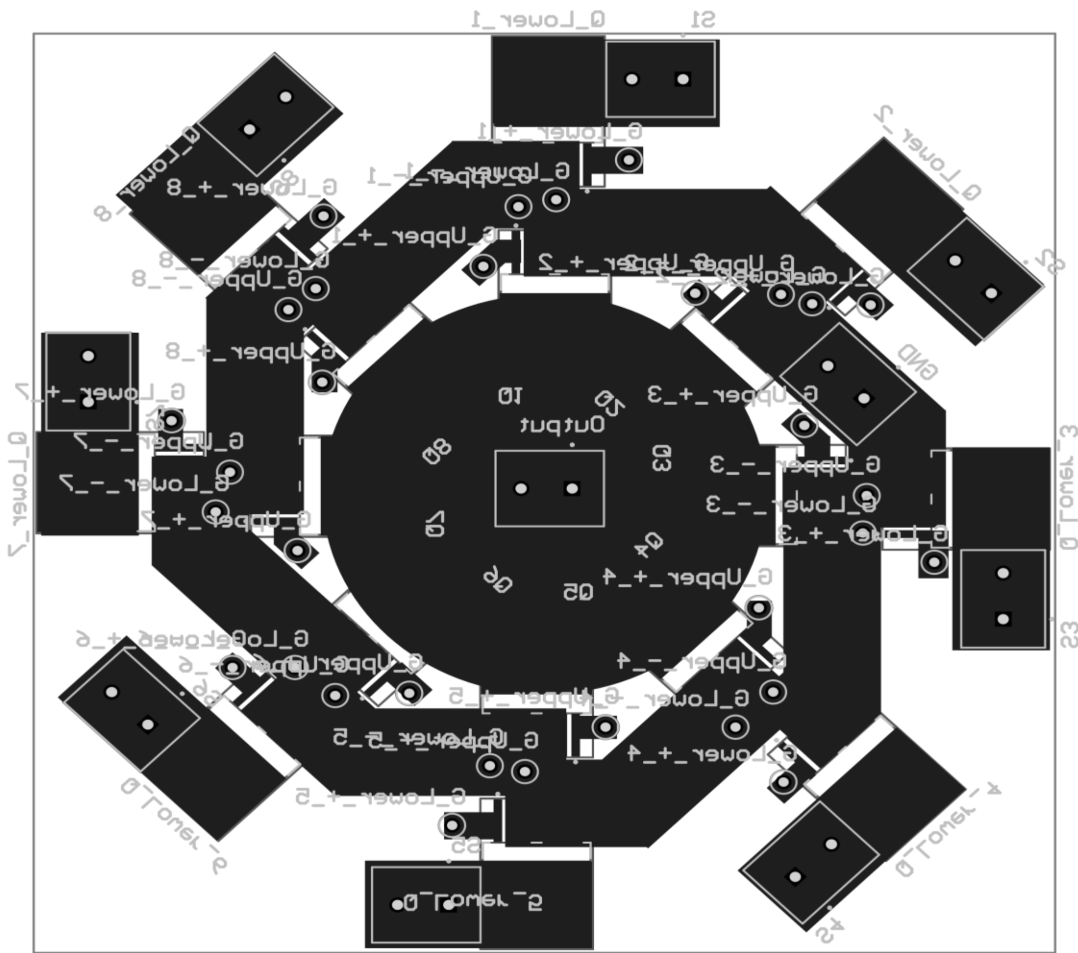
Figure B.2 shows the breakdown voltage experimental setup shown in Fig. 3-6. The D.U.T. is connected to the high voltage supply, where the voltage is ramped up and the voltage is measured using the NI card.



B.2: Experimental setup for the breakdown voltage test

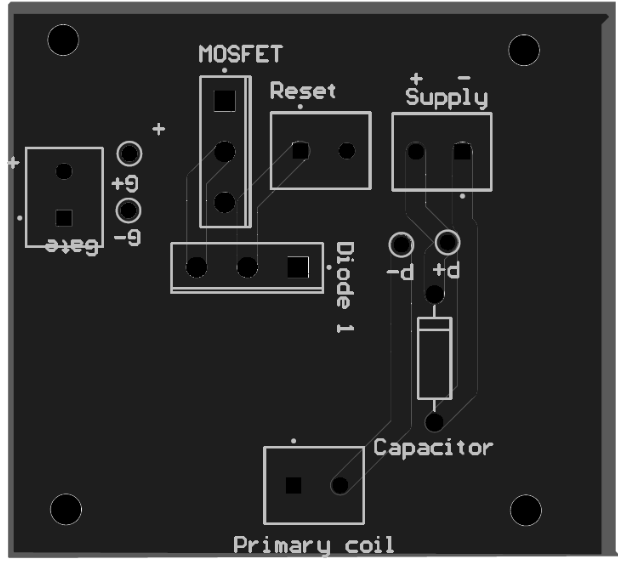
Appendix C: PCB schematics

The PCB diagram is shown in Fig. 5-9 and is presented in C.1. As seen in the figure, the MOSFET devices are laid out in parallel to maximise the output current and minimise the losses in the devices. The MOSFETs are laid out in a symmetrical octagonal shape to enhance current sharing among the MOSFETs.



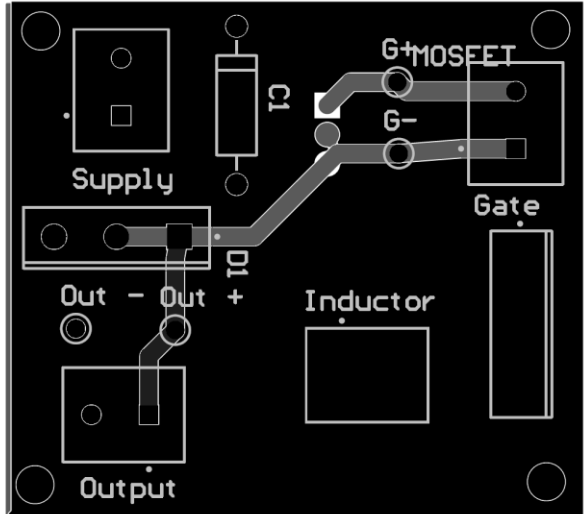
C.1: PCB circuit of the forward converter

Figure C.2 shows the primary side circuit presented in Fig. 5-9. The output of this circuit is connected to the step-down voltage transformer which then feeds the forward converter shown in C.1.



C.2 Primary side

Fig. C.3 shows the pre-regulator circuit presented in Fig. 5-9. The pre-regulator input is connected to a power supply and the output is connected to the primary side circuit.



C.3: Pre-regulator circuit