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Rectifier Power Converter for Marine Applications with Compensating Capacitor and Boost Converter Stage

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ABSTRACT

Environmental concerns and new emissions regulations, as well as increasing power needs for marine electrical grids, are pushing the development of more efficient power converters for shipboard power systems (SPS). The priorities for SPS design are reliability and power density especially in harsh operating conditions. Safety, space, and weight are of paramount importance requirements on a ship. One factor affecting the design of SPS is the high inductive impedance presented by ac generators, which requires high voltage ratios to compensate for. Therefore, ac-dc converters, sitting as they do between ac generators and the dc bus of the SPS, are identified as a point of potential development to improve the form factor and efficiency of SPS. A novel series capacitor compensation technique is proposed and applied to an ac-dc boost rectifier. Time-averaged equations are derived and compared to simulated waveforms generated using MATLAB/Simulink. Total harmonic distortion (THD) and power factor (PF) are calculated and measured. THD is found to be the limiting factor in designing the proposed compensator. The circuit is simulated in one and three phases, and several input-to-output voltage ratios are compared. To verify the practicality of the compensation method, a single-phase 1 kW rated prototype is implemented and practical results are presented and compared with the simulated waveforms. It is found that the compensation method can control THD to acceptable levels for a large range of inductive impedances, suggesting that this solution should be further developed and investigated for application in SPS.

LIST OF ABBREVIATIONS

Abbreviation	Term
ac	Alternating Current
ADC	Analogue-to-Digital Converter
CCM	Continuous Conduction Mode
DAC	Digital-to-Analogue Converter
dc	Direct Current
ECA	Emission-Controlled Area
ESS	Energy Storage System
FB	Full-Bridge
FPGA	Field-Programmable Gate Array
HB	Half-Bridge
IGBT	Insulated-Gate Bipolar Transistor
IGCT	Integrated Gate-Commuted Thyristor
IMO	International Maritime Organization
IPS	Integrated Power System
MMC	Modular Multilevel Converter
MVDC	Medium Voltage Direct Current
NP	Naval Package
NPC	Neutral-Point-Clamped
p.u.	Per unit
PC	Personal Computer
PCB	Printed Circuit Board

PEBB	Power Electronic Building Block
PF	Power Factor
PHIL	Power Hardware-In-the-Loop
PI	Proportional-Integral
RMS	Root Mean Square
SDG	Sustainable Development Goals
SiC	Silicon Carbide
SNR	Signal-to-Noise Ratio
SPS	Shipboard Power Systems
THD	Total Harmonic Distortion
VHDL	VHSIC Hardware Description Language
WBG	Wide Band Gap

LIST OF SYMBOLS

Symbol	Term	Unit
$\frac{di}{dt}$	Slope of input current	As
I_{out}	Average load current	
i_β	Initial condition for input current for overcompensated scenario	A
$V_{c\beta}$	Initial condition for voltage across C_{comp} for overcompensated current, defined as $-\frac{\sqrt{2}I_{in}}{\omega C}\cos\beta$	V
$\hat{v}$	Peak value of input voltage	
a_1, b_1	Fourier coefficients of the first harmonic of input current	
C	Value of capacitance used for compensation	mF
c	Variable defined as $\frac{1}{\omega\sqrt{LC}}$	
C_{comp}	Compensating capacitor	mF
C_{out}	Output capacitor	uF
D	Boost diode	
d	Duty cycle	%
$D_{\text{a}} - D_{\text{d}}$	Diode in full bridge rectifier	
f_{ac}	Ac frequency	Hz
f_{max}	Maximum switching frequency	
f_{sw}	Switching frequency	kHz
H	Hysteresis Band	A

H_{min}	Minimum hysteresis band	A
I_{in}	RMS input current	A
i_{in}	Instantaneous input current	A
i_{in}^{*}	Instantaneous input current reference	A
L	Value of inductance supplied by ac generator	mH
L_{ac}	Interfacing inductance	mH
m_1	Variable defined as $\sin(c\Delta)\cos(\Delta+\beta)$	
m_2	Variable defined as $\cos(c\Delta)\sin(\Delta+\beta)$	
m_3	Variable defined as $\sin(c\Delta)\sin(\Delta+\beta)$	
m_4	Variable defined as $\cos(c\Delta)\cos(\Delta+\beta)$	
m_5	Variable defined as c^2-1	
N	Number of submodules per arm in MMC topology	
P	Input power	W
R_{out}	Load resistance	Ω
S	Active switch	
T_{min}	Minimum switching period	s
T_{off}	Duration of OFF time for switch	s
T_{on}	Duration of ON time for switch	s
Ts	Switching period	s
v_c	Instantaneous voltage across capacitor	V
V_c	Initial condition for voltage across C_{comp} for undercompensated current, defined as $-\frac{\sqrt{2}I_{in}}{\omega C}$	V
V_{dc}	DC Voltage	V

V_{in}	RMS Input Voltage	V
v_{in}	Instantaneous input voltage	V
v_{ref}	Reference voltage for SPWM	V
V_o	Dc output voltage	kV
X_C	Capacitive impedance	Ω
X_L	Inductive impedance	Ω
X_{LC}	Total reactance at input of circuit	Ω
α	Detuning angle, undercompensated current	Radians
β	Detuning angle, overcompensated current	Radians
Δ	Difference between γ and β, defined as $\gamma - \beta$	Radians
γ	Second angle, overcompensated current	
π	Pi	
ϕ	Phase shift of the fundamental component of i_{in} from v_{in}	Radians
t	Time	s
ω	Angular frequency $2\pi f$	Radians
v_L	Instantaneous voltage across interface inductor	V
$v_{carrier}$	Carrier voltage for SPWM	V

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CHAPTER 1: INTRODUCTION

1.1 Background

Some 80% of the world's traded goods are shipped by marine vessel, which in 2020 amount to around 11 billion tons. Merchants have been trading goods across the sea for thousands of years, but it is relatively recent in human history that electricity has been a part of the vessels. The first electrical power system on a ship was a dc network installed on the SS Columbia in the 1880s to power its new lightbulbs [1]. In the early 1900s, ships used steam-turbine-coupled generators for propulsion, with service loads supplied by different generators [2]. Variable speed drives were invented in the 1980s, which allowed for electric propulsion [1]. This in turn meant that SPS could have a single bus with multiple generators and loads, also known as an integrated power system (IPS) [2]. Throughout their history, SPS priorities have remained the same: reliability, efficiency, and maneuverability [3].

Modern marine electrical systems are testing the advantages of zonal architectures and dc networks. This refers to systems, which are separated into redundant zones with independent power sources that can be isolated in case of fault. Disadvantages come into play with the complex control and fault detection algorithms needed for zonal architectures. However, dc power systems are made more interesting by this direction of SPS design because there is no need to synchronize frequencies of different ac sources. Many ships are beginning to integrate renewable sources like solar, which are inherently dc, which again is aided by zonal design and dc systems. Dc systems outperform ac systems in power quality, reliability, high power transmission efficiency, energy losses, and cost [1].

The contemporary SPS contains several generators and supplies electricity to every service on the ship. Gas-turbine and diesel generators are the most common generators; nuclear has been used most extensively in naval ships but is not commercially popular [2] and liquified natural gas is another alternative [3]. The loads supplied by each SPS include the propulsion system, pumps and compressors for heating and ventilation, control and communication systems, and any hospitality services provided for passengers and crew. Increasing sizes of ships, as well as the addition of new electric systems, are increasing the power requirements of SPS [3]. Presently, SPS power levels are around 2 – 7 MW for smaller ships and 10 – 20 MW for larger ships such as cruise liners [4].

Every SPS with an ac generator, whether ac or dc distribution, and no matter the power level, requires ac-dc power conversion. Three-phase ac-dc converters are the most used converters in SPS [5]. Converters that transform voltage and current from ac to dc are known as rectifiers. A full bridge rectifier consisting of four diodes is shown in Figure 1.1. Figure 1.2 shows the ac voltage v_{in} at the input and the resulting output voltage v_o. Using a passive filter, such as a capacitor, at the output, the ripple of the output voltage can be decreased until it is a usable dc voltage, as seen in Figure 1.3.

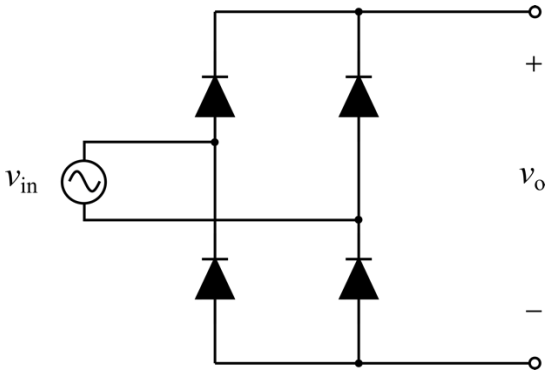


Figure 1.1 A full-bridge rectifier. Ac input voltage v_{in} is rectified to output voltage v_o.

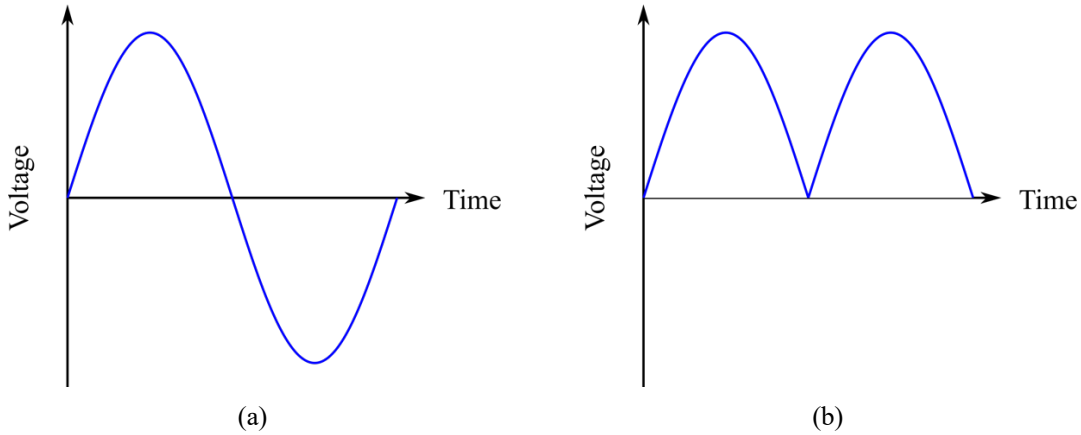


Figure 1.2 Input and output voltages of full bridge rectifier. a. v_{in}. b. v_o.

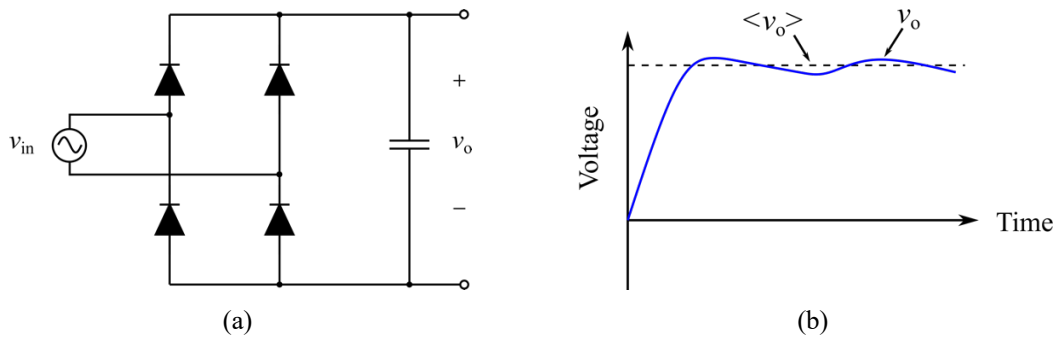


Figure 1.3 a. Full-bridge rectifier with output filter capacitor. b. Average and instantaneous output voltage $<v_o>$ and v_o.

The priorities of designing rectifiers for SPS are the reliability and power density of the converter [6]. The reliability of the converter comes down to the number of power semiconductors and complexity of the design. Therefore, the most common rectifiers found in SPS are the passive diode rectifier and thyristor rectifier [1]. These rectifiers however require large passive components for filtering harmful harmonics from the ac current. Additionally, ac generators present with a large inductive impedance, which lowers the active power and lessens the efficiency. Addressing this impedance is typically done with high voltage ratios, which increase the voltage stress on components and increase size requirements for passives.

1.2 Research Motivation

New environmental regulations and the climate crisis have increased interest in the electrification of both commercial and naval ships. The United Nations has put together Sustainable Development Goals (SDGs), which are a worldwide call-to-action to implement strategies to reduce inequality and climate impacts at the same time. SDG 13 is to “take urgent action to combat climate change and its impacts” and specifies emissions targets for participating countries and industries [7]. Additionally, the International Maritime Organization (IMO) has defined emission-controlled area (ECA) zones where new emission limits for vessels sailing through came into effect January 2023 [3]. This directly impacts the marine shipping and cruise industries, as ships must pass through these coastal ECA zones to reach ports.

In 2017, China produced the world's first all-electric cargo ship, which could travel up to 50 miles on a single charge. A huge step forward for modern day ship design, but this ship would not be able to carry freight over the distances needed for modern commerce.

In terms of passenger ships, the first fully electric battery powered ferry, the MF Ampere, began operation in 2014. However, the combined power of its batteries was around 1 MW, which is quite small when compared to the 4 MW supplied by a single diesel generator made by Fairbanks Morse, several of which could be used on larger ships [3]. This difference in energy density is the reason that while ships power systems are increasingly electrified, they are still typically powered using some form of ac generator powered by fossil fuels. Therefore, there is still a need to reduce emissions, increase efficiency, and integrate renewable energy sources into SPS.

One way to push SPS further in these areas is to improve the ac-dc conversion stage. In an 18-MVA system, the transformers can weigh up to 35 tons [5]. Less weight would mean less fossil fuel is needed to power the vessel. Reducing voltage is one way to reduce size needs for all downstream components. However, voltage levels are often dictated by the large inductive impedance of ac generators, so to reduce voltage ratios this impedance must be compensated in some way. In addition, the output of the generator is connected to the dc rail through a rectifier and boost converter.

This is an interesting question because the boost converter is a well-known and easily implemented circuit, with only one active switch per phase, which is appealing to industry because of the cost and control complexity of multi-switch topologies. For this reason, the boost converter is often used in grid-connected applications as a power factor corrector. However, high impedance, causes a large current distortion when using the boost topology. High total harmonic distortion (THD) can cause damage to generator and other equipment on ac grid, as well as lessening the efficiency of the converter. 8% is the limit on total THD in SPS [1].

In order to use the boost topology, a capacitor is placed in series with the inductive impedance of the source to compensate the reactive power. Since the boost topology's inductor is at the input of the converter, the ac generator's inductive impedance can be used as the boost inductor to improve power density and allow room for the new capacitor. Series capacitor compensation is a technique well-known from ac power systems but has

not been used in this context because SPS designers typically avoid bulky passives. However, this solution replaces the boost inductor with the ac generator impedance and allows the voltage ratio to be lowered so that the rest of the system can be sized down.

1.3 Research Objectives

The aim of this research is investigating the use of a series compensating capacitor to allow the rectification of the voltage produced by an ac generator using a boost converter.
The main research objectives of this thesis are as follows:

- Review existing literature to identify state of the art
- Perform detailed time domain analysis of the proposed circuit and describe its operation
- Determine design requirements and limiting factors
- Simulate circuit in one and three phases
- Build experimental prototype to test the proposed converter

1.4 Thesis Organization

This thesis is organized into six chapters, which are outlined and presented as follows:

- **Chapter 1** provides background information on the context and motivation behind the research and provides an outline of the structure of the thesis.
- **Chapter 2** reviews the existing literature on ac-dc converters used within shipboard power systems.
- **Chapter 3** presents the operation and mathematical analysis of a new rectifier for marine applications with compensating capacitor and boost converter stage.
- **Chapter 4** presents the methodology and results of simulating the new converter topology.
- **Chapter 5** details the experimental equipment used to test the compensation concept and proposed topology and the results of the tests.

- **Chapter 6** presents the conclusions of the research, the author's contributions, and suggestions for future research.

CHAPTER 2: AC-DC INTERFACE CONVERTERS IN SHIPBOARD POWER SYSTEMS

In this chapter, a detailed survey of ac-dc converters used in shipboard power systems (SPS) is presented. As alternative power sources are further integrated and the power requirements for SPS continue to increase, innovation in power electronic converters is important to ensure the efficiency and power density required by these systems. Ac-dc converters are necessary for SPS function as state-of-the-art marine power generation systems still rely on ac generators even with a dc distribution system. The large inductive impedance of ac generators presents a design challenge that the ac-dc converter must address. First an overview of SPS architectures, ac vs. dc distribution, and major system components is given, then the existing ac-dc converter solutions are presented. The main types of converters discussed in the survey are diode, thyristor, and insulated-gate bipolar transistor (IGBT) -based rectifiers and modular multilevel converters. They are compared in terms of cost, reliability, complexity, and power density.

2.1 Shipboard power systems

There is continuous desire for improvement in SPS due to environmental concerns and increasing power demands. Stricter emissions standards have encouraged the marine industry to reduce emissions, improve efficiency, and include more renewable energy sources on-board, changing the landscape of SPS development [1]. These changes expedite the need for hybrid or all-electric SPS, which means an increase in the power handled by the SPS [8]. The addition of wind and solar energy complicates energy management in the system as well [9]. SPS power levels are currently typically 2 – 7 MW for smaller ships and 10 – 20 MW for larger ships like cruise liners and naval vessels [4], with future systems reaching 30 – 50 MW. Higher voltage is needed to keep current down with higher power in order to increase power density and efficiency to keep ships same size [5]. Higher power and voltage also increase the risk of cable fault in SPS, which already has higher risk and more stringent requirements for clearing faults quickly than land-based grids. The use of power electronic converters increases power density but introduces harmonics into the ac

sections of the SPS. Traditionally these harmonics are addressed with passive filtering techniques in the form of bulky capacitors and inductors, which add to the size, weight, and cost of the SPS. They add to safety concerns as well; in the case of a short circuit, it is necessary to dissipate the energy stored in the filter. Some power electronics advancements are driving innovation for SPS design such as wide bandgap (WBG) devices, power electronics building blocks (PEBB), dc power systems, and zonal architectures.

SPS architectures have evolved over time due to the availability of technologies and the needs of ship users. The most important properties of SPS are reliability, dependability, and survivability [10]. Reliability refers to the mean length of time that components last, dependability is the ability of the system to continue working if one part fails, and survivability is the ability of the vital services to continue even if major damage is sustained [10]. To achieve these three properties, often grouped under the one heading of reliability, the best design technique is redundancy. Figure 2.1 shows how redundancy is used in SPS architectures: auxiliary generators are included in case a main generator fails, and crossties or breakers can be closed if an entire set of generators fail.

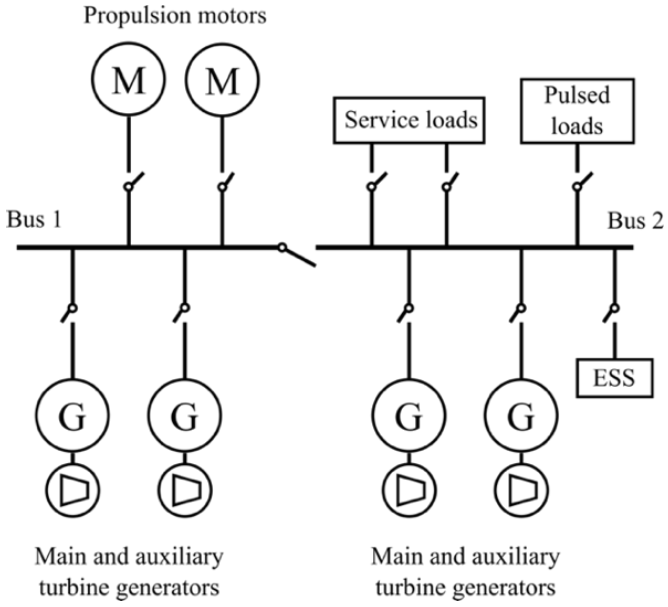


Figure 2.1: Isolated radial architecture of SPS. Modified from [4].

Recently, it has become common for SPS to been designed in the style of an integrated power system (IPS). Older systems (Figure 2.1) had one set of generators for the propulsion system and another set for service and other loads. The SS Canberra was an example of

non-integrated power distribution [3]. The advantage of this design is that the service loads are not impacted by transients and oscillations in the propulsion system. However, since the buses are not connected, excess capacity of the propulsion system not always used, and the system overall is relatively inefficient. Meanwhile, in IPS, service loads and propulsion are distributed symmetrically between the busses. The main advantage of this design is the ability to share power between consumer systems, which improves power flexibility and availability.

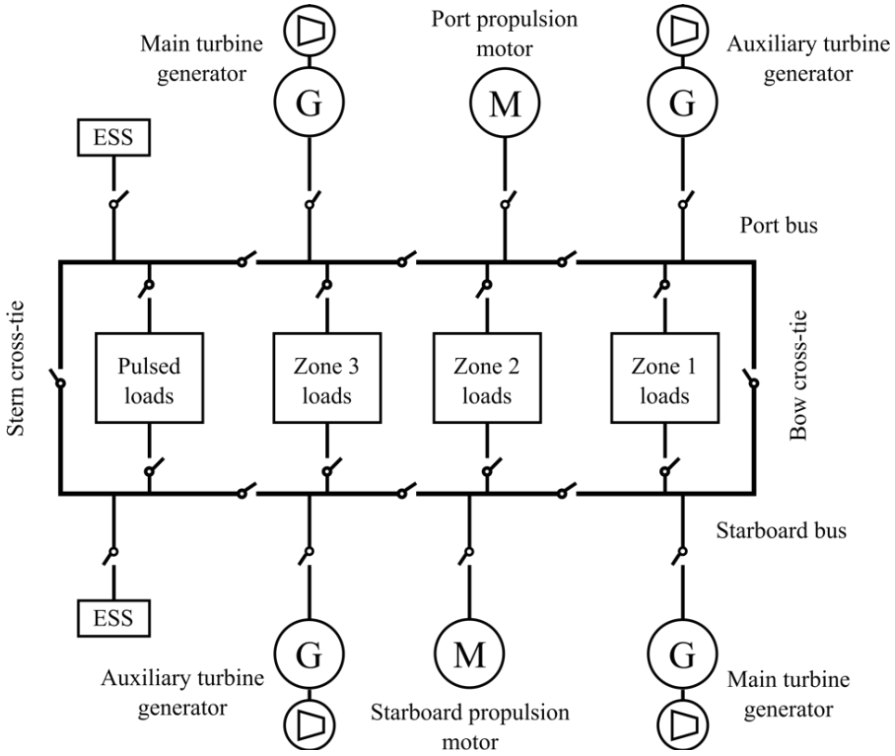


Figure 2.2: Zonal IPS architecture of SPS. Modified from [4].

IPS designs can have one of several distribution models: zonal, radial, or ring. Modern systems are moving towards zonal architecture (Figure 2.2), where the system is separated into redundant zones with independent power sources. The advantage of this architecture is that each zone can be isolated from other others in case of fault, with redundant zones supply power to affected systems. However, it is more complex to control and ensure communication between zones, and systems therefore need advanced fault detection and isolation algorithms. Radial IPS as shown in Figure 2.3 generally has 2 buses with

generators and energy storage systems (ESS) supplying both, which in turn supply pulsed power loads and service loads [2]. The propulsion system is split into port and starboard systems, which are supplied independently by the two buses; however, there is an isolating switch, which can be connected if the generation system of one bus fails. Ring distribution is another option which is used more rarely than radial or zonal. It is similar to zonal distribution but different in one fundamental way, that each load and generation system has only one point of coupling to the bus. If any of these connections fail, vital services or power systems may be unusable. Therefore zonal, having more dependability and survivability than the other two systems, has been the focus of most development in SPS recently.

The move to zonal architecture is enabling another innovation in SPS: the move from ac to dc distribution. While the first power systems on-board ships relied on dc distribution, since the invention of turbine generators, ac systems have dominated the marine power system space. Recently, dc power systems becoming source of interest because many ships already integrate renewable sources which are inherently dc, and a dc system makes integration simpler. Other advantages of dc over ac include reliability, high transmission efficiency, power quality, and lower cost [1]. One factor that causes these advantages is impedance. Ac impedance causes reactive currents which lower power transfer capacity, and cause a high voltage drop along transmission lines because ac impedance is greater than the simple ohmic voltage drop. Additionally, dc lines do not experience the skin effect, nor does power factor affect them [10]. The efficiency of the generation system can be improved with dc because the speed of the prime movers can be decoupled from the distribution grid and each other, allowing them to run at optimized speeds during lower power periods. This simplifies control as well, because the speed and voltage of the sources do not have to match as in ac. One trade-off between the two solutions is that while dc system transformers can have a smaller footprint, ac transformers tend to be more reliable. Ac systems continue to have simpler fault protection than dc, as ac breakers can use the zero crossing of voltage to clear faults and development of high power, high voltage dc breakers is still ongoing. However, even within ac systems, the service and pulsed power loads require ac-dc conversion. Since both ac and dc bus systems remain in use, ac-dc converters applicable to both systems will be explored.

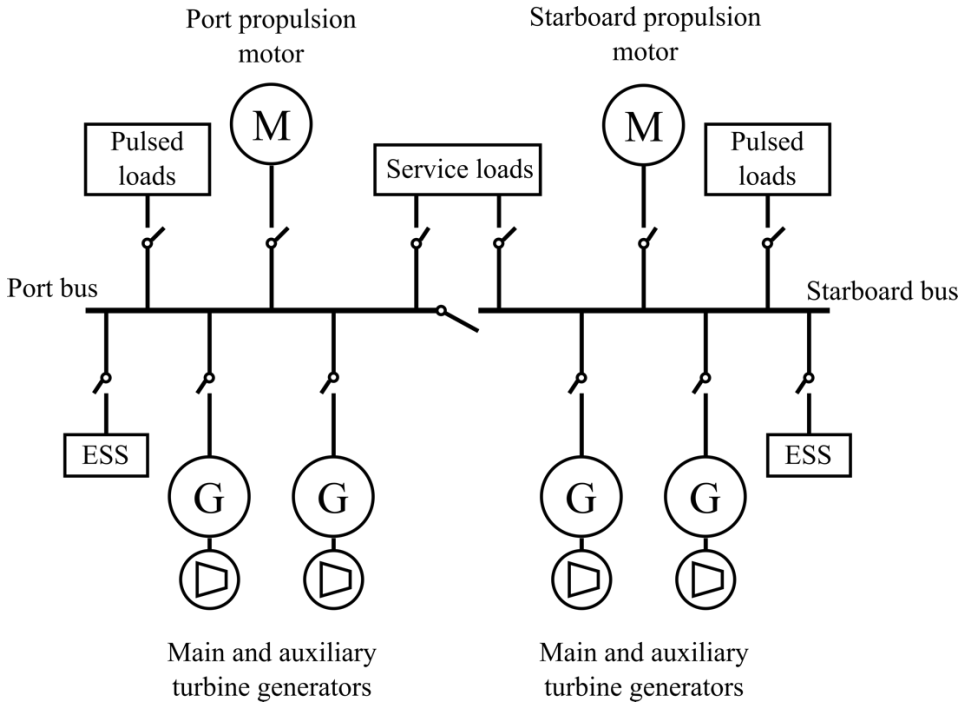


Figure 2.3: Radial IPS architecture of SPS. Modified from [4].

All SPS, whether ac or dc, are formed of the same basic components. The first are the power generation modules, made up of the prime mover and generator, plus a gearbox to couple them in ac distribution. Generator impedance often runs up to the 1 p.u. range, which increases reactive power and harmful harmonics which could cause vibration damage to the generator and decrease performance of the SPS. Thus, designers need to increase the working voltage to lessen the impacts of this impedance. Other SPS system components include ESS, which are useful to balance power when ac systems experience frequency fluctuations, as well as to bring more functionality and reliability to the system as a whole [3]. Technologies used for this application include batteries, ultra-capacitors, flywheels, and superconductors. To interface with the distribution system, an ESS requires bidirectional converters which can control active and reactive power. SPS loads include propulsion, pumps and compressors, control and communication systems, and on naval vessels, pulsed power loads, i.e., weapons needing quick bursts of high power. Different loads have different time constants, i.e., how quickly their power needs change [3], and

therefore the connections and specifications of each load can have a great effect on its power supply needs.

Ac-dc converters are some of the most used converters in SPS and have a great impact on ac power quality and the power density of the overall power system. In dc systems, rectifiers lie between the generator and the dc bus, while in ac systems, they deliver power from the ac bus to loads needing a dc link, such as variable speed drives [11]. In ac systems, harmonics from the rectifier harm the entire distribution system. In both systems, these harmonics could reach the generation system and cause harmful physical vibrations to the generators. According to international standards set forth for SPS design, allowable THD is 8%, with no single harmonic being larger than 5%. This standard is stricter for naval vessels, where THD must be below 5% and no single harmonic can be greater than 3% [3]. Rectifiers tend to fall into the category of high-power converters with low frequency components, which contribute more harmonics than low-power converters. This means they often contribute to the bulkiness of the power system as well as being an important design decision for engineering working to limit harmonics in SPS. As power converters, they also include power semiconductors, which are the limiting factor in terms of fault current withstand compared to other equipment in the SPS like cables, generators, and transformers [6]. Therefore, their design determines the fault tolerance of the whole system. As the importance of ac-dc converters to SPS has been established, existing technologies will now be summarized and discussed.

2.2 Overview of Generators for Marine Applications

The electrical machines that generate the power on ships are important to survey because their intrinsic properties affect the design of the rest of the power system. They are paired with a prime mover, either an internal combustion engine such as a diesel engine, or a gas turbine. The prime mover forces a shaft to rotate, which is usually coupled to the generator through a gearbox to control rotor speed. In AC SPS, the rotation speed is fixed to supply a fixed ac frequency to the ship's grid, while in DC SPS the speeds can be variable to maximize efficiency [6].

Synchronous generators are ubiquitous in the SPS industry. In a wound-field salient pole alternator, the rotor is made up of a magnetized winding attached to the rotating shaft of the prime mover, creating a rotating magnetic flux. This in turn generates alternating current in the armature windings. The synchronous name comes from the fact that the frequency of the ac current generated is directly related to the speed of the rotor. It is common for generators used in SPS to have 8 or 10 poles (p) and have a rotational speed (n) of 720 or 750 rpm [6] to generate 50 or 60 Hz. These values are related as follows [12].

$$f_{ac} = \frac{p}{2} \times \frac{n}{60} \tag{2.1}$$

The output voltage of the generator will vary with load, but the effects of this can be lessened by the use of an automatic voltage regulation (AVR). The AVR controls the excitation current to limit the terminal voltage to $\pm 2.5\%$ of nominal voltage under steady state; however, voltage can vary up to 20% during a transient on the load [12].

Permanent magnet generators use a permanent magnet to generate the magnetic field instead of excitation of the rotor field winding. They are being researched as a solution for MVDC SPS because they are more efficient at higher speeds because of the lack of excitation losses [13]. They also do not need external excitation, and therefore have fewer moving pieces. However, they have their shortcomings as well: the flux cannot be controlled with an AVR in the same way and the magnet itself is mechanically unreliable [13].

The output voltage or a generator is equal to the excitation voltage minus the armature reaction voltage and the voltage drop across the armature, which has both reactive and resistive components. The leakage reactance of the armature and the reactance derived from the armature reaction can be modelled as an inductor in series with the generated voltage. Based on the design specifications used in [14], this series reactance can be anywhere from 0.05 to 0.93 per unit. According to [15], reactances in the 1 to 2 per unit range are common for turbine generators, and the effective reactance can change with load. The power factor of the generators can range from 0.65 [16] to 0.96 [14].

2.3 Ac-dc converter topologies for SPS

Rectifiers in SPS must have serval important characteristics and meet the voltage and power requirements of the system. SPS power levels can range from 4 – 40 MW, and a rectifier in that system may need to be designed for up to a quarter of the total power in the system. Voltage levels range from 0.5 – 20 kV typically, depending on the kind of ship. The ultimate goal of power converter design in SPS is to maximize efficiency and reliability while minimizing size, weight, and cost. A common trade-off in this design process is that higher switching frequency decreases size but increases switching loss [1]. The list of need-to-haves in an ac-dc converter in SPS includes high reliability, low power density, high efficiency, low cost, and to perform the necessary ac-dc power conversion. They must perform this duty without exceeding the limits on harmonics in the system. The impedance of generator systems in SPS make this more difficult, as the impedance of the generator can have unwanted effects on the current with some topologies [17]. Some elements that can be useful but are not necessary in every design are the ability to control dc bus voltage and ac current, scalability, modularity, and bidirectionality.

2.3.1 Diode Rectifiers

Diode bridge rectifiers are the most popular ac-dc converter used in SPS because of their simplicity, reliability, and cheapness [2]. The basic topology as shown in Figure 2.4 is formed of three legs with two diodes each with a single phase from the ac source connected between the two diodes. The diodes are passively switched with the ac voltage as they become forward biased with positive voltage and vice versa. The topology as described thus far, also called a six-pulse diode rectifier, is synonymous with high harmonics and requires large passive filtering components to achieve workable THD. Therefore, it is common practice to use several bridges in series or parallel in twelve, twenty-four, or even higher pulse number rectifiers. Though these designs increase the number of components, diodes are cheap and require no control to function. This lack of control is easier from a development perspective, but it means that the output voltage will be set by the input voltage level alone. For this reason, diode rectifiers are often paired with dc-dc converters to control the dc bus and power flow.

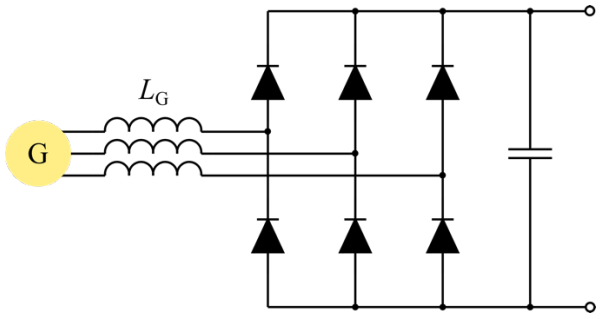


Figure 2.4 Six-pulse diode rectifier. G represents the generator and L_G is the per-phase impedance presented by the generator.

The diode rectifier is known for its simple, cost-effective, and robust design, but it requires bulky passive components and has no fault management capabilities. The advantages to using diodes in the bridge rectifier format come down to the low cost and robustness of the devices themselves. However, this topology cannot control dc voltage or ac current; to achieve those aims it must be paired with a dc-dc converter on the output, adding more active devices and filtering components. As mentioned previously, the six-pulse rectifier has high harmonics. Twelve-pulse converters commonly use phase-shift transformer pairs to eliminate the 5^{th} and 7^{th} harmonic from the nonlinear loads, but size and weight of these transformers are a major downside in SPS applications [18]. Another issue is fault handling; since diodes are uncontrolled, in the diode rectifier, generator will feed into the short circuit, need extra switches to clear the fault [19]. In a series multi-pulse diode rectifier, a short circuit in one unit renders the other units useless as well [20]. Also, the large dc filter capacitors necessary for the stabilization of the dc bus contribute to dc transients and make it more difficult to clear faults. De-excitation of the generator is one way to limit fault current, but generator dynamics are slow acting compared to the speed of short circuits and the damage they can do [21, 22].

Many practical demonstration systems of SPS solutions have taken advantage of the simplicity of diode rectifiers with the added control possibilities of pairing it with a dc-dc converter (Figure 2.5). The Italian Navy commissioned Naval Package (NP) 1 and 2 for demonstrative purposes. NP1 was a 2 MW system, which used two six-pulse diode rectifiers connected in series, using generator excitation to control the output [23]. The NP2 system had the same power level but double the pulse number, connecting four six-pulse

diode rectifiers in series, and pairing them with dc-dc converters to control the dc output [24, 25]. Another study [26] proposed a diode rectifier and dc-dc converter pairing, this time using a single six-pulse diode rectifier and an interleaved dc-dc stage. The dc-dc stage is a four-phase interleaved boost converter with an integrated gate-commuted thyristor (IGCT) as an active switch; this second stage ensures current limiting, removing the need for a large transformer and reducing the footprint of the rectifier. The interleaving of the dc-dc stage reduced current stress on components in that stage, which must handle the full three phase power. The interleaved dc-dc stage solution was developed further in [8], where a voltage control strategy was presented to coordinate between the two stages. To address the size of transformers in multi-pulse diode rectifier designs, a new shunt transformer design was patented in [18]. In [27] the practicality of the magnetic-integrated multi-pulse converter transformer is shown, and the specific effects on the power quality of the system are investigated.

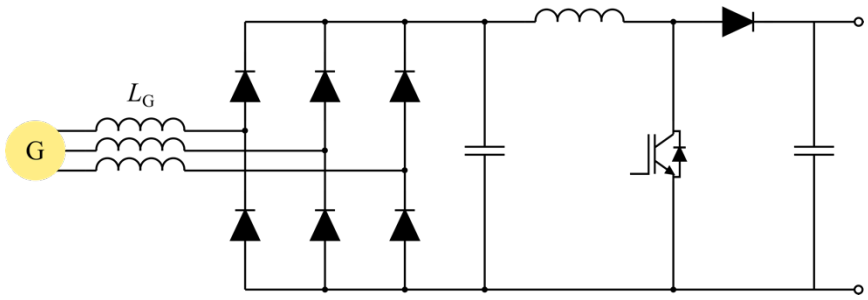


Figure 2.5 Diode rectifier with dc-dc boost converter.

2.3.2 Thyristor Rectifiers

The thyristor bridge rectifier topology (Figure 2.6) is laid out in much the same way as the diode rectifier except the passive diodes are replaced with thyristors. Thyristors are robust devices that are already used commercially in SPS [28, 29]. They act similarly to diodes except they block forward voltage conduction until receiving an external trigger. By controlling the phase-angle of the thyristor turn-on, limited control of the dc voltage is possible [29]. Like the diode rectifier, this topology's basic form is a six-device bridge

rectifier but is often expanded to twelve and twenty-four pulse designs. A higher number of pulses corresponds to improved power quality, increased frequency of output ripple, and decreased amplitude of output ripple [30]. Bridges in multi-pulse thyristor rectifiers (TRs) can be connected in parallel or series depending on turns ratio of transformer [26]. In a six-pulse thyristor rectifier, the transformer solely provides isolation. In a twelve-pulse rectifier, the transformer is typically delta/delta-wye, with two three-phase outputs, each 30˚ apart. Twenty-four-pulse and above require even more complicated transformer design: twenty-four-pulse uses zig-zag transformers [30] and each source is placed 15˚ apart [29]. Thyristor rectifiers have several advantages such as robustness and fault management, but their disadvantages make their design less straight forward than it first appears. The most robust semiconductor devices commonly used in SPS, thyristors highest thermal withstand of the high-power semiconductors [6]. Thyristor rectifiers can clear dc fault current by changing the firing angle in a technique called fold-back fault control. Active fold-back control was proposed in [31] to achieve even faster fault response. Despite these advantages, thyristor rectifiers still require a large low-frequency transformer, cannot control ac current, and have only limited dc voltage control. The range of voltage control can be expanded, but only at the expense of converter performance, leaving the generator to precisely control ac voltage for proper regulation [26]. Additionally, control of dc voltage implies some amount of reactive power absorption, which would require the addition of another circuit, in which case the designer might as well use the cheaper and simpler diode rectifier with dc-dc converter [20].

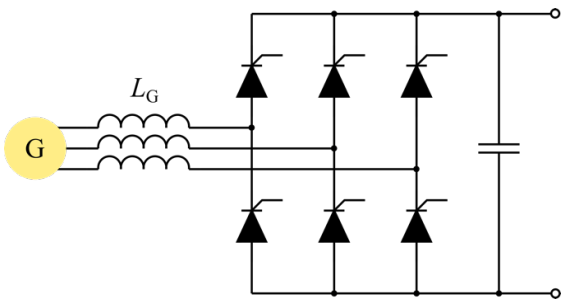


Figure 2.6 Six-pulse thyristor rectifier.

Nevertheless, thyristor rectifiers are popular in the field of research into future SPS. The thyristor firing angle method to control dc voltage was presented and modelled for a 30 –

50 MW system in [29]. In [32], the thyristor rectifier is compared directly to the diode rectifier paired with dc-dc converter, finding that while it had fewer conversion stages, the thyristor rectifier required 75% greater filtering components to the diode rectifier solution. In [2], it is noted that as of 2022, thyristor rectifiers are already commonly used in low voltage shipboard networks, while research is being done to progress to medium voltage systems.

2.3.3 Active Rectifiers

Another topology with the same format is the active rectifier, which simply replaces the diode or thyristor with active semiconductor switches (Figure 2.7). The active rectifier uses IGBTs, which are fully active semiconductor devices which require a trigger for turning on and off. This allows for full control of the voltage and current, as well as directional flow of power. Active rectifiers were proposed to replace passive diode rectifiers to improve control flexibility, but the overall system must be designed to take best advantage of this new topology [33]. To ensure proper voltage regulation, it's necessary to have a voltage or flux regulator on generator so that the active rectifier can operate as designed [34].

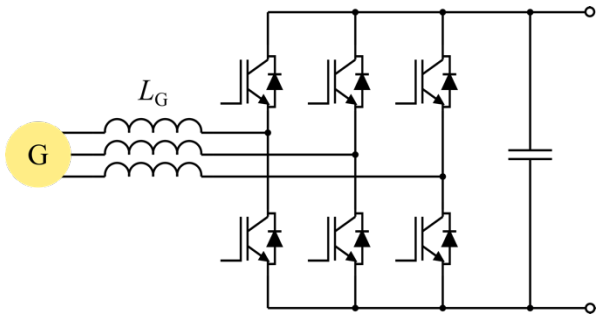


Figure 2.7 Six-pulse active rectifier with IGBTs.

Though active rectifiers have been considered for SPS, their disadvantages tend to outweigh the gains. The advantages include controllable power factor, lower harmonic input, bidirectional power flow, and control of the dc voltage [33]. However, even if all diodes in rectifier are replaced with IGBTs with anti-parallel diodes, the generator can still feed a short circuit fault through the diodes [19]. Additionally, active devices increase cost

and complexity, and the bidirectional capability not necessary for conversion from generators [2]. So far, they have only been studied, not implemented in practical systems.

2.3.4 Modular Multilevel Converters

Modular converter topologies lend themselves well to the design of high-power systems like SPS [2]. The most investigated one of these in SPS is the modular multilevel converter (MMC), shown in Figure 2.8. Each MMC leg has an upper and lower arm with N number of submodules with a floating dc capacitor, as well as an arm inductor in series the submodules [35]. These inductors, in series with PEBBs, can be used to limit fault current [36]. The submodules can be either half bridge (HB) or full bridge (FB) configuration (Figure 2.9). The HB-submodule-based MMC is cheaper but cannot handle faults as well as FB. To interrupt fault current, one phase leg must generate negative voltage on the dc bus, and HB PEBBs can only be positive or zero instantaneous voltage [36]. Multilevel topologies such as neutral-point-clamped converters are limited in voltage levels by practical issues like voltage imbalance; MMC submodules can be stacked to increase voltage without those issues.

The flexibility and redundancy of MMC make it an attractive solution for SPS, at the cost of a bulky footprint and high price of design and manufacture. The modularity of the converter means that converters with different voltages and power levels can use the same submodules, and mass production of these submodules could help with cost [37]. The MMC can be used also as dc-dc converter [38], and due to its flexible design the PEBBs could be used to design MMCs in different areas of the ship with different needs but the same fundamental building blocks. Additionally, the capacitors in each submodule can be used to integrate energy storage into the converter itself [39]. Other advantages include lower switching frequency, low harmonic content, fewer passive elements necessary for filtering, current limiting ability, redundancy, and the reduction of voltage across individual switching devices [37]. On the other hand, the many levels in this design lead to bulkiness and a large footprint, and more components lessen the reliability and efficiency compared to two-level rectifiers. The control of this converter also requires more engineering and developmental capital.

cascaded without limit theoretically [40].

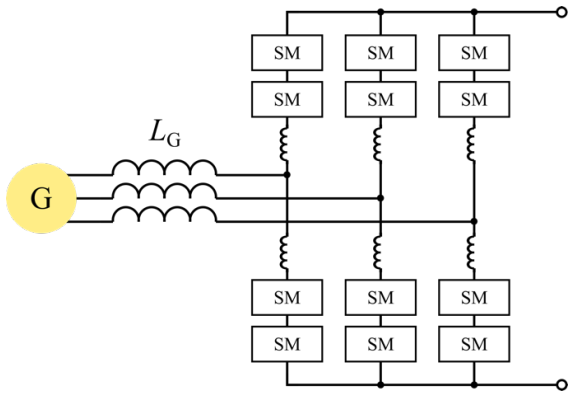


Figure 2.8 Example MMC with N = 2.

Research is being done on MMC and its fault handling capabilities and application in SPS [37, 41, 36]. The medium voltage dc (MVDC) power hardware-in-the-loop (PHIL) laboratory at Florida State University Centre for Advanced Power Systems created a 5 MW system with four 6 kV MMCs that can be connected in series to deliver 24 kV, designed to be able to test fault management in breaker-less MVDC SPS [37, 41]. Another group tested the use of Silicon Carbide (SiC) devices in an MMC with FB submodules to address fault response issues in MVDC SPS [36].

Other multilevel topologies are typically not used as rectifiers in SPS design, as their advantages are outweighed by their disadvantages [4]. For instance, three-level voltage source converters have the same problem as two-level active rectifiers in that they cannot control fault current because the freewheeling diodes conduct, and they become diode rectifiers when the dc voltage drops below a certain threshold [41]. A dual-active bridge-based rectifier has been proposed to provide galvanic isolation between the ac and dc sides, but it does not have the expandability of the MMC topology [26]. Ultimately, these topologies have the complexity of the MMC but none of the other benefits of MMC such as modularity and flexibility.

(a) (b)

Figure 2.9 Common submodule configurations for MMC converter a. full bridge b. half bridge.

2.4 Comparison of topologies

Table 2.1 summarizes the strengths and weaknesses of the existing rectifier topologies. One study [42] compared the reliability of two-level, three-level, and MMC converters using stochastic processes to predict the behaviour of the IGBTs. It was found that while MMCs performed better in the short term, the two-level and three-level converters had lower predicted failure rates in the long term. A comparison of protection schemes using a six-pulse diode rectifier, six-pulse thyristor rectifier, or active rectifier, found the thyristor rectifier was most promising because of fault current blocking and thermal withstand, i.e., higher surge current rating [6]. Comparing the large signal stability behaviour of the thyristor converter vs. the diode rectifier paired with dc-dc converter, it was found that the systems exhibited similar behaviour, but the thyristor converter required larger filter components to achieve equivalent performance [32]. Thyristor-based converters and MMCs with FB submodules can stop energy flow in case of fault, limiting damage to the converter, and in [19] it is shown that the dc link capacitors in the MMC submodules can be used to store short circuit energy, further increasing its fault-limiting capabilities. Some studies, e.g., [2], have suggested that MMC is the preferred design for high power ships and smaller ships with radial power systems should use diode or thyristor rectifiers because the gains in control of the MMC are only worth it at higher power. However, as noted previously, the reliability of all topologies lessens at higher powers, and MMC is already the least reliable topology. According to [11], the diode rectifier is the ideal choice for SPS because they are already in extensive commercial use, while the fault-limiting of the

thyristor rectifier and voltage control of the MMC can be achieved with the correctly designed dc-dc converter, saving space, cost, and achieving the most reliable system.

TABLE 2.1 COMPARISON OF TOPOLOGIES FOR AC-DC CONVERTERS FOR SPS

	Diode	Thyristor	Active	MMC	
				HB	FB
Output voltage levels	Two	Two	Two	2N+1*	
Switching frequency	50/60 Hz	3-10 kHz		100s Hz	
Number of Switches	6/12/24 diodes^	6/12/24 thyristors^	6/12/24 IGBTs^	12N	24N
Control complexity	None	Low		High	
DC bus regulation	No	Some	Yes	Yes	
Reliability	High	High	Medium	Low	
Fault tolerance	Low	Medium	Low	Medium	High
Size of passive filter	Medium-Large	Large	Medium	Small	

* N represents the number of submodules per arm, ^ depends on paralleling design.
Table modified from [11].

2.5 Capacitor Compensation Techniques

Passive components such as capacitors and inductors are included in electronics designs to diminish or let pass certain frequency bands of signals. Capacitors tend to block dc currents but allow higher ac frequencies to pass through, while inductors do the opposite. Since the generators used in SPS include a large inductance as part of their architecture, the compensation techniques considered will be capacitive in nature. There are two types of capacitor compensation: shunt and series.

2.5.1 Shunt Capacitor Compensation

Shunt capacitor compensation is primarily used to filter high frequency ac harmonics out of a signal, as it will pass those frequencies. In ac power systems, capacitor banks connected or switched in parallel configurations are used to improve power quality that is degraded due to nonlinear loads proliferating on the utility, as well as to balance loads [43]. Some benefits of shunt capacitor compensation are that they need only be sized for voltage

and ripple currents. However, they are susceptible to overvoltage failures and values must be carefully chosen to avoid LC resonances that will affect the machines on either end of the line [44]. Shunt capacitors are also used in power electronic circuits to filter out the high frequency voltage ripple created by switching regulators.

2.5.2 Series Capacitor Compensation

Series capacitor compensation refers to the configuration where a capacitor is connected in series between the input and output of the signal. This technique is used in ac power systems to compensate for the inductive reactance of long transmission lines [45]. In comparison to shunt capacitor compensation, the capacitor here must pass the full rated current of the system, leading to a shorter expected lifetime and increase in the volume necessary for these components. Another potential drawback is the occurrence of subsynchronous resonance (SSR) in ac generators [46]. SSR occurs when the resonant frequency of the inductance of the armature and the compensating capacitance is below the excitation frequency of the generator. This can happen either as a result of long-term system operation at a non-optimal point or a fault event that increases the strain on the generator's mechanical parts [47]. Research is being done on mitigation techniques of SSR as it is a common problem with the interaction of series-compensated transmission lines and the induction generators used in wind farms [48].

For ac-dc converters used in marine SPS, there are several benefits to using series capacitor compensation. It will allow for the compensation of the large inductive impedance of the generator at the ac frequency, while allowing the high frequency operation of the converter to continue unimpeded. As the value of per unit reactance goes so, the actual value of capacitance decreases, so at very high levels of impedance, the compensating network will actually be smaller.

2.6 Summary

SPSs continue to need technological innovation and ac-dc conversion is an important aspect in their design. The climate crisis has created the desire to use renewables as much as possible in transportation, as the shipping industry is a large contributor to the carbon output of humanity. Increasing efficiency and decreasing the weight and footprint of

shipboard power systems also leads to less energy used and carbon emitted. Designers of electrical systems must achieve all of this to comply with new environmental regulations while additionally hitting the market in the most important aspects of traditional ship design: cost, reliability, and power density.

The existing literature has investigated several ac-dc topologies, each with their own strengths and weaknesses. The diode rectifier is simple and relatively cheap, but high harmonics necessitate large filtering elements and by itself it has limited control over output voltage or fault-limitation. For this reason, it is often paired with a dc-dc converter such as a boost, which only adds one active switch per three phases and achieves much greater control over voltage and decreases harmonics. The thyristor rectifier is also simple and cheap and additionally can limit fault current. However, the necessary passive components are even larger than those needed for a simple diode rectifier, and some studies claim that an additional circuit is also required for full regulation of the voltage and to absorb power during a fault. The active rectifier provides voltage regulation and control flexibility, but at higher cost and without the modularity and fault current limitation of the FB-MMC. The MMC using FB submodules can achieve the same harmonic levels with much smaller passive filters and has fault-handling capabilities far beyond the previous topologies. However, the complexity, cost, and many semiconductors make it less attractive as a solution for all contemporary SPS. The topology presented in the following chapters will build upon the diode rectifier paired with the boost converter, taking advantage of the simple implementation, and adding an ac compensation element.

While these solutions take for granted the high impedance of the ac generators, there is more work to be done in mitigating this impedance. By looking at compensation on the ac side, the design parameters of the ac-dc conversion stage become less stringent, and more options become available. This compensation technique can in future be applied to existing topologies as well to improve their performance. The advantages of this design are that the boost converter can use impedance of the generator as the boost inductor and there is no need for capacitor between diode rectifier and boost. The proposed technology uses twelve diodes for three phases; however, this is not necessarily a downside as diode rectifiers often use twelve and twenty-four-pulse designs.

CHAPTER 3: NEW RECTIFIER FOR MARINE APPLICATIONS WITH COMPENSATING CAPACITOR AND BOOST CONVERTER STAGE

Chapters 1 and 2 introduced the problems faced by designers of ac-dc converters in shipboard power systems (SPS) and highlighted the major topologies used in the industry today and being researched for future use. This chapter presents a new rectifier topology based on the ac-dc boost converter, which uses series capacitor compensation on the ac side to overcome generator impedance and deliver high power quality. First, the circuit topology is described, then circuit operation and relevant time-averaged current equations are derived. Design principles are presented based on the operation of the circuit. Equations for power factor (PF) and total harmonic distortion (THD) are derived and the predictions are discussed.

3.1 Proposed Topology

Figure 3.1 shows the circuit diagram of the (a) three-phase and (b) single-phase boost converter with the proposed series capacitor compensation. For MVAC applications, there is a transformer included in the powertrain, which is shown on the inputs in Figure 3.1; for MVDC IPS this would not be present [11]. For ac generator applications, the converter must have three phases, the outputs of which are connected in series to generate a larger dc link voltage. The twice line frequency voltage ripples on the individual output capacitors effectively cancel each other out, for a much smaller ripple on three-phase output voltage V_{dc}. The diode bridge provides uncontrolled rectification, which is ideal in SPS as cost and complexity are both detrimental to the success of power systems in marine applications. The boost converter uses the internal generator impedance, which is usually a hinderance to converter performance, as the boost inductor, allowing the output voltage to be controlled with a single active switch and boost diode. The addition of the compensating capacitor decreases ac current harmonic content to acceptable levels and since this topology does not need a dc link between rectifier and boost, does not significantly add to the passive elements of the design.

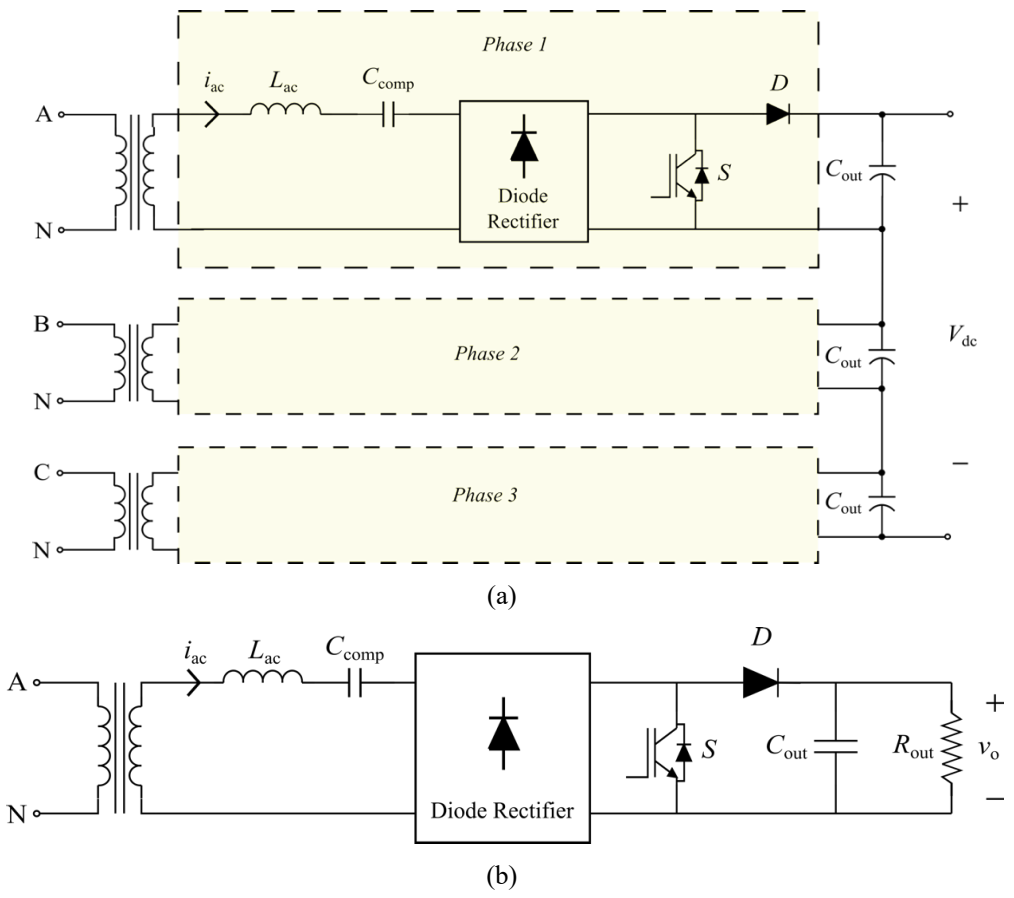


Figure 3.1 Proposed boost converter with series compensating capacitor Ccomp (a) three-phase (b) single-phase.

The single-phase version of the circuit in Figure 3.1b will be used to simplify the analysis and design method presented in this section. A traditional ac-dc boost circuit consists of a diode rectifier, an inductor, a switch *S*, a diode *D*, and an output capacitor to smooth the rectified and boosted voltage. The inductor acts as a power storage and transfer element, allowing the duty cycle of the active switch to define the level of the output voltage. This circuit differs from the traditional topology in the addition of the compensating capacitor C_{comp}. This capacitor is placed in series with the inductor L_{ac} on the ac side of the rectifier. L_{ac} is chosen to model the high source inductance of an ac generator, while also acting as the boost inductor element.

3.2 Circuit Operation

Figure 3.2 shows the equivalent circuit that will be used for the sake of analysis. The following assumptions are made:

- v_{in} is a purely sinusoidal voltage.
- Circuit is operated in continuous current mode (CCM).
- Ideal elements used with no parasitic resistances.
- Switching frequency f_{sw} is several orders of magnitude greater than line frequency f_{ac}.

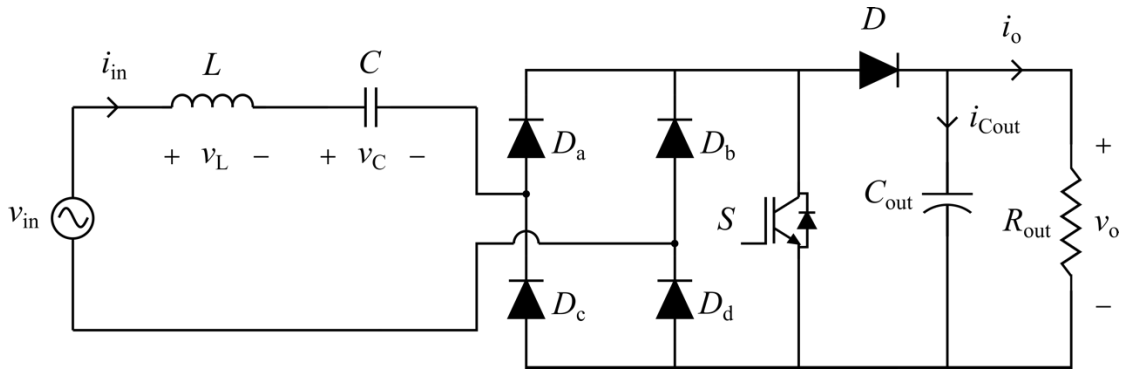
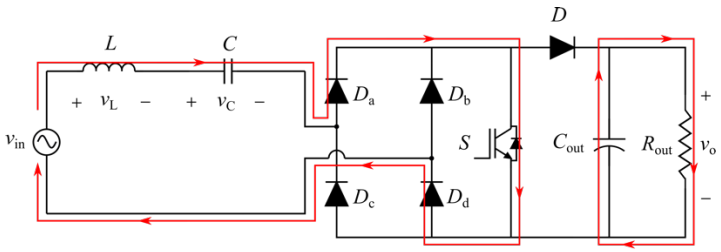
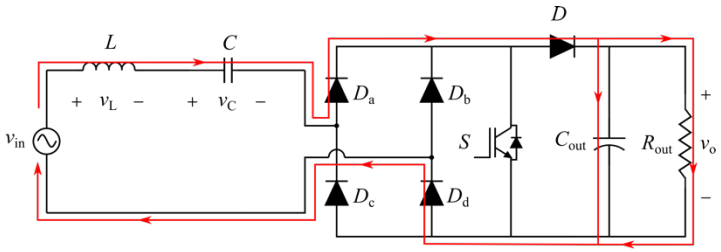
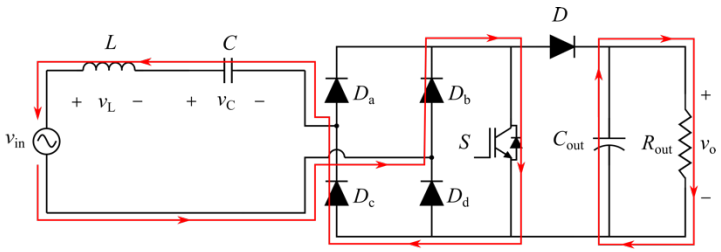


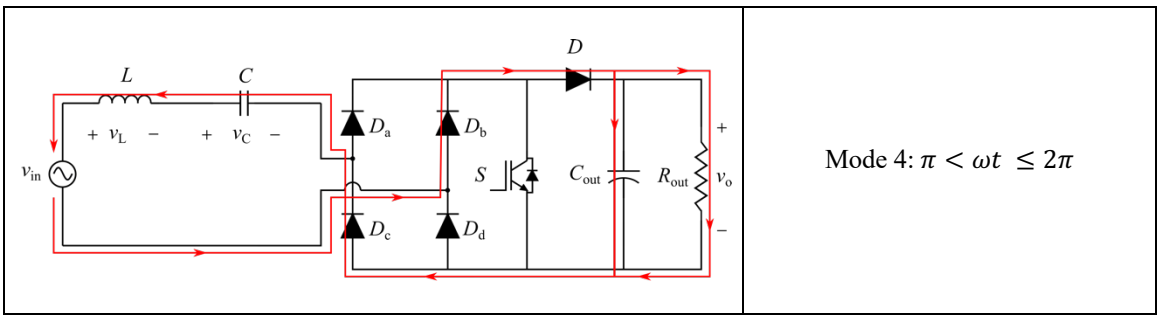
Figure 3.2 Equivalent circuit used for analysis.

The sequence of operation of the circuit is shown in Table 1. Assuming continuous current, the boost has two distinct states per switching period, one when the switch is on and one when it is off. The first state has a duration of dT_s where d is the duty cycle of the active switch and T_s is the length of the switching period, or $1/f_s$. The second state then has duration $(1 - d)T_s$. During the first state, the input current i_{in} flows through the switch S, and the voltage over inductor L is equal to v_{in}. During this state, L is charged up as i_{in} rises. Meanwhile, the output capacitor discharges through the load resistor, resulting in v_o decreasing. During the second state, current flows through diode to charge output capacitor, increasing v_o. The inductor discharges as i_{in} falls. In addition to the two switches states, the operation of the circuit is broken into two half-cycles of the sinusoidal input voltage. For the first half cycle, while the voltage is positive, current flows through rectifying diodes D_a and D_d, while during the second half-cycle diodes D_b and D_c become forward biased and

allow current to pass through them. This creates a total of four modes of operation which are detailed in Table 3.1. The equations are the same between the half-cycles but different between the switching states.

TABLE 3.1: SEQUENCE OF OPERATION

Circuit Configuration and Current Flow	Operating Equations
	Mode 1: $0 < \omega t \leq \pi$, $0 < t \leq dT_s$ $v_{in} = v_L + v_C$ (3.1) $0 = \frac{v_o}{R_{out}} + C_{out}\frac{dv_o}{dt}$ (3.2)
	Mode 2: $0 < \omega t \leq \pi$, $dT_s < t \leq T_s$ $v_{in} = v_L + v_C + v_0$ (3.3) $i_{in} = \frac{v_o}{R_{out}} + C_{out}\frac{dv_o}{dt}$ (3.4)
	Mode 3: $\pi < \omega t \leq 2\pi$



Equations (3.1) and (3.3) can be re-written with respect to the slope of i_{in} using the formula for voltage across an inductor.

$$\frac{di_{in}}{dt} = \frac{v_{in} - v_C}{L} \tag{3.5}$$

$$\frac{di_{in}}{dt} = \frac{v_{in} - v_C - v_o}{L} \tag{3.6}$$

Figure 3.3 details the relationship of i_{in} and reference current i_{in}^* during one switching period T_s. The slope of i_{in} is dependent on the size of L and the voltages v_{in}, v_c, and v_o. Figure 3.4 shows the behaviour of the converter currents and voltages in the circuit over two switching cycles. The diode and switch must block V_{dc} and i_{in} increases and decreases with the on and off periods of the switch.

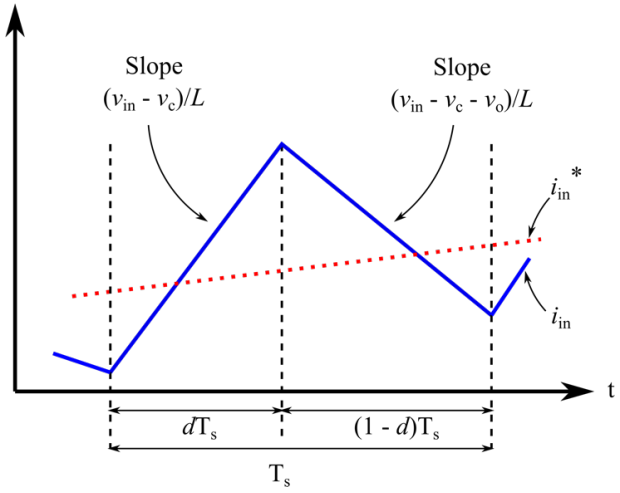


Figure 3.3 Input current behaviour over switching period T_s.

The effect of L on the slope of the current causes the phenomenon known as the *detuning effect* [49]. With no compensating capacitor, the slope of the current while the switch is on

becomes v_{in}/L. At the zero-crossing point of v_{in}, the slope becomes zero, and must recover from there. The larger the ac inductance, the longer it takes to recover, resulting in the detuning effect as shown in Figure 3.5. Detuning angle α is the measurement in radians of where ac current i_{in} reaches the reference current i_{ref} and resumes switching operation. This is relevant to the SPS application because ac generators typically present with a very high inductive impedance, sometimes 1 p.u. or greater. This impedance complicates ac-dc converter design, requiring very high voltages to ensure proper performance without ac compensation.

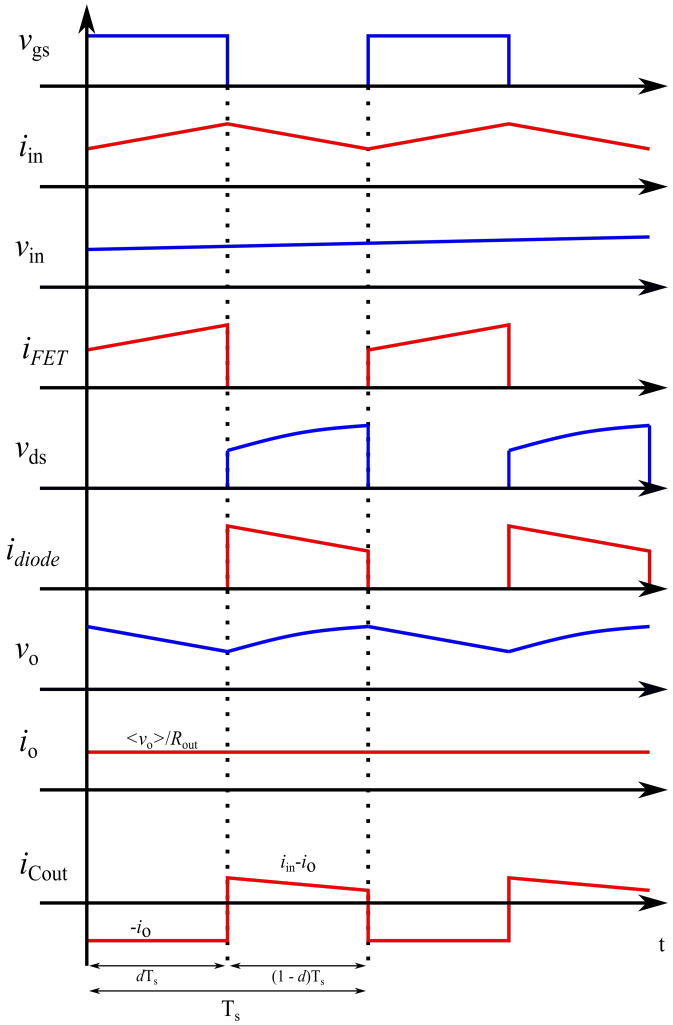


Figure 3.4 Converter current (in red) and voltage (in blue) waveforms over two switching periods, where d is the duty cycle and T_s is the length of the switching period.

The capacitor compensation works in the following way. Capacitive impedance is such that voltage across the capacitor is at its peak when ac voltage crosses zero, thus allowing $\frac{di}{dt}$ to be nonzero. The converter is presumed to be "perfectly compensated" when the detuning angle α is zero, which occurs when the per unit reactance of the capacitor is equal to that of the inductor.

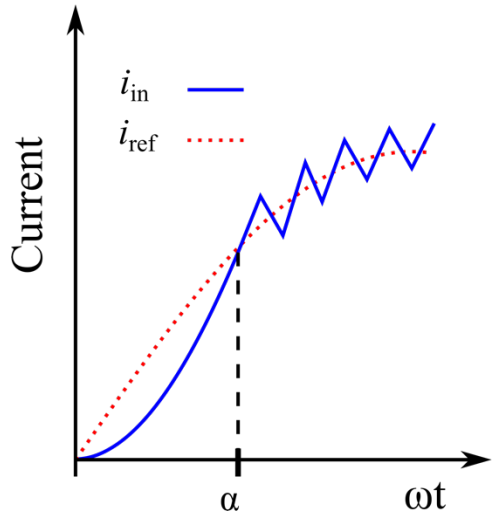


Figure 3.5 Input current behaviour over switching period T_s.

When the compensation is too great, however, the current exhibits overcompensated behaviour. In this case, the voltage across the capacitor is too great and causes the slope of the current to become negative during the on time of the switch. Since the current should be sloping upward during this time and turning the switch off leads to negative slope, the controller keeps the gate signal on while the current falls. It continues falling until it reaches the negative of the reference, where it finally can turn the switch off and resume normal operation. This happens before the zero-crossing of the voltage, and the current is normally regulated on the upswing of the waveform. Figure 3.6 shows the comparison of the undercompensated and overcompensated cases. Detuning angle α was previously discussed and refers to where on the waveform current resumes normal switching operation in the undercompensated case. Angles β and γ are defined for the overcompensated case as the angle at which the current begins to fall below the reference and where it resumes normal function, respectively.

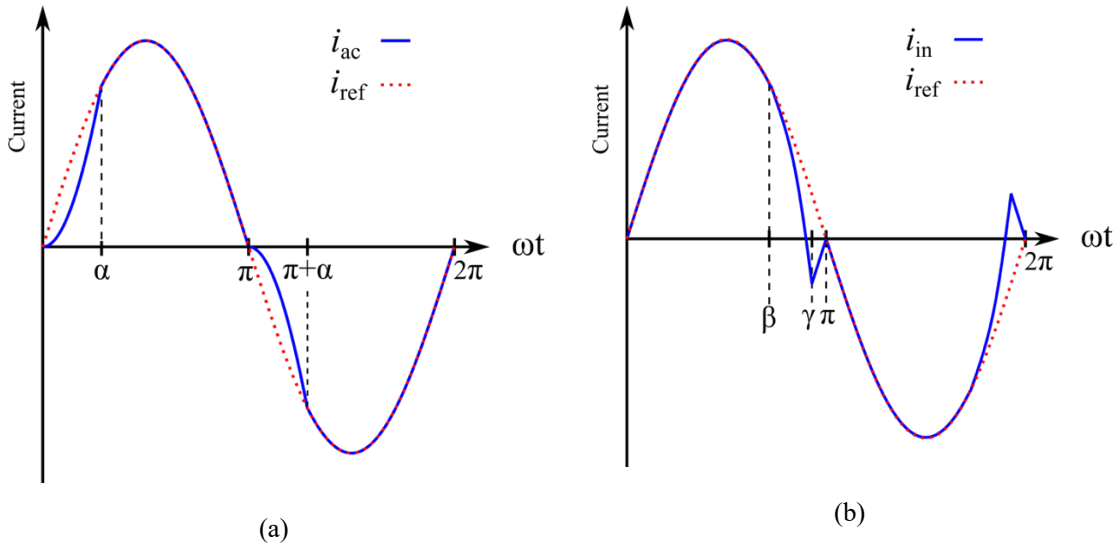


Figure 3.6 Ac current in the (a) undercompensated and (b) overcompensated cases. Angle alpha is the detuning angle in the undercompensated case, angle beta is where the current begins to fall in the over compensated case and gamma is where it regains normal switching operation and rises to zero.

3.3 Time-averaged current equations

To predict the behaviour of and design the circuit, the time-averaged current must be derived. These current equations are important to calculate values like active power, rms current, PF and THD. These values will be used to estimate the time-averaged equations. In Chapter 4, the predicted values will be compared with the results of the circuit simulated in MATLAB/Simulink software to prove the accuracy of the estimated equations. Subsections 3.3.1 and 3.3.2 will outline the derivation of the current equations for both the under and overcompensated cases, as these must be found individually. The current is broken up in distinct segments, two for the undercompensated case and three for the overcompensated case, which each have their own equations and are separated by the angles defined above.

3.1.1 Undercompensated current

While the switch is turned on, the following equality can be written:

$$v_L + v_C = v_{in} \tag{3.7}$$

This equation can be rewritten in terms of current $i(t)$:

$$L\frac{di_{in}(t)}{dt}+\frac{1}{C}\int i_{in}(t)=\hat{v}\sin\omega t \tag{3.8}$$

where, L is ac inductance, C is the compensating capacitance, $\hat{v}$ is the peak of ac voltage, and ω is equal to $2\pi f_{ac}$. Taking the Laplace Transform to move to the s domain, the equation can be rewritten as:

$$L\big(sI(s)-i_{in}(0)\big)+\frac{1}{C}\Big(\frac{I(s)}{s}+\frac{V_c}{s}\Big)=\hat{v}\Big(\frac{\omega}{s^2+\omega^2}\Big) \tag{3.9}$$

where $i_{in}(0)$ and V_c are the initial conditions of the current and the capacitor voltage at $\omega t=0$. In this case, $i_{in}(0)=0$ and thus can be eliminated from the equation, which simplifies to:

$$I(s)\left(sL+\frac{1}{sC}\right)+\frac{V_c}{sC}=\hat{v}\Big(\frac{\omega}{s^2+\omega^2}\Big) \tag{3.10}$$

Solving for I(s) results in:

$$I(s)=\frac{\hat{v}}{L}\Big(\frac{\omega}{s^2+\omega^2}\Big)\Big(\frac{s}{s^2+a^2}\Big)-\frac{V_c}{aL}\Big(\frac{a}{s^2+a^2}\Big) \tag{3.11}$$

where $a=1/\sqrt{LC}$. Taking the Inverse Laplace Transform to move back into the time domain, the time-averaged equation for $i_{in}(t)$ in the undercompensated case is defined as follows:

$$i_{in}(t)=\begin{cases}\dfrac{\sqrt{2}V_{in}}{X_{lC}}(\cos at-\cos\omega t)-\dfrac{V_C}{aL}\sin at\,, & 0<\omega t<\alpha\\ \sqrt{2}I_{in}\sin\omega t\,, & \alpha<\omega t<\pi\end{cases} \tag{3.12}$$

3.3.1 Overcompensated current

In the overcompensated case, there are three segments of current to define. The first segment is simply the expected sinusoidal current, while the third segment is the negative of that. The second segment, falling between β and γ, can be solved for using the same equation as the undercompensated case, but using the initial condition of $\omega t=\beta$. To simplify the analysis, this initial condition can be taken as the starting point of the current, in which case the ac voltage must be shifted by β. Therefore, the starting equation is:

$$L\frac{di_{in}(t)}{dt}+\frac{1}{C}\int i_{in}(t)=\hat{v}\sin(\omega t+\beta) \tag{3.13}$$

Taking the Laplace Transform to move to the s domain, the equation can be rewritten as:

$$L\big(sI(s) - i_\beta\big) + \frac{1}{C}\left(\frac{I(s)}{s} + \frac{V_{c\beta}}{s}\right) = \hat{v}\left(\frac{s\sin\beta + \omega\cos\beta}{s^2 + \omega^2}\right) \tag{3.14}$$

where i_β and $V_{c\beta}$ are the initial conditions of the current and the capacitor voltage at $\omega t = \beta$. By manipulating terms and solving for I(s), the following equation in the Laplace domain is reached:

$$I(s) = \frac{\hat{v}}{L}\left(\frac{s\sin\beta + \omega\cos\beta}{s^2 + \omega^2}\right)\left(\frac{s}{s^2 + a^2}\right) - \frac{V_{c\beta}}{aL}\left(\frac{a}{s^2 + a^2}\right) + i_\beta\left(\frac{s}{s^2 + a^2}\right) \tag{3.15}$$

Taking the Inverse Laplace Transform to move back into the time domain, the time-averaged equation for $i_{in}(t)$ in the overcompensated case is defined as follows:

$$i_{in}(t) = \begin{cases} \sqrt{2}I_{in}\sin\omega t\,, & 0 < \omega t < \beta \\ \dfrac{\sqrt{2}V_{in}}{X_{lC}}\left(\dfrac{-\omega\cos\beta\cos at + a\sin\beta\sin at + w\cos(\beta + \omega t)}{a^2 - \omega^2}\right) - \dfrac{V_C}{aL}\sin at + i_\beta\cos at\,, & \beta < \omega t < \gamma \\ -\sqrt{2}I_{in}\sin\omega t\,, & \gamma < \omega t < \pi \end{cases} \tag{3.16}$$

3.4 THD and Power Factor

THD and power factor of the input current are important values to be able to predict to design the system. The level of harmonics in the input current will determine the efficiency of the converter and large harmonics can lessen the lifetime of the ac generator. THD is a measure of how much of a signal is made up of non-fundamental components.

3.4.1 Total Harmonic Distortion

To calculate THD, the Fourier coefficients of the first harmonic of the current, a_1 and b_1 are calculated. These are used to calculate angle ϕ, which represents the phase shift of the fundamental component of i_{in} from v_{in} [49].

$$a_1 = \frac{\omega}{\pi}\int_0^{2\pi/\omega} i_{in}(t)\cos(\omega t)\,dt \tag{3.17}$$

$$b_1 = \frac{\omega}{\pi}\int_0^{2\pi/\omega} i_{in}(t)\sin(\omega t)\,dt \tag{3.18}$$

$$\phi = \tan^{-1}\frac{a_1}{b_1} \tag{3.19}$$

THD is then calculated using ϕ and the power factor:

$$THD = \sqrt{\frac{\cos^2\phi}{PF^2} - 1} \tag{3.20}$$

To find a_1 and b_1, i_{in} is broken into its different segments and the harmonic coefficients of each segment are found. For the undercompensated case, these components are designated as follows:

$$a_1 = a'_1 + a''_1 \tag{3.21}$$

$$b_1 = b'_1 + b''_1 \tag{3.22}$$

where, a'_1 is the coefficient of the segment of i_{in} between 0 and α, and a''_1 is calculated from the segment between α and π. The components of b_1 are defined similarly. By integration, the components of the harmonic coefficients of the undercompensated current are found to be:

$$a'_1 = \frac{2\sqrt{2}V_{in}}{\pi X_{LC}}\left(\frac{c\cos\alpha\sin\alpha - \sin\alpha\cos c\alpha}{c^2-1} - \frac{\alpha + \sin\alpha\cos\alpha}{2}\right) - \frac{2V_c}{\pi L}\left(\frac{c - \sin\alpha\sin c\alpha - c\cos\alpha\cos c\alpha}{c^2-1}\right) \tag{3.23}$$

$$b'_1 = \frac{2\sqrt{2}V_{in}}{\pi X_{LC}}\left(\frac{c\sin\alpha\sin\alpha + \cos\alpha\cos c\alpha - 1}{c^2-1} - \frac{\sin^2\alpha}{2}\right) - \frac{2V_c}{\pi L}\left(\frac{\cos\alpha\sin c\alpha - c\sin\alpha\cos c\alpha}{c^2-1}\right) \tag{3.24}$$

$$a''_1 = \frac{2\sqrt{2}I_{in}}{\pi}\left(\frac{\cos^2\alpha}{2} - 1\right) \tag{3.25}$$

$$b''_1 = \frac{2\sqrt{2}I_{in}}{\pi}\left(2(\pi-\alpha) + \frac{\sin 2\alpha}{4}\right) \tag{3.26}$$

where, c is a constant and V_C is the initial capacitor voltage at $\omega t = 0$, defined as follows.

$$c = \frac{1}{\omega\sqrt{LC}} \tag{3.27}$$

$$V_c = -\frac{\sqrt{2}I_{in}}{\omega C} \tag{3.28}$$

For the overcompensated case, the components are designated as follows:

$$a_1 = a'_1 + a''_1 + a'''_1 \tag{3.29}$$

$$b_1 = b'_1 + b''_1 + b'''_1 \tag{3.30}$$

where, a'_1 is the coefficient of the segment of i_{in} between 0 and β, and a''_1 is calculated from the segment between β and γ, and a'''_1 is calculated from the segment between γ and π. The components of b_1 are defined similarly.

$$a'_1 = \frac{\sqrt{2}I_{in}}{\pi}[1 - \cos^2\beta] \tag{3.31}$$

$$b'_1 = \frac{\sqrt{2}I_{in}}{\pi}[\beta - sin\beta cos\beta] \tag{3.32}$$

$$\begin{aligned} a''_1 = \frac{2}{\pi}\Bigg[\frac{\sqrt{2}V_{in}}{L(a^2-\omega^2)}\Bigg(&-\omega\cos\beta\left(\frac{cm_1 - m_2 + \sin\beta}{m_5}\right) \\ &+ \frac{\omega\big(\sin\big(2(\beta+\Delta)\big) - \sin 2\beta + 2\Delta\big)}{4} \\ &+ a\sin\beta\left(\frac{c\cos\beta - cm_3 - cm_4}{m_5}\right)\Bigg) + i_\beta\left(\frac{cm_1 - m_2 + \sin\beta}{m_5}\right) \\ &- \frac{V_{c\beta}}{aL}\left(\frac{c\cos\beta - cm_3 - cm_4}{m_5}\right)\Bigg] \end{aligned} \tag{3.33}$$

$$b''_1 = \frac{2}{\pi}\left[\frac{\sqrt{2}V_{in}}{L(a^2-\omega^2)}\left(-\omega\cos\beta\left(\frac{cm_3+m_4-\cos\beta}{m_5}\right)+\frac{\omega\sin\Delta\sin(2\beta+\Delta)}{2}\right.\right.$$
$$\left.+a\sin\beta\left(\frac{c\sin\beta-cm_2+m_1}{m_5}\right)\right)+i_\beta\left(\frac{cm_3+m_4-\cos\beta}{m_5}\right) \quad (3.34)$$
$$\left.-\frac{V_{c\beta}}{aL}\left(\frac{c\sin\beta-cm_2+m_1}{m_5}\right)\right]$$

$$a'''_1 = \frac{\sqrt{2}I_{in}}{\pi}[1-\cos^2\gamma] \quad (3.35)$$

$$b'''_1 = \frac{\sqrt{2}I_{in}}{\pi}[\gamma-\pi-sin\gamma cos\gamma] \quad (3.36)$$

where, c is the constant defined in Equation 3.27, $V_{C\beta}$ is the capacitor voltage at $\omega t = \beta$, and m_1 through m_5 and Δ are variables defined as follows.

$$V_{c\beta} = -\frac{\sqrt{2}I_{in}}{\omega C}\cos\beta \quad (3.37)$$

$$m_1 = \sin(c\Delta)\cos(\Delta+\beta) \quad (3.38) \qquad m_2 = \cos(c\Delta)\sin(\Delta+\beta) \quad (3.39)$$

$$m_3 = \sin(c\Delta)\sin(\Delta+\beta) \quad (3.40) \qquad m_4 = \cos(c\Delta)\cos(\Delta+\beta) \quad (3.41)$$

$$m_5 = c^2-1 \quad (3.42) \qquad \Delta = \gamma-\beta \quad (3.43)$$

3.4.2 Power Factor

Power factor (PF) can be split into two categories, displacement and distortion power factor. Displacement power factor refers to the degrees to which the current leads or lags the voltage, which impacts the amount of real power that is delivered to the output. The closer the zero-crossing of the current is to the voltage's, the closer to unity power factor the system is. Distortion power factor refers to the level of harmonics that are present in the current, or the amount of the signal that is made up of the fundamental frequency versus higher frequency components. In this thesis, power factor refers to the distortion power

factor, as no leading or lagging currents were investigated. PF is defined as the ratio of real power P to apparent power, which is the product of RMS input voltage and current.

$$PF = \frac{P}{V_{in} I_{in}} \tag{3.44}$$

First, the average power Pin is solved for using the following equation and a MATLAB script and breaking the input current into two or three segments according to the level of compensation.

$$P_{in} = \frac{\omega}{\pi} \int_0^{2\pi} i_{in}(t) \hat{V}_{in} \sin(\omega t)\, dt \tag{3.45}$$

I_{in} is calculated using a MATLAB script as well. These values, along with input voltage, were then used to generate the PF values for a range of X_L and X_C values, as shown in Figure 3.7. Input voltage was set to 690 V and input power was set to 4 MW x 1/3 to model a single phase of an ac generator for SPS applications. The figure shows values calculated from solely inductive and capacitive impedance. In reality, generators typically have a high resistance coming from the armature, which would reduce the PF to as low as 0.65 [16]. This figure is focused however only on the comparative effects of capacitive and inductive impedance.

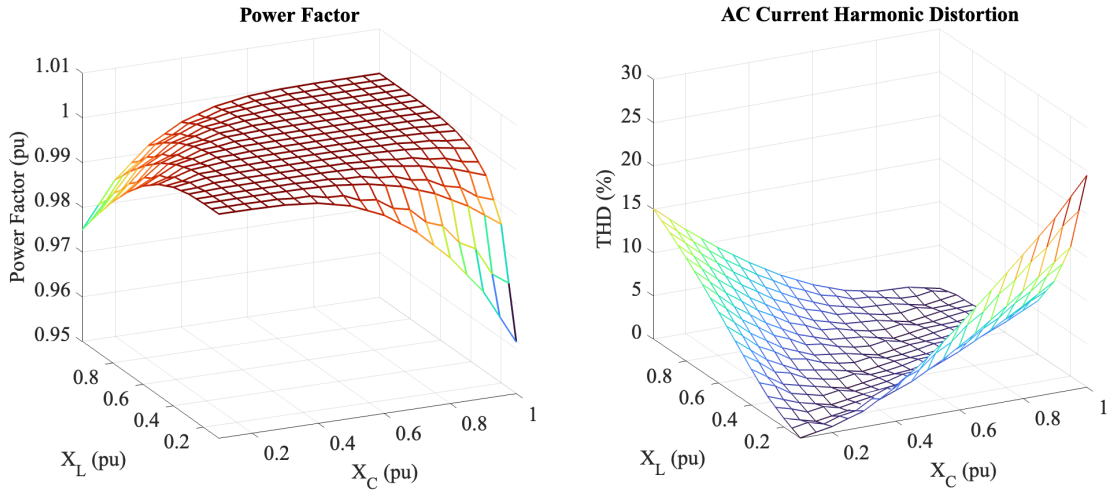


Figure 3.7 Power factor and total harmonic distortion of ac current calculated for a range of X_L and X_C using the mathematical models described in 3.4.1 and 3.4.2.

3.4.3 PF and THD Analysis

The plots in Figure 3.7 show the calculated THD and PF of ac current with parameter ranges of L_{ac} = 0.1 to 1 p.u. and C_{comp} = 0.1 to 1 p.u. The general pattern immediately clear is that THD is lower, and PF is higher when the values of inductive and capacitive reactance match more closely. On closer inspection, it becomes clear that THD is the limiting factor. In the PF plot, the warm colour region (yellow, red, orange) represents the values closest to 1, and when compared to the *z*-axis, most of this plot falls above a power factor of 0.95. i.e., all but the most extreme cases are within an acceptable range of power factor. However, the THD plot on the right shows much steeper slopes in the areas of the graph where the reactances are not equal. Only the deep purple range of the graph falls under the 5% THD limit acceptable for naval ships applications. This suggests that THD is the limiting factor for this design; while PF may be acceptable for given parameters, THD may not be. Therefore, the focus of the analysis of results in further chapters will be on the THD of the ac current.

3.5 Design Principles

An important aspect of the analysis of a newly proposed circuit is the question of how to design the circuit to given standards of operation. This section will look at the design of the converter if the impedance and voltage of the ac generator (source) is known, and the output power is defined by the system.

3.5.1 Voltage Ratio

As this is a boost converter, the output voltage is expected to be larger than the input voltage.

Assuming lossless circuit, P = Pin = Po, means that:

$$V_{in}I_{in} = V_oI_o \tag{3.46}$$

where, V_{in} and I_{in} are the RMS values of input voltage and current and V_{out} is the average value of output voltage. Using Kirchhoff's current law, it can be seen that $I_o = (1 - d)I_{in}$, where d is the average duty cycle over the ac cycle. Therefore,

$$V_o = \frac{V_{in}}{(1-d)} \tag{3.47}$$

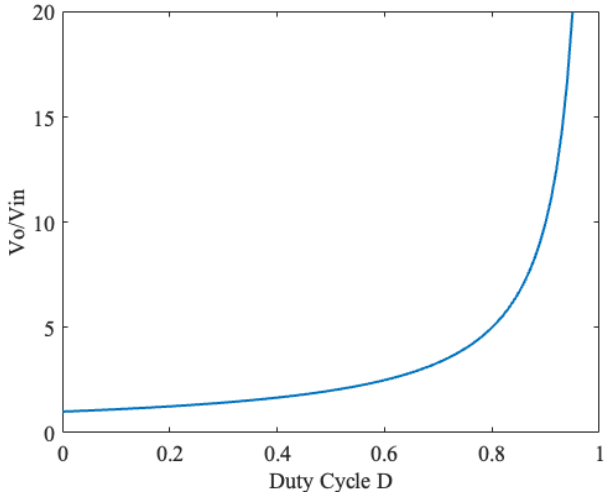


Figure 3.8 Ratio of output voltage to RMS input voltage versus average duty cycle d.

3.5.2 Compensating Capacitor

The ac capacitor is novel addition to this topology, and therefore needs careful consideration as to how it affects the design of the system. First, for a given impedance of the generator, what are the boundaries of the capacitor value that allow the system to remain within recognized limits of harmonics and power factor. Input voltage was set to 690 V and input power was set to 4 MW x 1/3 to model a single phase of an ac generator for SPS applications.

Figure 3.9 shows the total harmonic distortion of the ac input current as the compensating capacitor varies, calculated using the derived equations in Section II – B for different values of inductive reactance from the source. The dotted line shows the THD level of 5%, under which the THD will be in a safe range for industrial applications. Where the reactance of the generator is equal to the reactance of the compensating capacitor, THD is zero. However, there is a range of acceptable values of X_C which keep THD below 5%. From a design perspective, the smallest value of a capacitor is generally the cheapest and most spatially efficient. X_C is inversely proportional to the value of C_{comp}; therefore, the designer should choose the maximum value of X_C for the given value of X_L to stay below 5% THD.

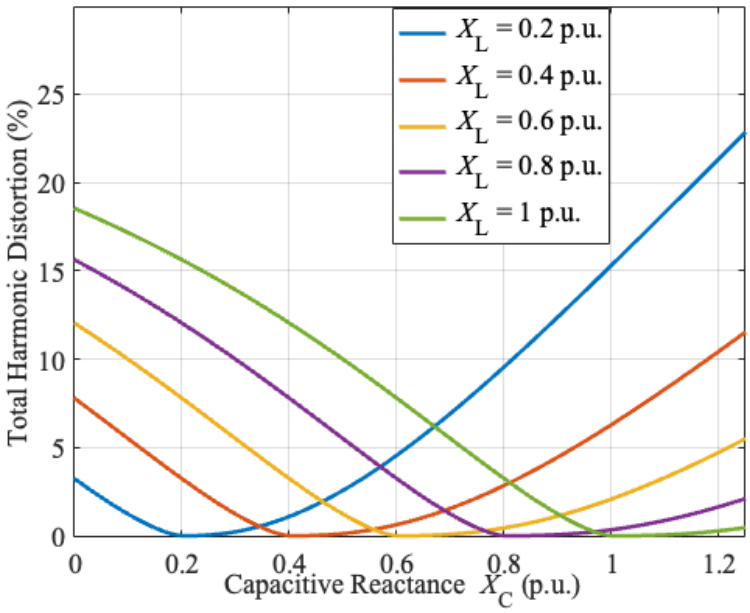


Figure 3.9 Total harmonic distortion of ac input current verses values of compensating reactance for different values of generator impedance XL. Values generated used Vin = 102 V, Iin = 6 A.

Power factor can be a limiting element in a design as well. Figure 3.10 shows the effect of C_{comp} on power factor at different values of generator impedance. When the reactance values are equal and opposite, PF is 1. However, some reactive power is permissible and can allow the designer some flexibility in component sizes and control. Generally speaking, PF of over 0.9 is acceptable. It can be seen by comparing Figures 3.9 and 3.10, which were plotted using the same parameters, that THD rises above 5% in each direction more quickly than PF falls below 0.9. In fact, for these parameters, PF never falls below 0.96. Therefore, THD is the limiting design factor of C_{comp} between the two.

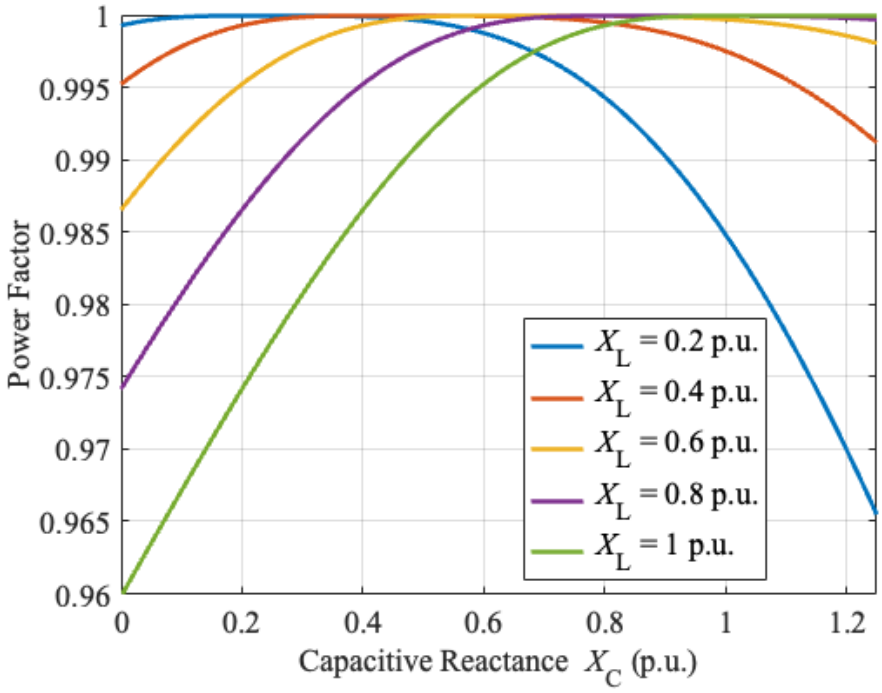


Figure 3.10 Power factor of ac input current verses values of compensating reactance for different values of generator impedance X_L.

3.6 Summary

In this chapter, a novel circuit for ac-dc power conversion in SPS was presented. The circuit uses an ac capacitor to compensate for the large inductive reactance characteristic of ac generators, present in all SPS. This inductive reactance would otherwise make the use of an ac-dc boost converter impractical because of the detuning effect, which results in harmful harmonics into the ac current. The topology and its operation were described in detail, and equations for ac current were derived. It was shown that the topology addresses the detuning effect and can limit THD to within acceptable levels or nearly eliminate harmonics from the ac current. The effects of over- and under-compensation were investigated and the design criteria for circuit design were presented. In the following chapter, the equations derived here will be tested and verified via simulation to corroborate the design claims made in this chapter.

CHAPTER 4: SIMULATION RESULTS

Chapter 3 discussed the topology of the proposed compensation technique for shipboard rectifiers as applied to an ac-dc boost converter. The circuit was modelled mathematically and shown to be a viable solution to the high THD resultant from the boost topology. In this chapter, the proposed compensation technique is modelled and simulated in MATLAB/Simulink software. The model of the circuit from the previous chapter is verified, proving the design criteria can be met by the topology. The values of detuning angles α and β, power factor (PF), and total harmonic distortion (THD) are compared between the simulated and theoretically generated waveforms to prove the compensation technique works as predicted. The circuit is simulated as a single-phase system first and then expanded to three phases. Two methods of control are considered and compared: hysteresis and sinusoidal pulse width modulation (SPWM). Finally, the results of different input to output voltage ratios are presented to demonstrate the advantage of the compensation technique.

4.1 Simulation description and parameters

The simulated circuit was built in Simulink with the parameters listed in Table 4.1. These values were chosen to be representative of realistic system parameters [24]. The ac generators used in medium- to high-power shipboard power systems are components built and sold by a limited number of manufacturers, and therefore researchers have real-world values to choose from in simulation studies. These values were chosen based on typical shipboard power system (SPS) characteristics [41], as well as values that would most clearly show the differences in compensation levels. 690 V is used as the value of generator voltage except in Section 4.5: Voltage Ratio Comparison; in Section 4.5, the input voltage is adjusted to provide different ratios between input and output voltage. MVDC rectifiers are often designed to provide up to 6 kV, which is set as the three-phase output voltage. Therefore, each individual phase is designed to provide up to 2 kV.

TABLE 4.1: SIMULATION PARAMETERS

Parameter	Value
Number of phases	1
DC Voltage V_{dc}	2 kV / 6 kV
AC Voltage RMS v_{in}	690 V
AC Current RMS i_{in}	1.93 kA
AC frequency f_{ac}	50 Hz
Max switching frequency f_{sw}	10 kHz
Rated power S	1.33 MW / 4 MW
Interfacing inductance L_{ac}	0.25, 0.75 pu*
Compensating Capacitor C_{comp}	0, 0.75 pu*
Output Capacitor C_{out}	10 mF
Load Resistance R_{out}	27 Ω

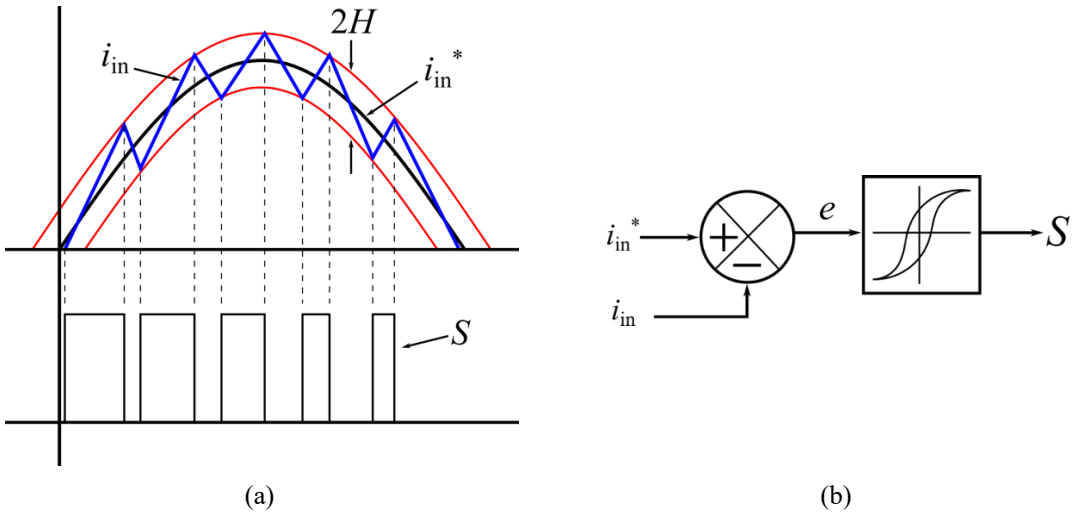
*Results for further values in Appendix A.

4.2 Control Methods

To choose the control method used in the study, two methods were initially used and compared. Hysteresis control has the advantages of ease of implementation and quick reaction to faults, but it has the drawback of a variable switching frequency. Most modern electronics designers prefer fixed switching frequency control methods in order to optimize the system around switching speed, selection of switches, and power losses. To test the effectiveness of hysteretic control versus fixed frequency control, SPWM was chosen as the most basic method of fixed frequency.

Hysteresis control is based on the concept of hysteresis, in which the state of a system depends on its history. In this case, the input current is measured and compared to a reference. When i_{in} is with a certain amount larger than the reference, the switch is turned off; when it is that amount lower than the reference, the switch is turned on. This amount is known as the hysteresis band H. Whether H is added or subtracted to the reference

depends on the state of the switch, i.e., whether it was on or off. This control method is detailed in Figure 4.1.



(a) (b)

Figure 4.1: Generation of gate signals using hysteresis. a. The reference current i_{in}* is compared to measured input current i_{in} to generate gate signal *S*. b. The error *e* between signals is fed to a hysteresis controller, which supplies the gate signals.

SWPM control is a carrier modulation method, which uses an independent sawtooth or triangle waveform to set the frequency and duty cycle of the active switch. For this method, the current is subtracted from a reference, and based on this error a controller, such as proportional-integral (PI), generates a signal to be compared to the carrier. The percentage of the carrier signal that is below the output signal of the controller is the instantaneous duty cycle of the switch. Figure 4.2 demonstrates how this control works.

For the SPWM control simulation, the switching frequency f_{sw} is chosen to be 10 kHz. To have a fair comparison, *H* is chosen to limit the maximum hysteresis switching frequency (f_{max}) to 10 kHz. To calculate the minimum *H*, the minimum on and off times of the switch must be added together; from there, *H* can be solved for. The general equations for the on and off times of the switch are shown in Equations 4.1 and 4.2.

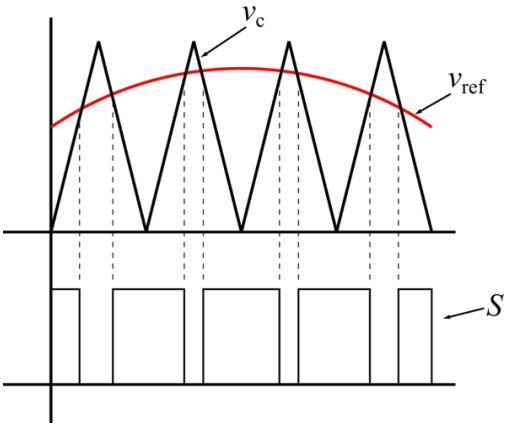


Figure 4.2. Generation of gate signals using sinusoidal PWM. The reference voltage v_{ref} is generated by a PI controller and compared to carrier voltage v_c to generate gate signal S.

$$T_{ON} = \frac{\Delta iL}{v_{in} - v_c} \tag{4.1}$$

$$T_{OFF} = \frac{-\Delta iL}{v_{in} - v_c - V_o} \tag{4.2}$$

Δi is two times H, and the worst-case scenario is the shortest possible on and off times; therefore, the circuit with $v_c = 0$, $v_{in} = \hat{v}_{in}$, and the lowest value of L will be taken as the worst-case scenario. By making these adjustments and adding these equations together, the minimum switching period, T_{min}, can be found:

$$T_{min} = \frac{2HL_{min}(-V_o)}{\hat{v}_{in}(\hat{v}_{in} - V_o)} \tag{4.3}$$

The maximum switching frequency is:

$$f_{max} = \frac{1}{T_{min}} \tag{4.4}$$

By substitution, the minimum hysteresis band H_{min} can be found to be:

$$H_{min} = \frac{-\hat{v}_{in}(\hat{v}_{in} - V_o)}{2f_{max}L_{min}V_o} \tag{4.5}$$

If $\hat{v}_{in} = \sqrt{2} * 690$, $V_o = 2\ kV$, $f_{max} = 10\ kHz$, and $L_{min} = 284\ uH$, the minimum hysteresis band will be $\pm 3.22\%$.

Figures 4.3 and 4.4 show a comparison between the two methods of control, with the switching frequency set to 10 kHz for SPWM and the hysteresis band set to $\pm 3.22\%$ as calculated in Equation 4.5. In each figure, the upper plot shows the hysteresis-controlled current in blue, and the lower plot shows the SWPM-controlled current in magenta, and the sinusoidal reference current is shown in green in each plot.

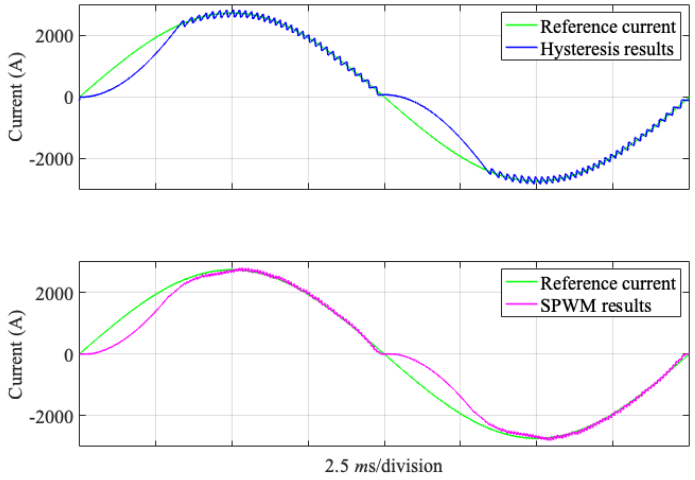


Figure 4.3. Comparison of simulated results collected using X_L = 0.5 p.u., no compensating capacitor, and two different methods of control.

While the hysteresis-controlled current is below the reference, the switch is constantly closed, allowing the minimum time before the current rises to its expected value. Using hysteresis, $\alpha = 61^{\circ}$. However, the SPWM circuit resulted in $\alpha = 90^{\circ}$, which is likely the result of a poorly tuned PI controller.

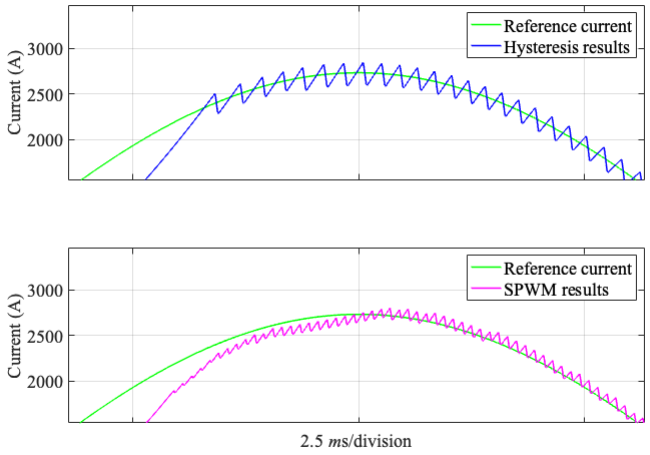


Figure 4.4: Close up comparison of simulated results collected using X_L = 0.5 p.u., no compensating capacitor, and two different methods of control.

Additionally, the resulting THD of the input current was compared using the two control methods. Figure 4.5 shows this comparison. Hysteresis results are shown in blue and SPWM results are in red. With no compensating capacitor, the resulting THDs are not significantly different. However, with a large compensation added, the SPWM control results in consistently larger THD. This is likely because the PI control constants were not optimized. Hysteresis control was determined to provide the results necessary and for the sake of experimental efficiency, it was decided to continue collecting results with hysteresis control.

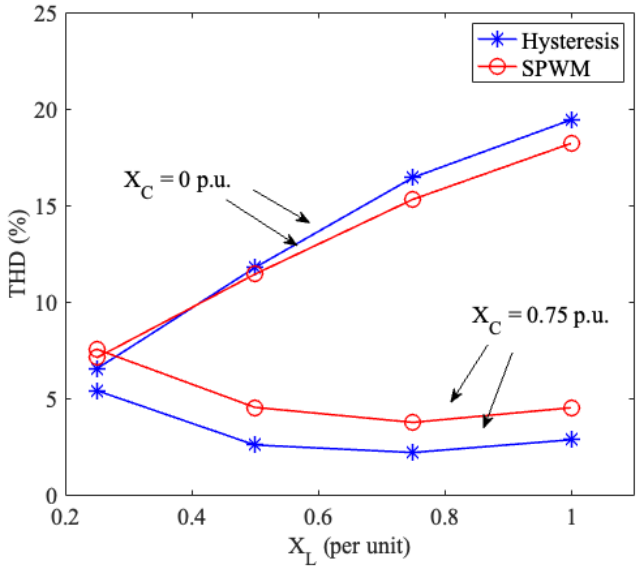


Figure 4.5: A comparison of the THD results from SPWM and hysteresis control with two levels of capacitor compensation.

4.3 Single-Phase Results

Figure 4.6 shows the single-phase circuit under simulation and the control used. L_{ac} is used to emulate the inductive reactance seen from the generator. C_{comp} is the compensating capacitor. The ac voltage is rectified by diode bridge (D_a – D_b), and the boost output converter is represented by S, the active switch, and D, the boost diode. C_{out} smooths the output voltage V_o, which is measured across R_{out}. The input voltage and current are used to measure input power, which is subtracted from the reference power. The resulting error is fed into a PI controller, the output of which is multiplied by a per unit sinewave calculated

from the input voltage. This generates the reference current, which is compared to the measured input current, which through hysteresis generates the gate signal for the switch.

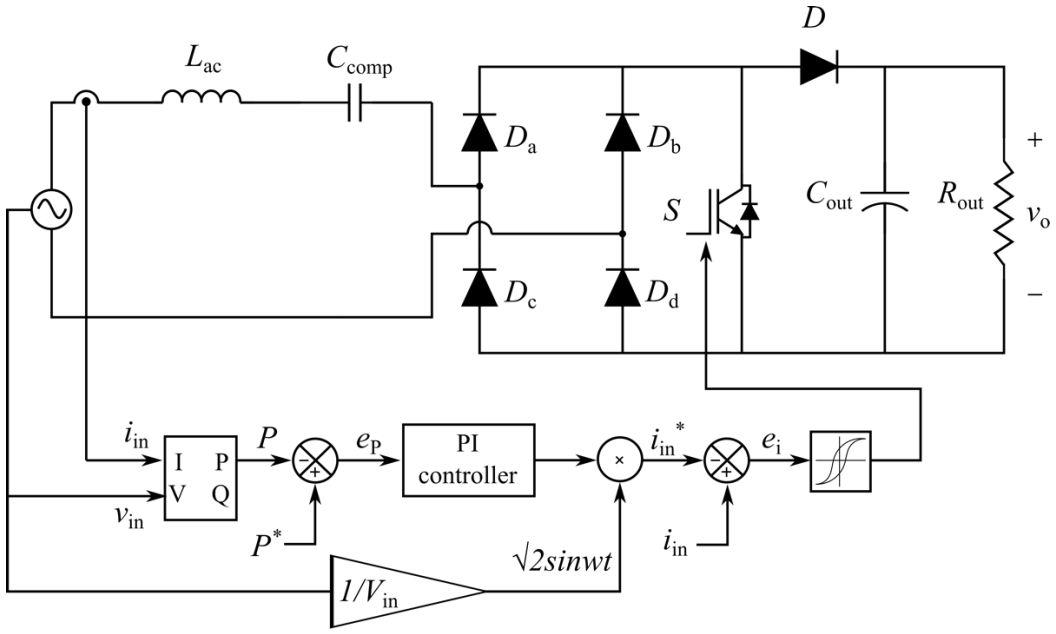


Figure 4.6: Single-phase circuit and hysteresis control diagram.

Figure 4.7 shows the selected simulation results for the ac-dc boost converter with capacitor compensation of 0 p.u. and 0.75 p.u. where v_{in} = 690 V, i_{in} = 1.93 kA, and f_{ac} = 50 Hz. Simulated current is shown in blue while waveforms based on the mathematical analysis of Chapter 3 are shown in green. In Figure 4.7a and b, the detuning effect of an undercompensated circuit can be clearly seen, with detuning angle α increasing with the per unit inductive impedance. In Figure 4.7a, $\alpha = 36^{\circ}$, while in Figure 4.7b, $\alpha = 72^{\circ}$. Moving to Figure 4.7c, the circuit is now overcompensated. For this case, there is no α, but rather angle $\beta = 150^{\circ}$, which is where the current falls from its sinusoidal envelope. Figure 4.7d shows the case of the perfectly compensated circuit, where $X_C = X_L$. The simulated current shows the expected behaviour of following the sinusoidal reference all the way through the waveform, i.e., $\beta = 180^{\circ}$ or $\alpha = 0^{\circ}$.

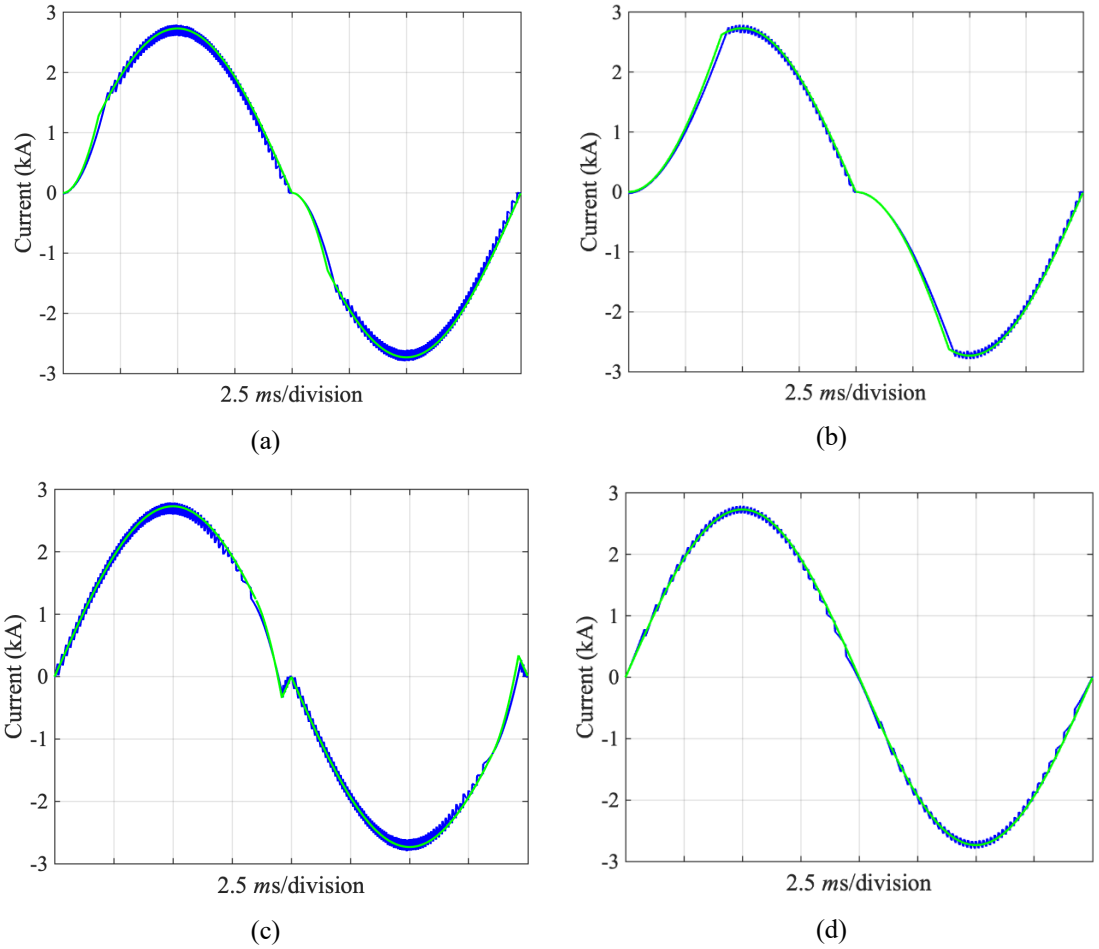


Figure 4.7: Simulated and calculated results with different values of inductance and compensating capacitor. Blue is simulated current, and green is calculated current. a) X_L = 0.25 p.u., X_C = 0 p.u., b) X_L = 0.75 p.u., X_C = 0 p.u., c) X_L = 0.25 p.u., X_C = 0.75 p.u., d) X_L = 0.75 p.u., X_C = 0.75 p.u.

Tables 4.2 through 4.5 show the values of THD and PF for the selected results shown in Figure 4.1. Two conclusions can be drawn from the data: the accuracy of the mathematical model and the limiting factor in the design of the converter. Comparing simulated and calculated values for both PF and THD, the values show the expected increase or decrease in PF and THD with impedance with one notable example. The first row of results in each table was collected for two values of X_L with no compensating capacitor. As expected, there is a decrease in PF and an increase in THD in both the calculated and simulated values as X_L gets larger. Angle α increases with X_L, as can be seen in Figure 6a and 6b, so it is expected for the PF and THD of the current to worsen. The calculated values match the simulated values closely, showing the accuracy of the mathematical model. The THD is

slightly higher for the simulated current in all cases because it contains the instantaneous current deviations, where the calculated values use the time-averaged current. Hence, for the value of THD in Table 4.5 where the impedances have the same per unit value, the THD is exactly 0, as it is calculated from a pure sine wave.

TABLE 4.2: SIMULATED PF

	X_L = 0.25 p.u.	X_L = 0.75 p.u.
X_C = 0 p.u.	0.9994	0.9855
X_C = 0.75 p.u.	0.9999	1.000

TABLE 4.3: CALCULATED PF

	X_L = 0.25 p.u.	X_L = 0.75 p.u.
X_C = 0 p.u.	0.9987	0.9776
X_C = 0.75 p.u.	0.9978	1.000

TABLE 4.4: SIMULATED THD

	X_L = 0.25 p.u.	X_L = 0.75 p.u.
X_C = 0 p.u.	6.62%	16.0%
X_C = 0.75 p.u.	5.24%	2.20%

TABLE 4.5: CALCULATED THD

	X_L = 0.25 p.u.	X_L = 0.75 p.u.
X_C = 0 p.u.	4.42%	14.8%
X_C = 0.75 p.u.	5.01%	0.00%

Comparing the results of PF versus the THD found for these scenarios, THD stands out clearly as the limiting factor in designing for level of compensation. For all values of X_L and X_C, PF remains above 0.95, while THD ranges up to 16% for the selected results. International standards limit the introduction of total THD to the ac power system on a commercial ship to 8% and 5% for naval vessels. Therefore, designers using reactive power compensation should leave margin for THD; if the THD is within an acceptable range, the PF will be as well.

4.4 Three-phase Results

Figure 4.8 shows how the circuit is expanded to three phases. The dc link capacitors of each phase are connected in series to provide an increased dc bus voltage V_o. The values of L_{ac} and C_{comp} are kept the same across all three phases. Results of input current, the

voltages across individual dc link capacitors, and the overall output voltage are collected and presented below.

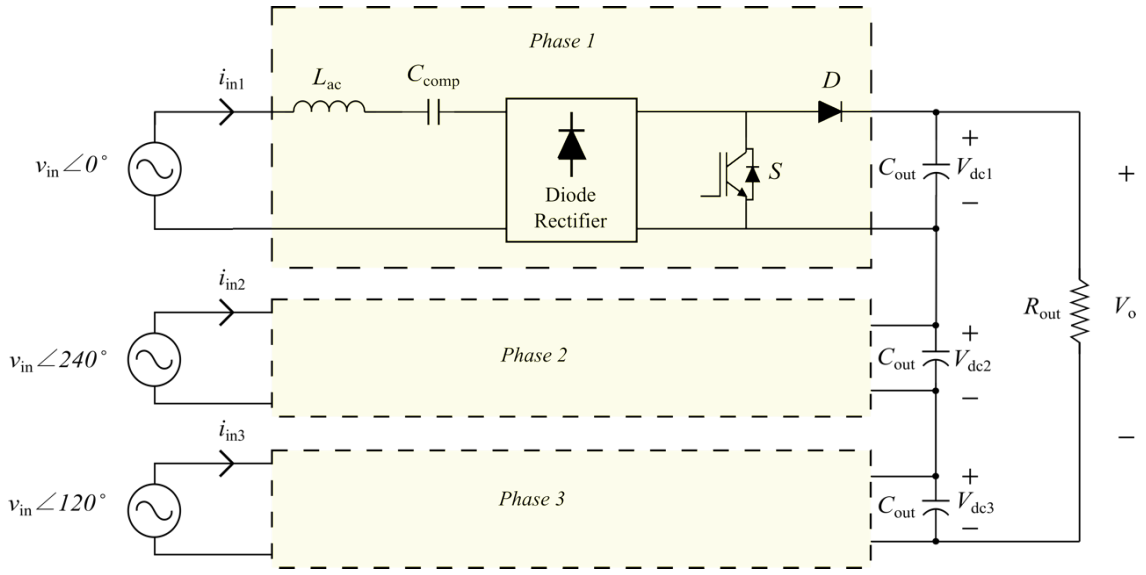


Figure 4.8: Three-phase boost rectifier with capacitor compensation.

First, the operation of the compensation in three phases can be seen in Figures 4.9 and 4.10. Figure 4.9 shows the characteristic detuning effect in three phases with an inductive reactance of 0.75 p.u. The detuning angle $\alpha = 1.43$ radians, the same as the angle observed with these conditions in the single-phase system. This suggests that the analysis of the current in the single-phase circuit is applicable to an increased number of phases. Figure 4.10 shows the resulting current with a compensating capacitor of equivalent per unit value, where the current can be seen to follow the sinusoidal reference with no detuning angle.

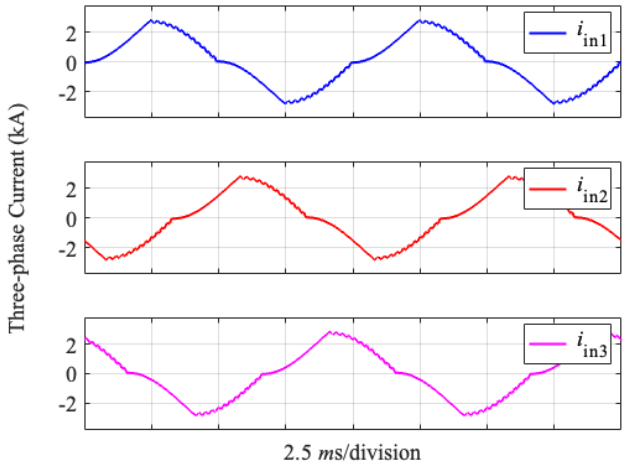


Figure 4.9: Input currents of the circuit simulated in three phases with X_L = 0.75 p.u. and X_C = 0 p.u. for each phase.

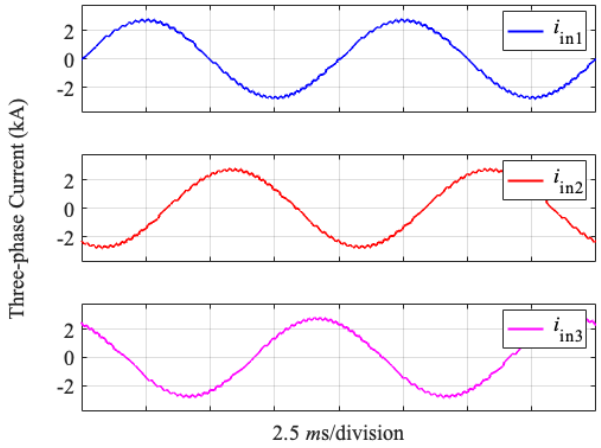


Figure 4.10: Input currents of the circuit simulated in three phases with X_L = 0.75 p.u. and X_C = 0.75 p.u. for each phase.

Another feature of the three-phase system to investigate is the output voltage and the sizing of the dc link capacitors. ±10% voltage ripple was chosen as a baseline to compare single-phase and three-phase systems; however, for a practical system this would be quite high; for example, in [14], the goal for output ripple is 0.2%. For a single phase, to achieve this maximum of ±10% voltage ripple, the value of C_{out} is 4.5 mF.

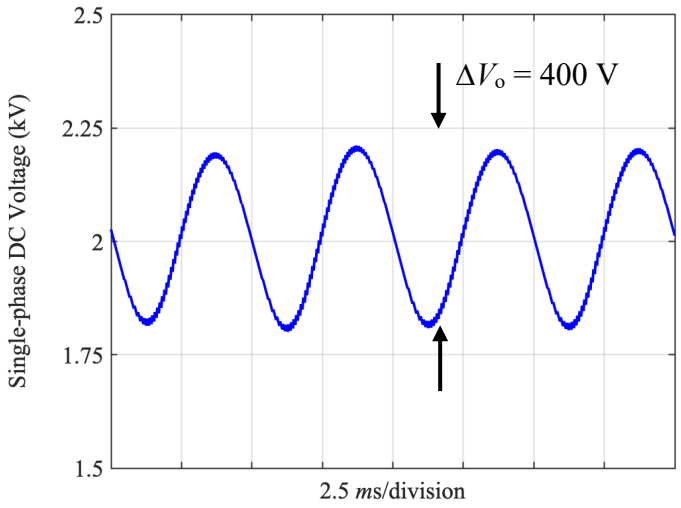


Figure 4.11: Output voltage of the single-phase circuit with C_{out} = 4.5 mF. 200 V is 10% of 2 kV, and ΔV_o = 400 V, or $\pm$10%.

However, with the outputs of three phases in series, the output ripples are cancelled out by each other, leading to a much smaller ripple on the overall output voltage. Figures 4.12 and 4.13 demonstrate this phenomenon, show that $< \pm 10\%$ on the 6 kV bus can be achieved with a C_{out} value that is smaller by a factor of 9, while the individual phases may have ripples of $> \pm 75\%$. This is an important design point as the sizing of dc link capacitors is often one of the prohibitive elements in making a design less heavy and more power dense.

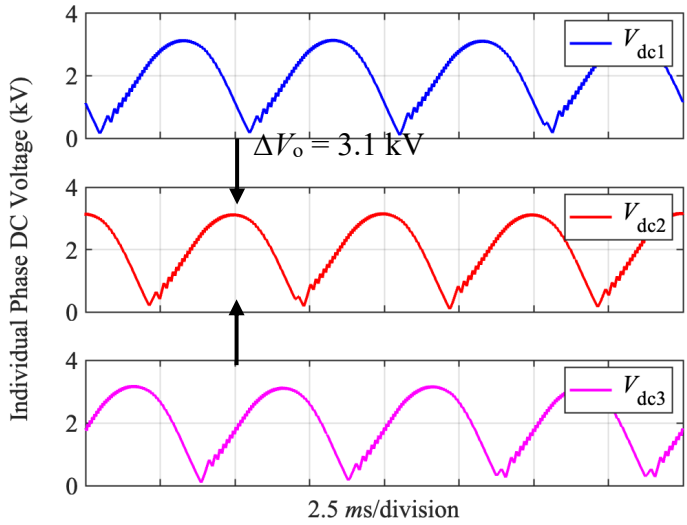


Figure 4.12: Output voltage of each phase of the three-phase circuit with C_{out} = 0.5 mF.

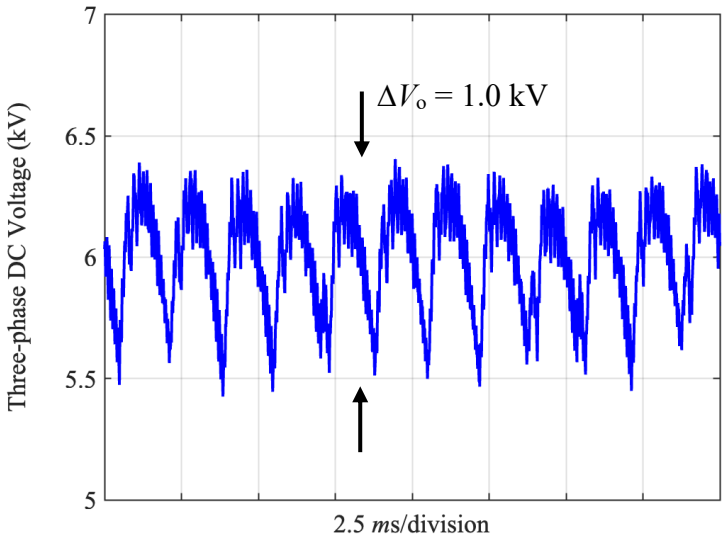
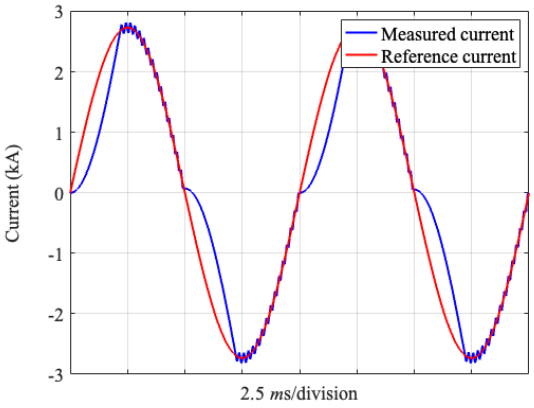


Figure 4.13: Voltage ripple on the three-phase dc bus C_{out} = 0.5 mF.

4.5 Voltage Ratio Comparison

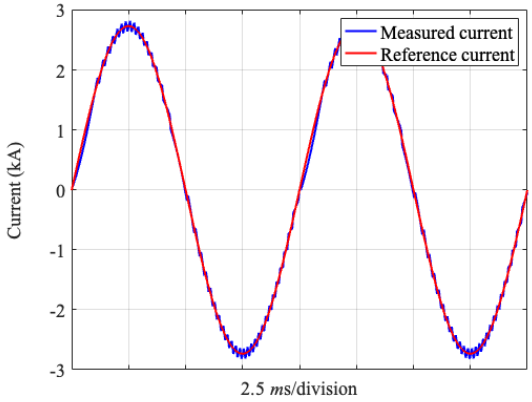
The main advantage of the capacitor compensation technique is the lower voltage ratio that can be used in design. Figure 4.14 shows a comparison of input current with X_L = 0.75 p.u. for three different voltage ratios and both zero and perfect compensation. The first set of results (Figure 4.14a and b) uses the same values as previously in this chapter, V_o = 2 kV, and V_{in} = 690 V. The next set of results (Figure 4.14c and d) increase the input voltage to 1 kV. The final pair (4.14e and f) shows the results of V_{in} = 1.4 kV, which is chosen as the largest value before the instantaneous value of input voltage could be larger than the output voltage.

These results show how as the voltage ratio decreases, i.e., the voltages become closer in value to each other, the input current eventually completely loses its "grip" on the reference. However, in each instance, the capacitor compensation allows the current to become sinusoidal and in phase with the voltage once again.



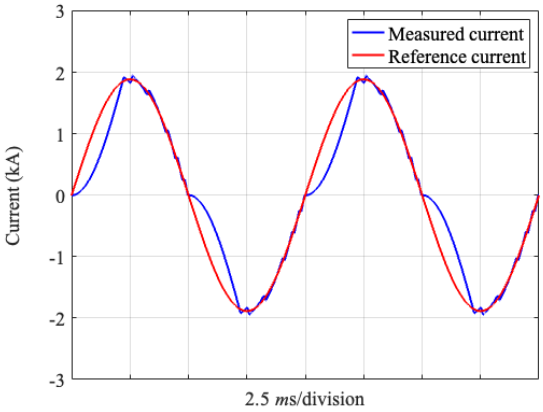
v_{in} = 690 V, X_L = 0.75 p.u., X_C = 0 p.u.

(a)



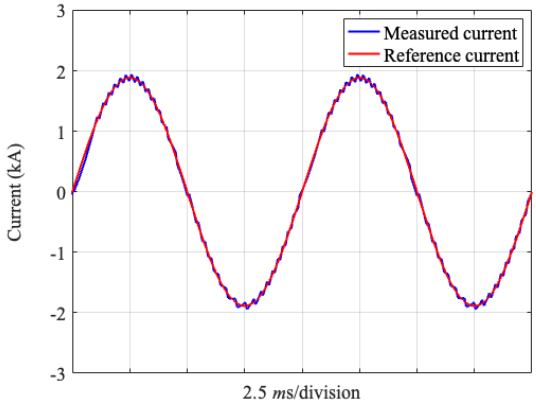
v_{in} = 690 V, X_L = 0.75 p.u., X_C = 0.75 p.u.

(b)



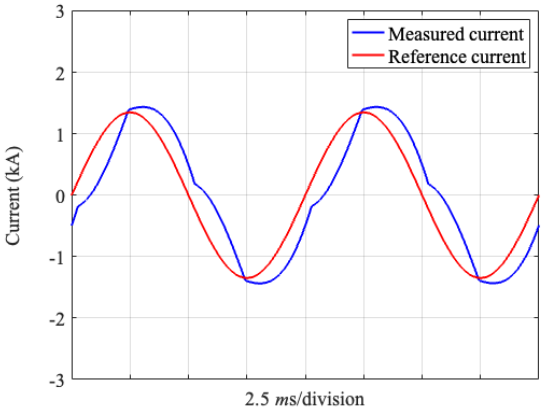
v_{in} = 1000 V, X_L = 0.75 p.u., X_C = 0 p.u.

(c)



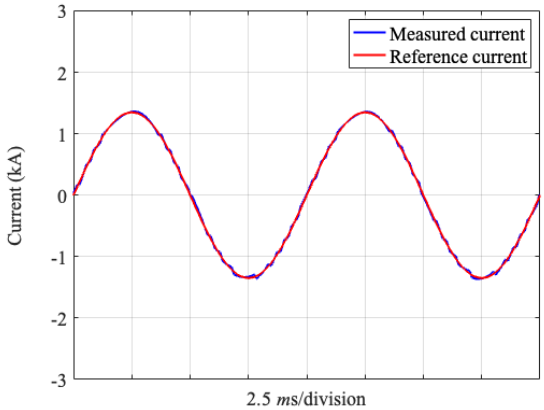
v_{in} = 1000 V, X_L = 0.75 p.u., X_C = 0.75 p.u.

(d)



v_{in} = 1400 V, X_L = 0.75 p.u., X_C = 0 p.u.

(e)



v_{in} = 1400 V, X_L = 0.75 p.u., X_C = 0.75 p.u.

(f)

Figure 4.14: Input current and its reference for three different input voltage levels and either no capacitor compensation or perfect compensation.

4.6 Summary

The high per unit impedance of ac generators tends to add a layer of design difficulty to engineers designing shipboard power systems. To keep THD within acceptable limits, high voltage ratios are often needed, and some topologies are avoided because of the current distortion caused. The application of series capacitor compensation was therefore proposed and its effects in an ac-dc boost converter were investigated in Chapter 3. Design equations for current, PF, and THD were derived to enable designers to properly size components and choose compensation parameters for the operating point of the system. In order to validate these equations, a single-phase simulation was created, and results were compared in this chapter. The results show a good match between the theoretical model and the simulation, which means that these equations are viable to be used to predict the behaviour of the circuit. The model was expanded to three phases, to verify the practicality of the circuit for ac generators. Three levels of voltage ratios were compared in terms of the effectiveness of compensation, and it was seen that even at very low ratios, the capacitor compensation allowed for expected current flow.

CHAPTER 5: EXPERIMENTAL VALIDATION

Chapter 4 presented the simulation results for the proposed circuit to verify the theoretical analysis provide in Chapter 3. Chapter 5 will present the experimental circuit and results that validate the practicality of the theoretical model and operation of the circuit. First, the prototype requirements were defined and refined. Schematics for the semiconductor subcircuit are developed in Altium, and a PCB design is created. Other components are sourced from lab resources or procured online, and the power board and circuit are manually soldered and assembled. The prototype is controlled using a TI C2000 micro controller, which is programmed using C code in Code Composer Studio. A single-phase 1 kW prototype is created, and results collected. The values of total harmonic distortion (THD) are compared between the simulated and experimental waveforms.

5.1 Experimental Design

To perform the experiments needed to validate the compensation technique, it was necessary to build a single-phase ac-dc boost converter. Given this general system description, the basic system requirements were produced, and a block diagram of the generalized system was drawn. From this, the detailed system requirements became clear, and parts were selected.

5.1.1 Basic System Requirements

Based on the general system description given above, the basic system requirements can be inferred. To test the compensation method, an ac voltage source with controllable inductive impedance was required, as well as several values of capacitor capable of handling the ac current. The ac voltage must be rectified, which, along with the boost stage, required power semiconductors. The input current was to be controlled using measurements of the input voltage and current, which meant that a processor, analogue sensing circuitry, and digital-to-analog and analog-to-digital converters (DAC and ADC) were all necessary. The ac frequency of 50 Hz suggests a relatively low frequency needed

for control, in the 10s of kHz. Since it was impractical to build a prototype at the power level used in commercial ships, 1 kW was chosen as an acceptable design requirement.

5.1.2 Experimental System Requirements

Following the basic system requirements outlined above, the detail requirements of each part of the system can be defined as follows:

5.1.2.1 Processor

For the processor, the storage and speed requirements are quite minimal, so the highest priority was ease of programming and how quickly it could go from box to being useful. Other requirements were that it needed to be programmable from a PC and either contain or communicate with analogue data converters.

5.1.2.2 Data converters

The data converters must have a high enough number of bits and sample rate for acceptable signal to noise (SNR) ratio and to avoid aliasing. Single-ended, 12-bit channels were sufficient for the need here.

5.1.2.3 Current and voltage sensing

These sensors and their circuits must measure ac voltage and current and provide biased signals for ADC with a high-impedance input buffer and anti-aliasing filter. To use a comparable hysteresis band to the simulations done in Chapter 4, the sensors should provide an accuracy of ± 0.3 A and 1V. High immunity to external interference is a plus because of noisy lab environment.

5.1.2.4 Ac supply

The ac supply must provide controlled voltage as well as safety for users and protection from transients.

5.1.2.5 Ac impedance

The ac impedance must be modular or have easily controlled levels of capacitance and inductance. These components must be rated for 10s of Amps at 50 Hz and be in the millifarad and millihenry range.

5.1.2.6 Rectifier and boost stage

The semiconductors of this prototype must provide full bridge rectification, as well as one active switch and one diode for the boost stage. High voltage ratings and excellent reverse recovery are necessary for a robust prototype.

5.1.3 Components Selection

Table 5.1 shows the important components and their specifications. To control the input voltage, a variable ac power supply, or variac transformer, was used. To mimic the effects of the large impedance of an ac generator, large inductors are used, listed here as interfacing inductance L_{ac}. For the compensating capacitors, polypropylene film capacitors designed for use in motors were chosen, because they provided the highest level of capacitance while handling the voltage and current needed for the series placement. To reach the values of interfacing inductance and compensating capacitance needed, several of the components listed are used in series and parallel respectively.

For the power semiconductors, a 1200V IGBT and a 1200V Silicon Carbide (SiC) diode were chosen for the active switch and boost diode respectively. The IGBT uses trench technology to lower conduction losses and contains an ultrafast soft recovery diode for low switching losses. The diode was chosen as a 1.2 kV SiC Schottky Diode.

In terms of control and sensing circuitry, the processor was the most important selection. It was determined that a microcontroller would provide the functions necessary, with no need for the excess processing power of an FPGA or other processor. Additionally, the ease of programming using C/C++ rather than using Verilog/VHDL was a plus. For plug-and-play functionality, a launchpad kit made by TI where a microcontroller comes already placed on a board with header connectors and a computer interface was selected. The analogue subsystem of the microcontroller had data converters built in, which sidestepped the need to design those analogue circuits separately. However, the current and voltage sensor circuits had to be configured for the chosen control system. To provide the accuracy and noise-immunity necessary, Hall effect transducers were used in conjunction with amplifiers to buffer and bias the signal that would be sent to the ADCs.

TABLE 5.1: EXPERIMENTAL COMPONENTS

Component	Part number	Specifications
Interface inductor	ARW U37459	12.5 mH, 30 A (AC/DC)
Compensating capacitors	Ducati Energia 4.16.10 series	25 – 50 uF, 450 V
Diode Bridge	VS-GBPC2512A	1200 V, 25 A
IGBT	IRG7PH35UD-EP	1200 V, 25 A (T 100˚C)
Boost diode	C4D15120D	1200 V, 24 A (T 135˚C)
Microcontroller	Microcontroller: TMS320F28379D LaunchPad: LAUNCHXL-F28379D	Two 32-bit CPUs, 200MHz
Current sensor	LA 55-P Current Transducer	50 A, ±0.3 A error
Voltage sensor	LV 25-P Voltage Transducer	500 V, ±0.765 V error
Output Capacitor	ALS30A332NP450	3300 uF, 450 V, 16 A

5.1.4 System Block Diagram

Figure 5.1 shows a block diagram of the experimental system.

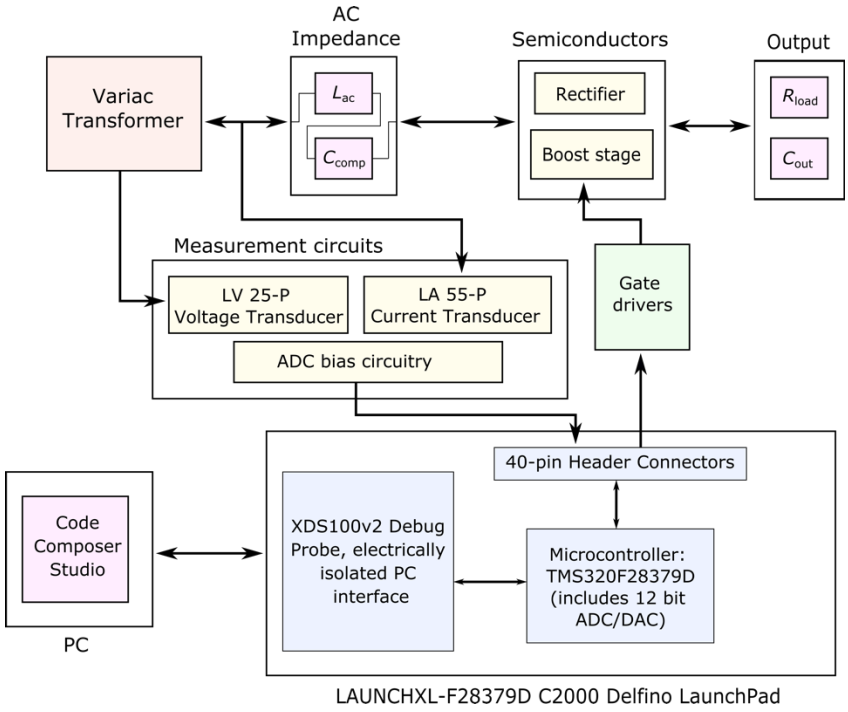


Figure 5.1. Block diagram of experimental prototype system.

5.1.5 Laboratory Set Up

Figures 5.2 through 5.4 show details of the experimental circuit. Figure 5.1 shows the set up downstream of L_{ac} and C_{comp}, beginning with the input voltage and current measurement boards. Those circuits send voltages to the ADCs on the microcontroller, where they are converted to digital signals and used to determine the switching signal sent to the gate driver. The signal processing was coded in C using Code Composer Studio to provide an open-loop hysteretic control. The bridge rectifier is contained in a single module, mounted on a heatsink. The rectified voltage is fed to the boost stage, where the gate driver sends signals to the IGBT to turn on and off to control the flow of power to the output capacitor and resistive load.

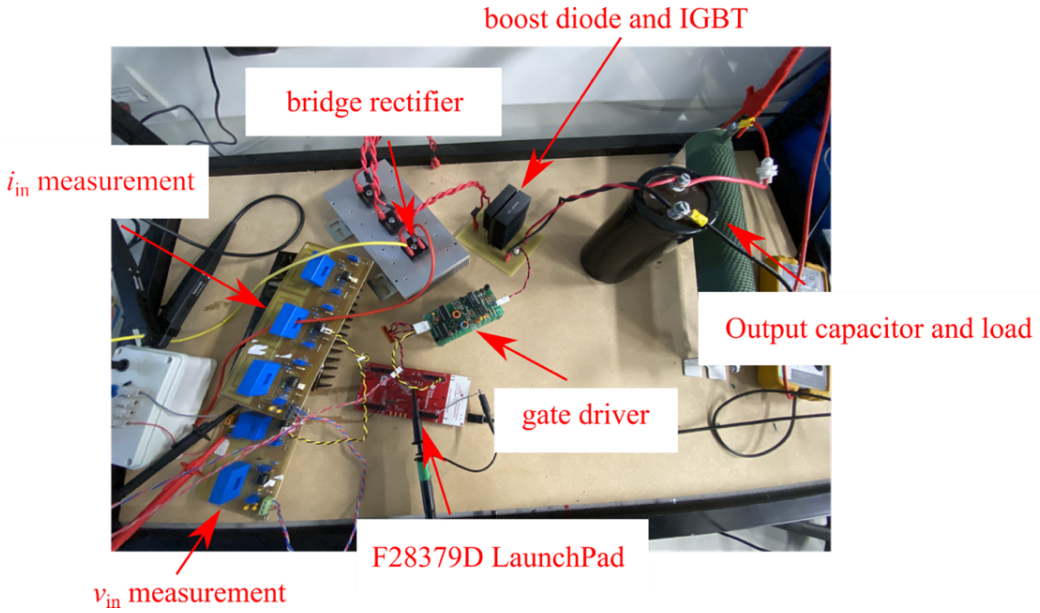


Figure 5.2. Experimental circuit used to collect single phase results.

Figure 5.3 shows one inductor that was used as the ac impedance in the experimental circuit. By using several in series and combining either the 5 or 10 mH tapped inductor value, the various levels of inductance were reached. Figure 5.4 shows the bank of capacitors used in parallel to reach equivalent per unit values to the inductance. Values of 50, 40, 30, and 25 µF were all used to reach the various levels needed.

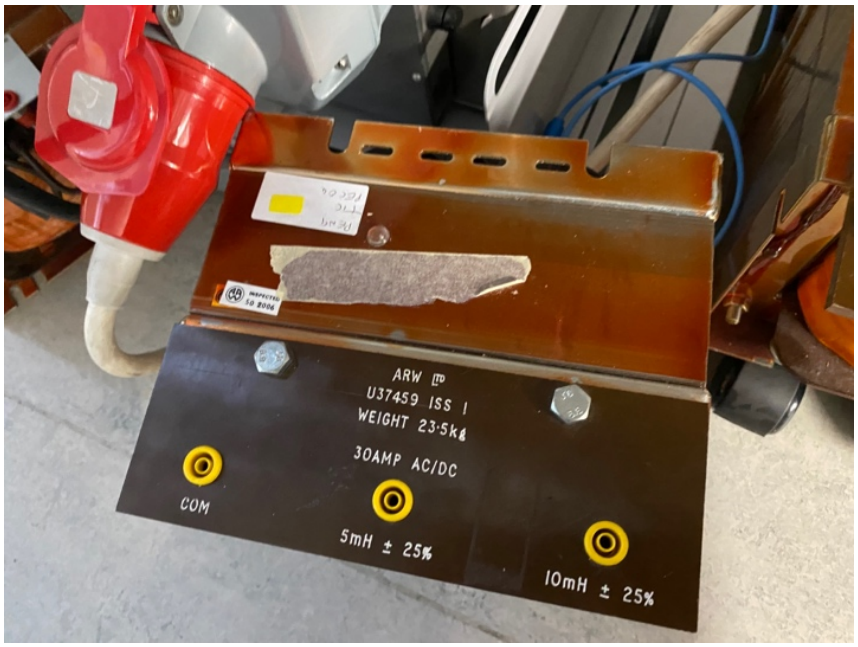


Figure 5.3. Inductor used as L_{ac} in experimental circuit.

Figure 5.4. Capacitor bank used as C_{comp} in experimental circuit.

5.2 Experimental Results

The following results were collected using the parameters specified in Table 5.2. These values were chosen based on the baseline ratings of certain components (e.g., the variac), as well as the ratio of input voltage to current. This ratio affects the severity of the detuning effect, and so RMS values of 85 V and 6.2 A were selected in order to provide comparable results to the simulation results in the previous chapter.

TABLE 5.2: EXPERIMENTAL PARAMETERS

Parameter	Value
Number of phases	1
DC Voltage V_{dc}	230 V
Input Voltage V_{in}	85 V
Input Current I_{in}	6.2 A
Frequency f_{ac}	50 Hz
Input power P	527 W
Interfacing inductance L_{ac}	X_L = 0.25, 0.75 p.u.*
Compensating Capacitor C_{comp}	X_C = 0, 0.75 p.u.*
Output Capacitor C_{out}	3300 μF
Load Resistance R_{out}	100 Ω

*Results with further values in Appendix B.

Results are presented as frames taken from the oscilloscope with ac voltage on top (orange), ac current in the middle (blue), and dc output voltage on the bottom (green). Per unit values of 0 and 0.75 for compensating capacitor and 0.25 and 0.75 for the interfacing inductance were used. THD values are shown for the input current in each subfigure. These values were calculated by capturing the input current waveform via PicoScope as a csv file, and then using MATLAB to calculate the THD across ten cycles of the waveform.

With no compensating capacitor, the THD can be seen to increase from very low to around 15% with the increase of inductive reactance from 0.25 to 0.75 pu (Figure 5.5 a and b). However, with the compensating capacitor, the waveform shows overcompensation

(Figure 5.5c) and perfect compensation (Figure 5.5d). Here, the THD is greater on the left, showing the characteristic pre-zero-crossing distortion. The final scope image on the bottom right shows the practical result of equal per unit values of inductance and capacitance.

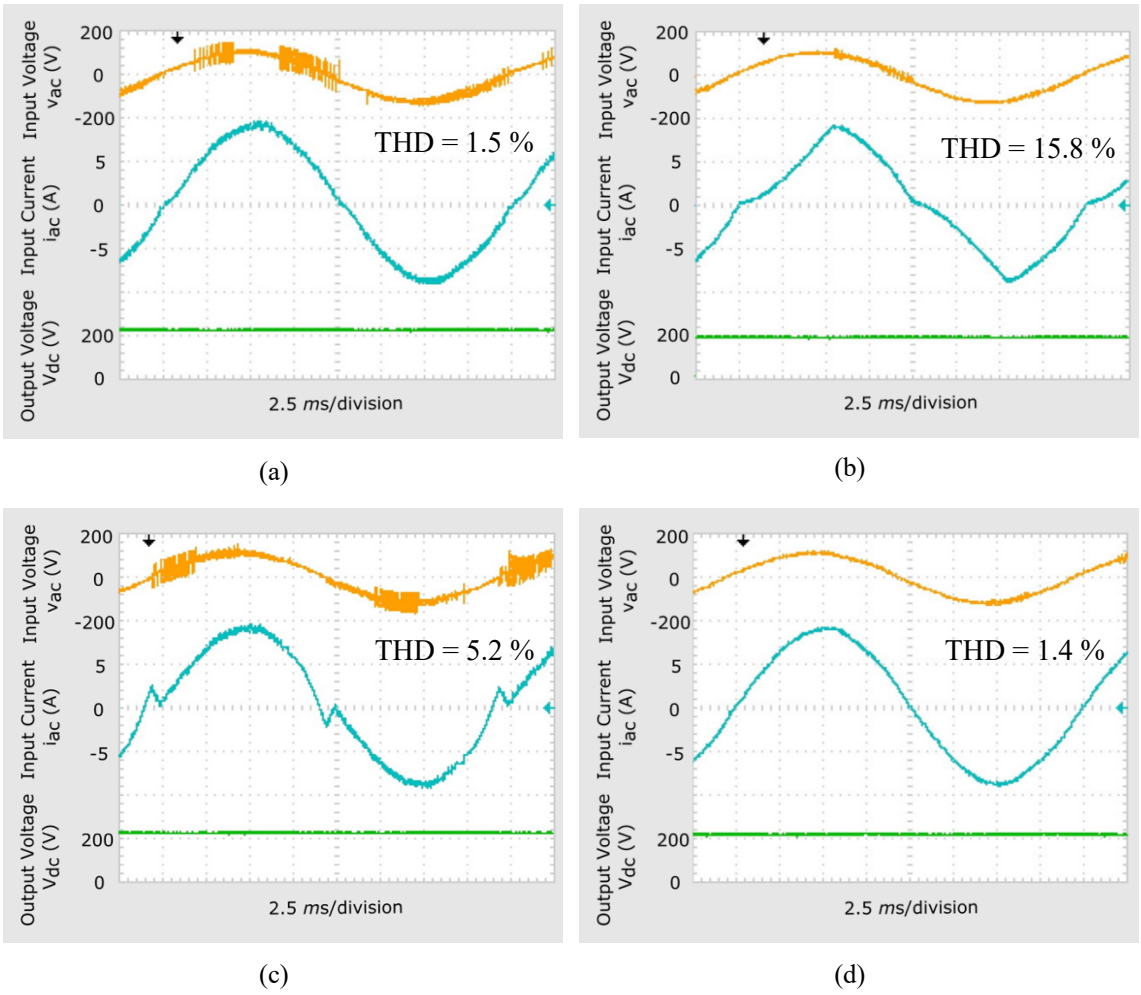


Figure 5.5. Experimental results with different values of inductance and compensating capacitor. Orange shows input voltage, blue is input current, and green is output voltage. a) X_L = 0.25 p.u., X_C = 0 p.u., b) X_L = 0.75 p.u., X_C = 0 p.u., c) X_L = 0.25 p.u., X_C = 0.75 p.u., d) X_L = 0.75 p.u., X_C = 0.75 p.u.

5.3 Analysis and Discussion of Experimental Results

In Figure 5.6, the input current waveform data gathered with the PicoScope was plotted in red alongside the simulation results in blue. By comparing these waveforms, a close match is seen between the angles of detuning and the predicted shape of current while the switch

remains on after the zero crossing. There are minor discrepancies; for example, in Figure 5.6a, the slope of the current during the detuning event is shallower in the experimental results than in the simulation. This could be due to small discrepancies in the impedance used in the experimental set up, for instance the amount of resistance provided by the inductors and cables used verses the resistance used in the simulation.

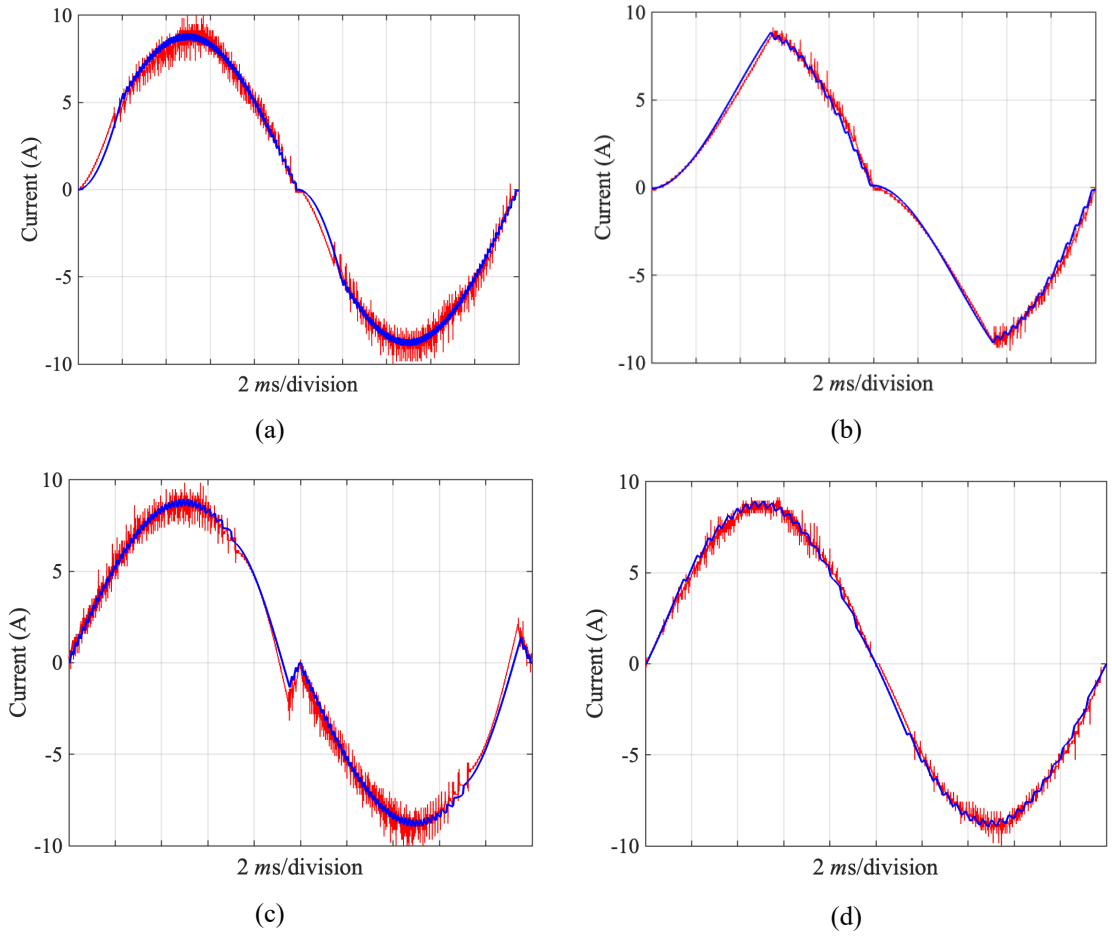


Figure 5.6. Comparison of experimental results and simulated ac current. Blue is simulated ac current, and red is collected experimental ac current. a) X_L = 0.25 p.u., X_C = 0 p.u., b) X_L = 0.75 p.u., X_C = 0 p.u., c) X_L = 0.25 p.u., X_C = 0.75 p.u., d) X_L = 0.75 p.u., X_C = 0.75 p.u.

Figure 5.7 maps out the THD values of experimental and simulated input current for values of X_L = 0.25, 0.5, 0.75, and 1 pu and X_C = 0 and 0.75 pu. Simulated values are shown in blue while experimental are in red. This graph clearly shows that without compensation, the THD levels quickly rise out of an acceptable range as the inductive impedance rises towards 1 pu. However, with a value of 0.75 capacitance, the THD in all cases is kept below 8%. This suggests that with one static capacitor value, chosen based on the expected

impedance of a generator, the THD of the input current can be held within a reasonable range. Furthermore, small deviations from the expected impedance due to manufacturing or small dynamic changes in load will not force the THD out of range.

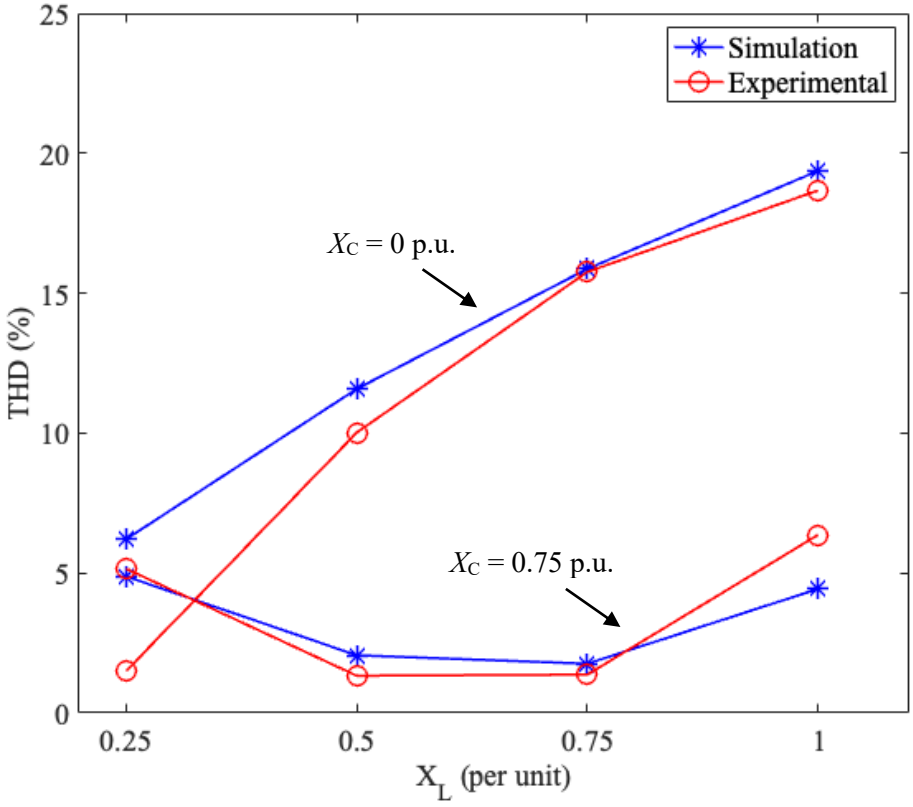


Figure 5.7. Comparison of input current THD in simulated (blue) and experimental (red) results. The upper two lines represents values collected with no compensating capacitor, the lower were collected with X_C = 0.75 p.u.

This comparison between the simulations and experimental results shows a close match between the values of THD for given per unit values of inductor and capacitor. There is one point that appears to be a true outlier in this pattern: the experimental value where X_L = 0.25 and X_C = 0 pu, which is 1.5% while its corresponding simulated value is 6.2%. This case can be seen in the waveform presented in Figure 5.6a. Looking closely, the simulated current falls below the experimental, or further away from the original sine wave; in other words; there is a higher harmonic content in the simulated waveform, corresponding to the higher THD calculated by MATLAB. This difference between the experimental and simulated current most likely comes from some unaccounted-for resistance and

capacitance present in the practical circuit but not the simulation. The simulations did include estimated resistances based on measurements taken of the inductors and capacitors in the lab. For other cases, the level of capacitance and inductance is high enough that the stray impedance has less of an impact on the results.

5.4 Summary

A 1 kW single-phase prototype was built in the lab to verify the practical application of the circuit discussed in Chapter 3 and simulated in Chapter 4. The circuit was designed based on the general system description and subsequent part requirements. The primary objective was to be able to test the compensation theory, and therefore modular parts were used to stand in for the inductance of an ac generator, and motor drive capacitors were used to as the ac compensating capacitors. Once the experimental prototype was ready, the input current waveforms were recorded for different cases of ac impedance and the THD values calculated. The analysis shows that with no compensation, the values of THD are not within acceptable limits for the higher values of inductance, which are likely to be found in practical generators. However, with a compensating capacitor of 0.75 p.u., the THD was below 8% for all values of inductance, suggesting that the compensation technique could be practical even given slight variations in manufacturing and hence inductance.

6 CONCLUSION

5.1 General conclusions

The research presented in this thesis focussed on the design and analysis of a series-capacitor-compensated ac-dc boost converter for SPS. Firstly, the background of SPS and their design was presented. A known issue in SPS design is the high inductive impedance presented by ac generators by virtue of their architecture. This high impedance forces engineers to design systems with high voltage ratios, which in turn affects all downstream components.

A series capacitor compensation method for the ac generator impedance was proposed and applied to an ac-dc boost rectifier circuit. The circuit operation was studied, and equations for current, PF, and THD were derived for the under and overcompensated cases. The circuit was then simulated using MATLAB/Simulink, and the mathematical model was shown to predict the simulated THD values to within 2.5%. The circuit was then simulated in three phases and with the outputs connected in series, a factor of 9 reduction in per phase capacitance was achieved. A comparison between different input to output voltage ratios was performed, and it was shown that as the input voltage was raised, uncompensated current worsened in terms of THD, while compensated current stayed below 5%. An experimental circuit was built to test the practical application of the compensation technique in this topology. When compared to simulations, the majority of practical THD results fell within 1% of predicted values, showing that the mathematical model and simulations were able to predict the behaviour of the practical circuit.

In conclusion, the series capacitor compensation was proven to work as theorized for this circuit, and the work done here could be expanded to other topologies as well. The range of varying inductive impedance with acceptable THD for a given compensating value was found to be quite large: a compensation value of 0.75 p.u. reduced THD to below 8% for ac impedance values from 0.25 to 1 p.u. This suggests that the value of a compensating capacitor need not be too exact; manufacturer's variation in the capacitors or generator, as well as some load transients, may not render the use of a static compensation component

useless. Overall, this is a promising solution to the issue of ac generators' high inductive impedance in SPS design.

6.1 Future research

Further research should include the development of a closed-loop control method and a system stability analysis to investigate the reaction of the system to load transients, because environmental factors like waves and certain SPS loads can affect the power required at short notice. Voltage mismatch and phase balancing might be addressed by this new control method as well. The experimental circuit could be expanded to three phases, which would reflect the practical application more closely. Additionally, the use of an ac generator, instead of static components as approximations, would enhance the reality of the practical circuit. This could also be achieved by investigating a range of power factors and the addition of realistic resistance into the models and practical circuit. With more time and resources, the compensation method could be tested on an SPS testbed at realistic voltage and power levels, and the practicality of the actual components themselves could be compared, as size and weight are extremely important in SPS design.

Another way this research could be expanded upon would be to apply the same compensation method to other circuits. For example, the boost stage could be paralleled to allow for more current margin in the power semiconductors. Or a different topology could be used altogether. The effect the compensation would have on a thyristor rectifier or MMC converter would be interesting to investigate further, as these are topologies used in contemporary SPS research and design.

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Appendices

Appendix A: Full Simulation Results

AC Current Waveforms

Parameters: v_{in} = 690 V, P_{in} = 1 MW

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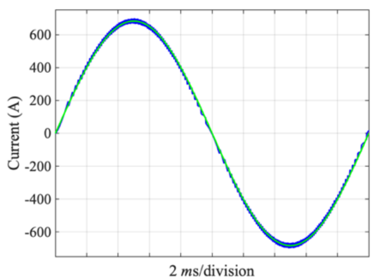
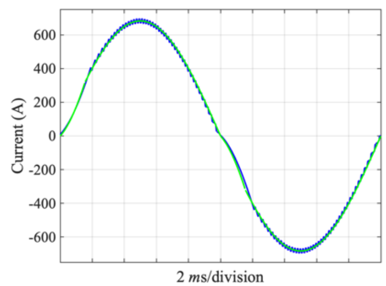
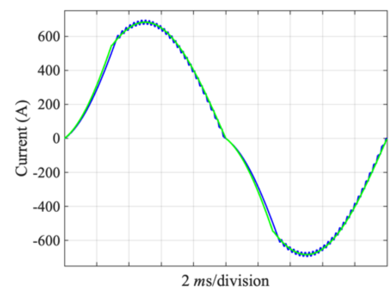
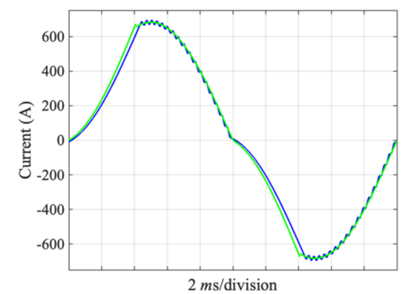
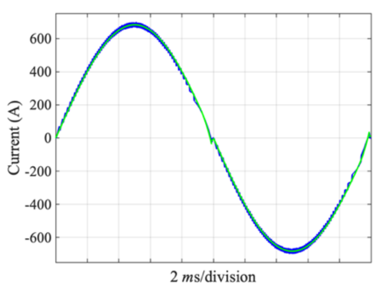
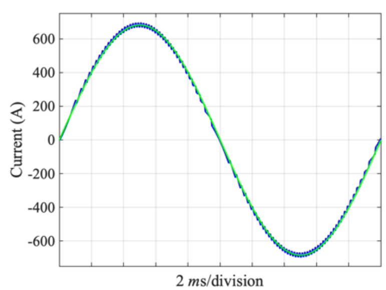
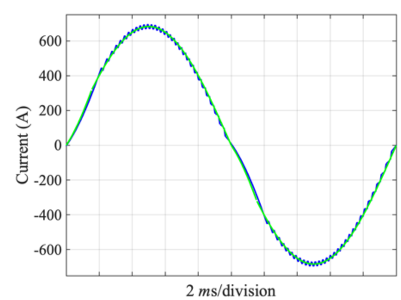
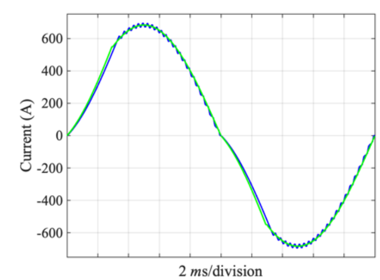
X_C = 0.25 pu				
X_C = 0.5 pu				

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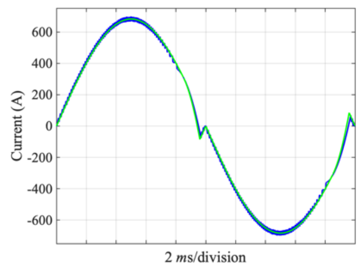
<td> 
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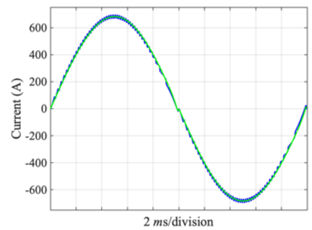
<td> 
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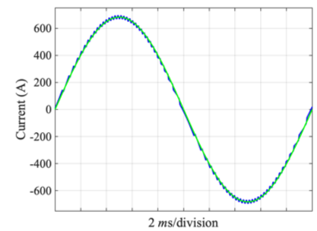
<td> 
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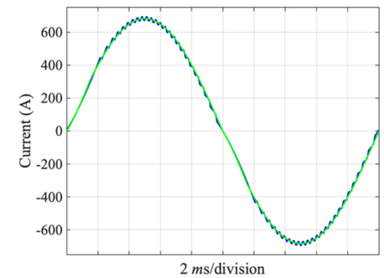
<td> 
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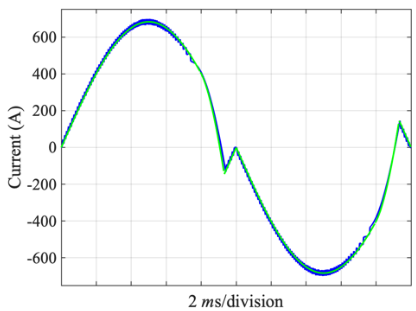
<td> 
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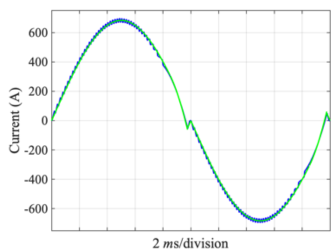
<td> 
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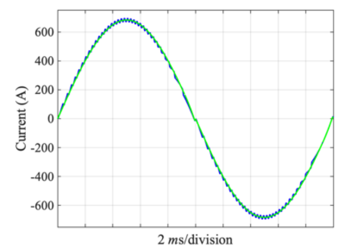
<td> 
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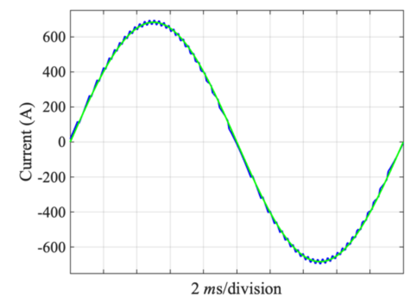
<td> 
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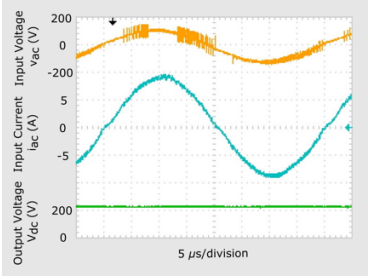
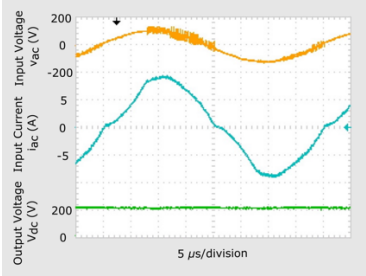
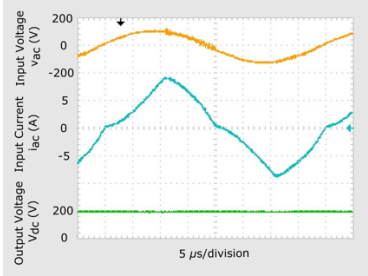
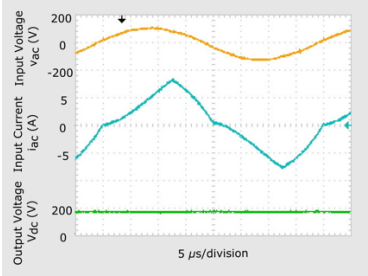
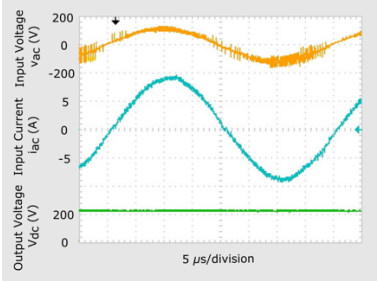
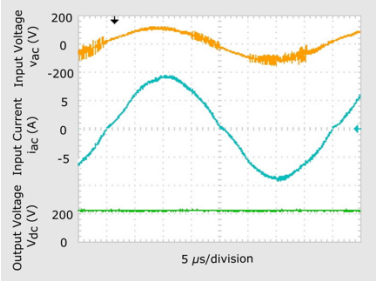
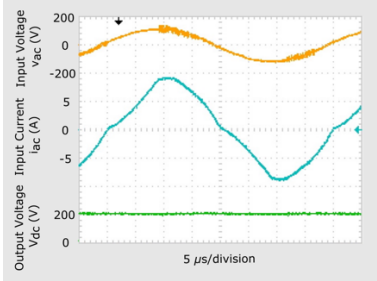
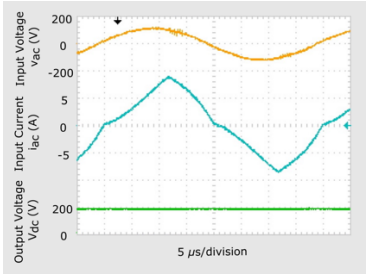
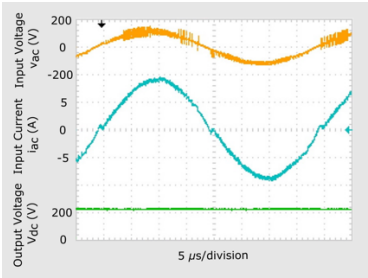
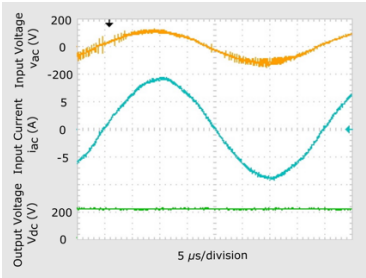
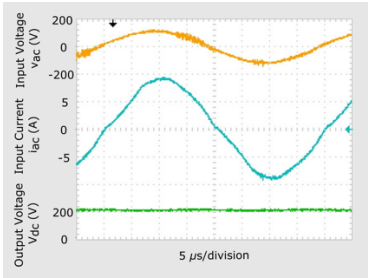
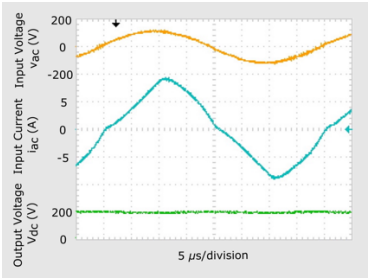
Appendix B: Full Hardware Results

Orange: input voltage, blue: input current, green: output voltage

Parameters: v_{in} = 85 V, P_{in} = 530 W

	X_L = 0.25 p.u.	X_L = 0.5 p.u.	X_L = 0.75 p.u.	X_L = 1 p.u.
X_C = 0 p.u.				
X_C = 0.25 p.u.				
X_C = 0.5 p.u.				

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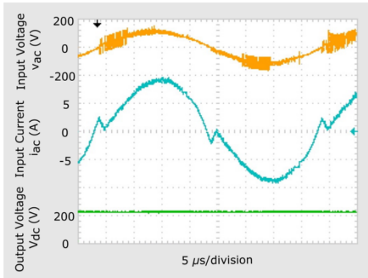
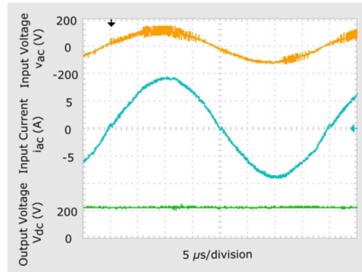
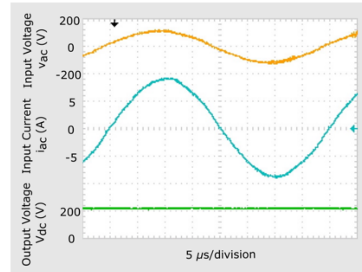
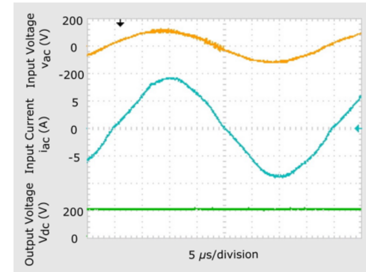
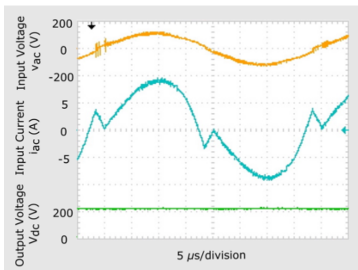
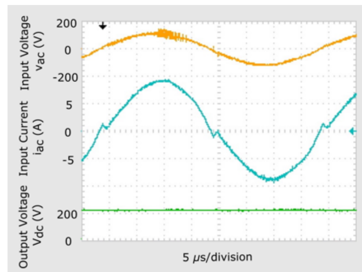
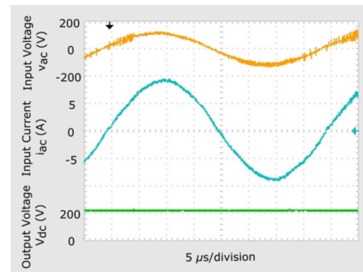
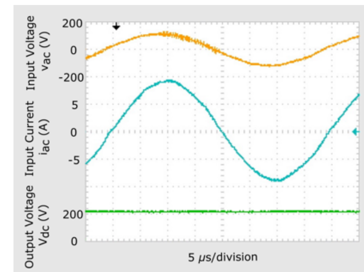
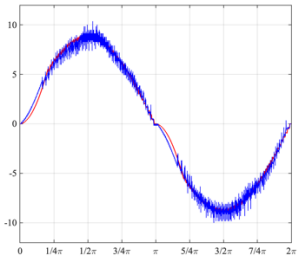
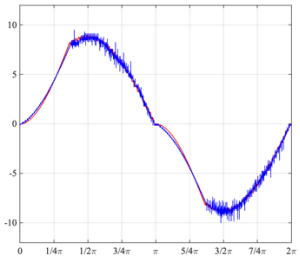
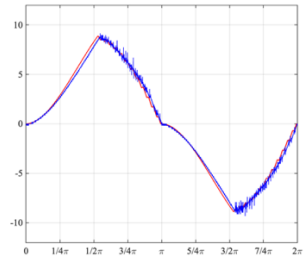
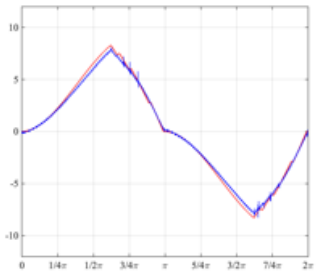
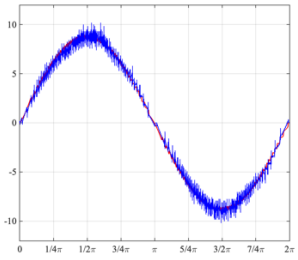
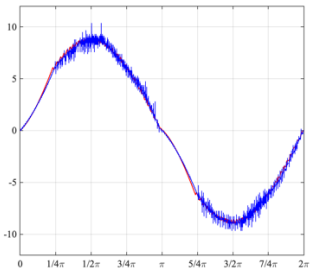
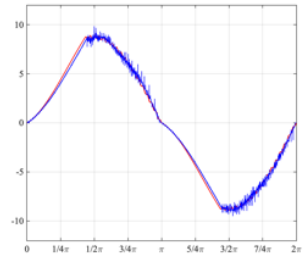
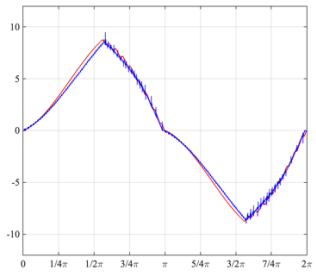
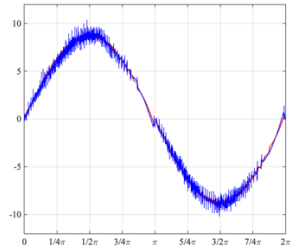
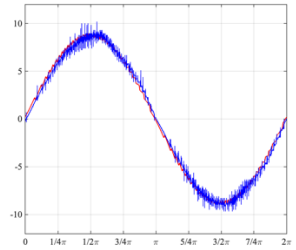
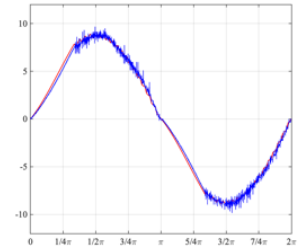
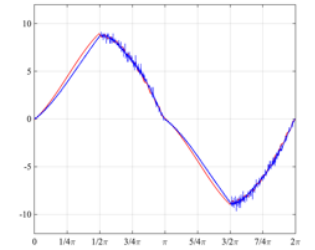
X_C = 0.75 p.u.				
X_C = 1 p.u.				

	X_L = 0.25 p.u.	X_L = 0.5 p.u.	X_L = 0.75 p.u.	X_L = 1 p.u.
X_C = 0 p.u.				
X_C = 0.25 p.u.				
X_C = 0.5 p.u.				
	X_L = 0.25 p.u.	X_L = 0.5 p.u.	X_L = 0.75 p.u.	X_L = 1 p.u.

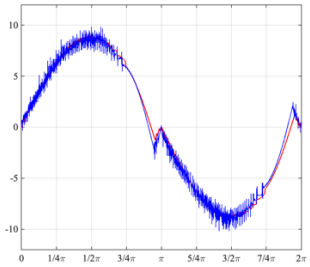
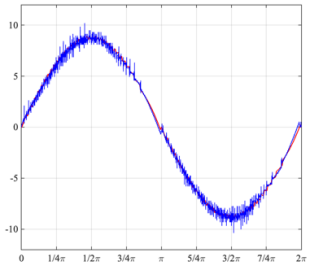
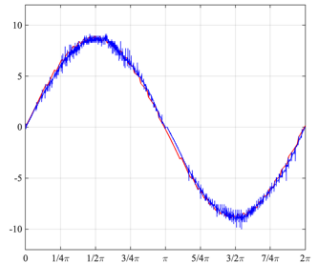
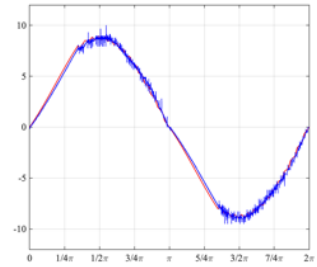
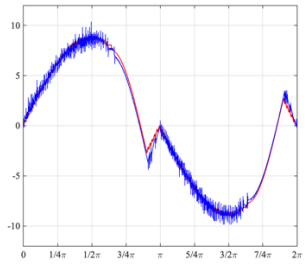
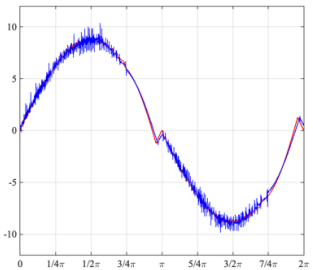
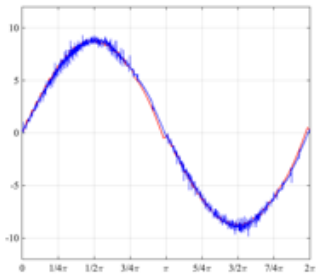
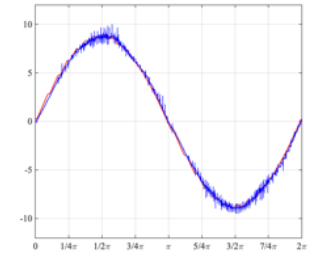
X_C = 0.75 p.u.				
X_C = 1 p.u.				

Figure ii-2. Full experimental results with different values of inductance and compensating capacitor. Blue is experimental current, and red is simulated current.