Vacuum Growth of N-octylphosphonic Acid Monolayer for Low-Voltage Organic Thin-Film Transistors

By

SWATI GUPTA

Submitted in fulfilment of the requirements for the
Degree of Doctor of Philosophy

Department of Electronic and Electrical Engineering
University of Strathclyde

Author's declaration

I declare that all the work presented in this thesis has been carried out by me, unless otherwise acknowledged.

Swati

SWATI GUPTA

February 2014

Dedicated to my supervisor,
loving parents,
and
husband
who have strongly believed in me ...

Acknowledgements

First of all, I would like to convey my sincere gratitude to my PhD supervisor, Dr. Helena Gleskova. Her guidance and support during my entire PhD studies were immense. Over the past three years she has always encouraged me to get involved in various activities. She also has the best possible research equipment in the laboratory. I am lucky to have her as my PhD supervisor.

My parents have dreamt about me getting a good-quality higher education since my childhood. They gave up many comforts to make it possible for me and I now feel very happy to fulfil their wishes. I'm sure they will be very proud of my achievements. My husband, Prashant Saxena, deserves many thanks for being with me all the time and patiently listening to all my frustrations. I am extremely happy to have a wonderful supervisor, parents, and husband. The support from relatives: Neha, Saurabh, Rahul, and uncle Ashok are much appreciated. I would also like to mention the help of my friends Bhuvanesh, Niharika, Krishna, Naresh, Pallavi, and Bhoomi throughout my PhD.

Thanks to Prof. Rein Ulijn to offer me an opportunity to use the Atomic Force Microscope in his laboratory and Dr. Mischa Zelzer to train me on the instrument. Dr. Dimitrios Lamprou and Dr. Pavol Šutta conducted water contact angle and Fourier transform infrared spectroscopy measurements, respectively. Their contributions to the material characterization were very helpful in understanding several aspects of my research. Pentacene purification was performed in-house by Dr. Gleskova. The thickness measurements performed by Dr. Gordon Brown were helpful in the calibration of semiconductor deposition.

Several courses conducted by the researcher development programme of the University of Strathclyde helped me to improve my writing and presentation skills. Finally, I would like to thank my funding agencies – Scottish Funding Council and University of Strathclyde. Many thanks also go to Prof. Ivan Andonovic and Prof. Ivan Glesk for providing funds for conference attendance.

Certificate

This thesis is the result of the author's original research. It has been accomplished by the author and has not been previously submitted for examination which has led to the award of a degree.

Swati

Swati Gupta

Date: February 2014

Abstract

This thesis optimizes the vacuum, vapour-phase self-assembly of n-octyl phosphonic acid monolayer. This monolayer is chemisorbed to the aluminium oxide (AlO_x) and together they form an ultra-thin gate dielectric in organic thin-film transistors based on pentacene. The electrical measurements of the transistors and the corresponding metal-insulator-metal structures were combined with the characterization of n-octylphosphonic acid monolayers using the atomic force microscopy, water contact angle measurement and Fourier transform infrared spectroscopy. The results show that the properties of the organic monolayer depend on its evaporation rate, growth temperature and the post-growth annealing and affect the performance of the as-fabricated transistors as well as the transistor bias-induced instability.

Table of Contents

List of figures

List of Tables

List of symbols and acronyms

A	Area of the channel
AFM	Atomic force microscopy
AlO_x	Aluminium oxide
Al_2O_3	Aluminium oxide
C	Capacitance
C-TLM	Contact transmission line method
C_8PA	N-octylphosphonic acid
d	Dielectric thickness
E_{BD}	Electric breakdown field
E_f	Fermi energy
E_g	Energy gap
FET	Field-effect transistors
FTIR	Fourier-transform infrared spectroscopy
FWHM	Full width at half maximum
HOMO	Highest occupied molecular orbital
I_D	Drain current
I_G	Gate current
I_{on}	Transistor on-current
I_{off}	Transistor off-current
I_{on}/I_{off}	Transistor on-off current ratio
J	Current density
k	Boltzmann’s constant
L	Channel length
LUMO	Lowest unoccupied molecular orbital
MIM	Metal-insulator-metal
MOSFET	Metal-oxide-semiconductor field-effect transistor
OLED	Organic light-emitting diode
OSC	Organic solar cell
OTFT	Organic thin-film transistor
p	Hole density

PEN	Polyethylene naphthalate
PET	Polyethylene terephthalate
PI	Polyimide
q	Charge of electron
Q	Charge density
R_a	Average surface roughness
R_c	Contact resistance
R_{ch}	Channel resistance per unit channel length
R_q	Root-mean-square (RMS) surface roughness
R_T	Total resistance
S	Subthreshold slope
SAM	Self-assembled monolayer
SiO_2	Silicon dioxide
Si_3N_4	Silicon nitride
t	Thickness of the transistor channel
T	Absolute temperature
V_{DS}	Drain-to-source voltage
V_{GS}	Gate-to-source voltage
V_x	Voltage at the distance x from the source
V_{th}	Threshold voltage
W	Channel width
WCA	water contact angle
β	Stretching parameter
ε_o	Permittivity of vacuum
ε_r	Relative permittivity
μ	Field-effect mobility, hole mobility
σ	Electrical conductivity
τ	Time constant

Chapter 1

Introduction

1.1 Organic electronics

The organic electronic devices were first fabricated in 1980 and since then organic thin-film transistors (OTFTs), organic solar cells (OSCs), organic light-emitting diodes (OLEDs) and organic sensors have attracted commercial interest. When compared to conventional inorganic devices, their main advantages are low fabrication temperature, low-cost, and non-planar form factors. Consequently, organic devices can be fabricated on various plastic substrates such as polyimide (PI), polyethylene naphthalate (PEN), or polyethylene terephthalate (PET) [1] that provide the basis for mechanical flexibility. Thus foldable pressure sensors [1], flexible OLED displays [2], e-paper [3], or RFID tags [4] are possible.

(a) (b)

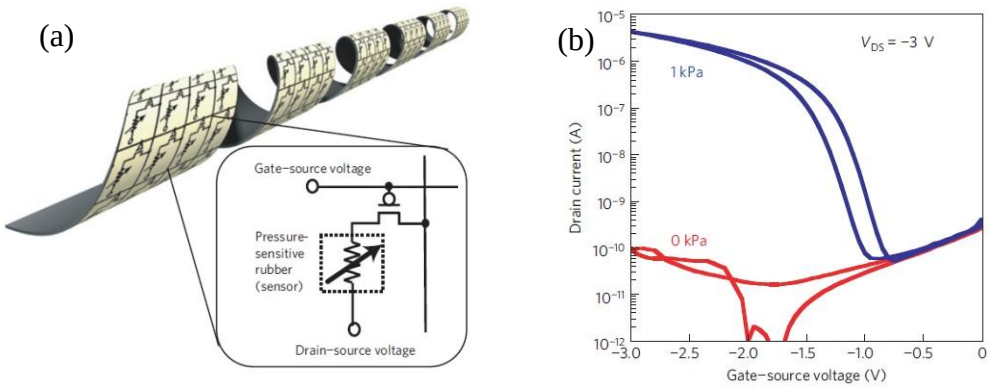

Figure 1.1: Circuit diagram of ultra-flexible active-matrix pressure-sensor array in the shape of tightly wound helix (a) and transfer characteristics of the pressure sensor at two different pressures (b) [1].

(a) (b)

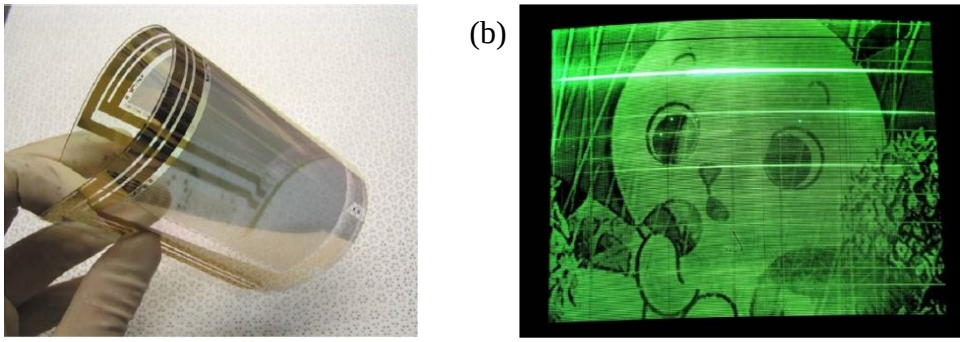

Figure 1.2: OTFT backplane (a) and a 5-inch active matrix OLED display (b) [2].

An array of organic pressure sensors with their pressure response is shown in Figure 1.1. Active-matrix OLED display with OTFT backplane is shown in Figure 1.2 and an array of actuators based on carbon nanotubes in Figure 1.3. The current research in organic electronics is very diverse and covers the development of new materials, devices, processes for large-area fabrication, large-scale device integration, device physics [5], and modelling.

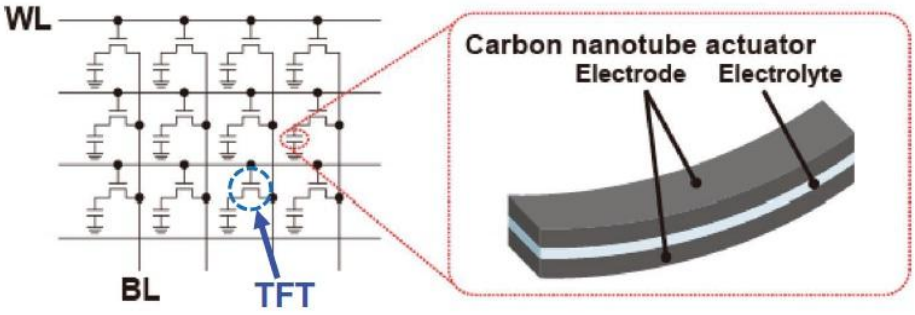

Figure 1.3: Active matrix array of actuators based on carbon nanotubes [6].

1.2 Motivation for research

Thin-film transistor is a fundamental component of electronic circuits such as inverters [7–10], logic gates and active-matrix display backplanes [2, 6]. Appropriate selection of the gate dielectric, semiconductor and transistor contacts leads to OTFTs that can operate within 2-3 volts [11–14]. Thus the implementation of OTFTs leads to low power consumption, while offering thin, rugged electronics with desirable mechanical properties.

OTFT fabrication typically includes wet or dry processing steps for the deposition of the dielectric and semiconductor layers [11–14], and vacuum evaporation of metal electrodes. However, a completely dry OTFT fabrication process is also possible, as will be shown in this thesis. In such a case all transistor layers – dielectric, semiconductor, and contacts are prepared by dry deposition techniques involving vacuum thermal evaporation and oxidation by ozone. Wet steps are omitted, which avoids the degradation of plastic substrates by solvents. Also, the maximum temperature applied during the fabrication process is 160°C and hence this process is transferrable to plastic substrates.

1.3 Thesis objectives

This thesis aims to optimize OTFTs performance based on pentacene and a bi-layer dielectric consisting of aluminium oxide (AlO_x), prepared by UV/ozone oxidation of aluminium, and a vacuum, vapour-phase self-assembled monolayer of n-octylphosphonic acid (C_8PA). AlO_x functionalized with such C_8PA monolayer forms an ultra-thin bi-layer dielectric that exhibits large capacitance, low leakage current density and high breakdown field. C_8PA self-assembly process consists of two steps. Firstly, a thickness corresponding to several C_8PA monolayers is thermally evaporated. Afterwards, the sample is heated without breaking vacuum to remove the physisorbed molecules.

This research aims to improve the process of C_8PA vacuum assembly and thus improve the properties of the AlO_x/C_8PA bi-layer dielectric and optimize the OTFT performance. Properties of C_8PA monolayers are examined by Fourier-transform infrared spectroscopy (FTIR), atomic force microscopy (AFM) and water contact angle (WCA) measurement and their correlation with transistor performance is sought. Finally, the link between the C_8PA structure and OTFT bias-stress instability is studied for the first time.

1.4 Thesis outline

Chapter 2 explains the operation and fabrication process of OTFTs. Chapter 3 describes the fabrication methods of metal-insulator-metal (MIM) and OTFT devices and samples for material characterization. The chapter also includes the basics of electrical, surface and structural measurements. Chapter 4 discusses the initial OTFT

optimization that involves optimization of pentacene and all transistor contacts while the C_8PA layer is not yet optimized. Chapter 5 demonstrates that the vacuum, vapour-phase self-assembly leads to chemisorption of C_8PA molecules to AlO_x. The effect of C_8PA growth temperature on the monolayer formation and OTFT properties is discussed in Chapter 6. Chapter 7 presents the optimization of pentacene growth temperature while the pentacene evaporation rate is kept constant. Chapter 8 summarizes the effect of C_8PA deposition rate on C_8PA self-assembly and transistor performance. OTFT bias-stress effect is discussed in Chapter 9. Chapter 10 concludes the thesis while summarizing the results and providing suggestions for future work.

1.5 Thesis contribution

This research represents a seminal contribution to the development of vacuum vapour-phase self-assembly of n-octylphosphonic acid monolayer on aluminium oxide prepared by UV/ozone oxidation. The AlO_x/C_8PA bi-layer dielectric has thickness of ~10 nm, leakage current density of 10^{-7} A/cm^2 at –3 V and breakdown field of 6 MV/cm.

A correlation between the C_8PA growth temperature (25–150°C), evaporation rate (0.3–10 Å/s), and post-deposition annealing at 160°C (25–210 minutes) and the surface and structural properties of the monolayer were understood. The metal-insulator-metal structures and pentacene organic thin-film transistors implementing such monolayers were investigated, including the bias-stress induced transistor instability. Experimental techniques such as Fourier Transform Infrared Spectroscopy, Water Contact Angle, Atomic Force Microscopy, and comprehensive

electrical measurements were employed. The effect of pentacene purity, deposition rate and growth temperature were also briefly studied.

The results show that the C_8PA monolayer exhibits the best surface and structural properties when it is grown at 25°C at a rate of ~3 Å/s and subsequently annealed at 160°C for 180–210 minutes. Such process parameters resulted in an improved performance of organic thin-film transistors based on pentacene, both on a short- and long-term time scale. Consequently, this research uncovered a clear correlation between the properties of the monolayer and the long-term electrical stability of the organic transistors.

Chapter 2

Organic thin-film transistor (OTFT)

This chapter introduces the organic thin-film transistors, their structure, operation, characterization, and a general approach to achieving their low-voltage operation. The metal-insulator-metal (MIM) structure, field-effect transistor, carrier transport in semiconductors, and operation of organic thin-film transistor is discussed in Sections 2.1 to 2.4, respectively. Additional information pertinent to OTFT performance and characterization is presented in Section 2.5. The state of the art of low-voltage OTFTs is included in Section 2.6. Section 2.7 summarizes the approach taken in this research to develop low-voltage organic thin-film transistors.

2.1 Metal-insulator-metal structure

A metal-insulator-metal structure (or a parallel-plate capacitor) consists of two parallel conducting layers and a dielectric inserted between them; the conductors

can be of the same or different metals. Dielectric material is polarized in the presence of the electric field, i.e. the neutral charge of each atom is distorted and the formed dipole moment is aligned with electric field lines. The polarization capacity of a dielectric is characterized by the relative permittivity of the dielectric ε_r.

A voltage *V* applied across the conductors/plates induces a static electric field (*E*) as shown in the MIM structure depicted in Figure 2.1. The electric field causes polarization in the dielectric which results in the appearance of positive charge on higher voltage plate and a negative charge on the other plate.

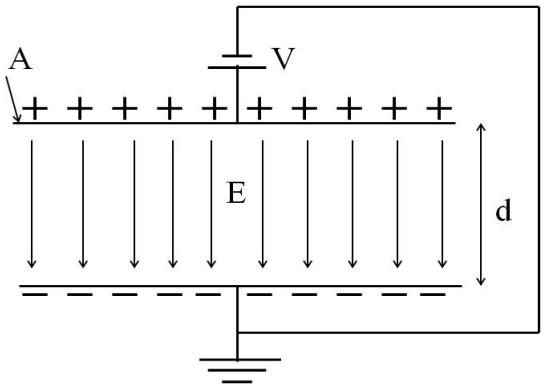

Figure 2.1: The schematic of metal-insulator-metal (MIM) structure. *A* is the area of the metal electrodes and *d* is the thickness of the dielectric.

The density of accumulated charge *Q* depends on the capacitance per unit area *C* of the dielectric and the applied voltage *V*, as expressed by Eq. (2.1)

$$Q = CV \tag{2.1}$$

The capacitance per unit area of the dielectric with thickness *d* and relative permittivity of ε_r is given by Eq. (2.2), where $\varepsilon_o = 8.854\times10^{-12}$ F/m is the permittivity of vacuum. The SI unit of the capacitance is Farad (F) and *C* is typically expressed in $\mu F/cm^2$.

$$C = \frac{\varepsilon_o \varepsilon_r}{d} \tag{2.2}$$

2.2 Field-effect transistor

Field-effect transistor (FET) is a three terminal device with source, drain, and gate electrodes as shown in Figure 2.2. The gate electrode is separated from the semiconductor by the gate dielectric, while the source and drain are in direct contact with the semiconductor. The transistor is typically symmetric with respect to the source and drain contacts. In this thesis the grounded electrode is referred to as source, while the other biased electrodes are drain and gate.

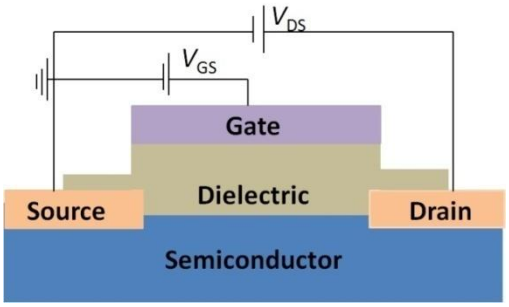

Figure 2.2: Cross-section of a field-effect transistor.

FET has an important feature that allows the control of current between the source and drain terminals (I_D) by changing the voltage on the third, gate terminal (V_{GS}). The gate electrode is typically made of conducting materials like Al, Cr, Au, etc., while the gate dielectric is made of insulating materials like silicon dioxide (SiO_2), aluminium oxide (Al_2O_3), silicon nitride (Si_3N_4), insulating polymers, etc.

The semiconductor layer is either based on inorganic (Si, Ge, etc.) or organic (pentacene, sexithiophene, etc.) materials. The best known FET that utilizes crystalline silicon as semiconductor and silicon dioxide as the dielectric is called

metal-oxide-semiconductor field-effect transistor (MOSFET). FET with organic semiconductor is known as organic field-effect transistor (OFET). Some dielectrics and semiconductors used in organic FETs are discussed in Section 2.6.

Many organic field-effect transistors employ the thin-film transistor structure and therefore OFETs are also known as organic thin-film transistors (OTFTs). It is possible to use undoped semiconductors in these designs [5]. TFT structures shown in Figure 2.3(a) and (b) are bottom-contact top-gate and bottom-gate top-contact, respectively. In this thesis, transistors with bottom-gate top-contact structure are studied.

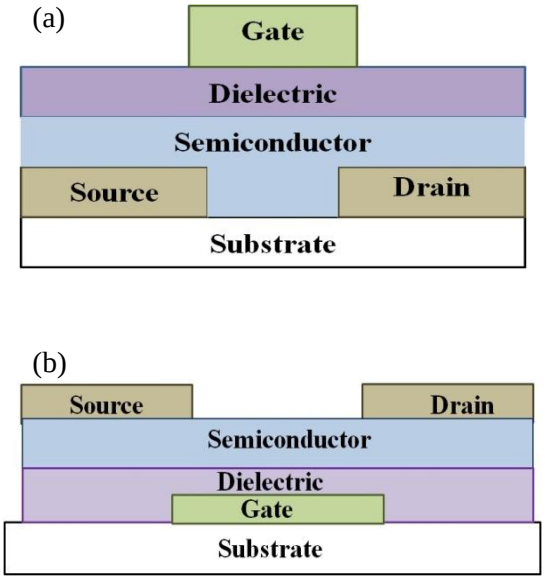

Figure 2.3: Thin-film transistor structures: bottom-contact top-gate (a) and bottom-gate top-contact (b).

2.3 Carrier transport in OTFTs

In an isolated atom the electron energy states form discrete levels, while the interactions between the neighbouring atoms in a solid lead to a formation of bands

of energy states. In inorganic semiconductors one is primarily concerned with the valence and conduction bands [15]. At the temperature of 0 K the valence band is fully filled with electrons, while the conduction band is empty. In an intrinsic semiconductor there are no allowed electron energy states between the valence and conduction bands and this energy gap (E_g) between the valence and conduction bands is called 'band gap'. The electron needs energy larger than E_g to move from valence to the conduction band. Based on the value of E_g semiconductors can be divided into small band gap and large band gap semiconductors. When the value of E_g becomes very large, the material becomes an insulator because very high energy is required to move the electron from the valence to the conduction band. Semiconductors have much smaller band gap than insulators and because of it the semiconductors allow conduction of charge while the dielectrics hinder charge transport.

Compared to the inorganic semiconductors, organic semiconductors consist of quite complex organic molecules and typically lack perfect molecular order. The electron energy states are determined by the overlap between the neighbouring molecular orbitals and the energy states are described in terms of the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO). HOMO and LUMO are analogous to the valence and conduction bands of inorganic semiconductors.

In metals there is no gap between the valence and conduction bands and the position of the Fermi energy (E_f) becomes a useful quantity when considering the charge transport between the metal and semiconductor. E_f represents the highest occupied electron energy state at the absolute temperature. Therefore, the energy

barrier for electron injection from the metal to semiconductor is the difference between E_f and LUMO. Similarly, the energy barrier for hole injection from metal to semiconductor is the energy difference between HOMO and E_f. This is shown in Figure 2.4(a) and (b). The alignment of E_f with HOMO results in good hole injection (Figure 2.4(a)), while the alignment of E_f with LUMO results in good electron injection (Figure 2.4(b)).

In OTFT, the selection of source/drain contacts and semiconductor material determines whether the OTFT operates as a p-channel or n-channel device. Charge is injected from the source into the semiconductor, followed by its transport through the channel at the semiconductor/dielectric interface and collection at the drain terminal. This project uses the organic semiconductor pentacene and gold source/drain contacts. This combination of materials leads to an estimated hole injection barrier of 0.47 eV [16].

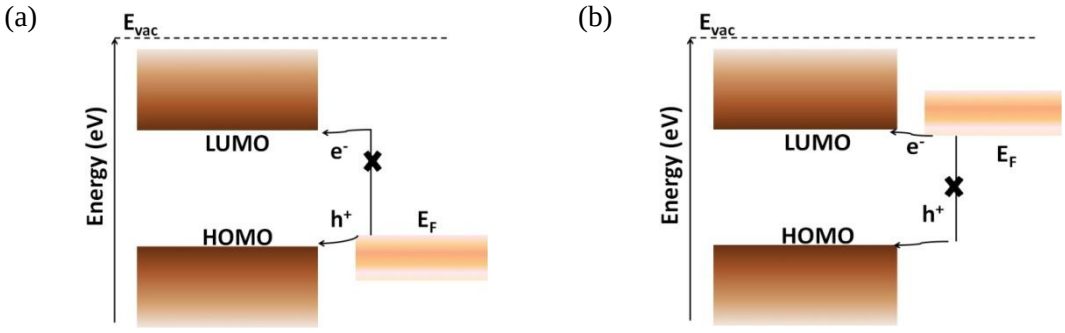

Figure 2.4: Alignment of E_f (metal) with HOMO/LUMO levels (organic semiconductor) for hole (a) and electron (b) injection.

There is a possibility of both hole and electron injection from metal to semiconductor, if E_f is closer to middle of the band gap. In these transistors,

depending on the applied voltage, either hole or electron injection takes place at a given time. These transistors are called ambipolar.

2.4 OTFT operation

On applying a gate-to-source voltage (V_{GS}), charge carriers accumulate near the semiconductor/dielectric interface. This charge is equal in magnitude but of opposite sign to that on the gate electrode. A negative V_{GS} induces an accumulation of holes while the positive V_{GS} would result in accumulation of electrons. Therefore, negative and positive V_{GS} is needed to turn the p- and n-channel OTFTs on, respectively.

On applying the drain-to-source voltage (V_{DS}), the layer of accumulated charge (transistor channel) will become part of the closed electrical loop and the charge is continuously injected at the source electrode and extracted at the drain. Figure 2.5 depicts the formation of a conducting channel in the p-channel OTFT, where the holes move in the direction of the electric field. In the n-channel OTFT the electrons accumulated near the semiconductor/dielectric interface move against this electric field. Therefore, negative and positive V_{DS} are applied to p-channel and n-channel OTFT, respectively. It results in the movement of holes in p-channel (electrons in n-channel) from the source to the drain. All OTFTs presented in this thesis are p-channel and, therefore, they are biased with negative V_{DS} and V_{GS}.

The magnitude of drain current I_D is dependent on the accumulated charge Q. Thus, the larger the value of Q, the larger is the drain current. In an ideal transistor, accumulated carriers at the semiconductor/dielectric interface should flow along the

channel but in a real transistor some of the carriers cross the dielectric resulting in gate current I_G of small magnitude.

Similarly, in a practical transistor the defects/traps in the semiconductor or near its interface cause reduction in the accumulated charge. Therefore, the charge density follows Eq. (2.3) instead of Eq. (2.1), where V_{th} is the threshold voltage.

$$Q = C(V_{GS} - V_{th}) \tag{2.3}$$

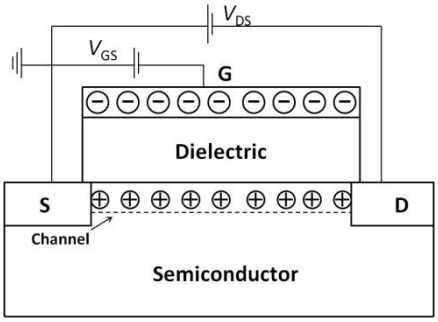

Figure 2.5: Channel formation at the semiconductor/dielectric interface of a p-channel OTFT. The cross section is not to scale.

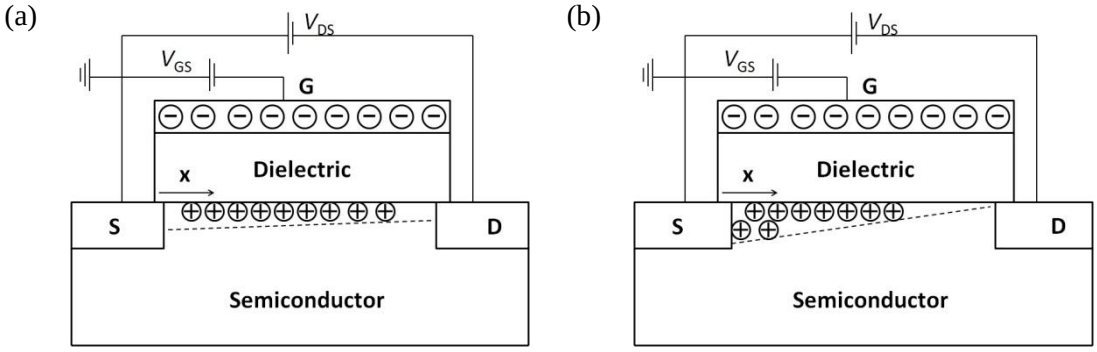

Figure 2.6: Schematic of the channel formation at semiconductor/dielectric interface for the linear (a) and saturation regimes (b).

OTFT has different operation regimes depending on the magnitude of the applied V_{GS} and V_{DS}. Linear (Figure 2.6(a)), saturation (Figure 2.6(b)), and subthreshold regimes are described in Sections 2.4.1 to 2.4.3.

2.4.1 Linear regime ($|V_{DS}| < |V_{GS} - V_{th}|$)

When $|V_{DS}| > 0$, a horizontal electric field arises along the x-direction of the channel. Let us assume that V_x is a voltage at the distance x from the source. Thus, the effective voltage in the channel at the point x is $V_{GS}-V_{th}-V_x$ and the accumulated charge per unit area is given by Eq. (2.4) (see also schematic in Figure 2.6 (a)):

$$Q(x) = C(V_{GS} - V_{th} - V_x) \tag{2.4}$$

According to Ohm's law (Eq. (2.5)) the current density J is the product of the electrical conductivity σ and electric field E. The conductivity and electric field along the channel are given according to equations (2.6) and (2.7), respectively. The electric field along the channel E_x is much smaller compared to the perpendicular field induced by gate electrode, a condition known as gradual channel approximation [15].

$$J = \sigma E \tag{2.5}$$

$$\sigma = qp\mu \tag{2.6}$$

$$E = -\frac{dV_x}{dx} \tag{2.7}$$

where q is charge of electron, p is hole density and μ is hole mobility. Substituting Eqs. (2.6) and (2.7) into Eq. (2.5) and setting $J = I/A$ results in the following:

$$I = qp\mu A\frac{dV_x}{dx} \tag{2.8}$$

where A is the cross-sectional area of the channel given by the channel width W and the thickness of the accumulation layer t. Since the hole density p is the charge per unit area Q divided by t, Eq. (2.8) can be rewritten:

$$I = q\frac{Q(x)}{t}\mu(Wt)\frac{dV_x}{dx} \tag{2.9}$$

Substitution of Eq. (2.4) into the Eq. (2.9) results in the following relation:

$$Idx = qC(V_{GS} - V_{th} - V_x)\mu W dV_x \tag{2.10}$$

To obtain the drain current as function of the applied voltages, the above equation is integrated over the channel length. While the drain current is constant along the channel, V_x = 0 V for x = 0 and $V_x = V_{DS}$ for $x = L$. The integration limits are shown in the Eq. (2.11) and solved.

$$\int_0^L Idx = qC\mu W\int_o^{V_{DS}}(V_{GS} - V_{th} - V_x)dV_x \tag{2.11}$$

$$I_D = qC\mu\frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{{V_{DS}}^2}{2}\right] \tag{2.12}$$

$$I_D = \mu C\left(\frac{W}{L}\right)V_{DS}\left[\left(V_{GS} - V_{th}\right) - \frac{V_{DS}}{2}\right] \tag{2.13}$$

$$I_D \approx \mu C\left(\frac{W}{L}\right)(V_{GS} - V_{th})V_{DS} \tag{2.14}$$

Since in the linear regime $|V_{DS}|$ is much smaller than $|V_{GS}-V_{th}|$, the second term $V_{DS}/2$ in Eq. (2.13) is negligible when compared to $V_{GS}-V_{th}$. Therefore Eq. (2.13) reduces to Eq. (2.14). The drain current is a linear function of the drain-to-source voltage, and therefore, this operation regime is known as the linear regime.

2.4.2 Saturation regime ($|V_{DS}| > |V_{GS} - V_{th}|$)

At higher V_{DS}, the voltage V_x along the channel also increases, resulting in a more rapid drop in the accumulated charge density Q (see Eq. (2.4)) when moving from the source to drain. The largest V_x occurs at the drain terminal, resulting in the minimum Q. V_{DS} at which $(Q|_{x=L}) = 0$ is the starting point of the saturation regime and known as V_{DSsat}. As shown in Figure 2.6(b), the channel is pinched-off at the drain terminal for V_{DSsat}. Setting $Q = 0$ and $V_x = V_{DS}$ in Eq. (2.4) (condition at the drain terminal) results in $V_{DSsat} = V_{GS} - V_{th}$. As V_{DS} rises above V_{DSsat}, the pinch-off point shifts towards the source terminal and the effective channel length is given by $L - \Delta L$. The voltage at the pinch-off point of the channel is $V_{GS} - V_{th}$ and it remains constant.

The drain current as a function of the applied voltages is obtained by integrating Eq. (2.10) along the channel. In saturation regime, $V_x = 0$ V at $x = 0$ and $V_x = V_{GS} - V_{th}$ at $x = L$.

$$\int_0^L I dx = qC\mu W \int_o^{V_{GS}-V_{th}} (V_{GS} - V_{th} - V_x) dV_x \tag{2.15}$$

$$I_D = \mu C \left(\frac{W}{2L} \right) (V_{GS} - V_{th})^2 \tag{2.16}$$

Beyond the pinch-off voltage, the drain-current is controlled by V_{GS} only. Consequently, the drain current does not change with the applied V_{DS}, known as the saturation regime.

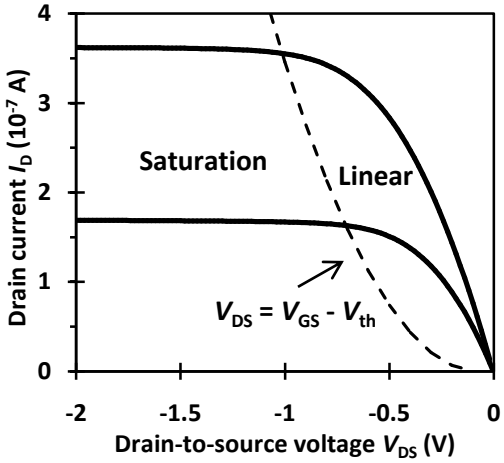

Figure 2.7: The drain current as function of V_{DS} in the linear and saturation regimes. The dashed line represents the boundary between two regimes.

In Figure 2.7 the linear and saturation regimes are indicated on the output characteristics. The dashed line is the boundary between both operating regimes. Drain current changes linearly for small V_{DS} but has almost constant value for larger V_{DS}.

2.4.3 Subthreshold regime ($|V_{GS}| < |V_{th}|$)

In a transistor, the turn-on transfer characteristic does not have a shape of a step function; instead, there is an exponential increase in the drain current for gate-source voltage just below the threshold voltage. This operating region that occurs 0.2 to 0.5 V below the threshold voltage is known as subthreshold region. The current in this region is typically expressed as an exponential function of V_{GS} [17]:

$$I_D = I_o \exp\left(\frac{q\,|V_{GS} - V_{th}\,|}{nkT}\right) \tag{2.17}$$

where k and q are Boltzmann's constant and the electronic charge. The inverse subthreshold slope S is defined as $[\partial \log_{10}(I_D)/\partial V_{GS}]^{-1}$and a smaller value is desirable for faster transition of the transistor from the off- to the on-state and vice versa.

2.5 Figures of merit

The transistor gate current I_G is correlated to the leakage current through the MIM structure that encompasses the gate dielectric used in the OTFT. MIM current densities are compared and the lower values indicate better insulating properties. The current through the MIM structure is usually small but when the voltage reaches a critical value, the dielectric material suffers an electrical breakdown that manifests itself by an irreversible large current flow. The voltage at which this phenomenon occurs is known as the breakdown voltage. Since the breakdown voltage depends on the dielectric thickness, the electric breakdown field E_{BD} is used to compare different MIM structures. E_{BD} is the breakdown voltage divided by the thickness of the dielectric.

The transistor drain current is proportional to the gate dielectric capacitance. To achieve larger drain current, higher capacitance is required. The growth of organic semiconductor depends on the underlying surface and low dielectric surface roughness can improve the semiconductor growth. This is important in the bottom-gate, top-contact OTFTs where the semiconductor is deposited on top of dielectric.

According to Eqs. (2.14) and (2.16), the high field-effect mobility and low threshold voltage also lead to larger drain current. The maximum and minimum drain current in the saturation regime is the on-current (I_{on}) and off-current (I_{off}), respectively. I_G and I_{off} should be as small as possible to lead to low power

dissipation in the transistor off-state. In addition, large ratio between the on- and off-current, I_{on}/I_{off}, is required for logic circuits.

In summary, the figures of merit of the OTFT dielectric are its capacitance, leakage current density, surface roughness, and the breakdown voltage. The figures of merit of OTFTs are the field-effect mobility, threshold voltage, subthreshold slope, on-current, off-current, gate-leakage current, and the on/off current ratio. The optimum OTFT performance is obtained by the proper selection of the dielectric, semiconductor, and source/drain contacts. The semiconductor/dielectric interface affects the field-effect mobility and the threshold voltage, as well as the stability of the transistor under the prolonged electrical bias. The interface between the semiconductor and the source/drain contacts affects the contact resistance. Consequently, both interfaces play an important role in determining overall performance.

This thesis focuses on the optimization of an ultra-thin AlO_x/C_8PA bi-layer dielectric through the comprehensive investigation of C_8PA monolayer formation. Next, some of the previously developed dielectrics for low-voltage organic thin-film transistors are presented.

2.6 State of the art

The use of organic thin-film transistors in inverters [8, 18–20], Braille displays [6], amplifiers and NAND or NOR digital gates [21] aims for reduction in their operating voltages. Low transistor operating voltage reduces power consumption in the electronic circuits and is one of the primary concerns of very large scale integrated devices. The role of a dielectric in achieving the low voltage is

best explained by Eq. (2.1). The high capacitance is a key approach to achieving low-voltage operation. High capacitance values can be achieved with high-k and/or ultra-thin dielectrics (see Eq. (2.2)).

Cyanoethylated poly(vinyl-alcohol) [22] and barium titanate ($Ba_{1.2}Ti_{0.8}O_3$) [23] have ε_r of ~ 12.5 and 15.5, respectively, and therefore such dielectrics with thickness >100 nm resulted in low operating voltage of 3 and 5 V. The capacitance value of high-ε_r dielectric is large even for slightly thicker dielectric layers, which results in low operating voltage and small leakage current density. The achieved leakage current densities are 1×10^{-7} A/cm^2 at 2 MV/cm [22], 4.8×10^{-8} A/cm^2 [23] and 1×10^{-7} A/cm^2 at 1 MV/cm [24]. However, with the exceptions of [13], such OTFTs typically exhibit high inverse subthreshold slope [23, 25] and low on/off current ratio [26].

OTFTs with medium-ε_r gate dielectrics such as aluminium oxide (ε_r ~6.2) [27] have achieved low operating voltages through reduction in thickness [12]. However, very thin aluminium oxide layers exhibit high leakage currents, e.g. $>10^{-6}$ A/cm^2 at 2 V [12]. Hence, these ultra-thin dielectrics have their limitations in OTFTs.

To obtain low leakage current with aluminium oxide, the oxide surface has been modified with polymer layers [28–31] or self-assembled monolayers (SAMs) [11, 32–37]. These treatments reduce the leakage current density and increase the breakdown voltage, while slightly lowering the capacitance. Thus, low operating voltage and low leakage current density are obtained simultaneously. For example, OTFT with 100-nm-thick aluminium oxide need 40 V [38] to turn on, while AlO_x surface modified with polymer layers reduced the operating voltage to 6 to 8 V [29,

30]. This polymer treatment also led to an increase in the breakdown field from 1 MV/cm to 4 MV/cm [29]. Further reduction in OTFT operating voltages down to 3 V was achieved with organic self-assembled monolayers. The use of self-assembled monolayer in OTFTs was introduced by Vuillaume's group [39]. Even though the typical thickness of organic monolayer is around 1-2 nm, it can reduce the dielectric leakage current density by orders of magnitude [40].

The overall leakage current density obtained for silicon dioxide functionalized with SAM and aluminium oxide/SAM was 10^{-9} A/cm^2 at 1 V [39] and 5×10^{-8} A/cm^2 at 2 V [18], respectively, and these values are comparable to those obtained with thicker high-ε_r dielectrics [22–24]. Reduction in leakage current density depends on how well the SAM covers the inorganic oxide [18]. Depending on the underlying dielectric, the use of the same organic monolayer can result in improvement as well as deterioration. For example, (18-phenoxy-octadecyl) trichlorosilane SAM resulted in enhancement of OTFT performance on silicon dioxide [40] while it caused degradation on aluminium oxide [12].

Among different phosphonic acids, alkyl phosphonic acids are widely used to form SAM dielectrics [11, 18, 32, 34, 37, 41]. Reduction in OTFT operating voltage down to 3 V is achievable with alkyl phosphonic acid on aluminium oxide [11, 18, 32, 37]. The surface energy of alkyl phosphonic acid of 25 mJ/m^2 [42] is favourable for several organic semiconductors. The field-effect mobility of 0.7 cm^2/Vs [11], 0.6 cm^2/Vs [18], 0.28 cm^2/Vs [32], and 1.5 cm^2/Vs [43] were obtained using alkyl phosphonic acid SAM and pentacene semiconductor.

2.7 Summary

This research focuses on the use of medium-ε_r aluminium oxide (AlO_x) functionalized with a monolayer of n-octylphosphonic acid (C_8PA) and implemented as a dielectric in low-voltage OTFTs that operate at 2 V. The leakage current of the ultra-thin (~9 nm thick) AlO_x is reduced when C_8PA SAM is added on top of it. The novelty of this research includes the optimization of the self-assembly of C_8PA monolayer using a vacuum, vapour-phase growth. This AlO_x/C_8PA dielectric is successfully implemented in OTFTs using a conjugated, small-molecule pentacene as the semiconductor. Pentacene was selected among different small-molecule organic semiconductors because its interface with solution-deposited alkyl phosphonic acids has been studied widely and OTFTs based on pentacene often exhibit high field-effect mobility. The vacuum, vapour-phase self-assembly of C_8PA monolayer opens up the possibility for completely dry OTFT fabrication process amenable to roll-to-roll processing. The correlation between the surface and structural properties of the AlO_x/C_8PA bi-layer dielectric and OTFT performance is investigated.

Chapter 3

Methodology

This chapter describes the fabrication of devices and supporting structures and the electrical, surface and structural measurements performed on them. The fabrication process of OTFT and MIM structures is explained in Section 3.1, while the preparation of samples for material characterization is described in Section 3.2. Electrical measurements of MIM structures and OTFTs are discussed in Section 3.3 and 3.4, respectively. These sections also explain how various parameters were extracted from measurements. Surface and structural measurements are presented in Sections 3.5 and 3.6. The summary of the experiments conducted in this thesis is presented in Section 3.7.

3.1 Fabrication of OTFTs and MIM structures

The cross-section of the OTFT structure used in this project is shown in Figure 3.1. The bottom gate electrode is made of aluminium and the top source/drain contacts are made of gold. Aluminium oxide (AlO_x) and n-octylphosphonic acid (C_8PA) form the dielectric bi-layer and pentacene is the organic semiconductor.

OTFT and MIM structures were fabricated side by side. A schematic of the transistor fabrication process is presented in Figure 3.2. All thermal evaporation steps were conducted in Minispectors (Kurt J. Lesker) high vacuum system (base pressure of ~ 10^{-7} mBar) enclosed in a N_2-filled glove box with O_2 and H_2O content less than 1 particle-per-million (ppm). The system allows the control of the layer thickness, deposition rate and deposition temperature. Both metals and organic materials were thermally evaporated. All organic materials were deposited from 1-cm^3 crucibles. Their temperature is computer controlled, allowing the control of the desired evaporation rate. Contamination during loading/unloading of the material is avoided by using the integrated glove box.

For aluminium deposition an alumina-coated tungsten crucible was used, while gold was deposited from a tungsten boat. Materials were heated above their melting points and deposited on the substrate placed above the evaporation sources.

The oxidation of aluminium was performed in an ultraviolet ozone cleaning systems (UVOCS) enclosed under a Hepa filter. A low-pressure quartz mercury lamp emits UV light at ~185 and ~254 nm, resulting in the generation of ozone. Ozone is a strong oxidizer, leading to the formation of aluminium oxide (AlO_x) on the surface of aluminium.

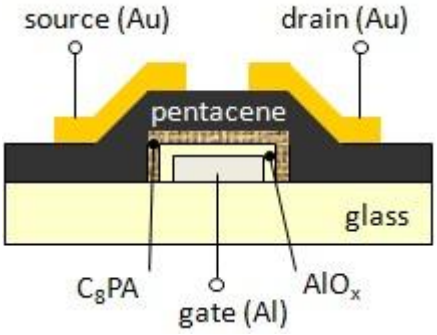

Figure 3.1: Cross-section of organic thin-film transistor.

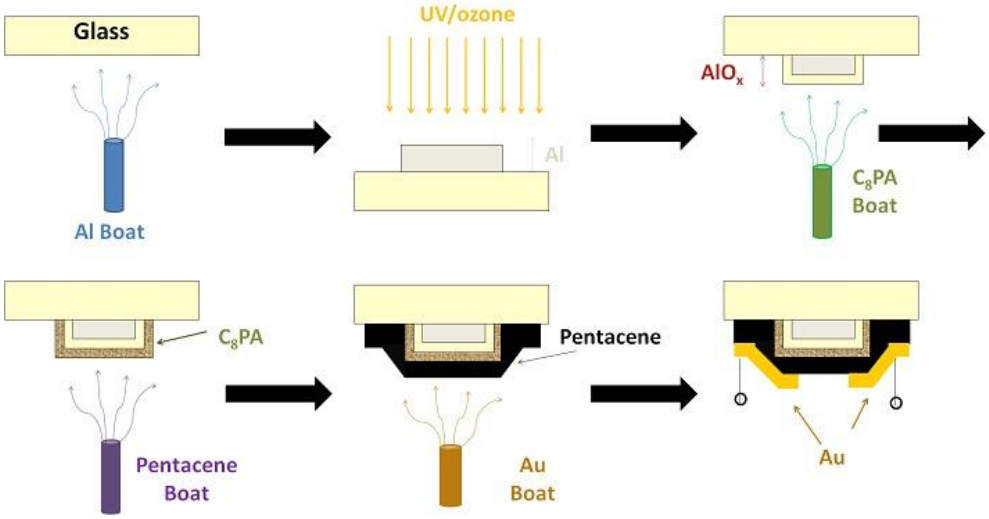

Figure 3.2: Schematic of OTFT fabrication process.

All OTFT and MIM structures were prepared by vacuum vapour deposition; meaning that all layers – aluminium, C_8PA, pentacene, and gold were thermally evaporated in vacuum. Only the oxidation of aluminium was performed in ambient environment. Firstly, 20-nm-thick aluminium was evaporated on an Eagle 2000 glass substrate. The purity of the aluminium was 99.999%. Part of the gate electrodes (away from the transistor islands) was capped with a 20-nm-thick gold layer to prevent their oxidation during UV/ozone exposure. To prepare a self-assembled monolayer using vacuum evaporation, ~10-nm-thick C_8PA layer corresponding to

several monolayers was thermally evaporated on top of AlO_x and subsequently heated to 135-160°C to remove the physisorbed molecules. The end result is a self-assembled C_8PA monolayer. In some experiments this AlO_x/C_8PA bi-layer dielectric was prepared together with bare aluminium oxide (AlO_x) to provide comparative study. The transistors were completed by the evaporation of pentacene and the source/drain gold contacts of 50 nm each. The purity of gold was 99.99%, while pentacene was purified in-house.

The fabrication of MIM structures followed the same process, except the semiconductor layer was omitted. Therefore, during pentacene deposition, the MIM structures were fully masked. Additional fabrication details pertinent to transistors discussed in the following chapters are summarized in Section 3.7.

3.2 Fabrication of samples for material characterization

The experiments described in Chapters 5, 6, and 8 include the Fourier Transform Infrared Spectroscopy (FTIR) and Water Contact Angle (WCA) measurements. To conduct these measurements, AlO_x and AlO_x/C_8PA layers were grown on glass substrates exactly in the same manner as fabrication of the corresponding MIM and OTFT structures.

3.3 MIM structures: measurement and evaluation

The electrical measurement of the MIM structures was performed with Agilent B1500A semiconductor device analyser under ambient environmental conditions. Three types of measurements were performed: capacitance as a function of a.c. frequency (C-f) (Figure 3.3) and I-V measurements for low (Figure 3.5(a)) and high voltages (Figure 3.5(b)). From these measurements, the capacitance per unit area, leakage current density, AlO_x and C_8PA thickness, and the breakdown voltage were extracted.

3.3.1 Capacitance measurement

The capacitance of the MIM structures was measured between 1 kHz and 1 MHz as shown in Figure 3.3. The capacitance did not change significantly within this frequency range.

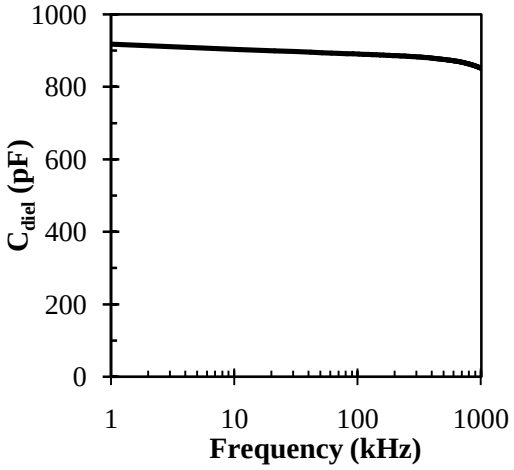

Figure 3.3: Capacitance of MIM structure as a function of a.c. frequency.

3.3.1.1 Capacitance per unit area (*C*)

The mean capacitance per unit area was calculated from several MIM structures at various frequencies and the mean capacitance (*C*) obtained at a frequency of 100 KHz is used in the calculation of the OTFT field-effect mobilities. Let's express the capacitance per unit area of the bi-layer dielectric as *C* and the individual AlO_x and C_8PA capacitances as C_{AlOx}, and C_{C8PA}, respectively. Since it is not possible to measure C_{C8PA}, its value is calculated from the measured *C* and C_{AlOx}. In a bi-layer dielectric C_{C8PA} and C_{AlOx} are in series and follow the relation $1/C = 1/C_{AlOx} + 1/C_{C8PA}$.

3.3.1.2 AlO_x and C_8PA thickness

As shown in Figure 3.4, AlO_x and C_8PA layers have the same cross-sectional area *A* but different thicknesses d_1 and d_2. The relative permittivity of AlO_x and C_8PA is ~6.8 [44] and ~2.1 [45], respectively. The C_8PA thickness is extracted from the calculated C_{C8PA} capacitance using the expression for parallel plate capacitor $d_2 = \varepsilon_2/C_{C8PA}$, where ε_2 is the permittivity of C_8PA.

3.3.2 Current-voltage measurement

Current-voltage characteristics were measured on $Al/AlO_x/Au$ and $Al/AlO_x/C_8PA/Au$ MIM structures by varying the voltage on the Al electrode and keeping the Au contact grounded. These measurements were performed for two different voltage regimes. The leakage current density and the breakdown voltage were extracted from these measurements.

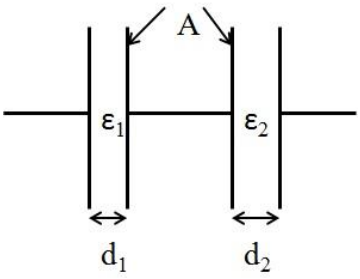

Figure 3.4: Electrical model of the bi-layer AlO_x/C_8PA MIM structure.

3.3.2.1 Leakage current density

From the current-voltage characteristic (Figure 3.5(a)), the leakage current density is calculated. The measured current as a function of the applied voltage is divided by the area of the MIM structure. The leakage current density of different MIM structures is compared for voltages smaller than 3 V, which is the regime of OTFT operation.

3.3.2.2 Breakdown voltage

The current-voltage characteristic of a typical MIM structure for the high voltage regime is shown in Figure 3.5(b). The breakdown voltage is defined as voltage at which the current through the MIM structure reaches 1 mA/cm^2. An abrupt rise in the leakage current that corresponds to electrical breakdown can be seen in Figure 3.5(b) around 5 V. Since the OTFT operating voltage is limited by the breakdown voltage of the gate dielectric, higher breakdown voltages are desirable.

3.4 OTFTs: measurement and evaluation

The transfer and output characteristics of the OTFTs were measured under ambient environmental conditions using an Agilent B1500A semiconductor device

analyser in a sweep mode. OTFT hysteresis was obtained by stepping the gate voltage from positive to negative values and back.

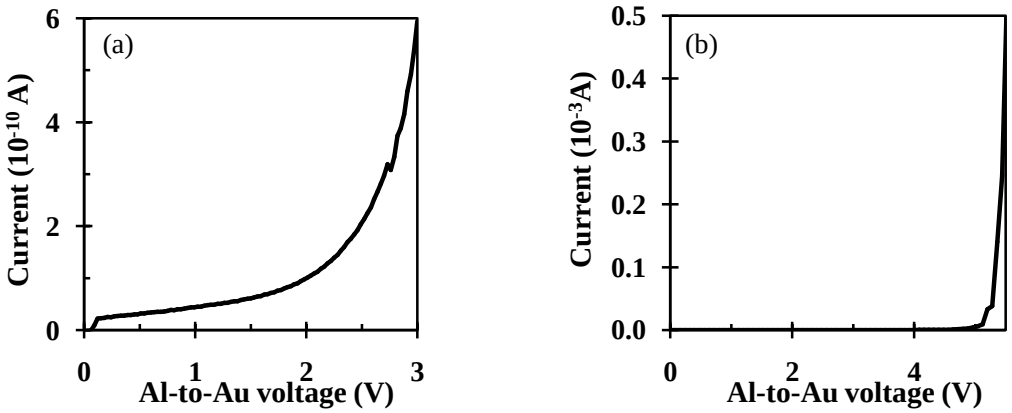

Figure 3.5: The current-voltage measurement of MIM structure for lower (a) and higher (b) voltages.

3.4.1 Transfer characteristics

The transfer characteristics plot the drain current as a function of the gate-to-source voltage for a set of drain-to-source voltages. An example is shown in Figure 3.6. The transfer characteristics were measured for two different drain-to-source voltages V_{DS} that correspond to the linear and saturation regimes.

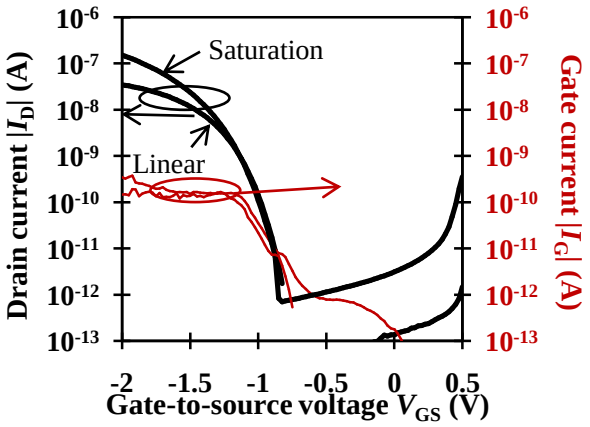

Figure 3.6: The transfer characteristics of OTFT for V_{DS} = –0.1 V (linear regime) and –2 V (saturation regime).

The gate current I_G is measured along with I_D. All currents are plotted on the same logarithmic scale. From the transfer characteristics in the linear regime the field-effect mobility and threshold voltage were calculated. In the saturation regime, in addition to these two parameters, the subthreshold slope, off- and on-currents and on/off current ratio were extracted. The off-current is defined as the minimum $|I_D|$ for V_{DS} = –2 V. Similarly, the on-current is defined as the maximum $|I_D|$ for V_{DS} = –2 V. The channel and contact resistances were calculated from OTFT transfer characteristics in the linear regime for transistors with the same W and different L.

3.4.1.1 Field-effect mobility and threshold voltage

The current-voltage relation in the linear and saturation regime is given by Eq. (2.14) and (2.16), respectively. The field-effect mobility in the linear regime is calculated from the linear fit of I_D vs. V_{GS} using Eq. (3.1) and in the saturation regime from the linear fit of $\sqrt{I_D}$ vs. V_{GS} using Eq. (3.2) (Figure 3.7(a) and (b)).

$$\mu = \left(\frac{\partial I_D}{\partial V_{GS}}\right)\frac{1}{C\left(\frac{W}{L}\right)V_{DS}} \tag{3.1}$$

$$\mu = \left(\frac{\partial \sqrt{I_D}}{\partial V_{GS}}\right)^2 \frac{1}{C\left(\frac{W}{2L}\right)} \tag{3.2}$$

In both cases the intercept on the voltage axis provides the threshold voltage V_{th}. OTFT field-effect mobility, threshold voltage in the linear and saturation regimes are extracted by the MATLAB program given in Appendix A and B, respectively. The field-effect mobilities in the linear and saturation regime differ by ±10%. Linear field-effect mobility is presented in this thesis.

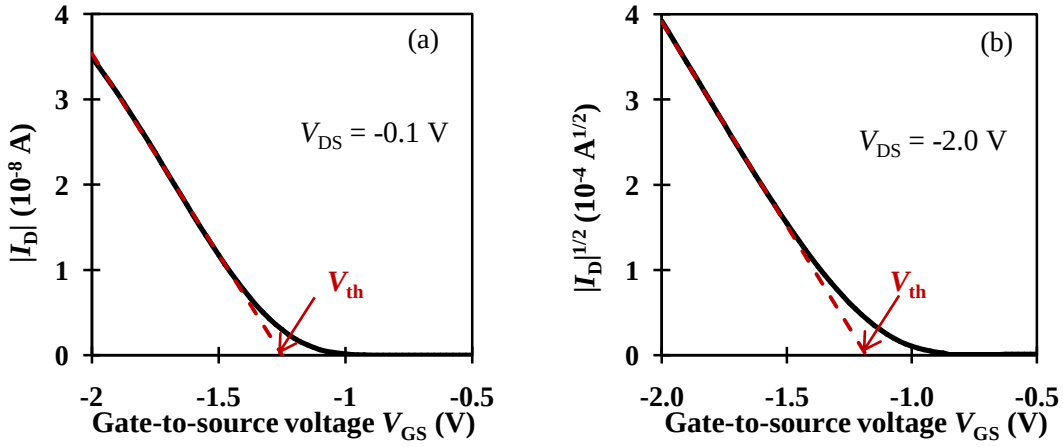

Figure 3.7: Extraction of the slope and threshold voltage for V_{DS} = –0.1 V (a) and –2.0 V (b).

3.4.1.2 Subthreshold slope

In the subthreshold regime I_D changes exponentially with V_{GS} as described by Eq. (2.17). Hence, the plot of log ($|I_D|$) vs. V_{GS} should follow a linear dependence. Extraction of this slope is shown in Figure 3.8. The inverse of this slope is known as subthreshold slope S given by:

$$S = \left[\frac{\partial}{\partial V_{GS}} (\log_{10} | I_D |) \right]^{-1} \tag{3.3}$$

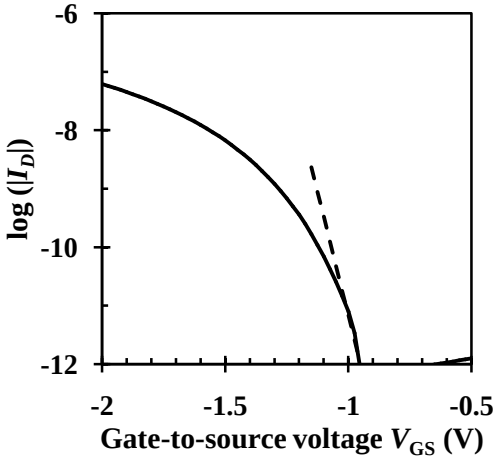

Figure 3.8: Extraction of the subthreshold slope from the transfer curve in saturation regime.

The subthreshold slope was extracted by fitting Eq. (3.3) to three data points in the subthreshold region using the program in Appendix C. Three different sets of points were fitted for each transistor and the lowest value (out of three) is presented in the thesis.

3.4.1.3 Contact and channel resistances

The contact resistance (R_c) refers to the resistance between the source/drain contact and the transistor channel. Ideally, this should be zero but in practical OTFTs this resistance is not negligible. The contact resistance is more dominant in OTFTs with short channel length.

In the linear regime it is assumed that the channel is uniform along its length and controlled by the gate voltage. The channel resistance is given by $L/[\mu CW(V_{GS}-V_{th})]$ and as such is proportional to the channel length L. Hence, instead of the total channel resistance, the channel resistance per unit length R_{ch} ($\Omega/\mu m$) is a figure of merit. R_{ch} is equal to $1/[\mu CW(V_{GS}-V_{th})]$.

The total resistance R_T of an OTFT is divided between the channel and the contact resistance. R_T is calculated by dividing the drain-to-source voltage by the drain current. To extract R_{ch} and R_c from the total resistance, the classical transmission-line method (C-TLM) [46] is employed. This method is applied to OTFTs with similar channel and contact properties; the only difference is their channel length. The method works best for OTFTs fabricated together.

In C-TLM, the total resistance multiplied by the channel width ($R_T \times W$) is plotted against the channel length L for different V_{GS}, as shown in Figure 3.9. Eq. (3.4) describes the relation between the total resistance and the contact resistance.

Hence, the slope divided by W (Figure 3.9) corresponds to R_{ch} and the intercept on y-axis divided by W gives R_c.

$$R_T W = \frac{L}{\mu C(V_{GS} - V_{th})} + R_C W \tag{3.4}$$

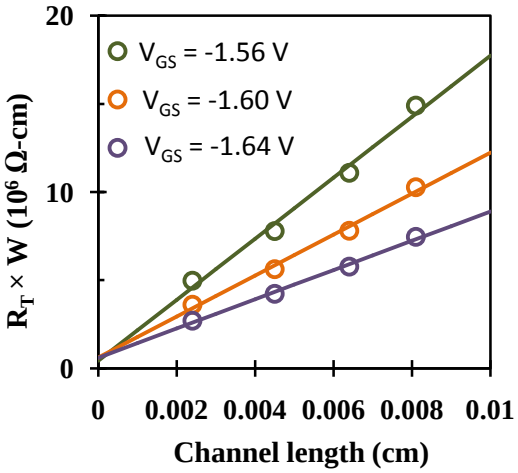

Figure 3.9: Extraction of the contact and channel resistances using C-TLM method.

3.4.2 Output characteristics

The output characteristic is a plot of drain current I_D as a function of the drain-to-source voltage V_{DS} for a set gate-to-source voltage V_{GS}. An example of an OTFT output characteristic is shown in Figure 2.7. Each output characteristic captures the transistor behaviour in both linear and saturation regimes. The drain current is effectively zero for V_{GS} smaller than V_{th}.

3.4.3 Transistor hysteresis

Hysteresis is obtained by measuring the transfer characteristic in both directions, i.e. from positive to negative and from negative to positive V_{GS}. In

p-channel OTFTs, sweeping V_{GS} from the positive to negative voltage brings the transistor from the off- to the on-state. Similarly, sweeping V_{GS} from the negative to positive voltage values brings the transistor from the on- to the off-state. Ideally, there should be no difference between these two measurements, i.e. no hysteresis should be observed. An example of such measurement is shown in Figure 3.10.

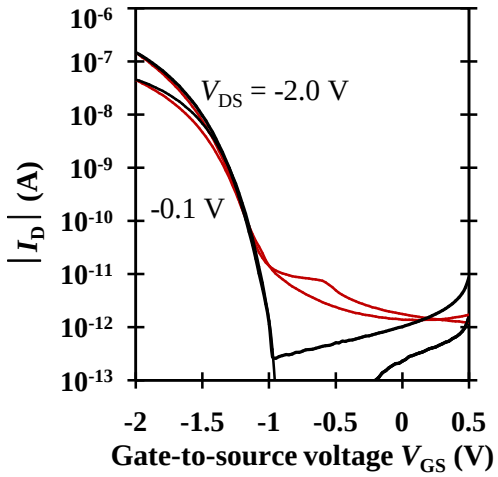

Figure 3.10: Transistor hysteresis for V_{DS} of –0.1 and –2 V. The black and red lines correspond to the off-to-on and on-to-off measurement, respectively.

3.4.4 Bias stress measurement

When a p-channel transistor is turned on, the holes are trapped into localized electronic states near the semiconductor/dielectric interface. This leads to increased threshold voltage and decreased on-current and possibly an increased subthreshold slope and decreased field-effect mobility.

Bias stress measurements were performed for some transistor sets. All transistors were biased for up to 5000 s, with the source and drain electrodes grounded. The transfer characteristic was measured after 10, 30, 70, 100, 200, 600,

1000, 2000, and 5000 s of bias stress. These transfer characteristics were used to extract OTFT parameters: the field-effect mobility, threshold voltage, subthreshold slope, and the on-current at $V_{DS} = V_{GS} = -3$ V.

Stretched exponential functions were used to fit the changes in the threshold voltage, subthreshold slope, field-effect mobility, and the drain current as a function of the bias stress time. The form of these stretched exponential equations depends on whether a change in the parameter or the normalized parameter is fitted:

$$\Delta V_{th} = |V_{th}(t) - V_{th}(0)| = |V_{th}(\infty) - V_{th}(0)| . \left[1 - e^{-(t/\tau_{Vth})^{\beta_{Vth}}}\right] \quad (3.5)$$

$$\Delta S(t) = S(t) - S(0) = \left(S(\infty) - S(0)\right) . \left[1 - e^{-(t/\tau_S)^{\beta_S}}\right] \quad (3.6)$$

$$\frac{\mu(t)}{\mu(0)} = \frac{\mu(\infty)}{\mu(0)} + \left[1 - \frac{\mu(\infty)}{\mu(0)}\right] . e^{-(t/\tau_\mu)^{\beta_\mu}} \quad (3.7)$$

$$\frac{I_D(t)}{I_D(0)} = \frac{I_D(\infty)}{I_D(0)} + \left[1 - \frac{I_D(\infty)}{I_D(0)}\right] . e^{-(t/\tau_{ID})^{\beta_{ID}}} \quad (3.8)$$

Here $\Delta V_{th}(t)$ is the threshold voltage shift, $V_{th}(t)$ is the threshold voltage after t seconds of bias stress, $V_{th}(0)$ is the initial threshold voltage before the application of the electrical bias, $V_{th}(\infty)$ is the equilibrium threshold voltage after prolonged electrical bias, τ_{Vth} is a time constant and β_{Vth} is the stretching parameter ($0 < \beta_{Vth} \leq 1$). Similarly, $\Delta S(t)$ is the change in the subthreshold slope after t seconds, $S(t)$ is the subthreshold slope after t seconds of bias stress, $S(\infty)$ is the equilibrium subthreshold slope after very long time, $S(0)$ is the initial subthreshold slope before the application of the electrical bias, τ_S is a time constant, and β_S is the stretching parameter. $\frac{\mu(t)}{\mu(0)}$ is the field-effect mobility after t seconds of bias stress normalized with respect to

the initial mobility, $\frac{\mu(\infty)}{\mu(0)}$ is the normalized equilibrium mobility after prolonged electrical bias, τ_μ is a time constant, and β_μ is the stretching parameter. Finally, $\frac{I_D(t)}{I_D(0)}$ is the normalized drain current after *t* seconds of bias stress, $\frac{I_D(\infty)}{I_D(0)}$ is the normalized equilibrium drain current after prolonged electrical bias, τ_{ID} is a time constant, and β_{ID} is the stretching parameter.

The fitting parameters (τ, β, and equilibrium value) were extracted from the least square fit of the data to Eqs. (3.5) – (3.8) using the MATLAB program given in Appendix E. The fitting is most sensitive to the stretching parameter β and, therefore, the boundary conditions of β were altered several times to achieve good accuracy.

3.5 Surface properties

To complement the electrical characterization of the devices, Atomic Force Microscopy (AFM) and Water Contact Angle (WCA) measurements on AlO_x and AlO_x/C_8PA were performed. Pentacene and gold surfaces were also studied by AFM.

3.5.1 Water Contact Angle (WCA)

The angle formed at the interface between the liquid (water droplet) and the underlying solid surface is the contact angle θ (Figure 3.11 [47]). In the bulk of the water droplet the resulting net force on each molecule is zero because the forces from the neighbouring molecules are balanced. However, the absence of neighbouring molecules near the surface of the droplet leads to a non-zero force known as surface tension. When a droplet of water rests on the surface of a solid, the shape of the

droplet is determined by the balance of the interfacial tensions between the liquid, vapour, and solid.

In 1805 Young formulated the following relationship at a point where all three phases meet [47]:

$$\sigma_s = \gamma_{sl} + \sigma_l \cdot \cos\theta \tag{3.9}$$

where σ_s and σ_l is the surface tension of the solid and liquid, respectively, γ_{sl} is the interfacial tension between the solid and liquid phases and θ corresponds to the angle between vectors σ_l and γ_{sl}.

As mentioned above, the shape of the water droplet is determined by its interaction with the solid surface. When the water droplet is placed on the solid of low surface energy, the interaction between them is weak. The solid surface is hydrophobic and the contact angle is larger than 90°. The stronger the interaction between the solid surface and the water droplet, the smaller is the contact angle [48]. Hydrophilic surfaces have water contact angle smaller than 90°.

Surface tension responsible for the shape of the droplet is affected marginally by the external forces such as gravity and air pressure. In addition, factors such as (i) evaporation of the liquid, (ii) migration of substances from the solid into the liquid and vice versa, (iii) chemical reactions between the solid and liquid, and (iv) the solid being dissolved or swollen by the liquid, influence the measurement. Therefore, measurements of dissimilar samples conducted in a short time interval are compared in this thesis.

Static water contact angle measurements were performed in ambient air with a Krüss DSA30B goniometer. The sample was mounted on the horizontal stage and

~5-6 µL Millipore water droplet was placed on the measured surface and the image was captured with a high resolution camera. Both left and right static contact angles were measured for each droplet. The mean and standard deviation of the contact angle were obtained from at least four measurements.

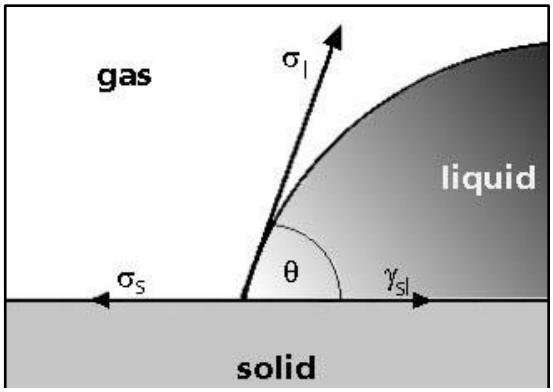

Figure 3.11: A schematic of a liquid droplet showing the balance of the interfacial tensions at the point where three phases meet [47].

3.5.2 Atomic Force Microscopy (AFM)

Surface images of C_8PA, AlO_x, Au, and pentacene were obtained with diInnova AFM using a silicon probe in the tapping mode. This mode prevents the damage to the surface of the measured material because the cantilever oscillates (moves up and down) at its resonant frequency while scanning the surface. In such a case the surface topography of soft surfaces such as C_8PA can be obtained. Through the feedback mechanism, a constant force between the tip and the measured surface is maintained.

The average (R_a) and root-mean-square (R_q) surface roughness of AlO_x and AlO_x/C_8PA surfaces were extracted from several scanned areas. An example of surface having the average surface (R_a) and root-mean-square (RMS) roughness (R_q)

are shown in Figure 3.12. Z(x) is the distance from a line parallel to the substrate surface.

R_a is the average of Z(x) values, while R_q is the average of the squares of Z(x). Mathematical expression for R_a and R_q is given by Eqs. (3.10) and (3.11), respectively.

$$R_a = \frac{1}{L}\int_0^L Z(x) \tag{3.10}$$

$$R_q = \sqrt{\frac{1}{L}\int_0^L |Z(x)|^2} \tag{3.11}$$

The average surface roughness is the mean of the measured profile and therefore it does not capture the height/depth of the peaks/valleys. A surface with similar peaks and valleys can lead to zero average surface roughness while, in reality, it is rough. Using the squares of the roughness values (RMS) provides more accurate information about the surface roughness than the average value [49]. In this thesis, values of R_q of AlO_x/C_8PA surfaces prepared at different conditions are compared.

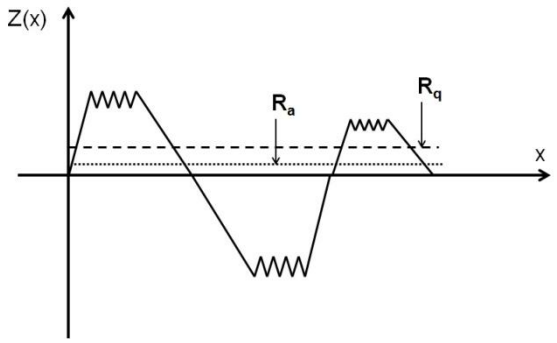

Figure 3.12: Surface profile showing the average (R_a) and root-mean-square (R_q) surface roughness.

The pentacene grain structure was evaluated from AFM surface images. The surface of Au source/drain contacts was also investigated with the aim to understand the interface between the semiconductor and the source/drain contacts.

3.6 Structural properties – Fourier Transform Infrared Spectroscopy (FTIR)

In linear and non-linear molecules the number of normal modes of vibrations is 3N−5 and 3N−6, respectively, where N is the number of atoms/molecules involved. The linear molecules, e.g. hydrogen or nitrogen, have only 3(2)−5 = 1 mode of vibration [50]. Non-linear molecular group of methyl ($-CH_3$) and methylene ($-CH_2$) results in 9 and 6 modes of vibration, respectively [50].

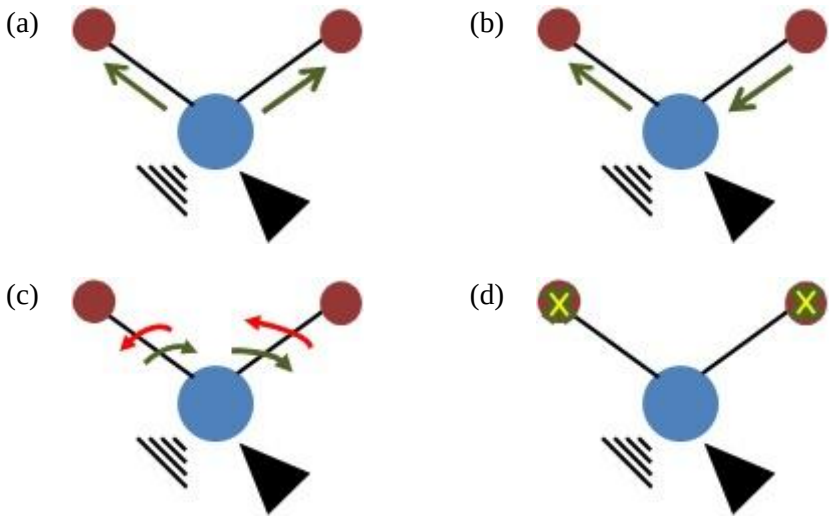

Figure 3.13: Vibration modes of $-CH_2$: symmetric stretching (a), asymmetric stretching (b), rocking (c), and wagging (d). The arrows show the direction of motion. The H atoms (brown) move out of the plane in (d) and this motion is denoted by the crosses.

Some common modes of vibrations such as stretching, rocking, wagging, and twisting are described using $-CH_2$. In stretching mode the bond length changes between C and H atoms. The symmetric and asymmetric vibration is shown in Figure 3.13(a) and (b), respectively. In the rocking mode both H atoms move right and left while the angle between them is maintained. In the wagging mode both H atoms move forward and backward with respect to the plane of the paper while the angle between them does not change. These two modes are shown in Figure 3.13(c) and (d). The twisting mode is similar to the wagging mode except one H atom moves forward while the other moves backward (with respect to the plane of the paper).

A molecular vibration is a consequence of the absorption of a photon by an existing dipole. The photon can be described by energy E, wavelength λ or the wavenumber $\bar{\upsilon}$. To a first approximation, the vibration of a diatomic molecule can be modelled by a simple harmonic oscillator. An example of the two atoms of masses m_1 and m_2 connected to a spring of the spring constant K is shown in Figure 3.14.

The vibrating masses m_1 and m_2 follow Eq. (3.12) to balance their centre of mass. The heavier mass m_1 has smaller displacement X_1 than the lighter mass m_2. The classical vibration frequency ν of two masses on the spring is given by Eq. (3.13).

$$m_1X_1 = m_2X_2 \tag{3.12}$$

$$\nu = \frac{1}{2\pi}\sqrt{K\left(\frac{1}{m_1}+\frac{1}{m_2}\right)} \tag{3.13}$$

Eq. (3.13) shows that the frequency of oscillation depends on the masses of atoms and the spring constant K. In molecular vibrations, K would represent the bond strength instead of the spring constant. In addition, the wavenumber $\bar{\upsilon}$ is used instead of ν. The wavenumber $\bar{\upsilon} = \nu/c$, where c is the speed of light; the unit of $\bar{\upsilon}$ is cm^{-1}.

Two dissimilar atoms attached via a bond have the same frequency of vibration, affected by their surrounding, while their amplitudes differ. The approximate range of K for a single, double and triple bond is $(3\text{-}6)\times10^{-8}$, $(10\text{-}12)\times10^{-8}$, and $(15\text{-}18)\times10^{-8}$ N/Å [50], respectively. The calculation of the vibration frequencies for large molecules is quite complex. Nevertheless, Eq. (3.13) points to the fact that vibrations of lighter atoms such as hydrogen are found at a higher wavenumber when compared to heavier atoms. Stronger bonds also result in a higher wavenumber.

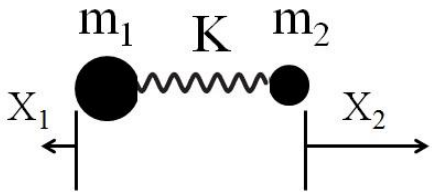

Figure 3.14: A schematic of the diatomic molecule motion. The masses m_1 and m_2 have displacements of X_1 and X_2. K is the spring constant.

The molecular vibrations are measured by Fourier Transform Infrared Spectroscopy (FTIR). Infrared light is an electromagnetic radiation with wavelengths between 700 nm and 1 mm. In FTIR, a polarized infrared beam is incident on the sample. Part of the light is absorbed by the measured surface and the rest is reflected. This measurement is repeated for different combinations of frequencies. A Fourier Transform is used to obtain absorbance at each frequency (wavenumber). When the frequency of the incident infrared light corresponds to the resonant frequency of an existing molecular dipole, strong absorption occurs and this property is used in the study of the molecular structure. The frequencies of interest are divided into the near-IR (14000-4000 cm^{-1}), mid-IR (4000-400 cm^{-1}) and the far-IR regions (400-10 cm^{-1}).

Infrared light, being an electromagnetic wave, consists of an electric and magnetic component; however IR spectroscopy is only concerned with the electric field. The electric field is assumed to be constant because the wavelength of the incident light is much larger than the distance between the studied atoms. The electric field forces the positive and negative charges to move in the opposite directions, causing a change in the dipole moment as shown in Figure 3.15. The dipole oscillates with the frequency of the incident light and the intensity is proportional to the square of the change in the dipole moment [50]. The IR spectrum is obtained by plotting the absorbance or transmittance of the material under investigation versus the wavenumber $\bar{\upsilon}$ of the monochromatic light.

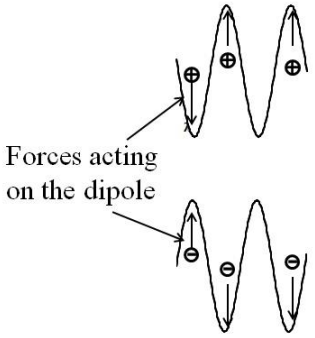

Figure 3.15: Schematic of the forces acting on a dipole.

FTIR was measured with Nicolet 380 spectrometer in ambient air. The beam diameter was ~ 2 mm. PeakFit analysis provided the location of the peaks, their intensity, full width at half maximum (FWHM) and integral area. The absorbance of AlO_x/C_8PA and the reference AlO_x were measured. The data was interpreted based on the known vibration frequencies of the relevant chemical functional groups.

3.7 OTFT optimization

Each fabricated transistor series (an individual experiment) contained three to six sets of MIM and OTFT structures that, with the exception of one step, were fabricated side by side. This was done to study the effect of a single parameter, for example pentacene purity or pentacene, gold, and phosphonic acid evaporation rates. Often, one transistor sample in the series was fabricated according to the previously tested recipe and used to confirm the run-to-run repeatability of the fabrication process. Each set had several OTFT and MIM structures.

3.7.1 Optimization of pentacene layer

The effect of pentacene purity and its evaporation rate on OTFT performance was evaluated. This experiment incorporated the OTFT electrical measurements and AFM surface images of pentacene. From these preliminary experiments the pentacene evaporation rate was chosen for further transistor fabrication.

3.7.2 Optimization of source/drain and gate contacts

Initially, one transistor series was fabricated to pre-optimize the interface between pentacene and the source/drain contacts by varying the gold deposition rate from 0.3 to 30 Å/s. The OTFT source/drain contact and channel resistances were extracted as functions of the gold evaporation rate and compared to field-effect mobilities. Also, AFM images of gold deposited at different deposition rates were obtained.

In the next series, the surface roughness of aluminium oxide was studied as a function of aluminium evaporation rate and UV/ozone exposure time.

The optimization of the gate and source/drain electrodes and semiconductor layer was done prior to the optimization of vacuum-grown C_8PA monolayer and is discussed in detail in Chapter 4. In the final stages of the transistor optimization process another pentacene optimization was performed. In this case the pentacene deposition temperature was varied between 55 to 80°C and the results are presented in Chapter 7.

3.7.3 Optimization of n-octylphosphonic acid (C_8PA) monolayer

The first experiment was conducted to confirm the chemisorption of C_8PA on AlO_x. At the same time, the effect of post-deposition annealing was investigated. Further experiments were related to optimization of C_8PA SAM growth, namely the deposition temperature and deposition rate. AFM, WCA, FTIR, and electrical measurements were performed. C_8PA thickness is ~1 nm for the majority of the C_8PA preparation conditions, but variation in the electrical properties of OTFT and MIM structures, as well as differences in the structural and surface properties of AlO_x/C_8PA were observed. The following three experiments aimed to optimize the C_8PA monolayer growth.

3.7.3.1 C_8PA desorption/post-annealing

~10-nm-thick C_8PA layer was deposited at the rate of 3 Å/s at room temperature. Afterwards, the substrate temperature was set to 160°C to remove the

physisorbed molecules. The desorption/annealing time was varied from 25 to 210 minutes. The details of the experiment and the experimental findings are presented in Chapter 5.The experiment confirmed the chemisorption of n-octylphosphonic acid to the aluminium oxide.

3.7.3.2 C_8PA growth temperature

~10-nm-thick C_8PA layer was deposited at the rate of 3 Å/s at various substrate temperatures. The minimum and maximum temperature was 25°C and 150°C, respectively. Post-deposition annealing was performed at 160°C for 180 minutes on all samples. Chapter 6 explains the objective and the results of the experiment.

3.7.3.3 C_8PA deposition rate

~10-nm-thick C_8PA layer was deposited at various rates (0.3, 1, 3, and 10 Å/s). The post-deposition annealing was the same as in the previous experiment. Chapter 8 presents the details and results of the experiment.

The results of the transistor bias-stress are discussed in Chapter 9. Finally, the reader should be reminded that only one preparation parameter was varied in each experiment. Consequently, the preparation of the gate electrode, AlO_x dielectric, pentacene and Au source/drain contacts was the same within the given experiment.

3.8 Summary

This chapter presented the fabrication of OTFT, MIM and supporting structures and explained in detail the electrical, surface and structural measurements

performed on them. The parameters extracted from these measurements constitute a widely accepted standard in the material and device characterization research community. The novelty of this thesis is the introduction of Eqs. (3.6) – (3.8) employed in the evaluation of bias-stress induced transistor degradation.

Chapter 4

OTFT: Optimization of contacts and pentacene growth

Improvement in OTFT performance requires optimization of all layers. In this chapter the experimental details and results of semiconductor, source/drain contact and aluminium oxide optimization are presented. The optimization of the C_8PA monolayer is discussed in the following chapters.

The effect of pentacene purity and its evaporation rate on transistor performance is presented in Section 4.1. In this case pentacene was deposited at room temperature. The gold evaporation rate was studied with the aim to improve the interface properties between pentacene and the Au source/drain contacts. This study

is included in Section 4.2. A brief optimization of aluminium oxide with respect to its surface roughness is presented in Section 4.3.

4.1 Optimization of pentacene growth

The electrical conductivity of organic semiconductors depends on the molecular stacking and, consequently, on the semiconductor layer growth. The growth of pentacene is affected by the semiconductor thickness [51], underlying dielectric [22], substrate temperature [27], etc. Impurities and defect states in pentacene also lead to lower field-effect mobility [52]. For example, impurities present in pentacene did not change the crystalline quality but accumulation of impurities at pentacene grain boundaries affected the charge transport [53, 54] and lowered the field-effect mobility.

Here, three factors affecting the pentacene growth were studied: pentacene purity, its deposition rate and deposition temperature. The first two factors are presented in this chapter and the last one in Chapter 7. Pentacene of two different purities was deposited at the rates of 0.02, 0.05, 0.08, 0.16, 0.24, and 0.32 Å/s at room temperature. The initial transistor sets aimed to pre-optimize the pentacene growth, while keeping all other fabrication parameters the same. Three- and four-time purified pentacene was evaporated at room temperature at various rates.

Pentacene was purchased from two suppliers. One-time purified pentacene was purchased from Tokyo Chemical Industry (TCI) and three-time purified pentacene from Sigma-Aldrich. In-house sublimation purification of one-time purified pentacene was performed in a three-zone tube furnace at a pressure of ~ $1x10^{-5}$ mBar. During each sublimation step the temperature window of the pentacene

sublimation process was controlled, i.e. the species with sublimation temperature lower than T_1 and higher than T_2 ($T_1 < T_2$) were removed from the pentacene source material. The three-time purified pentacene from Sigma-Aldrich is denoted as '3x' and the four-time purified pentacene as '4x' (pentacene from TCI underwent in-house purification three times).

4.1.1 Device fabrication

Two sets of six samples corresponding to different pentacene purity and evaporation rate were prepared. The total thickness of the gate dielectric was ~20 nm (~19 nm of AlO_x and ~1 nm of C_8PA) in all samples [44], corresponding to capacitance of ~0.28 $\mu F/cm^2$, breakdown voltage of ~10 V and a gate leakage current density less than 1×10^{-7} A/cm^2. Pentacene was separately deposited on each sample, while all other transistor layers were prepared side by side. Both the three- (3x) and four-time (4x) purified pentacene were thermally evaporated at rates of 0.02, 0.05, 0.08, 0.16, 0.24, and 0.32 Å/s. The thickness of the pentacene layer was 50 nm and the depositions were performed at room temperature.

4.1.2 Results: OTFTs

Transistor parameters such as the threshold voltage, field-effect mobility, off-current, subthreshold slope, and on/off current ratio for OTFTs with 3x and 4x-pentacene were extracted from the transfer characteristics. The channel and contact resistances of OTFTs with 4x-pentacene were calculated. AFM surface topography of 4x-pentacene was also obtained as a function of pentacene evaporation rate. These experimental results are presented next.

4.1.2.1 Threshold voltage and field-effect mobility

The average threshold voltage for both pentacene purities is shown in Figure 4.1(a). The variation in the threshold voltage with pentacene evaporation rate is relatively small for 4x-pentacene while a larger variation was observed for 3x-pentacene. Since the primary factor affecting the threshold voltage is the gate dielectric, which is the same in all transistors, one would not expect large variations. Nevertheless, larger variation is observed for 3x-pentacene.

Figure 4.1(b) shows the mean values and the standard deviations of the field-effect mobilities. The field-effect mobility increases with increasing evaporation rate for OTFTs with 4x-pentacene. The field-effect mobility of the transistors with 3x-pentacene exhibits a maximum at the evaporation rate of ~0.24 Å/s. Four-time purified pentacene resulted in higher mobility overall, if compared to three-time purified pentacene. When the pentacene evaporation rate rose from 0.02 Å/s to 0.32 Å/s, the field-effect mobility increased by a factor of three.

4.1.2.2 Off-current and on/off current ratio

The average value of the off-current is shown in Figure 4.1(c). The off-current is almost the same for all OTFTs with 4x-pentacene, although a slight decrease in the off-current is seen with increasing evaporation rate. On the other hand, OTFTs with 3x-pentacene exhibit larger variation in off-current. Also, their off-current is slightly higher than that of OTFTs with 4x-pentacene.

On/off current ratio of OTFTs with channel length of 30 μm and channel width of 1000 μm is shown in Figure 4.1(d). Here, the on-current is the current at $V_{DS} = V_{GS} = -3.0$ V. For all evaporation rates, the current ratio is higher when 4x-

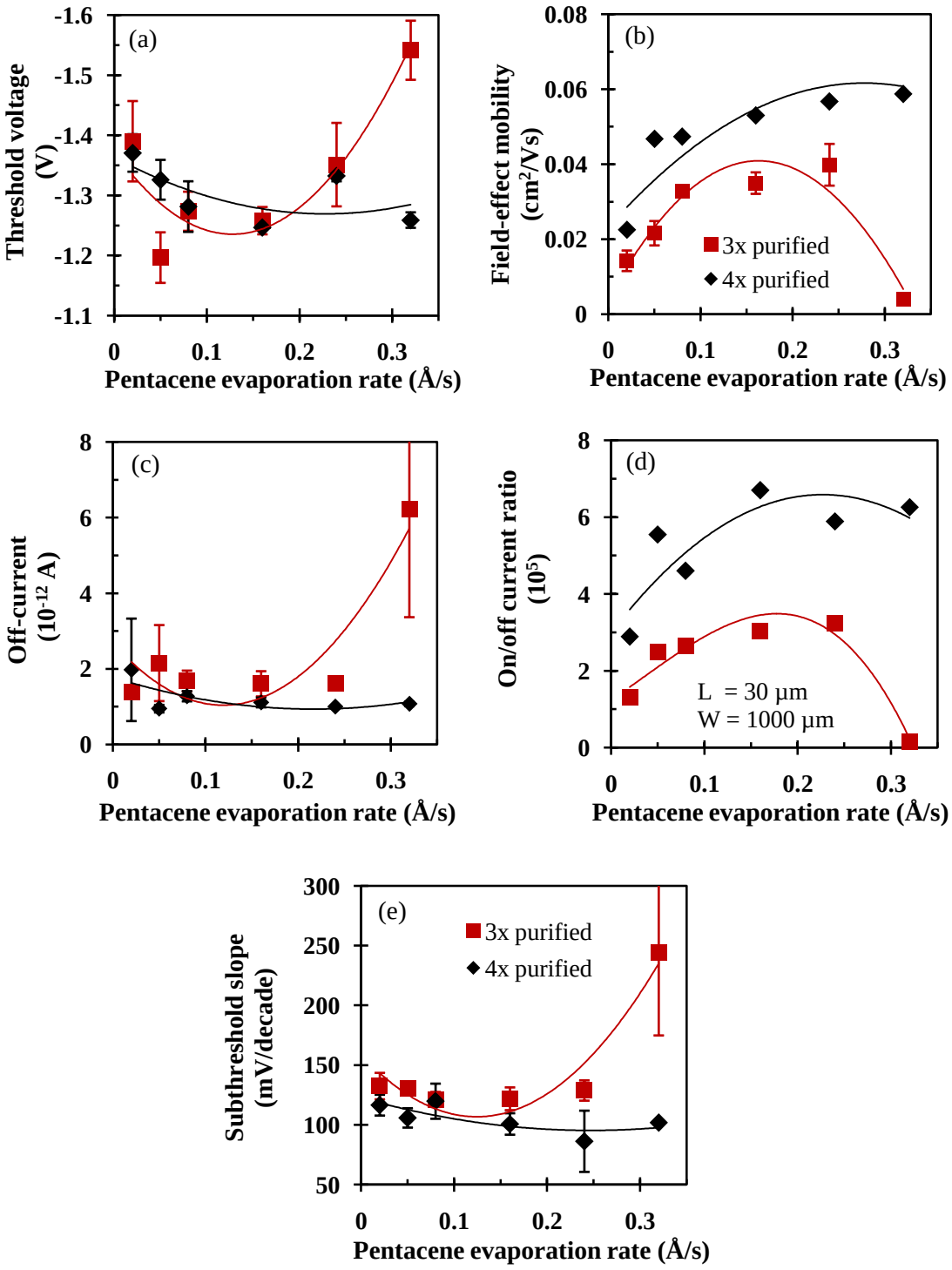

Figure 4.1: OTFT threshold voltage (a), field-effect mobility (b), off-current (c), on/off current ratio (d), and subthreshold slope (e) as functions of pentacene purity and evaporation rate.

pentacene is used, reaching a value of ~6×10^5 for higher rates. For OTFTs with 4x-pentacene the current ratio does not change for evaporation rates higher than 0.16 Å/s.

4.1.2.3 Subthreshold slope

The subthreshold slopes of all OTFTs are shown in Figure 4.1(e). The subthreshold slope is lower for OTFTs with four-time purified pentacene, with values of ~100 mV/decade. With the exception of the highest evaporation rate, the subthreshold slope of OTFTs with 3x-pentacene is ~130 mV/decade. The lower value of subthreshold slope is an indication of reduced dielectric/semiconductor interface trap density.

4.1.2.4 AFM of four-time purified pentacene

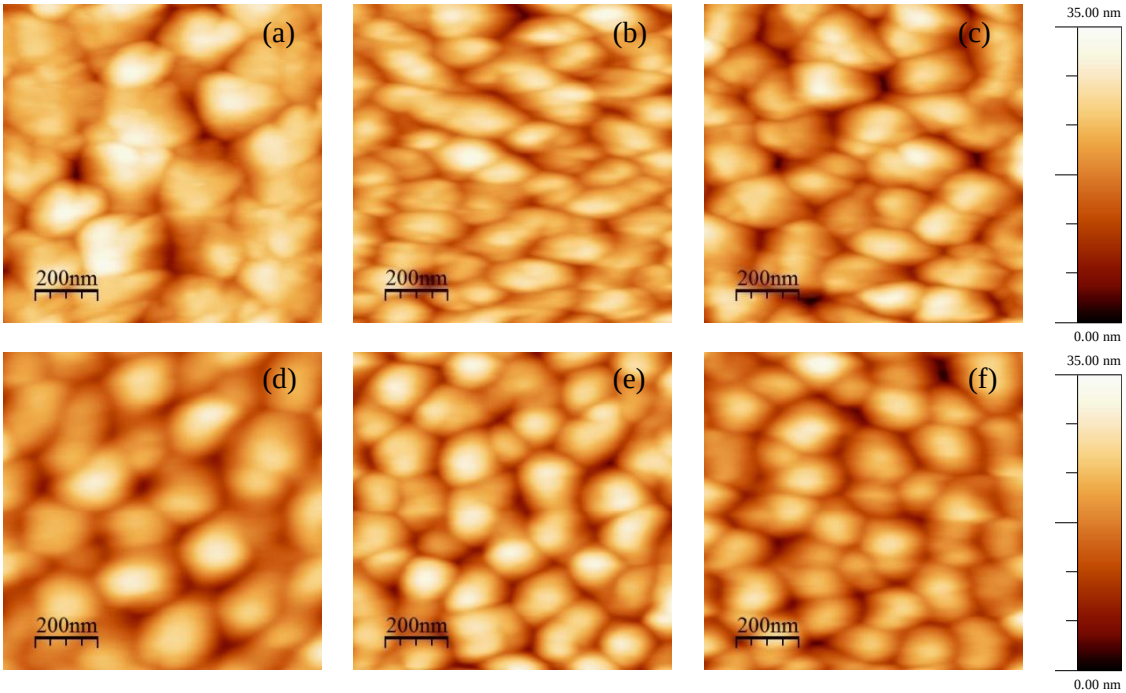

Figure 4.2: AFM surface images of four-time purified pentacene deposited at a rate of 0.02 (a), 0.05 (b), 0.08 (c), 0.16 (d), 0.24 (e), and 0.32 Å/s (f).

As seen in the previous sections, the OTFTs with 4x-pentacene exhibit better overall performance. Next, AFM height images of 4x-pentacene deposited at rates of 0.02, 0.05, 0.08, 0.16, 0.24, and 0.32 Å/s are shown in Figure 4.2(a)-(f). It is observed that the pentacene grains contain fewer sub-grains and become more tightly connected at higher evaporation rates, even though the overall grain size is reduced.

4.1.2.5 Channel and contact resistances of OTFTs with four-time purified pentacene

The effect of pentacene evaporation rate on the channel and contact resistance of OTFTs with four-time purified pentacene is shown in Figure 4.3. The channel width is 1000 µm and lengths are between 25 and 90 µm. The channel resistance per unit channel length is lower for evaporation rates between 0.08 and 0.32 Å/s. The contact resistance is independent of pentacene evaporation rate.

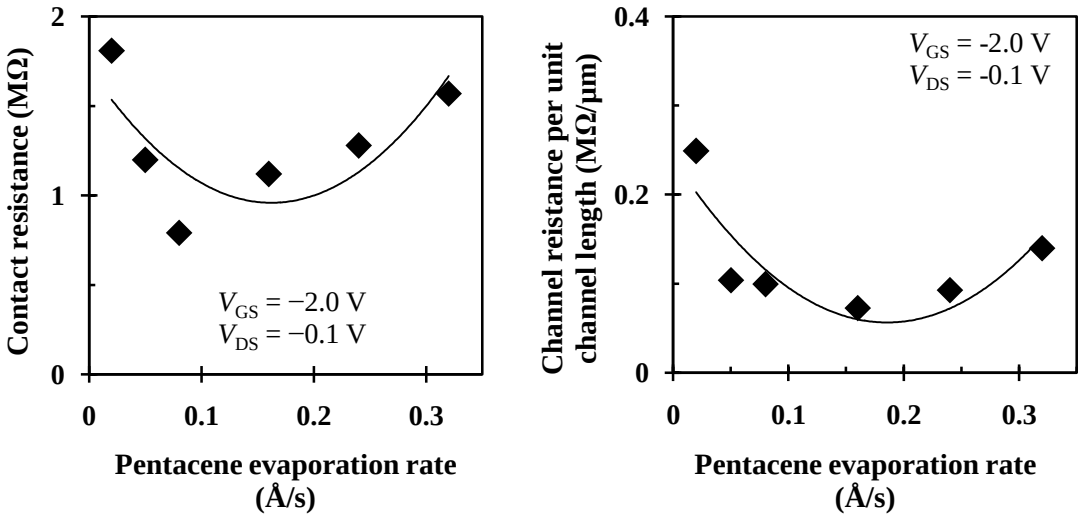

Figure 4.3: Contact and channel resistances of four-time purified pentacene as functions of pentacene evaporation rate.

4.1.3 Summary: pentacene evaporation rate and purity

The OTFTs containing four-time purified pentacene exhibit the highest field-effect mobility of ~0.06 cm^2/Vs at the highest pentacene evaporation rate of 0.32 Å/s. Along with improvement in the field-effect mobility, the off-current and subthreshold slope are also lowered when four-time purified pentacene is used, indicating an improved semiconductor/dielectric interface.

AFM images of four-time purified pentacene deposited at different rates reveal tighter connection between grains and less sub-grain structure for higher evaporation rates, even though the actual grain size becomes smaller. According to Shtein *et al.* [55], the electrical conductivity increases with improved physical contact between the pentacene grains. Knipp *et al.* [56] and Hill et al. [41] also showed that the pentacene grain size is not a unique indicator of electronic properties. In their OTFTs with octadecyltrichlorosilane SAM and pentacene, they observed higher field-effect mobility in transistors with SAM even though the inclusion of SAM led to pentacene with smaller grain size [57]. Also, Acton et al. [14] found that smaller grains (~150-350 nm) with improved inter-grain contact result in higher mobility than larger dendritic grains (~800 nm) with inter-grain voids acting as scattering centres.

Yang et al. [58] suggested tighter packing between pentacene grains as more pentacene was deposited on the existing pentacene molecules. Also, Rao et al. [59] suggested that lack of interconnectivity between pentacene grains at lower evaporation rate caused decrease in the mobility. The results presented in this section are consistent with these previous observations.

The inverse subthreshold slope of ~100 mV/decade for OTFTs with 4x-pentacene is similar to that achieved by Halik *et al.* [40] and Klauk *et al.* [46]. This value indicates lower trap density at the semiconductor/dielectric interface with increased pentacene purity. The channel and contact resistances of OTFTs with four-time purified pentacene are comparable to Klauk *et al.* [46]. The channel resistance becomes lower at higher pentacene evaporation rates, indicating better pentacene polycrystalline morphology and possibly improved dielectric/semiconductor interface.

Similar dependence of the transistor field-effect mobility at lower pentacene evaporation rates for 3x- and 4x-pentacene, but the overall higher field-effect mobilities in the OTFTs with 4x-pentacene, indicate improved pentacene purity and suitable pentacene purification procedure. Further increase in the OTFT field-effect mobility at pentacene rate of 0.32 Å/s for the 4x-pentacene, accompanied by increased temperature of the pentacene evaporation source, indicates that the purification reduced impurities with higher sublimation temperature. Further, fifth purification step did not lead to a measurable improvement in the OTFT performance.

4.2 Optimization of Au source/drain contacts

The selection of the source/drain contact material and its deposition affects the OTFT performance by controlling the charge injection from the source into the channel as well as the charge extraction at the drain. It has been shown that the gold evaporation rate [16, 60, 61] and the substrate temperature during gold deposition [62] affect the source/drain contacts and, consequently, the OTFT performance. Gold

contacts also depend on the selected method of deposition, e.g. e-beam, thermal evaporation, or sputtering.

The effect of gold evaporation rate on the OTFT performance was examined. Source/drain gold contacts were thermally evaporated at rates of 0.3, 3, and 30 Å/s; all other transistor layers were identical.

4.2.1 Device fabrication

One sample was prepared for each Au evaporation rate. In top-contact OTFTs, the source/drain contacts are the top most transistor layer deposited on pentacene. With the exception of the Au evaporation, all samples were prepared side by side. The gate dielectric capacitance of AlO_x/C_8PA was 0.4 μF/cm^2. 50-nm-thick 4x-pentacene was deposited at evaporation rate of 0.24 Å/s at room temperature. Finally, 50-nm-thick Au source/drain contacts were evaporated at rates of 0.3, 3, and 30 Å/s.

4.2.2 Results: OTFTs

Transistors with various channel lengths have been measured and the channel resistance per unit channel length and contact resistance were extracted using the procedure described in section 3.4.1.3.

4.2.2.1 Channel and contact resistance

The channel resistance per unit channel length and contact resistance for three gold evaporation rates is shown in Figure 4.4(a) and (b), respectively. As expected, the channel resistance does not change with increasing gold evaporation rate. On the

other hand, the contact resistance is lowered by a factor of ~2 at lower V_{GS} when the gold evaporation rate rises from 0.3 to 3 Å/s. Both resistances are lowered at higher gate-to-source voltages. The value of contact resistance for Au evaporated at 3 Å/s is similar to that obtained in Figure 4.3(a). This shows the reproducibility of the transistor fabrication process with respect to the source/drain contact formation.

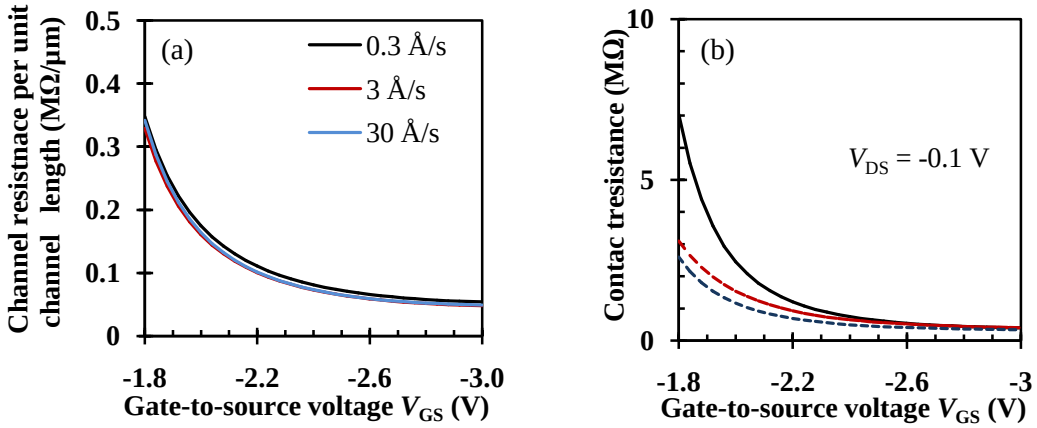

Figure 4.4: OTFT channel resistance (a) and contact resistance (b) as functions of gate-to-source voltage for various gold evaporation rates.

4.2.2.2 Field-effect mobility

The mean and standard deviation of the field-effect mobility as a function of gold evaporation rate is shown in Figure 4.5. The higher evaporation rate leads to higher mobility. The lower contact resistance at higher Au evaporation rate indicates improved charge injection/extraction to/from the channel that results in larger field-effect mobility.

4.2.2.3 Gold and pentacene morphology

To understand the effect of gold evaporation rate, Au surface topography was studied using AFM. AFM images of the Au surface for evaporation rate of 0.3, 3,

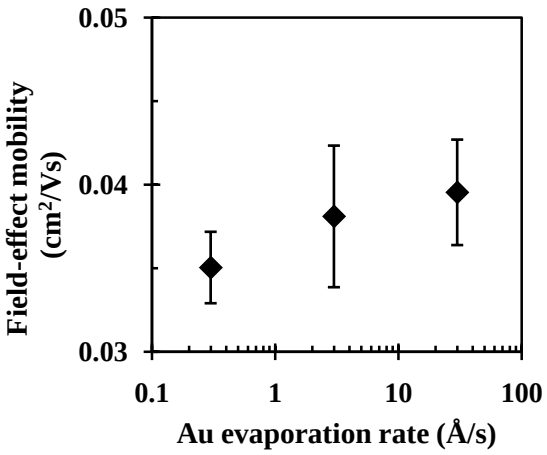

Figure 4.5: OTFT field-effect mobility as a function of Au evaporation rate.

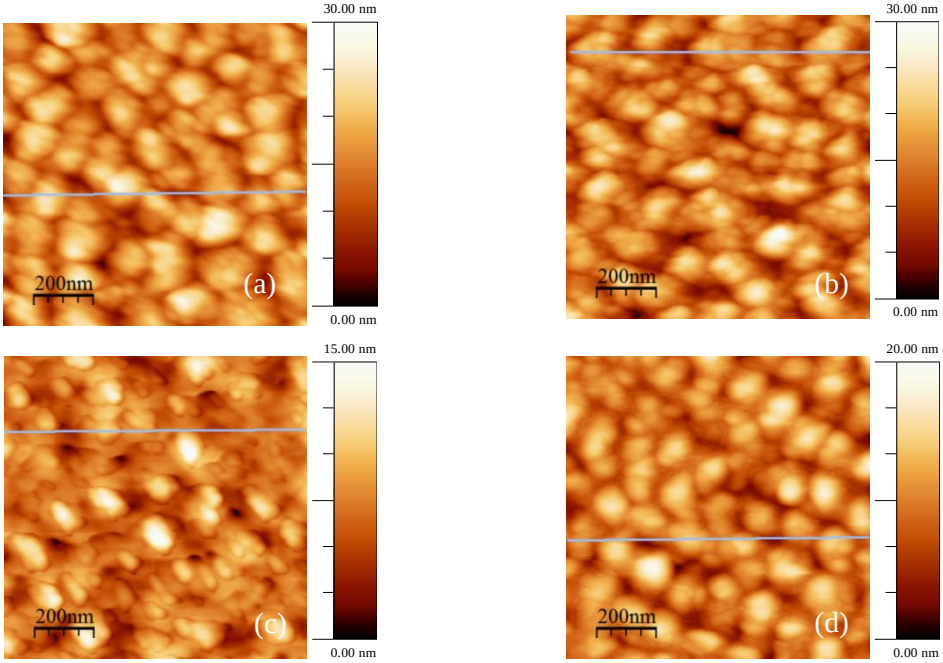

Figure 4.6: AFM images of Au source/drain contacts evaporated at rate of 0.3 (a), 3 (b), and 30 Å/s (c). Reference image of pentacene is shown in (d). The bluish lines indicate individual traces shown in Figure 4.7.

and 30 Å/s are shown in Figure 4.6(a)-(c). The corresponding pentacene surface is shown in Figure 4.6(d). For lower evaporation rates, Au surface topography resembles that of pentacene while at the highest rate different features appear.

Figure 4.7 shows one-dimensional height profiles of surfaces shown in Figure 4.6. The trace shown in Figure 4.7(a)-(c) corresponds to Au evaporated at rate of 0.3, 3, and 30 Å/s, respectively; and the trace in Figure 4.7(d) to bare pentacene. The peak-to-valley difference is around 16, 12, and 8 nm for gold evaporation rates of 0.3, 3, and 30 Å/s, respectively, while it is ~12 nm for pentacene.

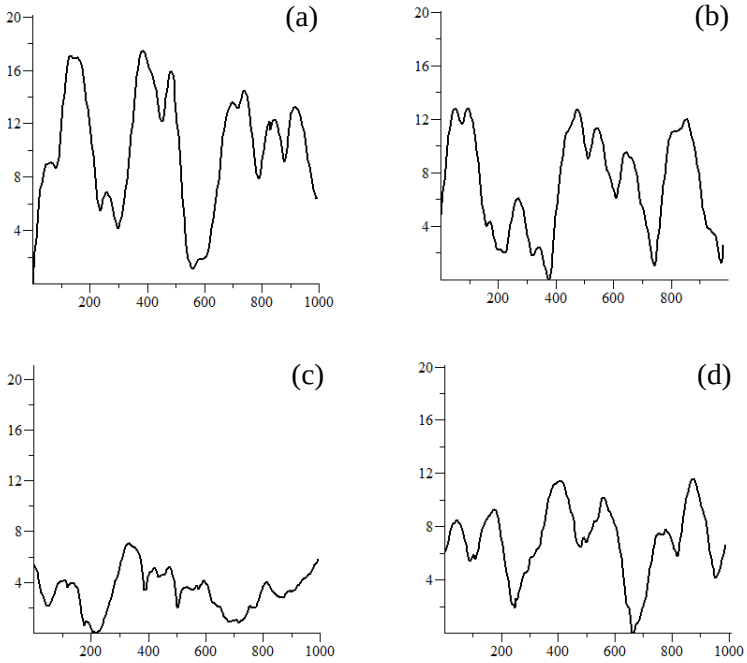

Figure 4.7: Surface profile of Au /pentacene with Au evaporated at 0.3 (a), 3 (b), and 30 Å/s (c). The profile of pentacene is in (d). Both x and y-axes have scales in nm.

4.2.3 Summary: Au evaporation rate

Park et al. [61] observed that Au atoms are tightly bound to each other at higher evaporation rate. They also concluded that the gold does not 'penetrate' into pentacene at any evaporation rate when thermal evaporation process is used. It was observed that the Au surface copies that of the underlying pentacene for lower evaporation rate, a finding similar to that of Park et al. [61] who varied the Au

evaporation rate up to 15 Å/s. However, different surface image was obtained for Au evaporated at rate of 30 Å/s.

The increase in the Au evaporation rate from 0.3 to 3 Å/s leads to a measurable decrease in the contact resistance, while a further increase in the evaporation rate by an order of magnitude provides negligible benefit. The reduction in the contact resistance with increasing Au evaporation rate was also observed by Zhang et al. [16], Cho et al. [60], and Park et al. [61]. The contact resistance values obtained at Au evaporation rates of 3 and 30 Å/s are similar to those obtained by Zhang et al. [16]. Also, according to Zhang et al. [16], pentacene film can be damaged due to high flux of Au atoms during deposition in e-beam evaporation system. Consequently, for our future OTFTs, the moderate evaporation rate of 3 Å/s was selected.

The total channel resistance is proportional to the channel length, while the contact resistance is independent of it. Hence, at very low Au evaporation rate, the contact resistance can be higher than the total channel resistance for OTFTs with short channel length (L< 30 μm). Klauk et al. [63] showed that in such a case, the OTFT performance is dependent on the contacts instead of the intrinsic carrier mobility of the organic semiconductor, which is not desirable.

4.3 Surface roughness of Al gate electrode

Hydrophilic AlO_x is functionalized with a monolayer of n-octylphosphonic acid (C_8PA) that renders its surface hydrophobic. The total length of C_8PA molecule is ~1.2 nm. Hence, the surface roughness of the aluminium oxide was studied and minimized to promote good alignment of C_8PA molecules.

Aluminium gate electrode is prepared by thermal evaporation of aluminium. The effect of the evaporation rate on aluminium surface roughness was studied for rates of 0.3, 3, and 10 Å/s. The thickness of deposited aluminium is ~20 nm. The mean and standard deviation of surface roughness of aluminium were calculated from several AFM images of 1×1 μm^2 area.

Figure 4.8 shows the Al RMS surface roughness as function of the evaporation rate. The average surface roughness was 1.13, 0.68, and 0.69 nm at the evaporation rate of 0.3, 3, and 10 Å/s, respectively.

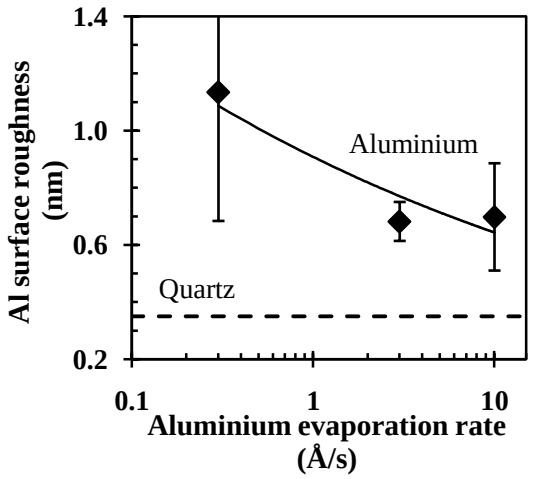

Figure 4.8: Surface roughness of aluminium as function of aluminium evaporation rate. The surface roughness of quartz substrate is shown as dashed line.

4.3.1 Summary: aluminium surface roughness

The evaporation rate of 3-4 Å/s was used in all future experiments. The part of Al gate electrode was oxidized to convert Al into AlO_x. Previously, the effect of UV/ozone exposure time on AlO_x thickness and threshold voltage were investigated [44]. It was observed that the increase in UV/ozone exposure time from 5 to 60 minutes lowered the OTFT threshold voltage and the 60-minute UV/ozone exposure

of Al led to formation of ~7 nm thick AlO_x. This step was kept identical in all experiments.

Since oxidation is a self-limiting process, increasing the oxidation time beyond one hour does not lead to appreciable increase in the oxide thickness. Therefore, if required, the oxide thickness is increased by evaporating additional ultrathin Al layer (1.5 nm) and its subsequent oxidation using UV/ozone treatment. This leads to increase in AlO_x thickness by ~2 nm. It has been shown previously that this step can be repeated up to 6 times while leading to good MIM and OTFT performance [44]. Hence, the overall thickness of AlO_x could range from ~9 to ~19 nm, depending on the number of the 1.5-nm-thick Al layers. Nevertheless, the OTFTs presented in the next chapters contain 9-nm-thick AlO_x.

AFM image of AlO_x prepared by this optimized fabrication method is shown in Figure 5.3(a) and its RMS surface roughness is 0.45 nm. The low surface roughness of AlO_x is required for obtaining proper alignment of self-assembled C_8PA molecules.

4.4 Conclusion

Higher pentacene purity leads to OTFTs with improved field-effect mobility. The maximum mobility of ~0.06 cm^2/Vs was achieved at the highest pentacene evaporation rates of 0.24–0.32 Å/s when using four-time purified pentacene. The lowest threshold voltage of ~–1.25 V and subthreshold slope of ~100 mV/decade were also obtained for OTFTs with four-time purified pentacene. The AFM surface images of four-time purified pentacene indicate that although the higher evaporation

rate leads to smaller pentacene grain size, the grains exhibit less sub-grain structure and tighter packing.

As expected, the channel resistance does not change with increasing gold evaporation rate, indicating that the properties of the semiconductor/dielectric interface do not change. An increase in gold evaporation rate from 0.3 to 3 Å/s lowers the contact resistance by a factor of ~2 and further increase in the rate to 30 Å/s provides additional negligible reduction. The increase in the field-effect mobility is also very minor. Overall, lower contact resistance and higher field-effect mobility are achieved at higher Au evaporation rate, indicating improved charge carrier injection/extraction.

Based on these findings, all future transistors implement four-time purified pentacene evaporated at a rate of 0.24 Å/s and Au source/drain contacts evaporated at a rate of 3 Å/s.

The growth of pentacene and the source/drain contacts was pre-optimized before the optimization of C_8PA monolayer proceeded. Along with the optimization of these layers, the overall dielectric thickness was reduced from 20 nm (Section 4.1) to ~11.5 nm (Section 4.2) by reducing the number of 1.5-nm-thick aluminium layers (described in Section 4.3.1). In both cases the OTFTs operate within 3 V and therefore, in the future OTFTs the thickness of the gate dielectric was reduced to 10 nm and the transistors were examined at 2 V.

Chapter 5

Vacuum vapour-phase self-assembly of C_8PA

In the previous chapter, the pre-optimization of all transistor layers other than C_8PA was discussed. In this chapter, the vacuum vapour-phase growth of n-octylphosphonic acid monolayer is presented. Section 5.1 briefly describes the steps involved in C_8PA monolayer growth on top of AlO_x. Section 5.2 discusses the preparation of samples for material and electrical characterization that involve AlO_x functionalized with C_8PA. Results from the material characterization are included in Section 5.3. The results of electrical measurements conducted on MIM and OTFT structures are presented in Sections 5.4 and 5.5, respectively. Section 5.6 discusses the experimental findings that confirm the presence of C_8PA on AlO_x. In addition, the effect of C_8PA desorption/annealing time on the dielectric properties and OTFT performance is analysed. Finally, Section 5.7 concludes this chapter.

5.1 Introduction

Monolayers based on alkyl phosphonic acids can be assembled on aluminium oxide [42, 64–66], hafnium oxide [67], nitinol [68], gallium nitride [69, 70], and titanium oxide [71]. Alkyl phosphonic acid molecules can be divided into two parts: head (anchor) group and the aliphatic tail. The head group is chemisorbed on a substrate while the tail group reacts with the outer film. The chemical structure of n-octylphosphonic acid (C_8PA) showing the head group and tail is presented in Figure 5.1.

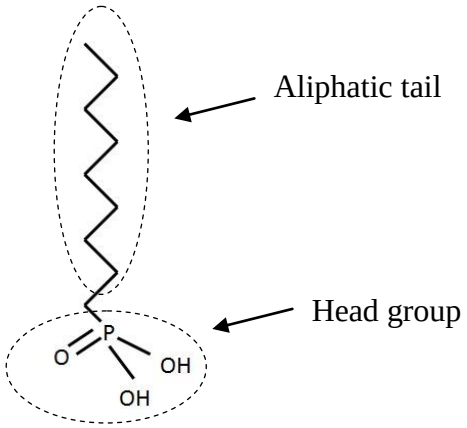

Figure 5.1: Chemical structure of n-octylphosphonic acid (C_8PA).

To date self-assembled monolayers based on alkyl phosphonic acids [11, 14, 18, 32, 37] have been obtained by solution process only. In such a case chemisorption of alkyl phosphonic acid molecules on the surface of AlO_x has been demonstrated. An alternate approach using vacuum vapour-phase self-assembly of C_8PA is presented in this chapter. The experiment aimed to explore whether vapour-phase growth in vacuum would also lead to the chemisorption of C_8PA molecules to AlO_x. The monolayer self-assembly consists of thermal evaporation of approximately 10-nm-thick (~9 monolayers) C_8PA layer followed by a thermal

desorption of the physisorbed C_8PA molecules at a pressure of $<10^{-6}$ mbar and temperature of 160°C. Taking into account the temperature profile of the heated sample, ~30 minutes of heating would be needed to re-evaporate the whole 10-nm-thick C_8PA layer if no chemisorption occurred. Consequently, after the 25-minute desorption some C_8PA molecules might be still present, while longer desorption should result in the removal of the whole layer. However, if chemical bonding between C_8PA molecules and AlO_x surface occurs, then the substrate temperature of 160°C would not be high enough to break these bonds. Therefore, post-growth desorption times of 25, 60, 90, and 210minutes were selected. Comprehensive electrical and material characterization confirmed the presence of C_8PA on the surface of AlO_x for all desorption times. In addition, an understanding of the properties of AlO_x functionalized with C_8PA and the effect of C_8PA desorption/annealing time on OTFT performance was developed.

5.2 Sample/device fabrication

AlO_x and AlO_x/C_8PA samples for surface and structural characterization and corresponding MIM and OTFT devices were fabricated. The cross-section of the OTFT is shown in Figure 3.1. The procedure for the fabrication of MIM and OTFT devices is described in Section 3.1.

First of all, a layer of ~9 nm-thick aluminium oxide was prepared on glass using UV/ozone oxidation. The optimized method of AlO_x preparation is presented in Section 4.3. Some samples for material characterization were used as reference with no further C_8PA layer deposition. The remaining samples followed with the growth of C_8PA.

10-nm-thick C_8PA layer was deposited on top of AlO_x at room temperature and afterwards the substrate temperature was set to 160°C for 25, 60, 90, and 210 minutes. This completed the samples for material characterization, while semiconductor and metal layers were required to complete the devices. Pentacene and gold were deposited using the pre-optimized parameters described in Chapter 4. Since the MIM and transistor structures were fabricated side by side, the MIM structures were masked during the pentacene evaporation.

5.3 Results: surface and structural properties

WCA and AFM measurements were employed to measure the AlO_x and AlO_x/C_8PA surface properties, while their structural properties were measured by FTIR.

5.3.1 WCA

WCA of aluminium oxide is shown in Figure 5.2(a). AlO_x surface is hydrophilic with a contact angle of 46.6°±0.2°. As-deposited C_8PA surface (shown in Figure 5.2(b)) is hydrophobic with a contact angle of 101.5°±0.3°. Figure 5.2 (c) and (d) present the contact angle measurement of C_8PA desorbed for 25 and 210 minutes, respectively. The angle value is slightly increased when the desorption time is increased from 25 to 210 minutes, leading to a WCA of 107.4°± 0.5° for the latter.

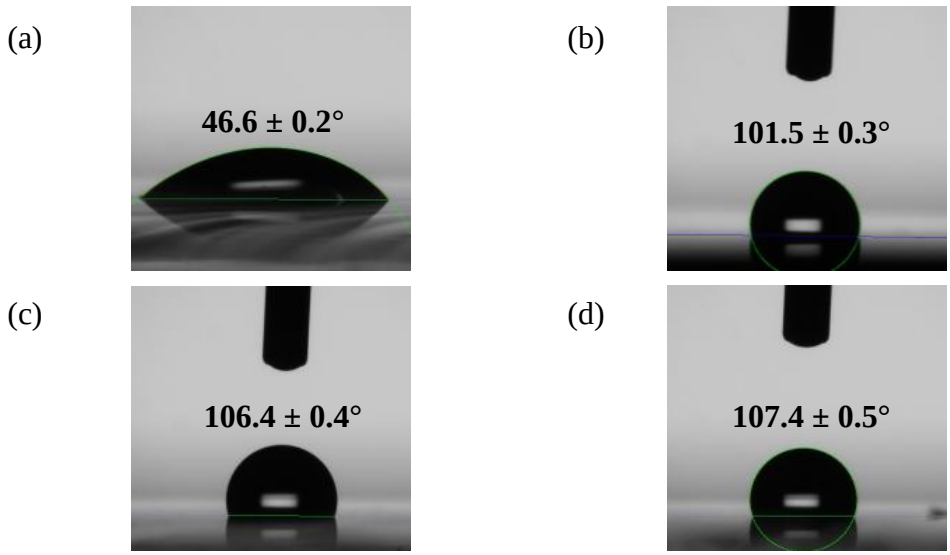

Figure 5.2: Water contact angle of bare AlO_x (a); C_8PA in its as-deposited state (b), and after 25-minute (c) and 210-minute (d) desorptions.

5.3.2 AFM

Figure 5.3(a) shows AFM image of AlO_x surface with average RMS surface roughness of 0.45 nm. Figure 5.3(b) shows AFM image of C_8PA surface immediately after deposition, while Figure 5.3(c) and (d) depict the C_8PA surface after a 25- and 210-minute desorption, respectively.

As-deposited C_8PA exhibits very high RMS surface roughness of 4.5 nm. RMS roughness of 0.48 and 0.36 nm is achieved for AlO_x/C_8PA surface after the 25- and 210-minute desorption, respectively. The RMS roughness after 25minutes is similar to that of bare AlO_x, while it is slightly lower after 210minutes. One could also notice similar features on the surface of bare AlO_x and the surface of C_8PA after the 210-minute desorption. The similar topography of AlO_x with and without phosphonic acid monolayer was also observed in the solution self-assembly [42].

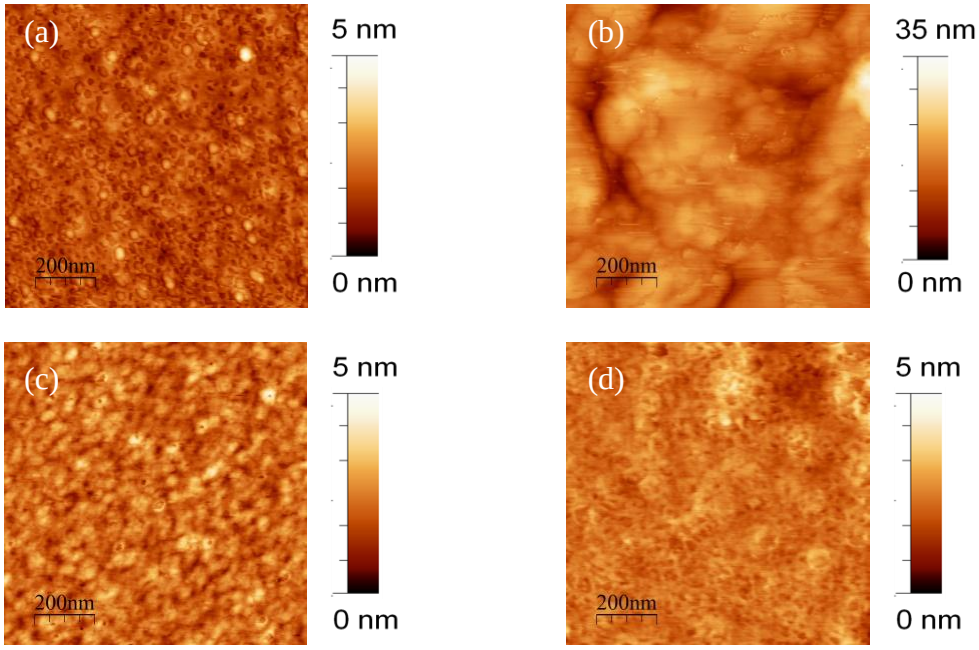

Figure 5.3: AFM surface images of bare AlO_x (a); and C_8PA immediately after deposition (b), and after 25-minute (c) and 210-minute (d) desorptions.

5.3.3 FTIR

Figure 5.4 shows the relevant sections of the FTIR spectra of C_8PA/AlO_x bi-layers with C_8PA annealed to 160°C for 25, 90, and 210 minutes, as well as the reference non-annealed AlO_x layer.

Figure 5.4(a) depicts a broad absorption band at ~1110 cm^{-1} associated with Al–O–P stretch mode resulting from the phosphonate head group bonded to the surface of aluminium oxide [72]. The band is centred near 1110 cm^{-1} and it is shifted to slightly higher wave numbers for C_8PA annealed for 25 minutes when compared to that annealed for 90/210 minutes. The integral intensity of the peak is reduced between 25 and 90 minutes and then slightly increased after the 210-minute annealing. In addition, the right shoulder of the peak (near 1150 cm^{-1}) is reduced with the increasing annealing time.

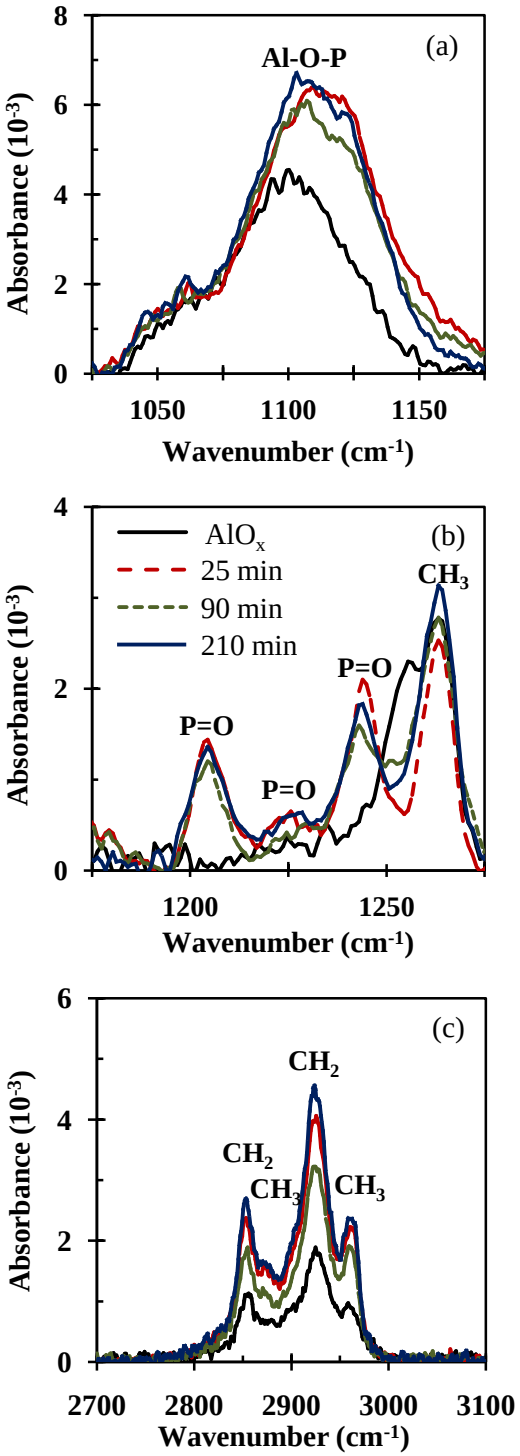

Figure 5.4: Sections of FTIR spectra of AlO_x/C_8PA bi-layer with C_8PA desorbed for various times. AlO_x reference layer is shown as well.

The reference AlO_x sample exhibits a peak located near 1100 cm^{-1}, associated with the Al–OH groups [73], that overlaps with the band of the phosphonate salts. The absorbance of this band is decreased and shifted to higher wavenumber when the AlO_x is annealed for 3 hours (see Section 6.3.3). Consequently, the reduction in the integral intensity of the 1110 cm^{-1} band between 25- and 90-minute anneals may be associated with the reduction in the Al–OH mode, while the increase in the integral intensity of this band between 90- and 210-minute anneals is associated with C_8PA monolayer.

Figure 5.4(b) shows the vibrations of the P=O bond of C_8PA at ~1204, 1226, and 1244 cm^{-1} [74] and a vibration at 1263 cm^{-1} assigned to the methyl group. In addition, the reference AlO_x sample exhibits a vibration at 1255 cm^{-1} that is not observed after the 3-hour annealing (Section 6.3.3). The amplitude of the P=O vibrations is reduced between 25- and 90-minute annealing and then slightly increased after the 210-minute annealing. Vibrations in the region of 2500-2800 cm^{-1} and 2200-2400 cm^{-1} associated with the P–OH groups of C_8PA [74] are not observed irrespective of the annealing time.

Absorbance peaks in the region of 2800–3000 cm^{-1} shown in Figure 5.4(c) correspond to the symmetric/asymmetric stretching modes of CH_2/CH_3 groups. The centre of the symmetric and asymmetric CH_2 stretching mode is located at ~ 2853 $cm^{-1}$and 2925 cm^{-1}, respectively. These values are similar to those reported for C_8PA monolayers assembled from solutions [43]. Since the C_8PA molecules are attached to the AlO_x surface and thus immobilized, changes in these peak positions with desorption/annealing are unlikely. On the other hand, changes in the molecular alignment are possible because C_8PA source material readily evaporates at the

temperature of 160°C. The increase in desorption time from 25 to 90 minutes increases the full width at half maximum (FWHM) of CH_2 stretching modes by 1-2 cm^{-1}. Further increase in desorption time from 90 to 210 minutes reduces their FWHM to or below the value achieved for C_8PA annealed for 25 minutes. In addition, the increase in the desorption time from 25 to 90 minutes leads to a decrease in the amplitude and integral intensity of all four peaks, accompanying the removal of the remaining physisorbed C_8PA molecules. On the other hand, the increase in desorption time from 90 to 210 minutes leads to a substantial increase in the amplitude of all four peaks. This is related to changes in the alignment of C_8PA molecules since the annealing can only remove molecules from the monolayer. On average, the intensity rises by 39% and the integral intensity by 45%. The slight change in the mean C_8PA thickness also suggests an increased average tilt of the molecules away from the surface normal by ~ 2° (Section 5.4).

5.4 Results: MIM structures

The dielectric capacitance, leakage current density, and breakdown voltage of bare AlO_x and AlO_x functionalized with n-octylphosphonic acid (AlO_x/C_8PA) were investigated as a function of C_8PA desorption time. Also, from the capacitance values, C_8PA thickness was extracted as a function of C_8PA desorption time.

5.4.1 Capacitance

Figure 5.5(a) shows the average capacitance per unit area. The capacitance of bare AlO_x is 0.63±0.01 μF/cm^2. AlO_x/C_8PA capacitance value is lower than that of AlO_x due to presence of C_8PA. It increases from 0.41 to 0.46 μF/cm^2 as the C_8PA

desorption time rises from 25 to 210 minutes. The large deviation in the capacitance value for the 25-minute desorption is likely a consequence of the non-uniform as-deposited C_8PA thickness resulting in different progression of the desorption process and a larger variation in the properties of the dielectric. This is in agreement with the AFM results (Figure 5.3(c)) confirming that the 25-minute desorption leads to surface roughness of 0.48 nm, while the surface roughness is reduced to 0.36 nm after the 210-minute desorption.

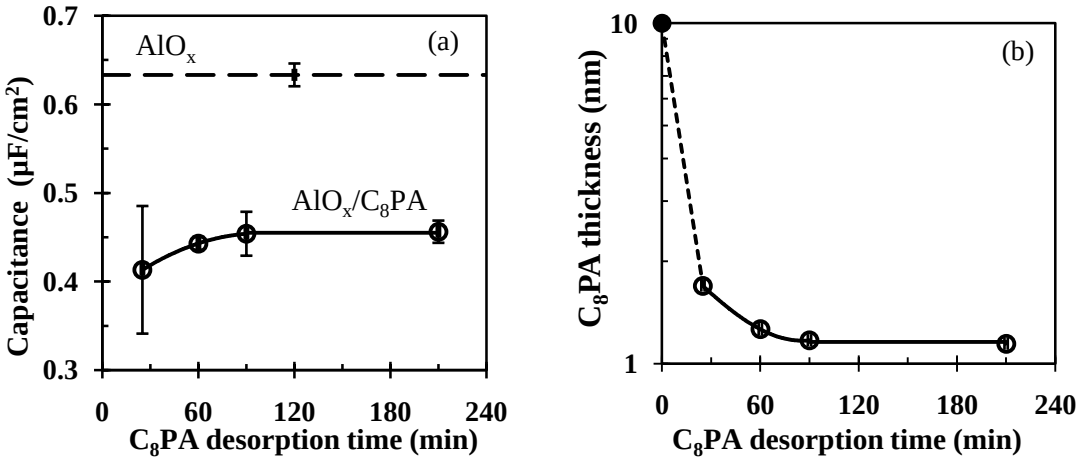

Figure 5.5: Capacitance of AlO_x/C_8PA per unit area as function of C_8PA desorption time (a). The capacitance of the reference AlO_x MIM structure is shown for comparison. The extracted C_8PA thickness is shown in (b).

5.4.2 AlO_x and C_8PA thickness

The thickness of AlO_x and $C_8PA$are calculated from the method described in Section 3.3.1.2. The thickness of AlO_x is 9.5 nm and this value is similar to the one obtained in Section 4.3. It shows the repeatability of the aluminium oxide layer from run to run.

C_8PA thickness calculated from the capacitance values of phosphonic acid (C_{C8PA}) is shown in Figure 5.5(b). After 25, 90, and 210 minutes of desorption, the

C_8PA thickness is 1.56, 1.15, and 1.14 nm, respectively. The thickness of the as-deposited C_8PAlayer is 10 nm, as determined from AFM. The desorption process removes the physisorbed molecules and the 10-nm-thick C_8PA layer is reduced to ~1.1 nm after 90 minutes of heating. Further 2-hour desorption has negligible effect on its thickness.

5.4.3 Leakage current density

Figure 5.6(a) shows the leakage current densities of AlO_x and AlO_x/C_8PA dielectrics for various C_8PA desorption times. The leakage current density through AlO_x and AlO_x/C_8PA dielectric is ~6×10^{-7} and ~10^{-7} A/cm^2 at the voltage of –3 V, respectively, although some AlO_x/C_8PA structures exhibit leakage current density as low as 4×10^{-8} A/cm^2. The leakage current density of AlO_x/C_8PA does not change much with desorption time. The lower leakage current density for the applied negative voltage is a benefit for p-channel OTFTs because their operation also requires the negative voltages only.

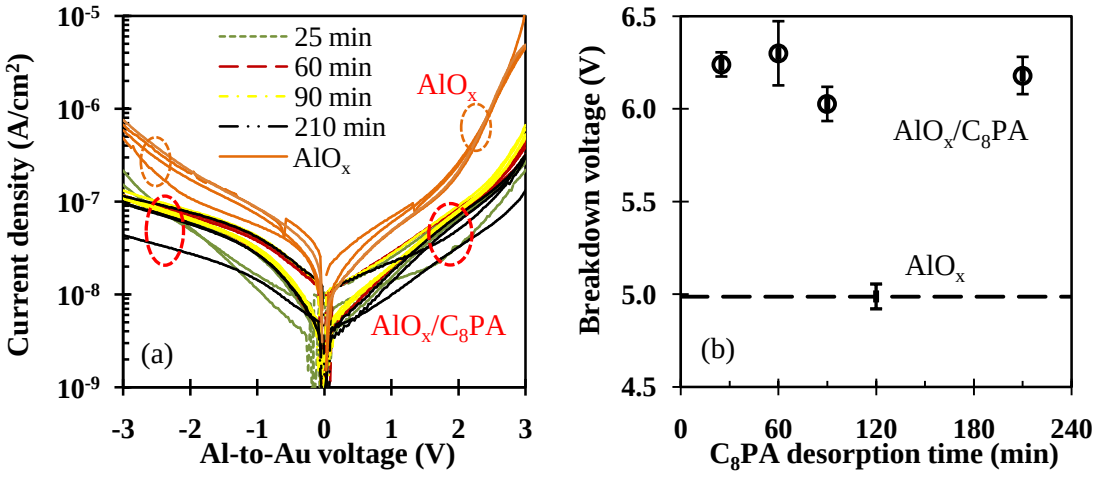

Figure 5.6: Current density (a) and breakdown voltage (b) of AlO_x reference and AlO_x/C_8PA bi-layer as functions of C_8PA desorption time.

5.4.4 Breakdown voltage

The dielectric breakdown voltages are shown in Figure 5.6(b). The mean breakdown voltage of AlO_x and AlO_x/C_8PA is ~5 and ~6.2 V, respectively. The breakdown voltage and the leakage current density of AlO_x/C_8PA MIM structures do not change much with the applied desorption time. The electric breakdown field of AlO_x and AlO_x/C_8PA calculated from the above layer thickness is ~5 and ~6 MV/cm, respectively.

To summarize, the as-deposited, ~10-nm-thick C_8PA layer is reduced down to a monolayer (~1nm) by removing the non-chemically bonded C_8PA molecules via thermal heating. The measurements show that although this process is completed in approximately 60 minutes, the monolayer is present even after 2.5 hours of additional heating. Functionalizing the AlO_x surface with thermally evaporated C_8PA monolayer lowers the leakage current density to ~10^{-7} A/cm^2 at –3V, increases the breakdown voltage to 6.2 V and the breakdown field to ~6 MV/cm.

5.5 Results: OTFTs

The OTFT transfer, output, and hysteresis characteristics were measured and the field-effect mobility, threshold voltage, subthreshold slope, off-current, and on/off current ratio as a function of C_8PA desorption time were compared.

5.5.1 Transfer and output characteristics

Transfer characteristics of OTFTs employing C_8PA desorbed for 210 minutes are shown in Figure 5.7(a) for drain-to-source voltages of –0.1 and –2 V. Figure

5.7(b) shows the corresponding output characteristics for the gate-to-source voltages of 0, –0.5, –1.0, –1.5, and –2 V.

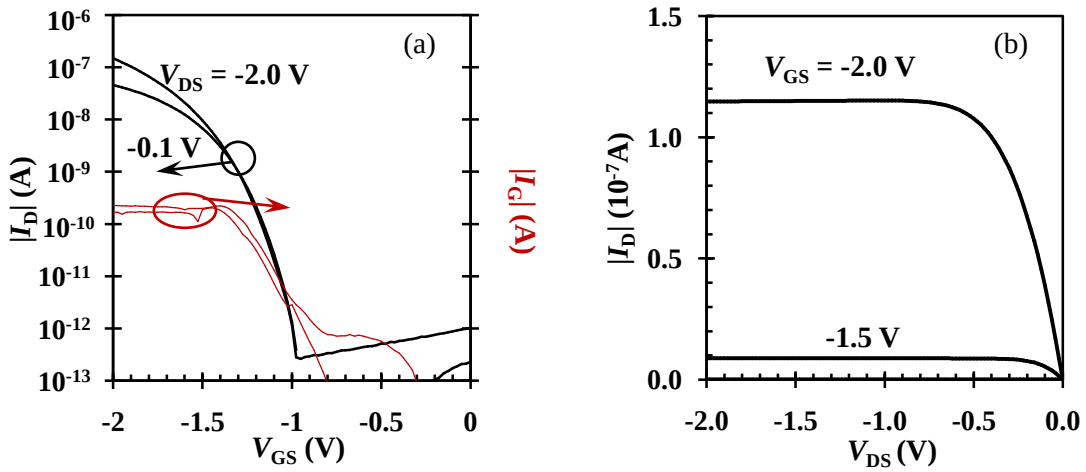

Figure 5.7: Transfer and output charactersitics of OTFT with L = 30 µm and W = 1000 µm. C_8PA desorption time was 210 minutes.

5.5.2 Field-effect mobility and threshold voltage

Figure 5.8(a) shows the field-effect mobility of OTFTs with AlO_x/C_8PA dielectric desorbed for 25, 60, 90, and 210 minutes. The mobility increases with C_8PA desorption time. The maximum field-effect mobility is ~0.04 cm^2/Vs for the longest 210-minute desorption. The threshold voltage of OTFTs as a function of desorption time is shown in Figure 5.8(b). The threshold voltage increases from ~ –1.2 to ~ –1.4 V when the desorption time changes from 25 to 210 minutes.

5.5.3 Off-current and on/off current ratio

Figure 5.8(c) shows the mean OTFT off-current as function of C_8PA desorption time. The increase in C_8PA desorption time from 25 to 210 minutes leads to a reduction in the off-current from ~5×10^{-12} A to <1×10^{-12} A. The on/off current

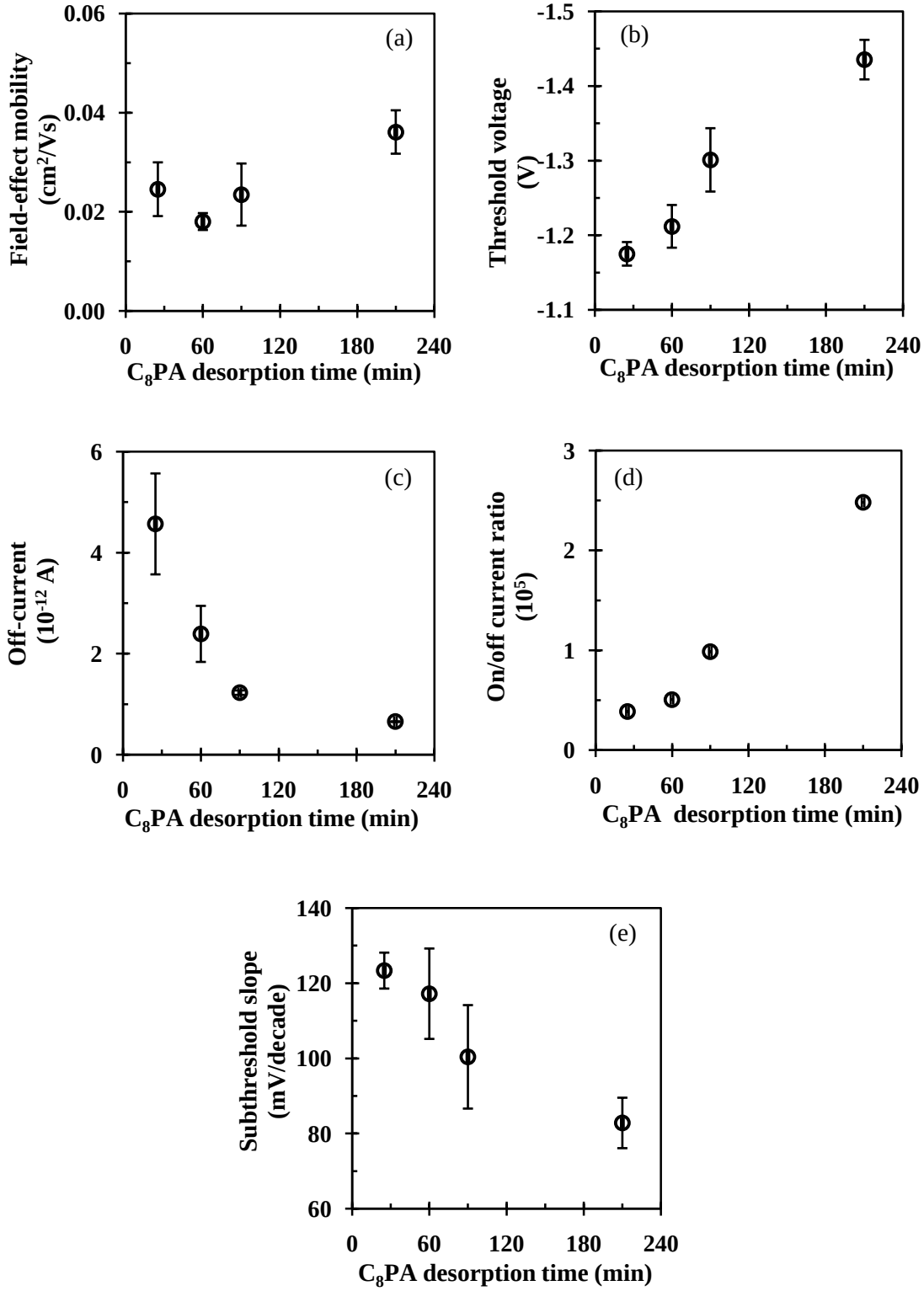

Figure 5.8: Field-effect mobility (a), threshold voltage (b), off-current (c), on/off current ratio (d), and subthreshold slope (e) of OTFTs as functions of desorption time.

ratio of OTFT with 30 μm channel length is shown in Figure 5.8(d). The reduction in the off-current also led to an increase in the on/off current ratio from ~3.8×10^4 to ~2.5×10^5. The increase in on/off current ratio was also observed for all other channel lengths.

5.5.4 Subthreshold slope

The subthreshold slope decreased from ~120 mV/decade to ~80 mV/decade when C_8PA desorption time increased from 25 to 210 minutes, as shown in Figure 5.8(e). The decrease in the subthreshold slope is an indication of the reduced trap density at the semiconductor/dielectric interface.

5.5.5 Hysteresis

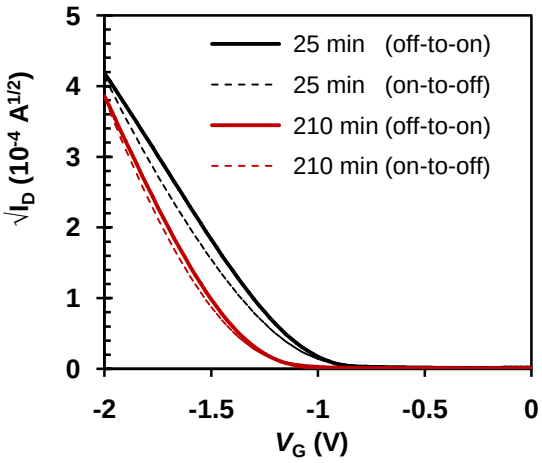

Figure 5.9: Hysteresis of the transfer characteristics of OTFTs with C_8PA desorbed/annealed for 25 and 210 minutes.

The hysteresis of the transfer characteristics of OTFTs with C_8PA desorbed for 25 and 210 minutes is shown in Figure 5.9. The difference in the off-to-on and on-to-off current is reduced for longer desorption time.

5.5.6 Pentacene morphology

To better understand the correlation of OTFT parameters with pentacene morphology, Figure 5.10shows AFM images of a 50-nm-thick pentacene layer deposited on AlO_x/C_8PA after the 25-minute (Figure 5.10(a)) and 210-minute (Figure 5.10(b)) desorption. As shown in Figure 5.10(a), the larger grains of ~150-nm diameter contain sub-grains. The sub-grain structure is suppressed in Figure 5.10(b), although the overall pentacene grain size is slightly smaller.

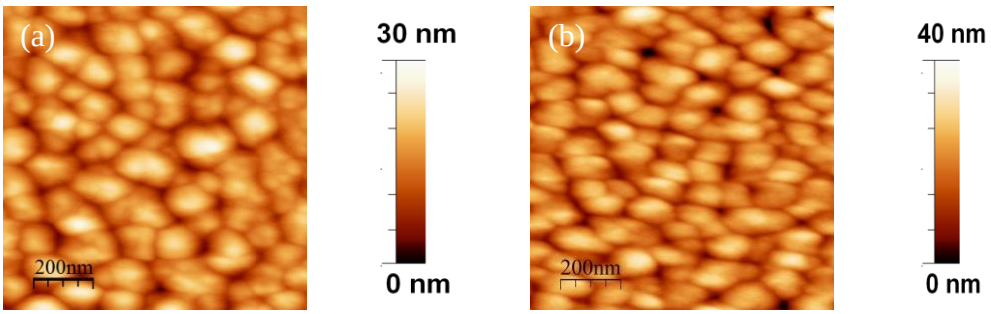

Figure 5.10: AFM surface images of pentacene deposited on C_8PA after the 25-minute (a) and 210-minute (b) desorption.

5.6 Discussion

According to Hoque et al. [42], AlO_x and C_8PA surfaces are hydrophilic and hydrophobic, respectively. The water contact angle of AlO_x is 46.6° showing that its surface is hydrophilic; AlO_x/C_8PA is >100° irrespective of desorption time demonstrating a hydrophobic surface. The change in water contact angle of the AlO_x

surface from 46.6° to 101.5° after C_8PA deposition shows that thermally evaporated C_8PA is present on top of AlO_x. An increase in the C_8PA contact angle after 25minutes of desorption is a likely consequence of removal of the physisorbed molecules with their hydroxyl groups. The hydrophobic nature of C_8PA surface is improved when the desorption time is increased from 25 to 210 minutes, leading to a water contact angle of 107.4°±0.5° for the latter. This value is higher than that achieved for C_8PA assembled from solutions [42] and similar to that obtained for the longer-chain alkyl phosphonic acids [18, 32, 75].

The AFM topography shown in Figure 5.3(a) reveals that aluminium oxide prepared by UV/ozone oxidation of thermally evaporated aluminium has roughness of 0.45 nm while the as-deposited C_8PA layer is very rough with mound-like morphology. Its morphology and RMS roughness change rapidly after desorption of the non-bonded C_8PA molecules, leading to roughness of 0.48 nm after the 25-minute desorption and slightly surpassing the RMS roughness of AlO_x after 210minutes. The roughness values of AlO_x/C_8PA are in contrast to the results reported by Ashall et al. [31] and Ma et al. [34] who reported that the surface roughness of phosphonic acid monolayer was higher than that of the underlying oxide. The vacuum grown C_8PA layer has roughness of 0.36 nm after 210 minutes of desorption and it is the lowest value for alkyl phosphonic acid reported to date. Such small surface roughness is comparable to that achieved with polymer dielectrics [31, 51]. The solution processed monolayers resulted in roughness of 0.76-3.2 nm depending on the chain length [11].

Water contact angle and AFM measurements confirm the difference in surface properties of AlO_x with and without C_8PA layer. Also, they prove that C_8PA

layer remains on the surface of the aluminium oxide even after prolonged heating. During C_8PA deposition, the C_8PA source material starts to evaporate at a temperature of ~130°C. Therefore, when the AlO_x/C_8PA surface is heated at a higher temperature, the organic molecules that are not chemically bonded to AlO_x can re-evaporate from the surface in ~30 minutes. Since the AFM and water contact angle measurements confirm the C_8PA presence even after 3.5 hours, this is possible only if the C_8PA layer is chemically bonded to AlO_x.

The head group of C_8PA (Figure 5.1) contains two P-OH bonds and one P=O bond that facilitate the attachment of C_8PA to AlO_x surface. Previous research on solution-processed alkyl phosphonic acids on aluminium oxide has shown that the organic molecules chemisorb to AlO_x [11, 18, 32, 37, 42]. The aliphatic chain was observed to orient away from the AlO_x surface. Similarly, in vacuum vapour deposition of phenylphosphonic acid on aluminium oxide, an outward phenyl ring formation was observed with phosphonate interface (Al-O-P) [76].

A proposed reaction between the aluminium oxide terminated with hydroxyl groups (HO−Al−) and alkyl phosphonic acid ($R-PO(OH)_2$) is [77]:

$$R-PO(OH)_2 + HO-Al- \rightarrow R-(OH)OP-O-Al + H_2O$$

The reaction proceeds via an acid-base condensation mechanisms in three stages and ultimately results in tridentate binding configuration of the phosphonic acids [78–80]. Initially the two P–OH groups of the C_8PA head group react with two Al–OH groups on the surface of aluminium oxide to produce two P–O–Al bonds of a bidentate complex and two water molecules. In the last step, the P=O group forms the third P–O–Al bond and converts the bidentate complex into a tridentate one. (P–O–Al stretch mode is located near 1100 cm^{-1} [66].)

Even though the mechanism of this reaction is not fully understood, three possible reaction paths have been proposed for the P=O group. In the first case the P=O groups react with the surface Al atoms, where the number of unsaturated Al atoms determines the maximum number of the tridentate complexes [81]. In the second case the –OH groups on the surface of aluminium oxide are protonated and released as water, allowing the formation of the P–O–Al bond [82]. In the third case, a hydrogen bond is formed between the P=O group and the surface hydroxyl group (P=O···H–O) [65]. Tridentate bonding was observed by Giza et al. [66] and Hotchkiss et al. [83] for n-octadecylphosphonic acid (C_{18}PA) on ZnO and AlO_x, respectively; but it was not observed for C_{18}PA deposited on ITO [72].

In the FTIR data shown in Figure 5.4(c) peaks corresponding to methyl and methylene groups were observed for all C_8PA desorption times which indicates the presence of aliphatic tails. Since the water contact angle of the AlO_x/C_8PA surface is very high, the outward facing aliphatic tails are obtained during the vacuum vapour-phase self-assembly of C_8PA. Also, the absorbance peak near 1100 cm^{-1} confirms the formation of the phosphonate (Al–O–P). An increase in desorption time from 25 to 90 minutes removes the remaining physisorbed molecules and the peaks corresponding to P=O bond are reduced, while the disorder between the aliphatic tails is slightly increased and the vibrations of the phosphonate salts are shifted to a lower wavenumber. Extension of desorption time from 90 to 210 minutes primarily improves the molecular alignment within the organic monolayer. The surface characteristics obtained from AFM and WCA measurements and the structural information provided by FTIR prove that the thermally-evaporated C_8PA molecules

are attached to AlO_x surface. An increase in desorption time from 25 to 210 minutes leads to a change in the surface and structural properties of C_8PA.

Next, a discussion of the effect of C_8PA desorption time on the electrical properties of MIM structures and OTFTs is presented. AlO_x dielectric has capacitance of 0.63 μF/cm^2 while AlO_x/C_8PA capacitance values are reduced to 0.41-0.46 μF/cm^2 depending on desorption time. The lower capacitance values of the AlO_x/C_8PA dielectric as compared to AlO_x dielectric are a consequence of the presence of C_8PA layer on top of AlO_x. As confirmed by FTIR measurements, the 90-minute anneal removes all physisorbed molecules and results in the reduction ofC_8PA thickness. Consequently, the capacitance of AlO_x/C_8PA bi-layer is increased. After the 25-minute desorption the capacitance value is 0.41 μF/cm^2, while the 60- and 90-minute desorption results in capacitance of 0.44 and 0.45 μF/cm^2, respectively.

The C_8PA thickness calculated from the capacitance value (assuming no change in the relative permittivity of C_8PA) is 1.69 and 1.26 nm for the 25- and 60-minute desorption, respectively. The change in the capacitance value is negligible after the 90- and 210-minute desorption and the corresponding C_8PA thickness value is 1.10 nm. In fact, no change in the C_8PA thickness is expected after all physisorbed molecules are removed because the temperature of 160°C is not high enough to break the C−C or P−C bonds. Previously, Davies et al. found that the chemisorbed methyl phosphonic acid (C_3PA) prepared in solution is thermally stable to at least ~300°C [84] and the thermal decomposition of C−C bond in methane and ethane is predicted to require at least 600°C. Therefore, another 120 minutes of heating does not affect the capacitance value even though the additional heating leads to the structural

changes in the C_8PA monolayer, as observed from FTIR. The capacitance value after the 90-minute desorption has slightly larger deviation than the one for 210-minute desorption possibly resulting from molecular disorder. The thickness of the C_8PA monolayer is similar to that calculated by Jedaa et al. [32]. Hence, it can be concluded that once the C_8PA monolayer is formed, the additional heating at 160°Cdoes not cause its detachment from AlO_x surface.

9.5-nm-thick AlO_x has leakage current density of 6×10^{-7} A/cm^2 at –3 V. The current density reduced by almost an order of magnitude when ~1-nm-thick C_8PA monolayer was added on top. Consequently, the leakage current density of the 10-nm-thick AlO_x/C_8PA bi-layer dielectric ranges from 10^{-7} A/cm^2 to 4×10^{-8} A/cm^2 with increasing desorption time. Even though the thickness of C_8PA is almost the same after 90 and 210minutes of desorption, the current density of AlO_x/C_8PA is slightly smaller after 210 minutes, demonstrating a slight improvement in the dielectric properties after two additional hours of desorption/annealing. Even though phosphonic acids with longer aliphatic tails lead to lower leakage current density [11, 32], the leakage current density obtained in this work is similar to that obtained for alkyl phosphonic acid with longer chain (C_{18}PA) by Jedaa et al.[32], Ma et al.[34], and Wöbkenberg et al. [37].

The breakdown voltage of AlO_x/C_8PA dielectric is about 1.2 volts higher than that of AlO_x without C_8PA. The breakdown voltage increases with the thickness of the dielectric and the larger breakdown field of AlO_x/C_8PA versus AlO_x means that the former dielectric is better than the latter. This breakdown field is higher than that achieved for thicker dielectrics based on aluminium oxide coated with polymer layer [30].

The dielectric capacitance of AlO_x/C_8PA of 0.46 μF/cm^{2}is comparable to that used in low-voltage OTFTs fabricated by Kippelen's group [85], Yoon et al. [86], Anthopoulos's group [87], and Lee's group [88]. AlO_x/C_8PA breakdown field of 6.2 MV/cm is higher than that of other dielectrics in organic devices, e.g. hafnium oxide [86], amorphous fluropolymer Cytop [89], and PMMA [90].

The leakage current density and the insulating properties of the dielectric depend on the dielectric preparation method. The presented AlO_x/C_8PA dielectric with vacuum-grown C_8PA resulted in leakage current density similar to that reported by Klauk et al. [18]; and the electric breakdown field comparable to that obtained by Jedaa et al. [32] when using solution-processed alkyl-phosphonic acid monolayer on top of AlO_x. The achieved dielectric properties of the AlO_x/C_8PA bi-layer confirm that the developed low-temperature, solvent-free process is a viable fabrication option for organic electronics. The reduction in the leakage current density, increase in the breakdown electric field, and improvement in the surface roughness confirm that dry C_8PA monolayer provides good step coverage and offers an alternative path to alkyl phosphonic acid monolayers prepared from solution.

The performance of OTFTs is comparable to that of OTFTs that implement alkyl phosphonic acids assembled from solution. The drain current is three orders of magnitude higher than the gate current, demonstrating good insulating properties of the dielectric bi-layer. This ratio is higher than that for pentacene-based OTFTs with $C_{14}PA$ [32, 36] and lower than that for pentacene based OTFTs with $C_{18}PA$ [18].

The maximum field-effect mobility is 0.04 cm^2/Vs, comparable to mobility achieved with C_6PA by Jedaa et al. [32]. The increase in the mobility with increasing C_8PA desorption time is correlated with lower surface roughness of C_8PA

monolayer. Higher field-effect mobility was achieved for similar OTFT structures with pentacene dendrites that are several micrometers in size [11]. The pentacene grains are ~100 nm in diameter (Figure 5.10) and lead to field-effect mobility of 0.04 cm^2/Vs, one order of magnitude lower than the mobility of OTFTs with pentacene dendrites of 2-3 μm in size [11]. Consequently, the OTFT mobility is well correlated with the pentacene morphology.

The OTFT threshold voltage increases from ~–1.2 V to ~–1.4 V as the C_8PA desorption time increases from 25 to 210 minutes. According to Zhang et al. [28], improper passivation of –Al–OH results in earlier turn-on voltage and lower threshold voltage of the transistors. The low threshold voltage can result in higher off-current and, consequently, lower on/off current ratio [28, 91]. OTFTs with C_8PA desorbed for 210 minutes exhibit the lowest off-current, the highest on/off current ratio, and the highest threshold voltage among the fabricated OTFTs. The on/off current ratio is the best among OTFTs with alkyl phosphonic acids of short alkyl chains reported to date [11, 32]. The achieved on/off current ratio is also higher than that obtained for pentacene OTFTs with Al_2O_3/OTS [28], $HfO_2/C_{18}PA$[14], $AlO_x/C_{10}PA$ and $AlO_x/C_{18}PA$ [11] dielectrics. It is however smaller than that reported by Klauk et al. for pentacene OTFTs with $AlO_x/C_{18}PA$dielectrics [18].

The reduction in the subthreshold slope with increasing desorption time is a result of the C_8PA surface having low surface roughness and low density of traps, similarly to effects observed in [28, 31, 34]. The lowest subthreshold slope of ~80 mV/decade achieved after the 210-minute C_8PA desorption is only slightly higher than the best reported value of 75 mV/decade for the interface between an alkyl phosphonic acid monolayer and pentacene [92].

When considering all results collectively, the post-deposition heating (desorption step) of C_8PA layer has dual function; removes all physisorbed molecules down to a single layer and subsequently anneals the remaining C_8PA monolayer. The desorption temperature is high enough to counteract the weak interaction between the alkyl chains of neighbouring molecules. Even though the molecules in the C_8PA monolayer are attached to the AlO_x surface, the thermal energy supplied during the desorption step allows minor realignment of the molecules to minimize the energy of the system.

AFM images presented in Figure 5.10 reveal that the pentacene grain size is ~100 nm when it grows on AlO_x/C_8PA after the 210-minute desorption. This grain size is comparable to thermally evaporated pentacene on HfO_2/PA [14], Al_2O_3/OTS [28], AlO_x and AlO_x/C_{18}PA [31], SiO_2/octadecyltrichlorosilane [55, 57, 93] and low surface energy polyimide-siloxane [58].

5.7 Conclusion

Vacuum, vapour-phase, self-assembly of C_8PA monolayer on AlO_x was developed. To grow a monolayer, the thickness corresponding to several C_8PA monolayers was deposited, followed by a thermal desorption of the physisorbed molecules. Water contact angle, AFM, and FTIR measurements confirm that C_8PA molecules are chemically bonded to the surface of AlO_x, while the aliphatic tails are oriented away from the binding surface. In addition, the capacitance measurements show that the ~10-nm-thick C_8PA layer reduces to ~1.56 nm after 25 minutes of desorption and ~1.1-nm-thick monolayer remains after 90 minutes. The monolayer remains attached to the AlO_x surface even after 3.5-hours of prolonged heating at the

temperature of 160°C, while the monolayer structure improves during the prolonged heating, resulting in improved electrical properties of the AlO_x/C_8PA gate dielectric and OTFTs.

When the C_8PA monolayer is deposited in vacuum on a 9.5-nm-thick AlO_x with RMS surface roughness of 0.45 nm, the leakage current density is reduced by ~an order of magnitude and the breakdown voltage is increased by ~1.2 V. The AFM measurements show that the RMS roughness of the optimized C_8PA surface is 0.36 nm. This value is comparable to polymer dielectrics and smaller than the values previously reported for alkyl phosphonic acids. In addition, the water contact angle measurement of the optimized C_8PA surface is 107.4°±0.5°, a value similar to that of $C_{18}PA$ monolayers assembled from solutions.

To provide a practical demonstration of this vacuum vapour-phase self-assembly, low-voltage OTFTs based on pentacene and dry AlO_x/C_8PA gate dielectric bi-layer were fabricated. They operate within 2 V and exhibit good linear/saturation behaviour characteristics. However, the OTFT parameters are dependent on C_8PA desorption time. Increase in the C_8PA desorption time leads to an increase in the field-effect mobility from ~0.02 cm^2/Vs to ~0.04 cm^2/Vs, increase in the threshold voltage from ~–1.2 to ~–1.4 V, decrease in the subthreshold slope from ~120 mV/decade to ~80 mV/decade, decrease in the off-current from ~5×10^{-12} A to <1×10^{-12} A, and increase in the on/off current ratio from ~3×10^4 to ~2.3×10^5. These results collectively confirm that the applied desorption step removes all physisorbed C_8PA molecules down to a single layer and improves the alignment between the aliphatic tails of C_8PA monolayer.

Chapter 6

Effect of substrate temperature on vapour-phase assembly of C_8PA

In the previous chapter, the vacuum vapour-phase self-assembly of n-octyl-phosphonic acid (C_8PA) monolayer on aluminium oxide (AlO_x) was described. This chapter presents the effect of substrate temperature on the C_8PA vapour-phase assembly.

The experiment conducted to study the effect of the substrate temperature is introduced in Section 6.1 and the preparation of samples for the material characterization as well as the device fabrication is described in Section 6.2. The measured structural and surface properties of AlO_x and AlO_x/C_8PA are given in Section 6.3. Sections 6.4 and 6.5 present the results of the electrical measurements performed on MIM and OTFT structures, respectively. Correlation of the material

and electrical properties is discussed in Section 6.6. Finally, all experimental findings are summarized in Section 6.7.

6.1 Introduction

Though vapour-phase self-assembly of organic monolayers is compatible with roll-to-roll processing and avoids using orthogonal solvents, such processes are much less explored than their solution-based counterparts. Previous research studied the effect of the exposure time [94], and deposition rate [76], or used a special molecular design with different chemical properties of the head and tail groups of the organic molecule [40, 95–97]. This chapter builds on the experimental findings presented in the previous chapter, while exploring the effect of C_8PA growth temperature on the monolayer self-assembly.

10-nm-thick C_8PA layer is deposited on to substrates held at temperatures of 25, 75, 125, and 150°C and subsequently desorbed/annealed for 3 hours at 160°C. Even though in the previous experiment the best transistor performance was obtained after the 210-minute desorption, here a 180-minute desorption was selected in the attempt to reduce the fabrication time while maintaining the transistor performance. It was concluded earlier that the 90-minute desorption was sufficient to form a monolayer while the additional heating improved the alignment of the C_8PA molecules within the monolayer. Consequently, one would expect comparable results when the C_8PA anneal is reduced from 210 to 180 minutes.

Similar to the growth of inorganic materials, the elevated substrate temperature applied during C_8PA growth may affect the chemisorption of C_8PA molecules on AlO_x as well as the overall growth kinetics, leading to different

structural and electrical properties of the formed monolayer. The structural properties were measured by FTIR, while the surface properties were investigated by WCA and AFM. Electrical properties of the MIM structures and OTFTs were also measured and analysed and the correlation between the electrical and material properties was sought.

6.2 Sample/device fabrication

7.5×7.5 cm^2 glass substrate was cut into four pieces to prepare samples for FTIR measurements. Another glass substrate was cut into smaller pieces to fabricate samples for water contact angle measurement. ~10-nm-thick aluminium oxide was prepared using the method described in Section 4.3.

Other than the reference AlO_x samples and devices, C_8PA monolayer was prepared to study the effect of C_8PA deposition temperature. Approximately 10-nm-thick C_8PA layer was evaporated on the surface of AlO_x at substrate temperatures of 25, 75, 125, or 150°C. Afterwards, the substrate temperature was raised to 160°C for 3 hours to remove all physisorbed molecules. This completed the preparation of AlO_x and AlO_x/C_8PA samples for material characterization that included FTIR and WCA measurements on fresh specimens.

In OTFTs, 50-nm-thick pentacene was deposited on AlO_x/C_8PA bi-layer and reference AlO_x dielectric. The MIM structures were fully masked during this deposition. Finally, 50-nm-thick gold contacts were evaporated to complete the MIM and OTFT structures. Except raising the pentacene substrate temperature to 70°C, all other deposition parameters of pentacene and gold were identical to those in Chapter 5. Several MIM and OTFT devices were fabricated for each C_8PA growth

temperature and the reference AlO_x. The transistor cross-section is shown in Figure 3.1. The fabricated transistors have nominal channel lengths of 30, 50, 70, and 90 μm and a channel width of 1000 μm.

6.3 Results: surface and structural properties

WCA, AFM, and FTIR measurements were performed in ambient air and the results are given below.

6.3.1 WCA

The water contact angles of AlO_x/C_8PA surfaces as function of the C_8PA growth temperature are given in Table 6.1. AlO_x/C_8PA exhibits contact angle values larger than 107° for all temperatures, showing that AlO_x/C_8PA is hydrophobic irrespective of the growth temperature. However, there is a slight decrease in the water contact angle with increasing C_8PA deposition temperature. The maximum value of 113.5°±1.4° and the minimum value of 107.9°±0.8° are obtained for n-octylphosphonic acid monolayer deposited at 25 and 150°C, respectively.

In this experiment, the measured contact angle of AlO_x/C_8PA is 113.5°±1.4° at 25°C and AlO_x has the value of 30.8±0.7°, while in the previous measurement the measured values were 107.4°±0.5° and 46.6±0.2°, respectively. Such small difference in C_8PA contact angle values can be attributed to different external factors such as air humidity or sample storage and transportation. The larger difference in the water contact angle of AlO_x is attributed to UV/ozone treatment that leads to a smaller value if applied prior to the water contact angle measurement.

Table 6.1: Water contact angle of AlO_x/C_8PA surface as a function of C_8PA growth temperature. AlO_x is added as a reference.

Growth temperature (°C)	Water contact angle (°)
25	113.5 ± 1.4
75	112.1 ± 1.4
125	111.1 ± 0.7
150	107.9 ± 0.8
AlO_x reference	30.8 ± 0.7

6.3.2 AFM

The AFM surface topography of reference AlO_x is shown in Figure 6.1(a) and the surface of AlO_x/C_8PA deposited at temperatures of 25, 125, and 150°C is presented in Figure 6.1(b)-(d). The RMS surface roughness of AlO_x/C_8PA grown at 25, 125, and 150°C is 0.36, 0.38 and 0.54 nm, respectively. It shows that the surface roughness of AlO_x/C_8PA increases with C_8PA substrate temperature. The reference AlO_x surface roughness is 0.46 nm.

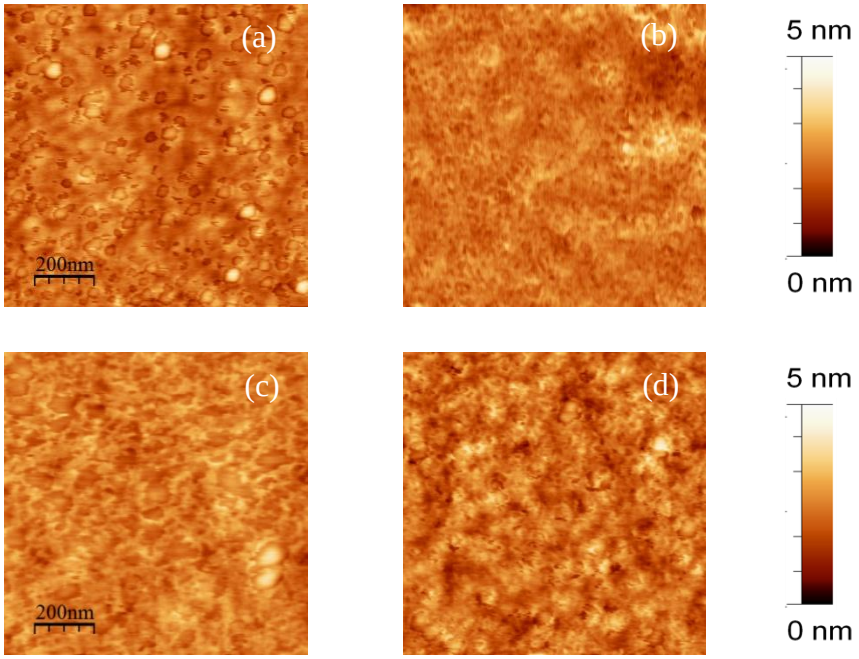

Figure 6.1: AFM surface image of C_8PA grown at temperature of 25 (b), 125 (c), and 150°C (d). The reference AlO_x surface topography is shown in (a).

The topography and the surface roughness of the reference AlO_x and AlO_x/C_8PA deposited at 25°C are similar to the experimental data presented in Section 5.3.2. The surface roughness of AlO_x/C_8PA with C_8PA deposited at 25 and 125°C is lower than that of reference AlO_x, while it is higher for C_8PA deposited at 150°C.

6.3.3 FTIR

FTIR data includes C_8PA monolayer self-assembled on AlO_x at substrate temperatures of 25, 75, and 150°C and the reference AlO_x layer. The section of FTIR spectrum from 1025 to 1175 cm^{-1} and from 1175 to 1275 cm^{-1} is shown in Figure 6.2(a) and (b), respectively. This data provides information about the chemisorption of the phosphonate group to AlO_x surface, while the data presented in Figure 6.2(c) carries information about the aliphatic tails of C_8PA.

The broad absorption band centred near 1110 cm^{-1} is present in all samples as shown in Figure 6.2(a). In AlO_x/C_8PA samples, it is interpreted as evidence of chemisorption of the phosphonate group to the surface of AlO_x (Section 5.3.3) and therefore, the main contribution to this vibration band is from Al–O–P stretch mode [72]. The integral intensity of this band is slightly smaller for C_8PAgrown at

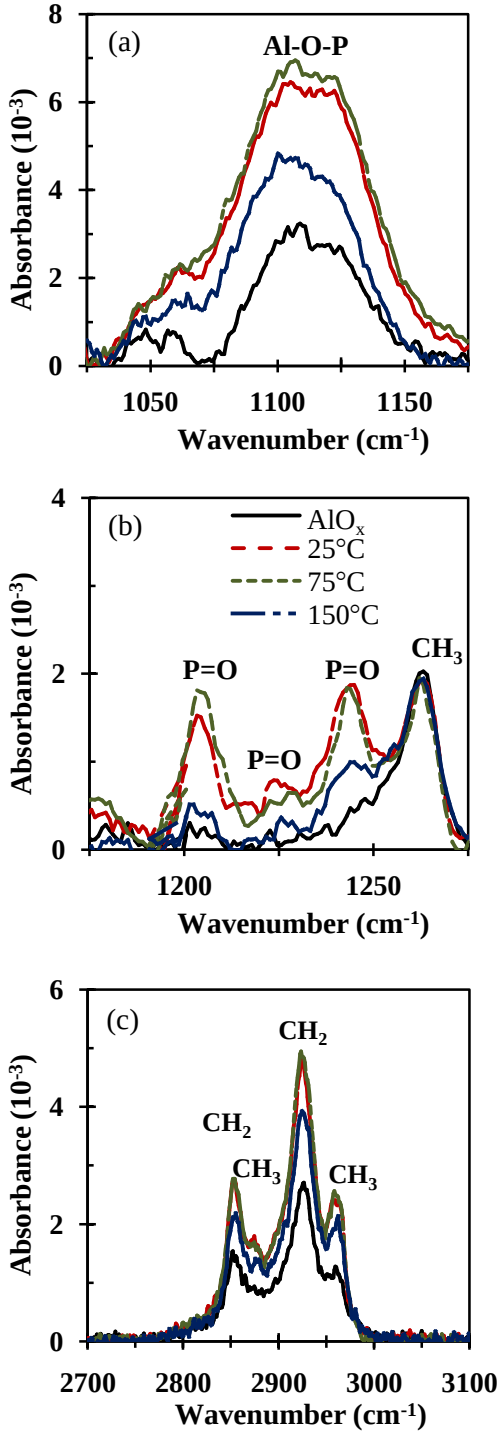

Figure 6.2: FTIR spectrum of AlO_x/C_8PA with C_8PA deposited at substrate temperature of 25, 75, and 150°C. The reference AlO_x is shown as well.

substrate temperature of 25°C, if compared to that grown at 75°C, and much larger than that of C_8PA grown at 150°C. The AlO_x/C_8PA absorption for C_8PA grown at 25°C is similar to that presented in Figure 5.4 for the 210-minute desorption.

The broad absorption peak in the reference AlO_x sample located near 1100 cm^{-1} overlapping with the band of the phosphonate salts is associated with the Al–OH groups. The 3-hour annealing of AlO_x shifted the band to a higher wavenumber if compared to the non-annealed AlO_x shown in Figure 5.4(a). The integral intensity is also reduced after annealing.

The reference AlO_x sample exhibits a weak vibration at 1263 cm^{-1} assigned to the methyl group. Three absorption peaks in AlO_x/C_8PA at ~ 1204, 1226, and 1244 cm^{-1} are related to the P=O bond of the phosphonic acid [74]. These peaks were observed in the previous experiment as well. While the amplitude and integral area of these three vibration bands are similar for C_8PA grown at 25 and 75°C, they are visibly reduced for C_8PA grown at 150°C. The centre position of the two stronger peaks located near 1204 and 1244 cm^{-1} and their FWHM do not change with C_8PA growth temperature. At 150°C, the low absorbance intensity at 1204, 1226, and 1244 cm^{-1} is an evidence of fewer P=O bonds.

The integral intensity is also lower in the region of 2800-3000 cm^{-1} (Figure 6.2(c)) corresponding to methylene ($-CH_2$) and methyl ($-CH_3$) groups. Both of these confirm that fewer C_8PA molecules are present on AlO_x surface at substrate temperature of 150°C.

The symmetric and asymmetric CH_2 and CH_3 stretching modes observed in the reference AlO_x sample may be due to the presence of methane in the ambient atmosphere. These modes become stronger in the AlO_x/C_8PA layers where the

aliphatic chain of the phosphonic acid contributes to the absorbance. For C_8PA grown at 25°C their centre positions lay at $\nu_s(CH_2)$ = 2853 cm^{-1}, $\nu_a(CH_2)$ = 2925 cm^{-1}, $\nu_s(CH_3)$ = 2874 cm^{-1}, and $\nu_a(CH_3)$ = 2961 cm^{-1}. With an increasing C_8PA grown temperature, all maxima are marginally shifted to higher wavenumber, indicating an increased molecular disorder with increasing growth temperature. For C_8PA grown at 150°C $\nu_s(CH_2)$ = 2854 cm^{-1}, $\nu_a(CH_2)$ = 2926 cm^{-1}, $\nu_s(CH_3)$ = 2878 cm^{-1}, and $\nu_a(CH_3)$ = 2961 cm^{-1}. The full width at half maximum (FWHM) of the asymmetric CH_2 stretch does not change, while the FWHM of the symmetric CH_2 stretch is increased by 5 cm^{-1} when the C_8PA substrate temperature is raised from 25 to 150°C. While the amplitude and integral area of all vibration bands between 2700 and 3100 cm^{-1} are similar for C_8PA grown at 25 and 75°C, they are visibly reduced for C_8PA grown at 150°C.

Finally, molecules containing P–OH groups exhibit two broad bands of the OH stretching vibration appearing near 2600 cm^{-1} and 2200 cm^{-1} [74]. Neither of these absorption bands is observed in the measured spectrum, indicating that the chemisorption of all C_8PA molecules proceeds via the P–OH groups at all growth temperatures.

Even though the C_8PA layer is present on the surface of AlO_x for all deposition temperatures, differences in the surface and structural properties were observed as function of the deposition temperature (Sections 6.3.2 and 6.3.3). These changes in C_8PA monolayer affect the electrical properties of the MIM and OTFT devices, as discussed next.

6.4 Results: MIM structures

The capacitance and leakage current density of bare AlO_x and AlO_x/C_8PA bi-layer as functions of C_8PA substrate temperature were measured. The capacitance data was used to calculate the thickness of C_8PA layer with respect to its growth temperature.

6.4.1 Capacitance

The total capacitance per unit area of AlO_x and AlO_x/C_8PA MIM structures at 100 kHz is shown in Figure 6.3(a). The mean capacitance of AlO_x is 0.57 $\mu F/cm^2$. The AlO_x/C_8PA bi-layer has capacitance of 0.43 $\mu F/cm^2$ for C_8PA grown at 25°C. This value is slightly higher for C_8PA substrate temperatures of 75 and 125°C. When C_8PA is grown at 150°C, the capacitance value reaches 0.54 $\mu F/cm^2$.

6.4.2 AlO_x and C_8PA thickness

The thicknesses of AlO_x and C_8PA are extracted according to the method described in Section 3.3.1.2. AlO_x has thickness of 10 nm and the C_8PA thickness for growth temperature of 25°C is 1.03 nm. Both values are similar to the values obtained in the previous experiment. C_8PA thickness as a function of C_8PA growth temperature is presented in Figure 6.3(b). A decrease in the C_8PA thickness with increasing growth temperature was observed. The growth temperatures of 75, 125, and 150°C resulted in the thickness of 0.78, 0.72, and 0.17 nm, respectively.

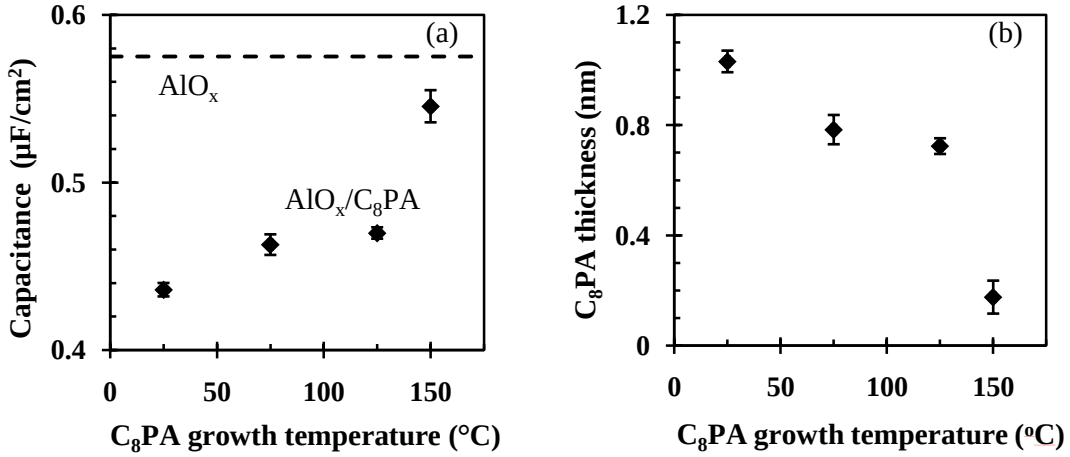

Figure 6.3: Capacitance per unit area of AlO_x/C_8PA dielectric (a) and C_8PA thickness (b) as functions of C_8PA growth temperature. The dashed line in (a) corresponds to the reference AlO_x capacitance.

6.4.3 Leakage current density

The leakage current density of AlO_x/C_8PA and the corresponding AlO_x are shown in Figure 6.4. The leakage current density of AlO_x is ~3×10^{-7} A/cm^2 at –3 V. This value is reduced to ~1×10^{-7} A/cm^2 when the AlO_x is functionalized with the vacuum-grown C_8PA monolayer. The growth temperature of the organic monolayer has only minor effect on this value, leading to the lowest current when the layer is grown at 25°C.

6.5 Results: OTFTs

In this section the electrical characteristics of OTFTs with AlO_x and AlO_x/C_8PA gate dielectric are compared. The effect of C_8PA substrate temperature on the OTFT performance is observed.

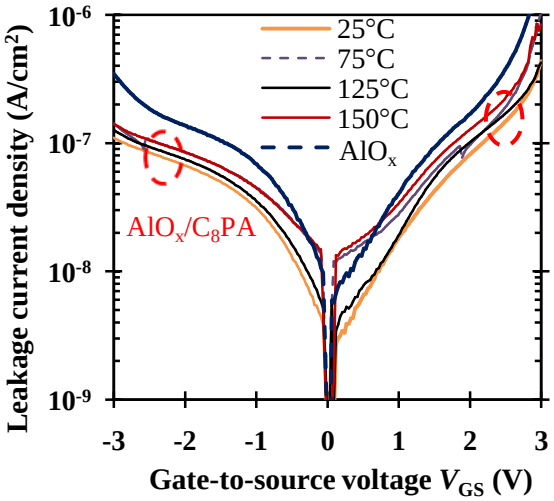

Figure 6.4: Leakage current density of AlO_x and AlO_x/C_8PA MIM structures.

6.5.1 Transfer and output characteristics

Figure 6.5(a) and (b) depict the transfer characteristics of OTFTs with AlO_x/C_8PA gate dielectric for C_8PA substrate temperature of 25 and 150°C, respectively. The corresponding output characteristics are presented in Figure 6.5(c) and (d). The transfer and output characteristics of the reference AlO_x OTFT are shown in Figure 6.6(a) and (b), respectively.

When C_8PA is grown at 25°C, the drain current of OTFT with the bi-layer gate dielectric is three times higher than that of OTFT implementing bare AlO_x, for the same channel dimensions. However, when C_8PA is grown at 150°C, the drain current becomes lower when compared to the reference AlO_x OTFT. Increase in the substrate temperature leads to higher gate current and lower drain current.

6.5.2 Threshold voltage and field-effect mobility

Figure 6.7(a) depicts the threshold voltages of the OTFTs. The mean value of the threshold voltage increases slightly from –1.19 to –1.25 V when C_8PA growth

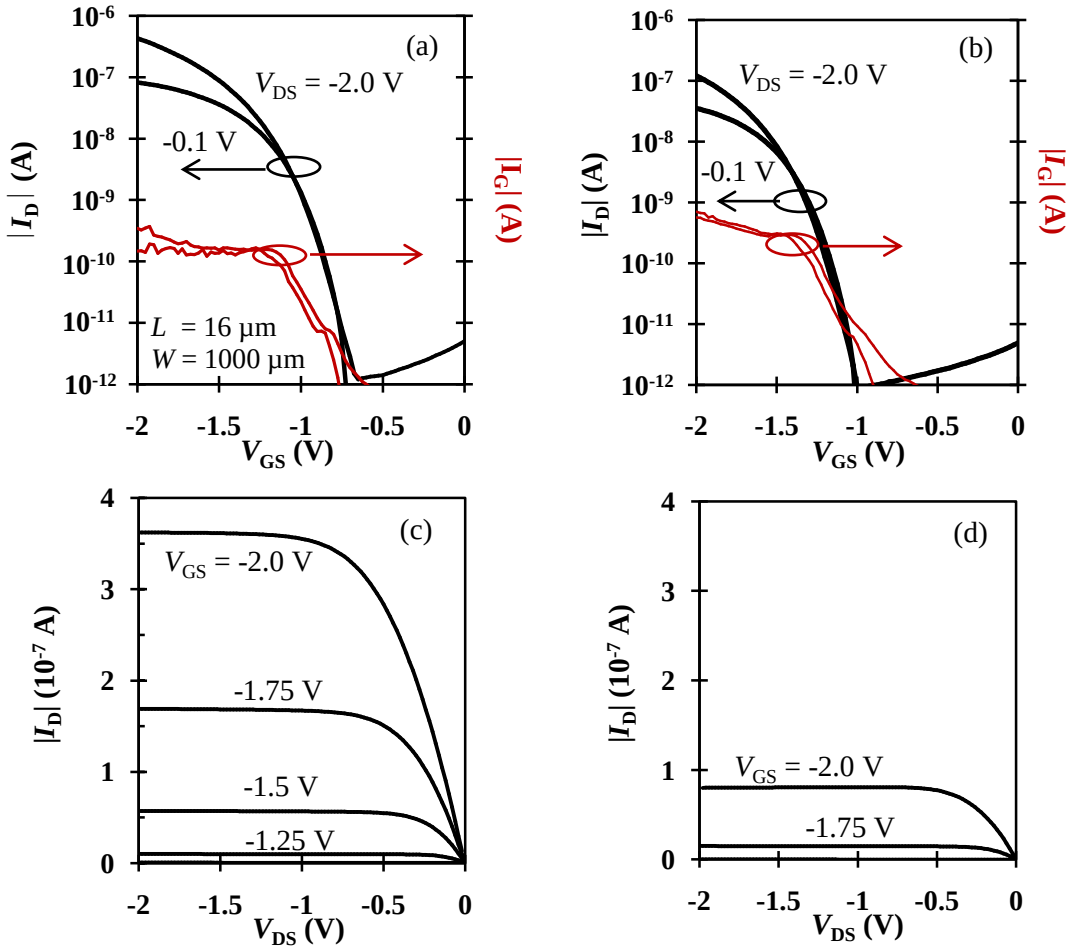

Figure 6.5: The transfer characteristics of OTFT with AlO_x/C_8PA dielectric. C_8PA growth temperature is 25 (a) and 150°C (b). The corresponding output characteristics are shown in (c) and (d).

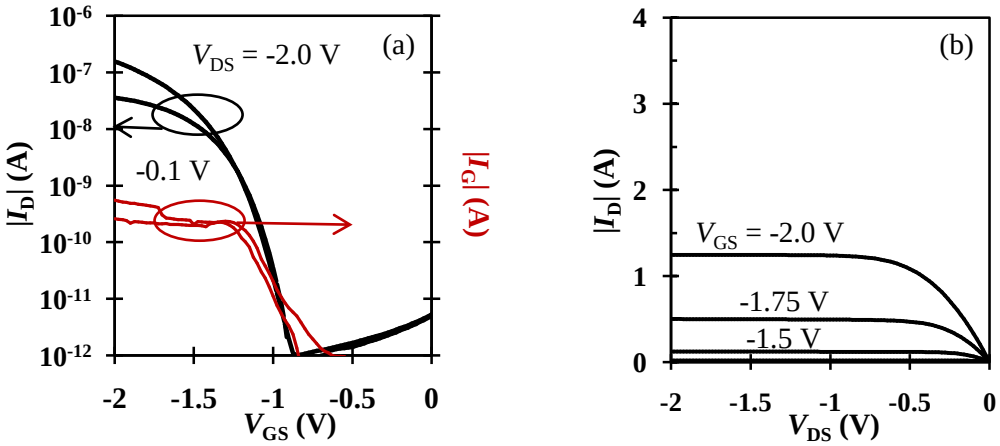

Figure 6.6: Transfer (a) and output (b) characteristics of OTFT with AlO_x gate dielectric. L = 25 µm and W = 1000 µm.

temperature is raised from 25 to 75°C; the values are similar within the error of measurement. On the other hand, a higher threshold voltage of –1.38 V is achieved for OTFTs implementing C_8PA grown at 150°C. Up to C_8PA substrate temperature of 125°C, the threshold voltage of OTFTs with bi-layer dielectric is lower than that of OTFTs with bare AlO_x. On the other hand, the threshold voltage of AlO_x/C_8PA OTFTs with C_8PA grown at 150°C is higher than that of OTFTs with bare AlO_x. The minimum threshold voltage of ~–1.2 V is achieved for C_8PA grown at 25°C. This value is lower than the one obtained in the previous experiment (Figure 5.8(b)).

Figure 6.7(b) depicts the field-effect mobility of OTFTs as function of C_8PA deposition temperature. The mobility of the reference AlO_x OTFTs is shown as well. The field-effect mobility decreases from 0.060 to 0.026 cm^2/Vs when the substrate temperature during C_8PA deposition is raised from 25 to 150°C. OTFTs with bare AlO_x have the mobility of 0.023 cm^2/Vs, the lowest value among all OTFTs. The dependence of the field-effect mobility on C_8PA growth temperature is discussed in Section 6.6.

6.5.3 Off-current and on/off current ratio

The mean values and standard deviations of OTFT off-current are shown in Figure 6.7(c). C_8PA growth at 25°C leads to the off-current of ~10^{-12} A, similar to the off-current of the reference OTFT. This value is slightly reduced for OTFTs implementing C_8PA grown at elevated temperature, reaching a minimum value of ~5×10^{-13} A at a grown temperature of 125°C.

Figure 6.7(d) shows the on/off current ratio of OTFTs with 30 μm channel length. The on-current of OTFTs with C_8PA grown at 25°C is two times higher than

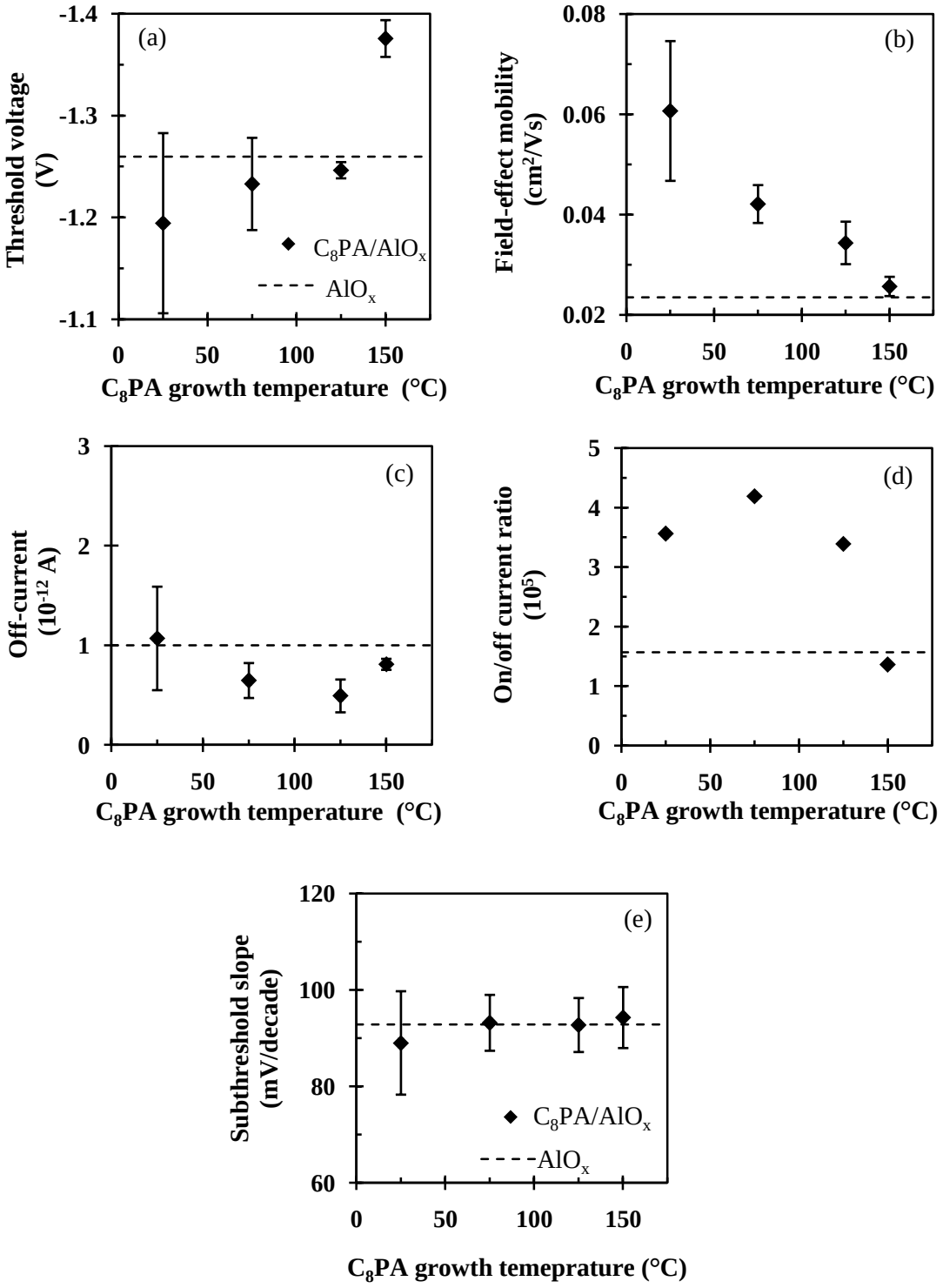

Figure 6.7: Threshold voltage (a), field-effect mobility (b), off-current (c), on/off current ratio (d), and subthreshold slope (e) as functions of C_8PA growth temperature. The dashed line represents the value of the reference AlO_x OTFTs.

that of OTFTs with C_8PA grown at 125°C. However, due to a larger off-current obtained for OTFTs with C_8PA grown at 25°C, their on/off current ratio is only slightly higher. Similarly, 75°C leads to the lowest off-current and the maximum on/off current ratio. The on/off current ratio is 3.56×10^5 for C_8PA grown at 25°C which is ~ 2.5 times higher than that of the reference AlO_x OTFTs.

6.5.4 Subthreshold slope

Figure 6.7(e) depicts the subthreshold slope of OTFTs. The subthreshold slope of AlO_x/C_8PA OTFTs is comparable to that of the reference AlO_x OTFTs. Mean values of ~90 mV/decade are observed and the variation in the C_8PA growth temperature leads to similar values of the subthreshold slope. The subthreshold slope of the reference AlO_x OTFTs is 93 mV/decade.

6.5.5 Hysteresis

Figure 6.8 shows the hysteresis of the transfer characteristic for AlO_x and AlO_x/C_8PA OTFTs. The hysteresis depends on the maximum applied $|V_{GS}-V_{th}|$ (overdrive) voltage. According to Figure 6.8, the hysteresis of AlO_x/C_8PA OTFT with larger overdrive voltage is comparable to that of AlO_x OTFT.

6.5.6 Pentacene morphology

Figure 6.9(a) and (b) show pentacene deposited on C_8PA grown at 25 and 125°C, respectively, while Figure 6.9(c) shows pentacene deposited on bare AlO_x. The grain diameter is around 300 nm for C_8PA grown at 25°C. Both AlO_x and C_8PA grown at 125°C lead to smaller pentacene grains.

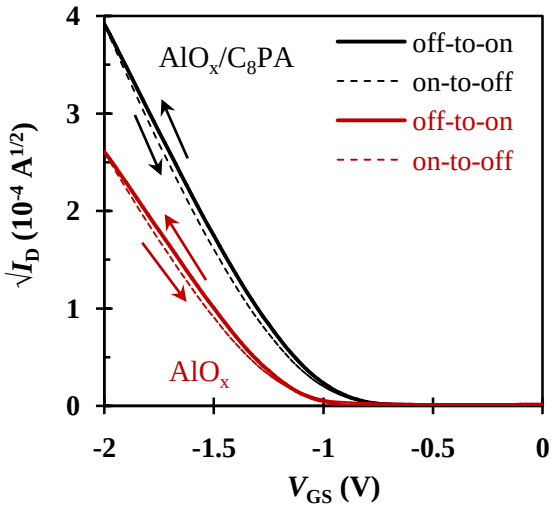

Figure 6.8: The hysteresis of AlO_x/C_8PA and AlO_x OTFTs. The solid and dashed line represents off-to-on and on-to-off direction, respectively.

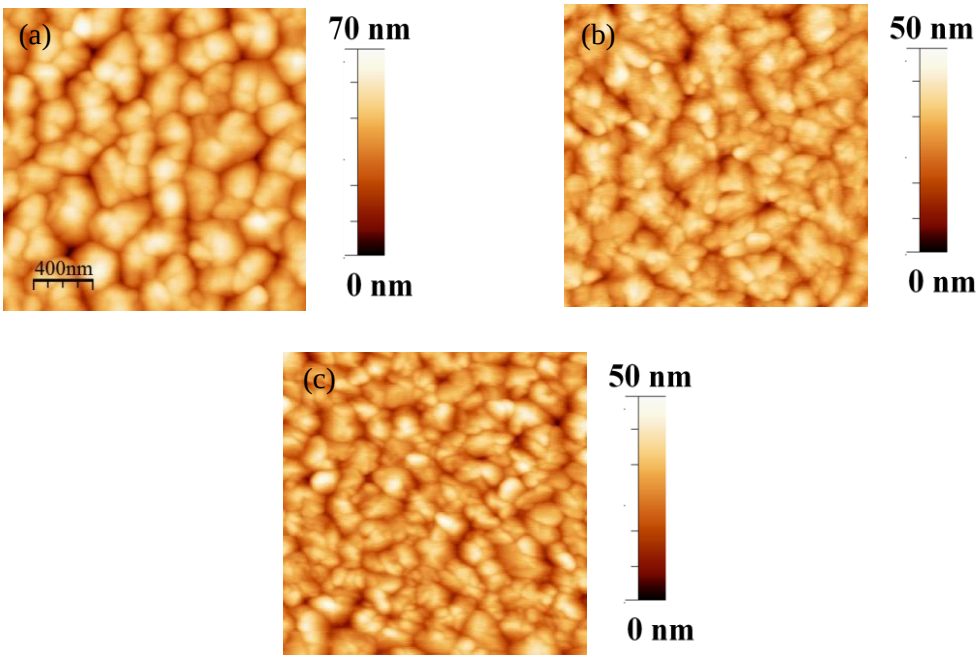

Figure 6.9: AFM images of pentacene deposited on AlO_x/C_8PA where C_8PA is grown at 25 (a) and 125°C (b). Reference sample of pentacene grown on AlO_x is shown in (c).

6.6 Discussion

Chemisorption of n-octylphosphonic acid to aluminium oxide surface using vacuum vapour-phase deposition has been demonstrated in the previous chapter. Here, the effect of C_8PA deposition at elevated substrate temperature on C_8PA self-assembly and subsequently on MIM and OTFT electrical properties was studied.

The reaction between AlO_x and C_8PA has been discussed in Section 5.6. The broad band of AlO_x/C_8PA near 1100 cm^{-1} indicates condensation reaction of Al–OH and C_8PA head group. The integral area of the band near 1100 cm^{-1} is similar for C_8PA grown at 25 and 75°C. However, when C_8PA is grown at 150°C, the area is substantially smaller. The absence of P–OH absorption bands means that both P–OH sites of the C_8PA head group are consumed in the chemisorption process regardless of the C_8PA growth temperature. For all C_8PA growth temperatures, small P=O vibrations are observed between 1200 and 1250 cm^{-1}, suggesting that some C_8PA molecules exhibit bidentate bonding.

The centre positions of the symmetric and asymmetric CH_2 and CH_3 vibration bands indicate a less ordered molecular structure, as a result of the weak interaction between short aliphatic tails. These values are however similar to C_8PA monolayers self-assembled from solutions [43]. The surface exposure of methylene groups in addition to the methyl groups previously resulted in lower water contact angle [98], which would explain the observed reduction in the water contact angle of C_8PA monolayers deposited at elevated substrate temperature and the increase in its surface roughness. For C_8PA monolayer grown at 150°C the surface roughness is ~0.54 nm, higher than that achieved for C_8PA grown at 25°C. Finally, the reduction in the

integral intensity of all vibration peaks for C_8PA grown at 150°C is associated with fewer chemisorbed molecules. In summary, FTIR measurements confirm that the increasing C_8PA growth temperature leads to chemisorption of fewer C_8PA molecules. Similar absorbance spectra of C_8PA grown at 25°C and annealed for 180 and 210 minutes indicate that C_8PA structure is not affected by shorter desorption/annealing. The water contact angle of C_8PA is higher than 107° for all growth temperatures, showing that the C_8PA layer is present at all temperatures. With increasing C_8PA growth temperature from 25 to 150°C, the water contact angle decreases from 113.5°±1.4° to 107.9°±0.8° and an increase in the surface roughness from 0.36 to 0.54 nm is observed. When combined with the FTIR results, this indicates low surface coverage by C_8PA molecules at high deposition temperature. At lower C_8PA growth temperatures AFM reveals different features in the AlO_x/C_8PA surface topography, suggesting a growth variation with the deposition temperature.

From Figure 6.3(a) it can be observed that the increase in C_8PA growth temperature from 25 to 125°C leads to a minor increase in the capacitance value, correlated with a negligible increase in the C_8PA surface roughness, and a decrease in the water contact angle. Even though the change in the C_8PA growth temperature from 25 to 125°C leads to gradual minor deterioration of the C_8PA material properties, the best dielectric properties are obtained at the lowest growth temperature of 25°C. A large increase in the capacitance occurs for C_8PA grown at 150°C, accompanied by a larger increase in the C_8PA surface roughness and a decrease in the water contact angle. This is an indication of a much reduced coverage of AlO_x with C_8PA molecules, supported by the overall reduction in the integral

intensity of all vibration bands associated with C_8PA. According to Hauffman et al. [65], low monolayer coverage is related to a ‘‘lying down’’ phase, while high coverage leads to a ‘‘standing up’’ phase. The high capacitance value of C_8PA monolayer grown at 150°C supports the fact that C_8PA molecules are lying down while they are standing up for monolayer grown at 25°C. The monolayer thickness calculated from the capacitance value is ~1 nm for C_8PA grown at 25°C, while it is reduced to ~0.2 nm for C_8PA grown at 150°C.

C_8PA monolayer grown at 25°C also leads to the lowest leakage current as shown in Figure 6.4. The higher growth temperature results in slightly larger leakage current density. This is most likely the consequence of a more disordered and/or thinner C_8PA monolayer.

All of the measured material characteristics: water contact angle, RMS surface roughness of AlO_x, molecular ordering of aliphatic tails and chemisorption of C_8PA on AlO_x surface are well correlated. They confirm that AlO_x/C_8PA surface with C_8PA grown at 25°C exhibits the highest water contact angle, the lowest surface roughness, and the best molecular ordering. The lowest leakage current density is also obtained at 25°C, indicating that the leakage current density can be lowered through improved C_8PA growth. Thus the improvement of vacuum vapour-phase self-assembly of alkyl phosphonic acids becomes the key requirement in the OTFT optimization process.

As shown in Figure 6.5 and Figure 6.6, pentacene-based OTFTs with bare AlO_x and AlO_x/C_8PA bi-layer dielectric exhibit good transistor behaviour in the linear and saturation regimes. However, when comparing OTFTs with the same contact geometries (Figure 6.5(a) and Figure 6.6(a)), three-time higher on-current is

observed for transistors implementing AlO_x/C_8PA if compared to the reference AlO_x OTFTs. The leakage current density of the bi-layer dielectric is also lower than that of bare AlO_x. The capacitance of AlO_x and AlO_x/C_8PA at 25°C is 0.57 and 0.43 $\mu F/cm^2$, respectively. The higher capacitance of AlO_x should lead to larger OTFT drain-current (equations (2.14) and (2.16)) when compared to AlO_x/C_8PA OTFTs. Since the opposite behaviour is observed experimentally, this could occur only if the AlO_x/C_8PA bi-layer dielectric leads to higher field-effect mobility. The average field-effect mobilities are 0.060 and 0.023 cm^2/Vs for AlO_x/C_8PA and AlO_x OTFTs, respectively. The increase in the OTFT on-current is related to pentacene growth on AlO_x/C_8PA when compared to AlO_x surface. The same pentacene deposition conditions resulted in different pentacene morphology on AlO_x/C_8PA and AlO_x as shown in Figure 6.9(a) and (c), respectively. Previously Ashall et al. [31] reported that AlO_x, $AlO_x/C_{18}PA$, and AlO_x/PMMA dielectrics exhibit different pentacene morphology irrespective of the same pentacene growth parameters. Their observation is consistent with our findings.

Pentacene morphology is also dependent on the surface roughness and molecular ordering within the SAM [11, 75]. The results show that C_8PA growth temperature affects pentacene morphology. The average pentacene grain size on AlO_x/C_8PA is around 300 nm, larger than that reported in the Chapters 4 and 5, although not yet fully optimized. This is likely a result of the increased substrate temperature during pentacene deposition compared to previous experiments. The largest pentacene grain size for C_8PA grown at 25°C is correlated with the lowest surface roughness, highest water contact angle, and more ordered C_8PA SAM. In the previous chapter, improvements in C_8PA growth were obtained with longer

desorption time which led to the maximum field-effect mobility. Here, the best molecular ordering at 25°C results in the highest field-effect mobility of ~0.060 cm^2/Vs. The reduction in the field-effect mobility at higher C_8PA growth temperature is correlated with smaller pentacene grains that are a likely consequence of the increased dielectric surface roughness. A slight increase in the field-effect mobility of OTFTs as compared to the previous chapter is a result of increased pentacene grain size.

Higher C_8PA growth temperature leads to an increase in the threshold voltage while the subthreshold slope is not affected. The lowest threshold voltage is achieved for OTFTs with C_8PA grown at 25°C. Comparing threshold voltages of all OTFTs one would infer that low C_8PA molecular coverage with lying down aliphatic tails leads to higher threshold voltage. For C_8PA grown at 150°C this threshold voltage is even higher than that of the reference AlO_x OTFTs.

In the previous chapter, a decrease in the subthreshold slope with increasing desorption time was observed. This chapter shows that within the standard deviations the subthreshold slope does not change with C_8PA growth temperature. The mean value is however slightly increasing with rising C_8PA growth temperature, indicating a minor increase in the trap density at the semiconductor/dielectric interface.

The surface and structural properties of C_8PA grown at 25°C are similar to those obtained in the previous chapter for C_8PA with 210-minute desorption. Therefore, the increase in the field-effect mobility and decrease in the threshold voltage are consequence of the pentacene deposition at higher substrate temperature. Therefore, in the next chapter the effect of pentacene growth temperature is studied using optimized C_8PA growth.

6.7 Conclusion

The effect of substrate temperature on C_8PA self-assembly using a vacuum vapour deposition was studied. C_8PA coverage and molecular ordering on top of AlO_x depend on the C_8PA growth temperature. The properties of the AlO_x/C_8PA dielectric and the OTFT performance are also influenced by the C_8PA growth temperature. The material properties (WCA, FTIR, and AFM) of AlO_x/C_8PA are correlated with their electrical behaviour in MIM and OTFT structures.

C_8PA monolayer grown at 25°C resulted in the smallest AlO_x/C_8PA surface roughness of 0.36 nm, the largest water contact angle of 113.5°±1.4° and the best molecular ordering. At the same time, the AlO_x/C_8PA with C_8PA grown at 25°C led to the lowest leakage current density of ~7×10^{-8} A/cm^2 at –2 V, the capacitance of 0.43 µF/cm^2, the highest OTFT mobility of ~0.060 cm^2/Vs and the lowest threshold voltage of –1.19 V. The increase in C_8PA growth temperature led to higher AlO_x/C_8PA surface roughness, smaller water contact angle, and lower molecular ordering. Also, the AlO_x/C_8PA dielectrics with C_8PA deposited at elevated substrate temperature led to higher leakage current density, higher capacitance, lower OTFT mobility, and higher threshold voltage. For C_8PA deposited at 150°C, low molecular coverage with lying down aliphatic tails was observed.

Chapter 7

Pentacene growth temperature

In Chapter 4, the effect of pentacene evaporation rate and purity on OTFT performance was studied for pentacene grown at room temperature. In the subsequent Chapters 5 and 6 the vacuum vapour self-assembly of C_8PA was understood in terms of C_8PA annealing time and growth temperature. In this chapter the effect of substrate temperature during pentacene growth on OTFT performance and pentacene morphology is presented. The substrate temperature was varied from 55°C to 80°C while the deposition rate was kept at 0.24 Å/s.

Section 7.1 reviews the effect of C_8PA self-assembly on the growth of organic semiconductor and the corresponding OTFT performance. Section 7.2 describes the device fabrication. Sections 7.3 and 7.4 present the results of MIM and OTFT structures, respectively. Section 7.5 discusses the experimental findings and finally the summary is given in Section 7.6.

7.1 Introduction

The growth of pentacene is sensitive to the surface properties of the underlying layer. In the case of bi-layer dielectrics (metal-oxide and organic monolayers), SAM ordering, alkyl chain-lengths [11, 41, 43, 93] and terminating groups [75] influence pentacene growth and OTFT performance. The larger grain size was observed for the intermediate chain length of ~10-14 carbon atoms [11, 41, 43, 75]. In addition, in solution-processed self-assembled monolayers, the growth of pentacene was found to be sensitive to the deposition temperature [43, 55].

When studying the effect of C_8PA annealing on the OTFT performance (Chapter 5), the longest C_8PA annealing time resulted in smaller pentacene grains of ~150 nm but the highest field-effect mobility. In that case pentacene was grown at room temperature. When studying the effect of C_8PA growth temperature on the OTFT performance (Chapter 6), the lowest C_8PA deposition temperature resulted in highest field-effect mobility and largest pentacene grain size of ~300 nm. In that case pentacene was deposited at an elevated substrate temperature of 70°C. Consequently, the field-effect mobility increased from 0.036 to 0.061 cm^2/Vs when the pentacene growth temperature was raised from 25 to 70°C. Therefore, this chapter aims to explore the effect of pentacene growth temperature on its morphology and OTFT performance while keeping the C_8PA growth the same.

The effect of substrate temperature during pentacene growth is studied in the temperature range from 55 to 80°C while its deposition rate is kept at 0.24 Å/s. Based on the experimental findings presented in the previous chapters, the C_8PA monolayer is grown at room temperature and subsequently annealed for 3 hours at 160°C. Electrical properties of MIM and OTFT structures are measured and the

device performance is analysed. Pentacene morphology is studied with AFM. The correlation between the channel/contact resistance, pentacene morphology and OTFT performance is discussed.

7.2 Device fabrication

Six different OTFT samples and the corresponding MIM structures were prepared. The OTFTs were fabricated side by side with the exception of the pentacene which growth temperature was varied between samples. The temperature range was between 55°C and 80°C with an increment of 5°C. Aluminium oxide followed the same preparation method as in Chapters 5 and 6.

The growth of pentacene is sensitive to the underlying dielectric and, therefore, to avoid the effect of C_8PA variation on the pentacene growth, the dielectric layer of all OTFTs and MIM structures was prepared at the same time. The thickness of pentacene was 50 nm and the evaporation rate was 0.24 Å/s. After pentacene deposition, 50-nm-thick gold source/drain contacts were evaporated on all structures at the rate of ~3 Å/s.

7.3 Results: MIM structures

The mean and standard deviation of the capacitance measured for the MIM structures is 0.45±0.01 μF/cm^2. The leakage current density is ~10^{-7} A/cm^2. Both of these values are similar to the values obtained in the previous experiments (Sections 5.4 and 6.4), indicating the reproducibility of the dielectric properties.

7.4 Results: OTFTs

Section 7.4.1 includes examples of the measured OTFT transfer characteristics. The threshold voltage and field-effect mobility, off-current and on/off current ratio, and subthreshold slope as functions of pentacene deposition temperature are presented in Sections 7.4.2-7.4.4, respectively. Finally, the effect of pentacene growth temperature on the channel and contact resistance and pentacene morphology is explained in Section 7.4.5 and 7.4.6, respectively.

7.4.1 Transfer characteristics

The transfer characteristics of OTFTs with pentacene deposited at substrate temperatures of 55°C and 80°C are depicted in Figure 7.1(a) and (b), respectively. Both OTFTs have the same contact geometry. The drain current at $V_{GS} = V_{DS} = -2.0$ V is 0.59 μA and 0.44 μA for pentacene grown at 55°C and 80°C, respectively.

7.4.2 Threshold voltage and field-effect mobility

Figure 7.2(a) shows the threshold voltage of OTFTs as a function of the pentacene growth temperature. The variation in the threshold voltage for all deposition temperatures is small. The threshold voltage of all OTFTs lays between -1.05 and -1.20 V. The minimum value of -1.05 V is achieved at 55°C while the maximum of ~ -1.17 V is found at 65°C. The threshold voltage of OTFTs with 210-minute C_8PA desorption is ~ -1.45 V (Chapter 5), while the OTFTs shown above exhibit threshold voltage of ~ -1.10 V. The reduction in the threshold voltage is a consequence of the increased growth temperature of pentacene.

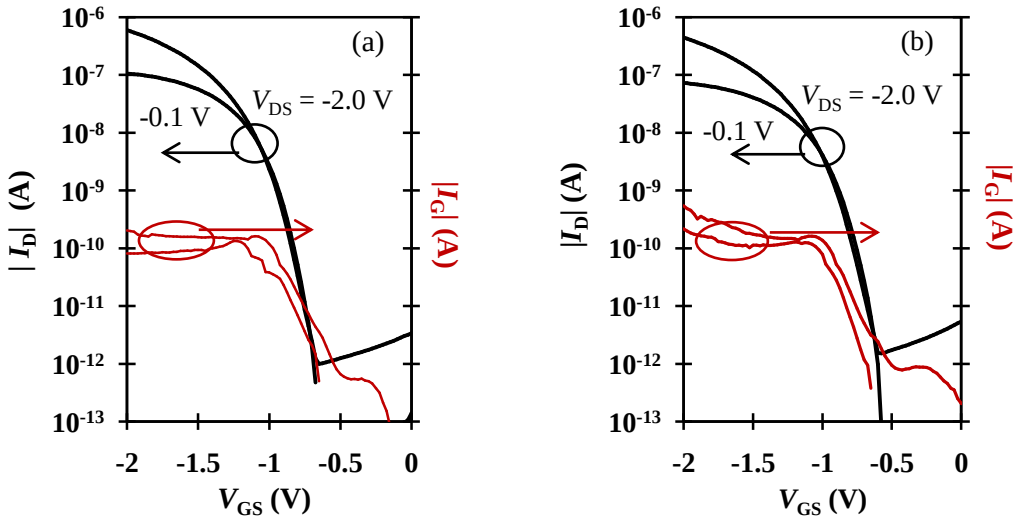

Figure 7.1: Transfer characteristics of OTFTs with L = 22 µm and W = 1000 µm. Substrate temperature during pentacene growth is 55 (a) and 80°C (b).

Figure 7.2(b) shows the mean and standard deviation of the OTFT field-effect mobility as a function of pentacene growth temperature. The mobility is 0.063±0.024 cm^2/Vs at 55°C, the maximum among all substrate temperatures. The mobility decreases with increasing substrate temperature and reaches the minimum value of 0.034±0.004 at 70°C. Pentacene growth temperatures of 75 and 80°C resulted in a mobility of 0.050±0.004 and 0.047±0.015 cm^2/Vs, respectively. These values are higher than the mobilities obtained for 60, 65, and 70°C but lower than the one obtained for 55°C.

7.4.3 Off-current and on/off current ratio

The mean and standard deviation of the off-current is shown in Figure 7.2(c). The off-current is ~1×10^{-12} A with the exception of OTFTs with pentacene grown at

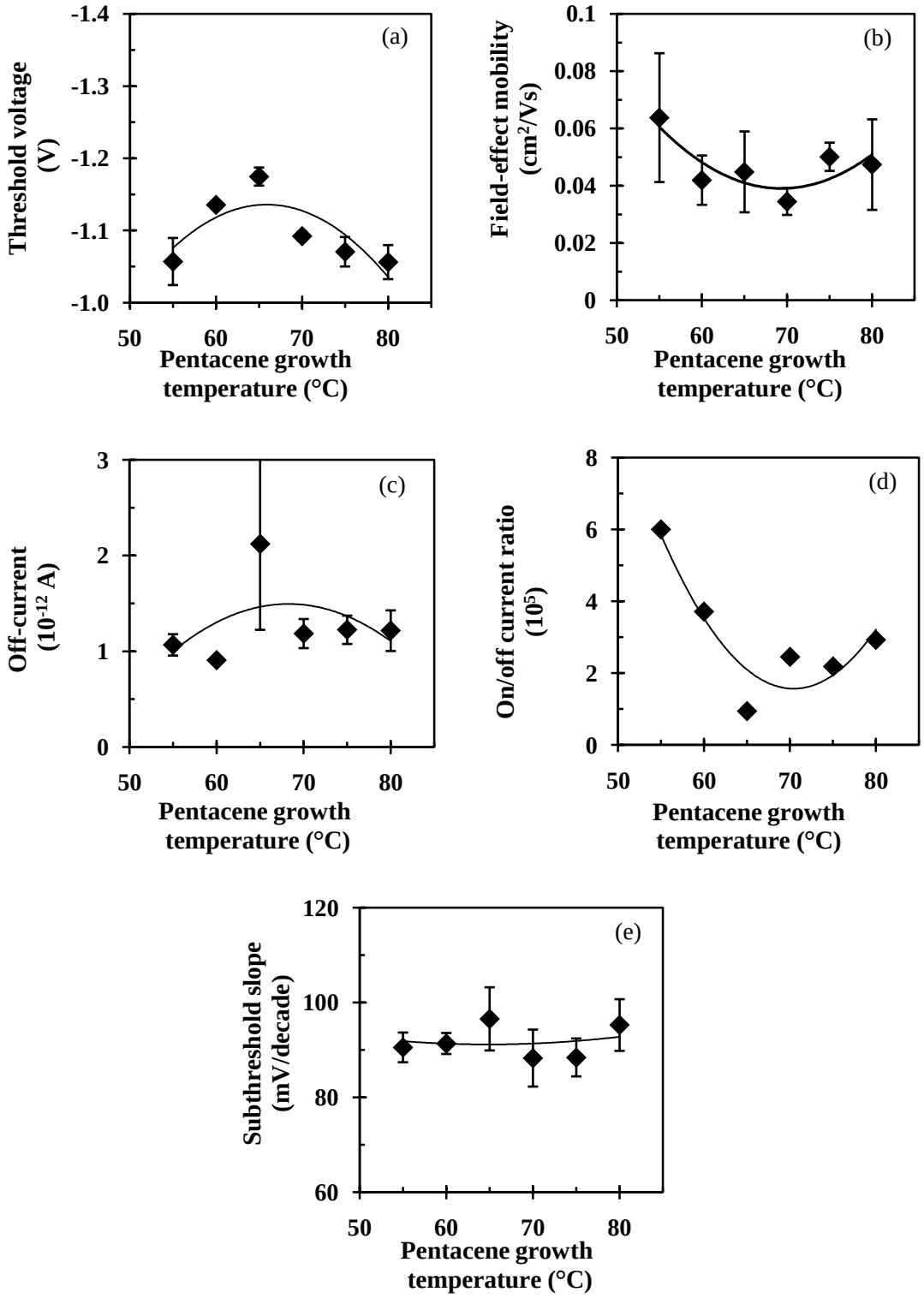

Figure 7.2: OTFT threshold voltage (a), field-effect mobility (b), off-current (c), on/off current ratio (d), and subthreshold slope (e) as functions of substrate temperature during pentacene deposition.

65°C. Figure 7.2(d) shows the on/off current ratio of OTFTs with channel length of 22 μm. The ratio is higher than 10^5 for all deposition temperatures except 65°C. The maximum on/off current ratio is 6×10^5 at the temperature of 55°C. This ratio is lowered for higher substrate temperatures.

7.4.4 Subthreshold slope

The OTFT subthreshold slope as a function of pentacene growth temperature is presented in Figure 7.2(e). The mean value of the subthreshold slope is about 90 mV/decade for all deposition temperatures. In summary, the off-current and subthreshold slope do not change appreciably with pentacene growth temperature.

7.4.5 Channel and contact resistances

In this section the channel and contact resistances are presented as a function of pentacene growth temperature with the exception of 65°C. Due to large variation in the OTFT performance at 65°C, this point is not included in the analysis. Figure 7.3(a) and (b) show the channel resistance per unit channel length and the contact resistance as a function of pentacene growth temperature, respectively.

The minimum R_{ch} is 2.4×10^4 Ω/μm at a pentacene growth temperature of 55°C. The value increases with increasing substrate temperature up to 70°C and further increase in the temperature leads to a decrease in R_{ch}. As expected, R_c does not change significantly with pentacene deposition temperature, averaging a value of 0.53±0.03 MΩ for all growth temperatures.

R_{ch} was 9.2×10^4 Ω/μm (Section 4.1.2.5) for OTFTs with pentacene deposited at room temperature; the elevated pentacene deposition temperature leads to lower

R_{ch}. To understand the behaviour of R_{ch}, the pentacene morphology measured by AFM is presented next.

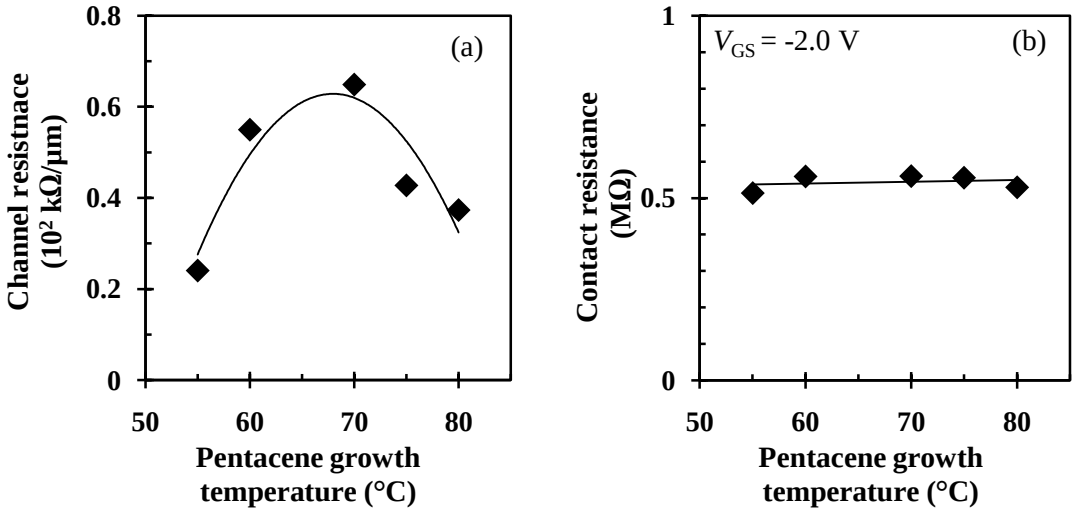

Figure 7.3: The OTFT channel resistance per unit channel length (a) and contact resistance (b) as functions of pentacene growth temperature.

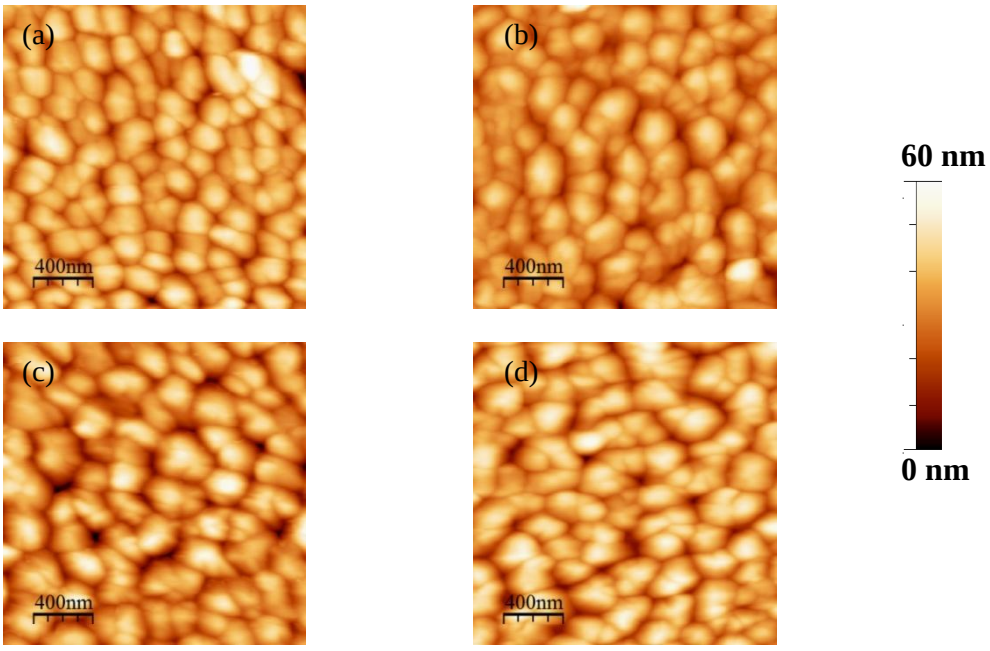

Figure 7.4: AFM surface topography of pentacene deposited at substrate temperature of 55 (a), 60 (b), 65 (c), and 75°C (d).

7.4.6 AFM

AFM surface image of pentacene deposited at substrate temperature of 55, 60, 65, and 75°C is shown in Figure 7.4(a)-(d), respectively. The pentacene grain size increases with increasing substrate temperature. On the other hand, the grain boundaries are more pronounced at higher temperatures of 65 and 75°C when compared to 55 and 60°C.

7.5 Discussion

Prior to the C_8PA optimization, the effect of pentacene evaporation rate and purity on OTFT performance was studied and presented in Chapter 4. At that time, pentacene was deposited at room temperature. This chapter studied the effect of pentacene growth temperature in combination with the optimized C_8PA layer. The difference in the transfer characteristics with substrate temperature during pentacene deposition can be seen in Figure 7.1. The change in the growth temperature from 55 to 80°C reduced the on-current from 0.59 to 0.45 μA; a reduction of 33%. As shown in Figure 5.7, the on-current is 0.15 μA for OTFT with pentacene deposited at room temperature and the same transistor geometry. Thus the on-current is increased four times when pentacene growth temperature is increased from room temperature to 55°C.

In Chapter 4 the subthreshold slope and off-current were found to be independent of the pentacene evaporation rate when more purified pentacene was used, while the threshold voltage was decreasing with increasing evaporation rate for the four-time purified pentacene. Here, negligible changes in these parameters were observed with changing pentacene growth temperature with the exception of

65°C(see Figure 7.2). However, the subthreshold slope is about 10 mV/decade smaller and $|V_t|$ is ~0.2 V lower. Both, the decrease in the subthreshold slope and threshold voltage are a result of the higher pentacene growth temperature.

The field-effect mobility varies between 0.063and ~0.038 cm^2/Vs when the substrate temperature is raised from 55 to 80°C. The mobility decreased when the growth temperature was raised from 55 to 70°C and then slightly increased between 75 and 80°C. The highest mobility was obtained at pentacene growth temperature of 55°C. Compared to the room temperature growth (Chapter 5), the OTFT field-effect mobility is doubled for the same C_8PA layer. In Chapter 6, the value of 0.060 cm^2/Vs of the field-effect mobility obtained for OTFTs with pentacene grown at 70°C is similar to the value of 0.063 cm^2/Vs obtained here for the substrate temperature of 55°C.

In summary, the optimized pentacene growth temperature is ~55-60°C for the chosen pentacene deposition rate of 0.24 Å/s. In fact, other groups also reported the best OTFT performance when the pentacene was deposited at substrate temperature of ~60°C on alkyl phosphonic acids [18, 41, 75].

As mentioned above, all OTFTs exhibit similar off-current except for OTFTs with pentacene deposited at substrate temperature of 65°C. The higher on-current or field-effect mobility resulted in the highest on/off current ratio 6×10^5 at pentacene growth temperature of 55°C. The on/off current ratio is around 2.5 times higher than for OTFTs with pentacene deposited on similar C_8PA layer at room temperature (Chapter 5). This on/off current ratio is higher than the one achieved for the OTFTs operating within 2-3 V [11, 22, 97] and lower than the one obtained for HfO_2/C_nPA (n = 6-18) [18, 43].

The contact resistance of 0.53±0.03 MΩ is independent of pentacene growth temperature varied between 55 and 80°C. In Chapter 4 the contact resistance was 1.54±0.41 MΩ for pentacene deposited at room temperature. Clearly, the elevated substrate temperature is preferred over the room temperature; a fact observed by many others.

While the contact resistance does not change with elevated pentacene growth temperature, the channel resistance does. The lowest channel resistance of 2.4×10^4 Ω/μm is obtained at the temperature of 55°C, a value that is four times lower than R_{ch} obtained for pentacene grown at room temperature. The total resistance of OTFT is directly proportional to R_{ch} and therefore a lower value is sought. The higher channel resistance for the intermediate temperature range (65-75°C) can be consequence of the poorly connected pentacene grains.

Pentacene grain size is ~300-400 nm for all growth temperatures (Figure 7.4) with a slight increase in the grain size at higher substrate temperature. However, the grains are more tightly connected at 55°C. Overall, the grain size is increased two-fold when compared to the room temperature deposition; but yet smaller than the one achieved by others for similar deposition conditions [18, 41, 75]. The lower field-effect mobility can result from smaller grain size or loose packing of grains. The tighter connection between grains at 55°C resulted in higher field-effect mobility [55, 58], even though the grain size is slightly smaller.

7.6 Conclusion

The effect of pentacene grown at elevated substrate temperature was studied. Compared to the room temperature growth, the optimized pentacene growth

temperature resulted in lower OTFT threshold voltage and improved field-effect mobility and on/off current ratio. The maximum field-effect mobility of 0.063 cm^2/Vs and on/off current ratio of 6×10^5 was achieved for pentacene growth temperature of 55°C. In addition, the minimum channel resistance was obtained at 55°C, resulting in the lowest total resistance since the contact resistance was not affected by the growth temperature.

The pentacene morphology changes with pentacene growth temperature. The tightly packed smaller pentacene grains lead to higher field-effect mobility when compared to larger, loosely-packed grains. Consequently, pentacene deposition would be performed at 55°C in the future experiments.

Chapter 8

Effect of evaporation rate on vapour-phase assembly of C_8PA

The effect of C_8PA desorption time and growth temperature are summarized in Chapters 5 and 6, respectively. In this chapter the effect of C_8PA evaporation rate on its vapour-phase self-assembly is studied. The C_8PA self-assembly procedure incorporates the optimized desorption time of 3 hours and growth temperature of 25°C, while the C_8PA evaporation rate is varied. In addition, based on the pentacene optimization experiments presented in Chapters 4 and 7, the pentacene deposition rate and substrate temperature are 0.24 Å/s and 55°C, respectively.

Section 8.1 summarizes the process parameters used for the C_8PA self-assembly. Fabrication of the structures and devices is described in Section 8.2. The results from the surface and structural characterizations are included in Section 8.3. The electrical performance of MIM and OTFT devices is presented in Section 8.4 and 8.5, respectively. The experimental findings are discussed and compared to those presented in previous chapters in Section 8.6. Finally, Section 8.7 concludes the chapter.

8.1 Introduction

A layer corresponding to several C_8PA monolayers is deposited in vacuum and subsequently heated to remove the physisorbed molecules. As seen in Chapters 5 and 6, the number of chemisorbed C_8PA molecules is mainly affected by the growth temperature, while the post-deposition desorption/annealing affects the structure of the monolayer. The remaining parameter that can be easily controlled during the thermal evaporation is the evaporation rate. Therefore, this chapter presents the effect of C_8PA evaporation rate on the C_8PA self-assembly and OTFT performance.

In the thermal evaporation process, layer growth and structure depend on the evaporation rate. The effect of pentacene, gold, and aluminium evaporation rate on OTFT performance was studied in Chapter 4. Here, experimental data confirms that the C_8PA monolayer is also affected by its evaporation rate. C_8PA evaporation was done at rates of 0.3, 1, 3, and 10 Å/s. The C_8PA growth temperature was fixed at 25°C and the post-deposition annealing lasted for 3 hours.

WCA and FTIR data provide information about C_8PA surface and structure. The electrical measurements of MIM and OTFT devices were conducted to

understand the effect of C_8PA evaporation rate on their electrical characteristics. The surface morphology of pentacene grown on C_8PA monolayer deposited at various rates is also presented.

8.2 Sample/device fabrication

Samples for WCA and FTIR characterization were prepared together on a glass substrate. Aluminium gate and AlO_x were prepared in the same manner as described in Chapters 5 to 7. C_8PA evaporation followed next and each sample underwent evaporation at a different rate, followed by a 3-hour desorption/annealing step used in Chapters 6 and 7. The evaporation rates of C_8PA were 0.3, 1, 3, and 10 Å/s. A reference AlO_x sample (no C_8PA layer) was also prepared.

The dielectric layers of the MIM and OTFT structures were prepared in the same manner. In the OTFTs, the pentacene was evaporated at the rate of 0.24 Å/s at a substrate temperature of 55°C. The MIM structures were fully masked during pentacene deposition. Both the MIM and OTFT structures were completed by evaporating a 50-nm-thick gold.

8.3 Results: surface and structural properties

This section presents WCA and FTIR measurements of the reference AlO_x and AlO_x functionalized with C_8PA deposited at different rates.

8.3.1 WCA

Table 8.1 shows WCA of reference AlO_x and AlO_x/C_8PA for C_8PA evaporated at 0.3, 1, 3, and 10 Å/s. The contact angle of AlO_x/C_8PA is higher than

109° for all rates, confirming the presence of C_8PA on top of AlO_x. The reference AlO_x has contact angle of 21.8±0.2°, a highly hydrophilic surface. There is not much variation in WCA with C_8PA evaporation rate. Nevertheless, the maximum contact angle of 112.1±0.5° was obtained for the rate of 1 Å/s.

In the previous experiment, the WCA of AlO_x/C_8PA for C_8PA deposited at substrate temperature of 25°C was 113.5±1.4°. The value obtained in this experiment is 112.1±0.5° under the same C_8PA preparation condition. Both values are the same within the error measurement. WCA of the reference AlO_x surface is lower than that obtained in the previous chapters (Section 5.3.1 and 6.3.1). However, its surface properties are more likely to dependent on the sample history, air humidity, etc. (Section 6.3.1).

Table 8.1: Water contact angle of AlO_x/C_8PA as a function of C_8PA evaporation rate. The reference AlO_x is also included.

C_8PA evap. rate (Å/s)	WCA(°)
0.3	111.5 ± 0.3
1	112.1 ± 0.5
3	109.3 ± 0.6
10	109.9 ± 1.3
Aluminium oxide	21.8 ± 0.2

8.3.2 FTIR

Figure 8.1(a) shows the Al−O−P stretching mode near 1100 cm^{-1} resulting from the chemisorption of phosphonic acid to aluminium oxide. The spectra coincide for all evaporation rates except 10 Å/s. Compared to those shown in Figures 5.4(a) and 6.2(a) one can observe the narrowing of the peak near 1060 cm^{-1} and appearance of a peak near 1160 cm^{-1}. Both of these originate in the reference AlO_x/Al/glass

sample that exhibits slightly different absorbance than that shown in Figure 6.2(a). However, there is a good correlation of the Al−O−P band among similar samples (compare the absorbance for 3 Å/s in Figure 8.1(a) to that of 210-minute desorption in Figure 5.4(a) and 25°C deposition in Figure 6.2(a)). The Al−O−P absorbance for C_8PA deposited at 10 Å/s is shifted to higher wavenumbers and its integral intensity is similar to that for lower deposition rates. The broad absorbance peak of the reference aluminium oxide near 1100 cm^{-1} reflects the presence of Al−OH groups. The intensity of this peak is reduced when compared to AlO_x shown in Figure 6.2(b), even though both were prepared in a similar way.

Figure 8.1(b) shows the peaks corresponding to P=O bonds. Here, the reference AlO_x sample shows stronger absorbance in the region between 1220 and 1250 cm^{-1}, a feature previously not observed (see Figure 6.2(b)). Similarly to previous FTIR measurements, C_8PA adds absorbance at ~1204, 1226, and 1244 cm^{-1}. The variation in C_8PA evaporation rate mostly affects the absorbance at 1226cm^{-1}, leading to reduced integral intensity with increasing evaporation rate. The peak at 1263 cm^{-1} resulting from the methyl groups was previously similar for AlO_x and AlO_x/C_8PA layers, leading to the belief that it is associated with ambient methane (Figures 5.4(b) and 6.2(b)). However, Figure 8.1(b) shows stronger absorbance of AlO_x/C_8PA at 1263 cm^{-1} when compared to AlO_x. Consequently, better understanding of AlO_x absorbance peaks is needed in the future.

Figure 8.1(c) shows the FTIR spectra in the region of 2700-3100 cm^{-1} corresponding to the symmetric/asymmetric stretching modes of CH_2/CH_3 groups.

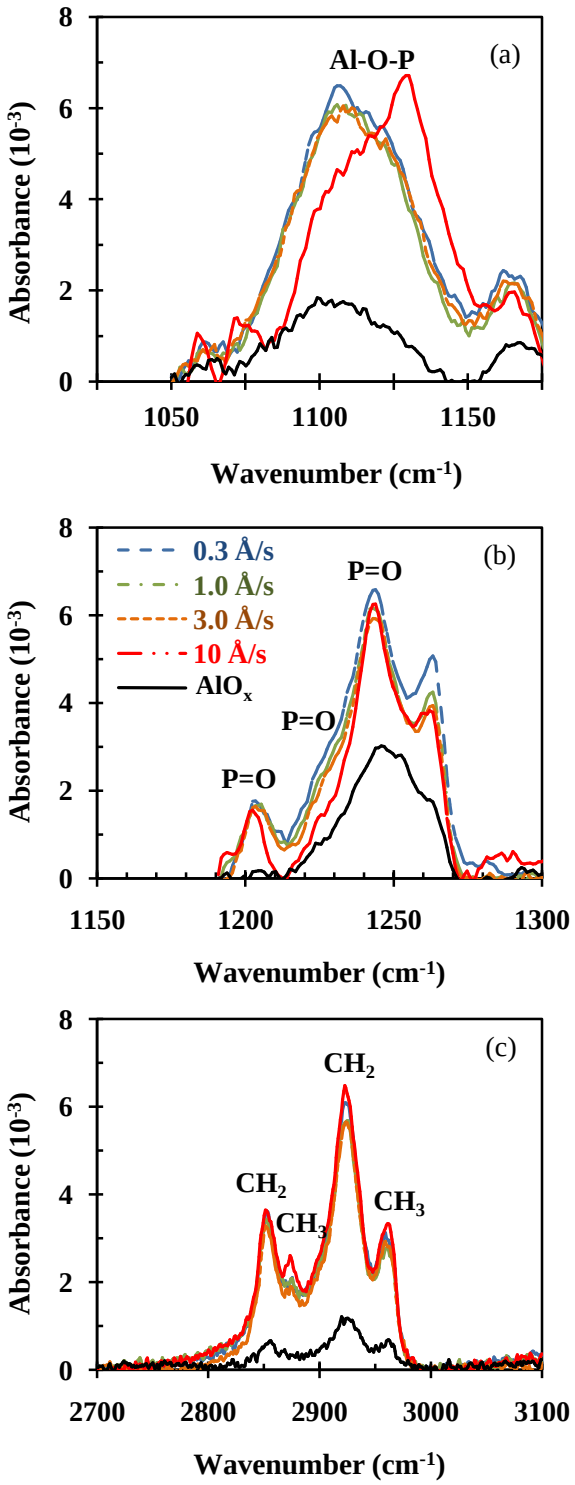

Figure 8.1: FTIR spectrum of AlO_x/C_8PA with C_8PA deposited at the rate of 0.3, 1, 3, and 10 Å/s. The reference AlO_x is shown as well.

The centre positions of these peaks are the same as those obtained in Sections 5.3.3 and 6.3.3. When comparing the amplitude of the peaks for changing deposition rate, slightly higher values are observed for C_8PA evaporation rates of 0.3 and 10 Å/s than 1 and 3 Å/s. Full width at half maximum (FWHM) of the CH_2 asymmetric stretching mode is similar for 0.3 and 1 Å/s. It is increased by 1 cm^{-1} for 3 Å/s and subsequently reduced by 3 cm^{-1} for 10 Å/s. On the other hand, the FWHM of the CH_2 symmetric stretching mode shows a very minor increase with increasing C_8PA evaporation rate. Consequently, none of the studied C_8PA evaporation rates indicates a clear improvement in themolecular alignment within the monolayer, although minor changes in the absorbance peaks are observed.

In summary, the FTIR measurements confirm the formation of Al−O−P bonds and the presence of surface aliphatic chains (see WCA measurement) for all C_8PA evaporation rates. The changing evaporation rate leads only to minor changes in the FTIR spectra of the organic monolayer.

8.4 Results: MIM structures

The capacitance and the leakage current density of AlO_x and AlO_x/C_8PA MIM structures and the extracted thickness of C_8PA monolayer are described next.

8.4.1 Capacitance

Figure 8.2(a) shows the capacitance of AlO_x/C_8PA dielectric as a function of C_8PA evaporation rate. The capacitance changes slightly with C_8PA evaporation rate with values between 0.45 and 0.48 µF/cm^2. The reference AlO_x (no C_8PA layer) dielectric has capacitance of 0.66 µF/cm^2.

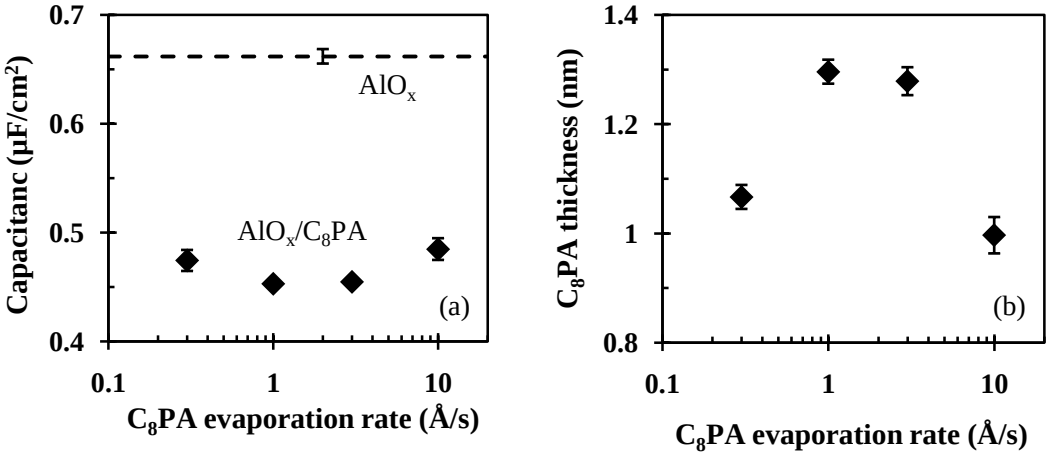

Figure 8.2: Capacitance per unit area of AlO_x/C_8PA (a) and C_8PA thickness (b) as functions of C_8PA evaporation rate. The dashed line corresponds to the reference AlO_x capacitance.

8.4.2 AlO_x and C_8PA thickness

The thickness of aluminium oxide calculated from its capacitance value is 9.0 nm. The change in C_8PA thickness with evaporation rate is shown in Figure 8.2(b). At the evaporation rates of 0.3 and 10 Å/s the thickness is ~1.05 nm. It increases slightly to ~1.25 nm for evaporation rates of 1 and 3 Å/s.

Previously, thickness larger than a monolayer was obtained for the short desorption of 25 minutes. Less than a monolayer thickness was observed for C_8PA deposited at elevated substrate temperatures. The remaining C_8PA self-assembly conditions led to the thickness corresponding approximately to a monolayer.

8.4.3 Leakage current density

Figure 8.3 shows the leakage current density of both reference AlO_x and bi-layer AlO_x/C_8PA dielectrics. Aluminium oxide has leakage current density of ~10^{-6} A/cm^2 at –3 V and it reduces to ~10^{-7} A/cm^2 after it is functionalized with C_8PA. The

current density of AlO_x/C_8PA does not change much with C_8PA evaporation rate; although a marginal decrease is observed with increasing evaporation rate. In addition, the values are comparable to those obtained in Sections 5.4.3 and 6.4.3.

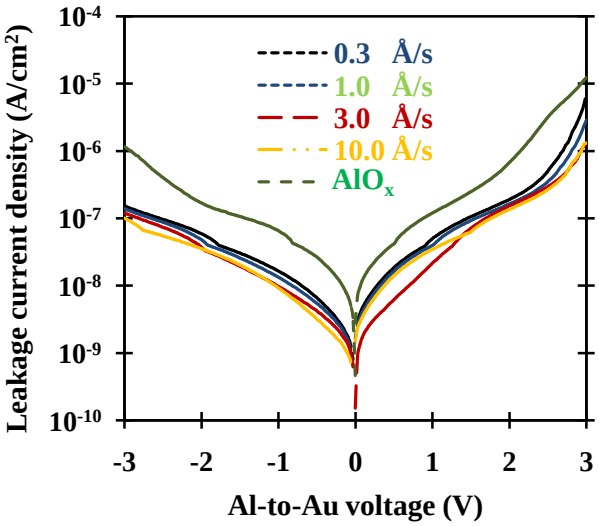

Figure 8.3: Leakage current density of AlO_x and AlO_x/C_8PA MIM structures.

C_8PA evaporation rate has only weak effect on the wetting and structural properties of AlO_x/C_8PA bi-layer. Although minor changes in the capacitance, C_8PA thickness, and leakage current density are observed, the C_8PA evaporation rate does not have a large effect on these properties. Overall, no clear correlation with the evaporation rate is observed.

8.5 Results: OTFTs

The transistor characteristics and parameters of $Al/AlO_x/C_8PA$/pentacene/Au OTFTs as functions of C_8PA evaporation rate are presented next. The effect of C_8PA evaporation rate on the pentacene morphology is also shown.

8.5.1 Transfer characteristics

Figure 8.4 shows the transfer characteristics of transistors with 25-µm channel length and C_8PA evaporated at rates of 0.3 and 1 Å/s. The on-current is 0.07 and 0.13 µA for the rate of 0.3 and 1 Å/s, respectively, showing that the C_8PA evaporation rate affects the drain current of the transistor.

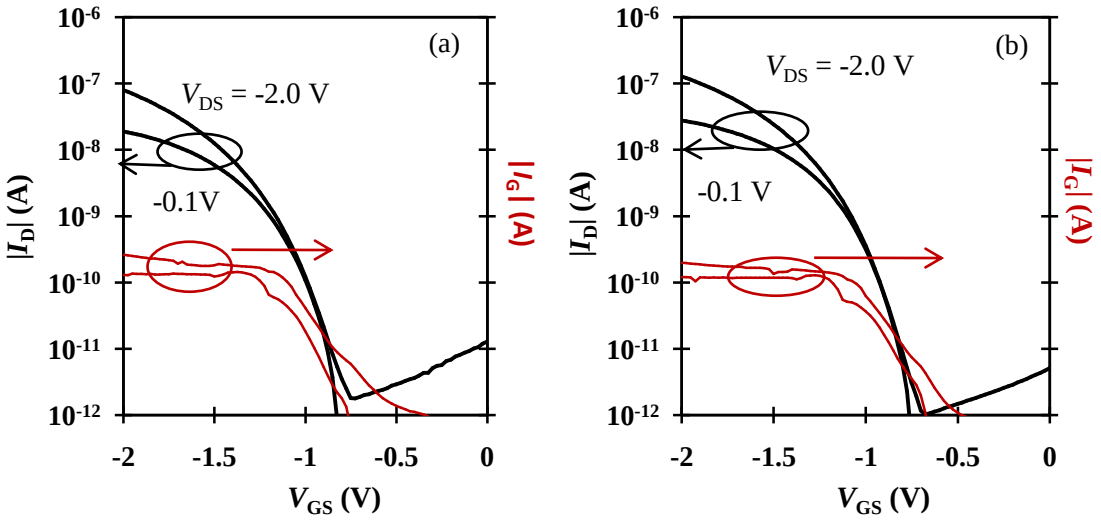

Figure 8.4: Transfer characteristics of OTFTs with C_8PA deposited at 0.3 (a) and 1 Å/s (b). The channel length and width are 25 and 1000 µm, respectively.

8.5.2 Field-effect mobility and threshold voltage

The mean and standard deviation of the OTFT field-effect mobility and threshold voltage as functions of C_8PA evaporation rate are shown in Figure 8.5(a) and (b), respectively. The mobility increases from 0.012 to 0.024 cm^2/Vs when C_8PA evaporation rate is increased from 0.3 to 1 Å/s and it remains more or less constant after that. In this experiment a new pentacene material was used and it was deposited by using the optimized conditions obtained from the previous experiment (Chapter 7). Nevertheless, the field-effect mobility is lower than that achieved in Chapter 7.

This is attributed to the pentacene source material that affected the remaining transistor parameters as well.

The threshold voltage decreases with increasing C_8PA evaporation rate. It changes from −1.21 to −1.07 V when the evaporation rate rises from 0.3 to 10 Å/s. The threshold voltage of ~−1.15 volts is similar to that obtained in Chapter 6. The new pentacene material resulted in lower field-effect mobility and drain current, while the threshold voltage was maintained.

8.5.3 Off-current and on/off current ratio

Figure 8.5(c) shows the mean and standard deviation of the off-current of OTFTs as function of C_8PA evaporation rate. The off-current is ~1×10^{-12} A for all evaporation rates within the error of measurement. The values are similar to the ones obtained in previous chapters, while the on-current is lower. Consequently, the on/off current ratio of OTFTs with L = 25 μm (Figure 8.5(d)) is also reduced when compared to previous OTFTs. The larger value of the off-current for 3 Å/s resulted in lower on/off current ratio, otherwise the ratio increases with increasing C_8PA evaporation rate.

8.5.4 Subthreshold slope

The mean and standard deviation of the OTFT subthreshold slope is shown in Figure 8.5(e). The mean value is about 120 mV/decade for all evaporation rates, although a marginally lower values are seen for 1 and 3 Å/s. The higher value of the subthreshold slope, as compared to the previous experiment, indicates the presence of more traps at the semiconductor/dielectric interface.

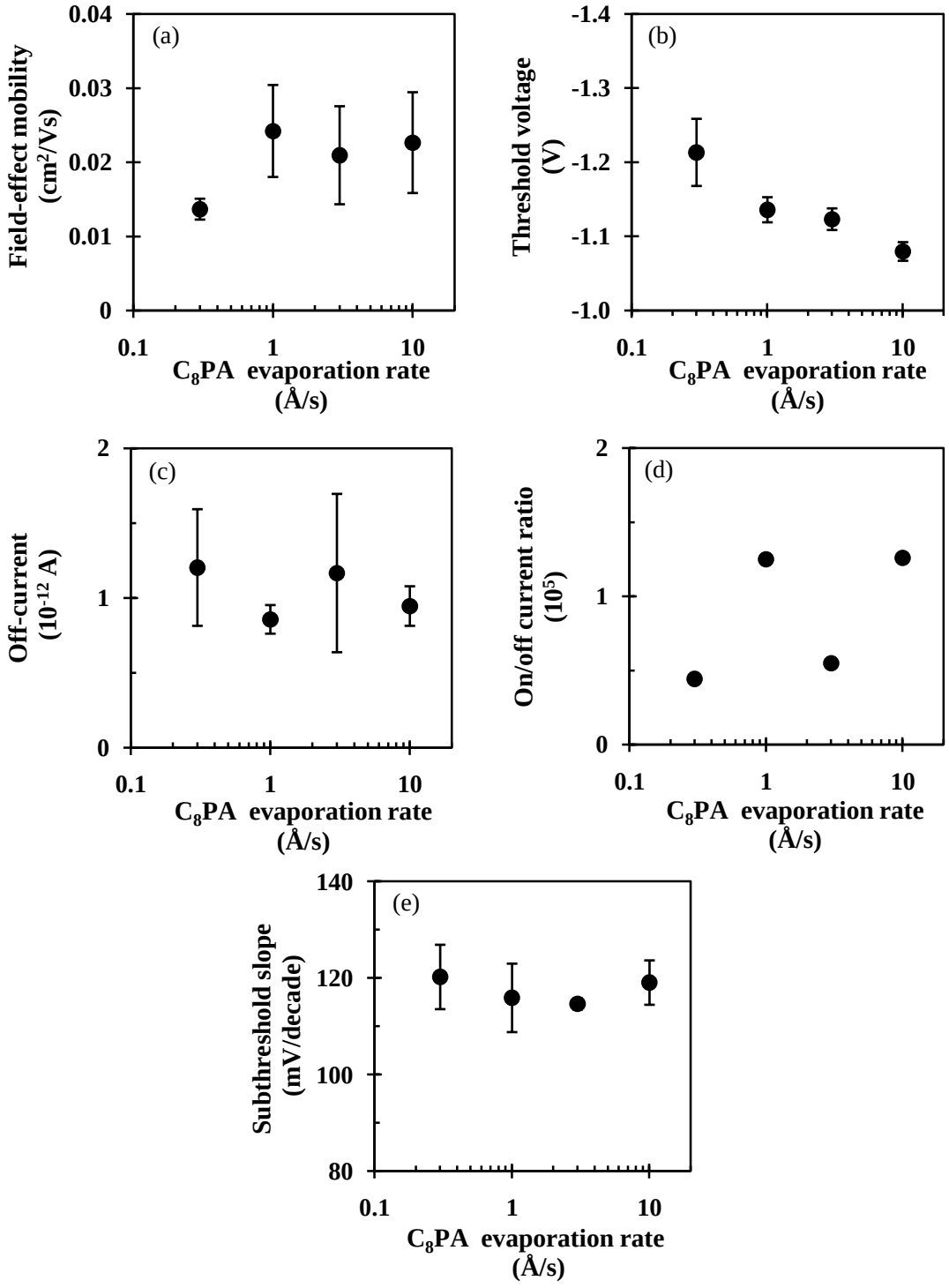

Figure 8.5: Field-effect mobility (a), threshold voltage (b), off-current (c), on/off current ratio (d), and subthreshold slope (e) of OTFTs as functions of C_8PA evaporation rate.

8.5.5 Pentacene morphology

Morphology of pentacene deposited on C_8PA evaporated at 0.3, 1, 3, and 10 Å/s is shown in Figure 8.6(a)–(d), respectively. The grain size increases from ~100 nm to ~300 nm as the C_8PA evaporation rate increases.

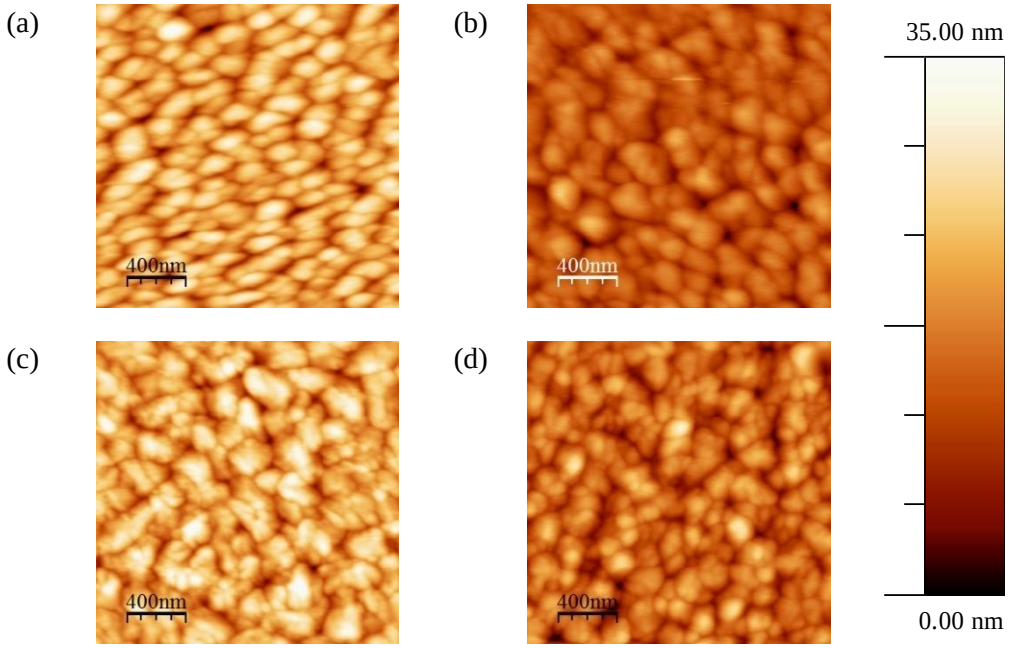

Figure 8.6: AFM surface image of pentacene deposited on C_8PA evaported at 0.3 (a), 1 (b), 3 (c), and 10 Å/s (d).

8.6 Discussion

The value of the water contact angle (>109°) shows the presence of C_8PA molecules on top of AlO_x for all evaporation rates. There is no clear dependence between WCA and C_8PA evaporation rate and WCA values are similar to those obtained in Chapters 5 and 6 and during the solution self-assembly [42].

The FTIR measurements confirm the formation of Al−O−P bonds for all C_8PA evaporation rates (absorbance peak near 1100 cm^{-1} is similar to that observed

in Chapters 5 and 6), even though the absorbance peak for the highest evaporation rate of 10 Å/s is shifted to higher wavenumbers. Weak absorbance is observed in the region from 1200 and 1250 cm^{-1} that corresponds to P=O bonds. The absorbance at 1204 cm^{-1} is not changing with the evaporation rate and is similar to that observed in Chapters 5 and 6. The intensity of the peaks near 1226 and 1244 cm^{-1} is slightly higher than that observed in Chapters 5 and 6. However, this is affected by the increased absorbance from the reference AlO_x for these wavenumbers. The position and FWHM of the absorbance peaks corresponding to the symmetric/asymmetric stretch of CH_2/CH_3 are similar to those reported in Chapters 5 and 6. Overall, the changing evaporation rate leads only to minor changes in the FTIR spectrum.

In Chapters 5 and 6 the capacitance of the reference AlO_x was 0.63 and 0.57 $\mu F/cm^2$, respectively. The value obtained in this experiment is 0.66 $\mu F/cm^2$. The small deviation in the capacitance value from run to run confirms that the thickness of AlO_x prepared by UV/ozone oxidation of aluminium is reproducible within about ±5%.

For evaporation rates of 0.3 and 10 Å/s the AlO_x/C_8PA capacitance is ~0.48 $\mu F/cm^2$, while it is 0.45 $\mu F/cm^2$ for 1 and 3 Å/s. The calculated C_8PA thickness is 1.06 and 1.00 nm for 0.3 and 10 Å/s, respectively. The intermediate evaporation rates of 1 and 3 Å/s lead to C_8PA thickness of 1.29 and 1.27 nm, respectively. As mentioned in Chapter 5, the monolayer thickness is around 1.1 nm. Here, the mean thickness of 1.15±0.15 nm was obtained.

The leakage current density of AlO_x/C_8PA is ~10^{-7} A/cm^2 and it increases to ~ 10^{-6} A/cm^2 for AlO_x. The leakage current density of the bi-layer is similar to that obtained in Chapters 5 and 6.

Along with a slight decrease in the leakage current density with increasing C_8PA evaporation rate, the threshold voltage is also reduced. The lowest threshold voltage of –1.07 V is obtained for the highest evaporation rate of 10 Å/s. It is the minimum threshold voltage obtained in all of the experiments. The evaporation rates of 1 and 3 Å/s lead to threshold voltage of ~–1.12 V, a value similar to that obtained for 25°C growth temperature and 180-minute desorption in Chapter 6.

The off-current exhibits similar values to those obtained in previous experiments. The off-current was reduced from $\sim 5\times10^{-12}$ A to $<1\times10^{-12}$ A when the C_8PA desorption time increased from 25 to 210 minutes (Chapter 5). Values around 1×10^{-12} A were obtained in Chapters 6 and 7 and similar values are found here. The on/off current ratio is lower than that obtained in previous experiments. However, this is a result of reduced transistor on-current.

OTFT results suggest that C_8PA deposited at moderate to high rates ranging from 1 to 10 Å/s leads to comparable OTFT performance, while the lowest rate of 0.3 Å/s leads to slightly higher threshold voltage and lower field-effect mobility.

The structural, surface, and electrical properties of AlO_x/C_8PA are found to be reproducible. OTFT off-current and threshold voltage are also similar to the values found in previous experiments. However, the field-effect mobility is the lowest among all experiments. It appears to be a consequence of the environmentally-degraded pentacene source material. The results of Chapter 4 show that pentacene purity affects the field-effect mobility, on/off current ratio, and subthreshold slope, while the threshold voltage and off-current are not visibly affected. These findings suggest that the higher subthreshold slope and lower field-

effect mobility found in this experiment are correlated with deteriorated pentacene purity.

The variation in C_8PA desorption time and growth temperature led to changes in pentacene morphology and subsequently, in OTFT parameters. Here, the effect of C_8PA evaporation rate on pentacene morphology is shown in Figure 8.6. The largest grain size was obtained for pentacene deposited on top of C_8PA evaporated using intermediate rates of 1 and 3 Å/s. The OTFT drain currents scale with the pentacene grain size.

8.7 Conclusion

The effect of C_8PA evaporation rate on AlO_x/C_8PA surface, structural, and electrical properties, and OTFT performance was studied. The surface, structural, and electrical properties of AlO_x/C_8PA were found to be well correlated to the previous experiments. In addition, the changing C_8PA evaporation rate led only to minor changes in these properties with no clear indication that certain evaporation rates would lead to improved properties overall. However, the analysis of the OTFT performance suggests that medium to high evaporation rates ranging from 1 to 10 Å/s lead to slightly better transistor parameters. The minimum leakage current density and threshold voltage were achieved for C_8PA evaporated at 10 Å/s. However, it is quite difficult to achieve such high evaporation rate in the existing Minispectros system. Consequently, rates of 1 Å/s and higher are more suitable for C_8PA evaporation in the future, leading to a decrease in $|V_{th}|$ by ~ 0.06 V.

Chapter 9

Bias-stress effect

The changes in the C_8PA monolayer structure with desorption/annealing, growth temperature and deposition rate were presented in Chapters 5, 6, and 8, respectively. These chapters also described the effect of C_8PA structure on the performance of as-fabricated OTFTs. This chapter presents the effect of bias stress on the OTFTs presented in Chapters 5, 6, and 8. In addition, it seeks the correlation between the C_8PA structure and the kinetics of the bias-induced degradation.

The bias-induced degradation of the threshold voltage, subthreshold slope, field-effect mobility, and the on-current of the transistors presented in Chapter 5 is described in Section 9.2. The effect of C_8PA growth temperature (Chapter 6) and deposition rate (Chapter 8) on the bias-induced transistor degradation is presented in Section 9.3 and 9.4, respectively. Section 9.5 gives the discussion of the experimental findings. Finally, Section 9.6 summarizes the correlation between the bias-induced transistor degradation and the C_8PA microstructure.

9.1 Introduction

There is a general agreement that alkyl phosphonic acids with shorter aliphatic tails form more disordered monolayers than phosphonic acids with longer tails. Nevertheless, the performance of the transistors varies widely when such monolayers assembled from solution are implemented in OTFTs. While studying the effect of the aliphatic chain length (C_6PA–C_{18}PA) on thin-film transistors, Acton et al. [43] obtained the highest mobility and low threshold voltage for HfO_2/C_nPA/pentacene transistors using C_8PA. This coincided with the largest pentacene grain size and a large disorder between aliphatic tails of C_8PA monolayer. Fukuda et al. [11] observed the highest as-fabricated field-effect mobility, threshold voltage and on/off current ratio for AlO_x/C_nPA/pentacene transistors implementing C_{14}PA monolayer for which the largest pentacene grain size was observed. However, when transistors with C_{14}PA and C_{18}PA monolayers were subjected to similar bias stress, a slightly smaller decrease in the drain current with bias stress was observed for transistors with C_{18}PA, in which the pentacene grain size was smaller and the order between the aliphatic tails should have been better. Hill et al. [41] performed similar experiment and achieved the best transistor performance for C_8PA monolayer. In addition, they obtained similar mobilities and threshold voltages for transistors with C_6PA and C_{14}PA monolayers, even though the grain size of pentacene grown on these two monolayers was vastly different. These results point to the fact, that both the pentacene morphology and the structure of the alkyl phosphonic monolayer affect the performance of the as-fabricated transistors and their long-term bias stability. This is in agreement with the results from poly(3-hexylthiophene) OTFTs that show that the gate dielectric plays a more critical role in

the transistor bias-induced degradation process and, in fact, the degradation in the transistor on-current can be separated into charge trapping in the semiconductor-side and the gate-dielectric-side of the semiconductor/dielectric interface [99].

In Chapter 5, a solution-free growth of C_8PA monolayer using vacuum thermal evaporation was demonstrated. In addition, the effect of C_8PA growth temperature and rate were presented in Chapter 6 and 8, respectively. These parameters exhibited a pronounced effect on the performance of the as-fabricated transistors, pointing to the importance of the monolayer microstructure in the charge carrier transport within the transistor. Shorter post-deposition annealing also resulted in C_8PA thickness larger than a monolayer (~ 1.5 monolayers), while the higher growth temperature (~150°C) led to thickness smaller than a monolayer, both mimicking the results obtained during the solution self-assembly [65]. Consequently, the developed dry process can be used as a tool for correlating the structural changes in the C_8PA monolayer with the long-term transistor performance, while eliminating the effect of possible solvent traces. Understanding this link comprises an important step toward stable OTFTs.

9.2 Effect of C_8PA desorption/annealing time on bias stress

From the FTIR data (Section 5.3.3) of C_8PA layer annealed for 25, 90, and 210-minutes, the amplitudes of the peaks corresponding to P=O bond and $C-H_2$ and $C-H_3$ stretch are reduced between the 25- and 90-min anneals and then marginally increased after the 210-min anneal. This reflects the removal of the physisorbed molecules in the initial stage of the desorption/annealing process, followed by the

improved ordering between the C_8PA molecules. In addition, the vibration of the phosphonate salts was shifted to lower wavenumbers in the early stage of the desorption process. Thus, the C_8PA desorption/annealing affects the monolayer structure.

The increasing C_8PA annealing time resulted in both higher gate dielectric capacitance (Figure 5.5(a)) and higher initial threshold voltage (Figure 5.8(b)). Consequently, the induced capacitive charge ($Q = C\,|\,V_{GS} - V_{th}\,|$) in the beginning of the transistor bias stress experiment was the same within ±5% for all C_8PA annealing times.

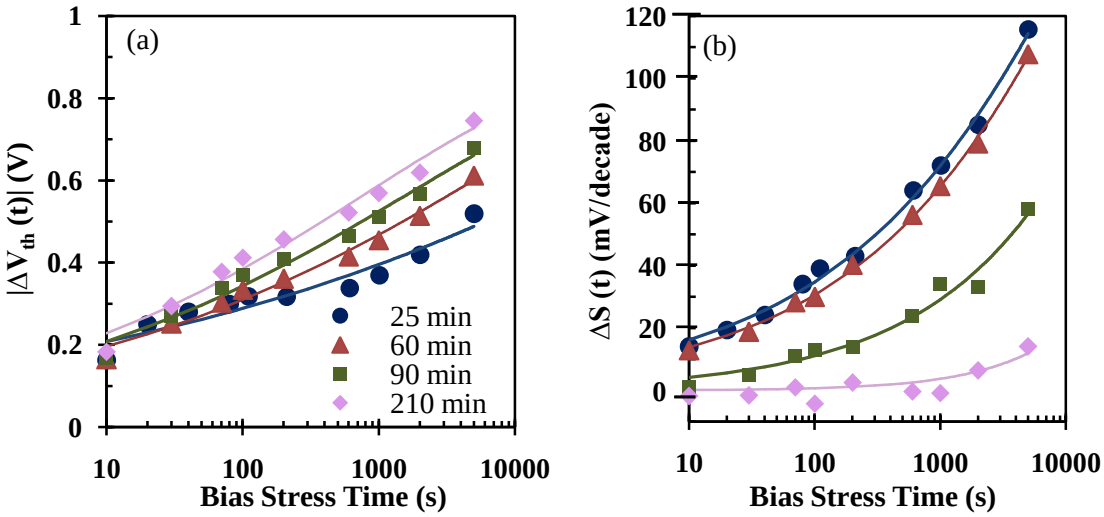

Figure 9.1: Change in the threshold voltage (a) and subthreshold slope (b) as functions of bias stress time and C_8PA annealing time.

9.2.1 Threshold voltage and subthreshold slope

Figure 9.1 shows the changes in the threshold voltage and subthreshold slope as functions of the bias stress time and C_8PA desorption/annealing. The curves

represent the least-square fits of the data points to the stretched-exponential functions given by Eqs. (3.5) and (3.6).

The longest desorption time of 210 minutes resulted in the largest threshold voltage shift and the smallest change in the subthreshold slope. The values extracted from the stretched-exponential fits are included in Table 9.1. The time constant of the threshold voltage shift decreases with the rising C_8PA annealing time, while the stretching parameter increases. The stretched exponential fit presented for OTFTs with C_8PA annealed for 25 minutes should be taken with reservation, since its correlation factor R^2 is only 0.91.

Table 9.1: Time constants and stretching parameters obtained from Figure 9.1.

Desorption time (min)	τ_{Vth} (s)	β_{Vth}	τ_S (s)	β_S
25	3.3×10^6	0.15	4.0×10^4	0.35
60	8.8×10^3	0.23	7.0×10^4	0.36
90	1.6×10^3	0.26	5.3×10^6	0.42
210	7.5×10^2	0.28	3.7×10^{10}	0.72

The time constant and the stretching parameter of the subthreshold slope change depend strongly on C_8PA desorption/annealing time. As the annealing time rises from 25 to 210 minutes, the time constant increases from 4.0×10^4 s to 3.7×10^{10} s and the stretching parameter rises from 0.35 to 0.72.

9.2.2 Field-effect mobility and the on-current

Figure 9.2 depicts the changes in the normalized field-effect mobility and on-current as functions of bias stress time and C_8PA desorption/annealing. The longest

desorption time of 210 minutes resulted in the lowest reduction in the field-effect mobility and the fastest degradation of the on-current.

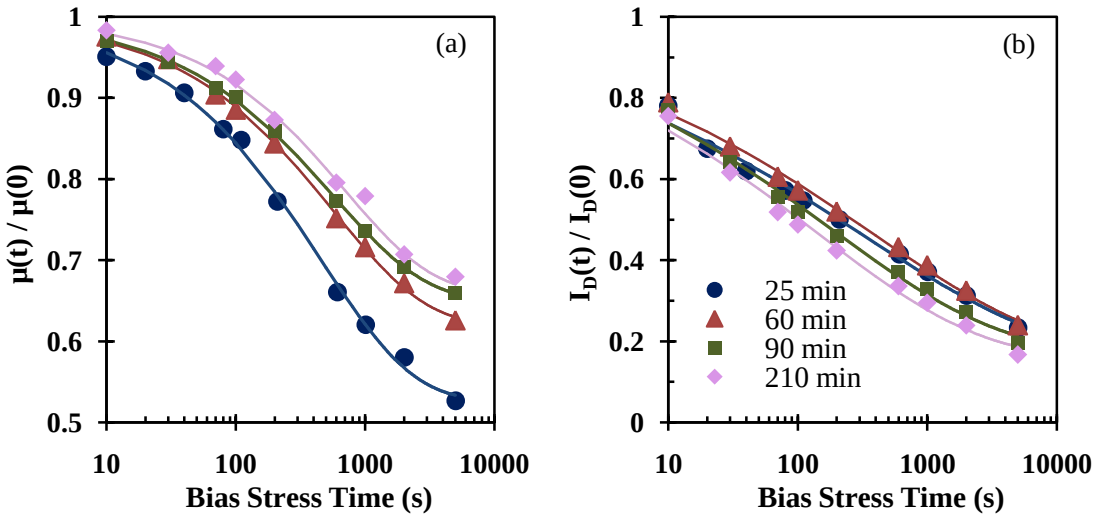

Figure 9.2: Normalized field-effect mobility (a) and on-current (b) as functions of bias stress time and C_8PA annealing time.

The curves depict the least-square fits of the data to the stretched-exponential functions (Eqs. (3.7) and (3.8)) and the extracted time constants and stretching parameters are presented in Table 9.2.

Table 9.2: Time constants and stretching parameters obtained from Figure 9.2.

Desorption time (min)	τ_μ (s)	β_μ	τ_{ID} (s)	β_{ID}
25	4.5×10^2	0.61	3.0×10^2	0.29
60	5.7×10^2	0.61	3.7×10^2	0.30
90	5.7×10^2	0.61	1.8×10^2	0.33
210	7.0×10^2	0.65	1.4×10^2	0.34

The drop in the field-effect mobility exhibits similar time constants for all C_8PA annealing time. The equilibrium value of $\frac{\mu(\infty)}{\mu(0)}$ is 0.53, 0.62, 0.65, and 0.67 for

C_8PA annealing times of 25, 60, 90, and 210 minutes, respectively. The increasing C_8PA desorption time leads to a slight decrease in the time constant of the normalized drain current and a small increase in the stretching parameter. The equilibrium value of $\frac{I_D(\infty)}{I_D(0)}$ is ~ 0.16 for all C_8PA desorption times, indicating that even though the structure of the monolayer (Section 5.3.3) affects the kinetics of the transistor degradation process, the same bias stress ultimately leads to the same normalized equilibrium drain current.

9.3 Effects of C_8PA growth temperature on bias stress

Section 6.3.3 showed the structural changes in C_8PA monolayer (FTIR data) with growth temperature. The chemisorption of fewer C_8PA molecules at higher substrate temperature was observed from the reduction in the integral intensity of all vibration peaks. This section shows how the C_8PA growth temperature influences the transistor behaviour under the prolonged bias stress. According to Figures 6.3(a) and 6.7(a), both the dielectric capacitance and the threshold voltage increase with the deposition temperature. Thus, the initial charge carrier density induced by the gate voltage of −3 V is similar in all OTFTs.

The OTFT with C_8PA grown at 25°C was bias-stressed three weeks after the other transistors due to technical difficulties with the measurement equipment. Consequently, the degradation of the normalized field-effect mobility may be affected as a result of progressed pentacene oxidation.

9.3.1 Threshold voltage and subthreshold slope

Figure 9.3 shows the changes in the threshold voltage and subthreshold slope as functions of bias stress time and C_8PA growth temperature. The threshold voltage shift decreases with the rising C_8PA growth temperature, while the change in the subthreshold slope increases. This finding agrees with that of Section 9.2.1, where the improvement in C_8PA molecular alignment led to reduced degradation of the subthreshold slope and an increased degradation of the threshold voltage.

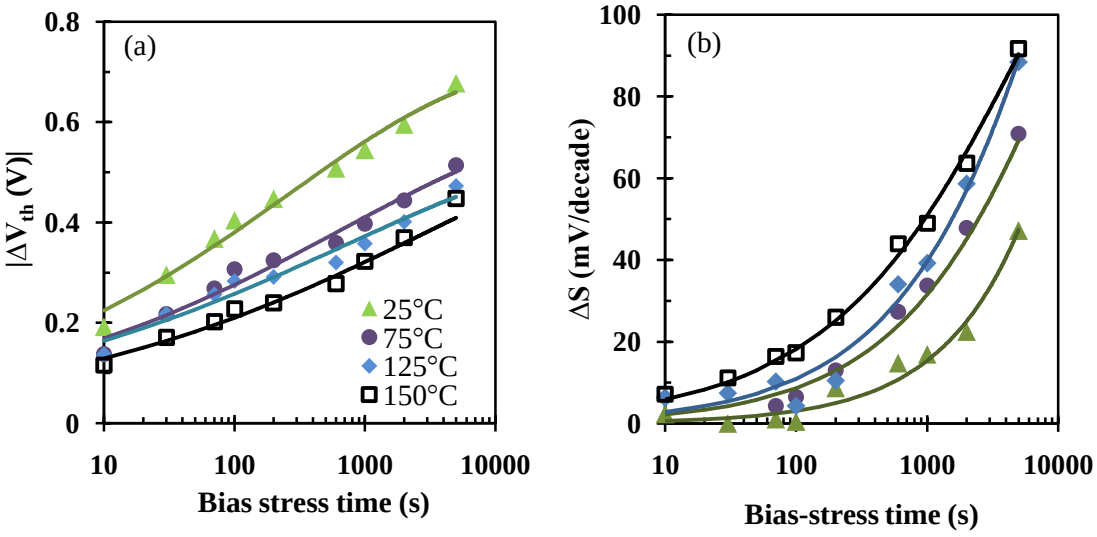

Figure 9.3: Change in the threshold voltage (a) and subthreshold slope (b) as functions of bias stress time and C_8PA growth temperature.

The time constants and stretching parameters obtained from the least square fit of the data of Figure 9.3 to Eqs. (3.5) and (3.6) are shown in Table 9.3. The time constant of the threshold voltage increases from 2.6×10^2 s to 2.9×10^3 s and the stretching parameter decreases from 0.30 to 0.25 when the C_8PA growth temperature is increased from 25 to 150°C. The values obtained for C_8PA grown at 25°C are in good agreement with those achieved in Section 9.2.1 for the 210-minute desorption.

Previously, in Section 9.2 the shorter annealing times also resulted in the longer time constant and smaller stretching parameter. Consequently, low C_8PA growth temperature and long annealing time result in better alignment between C_8PA molecules and tighter molecular packing that manifest themselves as larger stretching parameter and smaller time constant of the bias-induced shift in the threshold voltage.

The time constant of the subthreshold slope reduces from 9.5×10^{10}s to 5.0×10^{3} s and the stretching parameter from 0.70 to 0.51 upon rising the growth temperature from 25 to 150°C. Similar dependencies were observed in Section 9.2.1 with decreasing desorption time. The values obtained for C_8PA grown at 25°C are in good agreement with those achieved in Section 9.2.1 for the 210-minute desorption.

Table 9.3: Time constants and stretching parameters obtained from Figure 9.3.

Growth temp. (°C)	τ_{Vth} (s)	β_{Vth}	τ_S (s)	β_S
25	2.6×10^{2}	0.30	9.5×10^{10}	0.70
75	6.7×10^{2}	0.27	1.1×10^{4}	0.60
125	6.9×10^{2}	0.25	1.7×10^{4}	0.59
150	2.9×10^{3}	0.25	5.0×10^{3}	0.51

9.3.2 Field-effect mobility and the on-current

Figure 9.4 shows the normalized field-effect mobility and on-current as functions of transistor bias-stress time and C_8PA growth temperature. The degradation of the mobility and the on-current is the lowest for OTFTs with C_8PA grown at 25°C. The degradation of the normalized mobility is visibly reduced for C_8PA grown at 25°C and is likely affected by the delay in the bias-stress

measurement of that particular transistor. The equilibrium values of the normalized on-current are 0.16 for 25°C and ~0.08 for all higher growth temperatures. The higher equilibrium transistor on-current achieved for C_8PA grown at 25°C is affected by the smaller reduction in the mobility. Similar values achieved for 75, 125 and 150°C suggest that the C_8PA microstructure does not affect the equilibrium value, an observation similar to that found in Section 9.2.2.

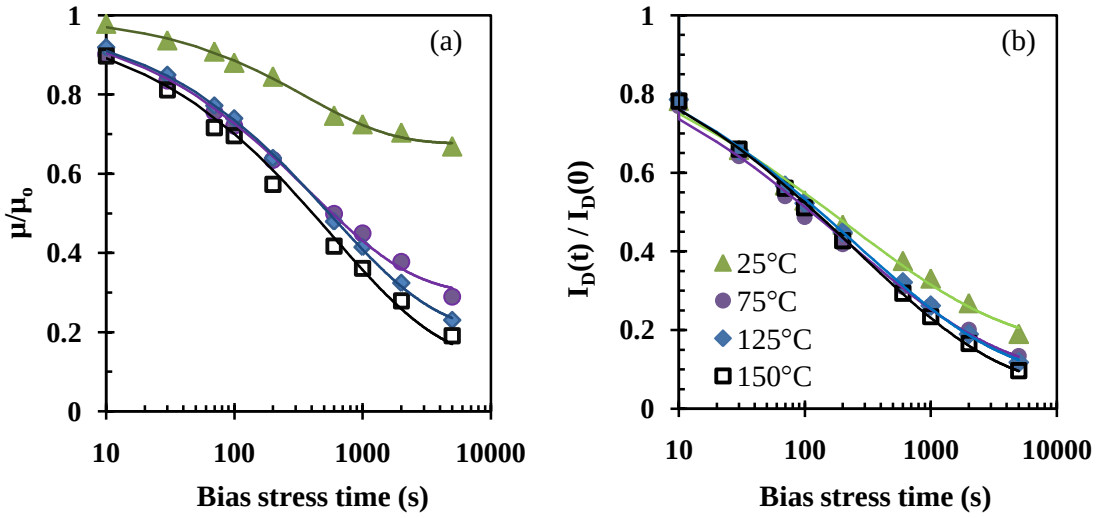

Figure 9.4: Normalized field-effect mobility (a) and on-current (b) as functions of bias stress time and C_8PA deposition temperature.

The stretched-exponential parameters of the normalized field-effect mobility and on-current are shown in Table 9.4. The mobility time constants are similar to those shown in Table 9.2. With the exception of 25°C, the stretching parameters are similar for all growth temperatures, although lower than those shown in Table 9.2. The stretching parameter of ~0.5 could be associated with higher pentacene growth temperature leading to larger pentacene grain size. The higher value of β_μ obtained at 25°C could result from more ordered C_8PA monolayer and/or the delay in the measurement. However, as one will see in Section 9.4.2, this value is similar to that

obtained in the following experiment for similar OTFT and it also matches the values obtained in Section 9.2.2.

Table 9.4: Time constants and stretching parameters obtained from Figure 9.4.

Growth temp. (°C)	τ_{μ} (s)	β_{μ}	τ_{ID} (s)	β_{ID}
25	3.6×10^{2}	0.65	2.2×10^{2}	0.34
75	3.8×10^{2}	0.53	2.2×10^{2}	0.35
125	5.6×10^{2}	0.53	2.6×10^{2}	0.37
150	5.7×10^{2}	0.50	2.6×10^{2}	0.38

For the on-current, both the time constant (τ_{ID}) and stretching parameter (β_{ID}) increase slightly with the C_8PA growth temperatures. This is in contrast to the values obtained in Section 9.2.2, where the stretching parameter increased for more ordered C_8PA layer. Nevertheless, the OTFT with C_8PA deposited at substrate temperature of 25°C and that with C_8PA annealed for 210 minutes (Section 9.2.2) exhibit similar stretching parameters and time constants.

9.4 Effect of C_8PA evaporation rate on bias stress

In Sections 9.2 and 9.3 the effect of C_8PA annealing time and growth temperature on bias-induced transistor instability was shown. This section presents the effect of C_8PA deposition rate on the bias-induced transistor degradation.

Since the capacitance of the gate dielectric was changing slightly, the bias-stress gate voltage was slightly adjusted for some OTFTs to produce the same initial charge carrier density regardless of the C_8PA growth rate.

9.4.1 Threshold voltage and subthreshold slope

Figure 9.5 shows the changes in the threshold voltage and subthreshold slope with bias stress time and C_8PA evaporation rate. V_{th} increases with the applied bias and the smallest threshold voltage shift occurs for the intermediate evaporation rate of 3 Å/s, while the largest shift occurs for the lowest evaporation rate of 0.3 Å/s. The subthreshold slope exhibits the smallest rise for the rates of 3 and 10 Å/s and a larger change is observed when the evaporation rate is decreased.

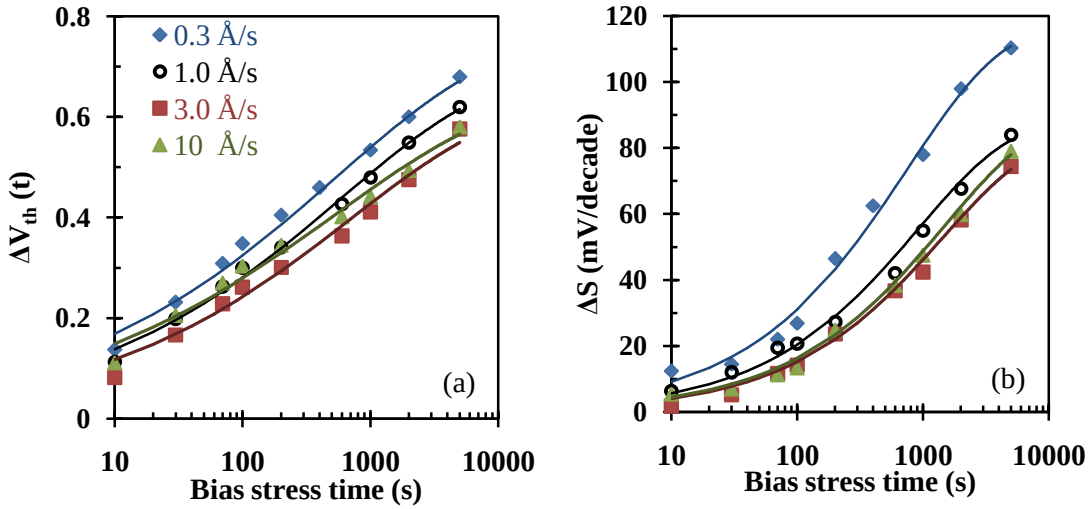

Figure 9.5: Change in the threshold voltage (a) and subthreshold slope (b) as functions of bias stress time and C_8PA evaporation rate.

The stretched exponential fits of the threshold voltage and subthreshold slope are indicated by the solid lines in Figure 9.5. τ_{Vth} is approximately the same for all evaporation rates and the variation in β_{Vth} is also small. Nevertheless, the highest values of β_{Vth} are achieved for medium evaporation rates of 1 to 3 Å/s. Similar is true for the time constant and the stretching parameter of the change in the subthreshold slope. Overall, the values of β_{Vth} are slightly higher than those in Tables 9.1 and 9.3.

Tables 9.3 and 9.1 show that C_8PA growth at 25°C and the post-deposition annealing for 210 minutes both lead to the largest stretching parameter of ~0.7 for the subthreshold slope. Here it is ~0.6 for all evaporation rates. The small differences in the stretching parameter for alike samples can be attributed to the variation in pentacene growth.

Table 9.5: Time constants and stretching parameters obtained from Figure 9.5.

Evap. rate (Å/s)	τ_{Vth} (s)	β_{Vth}	τ_S (s)	β_S
0.3	5.4×10^2	0.35	7.5×10^2	0.58
1.0	5.8×10^2	0.37	9.2×10^2	0.60
3.0	7.0×10^2	0.37	1.4×10^3	0.60
10.0	5.4×10^2	0.35	1.5×10^3	0.59

9.4.2 Field-effect mobility and the on-current

Figure 9.6 shows the changes in the on-current and field-effect mobility as functions of bias stress time and C_8PA evaporation rate. Both parameters decrease with bias-stress irrespective of the C_8PA evaporation rate. The equilibrium value of the normalized field-effect mobility is 0.41, 0.47, 0.48, and 0.52 for the evaporation rate of 0.3, 1, 3, and 10 Å/s, respectively, leading to the smallest overall drop for the rate of 10 Å/s.

The normalized values of the on-current after prolonged bias stress, in the order of increasing evaporation rate, are 0.11, 0.17, 0.19, 0.18. The largest reduction in the on-current is observed for the lowest evaporation rate of 0.3 Å/s, while the degradation is similar for all other evaporation rates.

The corresponding time constants and stretching parameters are listed in Table 9.6. τ_{ID} is ~10^2 and τ_μ ~10^3 s for all evaporation rates. β_μ is ~ 0.63 for

evaporation rates less than 10 Å/s and it increases to 0.70 for 10 Å/s. β_{ID} reaches the maximum value of 0.44 at the evaporation rates of 1 and 3 Å/s. Overall, the values of β_{ID} are higher than those in Table 9.2 and Table 9.4. This could be a consequence of using a new batch of pentacene and different pentacene deposition temperature.

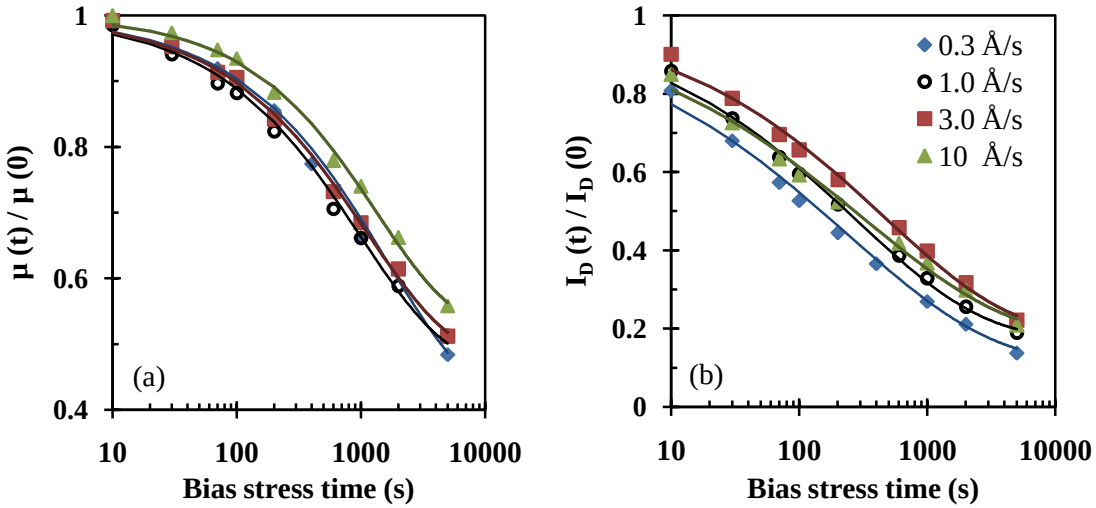

Figure 9.6: Normalized field-effect mobility (a) and on-current (b) as functions of bias stress time and C_8PA evaporation rate.

Table 9.6: Time constants and stretching parameters obtained from Figure 9.6.

Evap. rate (Å/s)	τ_{μ} (s)	β_{μ}	τ_{ID} (s)	β_{ID}
0.3	1.6×10^{3}	0.62	2.4×10^{2}	0.38
1.0	1.0×10^{3}	0.63	2.8×10^{2}	0.44
3.0	1.1×10^{3}	0.63	4.6×10^{2}	0.44
10.0	1.3×10^{3}	0.70	3.2×10^{2}	0.39

9.5 Discussion

Equations (3.5)-(3.7) assume different degradation kinetics for the threshold voltage, subthreshold slope and the field-effect mobility. In fact, it is possible that different factors affect the OTFT parameters in different manners. It was found that

the exposure of pentacene OTFTs to ambient atmosphere mainly lowers the field-effect mobility [100, 101] as a result of the oxidation of the central benzene ring of pentacene. This aging phenomenon does not affect the subthreshold slope but it leads to the reduction in the on-current and rise in the off-current [101]. In OTFTs based on semi-crystalline polythiophene the observed irreversible degradation in the subthreshold slope is unrelated to the threshold voltage shift [102].

In optimized field-effect transistors, the bias-induced degradation proceeds through the shift in the threshold voltage, while the changes in the mobility and subthreshold slope are negligible. However, if very large gate-source/drain voltage is applied, degradation in all transistor parameters is observed and this behaviour is not unique to OTFTs (refs. [103, 104] for transistors based on hydrogenated amorphous silicon). In the presented OTFTs the changes in all parameters are observed and this likely results from the high carrier concentration in the transistor channel if compared to other thin-film transistor technologies. Nevertheless, transistor optimization should aim to reduce the degradation in these parameters.

The stretched-exponential function dictates that while the initial degradation is faster-than-exponential, the degradation stops eventually, as one would expect in the case when the threshold voltage of the transistor approaches the gate bias voltage. The smaller the value of β, the faster is the initial degradation. Similarly the smaller is the time constant, the faster the final equilibrium value is achieved. Assuming that the degradation of various transistor parameters requires a channel formation near the semiconductor/dielectric interface, the degradation of the threshold voltage, subthreshold slope and the field-effect mobility would cease when the gate voltage is not high enough to cause the accumulation of holes.

As can be seen from Table 9.1 and Table 9.2, the stretching parameters of the normalized mobility, normalized on-current, threshold voltage shift and change in the subthreshold slope are increasing with the rising annealing time of C_8PA monolayer. The stretching parameters of all OTFT parameters, except the normalized on-current, are increasing with the reduction in C_8PA growth temperature (Table 9.3 and Table 9.4). When the C_8PA evaporation rate is varied, the stretching parameters peak at medium evaporation rate in the range of 1-3 Å/s (Table 9.5 and Table 9.6).

The larger value of β means a less-stretched exponential behaviour and the distribution of the trapping energies ΔE_T responsible for the degradation of any transistor parameter becomes narrower ($\Delta E_T = k_B T/\beta$ [99]). In other words, the microscopic environments at or near the semiconductor/dielectric interface become less varied. Consequently, the growth temperature of 25°C, medium evaporation rate of 1-3 Å/s and the 210-minute post-deposition annealing lead to microscopically least varied C_8PA monolayer (largest stretching parameters). This is in agreement with FTIR findings that show that these conditions lead to monolayers with the best molecular ordering.

Zschieschang et al. [100] observed a rise in the stretching parameter β_{Vth} from 0.29 to 0.42 as V_{DS} increased from 0 to 2 volts. Zhang et al. [28] and Gu et al. [105] obtained β_{Vth} ~0.4 for higher V_{DS}. Our transistors exhibit an increase in β_{Vth} with increasing C_8PA annealing time and decreasing C_8PA growth temperature, reaching a value of 0.28-0.30 for C_8PA grown at 25°C and annealed for 3-3.5 hours. This is similar to the value reported for zero V_{DS} in [100]. β_{Vth} reaches slightly higher value of ~0.36 for OTFTs with varied C_8PA evaporation. At the same time, the dependence of β_{Vth} on the deposition rate is small.

The change in pentacene growth temperature from 25°C (Section 9.2) to 65°C (Section 9.3) and 55°C (Section 9.4) resulted in the slight reduction in the threshold voltage shift, increase in the stretching parameter (β_{Vth}) and decrease in the time constant (τ_{Vth}). These differences may be attributed to different pentacene source material and different growth.

Contrary to the threshold voltage, the time constant of the subthreshold slope increases with the rising annealing time and decreasing substrate temperature, meaning that is takes longer to reach the equilibrium. The increase in the inverse subthreshold slope of the transfer characteristic with bias stress is typically associated with the generation of additional defect states at the semiconductor/dielectric interface. As the annealing progresses, the generation of such states is suppressed and their energy distribution becomes narrower. Similar effect is observed for higher C_8PA evaporation rates.

The time constants and the stretching parameters of the normalized mobility are neither particularly sensitive to C_8PA annealing time nor the growth temperature or rate suggesting that the primary factor controlling the mobility degradation is not the structure of the organic monolayer. In agreement with the previous observations it is believed that the oxidation of pentacene is the main factor and the minor variations in the pentacene morphology and the growth temperature may account for some differences in the reduction of the normalized mobility with the bias stress time [100, 106].

Finally, the degradation of the on-current is a combined effect of changes in the threshold voltage, mobility, and the subthreshold slope. C_8PA annealing time, deposition temperature, and deposition rate have only minor effect on the

degradation of the on-current. The equilibrium value of normalized on-current after the prolonged bias stress is ranging from 0.08 to 0.18 and is ~0.16 for similar C_8PA self-assembly.

The FTIR data (shown in Section 5.3.3) depicted that the increase in the desorption time from 25 to 90 minutes leads to the removal of the remaining physisorbed C_8PA molecules, while slightly increasing the disorder between the aliphatic tails and shifting the vibrations of the phosphonate salts to lower wavenumbers. Increasing the desorption time from 90 to 210 minutes primarily improved the molecular alignment within the organic monolayer. Similarly, the data in Section 6.3.3 revealed that higher substrate temperature led to less ordered and less dense C_8PA monolayer. The increased monolayer disorder manifests itself as reduced degradation of the subthreshold slope and normalized mobility and an increased degradation of the threshold voltage.

9.6 Conclusion

The bias-induced instability of low-voltage transistors based on pentacene and thin AlO_x functionalized with vapour-deposited n-octylphosphonic acid monolayer was studied as a function of C_8PA microstructure, where the C_8PA structural changes are induced by desorption time, growth temperature, and deposition rate. A strong correlation was uncovered between the degradation of the threshold voltage and subthreshold slope and the C_8PA microstructure, while the field-effect mobility seems to be primarily affected by the oxidation of pentacene [100].

Stretched-exponential functions were fitted to changes in the threshold voltage, subthreshold slope, and normalized field-effect mobility as functions of the bias stress time. The different time constants and stretching parameters suggest that these transistor parameters do not follow the same kinetics. Nevertheless, their stretching parameters are higher at longer desorption time, lower substrate temperature and moderate deposition rate of C_8PA. This implies that the time responses become less stretched and the distribution of the trapping energies responsible for the degradation of any transistor parameter becomes narrower. Consequently, the microscopic environments at or near the semiconductor/dielectric interface become less varied.

Finally, the bias stress experiments confirm that the optimum conditions for the vapour-phase self-assembly of C_8PA monolayer include the growth at 25°C, medium growth rate of 1-3 Å/s and the 210-minute post-deposition annealing.

Chapter 10

Conclusion and future work

Section 10.1 concludes all the experiments conducted in the thesis. The scope for future work is presented in Section 10.2.

10.1 Conclusion

In this thesis the vacuum, vapour-phase self-assembly of n-octylphosphonic acid monolayer on aluminium oxide was optimized. The correlation between the C_8PA growth temperature, evaporation rate, and post-deposition annealing and the properties of the monolayer were understood. The MIM structures and OTFTs based on pentacene and implementing such monolayers were investigated, including the bias-stress induced transistor instability. Experimental techniques such as FTIR, WCA, AFM, and comprehensive electrical measurements were employed. The effect of pentacene purity and deposition rate and temperature were also briefly studied.

The presence of C_8PA monolayer on top of AlO_x results in lowering of the dielectric capacitance from ~0.60 μF/cm^2 to ~0.45 μF/cm^2. The leakage current density is also lowered by an order of magnitude when the C_8PA monolayer is added on top of AlO_x and the current density of ~ 10-nm-thick AlO_x/C_8PA bi-layer is ~10^{-7} A/cm^2 at –3 V.

Both types of dielectric, aluminium oxide and AlO_x/C_8PA bi-layer, resulted in low-voltage OTFT operation below 2 V. When the bi-layer dielectric was used, the drain current was at least 3 orders of magnitude higher than the gate current, showing good insulating properties. The off-current of most of the OTFTs with bi-layer dielectric is ~10^{-12} A. The field-effect mobility is increased from 0.026 cm^2/Vs to 0.060 cm^2/Vs when aluminium oxide is functionalized with phosphonic acid. Thus, the higher on-current is achieved with bi-layer dielectric for the same operating voltage and these OTFTs can be used in electronic circuits. The low gate current reduces the power dissipation during the device operation and low off-current during the off-state of the device.

The developed vapour-phase self-assembly consists of two steps. Firstly, an approximately 10-nm thick C_8PA layer is deposited on AlO_x. Afterwards the substrate temperature is set to 160°C to remove all physisorbed molecules. The thickness corresponding to a monolayer was obtained after ~90-minute desorption. The as-deposited, 10-nm-thick C_8PA layer is very rough with RMS surface roughness of 4.5 nm. This is reduced to 0.45 nm after 25 minutes of desorption. The water contact angle of aluminium oxide surface is low (20–40°), confirming hydrophilic properties. After chemisorption of the C_8PA monolayer the surface becomes hydrophobic with WCA of ~110°. Longer desorption time and lower C_8PA

growth temperature lead to increased WCA while the evaporation rate does not have much effect.

The structure of the C_8PA monolayer is improved by longer desorption/annealing, leading to the surface roughness of 0.36 nm after 210 minutes of desorption. Longer desorption decreases the transistor off-current and subthreshold slope and increases the field-effect mobility, on/off current ratio, and the threshold voltage. The capacitance, AFM, and FTIR confirmed that desorption removes physisorbed molecules and subsequently improves the molecular alignment between the aliphatic tails of C_8PA molecules.

Increase in the C_8PA growth temperature from 25°C to 150°C leads to the reduced molecular ordering, increased surface roughness, and smaller water contact angle. The elevated growth temperature also resulted in higher leakage current density, lower OTFT mobility, and higher threshold voltage. The maximum field-effect mobility and minimum threshold voltage was achieved for the lowest deposition temperature of 25°C.

The C_8PA deposition rate exhibited the least effect on the structural and surface properties of AlO_x/C_8PA bi-layers and the corresponding MIM and OTFT structures. Nevertheless, the evaporation rates in excess of 1 Å/s led to slightly better OTFT performance.

Pentacene deposition conditions mainly affected the pentacene morphology, field-effect mobility, and on/off current ratio. In summary, the tightly packed pentacene grains often resulted in better field-effect mobility. The maximum field-effect mobility of 0.063 cm^2/Vs and on/off current ratio of 6×10^5were achieved for pentacene deposition temperature of 55°C.

The OTFT bias-induced instability was studied for the following C_8PA parameters: desorption/annealing time, deposition temperature and evaporation rate. Degradation of the threshold voltage and subthreshold slope were found to be well correlated to C_8PA microstructure, while the degradation of the field-effect mobility was mostly affected by the oxidation of pentacene in the ambient air. The stretching parameters of the stretched-exponential fits were higher for longer C_8PA desorption time, lower growth temperature, and moderate evaporation rate. The increase in the stretching parameters indicates narrower distribution of the traps causing the degradation of the threshold voltage, subthreshold slope, field-effect mobility, and the on-current.

10.2 Future work

Vacuum, vapour-phase self-assembly of n-octylphosphonic acid monolayer was understood from AFM, FTIR, and water contact angle measurements. C_8PA thickness was calculated from the capacitance values of AlO_x/C_8PA and the corresponding AlO_x. In the future, the X-ray reflection could be used. Similarly, to understand the properties of aluminium oxide prepared by UV/ozone oxidation of aluminium, FTIR and X-ray photoelectron spectroscopy (XPS) should be performed. The results of this thesis suggest possible incorporation of carbon, oxygen, etc., into the oxide.

In this thesis the performance of OTFTs based on ultra-thin AlO_x/C_8PA dielectric and pentacene was improved through the optimization of several transistor layers. Further improvement in the transistor performance is possible by changing the device geometry as explained next.

The OTFT capacitance has two components: intrinsic and parasitic. The parasitic component arises from the overlap between the gate and source/drain contacts. The gate current is also proportional to this overlapping area. A top view of the OTFT showing the overlap is in Figure 10.1.

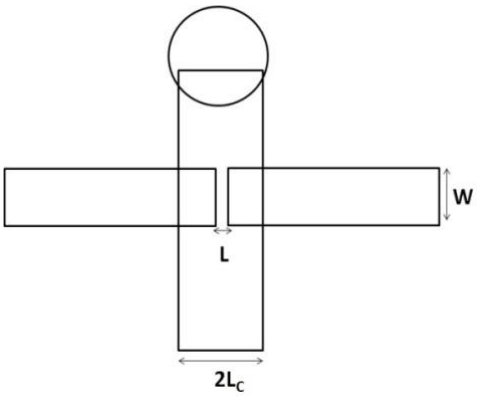

Figure 10.1: OTFT top view. $2L_C$ is the gate-contact length and W and L are the transistor dimensions.

The parasitic capacitance (C_G) of the above capacitor is given by Eq. 10.1:

$$C_G = C \times W \times (2L_C\text{-}L) \qquad (10.1)$$

where $2L_C$ and L is the gate-contact length and transistor channel length, respectively. C is the overlap capacitance per unit area. The larger gate-contact length results in larger parasitic capacitance.

The dimensions of transistors fabricated in this thesis are: L = 30, 50, 70, and 90 µm, W = 1000 µm and $2L_C$ = 500 µm. Large L_C was selected because of the manual mask alignment. In the future, high-resolution masks (reducing L_C) should be aligned under the microscope. The reduction in the gate current can also result in a drain current increase. Consequently, higher field-effect mobility and on/off current ratio are expected.

The maximum temperature during the vapour-phase self-assembly of C_8PA monolayer was 160°C which was also the maximum temperature in the OTFT fabrication. All of the devices presented in this thesis were fabricated on glass substrates but the process is amenable to plastic substrates. The study of these OTFTs on plastic substrates would be of great interest. The comparable dielectric properties should be obtained on a smooth plastic substrate. Since the field-effect mobility of OTFT with pentacene is low, other organic semiconductors such as DNTT can be used.

Monolayers based on phosphonic acids are widely used in OTFTs to achieve the low-voltage operation. In this thesis, only n-octylphosphonic acid was studied. The phosphonic acids with longer alkyl chains (C_{10}PA, C_{14}PA, and C_{18}PA) self-assembled from solutions have been studied by others [11, 32, 41]. Vapour-phase growth of longer alkyl phosphonic acids would be of interest, since these molecules may lead to less disordered monolayers, a phenomenon observed in solution self-assembly of such species.

Finally, further optimization of the OTFT performance would lead to a robust transistor technology that is necessary for circuit applications such as active-matrix addressing, sensor arrays and electronic skin.

REFERENCES

[1] T. Sekitani, U. Zschieschang, H. Klauk, T. Someya, "Flexible organic transistors and circuits with extreme bending stability," *Nature Materials* **9** (2010) pp. 1015–1022.

[2] Y. Fujisaki, Y. Nakajima, T. Takei, H. Fukagawa, T. Yamamoto, H. Fujikake, "Flexible active-matrix organic light-emitting diode display using air-stable organic semiconductor DNTT," *IEEE Transactions on Electron Devices* **59** (2012), pp. 3442–3449.

[3] S.W. Oh, C.W. Kim, H.J. Cha, U. Pal, Y.S. Kang, "Encapsulated-dye all-organic charged colored ink nanoparticles for electrophoretic image display,"*Advanced Materials* **21**(2009), pp. 4987-4991.

[4] B.K.C. Kjellander, W.T.T. Smaal, K. Myny, J. Genoe, W. Dehaene, P. Heremans, G.H. Gelinck, "Optimized circuit design for flexible 8-bit RFID transponders with active layer of ink-jet printed small molecule semiconductors,"*Organic Electronic* **14** (2013), pp. 768-774.

[5] "Organic electronics materials, manufacturing and applications," (Editor: H. Klauk), Wiley-VCH, Germany, (2006), pp. 3-33.

[6] K. Fukuda, T. Sekitani, U. Zschieschang, H. Klauk, K. Kuribara, T. Yokota, T. Sugino, K. Aska, M. Ikeda, H. Kuwabara, T. Yamamoto, K. Takimiya, T. Fukushima, T. Aida, M. Takamiya, T. Sakurai, T. Someya, "A 4 V operation, flexible braille display using organic transistors, carbon nanotube actuators, and organic static random-access memory," *Advanced Functional Materials* **21** (2011), pp. 4019–4027.

[7] Y. Choi, H. Kim, K. Sim, K. Park, C. Im, S. Pyo, "Flexible complementary inverter with low-temperature processable polymeric gate dielectric on a plastic substrate," *Organic Electronics* **10** (2009), pp. 1209–1216.

[8] X.-H. Zhang, W.J. Potscavage, S. Choi, B. Kippelen, "Low-voltage flexible organic complementary inverters with high noise margin and high dc gain," *Applied Physics Letters* **94** (2009), p. 043312.

[9] J. B. Kim, C. Fuentes-Hernandez, D.K. Hwang, W.J. Potscavage Jr., H. Cheun, B. Kippelen, "Vertically stacked hybrid organic–inorganic complementary inverters with low operating voltage on flexible substrates," *Organic Electronics* **12** (2011), pp. 45–50.

[10] T. C. Huang, K. Fukuda, C. M. Lo, Y. H. Yeh, T. Sekitani, T. Someya, "Pseudo-CMOS : A design style for low-cost and robust flexible electronics," *IEEE Transactions on Electron Devices* **58** (2011), pp. 141–150.

[11] K. Fukuda, T. Hamamoto, T. Yokota, T. Sekitani, U. Zschieschang, H. Klauk, T. Someya, "Effects of the alkyl chain length in phosphonic acid self-assembled monolayer gate dielectrics on the performance and stability of low-voltage organic thin-film transistors," *Applied Physics Letters* **95** (2009), p. 203301.

[12] K.D. Kim, C.K. Song, "Low voltage pentacene thin film transistors employing a self-grown metal-oxide as a gate dielectric," *Applied Physics Letters* **88** (2006), p. 233508.

[13] M.F. Chang, P.T. Lee, S.P. Mcalister, A. Chin, "Low Subthreshold Swing HfLaO/Pentacene Organic Thin-Film Transistors," *IEEE Electron Device Letters* **29** (2008), pp. 215–217.

[14] O. Acton, G. Ting, H. Ma, J.W. Ka, H.-L. Yip, N. M. Tucker, "π-σ-phosphonic acid organic monolayer/Sol-Gel hafnium oxide hybrid dielectrics for low-voltage organic transistors," *Advanced Materials* **20** (2008), pp. 3697–3701.

[15] B.G. Streetman, S.K. Banerjee, "Solid state electronic devices," Pearson/Prentice Hall, 6th Edition, (2010).

[16] X.-H. Zhang, B. Domercq, B. Kippelen, "Effect of Au deposition rate on the performance of top-contact pentacene organic field-effect transistors," *Synthetic Metals* **159** (2009), pp. 2371–2374.

[17] S. M. Sze, "Semiconductor devices physics and technology," John Wiley & Sons Singapore Pte. Limited, 3rd Edition, (2013).

[18] H. Klauk, U. Zschieschang, J. Pflaum, M. Halik, "Ultralow-power organic complementary circuits," *Nature* **445** (2007), pp. 745–748.

[19] J.B. Koo, S.J. Yun, J.W. Lim, S.H. Kim, C.H. Ku, S.C. Lim, J.H. Lee, T. Zyung, "Low-voltage and high-gain pentacene inverters with plasma-enhanced atomic-layer-deposited gate dielectrics," *Applied Physics Letters* **89** (2006), p. 033511.

[20] K. Fukuda, T. Sekitani, T. Yokota, K. Kuribara, T. Huang, T. Sakurai, U. Zschieshang, H. Klauk, M. Ikeda, H. Kuwabara, T. Yamamoto, K. Takimiya, K. Cheng, T. Someya, "Organic pseudo-CMOS circuits for low-voltage," *IEEE Electron Device Letters* **32** (2011), pp. 1448–1450.

[21] J. M. Rabaey, "Digital integrated circuits: a design perspective," Prentice-Hall International (UK), 1996.

[22] S.H. Kim, S.Y. Yang, K. Shin, H. Jeon, J.W. Lee, K.P. Hong, C.E. Park, "Low-operating-voltage pentacene field-effect transistor with a high-dielectric-constant polymeric gate dielectric," *Applied Physics Letters* **89** (2006), p.183516.

[23] C.-Y. Wei, S.-H. Kuo, Y.-M. Hung, W.-C. Huang, F. Adriyanto, Y.-H. Wang, "High-mobility pentacene-based thin-film transistors with a solution-processed barium titanate insulator," *IEEE Electron Device Letters* **32** (2011), pp. 90–92.

[24] L.F. Deng, Y.R. Liu, H.W. Choi, C.M. Che, P.T. Lai, "Improved performance of pentacene OTFTs with HfLaO gate dielectric by using fluorination and nitridation," *IEEE transactions on device and material stability* **12** (2012), pp. 520–528.

[25] L.F. Deng, P.T. Lai, W.B. Chen, J.P. Xu, Y.R. Liu, H.W. Choi, C.M. Che, "Effects of different annealing gases on pentacene OTFT with HfLaO gate dielectric," *IEEE Electron Device Letters* **32** (2011), pp. 93–95.

[26] M.F. Chang, P.T. Lee, S.P. McAlister, A. Chin, "Small-subthreshold-swing and low-voltage flexible organic thin-film transistors which use HfLaO as the gate dielectric," *IEEE Electron Device Letters* **30** (2009), pp. 133–135.

[27] J. Lee, J.H. Kim, S. Im, "Effects of substrate temperature on the device properties of pentacene-based thin film transistors using Al_2O_{3+x} gate dielectric," *Journal of Applied Physics* **95** (2004), pp. 3733-3736.

[28] X.-H. Zhang, S.P. Tiwari, B. Kippelen, "Pentacene organic field-effect transistors with polymeric dielectric interfaces: performance and stability," *Organic Electronics* **10** (2009), pp. 1133–1140.

[29] H. Yang, C. Yang, S.H. Kim, M. Jang, C.E. Park, "Dependence of pentacene crystal growth on dielectric roughness for fabrication of flexible field-effect transistors," *ACS Applied Materials &Interfaces* **2** (2010), 391–396.

[30] J.-M. Choi, D.K. Hwang, S.H. Jeong, J.H. Park, E. Kim, J.H. Kim, S. Im, "Polymer/AlO_x bilayer dielectrics for low voltage organic thin film transistors," *Journal of the Electrochemical Society* **154**(2007) pp. 331-335.

[31] D. Ashall, S.J. Fakher, M.F. Mabrook, "Enhanced performance of AlO_x-based organic thin-film transistors," *IEEE International Conference on Nanotechnology* 2011, 61–66.

[32] A. Jedaa, M. Burkhardt, U. Zschieschang, H. Klauk, D. Habich, G. Schmid, M. Halik, "The impact of self-assembled monolayer thickness in hybrid gate dielectrics for organic thin-film transistors," *Organic Electronics* **10** (2009), 1442–1447.

[33] K. Fukuda, T. Yokota, K. Kuribara, T. Sekitani, U. Zschieschang, H. Klauk, T. Someya, "Thermal stability of organic thin-film transistors with self-assembled monolayer dielectrics," *Applied Physics Letters* **96** (2010), p. 053302.

[34] H. Ma, O. Acton, G. Ting, J.W. Ka, H.-L. Yip, N. Tucker, R. Schofield, A.K.-Y. Jen, "Low-voltage organic thin-film transistors with π-σ-phosphonic acid molecular dielectric monolayers," *Applied Physics Letters* **92** (2008), p. 113303.

[35] U. Zschieschang, F. Ante, T. Yamamoto, K. Takimiya, H. Kuwabara, M. Ikeda, T. Sekitani, T. Somey, K. Kern, H. Klauk, "Flexible low-voltage organic transistors and circuits based on a high-mobility organic semiconductor with good air stability," *Advanced materials* **22** (2010), pp. 982–985.

[36] M. Novak, C. M. Jäger, A. Rumpel, H. Kropp, W. Peukert, T. Clark, "The morphology of integrated self-assembled monolayers and their impact on devices – A computational and experimental approach," *Organic Electronics* **11** (2010), pp. 1476-1482.

[37] P.H. Wöbkenberg, J. Ball, F.B. Kooistra, J.C. Hummelen, D.M. de Leeuw, D.D.C. Bradley, "Low-voltage organic transistors based on solution processed semiconductors and self-assembled monolayer gate dielectrics." *Applied Physics Letters* **93** (2008), p. 013303.

[38] L.A. Majewski, M. Grell, S.D. Ogier, J. Veres. "A novel gate insulator for flexible electronics," *Organic Electronics* **4** (2003), pp. 27–32.

[39] J. Collet, D. Vuillaume, "Nano-field effect transistor with an organic self-assembled monolayer as gate insulator," *Applied Physics Letters* **73** (1998), p. 2681.

[40] M. Halik, H. Klauk, U. Zschieschang, G. Schmid, C. Dehm, M. Schütz, S. Maisch, F. Effenberger, M. Brunnbauer, F. Stellacci, "Low-voltage organic transistors with an amorphous molecular gate dielectric," *Nature* (**431)** 2004, pp. 963–966.

[41] I.G. Hill, C.M. Weinert, L. Kreplak, B.P. Zyl, "Influence of self-assembled monolayer chain length on modified gate dielectric pentacene thin-film transistors," *Applied Physics A* **95** (2009), pp. 81–87.

[42] E. Hoque, J. A.DeRose, G. Kulik, P. Hoffmann, H.J. Mathieu, B. Bhushan, "Alkylphosphonate modified aluminum oxide surfaces," *The Journal of Physical Chemistry B***110** (2006), pp. 10855–10861.

[43] O. Acton, G.G. Ting, P.J. Shamberger, F.S. Ohuchi, H.Ma, A.K.-Y. Jen, "Dielectric surface-controlled low-voltage organic transistors via n-alkyl phosphonic acid self-assembled monolayers on high-k metal oxide," *ACS applied materials & interfaces* **2** (2010), pp. 511–20.

[44] K. C. Chinnam, S. Gupta, H. Gleskova, "Aluminium oxide prepared by UV/ozone exposure for low-voltage organic thin-film transistors," *Journal of Non-Crystalline Solids* **358** (2012), pp. 2512–2515.

[45] http://www.engineeringtoolbox.com/relative-permittivity-d_1660.html.

[46] H. Klauk, U. Zschieschang, and M. Halik, “Low-voltage organic thin-film transistors with large transconductance,” *Journal of Applied Physics* **102** (2007), p. 074514.

[47] http://www.kruss.de/en/theory/measurements/contact-angle.html, accessed on Septermber 24th, 2013.

[48] Y. Yaun and T.R. Lee, "Contact angle and wetting properties" in *Surface Science Techniques*, (Editors: G. Braco, B. Holst), pp. 1-10, Springer 2013.

[49] R. R. L. De Oliveira, D. A. C. Albuquerque, T. G. S. Cruz, F. M. Yamaji, F. L. Leite, *Measurement of the nanoscale roughness by atomic force microscopy: basic principles and applications* in Atomic Force Microscopy- Imaging, Measuring and Manipulating Surfaces at Atomic Scales, (Editor: V. Bellitto), pp. 155–158, InTech 2012.

[50] P. J. Larkin, *IR and Raman Spectroscopy Principles and Spectral Interpretatio,* Elsevier 2011, USA.

[51] S. Mun, J. Choi, K.H. Lee, K. Lee, S. Im, “Determining the optimum pentacene channel thickness on hydrophobic and hydrophilic dielectric surface,” *Applied Physics Letters* **93 (**2008), p. 233301.

[52] O.D. Jurchescu, J. Baas, T.T.M. Palstra, “Effect of impurities on the mobility of single crystal pentacene,” *Applied Physics Letters* **84** (2004), pp. 3061-3063.

[53] I. Salzmann, S. Duhm, R. Opitz, J.P. Rabe, N. Koch, “Impact of low 6,13-pentacenequinone concentration on pentacene thin film growth,” *Applied Physics Letters* **91** (2007), p. 015919.

[54] E. Gomar-Nadal, B.R. Conrad, W.G. Cullen, E.D. Willams, “Effect of impurities on pentacene thin film growth for field-effect transistors,” *Journal of Physical Chemistry C***112** (2008), pp. 5646–5650.

[55] M. Shtein, J. Mapel, J.B. Benziger, S.R. Forrest, “Effects of film morphology and gate dielectric surface preparation on the electrical characteristics of organic-vapor-phase-deposited pentacene thin-film transistors,” *Applied Physics Letters* **81** (2002), pp. 268–270.

[56] D. Knipp, R.A. Street, A. R. Völkel, “Morphology and electronic transport of polycrystalline pentacene thin-film transistors,” *Applied Physics Letters* **82** (2003), pp. 3907–3909.

[57] D. Knipp, R.A. Street, A. Völkel, J. Ho, "Pentacene thin film transistors on inorganic dielectrics: morphology, structural properties, and electronic transport," *Journal of Applied Physics* **93** (2003), pp. 347–355.

[58] S.Y. Yang, K. Shin, C.E. Park, "The effect of gate-dielectric surface energy on pentacene morphology and organic field-effect transistor characteristics," *Advanced Functional Materials* **15** (2005), pp. 1806–1814.

[59] I.V.K. Rao, S. Mandal, M. Katiyar, "Effect of pentacene deposition rate on device characteristics of top contact organic thin film transistors," *International Workshop on Physics of Semiconductor Devices*, Mumbai India (16^{th} – 19^{th} December 2007), pp. 594-596.

[60] J.H. Cho, D.H. Kim, Y. Jang, W.H. Lee, K. Ihm, J.-H. Han, S. Chung, K. Cho, "Effects of metal penetration into organic semiconductors on the electrical properties of organic thin film transistors," *Applied Physics Letters* **89** (2006), p. 132101.

[61] J. Park, J. S. Choi, "Study on the characteristics of metal–organic interface for organic thin-film transistors," *Synthetic Metals* **155** (2005), 657–661.

[62] Y. Kim, D. Jeon, "Effect of deposition temperature on the morphology and contact resistance of Au on pentacene," *Journal of Applied Physics* **108** (2010), p.016101.

[63] H. Klauk, G. Schmid, W. Radlik, W. Weber, L. Zhou, C.D. Sheraw, J.A. Nichols, T.N. Jackson, "Contact resistance in organic thin film transistors," *Solid-State Electronics* **47** (2003), 297–301.

[64] T. Lenz, T. Schmaltz, M. Novak, M. Halik, "Self-assembled monolayer exchange reactions as a tool for channel interface engineering in low-voltage organic thin-film transistors," *Langmuir* **28** (2012), pp. 13900–04.

[65] T. Hauffman, O. Blajiev, J. Snauwaert, C.v. Haesendonck, A. Hubin, H. Terryn, "Study of the self-assembling of n-octylphosphonic acid layers on aluminum oxide," *Langmuir* **24** (2008), pp. 13450–13456.

[66] M. Giza, P. Thissen, G. Grundmeier, "Adsorption kinetics of organophosphonic acids on plasma-modified oxide-covered aluminum surfaces," *Langmuir* **24** (2008), pp. 8688–94.

[67] G.G. Ting, O. Acton, H. Ma, J.W. Ka, A.K.-Y. Jen, "Study on the formation of self-assembled monolayers on sol-gel processed hafnium oxide as dielectric layers," *Langmuir* **25** (2009), pp. 2140–47.

[68] R. Quinones, E.S. Gawalt, "Study of the formation of self-assembled monolayers on nitinol," *Langmuir* **23** (2007), pp. 10123–30.

[69] B.S. Simpkins, S. Hong, R. Stine, A.J. Mäkinen, N.D. Theodore, M.A. Mastro, C.R. Eddy, P.E. Pehrsson, "Assembly of phosphonic acids on GaN and AlGaN," *Journal of Physics D: Applied Physics* **43** (2001), p. 015303.

[70] T. Ito, S.M. Forman, C. Cao, F. Li, C.R. Eddy, M.A. Mastro, R. T. Holm, R.L. Henry, K.L. Hohn, and J.H. Edgar, "Self-Assembled monolayers of alkylphosphonic acid on GaN substrates," *Langmuir* **24** (2008), pp. 6630–35.

[71] D.M. Spori, N.V. Venkataraman, S.G.P. Tosatti, F. Durmaz, N.D. Spencer, S. Zucher, "Influence of alkyl chain length on phosphate self-assembled monolayers," *Langmuir* **23** (2007), pp. 8053–8060.

[72] P. Thissen, A. Vega, T. Peixoto, Y.J. Chabal, "Controlled, low-coverage metal oxide activation of silicon for organic functionalization: unraveling the phosphonate bond," *Langmuir* **28** (2012), pp. 17494–17505.

[73] K. Wapner, M. Stratmann, G. Grundmeier, "Structure and stability of adhesion promoting aminopropyl phosphonate layers at polymer/aluminium oxide interfaces," *International Journal of Adhesion and Adhesives* **28** (2008), pp. 59–70.

[74] Milwaukee, *The Aldrich Library of FTIR Spectra*. 1997.

[75] D.O. Hutchins, T. Weidner, J. Baio, B. Polishak, O. Acton, N. Cernetic, H. Ma, A. K.-Y.Jen, "Effects of self-assembled monolayer structural order, surface homogeneity and surface energy on pentacene morphology and thin film transistor device performance," *Journal of Materials Chemistry C***1** (2013), p. 101.

[76] N. Tsud, M. Yoshitake, "Vacuum vapour deposition of phenylphosphonic acid on amorphous alumina," *Surface Science* **601** (2007), pp. 3060–3066.

[77] E. Hoque, J.A. DeRose, P. Hoffmann, B. Bhushan, H.J.J. Mathieu, "Alkylperfluorosilane self-assembled monolayers on aluminum: A comparison with alkylphosphonate self-assembled monolayers," *Journal of Physical Chemistry C***111** (2007), pp. 3956–3962.

[78] L.G. Hector, S.M. Opalka, G.A. Nitowski, L. Wieserman, D.J. Siegel, H. Yu, J. B. Adams, "Investigation of vinyl phosphonic acid / hydroxylated," *Surface science* **494** (2001), pp. 1–20.

[79] D.L. Allara, R.G. Nuzzo, "Spontaneously organized molecular assemblies. 1. formation, dynamics, and physical properties of n-alkanoic acids adsorbed from solution on an oxidized aluminium surface," *Langmuir* **1**(1985), pp. 45–52.

[80] I. Maege, E. Jaehne, A. Henke, H.-J.P. Adler, C. Bram, C. Jung, M. Stratmann, "Self-assembling adhesion promoters for corrosion resistant metal polymer interfaces," *Progress in organic coatings* **34** (1998), pp. 1-12.

[81] M.K. Templeton, W.H. Weinberg, “Adsorption and decomposition,” *Journal of the American Chemical Society* **107** (1985), pp. 97–108.

[82] R. Luschtinetz, A.F. Oliveira, J. Frenzel, J. Joswig, G. Seifert, H.A. Duarte, “Adsorption of phosphonic and ethylphosphonic acid on aluminum oxide surfaces,” *Surface Science* **602** (2008), pp. 1347–1359.

[83] P.J. Hotchkiss, M. Malicki, A. J. Giordano, N.R. Armstrong, S. R. Marder, “Characterization of phosphonic acid binding to zinc oxide,” *Journal of Materials Chemistry* **21** (2011), pp. 3107–3112.

[84] P. R. Davies, N. G. Newton, “The chemisorption of organophosphorus compounds at an Al (1 1 1) surface” *Applied Surface Science* **181** (2001), pp. 296–306.

[85] X.-H. Zhang, S.P. Tiwari, S.-J. Kim, B. Kippelen, “Low-voltage pentacene organic field-effect transistors with high-κ HfO_2 gate dielectrics and high stability under bias stress,” *Applied Physics Letters* **95** (2009), p. 223302.

[86] W.-J. Yoon, P.R. Berger, “Atomic layer deposited HfO_2 gate dielectrics for low-voltage operating, high-performance poly-(3-hexythiophene) organic thin-film transistors,” *Organic Electronics* **11** (2010), pp. 1719–1722.

[87] J.M. Ball, P.H. Wöbkenberg, F. Colléaux, M. Heeney, J.E. Anthony, I. McCulloch, D.D.C. Bradley, T.D. Anthopoulos, “Solution processed low-voltage organic transistors and complementary inverters,” *Applied Physics Letters* **95** (2009), p. 103310.

[88] C. S. Kim, S.J. Jo, S.W. Lee, W.J. Kim, H.K. Baik, S.J. Lee, “Surface-modified high-k oxide gate dielectrics for low-voltage high-performance pentacene thin-film transistors,” *Advanced Functional Materials* **17** (2007), pp. 958–962.

[89] T. Umeda, D. Kumaki, S. Tokito, “High air stability of threshold voltage on gate bias stress in pentacene TFTs with a hydroxyl-free and amorphous fluoropolymer as gate insulators,” *Organic Electronics* **9** (2008), pp. 545–549.

[90] Y. Noh, H. Sirringhaus, “Ultra-thin polymer gate dielectrics for top-gate polymer field-effect transistors,” *Organic Electronics* **10** (2009), pp. 174–180.

[91] Y. Jang, D.H. Kim, Y.D. Park, J.H. Cho, M. Hwang, “Low-voltage and high-field-effect mobility organic transistors with a polymer insulator,” *Applied Physics Letters* **88** (2006), p. 072101.

[92] O. Acton, M. Dubey, T. Weidner, K.M. O’Malley, T.-W. Kim, G.G. Ting, D. Hutchins, J.E. Baio, T.C. Lovejoy, A.H. Gage, D.G. Castner, H. Ma, A. K.-Y. Jen, “Simultaneous modification of bottom-contact electrode and dielectric surfaces for

organic thin-film transistors through single-component spin-cast monolayers," *Advanced Functional Materials* **21** (2011), pp. 1476–1488.

[93] S. P. Tiwari, K.A. Knauer, A. Dindar, B. Kippelen, "Performance comparison of pentacene organic field-effect transistors with SiO_2 modified with octyltrichlorosilane or octadecyltrichlorosilane," *Organic Electronics* **13** (2012), pp. 18–22.

[94] H.A. Budz, R.R. LaPierre, "Properties of octadecanethiol self-assembled monolayers deposited on GaAs from liquid and vapor phases," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **26** (2008), pp. 1425–1431.

[95] H. Sugimura, K. Ushiyama, A. Hozumi, O. Takai, "Micropatterning of alkyl- and fluoroalkylsilane self-assembled monolayers using vacuum ultraviolet light," *Langmuir* **16** (2000), pp. 885–888.

[96] X. Zhu, J. A. Mulder, W. F. Bergerson, "Chemical vapor deposition of organic monolayers on Si (100) via Si-N linkages," *Langmuir* **15** (1999), pp. 8147–8154.

[97] S. a DiBenedetto, D.L. Frattarelli, A. Facchetti, M.a Ratner, T. J. Marks, "Structure-performance correlations in vapor phase deposited self-assembled nanodielectrics for organic field-effect transistors," *Journal of the American Chemical Society* **131** (2009), pp. 11080–90.

[98] J. Park, A.C. Smith, T.R. Lee, "Loosely packed self-assembled monolayers on gold generated from 2-alkyl-2-methylpropane-1,3-dithiols," *Langmuir* **20** (2004),pp. 5829–5836.

[99] H.H. Choi, M.S. Kang, M. Kim, H. Kim, J.H. Cho, K. Cho, "Decoupling the bias-stress-induced charge trapping in semiconductors and gate-dielectrics of organic transistors using a double stretched-exponential formula," *Advanced Functional Materials* **23** (2013), pp. 690-696.

[100] U. Zschieschang, R.T. Weitz, K. Kern, H. Klauk, "Bias stress effect in low-voltage organic thin-film transistors," *Applied Physics A* **95** (2008), pp. 139–145.

[101] S. Cipolloni, L. Mariucci, A. Valletta, D. Simeone, F. De Angelis, G. Fortunato, "Aging effects and electrical stability in pentacene thin film transistors," *Thin Solid Films* **515**(2007), pp. 7546–7550.

[102] R. A. Street, "Bias-induced change in effective mobility observed in polymer transistors," *Physical Review B***77** (2008), p. 165311.

[103] H. Gleskova, S. Wagner, "DC-gate-bias stressing of a-Si:H TFTs fabricated at 150°C on polyimide foil," *IEEE Transactions on Electron Devices* **48** (2001), pp. 1667–1671.

[104] H. Sirringhaus, “Reliability of Organic Field-Effect Transistors,” *Advanced Materials* **21**(2009), pp. 3859–3873.

[105] G. Gu, M.G. Kane, S.-C. Mau, “Reversible memory effects and acceptor states in pentacene-based organic thin-film transistors,” *Journal of Applied Physics* **101** (2007), p. 014504.

[106] H. Klauk, U. Zschieschang, R.]T. Weitz, H. Meng, F. Sun, G. Nunes, D.E. Keys, C.R. Fincher, Z. Xiang, “Organic transistors based on Di(phenylvinyl)anthracene: performance and stability,” *Advanced Materials* **19**(2007), pp. 3882–3887.

List of publications

Patent application

1. H. Gleskova, K.C. Chinnam, S. Gupta, "Methods for forming an organic layer on a substrate," Application no.: WO2013021149A3, filed on July 31st, 2012.

Journal papers

1. H. Gleskova, S. Gupta, P. Šutta, "Structural changes in vapour-assembled n-octylphosphonic acid monolayer with post-deposition annealing: Correlation with bias-induced transistor instability," Organic Electronics **14** (2013) 3000-3006.
2. S. Gupta, P. Šutta, D. A. Lamprou, H. Gleskova, "Effect of substrate temperature on vapor-phase self-assembly of n-octylphosphonic acid monolayer for low-voltage organic thin-film transistors," Organic Electronics **14** (2013), 2468-2475.
3. S. Gupta, H. Gleskova, "Dry growth of n-octylphosphonic acid monolayer for low-voltage organic thin-film transistors," Organic Electronics **14** (2013), 354-361.
4. K.C. Chinnam, S. Gupta, H. Gleskova, "Aluminium oxide prepared by UV/ozone exposure for low-voltage organic thin-film transistors," Journal of Non-crystalline Solids **358** (2012), 2512-2515.

Conference proceedings

1. S. Gupta, H. Gleskova, "Optimizing the deposition rate of vacuum-grown n-octylphosphonic acid monolayer for low-voltage thin-film transistors," Euro Display 2013 proceeding, 16th – 19th September 2013, London UK.
2. S. Gupta, K.C. Chinnam, M. Zelzer, R. Ulijn, H. Gleskova, "Optimizing pentacene growth in low-voltage organic thin-film transistors prepared by dry fabrication technique," MRS Proceedings **1435** (2012).

Invited talks

1. S. Gupta, "Development of ultra-thin bi-layer dielectric and its implementation in organic thin-film transistors," Indian Institute of Technology Gandhinagar, India, July 2013.
2. S. Gupta, "Vacuum vapour growth of n-octylphosphonic acid monolayer for low-voltage organic thin-film transistors," Ecole Polytechnique Federal de Lausanne, Switzerland, October 2013.

Posters

1. S. Gupta, H. Gleskova, "Optimizing the deposition rate of vacuum-grown n-octylphosphonic acid monolayer for low-voltage thin-film transistors," Euro Display 2013, 16^{th} – 19^{th} September 2013, London UK – *received prize from the Society for Information Display for the best poster*.
2. S. Gupta ,P.Šutta, H. Gleskova, "Effect of post-deposition annealing on the structure of vacuum-grown n-octylphosphonic acid," International Conference on Organic Electronics, 17^{th} – 19^{th} June 2013, Grenoble, France.
3. S. Gupta**,** K.C. Chinnam, M. Zelzer, R. Ulijn, H. Gleskova, "Optimizing pentacene growth in low-voltage organic thin-film transistors prepared by dry fabrication technique," 2012 Materials Research Society Spring Meeting, 9^{th} – 13^{th} April 2012, San Francisco USA.
4. S. Gupta, H. Gleskova, "Vacuum-grown organic monolayers as gate dielectrics in low-voltage organic thin-film transistors," Glasgow Research Partnership in Engineering Conference, Glasgow, UK, June 2013.
5. S. Gupta, H. Gleskova, "Optimizing the semiconductor-dielectric interface in low-voltage organic thin-film transistors," Research Presentation Day of the Faculty of Engineering, University of Strathclyde, Glasgow, UK, June 2012.
6. S. Gupta, H. Gleskova, "Controlling the surface roughness of aluminium oxide in organic thin-Film transistors with ultra-thin gate dielectrics," University Research Day, University of Strathclyde, Glasgow, June 2012.

7. S. Gupta, K.C. Chinnam, H. Gleskova, “Effect of pentacene growth on low-voltage organic Thin-Film Transistors,” Workshop of the Glasgow Research Partnership in Engineering, Glasgow, UK, June 2011.
8. S. Gupta, K.C. Chinnam, H. Gleskova, “Study of pentacene growth in low-voltage organic thin-film transistors,” University Research Day, University of Strathclyde, Glasgow, UK, June 2011.
9. S.Gupta, K.C. Chinnam, H. Gleskova, “Low-voltage organic thin-film transistors,” Research Presentation Day of the Faculty of Engineering, University of Strathclyde, Glasgow, UK, January 2011.

Appendix A

Extraction of field-effect mobility and threshold voltage in linear regime

```
clear all
a = dlmread('01Oct 2013 S1R4T1 Id-Vg3.txt');
L = 1;
Cox = 4.74e-7;
W = 1000;
Vd = 0.1;
vglin = a(1:101,1);
idlin = a(1:101,2);
vg1 = input('Enter starting value of gate-source voltage in linear regime');
vg2 = input('Enter ending value of gate source voltage in linear regime');
bl1 = abs(vglin-vg1);
bl2 = abs(vglin-vg2);
[cl1, i] = min(bl1);
[cl2, j]= min(bl2);

vglin1 = vglin(i:j,1);
idlin1 = idlin(i:j,1);

d = polyfit(vglin1,idlin1,1);
vglindiff= (vglin(i)-vglin(j))/20;
for x1 = 1:1:20
  xfit1(x1) = vglin(j) + vglindiff*(x1-1);
  dfit1(x1) = polyval(d,xfit1(x1));
end
mulin = (d(1) * L) /(Cox * W * Vd)
vthlin = -d(2)/d(1)
plot(vglin,idlin,'r',xfit1,dfit1,'k');
```

Appendix B

Extraction of field-effect mobility and threshold voltage in saturation regime, on-current and on/off current ratio

```
clear all
a = dlmread('01Oct 2013 S1R4T1 Id-Vg3.txt');
L = 1;
Cox = 4.74e-7;
W = 1000;
vg3 = input('Enter starting value of gate-source voltage in saturation regime');
vg4 = input('Enter ending value of gate source voltage in saturation regime');
vgsat = a(102:202,1);
idsat = a(102:202,2);
sqrtidsat = sqrt(-idsat);
bs1 = abs(vgsat-vg3);
bs2 = abs(vgsat-vg4);
[cs1, k] = min(bs1);
[cs2, l]= min(bs2);
vgsat1 = vgsat(k:l,1);
sqrtidsat1 = sqrtidsat(k:l,1);
e = polyfit(vgsat1,sqrtidsat1,1);
vgsatdiff = (vgsat(k)-vgsat(l))/20;
for x2 = 1:1:20
  xfit2(x2) = vgsat(l) + vgsatdiff*(x2-1);
  dfit2(x2) = polyval(e,xfit2(x2));
end
musat = (e(1)^2 * 2 * L)/(Cox *W)
vthsat = -e(2)/e(1)
plot(vgsat,sqrtidsat,'r',xfit2,dfit2,'k');
ion = idsat(101,1)
ioff = -max(idsat)
```

Appendix C

Extraction of subthreshold slope

```
clear all
a = dlmread('01Oct 2013 S1R4T1 Id-Vg3.txt');
%L = input('Enter the channel length');

vg5 = input('Enter starting value of gate source voltage in subthreshold regime');
vg6 = input('Enter ending value of gate source voltage in subthreshold regime');
vgsat = a(102:202,1);
idsat = a(102:202,2);
igsat = a(102:202,3);

logid = log10(-idsat);
logig = log10(-igsat);
bl3 = abs(vgsat-vg5);
bl4 = abs(vgsat-vg6);

[cm1, s1] = min(bl3);
[cm2, s2]= min(bl4);

vgsub1 = vgsat(s1:s2,1);
idsub1 = logid(s1:s2,1);
e = polyfit(vgsub1,idsub1,1);
subth = -1000/e(1)

plot(vgsat,logid,vgsat,logig,vgsub1,idsub1,'linewidth',5)
```

Appendix D

Extraction of the channel and contact resistances

```
clear
a1 = dlmread('13Jul 2012 S3R2T1 Id-Vg3.txt');
a2 = dlmread('13Jul 2012 S3R2T2 Id-Vg3.txt');
a3 = dlmread('13Jul 2012 S3R2T3 Id-Vg3.txt');
a4 = dlmread('13Jul 2012 S3R2T4 Id-Vg3.txt');

vg = a1(1:101,1);
W = 0.1; % W in cm
vd = -0.1;
% The second column in every input file is the drain-current.
i(:,1) = a1(1:101,2);
i(:,2) = a2(1:101,2);
i(:,3) = a3(1:101,2);
i(:,4) = a4(1:101,2);
% R total = Vd/Id, hence taking inverse of I and muliplying it by vd gives total resistance
invi = 1./i;
vg1 = input('Enter the starting value of Vgs');
vg2 = input('Enter the ending value of Vgs');
% Choosing the voltage range for which transistor operates in linear regime
bl1 = abs(vg-vg1);
bl2 = abs(vg-vg2);
[cl1, j] = min(bl1);
[cl2, k]= min(bl2);
l = [24 43 62 80]; % l is in micrometer
 l = l*1e-4; % l in cm
for x = j : 1 : k
for y = 1:1:4
isel(x-j+1,y) = -invi(x,y);
        % R(Total)*W = R(contact)*W + {L/(mu*C*(vg-vth))},
```

```
%  R(channel) = {L/(mu*C*(vg-vth)*W)} -->
rsel(x-j+1,y) = vd*invi(x,y)*W; % To present total resistance in ohm-cm.
end
vgsel(x-j+1,1) = vg(x,1);
p(x-j+1,:) = polyfit(l,rsel(x-j+1,:),1); % Linear fit to the rtotal X W(ohm-cm)vs. length
rc(x-j+1,:) = p(x-j+1,2); %linear-fit intercept corresponds to the contact resistance
rch(x-j+1,:) = p(x-j+1,1); %Channel resistance = slope * (L/W);
end

ls = (0:10:100)*1e-4;
d = 5;
for m = 1 : d : 21
   rplot(1+(m-1)/d,:) = polyval(p(1+(m-1)/d,:),ls,1);
rselec(1+(m-1)/d,:) = rsel(1+(m-1)/d,:);

end
plot(ls,rplot,'-',l,rselec,'o','linewidth',3)
xlabel('Channel length L (cm)','fontweight','b','fontsize',14);
ylabel('R_{Total} X W (\Omega-cm)','fontweight','b','fontsize',14);
set(gca,'fontweight','b');
set(gca,'fontsize',14);
set(gca,'linewidth',2);
```

Appendix E

Extraction of bias-stress parameters

```
function [par_hat, fval, exitflag, output, R2] = id_shift
t = [10 30 70 100 200 600 1000 2000 5000]';
id = [0.7892 0.6806  0.6057 0.5718 0.5200 0.4324 0.3873 0.3251 0.2397
 0.76966 0.6435 0.5545 0.5194 0.46     0.3718 0.33     0.2734 0.1970]';
y = id(:,1);
func = @(par_hat) sqrt( sum( (y -  par_hat(3)- ((1 -par_hat(3))* exp(-((t*1e-3)./par_hat(1)).^par_hat(2)))).^2 )) ;
options = optimset('MaxIter',100000000,'MaxFunEval',1e6,'TolX',1e-15,'TolFun',1e-15,'algorithm','interior-point');
lb = [0, 0.1, 0];
ub = [0.4, 0.7, 0.2];
[par_hat,fval,exitflag,output] = fmincon (func, [0.3,0.5, 0.12],[],[],[],[],lb,ub,[],
options);
t_ex = zeros(1000,1);
for i = 1:1000
   t_ex(i) = 10*i;
end
y_ex = par_hat(3)+ (1 -par_hat(3))* exp(-((t_ex*1e-3)./par_hat(1)).^par_hat(2));
figure;
semilogx(t,y,'*');
hold on
semilogx(t_ex, y_ex);
Stot = 0;
ybar = sum(y)/length(y);
for i = 1:length(t)
   Stot = Stot + (y(i) - ybar)^2;
end
resnorm = fval* fval;
R2 = 1- resnorm/Stom
```