Fault management in networks incorporating Superconducting Cables (SCs) using Artificial Intelligence (AI) techniques.

Eleni Tsotsopoulou

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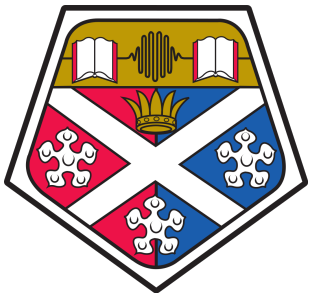

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Abstract

With the increasing penetration of renewable energy sources, the immense growth in energy demand and the ageing of existing system infrastructure, future power systems have started to face reliability and resiliency challenges. To mitigate these issues, the need for bulk power corridors which enable the effective sharing of the available power capacity, between countries and from remote renewable energy sources, is rendered imperative. In this context, the deployment of multi-layer Superconducting Cables (SCs) with High Temperature Superconducting (HTS) tapes have been considered as a promising solution towards the modernisation of power systems. As opposed to conventional copper cables, SCs are characterised by a plethora of technically-attractive features such as compact structure, higher current-carrying capability, lower losses, higher power transfer at lower operating voltages and over longer distances, and reduced environmental impact.

The performance of SCs is mainly determined by the structure of the cable and the electro-magneto-thermal properties of the HTS tapes, accounting for the critical current, critical temperature and critical magnetic field. Particularly, during steady state conditions, HTS tapes operate in superconducting mode, providing tangible benefits to power system operation such as a current-flowing path with approximately zero resistance. However, under certain transient conditions (e.g., electric faults), when the fault current flowing through HTS tapes reaches values higher than the critical current, HTS tapes start to quench. The quenching phenomenon is accompanied by a rapid increase in the equivalent resistance and temperature of SCs, the generation of Joule heating and the subsequent reduction in fault current magnitudes. Consequently, the transition of SCs from superconducting state to resistive state, during transient conditions, introduces many variables in the fault management of such cable technologies. Therefore, in order to exploit the technological advantages offered by SC applications, accommodate their wide-scale deployment within future energy grids, and accelerate their commercialisation, the detailed evaluation of their transient response and the consequent development of

reliable fault management solutions are vital prerequisites.

On that front, one of the main objectives of this thesis is to provide a detailed fault signature characterisation of AC and DC SCs and develop effective and practically feasible solutions for the fault management of AC and High Voltage Direct Current (HVDC) grids which incorporate SCs. As the fault management (i.e., fault detection, fault location, and protection) of SCs has proven to be a multi-variable problem, considering the complex structure, the unique features of SCs, and the quenching phenomenon, there is a need for advanced methods with immunity to these factors. In this context, the utilisation of Artificial Intelligence (AI) methods can be considered a very promising solution due to their capability to expose hidden patterns and acquire useful insights from the available data. Specifically, data-driven methods exhibit multifarious characteristics which allow them to provide innovative solutions for complex problems. Given their capacity for advanced learning and extensive data analysis, these methods merit thorough investigation for the fault management of SCs. Their inherent potential to adapt and uncover patterns in large datasets presents a compelling rationale for their exploration in enhancing the reliability and performance of superconducting cable systems. Therefore, this thesis proposes the development of novel, data-driven protection schemes which incorporate fault detection and classification elements for AC and multi-terminal HVDC systems with SCs, by exploiting the advantages of the latest trends in AI applications. In particular this thesis utilises cutting-edge developments and innovations in the field of AI, such as deep learning algorithms (i.e., CNN), and state-of-the-art techniques such as the XGBoost model which is a powerful ensemble learning algorithm. The developed schemes have been validated using simulation-based analysis. The obtained results confirm the enhanced sensitivity, speed, and discrimination capability of the developed schemes under various fault conditions and against other transient events, highlighting their superiority over other proposed methods or existing techniques. Furthermore, the generalisation capability of AI-assisted schemes has been verified against many adverse factors such as high values of fault resistance and noisy measurement. To further evaluate the practical feasibility and assess the time performance of the proposed schemes, real-time Software In the Loop (SIL) testing has been utilised.

Another very important task for the effective fault management of AC and DC SCs is the estimation of the accurate fault location. Identifying the precise location of faults is crucial for SCs, given their complex structure and the challenging repair process.

As such, this thesis proposes the design of a data-driven fault location scheme for AC systems with SCs. The developed scheme utilises pattern recognition techniques, such as image analysis, for feature extraction. It also incorporates AI algorithms in order to formulate the fault location problem as an AI regression problem. It is demonstrated that the scheme can accurately estimate the fault location along the SCs length and ensure increased reliability against a wide range of fault scenarios and noisy measurements. Further comparative analysis with other data-driven schemes validates the superiority of the proposed approach.

In the final chapter the thesis summarises the key observations and outlines potential steps for further research in the field of fault management of superconducting-based systems.

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Chapter 1

Introduction

1.1 Introduction to the Research

Power systems are experiencing a rapid transition, emanating from the gradual decommissioning of large Synchronous Generators (SGs) and the progressive deployment of Inverter-Connected Generators (ICGs). Traditional power transmission and distribution grids are evolving towards full decarbonisation in response to European Union (EU) net zero carbon emission targets. In view of its commitment to the Paris Agreement [1], the European Commission sets an overall goal, across the EU, for a 32% share of Renewable Energy Sources (RES) in the power generation mix by 2030, and 75% to 100% by 2050 [2]. Specifically, future energy scenarios predict that Europe will need more than $2,200$ GW of solely wind and solar power by 2050 [3, 4]. Zero carbon operation targets require radical change in the way that power systems are designed to operate. A typical example of this change is the utilisation of remote generating facilities, such as large Wind Farms (WFs), interconnected through long-transmission lines which will become the norm for power transmission in the near future.

The accelerated uptake of intermittent RES-based technologies coupled with the rapid growth of global electricity demand and the ageing of existing system infrastructure have a great impact on network operation, resiliency, and security of supply. Hence, towards the decarbonisation of power systems, the physical infrastructure of the grid will need to evolve from generation to consumption level and consequently new challenges are emerging. A major challenge that remains to be tackled is how to support the transition to net zero grids and concurrently ensure security and reliability of the system. On that front, the industry in collaboration with the research engineering community

have started to seek innovative technologies which can overcome the aforementioned restrictions, enable a more efficient interchange of power, and harness the potential of RES.

Within this context, the development of bulk power corridors for providing electric power over long distances is a prerequisite to address the congestion challenges in power systems, enabling the uptake of RES [5]. As energy connectivity can be considered a key factor for facilitating the potential of power grid decarbonisation, the deployment of Superconducting Cables (SCs) in future energy grids has started to receive increasing attention in the energy sector.

SCs are becoming increasingly competitive compared to conventional transmission lines and cables. This stems from their superior advantages such as the capability to transfer power over long distances at lower voltage levels [6] and with reduced power losses [7]. Furthermore, their reduced environmental impact, compact size and high current-carrying capability [8] have made the SCs a very promising alternative for power transmission in future net zero grids. SC applications, harnessing the unique features of the superconducting materials, have been the focus of a plethora of research [9, 10].

The concept of employing SCs to transfer GW of power over long distances with approximately zero losses has been investigated for decades, resulting in SC technologies which are considered a feasible solution for real-world power system applications and are progressively maturing [11]. Specifically, the utilisation of SCs to provide connectivity between remote RES and centrally located load centres has been conceptualised by the "Supergrid" project [12]. In recent years, the key findings derived from many demonstration and field projects have highlighted the technically-attractive features of SCs which can accommodate the modernisation of power grids and offer many benefits over their conventional counterparts. The main advantages of the deployment of SCs are laid out hereafter:

- For the same voltage level and cross-sectional area, the current-carrying capability of SCs is three to five times that of conventional copper cables. Therefore, the installation of SCs can address congestion problems, especially in high power density areas such as metropolitan meshed networks [13].

- SCs can transfer the equivalent power capacity of conventional cables at lower voltage levels, while still enabling bulk power transfer at high capacities. Lower operating voltages result in lower volume and size of electrical equipment at both

ends of the cable, eliminating the need for associated auxiliary equipment and preventing capital-intensive grid reinforcement [14].

- When SCs operate in superconducting state they exhibit approximately zero resistance which originates from their compact size and the perfect diamagnetism (i.e., Meissner effect [15]). Therefore, SCs provide a current-flowing path with low electrical losses, reducing the overloaded power burden of the parallel connected transmission pathways.

- The fault current limiting functionality of SCs, emanating from their design and the electro-thermal properties of the High Temperature Superconducting (HTS) tapes, is considered an advantageous feature for the densely populated areas which are characterised by increasing electrical power installation [16].

Thus far, many initiatives promoting the deployment of AC and DC SCs in AC transmission systems and High Voltage Direct Current (HVDC) grids, respectively, have been conducted worldwide. For several years, AC SCs have been more mature and cost-effective than DC SCs. Initially, AC SC-based demonstration projects were focused on the deployment of AC SCs with short-length, especially for high-capacity connections in urban areas to address congestion challenges [13]. As the technology of SCs advances, the tendency to investigate AC SCs with longer length for the transmission level is increasing. High power HTS AC transmission or distribution systems for congested urban areas have reached Technology Readiness Level (TRL) 7 as demonstrated by integrated pilot projects. The Shingal Project in South Korea represents the first commercial project of its kind and has advanced to TRL 8. Notably, projects utilising 154 kV in Jeju (South Korea) and 138 kV in Long Island (US) have been discussed as well [17].

Simultaneously, growing attention is focused towards DC SCs for HVDC links. During the last few years, extensive efforts have been concentrated on the installation of DC SCs in HVDC grids for the connection of remote RES or offshore WFs, and the interconnection of national grids. Existing research assigns a TRL of 5 due to the limited testing on integrated systems. However, the recent demonstration nb.5 of the FP7 funded Best Paths project, with capacity of $5 - 10$ kA at voltages between $200 - 320$ kV, suggests that a TRL of a minimum of 6 has been achieved [18]. The unique features of DC SCs combined with the advantages offered by HVDC transmission systems, in terms of bulk power transfer, have the potential to revolutionise future power grids and facilitate the

realisation of RES-dominated systems [19] [20].

The landmark SC-based projects are presented in Table 1.1 and are categorised by date, cable type, voltage, current level, and length.

Table 1.1: Landmark projects of AC and DC SCs.

Project	**Year**	**Cable type**	**Voltage (kV)**	**Current (kA)**	**Length (m)**	**Reference**
Albany (US)	2006	AC (3Ph)	34.5	0.8	350	[21]
Long Island (US)	2008	AC (3Ph)	138	2.4	600	[22]
New York (US)	2016	AC (3Ph)	10	4	300	[23]
Hannover (Germany)	2010	AC (3Ph)	20	3.2	30	[24]
Yokohama (Japan)	2012	AC (3Ph)	66	1.75	250	[25]
Ampacity (Germany)	2014	AC (3Ph)	10	2.3	1000	[26]
KEPRI (South Korea)	2014	DC	80	3.25	100	[27]
Ishikari (South Korea)	2014	DC	-	-	500 and 1000	[28]
Best Paths	2019	HVDC	320	10	30	[18]
Shingal (South Korea)	2019	AC (3Ph)	23	1.26	1000	[29]
St. Petersburg (Russia)	2020	DC	20	3.2	-	[30]
SuperLink (Germany)	2021	AC (3Ph)	110	3.2	1200	[9]

Although SCs can technically contribute to the mission of system modernisation, their application in power system apparatuses were not economically possible due to their large installation cost (e.g., superconducting material, cooling systems) [13]. As the research progresses, better understanding of superconductivity is acquired and SC technology is becoming more affordable and reaching market maturity. A milestone in the integration of SCs in power systems, and the commercial applications of SCs, was the discovery of second generation ($2G$) HTS tapes, which present remarkable properties such as operation in superconducting state at higher temperatures ($T \geq 77\ K$) (therefore lower requirements for cooling) and fault current limiting capability [31].

Furthermore, the numerous possibilities that SCs can unlock and the advantages they offer (i.e., eliminated electrical losses, high current characteristics, etc.) can lead to significant reduction in the capital and operational costs [14]. On that front, a techno-economic assessment between conventional HVDC systems and superconducting-based HVDC grids has been conducted in [32]. The results are demonstrated in Fig. 1.1 and reveal that SCs can be considered a cost-competitive option for future power grids, presenting significantly lower lifecycle costs than HVDC systems with conventional feeders. More specifically, superconducting-based HVDC systems result in lower costs from electrical losses, due to the physical properties of the superconducting materials, lower unavailability costs, and lower capital costs (i.e., lower volume of electrical equipment) compared to conventional HVDC systems. On the other hand, there are costs associated with the cooling of superconducting-based HVDC grids to cryogenic temperatures,

however, these cooling costs are not dependent on SC capacity (i.e., 4 *GW* system and 7 *GW* system require the same cooling expenditures). Furthermore, Superconducting-HVDC system exhibits a much higher capacity deployment rate. Although, the installation rate of DC SCs, as an emerging technology, is slower compared to conventional DC cables, the substantial power capacity provided by superconducting technology enables a far greater capacity to the offshore grid with each installation (10 *GW* versus 2 *GW*), eliminating the number of the required cables.

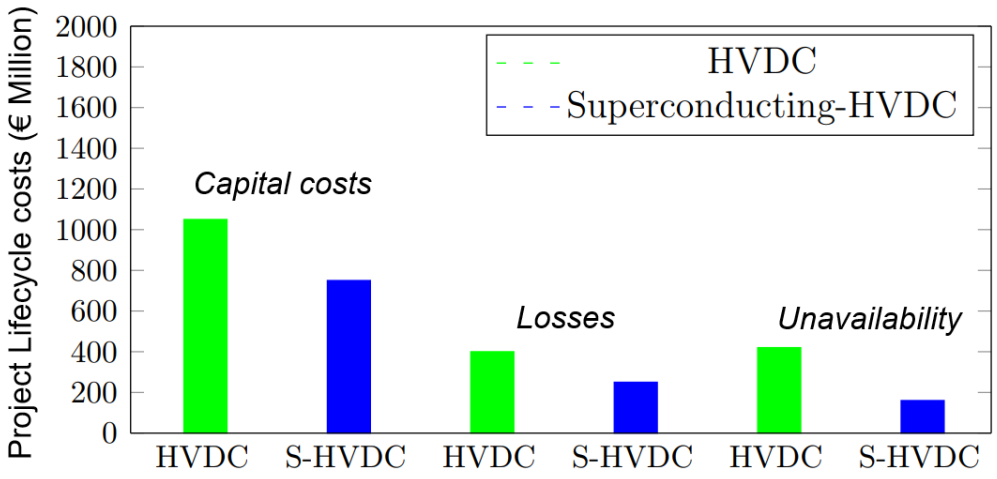

Figure 1.1: Lifecycle cost comparison between conventional HVDC systems and Superconducting-based HVDC systems.

It is therefore evident that the deployment of AC and DC SCs are anticipated to play a key role in the decarbonisation of future power grids. However, even though SCs offer many advantages compared to their conventional counterparts, their installation in power systems is accompanied by several challenges. The main factors that hinder the wide-scale commercialisation of SCs are the technical issues emanating from their transient performance, their complex structure, and the complexity of their cooling systems [33]. The response of SCs during transient conditions (i.e., electric faults) is dominated by the quenching phenomenon and the properties of HTS tapes, which form the basis of the manufacturing of SCs. Consequently, the fault management of SCs is crucial to ensure the reliability and safety of such cable technologies and the system as a whole. In this context, the work presented in this thesis investigates, analyses and addresses the associated challenges with the integration of SCs in AC and HVDC systems from a fault management perspective.

1.2 Research Motivation

As the deployment of SCs has gradually entered the stage of engineering applications, it has been realised that for their practical implementation and operation there are several outstanding issues to be solved. Given the key role of SCs in future power grids, acquiring a deep understanding of their behavior during different system conditions (i.e., steady state and transient conditions), and ensuring their safe and reliable operation is vital.

The performance of SCs is dictated by their structure, the electro-thermal properties of HTS tapes, and the system conditions. All commercially available HTS tapes for SCs are coated conductors consisting of multiple layers of different materials [34]. Therefore, SCs are characterised by a complicated design process and geometric features and they operate as complex elements from the reliability perspective [9]. During steady state conditions, SCs operate in a superconducting state and constitute a current-flowing path with approximately zero resistance [35]. Under transient conditions (i.e., electric faults), when the current flowing through SCs increases and exceeds a critical value, SCs start to quench. During the quenching phenomenon, as the fault current continues to increase, the resistance and temperature of SCs increase dramatically, resulting in the transition of SCs into a highly-resistive state. This abrupt rise in SCs equivalent resistance results in the reduction of the fault current levels. The effect of the dynamically changing resistance and subsequent suppressed fault current magnitudes lead to many fault-related issues, especially for operation of protection and fault location schemes.

For the reliable and healthy operation of AC and HVDC systems, the incorporated protection schemes shall be capable of meeting the following requirements [36]:

- Selectivity
- Sensitivity
- Dependability
- Stability
- Security
- Speed of operation
- Simplicity

In particular, protection selectivity refers to the the effectiveness of a protection system in detecting and correctly identifying faults. A highly sensitive protection system minimizes the likelihood of missing real faults, thus enhancing the reliability and safety of the network [37]. Stability in protection systems refers to the system's ability to maintain consistent and reliable performance over time. It ensures that the protection system doesn't produce false alarms under normal operating conditions or faults beyond the protection zone. A stable protection system is essential to prevent unnecessary interruptions to the electrical network [37]. Protection selectivity is about the ability of the system to precisely identify and isolate the faulty component or section of the network when a fault occurs. It ensures that only the affected part is disconnected or protected, while the rest of the network remains operational. Selectivity is crucial to minimise downtimes and achieve protection coordination [38]. Dependability is a measure of the level of confidence or assurance that a protection system, will indeed operate accurately during a fault occurred within the protection zone [38]. Protection security is a measure of the level of certainty that the protection scheme will not trigger erroneously or exceed its designed response speed [39]. Finally, operational speed in protection systems refers to the system's response time when a fault is detected and is vital to minimise the impact of faults on the network and prevent damage to equipment, while simplicity refers to its ease of design, implementation, and operation [39]. The aforementioned criteria, apart from the simplicity, will be considered for the development of the protection schemes.

The integration of SCs in AC transmission systems, with inherent fault current limiting capability and variable resistance, imposes a negative impact on the performance of existing protection schemes (i.e., over-current, distance protection) regarding their sensitivity, dependability, and operating time. Furthermore, the discrimination, stability, and security of protection systems may be jeopardised by external faults or other transient events (i.e., load switching) which lead to the quenching of SCs.

With respect to HVDC systems, as the deployment of DC SCs is still in its infancy, the impact of the quenching phenomenon on the fault management of such systems has not been thoroughly studied. DC-side faults are the main issue when considering HVDC technology due to the rapidly increasing fault currents and the lack of natural zero-crossing. Therefore, a short fault clearance time (i.e., in the range of 5 ms) is of major importance for the healthy operation of HVDC systems [40]. For the case of meshed HVDC systems, fast fault clearance time is considered extremely challenging to

achieve with discriminative line disconnection (i.e., only the fault line is disconnected). Therefore, another key factor for the successful protection of multi-terminal HVDC systems is the increased selectivity in order to ensure that the unaffected system's parts remain operational and minimise the downtimes. The installation of DC SCs, and their quenching during transient conditions, may cause malfunctions to the well-established protection schemes.

As such, the above-mentioned factors render the need for detailed fault signature characterisation of SCs and the development of efficient fault management solutions, imperative. Therefore, the integration of SCs into power systems has unlocked a new research path for the area of power systems fault management. In this context, one of the main objectives of this thesis is to characterise the fault response of SCs from a fault management perspective and assess the impact of fault parameters (i.e., fault resistance, type, location) on the quenching phenomenon. The acquired insights will be utilised for the development of sensitive, discriminative, and fast protection schemes for AC and HVDC systems with SCs.

Additionally, another important function that must run alongside the protection, for the effective fault management, is the accurate estimation of the fault location. In particular, when a fault occurs on a feeder, protection systems initiate the selective tripping signal for the corresponding Circuit Breaker (CB) in order to prevent the adverse effects on power system operation. Following this, the precise fault localisation is of paramount importance in order to enable rapid restoration and minimise the system down time [41]. More precisely, for the case of SCs the accurate identification of fault location is very important considering their complex configuration (i.e., cooling liquid tubes, tapes, etc.) and the challenges in the repair procedure [9]. Specifically, SCs consist of complex, multi-layered structures comprising various materials with distinct properties, including superconducting layers, insulation layers, stabilisers, and cryogenic cooling systems. This intricate design significantly complicates the task of identifying fault locations and performing necessary repairs. Furthermore, the elevated costs associated with superconducting materials make precise fault localisation imperative. This challenge is further exacerbated by the absence of standardized procedures for the operation and repair of superconducting systems. To address this issues, another main objective of the presented work is the development of a novel fault location scheme for SCs incorporated in AC systems.

It is evident that the fault management of SCs is a multi-variable problem. The integration of SCs results in many changes in the physical infrastructure and the information layer of the system. As the complexities, the uncertainties, and the search space increase, conventional methods of power system analysis and fault management are proven to be inefficient, diminishing system security. Consequently, more advanced tools need to be explored such as Artificial Intelligence (AI) methods.

AI methods have emerged as a compelling solution due to their remarkable computational power and efficiency, particularly in tackling non-linear problems involving high-dimensional data. In the context of SCs fault management, AI-based tools offer a range of distinct advantages. Firstly, they excel in handling high-dimensional data, adept at capturing intricate relationships that may elude conventional methods. Secondly, AI techniques can adapt and learn from extensive datasets, enabling them to discern fault patterns, even within complex SC systems. For instance, deep learning algorithms can dynamically adjust fault management strategies based on historical fault data and evolving network conditions. Thirdly, AI tools possess the capacity to uncover latent information within data, unveiling hidden insights that prove invaluable for fault detection, classification, and precise localisation. For example, pattern recognition algorithms can analyse and learn spatial and positional relationships within data, extracting useful information required for fault management applications. Furthermore, their ability to continuously learn and adapt to evolving scenarios renders them as robust solutions perfectly aligned with the ever-changing landscape of electrical power infrastructure. These inherent advantages of AI present significant potential to enhance the security, reliability, and efficiency of SC fault management, rendering it a highly promising choice for effectively addressing the unique challenges posed by SCs.

In this context, over the last few years there has been a progressive deployment of AI-based methods in numerous power system applications, including fault management [42–44]. With regards to the research area of superconductivity, AI techniques have been gradually adopted for: i) the discovery of new superconducting materials, ii) the optimisation of the superconductor design process and modelling, and iii) the condition monitoring of large-scale superconducting installations [33].

The reported promising results justify that AI can play a vital role in the dissemination of superconducting applications [45–49]. However, there is no research conducted in the technical literature on the deployment of data-driven techniques in fault detection

and location for SCs. As such, this thesis applies AI methods towards overcoming the limitations of conventional techniques and developing efficient solutions for the fault management of systems with AC and DC SCs.

1.3 Research Methodology

The research proposed in this thesis has been conducted in discrete stages which are presented in Figure 1.2 along with the interdependencies between them.

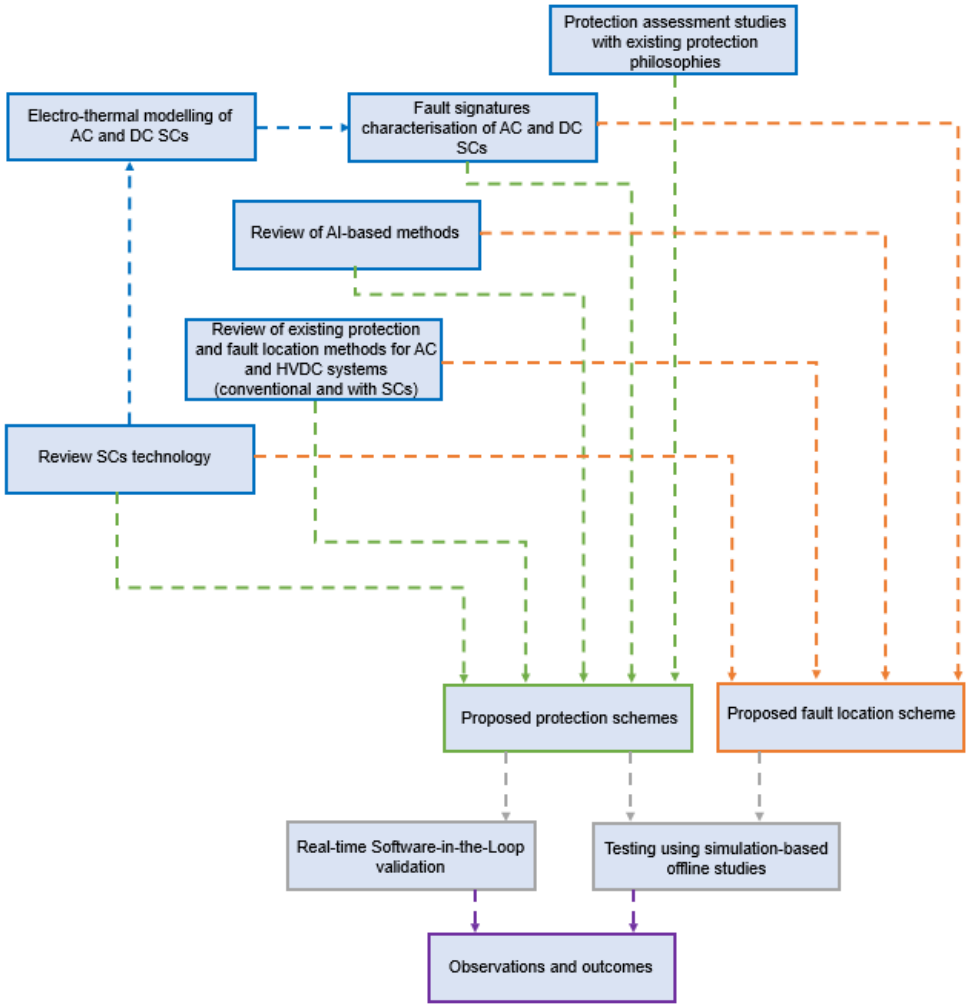

Figure 1.2: Overview of research methodology.

Initially, a review of the operating principles of SCs was carried out in order to provide the theoretical basis for the understanding of such cable technology. The literature review was focused on the main characteristics of the different types of superconductors (i.e., Type I and Type II) and the most widely-used SC configurations. This was followed by a concise literature survey of the emerged challenges, from a fault management perspective,

in the power grids with superconducting feeders. In particular, an extensive review was conducted on the proposed protection and fault location philosophies for SCs in AC grids, aiming to identify the limitations of the proposed methods and determine the research gaps in the fault management of SCs. For the case of DC SCs in HVDC systems, since there is a lack of technical literature related to the fault management solutions, a literature survey was conducted on the incorporated DC SCs within systems and the analysis of their transient behavior, followed by an assessment of the existing protection solutions for HVDC grids. Finally, the AI-based methods for power systems applications have been reviewed and their potential for developing advanced fault management solutions for AC and DC SCs was discussed.

The key findings highlight that there is plenty room for improvement in the research of protection of AC SCs. Although there are a few reported studies which propose protection schemes for AC SCs, there are still many challenges to be resolved in order to provide fast and discriminative fault detection, especially under the influence of highly-resistive faults. With regards to the DC SCs integrated within HVDC systems, there are no reported studies or discussions on fault management. The literature survey showed that many studies have been focused on the fault analysis of DC SCs in meshed systems, however, there is still a need for reliable protection schemes which will comply with the HVDC systems protection requirements and concurrently address the influence of the quenching phenomenon.

On that front, AI-based methods present potential for developing innovative fault detection and identification schemes with strong learning capability for AC and DC SCs. Many protection methods have been proposed in the technical literature for conventional systems without SCs which incorporate AI techniques or hybrid methods which are composed of different AI models or combine AI and signal processing algorithms. Despite the robust performance of such techniques against all fault conditions and their immunity to varying fault parameters (i.e., fault resistance, fault type, and fault location), their practical feasibility has not been discussed and their applicability for real-time implementation has not been examined thoroughly. To guarantee the effectiveness and generalisation capability of AI models for real-world power system applications, comprehensive testing and validation procedures should be conducted. Initally it is important to extract datasets with adequate variability and distinct features and afterwards to perform rigorous validations tests against a variety of fault scenarios (considering different

fault types, locations, internal and external faults). Additionally, continuous monitoring and model retraining, utilising real-time field data from SC operation, can enhance the adaptability and reliability of AI-based protection schemes, ensuring their seamless integration into practical applications. Lastly, evaluating the performance of such schemes in real-time settings becomes indispensable. Conducting tests like Software-In-the-Loop (SIL) or Hardware-In-the-Loop (HIL) tests scrutinises the AI-based protection schemes' real-time performance, providing a critical assessment of their capabilities for real time implementation. These comprehensive steps collectively contribute to the reliability and practicality of AI-driven fault management solutions.

Additionally, it has been found that there is no reported research which addresses the challenge of the fault location on SCs. In this context, the literature survey showed that according to the main advantages and disadvantages of the proposed fault location schemes, AI-based approaches could be considered a promising solution for the precise fault localisation in systems with SCs.

Prior to the development of the algorithms, the fault signature characterisation of SCs is required for the proper design of the proposed schemes. Therefore, at the following stage of the research, the analytical modelling of AC and DC SCs was developed, utilising coupled electro-thermal equations in order to evaluate their transient response and acquire useful insights related to their fault management requirements. For this purpose, a model of an AC power system and a multi-terminal HVDC grid have been developed in Matlab/Simulink. A systematic iterative transient simulation analysis was conducted which aimed to investigate the performance of SCs under different transient conditions by analysing the stages of the quenching process based on the resulting voltage and current signatures.

At the next stage, it was of paramount importance to illustrate the limitations of existing protection methods and subsequently highlight the need for more advanced and efficient solutions. Therefore, existing protection philosophies, such as over-current threshold-based techniques for AC systems and derivative-based protection methods for multi-terminal HVDC systems, have been developed in Matlab/Simulink. The performance of these methods was investigated in compliance with the main protection requirements accounting for sensitivity and stability.

Based on the identified limitations and research gaps, novel protection schemes with discriminative fault detection and classification elements for AC distribution systems

with SCs have been proposed. The developed schemes utilise feature extraction tools, such as signal processing techniques and AI models. Furthermore, the capabilities of the latest AI-trends have been exploited to overcome the fault-related issues in multi-terminal HVDC systems with SCs and provide adequate protection of HVDC substations by enhancing the protection sensitivity, stability, and speed.

The performance of the proposed schemes has been validated by simulation-based analysis, considering all fault types and other disturbances. The results verified the increased sensitivity of the developed schemes and their high operational speed, even during the most challenging scenarios such as highly-resistive faults, and additionally confirmed their stability against other disturbances (i.e., load switching events). Furthermore, the generalisation capability and the learning strength of the proposed AI algorithms was validated against many adverse factors such as additive random noise. Finally, for the evaluation of the practical feasibility of the proposed schemes, their performance was also assessed using real-time Software-In-the-Loop (SIL) testing.

Following the protection schemes and driven by the recent advancements in the pattern recognition techniques for power systems applications, such as image analysis, the presented work addressed the challenges related to fault location on AC SCs. Specifically, a data-driven scheme has been developed which incorporates the transformation of time-domain signals to time-to-frequency domain (spectrograms) and a AI algorithm in order to perform fault localisation along the AC SCs. The effectiveness of the proposed fault location scheme was tested under a wide range of scenarios, including different fault types, fault resistance values, and fault inception angles at various positions. Furthermore, for validation purposes, the developed scheme has been compared with other widely-used data-driven algorithms and its superiority in terms of accurate fault location estimation has been highlighted.

1.4 Principal Contribution

The main objective of the presented work is to fulfill the previously described research gaps and contribute to the area of fault management of AC and HVDC grids with SCs by conducting electro-thermal modelling of AC and DC SCs, investigating the transient performance SCs and developing novel protection and fault location algorithms.

With the general recognition of the sparsity of technical literature regarding novel fault management strategies for AC and DC SCs, the key contributions of this thesis are

listed hereafter:

- Detailed fault signature characterisation of AC and DC SCs integrated into AC systems with ICGs and multi-terminal HVDC grids with Modular Multilevel Converters (MMCs), respectively. Specifically, the performance of SCs has been evaluated through systematic Electro-Magnetic Transient (EMT) type simulation studies under various fault conditions (i.e., highly-resistive faults, close-up faults, DC-side faults, etc.). The main goal is to provide an enhanced insight of the quenching phenomenon and its impact on the prospective AC and DC fault currents and subsequently identify the arisen challenges from a protection perspective. Furthermore, the response of the modelled SCs has been assessed during other transient events (i.e., load switching events). Such a detailed study which considers the influence of different fault parameters (i.e., fault location, fault type, fault resistance, and inception angle) and the impact of other transient events on the quenching of SCs has not yet been found in the technical literature.

- Detailed analysis and investigation of the protection challenges resulting from the deployment of SCs. Simulation-based analysis has shown the limitations of existing protection philosophies for AC systems and multi-terminal HVDC systems with SCs. A series of protection assessment studies were formulated, evaluating the sensitivity and stability margins of the proposed AC and DC protection schemes in the literature (i.e., over-current threshold-based solutions, and derivative-based philosophies). The results indicated that existing protection techniques are not suitable to provide reliable solutions for SCs, introducing a trade-off between protection sensitivity and stability. Therefore, this work highlighted the need for further research protection applications for SCs and for enhanced solutions, which shall consider the unique transient characteristics of such cable technology. No such protection assessment studies have been found in the technical literature, especially for SCs installed in HVDC systems.

- Advanced protection scheme entailing sensitive fault detection and classification components for protection of AC SCs installed in AC systems with ICG units. The proposed schemes utilise data-driven AI-based techniques which are the state-of-the-art trend in power system protection. The performance of the developed data-driven schemes has been scrutinised considering their capability to detect different fault

types occurring on SCs and remain stable against other transient events, such as load-switching events, or external faults. Furthermore, the proposed schemes were tested for real-time implementation using SIL to ensure that such solutions are computationally practical to be implemented in real-time. The results indicated that the proposed schemes are capable of detecting and classifying correctly the internal faults, while remaining stable under the influence of other transient events which lead to the quenching of SCs.

- Novel fault location scheme for the identification of the fault position along the length of AC SCs. This work formed the fault location function as a Machine Learning (ML) regression problem. Specifically, a data-driven scheme has been proposed which exploits the advantages of image analysis techniques and DL algorithms for pattern recognition and feature extraction. The results revealed that the proposed scheme is capable of consistently maintaining high accuracy in the fault location estimation. Furthermore, the effectiveness of the developed fault location scheme has been compared with other data-driven algorithms widely-used in fault location applications.

- Advanced protection scheme composed of fault detection and classification algorithms for DC SCs integrated in multi-terminal HVDC systems, which utilises the principles of the latest trends in AI classifiers. The proposed scheme adopts centralised protection philosophy (on the substation level), is designed to detect and classify faults in HVDC substations accounting for bus faults and faults applied on SCs or conventional feeders, and eliminates the need for a long-distance communication link. The suitability of the developed scheme has been verified using transient simulation-based studies and further validated for real-time implementation using SIL testing to confirm its operation for real-time applications. The results indicated the fast and discriminative fault detection and classification for different fault types, locations, and resistances. On that front, the proposed scheme provides a solid foundation for the safe and reliable incorporation of SCs in multi-terminal HVDC grids.

1.5 Thesis Overview

The thesis is organised into seven chapters. The outline of these chapters is described below:

Chapter 2: provides the theoretical foundation for the basic properties of superconductors and the quenching phenomenon along with a review of the widely-adopted SC configurations. Furthermore, the chapter presents a detailed methodology for the electro-thermal modelling of AC and DC SCs. Specifically, the mathematical formulation of the electro-thermal analogy in SCs is described in detail.

Chapter 3: assesses the transient response of AC and DC SCs and provides useful insights from a fault management perspective. Specifically, this chapter demonstrates the results and key observations of the fault signatures characterisation of AC and DC SCs. This was carried out by means of EMT simulation-based studies considering various fault conditions and transient events.

Chapter 4: presents the development of two novel data-driven protection schemes for AC SCs integrated in AC systems with ICGs. The potential of AI-based protection techniques for the fault management of AC SCs has been identified by the conducted literature survey and the limitations of the existing protection solutions have been revealed by a qualification protection assessment study which considers conventional schemes. The performance of the proposed AI-based schemes were verified based on transient simulation-based studies and real-time SIL testing.

Chapter 5: proposes the development of a novel fault location scheme for AC SCs. The review conducted in this chapter points out the advantages offered by AI methods to fault location applications and their potential for AC systems with SCs. On that front, in this chapter, an advanced fault location scheme based on AI-methods and feature extraction tools is developed to perform the fault localisation on AC SCs. Transient simulation-based studies are employed to verify the robust performance of the proposed scheme. Additionally, a comparative analysis with a widely-used data-driven algorithm in fault location applications is presented to validate the superiority of the proposed scheme.

Chapter 6: describes the development of a novel protection scheme for multi-terminal HVDC systems with SCs which utilises the latest trends in AI classifiers. Considering the identified gap in the technical literature for protection applications in HVDC systems with DC SCs, this chapter initially presents a qualification analysis in order to demonstrate

the limitations of existing protection strategies. The obtained results underline the need for more advanced solutions for the adequate protection of HVDC incorporated DC SCs. Therefore, the development of an innovative protection scheme entailing sensitive fault detection and classification components is discussed and several simulation-based studies are presented to validate its performance. The simulation-based verification is followed by SIL testing which highlights the suitability of the proposed algorithm for real-time implementation.

Chapter 7: concludes the thesis by summarising and highlighting the key observations and the main contributions derived by the presented research. Furthermore, plans and potential avenues for future work in this area are also suggested.

1.6 Publications

Journal Papers - Leading author:

- 'Modelling and fault current characterization of Superconducting Cable with high temperature superconducting windings and copper stabilizer layer',
  E. Tsotsopoulou, A. Dyśko, Q. Elwakeel, M. Elshiekh, W. Yuan, C. D. Booth and D. Tzelepis
  Energies
  DOI: 10.3390/en13246646

- 'Time-domain protection of Superconducting Cables based on Artificial Intelligence classifiers'
  E. Tsotsopoulou, A. Karagiannis, P. Papadopoulos, A. Dyśko, M. Yazdani-Asrami, C.D. Booth and D. Tzelepis
  IEEE Access
  DOI: 10.1109/ACCESS.2022.3142534

- 'Advanced fault location on Superconducting Cables based on Deep Learning algorithms'
  E. Tsotsopoulou, X. Karagiannis, T. Papadopoulos, A. Chrysochos, A. Dyśko, Q. Hong and D. Tzelepis
  International Journal of Electrical Power & Energy Systems,
  DOI: https://doi.org/10.1016/j.ijepes.2022.108860

- 'Protection Scheme for Multi-terminal HVDC System with Superconducting Cables based on Artificial Intelligence Algorithms'
  E. Tsotsopoulou, X. Karagiannis, T. Papadopoulos, A. Chrysochos, A. Dyśko and D. Tzelepis
  International Journal of Electrical Power & Energy Systems,
  DOI: https://doi.org/10.1016/j.ijepes.2023.109037

JOURNAL PAPERS - CO-AUTHOR:

- 'Voltage and current measuring technologies for high voltage direct current supergrids: a technology review identifying the options for protection, fault location and automation applications'
  D. Tzelepis, V. Psaras, **E. Tsotsopoulou**, S. Mirsaeidi, A. Dyśko , Q. Hong, V.C. Nikolaidis, V. Papaspiliotopoulos, G. Fusiek, G. Burt, P. Niewczas and C. D. Booth
  IEEE Access
  DOI: 10.1109/ACCESS.2020.303590

CONFERENCE PAPERS - LEADING AUTHOR:

- 'Protection performance assessment with grid-forming converter acting as reference generator during black-start'
  E. Tsotsopoulou, D. Tzelepis, A. Alvarez, N. Miller and A. Dyśko
  IET - Developments in Power System Protection (DPSP), March 2022
  DOI: 10.1049/icp.2022.0952

- 'Assessment of over-current protection for superconducting cables'
  E. Tsotsopoulou, A. Dyśko and D.Tzelepis
  IET - Developments in Power System Protection (DPSP), March 2022
  DOI: 10.1049/icp.2022.0926

CONFERENCE PAPERS - CO-AUTHOR:

- 'Impact of synchronous condensers on transmission line protection in scenarios with high penetration of renewable energy sources'
  D. Tzelepis, **E. Tsotsopoulou**, V. Nikolaidis, V. Papaspiliotopoulos, Q. Hong and C.D. Booth
  IET - Developments in Power System Protection (DPSP), March 2020
  DOI: 10.1049/cp.2020.0095

BOOK CHAPTERS-CO-AUTHOR:

- 'Measuring technologies for Future Power Grids"

  D. Tzelepis, **E. Tsotsopoulou**, Q. Hong, V. Terzija and C.D Booth

  Reference Module in Materials Science and Materials Engineering, Elsevier, October, 2022

  DOI: https://doi.org/10.1016/B978-0-12-821204-2.00147-1

Chapter 2

Superconductors and Modelling of SCs

2.1 Basic properties of superconductors

Superconductors exhibit remarkable properties, such as zero resistance and magnetic flux exclusion (i.e, diamagnetism), when operating in superconducting state [50]. Three interdependent critical boundaries define the superconducting state of superconductors, as depicted in Figure 2.1. These are the critical temperature, T_C, critical current density, J_C (or critical current I_C), and critical magnetic field, H_C. Superconductors lose their superconducting properties and transition to a non-superconducting region, known as the highly-resistive state, if any of the critical boundaries are exceeded [14].

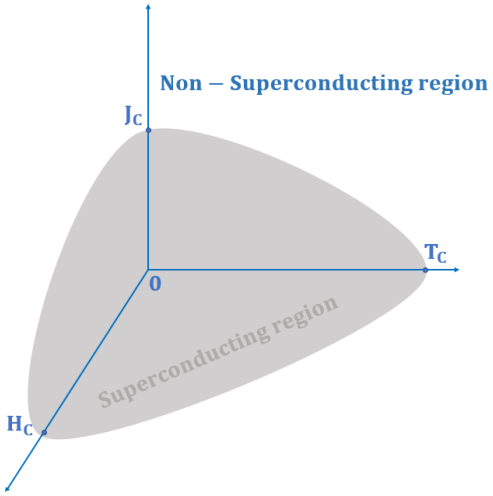

Figure 2.1: Temperature, current-density and magnetic-field locus, highlighting superconducting and non-superconducting regions.

The critical boundary condition of H_C divides the superconductors into two categories, namely Type I and Type II [31]. The external magnetic field, H, is calculated as a function of the magnetisation, M, of the superconducting material and the flux density, B, of the superconductor, and is given by (2.1) [14]:

$$B = \mu_0 \cdot (H + M) \tag{2.1}$$

Type I superconductors obey the Meissner effect which results in the expulsion of the magnetic field from the interior of the superconductor (i.e., $B = 0$ and $M = -H$) [51] during the transition to superconducting state. In particular, when Type I superconductors are cooled below their T_C they present a loss of resistance to the flow of electrical currents. The Meissner effect is realised when the value of the applied external field is below H_C and a screening current is induced inside the volume of the superconductor, canceling the applied magnetic field. Superconductors in the Meissner state exhibit perfect diamagnetism.

When the value of the applied magnetic field exceeds H_C, the magnetic field fully penetrates into the superconductor volume, causing the superconductor to transit to a highly-resistive state (i.e, $M = 0$ and $B = \mu \cdot H$). This is the main limitation of Type I superconductors which are characterised by low values of H_C (e.g., 41 mT) and enter abruptly to the highly-resistive state when they are exposed to low magnetic fields.

Conversely, Type II superconductors have two critical magnetic field boundaries: the lower boundary, H_{C1}, and the upper boundary, H_{C2}. Type II superconductors operate in superconducting state when they are cooled below T_C and the applied magnetic field is lower than H_{C1}. However, they enter into a highly-resistivity state when they are exposed to magnetic fields higher than H_{C2}. The magnetic fields with value between H_{C1} and H_{C2} penetrate partially into the interior of the superconductor in the form of magnetic field vortices (i.e., small tubes where magnetic flux can travel through the material), forcing the superconductor to operate in a mixed state [52]. Therefore, Type II can be subjected to higher external magnetic fields and retain their superconducting properties. Some representative examples of Type II superconductors are Nb_3Sn with H_{C1} equal to 30 T and Yttrium Barium Copper Oxide ($YBCO$) with H_{C1} within the range of $8 - 10$ T [53].

The discovery of Type II superconductors has unlocked many possibilities for the incorporation of superconductivity in large-scale power system applications. Table

2.1 presents a comparison between the main characteristics of Type I and Type II superconductors. Considering the gradual transition to the highly-resistive state of Type II superconductors and their applicability for power system applications, this thesis considers the $YBCO$ superconducting material for the modelling of SCs.

Table 2.1: Comparison between Type I and Type II superconductors.

Type I	**Type** II
Low critical temperature, T_C, up to 10 K	High critical temperature, T_C, greater than 10 K
Low critical magnetic field, H_C	High critical magnetic field, H_C
Obeys the Meissner phenomenon	Partially obeys the Meissner phenomenon
Abrupt transition to highly-resistive state	Gradual transition to highly-resistive state
There is no mixed state	Mixed state exists
Applicable for limited technical applications	Applicable for large-scale power system applications

SCs constitute one of the most widely investigated applications which exploit the benefits provided by superconductors. The superconducting state appears after cooling SCs below T_C, which differs for each type of superconducting material [54]. Within the superconducting region, SCs present perfect conductivity (no resistance to the passage of electrical current), eliminating any dissipation of energy. However, when one of the three critical boundaries is exceeded (i.e., J_C/I_C, T_C, and H_C), due to a transient event (i.e., presence of a fault), the quenching of SCs is initiated. The quenching phenomenon can be defined as the transition of SCs from the superconducting state to the mixed state and finally to the highly-resistive state. In power systems one of the most frequent events which leads to the quenching of SCs is the occurrence of a fault. The quenching phenomenon of SCs will be discussed in more detailed in the following subsections.

2.2 From 2G HTS tapes to SCs

Ever since the discovery of superconductivity, several techniques were investigated with regards to the fabrication of HTS tapes, which constitute the basis of SC manufacturing. It became apparent that composite techniques are required for the fabrication of HTS tapes in order to achieve increased values of J_C, ensure adequate performance of the superconductors in a wide range of magnetic fields, and compensate the manufacturing cost [55]. On that front, after many years of research and development, the invention of $2G$ HTS tapes was a remarkable technical accomplishment which accelerated the integration of SCs in power systems [9]. The transition from $1G$ (first generation) HTS tapes to $2G$ emanates from the fact that the latter provide higher J_C, better mechanical

properties, and are also expected to be more economically profitable [56].

2G HTS tapes are formed as coated conductors and are composed of different layers accounting for a superconducting layer, stabiliser layers, one substrate layer, and one silver layer. The material and geometrical specifications (i.e., thickness, width) of each layer vary depending on the manufacturer, such as American Superconductor Corporation (AMSC), Nexans, Fujikura, Sumitomo Electric and SuperPower. Figure 2.2a illustrates the typical structure of a 2G HTS tape based on the specifications proposed by SuperPower [34]. As can be observed, the superconducting layer is made of $YBCO$ and is deposited on a stack buffered substrate made of Hastelloy $C276$, and is also covered with a silver layer in order to improve the electrical conductivity. Copper stabiliser layers cover the tape to enhance the mechanical strength. The $YBCO$ superconducting layer is solely responsible for conducting the transportation of current, while copper stabiliser layers are utilised as an alternative current path during quenching in order to protect the cable from excessive thermal stresses which can lead to SC destruction.

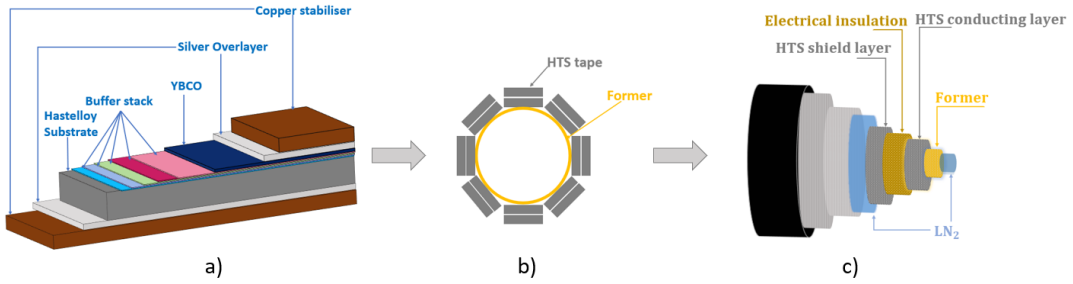

Figure 2.2: Design schematics from 2G HTS tape to SC: a) $YBCO$ Coated Conductor manufactured by SuperPower b) arrangement of HTS tape around former c) typical configuration of SC.

The structure of SCs is composed of many HTS tapes assembled to form a stack. In particular, as can be seen in Figure 2.2b, HTS tapes are attached closely to a stranded former, which is the core of the SC, and are twisted spirally along the stack axis to minimise the gap [57]. The twisting of stacked HTS tapes is important and allows the development of SCs with reduced magnetic flux coupling among HTS tapes, high current-carrying capability, and compact size.

The former of a SC is typically manufactured as a hollow tube made of copper or stainless steel. The main purposes of the former are to provide a bypass current path during quenching (along with the stabiliser layers), mechanical support, and a channel for the liquid cooler. The former should be designed in such a way that imposes the

lowest heat load to the cooling system during quenching [9].

Figure 2.2c shows a typical design schematic for a SC with $2G$ HTS tapes. Several layers of HTS tapes are attached around the former to give the HTS conducting layer and HTS shield layer of the SC. The number of layers of HTS tapes which compose the HTS conducting and shield layers is determined by I_C and the former radius [58]. The shield layer is utilised to block electromagnetic fields. A current in the same order of the transport current flowing through the HTS conducting layer circulates in the shield. A dielectric layer is placed between the HTS conducting and shield layers and provides electrical insulation. The thickness and type of the dielectric material are selected based on the voltage level of the grid. Finally, the SC cooling system is composed of a cryostat with Liquid Nitrogen (LN_2) at $65 - 70$ K, which is circulated in the cable loop to refrigerate the SC and sustain its temperature below T_C [7].

The performance of a SC is determined by the physical properties and geometrical characteristics of the different layers which compose the HTS tapes (i.e., T_C, J_C of superconducting layer, specific heat of each material, thickness and width of each layer), the former thickness and radius, and the type of cooling system [59]. All these factors must be adjusted with respect to the grid parameters (i.e., voltage levels, maximum potential fault current) in order to properly model SCs and investigate their response under different conditions (i.e., steady state and transient) [60]. All these design specifications have been considered in this thesis for the detailed electro-thermal modelling of AC and DC SCs which will be presented in the following subsections.

2.3 Configurations of SCs

SCs are the most advanced of the superconducting-based applications in the energy sector with numerous successful pilot projects around the world [61]. In particular, AC SCs have started to be utilised to solve congestion problems in urban centres or metropolitan areas, while DC SC applications are considered a promising solution for bulk power transmission from remote RES to load centres [62].

Several design topologies of SCs have been developed in recent years in an attempt to minimise the capital and operating costs, and accelerate the commercial deployment of such technology. The diversity in the applications of SCs results in different electromagnetic structures, dielectric types, and cooling system configurations, with each offering their own advantages and limitations [9].

The configurations of SCs can be classified into distinct categories based on the layout of the layers of HTS tapes, as well as the voltage level. The most widely used geometric configurations are depicted in Figure 2.3 and include: i) the concentric SC (triaxial) (Figure 2.3a), ii) the triad or "three-core" SC (three phases in one cryostat) (Figure 2.3b) and iii) the "single-core" SC (three separate phases with seperate cryostats) (Figure 2.3c).

The concentric configuration of an AC SC is presented in Figure 2.3a. The most important attribute of this configuration is the compact size, which reduces the total cryogenic surface area, utilises less superconducting material, and subsequently reduces the cost [7]. The layers of HTS tapes are helically wound around the former tube, while three layers of dielectric separate the three phases for AC SCs. This configuration offers higher current-carrying capacity, and has the lowest inductance compared to other cable designs [57]. However, the major drawback is the non-uniform distribution of the current among HTS tapes, making the manufacturing process more challenging [63]. This design has been successfully implemented for voltage levels within the range of 13.8 kV-50 kV [64].

Figure 2.3b shows an AC SC with the three phases placed within the same cryostat. This structure leads to a larger cable size and requires the addition of a HTS shield layer in order to reduce the magnetic field, resulting in increased cost [65]. The main advantage of this cable configuration is the uniform current distribution among HTS tapes. In practical deployment, triad SCs are utilised for voltage levels higher than 66 kV.

Finally, a single-core SC is shown in Figure 2.3c. In this type of cable configuration, each conductor is contained in separate cryostats and is usually recommended for voltages up to 138 kV for bulk power transmission over long distances [29]. However, as each conductor requires separate inlet and outlet paths for cooling, the cost is dramatically increased.

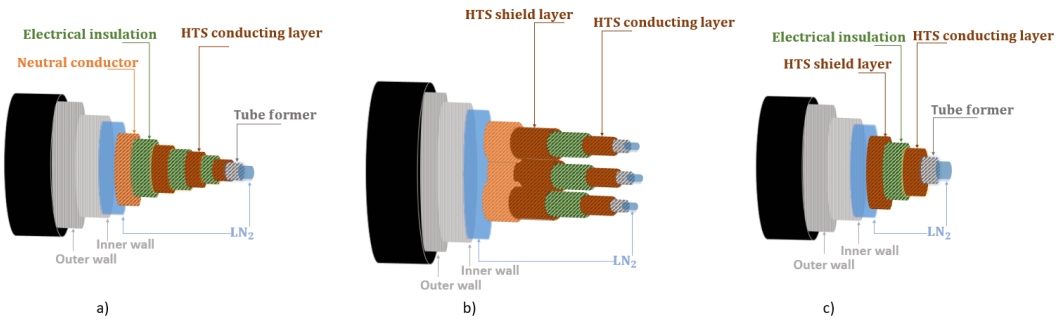

Figure 2.3: Overview of SC design: a) concentric b) triad c) single-core.

SCs are also classified with respect to the type of dielectric used. Specifically, in Cold Dielectric (CD) SCs, the electrical insulation layer is usually made of Polypropylene Laminated Paper (PPLP) and is kept at cryogenic temperatures in the inner envelope [60]. This type of SC consists of a large cooling surface area, resulting in a smaller heat load and higher cooling power. Conversely, in Warm Dielectric (WD) SCs, the dielectric layer is not immersed in the cooling liquid, reducing the power required for cooling [66]. The main drawbacks of the WD configuration is the need for separate cryostats for each conductor, more expensive electrical insulation, and higher inductances and capacitances [9]. Table 2.2 presents a comparison between CD and WD SCs.

Table 2.2: Comparison between CD and WD SCs.

Characteristics	**WD**	**CD**
Magnetic field	Present	Cancelled
AC Losses	High	Low
Current-carrying capacity	High	Very high
Type of dielectric layer	XLPE	PPLP
SC inductance / capacitance	Similar to conventional cables	Low
Number of cryostats	Seperate cryostat for each conductor	Conductors in the same or separate cryostat
Type of shield layer	Metallic material	Metallic or HTS material

In the presented research, a CD single-core configuration has been considered for the modelling of SCs as they present lower losses and increased current-carrying capability.

2.4 Electrical equivalent of HTS tapes and the quenching of SCs

The quenching of a SC determines the transition to the highly-resistive state, leading to temperature increase as well as thermal and electromagnetic forces [67]. Analysing the quenching phenomenon is of paramount importance in the development of SC models which will accurately represent their electro-thermal behaviour. The utilisation of electrical equivalent circuit models has been considered as one of the fastest and most accurate methods to gain a better understanding of the electro-thermal response of SCs under different system conditions (i.e., steady state and transient) [68]. Based on the electrical equivalent approach, HTS tapes (Figure 2.2a) can be modelled as parallel connected electrical resistances which correspond to each layer of HTS tape (i.e., superconducting layer, stabilisers, substrate silver). In this context, each conductor of the SC is modelled as the equivalent electrical circuit of all HTS tapes and the former, connected in parallel. Figure 2.4 shows the equivalent electrical circuit of one HTS

tape. The self and mutual inductances have been neglected at this stage for the tape analysis [69] (self and mutual inductances have been considered during the detailed electro-thermal modelling of SCs).

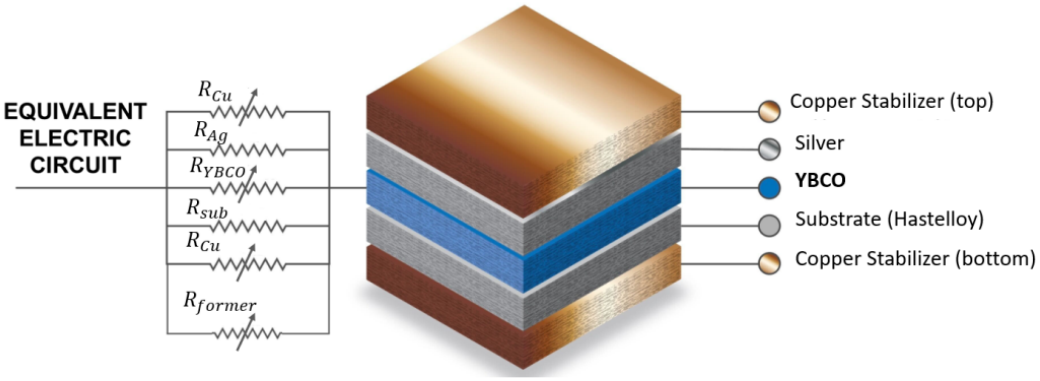

Figure 2.4: Equivalent circuit model of an HTS tape.

As can be observed in Figure 2.4, the resistance of the $YBCO$ layer, R_{YBCO}, copper stabiliser layers, R_{CU}, and former, R_{former}, have been modelled as variable resistors in order to represent their variability during quenching. Conversely, the resistance of the silver, R_{Ag}, and substrate, R_{sub}, layers have been modelled as constant resistances, as their change during quenching is comparatively negligible.

In steady state conditions, SCs operate in superconducting state and transmit bulk power with approximately zero losses. Under these conditions, the current flows solely through the $YBCO$ layer and the SC behaves as a perfect conductor. During transient events (i.e., faults) when the current flowing through the SC increases, the $YBCO$ layer starts to quench, losing its superconducting properties. Specifically, when the current exceeds a predefined threshold, known as the critical current, I_C, the current density exceeds the threshold J_C and quenching is initiated. In this thesis the uniform current distribution among the HTS tapes has been assumed and the SC has been modelled as lumped model, allowing for the consideration of simultaneous quenching along the SC length. It should be noted that this simplification does not adversely affect the efficacy of the developed protection and fault location schemes which rely on the resulting fault current and voltage signatures across the entire cable.

Under these transient conditions, R_{YBCO} undergoes a non-linear increase and the SC operates in the mixed state (intermediate state between superconducting and highly-resistive). During the mixed state, the current starts to be diverted into the copper stabiliser layers and the former, which present lower resistances compared to $YBCO$.

This is known as the current sharing process. The amount of current which is diverted to the copper stabiliser layers and the former is dependent on their design specifications.

When the current starts flowing through the copper stabiliser layers and the former, this causes the generation of Joule heat which subsequently leads to an increase in the temperature, T, of the SC. On that front, R_{CU} and R_{former} increase as a function of T and consequently the total resistance of the SC reaches very high values, affecting the system current magnitudes. The rapid increase in the total resistance of the SC causes further increases in T. When the value of T exceeds the value of T_C, the SC enters the highly-resistive state within milliseconds (i.e., a single AC cycle). The time required for the transition of the SC from superconducting state to the highly-resistive state is dependent on system conditions and the cooling system which is responsible for the removal of the generated Joule heat [9]. The flowchart presented in Figure 3.2 shows a representation of the quenching phenomenon.

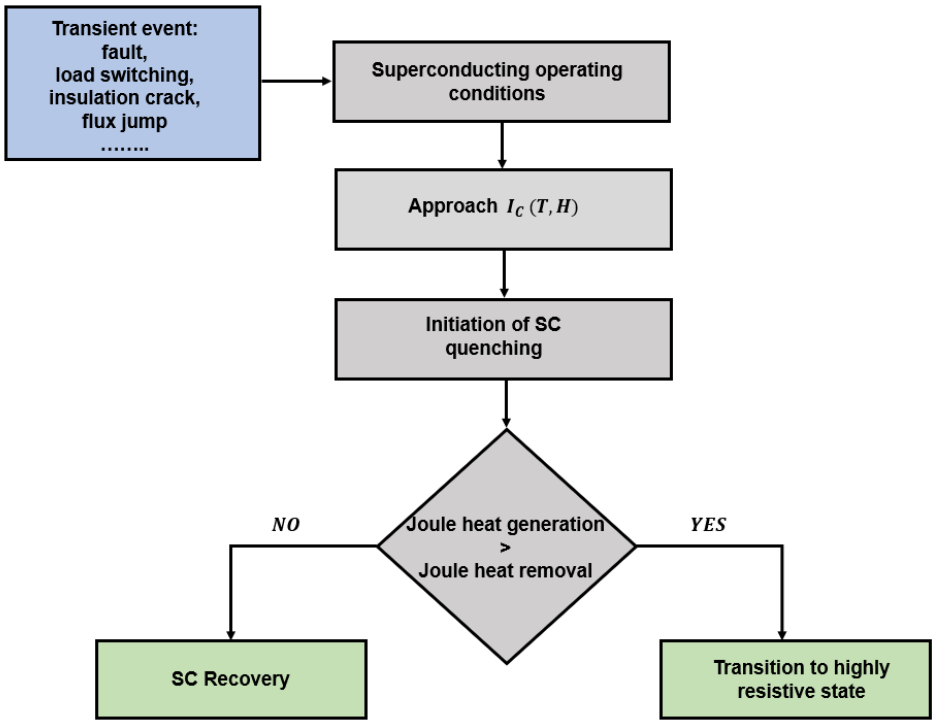

Figure 2.5: Overview of quenching phenomenon

Hence, it can be concluded that the quenching of SCs enforces the appearance of a variable resistance which imposes: i) the current redistribution within the SC, ii) a dynamic change in the equivalent resistance of the system, and iii) has an impact of the fault signatures. All these factors introduce new variables in the fault management of power grids with SCs, which is the main focus of the presented research. Therefore, the

investigation of SCs inherent current-limiting capability, as an extension of their primary function as a lossless transmission media, is rendered imperative.

2.5 Electro-thermal modelling of AC SC

The previously discussed principles of superconductors along with the design specifications of HTS tapes form the basis for the electro-thermal modelling of SCs. This section presents the mathematical formulation of coupled electro-thermal modelling of an AC SC composed of three single-core phases and $2G$ HTS tapes in Matlab/Simulink.

2.5.1 Numerical modelling of the HTS tapes

In the presented work, the structure of the commercially available $2G$ HTS tape proposed by SuperPower and presented in Figure 2.2a has been selected. The electrical equivalent circuit of each tape corresponds to that illustrated in Figure 2.4. For the modelling of the SC, the lumped electrical parameters model coupled with a discrete thermal model has been utilised.

The number of HTS tapes within the SC has been selected considering the derating factor, λ, given by (2.2), which expresses the ratio between the operating current at superconducting state, I_{op}, and the I_C of the HTS tapes at zero applied magnetic field [31, 70]. A λ equal to 80 % has been chosen to consider a safety margin of 20 % before quenching and achieve high power transfer in steady state conditions:

$$\lambda = \frac{I_{op}}{I_C} = 80\% \tag{2.2}$$

For simplification of the electro-magnetic performance of the SC, a uniform distribution of the current has been assumed among HTS tapes and a uniform distribution of the current density, J, among each tape [71].

The transition from the superconducting state to the highly-resistive state can be described by the $E-J$ power law and the resistivity of the superconducting layer $YBCO$, ρ_{YBCO}, is given by (2.3):

$$\rho_{YBCO} = \frac{E_C}{J_C(T)} \cdot \left(\frac{J}{J_C(T)}\right)^{n-1} \tag{2.3}$$

where, $E_c = 1$ $(\mu V/cm)$ refers to the critical electric field, J denotes the operating current density (A/m^2), and n is a superconductor macroscopic property related to the

steepness of the transition to the highly-resistive state which has been set equal to 30 [72]. Finally, J_C is the critical current density (A/m^2) and it is calculated as a function of T (K) and the working magnetic field, H (T), based on (2.4):

$$J_C(T) = \begin{cases} J_{C0}(H) \cdot (\frac{(T_C - T(t))^a}{(T_C - T_0)^a}) & \text{for} \quad T < T_C \\ 0 \quad \text{for} \quad T \geq T_C \end{cases} \tag{2.4}$$

where, J_{C0} is the critical current density (A/m^2) at the initial temperature, $T_0 = 70$ (K), and has been set to 1.5 [59].

When a SC operates in superconducting state, J is below J_C, T is below T_C, and $\rho_{YBCO} = 0$ Ωm. Consequently, the current flows predominantly through the $YBCO$ layer, generating approximately zero losses. Conversely, during transient conditions, when the current flowing through the SC increases and quenching is triggered, the $YBCO$ layer presents high values of resistivity (higher compared to normal conductors in cryogenic conditions [67]). Specifically, under these conditions, ρ_{YBCO} presents a non-linear increase according to (2.3), J_C is reduced to 0 A/m^2 and the SC operates in a mixed state. As it was mentioned in subsection 2.4, during the mixed state, the current starts to be diverted into the copper stabiliser layers and the former, resulting in a further increase in T which leads to a transition to the highly-resistive state. In the highly-resistive state, the resistivity of the copper stabiliser layers, ρ_{Cu}, changes as a function of T based on (2.5) [73]:

$$\rho_{Cu} = (0.0084 \cdot T - 0.4603) \cdot 10^{-8}, \; 250 \; K > T \geq 70 \; K \tag{2.5}$$

During the modelling of HTS tapes, R_{Ag} and R_{sub} have been neglected as they do not have any significant impact on quenching. However, the thickness of the substrate and silver layers have been considered in the modelling process as the total thickness of the HTS tape affects the thermal properties of the SC. The specifications of the employed HTS tapes are presented in Table 2.3 [34].

2.5.2 Structure of AC SC

The AC SC has been devised with a cross-sectional structure as depicted in Figure 2.6 and composed of three conductors contained in three separate cryostats. Table 2.4 details the geometrical characteristics of the developed AC SC.

Each phase consists of the former, HTS conducting layer, insulation layer, and HTS

Table 2.3: Specification of the HTS tape for the AC SC.

Parameters	Value
Thickness of $YBCO$ layer	1 μm
Thickness of copper layer	40 μm
Thickness of substrate layer	60 μm
Thickness of silver layer	3.8 μm
Tape width	4 mm
Tape critical current	250 A
Tape critical temperature	92 K

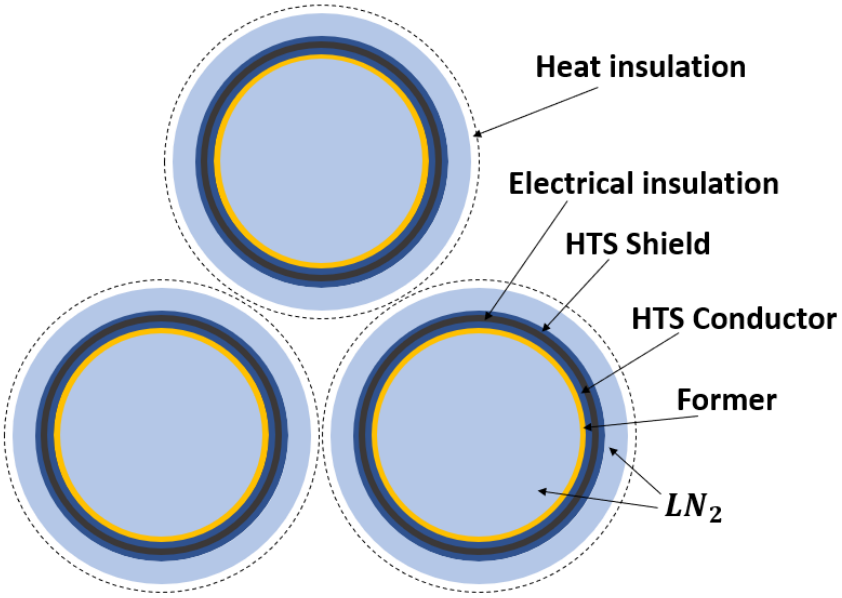

Figure 2.6: Cross-section of the AC SC model.

Table 2.4: Geometrical characteristics of AC SC.

Layer	Outer radius
Former tube (steel)	16.5 mm
HTS conducting layer	16.64 mm
Electrical insulation	18.64 mm
HTS shield layer	18.78 mm
Heat insulation	21.78 mm

shield layer. A PPLP, CD layer was considered between the HTS conducting and shield layer, acting as electrical insulation, while permitting the SC to operate at relatively low temperatures. The SC cooling system is composed of a cryostat with Liquid Nitrogen (LN_2) at $65 - 70$ K. The former is made of stainless steel and is modelled as a hollow tube. The resistivity of the former as a function of T is given by (2.6) [59]:

$$\rho_{steel} = 1.193 \cdot 10^{-6} - 7.529 \cdot 10^{-7} \exp(-T/647.113) \tag{2.6}$$

The total resistance of the SC is equal to the equivalent resistance of the parallel connected layers of the HTS tapes and the former, and is given by (2.7).

$$R_{SC_{eq}} = \begin{cases} R_{YBCO_{eq}} & \text{for} \quad T < T_C \; and \; I_{op} < I_C \\ R_{YBCO_{eq}} // R_{Cu_{eq}} // R_{former} & \text{for} \quad T < T_C \; and \; I_{op} > I_C \\ R_{Cu_{eq}} // R_{former} & \text{for} \quad T > T_C \; and \; I_{op} > I_C \end{cases} \tag{2.7}$$

where $R_{YBCO_{eq}}$ indicates the equivalent resistance of the $YBCO$ layer of all parallel connected HTS tapes, $R_{Cu_{eq}}$ corresponds to the equivalent resistance of the stabiliser layers of all parallel connected HTS tapes and $R_{SC_{eq}}$ is the equivalent resistance of the SC. The $R_{SC_{eq}}$ changes with respect to the operating state of the HTS tapes. Once the quenching is initiated and the current is shared among the $YBCO$ layers, copper stabiliser layers and former, the $R_{SC_{eq}}$ of the SC is calculated as the equivalent resistance of the parallel connected $R_{YBCO_{eq}}$, $R_{CU_{eq}}$ and R_{former}. In the highly-resistive state, the whole current is diverted to the copper stabiliser layers and the former, and therefore $R_{SC_{eq}}$ is given as the equivalent resistance of the parallel connected $R_{CU_{eq}}$ and R_{former}.

The per-unit length capacitances, C, and inductances, L, of the SC have been derived using the ATP-EMTP software based on the general formulation provided in [74]. For the calculation of C and L, the conducting layers and the shield layers of each phase have been considered along with the solenoid effect caused by the axial magnetic field generated by the helically wound HTS tapes around the former. The impact of the solenoid effect on the L calculation has been considered based on the approach proposed in [75]. Based on the structure of the SC in Figure 2.6, the electrical equivalent of the three phases of the AC SC can be established as shown in Figure 2.7. Each layer of each phase is composed of a variable resistance and self inductance. Moreover, there are mutual inductances between the layers. Specifically, $M_{C_iS_i}$ corresponds to the mutual inductance between the conducting and shield layer of phase i, $M_{C_iC_j}$ indicates the

mutual inductance between the conducting layers of phases i and j, $M_{S_iS_j}$ denotes the mutual inductance between the shield layers of phases i and j, and finally, $M_{C_iS_j}$ is the mutual inductance between the conducting and shield layer of phases i and j.

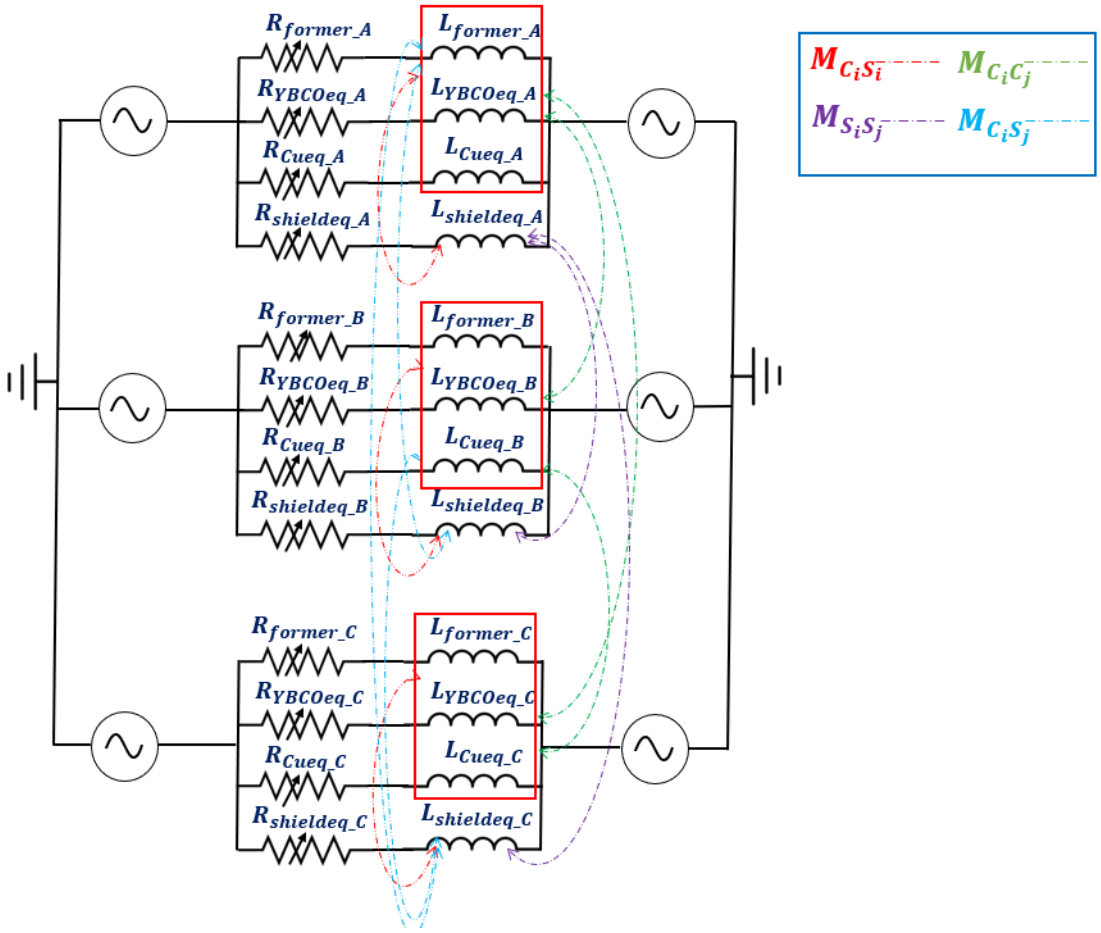

Figure 2.7: Electrical equivalent parallel circuit diagram of AC SC.

2.5.3 Thermal modelling

In this subsection, the electro-thermal analogy is employed in order to model the coupling between the thermal and electrical phenomena. Based on this approach, currents are translated into Joule heating and the resulting temperature variations into changes to the temperature-dependent properties of the SC.

Thus, considering the electro-thermal coupled modelling formulation, the sudden loss of superconductivity during quenching is translated into heat generation by the superconductor. The Joule heating generated by the SC due to the variations in $R_{SC_{eq}}$ is described by (2.8)

$$P(t)_{diss} = I(t)^2 \cdot R_{SC_{eq}} \tag{2.8}$$

where $I(t)$ (A) is the total current flowing through the SC.

Assuming that there is no heat transfer with the external environment, part of the generated Joule heat leads to an increase in T and the rest is absorbed by the LN_2 cooling system. In this adiabatic regime, the cooling power that is removed by the LN_2 refrigeration system is obtained with (2.9):

$$P(t)_{cooling} = h \cdot A \cdot (T(t) - 70) \tag{2.9}$$

where A (m^2) is the total area covered by the LN_2 cooling system and h $(W/m^2 \cdot K)$ is the heat transfer coefficient which determines the effectiveness of the cooling system and the time of SC recovery after quenching. The heat transfer coefficient, h, is a function of the temperature variation, ΔT, and has been calculated according to [76].

Considering the law of conservation of energy and combining equations (2.8) and (2.9), the net power of the SC is calculated by (2.10):

$$P(t)_{SC} = P(t)_{diss} - P(t)_{cooling} \tag{2.10}$$

Eventually, the increase in T of the SC can be calculated through (2.11):

$$T(t) = T_{t-1} + \frac{1}{C_{SC}} \cdot \int_0^t P(t)_{SC}\, dt \tag{2.11}$$

where C_{SC} (J/K) denotes the total heat capacity of the SC and is calculated as a function of the specific heat and the mass of the material of each SC layer. More specifically, the heat capacity of $YBCO$, C_{YBCO}, is given by (2.12):

$$C_{YBCO} = 2 \cdot T \cdot d_{YBCO} \cdot v_{YBCO} \cdot N \tag{2.12}$$

where d_{YBCO} (kg/m^3) is the density of the $YBCO$ material, v_{YBCO} (m^3) is the volume of the $YBCO$ layer, and N is the number of HTS tapes.

The heat capacity of the copper stabiliser and Hastelloy layers is calculated based on (2.13) and (2.14), respectively:

$$C_{CU} = c_{CU} \cdot d_{Cu} \cdot v_{Cu} \cdot N \tag{2.13}$$

$$C_{sub} = 2 \cdot T \cdot d_{sub} \cdot v_{sub} \cdot N \tag{2.14}$$

where d_{Cu} (kg/m^3) and d_{sub} (kg/m^3) are the density of copper and the substrate, respectively, c_{Cu} $(J/kg \cdot K)$ is the specific heat of copper, and finally, v_{CU} (m^3) and v_{sub} (m^3) are the volume of the copper stabiliser and substrate layers, respectively.

Similarly, the heat capacity of the electrical insulation and steel former are derived by (2.15) and (2.16), respectively:

$$C_{PPLP} = c_{PPLP} \cdot d_{PPL} \cdot v_{PPLP} \tag{2.15}$$

$$C_{steel} = c_{steel} \cdot d_{steel} \cdot v_{steel} \tag{2.16}$$

where d_{PPLP} (kg/m^3) and d_{steel} (kg/m^3) are the density of the PPLP and steel, respectively, c_{PPLP} $(J/kg \cdot K)$ and c_{steel} $(J/kg \cdot K)$ are the specific heat of the electrical insulation and the former, respectively, and v_{PPLP} (m^3) and v_{steel} (m^3) are the volume of the electrical insulation and the former.

For simplification of the modelling procedure, it has been considered that the HTS shield and the HTS conducting layers of each phase conductor, illustrated in Figure 2.6, consist of the same number of HTS tapes with the same specifications. Therefore, the total heat capacity of the SC, C_{SC}, is expressed according to (2.17):

$$C_{SC} = 2 \cdot C_{YBCO} + 2 \cdot C_{CU} + 2 \cdot C_{sub} + C_{PPLP} + C_{steel} \tag{2.17}$$

The values of the density and specific heat of each material are given in Table 2.5.

Table 2.5: Specific heat and density of each material.

Parameter	**Value**
Density of $YBCO$	5900 kg/m^3
Density of stainless steel	7500 kg/m^3
Density of copper	8940 kg/m^3
Specific heat of copper	185 $(J/kg \cdot K)$
Specific heat of stainless steel	21.78 $(J/kg \cdot K)$
Specific heat of PPLP	1930 $(J/kg \cdot K)$

It's worth reiterating that in the adopted electro-thermal modeling of SC, there exists an interdependence between current and temperature. When the current exceeds the

critical level, quenching occurs, resulting in the generation of Joule heat. This heat, in turn, elevates the cable's temperature, leading to changes in the temperature-dependent parameters. While the inductance and capacitance are typically considered constant during quenching based on [7, 73], the influence of the cable's structure on the magnetic field has been accounted by calculating mutual and self-inductances according to [74]. In this context, to achieve high-fidelity temperature-dependent modelling, an error tolerance is also applied in the thermal model which determines the temperature at each time step. Figure 2.8 shows an overview of the modelling process as developed in Matlab/Simulink which calculates the temperature at the next time step, T_{k+1}, based on (2.18):

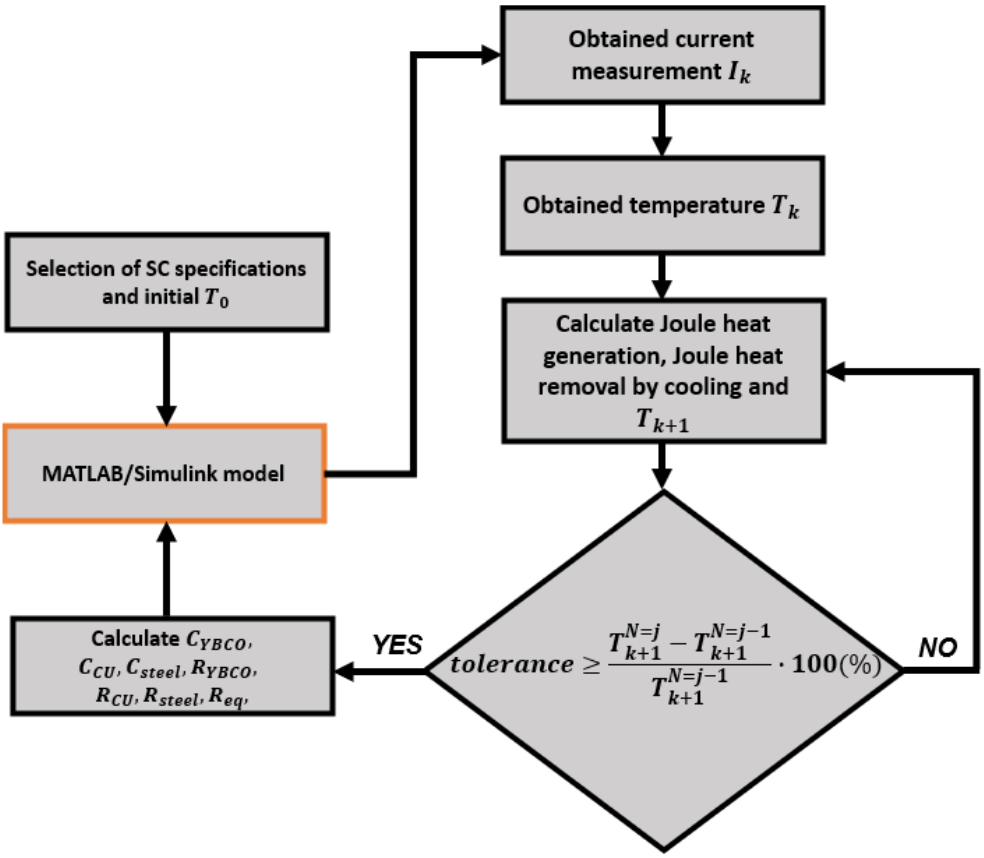

Figure 2.8: Electro-thermal modelling process of SC as developed in Matlab/Simulink.

$$e \geq \frac{T_{k+1}^{N=j} - T_{k+1}^{N=j-1}}{T_{k+1}^{N=j-1}} \cdot 100(\%) \tag{2.18}$$

where I_k and T_K are the current and temperature measurements of time step k respectively, and T_{k+1} is the calculated temperature of the next time step $k+1$. The index j indicates the simulation step. The calculation of T_{k+1} at each time-step is based

on an iterative process which is executed N times in order to realise the temperature tolerance constraint. At the end of each time step, the temperature-dependent properties of the SC are updated according to the T_{k+1} value. In the developed model, the value of e has been set to 0.01%.

2.6 Electro-thermal modelling of DC SC

The same mathematical formulation of the coupled electro-thermal modelling has been utilised for the development of two DC SCs. Specifically, the electro-thermal characteristics of both DC SCs have been modelled in Matlab/Simulink by combining equations (2.2) to (2.18).

The schematic configuration of the DC SCs is illustrated in Figure 2.9 and it consists of two concentric poles, the positive and negative pole [70]. The positive pole is located on top of the steel former and is composed of the HTS layer and copper stabiliser layer. The negative pole is placed on top of the electrical insulation layer and consists of the same number of HTS tapes which compose the HTS layer and the stabiliser layer. The current passing through the negative pole is nearly identical to the current flowing through the positive pole, but with opposite direction [77]. Similarly, to the case of AC SCs, the $YBCO$ superconducting material has been adopted for the HTS tapes. The number of HTS tapes is closely related to the determination of I_C for the DC SC, while the thickness of the dielectric material has been chosen in accordance with the voltage level of the grid. For the cooling of the DC SCs, LN_2 is circulating in the cable loop to sustain a constant T within the range of $65-70\ K$. All the layers are contained within a cryostat which provides thermal insulation.

The final (per unit length) values of C and L of the two DC SCs have been calculated utilising the general formulation proposed in [74]. The specifications of the HTS tapes are the same as those presented in Table 2.3. The only difference is the value of I_C, which is equal to 140 A for DC SC1 and 120 A for DC SC2. The geometrical characteristics of both DC SCs are presented in Table 2.6.

2.7 Summary

This chapter provides the theoretical background of the superconductors and their properties in order to provide the basis for the development of proper SC models.

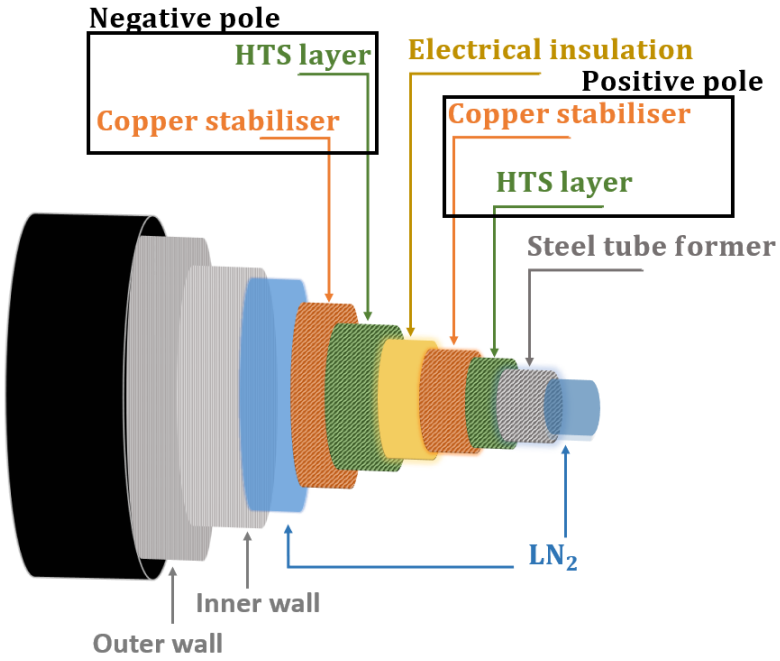

Figure 2.9: Schematic illustration of DC SC.

Table 2.6: Geometrical characteristics of DC SC1 and SC2.

Layer	Outer radius
Positive pole of SC1 / SC2	15.14 mm / 17.50 mm
Electric insulation of SC1 / SC2	27.14 mm / 29.50 mm
Negative pole of SC1 / SC2	27.28 mm / 29.64 mm
Outer wall of SC1 / SC2	110.23 mm / 111.34 mm

Superconductors are classified into Type I and Type II based on their behaviour in the applied external field. The analysis showed that Type II superconductors are characterised by more advantageous features compared to Type I as they present a gradual transition to the highly-resistive state and preserve their superconducting properties under a wider range of temperature. Additionally, the main advantages and drawbacks of the different SC configurations have been discussed. The selection of the proper cable configuration is determined by the operating voltage levels and the cost. Furthermore, SCs are categorised as either WD or CD with respect to the dielectric type. WD SCs present lower cooling requirements, however, their electrical insulation is more expensive than that of CD SCs and have higher inductances and capacitances. Furthermore, the structure of $2G$ HTS tapes has been analysed along with the quenching phenomenon which dictates the performance of SCs.

Following the theoretical background, the detailed mathematical formulation of the electro-thermal modelling of AC and DC SCs in Matlab/Simulink is presented.

Specifically, the electro-thermal analogy is employed in order to simplify the coupling between the thermal and electrical phenomena in SCs. On that front, the currents flowing through the SC, during quenching, lead to the generation of Joule heating, causing an increase in T of the SC. The subsequent temperature variations result in changes to the temperature-dependent properties of the SCs (i.e., C_{SC}, J_C, ρ_{YBCO}, ρ_{CU}) which have been captured with high accuracy.

For the selection of the design specifications, it has been revealed that HTS tapes must be protected electrically and thermally during quenching, considering alternative current paths (i.e., copper stabiliser layers). The number of HTS tapes which are wound around the former is determined based on the I_C of the SC and the former radius. Furthermore, the former specifications should be selected in a proper way in order to minimise the heat load on the cooling system, while the shield layer should be designed properly to provide a return path for the current.

Chapter 3

Fault Characterisation of AC and DC SCs

The fault analysis of SCs plays a vital role in preserving power systems safety, reliability and efficiency. During fault conditions, if SCs are not properly designed and adequately protected, they can be completely damaged during quenching (i.e., burnout, mechanical collapse, deformation, etc.). Therefore, it is important to study deeply the fault behaviour of SCs along with the influence of fault parameters on their fault response (i.e., fault type, location and resistance) prior to their deployment in power systems.

As the transient performance of SCs is dominated by the quenching phenomenon and electrothermal properties of HTS tapes [78], their implementation within AC and DC systems introduces new variables to the grid operation (i.e., variable resistance, reduced fault current magnitudes, etc.) and leads to many fault management challenges, accounting for fault detection, fault location and protection. Therefore, within the scope of developing advanced and reliable fault management solutions for SCs, extensive assessment studies are required in order to evaluate the performance of such cable technology under different transient conditions and reveal the challenges from the fault management perspective. On that front, a detailed fault characterisation of AC and DC SCs is analysed and discussed in this chapter, presenting a variety of fault scenarios. Such studies have been carried out utilising a model of an AC power system with the inclusion of ICGs, and a multi-terminal HVDC network with incorporated DC SCs. It is important to note that the challenges of protecting more complex multi-terminal HVDC grids often can cover the challenges met in point-to-point HVDC systems.

3.1 Power System Modelling and Fault Characterisation of AC SC

AC superconducting-based transmission technology is being progressively explored and its investigation has reached a more mature stage compared to that of DC superconducting-based technology. As reported in Chapter 1, the first SC projects were focused on the deployment of short-length AC SCs, creating the proper foundation for numerous demonstration sights and pilots [79, 80]. The dominant application of AC SCs consists of high capacity connections utilised to tackle congestion challenges and interconnect weak systems with great demand. Although SC applications are expected to be hugely influential for power transmission in future power grids, there are still challenges to be resolved emanating from their unique physical features and the lack of standardisation for the testing and fault performance analysis of SCs [9].

With the scope of acquiring a deeper insight into the transient performance of AC SCs, this chapter investigates the response of the AC SC model developed in Chapter 2 by conducting iterative simulation-based fault analysis under different fault conditions. More specifically, the simulation-based studies aimed to analyse the different stages of the quenching process along with the resulting fault current and voltage waveforms.

3.1.1 AC power system model

For the purposes of carrying out the assessment of AC SC fault response, EMT simulation studies have been conducted, considering the power system depicted in Figure 3.1.

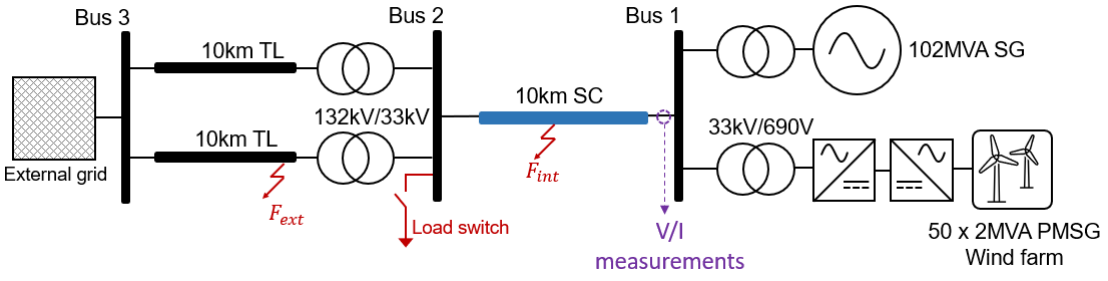

Figure 3.1: Test network.

The network under test has been developed in Matlab/Simulink and consists of a voltage source connected to Bus 3 with nominal voltage of 132 kV, which represents the equivalent network, and two different generation units, accounting for a SG and ICG, both connected to Bus 1 [81]. The SG unit has a nominal capacity of 102 MVA and for

modelling purposes, a standard salient pole synchronous machine has been utilised along with the integration of Automatic Voltage Regulator (AVR), Power System Stabiliser (PSS) and over-excitation limiter [82]. The ICG unit (i.e., a wind farm cluster) has a total capacity of 100 MVA and constitutes permanent magnet SGs connected via a Voltage Source Converter (VSC). The incorporated control scheme for the converters is the standard d-q axis current injection (DQCI).

A 10 km SC has been integrated between Bus 1 and Bus 2 at 33 kV for the power transmission from the generation units to the wider electrical grid. The parameters of the developed AC SC are presented in Table 3.1.

Table 3.1: Parameters of AC SC

Parameter	**Value**
Number of tapes n_{tapes}	25
Operating temperature T_0	70 K
Critical temperature T_C	92 K
Critical current per tape I_C	250 A
SC's length l	10 km
Rated voltage V	33 kV
Rated capacity S	202 MVA

The conducted studies consider different fault scenarios (i.e., internal and external faults) and transient events (i.e., load switching events). The ultimate goal is to disclose potential fault management challenges and consequently identify the requirements for the secure and reliable operation of AC SCs. One of the main prerequisites for designing protection and fault location schemes is to investigate the distinctive features and effects of internal faults (faults within the protection zone which must cause the initiation of a tripping signal), external faults (faults beyond the protection zone which must not lead to the initiation of a tripping signal) and transient events which must not lead to protection operation, in order to ensure the protection sensitivity, stability, selectivity and fault location accuracy. For that purpose, the presented studies aim to qualify and quantify the behavior of AC SC quenching during internal faults, occurring along AC SC's length, external faults applied at the adjacent lines, and load switching events.

Specifically, the simulated fault scenarios include all types of internal and external faults, accounting for three-phase (LLL), three-phase to ground (LLL-G), phase-to-phase (LL), phase-to-phase to ground (LL-G) and phase to ground (L-G), with different values of fault resistance R_f, (within the range of 0 Ω up to 300 Ω) [83]. Considering the

configuration of the developed SC, shown in Figure 2.6, an LL fault for example can be occurred when the superconducting layers of two adjacent phases come into direct electrical contact due to some external force, or mechanical stress applied to the SC, or degradation, or corrosion of the cable's insulation and protective layers. These type of faults may lead to cooling system malfunction and lead to quenching of SC. Furthermore, if the fault involves a breach in the cryogenic insulation layer, it may result in the leakage of LN2 from the cable. This can happen because the fault compromises the integrity of the cryogenic insulation.

Internal faults were applied at varying fault position along AC SC's length, considering as a reference the SC terminal connected at Bus 1, while external faults were applied at adjacent lines. Load switching events were simulated as the connection of loads, with different values of active and reactive power, at Bus 2.

3.1.2 Fault response of AC SC during different scenarios

The selected scenarios analysed in this subsection are summarised in Table 3.2. In particular, this subsection presents the simulation results of an LL-G internal solid fault applied at 40% of the AC SC's length, an LL-G internal resistive fault at 40% of the AC SC's length, an LL-G external solid fault at 30% of the adjacent line's length, and a load switching event with $P = 80\ MW$ and $Q = 20\ MVAr$. The main goal of this selection is to scrutinise the response of the AC SC against solid internal faults, assess the impact of fault resistance on SC quenching and investigate the potential of external faults and other transient events to lead to SC quenching. During all the scenarios, the fault or load switching event occurs at $t = 3.06\ s$. The analysis was conducted considering fault current and voltage measurements captured with a sampling frequency of 20 kHz at one terminal of the SC (as shown in Figure 3.1). Furthermore, it should be noted that during the fault, the SG and the ICG unit have been assumed to be connected. This assumption is made to investigate the natural response of the fault current contributed by both sources and its impact on the quenching of the SC.

Table 3.2: Representative scenarios for AC SC.

Scenario	**Fault type**	**Location**	**Fault resistance**
Solid internal fault ($F_{1_{AC}}$)	LL-G	40 % of SC's length	0 Ω
Resistive internal fault ($F_{2_{AC}}$)	LL-G	40 % of SC's length	50 Ω
Solid external fault ($F_{3_{AC}}$)	LL-G	at 30 % of adjacent line	0 Ω
Load switch (LS)	-	Bus 2	-

Scenario $\mathbf{F_{1_{AC}}}$

Figure 3.2 presents the performance of the AC SC during an LL-G solid fault, occurring at 40% of the AC SC's length and triggered at $t = 3.06\,s$.

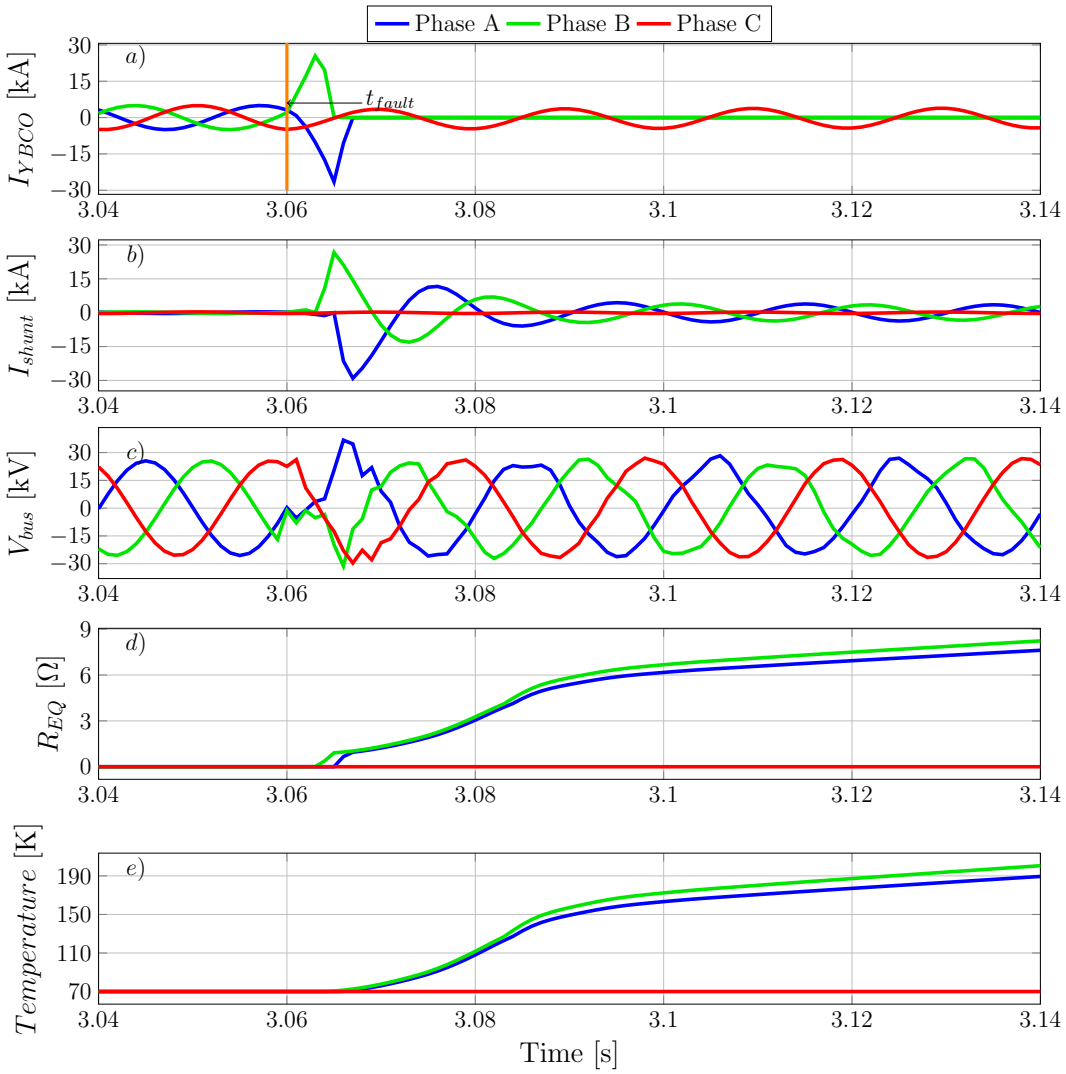

Figure 3.2: AC SC performance under a LL-G solid fault at 40% of the AC SC's length: a) Currents through YBCO layer b) Currents through copper stabiliser layers and former, c) Equivalent resistance, d) Temperature.

During pre-fault conditions, the AC SC operates at $T = 70\ K$ and the resistance of the YBCO layer is approximately zero, providing a current path with approximately zero losses. Figure 3.2a shows the current flowing through the YBCO layer of each phase. When the value of fault current flowing through phase A and phase B (which are the faulted phases) reaches the value of I_C, quenching of the HTS tapes is initiated, leading to an increase in the resistance of the YBCO layers and consequently in T of the AC SC [67]. Under these conditions, the fault current is re-distributed through the copper

stabiliser layers and the former (current indicated as I_{shunt} in Figure 3.2b) at $t = 3.064\ s$. The fault current diversion results in an increase in the resistivity of the copper stabiliser layers and the former based on (2.5) and (2.6), respectively, and a further increase in T of the AC SC. Figure 3.2d shows the change in equivalent resistance of the AC SC (which reaches values over 8 Ω), while Figure 3.2e demonstrates the resulting rise in T of the AC SC. When T exceeds $T_C = 92\ K$, the HTS tapes enter the highly-resistive state and a dramatic increase in R_{eq} can be observed in Figure 3.2d. Figure 3.2c demonstrates the three phase voltage signatures. Once the fault occurs at $t = 3.06\ s$, the voltage of phase A and phase B present a rapid reduction towards 0 kV. However, within the first fault cycle, phase voltages increase, by initially presenting high peaks followed by a gradual recovery to approximately their pre-fault magnitudes. The behavior of the fault voltage signatures is primarily influenced by two factors, the increase in R_{eq} inserted by the SC (where a higher equivalent resistance results in the presence of higher voltage peaks) and also the presence of the AVR of the SG which remains connected to the grid during the fault.

Therefore, it is evident that the presence of a solid internal fault initiates the quenching of AC SC and during the transition from superconducting state to highly-resistive state, the AC SC experiences a dynamic change of R_{eq} which affects the resulting fault current waveforms (and consequently the fault levels of the system) and the voltage signatures during the fault.

Scenario $\mathbf{F_{2_{AC}}}$

For the design of sensitive and effective protection and accurate fault location schemes, it is essential to consider resistive faults, which are anticipated to affect the resulting voltage and current waveforms. Figure 3.3 provides a deeper insight of the effect of R_f on the quenching process by presenting the fault current measurements under the influence of an LL-G fault with $R_f = 50\ \Omega$, occurring at 40% of the AC SC's length.

As depicted in Figure 3.3a and Figure 3.3b, during a resistive fault, the AC SC does not quench as the fault current flowing through YBCO layers does not reach the value of I_C. The YBCO layer remains in superconducting state and therefore there is no current sharing among the copper stabiliser layers and the former. Subsequently, R_{eq} of the AC SC is approximately zero (Figure 3.3d) and T is sustained at the operating temperature (i.e., $T_0 = 70\ K$) (Figure 3.3e). Furthermore, Figure 3.3c shows that no voltage drop is reported during the fault.

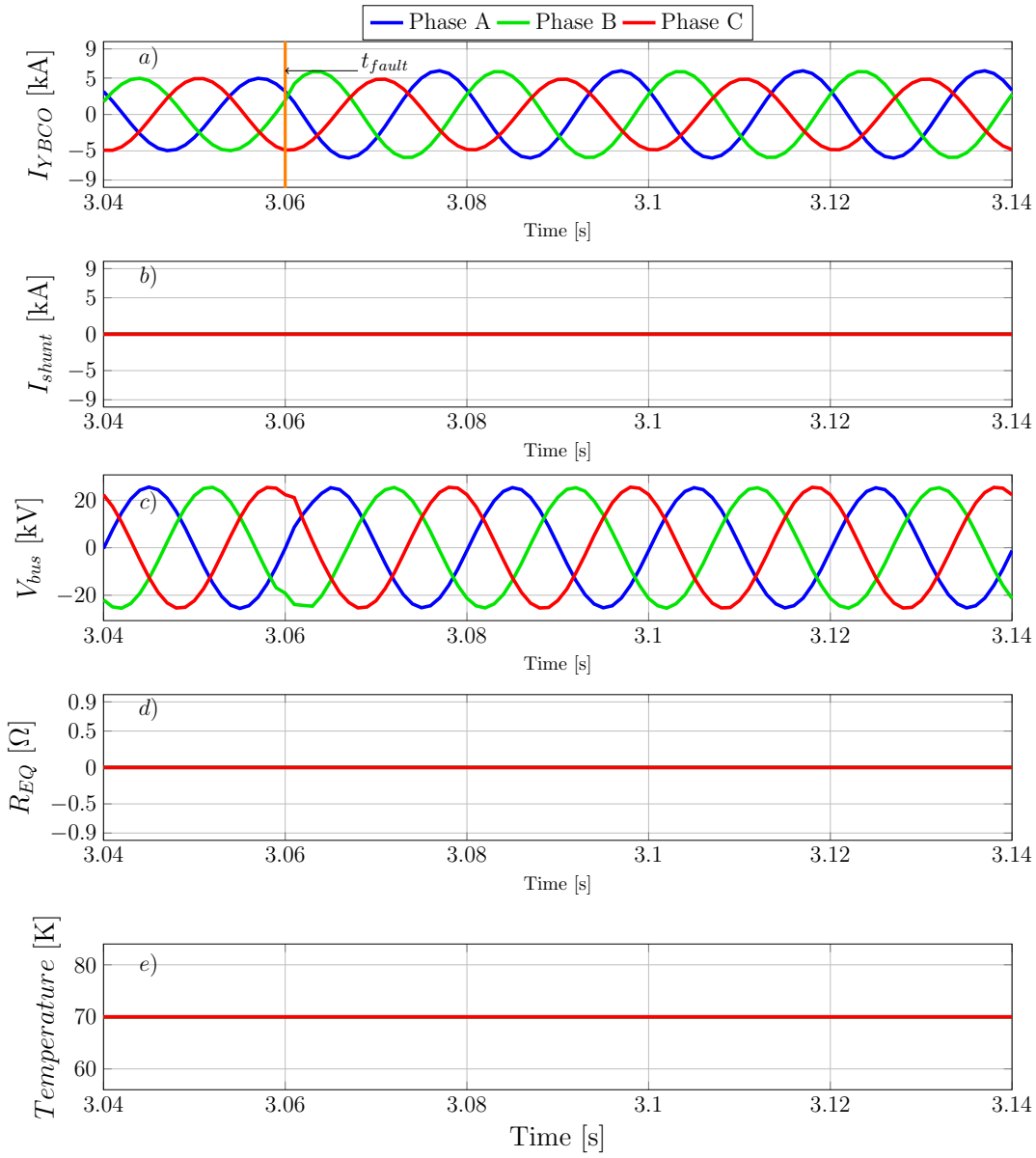

Figure 3.3: AC SC performance under a LL-G fault with $R_f = 50\Omega$ at 40% of the AC SC's length: a) Currents through YBCO layer, b) Currents through copper stabiliser layers and former, c) Equivalent resistance, d) Temperature.

Therefore, the presence of R_f reduces the prospective fault current, even below I_C, preventing the AC SC from quenching. Thus, high values of R_f affect the quenching process and make the detection and localisation of resistive faults challenging.

Scenario $\mathbf{F_{3_{AC}}}$

Figure 3.4 depicts the fault response of the AC SC during an LL-G external solid fault applied on the adjacent 132 kV line. As seen in Figure 3.4a, once the external fault is triggered at $t = 3.06$ s, the current flowing through the YBCO layers present a peak of 21 kA for phase A and 23 kA for phase B, while 4 ms after the fault occurrence the

fault current has been diverted to the copper stabiliser layers and former (Figure 3.4b). During quenching, R_{eq} of phase A reaches a value of 8 Ω, while R_{eq} of phase B is 6 Ω (Figure 3.4d). Correspondingly, due to the Joule heat generation, T of phase A increases to 91 K and of phase B to 85 K (Figure 3.4e). The voltage of phase A and phase B are reduced for a few ms, but once R_{eq} starts to increase, the fault current decreases and voltages present peak values (Figure 3.4c).

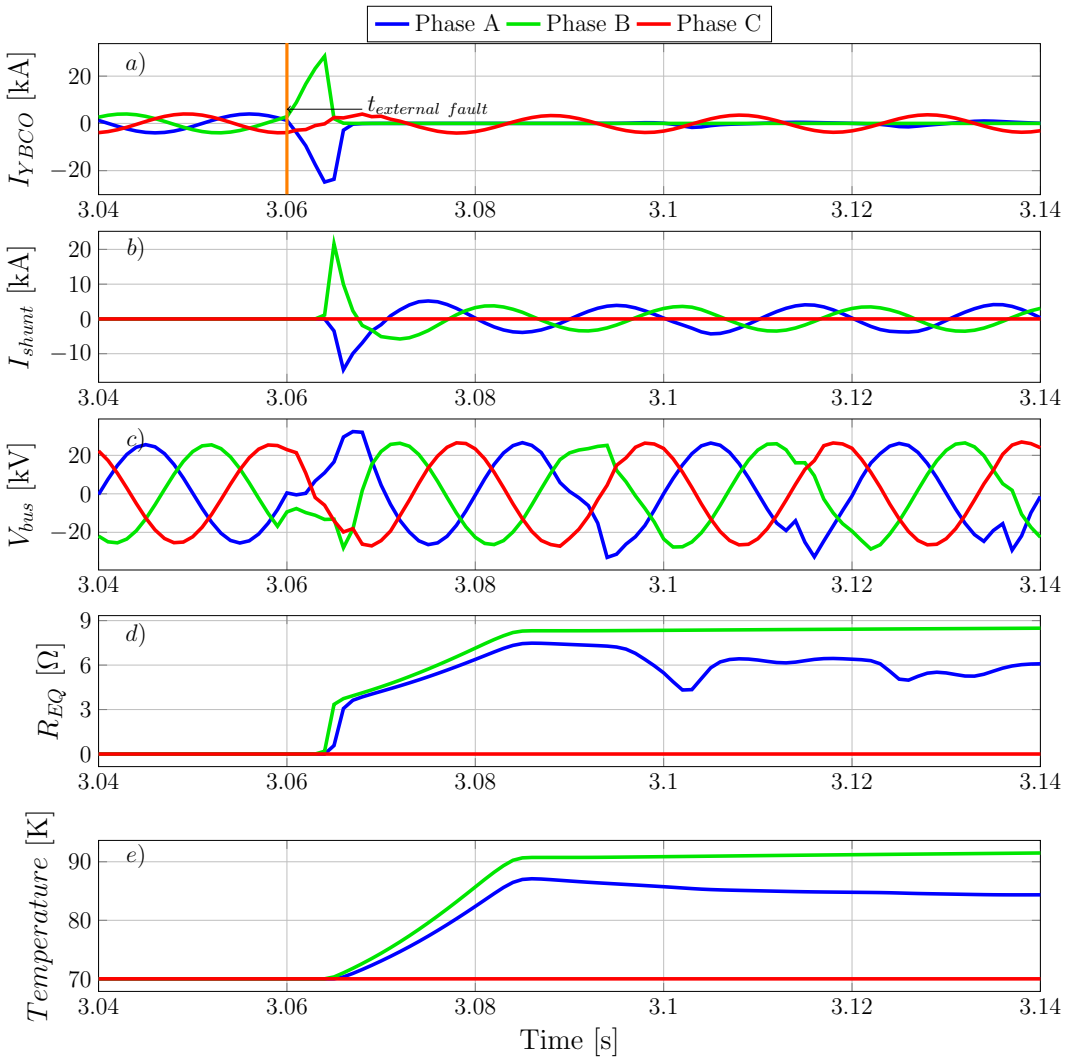

Figure 3.4: AC SC performance under an external LL-G solid fault on the 132 kV adjacent line: a) Currents through YBCO, b) Currents through copper stabilizer layers and former, c) Equivalent resistance, d) Temperature.

The results of the presented analysis demonstrate that the quenching of AC SCs can be caused by external faults, introducing many challenges to fault management of such cables, accounting for protection stability and selectivity and fault location accuracy.

Scenario LS

Figure 3.5a shows the results of a load switching event. Once the load is connected at Bus 2, the AC SC starts to quench when the current flowing through the YBCO layers exceeds I_C of the HTS tapes. At $t = 3.076\ s$, as is depicted in Figure 3.5b, the current is diverted to the copper stabiliser layers and the former. T of the AC SC then reaches values higher than T_C, as is shown in Figure 3.5d, and consequently the HTS tapes enter the highly-resistive state.

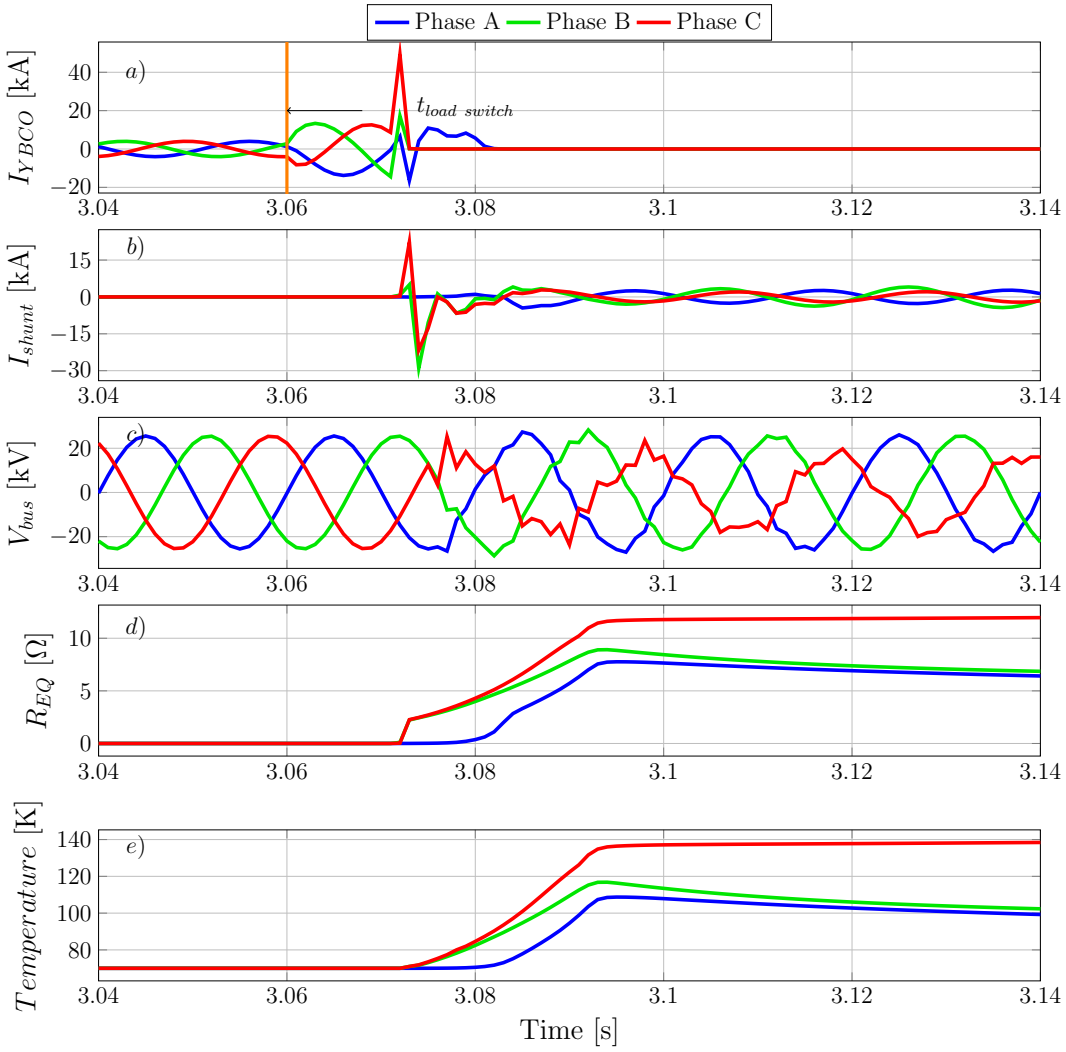

Figure 3.5: AC SC performance under a load switching event : a) Currents through YBCO layer, b) Currents through copper stabiliser layers and former, c) Equivalent resistance, d) Temperature.

Similar to external faults, the presence of a load switching event can initiate the quenching of AC SCs, affecting the protection stability, discrimination and security.

3.1.3 Discussion of AC SC fault analysis assessment

From the acquired results, the following observations can be derived for the fault management of AC SCs:

- During the quenching process, AC SCs present a dynamic change in R_{eq}, leading to a dynamic change in system total impedance and a suppression in the fault current levels. These new variables introduced by the deployment of AC SCs have an impact on the resulting fault current and voltage waveforms and consequently cause an adverse effect on the existing well-established protection and fault location schemes. For instance, the sensitivity of over-current protection schemes, which is based on the fault current magnitudes, or the accuracy of impedance-based fault location schemes, which require fault current and voltage measurements, shall be jeopardised during quenching, threatening system safety and resiliency. Furthermore, the introduction of high equivalent resistance leads to voltage spikes across SCs, raising new challenges for voltage-assisted protection schemes. The limitations of existing protection and fault location schemes will be discussed in the following chapters.

- During highly-resistive faults, AC SCs do not quench, affecting the sensitivity of protection schemes and accuracy of fault location schemes.

- The presence of other disturbances, such as load switching events and external faults, cause the quenching of AC SCs, endangering the protection stability, selectivity and security. The quenching of an AC SC during these conditions creates the risk of the false indication of an internal fault occurrence and subsequently can lead to protection nuisance tripping. Furthermore, the initiation of quenching during external faults and other disturbances in conjunction with the absence of quenching during highly-resistive internal faults causes challenges for the establishment of discriminative protection schemes and accurate fault location schemes.

Thus, the performance of SCs during transient conditions is a multi-variable complex problem. The obtained observations will be utilised as key drivers in the following chapters in order to discuss the limitations of existing protection and fault location schemes for the fault management of AC SCs and propose novel solutions which consider the particularities of such technology.

3.2 Power System Modelling and Fault Characterisation of DC SCs

Driven by the necessity for zero-carbon power generation, approximately more than 300 GW of offshore wind power is anticipated to be integrated in Europe by 2050 [84]. Following these generation reforms, the incorporation of HVDC transmission systems with DC SCs can help unlock numerous opportunities for the realisation of this target. Multi-terminal HVDC systems, as a natural extension of the existing point-to-point HVDC grids, satisfy all the requirements for enabling the target of energy connectivity without borders. Furthermore, the deployment of Modular Multilevel Converters (MMCs), compared to other converter topologies, unlocks advantageous functionalities for high-power applications, accounting for improvements in fault blocking capability, elimination of DC-link capacitor, and reduced semiconductor losses, which are analysed in more detail in [85–87]. In this section a detailed fault current characterisation of DC SCs is presented for a multi-terminal HVDC system with MMCs.

3.2.1 Multi-terminal HVDC power system model

Figure 3.6 presents the overall topology of the three-terminal HVDC grid model developed in Matlab/Simulink. The topology of the system is based on the concept proposed in [40] and considers the power transmission from a 66 kV AC offshore WF to a 400 kV onshore AC grid, through DC SCs. The system is constructed by adopting the symmetric monopole configuration and consists of i) three MMCs operating at ± 200 kV DC voltage, which represent the onshore and offshore valve stations, ii) current-limiting inductors connected at each cable end and iii) CBs which have been modelled by adopting a hybrid concept by ABB as reported in [88] (2 ms operation time with a maximum breaking current of 9 kA). The methodology for inductor design will be analysed in subsection 3.2.2 as it is a key factor for the fault characterisation of SCs and the subsequent designing of protection schemes.

The models of the MMCs are based on the detailed equivalent model of 401-level Half Bridge (HB) MMCs, which have been developed according to guidelines presented in [85]. Each MMC is composed of six arms with each arm containing series-connected Half-Bridge Submodules (HBSMs) along with an arm inductor. Each HBSM consists of two Insulated-Gate Bipolar Transistors (IGBTs) with anti-parallel diodes and one

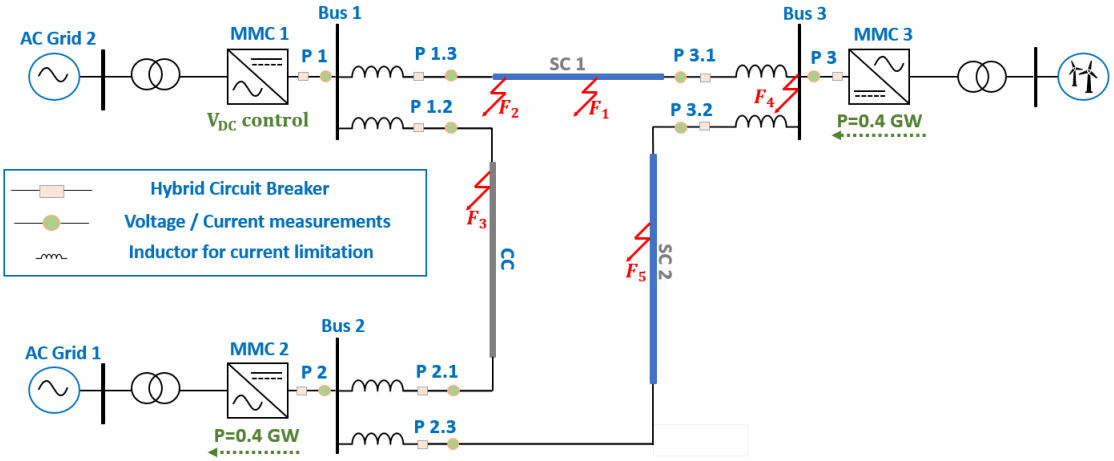

Figure 3.6: HVDC network model incorporating SCs and CC.

DC capacitor. In the presented work, the number of HBSMs of each arm has been selected equal to 400 in order to achieve a high number of voltage steps (the DC voltage is formed in discrete levels according to the number of MMC levels) and consequently provide high-quality sinusoidal output signals with reduced harmonic content. In the developed system depicted in Figure 3.6, MMC3 operates in grid-forming control mode for the integration of the power delivered by the WF. MMC1 is utilised for the DC voltage control of the HVDC network, while MMC2 controls the active P and reactive Q power exchange with the onshore AC grid 1. Specifically, 0.4 GW of offshore power is transmitted to onshore AC grid 1. For the modelling of the WF, an aggregated model with fully-rated inverter-based turbines has been utilised, preserving the accuracy of the simulation results [84]. Two bipolar DC SCs have been integrated within the system to connect Bus 3 with Bus 1 and Bus 2, respectively. The length of SC1 and SC2 is 100 km and 120 km, respectively, and they are utilised for the bulk offshore power transmission with approximately zero losses. For the fabrication of such long DC SCs, joints are utilised to connect HTS tapes and provide electrical continuity [84, 89, 90]. It is worthy of note that the detailed modelling of SC joints is beyond the scope of the presented work.

Bus 1 and Bus 2 are connected through a DC conventional cable (CC) developed according to the distributed parameters model. All cable sheaths are solidly bonded. The inclusion of the CC has been incorporated into the system for simplification purposes, aiming to achieve a more stable steady-state operation, especially in light of the MMCs' tuning and system configuration. The prospect of replacing a third SC with the CC could be considered as part of future research efforts.

The specifications of the AC and DC systems are demonstrated in Table 3.3. As it can be observed the rated current of CC and SC1 is 2 kA, while for SC2 is 2.2 kA. SC1 and CC have the same rated current, however, SCs are more efficient, compared to CC, as they have different geometric characteristics (i.e., smaller cross-section for the same voltage level) and present approximately zero losses due to the zero-equivalent resistance.

Table 3.3: System specifications

Parameter	**Symbol**	**Value**
AC onshore voltage	V_{ACON}	400 kV
AC offshore voltage	V_{ACOF}	66 kV
Rated current of CC and SC1	I_{rated}	2 kA
Rated current of SC2	I_{rated}	2.2 kA
DC voltage	V_{DC}	200 kV
DC inductor for SC1	L_{DC}	140 mH
DC inductor for SC2	L_{DC}	145 mH
MMC arm inductor	L_{arm}	0.1 $p.u.$
Cells per arm	C_{SM}	400
Conventional cable resistance	R_{Cable}	0.0146 Ω/km
Conventional cable inductance	L_{Cable}	0.158 mH/km
Conventional cable capacitance	C_{Cable}	0.275 $\mu F/km$

Similarly, to AC systems, prior to the development of the proposed schemes in HVDC grids, particular attention and specific case studies should be devoted to the characterisation of SCs' behaviour during transient conditions to acquire key insights and consequently ensure the power system safety and reliability. The conducted studies aim to acquire a deeper understanding of DC SCs response and their quenching during faults applied: ii) along their length, ii) at the adjacent CC and SC and iii) at buses, and consequently quantify the challenges from a fault management perspective. For this purpose a series of different fault scenarios have been investigated by conducting EMT simulation studies and utilising the system depicted in Figure 3.6. The fault scenarios include Pole-to-Pole (PP), positive Pole-to-Ground (PG) and negative Pole-to-Ground (NG) faults (incorporating various fault positions along the SCs and CC, and different values of fault resistance).

3.2.2 Design of DC inductance

As it is observed in Figure 3.6, SC1 , SC2 and CC are terminated with external inductances, L_{DC}, which are implemented to reduce the rate of change (rise) of DC fault current. The sizing of DC series inductances constitute a trade-off between the steady-state performance and the transient response of the superconducting-based HVDC link [91].

More specifically, as discussed in Chapter 2, the quenching of SCs is dependent on the

fault current (when the value of fault current exceeds I_C, the SC quenches). Therefore, a reduction in the rate of rise of DC fault current has an impact on the time initiation of the quenching process, making the fault detection on SCs more challenging and affecting the protection operational speed. In particular, if DC SCs do not quench quickly under the faulted conditions, the fault may develop and propagate, having catastrophic consequences for the whole system. On that front, the modelling of L_{DC} at the terminals of each SC has been established considering: i) their steady state performance (considering the tuning of MMCs), ii) the time required for the quenching initiation after the occurrence of an internal fault along the SC's length and iii) CB maximum breaking current.

Considering a solid PG fault at 95 % of SC1's length (50 km from Bus 3) (Figure 3.6) and different values of L_{DC}, the corresponding initiation time of quenching, t_{quen}, after the fault occurrence is reported in Table 3.4. It shall be noted that PP faults are the most severe due to the fact that they force the system to collapse and lead to DC SC quenching immediately after their occurrence. Therefore, for the design of L_{DC}, the presented work considered the t_{quen} derived during PG and NG faults. Furthermore, the sizing of L_{DC} has been investigated in accordance with the quenching triggered by solid faults because, as will be discussed in the following subsections, the presence of R_f jeopardises the quenching process.

Table 3.4: Time of quenching initiation with respect to the DC inductor value.

Inductance $[mH]$	130	140	150	160	170	180	190	200
Time of quenching initiation t_{quen} $[ms]$	0.05	0.08	0.68	0.98	1.18	1.29	1.87	1.96

As demonstrated in Table 3.4, an increase in the value of L_{DC} causes a delay in the quenching initiation. The minimum t_{quen} corresponds to L_{DC} of 130 mH. It should be noted that for the presented studies the inductors have been considered ideal and thus their resistance have been neglected. However, the simulation-based analysis showed that for $L_{DC} = 130$ mH the HVDC system is unstable during the steady state (considering the tuning of MMCs). Therefore, the selected value which provides a trade-off between the steady state performance and the transient response of SC1 is 140 mH. A similar analysis has been conducted for SC2 and the resulting L_{DC} value has been found equal to 145 mH.

Furthermore, the selection of L_{DC} for both SCs has been evaluated in accordance with the CBs' maximum breaking current. On that front, for CBs, the widely-used ABB-type proposed in [92] has been considered (9 kA maximum breaking current for

operation time of 2 ms). Figure 3.7 shows the resulting DC current flowing through SC1 and SC2 for the selected inductance values. The DC current traces have been generated for SC1 and SC2 during a solid PP fault (which is the most severe fault) at 30 % of each SC's length (30 km from Bus 3), respectively. The fault in both cases has been generated at $t = 0$ ms with 5 ms post-fault data.

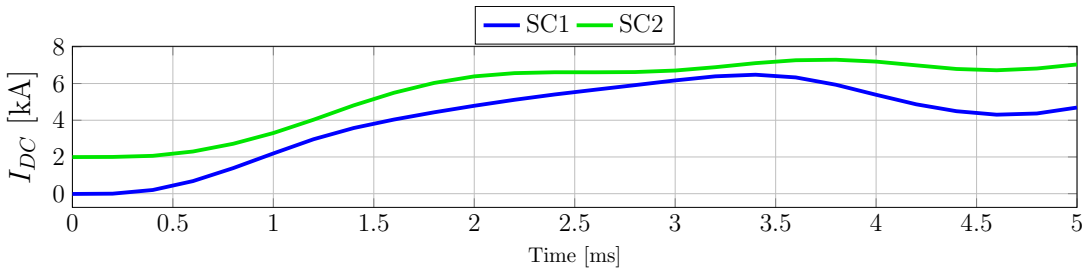

Figure 3.7: Fault DC current for the selected inductance values during a solid PP fault at 30 % of SC1's and SC2's length.

As can be seen in Figure 3.7, for both fault scenarios, the resulting DC fault current remains below the 9 kA threshold for the first 5 ms. Specifically, a solid PP fault at 30 % of SC1's length leads to maximum DC fault current at approximately 6.5 kA and as the R_{eq} of SC1 increases, the fault current is reduced and sustained at 4 kA. Respectively, for a PP fault at 30 % of SC2's length, the maximum DC fault current is 7.4 kA and due to the further surge of R_{eq}, the fault current is limited to 6.5 kA.

Therefore, the selected inductance value for both SCs leads to an appropriate steady state performance and does not add a delay to the quenching process. The fast initiation of the quenching phenomenon, after the fault occurrence, results in the reduction of the peak fault current levels and subsequently mitigates the stress across the CBs.

Finally, for the calculation of L_{DC} at the terminals of CC, the methodology proposed in [85] for the sizing of DC inductors in meshed HVDC systems has been adopted and the final value has been calculated equal to 133 mH.

3.3 Fault Characterisation of DC SCs

In this subsection, four representative fault scenarios will be analysed in order to extract useful features from the fault response of DC SCs. The selected scenarios aim to analyse the performance of SCs during the quenching phenomenon, the impact of R_f on the quenching phenomenon, and the effect of faults applied to CC and buses. Table 3.5 summarises the presented fault scenarios which include a PP solid fault applied at SC1

($F_{1_{DC}}$), a highly-resistive fault applied at the remote end of SC1 ($F_{2_{DC}}$), a PP solid fault at CC ($F_{3_{DC}}$), and a solid fault occurring at Bus 3 ($F_{4_{DC}}$). During all scenarios, the faults have been applied at $t = 5\ ms$ and are permanent. During the simulation studies, pre-fault (5 ms time window) and post-fault (20 ms time window) of current and voltage waveforms were measured at one terminal of the cables, the DC side of the converter and the corresponding bus. Specifically, of the system under test depicted in Figure 3.6, current measurements are obtained from SCs terminals P 3.1 and P 3.2, from point P.3 at the DC side of MMC3 and for CC at terminal P 1.2. Voltage measurements are obtained at Bus 3 from point P.3, Bus 2 from point P 2 and Bus 1 from point P.1. The generated signals have been captured with a sampling frequency of 20 kHz [40] and CB operations have been suspended in order to capture the natural response of the faults. Specifically, the resulting current and voltage waveforms represent the system natural response to faults and have been utilised to assess the order of magnitude. Furthermore, to emulate realistically the performance of MMCs during the transient conditions (i.e., faults), the fault blocking capability of the HBSMs has been considered. During the DC faults, when the fault current flowing through an MMC exceeds 1.2 $p.u.$ of its nominal current, the IGBTs are blocked for self-protection purposes [93]. During these conditions, the fault current flows through the anti-parallel diodes and the MMC operates as an uncontrolled rectifier.

Table 3.5: Representative fault scenarios

Scenario	Fault type	Fault location	Fault resistance
$F_{1_{DC}}$	PP	20 % of SC1's length (internal)	0 Ω
$F_{2_{DC}}$	PP	99 % of SC1's length (internal)	300 Ω
$F_{3_{DC}}$	PP	0.1 % of CC's length (external)	0 Ω
$F_{4_{DC}}$	PP	Bus 3 (external)	0 Ω

Scenario $\mathbf{F_{1_{DC}}}$

Figure 3.8 demonstrates the response of SC1, SC2, CC and the MMCs under the influence of a solid PP fault applied at 20 % of SC1's length (20 km from Bus 3). Figure 3.8a shows the DC currents flowing through SC1, SC2 and CC. During steady state conditions, the current flowing through SC2 is approximately 2 kA, while the current flowing through SC1 and CC is approximately 0 A. These simulation results show that during normal operation the offshore wind power (0.4 GW) is transmitted to onshore AC grid 1 (depicted in Figure 3.6) through SC2. It should be noted that due to the structure of HVDC grid and the current limiting inductors the power flow of the SC has a definite solution (it

should be noted that no power flow controllers have been considered in the presented studies).

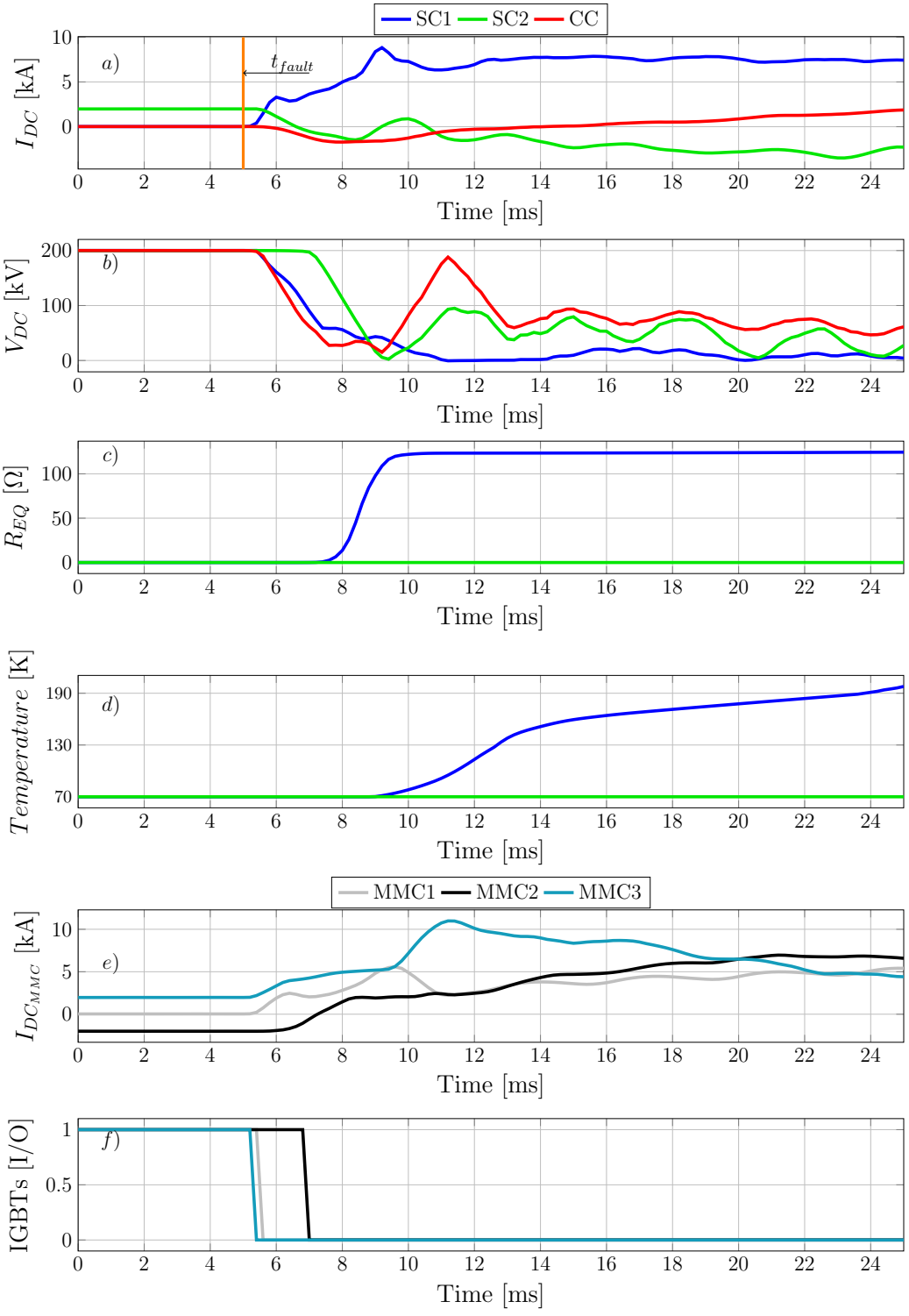

Figure 3.8: PP solid fault at 20 % of SC1's length: a) SC1, SC2 and CC DC currents, b) SC1, SC2 and CC DC pole-to-pole voltage, c) equivalent resistance of SC1 and SC2, d) temperature of SC1 and SC2 e) MMCs DC currents.

The fault occurs at $t = 5\ ms$, and then after 0.15 ms of the fault occurrence, SC1, which is the faulted line, starts to quench and the peak of the fault current is 8.96 kA. During the quenching process, R_{eq} of SC1 increases, (i.e., refer to Figure 3.8c), and the maximum value reached is approximately 120 Ω. The rapid increase in R_{eq} leads to the generation of Joule heat and consequently causes an abrupt increase in T of SC1, as observed in Figure 3.8d. SC1 operates in the highly-resistive state, causing a reduction in DC fault current which is sustained to approximately 7 kA. Specifically, at $t = 9\ ms$ the fault current reaches it peak, which is lower compared to the prospective fault current due to the increase in the equivalent resistance. After $t = 9\ ms$the fault current reach to a steady-state value. The pole-to-pole voltage of SC1, measured at Bus 3, is depicted in Figure 3.8b, and is depressed, however there is residual voltage during quenching due to the increase in the resistance of SC1.

The current infeed from SC2 and CC are demonstrated in Figure 3.8a and the rate of current rise is limited due to the inductive terminations. It should be noted that the solid fault applied on SC1 does not cause the quenching of SC2 and consequently T and R_{eq} of SC2 are sustained to 70 K (Figure 3.8d) and 0 Ω (Figure 3.8c), respectively.

Figure 3.8e presents the response of the MMCs during the fault. Initially, there is a rapid increase in the current from the MMCs due to the discharge of the submodule capacitor. However, once the current exceeds 1.2 $p.u.$ of the MMC rated current, the IGBTs are turned-off and the MMCs are blocked for self-protection. In particular, the binary signal which indicates the blocking of MMCs is depicted in Figure 3.8f. MMC1 and MMC3, which are directly connected to the faulted SC1, are blocked at 0.28 ms and 0.48 ms after the fault occurrence, respectively, while MMC2, which is the neighboring converter, is blocked 1.88 ms after the fault. Once the MMCs are blocked, they start to operate as uncontrollable rectifiers and the current depicted in Figure 3.8e corresponds to the fault current fed from the AC side. The fault current contribution of MMC3, which is the closest to the fault, is influenced by several factors, including the fault level behind MMC3, the blocking capability of MMC3, the termination inductors, and the equivalent resistance introduced by the SC.

Considering the results from this scenario, it is observed that the natural response of DC fault current is limited due to the increase in resistance of SCs which results in suppressed fault current magnitudes and residual voltages.

Scenario $\mathbf{F_{2_{DC}}}$

Figure 3.9 presents the transient performance of SC1, SC2, CC and the MMCs during a highly-resistive ($R_f = 300\ \Omega$) PP fault applied at 99 % of SC1's length (99 km from Bus 3). Figure 3.9a shows the DC fault currents of SC1, SC2 and CC. As is observed, SC1 does not quench during this fault scenario as the fault current flowing through the HTS tapes is predominantly limited by R_f and therefore does not exceed the value of I_C. More specifically, the peak current of SC1 is approximately 250 A, the voltage, measured at Bus 3, is slightly reduced to 198 kV (Figure 3.9b) and as observed in Figure 3.9c and Figure 3.9d, SC1 operates at superconducting state with $R_{eq} = 0\ \Omega$ and $T = 70\ K$.

Furthermore, SC2 maintains its superconducting properties during the fault period, operating as a zero resistance path (Figure 3.9c) at 70 K (Figure 3.9d). The voltage of CC, measured at Bus 1, presents a slight reduction to 197 kV, 2 ms after the fault occurrence (Figure 3.9b). This voltage dip can be explained by the fact that the fault is applied close to CC's connection point (1 km from Bus 1). Moreover, as demonstrated in Figure 3.9e and Figure 3.9f, the fault current did not trigger the MMCs' blocking. Thus the converters continue to operate with approximately constant DC current and the DC voltage is maintained by MMC1. As R_f increases, the IGBTs do not turn off, as the maximum permissible operating current (and hence equivalent thermal stress) has not been reached.

This scenario provides a deeper insight on the influence of R_f on the quenching process. In particular, during highly-resistive faults, the fault current is predominantly reduced by R_f, preventing the quenching of SCs.

Scenarios $\mathbf{F_{3_{DC}}}$ and $\mathbf{F_{4_{DC}}}$

The performance of SC1, SC2, CC and the MMCs has also been investigated against a PP external solid fault applied at 0.1 % of CC's length (0.06 km from Bus 1). During the fault period, the peak current flowing through SC1 is 5 kA (Figure 3.10a), the voltage of SC1, measured at Bus 3, is reduced to 50 kV (Figure 3.10b), R_{eq} reaches a value of 130 Ω (Figure 3.10c) and T rises up to 190 K (Figure 3.10d). Therefore, it is evident that the occurrence of a solid fault on CC leads to the quenching of SC1. As is depicted in Figure 3.10a, the fault current flowing through SC1 starts to reduce once R_{eq} starts to increase abruptly. The value of R_{eq} and T are retained to 130 Ω and 190 K, respectively. This can be explained considering the time required for SC1 to recover and its T to be reduced below T_C. The higher the peak value of T during the fault, the slower the

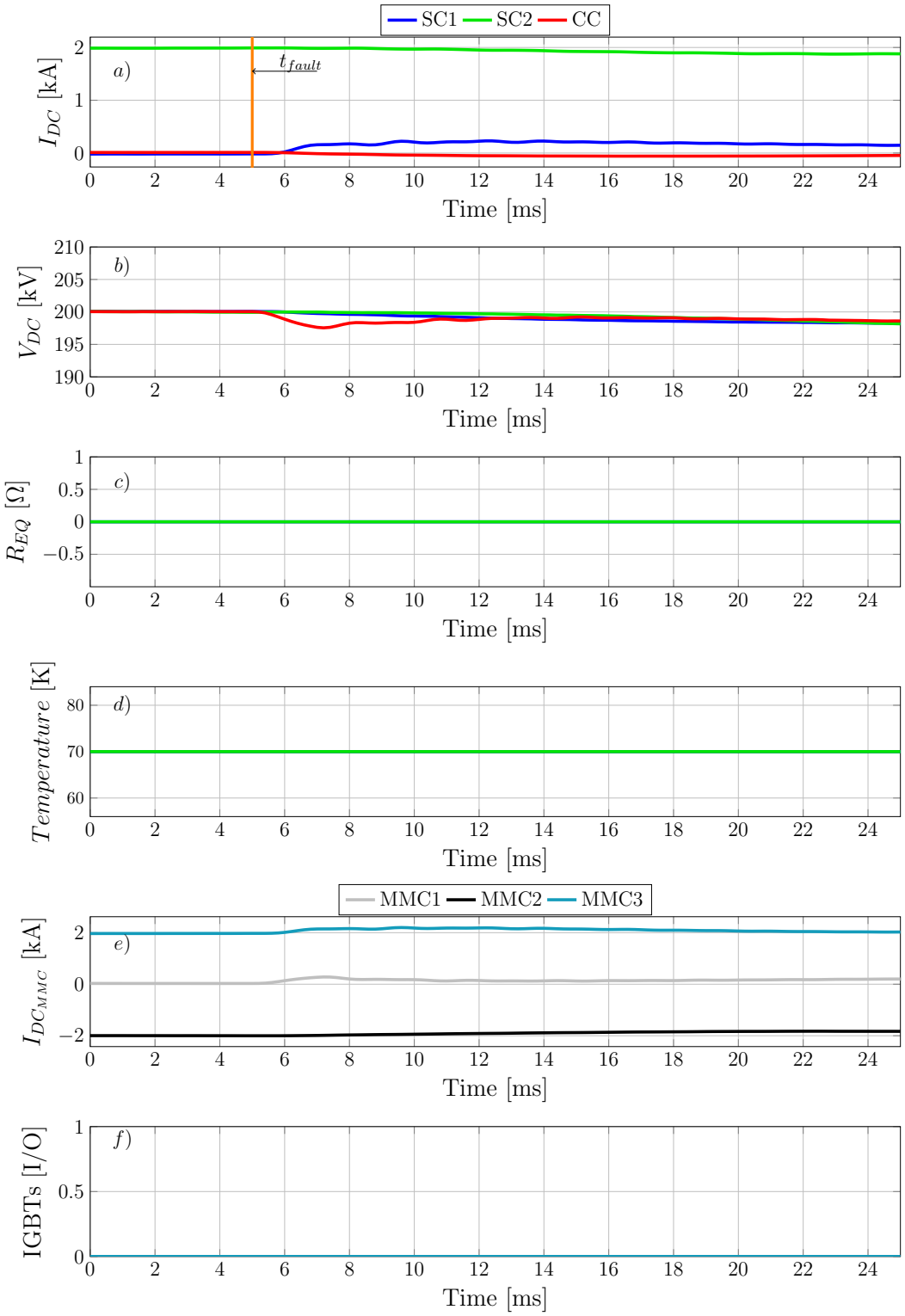

Figure 3.9: Highly-resistive PP fault at 99 % of SC1's length with $R_f = 300\Omega$: a) SC1, SC2 and CC DC currents, b) SC1, SC2 and CC DC pole-to-pole voltage, c) equivalent resistance of SC1 and SC2, d) temperature of SC1 and SC2 e) MMCs DC currents.

recovery process (within the range of a few *sec* to a few *min*) [94]. The recovery time of SCs is determined by the fault parameters, the structure of the SC, and the type and

efficiency of the cooling system [9].

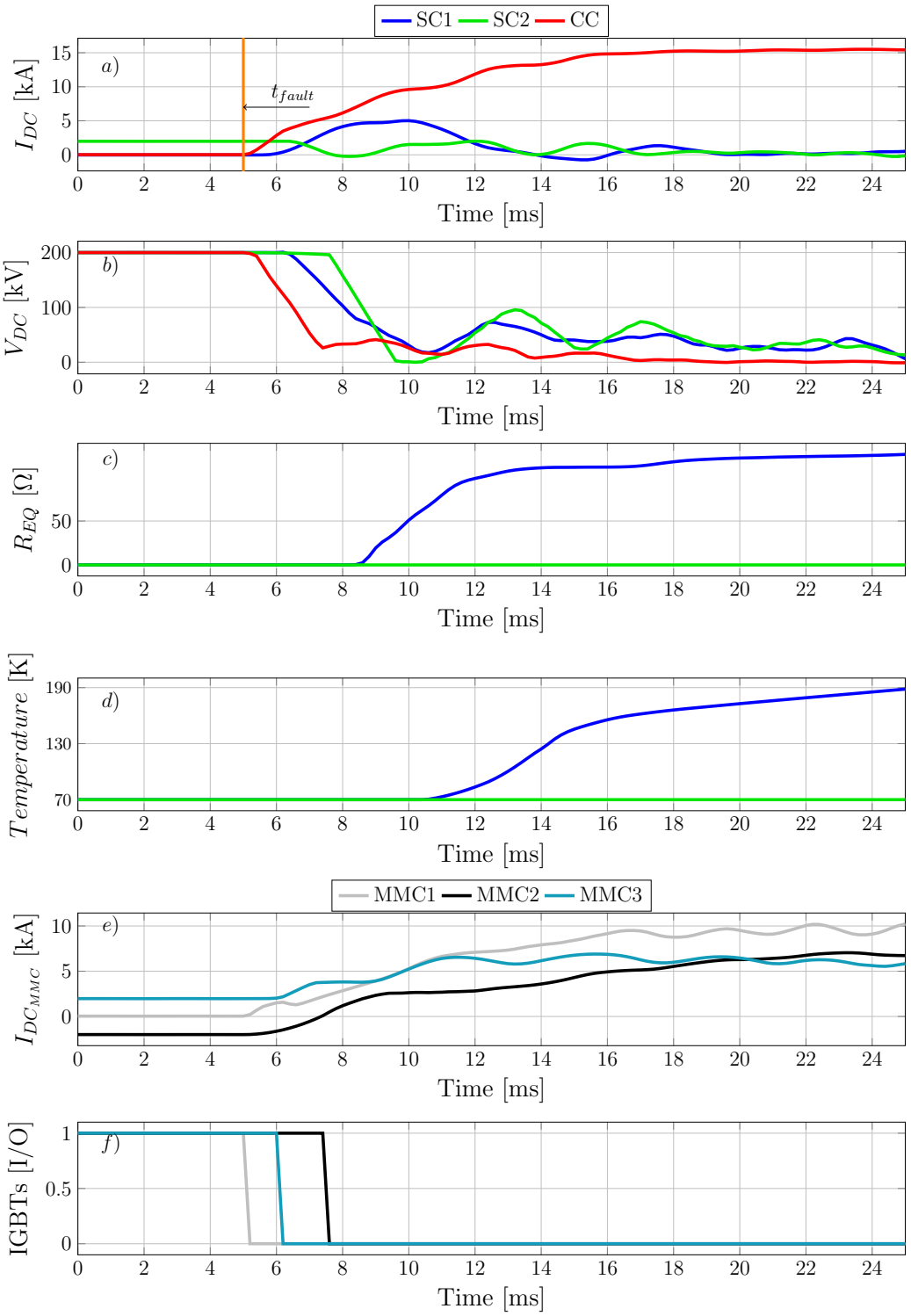

Figure 3.10: Solid PP fault at 0.1 % of CC's length: a) SC1, SC2 and CC DC currents, b) SC1, SC2 and CC DC pole-to-pole voltage, c) equivalent resistance of SC1 and SC2, d) temperature of SC1 and SC2 e) MMCs DC currents.

Furthermore, the presence of a solid PP fault applied on CC does not lead to the

quenching of SC2 and thus the T and R_{eq} of SC2, remain to 70 K and 0 Ω, respectively. The DC fault current flowing through CC is illustrated in Figure 3.10a, while the voltage dip, measured at Bus 2, is displayed in Figure 3.10b.

Regarding the response of the MMCs, as illustrated in Figure 3.10f, MMC1 is blocked within 0.03 ms, MMC2 within 2.52 ms and MMC3 within 1.1 ms after the fault, respectively. This causes them to start operating as uncontrollable rectifiers, feeding current to the faulted point.

Furthermore, the simulation results of a permanent PP solid fault at Bus 3, $F_{4_{DC}}$, are shown in Figure 3.11.

Figure 3.11a shows the DC currents flowing through the two SCs and CC. It is observed that for a solid fault at Bus 3 both SCs quench. More specifically, SC1 quenches 4 ms after the fault occurrence, presenting R_{eq} of approximately 140 Ω (Figure 3.11c) and a rise of T up to 190 K (Figure 3.11d). The voltage of SC1 (measured at Bus 3) is reduced to 0 kV as it is directly connected to the faulted bus. The DC current flowing through SC1 is sustained to 400 A as the increase in R_{eq} limits the fault current magnitude. The peak DC current flowing through SC2 is 10 kA (Figure 3.11a), while during the quenching, as R_{eq} reaches a value of 120 Ω (Figure 3.11c), the DC current through SC2 is maintained at 5 kA (Figure 3.11a). The DC current through CC presents a peak of 3.4 kA (Figure 3.11a) and the voltage of CC is decreased to 1.2 kV (Figure 3.11b). Figure 3.11e and Figure 3.11f show the response of the MMCs during the fault period. Specifically, the fault applied at Bus 3 causes the instantaneous blocking of MMC3, which is directly connected to the faulted bus, while the IGBTS of MMC1 and MMC2 are turned off 1.12 ms and 1.41 ms after the fault, respectively. It is worth reiterating that the fault current presented in Figure 3.11 corresponds to the natural response of the system during the fault, without considering the operation of CBs or thermal stresses.

By analysing the performance of SCs during $F_{3_{DC}}$ and $F_{4_{DC}}$ scenarios, it can be concluded that the quenching of DC SCs can be initiated by external faults.

3.3.1 Discussion of DC SCs fault analysis assessment

The results obtained during the fault current characterisation of DC SCs in a multi-terminal HVDC system lead to the following key points.

- The quenching of DC SCs results in reduced fault current magnitudes and residual voltages due to the presence of variable R_{eq}. These factors are anticipated to

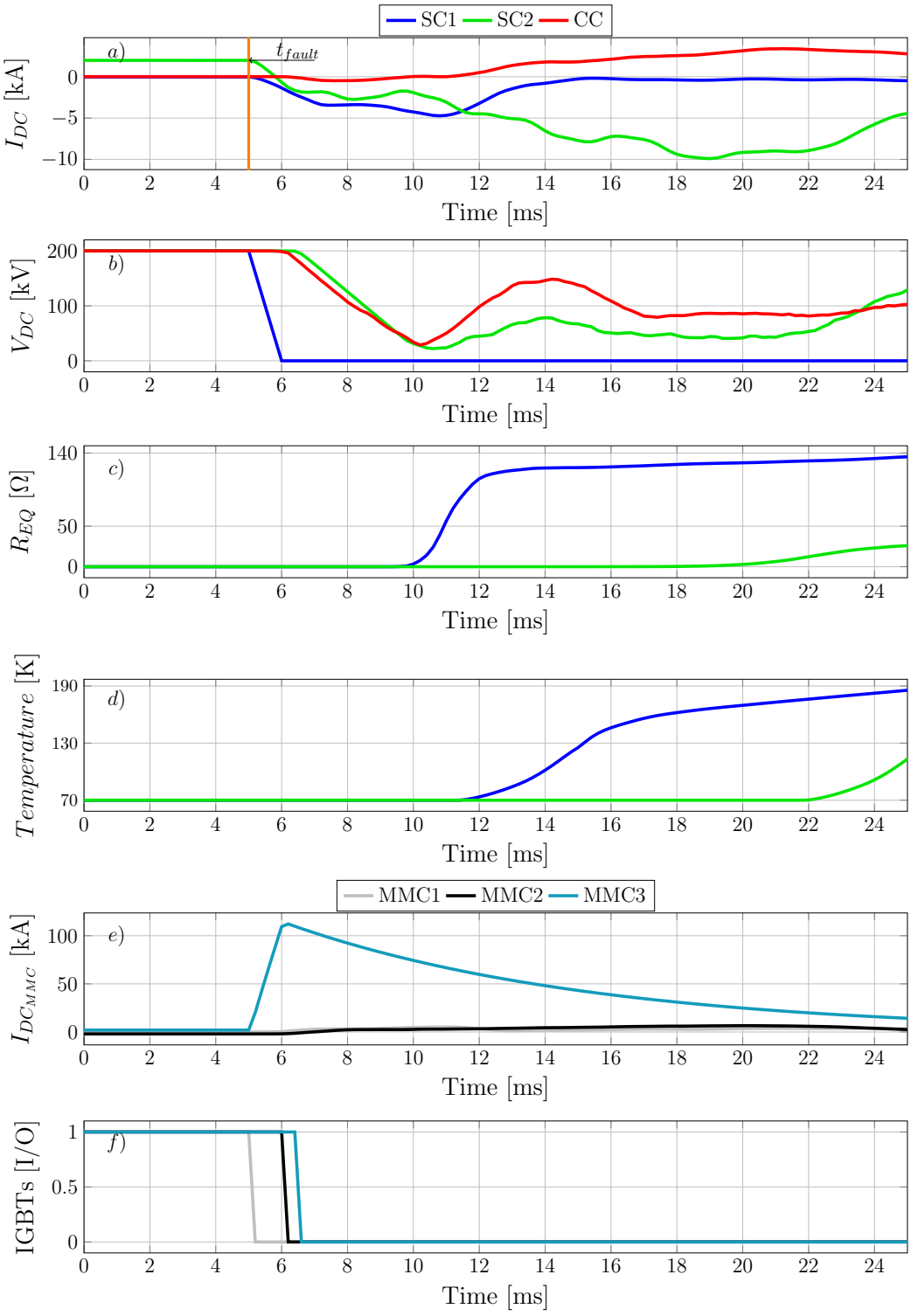

Figure 3.11: Solid PP fault at Bus 3: a) SC1, SC2 and CC DC currents, b) SC1, SC2 and CC DC pole-to-pole voltage, c) equivalent resistance of SC1 and SC2, d) temperature of SC1 and SC2 e) MMCs DC currents.

degrade the robustness of existing protection schemes which employ a logical relationship with limit thresholds (i.e., over-current, over-voltage, under-voltage,

derivative-based) and therefore constitute the key points which should be taken into consideration during the design of more advanced protection solutions.

- The initiation of quenching during external faults and the absence of quenching during highly-resistive internal faults may lead to unsuccessful fault detection and unnecessary system shutdown, respectively. Therefore, to ensure the secure and reliable operation of HVDC grids with SCs, protection schemes with a high degree of sensitivity, selectivity and security are required.

3.4 Summary

This chapter provides the outcomes of a comprehensive, simulation-based fault signatures characterisation of AC and DC SCs. The simulation analysis has been conducted based on i) a series of various faults applied on AC and DC SCs (i.e., faults with varied fault type, fault resistance and fault location) and ii) external faults or other disturbances (i.e., load switching events). The results obtained through the fault assessment analysis of both AC and DC SCs highlighted useful insights for the protection and fault location of such cable technology. Specifically, the simulation results revealed that SC quenching affects the fault current magnitudes and the resulting fault voltage measurements. Therefore, it is anticipated that the impact of variable resistance on fault current and voltage traces will introduce many challenges to existing protection schemes, particularly those based on logical relationships with limit thresholds, and fault location schemes. Furthermore, taking into account the initiation of SC quenching during external faults and other disturbances (i.e., load switching events) along with the impact of the fault resistance during internal resistive faults, the need for discriminative, sensitive and reliable protection schemes and accurate fault location methods is rendered imperative to ensure the secure operation of HVDC systems with SCs.

To perform the fault characterisation of AC and DC SCs, this chapter presents the modelling of a three-phase AC grid and a multi-terminal HVDC system which incorporate ICGs and SCs. More specifically, an AC 132 kV grid was developed in Matlab/Simulink which is comprised of two types of generating units accounting for a SG and ICGs. Regarding the HVDC network topology, a symmetric monopole has been adopted and developed in Matlab/Simulink. The developed HVDC network contains half-bridge MMCs which are considered as the preferred converter topology in recent

HVDC projects, two DC SCs and a CC. For the modelling of the HVDC grid, this chapter outlined and performed an approach for selecting the appropriate value of DC inductors at the terminals of DC SCs and CC. It has been observed that particularly, for the case of DC SCs, a dedicated design methodology is required which considers the fast initiation of quenching (to avoid quenching propagation during the fault), the steady-state performance of SCs (considering the tuning of MMCs) and the CBs current breaking capacity.

Chapter 4

Protection of SCs in AC systems

The protection of AC SCs against electric faults is an emerging research area due to the particularities of this technology. The preliminary work conducted in Chapter 3 focused on the fault characterisation and transient analysis of AC SCs. The concluding remarks indicated that the transition of HTS tapes to the highly-resistive state enforces the appearance of variable resistance which imposes: i) the current re-distribution among the different layers of AC SCs, ii) the dynamic change in the equivalent impedance of the system, iii) the reduction of the fault currents to a certain value and iv) the appearance of residual voltage during faults. All these factors are anticipated to have a negative impact on the well-established protection schemes (i.e., distance and over-current relays) and adversely affect the safety and security of the system. Consequently, the development of reliable protection solutions for AC SCs is one of the major challenges which hinders the full-scale commercialisation of such technology and thus impose an urgent need for novel protection schemes which will be designed to conform with the aforementioned features of SCs.

This chapter presents two novel data-driven protection schemes for the rapid, sensitive and discriminative fault detection and classification in AC grids with SCs. Validation studies incorporating simulation-based analysis and a real-time SIL testing platform are considered to evaluate the sensitivity, stability and operational speed of the developed schemes.

4.1 Assessment of SC Protection Schemes for AC Systems

The integration of AC SCs has unlocked a new research path for the area of power systems protection. In recent years, an increasing number of researchers have started to investigate the fault response of SCs and their impact on existing fault management strategies in order to accelerate the wide scale deployment of such cable technology. However, the number of protection solutions for AC SCs reported in the technical literature is limited.

A coordinated protection scheme based on differential relays, over-current, and directional over-current relays is proposed in [95] for a coaxial AC SC, integrated in a meshed Medium Voltage (MV) AC network. A decision-making algorithm was investigated in [96] to improve the performance of differential and over-current relays. In [97], a real-time protective algorithm using the symmetrical coordinate method and vector analysis during fault conditions was investigated for protection of a triaxial AC SC. The key development of this work is a methodology for the calculation of the protection settings with respect to the variations in the impedance of various topologies of AC SCs with inherent fault current limiting capability. Authors in [98] investigated the impact of SCs on protection systems, by proposing the utilisation of a differential relay as the primary protection and a distance relay as back-up protection. The results demonstrated that by applying the characteristics of SCs to relay settings, the fault detection is problematic, during single-phase to ground and three-phase faults, due to the variations in the SC resistance. Another effort to address the protection challenges of AC SCs is presented in [99]. Specifically, in this study the optimal impedance of an AC SC has been determined according to the fault current levels and the operating time of the over-current relay in order to address the impact of the variable AC SC resistance on the pre-defined protection settings and protection coordination. As a continuation of this work, the same authors propose in [100] a novel method named Expected Regret-based Impedance Selection (ERIS), based on which the impedance of an AC SC is determined under fault conditions. This also incorporates power system uncertainties, such as the connection status of the ICGs or lines. The numerical simulation results showed that the proposed methods can successfully determine the proper impedance of AC SCs from a power system protection perspective. Authors in [101] propose a correlation function for the detection of quenching, considering the phase difference between the voltage and current measurements. The developed method presents promising results related to the analysis of AC SC quenching, however, the proposed method is affected by harmonic components

and is vulnerable to the variations of the grid frequency. A quenching detection method which eliminates the harmonic interference is discussed in [102]. The developed algorithm is based on the Wavelet Transform (WT) of the voltage and current signatures measured at one terminal of the AC SC. Although the proposed scheme has been found to present increased sensitivity, its performance has not been scrutinised against different transient events and its practical feasibility has not been confirmed.

All the aforementioned protection schemes have formed a foundation for power system applications for AC SCs, however, none of them have been tested considering challenging transient conditions such as: i) the impact of resistive faults on protection sensitivity, ii) the protection discrimination by distinguishing highly-resistive internal faults and solid external faults and iii) protection stability against external faults and other disturbances. Additionally, there are no reported studies on the practical feasibility of these schemes, including consideration of anticipated time delays and the acquisition of necessary measurements and signals.

By assessing the reported studies and considering the AC protection requirements (i.e., sensitivity, stability, selectivity, security, operational speed), it can be concluded that the particularities of SC technology complicate the decision-making process of the existing protection schemes. Particularly, the impact of variable resistance on the resulting fault current and voltage waveforms results in an inability of distance protection relays to detect the fault and isolate the faulted zone [103]. This effect, in conjunction with the poor performance of distance relays against highly-resistive faults or in systems with high integration of RES [104], renders this type of protection insufficient for future grids with ICGs and AC SCs. Additionally, the reduced fault current magnitudes negatively impact the sensitivity of over-current protection schemes, compromising the overall system safety (the limitations of the over-current threshold-based methods will be analysed in subsection 1.2). Differential protection is one of the most popular protection schemes utilised in power system protection applications as it presents robustness under disturbances such as voltage and current variations [105]. Since the operation of the differential protection scheme relies on the comparison of remote and local signals, it is less affected by the quenching phenomenon than other existing schemes. However, as it is a communication-assisted scheme, it is affected by the communication time and reliability and requires equipment for data synchronisation in order to have efficient protection functionality [106, 107]. Another protection philosophy which is well established in AC

power systems for protection applications is the Travelling Wave (TW) based scheme. However, the application of TW-based methods to SCs requires cable models with a higher level of detail and granularity than is currently available. Specifically, the utilised SCs models shall cover a wide range of frequencies, as the TW effect can occur across a broad spectrum. Based on the technical literature, current models for SCs do not provide the necessary level of fidelity to accurately capture these effects, and therefore, TW-based methods cannot be effectively used to investigate the behavior of SCs.

Therefore, there are several outstanding issues which need to be solved for the protection of AC SCs. The goal of this thesis is to address the above-mentioned significant facets by proposing two novel protection schemes with fault detection and classification elements for the effective and reliable protection of AC grids with SCs.

4.2 Investigation of Over-Current Based Protection Solutions for AC SCs

Prior to presenting and analysing the proposed protection schemes, it is of paramount importance to highlight the need for more advanced and efficient protection solutions for AC SCs.

For this purpose, the studies presented in this section aim to assess the sensitivity and the stability margins of over-current threshold-based schemes for the protection of AC SCs. On that front, an over-current threshold-based protection logic has been developed in Matlab/Simulink and its performance has been investigated in terms of its sensitivity to internal faults as well as its stability against external faults and load switching events. The test cases have been obtained by conducting a series of faults using the AC network presented in Chapter 3 and depicted in Figure 4.1. The simulation studies contained internal, (F_{int}), and external, (F_{ext}), faults and load switching events. It is worth reiterating that external faults and load switching events can initiate the quenching of HTS tapes and consequently AC SCs, so it is of utmost importance to ensure that the protection scheme remains stable (i.e., the protection scheme does not falsely indicate the presence of an internal fault).

The internal faults were simulated at every 10% of the AC SC's length, while external faults were considered at the adjacent lines. All possible fault types were considered (i.e., LLL-G, LLL, LL-G, LL and L-G) with fault resistance up to 300 Ω. Load switching

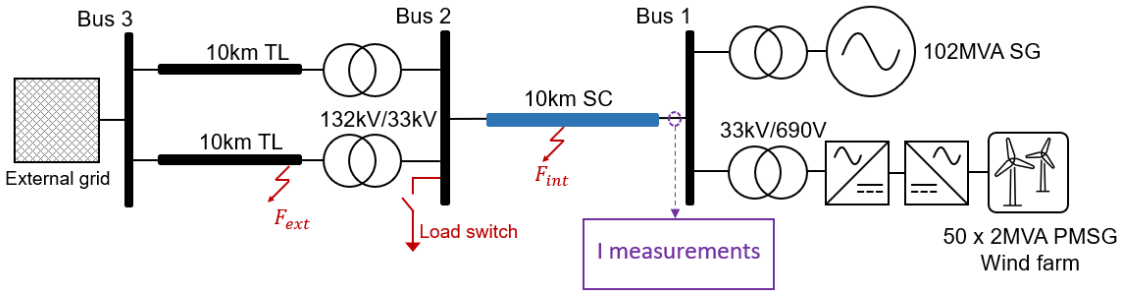

Figure 4.1: Examined AC network for over-current assessment.

events with different values of active and reactive power were simulated at the end of the AC SC at Bus 2. During the simulation process the three-phase currents flowing through the AC SC for all the investigated scenarios were captured at a sampling frequency of 20 kHz which is well-established and highly recommended for accurate and reliable measurements in power system applications [108, 109]. Particularly, for the presented studies it has been found that 20 kHz sampling frequency provides insights which are adequate to enhance the sensitivity and speed of protection schemes, while also enabling the utilisation of metering and data acquisition equipment with lower specification.

Regarding the current setting, a wide range of over-current thresholds was considered starting from 1.05 $p.u.$ to 2 $p.u.$ with steps of 0.1 $p.u.$ (base value corresponds to the nominal current). For the time settings, different values of time delay have been investigated starting from 40 ms to 120 ms with steps of 20 ms.

The performance of the over-current threshold-based scheme can be evaluated based on the results presented in Figure 4.2 which shows the total number of tripping signals initiated for internal faults, external faults, and load switching events, with respect to the pick-up current setting. The percentage of the tripping signals has been calculated by dividing the total number of scenarios, during which a tripping signal has been generated, by the total number of investigated fault scenarios for each case. The results presented in Figure 4.2 indicate that for a low over-current threshold (i.e., 1.05 $p.u.$), approximately 84% of the total number of internal faults are successfully detected. However, for the same current setting, the tripping signal is initiated during external faults and load switching events as well, resulting in the initiation of false tripping and eventually presenting a low degree of stability. To obtain high margins of stability, the threshold should be set to 1.4 $p.u.$ or beyond, which would comprise the element of sensitivity.

Furthermore, Figure 4.3 shows the number of tripping signals with respect to an increase in the time delay settings. The over-current threshold has been set equal to

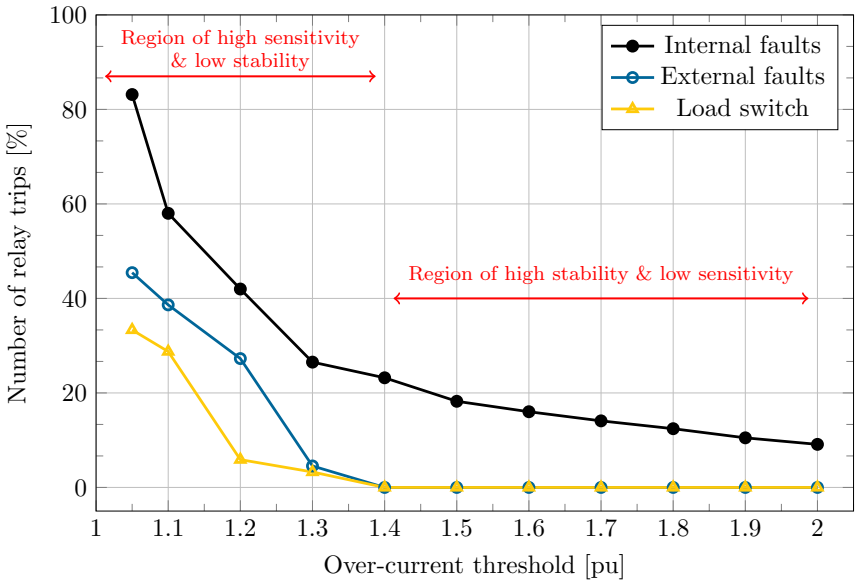

Figure 4.2: Performance of over-current threshold-based scheme under internal, external faults and load switching events with respect to the over-current threshold.

1.05 $p.u.$ and the results indicate that as the time delay increases, the protection sensitivity is deteriorated and the stability is improved. Specifically, for a time delay equal to 120 ms, the scheme remains stable against all the external faults and load switching events, but the internal faults remain undetected. Conversely, for low time delay settings the sensitivity of the over-current based scheme is improved, but the stability is jeopardised as a tripping signal is initiated for external faults and load switching events (i.e., initiation of false tripping signal).

Effectively, these results demonstrate that existing protection techniques, such as over-current based schemes, are not suitable to provide reliable solutions for AC SCs, combining both sensitivity and stability. In particular, it can be concluded that protection of AC SCs is a complex problem which cannot be solved with protection approaches based on threshold limits with time delays and grading. In future power grids, incorporating more ICG this challenge is expected to be more noticeable. This is due to the limited fault current contributed by ICGs [110], resulting in absence of quenching in SCs and consequently jeopardising the protection operational speed and reliability.

Undoubtedly, such a transition to a modern power grids with SCs creates an emerging need to reevaluate protection and fault management paradigms and investigate more advanced solutions. In particular, new criteria and approaches are required for the fault management solutions in order to ensure high degree of sensitivity, stability, accuracy and reliability. On that front, the work conducted in this chapter takes advantage of the

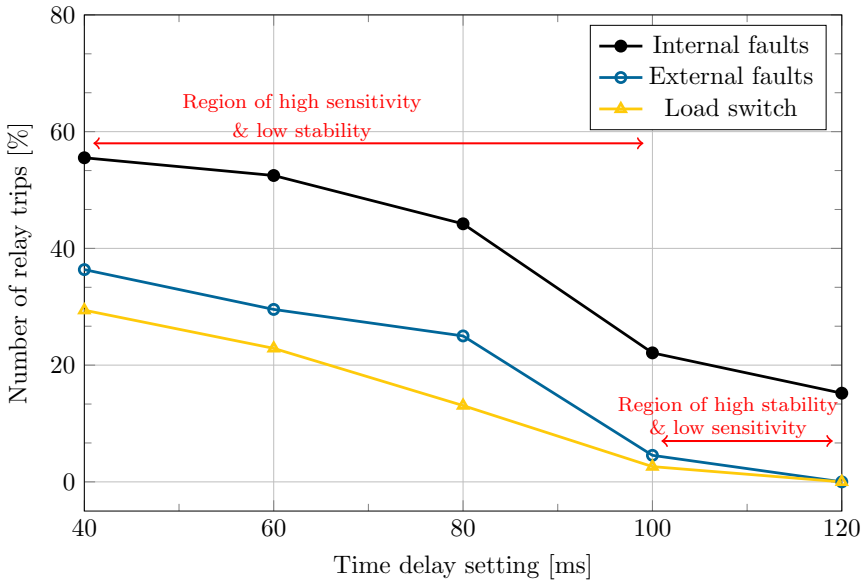

Figure 4.3: Performance of over-current threshold-based scheme under internal, external faults and load switching events with respect to the time delay setting.

benefits provided by AI-based techniques to propose robust and discriminative protection schemes for AC systems with SCs. AI-based methods have been selected and implemented to tackle the aforementioned limitations as powerful tools which are capable of providing fast, efficient, and accurate solutions for problems with a high level of complexity.

4.3 Introduction of AI in Applied Superconductivity

Recent developments have been proposed using AI to provide fast and efficient solutions to complex and nonlinear problems related to technical, manufacturing and economic aspects of applied superconductivity [111]. In many applications, AI methods have been applied to extract useful insights and hidden trends of the superconducting materials or to accelerate the discovery of new superconducting materials with potentially higher T_C [112–115]. Furthermore, the advantages of AI-based techniques have been exploited in the optimisation of the design procedure of superconducting apparatuses which constitutes a complex, time-consuming process with tight manufacturing constraints [71, 116–118]. The identification of the optimal size, structure and design parameters maximises the efficiency and reliability of the superconducting devices, while minimising the cost and losses. Another use of AI methods in large scale applications of applied superconductivity is in condition monitoring. In these tasks, the receiving signals of superconducting devices are continuously analysed and in conjunction with AI methods, operating conditions

of the devices can be determined [119, 120]. The obtained signals can include voltage, current, AC loss, or magnetic field. In particular, for AC SCs, due to their complex structure, the AI-based condition monitoring applications offer many advantages. AI can make predictions based on historical or reliable data and predict/forecast the temperature, AC losses and operation mode of SCs, supporting the uptake of such cable technology in real power systems. Additionally, AI-assisted condition monitoring has started to be utilised for the detection of magnet quenching [111]. Another application for AI in superconductivity which has started to gain increasing attention recently is the modelling of superconducting devices based on data rather than mathematical formulations. By taking advantage of the unique features of AI methods, the developed models reduce the high computational burden and present improved accuracy.

Therefore, a progressive merge of AI into applied superconductivity has started to be reported in the technical literature, creating new opportunities for the extensive investigation, development, and wide integration of SCs in future power grids [121].

4.4 Artificial Intelligence Algorithms for Fault Detection and Classification in Power Systems

Over the last few years, in the presence of digital transformation of power grids, an envisioned framework entailing AI algorithms has been emerged which is capable of providing meaningful real-time indicators and informed decisions for reliable fault management of power grids. This specific field of science has entered into the area of power system applications by offering disruptive solutions to tackle many challenges for future power systems. Essentially, purely mathematical expressions cannot be directly utilised to represent the state and behaviour of future power grids, since those expressions are of high order and multi-dimensional. At the same time, power grids themselves are becoming less subject to physics and more subject to control. For such reasons, the engineering community has started utilising AI methods to analyse big sets of data and expose physical quantities, which are invisible in direct measurements, towards the better understanding of the behaviour of power grids. The main benefits of these techniques are their precision and robustness to system parameter variations [122].

There are plenty of proposed AI algorithms utilised for fault detection and classification in distribution and transmission systems, such as Artificial Neural Networks (ANN),

Support Vector Machines (SVM) and tree-based algorithms. Each algorithm has its own characteristics and the selection of the appropriate model depends on the particularities of the specific task. The factors that play a significant role in determining which algorithm to use are composed of the type of the target value, the features of the available data, and the system computational efficiency [123]. The target value is used to categorise the problem into either a classification or regression task. When the target value is categorical, classification algorithms are utilised, while for continuous target values, regression models are appropriate. For the case of fault detection and classification of the fault as internal, external, or other events, the target value is categorical and thus the problem can be formed as a binary classification.

ANN algorithms are the most commonly used models in protection applications. This is because they offer a variety of advantages and exhibit excellent qualities such as the capability to incorporate with dynamic changes in power systems, the ability to find the solution for complex non-linear equations, normalisation and generalisation, and immunity to noise [124–127]. While there are several variations of ANNs, they all have great computational capabilities and are able to identify complex relationships among data. One drawback of ANN algorithms is that they are computationally intensive, requiring significant training time and computational power. However, recent advancements in technology, including optimisation functions and hardware with increased memory, have enabled the faster implementation of ANNs for power system applications [123]. To improve the efficiency and enhance the performance of ANN algorithms, many studies have started to focus on hybrid methods composed of ANN algorithms and feature extraction tools (i.e., WT) for reliable fault detection and classification in power grids. In particular, in [125], a hybrid method is reported for fault detection on distribution lines, utilising local currents from one end of the protected line. Specifically, the Discrete Wavelet Transform (DWT) is used as a feature extraction tool to obtain high-frequency components of the two aerial modal currents. The detailed coefficients are directly utilised as an input to train the ANN algorithm to perform fault detection and distinguish faults from other transient events. The results showed the accurate detection of faults, however, the presented method fails when a lighting strike evolves to a fault. The approach presented in [128] uses the WT of phase voltages and currents as inputs to train an ANN algorithm to perform fault detection and classification. The presented method is limited by the bandwidth of the measuring equipment as it requires information related

to high-frequency transients of the measured voltage. Additionally, the presence of other transient events which affect the protection discrimination have not been investigated. In [129], the combination of ANN and WT algorithms has been considered to address the challenge of detecting highly-resistive faults on transmission lines. The developed algorithm has been utilised to identify the faulty phase along with the specific feeder where the fault occurred. The results validated the performance of the developed method, however for the evaluation process only the testing dataset has been utilised and the effectiveness of the algorithm has not been scrutinised against previously unseen fault scenarios or other events such as external, faults. Furthermore, an intelligent fault detection algorithm for series compensated lines is reported in [130]. Particularly, the DWT technique is used to extract the detailed coefficients of pre-fault and post-fault signals of the three phase and ground fault currents at the sending end of a transmission line. The energy content of the detailed coefficients form the training data set fed into the ANN classifier. The resulting accuracy was 100% for the fault detection task and 97.43% for the fault classification task. However, during the simulation based studies, highly-resistive faults, multiple fault positions, and other transient events have not been considered.

Another widely used ML algorithm for fault detection and classification in power systems is the use of SVM models [124, 131]. SVM is a supervised learning algorithm which is based on statistical theory and is widely used for solving linear and non-linear classification, as well as regression, problems. Similar to ANN, SVM algorithms are characterised by high computational times during the training process. SVM possess excellent features for binary and multi-class classification problems, such as the capability to deal with arbitrarily structured data, over-fitting avoidance, avoiding convergence at local minima, and generalisation capability. Recently, the utilisation of SVM algorithms is reported for the development of hybrid methods for fault detection and classification in power grids. Specifically, in [132], a fault detection method for power distribution networks is proposed which uses DWT to extract the features of the transient fault current. The results showed that the performance of the proposed fault detection and classification technique yielded an accuracy of 98.5%. However, the performance of the developed method has not been validated against other transient events and external faults which may lead to protection maloperation. The normalised energy content of the detailed coefficients are used to train the SVM classifier for fault detection and fault

type classification. The work conducted in [133] presents an SVM-based algorithm for fault detection in long transmission lines. The proposed technique utilises the current waveform during a single cycle after a fault has occurred. The data is preprocessed using the wavelet packet transform to extract energy and entropy, and a feature matrix is created for the training of the SVM algorithm. The simulation results indicate that the developed method achieves accuracy of 99.21%.

Tree-based models constitute the last family of AI algorithms utilised for fault management problems. Advanced tree-based models such as Random Forest (RF) have low bias, do not require fine-tuning of hyperparameters, and have a low risk of overfitting. However, tree-based machine learning algorithms, such as Decision Trees (DT) and RFs, are not suitable to make predictions outside of the range of the training dataset (they present poor performance during extrapolation), they are not appropriate to handle high dimensional data with many correlated features, and their training process is time consuming [134]. Furthermore, DT and RF present poor performance compared to ANN and SVM algorithms during complex problems as they operate by learning simple thresholds on raw inputs, while ANN and SVM algorithms learn a better and more robust representation of the given data. A classifier based on the RF algorithm has been used in [135] to accurately identify and classify faults, utilising the total harmonic distortion of voltage and current at the point of common coupling. A hybrid method based on DWT and DTs is presented in [136] for detection and classification of power system faults, using the IEEE-34 node test system. The proposed method identifies the presence of a fault, using the sum of absolute values of detailed coefficients of the faulted current as the fault index [136]. In [137], the incremental quantity of faulted current signals was utilised as an indicative feature for the RF model to identify fault presence during a power swing. The resulting accuracy was 99.8% under various fault scenarios. However, the stability of the proposed method has not been evaluated against other transient events. A method for detecting and identifying faults in interconnected transmission lines using the DWT was proposed in [138]. The proposed method uses ANN and DT classifiers to classify faults into twenty-one categories for phase identification and four classes for ground fault identification. The accuracy of the classifiers was used to evaluate their performance, and the ANN classifier has been found to outperform DT with an accuracy of 100%.

Based on the literature review of fault detection and classification techniques using AI algorithms, it is clear that these methods can achieve very promising results with

respect to fault detection and classification in power systems. Hybrid approaches that combine AI classifiers with feature extraction tools tend to perform even better, presenting immunity against varying fault parameters, accounting for fault resistance, fault type, and fault location. However, it should be noted that the practical implementation and real-world performance of these methods have not been extensively evaluated and the time required for fault detection has not been thoroughly studied. Furthermore, even though such solutions have been found to be promising, there are some challenges related to the data generation, the computational requirements, and consequently the practical implementation of such solutions. In particular, most of the AI-based methods require databases composed of a variety of high-quality data (datasets which are characterised by variety, non over-fitted characteristics, and non-bias distribution [139]). In response to the challenge of data availability, as future power systems become data-rich, the emergence of Wide Area Measurement Systems (WAMs), based on Phase Measurement Units (PMUs), allow access to plentiful data, accelerating the widespread adoption of data-driven applications. In regards to the computational requirements, as the technology advances in both hardware and software, the computational burden is progressively minimised. Furthermore, with respect to the quality of the data, many pre-processing techniques have started to be utilised by the AI community in order to remove the bad or over-fitted data and increase the reliability and accuracy of AI models. Therefore, the progressive advancements in AI applications (i.e., deployment of AI-based high-fidelity digital twin models) and the easier access to various data would enable the seamless integration of AI methods into existing and future frameworks for establishing fault management strategies.

Considering future trends, the vital role that AI has started to play in the field of applied superconductivity and the compelling advantages offered by AI techniques in protection applications, the presented research proposes two hybrid AI-based schemes composed of fast and reliable fault detection and classification elements for the protection of AC SCs. Taking into consideration the aforementioned characteristics of AI algorithms and the complexity of the problem, ANN and SVM algorithms have been selected as the most suitable for the development of the proposed schemes.

4.5 Proposed Protection Schemes

In light of the unique advantages that AI-assisted fault management solutions offer, this section presents the development of two AI-based protection schemes for AC superconducting cables. As highlighted by the results of the fault analysis of AC superconducting cables in Chapter 3, effective fault management for these systems is a complex issue that requires new criteria and approaches to ensure a high degree of sensitivity, stability, accuracy, and reliability in the protection of AC superconducting cables.

The limitations of existing protection methods against the particularities of SCs technology have been revealed through an assessment of the current protection methods. To efficiently develop a reliable fault management scheme for SC, it is essential to realistically model SC performance during transient conditions and utilise advanced functions to perform tasks such as fault detection, classification, and location. The capabilities of AI-based models to address multi-variable, complex problems and extract meaningful insights are expected to play a crucial role in the fault management of SCs. Figure 4.4 presents an envisioned framework for the fault management of SCs, including potential input measurements, functions, and outputs.

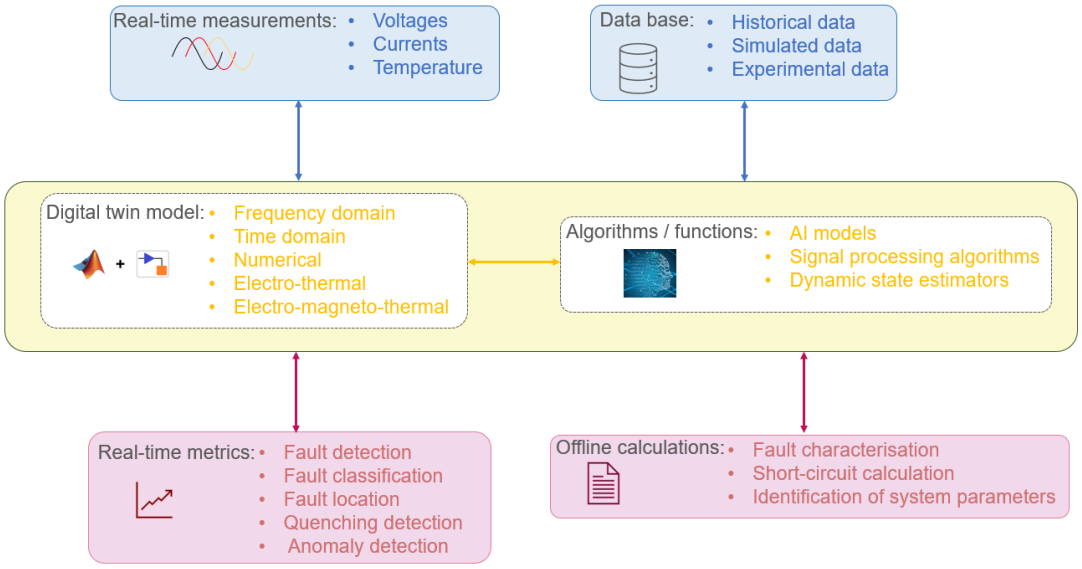

Figure 4.4: Envisioned framework enabling AI-assisted models for fault management of SCs.

4.5.1 Stages of the developed protection schemes

The proposed protection schemes are based on time-domain methods for discriminative detection and classification of faults in AC power systems incorporating SCs and high penetrations of RES. The presented schemes utilise feature extraction tools based on the Stationary Wavelet Transform (SWT), as well as AI classifiers to formulate the fault detection and classification features and discriminate between external faults, internal faults, and other network events. The performance of the proposed schemes has been validated through detailed transient simulation using verified models of SCs and ICGs. Moreover, their suitability for real-time implementation has been evaluated using the SIL testing environment. The developed data-driven protection schemes have been implemented in four discrete stages as illustrated in Figure 4.5. The following subsections describe in detail each stage of the development.

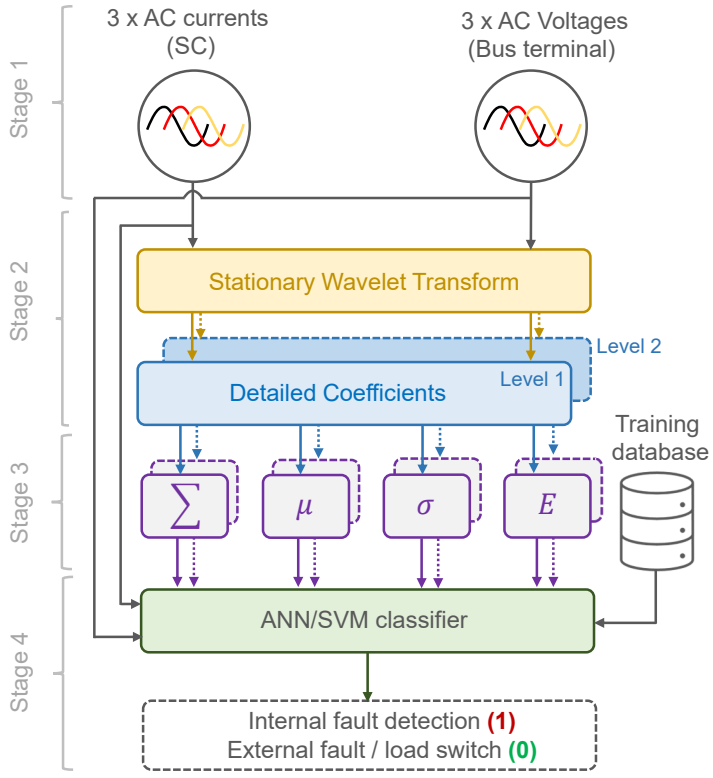

Figure 4.5: Schematic diagram of the proposed protection schemes with the fault detection and classification elements.

4.5.1.1 Stage 1 - Signal acquisition

At this stage, the three-phase current and voltage signals (i.e., currents flowing through the AC SC, and voltage at Bus 1 in Figure 4.1) are captured with a sampling frequency of 20 kHz. These signals are then passed through anti-aliasing filters, normalised, and packaged into appropriate windows to be processed by the SWT filters.

4.5.1.2 Stage 2 - SWT

The WT is a powerful tool for power system protection due to its capability to simultaneously analyse signals in the time and frequency domains. One of the main useful features of the WT is its inherent capability to detect signal singularities and disclose the useful information contained in measured quantities (e.g., voltages and currents) after a power system event. The WT can be distinguished in two categories: (i) Continuous Wavelet Transform (CWT) and (ii) DWT. The selection between them is a trade-off between the desired time resolution and processing requirements [140].

The DWT has been widely used for power system protection applications due to its reduced complexity and computational efficiency [141–143]. However, one of the significant drawbacks of the DWT is the effect of the downsampling process taking place at every decomposition level [144], leading to loss of information in the high frequency content of the analysed signal. A potential solution to overcome this drawback is the utilisation of the SWT algorithm, which does not downsample the signal, but instead it upsamples the filters by a factor of 2 at every decomposition level (by means of zero padding).

The output of the SWT at each decomposition level contains the same number of coefficients as the analysed signal. Therefore, the main advantage of the SWT is the preservation of the time information of the original signal at each level. The SWT algorithm can be implemented by applying discrete convolution to the analysed signal with the appropriate high-pass and low-pass filters, as in the case of the DWT, but without downsampling. Figure 4.6 illustrates the SWT procedure up to a decomposition level of 2.

Specifically, $x[k]$ is the original signal, $h_j[k]$ and $g_j[k]$ are the high-pass and low-pass filters at the $j-th$ level, and $A_j[k]$ and $D_j[k]$ are the approximation and detailed coefficients at the $j-th$ level. For the decomposition level j, the filters $h_j[k]$ and $g_j[k]$ are obtained by upsampling the filters at level $j-1$ which are then convolved with

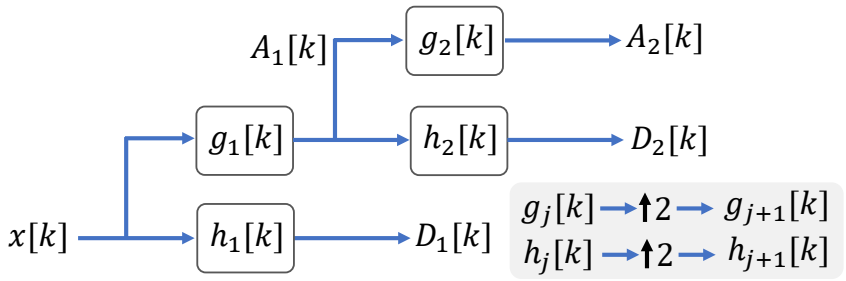

Figure 4.6: Stationary Wavelet Transform algorithm.

the approximation coefficient at level $j-1$ to produce the approximation and detailed coefficient of level j. For each decomposition level j, the detailed coefficients are calculated based on (4.1).

$$D_j[k] = \sum_{l=0}^{L-1} A_{j-1}[n] \times h_j[k-n] \tag{4.1}$$

where A_j is the approximation coefficients at level j, k is the index of the sample and L the order of the high pass filter $h[n]$.

In the presented research, the monitored parameters are subjected to Level 1 and Level 2 decomposition though the SWT technique. The selection of the most suitable decomposition levels is based on the frequency content of interest for the signal to be processed. Based on the literature, the *db*4 mother wavelet presents relatively high accuracy and reliability. Therefore it was selected for the purposes of the proposed scheme [141, 144, 145]. It shall be highlighted that wavelet design can be considered a dedicated and separate research area and is subject to the application requirements. Therefore, detailed design is beyond the scope of the presented work. Considering the *db*4 mother wavelet and the required level of decomposition, the required number of the samples per iteration is 8.

4.5.1.3 Step 3 - Feature extraction

A 30-sample moving data window with 29-sample overlap, has been applied on the monitored parameters and subsequent detailed coefficients at Level 1 and Level 2. The length of the data window has been selected based on offline trial simulations to achieve a high degree of reliability and efficiency in fault detection and classification. In the presented work, decomposition Level up to 2 has been selected as the maximum decomposition Level should not be set too high as the computational delay accumulates. However, this

should not be a significant limitation for the protection scheme since the most significant information for fault detection and classification lies in the high-frequency region, which corresponds to the lower decomposition Levels [146].

The numerical values contained within those time windows are used to extract feature vectors such as the sum $\sum(D_j)$, mean $\mu(D_j)$, standard deviation $\sigma(D_j)$, and energy content $E(D_j)$ of the absolute values of the detailed coefficients at Level 1 and Level 2. The $E(D_j)$ represents the amount of energy present in detailed coefficients, $\sigma(D_j)$ denotes the degree of variation of the detailed coefficients, $\mu(D_j)$ is the average value of the detailed coefficients and $\sum(D_j)$ represents the total value of the detailed coefficients [147]. The selection of the feature vectors has been determined through extensive offline trial and error simulations, aiming to unlock deeper and more meaningful insights in the nature and evolution of faults, and consequently enhance the performance of the ML algorithms. The feature vectors were calculated as presented in (5.8) to (5.11) below:

$$\sum(D_j) = \sum_{k=1}^{n_w} |D_j(k)| \tag{4.2}$$

$$\mu(D_j) = \frac{1}{2^j \cdot n_w} \sum_{k=1}^{n_w} |D_j(k)| \tag{4.3}$$

$$\sigma(D_j) = \sqrt{\frac{1}{2^j \cdot n_j} \sum_{k=1}^{n_w} (|D_j(k)| - \mu(D_j))^2} \tag{4.4}$$

$$E(D_j) = \sum_{k=1}^{n_w} [D_j(k)]^2 \tag{4.5}$$

where $D_j(k)$ is the $k-th$ detailed coefficient for each decomposition level $j = 1, 2$, and n_w is the window size.

These feature vectors can represent effectively the state of the AC SC during the simulated transient events and form the basis for fault detection and discrimination. It is worth highlighting that the feature vectors are normalised by subtracting the mean value and dividing by the standard deviation as presented in (5.12):

$$x(i)_{scaled} = \frac{x(i) - \overline{X}}{\sigma(X)} \tag{4.6}$$

where $x(i)$ is the value of the sample in the feature vector x, $\overline{X}$ is the mean value of each feature in the training set, and $\sigma(X)$ is the standard deviation of each feature in the

training set.

4.5.1.4 Stage 4 - Fault detection and classification

The normalised feature vectors along with the three-phase faulted current measurements obtained at the AC SC terminal connected to Bus 1, and voltage measurements captured at Bus 1 (Figure 4.1), have been utilised as inputs to ML-based algorithms to perform fault detection and classification. The main goal of the developed fault detection and classification elements is to provide fast detection of internal faults and reliable discrimination between internal faults, external faults and other disturbances. For that purpose the fault detection and classification task has been formulated as a binary classification problem and the developed detection and classification elements initiate at their output '1', for internal faults and '0', for external faults and other disturbances. Effectively, the output of the binary classification elements is used as a tripping signal which would ultimately go to the corresponding CB, which protects the AC SC, to clear the fault, however the presented studies evaluate the performance of the developed schemes considering up to initiation of the tripping signal. For the development of the detection and classification elements, ANN and SVM algorithms have been selected which have been proven to be fast and reliable for fault diagnosis in power systems [125,130,148,149]. The detailed analysis of the ML algorithms utilised in this work are presented in the following subsection.

4.5.2 ML-based algorithms

4.5.2.1 Artificial Neural Networks

ANNs represent a computational model inspired by the architecture and operations of biological neural systems. ANNs dynamically adapt their structure in response to input and output requirements, making them adept at modeling complex nonlinear relationships within data [150]. These networks are organised into layers, comprising interconnected nodes, or neurons. Two fundamental learning algorithms are employed in ANNs: the feed-forward algorithm and the back-propagation algorithm.

In the feed-forward approach, input data traverse from input nodes through hidden nodes to output nodes, following a forward path. Conversely, the back-propagation method leverages training data to iteratively refine the network by adjusting weights and biases associated with error values, ultimately converging towards correct output

predictions [151].

A pivotal component in ANNs is the transfer function, which plays a vital role in capturing the nonlinear relationships between input and output data [152]. Figure 4.7, presented below, illustrates a typical multi-layer ANN model. This architecture encompasses three layers: the input layer, hidden layer, and output layer. The input layer establishes connections with one or more hidden layers, where neurons are referred to as perceptrons, before reaching in the output layer.

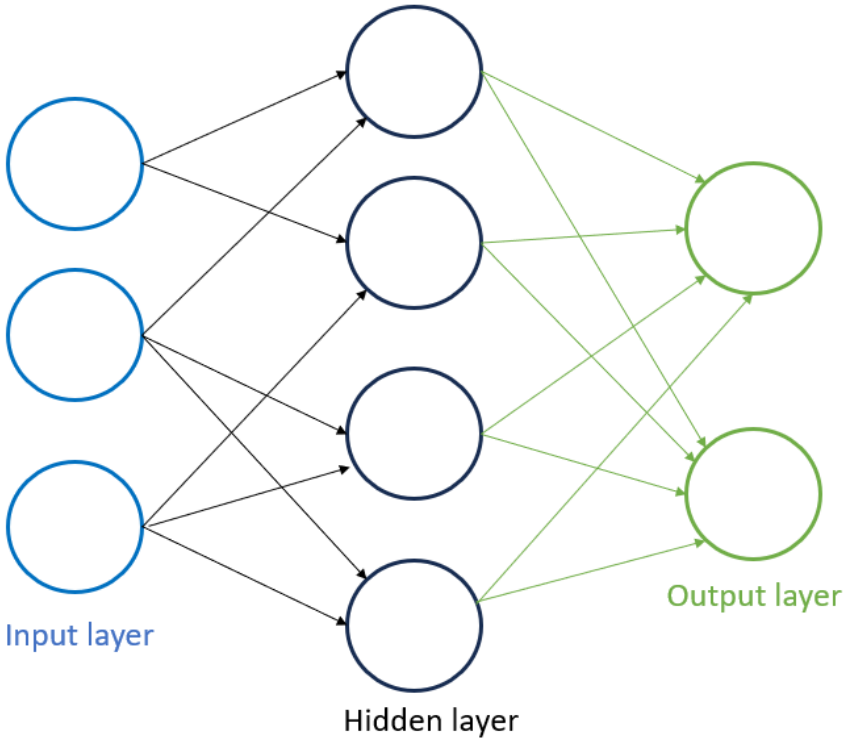

Figure 4.7: Typical multi-layer ANN model.

As it has been mentioned the training process consists of two steps: feed-forward approach and back-propagation process. In the context of the back-propagation neural network, the term "output" refers to the information that is fed back into the input phase to compute adjustments in the weights [152]. The process involves calculating the error at each step and location, starting from the final stage and transmitting the considered error backward. Initially, the weights of the back-propagation algorithm are randomly selected and incorporated into an input pair. Following each step, these weights are updated with new values, and this process is repeated for all possible input-output combinations found in the training data provided by the creator [153]. This repetition continues until the network converges to the desired target values within a predefined error

tolerance. This entire procedure is applied to each layer within the network, working in a reverse direction. Back-propagation is chosen for training due to its ability to handle large datasets [154]. The Mean Square Error (MSE) technique is employed to compute the error at each iteration (representing the loss function). The incorporation of back-propagation algorithm is as follows based on [128]. The network's objective during training is to minimise this error (MSE) by adjusting its weights and biases through the back-propagation algorithm.:

Forward propagation:

$$a_j = \sum_{i}^{m} [w_{ji}^{(1)} x_i] \tag{4.7}$$

$$z_j = f(a_j) \tag{4.8}$$

$$y_j = \sum_{i}^{M} [w_{ki}^{(2)} z_j] \tag{4.9}$$

Output difference:

$$\delta_k = y_k - t_k \tag{4.10}$$

Back propagation for hidden layers:

$$\delta_i = (1 - z_w^2) \sum_{k=1}^{K} [w_{kj} \delta_k] \tag{4.11}$$

where a_j denotes the weighted sum of inputs, w_{ji} is the weight related to the neuron connections, x_i corresponds to the inputs, z_i is the activation unit of the input, δ_k is the derivative of the error at kth neuron, y_i is the ith output, y_k is the activation of unit k, t_k denotes the corresponding target of the input and δ_j is the derivative of error.

The MSE function applied to each output in each iteration and is calculated based on Eq 4.12:

$$MSE = \frac{1}{N} \sum_{1}^{N} (E_i - E_o)^2 \tag{4.12}$$

where N is the number of iterations, E_i is the actual output and E_o is the output of the model.

The gradient of the error with respect to first layer weights and second layer weights

are calculated and in this step the previous weights are updated

The performance of ANN algorithms rely heavily on the fine tuning of their hyper-parameters [123]. On that front, in order to select the most-suitable ANN architecture and the best training model for fault detection and classification, a wide range of ANN network topologies have been tested. The optimum hyperparameters were set based on the Grid Search (GS) technique. For this purpose, hyperparameter tuning was performed, considering different combinations of hyperparameters. Specifically, the hyperparameters defined with the GS process are the following: i) the number of hidden layers, ii) the learning rate, iii) the batch size, and iv) the number of neurons at each hidden layer. The performance of all the combinations was evaluated based on the K-fold Cross-Validation (CV) technique. Specifically, the dataset was divided into K subsets and the model was trained and tested for each hyperparameter combination K times. In each iteration, $K-1$ subsets were used for training, while the remaining 1 fold was used for validation. The optimum combination of the hyperparameters was determined based on the K-fold CV score, which is the average of the scores obtained on each subset.

In this study, the 5-fold CV technique was utilised, while the F1-score was selected as the 5-fold CV evaluation metric, in order to select the optimum hyperparameters for the ANN algorithm. The optimum hyperparameters and subsequently the best ANN algorithm setup are presented in Figure 4.8.

The developed ANN model is a fully-connected, multi-layer model which consists of 1 input layer with 54 neurons (the number of neurons in the input layer is equal to the length of the feature vectors) and 8 hidden layers with 120 neurons in total. The GS 5-fold CV technique revealed that a deep ANN network is required in order to learn a robust data representation and present higher generalisation capability. Furthermore, to improve the performance of the ANN classifier, the drop-out technique was used for the hidden neurons during the training process in order to reduce interdependent learning amongst the neurons and consequently minimise over-fitting to the training data. The optimisation method used is the Adam optimiser, the learning rate has been defined based on the GS 5-fold CV technique, while the rest of the parameters were used as defined within the Pytorch framework.

The ANN algorithm operates as a binary classifier, and therefore it has one neuron in the output layer. The output value varies from 0 to 1 due to the utilisation of the log-sigmoid function as the activation function for the output layer. The equation of the

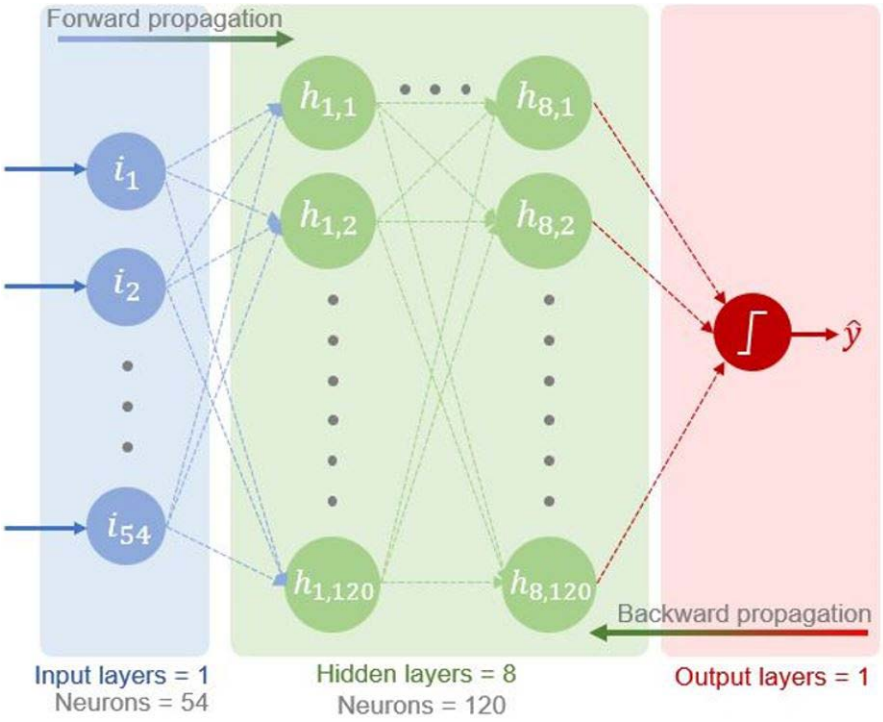

Figure 4.8: Architecture of the developed ANN algorithm.

log-sigmoid function is given by Eq 4.13:

$$\sigma(x) = \frac{1}{1 + e^{-x}} \tag{4.13}$$

An activation function in a neural network is a mathematical function that determines the output of a neuron or a node in a neural network. It introduces non-linearity to the network, enabling it to learn complex patterns and relationships in the data. Activation functions are essential because without them, a neural network, no matter how deep, would simply be a linear model, failing to handle non-linear relationships in data [153]. Specifically, the log-sigmoid function yields a probability value for each class. In this research, in order to convert the predicted probability value to a class label (0 or 1), a decision threshold equal to 0.9 has been selected for both the training and testing processes. This means that any probability above the threshold 0.9 corresponds to output 1 and indicates the presence of an internal fault, generating a tripping signal. The decision threshold allows the mapping of the log-sigmoid output to a binary classification category and its value is chosen to clearly indicate the split between the classes, increase classification accuracy, and limit misclassification [155]. The decision thresholds are subject to the classification problem and shall be tuned for each ML application individually [156]. In the presented work the decision threshold of 0.9 has been selected to penalise false

classifications. In subsection 4.6.1.1 the investigation of different decision thresholds and their impact on ML algorithms performance is presented.

4.5.2.2 Support Vector Machine

SVMs were originally developed for tackling classification problems within the context of statistical learning theory and structural risk minimisation [1]. The idea of the SVM algorithm is to non-linearly map the input vectors to a high dimensional feature space and define a decision boundary. For a given set of labeled training data, an optimal hyperplane is determined as a solution of an optimisation problem. The optimal hyperplane is the one that best separates the features into two classes. The selected data points from the training set which affect the position of the dividing hyperplane are called support vectors. By projecting the hyperplane onto the initial dimensions, the desired decision boundary can be determined. The SVM algorithm can be explained as a Wolf's dual optimisation problem based on [157]. The transformation of data into a feature space is accomplished through a non-linear transformation function denoted as Φ [133].

$$\Phi : R^n \rightarrow F^m \qquad x_i \rightarrow \Phi.(x_i) \tag{4.14}$$

Subsequently, within this high-dimensional feature space, the data can be rendered linearly separable through the application of another function, denoted as f. This function maps the data into a decision space (Y^2), where $Y \in (+1, -1)$

$$\Phi : F^m \rightarrow Y^2 \qquad \Phi.(x_i) \rightarrow f(\Phi.(x_i)) \tag{4.15}$$

In cases where the data exhibits linear separability, there exists a vector $w \in R^N$ and a scalar $b \in R$ such that $y_i(w.x_i + b) \geq 1$ for all the patterns included within the training data set. Consequently, the hyperplane is positioned in such a way that $w.x + b = 1$ for the closest points on one side and $w.x + b = -1$ for the closest points on the other side. This optimal hyperplane successfully separates points belonging to different classes while maximising the margin of separation. The identification of an optimal separating hyperplane involves solving the following equations based on Eq 4.16 [44]:

$$min\frac{1}{2} \parallel w^2 \parallel + C(\sum_{i=1}^{l}(\epsilon_i)) \tag{4.16}$$

the minimisation of Eq 4.16 is subject to $y_i(w.x_i + b) \geq 1 - \epsilon_i$ where $\epsilon_i \geq 0 \forall i$

The solution to this constrained optimisation problem is derived by constructing a Lagrangian based on Eq 4.17 [148]:

$$\lambda(w, b, a) = \frac{1}{2} \parallel w^2 \parallel -(\sum_{i=1}^{l} a_i(y_i(w.x_i + b) - 1) \tag{4.17}$$

Minimising the Lagrangian with respect to the primal variables w and b and maximising it with respect to the dual variable a_i, leads to the determination of the solution vector in terms of the training patterns. Once the optimisation problem is solved, the training points with $a_i > 0$ denote the support vectors, while w and b can be given by Eq 4.18 [149]:

$$w = \sum_{i=1}^{l} a_i y_i x_i \tag{4.18}$$

where x is a test vector and b can be calculated based on Eq 4.19:

$$b = y_{sv} - \sum_{i=1}^{l} a_i y_i k(x_i x_j) \tag{4.19}$$

Considering the above analysis and that sgn is the signal function, the optimal decision function is formulated as follows [149]:

$$f(x) = sgn(\sum_{i=1}^{l} a_i y_i k(x_i x_j + b) \tag{4.20}$$

where k denotes the kernel function and serves as a means to compute the inner product $\Phi(x_i, \Phi(x_j))$ within the feature space, acting as a function of the input data.

In the presented work the values of the SVM model parameters have been selected based on the combination of the GS and 5-fold CV methods and, similar to the ANN, the F1-score was utilised as the 5-fold C evaluation metric. The output of the SVM model is the actual class label (0 or 1) of the classified data, determined by the optimal hyperplane. For the final SVM model, the selected hyperparameters are the following: $C = 100$ and $\gamma = 1$, kernel function= Radial Basis Function (RBF).

4.5.3 System training

For the purpose of the simulation-based training, the system depicted in Figure 4.1 has been utilised and a series of systematic iterative simulations have been performed (similar to those presented in subsection 4.2 for the testing of the over-current based scheme).

Specifically, the simulated scenarios include internal faults applied at every 10% of the AC SC's length, external faults occurring at the adjacent lines considering all fault types (i.e., LLL-G, LLL, LL-G, LL and L-G) and R_f up to 300Ω, and load switching events occurring at Bus 2. The final dataset is composed of 1750 events. To prepare the dataset effectively for the proposed schemes, it's crucial to include both, fault and non-fault cases, in a balanced ratio while ensuring a variety of scenarios. This balance ensures that the proposed scheme encounter a realistic distribution of scenarios, aiding their ability to generalise well. A diverse dataset with a balanced ratio, such as 1:1 for fault and non-fault cases, helps prevent bias in the AI-based models' learning process, ultimately enhancing their predictive capabilities. For each simulation scenario, the waveforms of current flowing through the SC's phases (measured at the SC terminal connected to Bus 1), and the voltage measured at Bus 1, were captured for 5 cycles (1 pre-fault and 4 during fault). By using 1 pre-fault cycle, the scheme can establish a baseline for normal operation, while using 4 during fault cycles can provide more than enough information to accurately detect and classify the fault type. All the feature vectors presented in Subsection 4.5.1.3 were also extracted as part of the training process. Normalisation was also applied to scale the feature vectors prior to the training process in order to improve the performance of the ANN and SVM algorithms, and to accelerate the learning process. The monitored parameters and calculated feature vectors were used to create a Python-based training data base using the PyTorch open source library. From this dataset, 60% was used for training and 20% for validation, while the remaining 20% was used for testing according to common practice utilised in ML applications [158].

4.5.4 Anticipated time delays of the proposed schemes

It is important to ensure that the proposed protection schemes will operate correctly, despite delays expected in real-life implementation. The anticipated operating time t_{op} of the proposed scheme comprises the delays associated with the window-based processing t_{dw}, the delays of data processing t_{dt} (accounting for digitisation and transmission), and the time required by the ANN and SVM algorithms to produce a binary decision t_{ML}:

$$t_{op} = t_{dw} + t_{dt} + t_{ML} \tag{4.21}$$

The delay associated with the window-based processing t_{dw} can be calculated as follows:

$$t_{dw} = (n_{w-fv} - n_{w-ov}) \cdot t_s \tag{4.22}$$

where n_{w-fv} is the length of the processing window for the feature vectors, n_{w-ov} is the window overlap, and t_s is the sampling time. For this application a 30-sample window, with 29 samples overlap at 20 kHz, has been assumed that is efficient in terms of protection speed operation, reliability and computational speed and thus the t_{dw} is 50 μs.

The proposed protection schemes require 6 measurements to be digitised, concentrated, and transmitted to the protection system for further processing. Considering a modern centralised system with Merging Units (MUs) and an Ethernet switch based on IEC-61850 to collect and transmit all measurements in real-time, the overall time delays for digitisation and transmission t_{dt} can be calculated as follows [141]:

$$t_{dt} = t_s + t_{MU} + t_{Eth} + t_{ps} \tag{4.23}$$

where t_s is the maximum delay due to the analogue sampling (i.e., $t_s = 1/f_s = 1/20\,kHz = 50\ \mu s$), t_{MU} is the processing time in the MU (i.e., the time to encode the sampled values), t_{Eth} is the total maximum Ethernet network latency, and t_{ps} is the processing time for the protection system (i.e., the time to decode the sampled values). Assuming one Ethernet link and 8 competing measurements, t_{Eth} can be estimated to be 6.34 μs [141]. t_{MU} and t_{ps} can be estimated as 12 μs and 9.5 μs, respectively, based on the work conducted in [159]. Therefore, the overall resulting t_{dt} is 77.84 μs.

The time required by the ML-based algorithms (i.e., t_{ML}) to produce the tripping signal is subject to a number of variables such the algorithm complexity, the coding efficiency, the processing power of the system, etc. Therefore, t_{ML} cannot be assessed theoretically but will be evaluated experimentally in the following section.

4.6 Evaluation of the ANN and SVM Algorithms Based on AI Metrics

The performance of the proposed protection schemes has been initially assessed based on widely-used AI evaluation metrics. At the initial stage of the evaluation process, the robustness and classification capability of the developed algorithms were tested using the classification accuracy and F-1 score as evaluation metrics.

4.6.1 Accuracy evaluation

The ANN and SVM algorithms were tested using 20% of the pre-simulated dataset of 1750 cases, which contain all types of events. The accuracy and F1 score, both have been calculated based on the normalised confusion matrix produced for each binary classifier. Table 4.1 and Table 4.2 present the normalised confusion matrix of the ANN and SVM classifiers, respectively.

The high percentage value of True Positive (TP) predictions indicates the capability of both classifiers to correctly classify internal faults, while the high percentage value of the True Negative (TN) predictions show that both algorithms can predict correctly the external faults and load switching events, preventing protection operation during these events. Regarding the percentage value of False Positive (FP) and False Negative (FN) predictions, they must be in principle very low as they indicate incorrect predictions. Practically, these values would falsely flag the presence of an internal fault and the absence of external fault and load switching events, which would compromise the stability and sensitivity of the proposed schemes. From the perspective of power system protection, FN predictions have a more severe impact than that of FP, as the former results in undetected faults, threatening system security, while the latter will lead to false initiation of a tripping signal and consequently to reduced system availability.

The results presented in Table 4.1 and Table 4.2 show that the percentage of FP predictions for the ANN model is higher compared to those of the SVM, which suggests that SVM provides higher reliability and availability. Conversely, the percentage of FN predictions for the ANN is slightly lower compared to those of the SVM, which highlights that the ANN provides a higher degree of dependability. Generally, there is clearly a trade-off between the reliability and dependability.

Table 4.1: ANN confusion matrix.

	Predicted Negative	**Predicted Positive**
Actual Negative	TN=99%	FP=1.44%
Actual Positive	FN=0.96%	TP=99.6%

Table 4.2: SVM confusion matrix.

	Predicted Negative	**Predicted Positive**
Actual Negative	TN=99%	FP=0.048%
Actual Positive	FN=1.06%	TP=97%

The accuracy, ACC, and F1-score for both algorithms have been calculated based on

(4.24) and (4.25), respectively:

$$ACC = \frac{TP + TN}{TP + TN + FP + FN} \tag{4.24}$$

$$F1 - score = 2 \cdot \frac{precision \cdot recall}{precision + recall} = \frac{TP}{TP + 1/2 \cdot (FP + FN)} \tag{4.25}$$

Accuracy is a measure of how often the classifier makes the correct prediction and, as can be seen by (4.24), is defined as the ratio of the number of correct predictions to the total number of predictions. The F-1 score is a balance metric that presents the harmonic mean between precision and recall as can be seen by (4.25). Precision is a measure of the proportion of TP predictions among all positive predictions made by the classifier, while recall measures the proportion of TP predictions among all actual positive cases.

Taking into account the values presented in Table 4.1 and Table 4.2, the resulting accuracy of the ANN and SVM algorithms is 98.88% and 99.44%, respectively, while the resulting F-1 score is 98.87% and 99.43%, respectively. The results of the accuracy test indicate that the SVM algorithm is more effective at making correct predictions in a given number of scenarios. Thus, the SVM model demonstrates a higher level of sensitivity against internal faults and stability against external faults and load switching events. Furthermore, the higher value of F1-score for the SVM model indicates that SVM presents a better balance of correctly identifying the presence of an internal fault (high recall) and not identifying external faults and load switching events as internal faults (high precision).

4.6.1.1 Investigation of different decision thresholds for the ANN algorithm

This subsection investigates the accuracy and F-1 score of the ANN algorithm with respect to different decision thresholds. In particular, in subsection 4.6.1 it has been reported that the accuracy of the ANN algorithm is 98.88% and F-1 score 98.87% for decision threshold equal to 0.9. Additionally, the confusion matrix and accuracy of the ANN algorithm have been calculated considering decision thresholds equal to 0.5 (Table 4.3), 0.7 (Table 4.4) and 0.99 (Table 4.5), during the training and testing processes. The aim of this assessment is to evaluate the impact of the decision threshold on the performance of the ANN.

Upon examination of the data presented in Table 4.3, the resulting accuracy of the

Table 4.3: ANN confusion matrix for decision threshold equal to 0.5.

	Predicted Negative	**Predicted Positive**
Actual Negative	TN=98%	FP=2.4%
Actual Positive	FN=0.72%	TP=99.9%

ANN is 98.45% and the F-1 score is 98.46% for decision threshold equal to 0.5. A notable observation is that as the decision threshold decreases from 0.9 to 0.5, the value of FP increases which indicates that the models misclassify more external faults and switching events as internal faults and initiate a false tripping signal. The value of TP is increased, while the values of FN and TN present a slight decrease.

Table 4.4: ANN confusion matrix for decision threshold equal to 0.7.

	Predicted Negative	**Predicted Positive**
Actual Negative	TN=98.55%	FP=1.92%
Actual Positive	FN=0.96%	TP=99.6%

Considering the resulting confusion matrix in Table 4.4, the accuracy of the ANN classifier is 98.57% and the F1-score is 98.57% for a decision threshold of 0.7. As the decision threshold decreases, there is an increase in the number of FP classifications and thus more external and load switching events trigger the initiation of a tripping signal. Furthermore, there is a decrease in the number of TN classifications, while FN classifications remain the same.

Table 4.5: ANN confusion matrix for decision threshold equal to 0.99.

	Predicted Negative	**Predicted Positive**
Actual Negative	TN=99.75%	FP=0.73%
Actual Positive	FN=1.93%	TP=98.79%

Based on the results presented in Table 4.5, the resulting accuracy of the ANN algorithm is 97.40% and the F-1 score is 98.67% for a decision threshold of 0.99. As can be observed, a further increase in the decision threshold results in a further increase in the value of FN, compromising the sensitivity of the developed schemes. The number of FP and TP is decreased, while the value of TN is slightly increased.

Therefore, from the presented analysis, it can be concluded that as the value of the decision threshold increases, the range of predicted probabilities which indicate the presence of an internal fault is reduced. Specifically, for decision threshold equal to 0.99, only probabilities above 0.99 are converted to output '1' and initiate the corresponding tripping signal. This creates the challenge of an increase in FN predictions, affecting the

sensitivity of protection schemes and threatening system security. Conversely, when the decision threshold decreases from 0.9 to 0.7 and 0.5, the value of FP increases, leading to the initiation of a tripping signal for external faults and load switching events and consequently affecting the discrimination capability and stability of protection schemes, while the values of FN remain approximately unchanged. It is worth reiterating that the consequences of an increase in the value of FN and the subsequent increase in the number of undetected faults is more severe than an increase in the value of FP for the safety of the power system. Considering these observations and the resulting accuracy for each decision threshold, it can be determined that the value of 0.9 for the decision threshold of the ANN algorithm is appropriate for the investigated classification problem.

4.7 Offline Simulation Results

This section presents the simulation results for an internal LLL-G solid fault applied at 5% of the AC SC's length at $t = 10\ ms$. The primary objective of this section is to visually demonstrate Stage 1, Stage 2, and Stage 3 of the protection scheme development process. To achieve this, a series of figures are provided which depict the measured current and voltage signatures, as well as their SWT transformations and extracted feature vectors. It is worth reiterating that the offline simulation-based studies conducted at Stage 1, Stage 2 and Stage 3 of the development process were utilised to perform the SWT of the fault current and voltage signatures, calculate the detailed coefficients along with the corresponding feature vectors, and eventually form the dataset for the training and testing of the developed protection schemes.

Figure 4.9a to Figure 4.9c show the fault current and voltage signatures measured at one terminal of the AC SC and at Bus 1, respectively. Specifically, Figure 4.9a illustrates the fault current flowing through the YBCO layer for the three phases, Figure 4.9b shows the fault current flowing through the copper stabiliser layer and former for the three phases, and Figure 4.9c presents the voltage signatures for the three phases.

As depicted in Figure 4.9a, the fault is initiated at $t = 10\,ms$, leading to the quenching of the HTS tapes. As a result, the fault current is redirected to the copper stabiliser layer and the former (Figure 4.9b) which provides a path with lower resistance. Figure 4.9d through Figure 4.9l show the detailed coefficients of decomposition Level 1 and Level 2 for the fault current flowing through the YBCO layers, as well as the fault current flowing through the copper stabiliser layers and former for all three phases, and the

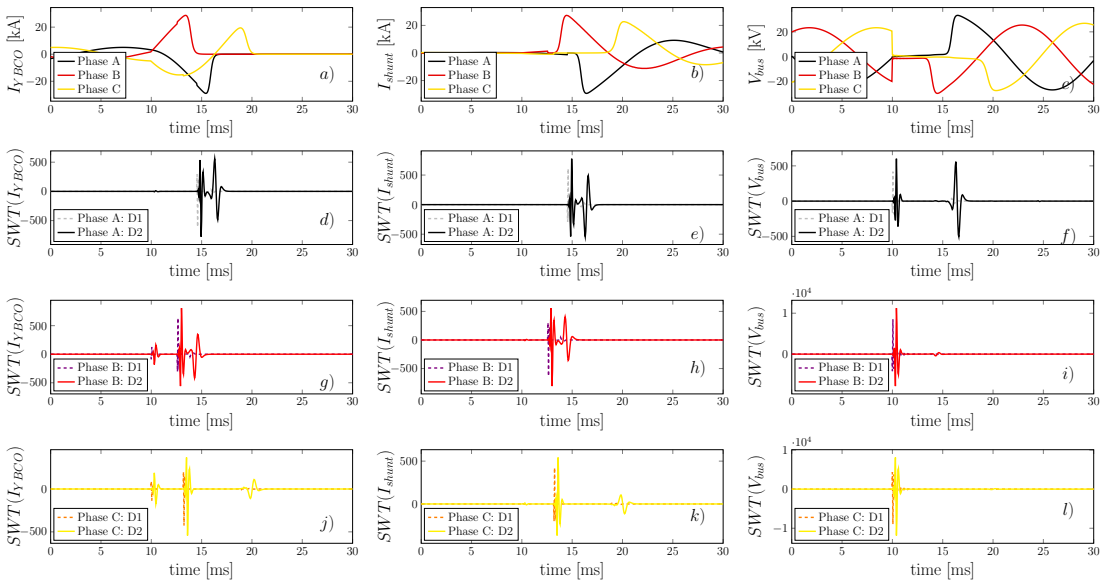

Figure 4.9: Detailed coefficients of decomposition Level 1 and Level 2 resulting from the SWT of the fault current and voltage waveforms during an internal, LLL-G solid fault at 5% of the AC SC's length.

detailed coefficients of the three-phase voltage signatures. As can be seen in Figure 4.9, the utilisation of the SWT technique leads to unique peaks which indicate the presence of a transient (i.e., fault).

Furthermore, the simulation results of the feature vectors are presented in the following figures. In particular, Figure 4.10a to Figure 4.10i depict the magnitude of the sum of absolute values of the resulting detailed coefficients of decomposition Level 1 and Level 2 for the three phases. Figure 4.11a to Figure 4.11i show the magnitude of the standard deviation of the absolute values of the current and voltage detailed coefficients of decomposition Level 1 and Level 2. Figure 4.12a to Figure 4.12i display the magnitude of the mean of the absolute values of the detailed coefficients of decomposition Level 1 and Level 2. Finally, Figure 4.13a to Figure 4.13i display the magnitude of the energy of the detailed coefficients of the current and voltage signatures derived from decomposition Level 1 and Level 2.

Based on the extensive simulation results, the SWT technique has proven to be an exceptionally powerful tool for feature extraction in power systems. The implementation of SWT enables the extraction of unique peaks, which in turn facilitate a more comprehensive understanding of the transient events occurring within the system. As a result, fault detection becomes increasingly distinct, an attribute commonly referred to as 'signal singularity' [160].

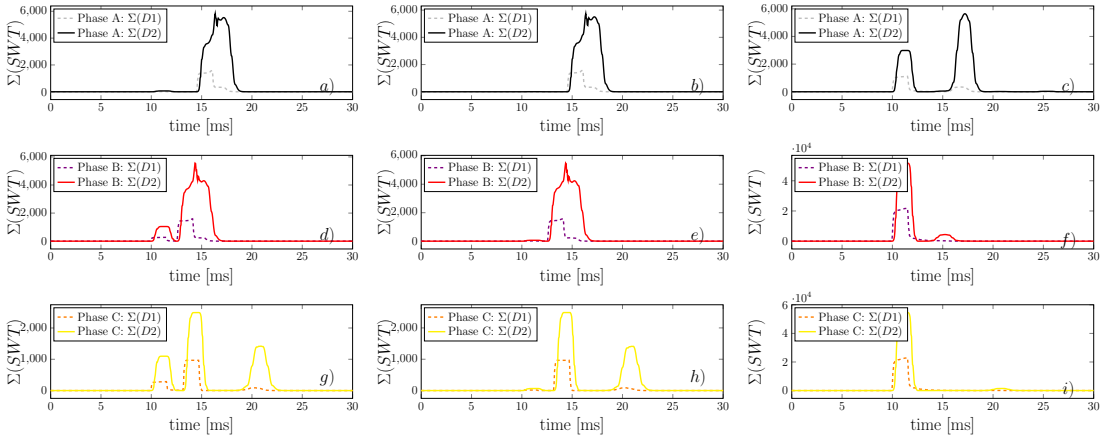

Figure 4.10: Sum of absolute values of the detailed coefficients of decomposition Level 1 and Level 2 for the three phases.

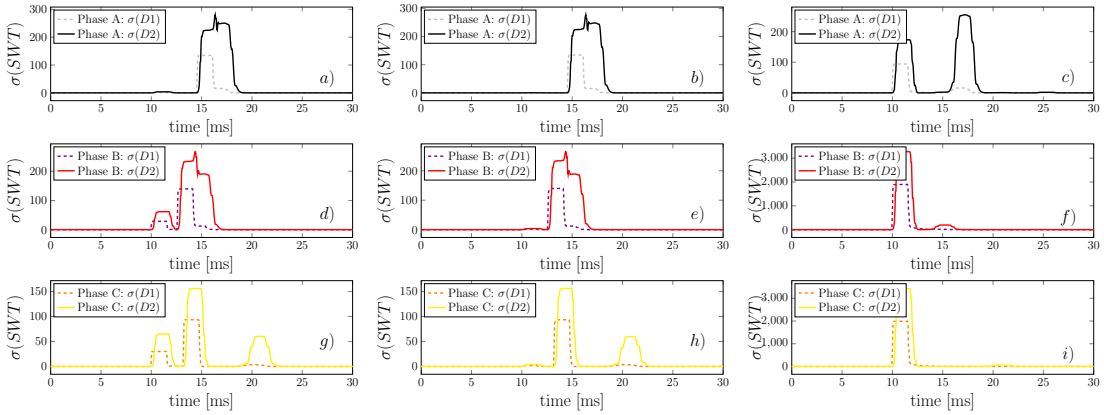

Figure 4.11: Standard deviation of absolute values of the detailed coefficients of decomposition Level 1 and Level 2 for the three phases.

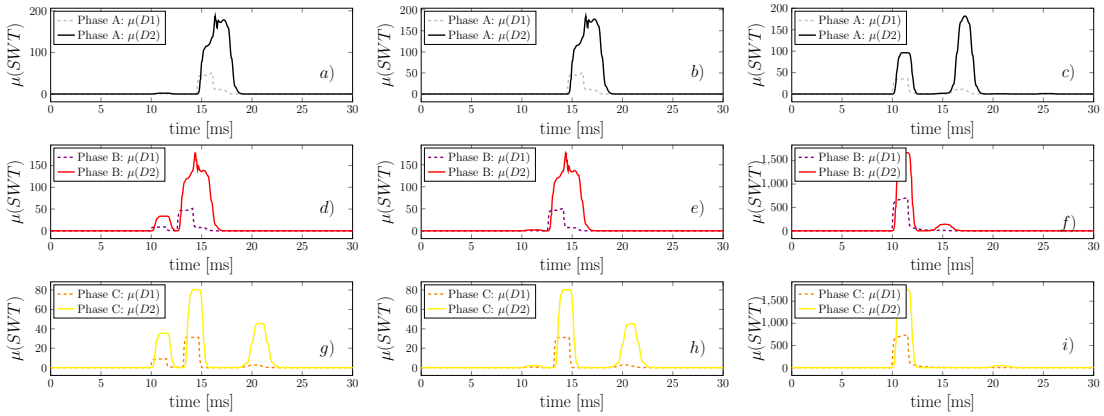

Figure 4.12: Mean of absolute values of the detailed coefficients of decomposition Level 1 and Level 2 for the three phases.

In addition to the identification of unique peaks, the SWT technique allows for the calculation of feature vectors, which are essential for recognising patterns and extracting

useful information. This comprehensive approach improves the overall performance of fault detection and classification elements within the proposed protection schemes. By incorporating the SWT technique, it is possible to develop more robust, accurate, and efficient fault detection and classification mechanisms, ultimately leading to enhanced reliability and stability within the power system infrastructure.

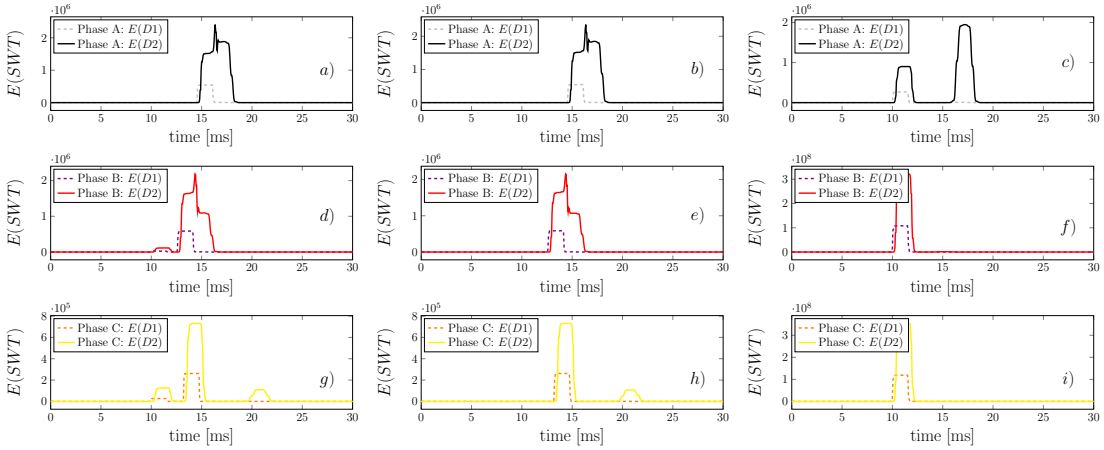

Figure 4.13: Energy of the detailed coefficients of decomposition Level 1 and Level 2 for the three phases.

4.8 Real Time Validation

In this section, the developed protection schemes have been evaluated in terms of their sensitivity against internal faults, stability against external faults and other transient events, and their operational speed. The time performance of the developed schemes has been further assessed against previously unseen scenarios (scenarios which do not belong to the initial dataset and thus are not part of the testing dataset).

The presented studies have been conducted based on a real-time SIL platform. They aim to validate that both schemes can effectively and quickly identify and classify transient events and thus ensure the safe and efficient operation of the power grid with AC SCs and validate the suitability of the algorithms for real-time implementation (i.e., their ability to produce a binary tripping signal in real-time). Additionally, the performance and execution time of the ANN and SVM algorithms have been evaluated using different hardware specifications in order to determine their computational requirements.

4.8.1 Testing environment for real-time validation

A diagram of the testing environment utilised for real-time testing of the proposed schemes is shown in Figure 4.14. A wide range of cases (i.e., internal faults, external faults and load switching events) were simulated using the Simulink-based model depicted in Figure 4.1, and the resulting waveforms were stored externally for post-processing. Such pre-simulated results were loaded on PC-A and were subsequently injected (on a sample-by-sample basis) to PC-B though TCP/IP sockets. The specifications for PC-A and PC-B are shown in Table 4.6.

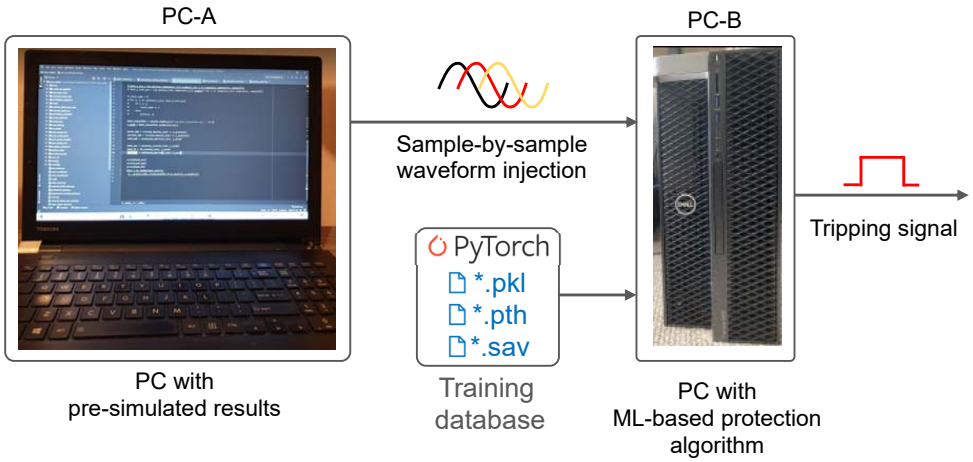

Figure 4.14: Overview of the testing environment.

The developed protection schemes were loaded in PC-B and the training database was also fed to PC-B for complementing the binary classifiers.

Effectively, the developed testing environment forms a real-time SIL platform for validating the proposed protection schemes in terms of their operational speed and capability to provide reliable fault detection and classification, taking into account realistic digital infrastructures.

Table 4.6: PC specifications

PC	Specifications
PC-A	i7-6500U, 2 cores, 4 threads, 2.4 GHz, 4 MB Cache
PC-B	i9-10980XE, 18 cores, 36 threads, 3/4.6 GHz, 24 MB Cache, GPU NVIDIA Quadro RTX 6000

4.8.1.1 Results of the sensitivity and stability assessment of the proposed protection schemes

Figure 4.15, Figure 4.16 and Figure 4.17 present the simulation results of representative test cases, which quantify the overall performance of the developed protection schemes. Effectively, such cases demonstrate the feasibility of the schemes to operate for internal solid and highly-resistive faults and remain stable for external faults and load switching events (in all scenarios, the event is triggered at $t = 10\ ms$).

Figure 4.15 illustrates the system response and the extracted feature vectors under an internal LG solid fault, occurring at 10% of the AC SC's length. For this scenario, only the detailed coefficients and the feature vectors for the faulted phase A are presented.

Figure 4.15a, Figure 4.15b and Figure 4.15c show the phase fault current signatures flowing through the YBCO layer, copper stabiliser layers and former, and the three-phase voltages, respectively. At the time of the fault occurrence at $t = 10\,ms$, the HTS tapes of phase A start to quench, reaching peak values of approximately 25 kA. Once the HTS tapes reach the highly-resistive state, the current is diverted to the copper stabiliser layer and the former (approximately 6 ms after the fault occurrence).

Figure 4.15d, Figure 4.15e and Figure 4.15f illustrate the detailed coefficients of decomposition Level 1 and Level 2 for the current flowing through the YBCO layer, copper stabiliser layers and the former, and the voltage, respectively, for the faulted phase A. As can be seen, the utilisation of the SWT technique aims to identify unique peaks in the fault signatures which indicate the presence of a transient (i.e., fault). The rest of the graphs demonstrate the magnitudes of the features vectors extracted from the current signal flowing through phase A of the SC and the corresponding voltage during the feature extraction stage of the protection schemes' development. In particular, Figure 4.15g, Figure 4.15h, and Figure 4.15i show the magnitude of the sum of absolute values of the detailed coefficients of decomposition Level 1 and Level 2. Figure 4.15j, Figure 4.15k, and Figure 4.15l depict the magnitude of the standard deviation of absolute values of the detailed coefficients of decomposition Level 1 and Level 2. Figure 4.15m, Figure 4.15n, and Figure 4.15o illustrate the magnitude of the mean of the detailed coefficients of decomposition Level 1 and Level 2 and finally, Figure 4.15p, Figure 4.15q, and Figure 4.15r present the magnitude of the energy of the detailed coefficients of decomposition Level 1 and Level 2.

The measurements and feature vectors presented in Figure 4.15 (alongside the ex-

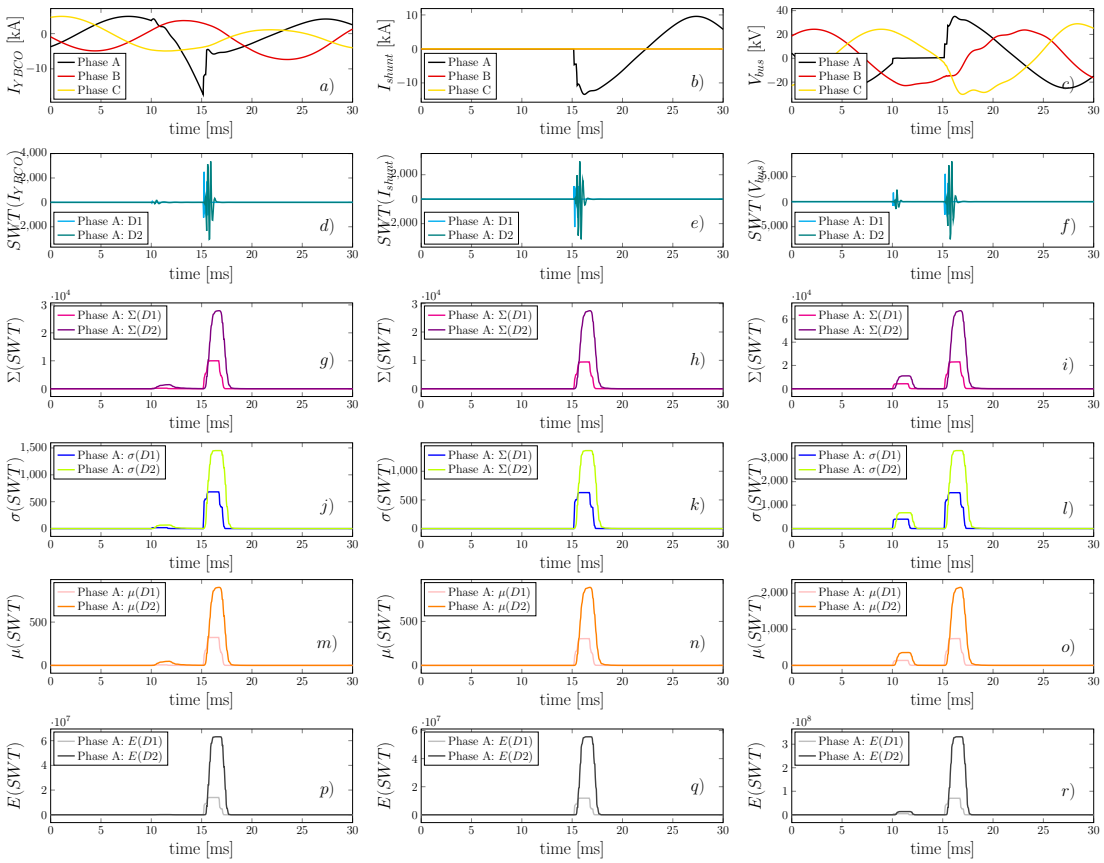

Figure 4.15: Feature vectors resulting from the SWT of the total current flowing through the AC SC for an internal LG solid fault at 10% of the AC SC's length.

tracted feature from the non-faulted phases B and C) were used as inputs to the ANN and SVM algorithms in order to produce a tripping signal, as presented in Figure 4.16.

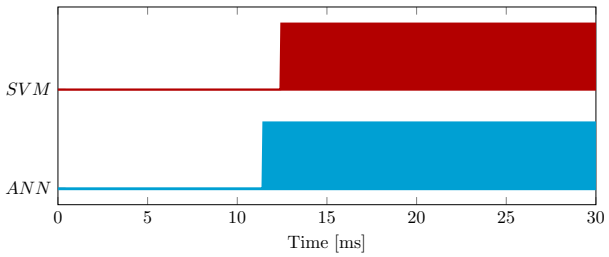

Figure 4.16: Tripping signal initiated by the ANN and SVM algorithms during a LG solid fault at 10% of the AC SC's length.

The produced binary signals confirm the capability of both models to detect and classify correctly the internal fault and initiate a fast tripping signal, validating the sensitivity of the proposed protection schemes. Particularly, the ANN algorithm initiates a tripping signal 1.38 ms after the fault occurrence, while SVM outputs the same signal after 2.45 ms. Therefore, both algorithms produce a fast tripping signal, providing

reliable fault detection and classification and presenting fast operational speed [161]. The total delay between the time instant of the fault occurrence and the initiation of the tripping signal is a sum of the measurement, collection, processing and transmission delays as discussed in Section 4.5.4, emanating from the realistic implementation of the proposed schemes, as well as the time required for the ANN and SVM algorithms to be executed and perform event classification.

For the validation of the discrimination capability of the developed schemes, Figure 4.17 demonstrates the fault current waveforms and the corresponding tripping signal during highly-resistive internal faults, an external fault, and a load switching event. Specifically, an LLL-G fault with fault resistance $R_f = 50\ \Omega$ was applied at 10% of the AC SC's length. The currents flowing through the YBCO layers are depicted in Figure 4.17a for the three phases and the currents of copper stabilisers layers and former in Figure 4.17d. It is evident that during the highly-resistive fault, the current flowing through the YBCO layer is lower than I_C, preventing the AC SC from quenching. Therefore, there is no current sharing between the YBCO, copper stabiliser layer and former, as the fault current is predominately limited by the high value of the fault resistance. It can be observed that highly-resistive faults can be considered the most challenging from a protection perspective because the obtained fault current and voltage signatures closely resemble those of steady-state conditions. Nevertheless, the proposed protection algorithms detect the internal fault and both algorithms produce a tripping signal as illustrated in Figure 4.17g. Specifically, the ANN initiates a tripping signal 1.43 ms after the fault occurrence and the SVM after 3.60 ms. Based on these results, it is evident that both models have been trained well and are able to make accurate predictions, increasing the sensitivity and reliability of the fault detection and classification elements. In this context, it is important to emphasise the significance of the SWT technique. Specifically, the time domain signals shown Figure 4.17a and Figure 4.17d closely resemble those obtained during steady-state conditions, making it challenging to detect quenching events. However, Figure 4.18 displays the resulting SWT transformation of voltage and current signatures during a highly-resistive fault, alongside the corresponding feature vectors. Through the application of SWT, it becomes evident that the appropriate peaks can be extracted, clearly indicating the presence of the fault and eventually enhance the effectiveness of the proposed protection schemes. Therefore, he utilisation of SWT achieves to detect these singularities in the analysed signals. It is worth reitarating, that

other transformation such as Fourier analysis was not chosen as it is not suitable for non-stationary signals [162]. Spectrograms were found to not perform well with ANN and SVM models [128]. Additionally, DWT, as it has already be analysed, was not preferred due to the loss of information at high frequencies resulting from downsampling at every decomposition level.

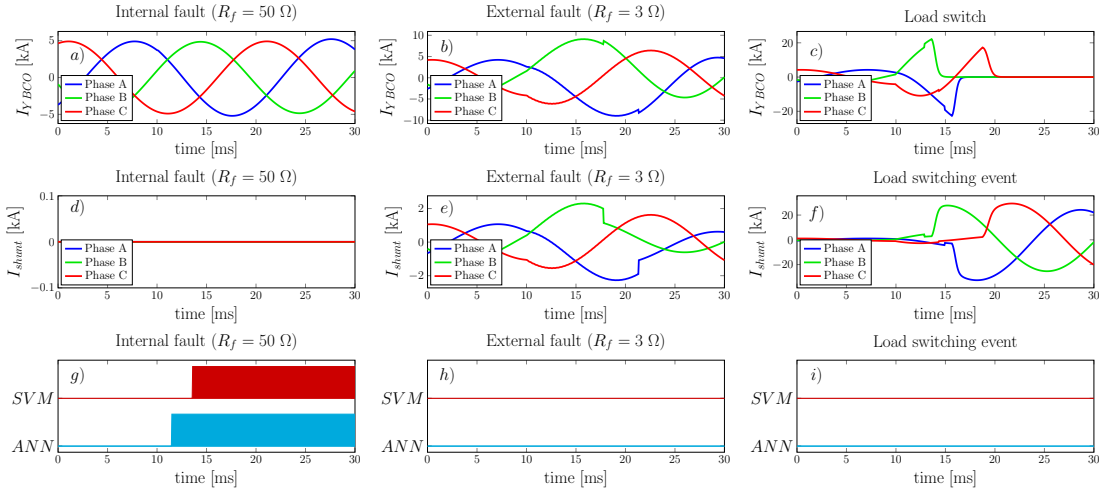

Figure 4.17: Simulation results of ANN/SVM output for internal LLL-G fault with $Rf = 50\ \Omega$ at 90 % of the AC SC's length, external LLL-G fault with $Rf = 3\ \Omega$, and a load switching event.

Figure 4.17b and Figure 4.17c present the current signatures for an LLL-G external fault with $R_f = 3\ \Omega$ applied at the adjacent 132 kV line, and a load switching event at Bus 2, respectively. As opposed to the highly-resistive internal fault, both of such events force the AC SC to quench. Particularly, during the external fault, the current flowing through the YBCO layers of the three phases present a peak of 8.9 kA for phase A, 10.5 kA for phase B, and 9.1 kA for phase C. Within the first 5 ms (Figure 4.17b) and 10 ms after the fault occurrence, the fault current has been diverted to the copper stabiliser layer and the former (Figure 4.17e).

For the load switching event (Figure 4.17c), once the load is connected at Bus 2, the AC SC starts to quench as the current flows through the YBCO layers of the three phases is higher than I_C. At $t = 15\ ms$ the current starts to flow through the copper stabiliser layers and the former (Figure 4.17e) which indicates that the HTS tapes have entered the highly-resistive state. Although the AC SC quenches due to the presence of an external fault and a load switching event, as can be seen from Figure 4.17h and Figure 4.17i, there is no tripping signal initiated for these scenarios. These results justify that the schemes demonstrate a high degree of stability during disturbances such as external faults and

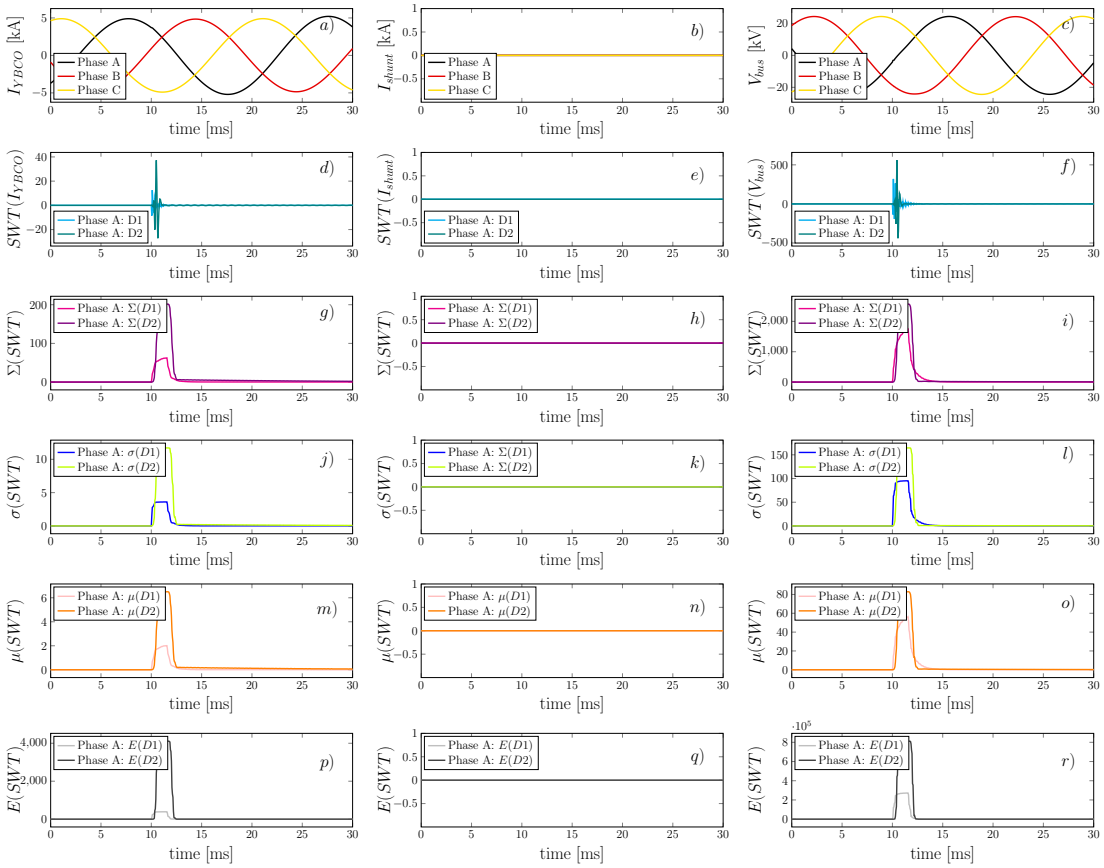

Figure 4.18: Feature vectors resulting from the SWT of the total current flowing through the AC SC for an internal LLL-G highly-resistive fault at 50% of the AC SC's length with $R_f = 50\ \Omega$.

load switching events which cause the quenching of the AC SC.

4.8.1.2 Results of the time performance assessment of the proposed protection schemes

The time performance of the protection schemes has been further tested on additional internal faults, encompassing fault occurrences at various percentages along the SC's length that were not part of the initial dataset. These tests were conducted for all types of faults and R_f up to 300 Ω (for this test R_f values which are not part of the initial dataset have been also considered). It is worth reiterating that such locations were not part of the initial dataset. Practically, this is the foreseen situation as any developed scheme is anticipated to accept inputs not necessarily similar to the trained cases. Some indicative results are presented in Table 4.7 and validate the effectiveness of the proposed schemes, as both are capable of detecting internal faults and initiating the corresponding tripping signal very fast. In terms of the comparison between the two algorithms, it is

noticeable that the ANN appears to initiate the tripping signal in shorter time scales.

Table 4.7: Time performance of developed protection schemes for previously unseen internal faults.

Internal fault			**ANN**	**SVM**	**Internal fault**			**ANN**	**SVM**
Location	Type	Rf [Ω]	Tripping time [ms]	Tripping time [ms]	Location	Type	Rf [Ω]	Tripping time [ms]	Tripping time [ms]
		0	1.507	2.692			0	1.437	3.196
		2	1.443	2.982			2	1.468	2.838
	LLL	13	1.498	2.580		LLL	5	1.439	2.623
		28	1.477	3.077			40	1.521	2.968
		250	1.516	2.791			75	1.519	2.770
		0	1.350	2.701			0	1.445	3.006
		7	1.435	2.701			9	1.487	3.013
	LLLG	18	1.028	2.933		LLLG	30	1.030	2.839
		201	1.480	2.579			43	1.500	3.204
		67	1.764	2.792			72	1.501	2.938
		0.5	1.441	3.133			0	1.440	2.920
		3	1.425	2.890			2	1.450	2.620
5%	LL	6	1.420	2.890	25%	LL	10	1.355	2.764
		215	1.520	3.100			32	1.473	3.077
		100	1.489	3.040			97	1.498	2.805
		0.5	1.476	3.037			0.9	1.461	3.033
		11	1.456	2.872			17	1.431	2.640
	LLG	20	1.471	3.147		LLG	31	1.460	3.009
		112	1.502	2.710			56	1.508	2.863
		98	1.499	3.190			90	1.470	2.850
		0.9	1.438	2.780			0.67	1.411	2.740
		5	1.440	3.210			6	1.462	3.059
	LG	140	1.436	3.067		LG	28	1.442	2.905
		255	1.513	3.099			33	1.488	3.088
		80	1.814	3.048			85	1.519	2.890
		0	1.455	2.877			0.9	1.458	3.167
		1	1.442	3.038			2	1.436	2.605
	LLL	17	1.503	2.673		LLL	8	1.459	3.030
		31	1.506	3.048			17	1.469	3.050
		60	1.487	2.810			85	1.495	3.202
		0	1.453	2.813			0	1.470	3.080
		3	1.447	3.109			2	1.452	2.921
	LLLG	6	1.448	3.005		LLLG	8	1.445	3.048
		140	1.509	3.101			50	1.479	2.630
		190	1.471	2.786			75	1.487	3.077
		0.4	1.427	2.630			0.3	1.455	3.037
		6	1.473	2.771			2	1.456	2.812
15%	LL	16	1.463	2.771	95%	LL	5	1.456	2.828
		270	1.469	3.161			19	1.484	2.980
		60	1.508	3.080			78	1.464	3.110
		0.9	2.210	2.761			0.7	1.460	2.640
		3	1.487	2.670			17	1.411	3.055
	LLG	11	1.790	3.000		LLG	15	1.440	2.875
		175	1.496	3.119			55	1.745	2.890
		100	1.496	2.799			90	1.494	3.190
		0	1.498	2.810			0	1.429	3.191
		6	1.468	3.208			5	1.435	3.179
	LG	122	1.449	2.897		LG	34	1.446	3.011
		67	1.480	2.690			79	1.493	2.680
		188	1.535	2.805			96	1.464	2.990

Specifically, for the ANN algorithm, the time required to produce a binary tripping signal lies within the range of 1.028 ms to 2.21 ms, with an average value of 1.47 ms. For the SVM algorithm, a tripping signal can be initiated within the range of 2.579 ms to 3.63 ms, with an average value of 2.91 ms. Therefore, ANN outperforms SVM with respect to the operation speed. The time performance of the developed schemes were compared with the protection solutions for AC SCs proposed in [96, 163], to demonstrate the superiority of both classifiers in terms of speed of operation, accounting for detection and discrimination. Specifically, the differential current relay proposed in [163] detects the internal faults on the AC SC in 0.86 s, while the differential scheme presented in [96]

detects the faults on the SC in approximately 0.25 s.

4.8.2 Execution of the proposed schemes using different hardware configurations

This subsection presents the feasibility of both the ANN and SVM algorithms to provide fast and precise fault detection and classification under different hardware configurations. Both algorithms have been executed (for the same scenario) at different computers in order to evaluate their execution time in conjunction with the anticipated hardware costs. Table 4.8 demonstrates the computers' hardware specifications.

Table 4.8: PC specifications for hardware sensitivity analysis.

PC	Specifications
PC-1	i7-6500U, 2 cores, 4 threads, 2.4 GHz, 4 MB Cache
PC-2	R7 4800H, 8 cores, 16 threads, 2.9/4.2 GHz, 8 MB Cache, GPU NVIDIA RTX 2060
PC-3	i9-10980XE, 18 cores, 36 threads, 3/4.6 GHz, 24 MB Cache, GPU NVIDIA Quadro RTX 6000

Figure 4.19 presents the execution time for the ANN and SVM algorithms running at different computers. It can be seen that the execution time of ANN is relativity low, compared to that obtained for SVM. Overall, the execution time of both models (considering all the anticipated delays introduced by the real implementation in subsection 4.5.4) is low, providing a high level of confidence that the proposed protection schemes are practical, considering realistic measurements and computation.

Another significant observation from this assessment is that real-time implementation of the proposed schemes can be achieved by relatively low-spec and cheap computers (i.e., PC-1) which could enable their wider adoption. Additionally, the utilisation of high-spec computers (i.e., PC-3) could only result in very small improvements in terms of execution time, which can be considered negligible, especially in the case of the ANN for which the execution time is practically very low.

4.9 Discussion

Two novel AI-based protection schemes have been presented in this chapter which include fault detection and classification elements for the protection of power systems which

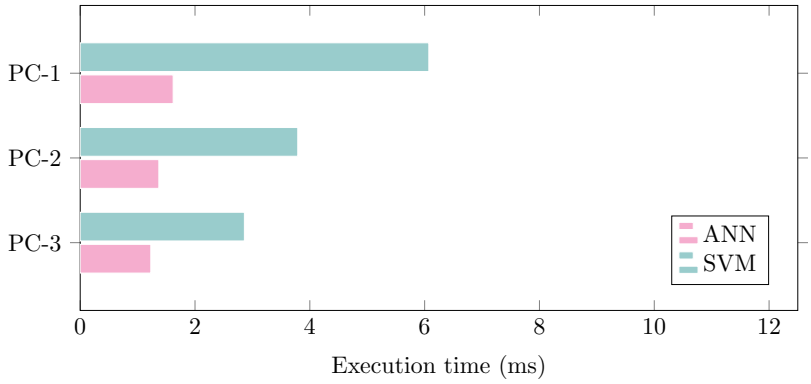

Figure 4.19: Execution time for the ANN and SVM algorithms running in different computers.

incorporate AC SCs. Following the successful evaluation of the proposed schemes, the obtained results revealed that both schemes can provide fast and discriminative fault detection and classification during various fault conditions, including solid and highly-resistive internal faults applied on AC SCs. Specifically, the key points derived are as follows:

- The results indicated that both proposed schemes are highly effective in detecting and classifying internal faults on AC SC systems, while remaining stable against external faults and other disturbances which cause the quenching of AC SCs.
- In terms of real-time performance, it has been found that both schemes were able to run correctly in a SIL testing environment, which simulates realistic digital infrastructures. They were able to initiate fast tripping signals with increased sensitivity against internal faults, highlighting their feasibility for real-time applications. Therefore, both schemes ensure the fast fault detection and classification considering the protection requirements for AC systems [164]. For comparison purposes, the ANN algorithm has demonstrated faster performance than SVM, with an average tripping signal initiation time of 1.47 ms, compared to the 2.91 ms corresponding to SVM.
- Additionally, the sensitivity analysis on different hardware requirements revealed that the proposed schemes can run on low-spec computers, reducing costs and increasing the potential for wider adoption in protecting AC SC systems.

4.10 Summary

In this chapter, the development of two AI-based protection schemes for AC systems with SCs was presented. The proposed schemes incorporate AI classifiers and signal processing techniques for the detection and classification of faults in AC systems. The challenges posed by the transient response of AC SCs, as previously discussed in Chapter 3, were considered for the designing of the proposed schemes.

Initially, a thorough review of reported protection schemes for AC SCs in the literature was carried out. It was found that much of the research conducted in this field is still in its early stages and primarily focused on combining conventional protection solutions such as over-current and differential relays. However, it has been noted that the proposed schemes for AC SCs have not been thoroughly tested in terms of their sensitivity considering challenging cases, such as highly-resistive faults, their discrimination capability against external faults or other events, and their operational speed. These factors are particularly important in light of the challenges posed by the quenching phenomenon and the need for fast fault detection in AC systems. Therefore, there remains a significant research gap in the area of protection for AC SCs and their unresolved issues.

Furthermore, this chapter has discussed the limitations of existing protection solutions when dealing with the transient response of AC SCs. A qualification study was conducted to assess the sensitivity and stability margins of over-current threshold-based solutions for protecting AC SCs. The observations obtained from this analysis highlighted that the utilisation of threshold-based over-current solutions for AC SCs is a trade-off between protection sensitivity and stability.

Additionally, this chapter has presented the benefits offered by AI methods in applied superconductivity and power systems protection applications. It has been found that AI techniques are increasingly being used in applied superconductivity to analyse large sets of data and real-time measurements, leading to a better understanding of the behaviour of such technology and the emergence of a new research field combining AI and superconducting applications. Moreover, it has been found that there is a growing focus on incorporating AI techniques in fault detection and classification tasks in power systems. In particular, the massive advancements in AI and the benefits provided by AI algorithms such as the ability to uncover hidden trends and extract useful information from measurements, render the utilisation of AI assisted protection schemes very promising. This chapter has also presented the advantages and drawbacks of widely

used AI algorithms.

For the development of the proposed schemes signal processing techniques such as SWT and AI classifiers were utilised. Specifically, the first scheme uses an ANN classifier, while the second scheme is based on the SVM algorithm. Initially, the performance of the developed AI algorithms was evaluated using common metrics such as accuracy and the F-1 score. The models with the highest classification capabilities were then integrated into the proposed protection schemes to perform fault detection and classification tasks. Validation tests have been conducted in terms of the sensitivity, stability, and time performance of the proposed schemes. Specifically, detailed transient simulations and a real-time SIL-based testing set-up have been utilised to scrutinise their effectiveness against various scenarios. The results showed that both schemes are characterised by enhanced reliability, superior stability, and high speed of operation. Both schemes operate successfully under highly-resistive faults, which do not lead to quenching of AC SCs, and differentiate them correctly from solid external faults which do cause the quenching of AC SCs. In particular, both classifiers are sensitive against internal faults and remain stable during external faults and load switching events, presenting an accuracy of 98.88 % for the ANN algorithm and 99.44 % for the SVM model. Based on the results, it has been found that the SVM algorithm results in a slightly higher ratio of correct predictions to the total number of predictions compared to the ANN algorithm. Therefore, from a protection perspective, the SVM-based scheme presents higher sensitivity against internal faults and better discrimination capability and stability against external faults and load switching events, ensuring the secure and reliable operation of the grid. The real-time assessment studies also revealed that both schemes initiate the desired tripping signal very fast, during previously unseen scenarios, and are in compliance with AC protection requirements. Specifically, it has been found that the ANN-based protection scheme has higher operational speed by initiating a tripping signal within the range of 1.028 ms to 2.21 ms with an average time of 1.47 ms, while the SVM-based scheme produces the corresponding tripping signal within the range of 2.579 ms to 3.63 ms with an average time of 2.91 ms. Therefore, the real-time SIL testing permits a high level of confidence that the proposed schemes are feasible for real-time protection applications. Furthermore, a sensitivity analysis conducted for different hardware specifications revealed that the proposed schemes eliminate the need for expensive computers, facilitating their practical implementation.

Chapter 5

Fault Location Scheme for SCs in AC Systems

In transmission networks, when a fault occurs on a feeder, protection systems initiate the selective tripping of the corresponding CBs in order to prevent the adverse effects on power system operation. Following fault detection, the precise estimation of the fault location is of paramount importance in order to facilitate rapid restoration of the system and minimise downtime [41]. Specifically, for SCs, fault location is a challenging task due to the unique properties of superconductors. SCs exhibit variable resistance, which has a significant impact on the fault current and voltage signatures, thereby affecting the performance of fault location methods that rely on voltage and current measurements. Furthermore, the accurate estimation of fault location on SCs is crucial due to their complex configuration (i.e., cooling liquid tubes and tapes) [9]. SCs are often buried underground or encased in protective shielding and are composed of multiple layers and parallel strands of superconducting wire, making the inspection and maintenance process difficult. Therefore, fault location on SCs is a crucial and challenging task that requires specialised techniques which shall be adjusted to their specific structure.

This chapter presents the development of a fault location scheme for SCs in AC systems, utilising the transformation of time-domain fault current and voltage measurements to the time-frequency domain, and exploiting the advantages of Convolutional Neural Network (CNN) algorithms to estimate the fault position along SCs. The proposed fault location scheme has been tested using the verified model of an AC SC presented in Chapter 2 and the AC network presented in Chapter 3. The results revealed that the proposed

fault location scheme is able to provide precise fault localisation for a wide range of fault scenarios, including different fault types, fault positions, fault resistance values, and fault inception angles. Furthermore, the robustness of the developed scheme has been verified against different influencing factors, accounting for very small increments of fault location, additive noise, and different values of sampling frequency. For validation purposes, the effectiveness of the CNN-based algorithm has been compared with other data-driven algorithms and the relevant advantages have been highlighted.

5.1 Review of Fault Location Techniques in AC Systems

In recent years, a variety of fault location methods have been reported in the literature, proposing different approaches such as impedance-based methods [165, 166], TW techniques [167–170], time-frequency domain reflectometry [171,172], and sparse measurement techniques [173, 174]. Figure 5.1 quantifies the research trend of fault location schemes for MV AC systems, as reported in the recent literature [175].

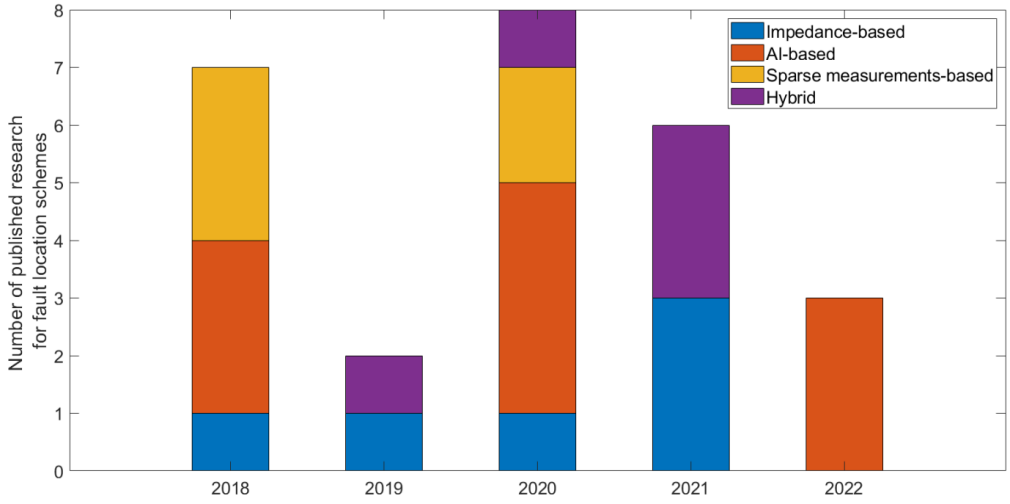

Figure 5.1: Research trend of fault location schemes reported in literature for the last few years.

As it can be inferred from the presented trend, AI is gaining popularity as a means of fault location in power systems, with a considerable number of researchers focusing on developing fault location schemes based on AI. As power systems become more complex, the traditional fault location methods may not be able to handle the increased complexity and uncertainty of power grids. AI algorithms, as discussed in Chapter 4, are particularly well-suited for handling large amounts of data and identifying hidden patterns and correlations. Furthermore, AI-based methods can continuously learn and

adapt to changing conditions in the power system, making them ideal for addressing their dynamic nature. Consequently, in more recent years, the trend of fault location schemes has shifted towards the AI–based and hybrid techniques (techniques which combine conventional methods such as impedance-based methods with AI algorithms) to improve the reliability, efficiency and accuracy of fault location applications.

The following sub-sections present a review of conventional and AI-based fault location schemes that have been proposed in the literature for MV AC systems. The proposed methods are evaluated based on of their accuracy in fault location estimation, robustness to noise, cost, and practical feasibility. Additionally, the potentials and limitations of such methods for AC systems with SCs are thoroughly discussed.

5.1.1 Impedance-based methods

The impedance-based approach is one of the earliest and most widely used techniques in the field of fault location. Impedance-based methods apply Kirchhoff's laws and their operating principles are based on the calculation of overall impedance between the beginning of the line and the faulted point [175]. With respect to input measurements, most studies use the voltage and current phasors for the estimation of fault location. However, [176] presents two alternative approaches, one based solely the fault current phasors and the other using only the current magnitude, with the former resulting in more accurate fault localisation. Moreover, studies conducted in [177] introduce an impedance-based fault location scheme that utilises solely voltage measurements from two points along the line. For this scheme, the placement of the measuring devices is not considered critical, enhancing its suitability for grids with bi-directional power flow. An impedance-based fault location scheme for systems with ICGs is proposed in [178]. The developed scheme calculates the impedance matrix based on pre-fault and during fault voltage and current synchronised measurements obtained from buses and the ICG terminal. The method has been found to be accurate under shunt fault types and addresses the capacitive effect of distribution lines and the bi-directional nature of ICGs. The same approach is proposed in [179], obviating the need for syncrhonised measurements by adopting an iterative load flow algorithm which estimates the unknown synchronisation angle. The direct circuit analysis is implemented by authors in [180] and [181] for the fault localisation of single-phase and phase-to-phase faults, respectively, in three-phase unbalanced systems. The proposed methods employed the matrix inverse

lemma in order to simplify the calculation of the fault location equation. The simulation results validated the effectiveness of the algorithms to precisely estimate the fault location and the robustness to the load uncertainty. However, the verification studies have not considered highly-resistive faults which are rendered the most challenging for fault location problems.

Moreover, there are studies which propose variations of the impedance-based method, including the utilisation of wide-band frequency analysis and Clark's transformation in a distributed parameter line mode [182] and the formation of fifth-order polynomial equations, with a focus on incorporating the capacitive effect into the equations [183]. This effect is explored further in [184], where faults are classified as either ground or line-to-line, and in [185], where the method is tested on an underground cable. In an effort to make the impedance-based method more suitable for active grids and improve accuracy, the golden section technique is suggested as a better analysis tool than the traditional fixed step technique [186].

The impedance-based methods constitute an easy-to-implement fault location solution and present adequate performance against resistive faults. Furthermore, impedance-based methods take into consideration the heterogeneity of the line in their calculations by analysing each section individually [175]. However, such methods are affected by loading conditions during the faults [187], and their applicability for systems with high penetration of ICGs has not been studied extensively. In this context, hybrid fault location methods have started to be investigated which combine the impedance-based techniques with AI tools [188, 189]. With respect to the fault location on SCs, as impedance-based fault location schemes rely on the measurement of electrical impedance in the cable system to determine the location of faults and considering the rapid change in the resistance of SCs during quenching, the accurate determination of the fault location based on impedance-based methods is challenging.

5.1.2 Travelling wave-based methods

TW-based methods have been proven to provide accurate estimation of the fault position along transmission lines by identifying the TW reflections and the time required for the wave to travel to the measuring point. In TW-based methods the fault location is estimated based on measurements acquired either from a single end or from both ends of the faulted circuit. The single-end methods eliminate the need for communication and

synchronisation between devices. The selection of each approach is a trade-off between the cost and the accuracy requirements.

The research conducted in [190] introduces a TW-based fault locator which depends on the first 2 wave arrival times in each line terminal to provide precise fault location estimation. Although there is reduced fault location estimation error under various fault conditions, the method demands sampling frequency within the range of MHz, compromising its feasibility for most commercial devices. A TW-based fault location method which combines the advantages of the DWT and CWT is presented in [191]. Based on the proposed approach, the faulted section is identified utilising the DWT of the synchronised voltage measurements. At the second step, if the identified fault occurs between measuring devices, the exact location is estimated by the DWT, otherwise the CWT is employed. The results showed accurate estimation of the fault location and robust performance against highly-resistive faults. A fault location scheme for hybrid feeders (i.e., overhead and coaxial power cable lines) is developed in [192] based on the use of the Electromagnetic Time-Reversal (EMTR) technique. According to this technique, measurement of the fault-originated electromagnetic transients are acquired from a single observation point, the back injection of the time-reversed recorded signal is simulated and the fault location is estimated trough a trial and error process by changing the fault location and impedance variables. The results validated the accurate fault location estimation, but the effectiveness of the method is based on the assumption that the system topology remains unchanged during the fault. Additionally, authors in [193] propose the construction of appropriate mother wavelets which comply with the admissibility criteria of the CWT. However, the obtained results showed high percentage error in the fault location estimation.

TW-based techniques provide accurate fault location estimation for a variety of fault conditions, independently of the network parameters. However, their implementation is accompanied by the installation of specialised and costly equipment (i.e., sensors, GPS, etc.), utilised for the recording of the transient waves, and usually require high sampling frequency in order to achieve high accuracy on the fault location estimation. Furthermore, the effectiveness of TW-based fault location schemes is affected by the amount of junctions existing between the measuring point and the faulted point, with more junctions resulting in a lower quality of fault signatures and, thus, recorded data. For the case of SCs, there are no reported studies in the literature which investigate

the utilisation of TW-based methods for SCs as current modeling techniques for SCs do not provide the necessary level of detail and granularity to effectively study the TW phenomenon.

5.1.3 Sparse and distributed measurements methods

The increasing penetration of ICG-based technology has created the necessity for continuous network monitoring and installation of sophisticated metering equipment. On that front, extensive research has started to be pursued regarding sparse measurements-based fault location schemes. Such techniques are based on the comparative analysis between actual voltage measurements acquired from multiple points along the network, and simulated voltage signals for all potential fault cases. The fault location is estimated according to the optimal match between the two voltage signals.

A fault-location scheme based on the monitoring capability of smart metering devices and on short-circuit theory is introduced in [194]. The main idea of the developed algorithm is to calculate the bus impedance matrix and the fault current at every bus, utilising voltage measurements before and during the fault occurrence. According to the results, the method can precisely indicate the fault location in most cases, however, the fault location estimation error is not eliminated during resistive faults. A similar methodology is presented in [195] which further addresses the challenge of the multi-source unbalanced nature of RES within the system. However, the main drawback of the proposed method stems from the need of synchronised voltage and current measurements from each generating unit and substation, increasing the cost dramatically. Many reported methods employ Intelligent Electronic Devices (IEDs) for the measurements acquisition [196–198]. Authors in [198] reduce the number of IEDs by proposing a fault location method based on the virtual nodal injection of negative sequence current and the Bayesian Compressive Sensing (BCS) theory. The method has been found to successfully locate the fault under the influence of many adverse factors (i.e., fault resistance, noise, bi-directional flows), however its effectiveness has been confirmed only for asymmetrical faults.

Fault location techniques based on sparse-measurements establish a simple and fast fault location solution which address the effect of RES. However, the influence of the monitoring devices distribution on the fault location accuracy is the major challenge of these methods. Insufficient and low cost devices lead to a compromise of fault location

scheme accuracy and applicability. In this context, many researchers have started to investigate optimisation methods for the device allocation with minimum cost [199] and combine sparse measurements with other methods such as the work conducted in [200, 201]. However, these methods require complex calculations and increase the difficulty in the implementation. An important prerequisite for the wider adoption of such methods is to overcome the high cost of required hardware and the computational burden. Therefore, considering the aforementioned drawbacks of sparse measurements fault location methods, they are not considered an adequate solution for MV systems with SCs.

5.1.4 Reflectometry

Reflectometry-based fault location techniques identify the characteristics of electrical lines by monitoring reflected waveforms. The utilised measurements in such methods can be in frequency or time-domain [202]. The main idea of reflectometry is to inject a low-voltage, high frequency signal to the faulted line and estimate the fault location with respect to the detected response (i.e., resulting current and voltage waveforms). An inductive directional coupling Spread Spectrum Time Domain Reflectometry (SSTDR) system is proposed in [171] for the fault location along power cables. The method incorporates a signal generator for the injection of the high frequency reference signal into the cable. A detection device captures the reference signal along with the reflected signal and estimates the fault location by calculating their cross correlation. The method has been verified experimentally, utilising a section of test cable and the results showed effective accurate fault location estimation.

Furthermore, a few reflectometry-based methods are reported in the technical literature for fault location estimation on SCs. Specifically, a time-frequency domain reflectometry has been reported in the literature for the real-time abnormality diagnosis (i.e, fault detection and fault location) of SCs [203]. However, the proposed scheme requires the addition of measuring components necessary to measure independently the reflected signals generated by each phase, resulting in higher cost. Furthermore, validation studies do not consider the dynamically changing impedance of the layers of SCs during quenching. Additionally, authors in [204] propose a Stepped Frequency Wave Reflectometry (SFWR) method for the identification of the fault location in joints, dielectric, and other SC parts. The cable under-test is a single-phase 22.9 $kV/50$ MVA

SC with length of 7 m. The resulting fault location estimation error is approximately 4.55%, while the proposed method has not been scrutinised against a variety of fault conditions, accounting for different fault types, locations, or highly-resistive faults. The same authors investigate the challenge of the fault localisation on SCs in [205], by applying a fundamental Time–Frequency Domain Reflectometry (TFDR) approach on a similar prototype SC with length of 7 m. The accuracy of the fault location identification is increased. However, the fault location estimation error is affected by the SC temperature and the performance of the developed method has not been confirmed for a wide range of fault scenarios. An improved TFDR method incorporated with filter-Ensemble Empirical Mode Decomposition (EEMD) noise reduction is presented in [206] for a 50 m three-phase SC. The obtained fault location estimation error is approximately 0.01%. Nevertheless, the conducted work considered only the case of a solid three-phase fault.

Despite the accurate estimation of the fault location, the need for external equipment and high sampling rates can be taken as drawbacks of these methods. The reflectometry-based schemes require external equipment (i.e., signal generator, fault recorder), constituting an expensive fault location solution.

5.1.5 AI-based methods

In response to the challenges posed by changes in power grids, the energy sector has sought more advanced approaches to fault management, taking into account both the physical infrastructure and the information layer. To that end, data-driven AI techniques have gained popularity due to their ability to uncover quantities that are not easily observable through direct measurements and to extract patterns from available data.

Relevant deployment of AI technology for fault location applications include the utilisation of CNNs [207], LSTMs [208], SVM [209], Tree-based techniques such as RF [210, 211], and XGBOOST regressors [212]. Furthermore, by taking advantage of tangible benefits provided by AI techniques, many hybrid fault location schemes have been proposed in the technical literature which are based on the combination between feature extraction techniques, such as the WT, to extract useful insight from the acquired measurements and AI algorithms to perform learning-based estimation of the fault location [213]. Additionally, besides the WT, there are other types of transformations used with AI models. One commonly used is the Clark–Concordia transformation [214, 215]. Furthermore, many researchers propose hybrid techniques that

combine the advantages of different AI algorithms. Indicatively, in [131] the combination of SVM and ANN algorithms has been presented, where the SVM classifier is utilised for the fault type classification and the ANN regressor for the estimation of the fault location. All these hybrid AI-based fault location methods provide high fault location accuracy and are robust against a variety of fault conditions. However, most of the reported methods have been evaluated based only on the testing dataset and do not consider previously unseen scenarios out of the initial dataset for the validation of the algorithm generalisation capability.

Additionally, the enhancement of conventional fault location methods performance with pattern recognition techniques has started to gain increasing interest in the literature [216]. One of the widely used pattern recognition techniques is image analysis which has a plethora of interesting features for power system applications and is considered an important field within AI. Based on the image analysis techniques, the images are converted into binary format in order to be digitally processed and analysed for the extraction of the useful information [217]. The image analysis technique has several advantages for feature extraction in power systems that can be utilised to perform accurate fault location. Specifically, for power system applications, image analysis techniques can be utilised as powerful tools to extract crucial features related to the power system conditions based on historical data, eliminating the need for expensive phasor synchronous measurements equipment. Image analysis techniques present high-dimensional data in a compact form, making it easier to identify patterns and features, reduce the data size and computational complexity by compressing the signals, and can be combined with AI algorithms to improve the accuracy of feature extraction, regression, and classification problems. The most powerful algorithm for image processing is the CNN [218]. CNNs have been widely used in image analysis tasks like Image recognition, Object detection, and Segmentation [219], [220], [221] as they present increased capability to extract spatial features on the analysed images (i.e., spatial features refers to the arrangement of pixels and the relations among them). However, there is a very limited number of publications for fault location problems which exploit the potential of image analysis [222].

AI fault location schemes may face difficulties regarding data availability and computational requirements. To address these challenges, appropriate data pre-processing and feature selection or dimensionality reduction techniques can be adopted to reduce the need for large volumes of training data [212]. As the fault location on SCs can be

considered a difficult task with increased complexity, AI-based techniques present great potential for addressing this challenge.

5.1.6 Assessment of review

This literature review of various fault location methods highlighted that the key factors contributing to a reliable fault location scheme are the increased accuracy, reduced complexity, lower cost, and reduced computational burden. Table 5.1 demonstrates a comparison of different fault location methods in terms of their features, such as accuracy, cost, robustness against noise, and practical feasibility (i.e., ease of implementation, required equipment, computational power). A desirable fault location scheme should possess high accuracy, high robustness against noise, high practical feasibility, and low cost.

As power systems evolve, methods such as the impedance-based schemes confront the problem of accuracy, especially for complex system topologies. To compensate for this, other methods, such as TW-based schemes and sparse-measurement-based methods are employed, but these methods increase the cost and reduce practical feasibility due to the need for synchronised measurements and expensive equipment. Overall, the adoption of AI-based methods has started to be considered the best alternative in fault location applications, presenting unique advantages which outweigh the challenges of the conventional methods. Based on the literature review and summarising Table 5.1, AI-based methods constitute the best trade-off between accuracy, cost and practical feasibility. AI fault location schemes present increased learning capabilities which can lead to accurate fault location estimation, do not require expensive equipment, and do not present complexity in terms of their implementation.

Table 5.1: Comparison of different features of fault location schemes.

Method	**Accuracy**	**Cost**	**Noise robustness**	**Practical feasibility**
TW	high	high	medium	low
AI	high	low	high	medium
Impedance	low	low	medium	high
Sparse meas.	high	high	medium	low

Furthermore, the conducted review revealed that despite the abundance of the proposed fault location schemes in the literature, the fault localisation on AC SCs has not been extensively studied [9]. Particularly, for the case of SCs, the precise identification of fault location is very important considering their complex configuration (i.e., cooling

liquid tubes, tapes, etc.). Initially it has been highlighted that even though all the reported methods have their own advantageous features, their applicability is limited when it comes to SCs due to the unique electro-magneto-thermal properties of HTS tapes and quenching. There is a limited number of studies based on the reflectometry approaches for the fault localisation on SCs. However, the proposed methods have not been validated for multiple fault conditions (i.e., various fault locations along the SC, highly-resistive faults), SCs with longer length, and other factors which affect the accurate estimation of the fault position such as the noisy measurements.

Driven by this research gap, this chapter proposes a fault location method for AC MV systems with SCs. Considering the recent advancements in AI, and the limitations of conventional methods, the developed fault location scheme constitutes a data-driven method which forms the fault location estimation on AC SCs to a regression problem, utilising AI techniques and powerful feature extraction tools such as image analysis. The detailed methodology for the development of the proposed scheme will be presented in the following sections.

5.2 Development of the Proposed Fault Location Scheme

This section presents the development of a novel data-driven scheme for fault localisation in power grids which incorporate AC SCs. The operating principles of the developed fault location scheme are based on the combination of image analysis techniques with AI tools which are deployed to estimate the fault location along the length of the AC SC. Specifically, the proposed scheme exploits the advantages of CNNs to estimate the fault position along AC SC's length. The operation of the proposed fault location scheme is based on single-ended current and voltage measurements from one terminal of the AC SC, which are available locally from the measuring equipment, eliminating the need for synchronised measurements from both ends. Implementing a single-end scheme is often more practical and cost-effective in real-world applications as it is less complex in terms of hardware and data gathering. The acquired measurements are transformed from time-domain to time-frequency domain as part of the feature extraction stage. The development of the proposed fault location scheme has been performed in distinct stages which are analysed in the subsequent subsections.

5.2.1 Stages of the proposed fault location scheme

The 4-stages of the development of the fault location scheme are illustrated in Figure 5.2. To aid the clarity of the description, a scenario of an LLL-G solid fault, at 50% along the AC SC's length, is utilised.

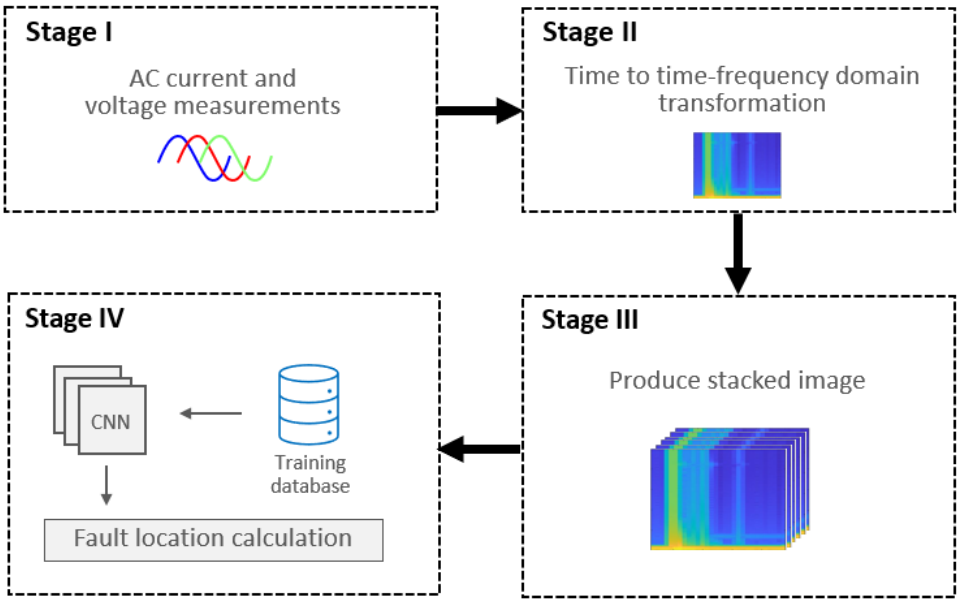

Figure 5.2: Flowchart of the development process of the CNN-based fault location scheme.

5.2.1.1 Stage I - Signal acquisition

Measurements of three-phase voltages and currents from one end of the AC SC are captured with sampling frequency of 20 kHz (the investigation of different sampling frequency values will be presented in subsection 5.4.4). In these studies it has been assumed that 5 cycles (1 pre-fault cycle, to avoid fluctuations and overlap of the pre-fault and during fault data, and 4 during the fault cycles) of data would be more than adequate for this application [223]. The recorded data are filtered via low pass anti-aliasing filters as per the Nyquist criterion, normalised and packaged into appropriate time windows to be processed for spectral analysis at the following stage of the algorithm. For the development of the fault location scheme the same model developed in Chapter 3 and depicted in Figure 5.3 has been utilised.

Figure 5.4 shows the filtered time-domain fault current and voltage traces for the tested fault case which represent the measurements utilised for the operation of the developed fault location scheme. The fault occurs at $t = 3.06$ s. Figure 5.4a shows 1

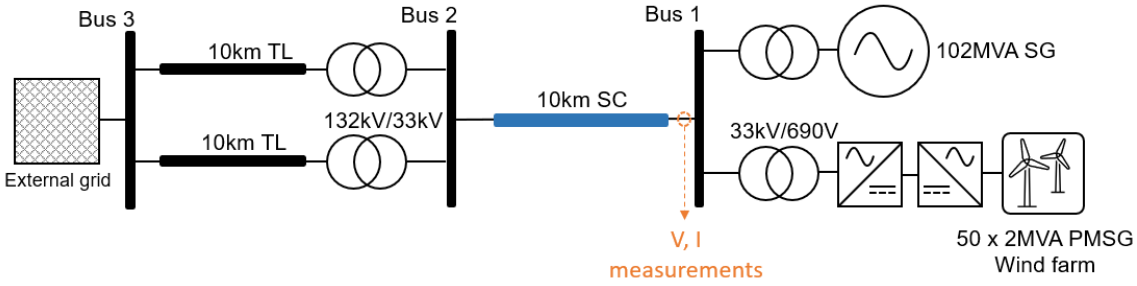

Figure 5.3: Tested AC network incorporating SC and a fault location scheme deployed at Bus 1.

pre-fault cycle and 4 during fault cycles of the total current flowing through the SC and Figure 5.4b demonstrates the voltage obtained at Bus 1.

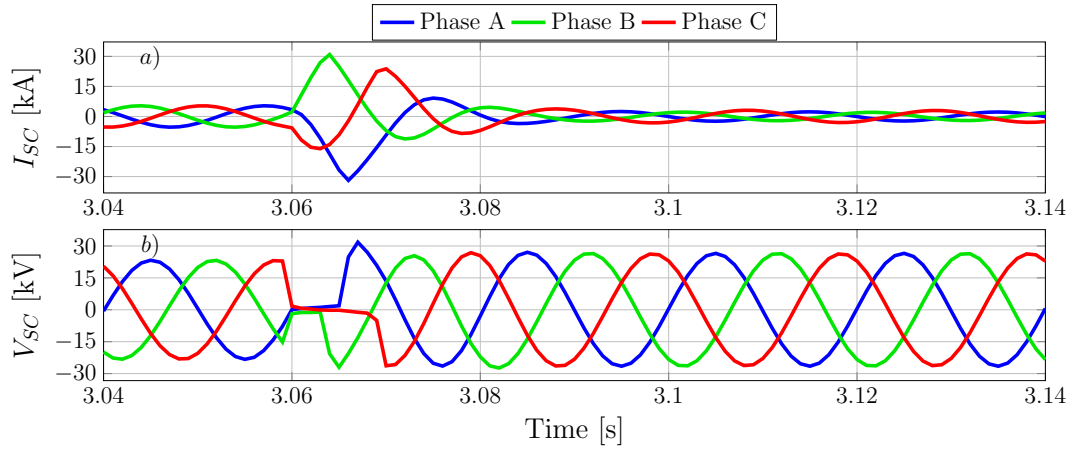

Figure 5.4: Voltage and current signatures during an LLL-G solid fault at 50% of the AC SC's length: a) three-phase currents, b) three-phase voltages.

5.2.1.2 Stage II - Signal to image transformation

At this stage, the time-domain signals (i.e., voltages and currents) are transformed to time-frequency domain in order to produce $2D$ images. Specifically, the fault current and voltage signatures, are utilised to produce the corresponding spectrograms, which are plotted within a time-frequency plane. Considering the advantages of image transformation discussed in 5.1.5, this method has been selected as a powerful feature extraction tool.

To compute the time-dependent spectrum, the non-stationary signal is divided into shorter segments of equal length. The length of each segment specifies the time resolution and must be smaller or equal to the signal duration. After relevant studies it has been found that image analysis provides better results for that specific problem when each

signal is divided into 8 segments of 250 samples each, with 50 samples overlap. A window-based Short-Time Fourier Transform (STFT) is applied on each segment to compute the corresponding spectrum [224]. Finally, the segments spectra are concatenated to construct the spectrogram [224], which enables the localisation of frequency in time, by means of a magnitude-dependent colormap. The STFT of a non-stationary signal, using a window function $c(t)$ which is centred at $t = \tau$, is given by (5.1). Furthermore, Figure 5.5 shows the spectrograms derived from the three-phase currents and voltages of Figure 5.4.

$$STFT(\tau, f) = \int y(t) \cdot c(t - \tau) \cdot e^{-i2\pi ft} dt \tag{5.1}$$

where $y(t)$ is the time-domain signal and f is the frequency.

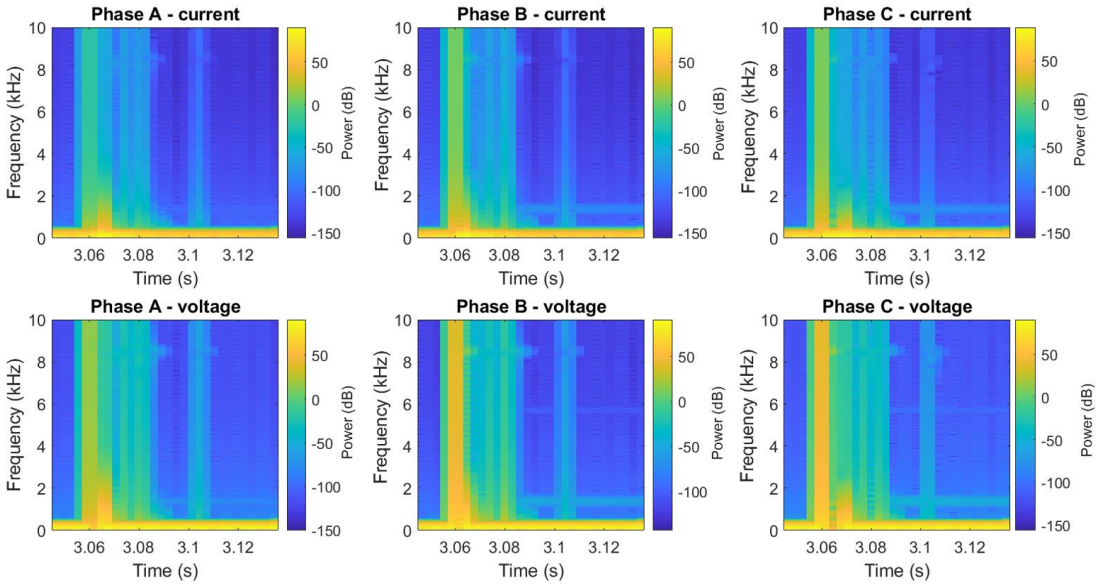

Figure 5.5: Current and voltage spectograms for an LLL-G solid fault at 50% of the AC SC's length.

5.2.1.3 Stage III - Image pre-processing

The resulting spectrograms with dimension $(H \times W)$, where H is the height and W is the width of the image, are stacked together to form a multi-layer image with dimensions $(L \times H \times W)$. Parameter L denotes the number of over-layered spectrograms which corresponds to $L = 6$ in this application. The resulting stacked image will be used as input to the AI model at the following stage. Figure 5.6 shows a stacked image stemming from the over-laying of the spectrograms produced by the three-phase current

and three-phase voltage signatures depicted in Figure 5.5. Image stacking is used in image analysis techniques to combine multiple images in order to capture more information, reduce the data load and thus computational effort, and increase the generalisation capability of the AI model [225]. For clarity, the sequence of stacking the voltage and current spectrograms has no impact on the performance of the developed scheme.

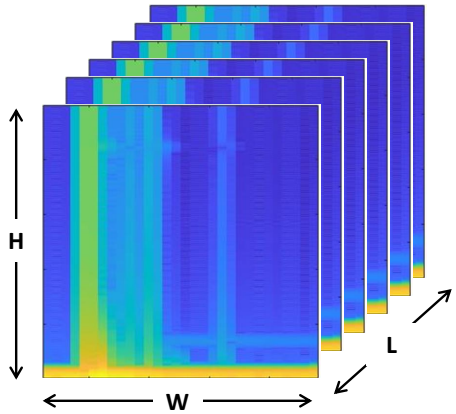

Figure 5.6: Stacked image composed of 3 current and 3 voltage spectrograms.

5.2.1.4 Stage IV - Estimation of fault location

At the final stage of the development process the fault location is estimated. The stacked images for all the fault scenarios are utilised as inputs to the AI-based network. The fault localisation on the AC SC has been formed as a regression problem where the AI network provides the value of the estimated fault location at its output.

A comprehensive analysis of different AI-based networks has been conducted and eventually the results revealed that CNNs are the most robust and effective algorithms for image processing. Furthermore, the motivation of utilising a CNN algorithm is their ability to capture sequence patterns in the input data.

Specifically, a CNN is a type of ANNs which presents outstanding performance when dealing with image analysis tasks. CNNs combines the ability of feature extraction and pattern recognition and is capable of preserving the spatial or positional relationships between input data points. Therefore, CNNs have have been widely applied to power systems applications for fault management [207,226,227]. Typically, a CNN is constructed by an input layer, a series of convolution layers with filters (kernels), pooling, and Fully Connected (FC) layers.

The convolution layer is utilised to extract local features of the input images, by

applying the convolution operation. In principle, the convolution operation is a linear operation of multiplication and addition of convolution filters (kernels) with the corresponding elements of the input feature map. The first convolution layer is utilised for the extraction of low-level features of the input images, accounting for image edges and gradient orientation. The addition of more convolution layers aims to capture high-level features are captured providing an overall understanding of the input images. The convolution operation is depicted in Figure 5.7.

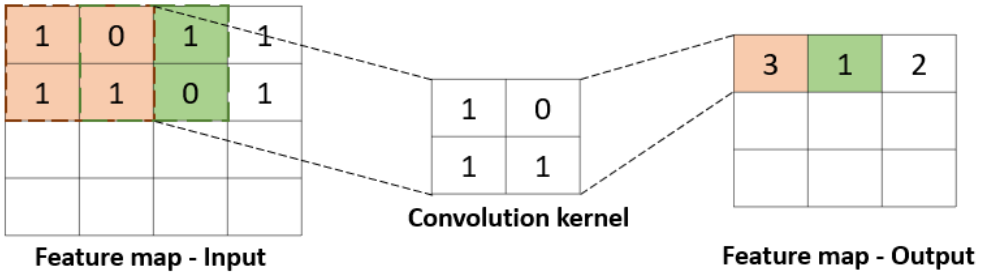

Figure 5.7: Overview of the convolution operation.

If the input data are formed to matrix $n \times n$ and the convolution kernel is $k \times k$, the output is an $m \times m$ matrix. The dimensional relation of the matrices is given by (5.2) [228]:

$$m = n - k + 1 \tag{5.2}$$

The convolution operation is based on the formula described in (5.3):

$$Y_o^l = f(\sum_{i \in m} Y_o^{l-1} \cdot K_{io}^l + b^l) \tag{5.3}$$

where Y_o^l denotes the output of the $l - th$ layer; Y_o^{l-1} is the input of the $l - th$ layer; B is the offset; K denotes the kernel element; and f is the activation function. In the presented research ReLU has been selected as the activation function for the convolution layers.

The purpose of the pooling layer is to scale data from the previous layer (subsampling of convolution layer), reduce the data dimension, and consequently reduce the computation time and prevent over-fitting [222]. Figure 5.8 illustrates the pooling process.

There are two groups of pooling models used in CNNs which are known as the average model and the maximum model. The average pooling model returns the average value of the feature map portion covered by the convolution kernel and its operation is expressed

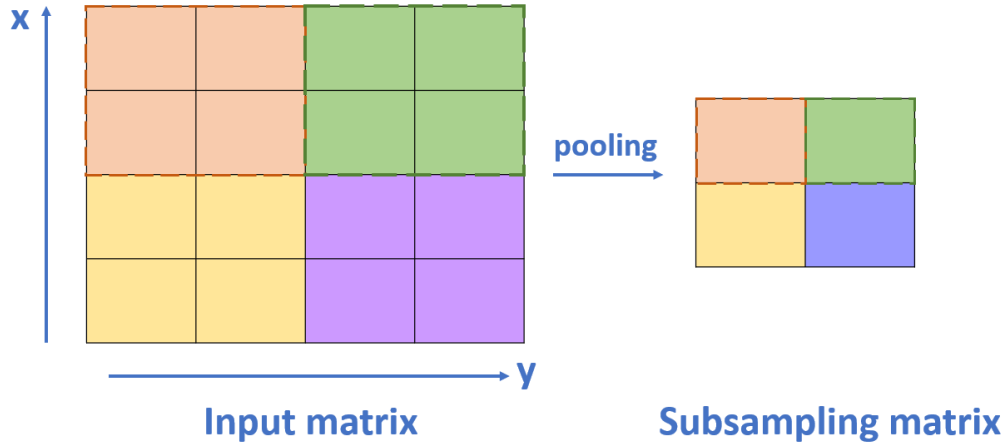

Figure 5.8: Pooling process in CNN model.

according to (5.4) [226], while the maximum pooling model calculates the maximum value of the feature map portion covered by the convolution kernel and its operation is described by (5.5) [226].

$$S_{ij} = \frac{1}{d^2}(\sum_{i=1}^{d}\sum_{j=1}^{d} F_{ij}) + b \tag{5.4}$$

$$S_{ij} = \max_{i=1,j=1}^{d}(F_{ij}) + b \tag{5.5}$$

where F denotes the input feature map, b is the bias parameter, d is the dimension of the pooling matrix, and S is the calculated subsampling matrix after the pooling process.

The proper pooling model for an image analysis problem should be selected by considering the specific features of the images (i.e., size and scale of objects in the image, presence of strong edges, and level of noise) [229]. In the presented work the max pooling model has been utilised because it tends to perform better in problems where the features are highly localised, with distinctive peaks and thus max pooling can effectively identify the maximum values in the spectrograms.

The output of the convolution and pooling layer is fed into a linear fully connected feed forward layer, where the associated activation function provides the desirable output. The output of the CNN model is the predicted fault location C_F, with the error of the fault localisation calculated according to (5.6):

$$error_{FL}[\%] = \left|\frac{C_F - A.C_F}{L_{SC}}\right| \cdot 100(\%) \tag{5.6}$$

where $A.C_F$ is the actual fault location and L_{SC} is the total length of the SC.

5.3 Selection of CNN Model

One of the main factors which determine the accuracy of the fault location scheme is the architecture of the utilised CNN model. On that front, several well-known CNN architectures, proposed by the computer vision community, have been evaluated in order to select the one which provides the most accurate fault location estimation [230]. An iterative simulation-based fault analysis was conducted in order to acquire the voltage and current measurements considering the system presented in Figure 5.3 and different fault types accounting for LLL, LLL-G, LL, LL-G and L-G, different values of R_f, (within the range of 0 Ω up to 300 Ω), and varying fault position (fault location with an increment of 10 % of the AC SC's length). The captured voltage and current fault signatures measured at Bus 1 (Figure 5.3) were utilised to produce the corresponding spectrograms and create the training data base.

For data pre-processing, the PyTorch open source ML library has been utilised. Consequently, a dataset of 1750 transient events has been created, from which 60% was used to train the CNN models, 20% was used for validation purposes, and the remaining 20% were used for testing purposes.

For the selection of i) the optimum hyperparameters, accounting for the batch size and the learning rate, and ii) the best training model of each CNN model, the GS 5-fold CV technique has been adopted to result in a CNN model with the best performance and reduce over-fitting on the training data (the process of the GS 5-fold CV technique has been explained in Chapter 4). For the selection of the CNN model hyperparameters, the mean fault location estimation error has been considered as a 5-fold CV score and it is given by (5.7):

$$\overline{error}_{FL}[\%] = \frac{1}{N}\sum_{i=0}^{N} |(\frac{\hat{y_i} - y_i}{L_{SC}})| \cdot 100(\%) \tag{5.7}$$

where $\hat{y_i}$ corresponds to the estimated fault location, y_i denotes the actual fault location, and N is the total number of data points.

The CNN models have been trained by the back propagation gradient descent method and the Adam optimiser has been utilised as the optimisation algorithm. The final trained CNN models (with the best combination of hyperparameters) were tested on the testing dataset, utilising again the mean fault location estimation error, $\overline{error}_{FL}$, as the

evaluation metric. For each CNN model, the combination which results in the lowest $\overline{error}_{FL}$ for the testing dataset has been selected. The obtained results are presented in Table 5.2.

Table 5.2: Tested CNN models and their performance on the testing dataset

CNN model	$\overline{\textbf{error}}_{\textbf{FL}}(\%)$
Inception-v3	0.74
ResNet50	3.16
ResNet101	2.76
ResNet152	3.02
Densenet	4.20
VGG11	0.97
VGG13	1.25
VGG16	0.88
VGG19	0.98

It is worth highlighting that the Inception-v3 CNN model with the following hyper-parameters: batch size = 4, learning rate = 0.001, presented the lowest $\overline{error}_{FL}$ and subsequently was selected as the best CNN model.

The layers of the Inception-v3 model are demonstrated in Table 5.3, along with the input size of each layer. The input image is 510×580 with 6 channels which correspond to the number of spectrograms (three-phase currents and three-phase voltages). At the output of the developed CNN model there is a fully-connected layer which yields the numerical value of the predicted fault location as a percentage of the AC SC length.

Table 5.3: The outline of the proposed CNN model

Layer type	**Input size**
conv	$510 \times 580 \times 6$
conv	$254 \times 289 \times 32$
con padded	$252 \times 287 \times 32$
pool	$252 \times 287 \times 64$
conv	$125 \times 143 \times 64$
conv	$123 \times 141 \times 80$
conv	$61 \times 70 \times 192$
3× Inception	$61 \times 70 \times 288$
5× Inception	$30 \times 34 \times 768$
2× Inception	$14 \times 16 \times 1280$
pool	$14 \times 16 \times 2048$
fully-connected	$1 \times 1 \times 2048$

5.4 Simulation Results and Validation

To examine the accuracy of the proposed fault location scheme, its performance has been evaluated under the occurrence of different fault scenarios. Furthermore, the impact of R_f, small increments of fault location, different fault inception angles, noise, and sampling frequency on the effectiveness of the proposed scheme has been investigated. The simulation-based results are analysed in the following subsections.

5.4.1 Fault location results

To achieve an overall performance assessment of the proposed scheme, its fault location estimation capability was evaluated based on additional faults, which have not been distributed equally along the AC SC length in contrary to the scenarios included in the initial dataset. Furthermore, fault resistance values up to 300 Ω have been investigated (for this test R_f values which are not part of the initial dataset have been also considered). The purpose for this is that any fault location scheme must present increased generalisation capability and be able to provide accurate fault location estimation with inputs not necessarily similar to the training dataset. Table 5.4 shows the results of the fault location estimation by presenting the values of the actual fault location, the predicted fault location produced at the CNN output, and the derived $error_{FL}$ calculated by (5.6).

The results validate the effectiveness of the proposed scheme. Specifically, the lowest $error_{FL}$ is 0.01%, the maximum error is 1.18% and the mean error, $\overline{error}_{FL}$, of all scenarios in Table 5.4 is 0.34%. It is important to highlight that the developed fault location scheme achieves accurate fault location estimation even in the case of close-up faults (i.e, faults occurring close to the head or end of the AC SC) and under the influence of highly-resistive faults.

Furthermore, Figure 5.9 presents the performance of the proposed fault location scheme under the influence of LLL-G faults occurred at every 5% of the SC's length for different values of R_f. The sensitivity analysis with respect to SC's length shows that the $error_{FL}$ lies within the range of 0.009% and 1.108% and consequently verifies the increased accuracy in fault location estimation.

Table 5.4: Fault location $error_{FL}$ for the CNN-based fault location scheme.

Fault type	R_f (Ω)	$A.C_F$ (km)	C_F (km)	error$_F$L (%)	Fault type	R_f (Ω)	$A.C_F$ (km)	C_F (km)	error$_F$L (%)	Fault type	R_f (Ω)	$A.C_F$ (km)	C_F (km)	error$_F$L (%)
LLL-G	0	0.4	0.36	0.4	LLL	0	0.52	0.559	0.39	LL-G	0	7.8	7.9	1
LLL-G	0	2.2	2.212	0.12	LLL	0	2.39	2.397	0.07	LL-G	0	2.4	2.48	0.8
LLL-G	0	8.7	8.62	0.8	LLL	0	7.76	7.77	0.1	LL-G	0	2.6	2.62	0.2
LLL-G	0	9.96	9.961	0.01	LLL	0	6.6	6.622	0.22	LL-G	0	8.95	8.915	0.35
LLL-G	2	5.2	5.31	1.1	LLL	2	3.13	3.149	0.19	LL-G	2	9.97	9.865	1.05
LLL-G	2	8.4	8.41	0.1	LLL	2	7.14	7.112	0.28	LL-G	2	0.91	0.816	0.94
LLL-G	5	8.7	8.72	0.2	LLL	5	9.9	9.908	0.08	LL-G	5	6.3	6.29	0.1
LLL-G	5	2.1	1.998	0.2	LLL	5	7.97	7.915	0.55	LL-G	5	0.9	0.815	0.85
LLL-G	15	3.6	3.69	0.9	LLL	15	4.99	5.1	1.1	LL-G	15	1.8	1.75	0.5
LLL-G	15	4.2	4.25	0.5	LLL	15	8.37	8.35	0.2	LL-G	15	2.71	2.627	0.83
LLL-G	200	3	3.009	0.09	LLL	200	2.48	2.448	0.32	LL-G	200	1.61	1.54	0.7
LLL-G	200	9.2	9.221	0.21	LLL	200	5.98	5.978	0.02	LL-G	200	9.52	9.487	0.33
LLL-G	250	9.98	9.981	0.01	LLL	250	9.13	9.161	0.31	LL-G	250	4.48	4.592	1.12
LLL-G	250	0.98	9.923	0.57	LLL	250	2.99	3.05	0.6	LL-G	250	1.13	1.098	0.32
LLL-G	300	0.14	0.146	0.06	LLL	300	0.45	0.454	0.04	LL-G	300	0.02	0.024	0.04
LLL-G	300	6.17	6.156	0.14	LLL	300	4.32	4.441	0.9	LL-G	300	8.92	8.941	0.21
Fault type	R_f (Ω)	$A.C_F$ (km)	C_F (km)	error$_F$L (%)	**Fault type**	R_f (Ω)	$A.C_F$ (km)	C_F (km)	error$_F$L (%)					
LL	0	1.64	1.644	0.04	L-G	0	6.9	6.924	0.24					
LL	0	2.67	2.648	0.22	L-G	0	1.81	1.79	0.2					
LL	0	7.45	7.464	0.14	L-G	0	2.7	2.68	0.2					
LL	0	9.39	9.393	0.03	L-G	0	3.33	3.324	0.06					
LL	2	6.49	6.46	0.3	L-G	2	2.25	2.264	0.14					
LL	2	8.15	8.151	0.01	L-G	2	5.5	5.618	1.18					
LL	5	9.21	9.131	0.79	L-G	5	6.38	6.37	0.1					
LL	5	5.14	5.141	0.01	L-G	5	7.31	7.23	0.8					
LL	15	4.29	4.275	0.15	L-G	15	9.79	9.781	0.09					
LL	15	7.11	7.116	0.06	L-G	15	1.11	1.09	0.2					
LL	200	0.71	0.693	0.17	L-G	200	4.4	4.418	0.18					
LL	200	9.54	9.561	0.21	L-G	200	9.99	9.96	0.3					
LL	250	1.38	1.401	0.21	L-G	250	3.99	3.988	0.02					
LL	250	9.79	9.831	0.41	L-G	250	8.48	8.501	0.21					
LL	300	0.05	0.052	0.02	L-G	300	4.11	4.108	0.02					
LL	300	6.99	6.954	0.36	L-G	300	0.44	0.437	0.03					

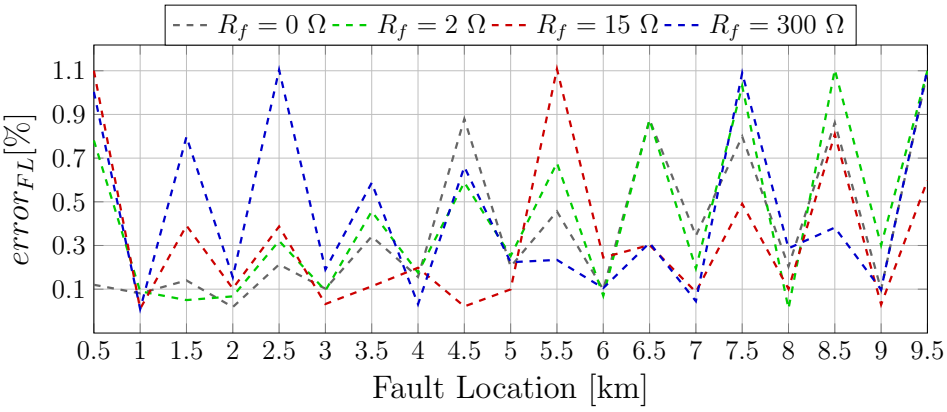

Figure 5.9: Absolute percentage of fault location error for LLL-G faults at each 5% of AC SC's length for different values of R_f.

5.4.2 Effect of small increments of fault distance

An incremental change of 10 m in fault location has been investigated in order to assess the sensitivity of the proposed scheme to small variations of the actual fault position. The aim of this analysis is to investigate that the proposed fault location scheme is accurate for small increments of fault location and consequently against the stochasticity of the sampling instant.

Specifically, the effectiveness of the fault location scheme has been evaluated for fault positions within the range of 5.9 km to 6.1 km with steps of 10 m. By changing the fault location by a small increment of 10 m, the influence of randomly varied sampling is investigated. Figure 5.10 shows the percentage fault location errors derived for this range

of fault positions during an LLL-G solid fault. It is evident that the $error_{FL}$ fluctuates between 0.95% to 0.1% which confirms the capability of the algorithm to provide high estimation accuracy for very small increments of fault location (in the range of 10 m).

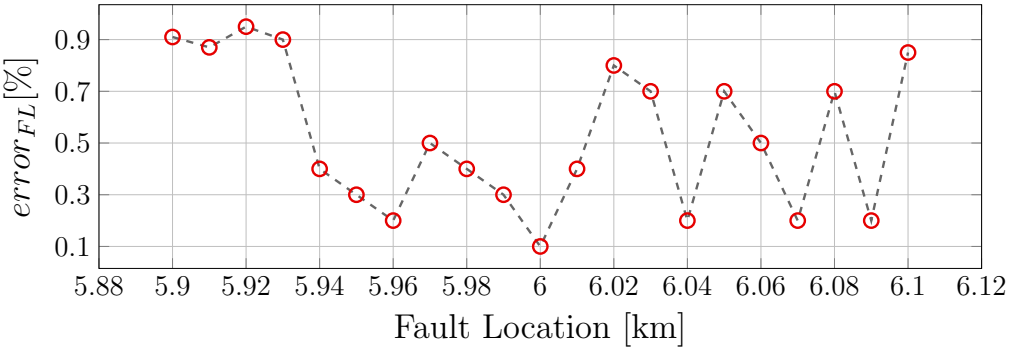

Figure 5.10: $error_{FL}$ with respect to 10 m increment of fault distance.

5.4.3 Effect of fault inception angle

In order to scrutinise the performance of the CNN-based scheme under different values of fault inception angles δ_f, an LL-G fault has been applied at 65% of the AC SC's length for δ_f from 0 up to 180 degrees with a step of 30 degrees. The main scope of this investigation is to evaluate the immunity of the fault location scheme to variations in the δ_f and subsequently in the time instant in the electric cycle when the fault occurs. The acquired results are presented in Figure 5.11 and confirm that the estimation capability of the proposed scheme is not affected by the changes in fault inception angle, yielding $error_{FL}$ equal to 0.27% which remains constant with respect to the changes in fault inception angle.

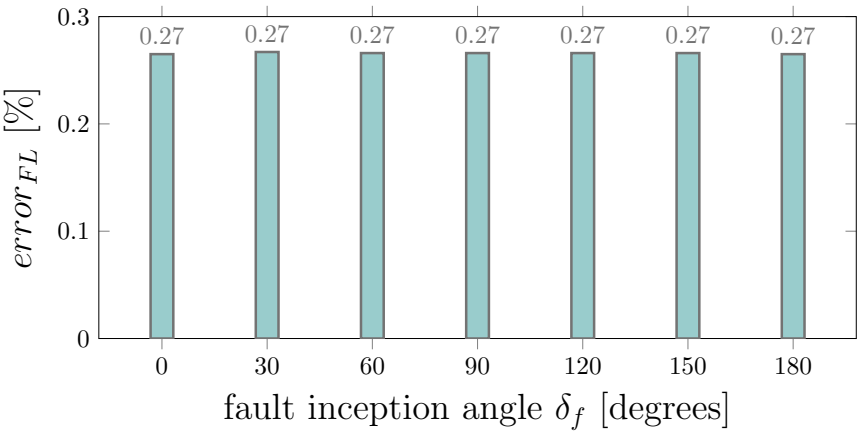

Figure 5.11: Impact of fault inception angle δ_f to fault location accuracy.

5.4.4 Effect of sampling frequency

The fault location scheme has been additionally tested with respect to the sampling frequency. In particular, the performance of the proposed scheme was evaluated for a series of testing scenarios, considering sampling frequencies from 20 kHz (the sampling frequency chosen for the presented studies) down to 5 kHz. Table 5.5 shows the resulting $error_{FL}$ from the conducted studies for some representative scenarios. As it can be seen, the fault location estimation accuracy is affected by the value of the sampling frequency. As the value of the sampling frequency decreases below 20 kHz, $error_{FL}$ presents a rapid increase and consequently the performance of the developed scheme is jeopardised. In particular, for 5 kHZ the maximum, $error_{FL}$, is 1.991% and the mean error, $\overline{error}_{FL}$, is 1.39%, while for 10 kHZ the maximum $error_{FL}$ is 1.321% and the mean error, $\overline{error}_{FL}$, is 0.9445%. The mean error, $\overline{error}_{FL}$, for the same scenarios with 20 kHZ is 0.1321%. Considering the complex structure of SCs, such an increase in $error_{FL}$ might have a great impact on the repairing process. Therefore, the obtained results reveal the requirements and the limitations of the developed scheme regarding the sampling frequency and conclude that for practical AC SC applications the initial basis of 20 kHZ constitutes the lowest sampling frequency which would lead to a precise fault location estimation.

Table 5.5: Fault location $error_{FL}$ of representative scenarios for different sampling frequency.

Fault type	**R_f (Ω)**	**Fault type A.C $_F$(km)**	**20 kHz**	**10 kHz**	**5 kHz**
LLL-G	0	5.20	0.022	0.68	1.190
LLL-G	50	9.41	0.063	0.855	1.405
LLL-G	200	1.30	0.080	0.970	1.381
LLL	300	8.10	0.621	1.182	1.991
L-G	0	2.11	0.041	1.149	1.942
L-G	2	6.30	0.132	0.941	1.230
L-G	150	4.70	0.048	0.959	1.382
LL-G	0	7.90	0.012	0.688	0.921
LL	0	3.22	0.032	0.710	0.994
LL	50	3.80	0.270	1.321	1.533

5.4.5 Effect of noise

In practical power systems applications, noise can be caused by power quality issues, transducers, or modulators and constitutes one of the most adverse factors which can potentially affect the accuracy of the fault location schemes. To assess the robustness of the proposed scheme under these conditions, the time-domain current and voltage

measurements of the testing scenarios have been subjected to artificial noise. Indicatively, Figure 5.12 demonstrates the spectrograms of phase A current resulting from the time-domain current signal without noise and with 100 dB signal-to-noise ratio (SNR), respectively, for an LLL-G solid fault applied 5.3 km from Bus 1 in Figure 5.3. Table 6.7 presents the obtained $error_{FL}$ with respect to an increasing noise amplitude for 6 representative fault scenarios from Table 5.4 (scenarios with the lowest and highest $error_{FL}$ prior to the noise addition).

It can be observed that, although the increase in the noise level (higher level of noise corresponds to lower value of dB) leads to an increase in $error_{FL}$, a satisfactory fault location rate can be achieved. As was expected, the highest rise in $error_{FL}$ is reported for SNR 30 dB.

Therefore, the proposed fault location scheme presents immunity against the additive noise to time-domain signatures of the testing scenarios. Furthermore, this analysis highlights the capability of the proposed algorithm to deal with more difficult testing scenarios and subsequently confirms that the developed CNN-based scheme does not face over-fitting issues and presents enhanced generalisation capability.

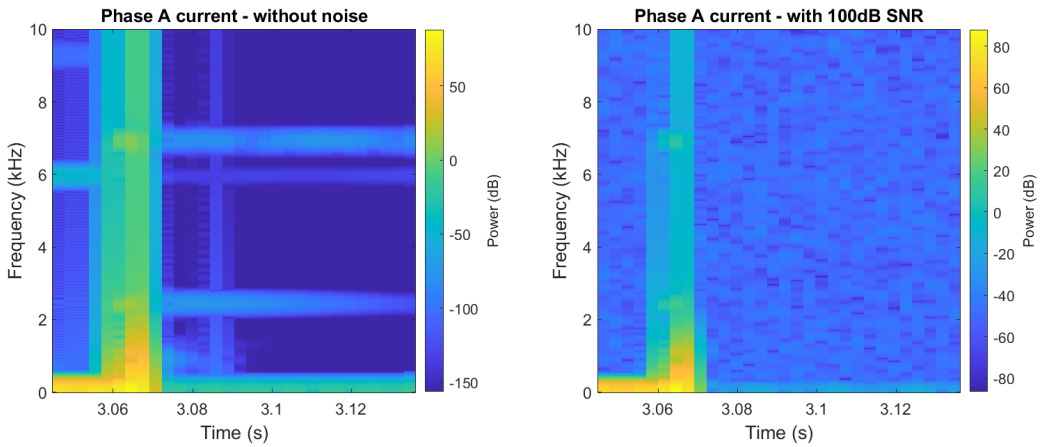

Figure 5.12: Spectrograms obtained from time-domain current signatures with and without noise

Table 5.6: Fault location $error_{FL}$ of representative scenarios with respect to additive noise on the testing scenarios.

Fault type	$\mathbf{R_f}$ **(Ω)**	**A.C$_F$(km)**	**without noise**	**100 dB**	**60 dB**	**30 dB**
LLL-G	0	8.8	0.010	0.056	0.107	0.200
LLL-G	0	6.82	0.110	0.211	0.387	0.402
LLL	2	5.2	1.100	1.130	1.191	1.286
LLL	200	2.98	0.380	0.420	0.513	0.589
LL-G	0	7.8	1.000	1.056	1.109	1.198
LL-G	15	1.8	0.5	0.769	0.807	0.980
LL	0	2.67	0.22	0.240	0.378	0.409
LL	300	0.02	0.040	0.091	0.147	0.242
L-G	2	5.50	1.180	1.228	1.210	1.289
L-G	250	3.99	0.020	0.073	0.154	0.253

5.4.6 Random masking and noise at the training dataset

In order to further evaluate the generalisation capability of the proposed scheme, data perturbation techniques were applied to the time-frequency domain signals of the training dataset. Those perturbation techniques include random masking and the addition of random noise. Specifically, the spectrograms obtained at Stage III of the development process, have been subjected to masking, by hiding portions of the image/spectrogram, and simultaneously to image noise.

Random masking is a widely used technique for computer vision applications [231,232], according to which small patches of the input image (the spectrograms in the presented work) are masked and set to zero during the training process. This random removal of information prevents the developed algorithm from being overly dependent on certain features of the input. Additionally, the addition of random image noise during the training process can be utilised to increase the variability of the training dataset and mitigate over-fitting of the algorithm to the training dataset.

The mean error, $\overline{error_{FL}}$, of the CNN-based fault location scheme on the testing dataset (i.e., considering random masking and image noise during the training process) has been found equal to 0.75%, which is very close to that reported in Table 5.2 (considering the initial model without perturbation techniques). Furthermore, the performance of the CNN model, with random masking and image noise, has been assessed based on the previously unseen fault scenarios reported on Table 5.4, similar to the initial model. Some representative cases are demonstrated in Table 5.7. The results revealed that the $error_{FL}$ for each scenario is low and therefore the fault location estimation accuracy remains high. Furthermore, the values of the resulting $error_{FL}$ for the investigated scenarios are very close to those resulting from the initial model (which does not consider

the perturbation techniques during the training process). Thus, no notable improvement has been reported regarding the fault location estimation accuracy and for most of the cases the initial model provides more accurate fault location estimation. The mean error, $\overline{error_{FL}}$, of Table 5.7, for the fault location scheme with the perturbation techniques during the training process, is 0.30% and for the initial CNN algorithm (i.e., without the perturbation techniques during the training process) it is 0.29%. Consequently, this analysis confirms that the initial CNN-based scheme has adequate generalisation capability, does not over-fit to the training dataset, and does not require perturbation techniques during the training process.

Table 5.7: Fault location error, $error_{FL}$ of representative scenarios considering perturbation techniques during the training process.

Fault type	$\mathbf{R_f}$ **(Ω)**	**A.C$_F$(km)**	**C$_F$(km)**	**error$_{FL}$(%)**
LLL-G	0	8.7	8.61	0.9
LLL-G	2	5.2	5.27	0.7
LLL-G	5	2.1	2.122	0.22
LLL-G	250	9.98	9.979	0.01
LLL-G	300	6.17	6.157	0.13
LLL	0	7.76	7.739	0.21
LLL	0	2.39	2.384	0.06
LLL	2	3.13	3.148	0.18
LLL	5	9.9	9.892	0.08
LLL	250	9.13	9.087	0.43
LL-G	0	2.6	2.572	0.28
LL-G	0	7.8	7.910	1.10
LL-G	2	9.97	9.879	0.91
LL-G	5	6.3	6.307	0.07
LL-G	200	9.52	9.475	0.45
LL	2	8.15	8.153	0.03
LL	2	6.49	6.456	0.34
LL	5	5.14	5.141	0.01
LL	15	7.11	7.102	0.08
LL	15	4.29	4.272	0.18
L-G	0	2.7	2.690	0.10
L-G	0	6.9	6.918	0.18
L-G	0	1.81	1.787	0.23
L-G	5	6.38	6.395	0.15
L-G	200	9.99	9.951	0.39

5.5 Comparative Analysis with Other Data-Driven Fault Location Schemes

The effectiveness of the developed fault location scheme has been further validated by comparing its performance with another widely used data-driven algorithm in power system applications. Specifically, the Long Short Term Memory (LSTM) algorithm has

been selected for comparison purposes as it is a widely adopted RNN model for fault management applications [233]. LSTM models are well-suited to processing sequences of data (i.e, time-series data) and adaptively learning the dynamic information of the input data by non-linear gating units. Their main advantage is that they extract the temporal correlation of time series data (serial correlations) and parallel dependencies (correlations of the input features) [208], while controlling the amount of information that needs to be retained.

5.5.1 Stages of the LSTM algorithm

The 3-stage algorithm developed for the estimation of the fault location on the AC SC based on the LSTM model is depicted in Figure 5.13. The following subsections describe each stage in detailed.

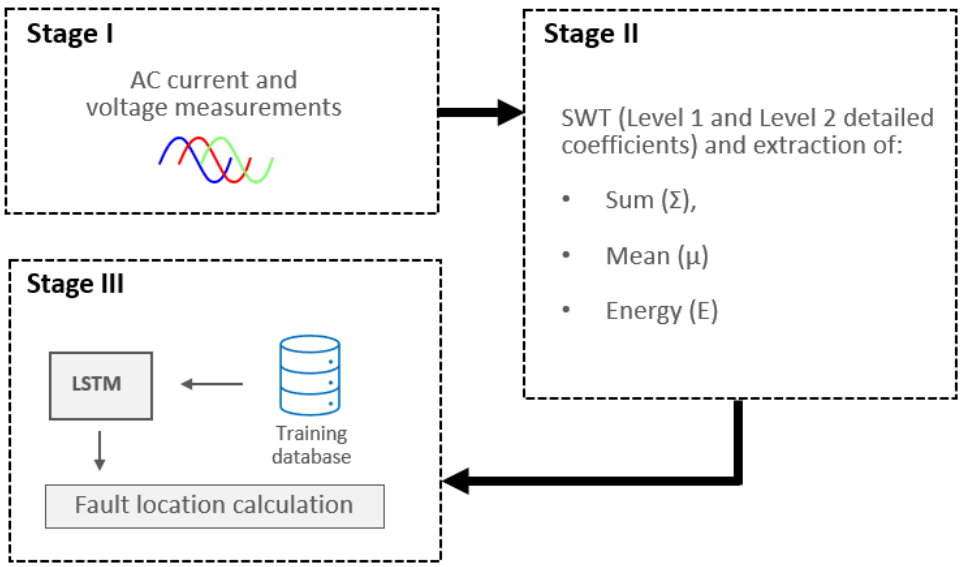

Figure 5.13: Schematic diagram of the LSTM-based fault location schemes.

5.5.1.1 Stage I - Signal acquisition

The same fault current and voltage measurements acquired in Section 6.3.1 were utilised to form the data basis for the fault location regression problem with the LSTM-based scheme. To ensure fair comparison between the schemes, a same sampling frequency of 20 kHz was considered.

5.5.1.2 Stage II - Feature extraction

At this stage, the SWT is applied as a power signal processing tool which detects signal singularities and extracts the useful insights from voltage and current measurements. As has been referred to in Chapter 4, SWT is a widely used WT for different power system applications (i.e., protection applications) as it is computationally efficient and presents reduced complexity [145].

For the LSTM-based fault location scheme, the faulted voltage and current signatures are subjected to Level 1 and Level 2 decomposition through the SWT technique, and the corresponding detailed coefficients are produced, utilising the *db*4 mother wavelet which presents high accuracy and reliability in power systems applications [144]. It should be noted that the exhaustive research of the appropriate type of mother wavelet is out of the scope of the presented work.

Once the detailed coefficients of decomposition Levels 1 and Level 2 are acquired, a moving data window has been utilised to extract feature vectors to form the data basis for the LSTM-based scheme. It has been assumed that a data window with length of 30 samples (29-sample overlap) is adequate for this purpose. The production of the feature vectors is performed at the end of Stage II. In particular, similar to the feature vectors generated for the fault detection and classification schemes in Chapter 4, the feature vectors for the LSTM-based fault location scheme include the absolute values of detailed coefficients at decomposition Level 1 and Level 2 and also the sum $\Sigma(D_j)$, mean $\mu(D_j)$, standard deviation $\sigma(D_j)$, and the energy content $E(D_j)$ of the detailed coefficients of decomposition Level 1 and Level 2. These have been calculated according to (5.8)-(5.11), respectively:

$$\Sigma(D_j) = \sum_{i=1}^{m_w} |D_j(i)| \tag{5.8}$$

$$\mu(D_j) = \frac{1}{2^j \cdot m_w} \sum_{i=1}^{m_w} |D_j(i)| \tag{5.9}$$

$$\sigma(D_j) = \sqrt{\frac{1}{2^j \cdot m_j} \sum_{i=1}^{m_w} (|D_j(i)| - \mu(D_j))^2} \tag{5.10}$$

$$E(D_j) = \sum_{i=1}^{m_w} [D_j(i)]^2 \tag{5.11}$$

where $D_j(i)$ denotes the $i-th$ detailed coefficient for $j = 1, 2$ decomposition level and m_w is equal to the window size.

At the data pre-processing stage, prior to the training of the LSTM model, the feature vectors along with the initial three-phase current and voltage signatures are normalised. For the normalisation process, the mean value is subtracted by each sample in the feature vector and the resulting values is divided by the standard deviation as presented in (5.12):

$$Y_{j,scaled} = \frac{Y_j - \overline{Y}}{\sigma(Y)} \tag{5.12}$$

where Y_j denotes each sample in the feature vector y or current/voltage signal y, $\overline{Y}$ and $\sigma(Y)$ correspond to the mean value and the standard deviation of each feature vector of current/voltage signal, respectively.

The normalised feature vectors and the normalised three-phase current and voltage signatures have been reshaped into a 3-dimensional matrix (batch size, sequence length, features) in order to meet the requirements of LSTM input data, and are used as inputs to train the LSTM model.

5.5.1.3 Stage III - Estimation of fault location

To perform the fault location estimation task, 2 different LSTM-based schemes have been investigated considering different datasets. The scope of this investigation was to evaluate the impact of different datasets on the LSTM-based fault location estimation capability and select the scheme with the best performance to be compared with the developed CNN-based scheme. The two models are composed of: i) the LSTM-based Scheme 1 which considers as inputs only the normalised three-phase current and voltage signatures, and ii) the LSTM-based Scheme 2 which considers the inclusion of SWT signal processing and thus accepts as input the normalised three-phase current and voltage signatures along with the extracted feature vectors. Furthermore, the comparison between these 2 schemes evaluates the impact of the SWT technique at the pre-process stage on fault location estimation accuracy.

The 3-dimensional matrix which is utlised as the input to LSTM-based Scheme 1 is $(32, 1600, 6)$, where 32 is the batch size, 1600 is the sequence length and 6 is the different number of features (3 phase currents and 3 phase voltages). For LSTM-based Scheme 2 the 3-dimensional matrix at its input is $(32, 1600, 42)$, where 42 is the number of features (3 phase currents, 3 phase voltages and 6 feature vectors for each current and voltage signature). The sequence length in an LSTM network refers to the number of time steps in a single sample of the input data. In other words, it is the length of

the input sequence that the LSTM network processes at a time. The sequence length is an important hyperparameter in an LSTM network, as it determines the amount of historical information that the network accesses to make predictions. If the sequence length is too short, the network may not be able to capture long-term dependencies in the data. If the sequence length is too long, the network may be computationally expensive or may struggle to fit the data due to overfitting. Therefore, choosing an appropriate sequence length for an LSTM network is an important part of the model design process, and it requires extensive trial and error studies.

The output of the LSTM layer is fed into a fully connected layer followed by a regression layer which produced the single value of the fault position as a percentage of the AC SC length, similar to the CNN model. Thus, for LSTM-based schemes the fault locations is calculated based on (5.6).

5.5.2 Selection of LSTM model

This section evaluates the performance of the developed LSTM-based schemes in order to select the best model to be compared with the proposed CNN-based fault location scheme. LSTM-based schemes have been developed utilising the PyTorch framework. The most-suitable hyperparameters of each LSTM model have been selected based on the GS 5-fold CV technique (similarly to the CNN model). Particularly, different combinations of i) hidden state size, ii) number of LSTM layers, iii) learning rate, and iv) batch size have been tested utilising the mean error, $\overline{error}_{FL}$, as the 5-fold CV score, given by (5.7).

The 2 LSTM-based schemes were evaluated on the testing dataset and the resulting mean error, $\overline{error}_{FL}$, is presented in Table 5.8.

Table 5.8: Tested LSTM-based schemes and their performance on the testing dataset

LSTM-based schemes	$\overline{\mathbf{error}}_{\mathbf{FL}}(\%)$
Scheme 1	0.95
Scheme 2	0.88

It is evident that LSTM-based Scheme 2, which incorporates the SWT technique, presents the lowest mean error, $\overline{error}_{FL}$, and therefore it has been selected for comparison purposes with the CNN-based fault location scheme. The resulting hyperparameters from the GS 5-fold CV technique are the following: learning rate = 0.001, batch size = 32, hidden size = 64, and number of LSTM layers = 4. The Adam optimiser algorithm was adopted for learning the weights and biases associated with the model during the

training process.

5.5.3 Results of the comparison between the LSTM and the CNN algorithm

This section presents the results of the comparative analysis between the proposed CNN-based fault location scheme and LSTM-based Scheme 2. Both schemes have been evaluated for additional fault cases which simulated different fault types, varying fault position (which do not belong to the initial data set), and varying R_f. The $\overline{error}_{FL}$ of the CNN-based model for these additional scenarios has been found to be 0.72%, while for LSTM-based Scheme 2 this is 1.10%. The results of some representative cases are presented in Table 5.9. The obtained observations validate the effectiveness of the proposed fault location scheme, as the CNN model yields lower $error_{FL}$ compared to LSTM-based Scheme 2 for all the scenarios. The mean error, $\overline{error}_{FL}$, of the CNN-based scheme for the presented scenarios in Table 5.9 is 0.32% and for LSTM-based Scheme 2 this is 1.88%. The results revealed that the CNN-based fault location scheme outperforms LSTM-based Scheme 2 and provides more accurate fault localisation, irrespective of the fault type, fault resistance, or fault position and thus it can be considered a more reliable scheme for the case of AC SCs.

5.6 Discussion

A novel data-driven fault location scheme for power grids with AC SCs has been developed based on fault current and voltage measurements captured from a single end of the AC SC and Bus 1, respectively. The proposed scheme utilises the combination of a time to time-frequency transformation and a CNN algorithm for the fault location estimation. According to the simulation results and the outcomes of the validation studies, the following remarks can be pointed out:

- The proposed CNN-based fault location scheme has been found to successfully provide accurate estimation of the fault location across a wide range of fault conditions, accounting for different fault positions, fault types (i.e., LLL, LLL-G, LL, LL-G, L-G), values of fault resistance up to 300 Ω, and fault inception angles (from 0 degrees to 180 degrees). It is worth highlighting that the developed fault location scheme presents robust performance, even in the case of close-up faults

Table 5.9: Results of the comparison between the CNN-based and LSTM-based fault location schemes.

Fault type	$\mathbf{R_f}$ **(Ω)**	$\mathbf{A.C_F}$**(km)**	**CNN error$_{FL}$(%)**	**LSTM error$_{FL}$(%)**
LLL-G	0	0.60	0.12	0.70
LLL-G	2	4.20	0.31	1.07
LLL-G	5	7.38	0.18	2.10
LLL-G	15	9.10	0.42	1.17
LLL-G	50	8.11	0.70	2.23
LLL-G	200	5.90	0.62	2.40
LLL-G	300	3.18	0.14	1.58
LL-G	0	3.56	0.09	2.27
LL-G	2	2.90	0.14	1.20
LL-G	5	7.30	0.33	1.00
LL-G	15	0.10	0.11	0.98
LL-G	50	8.80	0.34	2.07
LL-G	200	6.13	0.26	1.11
LL-G	300	9.56	0.57	2.77
L-G	0	1.70	0.23	1.90
L-G	2	7.10	0.22	0.98
L-G	5	3.98	0.43	2.13
L-G	15	2.40	0.24	2.99
L-G	50	4.45	0.17	2.56
L-G	200	9.90	0.33	3.71
L-G	300	8.19	0.39	2.84
LLL	0	1.14	0.18	0.99
LLL	2	2.34	0.20	1.09
LLL	5	3.84	0.38	1.99
LLL	15	4.19	0.23	2.01
LLL	50	8.50	0.22	2.11
LLL	200	7.13	0.43	2.12
LLL	300	9.30	0.21	2.03
LL	0	9.40	0.98	2.01
LL	2	1.40	0.07	1.01
LL	5	7.10	0.09	1.18
LL	15	2.60	0.44	1.29
LL	50	1.50	0.34	3.01
LL	200	3.12	0.44	2.13
LL	300	8.27	0.80	3.17

(i.e., fault location at 0.1% or 99% of the AC SC length) and under the influence of highly-resistive faults during which there is no quenching of the AC SC. The resulting mean fault location error, $\overline{error}_{FL}$, on the testing dataset has been found to be 0.74% while the $\overline{error}_{FL}$ for the additional scenarios utilised to further validate the performance of the developed scheme has been demonstrated to be 0.34 %.

- The effectiveness of the proposed method has been verified against small increments of fault location. Specifically, by changing the fault location with step of 10 m and evaluating its performance against the randomly varied sampling instance, the resulting fault location estimation error lies within the range of 0.95% to 0.1%. Furthermore, it can be concluded that despite the addition of noise in the testing

dataset, a successful fault locating rate is preserved.

- A sensitivity analysis revealed that the lowest sampling frequency for this fault location application is 20 kHz.

- The incorporation of perturbation techniques, such as masking and noise, in the training process resulted in a mean fault location estimation error, $\overline{error}_{FL}$, close to that of the initial model. Therefore, it has been confirmed that the initial model has sufficient generalisation capability, does not over-fit to the training dataset and thus eliminates the need for perturbation techniques which increase the complexity of the training process.

- The proposed fault location scheme eliminates the need for a communication link and expensive and complicated synchrophasor equipment.

- The reliability of the proposed fault location scheme has been demonstrated by comparing its performance with an LSTM-based network, which is a widely-used algorithm for fault location applications. The results indicated that the proposed CNN-based scheme outperforms the LSTM-based scheme in terms of fault localisation accuracy. In particular, during the comparative analysis, the proposed CNN-based scheme presents a mean fault location estimation error, $\overline{error}_{FL}$, of 0.72% for the same investigated scenarios, while the LSTM-based scheme gives 1.1%.

- The time to time-frequency transformation of non-stationary signals is well suited for studying signals in time and frequency domain simultaneously, and provides a more comprehensive analysis of signals which can lead to improved accuracy of fault location estimation.

- The integration of image analysis techniques with AI algorithms has the potential to enhance the precision of feature extraction and facilitate the accurate identification of fault location. Image analysis techniques, through their capability of representing high-dimensional data in a condensed form, enable the facilitation of pattern recognition and mitigate computational complexities. Furthermore, such techniques demonstrate resilience towards data with a high level of noise.

- An extensive investigation of CNN algorithms with regards to the resulting mean fault location estimation error, $\overline{error}_{FL}$, revealed that the Inception-v3 model

outperforms the rest of the CNN models for the feature extraction task of the constructed spectrograms.

5.7 Summary

In this chapter the fault location challenge in AC systems with SCs has been analysed. It has been found that the most important attribute of an effective fault location scheme is the accuracy in the fault location estimation. The accurate identification of the fault position accelerates the restoration process, eliminates the outage time and consequently enhances the system reliability. In particular for SCs, the need for reliable fault location schemes is rendered imperative due to their complex structure, the increased cost of such technology and the demanding restoration process.

In response to this challenge, this chapter proposes the development of a data-driven fault location scheme which incorporates feature extraction tools, such as image analysis techniques, and AI algorithms such as CNN models to address the challenge of accurate fault location on AC SCs. Initially, a literature review was conducted on the existing and proposed fault location techniques in the technical literature. The assessment showed that AI-based schemes provide a trade-off between accuracy, cost, and complexity and thus many researchers have started to focus on AI for the development of fault location applications. Furthermore, the key findings revealed the research gap in the area of fault location on SCs and assessed the potential of the existing methods for resolving this challenge. Although all the reported methods have their own advantages and drawbacks, it has been highlighted that conventional schemes, such as impedance-based, cannot provide accurate estimation of fault location on SCs or result in increased implementation cost (i.e., sparse and distributed measurements methods). Reflectometry-based schemes constitute the only solution proposed in the literature for the case of SCs, however, such schemes have not been validated against multiple fault scenarios or SCs with length up to several km. Furthermore Reflectometry-based schemes result in increased cost due to the need for external equipment.

The proposed CNN-based fault location scheme is a novel contribution to the fault location problem, leveraging the strong learning ability of CNNs. This has been found to provide a robust solution for the precise fault localisation of AC SCs. In particular the development of the proposed scheme has been based on the transformation of time domain current and voltage fault signatures to time-frequency domain, with image

analysis techniques used for the extraction of useful information. For the estimation of the fault location on AC SCs, an Inception-v3 CNN model has been utilised which presented mean fault location estimation error, $\overline{error}_{FL}$, equal to 0.74% on the testing dataset and 0.34% on additional fault scenarios which do not belong to the initial dataset. The successful identification of the fault position across the length of the AC SC has been verified for a wide range of fault scenarios including highly-resistive and close-up faults, with resistances up to 300 Ω. Specifically, the minimum fault location estimation error, $error_{FL}$, has been found to be 0.01% and the maximum 1.18%. The scheme has demonstrated its ability to maintain a high level of accuracy in the presence of noisy inputs and randomly varied sampling instances. Additionally, the scheme remains unaffected by changes in the fault inception angle. Furthermore, the increased generalisation capability of the developed scheme has been validated by a comparative analysis with an similar CNN algorithm which adopts perturbation techniques during the training process (i.e., perturbation techniques are utilised in AI applications to improve the learning process of the algorithm) and the results confirmed the effectiveness of the proposed scheme and highlight its learning capability without the need for perturbation techniques. Lastly, the proposed CNN-based scheme has been compared with an LSTM-based fault location scheme and the results have validated its superiority, achieving a mean fault location estimation error, $\overline{error}_{FL}$, of 0.72% compared to 1.10% for the LSTM-based scheme, for the same fault scenarios.

Chapter 6

Protection of DC SCs in HVDC Systems

HVDC technology offers several advantages over its AC counterparts, such as the capability for efficient bulk power transmission over long distances with minimal losses [234]. These attributes make HVDC systems ideal for connecting remote RES, such as offshore wind farms. In addition to this, HVDC systems present several commercial and technical benefits, including the interconnection of non-synchronous grids, independent control of active and reactive power, and increased resilience against disturbances due to its insensitivity to frequency variations [87]. These advantages make HVDC systems well-suited for enhancing the power flow controllability in power grids, improving their efficiency and stability, and providing a firewall against cascading blackouts [235, 236]. Therefore, HVDC transmissions will play a significant role in the transition of power grids towards sustainable net zero grids.

However, despite the numerous benefits, the implementation of HVDC systems is faced with several key challenges, primarily due to the particularities and complexity of the various technologies used in HVDC grids (i.e., converters, transformers, filters, CBs). One of the most crucial factors for the wide spread adoption of HVDC technology is the efficient protection of HVDC and AC systems. In particular, HVDC protection philosophy is consistent with the objectives of AC transmission protection which aim to achieve reliability, stability, dependability, security, sensitivity, selectivity and speed. However, there are some crucial differences, primarily related to the timeframe of events. Contrary to AC grid protection, which requires fault clearing time within the range of

hundreds of ms, HVDC protection requires very fast and discriminative schemes which detect and isolate the fault within the range of a few ms [164, 237]. The main factors which affect the fault clearing time in HVDC systems is the limits introduced by DC CBs and power electronic devices installed in the converters. In HVDC systems, when a fault occurs, the converter is blocked for self-protection, resulting in temporary loss of control over the converter (and partially the DC grid). Thus, very fast and reliable protection systems are needed in order to avoid damages in the components and minimise the impact of faults on the system. Furthermore, the DC-side faults, especially for Voltage Source Converter (VSC)-based HVDC systems, are characterised by increased magnitudes and rapid rising time [40]. This effect in conjunction with the absence of natural current zero crossing make the protection of HVDC systems a challenging task [238]. As such, HVDC systems require the development of advanced protection solutions which can accurately detect and respond to faults in a timely and effective manner while helping to ensure high levels of reliability.

SCs have the potential to revolutionise HVDC transmission systems, by providing additive benefits such as improved efficiency, reduced losses, and decreased overall cost of the system [91]. However, the fault response of DC SCs, which is dominated by the quenching phenomenon, exacerbates the challenge of HVDC protection. Specifically, the effect of quenching on fault current and voltage magnitudes can affect the sensitivity, selectivity, and operational speed of HVDC protection schemes and have a negative impact on the continued safe and reliable operation of HVDC systems. Therefore, to address these challenges it is important to develop advanced protection solutions which will be aligned with the HVDC protection requirements and consider the particularities of SC technology. The designed protection solutions should have a high degree of sensitivity, security, selectivity, and high operation speed.

On this front, this chapter proposes a novel data-driven, centralised protection scheme (on the substation level) for discriminative fault detection and classification in MMC-based multi-terminal HVDC systems with DC SCs and conventional DC cables. The developed protection scheme exploits the potential of the latest advancements in AI and presents the capability of detecting and classifying faults to all the elements connected to HVDC substations (i.e., buses, SCs and conventional cables).

6.1 Review of SCs in HVDC Systems and their Fault Management

Along with the advancement of superconducting-based technology, the deployment of DC SCs is gaining attention as the key player of power transmission in future grids. The first DC SC for industrial application was accomplished by the Chinese Academy of Science, in 2012, by designing a 1.3 kV, 10 kA unipolar cable with length 360 m [239]. To date, there are three landmark demonstration projects of DC SCs. In particular, the EU-funded Best Paths project, which investigates and validates the operation of a 30 m, 320 kV, 3.2 GW HVDC link for real-grid conditions with the developed technology to approach commercial deployment [18]. The Ishikari project, Japan, which demonstrates the deployment of 500 m and 1000 m DC SCs for the interconnection between a large scale PV cell with an Internet data center to provide DC power supply [28], and the St. Petersburg project which deploys the installation of a 2.5 km length DC SC at 20 kV [30].

The transient analysis of DC SCs has became one of the emerging research trends. Many studies have started to focus on the technical feasibility and the associated challenges of meshed HVDC grids with SCs. Specifically, authors in [91] addressed the power flow and transient stability issues of multi-terminal HVDC systems with VSCs and SCs, while a feedback current control scheme for the regulation of power distribution in a meshed HVDC system with SCs and Line Commutated Converters (LCCs) was developed in [240]. A detailed fault current characterisation of meshed HVDC system with MMCs and DC SCs is presented in [84]. The conducted simulation-based analysis evaluated the impact of SC fault current limiting capability on the DC fault current magnitudes, highlighting the potential of higher flexibility in terms of protection operation time. In [241] the fault current limiting capability of a 0.2 kV, 100 kA, 20 MW DC SC is investigated and the results showed reduction in current magnitude from 42.5 kA to 37.5 kA due to quenching phenomenon and the increase in the equivalent resistance of SC. The impact of DC SCs on fault levels is also studied in [242] for a 300 km DC SC in a meshed HVDC system with LCCs. The conducted studies showed that regardless of the fault type, the resulting fault current magnitudes can be 20 % reduced during the quenching of DC SCs. Furthermore, as the utilisation of Superconducting Fault Current Limiters (SFCLs) is considered a viable solution for current limitation in meshed HVDC systems [243, 244], several studies have started to propose the replacement of SFCLs by DC SCs with fault

current limiting functionality [245]. The obtained results demonstrated that DC SCs are more efficient in fault current limitation and present higher tolerance to highly-resistive faults. All the existing studies have carried out experimental tests on prototype DC SCs, or simulation-based analysis, for the assessment of steady-state, transient performance, and the mechanical suitability of DC SCs or the validation of the designing process of SCs and the operation of the cryogenic refrigeration system. However, there is no reported research, discussions, or proposed strategies for the protection of DC SCs, prohibiting the widespread adoption of such cable technology in large-scale HVDC applications.

The integration of SCs in HVDC systems complicates the fault management process due to the quenching of DC SCs and the resulting variations in resistance, affecting the impedance of the grid and fault current and voltage measurements. Ensuring the implementation of highly effective fault detection strategies for SCs is of paramount importance, given the unique characteristics and vulnerabilities associated with these systems. In particular, there is a growing demand for robust fault management strategies capable of accommodating the variable resistance introduced during the quenching process. Moreover, it is imperative to investigate scenarios in which the quenching process, responsible for transitioning the cable from a superconducting to a normal state, may experience delays due to structural complexities within the system or the intrinsic properties of the SC itself. In certain instances, quenching may not occur at all, as observed during highly-resistive faults. In such cases, the absence or delay in quenching can trigger a catastrophic sequence of events. The quenching process functions as a protective mechanism by dissipating excess energy and preventing the formation of hotspots within the cable. Therefore, there is an urgent need for highly sensitive protection schemes capable of detecting the initiation of quenching to mitigate these potential risks effectively.

In that aspect, conventional protection for HVDC systems may result in poor performance and endanger system safety. In particular, the sensitivity of over-current protection, which is utilised in HVDC systems as secondary transmission line protection, is affected by the reduced fault current magnitudes due to the quenching of DC SCs. Distance relays employ a calculation of apparent impedance through the measurement of voltage and current at the relay location. This calculation is utilised to identify faults and serves as the primary protective measure for AC transmission lines. Nevertheless, in HVDC grid protection, the complex impedance at the fundamental frequency is distinct

from that of the AC system, and the reliability of distance relays may be impacted by the resistance present during a fault [246]. Considering the variations in system impedance due to the quenching of DC SCs, distance protection relays are not suitable schemes. Differential protection is a communication-based scheme which operates if the difference between the sending and receiving end current exceeds the preset threshold. This type of protection is better suited for short distance transmission lines and bus protection as its response time is slow for long transmission lines with a high dependence on correct communication operation [247]. TW-based schemes are more suitable for HVDC transmission line protection [238]. However, the studies reported in [248, 249] showed the drawbacks of the TW-based approach against close-up faults, their difficulty to detect wave-peaks, and sensitivity to noise. Consequently, boundary protection is employed in addition to the TW technique to determine faults in the HVDC line. With respect to DC SCs, there is no reported research in the literature which investigates the effectiveness of TW-based schemes. Furthermore, the exploration of TW theory in SCs requires a more detailed modelling approach of SCs. Voltage and current derivative based protection schemes using the single end measurements have proven to be efficient for multi-terminal HVDC systems [250]. However, such schemes adopt a threshold-based operation, and their tuning shall be very challenging for the case of DC SCs. The performance of voltage and current derivative-based protection schemes against fault on DC SCs will be assessed in the following section.

Considering the limitations of conventional HVDC protection systems due to the particularities of DC SCs, researchers have started to investigate AI techniques for the protection of HVDC systems with SCs to overcome the complexities and challenges by relying on their inherent learning capabilities. However, this field of research is still at its infancy. More specifically, there is only one reported method [121] which is based on the monitoring of transmission characteristics for the detection of series faults (i.e., one or more conductors are damaged or disconnected) on DC SCs and utilises a ML model for the fault type classification. However, only the accuracy of the fault identification (i.e., detection and classification) has been presented without providing any insight about the time performance of the proposed method.

Filling the research gap in the literature and demonstrating the unique advantages over existing methods, this chapter presents a novel protection scheme for rapid and discriminative fault detection and classification in meshed HVDC system with SCs. The

proposed scheme adopts a centralised protection philosophy and is designed to detect and classify faults in HVDC substations, accounting for faults at buses and faults applied on SCs or conventional feeders. The basic idea behind centralisation is to move protection from multiple bay-level devices to a single central processing unit [251]. The proposed protection scheme utilises a centralised philosophy, situated at the substation level, as opposed to multiple bay-level devices. This approach is based on the key findings in the technical literature that suggest centralised protection schemes offer a more holistic protection solution, higher scalability, and improved protection discrimination [238, 251]. This is particularly important in HVDC systems where the time frames for fault detection and classification are tight.

6.2 Investigation of Derivative-Based Protection Philosophy

Prior to the analysis of the proposed protection algorithm, the performance of existing protection solutions for HVDC systems has been evaluated. In particular, this section demonstrates the limitation of derivative-based HVDC protection philosophies, such as current and voltage derivative-based schemes, which have been widely-proposed in the technical literature for fault detection and location applications for HVDC systems. Derivative-based schemes present increased sensitivity, speed, and accuracy, as well as removing the need for a communication link (i.e., only local measurements are required) [252].

In the presented work, the potential of utilising di/dt and dv/dt based protection has been assessed by conducting a qualification analysis regarding the current and voltage derivative threshold settings for the adequate detection of faults applied on SCs, which presents the basic challenges of the threshold-based protection schemes for HVDC systems with SCs. Further investigation of the settings adjustment is beyond the scope of the presented work. Specifically, for the presented studies, the multi-terminal HVDC network presented in Chapter 3 and depicted in Figure 6.1 has been utilised. The relay installed at point P 3.1 of SC1 has been utilised as an indicative test case and its operation is based on the local current or voltage measurements. The protection zone is bounded by the inductive terminations and the current and voltage derivative-based relay should operate only for forward faults (the direction is indicated by the grey arrow in Fig. 6.1)

within the protection zone (no protection directionality has been considered) in order to preserve the protection sensitivity and security.

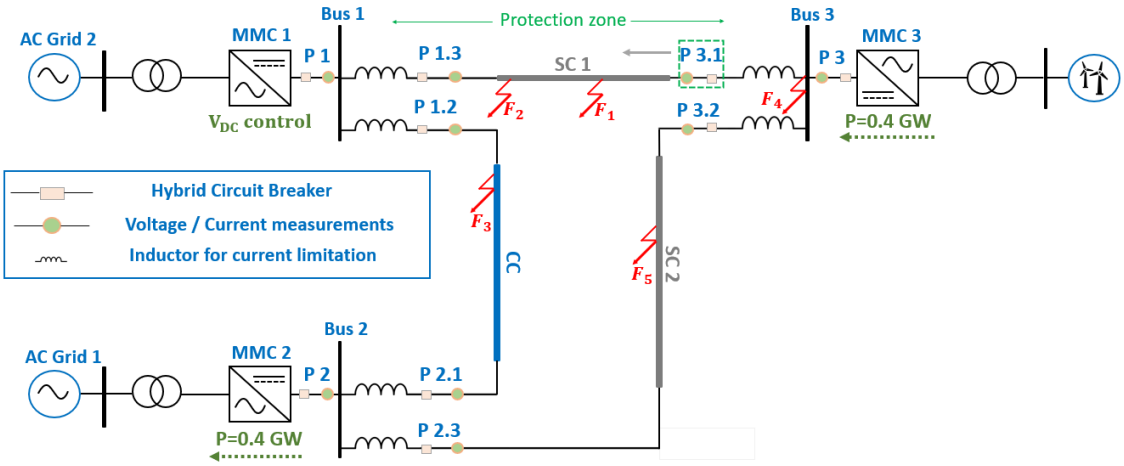

Figure 6.1: HVDC network model incorporating derivative-based protection scheme.

For the assessment of the proper current and voltage derivative threshold settings, a forward PP internal remote highly-resistive fault (i.e., F_2) and a forward PP solid external fault (i.e., F_3) have been considered. These fault scenarios have been selected as the most challenging for the evaluation of protection discrimination. Specifically, highly discriminative protection schemes should initiate a tripping signal for highly-resistive internal faults at the remote terminal and remain stable during solid external faults occurring beyond the boundary of the protection zone.

6.2.1 Assessment of derivative-based schemes

Figure 6.2a and Figure 6.2b show the di/dt of the current flowing through SC1 and measured at point P 3.1 during F_2 and F_3, respectively. As it is demonstrated, during F_2, which is a highly-resistive internal fault with $R_f = 200\ \Omega$, the first di/dt peak is presented 1.2 ms after the fault and is approximately 198 kA/s. During F_3, the first peak of di/dt is approximately 920 kA/s. The magnitude of the peak of di/dt, during F_2, is reduced due to the increase in the variable R_{eq} of SC1 and the high value of R_f. Specifically, during F_2, the magnitude of the first peak of di/dt is affected by: i) the variable resistance of SC1 and ii) the 200 Ω R_f, while the magnitude of the peak of di/dt during F_3 is affected by: i) the variable resistance of SC1 and ii) the current limiting inductance at the terminals of SC1 and CC which are equal to 140 mH and 133 mH, respectively. Therefore, the lower peak during the F_2 internal fault is explained based on

the higher value of current path's impedance while the peak during F_3 external fault is affected by the sizing of the inductors at the SC's terminals.

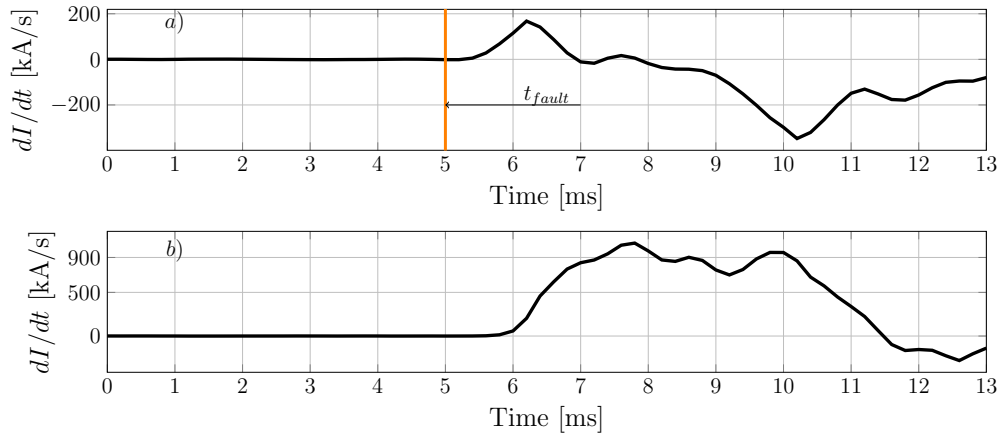

Figure 6.2: Results of di/dt during: a) a PP internal, remote highly-resistive fault at 99 % of SC1's length with $R_f = 200\ \Omega$ b) a PP external solid fault at 0.1 % of CC's length.

Effectively, the obtained results indicated that the selection of a low current threshold setting is required in order to ensure the detection of internal highly-resistive faults. Conversely, for low current threshold settings, the current derivative-based relay operates for external solid faults applied on the CC. Therefore, this protection philosophy presents a low level of protection selectivity. This is due to a trade-off between protection sensitivity and stability, where the protection of the SC may operate during solid external faults and result in the disconnection of the unfaulted SC or highly-resistive internal faults may remain undetected.

Figure 6.3a and Figure 6.3b depict the dv/dt of the voltage measurements captured at point P 3.1 during F_2 and F_3, respectively. It can be noticed that the peak of dv/dt, during F_2 is approximately 10 MV/s, 2.5 ms after the fault occurrence, while during F_3, the first peak of dv/dt is 50 MV/s.

Similar to the case of the current derivative-based relay, the results showed that the selection of a low voltage threshold setting is required for the secure operation against internal highly-resistive faults, jeopardising the protection stability against external solid faults applied on CC. Consequently, it can be concluded that the quenching, variations in R_{eq} of SCs, increase in R_f, and fault current limitation capability of SCs have an adverse impact on the proper selection of the voltage threshold setting.

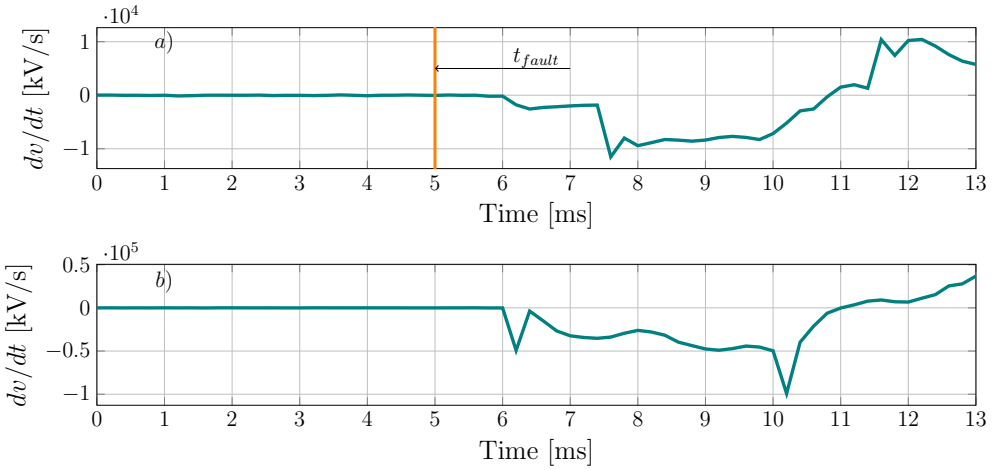

Figure 6.3: Results of dv/dt during: a) a PP internal, remote highly-resistive fault at 99 % of SC1's length b) a PP external solid fault at 0.1 % of CC's length.

6.3 Proposed Protection Scheme

The proposed data-driven protection scheme aims to address the aforementioned limitations and provide a reliable protection solution for HVDC systems with SCs. For that purpose, the proposed scheme exploits the advantages of advanced AI algorithms, such as the XGBoost model, for the development real-time fault detection and classification. In the presented work, the fault classification term refers to the identification of the faulted element (i.e., buses, SC1, SC2 and CC).

As an indicative example, the XGBoost-based scheme installed at Bus 3, shown in Figure 6.5, is a centralised cable and bus protection philosophy which protects the system against the faults occurring within the protection zone. The protection zone of the XGBoost-based scheme installed at Bus 3 includes faults occurring at Bus 3 (F_4), SC1 (F_1), and SC2 (F_5). Similar to Bus 3, the same centralised XGBoost-based protection philosophy has been assumed to be installed to the other two buses illustrated in Figure 6.1 (Bus 1 and Bus 2). In particular, the XGBoost-based scheme installed at Bus 1 detects and classifies faults occurring at Bus 1, SC1, and CC, while the protection zone of the XGBoost-based scheme installed at Bus 2 intends to cover faults applied at Bus 2, CC, and SC2.

An overview of the proposed XGBoost-based scheme is presented in Figure 6.4. The scheme operates based on the time-domain fault current measurements captured at one terminal of the cables and the DC side of the corresponding converters, as well as the fault voltage measurements obtained from the corresponding bus. Thus, there is no

requirement for communication and measurements transmission among the buses. The fault is classified in order to determine the faulted element within the protection zone or the presence of an external faults beyond the protection zone. Following the fault classification, the output of the XGBoost-based scheme is the desirable tripping signal that triggers the appropriate CB to clear the fault within the protection zone. Conversely, during a detected external fault the XGBoost-based protection shall remain stable. It should be noted that this work focuses on investigating the operation of the developed scheme up to the initiation of the tripping signal and does not cover the operation of the CB.

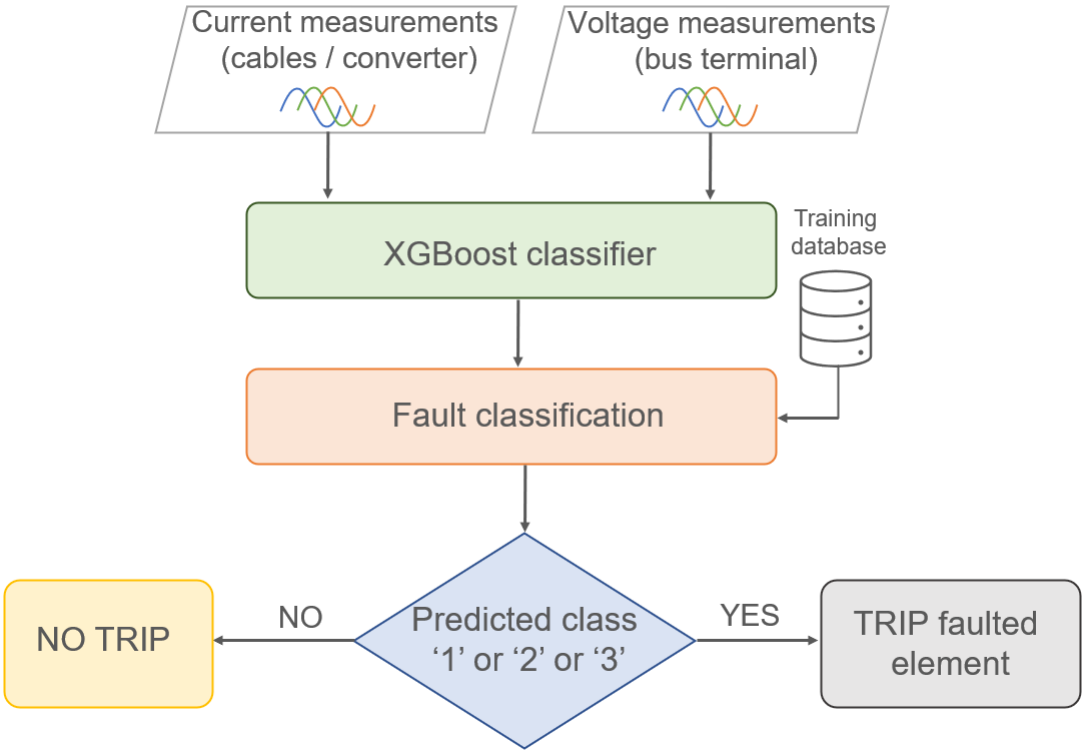

Figure 6.4: Overview of the XGBoost-based protection scheme for fault detection and classification in multi-terminal HVDC systems with SCs.

For the practical implementation of the proposed scheme, the design depicted in Figure 6.5 has been devised according to [238] which adheres to modern substation protection standards [253, 254]. As can be seen in Figure 6.5, Merging Units (MUs) could be installed to acquire the local current and voltage measurements based on the IEC 61869 standard. The MUs perform all the data processing, accounting for sampling and digitisation, and transmit the digital output of the current and voltage measurements to the centralised protection scheme via Ethernet using the IEC $61850-9-2$ protocol. The

protection functions are assumed to be implemented within the XGBoost-based scheme, while for the realisation of the fault clearance, the initiated tripping signal can be sent to the corresponding CBs via the Generic Object Oriented Substation Event (GOOSE) protocol defined by the IEC 61850 standard.

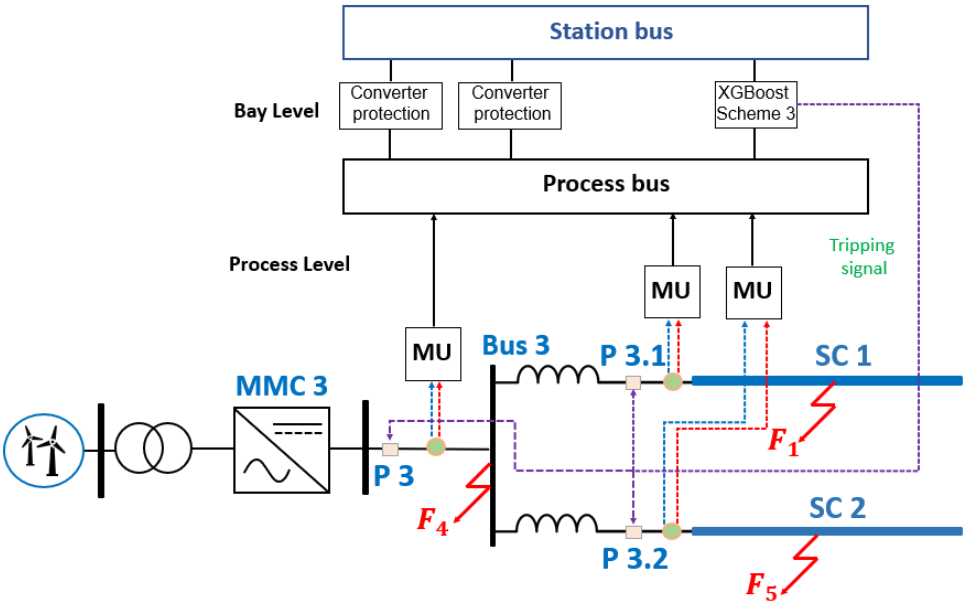

Figure 6.5: Outline of the practical implementation of the centralised XGBoost-based scheme installed at Bus 3.

The following subsections present the different stages that were followed during the development of the proposed scheme based on XGBoost.

6.3.1 Data generation and acquisition

Initially, with the scope of generating a diverse dataset, several fault scenarios were simulated using the system illustrated in Figure 6.1. The system parameters that have been modified during the iterative simulation process include the fault type, fault resistance, and fault position. Specifically, the fault scenarios include PP, PG, and NG fault types occurring at every 10% of SC1, SC2, and CC's length, as well as faults applied at the buses. For the resistive faults, 20 values of R_f have been considered within the range of 0 Ω to 350 Ω. The maximum fault resistance of 350 Ω has been selected as a typical value for highly-resistive faults in HVDC systems as reported in the technical literature [255–258]. The initial dataset is composed of 1800 fault scenarios.

During the simulation studies, 200 pre-fault and 200 post-fault samples of the current and voltage measurements were recorded and during the data acquisition process, the

generated signals are captured with a sampling frequency of 20 kHz which has been extensively investigated for protection applications in HVDC systems [40, 259]. The number of samples has been selected in order to preserve a high level of accuracy for fault detection and classification, and a low level of computational complexity. It should also be highlighted that even though IEC $61869-9$ has promoted the sampling frequency of 96 kHz for DC applications, the proposed scheme has demonstrated effective fault detection and classification accuracy and operational speed even at lower sampling frequencies. In particular, it has been found that a sampling frequency of 20 kHz is sufficient to meet the protection requirements while reducing computational needs.

6.3.2 Data pre-processing

One of the main advantages of tree-based algorithms, such as the XGBoost model, compared to other AI techniques, is the low requirements on data preparation [212]. Therefore, there is no need for extensive pre-processing of the obtained voltage and current measurements.

The final Python-based dataset has been formed based on the captured time-domain current and voltage measurements, without considering other features (i.e., current or voltage derivative) or transformations (i.e., WT). Prior to the training of the developed algorithm, the initial dataset was split into smaller datasets. Specifically, 80% of the initial dataset was used for training, while the remaining 20% for the testing of the XGBoost model. It should be noted that XGBoost has the capability to perform internal CV, hence it is not necessary to create a separate validation dataset.

6.3.3 Multi-class classification

The acquired current and voltage measurements are used as inputs to the XGBoost-based scheme to detect the presence of a fault and identify the faulted element. During the training process, the voltage and current measurements have been contaminated with random noise in order to represent the possible impact of noisy measurements on the fault detection and classification. Specifically, random noise within the range of 80 to 130 SNR have been added to the training dataset. This range of noise has been selected in order to consider reasonable levels of noise based on the selected sampling frequency and the voltage levels. Lower and higher levels of noise will be investigated during the testing process.

In the presented work, the fault detection and classification tasks have been formed as a multi-class classification problem. Specifically, for the scheme installed at Bus 3 (Figure 6.5) (which is the investigated centralised scheme), the XGBoost classifier initiates output '1' indicating faults at SC1, '2' indicating faults at SC2 and '3' for faults at Bus 3. Conversely, when the XGBoost output is '0', the presence of an external fault beyond the protection zone (i.e., fault at CC, Bus 1 and Bus 2) is identified. The correspondence between the predicted classes and the faulted element for the developed XGBoost-based scheme installed at Bus 3 is given in Table 6.1:

Table 6.1: Correspondence between predicted class and fault type for the developed XGBoost-based scheme installed at Bus 3.

XGBoost-based scheme	**Class**	**Fault**
at Bus 3	1	at SC1
	2	at SC2
	3	at Bus 3
	0	external

It is important to note that the detection of a fault within the protection zone (faults which belong to classes 1, 2, or 3) will lead to the initiation of the relative tripping signal, while faults classified as 0 indicate the absence of a tripping signal. The following subsection presents the advantages of the XGBoost model and justifies its selection for the development of the proposed scheme.

6.3.3.1 XGBoost algorithm for multi-class classification

The XGBoost algorithm is a decision tree-based ensemble model which is designed to be very efficient and easily applicable in fault management applications with tabular data [212]. The state-of-the-art XGBoost algorithms are very flexible and robust for complex classification problems as they combine the advantages of the tree-based ML algorithms with lower computational complexity and hence higher computational speed [260]. In particular, XGBoost operation depends on the modelling of tree algorithms, selecting different features of the initial dataset, and creating the conditional nodes. The boosting term refers to an ensemble ML method according to which weak learners are trained sequentially and combined to build a stronger learner with better predictive performance. Based on the main principles of the Gradient Boosting (GBM) framework, which constitutes the core of the XGBoost algorithm, during the training process each weak learner tries to eliminate the weaknesses of its predecessor, resulting in strong

learners with a high degree of accuracy.

The operation of the XGBoost algorithm is dependent on the minimisation of the objective function given by (6.1), using gradient descent:

$$Obj = \sum_{n}^{i=1} l(y_i, \hat{y_i}^{(t-1)} + f_t(x_i)) + \Omega(ft) \tag{6.1}$$

where l is the loss function which represents how well the model fits on the training dataset, $\hat{y_i}^{(t-1)}$ is the previous model at $t-1$, $f_t(x_i)$ is the new model, and $\Omega(ft)$ represents the regularisation function which measures the complexity of the trees.

The regularrisation terms on the tree structure are given by (6.2) [263]:

$$Omega(ft) = \gamma T_{\frac{1}{2}} \lambda \sum_{j=1}^{\gamma} (w_j^2) \tag{6.2}$$

where, T i the number of leaf nodes, w_j is the value predicted by the $j-th$ leaf node. The formula in (6.3) can be derived by performing the second-order Taylor expansion of the loss function [262]

$$\Omega(ft) = \sum_{j=1}^{T} [G_j w_j + \frac{1}{2}(H_j + \lambda) w_j^2] + \gamma T \tag{6.3}$$

where G_j and H_j can by expressed by (**??**) [263]:

$$G_j = \sum_{i \in 1} \nabla_{F_{t-1}} l(y_i F_{t-1}(x_i)) \tag{6.4}$$

$$H_j = \sum_{i \in 1} \nabla^2_{F_{t-1}} l(y_i F_{t-1}(x_i)) \tag{6.5}$$

Once the configuration of the decision tree has been established, the predicted values for each leaf node can be derived by setting the derivative of the loss function to zero, which can be expressed as follows [264]

$$w*_j = -\frac{G_j}{H_j + \lambda} \tag{6.6}$$

Nevertheless, identifying the best structure among all possible tree structures poses a challenging NP-hard problem. In real-world scenarios, a greedy approach is frequently employed to build a less-than-optimal tree structure. The fundamental concept involves iteratively dividing one leaf node at a time starting from the root node, and making the

split decision based on predefined criteria for each potential division [261]. XGBoost also employs specific criteria to determine the optimal splits. By incorporating the predicted value into the loss function, it becomes possible to achieve the minimum value of the loss function.

$$L_t^* = -\frac{1}{2}\sum_{j=1}^{T}\frac{G_j^2}{H_j+\lambda} + \gamma T \tag{6.7}$$

The Gain can be easily computed as the difference between the loss function before and after a split, as demonstrated below based on (6.8):

$$Gain = \frac{G_L^2}{H +_L +\lambda} + \frac{G_R^2}{H +_R +\lambda} + \frac{G_L^2 + G_R^2}{H +_L +H_R + \lambda} \tag{6.8}$$

In the context of XGBoost, the primary criterion for constructing the decision tree is to maximise the difference in the loss function before and after splitting. It's evident that a larger difference corresponds to a reduced overall loss function. By systematically examining all feature values, it identifies the optimal splitting point when the difference in the loss function before and after the split is at its maximum.

There are many comparative analyses reported in literature which highlight the advantages of the XGBoost algorithm over others. Particularly, authors in [265] demonstrate that the XGBoost algorithm is a scalable ensemble technique which outperforms gradient boosting and random forests classifiers in terms of accuracy and computational speed. The work conducted in [266] and [261] indicate that for more complex problems, the XGBoost algorithm provides a higher degree of accuracy compared to ANN and SVM classifiers, respectively, while concurrently reducing the execution time and the computational complexity. Furthermore, for multi-class classification problems, ANN algorithms require extensive tuning, both in parameters and model architecture, while the XGBoost algorithm performs well without extensive parameters tuning. The unique features of the XGBoost algorithm for fault diagnosis problems are presented in [212, 262, 267, 268] and the studies revealed that the XGBoost algorithm is a robust, computationally efficient algorithm which presents faster and more accurate results over other ML models. The main advantages offered by the XGBoost algorithm are listed as follows and showcase the superiority of the selected algorithm compared to other classification models:

- Fastest implementation of the GBM tree-based algorithms [266].
- Higher efficiency compared to conventional artificial neural network classifiers [260].

- Incorporates provision of regularisation, reducing over-fitting to the training dataset, and presenting enhanced generalisation capability.
- Utilises the power of the parallel pressing resulting in less computational time.

Therefore, the XGBoost algorithm combines efficiency, operational speed, and increased generalisation capability which are attributes very important for fault management problems.

In the presented work, in order to select the XGBoost model with the best prediction performance, hyperparameter tuning was performed prior to the commencement of the actual learning process. For this purpose, the training dataset was divided into 5-folds ($k = 5$) and each combination of hyperparameters is subjected to the 5-fold CV for the determination of the optimum combination. The 5-fold CV has been implemented based on the 'GridSearchCV' scikit-learn class, and as CV score the F1-score was selected. All the experiments were executed using AMD Ryzen 9 5900HX 16-core, 12-thread, 16GB cache up to 4.0 GHz max boost processor.

The optimum hyperparameters of the developed XGBoost scheme are presented in Table 6.2.

Table 6.2: Simulation scenarios

Hyperparameter	**Value**
booster	gbtree
alpha	10
number of estimators	200
lambda	1
maximum tree depth	3
learning rate	0.1

6.3.4 XGBoost-based scheme time delays

Prior to the testing of the developed scheme, for a realistic implementation, all the anticipated time delays within the HVDC substation should be identified. The expected total operating time of the XGBoost scheme, t_{op}, is calculated based on (6.9) and consists of time delays associated with the data processing, t_d, (including measurements digitisation and communication) and the XGBoost algorithm execution, $t_{XGBoost}$, (time required for the algorithm to provide the output signal). It should be noted that during the trial and error process for the XGBoost-based scheme, it was observed that the

utilisation of a window-based process does not enhance the performance of the developed scheme:

$$t_{op} = t_d + t_{XGBoost} \tag{6.9}$$

The developed protection philosophy at each bus is based on current and voltage measurements from all the cables and the converter attached to the corresponding DC bus. Considering the use of MUs as illustrated in Fig. 6.5 and an Ethernet switch for realisation of IEC 61850, the maximum anticipated time delay, t_d is given by (6.10):

$$t_d = t_s + t_{MU} + t_{Eth} + t_{pp} \tag{6.10}$$

where t_s denotes the maximum time delay resulting from the analogue sampling (i.e., t_s=50 μs); t_{MU} is the time required to encode the sampled values in the MUs and can be estimated at 12 μs according to [159]; t_{Eth} is the maximum time delay imposed by the Ethernet link latency and is estimated at 6.34 μs based on [238]; and t_{pp} is 9.5 μs, relying on the work conducted in [159], and refers to the maximum time required for the protection system to decode the sampled values. Therefore, the total t_d is 77.84 μs.

Finally, the time delay associated with the XGBoost algorithm, $t_{XGBoost}$, is determined by considering many factors accounting for coding efficiency and the power of the processing system. The total t_{op} of the proposed scheme will be assessed experimentally in the following section.

6.4 Simulation Results and Validation of the XGBoost-Based Scheme

The effectiveness and generalisation capability of the XGBoost-based scheme have been validated using proper evaluation metrics and time assessment studies. Initially, the ability of the developed scheme to detect and classify correctly different faults was evaluated on the testing dataset, considering the F1-score as the evaluation metric. Furthermore, real-time assessment studies were carried out using a SIL testing platform in order to validate the operation speed and thus the suitability of the proposed scheme for real-time implementation. Additionally, the performance of the scheme has been tested against the addition of noise in voltage and current time-domain measurements, emulating potential effects arisen by measurement-related noise.

6.4.1 F1-score evaluation

The F1-score is a widely used evaluation metric in ML applications. In particular, the F1-score provides a combination between the precision and recall evaluation metrics, considering the impact of both FP and FN predictions, respectively. The XGBoost classifier was tested using the allotted 20% of the initial dataset. The split of the initial dataset to 80% for training and the remaining 20% for testing is a common practice utilised in ML applications [158]. Table 6.3 shows the normalised confusion matrix generated during the testing process.

Table 6.3: XGBoost confusion matrix.

Actual / Predicted Condition	**Predicted Negative**	**Predicted Positive**
Actual Negative	TN=96%	FP=0.5%
Actual Positive	FN=3%	TP=98%

As concluded by Table 6.3, the high percentage of TP predictions indicates the number of samples which have been identified correctly as positives. Therefore, the high percentage of TP confirms the capability of the developed scheme to detect and classify correctly the faults within the protection zone. The increased value of TN percentage indicates the number of samples which have been correctly identified as negative. From a protection perspective, the high percentage of TN validates the stability of the developed scheme against external faults and thus confirms its discrimination capability. Regarding the percentage of FP which indicate the false initialisation of the tripping signal for an external fault, and the FN percentage which refers to the failure of tripping signal initiation for an internal fault, both are very low, validating the high degree of protection reliability and dependability. The total F1-score is calculated based on (4.25) in Chapter 4. From the values in the confusion matrix presented in Table 6.3, the final value of the F1-score is 98%.

6.4.2 Sensitivity analysis regarding train-test dataset split

In this subsection a sensitivity analysis was performed with respect to the train-test split percentages in order to evaluate the initial selection (80% of initial dataset for training and the remaining 20% for testing) and investigate its impact on the performance of the XGBoost model. For this purpose, the developed XGBoost model was tested on 35% of the initial dataset (the remaining 65% was utilised for training) and 50% of the initial dataset (the remaining 50% was utilised for training). Similar to sub-section 6.4.1, the

evaluation was performed based on the F1-score.

Table 6.4 and Table 6.5 present the normalised confusion matrices generated during the testing process on 35 % and 50 % of the initial dataset, respectively.

Table 6.4: XGBoost confusion matrix fro train-test split percentage of 65%-35%.

Actual / Predicted Condition	**Predicted Negative**	**Predicted Positive**
Actual Negative	TN=85%	FP=3%
Actual Positive	FN=11%	TP=90%

Table 6.5: XGBoost confusion matrix fro train-test split percentage of 50%-50%.

Actual / Predicted Condition	**Predicted Negative**	**Predicted Positive**
Actual Negative	TN=78%	FP=4%
Actual Positive	FN=27%	TP=86%

The resulting F1-score for the train-test split percentage of 65%-35% is 92%, and 84% for the train-test split percentage of 50%-50%. Therefore, it can be concluded that as the percentage of the initial dataset utilised for training is reduced, and thus the training set representativeness decreases, the resulting F1-score decreases as well. Specifically, as the percentage of the initial dataset assigned to the training process is reduced, the percentage of FP predictions increases, resulting in the false initiation of the tripping signal for faults beyond the protection zone and, hence, diminishes protection security. An increase is also observed in the percentage of FNs, which indicates the failure of tripping signal initiation, jeopardising the protection dependability and reliability. Conversely, as the percentage of the initial dataset utilised for training decreases, the resulting percentages of TP and TN predictions are reduced, affecting the protection sensitivity and stability, respectively. Based on the obtained results, the XGBoost algorithm trained with 80% of the initial dataset was selected for the presented studies.

6.4.3 Software in the loop testing for real-time validation

This subsection presents the results of the real-time assessment of the XGBoost-based scheme, considering realistic digital infrastructure. The ultimate goal is to acquire a deeper insight of the time response of the proposed scheme to validate its performance for real-time implementation. On that front, the performance of the XGBoost-based scheme at Bus 3 (illustrated in Figure 6.5) was tested with respect to time required for the initiation of the tripping signal. The assessment was conducted utilising the testing environment in Figure 6.6, which forms a real-time SIL platform. This is similar to the

real-time SIL set-up utilised for the ANN and SVM based schemes in Chapter 3.

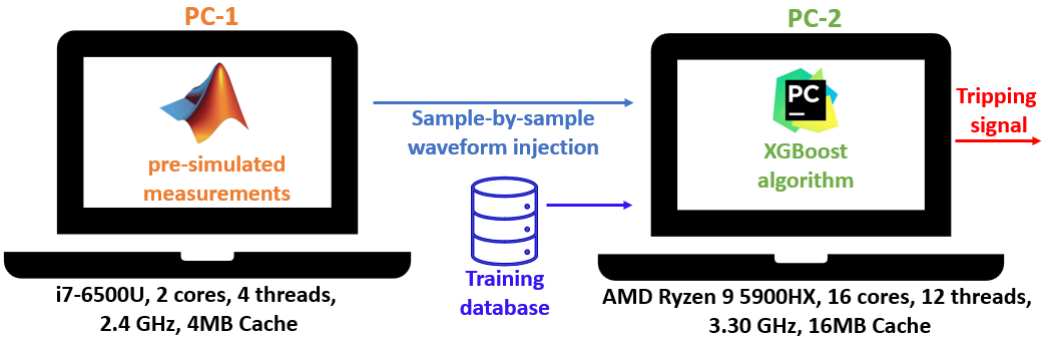

Figure 6.6: Overview of SIL testing environment used for time performance assessment of the XGBoost-based scheme at Bus 3.

A variety of fault scenarios were simulated utilising the network depicted in Figure 6.1, and the corresponding voltage and current measurements were extracted for post-processing. The simulated database was stored in PC-1 and the signatures were injected sample-by-sample to PC-2 through TCP/IP sockets configuration. The final trained XGBoost-based scheme was stored in PC-2 in order to generate the tripping signal. The specifications of PC-1 and PC-2 are presented in Figure 6.6.

Indicatively, Figure 6.7 shows the simulation results of a PP solid fault applied at 58% of SC1's length, at $t = 5\ ms$, which quantifies the time performance of the XGBoost-based scheme installed at Bus 3. Figure 6.7a to Figure 6.7c illustrate the utilised voltage and current measurements, accounting for the currents measured at the terminal of SC1, SC2 (Figure 6.7a), the DC side of converter MMC3 (Figure 6.7b), and the DC voltage at Bus 3 (Figure 6.7c). As it can be seen in Figure 6.7d, the fault is detected by the proposed scheme and the corresponding tripping signal is initiated approximately 0.5 ms after the fault occurrence. Thus the fault is detected within the time requirements of HVDC protection.

Furthermore, during the real-time SIL testing, the performance of the XGBoost-based scheme was evaluated on 200 previously unseen fault scenarios. The principal objective of this assessment is to further validate the generalisation capability of the proposed scheme against measurements which are not part of the training or testing datasets and evaluate the time response of the XGBoost-based scheme. Some of the results are presented in Table 6.6 and establish the effectiveness of the proposed protection philosophy. Specifically, the proposed scheme detects and classifies correctly the faults within the protection zone (i.e., faults applied at SC1, SC2, and Bus 3) and provide

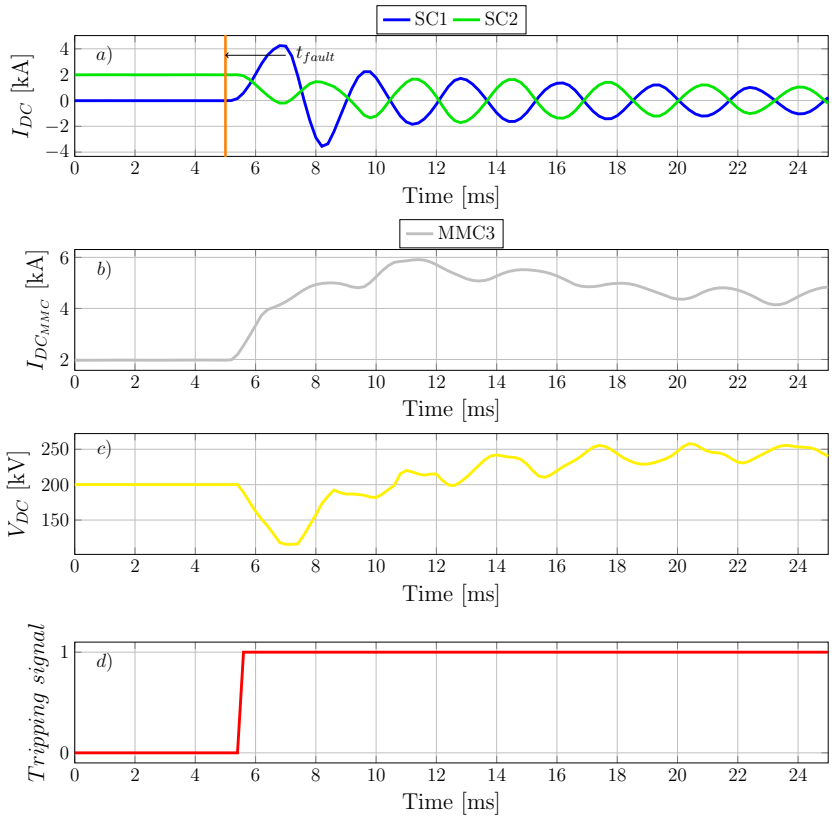

Figure 6.7: Overview of SIL testing environment used for time performance assessment of the XGBoost-based scheme.

the corresponding tripping signal (even during highly-resistive faults). Conversely, the scheme remains stable against external faults (faults applied on CC, Bus 1, and Bus 2) which belong to the protection zones of XGBoost schemes installed at Bus 1 and Bus 2. Regarding the operation time, which is of paramount importance in HVDC systems, the tripping signal is initiated within the time range of 0.0803 ms to 1.2341 ms, providing an average time of 0.2571 ms. Therefore, it can be concluded that the proposed scheme fulfills all the requirements of an effective protection solution for HVDC systems with SCs, accounting for increased discrimination, security, stability, and operational speed.

6.4.4 Impact of noise

The analysis presented in this subsection investigates the impact of noise on the performance of the proposed scheme. In practice, unwanted distortion may be introduced within the measurements emanating from quality issues in sensing and measuring equipment. Therefore, to de-risk the proposed scheme and validate its effectiveness under such conditions, the time-domain current and voltage measurements of the testing scenarios,

Table 6.6: Time performance of the XGBoost-based scheme installed at Bus 3 during previously unseen fault scenarios.

Faulted element	Fault type	Rf [Ω]	Location %	t_{op} [ms]	Faulted element	Fault type	Rf [Ω]	Location %	t_{op} [ms]
		0	0.50	0.0898			0	-	Stable
		2	15	0.0988			2	-	Stable
	PP	5	45	0.1091		PP	5	-	Stable
		50	65	0.1591			50	-	Stable
		300	99	0.2018			300	-	Stable
		0	87	0.0988			45	-	Stable
		100	1	0.1068			10	-	Stable
SC1		0	0.20	0.0901	Bus 1		0	-	Stable
		1	1.4	0.0951			1	-	Stable
	PG	10	32	0.0908		Positive PG	10	-	Stable
		30	74	0.1009			30	-	Stable
		350	98.90	1.0890			350	-	Stable
		2	92	0.1073			100	-	Stable
		95	20	1.0113			4	-	Stable
		0	1	0.0938			0	-	Stable
		3	13	0.0920			3	-	Stable
	NG	15	25.60	0.0901		NG	15	-	Stable
		25	58.90	0.1256			25	-	Stable
		1	0.05	0.0582			1	-	Stable
		0	97	1.0982			200	-	Stable
		100	98	0.1911			67	-	Stable
		0	2	0.0997			0	-	Stable
		2	17	0.0988			2	-	Stable
	PP	5	38	0.1003		PP	5	-	Stable
		50	49.50	0.1024			50	-	Stable
		300	64.90	0.1109			300	-	Stable
		350	12.5	0.1219			11	-	Stable
		3	75.2	0.9876			88	-	Stable
SC2		0	8	0.0956	Bus 2		0	-	Stable
		1	21	1.0841			1	-	Stable
	PG	10	37	1.0943		PG	10	-	Stable
		30	44.20	1.0928			30	-	Stable
		100	21.2	1.0867			35	-	Stable
		350	92	1.2341			350	-	Stable
		0	99	0.0431			16	-	Stable
		0	49.80	0.0998			0		Stable
		3	59	0.1023			3	-	Stable
	NG	15	81	0.1025		NG	15	-	Stable
		25	69.90	0.1037			25	-	Stable
		200	96	1.0984			200	-	Stable
		90	13.5	1.1014			100	-	Stable
		0	93.8	1.0004			1	-	Stable
		0	-	0.0827			0	0.89	Stable
		2	-	0.0838			2	12	Stable
	PP	5	-	0.0889		PP	5	48	Stable
		50	-	0.0908			50	67	Stable
		1	-	0.0887			100	0.4	Stable
		300	-	0.0907			300	99	Stable
		100	-	1.3104			1	88	Stable
Bus 3		0	-	0.0813	CC		0	3	Stable
		1	-	0.0921			1	18	Stable
	PG	10	-	0.0942		PG	10	47	Stable
		30	-	0.1022			30	85.3	Stable
		350	-	0.1030			350	91	Stable
		0.5	-	0.0532			100	11.1	Stable
		60	-	0.1702			2	76.7	Stable
		0	-	0.0803			0	2	Stable
		3	-	0.1012			3	27	Stable
	NG	15	-	0.0989		NG	15	58	Stable
		25	-	0.0832			25	76.7	Stable
		100	-	0.1355			100	18.2	Stable
		200	-	0.1540			200	98.8	Stable
		2	-	0.0849			2	5.6	Stable

investigated in section 6.4.3, have been contaminated with artificial noise. Figure 6.8 shows the fault current and voltage measurements of Figure 6.7 after the addition of artificial noise (SNR=30 dB).

It is worth reiterating that the XGBoost-based scheme has been trained on data with random noise within the range of 80 to 100 SNR. The presented results aim to confirm

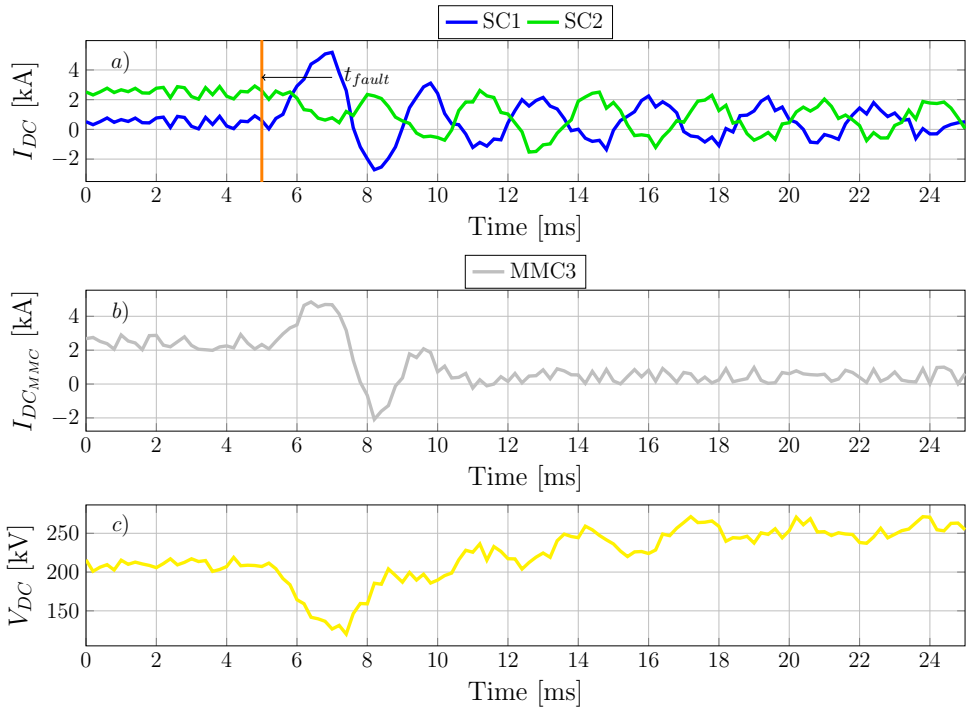

Figure 6.8: Current and voltage measurements after the addition of 30 dB noise.

the generalisation capability and the time response of the proposed scheme under the influence of a wider range of noise.

The final results are presented in Table 6.7 and show the maximum and average tripping time, t_{op}, of the XGBoost-based scheme installed at Bus 3. From the resulting time values, it is concluded that as the noise level increases (the value of the SNR decreases), the value of the t_{op} remains approximately the same.

More specifically, for the detection of the faults on SC1, the maximum t_{op} is 1.0982 ms for SNR 100 dB. For the same SNR, the average t_{op} is 0.2416 ms, while for SNR 30 dB, the maximum t_{op} is 1.0981 ms and the average t_{op} is 0.2412 ms. It is observed that an increase in the additive noise causes a minor change in the operational speed of the XGBoost-based scheme. The same trend is presented in the detection of the faults on SC2 and Bus 3. Furthermore, the proposed scheme remains stable during faults on CC, Bus 1, and Bus 2. Therefore, it is inferred that the performance of the developed scheme is not jeopardised by the addition of the noise.

6.5 Discussion

A novel centralised (on the substation level) protection scheme with fault detection and classification elements has been proposed for multi-terminal HVDC grid with DC SCs.

Table 6.7: Time performance of the XGBoost-based scheme considering artificial noise to current and voltage measurements of the testing scenarios.

SNR [dB]	SC1		SC2		Bus 3		Bus 1		Bus 2		CC	
	t_{op} max [ms]	t_{op} avg [ms]	t_{op} max [ms]	t_{op} avg [ms]	t_{op} max [ms]	t_{op} avg [ms]	t_{op} max [ms]	t_{op} avg [ms]	t_{op} max [ms]	t_{op} avg [ms]	t_{op} max [ms]	t_{op} avg [ms]
∞	1.0982	0.2416	1.2341	0.3513	0.1543	0.0952	Stable	Stable	Stable	Stable	Stable	Stable
100	1.0983	0.2415	1.2341	0.3513	0.1543	0.0952	Stable	Stable	Stable	Stable	Stable	Stable
80	1.0983	0.2415	1.2341	0.3512	0.1543	0.0951	Stable	Stable	Stable	Stable	Stable	Stable
60	1.0983	0.2414	1.2341	0.3512	0.1541	0.0949	Stable	Stable	Stable	Stable	Stable	Stable
30	1.0981	0.2412	1.2339	0.3510	0.1538	0.0944	Stable	Stable	Stable	Stable	Stable	Stable

The developed scheme utilises the principles of the XGBoost algorithm and protects the system against faults occurring along the cables (SCs and CC) and the buses. The results of the validation studies have highlighted the following key points:

- The proposed XGBoost-based scheme has been found to present high levels of sensitivity, stability, selectivity, and increased operational speed during different fault scenarios. These include various PP P-G and N-G faults, different fault locations, and different fault resistances.
- The XGBoost-based scheme presents increased sensitivity by initiating a fast tripping signal during the highly-resistive internal faults, while remaining stable during external faults.
- The accurate activation of the tripping signal, during all investigated scenarios, demonstrates the increased selectivity of the proposed scheme, highlighting its ability to effectively identify and classify the faulty components while keeping the unaffected parts operational. This capability enhances the system's overall reliability.
- The results from the real-time SIL testing validated the fast and accurate fault detection and classification under various fault conditions and consequently highlighted the applicability of the developed scheme for real-time implementation. Specifically, the results showed that the operation time lies within the range of 0.0803 ms and 1.2341 ms, which complies with the protection requirements for HVDC grids.
- The proposed protection scheme presents robustness against noisy measurements.

6.6 Summary

This chapter has presented a centralised protection scheme (at the substation level) for multi-terminal HVDC systems with SCs. It has been shown that the secure and reliable

operation of HVDC grids with DC SCs introduces the need for discriminative, fast, and sensitive protection solutions in order to comply with HVDC protection requirements and address the particularities of SC technologies.

Initially, a literature review on the existing HVDC protection solutions has been carried out and the key observations concluded the limitations of existing schemes to provide reliable protection for DC SCs in HVDC systems. To build upon this, a qualification assessment of widely used protection schemes in HVDC systems, such as current and voltage derivative-based schemes, has been presented and the results highlighted that the threshold-based protection schemes result in a trade-off between protection sensitivity and stability. Considering the restrictions of existing schemes, and the ever-increasing availability of data in future power grids, this chapter demonstrated the development of a novel data driven protection scheme which is comprised of fault detection and classification elements, exploiting the strong learning capabilities of the XGBoost algorithm.

The proposed scheme has been assessed based on offline simulations and real-time studies. The results showed that the XGBoost-based scheme can provide fast and discriminative protection for faults applied at the SCs, conventional cable, and buses (both solid and highly-resistive). This has been validated in detailed transient simulations and utilising AI evaluation metrics such as the F1-score. The resulting F1-score has been found to be equal to 98%, which confirms that the developed scheme can correctly detect and classify all internal faults and also classify correctly, and remain stable for, external faults beyond the protection zone. This evaluation underscores the increased sensitivity towards internal faults, the robust stability when dealing with external faults, beyond the protection zone, and the enhanced selectivity of the proposed scheme in effectively initiating a tripping signal for the corresponding CB. In particular, the XGBoost-based protection scheme demonstrates increased sensitivity, as evidenced by a significant rise in TPs and a corresponding decrease in FNs. Additionally, the scheme's stability is affirmed by the high percentages of TNs and a reduction in FPs. Furthermore, the developed scheme's selectivity is underscored by the notable decrease in the resulting FP values. The results from the real-time SIL testing validated the fast and accurate fault detection and classification under various fault conditions and consequently highlighted the applicability of the developed scheme for real-time implementation. Specifically, the results showed that the operation time lies within the range of 0.0803 ms and 1.2341 ms,

which complies with the protection requirements for HVDC grids. Furthermore, the XGBoost-based scheme presents increased discrimination capability by initiating a fast tripping signal during the highly-resistive internal faults and remaining stable during external faults. Additionally, the generalisation capability of the proposed scheme has been tested under the influence of noise. The results verified the robust performance of the XGBoost-based scheme despite noisy measurements. To conclude, the proposed scheme is suitable for the detection and classification of faults in HVDC grids with SCs, and can be considered a very promising solution for the implementation of fast and reliable DC bus and DC SC protection.

Chapter 7

Conclusions and Future Work

This chapter provides a summary of the key findings and contributions of the research, concluding the entire thesis. In addition, it suggests future work.

7.1 Summary and Key Outcomes

Chapter 1 of this thesis presented a discussion supporting the need for bulk power corridors to accelerate the decarbonisation of power systems and accommodate changes in grid infrastructure. The chapter emphasises the significant role that AC and DC SCs are expected to play in future power grids, owing to their numerous advantages, including bulk power transfer over long distances at lower voltage levels with minimal losses. As research into superconducting-based applications advances, SCs are increasingly viewed as a cost-effective solution to facilitate the integration of renewable generation from remote areas. Nevertheless, the deployment of SCs in power grids presents significant challenges, particularly regarding fault-related issues, which have been highlighted as a matter of major importance. The unique electro-thermal properties of SCs add complexity to the fault management of this technology. Thus, the main motivation of this work is the development of reliable and effective fault management solutions, including protection and fault location applications, to ensure the safe operation and increased reliability of SC systems. Initially, the research gap in the area of fault management of systems with SCs has been identified, which is followed by an overview of the research methodology and the analysis of the main contributions of this thesis. Furthermore, this chapter discussed the progressive deployment of AI-based techniques in power system applications, including protection and fault location applications. As the fault management of SCs is

a multi-variable problem, AI-based methods with strong learning capabilities have been deemed a viable solution to tackle this challenge and, therefore, have been selected as the primary tool for developing the proposed solutions.

Chapter 2 provided a theoretical background of superconductors and the quenching phenomenon. The chapter described the structure of SCs, starting from the HTS tapes that form the core of SC manufacturing and proceeding to the arrangement of HTS in SCs, along with an overview of the advantages and drawbacks of different SC configurations. It has been pointed out that the proper selection of SC configuration is based on voltage levels and cost considerations. Specifically, it has been highlighted that:

- The concentric configuration of AC SCs presents a compact size, reduced cryogenic surface area, utilisation of superconducting material, and cost. It also offers higher current-carrying capacity and lower inductance compared to other configurations. However, the non-uniform current distribution among HTS tapes makes the manufacturing process challenging. This design is preferred for voltage levels between 13.8 kV and 50 kV.

- Triad SCs are recommended for voltage levels higher than 66 kV and offer uniform current distribution among HTS tapes. However, this configuration requires the addition of a HTS shield layer, resulting in increased cost.

- Single-core SCs are recommended for voltages up to 138 kV for bulk power transmission over long distances. In this configuration each conductor is contained in separate cryostats, which significantly increases the cost, as each conductor requires separate inlet and outlet paths for cooling.

Furthermore, SCs are classified based on the type of dielectric used and their operating temperature. In particular:

- CD SCs exhibit higher cooling efficiency due to their larger cooling surface area. This makes them suitable for applications where efficient cooling is critical, such as large-scale power transmission. However, they may require more complex cooling systems to maintain the required low temperatures.

- WD SCs have reduced cooling power requirements due to their dielectric layer not being immersed in the cooling liquid. This design makes them more suitable for applications where cooling requirements are less stringent, and the higher operating

temperature is more manageable. WD SCs are characterised by higher inductances and capacitances, which can limit their applicability in certain applications.

Moreover, the chapter presented the mathematical formulation for the electro-thermal modelling of AC and DC SCs. This involved adopting the electrical equivalent of commercially available $2G$ HTS tapes and the electro-thermal analogy, to simplify the coupling between electrical and thermal phenomena in SCs and consequently represent the quenching of HTS tapes.

Chapter 3 described the outcomes of a detailed, simulation-based transient analysis of AC and DC SCs. The analysis was conducted to obtain a better understanding of the fault response of SCs, identify challenges from a fault management perspective, and lay the groundwork for the development of protection and fault location solutions. The studies presented in this chapter considered various fault scenarios and transient events and the analysis has been conducted based on the obtained current and voltage waveforms. For that purpose, the developed models of AC and DC SCs have been integrated within an AC transmission system with penetration of ICGs and a multi-terminal HVDC network with MMCs.

From the analysis, the following key observations can be reflected:

- During the quenching process, AC and DC SCs present fault current limiting capability, due to the rapid increase in the equivalent resistance, which leads to the suppression of the current magnitudes. Furthermore, the presence of high resistance during quenching leads to the appearance of residual voltage during faults. These effects impose a significant challenge on the existing current and voltage based protection schemes (i.e., over-current and distance protection) and constitute important aspects which should be considered for the effective fault management of AC and DC SCs.

- During highly-resistive faults, the fault current is predominately limited by the fault resistance resulting in a fault current magnitude lower than the critical current of the HTS tapes. Consequently, the quenching process is jeopardised, complicating the fault detection and location processes on AC and DC SCs. To address this challenge, increased sensitivity of the fault detection schemes is a prerequisite for the safe operation of such cables.

- The presence of other disturbances, such as load switching events and external

faults can lead to the quenching of AC and DC SCs, threatening the discrimination of protection and accuracy of fault location schemes. Hence, for reliable operation, protection solutions with a high degree of selectivity and stability, and fault location schemes with increased accuracy, are required.

- Termination inductors affect the current in HVDC systems by reducing the rate of change of current during a fault. Therefore, it is important to carefully consider the design of termination inductors, their impact on the quenching, and consequently the fault management of SCs.

Chapter 4 proposed two data-driven protection schemes incorporating fault detection and classification elements for MV AC systems with SCs. Initially, protection assessment studies were conducted to assess the efficacy of over-current threshold-based protection schemes, which are commonly used for MV AC system protection. The outcomes of these studies revealed that the performance of these protection methods is compromised by SC quenching and fault resistance, creating a trade-off between protection, sensitivity, and stability.

In view of these limitations, this chapter explored the potential of AI techniques for fault management of AC SCs. Specifically, it is demonstrated that AI-based techniques can handle complex, multi-variable problems such as AC system protection with SCs, and uncover latent information that can enhance the understanding of the power system response. Consequently, the proposed protection schemes leverage the advantages offered by AI methods, specifically ANN and SVM classifiers, in conjunction with signal processing techniques such as the WT. After thorough validation of both schemes for a series of scenarios including different fault types, location, and values of fault resistance as well as other transient events, the following noteworthy observations can be made.

- WT is proven to be an efficient feature extraction tool which reveals hidden information from the faulted voltage and current measurements.

- The proposed schemes have been found to be highly sensitive, even during highly-resistive faults, and stable against external faults and other disturbances.

- The performance of the schemes have been evaluated through detailed transient simulations and the results showed that the ANN algorithm detects correctly the internal faults with accuracy of 99.74%, while the SVM classifier with accuracy of 99.69%. Therefore, both algorithms increased discrimination capability by detecting

all types of internal faults and remaining stable against external faults and other transient events such as load switching events.

- The operational speed of the proposed schemes has been verified based on a SIL testing set-up which confirms the fast fault detection and initiation of the corresponding tripping signals. In particular, ANN and SVM algorithms detected the internal faults with average operation time of 1.47 ms and 2.91 ms, respectively. These average operation times are adequate as they result in rapid fault detection and classification, effectively minimising quenching propagation, preventing the SCs from reaching the critical temperature and consequently ensuring the system's safety.

- A sensitivity analysis, considering diverse hardware specifications, has revealed that the real-time implementation of the developed schemes can be realised using equipment characterised by comparatively modest specifications. The reduced financial burden associated with these schemes enhances their scalability and replicability, ultimately contributing to their widespread adoption and deployment as cost effective protection solutions.

- Both classifiers satisfy the requirements for sensitive, discriminative, and fast protection of AC systems with SCs. However, for comparison purposes it has been found that the ANN algorithm outperforms SVM in terms of the operational speed, presenting better capabilities for real-time implementation.

In Chapter 5 the challenges related to the fault location on AC SCs are discussed. It has been pointed out that the accurate estimation of the fault location is of paramount importance for the SC technology due to the complex configuration of such cables and the difficulties involved in the repair process. To address this issue, the chapter proposed a novel data-driven fault location scheme based on the CNN algorithm and the transformation of time-domain signals to the time-frequency domain.

The proposed scheme utilises measurements from one terminal of the AC SC and does not require time-synchronisation measurements. Its performance has been evaluated through detailed transient simulations that considered various fault scenarios and the impact of factors such as noisy measurements. In contrast to existing methods reported in the literature, which have limitations in terms of their deployment in superconducting-based grids, they account for the influence of variable resistance on the accuracy, the

electromagnetic theory of SCs, the requirement of time-synchronised measurements, and the need for external equipment. The proposed method provides accurate fault localisation, while addressing the aforementioned challenges. Validation studies demonstrate the following advantages of the proposed fault location scheme:

- The transformation of non-stationary signals from time domain to time-frequency domain is ideal for analysing signals concurrently in both domains. This approach provides a more complete analysis of signals, which can result in more accurate fault location estimation.

- The combination of AI algorithms with image analysis techniques provides the potential of improving the accuracy of feature extraction and identifying fault locations more precisely. Image analysis techniques have the ability to represent complex data in a simplified form, facilitating pattern recognition and reducing computational complexities. Additionally, these techniques demonstrate robustness when dealing with data that contains a significant amount of noise, which is particularly important in protection applications as measuring equipment is subject to noise, posing challenges to accurate fault detection and localisation.

- An extensive investigation of CNN algorithms with regards to the resulting mean fault location estimation error revealed that the Inception-v3 presents the best performance for the SC fault location problem.

- The proposed fault location scheme has been found to successfully estimate the fault location during all the investigated scenarios and maintain high accuracy of the fault location identification, even during highly-resistive and close-up faults, which are considered the most challenging. The mean fault location estimation error on the testing dataset has been found equal to 0.74%. According to the relevant technical literature, 0.74% mean fault location estimation error is low and based on the obtained results this low error rate reflects the efficacy and precision of the scheme in identifying fault locations and enabling prompt and accurate mitigation of faults in various situations, thus enhancing the overall reliability and performance of the system.

- The evaluation of the proposed scheme on previously unseen fault scenarios, resulting in a maximum fault location estimation error of 1.18% and a mean fault

location estimation error of 0.34%, demonstrates its outstanding performance and generalisation capability. The resulting errors are lower compared to error rates of existing schemes in the literature and indicates the scheme's robustness and adaptability to a wide range of situations, ensuring accurate and reliable fault location identification for maintaining the operational efficiency of the power system.

- The proposed scheme maintains increased accuracy against randomly varied sampling instants and changes in the inception angle. Specifically, for small variations of the actual fault position (i.e., 10 m), the resulting fault location estimation error ranges between 0.1% and 1.2%. The obtained error is low based on the relevant technical literature and indicates the scheme's robustness and precision in fault localisation.

- Sensitivity analysis revealed that a minimum sampling frequency of 20 kHz is sufficient for the adequate performance of the developed scheme. The selection of 20 kHz is consistent with established industry standards and is suitable for practical implementation in real-world scenarios.

- The proposed scheme has been found to be robust against noisy measurements.

- During the incorporation of perturbation techniques (i.e., noise and masking) in the training process, which are utilised to improve the generalisation capability of AI models, no notable improvement has been reported regarding the fault location estimation accuracy. Therefore, the generalisation capability of the developed scheme is increased.

- The comparative analysis with another data-driven scheme (i.e., LSTM-based scheme) validated the suitability of the proposed method to provide precise fault location on AC SCs. Specifically, the developed CNN-based scheme and the LSTM-based scheme resulted in mean fault location estimation errors equal to 0.73% and 1.1%, respectively, during the evaluation of the same fault scenarios.

Chapter 6 presented a centralised protection scheme (at substation level) for multi-terminal HVDC systems with DC SCs, which addresses the need for discriminative, fast, and sensitive protection solutions to ensure secure and reliable operation of HVDC grids with DC SCs. The chapter started by highlighting the limitations of existing protection schemes for DC SCs in HVDC systems by conducting a comprehensive

literature review and presenting a qualification assessment of widely used protection schemes in HVDC systems. The key obervations and the obtained results revealed that existing protection schemes present limitation with respect to protection sensitivity, stability and discrimination capability.

Given the limitations of existing protection schemes, the chapter presented a novel data-driven protection scheme that exploits the strong learning capabilities of the XGBoost algorithm. This scheme comprises fault detection and classification elements which are tested and validated based on offline simulations and real-time studies. The evaluation studies led to the following key observations:

- The developed scheme adopts the centralised protection philosophy, providing a holistic protection solution and eliminating the need for communication among substations. Furthermore, it has demonstrated increased sensitivity and discrimination capability to detect and classify correctly all the faults occurring to all the elements connected to HVDC substation (i.e., buses, SCs, and conventional feeders).

- The proposed scheme has been found to exhibit a high degree of stability and selectivity during external faults occurring beyond the protection zone. In practical deployment, this suggests that the number of nuisance tripping events and system downtime can potentially be minimised.

- The results of the real-time SIL testing showed a high speed of operation which is in compliance with the HVDC protection requirements (i.e., $2 - 5\ ms$), validating the feasibility of the developed scheme for real-time protection applications. Specifically, the resulting operation time is within the time range of 0.0803 ms to 1.2341 ms, providing an average time of 0.2571 ms.

- The proposed scheme has presented immunity to noisy measurements and increased generalisation capability against modifications in the network topology.

7.2 Future Work

This section discusses further research steps which can follow the successful development and validation of the presented fault detection, classification and location schemes.

7.2.1 Investigation of different control strategies and penetration levels of ICGs connected to the AC transmission network

The fault current characterisation of the AC SC presented in Chapter 3 and the development of the protection and location schemes analysed in Chapter 4 and Chapter 5, respectively, considered the integration of AC SCs in power grids incorporating ICGs which operate in DQCI control mode. However, the fault current contribution of ICGs is determined by their control strategy, and the system fault levels depend on the penetration level of ICGs, which may affect the quenching of SCs. Therefore, further investigation is required to explore the quenching of SCs considering different control strategies and penetration levels of ICGs in power systems incorporating SCs. Additionally, the efficacy of the developed schemes can be further validated against different ICG control designs in inverter-dominated networks.

7.2.2 Further investigation of AI algorithms

The protection and fault location schemes developed in this study were designed by incorporating robust AI algorithms that possess strong learning capabilities, such as the ANN and SVM models, which are among the most frequently proposed pattern recognition algorithms. The schemes also account for CNN models and the latest improvements in AI classifiers, such as the XGBoost algorithm. Additionally, the developed schemes were compared with other commonly used AI models, including LSTM models, for the fault location application. These algorithms were selected based on their unique advantages for similar power systems protection and fault location problems reported in technical literature, and were further validated, demonstrating successful outcomes. However, it is recommended that additional AI algorithms be evaluated for fault management in SCs, including upcoming trends in AI applications.

7.2.3 Development of back-up protection schemes

The proposed protection schemes, presented in Chapter 4 and Chapter 6 for AC and HVDC systems, respectively, have been developed as primary protection solutions. Based on the literature review, there is a lack of reliable solutions for the primary protection of AC and DC SCs. However, a next research step should be the development of adequate back-up protection schemes for AC and HVDC grids incorporating SCs.

7.2.4 Experimental validation

In the presented work, the development of SCs has been conducted in Matlab/Simulink providing accurate representation of their transient performance and the quenching phenomenon. Furthermore, the practical feasibility of the developed schemes has been validated using real-time SIL testing. The next step of this research should be the experimental validation of the developed SCs and the testing of the proposed schemes based on a scaled-down laboratory prototype.

7.2.5 Protection coordination of the three XGBoost-based protection schemes installed at HVDC substations

Following the successful development and evaluation of the proposed centralised XGBoost-based scheme for multi-terminal HVDC systems, more research shall be steered towards the simultaneous assessment of the three centralised XGBoost-based schemes installed at the three substations, along with the investigation of back-up protection schemes.

7.2.6 Re-evaluating protection and fault location schemes for next generation SCs

As future work, it is recommended to extend the assessment of the developed protection and fault location schemes and revisit the fault characterisation for the upcoming generation of SCs. These can include SCs fabricated using different superconducting materials (i.e., Bi-based oxide wires, MgB_2 wires), characterised by different specifications (i.e., increased critical boundaries, different layers of HTS tapes and modified configurations). Additionally, different cooling systems may be employed. On that front, a comprehensive evaluation of the proposed schemes, taking into account these diverse factors, will ensure that the protection and fault location schemes remain effective, robust, and adaptable for a broad spectrum of SC technologies. Furthermore, this exploration can potentially uncover new insights to enhance the performance and reliability of the developed schemes, contributing to the continued advancement of SC applications in power systems.

7.2.7 Development of high-fidelity SC models

SCs offer the potential to transform power transmission by significantly increasing energy efficiency and reducing losses. However, accurate modelling of their behavior, especially under transient conditions, remains a challenge. Although current models exist, there is a

need to develop high-fidelity models that can provide a more detailed understanding of the transient response of SCs, unlocking deeper insights. The development of detailed models of SCs can bring numerous benefits beyond unlocking deeper insights into their behavior. These models will also enable investigations into other protection and location schemes, such as those based on the TWs theory. Therefore, the development of high-fidelity models will aim to unlock the full potential of SCs in power systems and accelerate the realisation of a sustainable energy future.

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