University of Strathclyde
Department of Electronics and Electrical Engineering

Design of Module Level Converters in Photovoltaic Power Systems

Yachao Wang

A thesis presented in fulfilment of the requirements for the Degree of Doctor of Philosophy

January 2021

Dedicated to my family

This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

Signed: **Yachao Wang**

Date: 10/1/2021

Acknowledgement

I want to express my sincere gratitude to my supervisors Prof. Barry Williams and Dr. Derrick Holliday for their constructive supervision and continuous support. Special thanks to Dr. Ahmed Darwish for his invaluable suggestions based on his profound knowledge.

Thanks to every PEDEC members for all the fruitful academic discussions and team building activities.

Deepest love goes to my family for their unconditional support; and I want to extend the best wishes for their health and happiness.

Abstract

The application of distributed maximum power point tracking (DMPPT) technology in solar photovoltaic (PV) systems is a hot topic in industry and academia. In the PV industry, grid integrated power systems are mainstream. The main objective for PV system design is to increase energy conversion efficiency and decrease the levelized cost of electricity of PV generators.

This thesis firstly presents an extensive review of state-of-the-art PV technologies. With focus on grid integrated PV systems research, various aspects covered include PV materials, conventional full power processing DMPPT architectures, main MPPT techniques, and traditional partial power processing DMPPT architectures.

The main restrictions to applying traditional DMPPT architectures in large power systems are discussed. A parallel connected partial power processing DMPPT architecture is proposed aiming to overcome existing restrictions. With flexible 'plug-and-play' functionality, the proposed architecture can be readily expanded to supply a downstream inverter stage or dc network. By adopting smaller module integrated converters, the proposed approach provides a possible efficiency improvement and cost reduction. The requirements for possible converter candidates and control strategies are analysed. One representative circuit scheme is presented as an example to verify the feasibility of the design. An electromagnetic transient model is built for different power scale PV systems to verify the DMPPT feasibility of the evaluated architecture in a large-scale PV power system.

Voltage boosting ability is widely needed for converters in DMPPT applications. Impedance source converters (ISCs) are the main converter types with step-up ability. However, these converters have a general problem of low order distortion when applied in dc-ac applications. To solve this problem, a generic plug-in repetitive control strategy for a four-switch three-phase ISC type inverter configuration is developed. Simulation and experimental results confirm that this control strategy is suitable for many ISC converters.

Table of Contents

CHAPTER 1 Introduction

With increasing concerns for energy security and environmental issues, the development of renewable energy has significantly grown all over the world to reduce the usage of fossil fuel energy. Solar photovoltaic energy is a promising renewable resource of near infinite reserve.

At present, grid integrated photovoltaic power systems are mainstream in the PV industry. Relatively high levelized electricity cost and low energy conversion efficiency are the main barriers for solar power to compete with traditional generation types in the wholesale electricity market. The intrinsic variable nature of PV technology needs a maximum power point tracking (MPPT) function to be included in PV systems which also increases the difficulty for PV systems to be widespread installed. To increase competitiveness, large power scale PV systems with distributed MPPT modules have always been a hot topic and much has been done to optimise this type of systems. Novel topologies and system architecture with advanced control methodologies are demanded to maintain a balance between cost and efficiency. Studies in these aspects have attracted much attention in academia and industry.

1.1 Background and Motivation

The dominant driving force of modern industrialization is based on the combustion of exhaustible fossil fuels which has caused serious global problems such as environmental pollution, greenhouse gas emissions, global warming, and so on. According to the 2019 Edition of the global energy trends published by Enerdata, driven by steady economic growth, a historically high energy consumption 11.2 Gt and CO_2 emissions 27 Gt have been recorded in 2018 for G20 countries. However, fossil fuels still represent 80% of primary energy mix. Demand for electricity has been seen an increase of 3.7% and accounts for 20% in final energy consumption. There is strong growth in the renewable energy (solar and wind power production) sector and greater potential is expected [1].

The 2020 energy market has been greatly impacted by the covid19 pandemic according to newly released data, September 2020. The world economy is experiencing a bigger crisis than 2008-2009. With focused analysis in G20s, the final energy consumption has been seen a decrease by around 5%, while electricity demand has only dropped by 1.5% [2].

Although influenced by the pandemic in the short term, global energy consumption will still grow in the future and this growth trend will exert more pressure to combat global warming and meet the Paris Agreement's objectives [3].

Different types of renewables have been widely installed as promising solutions to tackle the global energy crisis. As the second largest deployed renewable technology in the world, the global PV market is continuously increasing at a high growth rate in terms of cumulative global installed capacity. At the end of 2019, global PV installations reached 623.2 GW [4].

Grid integration of PV systems represent the future advancement direction, driven by lower system costs. Grid connected PV systems account for approximately 99% of the PV market. Off-grid PV systems are not comparable and are mainly deployed in developing countries and remote areas [5].

Grid-connected centralized PV generators have dominated the global market since 2013, mainly promoted by the rapid development of utility-scale PV systems [6]. In recent years, the deployment of rooftop PV systems has reduced during this trend.

Compared with grid connected distributed PV generators, cheaper capital investment, faster plants construction and quicker use of PV electricity, are the main drivers for centralized PV generators to be built.

Generally, centralized PV generators are restricted by lower solar energy capture ability as central MPPTs are the main choice for this type of systems [7]. While distributed PV generators can implement distributed MPPT at the PV string or panel level to increase solar energy extraction efficiency. Distributed MPPT technologies usually come with higher initial equipment deployment cost [8]. Much research has been undertaken to deal with the issues of the higher levelized cost of distributed PV systems and the lower energy extraction efficiency of centralized PV systems [8][9][10]. With a growing penetration level of PV technologies in electricity networks, a bright future for the development of the PV industry is anticipated.

1.2 Photovoltaic Technologies

For photovoltaic (PV) electricity generation, the elementary mechanism is the photovoltaic effect, which is the process that converts electromagnetic radiation (sun light) directly into dc electricity. The basic photovoltaic producing device is the photovoltaic cell, also called a solar cell, which features a p-n junction fabricated from a semiconductor material [11].

Generally, the materials of PV cells can be divided into crystalline, thin-film and organic types. Crystalline silicon (single crystal and multi-crystalline silicon) makes up more than 90% of the world's cell production with commercial efficiencies from 16% to 25% [6]. The relatively low conversion efficiency of present PV materials is a barrier to PV industry growth. Research and progress into high efficiency materials and low cost production processes has been continuous since the first silicon PV cell was discovered in 1954 [12].

Table 1-1 gives a basic comparison of the primary commercial materials on the PV market. Although some advancements have been made experimentally, the PV market is still waiting for stable and commercial products with lower cost and higher efficiency [13].

Table 1-1 Comparison of dominating materials of commercial Photovoltaic cells

Materials		Efficiency	Features
Crystalline Silicon	Single Silicon (sc-Si)	16%-25%	Main commercial material with less expensive produce cost
	Multi-crystalline Silicon (mc-Si)	14%-18%	
III-V Compound GaAs-Ge		Over 40%	High cost and typically used for space applications
Thin Film Cells	Cadmium Telluride (CdTe)	22% in the lab	Less expensive to manufacture than crystalline cells potentially
	Organic Thin-film	22% in the lab	

There are several ways to model the PV cell electricity characteristic. A simple equivalent electrical model of one single PV cell is shown in Fig. 1-1, comprising a parallel connected current source and diode [14]. The output of the ideal photocurrent I_{ph} is proportional to the sun irradiance (solar energy) that hits the surface of the solar cell. The ideal current source and the reversed saturation current of the diode are both influenced by the ambient temperature. The series resistance R_s and shunt resistance R_{sh} are parasitic parameters whose magnitudes and impact are dependent on the geometry of the PV cell. Ideally, it can be assumed that R_s is zero and R_{sh} is infinite to simplify the model.

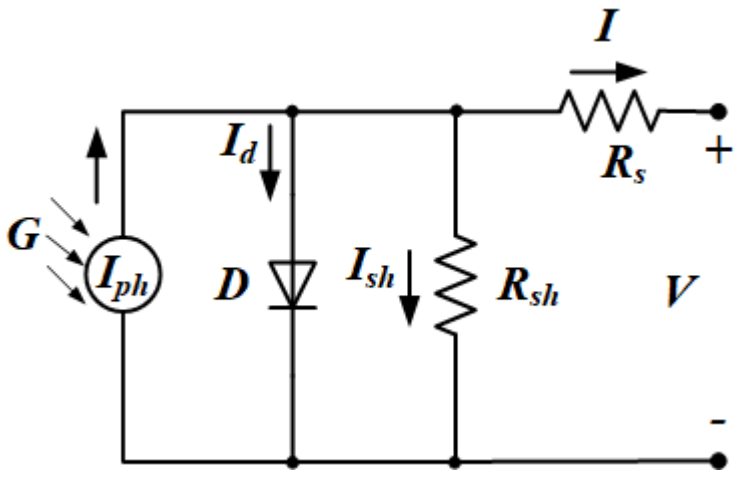


Fig. 1-1. Equivalent Circuit diagram of a basic PV cell

The electrical characteristic of the output current *I* and output voltage *V* is illustrated by the *I-V* curve in Fig. 1-2. The non-linear relationship between *I* and *V* is influenced by environmental parameters, such as ambient temperature and sun irradiance.

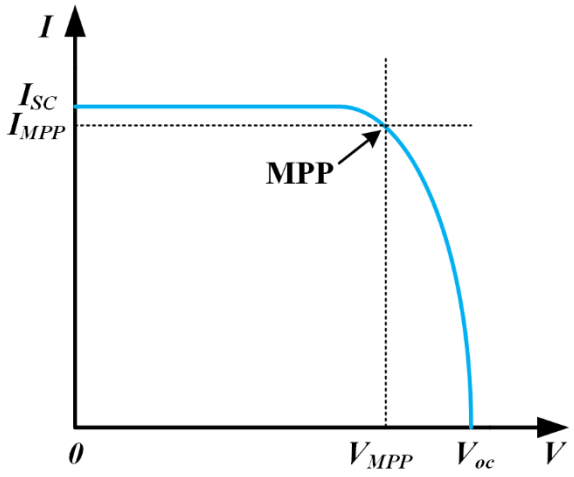


Fig. 1-2. Characteristic of *I-V* curve for a PV cell

The non-linear relationship between PV output current and voltage, necessitate techniques to achieve maximum energy output in practice. A maximum power point tracking (MPPT) algorithm is usually implemented in PV systems to deal with the non-linear feature of the PV material. MPPT can guarantee that the maximum power output can be extracted when environmental parameters vary [7]. Different MPPT techniques have been developed to improve the energy capture efficiency for different PV applications, and these will be reviewed in subsequent chapters.

The voltage magnitude of one single PV cell is low (usually less than 1 V) for most PV materials. Hence, the PV module, also called PV panel, is produced as the commercial elementary component for end users, which generally comprises multiple PV cells serially and parallel interconnected together to increase the output voltage and current level. Available commercial PV modules have different specifications considering different cost and demands of clients. The modules usually include 48, 54, 60, or 72 cells in industry. As mentioned, the present photovoltaic (PV) technologies in the market are mostly either monocrystalline or polycrystalline silicon modules. The open circuit voltages of such silicon modules range from 18 V to 26 V for a module of 36 cells or from 38 V to 46 V for one consisting of 72 cells [15].

To further boost the voltage level, the PV string is introduced with several PV modules connected in series. As with commercial PV modules, PV strings also have different specifications in commercial use.

For large scale PV systems, several PV strings are connected in parallel to form a PV array to cumulate a higher power level. There are also other terms to describe different types of PV generators, such as submodule and subarray. The design objective of a PV array is to increase the output voltage level by connecting PV modules in series and increase output current level by connecting PV strings in parallel. Usually, PV strings can be applied in a string level decentralized PV inverter system and PV arrays are used for a centralized PV inverter system. The detailed classification of different grid integrated PV systems is given in the following section.

1.3 Classification of Grid Connected PV Systems

Conceptually, a photovoltaic system is comprised of large number of PV modules connected to a utility grid (grid-connected system) or a series of loads (off-grid system). Compared with fast-evolved grid integrated PV systems, the share of off-grid PV installations is small. Off-grid systems can provide electricity for areas without a utility electricity network and storage batteries are usually demanded for off-grid applications.

Grid-connected PV systems represent approximately 99% of the global PV market. According to the IEA-PVPA 2020 report, the cumulative installed nominal PV power worldwide was more than 632 GW by the end of 2019, and most of the power is from grid-connected systems [5].

Grid-integrated PV systems can generally be classified into different types by power level. There are small PV systems (less than 50 kW), intermediate systems (between 50 kW and 1 MW), and large-scale systems (over than 1 MW). However, system boundaries with different power levels are not explicit due to the modularity nature and separated installation of PV systems [16].

In terms of MPPT implementation, grid-connected PV systems can also be classified into two main groups: centralized MPPT (CMPPT) and distributed MPPT (DMPPT) [11][8][17]. As shown in Fig. 1-3, the DMPPT category is defined based on the level at which MPPT is implemented: string, module, submodule and even cell

level where the MPPT function is applied. The future trends for MPPT implementation are dictated as the arrow direction towards finer granularity.

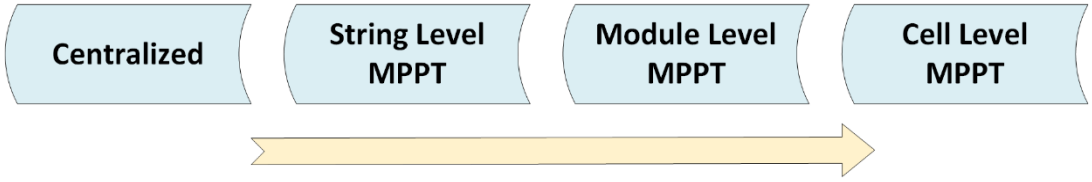


Fig. 1-3 Trends towards finer DMPPT

Inverters are needed to convert electricity from direct current (dc) power generated by PV modules to alternating current (ac) power supplied to the utility grid. Inverter based power configuration types fit into three broad categories: centralized inverter for the whole PV array, string inverter used for each string of modules, and distributed module integrated converters [18]–[21]. The centralized inverter is illustrated in Fig. 1-4 (a) with blocking diodes, often referred to as string diodes, connected in series with each string to prevent possible reversed current flow. As seen in Fig. 1-4 (b), the single-string and multi-string structures can be regarded as reduced versions of a centralized inverter. However, the MPPT function can be applied at the string level to increase operational efficiency. For larger utility-scale PV systems, 3-phase centralized inverters which have a typical power rating from 2 to 5 MW are the common choice. Installation of string inverter based configurations have grown rapidly, especially in the Asia-Pacific region [6].

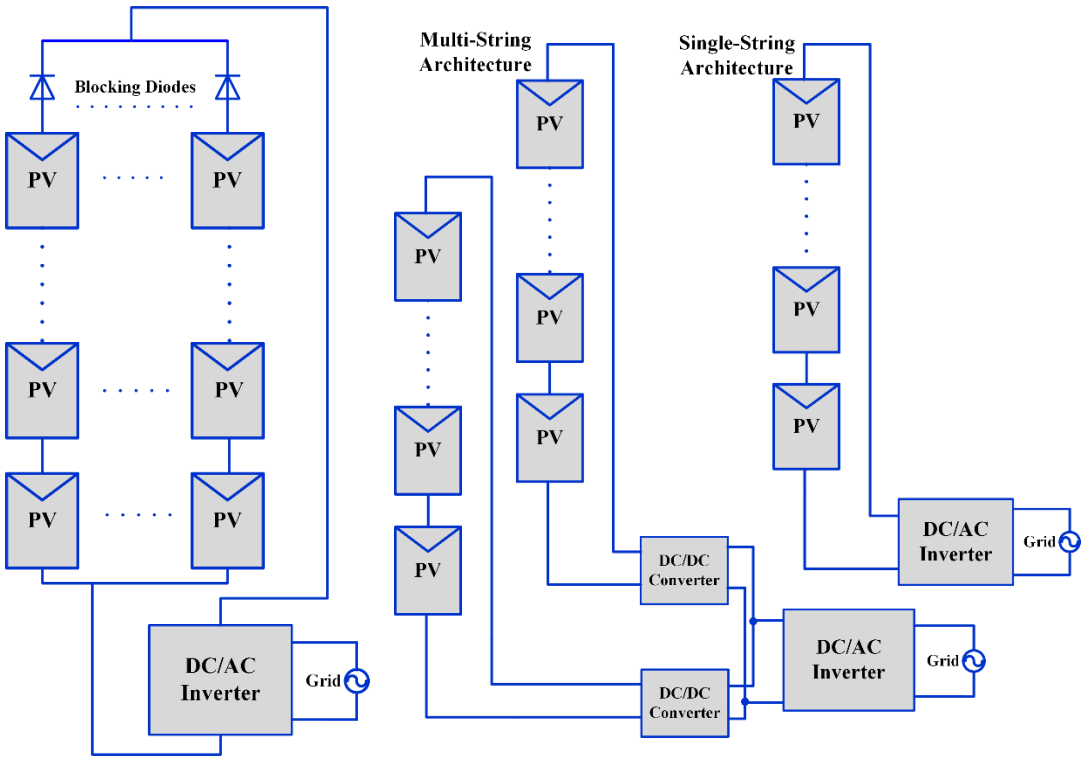


Fig. 1-4. Inverter configurations. (a) Centralized inverter, (b) Single-string and Multi-string inverter.

A centralized inverter is sourced by a PV array while a string inverter is supplied by a PV string, which means MPPT cannot be applied at the module level for both configurations [22]. Partial shading and PV module mismatching can have a disproportionate impact on system performance, since the least efficient PV modules (shaded or defective) will decide the whole system energy capture efficiency. In a centralized inverter system, several PV strings are parallel connected by string diodes to avoid reversed power flow, which causes losses in the diodes.

Module level distributed MPPT systems attempt to solve the mentioned problems in centralized and string level inverter systems. The module integrated converter (MIC) based DMPPT configuration is commercially available at present. There are different types of MIC DMPPT system architectures. They mainly consist of AC modules (microinverters) and dc optimizers, which are increasingly expanding, especially in the USA. The AC module, namely microinverter, directly converts the low PV module voltage, typically 22-45V, to the single phase AC grid level (100 to 240 V AC usually) [19][23][24]. The dc optimizer is a voltage boosting dc/dc

converter connected to the PV module [25][8]. These commercial MIC configuration types are illustrated in Fig. 1-5. The per module per converter structure removes the mismatch losses between PV modules and enables the ‘plug and play’ feature which makes it easier to enlarge the system. Although facilitating a significant boost of captured photovoltaic power, the AC module and DC optimizer based DMPPT architectures have limitations in terms of high initial equipment cost, high voltage conversion ratios and relatively low conversion efficiencies.

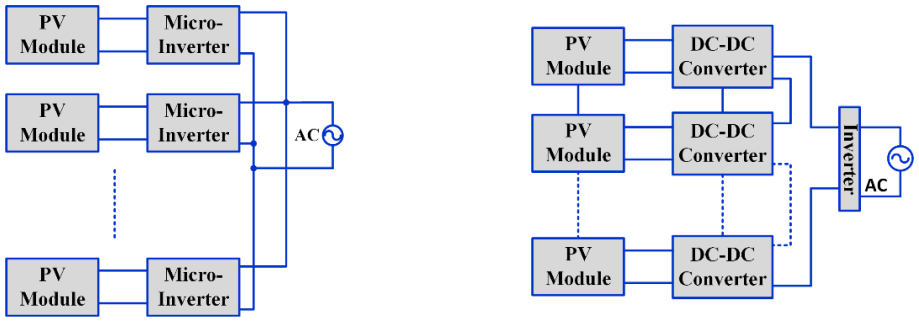


Fig. 1-5. Commercial Module Integrated Converter Configurations. (a) Parallel connected Micro-inverter and (b) series connected DC optimizer.

To retain the benefits of the MIC architecture and minimize potential cost and efficiency penalties induced by auxiliary converters, another module level DMPPT architecture, classified as partial or differential power processing PV systems, has been proposed. There are different connection types for partial power processing DMPPT system. The representative architecture is shown in Fig. 1-6. The auxiliary dc-dc converters are parallel interconnected within the PV string to balance unequal module operation points. Different from AC modules and DC optimizers, these auxiliary dc-dc converters do not process the full power generated by the PV module. They only process the mismatched power between two adjacent PV modules. The connection completeness of the associated PV string will not be broken by the shuffling converters which provides benefits related to grounding issues and system expansion. Under the ‘no mismatch, no processing’ principle, the required power rating, size and manufacturing cost for the auxiliary converters can be significantly reduced [8], [26]–[28]. Thus, the overall energy conversion efficiency can be increased.

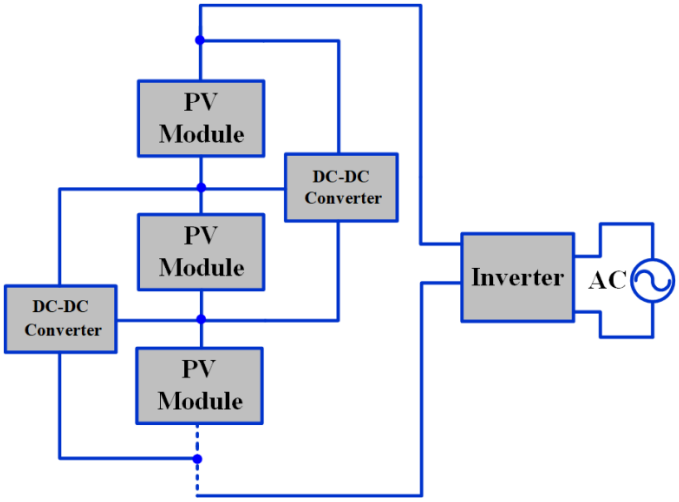


Fig. 1-6. A Representative diagram of the partial power processing configuration.

Despite the evident merits of partial power processing architectures, there are still limitations especially when implemented in utility scale PV systems. The typical architecture shown in Fig. 1-6 with mismatching current balancing ability can only be installed with a single-string inverter to ensure the possible maximum power output for every PV string, while multi-string inverter configurations are more desirable for large-scale power systems.

Centralized or multi-string inverters benefit from higher converter conversion efficiency, higher power density, and lower cost. Accordingly, for large-scale PV grid integration systems, it is a better strategy to integrate the partial power processing with centralized or multi-string inverters architectures. This concept presents emerging challenges for future PV system design, taken into consideration the appropriate converter topologies, novel system architecture, modelling and control.

1.4 Main Barriers and Research Objectives

To compete with traditional grid integrated electricity generators, photovoltaic powered generators present two main barriers: 1) lower energy conversion efficiency and 2) higher deployment cost. To achieve a higher penetration level for grid integrated PV systems, the following major obstacles should be addressed.

- High cost – The target of PV grid parity is to lower the levelized electricity cost of PV power at a price equal to or even below the cost of the on-grid price of conventional electricity generators [22][29]. If achieving this goal, large utility-scale PV systems have a bright future [30]. With the downward

tendency of the price per watt of a crystalline PV module, the price of PV inverters is more visible.

- Output power fluctuation – The intermittent nature of PV power may cause reliability and power quality issues for the electricity network. Therefore, investigation and analysis of different operation modes must be made for PV systems to comply with international grid connection codes and standards. In some cases, electricity storage equipment with a relatively short lifespan is needed which may increase the overall system cost.
- Low dc voltage –The distribution voltage level of ac grids in most countries is around 100 V to 240 V, while the transmission voltage level is usually over several kilo-volts. These are way higher than the voltage level of a typical PV module. Consequently, the primary drive for system design and optimization is to seek appropriate solutions to effectively and efficiently convert the low dc voltage power to a high ac voltage power [17].
- Low energy conversion efficiency of PV modules and short lifetime of PV inverters. Although some new PV materials have reported with over 44% energy efficiency in lab experiments, the energy conversion efficiencies for commercially available PV materials are only 16% to 25%. This is the most important reason for the low utilization factor of PV systems and can only be solved by advancement of PV materials and manufacturing industries. Modern PV modules usually have more than 25 years guaranteed operation time. While PV inverters lifespan vary from 10-15 years for sting level inverters to 20-25 years for DC optimizers. Some off-grid inverters have lower life-times, 2-10 years [31][32]. This contradiction of lifespan between PV modules and PV inverter is adverse for the balance of PV systems. It is necessary to prolong the lifetime of PV inverters to get a better system balance.

It can be concluded that, except for the low efficiency of the PV materials, the most important factors which hinder the development of the PV industry are the low dc voltage of a single PV cell and the intermittent nature of PV electricity.

Actually, these two factors interact. To increase the power level of PV systems, modules need to be connected in series and parallel forms to generate a PV string or PV array. In PV string or PV array based solar systems, string level or array level

MPPT is usually implemented. However, the intermittent nature of solar electricity needs module level or even cell level MPPT to increase the energy capture capability. These two requirements are difficult to realize in a commercially fabricated PV string or PV array, at present. The aim is to find a good solution to deal with this contradiction.

On the other hand, if central MPPT is used at the string level, the mismatch of PV modules will deteriorate MPPT performance and lower system efficiency. The low efficiency issue of PV systems will eventually increase PV electricity cost. A hopeful option is to implement module level DMPPT in large scale grid integrated PV systems. However, most of the present DMPPT schemes have higher initial equipment installation cost which may adversely increase PV electricity price.

To lower PV electricity cost and improve the system efficiency, one prospect of future PV technologies is to investigate a cost-effective method to implement module level DMPPT in larger-scale grid integrated PV systems. The multi-string or central inverter is widely used in the PV industry for higher conversion efficiency and lower system cost. It is the future trend to add modular features in centralized or multi-string inverter dominated PV systems to accomplish this objective. Several aspects aiming to realize this goal have been researched and more detailed reviews will be given in the following chapters. The main objective in this thesis is to find a good solution based on this promising prospect, as discussed in the following points:

- Converters with voltage boosting abilities are required to act as module integrated converters for DMPPT functions. Various step-up converter topologies are assessed focusing on their potential to be used in distributive utility scale PV systems. The dc-dc module integrated converters which can be integrated with centralized or multi-string inverters will be particularly reviewed and designed for a novel PV system architecture. The traditional large power centralized and string level inverter topologies have been widely analyzed and obtained some common agreement, so they will not be discussed in detail in this thesis.
- With increased dc link voltage utilization, impedance source converters have been widely studied and applied within PV systems. The general characters are examined considering passive impedance networks. Traditional control methods are compared and an advanced repetitive control strategy is imposed

for enhanced harmonic emission capability. Quantified analysis is performed with detailed modelling, circuit specification, and experimental realization.

- To combine the dc-dc MIC with centralized and string inverters efficiently, the partial power processing DMPPT architecture is a suitable choice. A variety of converter candidates for partial power processing systems are analyzed and compared. A novel partial power processing architecture is proposed to give a convenient connecting method with large scale centralized PV inverters. With reduced power ratings auxiliary converters, the system cost can be decreased and module level MPPT is achieved.
- A large-scale grid integration of PV system utilizing the proposed architecture is analysed in simulation to gain system performance evaluation. A simulation model is established to investigate the impact and potential problems for the utility grid that may arise due to the installation power capacity of the PV systems. At different operation modes, distributive control methods and an EMTP model are implemented with fault ride through ability.

1.5 Thesis Outline

This thesis is comprised of six chapters. Each chapter can be briefly described as follows:

Chapter 1 gives an overview of the state-of-the-art for photovoltaic power systems. To combat global energy problems, it is needed to develop new PV technologies to achieve a grid parity goal for PV electricity generators in global energy. The main barriers and present PV technologies are discussed to give a picture of the PV industry. It is found that large-scale grid integrated PV systems are the future trend. The main problem of a centralized-inverter-based PV system is low energy conversion efficiency. Various present solutions for this problem are reviewed and a promising prospect has been provided to give guidelines for further research in this thesis.

Chapter 2 reviews module integrated converter topologies and PV system configurations based on the module integrated converter (MIC). Standards and requirements are discussed regarding the possible influences of connecting PV generators to the utility grid. PV system connection types and MIC topologies are compared in three categories to give a clearer view of the application background and

restrictions. The main drive for innovative topologies and system configurations is to improve solar energy efficiency (independent on the PV cell technology) by using cost effective solutions. Another important factor is to match PV inverter lifetime with that of PV modules. Impedance source converters are also reviewed in this chapter to emphasise the control challenge for this type of converter. The proposed solution is given in Chapter 5 with detailed analysis of this general problem. This chapter provides background information and direction for the following research to combine MICs with centralized inverters for better PV system performance.

Chapter 3 gives a literature review and comprehensive analysis of the mismatch mechanism in PV systems. The composition feature of the fundamental building block in a PV system is illustrated to clarify the base reason for mismatched losses. The hot spot phenomenon caused by non-identical PV cells is analysed and conventional detection and protective methods are discussed. Two compensation solutions based on module integrated converters are reviewed respectively for series and parallel connected PV modules. The advantages and challenging aspects are concluded to give insight for future research.

In Chapter 4, a new partial power processing distributed MPPT architecture is proposed where the per PV string per central converter configuration is avoided. All the associated converters can be configured as partial power processors with reduced power rating. This architecture is convenient for parallel connection of PV strings to achieve increased power output. This novel architecture can combine the MIC with centralized PV inverters and then can be used in large-scale PV grid integrated power systems. Distributed control, improved reliability and smart grid functionality assistance can be realized. Modelling, control and performance evaluation are given and this system configuration is verified experimentally.

Chapter 5 investigates the control challenges for a set of high-order wide-output (HOWO) impedance source converters (ISCs) with comparison of different control strategies. Different impedance source converters with voltage boosting ability are applied in PV applications. The intrinsic passive impedance network provides lower order distortion of the ac output power which results in controller design difficulty. Generic digital repetitive control is used to solve the prominent second harmonic

problems of ISCs. Simulation and experimental validation are performed on a topology based on the semi-quasi Z source converter.

Chapter 6 presents the conclusion and future research plan. The authors contributions are highlighted. The restrictions for PV technologies and possible solutions are summarised. A promising prospect is expected for the future PV electricity market.

1.6 References

[1] "2019 Energy Trends Edition | 2019 Energy World | Enerdata." [Online]. Available: https://www.enerdata.net/publications/reports-presentations/2019-energy-trends.html. [Accessed: 04-Apr-2021].

[2] "Global Energy Trends 2020 - Update | Enerdata." [Online]. Available: https://www.enerdata.net/publications/reports-presentations/world-energy-trends.html. [Accessed: 05-Apr-2021].

[3] "The Paris Agreement | UNFCCC." [Online]. Available: https://unfccc.int/process-and-meetings/the-paris-agreement/the-paris-agreement. [Accessed: 31-Mar-2021].

[4] IEA-Pvp, "Snapshot of Global PV Markets 2020," *Www.Iea-Pvps.Org*, pp. 1–16, 2020.

[5] I. PVPS Task, *IEA PVPS report - Trends in Photovoltaic Applications 2020*. .

[6] IEA-PV, "TRENDS 2017 IN PHOTOVOLTAIC APPLICATIONS," 2017.

[7] M. A. G. de Brito, L. Galotto, L. P. Sampaio, G. d. A. e Melo, and C. A. Canesin, "Evaluation of the Main MPPT Techniques for Photovoltaic Applications," *IEEE Trans. Ind. Electron.*, vol. 60, no. 3, pp. 1156–1167, 2013.

[8] D. Shmilovitz and Y. Levron, "Distributed Maximum Power Point Tracking in Photovoltaic Systems - Emerging Architectures and Control Methods," *Autom. – J. Control. Meas. Electron. Comput. Commun.*, vol. 53, no. 2, 2012.

[9] E. Roman, R. Alonso, P. Ibanez, S. Elorduizapatarietxe, and D. Goitia, "Intelligent PV Module for Grid-Connected PV Systems," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1066–1073, 2006.

[10] S. Saha and V. P. Sundarsingh, “Novel grid-connected photovoltaic inverter,” *IEE Proc. - Gener. Transm. Distrib.*, vol. 143, no. 2, pp. 219–224, 1996.

[11] W. Xiao, *Photovoltaic Power System*. Hoboken, NJ, USA: John Wiley & Sons, Inc., 2017.

[12] S. Almosni *et al.*, “Material challenges for solar cells in the twenty-first century: directions in emerging technologies,” *Sci. Technol. Adv. Mater.*, vol. 19, no. 1, pp. 336–369, 2018.

[13] V. Benda, “Photovoltaics towards terawatts -2013; progress in photovoltaic cells and modules,” *IET Power Electron.*, vol. 8, no. 12, pp. 2343–2351, 2015.

[14] S. B. Kjær, “Design and Control of an Inverter for Photovoltaic Applications,” 2005.

[15] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, “Power inverter topologies for photovoltaic modules-a review,” in *Conference Record of the 2002 IEEE Industry Applications Conference. 37th IAS Annual Meeting (Cat. No.02CH37344)*, vol. 2, pp. 782–788 vol.2.

[16] W. Xiao, *Photovoltaic Power System Modelling, Design, and Control，Chapter 1*. Australia: JohnWiley & Sons Ltd, 2017.

[17] J. M. Carrasco *et al.*, “Power-Electronic Systems for the Grid Integration of Renewable Energy Sources: A Survey,” *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1002–1016, 2006.

[18] L. Bangyin, D. Shanxu, and C. Tao, “Photovoltaic DC-Building-Module-Based BIPV System-Concept and Design Considerations,” *Power Electron. IEEE Trans.*, vol. 26, no. 5, pp. 1418–1429, 2011.

[19] F. B. Soeren Baekhoej Kjaer John K. Pedersen, “A Review of Single-Phase Grid-Connected Inverters for Photovoltaic Modules,” 2005.

[20] T. Remus, L. Marco, and R. guez Pedro, “Photovoltaic Inverter Structures,” in *Grid Converters for Photovoltaic and Wind Power Systems*, Wiley-IEEE Press, 2011, p. 416.

[21] J. M. A. Myrzik and M. Calais, “String and module integrated inverters for single-phase grid connected photovoltaic systems - a review,” in *2003 IEEE*

Bologna Power Tech Conference Proceedings, 2003, vol. 2, p. 8 pp. Vol.2.

[22] G. G. M. L. S. S. Yaosuo Xue Kurthakoti C. Divya and M. Manjrekar, "Towards Next Generation PV Inverters," 2011.

[23] H. Hu, S. Harb, N. Kutkut, I. Batarseh, and Z. J. Shen, "A Review of Power Decoupling Techniques for Microinverters With Three Different Decoupling Capacitor Locations in PV Systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2711–2726, 2013.

[24] Q. Li and P. Wolfs, "A Review of the Single Phase Photovoltaic Module Integrated Converter Topologies With Three Different DC Link Configurations," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1320–1333, 2008.

[25] G. R. Walker and P. C. Sernia, "Cascaded DC-DC converter connection of photovoltaic modules," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 1130–1139, 2004.

[26] P. S. Shenoy, K. A. Kim, B. B. Johnson, and P. T. Krein, "Differential Power Processing for Increased Energy Production and Reliability of Photovoltaic Systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2968–2979, 2013.

[27] H. Zhou, J. Zhao, and Y. Han, "PV Balancers: Concept, Architectures, and Realization," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3479–3487, 2015.

[28] C. Olalla, D. Clement, M. Rodriguez, and D. Maksimovic, "Architectures and Control of Submodule Integrated DC-DC Converters for Photovoltaic Applications," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2980–2997, 2013.

[29] Q. Tu, J. Mo, R. Betz, L. Cui, Y. Fan, and Y. Liu, "Achieving grid parity of solar PV power in China- The role of Tradable Green Certificate," *Energy Policy*, vol. 144, p. 111681, Sep. 2020.

[30] T. Kerekes, E. Koutroulis, D. Séra, R. Teodorescu, and M. Katsanevakis, "An Optimization Method for Designing Large PV Plants," *IEEE J. Photovoltaics*, vol. 3, no. 2, pp. 814–822, 2013.

[31] "How Long Do Solar Inverters Last? (2020 Guide)." [Online]. Available: https://thosesolarguys.com/how-long-do-solar-inverters-last/. [Accessed: 10-

Apr-2021].

[32] A. Sangwongwanich, Y. Yang, D. Sera, and F. Blaabjerg, “Lifetime Evaluation of Grid-Connected PV Inverters Considering Panel Degradation Rates and Installation Sites,” *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1225–1236, 2018.

CHAPTER 2

Review of Module Integrated Converters for Full Power Processing DMPPT Architectures

This chapter reviews PV systems based on module integrated converters. With increasing penetration of grid integrated PV systems, the requirements for PV power regulation are more complex. However, due to the high cost of solar electricity, the main drive for the development of innovative topologies and system architectures is to pursue high energy convention efficiency. Module level distributed MPPT is widely applied, trying to deliver maximum PV generated power to ac grid.

Another important factor is to improve PV inverter lifetime to match the relative long lifetime of PV modules which usually has a guaranteed operation time of better than 20 years. The PV system based on module integrated converters is the future trend for higher efficiency and longer lifetime with anticipated system performance improvements, and can be applied in applications with different power levels.

This chapter discusses the demands and related standards for PV integrated inverters with functions to deal with possible power quality issues, such as anti-islanding, current harmonics and so on. Based on these functionality requirements, a conceptual comparison on basic operation principles of state of the art MIC topologies with emphasis on efficiency and system cost, will be developed.

2.1 Background

A central inverter is the dominant type for medium or large power grid integrated PV systems. Compared with distributed PV architectures, the lower initial installation cost and higher power inverter efficiency have made central inverter based PV architectures the main stream choice in the PV market. The main limitation is its central MPPT performance which can be severely worsened by mismatched PV modules within the PV array.

To overcome this problem, the string level inverter has been introduced to implement string level MPPT. As the basic commercial PV unit in a PV system, the PV module is usually treated as the basic operating cell for system optimization. To assist module level MPPT implementation, numerous dc-dc and dc-ac converters have been applied in different PV system architectures to gain the best solar power usability.

Conventional module level converters have to process all the power generated by the PV module which can make for high equipment costs. The trade-off between energy extraction ability and equipment cost has driven the development of partial power processing module level converters. In this thesis, module level DMPPT converters are analysed separately as full power and partial power processing types.

Compared with conventional full power processing converters, partial power processing converters can reduce equipment cost as well as realizing module level MPPT. However, the system connection is more complex and the control strategy is usually more difficult to implement. The classification of module level DMPPT architectures depends on the power processing types, as shown in Fig. 2-1. In this chapter, the full power processing conversion type will be reviewed, while the partial power processing conversion type will be discussed in Chapter 3.

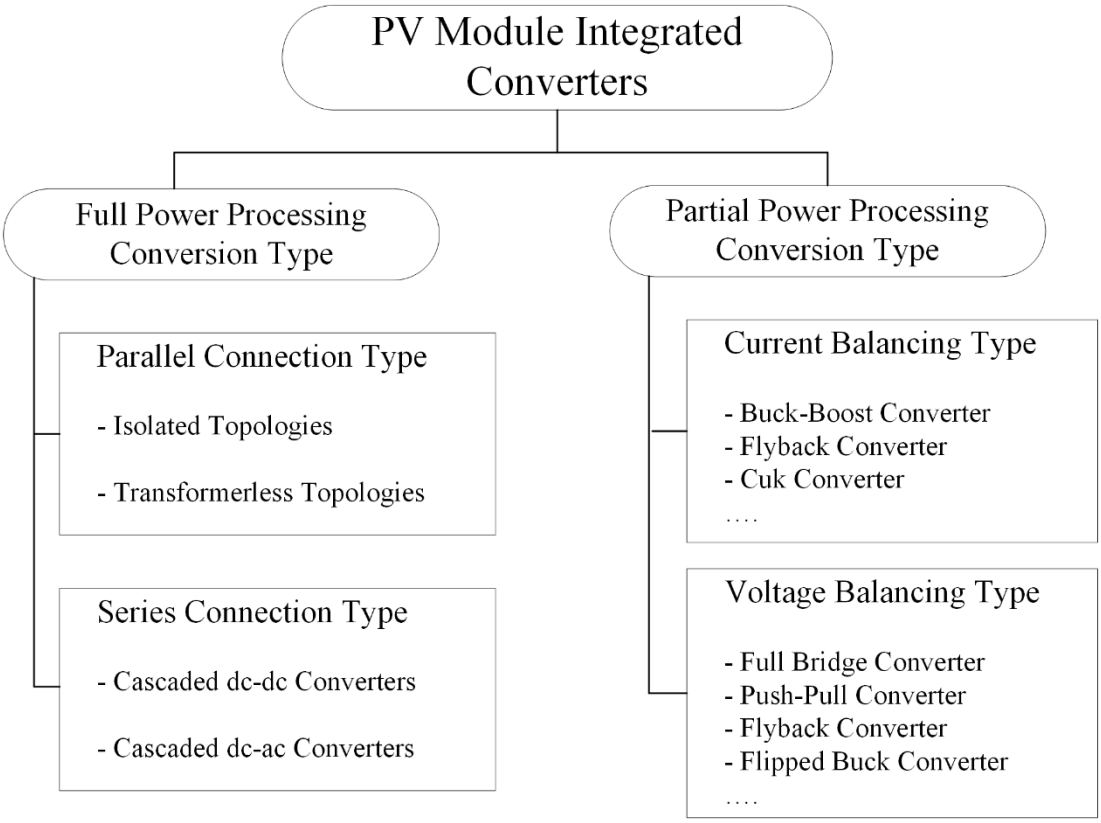


Fig. 2-1 Classification of PV module integrated converters according to power processing type.

Full power processing converters can be grouped into two categories according to the connection types. The converters of the parallel connection type mainly have a module level inverter structure which are also called AC modules or micro inverters. AC module based architectures are mainly used for single-phase low or medium power PV applications. Because of the relatively low dc voltage of a single PV module, high voltage boosting ability is necessary. The voltage boosting function can usually be achieved by isolated transformers or multi-stage transformer-less inverter topologies.

The series connected full power modules can be cascaded dc-dc converters or dc-ac converters. The basic converter cells for this series type are primarily buck, boost and buck-boost converters.

The concept of partial power processing is introduced to ensure module level MPPT can be achieved with a low level equipment cost. By implementing voltage balancing and current balancing ideas, the module level converters do not need to process all the power generated by its associated PV modules. The converters with

lower power ratings only need to operate when mismatch occurs between adjacent PV modules. If the module level converter is intelligent enough to operate only when it is needed, the power rating and size of the module level converters can be significantly decreased. Based on no mismatch, no power processing principle, several new PV architectures have been proposed which are called differential or partial power processing PV systems. The classifications and main converter types are shown in Fig. 2-1 and a detailed review is presented in Chapter 3.

The main standards and requirements for PV system operation will be listed in the next section, to give guidelines for the discussion that follows. Full power processing architectures will be reviewed mainly based on converter characteristics, system requirements and control implementation [1][2]. By reviewing previous research, it can be assessed that there is a possibility to increase energy efficiency by implementing module level MPPT. The main drawback is the increased equipment cost caused by installing many module converters. It is always a task to get a balance when designing such full power processing DMPPT PV systems.

2.2 Standards and requirements for grid-connected PV systems

It is a basic requirement for PV processers to meet the demands defined by the PV modules. For grid connected PV systems, another important requirement is to satisfy the grid connection standards defined by the utility supplier. There are several different standards and guidelines created by different areas and organizations. Their main objective is to guarantee the safety and reliability of the grid supply connected with PV generators. Various protective measures and equipment are stipulated specifically for PV grid integration systems. As an important member of distributed generation (DG) systems, the demands for general DG systems also apply to PV generation [3][4].

In this section, the world acknowledged standards are discussed. These standards cover most aspects of PV grid connecting issues regarding power quality, operation safety, islanding detection, and other considerations. A list of important standards and their publication organization are given, as an overview, in Table 2-1 [3][5].

Table 2-1 Standards List for PV- Grid Integration Systems

IEEE 1547TM-2003 (R2008)	IEEE Standard for interconnecting DRs with electric power systems
IEC 61727-2004	PV systems — characteristics of the utility interface
IEC 61000-3-2:2018	Electromagnetic compatibility (EMC) – Part 3-2: Limits – Limits for harmonic current emissions (equipment input current ≤ 16A per phase)
IEEE 929-2000	Recommended practice for utility interface of PV systems
CSA C22.3 No. 9-08 (R2015) Canada	Interconnection of DRs and electricity supply systems
ENA Engineering Recommendation G83 Issue 2-2012 (EREC G83) UK	Recommendations for the connection of type tested SSEG (up to 16 A per phase) in parallel with LV distribution systems
VDE-AR-N 4105-2011-08 German	Power generation systems connected to the LV distribution network – Technical minimum requirements for the connection to and parallel operation with LV distribution networks
GB/T 19939-2005 China	Technical requirements for grid connection of PV system
KEPCO Technical Guideline Korea	Korea Electric Power Corporation Technical Guideline for integrating DRs with the Grid
JEAC 9701-2012	Grid-interconnection Code

IEEE 1547-2008 with its amendment 2014 is the most widely used standard for integrating distributed resources within 10MVA electrical systems[6]. For low-voltage low-power PV systems below 10kVA, IEC 61727 is generally used to specify the related technical issues [7]. IEC 61000-3-2 regulates the limitations for harmonics injected into the public supply system[8]. IEEE 929 gives guidelines for small PV power systems in terms of many practical aspects such as personnel safety and equipment protection [9]. As well as these international regulations, many countries have created their own standards based on the international code, such as China, the UK, Germany and some other countries [3].

Considering the possible influences of connecting PV generators to the utility grid, the following points are usually covered in the mentioned standards:

1) Voltage regulating and frequency related control;
2) Current harmonics and dc current injection;
3) Islanding detection and operation;
4) Reliability and safety issues;
5) Malfunction of equipment;

6) Protective measures for overcurrent and overvoltage; and

7) Dispatching and planning schemes for PV generated power.

The main constraints for PV connected systems are summarized in Table 2-2 regarding different standards and their associated power ratings.

Table 2-2 A summary of main points in important standards

<table>
<tr><td>Stan No.</td><td colspan="2">IEEE 1547</td><td colspan="2">IEEE 929</td><td colspan="2">IEC 61727</td><td colspan="2">EN61000-3-2</td></tr>
<tr><td>Power Ratings</td><td colspan="2">10 MVA</td><td colspan="2">10 kW</td><td colspan="2">10 kVA</td><td colspan="2">16A@230V</td></tr>
<tr><td rowspan="8">Odd Harmonic</td><td colspan="5" rowspan="2"></td><td>Order (h)</td><td>Limit (A)</td></tr>
<tr><td>3-9</td><td colspan="2"><4.0%</td><td colspan="2"><4.0%</td><td>3</td><td>2.3</td></tr>
<tr><td>11-15</td><td colspan="2"><2.0%</td><td colspan="2"><2.0%</td><td>5</td><td>1.14</td></tr>
<tr><td>17-21</td><td colspan="2"><1.5%</td><td colspan="2"><1.5%</td><td>7</td><td>0.77</td></tr>
<tr><td>23-33</td><td colspan="2"><0.6%</td><td colspan="2"><0.6%</td><td>9</td><td>0.4</td></tr>
<tr><td>>33</td><td colspan="2"><0.3%</td><td colspan="2"></td><td>11</td><td>0.33</td></tr>
<tr><td colspan="5" rowspan="2"></td><td>13</td><td>0.21</td></tr>
<tr><td>(15-39)</td><td>2.25/h</td></tr>
<tr><td rowspan="3">Even Harmonic</td><td>2-8</td><td colspan="2" rowspan="2">Less than 25% of the odd harmonic limits</td><td colspan="2"><1.0%</td><td>2</td><td>1.08</td></tr>
<tr><td>10-32</td><td colspan="2"><0.5%</td><td>4</td><td>0.43</td></tr>
<tr><td colspan="5"></td><td>6</td><td>0.3</td></tr>
<tr><td>THD (%)</td><td colspan="5"><5%</td><td>8-40</td><td>1.84/h</td></tr>
<tr><td>DC Injection</td><td></td><td colspan="2">No more than 0.5% of rated output current</td><td colspan="2">No more than 1% of rated output current</td><td colspan="2"><0.22A</td></tr>
<tr><td rowspan="5">Voltage</td><td>Range (%)</td><td>Trip time</td><td>Range (%)</td><td>Trip time</td><td>Range (%)</td><td>Trip time</td><td colspan="2" rowspan="5">-</td></tr>
<tr><td>V<50</td><td>0.16s</td><td>V<50</td><td>6 cycles</td><td>V<50</td><td>0.1s</td></tr>
<tr><td>50≤V<88</td><td>2s</td><td>50≤V<88</td><td>120 cycles</td><td>50≤V<85</td><td>2s</td></tr>
<tr><td>110≤V<120</td><td>1s</td><td>110≤V<137</td><td>120 cycles</td><td>110≤V<135</td><td>2s</td></tr>
<tr><td>120≤V</td><td>0.16s</td><td>137≤V</td><td>2 cycles</td><td>135≤V</td><td>0.05s</td></tr>
<tr><td rowspan="2">Frequency</td><td>Range (Hz)</td><td>Trip time</td><td>Range (Hz)</td><td>Trip time</td><td>Range (Hz)</td><td>Trip time</td><td colspan="2" rowspan="2">-</td></tr>
<tr><td>59.3<f<60.5</td><td>0.16s</td><td>59.3<f<60.5</td><td>6 cycles</td><td>49<f<51</td><td>0.2s</td></tr>
</table>

Note: THD – Total harmonic distortion

Islanding is the situation in which distributed generators such as PV panels and wind turbines continue to supply power to utility grid when the electricity of the main grid is not present. It is required in most standards for PV systems to detect islanding and stop feeding the main electrical network within 2 seconds. There are usually three types of islanding detection methods, viz., passive, active and hybrid protection. The present active methods mainly include frequency shift, power variation and current injection. The passive protecting methods generally monitor voltages and frequency

changing rate. In many countries, it is required to combine active and passive methods to enhance islanding detection. In addition, a specified holding period after fault clearance is required by the grid-connection code before reclosing the main switch.

With an increasing PV system penetration level, it is important for manufacturers to understand and follow the relevant standards for safety and reliability reasons. These requirements and codes mainly cover three parts: the utility grid, PV modules and the operators or clients. The following sections will analyse how these demands and standards are achieved by existing inverter topologies and system configurations. The main objective is to recognize the most suitable solutions for interfacing PV systems to the grid.

2.3 Parallel connected module integrated inverters

As shown in Fig. 2-2, several micro-inverters can be parallel connected to the ac grid, or several dc-dc converters are parallel connected to one single central grid interfacing inverter. Restricted by the low voltage of a single PV module, this parallel connection type is mostly used for single phase PV applications.

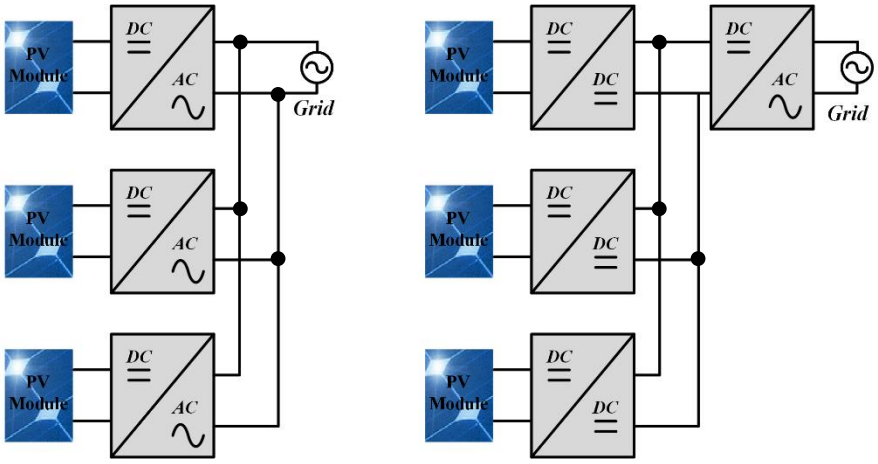


Fig. 2-2 Architectures for parallel connected module level converters: (a) parallel connected micro inverters and (b) parallel connected dc-dc converters with central inverter.

One single PV module with low dc voltage can be interfaced to a single phase ac grid with a higher voltage rating (110V-400V). The module level converters applied in parallel architectures need high voltage boosting ability. Hence, transformer isolated converters are usually a common choice to achieve a high step-up voltage ratio and safety requirements for single phase applications. Many transformer-less topologies have also been introduced to increase efficiency and reduce cost and size [5]. From a

modularity perspective, the transformer-less version can be seen as the future trend. Another important factor that needs to be considered is the low frequency harmonics in single phase PV applications. The power decoupling capacitor is a general solution and must be carefully selected during single phase PV inverter design. From the power stage view, multi-stage power conversion is usually selected to increase the voltage boosting ability, but single-stage novel topologies are also being widely researched [10][11][12].

Thus, parallel connected module level converters can be categorized and compared based on the following perspectives:

1) Transformer isolated or transformer-less topologies;
2) Positions of the DC decoupling capacitors; and
3) The number of cascaded power processing stages.

Firstly, the requirements and operation principle for dc decoupling will be analysed to provide background information for single phase PV applications. Secondly, the isolated single phase PV inverter will be discussed with consideration to three different positions of the dc decoupling capacitors. Then, transformer-less micro inverter topologies will be reviewed based on their basic step-up converter cells. The power stages will also be compared. Then the advantages and disadvantages will be drawn up for parallel connected full power processing module converters.

2.3.1 Power decoupling requirements for single phase PV inverter

a) Power decoupling principle

A generic grid-connected, single-phase PV inverter is shown in Fig. 2-3. For the MPPT algorithm, the output of PV module is a constant DC power. At a specific condition, the constant power is equal to I_M times U_M which are the current and voltage at this maximum power point.

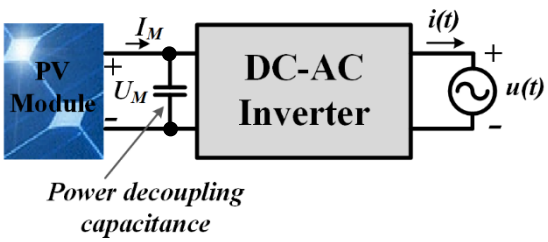


Fig. 2-3 Power decoupling in a generic single-phase PV inverter.

When the grid side voltage and current are expressed in the form of equation (1), where the ω is the line angular frequency.

$$\begin{cases} u(t) = U \sin \omega t \\ i(t) = I \sin(\omega t + \varphi) \end{cases} \tag{1}$$

The AC side time varying power can be obtained by multiplying the grid voltage *u(t)* and injected grid current *i(t)*, as in (2).

$$P_o(t) = \frac{1}{2}UI \cos \varphi - \frac{1}{2}UI \cos(2\omega t + \varphi) \tag{2}$$

Assuming the phase shift φ is zero, the grid power can be simplified to

$$P_o(t) = \frac{1}{2}UI - \frac{1}{2}UI \cos 2\omega t \tag{3}$$

If the power loss of the inverter is neglected, the average power part $P_{av} = \frac{1}{2}UI$ is equal to the DC power generated by the PV module. The pulsating power part $-\frac{1}{2}UI \cos 2\omega t$ oscillates at twice the grid frequency. To balance the power difference between the DC and AC side, energy storage components are needed as the decoupling device, which are usually decoupling capacitors [13][14]. The waveform of the total AC power $P_o(t)$ is plotted in Fig. 2-4.

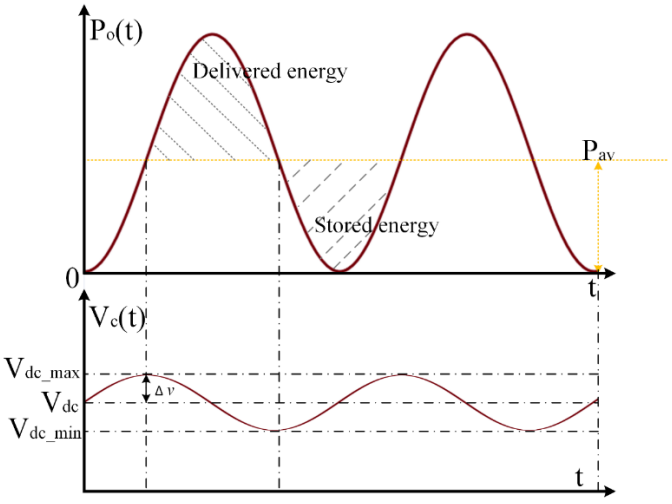


Fig. 2-4 The power balancing achieved by the decoupling capacitance

Due to the MPPT function, the average power output P_{av} is the value of $V_{MPP} \times I_{MPP}$ which is the maximum DC output power P_{dc} of the associated PV module. When P_{av} is greater than the instantaneous AC output power $P_o(t)$, the excess DC power will be stored in the decoupling capacitor. For the other half cycle of $P_o(t)$, the stored energy can be delivered to compensate the shortage of DC power.

To eliminate the relatively large second harmonic ripple of the ac output power, electrolytic capacitors are usually used and the capacitor voltage is depicted in Fig. 2-4. The capacitor can be selected according to the energy balancing principle considering the voltage ripple applied to it.

$$\begin{aligned} E &= 2\int_0^{\frac{T}{8}} (P_o(t) - P_{dc})dt \\ &= \tfrac{1}{2}CV_{dc\_\max}^2 - \tfrac{1}{2}CV_{dc\_\min}^2 \\ &= \tfrac{1}{2}C\left(V_{dc} + \Delta v\right)^2 - \tfrac{1}{2}C\left(V_{dc} - \Delta v\right)^2 \end{aligned} \tag{4}$$

where T is the fundamental period of ac side voltage and Δv is the absolute voltage ripple value of dc side voltage. Subtracting (3) from (4), the capacitance can be obtained as follows. The capacitor value can be influenced by factors: output DC power, line frequency, applied DC voltage to the capacitor, and absolute DC voltage ripple [13].

$$C = \frac{P_{dc}}{2\omega V_{dc}\Delta v} \tag{5}$$

b) DC decoupling capacitor selection

As a key component for the single phase micro inverter to deal with low frequency harmonics, the DC decoupling capacitor will affect the reliability, efficiency and control strategies of the PV system. Another influence is the PV system lifetime. Each micro inverter is often manufactured onto the back of a PV module for a 'Plug-N-Play' function, hence, it is required to match the lifetime of the two. It is widely known that the lifetime of micro inverter is mainly evaluated by the size of the decoupling capacitors, and the amount of current they carry. A high current involves high power loss and increased temperature inside the capacitor which is the main factor to determine the lifetime [14].

The normal choice is an electrolytic capacitor which offers a higher energy volume. However, the lifetime of electrolytic capacitors varies greatly among different materials, power ratings and applied environment. The electrolytic capacitor is the weakest element inside the inverter with a relatively short operational lifetime [15]. In industry, the trend is to replace electrolytic capacitors with film capacitors for a longer operational lifespan of the latter [16][17].

2.3.2 Isolated topologies with different power decoupling techniques

The transformer isolated topology is a typical version of the micro inverter, to amplify the low DC voltage level of PV module to the higher AC grid. As shown in Fig. 2-5, a high frequency or line frequency transformer can be implemented depending on the converter structure. Nowadays, to improve modularity and increase systematic efficiency, the high frequency transformer isolated micro inverter is the main type. Hence, discussion of high frequency isolated topologies on reliability, efficiency and control complexity will be given in the following section, with regard to different DC decoupling locations.

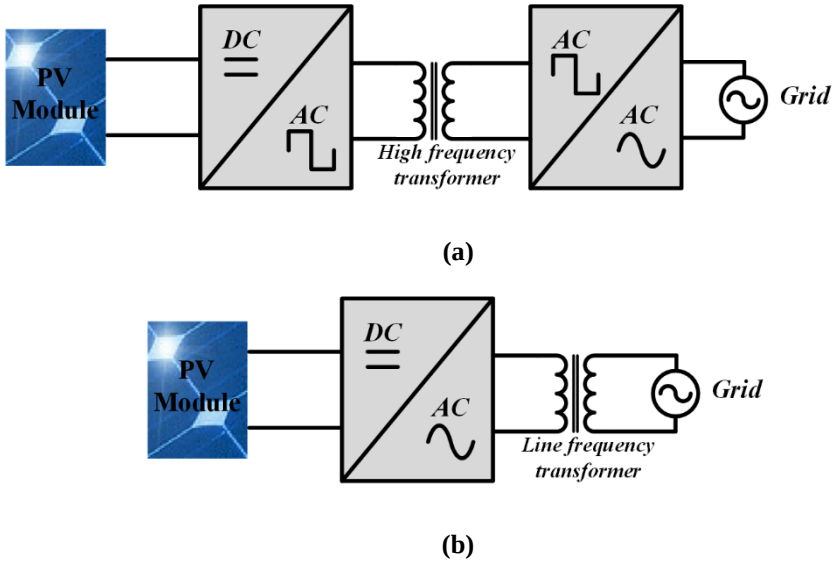


Fig. 2-5 Isolated PV module integrated inverters: a) high frequency transformer version and b) line frequency transformer version.

Micro inverter topologies can be categorized by different principles such as the number of cascaded power stages and AC grid interface features. The topology with a

pseudo DC link shown in Fig. 2-7 can be seen as a single power stage structure, with AC grid interfacing involving twice the line frequency. The DC link or AC link topologies shown in Fig. 2-6 and Fig. 2-8 are both multi power processing stages and their associated grid interfaces are high frequency PWM inverters.

A variety of high frequency isolated topologies have been presented to deal with power decoupling problems in single phase PV applications, with different features and efficiencies. According to the DC coupling capacitor positions, these topologies can fit into three groups, when referring to different topology configurations [14] [18]:

1. DC side decoupling for a micro-inverter with DC link;
2. AC side decoupling for a circuit without a DC link;
3. PV side decoupling for a topology with a pseudo DC link or without a DC link.

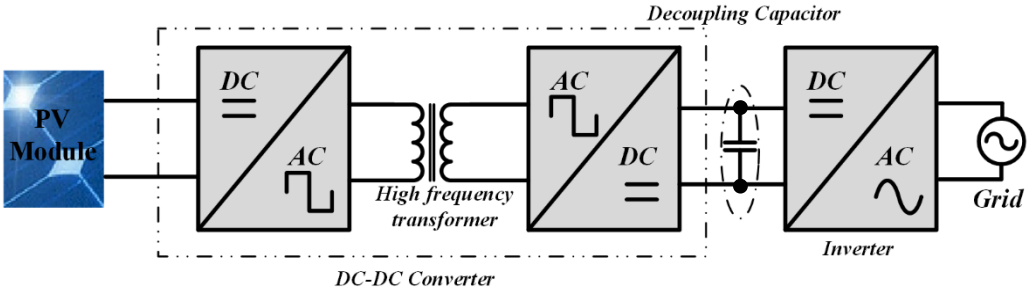


Fig. 2-6 Diagram of multi-stage topology with DC link configuration

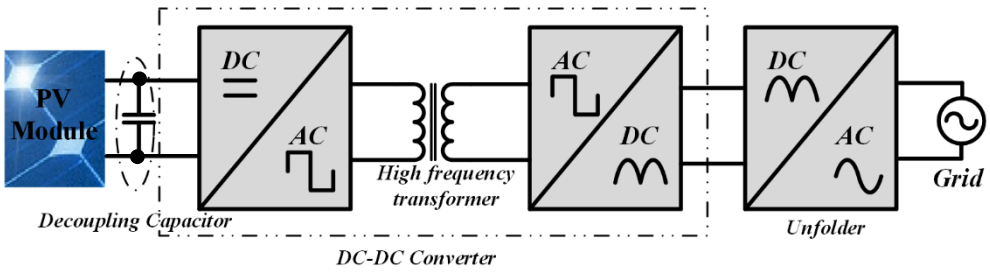


Fig. 2-7 Micro inverter topology with pseudo DC link configuration

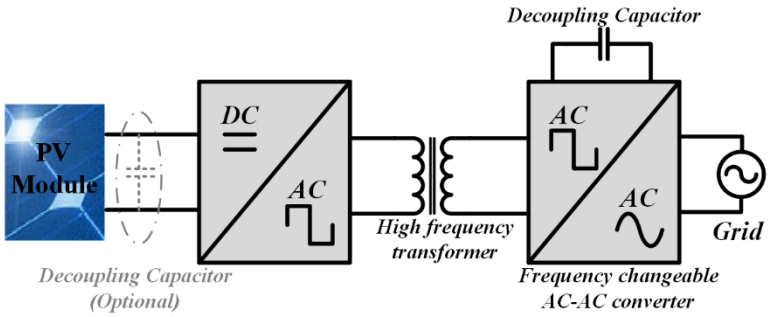


Fig. 2-8 Multi-stage micro inverter topology without DC link configuration

Different DC link configurations are designed for the single phase micro inverter to help reduce the decoupling capacitance. The representative topologies for three different positions of decoupling capacitors will be comparatively discussed.

a) PV side decoupling capacitor

Single power stage topologies for the single phase PV module level inverter are popular for their simple structures, high efficiency and low cost. This type of inverter generally has a pseudo DC link configuration as shown in Fig. 2-7. Thus the only position for the decoupling capacitor is at the PV side.

The utilization ratio of a PV module is the ability to extract the PV generated energy to the ac grid. To reach a high utilization ratio (>98%) and maintain maximum power output, the ripple amplitude of the PV side DC voltage must be sufficiently low (below 8.5%) [12].

When the decoupling capacitor is directly connected to the PV module, V_{dc} is the MPP voltage of its associated PV module which is usually a low DC voltage. The amplitude of the ripple Δv should be lower than 8.5% of the MPP voltage to reach a high utilization efficiency [19]. Based on this relationship, the PV side capacitance is quite high in present PV module specifications and could be 13.9mF for a 200W micro inverter to achieve a 98% utilization factor [15].

Several auxiliary power decoupling circuits have been designed to act as active filters to attenuate the pulsating power at twice line frequency in the single stage inverter [19]–[23]. With these additional circuits, the PV side capacitance can be reduced. In the following parts, two representative circuits will be discussed with one connected in series with the capacitor and the other is the parallel connection type.

A flyback module level inverter with two primary-side switches is shown in Fig. 2-9. Compared with the conventional flyback converter, the additional switch S_X converts the magnetizing current into the decoupling capacitance C_x when main switch S_M is off. The additional power decoupling circuit is series connected with the main power circuit and withstands the majority of the low frequency pulsating power. Hence, the averaged dc side current can be maintained constant and C_{DC} is small. Because the voltage ripple on C_x does not need to be too small for MPPT efficiency, the decoupling capacitor C_x is small enough to be a film capacitor[21]. For the cascaded decoupling power path, the overall conversion efficiency is low and is reported to be around 70% for the flyback inverter in [19]. Another issue is the complicated control and modulation strategy to attain the required small volume and low cost design objective.

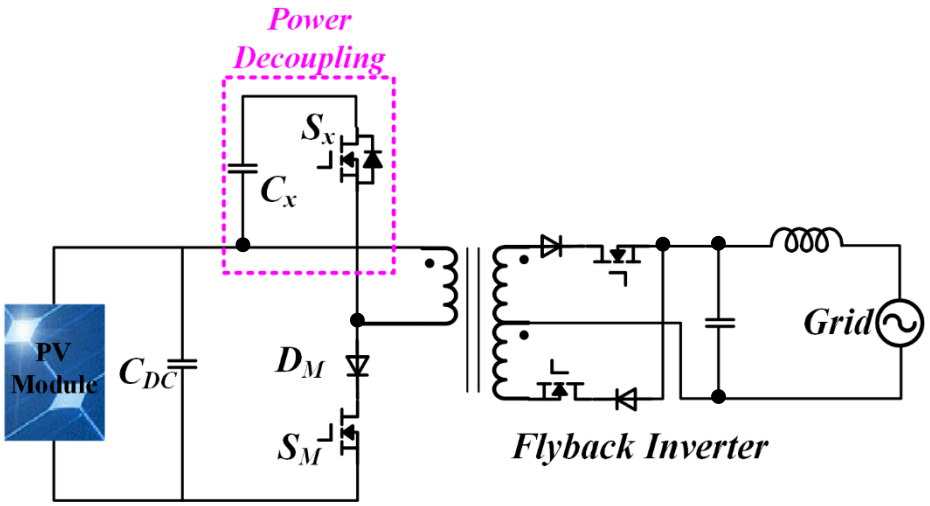


Fig. 2-9 Series connected power decoupling circuit for flyback PV module integrated Inverter

An auxiliary converter with bidirectional power flow, named Current Pulsation Smoothing Parallel Active Filter (CPS-PAF), is connected in parallel with the PV side capacitor C_{DC} as shown in Fig. 2-10 [23].

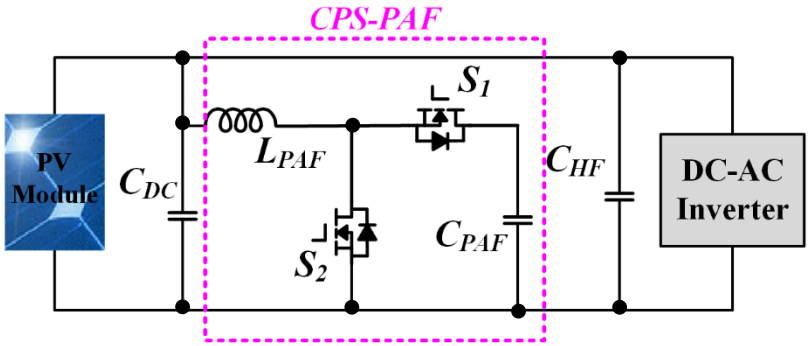


Fig. 2-10 Parallel connected active filter for current pulsation smoothing.

Different from the series connected ripple current reduction topologies, the CPS-PAF is independent of the PV inverter topology and deals with the current difference between the PV module output and the ac grid. When the grid current is larger than the PV module MPP current, the decoupling circuit acts as a buck-mode converter to supply the current difference from PV side to ac grid side. When the MPP current is larger than the ac grid current, the auxiliary circuit operates as a boost-mode converter. Thus, the second harmonic current ripple flows through the CPS-PAF circuit and the capacitor CPAF can be calculated as:

$$C_{PAF} = \frac{0.422\pi P_{DC}}{\omega(V_H^2 - V_L^2)} \tag{6}$$

where V_H and V_L are the maximum and minimum voltage of the PAF capacitor.

From equation (6), a large difference between V_H and V_L reduces the PAF capacitance, but this increases the switching losses. Hence, there is a trade-off between capacitance and system efficiency. Compared with a purely decoupling capacitor configuration, the capacitance in this structure can be significantly decreased. Thus, film capacitors can replace bulky electrolytic capacitors to prolong system lifetime.

The decoupling circuits are actually active energy buffers which allow the replacement of electrolytic capacitors with film capacitors. The common disadvantage is that the overall system efficiency is reduced due to the extra switching circuits. Although parallel connected circuits show less negative influence on system efficiency than the series connected circuits, problems cannot be resolved completely.

b) DC side decoupling capacitor

The multi stage inverter structure in Fig. 2-6 has a step-up DC-DC converter power stage. Generally, it is a common choice to put a small capacitor at the high DC voltage link. As discussed, the PV link DC voltage for single PV module is restricted to a low value and voltage ripple must be small enough to guarantee MPPT efficiency. The DC link configuration in Fig. 2-6 can tolerate higher voltage ripple.

According to equation (5), the decoupling capacitance value at the high voltage DC link can be significantly decreased compared with that at low voltage PV link. Thus, it is possible to remove the electrolytic capacitor with a high reliability film capacitor for longer lifetime and reduced system cost.

The middle DC link voltage must satisfy two requirements:1) stay within a safe operation region; and 2) must always be greater in magnitude than the instantaneous ac side voltage for proper dc-ac inversion [24]. The relationship between the dc link voltage and ac voltage is drawn in Fig. 2-11. The DC capacitance value is selected as follows.

$$C_{dc} = \frac{P_{PV}}{\omega V_{av} \Delta V} \tag{7}$$

where the DC average voltage is V_{av} and ΔV is the twice line frequency voltage ripple which is the difference between the maximum and minimum DC voltage.

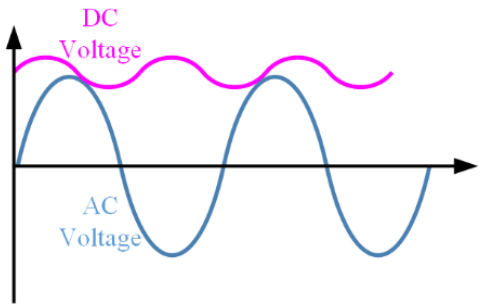


Fig. 2-11 Voltage waveforms for DC link configurations and AC grid side.

Theoretically, the voltage ripple ΔV needs to be increased for smaller DC link capacitance. However, the maximum DC voltage is predefined by the operation region and the minimum DC voltage must be above the instantaneous ac voltage. But higher DC voltage ripple causes higher ac current distortion. The DC voltage ripple is restricted by these two factors.

To resolve this issue, several control and modulation strategies attempt to decrease the ac current distortion incurred by DC voltage ripple. To attenuate the low frequency dc voltage ripple, the approach proposed in [24] uses a low bandwidth control loop to achieve 25% voltage ripple. However, system dynamic performance deteriorates due to a low cut-off frequency.

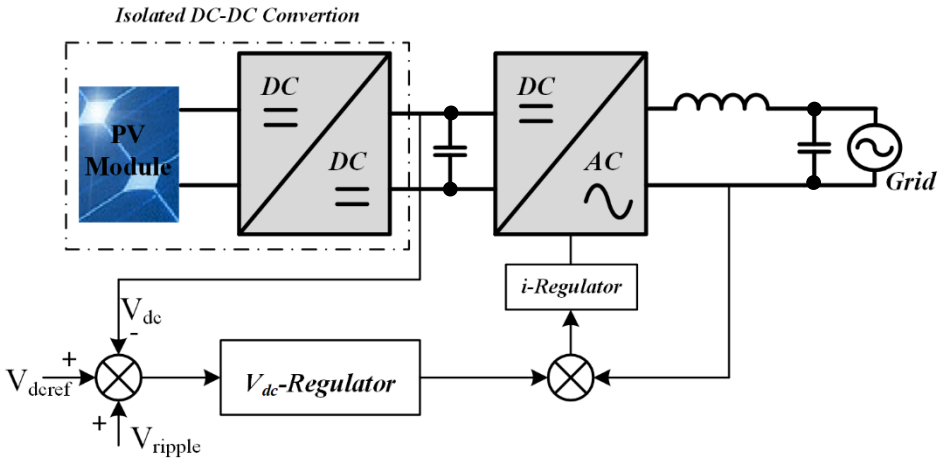


Fig. 2-12 Controller strategy based on voltage ripple estimation.

The concept of voltage ripple estimation is used in several publications to decouple the dc voltage ripple from the ac injected current. Both fast controller transient response and high bandwidth can be achieved in the presence of high dc voltage ripple. One representative control loop is shown in Fig. 2-12. The actual dc voltage is subtracted from the estimated voltage ripple, so influence from the dc side to ac side can be almost eliminated.

c) AC side decoupling capacitor

The multi stage inverter has a DC-AC-AC-AC structure, where the capacitor can be at the AC side with a combination of active and reactive components. For the high voltage swing at ac grid, it is possible to use film capacitors with high reliability.

One typical topology based on a current source inverter is presented to illustrate the ac decoupling operation principle [25]. As shown in Fig. 2-13, an extra phase is added to generate a power path for ac decoupling.

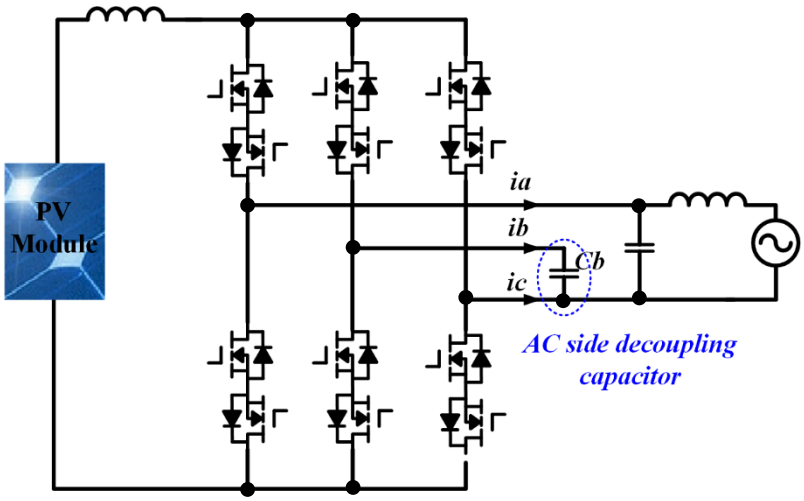


Fig. 2-13 Typical ac decoupling configuration topology.

This ac decoupling configuration can be seen as an unbalanced three phase ac system. To control this ac system, three phase voltages and currents are given in equation (8) and (9).

$$\begin{aligned} u_a &= U_a \sin \omega t \\ u_b &= U_b \sin(\omega t + \varphi_{ub}) \\ u_c &= 0 \end{aligned} \tag{8}$$

$$\begin{aligned} i_a &= I_a \sin(\omega t + \varphi_{ia}) \\ i_b &= I_b \sin(\omega t + \varphi_{ib}) \\ i_c &= -i_a - i_b \end{aligned} \tag{9}$$

The power can be calculated by:

$$\begin{aligned} P_{total} &= u_a i_a + u_a i_a + u_a i_a \\ &= ½\{U_a I_a \cos\varphi_{ia} + U_b I_b \cos(\varphi_{ub} - \varphi_{ib})\}\_P_1 \\ &-½\{U_a I_a \cos(2\omega t + \varphi_{ia}) \\ &\quad + U_b I_b \cos(2\omega t + \varphi_{ub} + \varphi_{ib})\}\_P_2 \end{aligned} \tag{10}$$

The first part P_1 in (9) is the constant DC power which is maintained at the PV maximum power. To isolate the twice frequency harmonic from the DC side, the

second part P_2 is controlled to be zero. Thus, the constraints for control strategy implementation are given in (11) and (12).

$$U_a I_a = U_b I_b$$
$$\varphi_{ia} = \varphi_{ub} + \varphi_{ib} + \pi \tag{11}$$

$$\varphi_{ib} = \varphi_{ub} + ½\pi$$
$$I_b = \omega C U_b \tag{12}$$

The power paths must be bidirectional to meet the control requirements. Moving the capacitor from the PV side to the AC side helps improve reliability.

The principle can also be applied to the voltage sourced inverter, as in [26], with an ac decoupling structure. A high frequency isolated single inverter can also use ac decoupling and one flyback inverter with ac decoupling capacitance is in [14].

In summary, lifetime and reliability are the main motivation behind the various power decoupling methods. The single stage inverter topology uses PV side decoupling circuits to solve these issues. However, circuit complexity is increased and overall system efficiency is influenced. For multi-stage inverters, dc-side decoupling or ac-side decoupling can be applied, while both require a complex control scheme. In practice, topology and decoupling methods should be designed based on considerations of cost, efficiency and energy performance ratio.

2.3.3 Transformer-less step-up topologies

The main objectives of modularized inverters are high efficiency, reliable operation and low manufacturing cost. Thus, non-isolated topologies are widely used for their high conversion efficiency and reduced architecture size.

The first PV inverter was a transformerless line commutated (voltage boost) inverter based on a thyristor bridge as shown in Fig. 2-12 (a). This kind of inverter configuration benefits from high efficiency, cheap implementation and robust operation. The low power factor (in the range of 0.6 to 0.7) implies special filter requirements. Thyristors have been replaced by high frequency semiconductor switches such as IGBTs and MOSFETs. A simple full bridge voltage source inverter is shown in Fig. 2-14(b) and the switching frequency can be significantly increased to

achieve a better quality factor [27]. Thus high frequency semiconductor devices are the trend for PV inverters. The single stage in Fig. 2-14(b) is a step down type inverter which means the PV module DC voltage must be greater than the AC grid voltage.

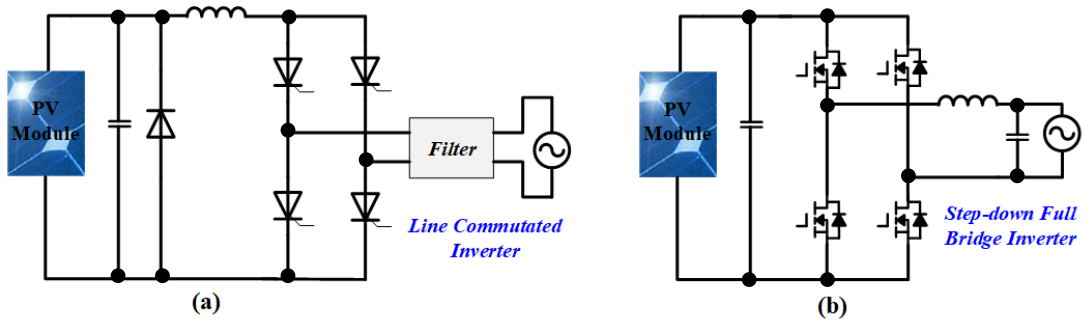


Fig. 2-14 Transformerless Full-Bridge Single-Phase PV Inverters. (a) Line commutated current source inverter topology and (b) Step down voltage source inverter topology.

For transformerless inverters, common mode voltages may be imposed on the PV side of configurations without a centre earth connection. Single phase inverters without isolation or earth connection cannot be used in some countries. The related standards and IEC documents are continuing to development in regards to earth connection requirements, such as UL 1741 and IEEE 929.

Novel topologies have been proposed to solve the grounding issue of transformerless inverters [11]. Except for grid requirements and power decoupling demands, leakage ground current monitoring and protection is important to topology design.

A non-isolated single-stage inverter version is usually not an attractive solution for voltage amplifying demanded in a module integrated inverter[15]. Boost converter stages are usually inserted to increase the dc voltage level. But series connected power conversion stages reduces efficiency, compared with a single-stage inverter structure. In the following section, transformerless topologies will be discussed based on power stages and ground current protection abilities. For each group, one representative circuit will be given to allow detailed analysis.

a) Two-Stage Topologies

A traditional two power stage configuration is depicted in Fig. 2-15 which consists of a boost dc-dc converter and a full bridge inverter. The higher DC link voltage has high tolerance to voltage ripple. So the decoupling capacitance C_p may be a film capacitor for longer life span. But the high voltage ripple deteriorates the ac side power factor.

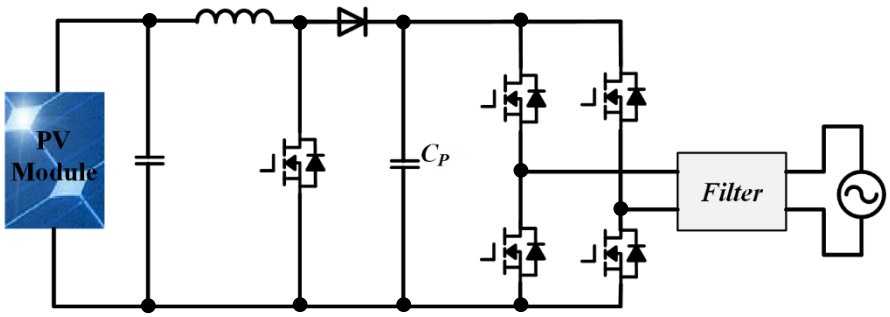


Fig. 2-15 Two power stage inverter with Boost DC-DC converter.

To improve the efficiency of this conventional two stage inverter, several modified topologies based on the boost dc-dc converter have been proposed. In [28], a dual mode inverter which applies a time sharing scheme during operation to decrease switching and conducting losses. Another modified inverter uses a soft switching principle [29].

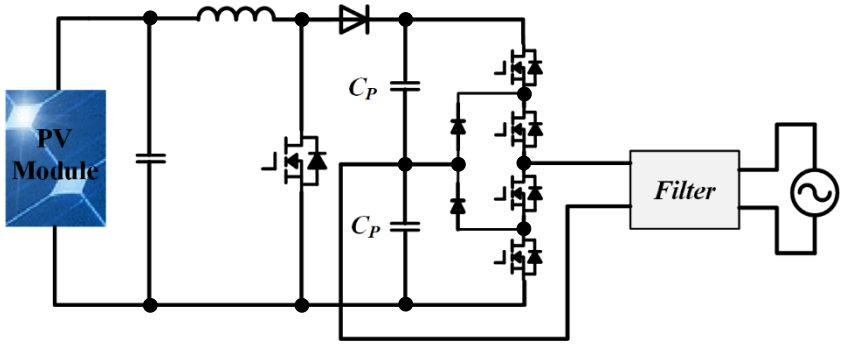


Fig. 2-16 Two stage configuration based on boost converter and NPC inverter.

One typical modification [30] replaces the full bridge inverter with a half bridge inverter, as shown in Fig. 2-16. The neutral-point-clamped configuration is used to reduce the filter size. An advantage is that the ground leak current can be reduced by connecting the middle point of dc stage to the grid neutral point. Several topologies

based on half bridges have been analysed in [5][11][31][32]. Emphasis has been on improving the boost voltage ratio and avoiding the bad influence of ground currents.

b) Pseudo-DC link Topologies

The topology structure on pseudo-DC link PV inverter is depicted in Fig. 2-17. The PV generated DC current is converted to sinusoidal DC current and then transformed into required AC current with an unfolding inverter. The inverter operates at line switching frequency which reduces the switching losses. The main disadvantage is the PV side large electrolytic capacitance which adversely affects system lifetime.

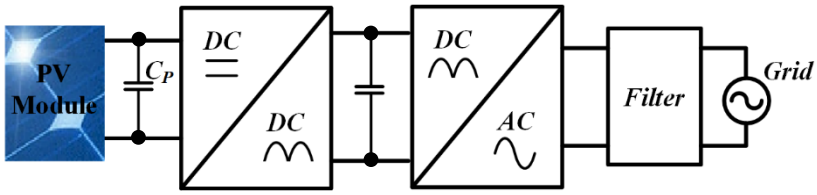


Fig. 2-17 Block diagram of PV inverter with Pseudo DC link.

Two typical topologies in [33] and [34] use inverting and non-inverting buck-boost dc-dc converters respectively. The discontinuous current mode is applied to both topologies. Low efficiency is a common problem for such buck-boost converter based topologies and the highest reported efficiency is 85% for a similar circuit in [35]. A time sharing scheme is applied in [36] to improve the efficiency to 98%. Basically, pseudo-DC link topologies suffer from large capacitance and low operational efficiency.

c) Single-Stage Topologies

Single power stage inverter structures are motivated by possible improved efficiency and increased system reliability. A typical topology is shown in Fig. 2-18 [37] in which the operation mode can be buck, boost or buck-boost to achieve single stage power inversion. This topology can accommodate a wide input voltage range to achieve high efficiency. Various similar topologies based on buck-boost operation can be found in [38], [39]. The buck-boost conversion stage can be integrated with the full bridge inverter and the associated topologies are shown in [40] and [10]. Several topologies apply a differential mode buck-boost converter or two buck-boost

converters for relatively independent power supply for each half cycle of the ac current [41][42]. The passive components are shared to reduce size and cost.

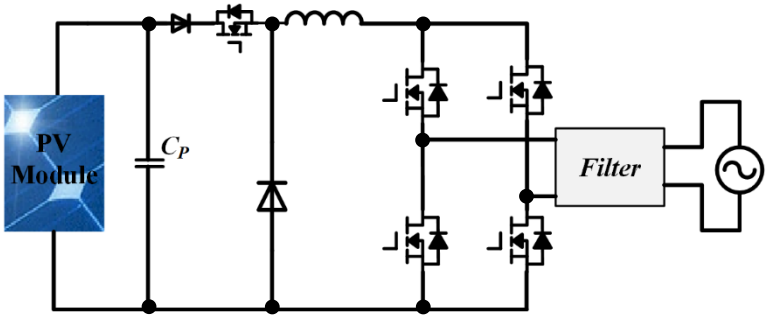


Fig. 2-18 A typical single stage PV inverter.

Similar to pseudo-DC link topologies, the bulky electrolytic capacitor is the factor to restrict developing single stage inverters. Voltage boosting ability is also a challenge. For these topologies, the full bridge inverter structure is implemented which means the leakage ground current may need treatment.

In conclusion, for the reviewed parallel connected inverters, it is difficult to select the best topology for a single phase PV inverter. Comprehensive analysis is necessary to select a premium solution in practice, considering power rating, voltage and current specifications. While the two stage transformerless topologies are usually better due to their higher voltage boosting abilities and lower DC link capacitance. The half-bridge inverter can be implemented with a combined high step-up dc-dc converter to solve the leakage ground current issue.

Thus, high step-up converter topologies are always a research topic for single phase PV applications. In Chapter 5, the impedance source converter based PV inverter will be analysed for its voltage boosting abilities. A new control strategy is proposed to solve common issues of high step up converters.

The main advantages of parallel connected PV systems are high reliability and low maintenance costs. The plug-and-play function provides flexibility for operation and system expansion. The essential function for parallel inverter structures is sufficient voltage magnifying ability. The restricted voltage boosting ability usually means that parallel connected configurations can only be applied in single phase PV applications. In the next section, series connection PV systems will be discussed.

2.4 Series connected module level PV system

Cascaded modular converters are used in single and three phase PV systems to implement distributed MPPT at high voltage levels. This type of full power processing DMPPT architectures can be divided into two groups: 1) cascaded DC-DC converters and 2) cascaded DC-AC converters, as shown in Fig. 2-19. In this section, the features for series connected MIC based DMPPT full power processing structures will be discussed in these two categories. A comprehensive review will be given for available converter candidates, control design, and application background.

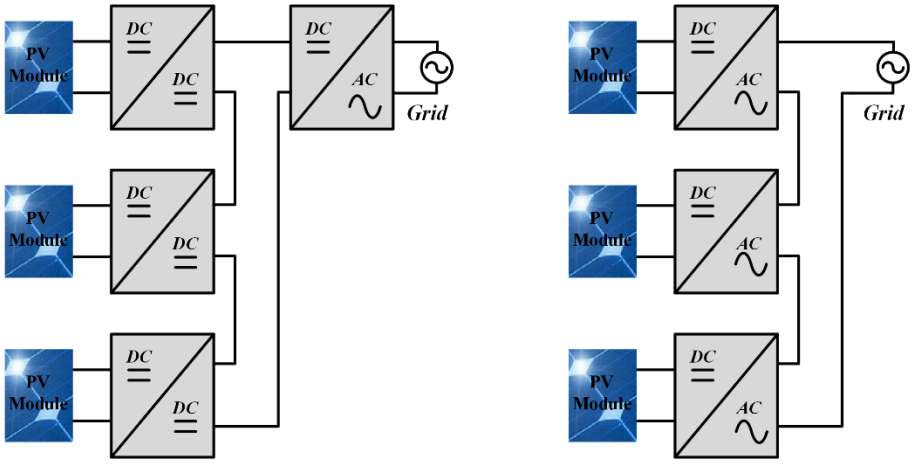


Fig. 2-19 Architectures of series connected full power processing DC-DC and DC-AC converters.

2.4.1 Cascaded DC-DC converter

The PV module integrated dc-dc converter is implemented to realize module level MPPT functionality. This type of converter is also called a front-end DC optimizer and each dc-dc converter deals with all the power generated by its associated PV module [43].

Compared to traditional string level architectures, cascaded dc-dc converters are more efficient and economical for applications in residential areas. It is reported to have up to a 40% increase in PV energy harvesting [44]. Another benefit is the availability to apply extra independent control and status monitoring with the integrated converter units. The number of MPPT units equals the number of PV modules. The MPPT functions are usually realized by individual dc-dc converters. A general solution is to apply a dual control scheme to each MIC. The MPPT reference

is supplied by a slow outer control loop and then fed into an inner controller with a higher bandwidth. A control structure is illustrated in Fig. 2-20 with two dc-dc converters and more converters can be used in practice. Each dc-dc converter is used as a MPPT unit with or without inner control and the central inverter is controlled by closed loop feedback.

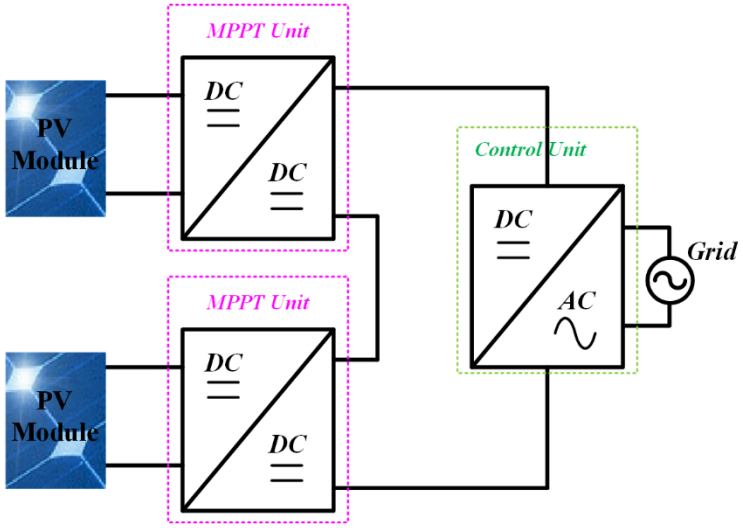


Fig. 2-20 MPPT and control scheme for cascaded dc-dc converters structure.

Parallel connected inverters must have large voltage step-up ability to convert the low PV module dc voltage to high ac voltage (240V ac). Usually more complex and less efficient topologies are implemented in series connection PV system [45].

In series connection PV systems, high voltage can be reached by stacking PV modules. Hence, a step-up topology is not a requirement. The widely used buck, boost, buck-boost and Cuk converters are possible solutions. Buck and boost units are easy to implement and show higher efficiency compared with other high order complex converters such as the Cuk and sepic converters [46]. One central inverter is needed for one PV string to interface to the ac grid. Two implementation architectures based on buck and boost converter cells are shown in Fig. 2-21 with two PV modules.

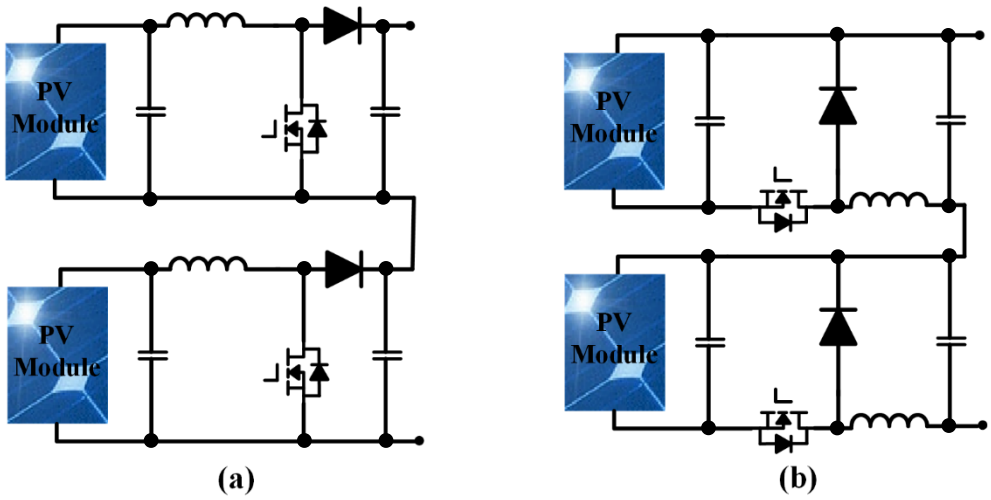


Fig. 2-21 The PV DC bus built with cascaded module converter. (a) Boost converter implementation and (b) Buck converter implementation.

The buck and boost converters have a simple structure and control. Although the boost converter is a step-up topology, the boost converter based cascaded PV system may not always deliver the allowable maximum power in extreme conditions. The boost converter does have the advantageous possibility of continuous input current. A PV string composed of buck converters can always transfer the maximum power for any shaded PV panels. High order converters such as the Cuk have continuous input and output characteristics, while the extra passive components complicate control.

The maximum and minimum number of PV modules differ for different converter types. For series connected buck converters, the control strategy is to step down the output voltage of shaded PV modules to match the string current. For boost converters, the output voltages of unshaded modules are increased to lower their current to match the current of shaded modules. The buck-boost converters can increase or decrease the output voltage which means more flexible control implementation. For a given DC bus voltage, the PV panel number for buck converters is the highest and for boost converters the number is the least, while the number for buck-boost converters is in the mid-range [47].

The main drawback is that each PV string needs a central inverter. In high power applications, it is difficult to parallel several PV strings to one central inverter and the equipment cost can be high.

2.4.2 Cascaded DC-AC converter

As one of the main multilevel converter types, the cascaded multilevel converter (CMC) topology is a promising solution for single phase PV systems. The topology is simple to implement and the requirement for isolated DC sources matches the distributed source nature of PV generators [48][49].

A cascaded H-bridge multi-level PV inverter is proposed in [2], as shown in Fig. 2-22. The outputs of several H-bridges are series connected to interface directly with the single phase ac grid. This architecture can also be applied at PV string level where one H-bridge inverter is directly connected to one PV string.

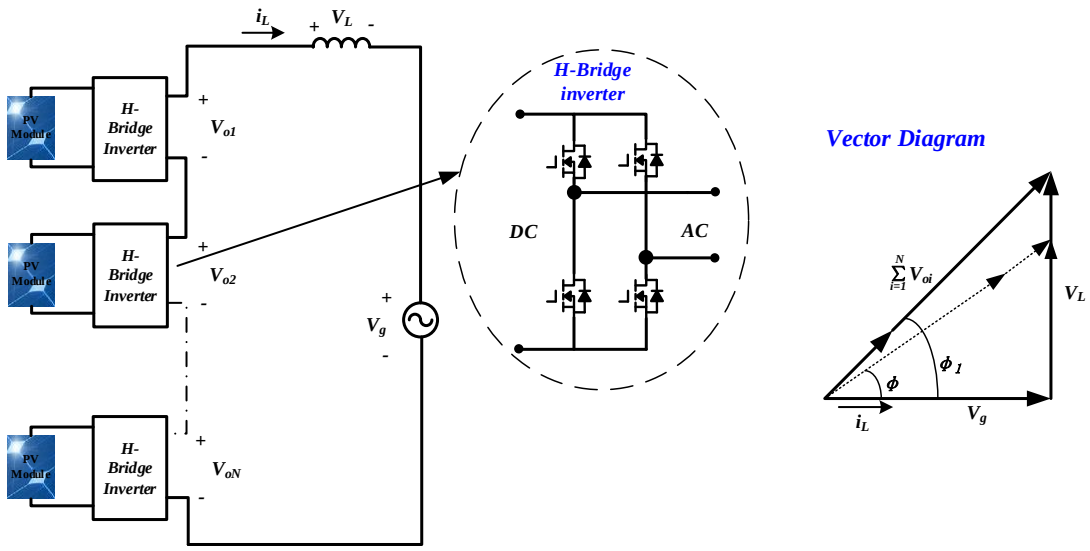


Fig. 2-22 Cascaded H-Bridge Multi-level PV inverter in a single phase PV system.

In comparison with the cascaded dc-dc converter configuration, the cascaded dc-ac converter structure does not need a central inverter for one PV string. Multilevel converter topologies have advantages of better output harmonic performance for multilevel output voltages levels. Hence, a smaller output filter can be designed which can reduce system costs and increase overall efficiency. The switching losses are significantly reduced compared with a central inverter, although the semiconductor count is increased, low voltage rated switching devices can be used.

In Fig. 2-22, if the number of PV modules is N, then the number of output voltage levels is $2N+1$. Different from series connected dc-dc converters, the control strategy is more complicated as the distributed MPPT and compensation to PV module

imbalance need to be directly dealt with by the dispersed dc-ac converters. In this scheme, the distribution of the overall ac modulating reference is adjusted dynamically based on the power contribution factor of each H-bridge module. With such a compensation and distribution strategy, the H-bridge string output voltage can be independently controlled around the grid voltage to perform normal power flow and grid voltage control. The vector diagram in Fig. 2-22 shows two unity power factor operational cases that supply different active power to the grid by varying the voltage phase difference [50].

2.5 Review of Impedance Source Converters

A single PV unit usually has a low output voltage. Matured schemes employ many units to create a high dc-link voltage for transferring the power through a conventional central inverter, which has only voltage step-down characteristics [51]. It has been discussed that this method does not guarantee an optimal operation point for each PV unit.

In many PV applications especially for single phase PV systems, power inverters with output voltage boosting ability are required to implement distributed MPPT function for improved energy utilization [5]. With such motivation, a range of high-order wide-output (HOWO) impedance source converters (ISCs) have been proposed for ac inverter applications that require voltage step-up ability [52][53].

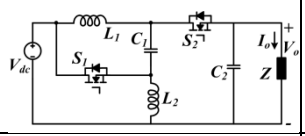
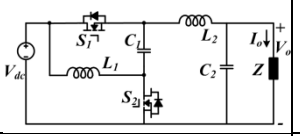
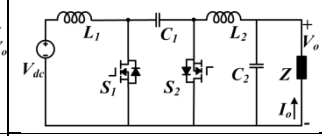
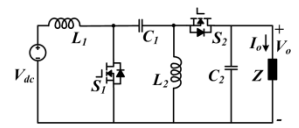
An impedance source converter has energy sourced by a current or voltage source, where a passive series path exists through more than one passive reactive element connected continuously between the energy source and the converter output or the energy source and its ground. With intrinsic passive impedance networks as energy sources, these converters can achieve output voltage boosting with either polarity, leading to improved dc-link voltage utilization compared with the conventional two-level converter [54].

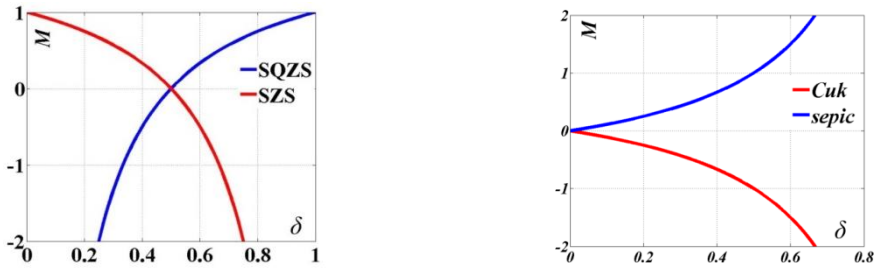
2.5.1 Operation principles of typical HOWO-ISC topologies

Four representative HOWO-ISC topologies, the Ćuk, sepic, semi-Z-source (SZS) and semi-quasi-Z-source (SQZS) topologies, are reviewed to give an understanding of their technical merits and operational challenges [55][56][57][58]. This set of converters consist of two inductors and two capacitors as in their dc-dc switched mode

classified by Tymerski [59]. By using an impedance network as a virtual energy source, these converters achieve improved dc-link voltage utilization and terminal current profiles. Based on inverter mode operation for a solar energy harvesting system, the characteristics of these topologies in three-phase configurations are analysed.

Table 2-3 Schematics, voltage transfer ratio, and voltage/current stresses of the power switches in four ISCs (δ'=1- δ).

	SZS G2[17]	SQZS G4[17]	Ćuk C5[17]	sepic G5[17]
Topology				
Voltage transfer ratio *M*	$M=-\frac{2\delta-1}{\delta'}$	$M=\frac{2\delta-1}{\delta}$	$M=-\frac{\delta}{\delta'}$	$M=\frac{\delta}{\delta'}$
Voltage stress	V_{dc}/δ'	V_{dc}/δ	V_{dc}/δ'	V_{dc}/δ'
Current stress	I_o/δ'	I_o/δ	I_o/δ'	I_o/δ'
input and output current	discontinuous/ discontinuous	discontinuous/continuous	continuous/continuous	continuous/discontinuous
High frequency isolated version	No	No	Yes	Yes



(a) **(b)**

Fig. 2-23 Steady-state voltage transfer ratio of: (a) SZS and SQZS; (b) Ćuk and sepic converters.

Table 2-3 summarizes the schematics and main operational features of four representative HOWO-ISC bidirectional topologies, including the semi-Z-source (SZS), semi-quasi-Z-source (SQZS), Ćuk and sepic converters, where all have two

inductors and two capacitors. In Table 2-3, where δ is the duty cycle of S_1 (complementally, $\delta'=1-\delta$ is the duty cycle of S_2) for all candidates, their voltage transfer ratio M can be derived from the inductor steady-state volt-second balance principle.

In Fig. 2-23 (a), the SZS and SQZS converters afford bi-polarity voltage output; while, as shown in Fig. 2-23 (b), the Ćuk and sepic converters have unipolar voltage gains. The extended output voltage range of these HOWO-ISCs create increased voltage and current stresses on the power switches, which are a function (M) of the duty cycle as in Table 2-3. Also, in [57][60] , the Ćuk and sepic converters can be derived into their high frequency isolated versions by using a coupled inductor.

The ISC topologies have been developed mainly to improve the AC side voltage magnitude (thus, dc-link voltage utilization) in the conventional half-bridge inverter [55]–[58], [61]. Using the basic converter modules in Table 2-3, both two-leg (four-switch) and three-leg (six-switch) configurations can be employed for three-phase dc-ac applications, as in Table 2-4.

As with typical six-switch three-phase (SSTP) inverters, and the topologies in Table 2-3**,** any dc components and zero sequence harmonics cancel in the output line-to-line voltages [55][57]. The four-switch three-phase (FSTP) inverter with two buck converters and the mid-point of dc-link capacitor feeding the three-phase output, reduces device and passive component count [62]. Similarly, for the ISC topologies, the sepic converter can be configured as a FSTP inverter by using the dc source positive terminal, since it has a positive step up/down gain [61]. This scheme inherits a dc offset common mode voltage between its dc ground and AC neutral point. To suppress such a dc common mode voltage, as shown in Table 2-4, the SZS and SQZS converters with bipolar voltage gain are developed as FSTP inverters in this thesis, among which the SQZS solution is selected as the case study for generic control design interpretation in Chapter 5. The Ćuk converter cannot be used as an FSTP inverter due to its negative voltage gain (the output cannot be within the input rail bounds).

2.5.2 Constraints of HOWO-ISCs

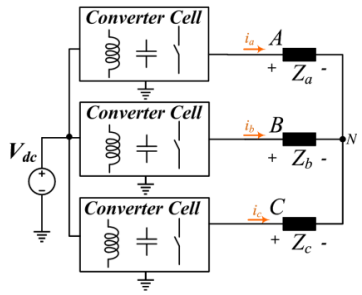
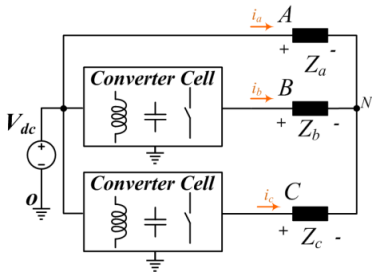
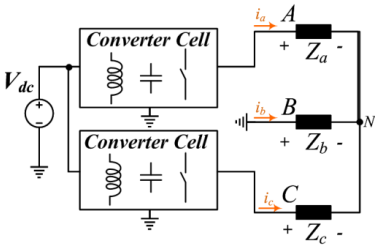
Although improved dc-link utilization can be achieved by ISC schemes, the passive components of their impedance network introduce a high number of poles and zeros (including RHP zeros) into their transfer functions. This leads to a low closed-

loop bandwidth, high steady-state error, and considerable lower order harmonic distortion for the HOWO-ISCs when conventional PI control is employed.

The six-switch three-phase converter inherits 2nd order harmonic distortion in its output voltage, which requires two parallel control loops to manage the fundamental and 2nd order harmonic simultaneously [55]. However, in the FSTP or single-phase applications, the lower order distortion is distributed continuously in the baseband including 3rd order harmonic components; hence this parallel loop method becomes complex and inefficient. The detailed analysis of the low order harmonic distortion is given in Chapter 5 with small signal modelling.

Table 2-4 Three-phase inverter configurations with the building blocks on Table 2-3.

V_m is the peak value of AC side phase voltage; ω is the fundamental angular frequency.

Three-phase inverter type	Possible topology in **Error! Reference source not found.**	Modulation Mechanism
 **SSTP inverter**	SZS, SQZS, Ćuk, sepic (with the zero sequence components being cancelled in the output line-to-line voltage) Ćuk and sepic can be high frequency transformer isolated	$V_{AN}(t) = V_m \sin \omega t$ $V_{BN}(t) = V_m \sin(\omega t - \frac{2}{3}\pi)$ $V_{CN}(t) = V_m \sin(\omega t + \frac{2}{3}\pi)$
 **FSTP inverter using positive dc terminal**	sepic (with positive voltage gain)	$V_{BO}(t) = V_{dc} - \sqrt{3}V_m \sin \omega t$ $V_{CO}(t) = V_{dc} + \sqrt{3}V_m \sin(\omega t + \frac{2}{3}\pi)$
 **FSTP inverter using dc side ground terminal**	SZS, SQZS (with bipolar voltage gain)	$V_{AB} = \sqrt{3}V_m \sin \omega t$ $V_{CB} = \sqrt{3}V_m \sin(\omega t + \frac{1}{3}\pi)$

To address this limitation, a generic repetitive control strategy applicable for all HOWO-ISC configurations is developed in Chapter 5. A comparison among several different popular control strategies for this type of converter is also given in that chapter.

2.6 Summary

Module level MPPT functionality is a promising solution to increase PV energy extracting ability and decrease system costs. This chapter gave a comprehensive review of various full power processing modular converters. The requirements and demands for PV system design have been listed according to international standards and guidelines.

According to the connecting type, parallel connected converters and series connected converters were reviewed separately.

Most parallel connecting architectures are restricted to a single phase ac grid. The main design consideration for a single phase PV system is the dc decoupling capacitor. According to the different decoupling capacitor positions, various topologies were compared. The trend is to build a high voltage DC-side to replace the bulky electrolytic capacitor with a film capacitor. Isolated topologies readily accomplish the high voltage requirement for ac grid interfacing. Transformerless topologies have attracted research attention for their potential to increase efficiency and reliability. Another advantage of non-isolated versions is compact design with reduced system cost and size. The leakage ground current restriction is the main consideration topic for transformerless topology designs.

Series connected module converters include cascaded dc-dc converters and cascaded dc-ac converters. Compared with parallel connected inverters, high voltage can be realized by series connecting PV modules, so that voltage step-up is not an aspect when selecting converter candidates.

Impedance source converters are widely applied in PV applications for their voltage boosting ability. The operation principle and control challenges are discussed to emphasize the general problem for this type of converters. In Chapter 5, a control scheme is proposed for high-order step-up module level inverters to deal with the common problems of impedance sourced converters.

All the module integrated converters reviewed are required to deal with all the power of the associated PV modules. The purpose of this review is to give insight into the possibility to apply MIC based PV systems in high power applications with more cost-effective solutions. In Chapter 3, partial power processing converters will be reviewed and a new topology will be presented in Chapter 4. Architectures with partial power processors can accomplish module level MPPT with reduced equipment cost and can be combined with a central inverter in large power applications.

References

[1] H. Zhou, J. Zhao, and Y. Han, "PV Balancers: Concept, Architectures, and Realization," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3479–3487, 2015, doi: 10.1109/TPEL.2014.2343615.

[2] B. Xiao, L. Hang, J. Mei, C. Riley, L. M. Tolbert, and B. Ozpineci, "Modular Cascaded H-Bridge Multilevel PV Inverter With Distributed MPPT for Grid-Connected Applications," *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, pp. 1722–1731, 2015, doi: 10.1109/TIA.2014.2354396.

[3] Y. K. Wu, J. H. Lin, and H. J. Lin, "Standards and Guidelines for Grid-Connected Photovoltaic Generation Systems: A Review and Comparison," *IEEE Trans. Ind. Appl.*, vol. 53, no. 4, pp. 3205–3216, 2017, doi: 10.1109/TIA.2017.2680409.

[4] K. Dang, H. Zhao, J. Yu, and T. Dang, "Study on interconnection standards of photovoltaic power generation," in *2011 International Conference on Electrical and Control Engineering*, Sep. 2011, pp. 6123–6126, doi: 10.1109/ICECENG.2011.6057011.

[5] D. Meneses, F. Blaabjerg, Ó. García, and J. A. Cobos, "Review and Comparison of Step-Up Transformerless Topologies for Photovoltaic AC-Module Application," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2649–2663, Jun. 2013, doi: 10.1109/TPEL.2012.2227820.

[6] Institute of Electrical and Electronics Engineers., *IEEE application guide for IEEE Std 1547, IEEE standard for interconnecting distributed resources with electric power systems*. Institute of Electrical and Electronics Engineers, 2009.

[7] "IEC 61727:2004 | IEC Webstore | invertor, smart city, LVDC." https://webstore.iec.ch/publication/5736#additionalinfo.

[8] "IEC 61000-3-2:2018 RLV | IEC Webstore | electromagnetic compatibility, EMC,

smart city, rural electrification." https://webstore.iec.ch/publication/62553.

[9] "IEEE 929-2000 - IEEE Recommended Practice for Utility Interface of Photovoltaic (PV) Systems." https://standards.ieee.org/standard/929-2000.html.

[10] L. G. Junior, M. A. G. de Brito, L. P. Sampaio, and C. A. Canesin, "Single stage converters for low power stand-alone and grid-connected PV systems," in *2011 IEEE International Symposium on Industrial Electronics*, 2011, pp. 1112–1117, doi: 10.1109/ISIE.2011.5984200.

[11] P. A. Application, "Review and Comparison of Step-Up Transformerless," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2649–2663, 2013.

[12] S. B. Kjær, *Design and control of an inverter for photovoltaic applications*. Institute of Energy Technology, Aalborg University, 2005.

[13] H. Hu, S. Harb, N. Kutkut, I. Batarseh, and Z. J. Shen, "Power decoupling techniques for micro-inverters in PV systems-a review," in *2010 IEEE Energy Conversion Congress and Exposition*, pp. 3235–3240, doi: 10.1109/ECCE.2010.5618285.

[14] H. Hu, S. Harb, N. Kutkut, I. Batarseh, and Z. J. Shen, "A Review of Power Decoupling Techniques for Microinverters With Three Different Decoupling Capacitor Locations in PV Systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2711–2726, 2013, doi: 10.1109/TPEL.2012.2221482.

[15] F. B. Soeren Baekhoej Kjaer John K. Pedersen, "A Review of Single-Phase Grid-Connected Inverters for Photovoltaic Modules," 2005, doi: 10.1109/TIA.2005.853371.

[16] H. Oldenkamp, I. J. de Jong, C. W. A. Baltus, S. A. M. Verhoeven, and S. Elstgeest, "Reliability and accelerated life tests of the AC module mounted OKE4 inverter," in *Conference Record of the Twenty Fifth IEEE Photovoltaic Specialists Conference - 1996*, 1996, pp. 1339–1342, doi: 10.1109/PVSC.1996.564381.

[17] "Electrolytic Capacitor » Capacitor Guide." http://www.capacitorguide.com/electrolytic-capacitor/.

[18] Q. Li and P. Wolfs, "A Review of the Single Phase Photovoltaic Module Integrated Converter Topologies With Three Different DC Link Configurations," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1320–1333, 2008, doi: 10.1109/TPEL.2008.920883.

[19] S. B. Kjaer and F. Blaabjerg, "Design optimization of a single phase inverter for photovoltaic applications," in *IEEE 34th Annual Conference on Power Electronics Specialist, 2003. PESC '03.*, vol. 3, pp. 1183–1190 vol.3, doi: 10.1109/PESC.2003.1216616.

[20] F. Schimpf and L. Norum, “Effective use of film capacitors in single-phase PV-inverters by active power decoupling,” in *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, 2010, pp. 2784–2789, doi: 10.1109/IECON.2010.5675091.

[21] T. Shimizu, K. Wada, and N. Nakamura, “Flyback-Type Single-Phase Utility Interactive Inverter With Power Pulsation Decoupling on the DC Input for an AC Photovoltaic Module System,” *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1264–1272, 2006, doi: 10.1109/TPEL.2006.880247.

[22] T. Shimizu and S. Suzuki, “A single-phase grid-connected inverter with power decoupling function,” in *The 2010 International Power Electronics Conference - ECCE ASIA -*, 2010, pp. 2918–2923, doi: 10.1109/IPEC.2010.5543511.

[23] A. C. Kyritsis, N. P. Papanikolaou, and E. C. Tatakis, “A novel Parallel Active Filter for Current Pulsation Smoothing on single stage grid-connected AC-PV modules,” in *2007 European Conference on Power Electronics and Applications*, 2007, pp. 1–10, doi: 10.1109/EPE.2007.4417545.

[24] F. Gao, D. Li, P. C. Loh, Y. Tang, and P. Wang, “Indirect dc-link voltage control of two-stage single-phase PV inverter,” in *2009 IEEE Energy Conversion Congress and Exposition*, 2009, pp. 1166–1172, doi: 10.1109/ECCE.2009.5316399.

[25] C. R. Bush and B. Wang, “A single-phase current source solar inverter with reduced-size DC link,” in *2009 IEEE Energy Conversion Congress and Exposition*, 2009, pp. 54–59, doi: 10.1109/ECCE.2009.5316285.

[26] T. Shimizu, T. Fujita, G. Kimura, and J. Hirose, “A unity power factor PWM rectifier with DC ripple compensation,” *IEEE Trans. Ind. Electron.*, vol. 44, no. 4, pp. 447–455, 1997, doi: 10.1109/41.605618.

[27] M. Calais, J. Myrzik, T. Spooner, and V. G. Agelidis, “Inverters for single-phase grid connected photovoltaic systems-an overview,” in *2002 IEEE 33rd Annual IEEE Power Electronics Specialists Conference. Proceedings (Cat. No.02CH37289)*, 2002, vol. 4, pp. 1995–2000 vol.4, doi: 10.1109/PSEC.2002.1023107.

[28] K. Ogura, T. Nishida, E. Hiraki, M. Nakaoka, and S. Nagai, “Time-sharing boost chopper cascaded dual mode single-phase sinewave inverter for solar photovoltaic power generation system,” in *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*, 2004, vol. 6, pp. 4763-4767 Vol.6, doi: 10.1109/PESC.2004.1354841.

[29] Y. Kim, J. Kim, Y. Ji, C. Won, and Y. Jung, “Photovoltaic parallel resonant dc-link soft switching inverter using hysteresis current control,” in *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2010, pp. 2275–2280, doi: 10.1109/APEC.2010.5433553.

[30] L. Ma, T. Kerekes, R. Teodorescu, X. Jin, D. Floricau, and M. Liserre, “The high efficiency transformer-less PV inverter topologies derived from NPC topology,” in *2009 13th European Conference on Power Electronics and Applications*, 2009, pp. 1–10.

[31] J. L. Duran-Gomez, E. Garcia-Cervantes, D. R. Lopez-Flores, P. N. Enjeti, and L. Palma, “Analysis and evaluation of a series-combined connected boost and buck-boost dc-dc converter for photovoltaic application,” in *Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, 2006. APEC ’06.*, 2006, p. 7 pp., doi: 10.1109/APEC.2006.1620657.

[32] S. V Araujo, P. Zacharias, and B. Sahan, “Novel grid-connected non-isolated converters for photovoltaic systems with grounded generator,” in *2008 IEEE Power Electronics Specialists Conference*, 2008, pp. 58–65, doi: 10.1109/PESC.2008.4591897.

[33] F.-S. Kang, C.-U. Kim, S.-J. Park, and H.-W. Park, “Interface circuit for photovoltaic system based on buck-boost current-source PWM inverter,” in *IEEE 2002 28th Annual Conference of the Industrial Electronics Society. IECON 02*, 2002, vol. 4, pp. 3257–3261 vol.4, doi: 10.1109/IECON.2002.1182920.

[34] S. Saha and V. P. Sundarsingh, “Novel grid-connected photovoltaic inverter,” *IEE Proc. - Gener. Transm. Distrib.*, vol. 143, no. 2, pp. 219–224, 1996, doi: 10.1049/ip-gtd:19960054.

[35] O. Abdel-Rahim, M. Orabi, and M. E. Ahmed, “High gain single-stage inverter for photovoltaic AC modules,” in *2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2011, pp. 1961–1967, doi: 10.1109/APEC.2011.5744865.

[36] Z. Zhao, M. Xu, Q. Chen, J. Lai, and Y. Cho, “Derivation of boost-buck converter based high-efficiency robust PV inverter,” in *2010 IEEE Energy Conversion Congress and Exposition*, 2010, pp. 1479–1484, doi: 10.1109/ECCE.2010.5618248.

[37] B. S. Prasad, S. Jain, and V. Agarwal, “Universal Single-Stage Grid-Connected Inverter,” *IEEE Trans. Energy Convers.*, vol. 23, no. 1, pp. 128–137, 2008, doi:

10.1109/TEC.2007.905066.

[38] R. O. Caceres and I. Barbi, “A boost DC-AC converter: analysis, design, and experimentation,” *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 134–141, 1999, doi: 10.1109/63.737601.

[39] T.-J. Liang, J.-L. Shyu, and J.-F. Chen, “A novel DC/AC boost inverter,” in *IECEC ’02. 2002 37th Intersociety Energy Conversion Engineering Conference, 2002.*, 2002, pp. 629–634, doi: 10.1109/IECEC.2002.1392119.

[40] S. Funabiki, T. Tanaka, and T. Nishi, “A new buck-boost-operation-based sinusoidal inverter circuit,” in *2002 IEEE 33rd Annual IEEE Power Electronics Specialists Conference. Proceedings (Cat. No.02CH37289)*, 2002, vol. 4, pp. 1624–1629 vol.4, doi: 10.1109/PSEC.2002.1023043.

[41] N. Vazquez, J. Almazan, J. Alvarez, C. Aguilar, and J. Arau, “Analysis and experimental study of the buck, boost and buck-boost inverters,” in *30th Annual IEEE Power Electronics Specialists Conference. Record. (Cat. No.99CH36321)*, 1999, vol. 2, pp. 801–806 vol.2, doi: 10.1109/PESC.1999.785602.

[42] N. Kasa, H. Ogawa, T. Iida, and H. Iwamoto, “A transformer-less inverter using buck-boost type chopper circuit for photovoltaic power system,” in *Proceedings of the IEEE 1999 International Conference on Power Electronics and Drive Systems. PEDS’99 (Cat. No.99TH8475)*, 1999, vol. 2, pp. 653–658 vol.2, doi: 10.1109/PEDS.1999.792757.

[43] D. Shmilovitz and Y. Levron, “Distributed Maximum Power Point Tracking in Photovoltaic Systems - Emerging Architectures and Control Methods,” *Autom. – J. Control. Meas. Electron. Comput. Commun.*, vol. 53, no. 2, 2012, doi: 10.7305/automatika.53-2.185.

[44] G. R. Walker and J. C. Pierce, “Photovoltaic DC-DC module integrated converter for novel cascaded and bypass grid connection topologies — Design and optimization,” in *2006 37th IEEE Power Electronics Specialists Conference*, 2006, pp. 1–7, doi: 10.1109/pesc.2006.1712242.

[45] G. R. Walker and P. C. Sernia, “Cascaded DC-DC converter connection of photovoltaic modules,” *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 1130–1139, 2004, doi: 10.1109/TPEL.2004.830090.

[46] E. Roman, R. Alonso, P. Ibanez, S. Elorduizapatarietxe, and D. Goitia, “Intelligent PV Module for Grid-Connected PV Systems,” *IEEE Trans. Ind. Electron.*, vol. 53, no. 4,

pp. 1066–1073, 2006, doi: 10.1109/TIE.2006.878327.

[47] M. Kasper, D. Bortis, and J. W. Kolar, “Classification and Comparative Evaluation of PV Panel-Integrated DC–DC Converter Concepts,” *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2511–2526, 2014, doi: 10.1109/TPEL.2013.2273399.

[48] J. Rodriguez, J.-S. Lai, and F. Z. Peng, “Multilevel inverters: a survey of topologies, controls, and applications,” *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, 2002, doi: 10.1109/TIE.2002.801052.

[49] M. Calais and V. G. Agelidis, “Multilevel converters for single-phase grid connected photovoltaic systems-an overview,” in *IEEE International Symposium on Industrial Electronics. Proceedings. ISIE’98 (Cat. No.98TH8357)*, vol. 1, pp. 224–229 vol.1, doi: 10.1109/ISIE.1998.707781.

[50] S. Ali Khajehoddin, P. Jain, and A. Bakhshai, *Cascaded Multilevel Converters and Their Applications in Photovoltaic Systems*. 2007.

[51] L. Zhang, K. Sun, L. Feng, H. Wu, and Y. Xing, “A Family of Neutral Point Clamped Full-Bridge Topologies for Transformerless Photovoltaic Grid-Tied Inverters,” *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 730–739, Feb. 2013, doi: 10.1109/TPEL.2012.2205406.

[52] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, and G. E. Town, “Impedance-Source Networks for Electric Power Conversion Part I: A Topological Review,” *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 699–716, Feb. 2015, doi: 10.1109/TPEL.2014.2313746.

[53] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, G. E. Town, and S. Yang, “Impedance-Source Networks for Electric Power Conversion Part II: Review of Control and Modulation Techniques,” *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1887–1906, Apr. 2015, doi: 10.1109/TPEL.2014.2329859.

[54] Fang Zheng Peng, “Z-source inverter,” *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504–510, Mar. 2003, doi: 10.1109/TIA.2003.808920.

[55] P. Li, G. P. Adam, Y. Hu, D. Holliday, and B. W. Williams, “Three-Phase AC-Side Voltage-Doubling High Power Density Voltage Source Converter With Intrinsic Buck–Boost Cell and Common-Mode Voltage Suppression,” *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5284–5298, 2015, doi: 10.1109/TPEL.2014.2366377.

[56] D. Cao, S. Jiang, X. Yu, and F. Z. Peng, “Low-Cost Semi-Z-source Inverter for Single-Phase Photovoltaic Systems,” *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3514–

3523, Dec. 2011, doi: 10.1109/TPEL.2011.2148728.

[57] A. Darwish, A. M. Massoud, D. Holliday, S. Ahmed, and B. W. Williams, “Single-Stage Three-Phase Differential-Mode Buck-Boost Inverters With Continuous Input Current for PV Applications,” *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8218–8236, Dec. 2016, doi: 10.1109/TPEL.2016.2516255.

[58] J. Knight, S. Shirsavar, and W. Holderbaum, “An improved reliability cuk based solar inverter with sliding mode control,” *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 1107–1115, Jul. 2006, doi: 10.1109/TPEL.2006.876786.

[59] R. Tymerski and V. Vorperian, “Generation, Classification and Analysis of Switched-Mode DC-to-DC Converters by the Use of Converter Cells,” in *INTELEC ’86 - International Telecommunications Energy Conference*, 1986, pp. 181–195, doi: 10.1109/INTLEC.1986.4794425.

[60] A. Ghasemi, E. Adib, and M. R. Mohammadi, “A new isolated SEPIC converter with coupled inductors for photovoltaic applications,” in *2011 19th Iranian Conference on Electrical Engineering*, May 2011, p. 1.

[61] M. S. Diab, A. Elserougi, A. M. Massoud, A. S. Abdel-Khalik, and S. Ahmed, “A Four-Switch Three-Phase SEPIC-Based Inverter,” *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4891–4905, 2015, doi: 10.1109/TPEL.2014.2363853.

[62] M. B. de Rossiter Correa, C. B. Jacobina, E. R. C. da Silva, and A. M. N. Lima, “A General PWM Strategy for Four-Switch Three-Phase Inverters,” *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1618–1627, Nov. 2006, doi: 10.1109/TPEL.2006.882964.

CHAPTER 3

Review of Partial Power Processing DMPPT Architectures

The *I-V* curve of a solar module exhibits a non-linear relationship between output current and terminal voltage. The maximum output power varies with sun irradiance and ambient temperature. In a PV string, the current must be the same for all its series connected modules. However maximum power point mismatch between modules may be caused by partial shading, manufacturing tolerances, etc. Then the string current will be limited to the least current output module, thus the power output of the string is decreased. In extreme conditions, shaded modules may introduce hot spots and induce permanent damage to the whole system. In this chapter, the PV module characteristics are described to emphasize the mismatch loss mechanism. The primary MPPT strategies to deal with mismatch losses are reviewed. The disadvantages of the full power processing DMPPT architecture are discussed. DMPPT architectures with partial power processing converters are a possible solution to inherit the merits of conventional DMPPT, with a reduced cost. In the last section, partial power processing DMPPT structures are reviewed in terms of two implementation features. Their main restrictions, when applied in large power systems, are discussed.

3.1 Background

The majority of commercialized photovoltaic (PV) technologies are either monocrystalline or polycrystalline silicon modules [1]. The open circuit voltages of such silicon modules range from 18V to 26V for a module of 36 cells or from 38V to 46V for one composed of 72 cells; in which the cell generated dc voltage is usually less than 1V [2]. The main challenge for PV systems is how to efficiently convert the low voltage direct current (dc) power produced by PV cells, to a high voltage alternate current (ac) power [3].

Existing PV inverters fit into three broad categories: centralized inverter, string inverter, and distributed micro-inverter. The micro-inverter continues to be a research topic and aims at a single PV module or even a single PV cell integrated architecture. It realizes module or cell level maximum power point tracking (MPPT) while dual-step or multi-step architectures are common for the high voltage amplification needed. Thus, the micro-inverter is suitable for low power application, such as residential roof installation. For a large power solar farm architecture, centralized or string inverters are mainstream. Generally, several PV modules are connected in series, creating a PV string, to increase the dc voltage level. The centralized inverter is fed from a PV array while a string inverter is usually sourced by one PV string [4].

The centralized and string configurations can only implement global MPPT which means the least efficient PV modules (shaded or defective) constrain the overall system energy capture efficiency. In order to solve this problem, module integrated dc-dc converters are proposed to perform distributed MPPT (DMPPT)[5].

Module level distributed MPPT architectures on full power processing converters were reviewed in Chapter 2. Different configuration types have been presented in academia and in industry, and micro inverters and DC optimizers are typical representatives. Although they force each single PV module to operate at its own maximum power point, to get the highest possible energy from PV generators, they are restricted from being widely used due to initial equipment cost and low conversion efficiency [6], [7]. But it is difficult to directly apply DMPPT in large scale PV grid connected systems. However, to increase competitiveness of PV generated electricity, large power scale PV systems have promising prospects to reduce the levelized electricity cost of PV power [4], [8], [9].

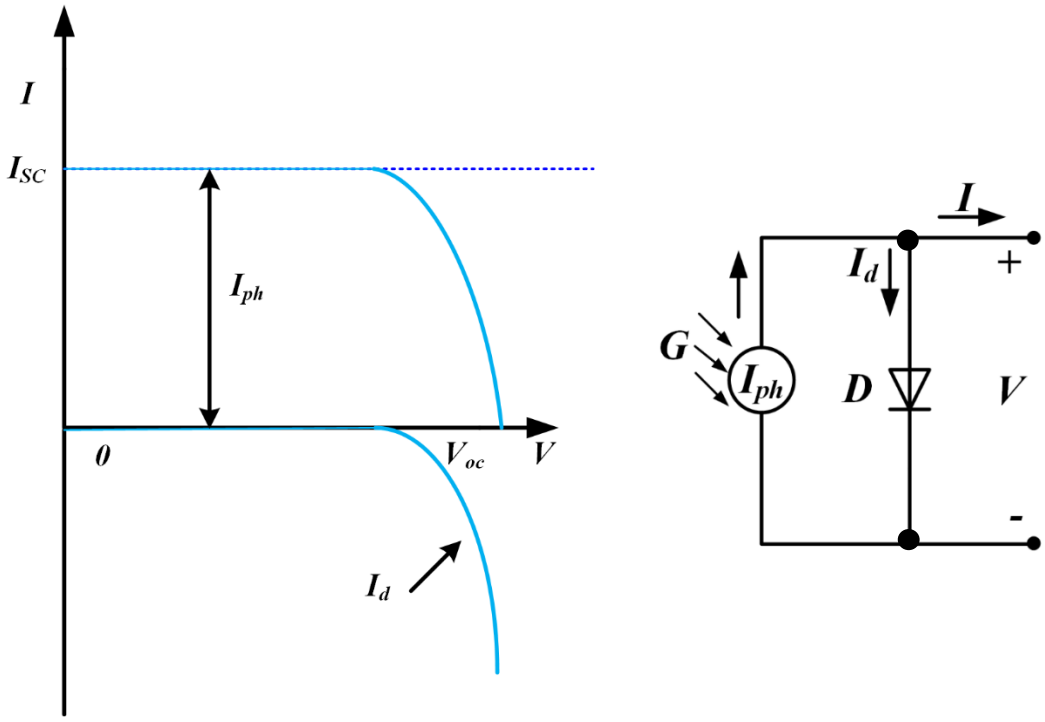
To retain the benefits of the DMPPT architecture and minimize potential cost and efficiency penalties incurred by auxiliary dc-dc converters, other DMPPT architectures, classified as partial or differential power processing approaches, have been proposed [10]. The main contribution of this kind of DMPPT architecture is the reduction of power processed by each auxiliary dc-dc converter. The reason such module level converters are named partial power or minimal power processing converter is that they only need to balance the generated power between PV modules. That means they can theoretically incur zero power loss when no mismatch occurs within the PV system. Thus, the electricity power ratings and costs of the partial power processing MICs can be significantly reduced. Another benefit is to provide more flexibility when connecting to large power centralized PV inverters. For these two advantages, they continue to be researched; thus it is worth reviewing such DMPPT structures.

Under the 'no mismatch, no processing' principle, a small fraction of PV generated power will be processed to maintain PV string balance, while most of the string's power flows directly without additional processing. The required power rating, size and manufacturing cost for the auxiliary converters are reduced. Thus, the conversion efficiency can be increased.

3.2 Mismatch Loss for PV Modules

3.2.1 PV Cell Characteristics

A single PV cell is the smallest element in a PV system, and is a p-n junction. It absorbs incident photon energy to generate electron-hole pairs which create electricity output. Ignoring the parasitic resistances of the PV cell, the electrical model and output characteristic is shown in Fig. 3-1. The light generated current I_{ph} is directly proportional to the absorption of sun irradiance and represented in Fig. 3-1(b) as an ideal current source. The overall output *I*-*V* relationship is the superposition of the current source and a shunt PV cell diode which is illustrated in Fig. 3-1 (a). The mathematical equation for this non-linear *I*-*V* relationship is explained by equation (1) where the photo current I_{ph} and diode reserved saturation current I_s are both temperature dependent parameters [8].



(a) **(b)**

Fig. 3-1 Single PV cell electrical characteristic: (a) output *I-V* curve and (b) simplified electrical model.

$$I = I_{ph} - I_s[\exp\left(\frac{qV}{nkT}\right) - 1] \quad (1)$$

n – Diode ideality factor.

q – Electron charge constant, 1.6e-19 C.

k – Boltzmann's constant, 1.38e-23.

T – Operating temperature, K.

The two important PV cell output characteristic parameters are:

1. Short circuit current I_{sc}: According to the equation (1), the short circuit current I_{sc} is equal to the photo current I_{ph} when the output voltage V is zero. So, it increases with sun irradiance absorbed by the cell area.
2. Open circuit voltage V_{oc}: When the output current I is zero, V_{oc} is expressed by equation (2) which shows a logarithmical relation with increased sun light.

$$V_{oc} = \frac{nkT}{q} \ln \left(\frac{I_{ph}}{I_s} + 1\right) \tag{2}$$

Another important solar cell factor is the maximum power point which is essential for PV system design. Graphically, the maximum power can be calculated as the largest rectangle within a given *I-V* curve. The expression for the maximum power point voltage V_{MPP} is shown in equation (3) [11]. A PV module is usually rated in terms of 'peak watts *Wp*' which is the maximum power output at standard sun light irradiance, 1kW/m^2.

$$\frac{d(IV)}{dV} = 0$$
$$V_{MPP} = V_{oc} - \frac{nkT}{q} \ln \left(\frac{V_{MPP}}{\left(\frac{nkT}{q}\right)} + 1\right) \tag{3}$$

The Fill Factor (FF) in expression (4) is another criterion to represent the quality of a PV module which is less than unity.

$$FF = \frac{V_{MPP} I_{MPP}}{V_{oc} I_{sc}} \tag{4}$$

In practice, the empirical expression in (5) is often used to give an approximate calculation for fill factor [12].

$$FF = \frac{v_{oc} - \ln (v_{oc} + 0.72)}{v_{oc}}$$
$$v_{oc} = \frac{V_{oc}}{nkt/q} \tag{5}$$

All the mentioned factors for the PV cell are based on a given sun irradiance, fixed temperature, and cell area. The effect of sun light is straightforward and can be seen from the given equations. While the influence of the PV cell operating temperature is more complicated. Temperature variations will mainly affect the open circuit voltage, diode saturation current and Fill Factor.

A Matlab Simulink model exists to simulate the influence of cell operational temperature and sun irradiance on the I/V and P/V characteristics of the commercial PV module 1Soltech 1STH-215-P. Fig. 3-2 shows the relationship between PV output characteristic and sun power at a specified temperature of 25°C. The MPP current and power decrease significantly with decreasing sun irradiance, while the MPP voltage changes slightly. In Fig. 3-3, the sun irradiance is set at 1000W/m^2 and the cell operational temperature varies, 25°C, 45°C and 65°C. The MPP current will not change significantly and the MPP voltage and power decrease with increased temperature.

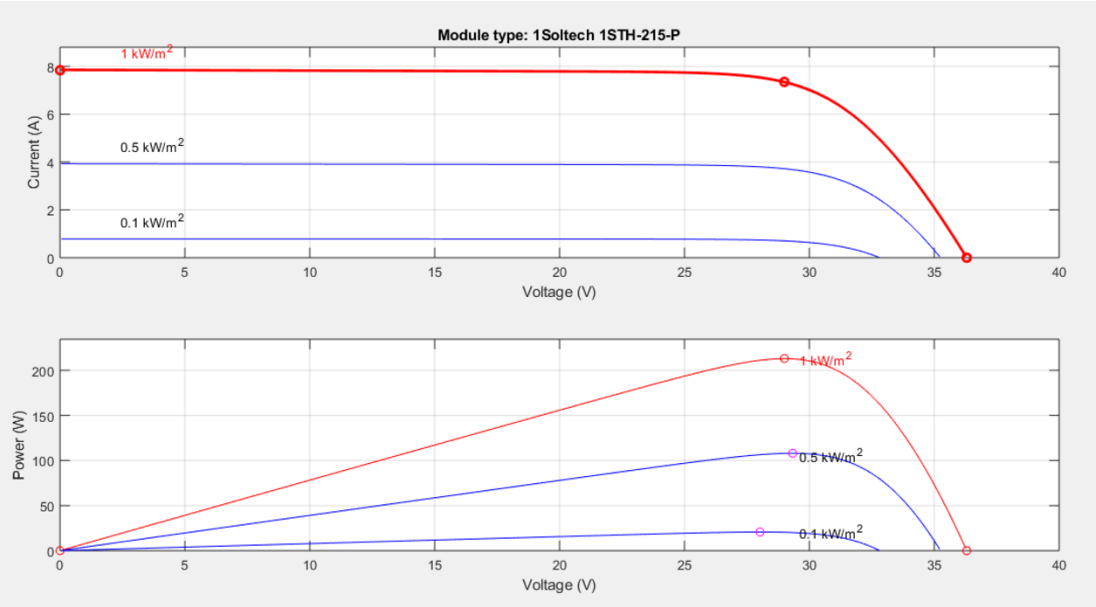


Fig. 3-2 PV module output characteristics influenced by different sun irradiance

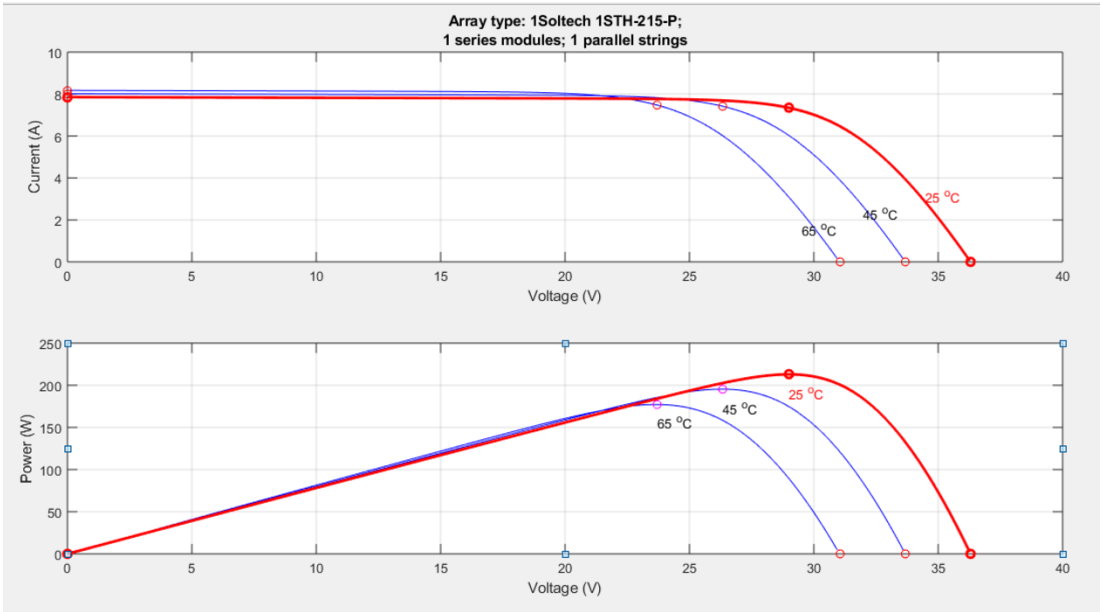


Fig. 3-3 PV module output characteristics affected by cell operational temperature variation.

3.2.2 PV Module Connection Type and Mismatch Loss Mechanism

For one PV cell, the maximum voltage is around 600 mV and the maximum photocurrent under 1000 W/m^2 of sun irradiance is about 30mA/cm^2. Cells are therefore usually connected in series and in parallel to obtain the desired power level. To get a nominal 12V, 36 cells are series connected.

Typical PV module connection is shown in Fig. 3-4. A group of PV cells are connected in series and then in parallel to form a PV module which is the basic building block for PV systems. And then these module blocks are further connected to form PV array with high power output [11]. The main reason for mismatch between PV modules inside the fully functional PV array is usually partial shading. Other factors such as different orientation of PV panels, dirt or dust on panels, different panel manufacturers and different aging can also contribute to mismatch loss [7].

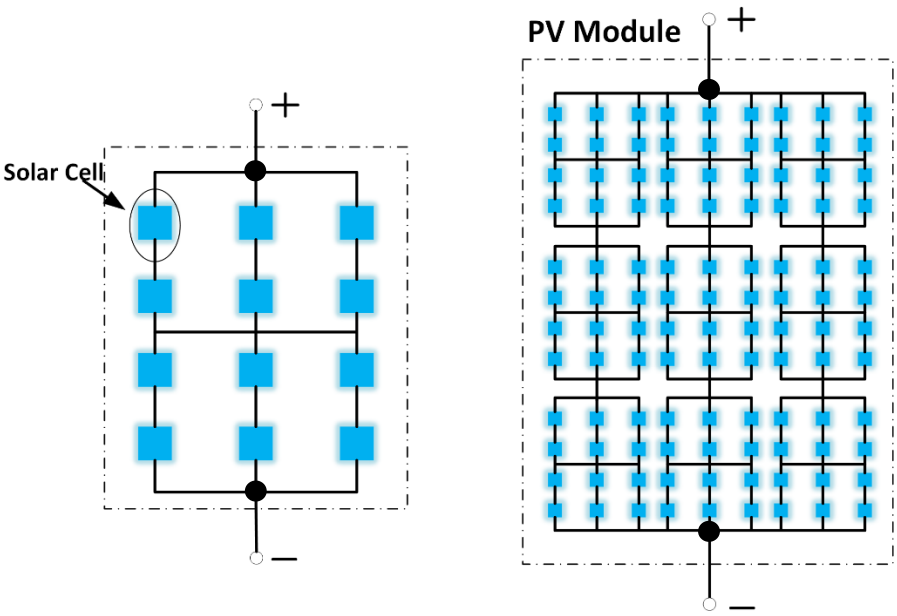


Fig. 3-4 Illustration of typical connection for a PV module.

If the number of parallel branches in a PV module is N_p and series connected cell number in each branch is N_s, then the total current and voltage relationship for the PV module can be derived from equation (6). Take the PV module in Fig. 3-4 as an example, N_p is 9 and N_s is 12.

$$I_{total} = N_p I_{ph} - N_p I_s [\exp\left(\frac{qV_{total}}{nkTN_s}\right) - 1] \quad (6)$$

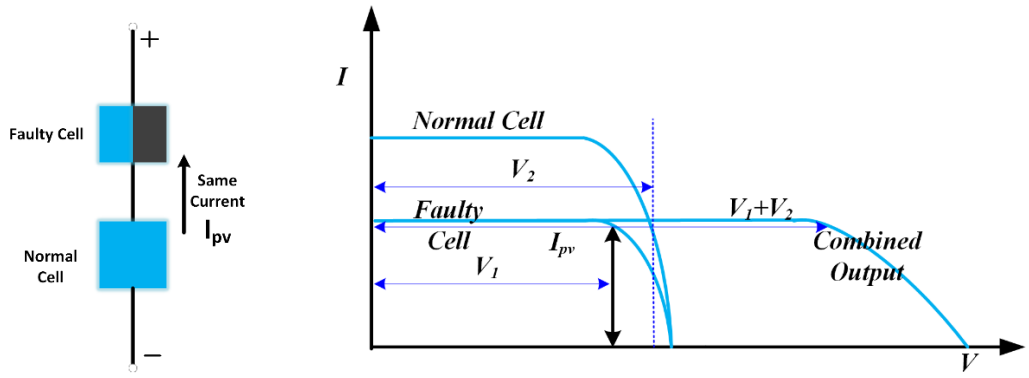
The *I-V* curve of the PV module shares the same shape as the PV cells, but with a scaler increase. The analysis based on one cell can be transplanted to the module level. To simplify analysis, mismatch loss will be discussed at the PV cell level, such that the mismatch mechanism and conclusions can be transplanted up to the module level PV system. It is reasonable and economical to analyse PV systems based on the PV module level. For the following sections, the PV module will be seen as the basic element to discuss compensation for mismatch losses and mismatch between cells can be ignored.

The ideal scenario is to build a PV module with cells having exact same characteristics, and to connect the PV modules to form a PV array with a higher dc voltage level. However, it is not possible to guarantee that PV cells or PV modules continuously have the same characteristics. Except for manufacturing reasons, degradation and partial shading are the main causes for a normal cell to become faulty

and generate less power output than usual. Mismatch loss is defined as the difference between the ideal output of a PV module and its actual output. Two typical scenarios are selected to clarify and illustrate the mismatch mechanism.

1) Mismatch between cells in series connection

As shown in Fig. 3-5 (a), two cells connected in series where one faulty cell generates less current than the normal cell. The maximum output current of the series string is confined to be as the same as the MPP current of the faulty cell. The MPP voltage can be found from the single cell *I-V* curve shown in Fig. 3-5 (b).



(a) (b)

Fig. 3-5 Mismatch loss for series connected cells. (a) One faulty cell is connected with a normal cell and (b) output *I-V* characteristics.

There is a difference between the desired maximum current and the actual maximum current for the normal PV cell. The forced current imbalance of the normal cell is the cause for the mismatch loss of the series connected PV string.

A PV string is usually comprised of many PV cells connected in series. In extreme conditions, if one cell generates less current than the others, the faulty cell may be reverse biased to become a load, not a power source. As shown in Fig. 3-6, the electrical characteristic of the faulty cell shifts to a lower MPP than the normal cells in the string. The string current is larger than the generated MPP current of the faulty cell. Then the faulty cell acts as a power sinking load, not a PV source. If the string is short circuited, the reverse voltage of the faulty cell is equal to the sum of voltages of all the other normal cells in the string. Significant power will be dissipated within the faulty cell. If the power sinking by the faulty cell is large and sustaining,

the temperature of the faulty cell may increase significantly and cause a hot spot within the string [13]–[15].

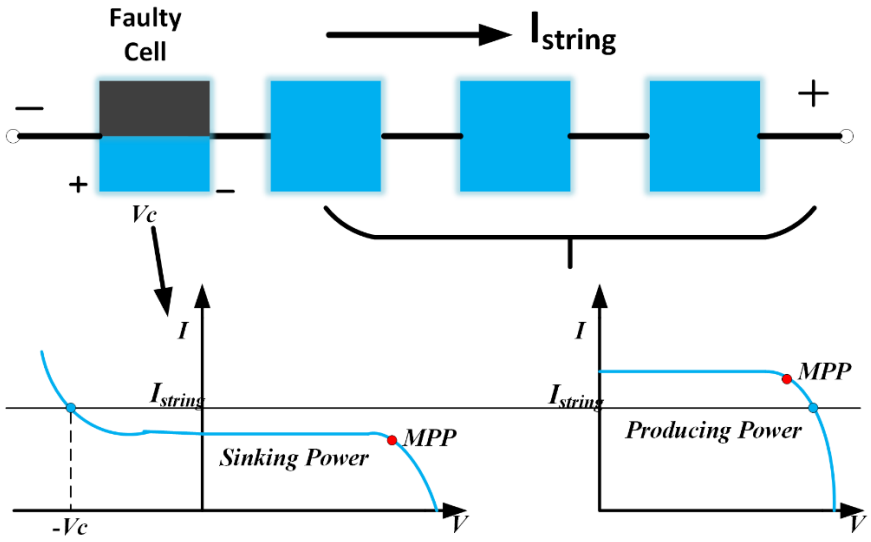


Fig. 3-6 Reverse bias of mismatched PV cell in a PV string.

Hot spotting results in serious consequences for the PV system. Manufacturers perform many tests before releasing a product to exclude the cells which may be susceptible to hot spotting. But hot spotting can also occur with partial shading and cell variation over a long operation period. Many detection and protective methods have been applied to this detection problem. A common way is to add a bypass diode to a group of cells within a PV module. The compensation function of the bypass diode is shown in Fig. 3-7. When the output current *I* is less than the generated photo current, the cell body diode will conduct the extra current and there is no current through the bypass diode. When the output current *I* is larger than the photo current, the additional current is flowing through the bypass diode. Hence, the bypass diode helps avoid sinking excessive power in a mismatched solar cell.

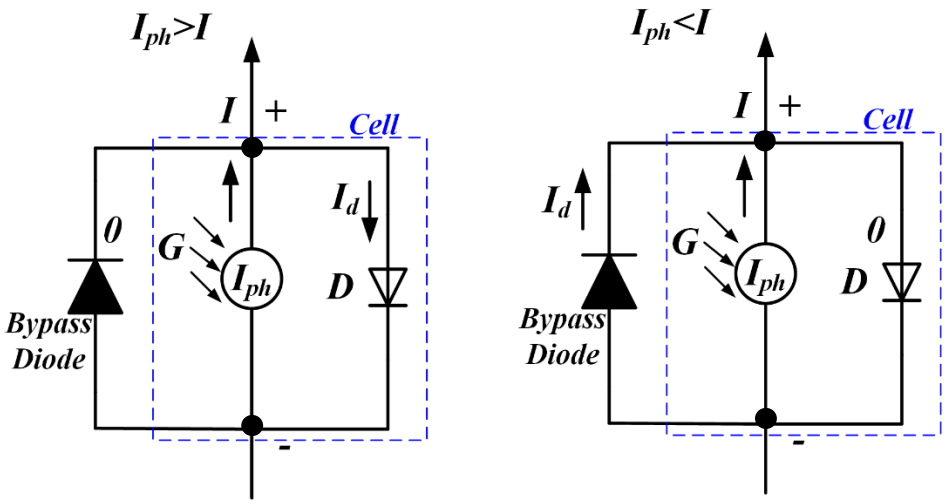


Fig. 3-7 Bypass Diode Compensating for Solar Cell Mismatch.

It is not practical or economical to add a bypass diode to every cell. Usually every 12 to 36 cells share one bypass diode to deal with possible hot spotting in a PV module. However, this complicates connection within the PV module and adds extra loss and cost.

2) Mismatch between cells in parallel connection

A simple model with two cells connected in parallel is given as an example to describe the mismatch loss for parallel connected cells. As shown in Fig. 3-8, the voltage of the PV string is restricted (reduced) by the faulty cell. The combined output current is the sum of the two cells. When the faulty cell exhibits lower maximum voltage output ability, the string's combined output voltage is decreased significantly by the faulty cell.

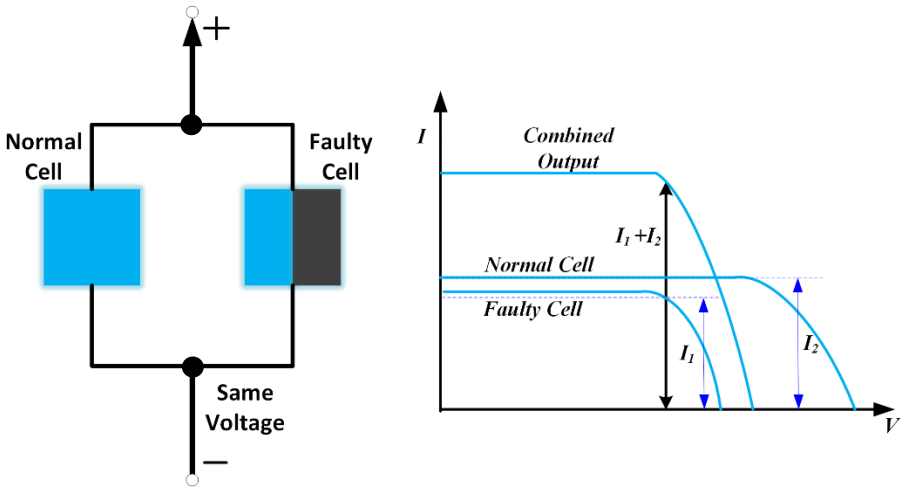


Fig. 3-8 Mismatch loss for parallel connected cells.

The mismatch mechanism for cells can be transferred to PV modules in practice. PV modules are connected in series and parallel for higher power output. Again, PV modules can be regarded as cells when dealing with mismatch losses. Current and voltage imbalance between PV modules have similar features as mismatched PV cells [16]. In this thesis, the mismatch compensation strategy will be discussed based on a module level for practical consideration. In next section, the main MPPT techniques will be reviewed, with strategies for dealing with different mismatch conditions included.

3.3 MPPT Strategies for Mismatched Conditions

One PV string consisting of parallel or series connected PV modules can exhibit a single global maximum power point which can be only achieved under uniform insolation and ideal PV module characteristics. In practice, this ideal condition usually cannot be satisfied for partial shading or other module mismatching factors. With mismatching, several different local MPPs can result in one PV string's output *I-V* or *P-V* curve. As shown in Fig. 3-9, a possible power-voltage characteristic curve during a partial shading condition shows one global MPP and two local MPPs. The challenge for the MPPT strategy design is to distinguish between the real global MPP and the local MPPs in mismatching conditions [17]–[19].

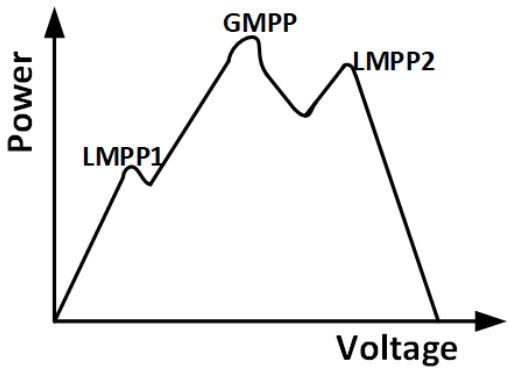


Fig. 3-9 *P-V* characteristic of a PV string showing one global MPP and multiple local MPPs in mismatching condition.

Many different MPPT algorithms have been proposed and implemented in the literature and for different PV applications [20][21]. The most widely used commercial MPPT techniques are Perturb and Observe (P&O) and Incremental Conductance (IC). The P&O method is also used in this thesis to implement MPPT in Chapter 4 and the operation principle of this algorithm is given in Appendix C.

Most conventional MPPT algorithms can only be applied to track one maxima which may lead to the wrong local MPPs during mismatching conditions [21]. To overcome this, traditional MPPT strategies can be optimized in three aspects to mitigate the influence of mismatching losses, viz.:

1) MPPT algorithm modification;
2) Converter connection alteration in the PV system architecture; and/or
3) PV panel connection variation according to non-uniform operating conditions.

In ideal circumstances, all of these methods can be used together for a PV system to attain real MPP tracking. In reality, a trade-off is needed to avoid high system cost caused by extra hardware and complex control implementation. Thus, most optimized MPPT strategies designed for mismatching conditions are a combination of one or two of the aspects mentioned, and can be classified into three categories in [21] in regards to their hardware configuration: CMPPT, DMPPT and RMPPT. In the following section, these three groups will be reviewed to highlight advantages and disadvantages.

i. Central MPPT (CMPPT) architecture

The CMPPT architecture applies a centralized converter for the whole PV array. The most widely used commercial traditional MPPT techniques are Perturb and Observe (P&O) and Incremental Conductance (IC) which readily lead to a false local MPP under non-uniform operating conditions [17]. To pursue the real global MPP, advanced MPPT algorithms can be implemented to optimize MPPT tracking accuracy [22][23][24]. Thus, CMPPT based modifications offer algorithm improvement.

In [17], the modified CMPPT strategies dealing with mismatching conditions are grouped into two types: 1) two-stage GMPPT algorithms and 2) soft computing-based optimization algorithms. The first method includes the detection of a mismatch occurrence and calculation and comparison of all LMPP to locate the real MPP. The latter soft computing method shows better performance to track the real global MPP

but suffers from a slow convergence speed. Basically, voltage sensor count, *P-V* curve scan portion, PV current measurement or not, and tracking speed are important factors during CMPPT based algorithm design.

In [21], similar classifications are applied to various CMPPT or the so called GMPPT methods: 1) techniques by hill climbing algorithms; 2) computational intelligence application; and 3) other approaches.

The Hill climbing algorithm (P&O or IC) is widely used in global MPP tracking and a large portion involve intelligence algorithms such as Fibonacci and PSO. The PV array voltage is measured for almost all of the CMPPT architectures and PV array current is generally needed. In a method using an artificial neural network, the sun irradiance is also measured.

To apply the Hill climbing algorithm, total or partial sweeping of the power-voltage curve identifies all the local MPPs and locates the global MPP correctly. The scanning technique has been optimized in many CMPPT architectures with advanced intelligence computing algorithms. The main converters are buck, boost or buck-boost based structures. The controlled parameters are usually PV array output voltage V_{PV} or duty cycle D of the main power converter.

In conclusion, the main advantages of the CMPPT are:

- Fewer sensors are necessary and
- Only one power stage is needed for MPPT tracking.

The main drawbacks of the CMPPT are:

- The sum of the available maximum power of all PV modules cannot be generated and
- Optimized algorithms are usually more complex than commercialized MPPT techniques.

ii. Distributed MPPT (DMPPT) architecture

DMPPT is similar to the concept discussed in Chapter 2 where the PV array is divided into distributed sections. The MPPT algorithm is implemented in the sub-sections to track the real global MPP. The operating condition for each PV module can be seen as a uniform state and mismatching within one PV module is ignored [25][26][27].

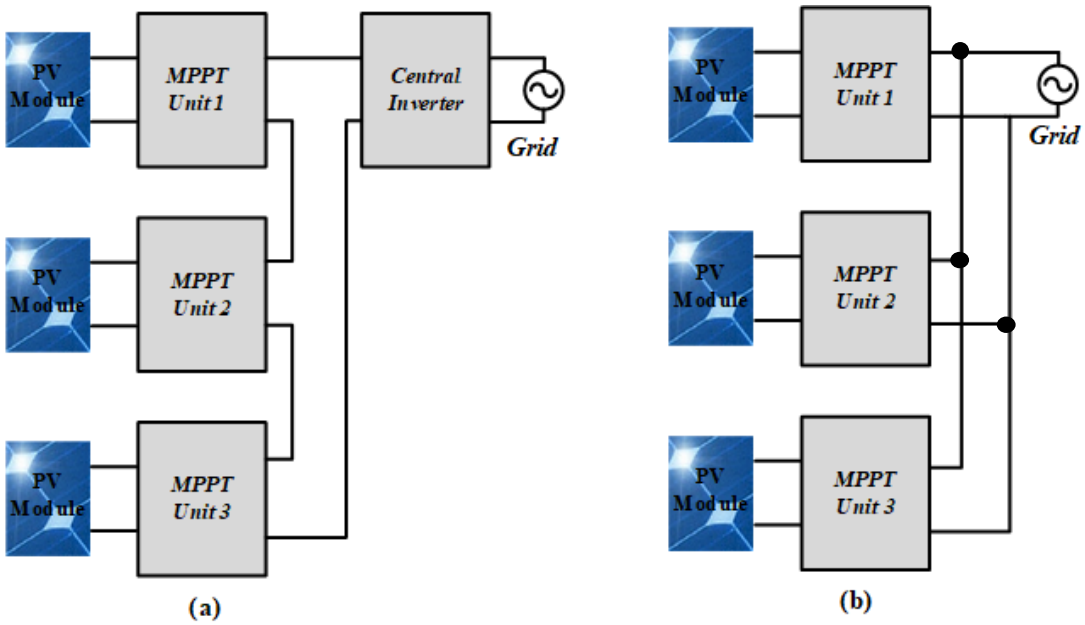


Fig. 3-10 DMMPPT architecture: (a) series connected and (b) parallel connected.

For full power processing distributed converters, it is straightforward to implement the DMPPT architecture. As shown in Fig. 3-10, one MPPT unit can be applied for a single dc/dc or dc/ac converter. The MPPT implementation for each unit is relatively independent, thus simple algorithms such as P&O and IC can be applied which reduces MPPT tracking complexity.

For the parallel connected structure in Fig. 3-10 (b), each MPPT can be controlled independently. While for series connected structure in Fig. 3-10 (a), the voltage constraint for each MPPT unit can be expressed as in (13), for a fixed dc bus.

$$V_{o,j} = V_{bus} \frac{P_j}{\sum_{i=1}^{n} P_i} \tag{7}$$

where the output voltage of each dc/dc converter is $V_{o,j}$ and the number of series connected converters is n. In a series connected structure, the MPPT units need to interact with each other to satisfy equation (13). Another important criteria is that the number of MPPT units should be the same as the sum of connected PV modules to avoid control redundancy [5]. As shown in Fig. 3-10 (a), the central inverter is not a MPPT unit.

The voltage limitation means the DMPPT architecture cannot deliver actual maximum power if the dc bus voltage is controlled to be a fixed value. The possible

solution is to use a PV string level inverter to allow a flexible string voltage. This increases the inverter number, with higher equipment cost compared with the centralized array level inverter implementation. In next chapter, a novel DMPPT architecture is proposed to give a high performance operation, with a high power centralized inverter.

For parallel connected DMPPT architectures, every sub-section converter is directly connected to the bus, thus, a high conversion ratio converter is needed to make sure the bus voltage can be maintained even during severe mismatch conditions.

Another concern is possible high switching loss and equipment cost which were discussed in Chapter 2. When no mismatch occurs, the full PV generated power has to pass through the sub-converter. There are several solutions to this problem. One is to combine the CMPPT with DMPPT. Without mismatching, the distributed converters are disconnected from the PV system to reduce losses. Another solution is to replace the full power processing sub-converters with partial power processing converters which can implement DMPPT with significantly reduced cost, and this solution will be discussed in detail in section 3.4.

iii. Real MPPT (RMPPT) architecture

A general structure of the RMPPT architecture is illustrated conceptually in Fig. 3-11. Multiple sensors are introduced for measurements of PV output voltages and currents at the PV module level as well as the PV array level. The cell operational temperature is also measured for each PV module to diagnose the mismatching condition. A matrix relay system is controlled by an algorithm to dynamically reconfigure the electrical connection of PV modules [28].

PV modules are interconnected dynamically by multiple switches. A control algorithm decides the switching of a matrix relays to give the best electrical configuration [29]. The reconfiguration algorithm makes a decision about the prime PV connection system according to the measurement results by exploring the stored possible PV configurations. As discussed in [20], a suitable PV connection type can be usually found to select a real global MPPT in a specific mismatching condition. It is a real time solution and does guarantee that all mismatch loss can be eliminated.

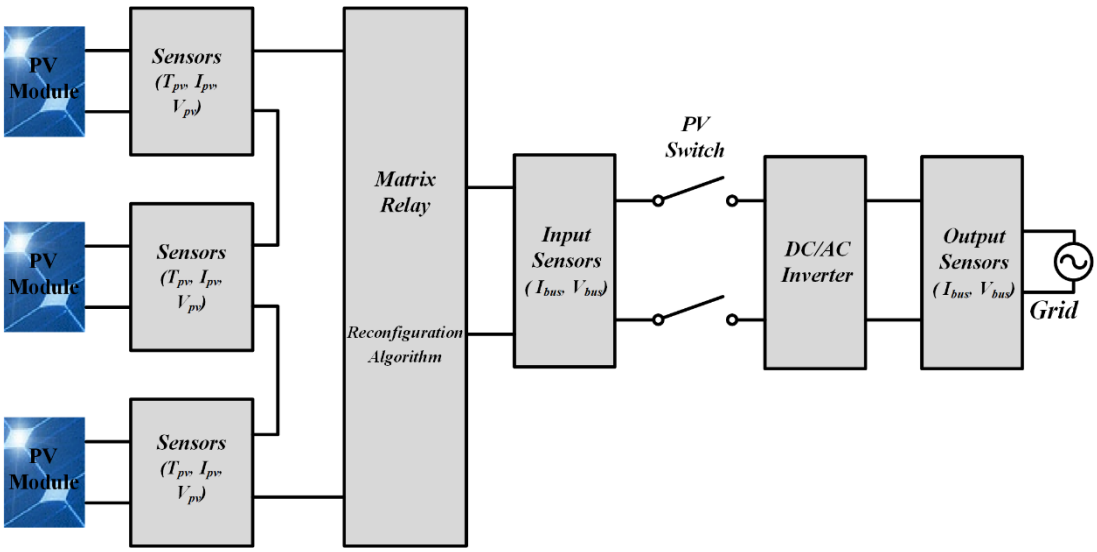


Fig. 3-11 RMPPT conceptual schematic.

After the matrix relay, a central inverter applies a global MPPT algorithm which is similar to the CMPPT concept discussed in the previous subsection. The PV switch disconnects the PV load with the PV generators when the matrix relay system is varying the physical connection types. The PV switch provides the electrical safety and can also breaks the circuit during electrical failure.

Compared with the CMPPT strategy, RMPPT can adjust the electrical configuration so the located GMPPT is close to the real available maximum power point. The concern for RMPPT is the requirement to disconnect the PV sources from the load to guarantee safety operation. Another burden is the extra source for the relay system and increased cabling because of the necessary reconfiguration.

iv. Conclusion

The CMPPT architecture needs the simplest hardware resources to enhance global MPP tracking accuracy. DMPPT and RMPPT architectures can extract more available solar energy during the same operating conditions, but their hardware structures and control strategies tend to be more complexed. The conventional DMPPT architecture uses full power processing converters which means higher hardware cost compared with CMPPT architectures. The hardware cost of the DMPPT architecture can be reduced by applying partial power processing converters which will be discussed in the next section.

It is not possible to select the best MPPT solution that suits all mismatched PV applications. The criteria for selecting a prime MPPT solution is influenced by different design objectives and investment plans, but there is a trend to use the DMPPT architecture. To mitigate DMPPT disadvantages, a partial power processing architecture offers a good balance.

3.4 Partial Power Processing DMPPT Implementation

Distributed MPPT architectures can be classified into two main categories according to power processing features: architectures dealing with the total PV generated power and architectures with partial power processing converters [7], [30]–[32]. The full power processing architectures were reviewed in Chapter 2 and are presently the main industrial DMPPT types. Different from full power processing converters, partial power converters process only a fraction of the PV generated power to fulfil a module level DMPPT function [5]. As shown in Fig. 3-12, the partial power path can involve a small portion of the full PV power and the total energy conversion efficiency can be increased.

In Chapter 2, full power processing converters were classified into series and parallel connecting types. Similarly, there are also series connected partial power converters to compensate the voltage variation in the PV string and parallel connected partial power converters to balance current mismatch between PV modules in a string [5], [33], [34].

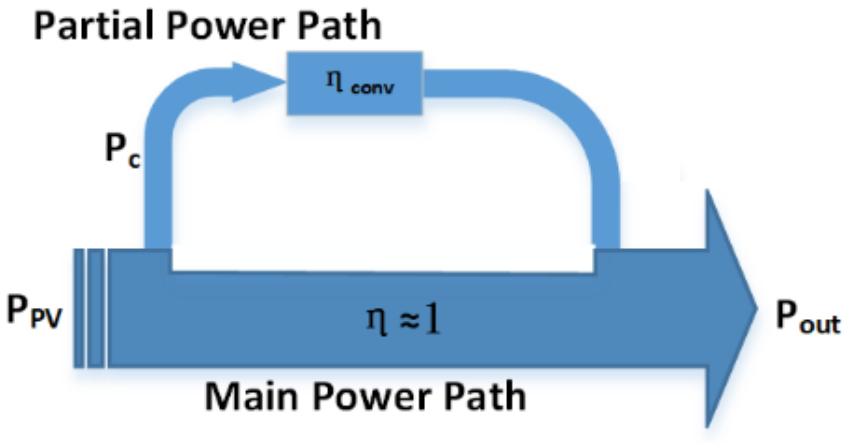


Fig. 3-12 The power path illustration for partial power processing architecture.

$$\eta_{total} = 1 - \frac{P_c}{P_{PV}}(1 - \eta_{conv}) \quad (8)$$

Partial power processing architectures pursue high efficiency DMPPT conversion with a significantly reduced system cost. Partial power processing converters must exhibit some special features and the control implementation is more complexed. This section reviews suitable converter candidates, controller design features and MPPT implementation requirements for applying partial processing DMPPT architectures in PV applications.

3.4.1 Current Balancing Differential Converters

For series connected photovoltaic modules in a PV string, current mismatch among modules can cause power loss for the entire PV string and possibly hotspot problems. The mismatch mechanism was discussed in section 3.2 along with conventional solutions and associated restrictions. All mismatches are discussed and compensated at PV module level in this chapter.

Module level MPPT tracking can significantly boost the energy captured from PV generators especially in conditions with varying sun irradiance. This benefit can be outweighed by relatively high cost for a large number of full-power module level converters, in a uniform sun distribution situation [16].

The concept of energy shuffling or current diverter from battery management has been applied in PV systems to mitigate the influence. The so-called parallel connected partial power converters (P-PPC) can equalize the PV panel voltages to combat mismatch losses with reduced hardware cost [10].

Different from typical module level front end converters such as micro-inverters and DC optimizers, partial power processing converters implement module level MPPT by treating the PV string as a whole system. To show the difference of the main power path and partial power path, the typical partial power processing configuration is redrawn in Fig. 3-13. The differential current balancers will not split the main power path of the entire PV string [33]. Most of the PV generated power flows through the main power path and only a small fraction of power flows through the auxiliary processors associated with mismatched modules. Thus, the power ratings of the module level converters can be decreased which reduces equipment cost.

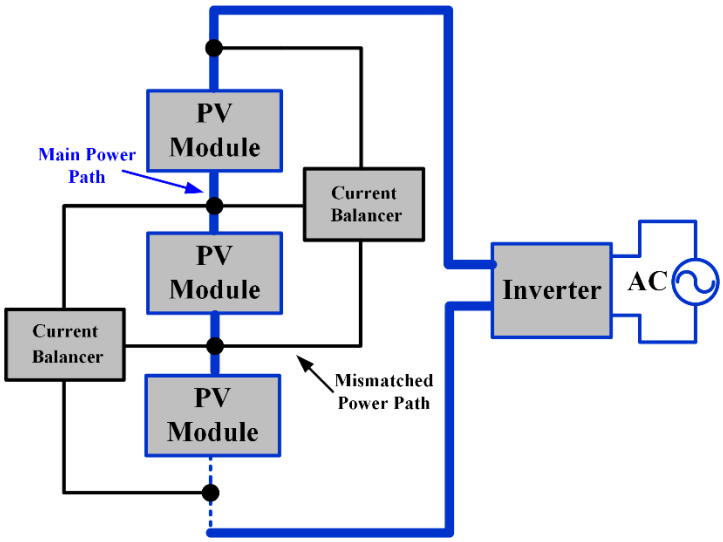


Fig. 3-13 A typical partial power processing architecture diagram based on current balancer.

In Fig. 3-13, a bidirectional dc/dc converter interlinks two adjacent PV modules to balance possible current mismatch. This kind of dc/dc converter is in a converter group termed current balancing differential converters, for discussion in this thesis. The compensating mechanism of the mismatch current is depicted in Fig. 3-14. Suppose PV Module 2 is shaded and its MPP current is less than the string MPP current. Then the associated dc/dc current balancing converter will supply the current difference between PV Module 1 and PV Module 2. The requirements for the current balancer is the ability to provide bidirectional current output. The inverting buck-boost and Cuk converters are candidates and connection examples are shown in Fig. 3-15.

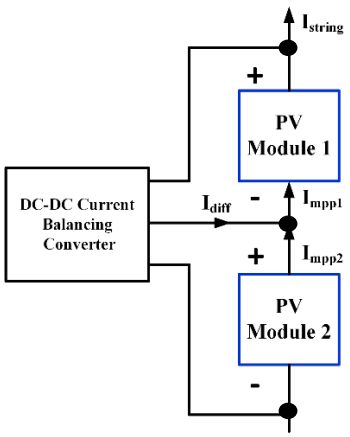


Fig. 3-14 Mismatch current compensated by the current balancing converter.

The circuit schematics of current balancer based partial power processing configurations are shown in Fig. 3-15. The buck-boost converter is implemented with fewer passive components counts. Practically each PV module needs a capacitor parallel connected to minimise any current ripple issue. The main advantage of the Cuk converter is its continuous input and output currents. However, one extra energy transferring capacitor and inductor are needed which increases equipment cost and circuit complexity. For the connection type in Fig. 3-15 (b), it beneficially decreases the MPP current ripple. Hence, large electrolytic capacitance may be avoided, with a small film capacitance, which increases PV system lifetime, reduces cost, and improves control response time.

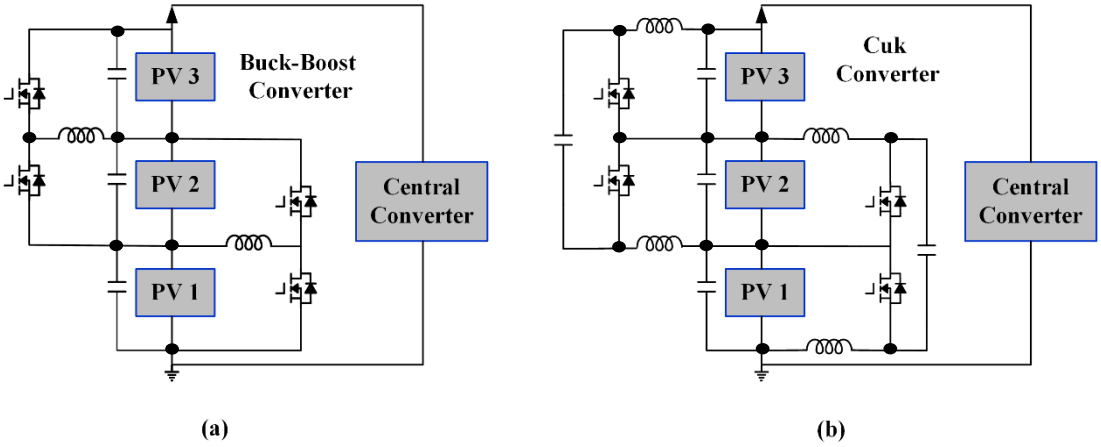


Fig. 3-15 Current balancing converters realised by
(a) inverting bidirectional buck-boost and (b) Cuk converters.

The number of converters equals the number of PV modules to guarantee the following linear equations have a unique solution for distributed MPPT realization.

$$I_{L,i} = I_{pv,i+1} - I_{pv,i} + D_{i-1}I_{L,i-1} + (1 - D_{i+1})I_{L,i+1} \tag{9}$$

$$D_i = \frac{V_{pv,i}}{V_{pv,i+1} + V_{pv,i}} \tag{10}$$

$$I_{main} = I_{pv,n} - D_{n-1}I_{L,n-1} = I_{pv,1} - (1 - D_1)I_{L,1} \tag{11}$$

The duty cycle ratio can be calculated from its associated PV module output voltage. There are only *n*-1 partial power dc/dc converters but *n* modules. A full power

processing central converter is necessary to complete the required DMPPT. Energy equilibrium needs to be achieved between the converters which necessitates careful control strategy designed.

Another approach to realize current balancing in a PV string is to balance the mismatched PV module current with the string current directly. As shown in Fig. 3-16, isolated flyback converters and grounded buck-boost converters are inserted between single PV module and the main DC bus. This type of configuration complicates the control design and MPPT implementation [33].

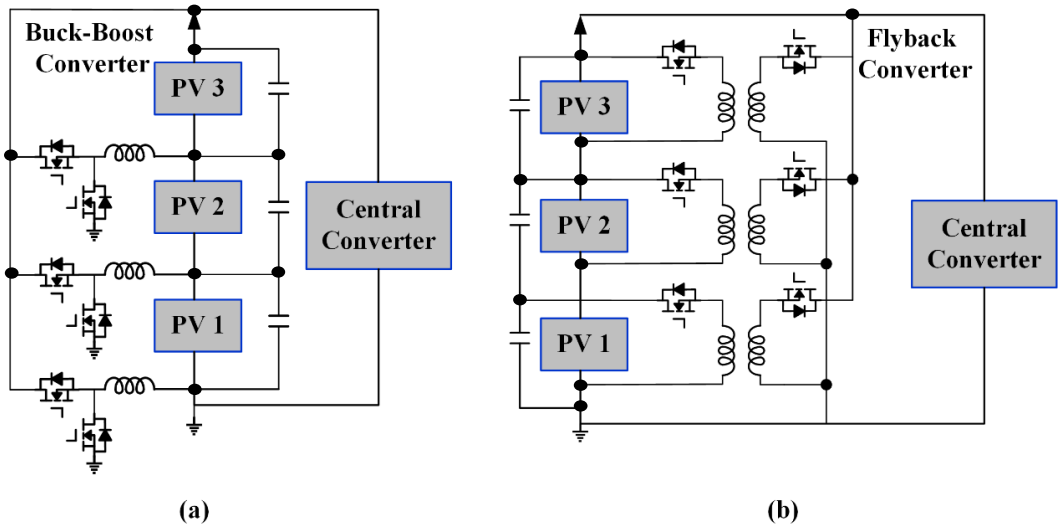


Fig. 3-16 Current balancing achieved between converter and DC bus. (a) Buck-boost DC-DC converters and (b) flyback isolated converters.

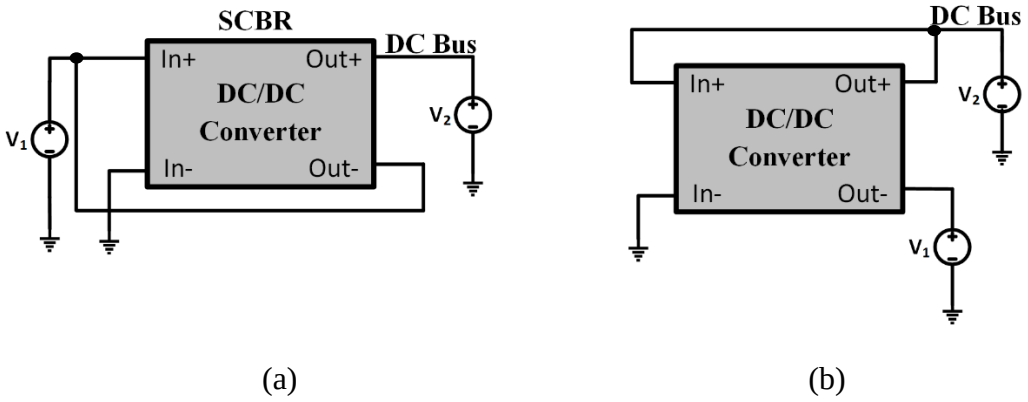
The main limitation of the current balancer based DMPPT architecture is that a full power processing central converter is always necessary for connection in high power applications or grid integration. Usually, PV strings have to be parallel connected to increase current output capability. To compensate the voltage differences between several PV strings, voltage balancing differential converters are proposed which are discussed in the following section.

3.4.2 Voltage Balancing Differential Converters

The partial power processing converter concept can be applied to voltage compensation to realize high efficiency dc-dc energy conversion [35][36]. The concept is realized by connecting a low power dc/dc converter in series with DC bus to increase or decrease the corresponding bus voltage. As shown in Fig. 3-17, the dc bus voltage

V_2 is the sum of converter output and voltage source V_1. This series connected boost regulator (SCBR) shown in Fig. 3-17(a) is proposed in [37] to meet the demands for application in small scale and inexpensive spacecraft. In this topology, the dc bus voltage V_2 must always higher than the input voltage V_1, so the compensating converter can be a basic buck-boost converter.

A similar dc bus regulator for spacecraft application is introduced in [38] and is called a series connected buck boost regulator (SCBBR). By implementing the operation principle of an autotransformer, the SCBBR combines the buck and boost mode in a series connected partial power converter. The associated dc bus voltage V_2 can be higher or lower than the input voltage V_1.



(a) (b)

Fig. 3-17 Partial power processing topologies with voltage compensation function. (a) Series connected boost regulator (SCBR); (b) partial power converter supplied by DC bus voltage.

The series connected DC-DC converter can be sourced by the DC bus, as shown in Fig. 3-17 (b). For applications in module level DMPPT PV systems, the voltage source V_1 can be the PV module MPP voltage and the V_2 is the PV string voltage. The architectures applying the series connected partial power converters (S-PPC) for PV module level MPPT are shown in Fig. 3-18. The terminology S-PPC is proposed in [7] and this converter type is defined as voltage balancers to emphasize their series voltage compensating functions in this thesis. The converter voltage output can add (with a non-inverting converter) or subtract (inverting converter) from PV module output voltage. Thus a voltage balancer with bipolar output is desirable to maintain a fixed DC bus while implementing DMPPT. This will facilitate the connection of several PV strings in parallel to one central inverter. Another advantage of bipolar series

converters is the flexibility of a variable number of PV modules and simple control strategy realization.

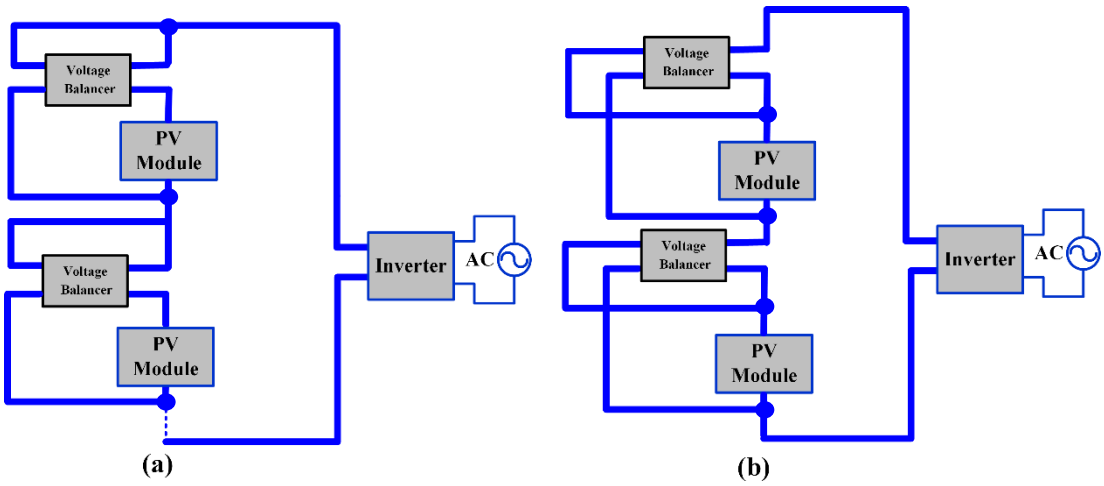


Fig. 3-18 PV Module integrated with series connected partial power converters. (a) voltage balancer based on S-PPC sourced by DC bus and (b) voltage balancer based on S-PPC sourced by single PV module.

Compared with full power processing DC-DC converters, the voltage balancers have the following advantages [39]:

- High efficiency - up to 98%;
- High power density;
- Low power rating; and
- Fault tolerant to converter failure.

These merits are inherited from the partial power processing feature and the special connection. To take advantage of these features, the voltage balancers should not use galvanic isolation which increases converter weight and power loss. However, to implement the architectures in Fig. 3-18, isolation is a requirement to avoid potential short circuit or loss of the ability to handle partial power processing [35].

S-PPCs need a wide voltage ratio range in order to deal with the most challenging shading scenarios. Generally, a complex topology with step-up and step-down ability is used for S-PPC converter implementation. However, the conversion efficiency is mainly dependent on the required voltage ratio which is a disadvantage for this type of architecture. The concept of component load factor (CLF) is used to compare the effective efficiency of different topologies. Converters with a low power

rating yield low CLF values and may result in cost effective module level MPPT [34][38].

The current and voltage balancing concept both exploit the fact that MPP voltage varies little with changing sun irradiance but changes with temperature variation.

Unlike full power processing distributed module converters, the control feedback design and MPPT algorithm for partial power converters are more complex. It is not possible to decouple the controller for each converter and independent module level MPPT for partial power converters is not possible. MPPT tracking for each sub-section needs to interact with others. In such partial power processing architectures, the main power path is the PV string and the control and MPPT strategy arranges the current shuffling between mismatched modules and the normal PV modules or PV string. The right number of MPPT units in suitable locations within a global architecture can guarantee extraction of the entire potential power, plus offers system stability.

It can be concluded that a partial power processing DMPPT architecture based only on the S-PPC or the P-PPC is not suitable for efficient module level MPPT implementation. To parallel connect PV strings with partial power converters, a fixed dc bus voltage should be provided. It is necessary to combine the voltage and current balancing ability in one PV system.

3.5 Summary

PV sources are intermittent, non-linear and produce power that varies with environmental conditions. The mismatching mechanism discussed in this chapter gives insight to why GMPPT tracking is important to increase PV system conversion efficiency. While the traditional DMPPT architecture is widely recognized as a promising solution, expensive hardware cost is the main obstacle for its application in the real world. The partial power converter was introduced to replace the traditional full power modular converter. The various partial power processing DMPPT architectures can be grouped into two viz., current and voltage balancing structures. However, an isolated full power processing central converter is a must for each PV string for global MPPT implementation and every PV string's output voltage is restricted to the addition of the PV modules' voltage at the maximum power point.

Thus, it is necessary to create a novel architecture with both voltage and current balancing ability to solve these problems.

In next chapter, a new partial power processing architecture is presented to combine the benefits of voltage and current compensation ability in one PV system. MPPT implementation will also be included within the analysis.

References

[1] V. Benda, "Photovoltaics towards terawatts -2013; progress in photovoltaic cells and modules," *IET Power Electron.*, vol. 8, no. 12, pp. 2343–2351, 2015.

[2] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "Power inverter topologies for photovoltaic modules-a review," in *Conference Record of the 2002 IEEE Industry Applications Conference. 37th IAS Annual Meeting (Cat. No.02CH37344)*, vol. 2, pp. 782–788 vol.2.

[3] J. M. Carrasco *et al.*, "Power-Electronic Systems for the Grid Integration of Renewable Energy Sources: A Survey," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1002–1016, 2006.

[4] G. G. M. L. S. S. Yaosuo Xue Kurthakoti C. Divya and M. Manjrekar, "Towards Next Generation PV Inverters," 2011.

[5] D. Shmilovitz and Y. Levron, "Distributed Maximum Power Point Tracking in Photovoltaic Systems - Emerging Architectures and Control Methods," *Autom. – J. Control. Meas. Electron. Comput. Commun.*, vol. 53, no. 2, 2012.

[6] G. R. Walker and P. C. Sernia, "Cascaded DC-DC converter connection of photovoltaic modules," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 1130–1139, 2004.

[7] M. Kasper, D. Bortis, and J. W. Kolar, "Classification and Comparative Evaluation of PV Panel-Integrated DC–DC Converter Concepts," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2511–2526, 2014.

[8] T. Kerekes, E. Koutroulis, D. Séra, R. Teodorescu, and M. Katsanevakis, "An Optimization Method for Designing Large PV Plants," *IEEE J. Photovoltaics*, vol. 3, no. 2, pp. 814–822, 2013.

[9] J. Biswas, A. M. Kamath, A. K. Gopi, and M. Barai, "Design, Architecture, and Real-Time Distributed Coordination DMPPT Algorithm for PV Systems," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 6, no. 3, pp. 1418–1433, 2018.

[10] G. R. Walker and P. C. Sernia, “PhotoVoltaic DC-DC Module Integrated Converter for Novel Cascaded and Bypass Grid Connection Topologies — Design and Optimisation,” in *Power Electronics Specialists Conference, 2006. PESC ’06. 37th IEEE*, pp. 1–7.

[11] S. R. Wenham, M. A. Green, R. Corkish, and M. E. Watt, *Applied Photovoltaics*. Earthscan, 2007.

[12] M. A. Green, “Accuracy of analytical expressions for solar cell fill factors,” vol. 7, pp. 337–340, 1982.

[13] K. A. Kim and P. T. Krein, “Photovoltaic hot spot analysis for cells with various reverse-bias characteristics through electrical and thermal simulation,” in *2013 IEEE 14th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2013, pp. 1–8.

[14] W. Herrmann, W. Wiesner, and W. Vaassen, “Hot spot investigations on PV modules-new concepts for a test standard and consequences for module design with respect to bypass diodes,” in *Conference Record of the Twenty Sixth IEEE Photovoltaic Specialists Conference - 1997*, 1997, pp. 1129–1132.

[15] M. Dhimish, V. Holmes, B. Mehrdadi, M. Dales, and P. Mather, “Output-Power Enhancement for Hot Spotted Polycrystalline Photovoltaic Solar Cells,” *IEEE Trans. Device Mater. Reliab.*, vol. 18, no. 1, pp. 37–45, 2018.

[16] P. Walker, Geoffrey R., Xue, John, & Sernia, “PV string per-module maximum power point enabling converters.,” in *In Duke, R. (Ed.) Australasian Universities Power Engineering Conference, AUPEC’03, University of Canterbury, Christchurch, New Zealand*, 2003.

[17] J. S. Goud, R. Kalpana, and B. Singh, “A Hybrid Global Maximum Power Point Tracking Technique With Fast Convergence Speed for Partial-Shaded PV Systems,” *IEEE Trans. Ind. Appl.*, vol. 54, no. 5, pp. 5367–5376, 2018.

[18] M. A. S. Masoum, H. Dehbonei, and E. F. Fuchs, “Theoretical and experimental analyses of photovoltaic systems with voltageand current-based maximum power-point tracking,” *IEEE Trans. Energy Convers.*, vol. 17, no. 4, pp. 514–522, 2002.

[19] A. M. S. Furtado, F. Bradaschia, M. C. Cavalcanti, and L. R. Limongi, “A Reduced Voltage Range Global Maximum Power Point Tracking Algorithm for Photovoltaic Systems Under Partial Shading Conditions,” *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 3252–3262, 2018.

[20] G. Velasco-Quesada, F. Guinjoan-Gispert, R. Pique-Lopez, M. Roman-Lumbreras, and A. Conesa-Roca, “Electrical PV Array Reconfiguration Strategy for Energy Extraction Improvement in Grid-Connected PV Systems,” *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4319–4331, 2009.

[21] J. D. Bastidas-Rodriguez, E. Franco, G. Petrone, C. A. Ramos-Paja, and G. Spagnuolo, “Maximum power point tracking architectures for photovoltaic systems in mismatching conditions: a review,” *IET Power Electron.*, vol. 7, no. 6, pp. 1396–1413, 2014.

[22] E. Bianconi *et al.*, “A Fast Current-Based MPPT Technique Employing Sliding Mode Control,” *IEEE Trans. Ind. Electron.*, vol. 60, no. 3, pp. 1168–1178, 2013.

[23] Y. Levron and D. Shmilovitz, “Maximum Power Point Tracking Employing Sliding Mode Control,” *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 60, no. 3, pp. 724–732, 2013.

[24] A. Ramyar, H. Iman-Eini, and S. Farhangi, “Global Maximum Power Point Tracking Method for Photovoltaic Arrays Under Partial Shading Conditions,” *IEEE Trans. Ind. Electron.*, vol. 64, no. 4, pp. 2855–2864, 2017.

[25] F. Wang, T. Zhu, F. Zhuo, H. Yi, S. Shi, and X. Zhang, “Analysis and Optimization of Flexible MCPT Strategy in Submodule PV Application,” *IEEE Trans. Sustain. Energy*, vol. 8, no. 1, pp. 249–257, 2017.

[26] M. Adly and K. Strunz, “Irradiance-Adaptive PV Module Integrated Converter for High Efficiency and Power Quality in Standalone and DC Microgrid Applications,” *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 436–446, 2018.

[27] F. Wang, T. Zhu, F. Zhuo, and H. Yi, “An Improved Submodule Differential Power Processing-Based PV System With Flexible Multi-MPPT Control,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 6, no. 1, pp. 94–102, 2018.

[28] A. A. Elserougi, M. S. Diab, A. M. Massoud, A. S. Abdel-Khalik, and S. Ahmed, “A Switched PV Approach for Extracted Maximum Power Enhancement of PV Arrays During Partial Shading,” *IEEE Trans. Sustain. Energy*, vol. 6, no. 3, pp. 767–772, 2015.

[29] Y. Mahmoud and E. F. El-Saadany, “Enhanced Reconfiguration Method for Reducing Mismatch Losses in PV Systems,” *IEEE J. Photovoltaics*, vol. 7, no. 6, pp. 1746–1754, 2017.

[30] B. Burger, B. Goeldi, S. Rogalla, and H. Schmidt, *Module integrated electronics - an overview*. 2010.

[31] B. Min, J. Lee, J. Kim, T. Kim, D. Yoo, and E. Song, “A New Topology With High Efficiency Throughout All Load Range for Photovoltaic PCS,” *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4427–4435, 2009.

[32] S. Abdourraziq, M. A. Abdourraziq, and C. Darab, “Maximum power point tracking applied to PV systems under partial shading conditions,” in *2017 International Conference on Electromechanical and Power Systems (SIELMEN)*, 2017, pp. 286–290.

[33] P. S. Shenoy, K. A. Kim, B. B. Johnson, and P. T. Krein, “Differential Power Processing for Increased Energy Production and Reliability of Photovoltaic Systems,” *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2968–2979, 2013.

[34] J. R. R. Zientarski, M. L. da S. Martins, J. R. Pinheiro, and H. L. Hey, “Evaluation of Power Processing in Series-Connected Partial-Power Converters,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 7, no. 1, pp. 343–352, 2019.

[35] J. Zhao, K. Yeates, and Y. Han, “Analysis of high efficiency DC/DC converter processing partial input/output power,” *2013 IEEE 14th Work. Control Model. Power Electron. COMPEL 2013*, pp. 1–8, 2013.

[36] H. Zhou, J. Zhao, and Y. Han, “PV Balancers: Concept, Architectures, and Realization,” *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3479–3487, 2015.

[37] R. M. Button, “A modular PMAD system for small spacecraft,” *AIP Conf. Proc.*, vol. 387, no. 1, pp. 263–268, Jan. 1997.

[38] A. G. Birchenough, “A High Efficiency DC Bus Regulator / RPC for Spacecraft Applications,” *AIP Conf. Proc.*, vol. 699, no. 1, pp. 606–613, Feb. 2004.

[39] M. S. Agamy *et al.*, “An Efficient Partial Power Processing DC/DC Converter for Distributed PV Architectures,” *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 674–686, 2014.

CHAPTER 4

Proposed Parallel Connected DMPPT Architecture with Partial Power Processing Converters

This chapter proposes a novel PV energy conversion architecture that achieves distributed maximum power point tracking (DMPPT) with partial power processing converters. Featuring both voltage and current compensation abilities, the per module per MPPT structure is obtained and a dc power interface is created with a controlled voltage level due to a series-connected voltage balancer. The proposed architecture allows flexible ‘plug-and-play’ performance for each string to connect to a down streaming inverter stage or a dc power network. A cost and size reduction can be expected by using lower electrical rating and smaller size module integrated converters (MICs). The operating mechanism, modelling, and control strategy of the proposed system are analysed; and simulation results are presented to establish its effectiveness.

4.1 Background

Partial power processing converters for efficient DMPPT to improve PV system efficiency, have been widely discussed in academia and industry [1]–[4]. Maximum power point mismatch between PV modules in a PV string can be caused by partial shading, manufacturing tolerances, temperature variation, etc. The string current will be restricted to the current of the PV module with the least current, without compensation. In some extreme conditions, hot spots and permanent damage are induced upon the whole PV system.

One partial power processing DMPPT architecture is designed to balance MPP current mismatch between modules with dc-dc converters in a string. A typical architecture with current balancing ability has been reviewed in Chapter 3. The different MPP currents between neighbouring PV elements are balanced by small non-isolated inverting bidirectional dc-dc converters. This is called a shuffling architecture for its current shuffling ability between adjacent modules. The ground of the shuffling converter is common to its associated PV modules, so isolation is only needed for the dc link central converter [5]. To facilitate fully distributed MPPT, the MPPT units equal the number of photovoltaic modules. Thus, the central converter is prerequisite to fulfil the power shuffling loop and ensure a stable and accurate MPPT algorithm.

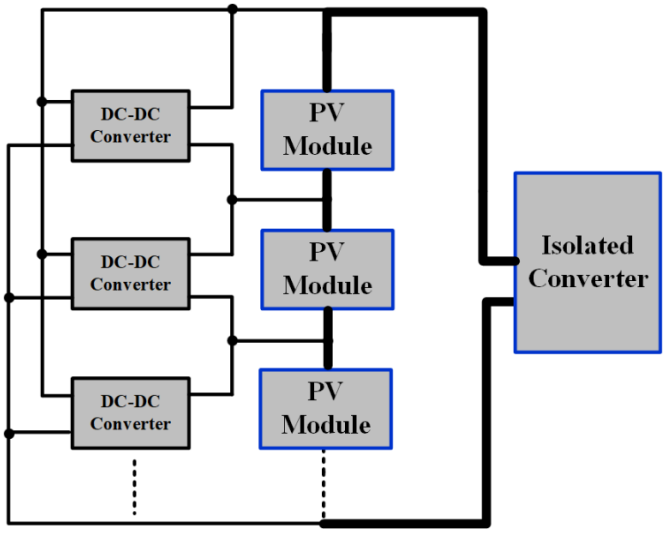


Fig. 4-1 RECC architecture

The returned energy current converter (RECC) based architecture in Fig. 4-1 features a shunt converter per module arrangement, while the output of all the

converters are connected in parallel across the PV string [6]. String current equalization is accomplished by compensating the current difference between the mismatched modules and the overall string with shunt dc-dc converters. In contrast to the shuffling architecture, the central converter is eliminated by the global MPPT algorithm.

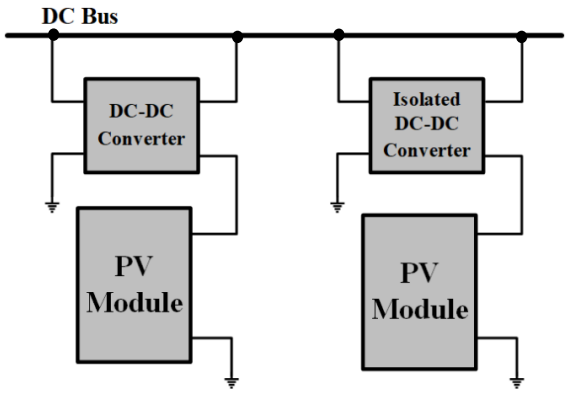


Fig. 4-2 PV balancer architecture

Neither of the previous two architectures have voltage compensation ability. One PV string's voltage is predetermined by the sum of its related modules' MPP voltages. An architecture based on a voltage balancing mechanism is shown in Fig. 4-2, in which one module is series connected with one converter, called PV balancer, to compensate the voltage difference between modules and the dc bus [7].

Compared with the larger current variation, MPP voltage varies less with changes in sun irradiance and ambient temperature. Thus, the power rating of the PV balancer can be reduced accordingly. However, in contrast with the mentioned current balancing architectures, the inherent connection of PV modules of each string must be reduced. Hence, it induces a grounding issue that only one module of the string can be grounded which can cause a potential safety hazard for maintenance electricians and consumers.

The proposed DMPPT architecture in this chapter balances both MPP currents and the voltages of PV modules connected in one PV string.

4.2 Implementation of the Proposed Architecture

4.2.1 Conceptual Illustration of the proposed architecture

The block diagram of the proposed architecture is shown in Fig. 4-3. This new architecture inherits the merits of conventional partial power processing DMPPT structures while avoiding their demerits. In Fig. 4-3, different to the PV balancer based configuration [7], a bipolar output, bidirectional, dc-dc converter called a voltage balancer, is series connected with a PV string, not a PV module, to compensate the voltage difference between the string and the associated dc bus. The input to output of the voltage balancer should be isolated which can be accomplished with isolated converter topologies. The other option is to use non-isolated converters sourced by an isolated external dc-dc converter. In the illustrated diagram, all the voltage balancers are sourced by an external isolated dc source v_{in}. Hence, several PV strings can be parallel connected to a dc interface for further power conversion. For dc to ac transformation, the inverter per string structure can be eliminated. A central inverter can be dc bus sourced, decreasing inverter cost and improving conversion efficiency.

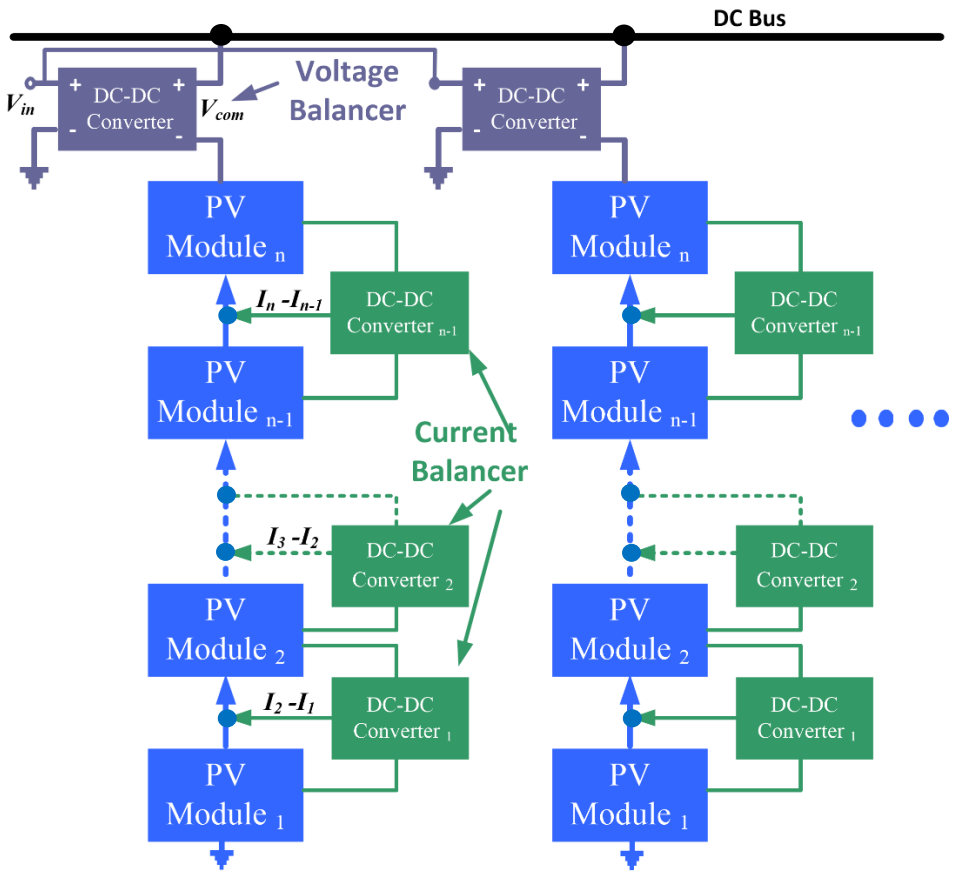


Fig. 4-3 Proposed current and voltage balancing architecture.

Within each PV string, the internal current balancing between adjacent PV modules is realized with dc-dc converters, current balancers, which have the same connection arrangement as the shuffling or RECC architecture [1]. For maximum energy capture efficiency, the dc interface voltage is set to be approximately the sum of modules MPP voltage under normal operation conditions. The DC voltage over each PV string can be variable over a small range to adjust for the ambient temperature and sun light change. Thus, the selected voltage balancer should have bipolar voltage output to compensate a possible positive or negative voltage bias. To simplify the design, the dc bus voltage can also be always greater than the sum of the MPP voltages. Then the voltage balancers are simpler bidirectional unipolar converters.

With no mismatch, the full PV power flows through the PV modules without any processing by the parallel connected current balancers. Ideally, the voltage deviation between the dc interface and the PV string is small enough to be neglected for which the voltage balancer will operate at a zero-voltage output. Thus, all the auxiliary dc-dc converters in the new architecture function as partial power processers to compensate mismatch between modules and the dc interface. Theoretically the auxiliary processors in this architecture achieve zero power loss under normal conditions.

Compared with DMPPT architectures based on full power processing converters, the main power flow path is not seriously affected by the auxiliary converters. For each PV string, the number of PV modules is equal to the number of related dc-dc converters (voltage and current balancers) as shown in Fig. 4-3. So, all the MPPT units are low power rated dc-dc converters.

To exploit all DMPPT system control degrees of freedom, an additional bipolar voltage converter with bidirectional power flow capability is employed as a voltage balancer to replace the traditional global MPPT central converter. Then the string is suitable for multiple PV strings parallel connection to a common dc bus. Current balancing dc-dc converters are necessary to eliminate the current mismatch of adjacent PV modules within one string. The detailed requirements for such voltage and current balancing converters will be investigated in the following sections. Several dc-dc

converter candidates will be analysed and compared to provide instruction for further design.

For a PV string with *n* PV panels, theoretically, the most available power for the whole string is equal to the sum of the maximum power of all the panels. To realize this, a PV panel integrated converter is necessary to implement independent operation during mismatching conditions. For each PV application, the reduced PV generated power due to the various converter operating efficiencies needs to be considered. Along with the equipment cost, size and lifetime, converter efficiency is an important factor for converter topology selection. The efficiency/power density (η/ρ) Pareto optimization concept can be applied to compare different PV panel integrated dc-dc converters [3].

Similar to full power processing converters, partial power processing converters can be classified into two connecting types. In this chapter, the features and requirements for series connected voltage balancing converters and parallel connected current balancing converters are discussed. Promising converter topologies will be reviewed based on the proposed architecture.

As discussed in Chapter 3, the system efficiency of the DMPPT architecture based on partial power processing converters is determined by the ratio of the converter processed power and the full PV power [8]. System efficiency η_{total} is given by equation (1), where P_c is the power flowing through the converter and P_{PV} is the full PV generated power. The partial power converter handles only a fraction of the power, during mismatching. To pursue high system efficiency, applied partial power converters can be selected to have high conversion efficiency in part load situations.

$$\eta_{total} = 1 - \frac{P_c}{P_{PV}}(1 - \eta_{conv}) \tag{1}$$

4.2.2 Circuit Realization for Voltage Balancers

The voltage balancing converters must be able to compensate the voltage difference between the dc bus and the series connected PV string. For the proposed architecture, the interleaved current balancers adjust the output voltage of each PV module to deal with the mismatch. Ideally, the PV string voltage is the sum of the MPP

voltages of all the series connected PV modules. The dc bus voltage is a fixed value and several PV strings are parallel connected to the dc bus.

Theoretically, the PV string voltage can be higher or lower than the DC bus voltage. But in most mismatching conditions, such as shading or temperature influences, the voltages of the mismatched PV modules will be lower than the normal PV modules. Thus, the number of PV modules in one PV string can be selected to make the DC bus voltage always a bit higher than the PV string voltage. In this kind of configuration, the voltage balancing converter can be a basic unipolar output voltage topology such as a buck-type topology to compensate the voltage difference.

Converter topologies with bipolar output voltages can also be selected to provide a more universal solution. Thus, the number of PV modules within one PV string can be selected with more flexibility. The dc bus voltage can be approximately equal to the PV string voltage level. When no mismatch occurs, the output of voltage balancer can be near zero and the power processed approaching zero. Based on the previous analysis, the system efficiency can be increased.

The voltage balancer fits into the catalogue of series connected partial power converters (S-PPC). Different from conventional S-PPC, it does not need to be sourced by its compensated PV string or PV module. It can be sourced by the dc bus or an external voltage input source to simplify control and to provide converter design flexibility [9]. The input and output of the voltage balancer can be decoupled which is an advantage compared with most existing S-PPC.

Parallel connected voltage balancing converters need to be isolated from the dc bus and each other. If a non-isolated topology is selected as the voltage balancer, an external power supply such as multi-channel isolated power supply can be used to source the various converters. Otherwise, an isolated topology is a must. To parallel connect several PV strings to one dc bus, the series connected voltage balancers must be ‘flipped’, if connected to the positive dc bus. (‘Flipped’ – as in Fig. 4-5, rather than the converter input and output being reference to a common 0V rail, the reference is the converter positive input rail.)

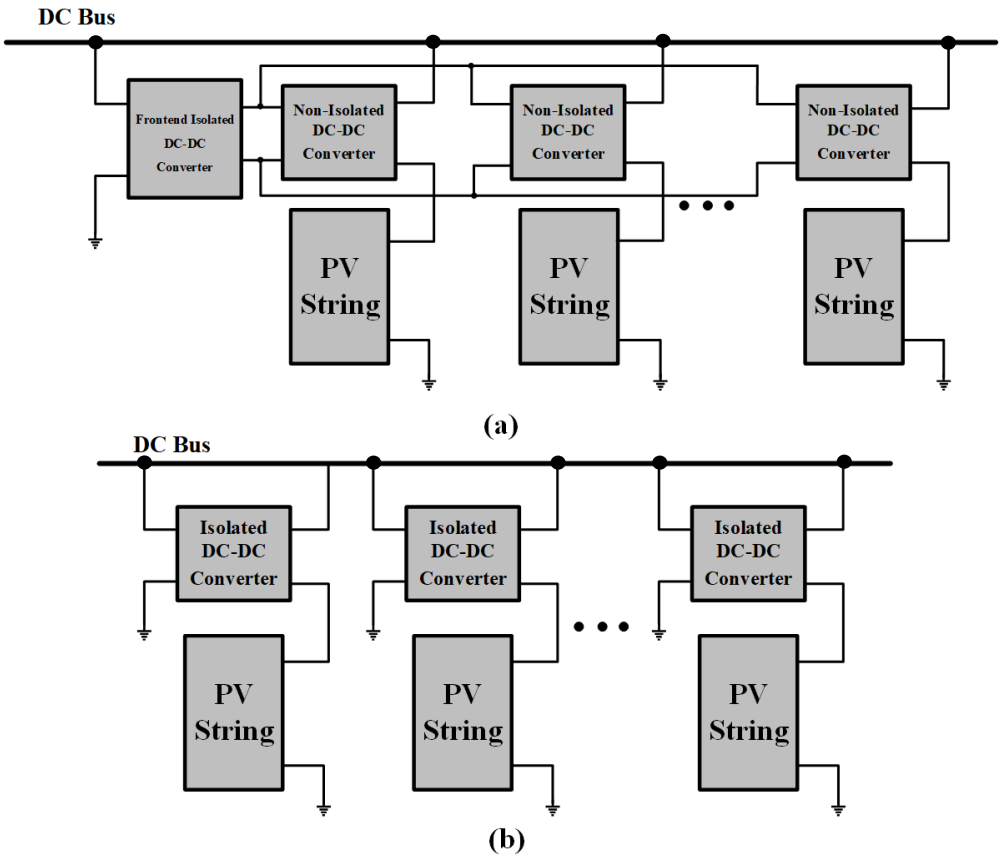


Fig. 4-4 Two main connecting types for voltage balancer.

(a) Type-I: Flipped non-isolated dc-dc converter sourced by external front-end isolated multi-channel dc power source and (b) Type-II: Isolated dc-dc converters sourced by dc bus.

Two main voltage balancing converter types are shown in Fig. 4-4. For a type I architecture, non-isolated dc-dc converters are sourced by a front-end multi-channel dc-dc converter which is an isolated step-down converter topology. The non-isolated converters should be flipped connected for parallel connection. The type II connection type uses isolated step-down dc-dc converters all sourced by the common dc bus. If the dc bus voltage is designed higher than the PV string voltage, the voltage balancers need unipolar output voltage ability. If the dc bus voltage is designed close to the PV string voltage, the voltage balancer should have bipolar output voltage ability.

In conclusion, the requirements for a voltage balancing converter are:

1) Minimum processed power in most mismatch conditions.
2) Compact design and reduced cost for implementation.
3) Adequate voltage compensating ability for PV string and DC bus.
4) Bipolar output voltage capability if the dc bus and PV string voltages are similar.

5) Electrical isolation from the dc bus.
6) Flipped connection if external power source is used.

Depending on system requirements, the series-connected dc-dc voltage compensator must offer either a unipolar or bipolar voltage range such that its processing power is either unidirectional or bidirectional.

I. Unipolar output voltage converter topologies

A unipolar output voltage dc-dc converter suitable for Type I connection can be a flipped buck converter as in Fig. 4-5 (a) [7]. To secure galvanic isolation as for Type II, the flyback converter topology is shown in Fig. 4-5 (b). These converters always inject power down-streaming if they are not bypassed [2], [7].

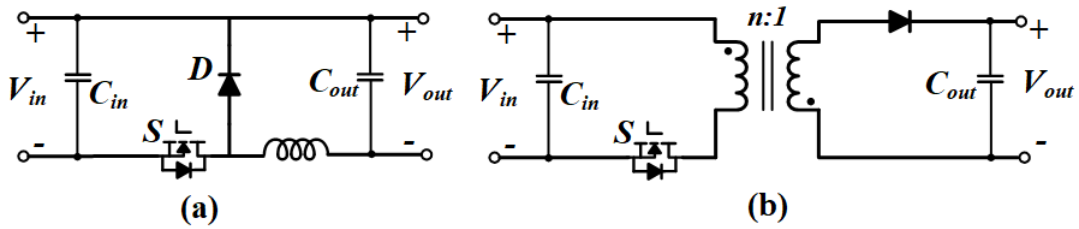


Fig. 4-5 Two topology representatives with unipolar output voltage capability. (a) Flipped buck converter for type I architecture and (b) Isolated Flyback converter for type II architecture.

II. Bipolar output voltage converter topologies

If the series dc-dc compensator needs to contribute power to and absorb power from the PV generation, it must provide bipolar voltage output, as the PV string current direction is fixed. For the Type I configuration in Fig. 4-4 (a), the four-quadrant dc chopper as in Fig. 4-6 (a) is a solution. An alternative is to use a flipped version of the semi-quasi-Z source converter introduced in Chapter 2, see Fig. 4-6 (c) [10], [11]. To add galvanic isolation when meeting Type II converter requirements, the isolated full-bridge DC-DC converter topology shown in Fig. 4-6 (b) is applicable, where the full-bridge operates in an inversion mode, and a current source type rectification stage is used in the secondary that can reverse the voltage for power reversal (current direction is maintained) [9].

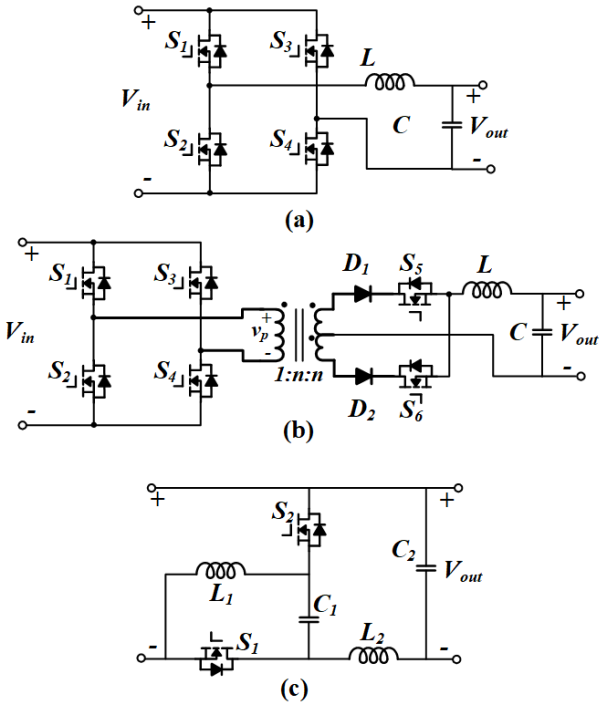


Fig. 4-6 Topology representatives with bipolar output voltage capability.
(a) Non-isolated four-quadrant DC chopper; (b) Isolated Full-bridge converter topology;
(c) Non-isolated semi-quasi-Z-Source converter topology.

4.2.3 Circuit Realization for Current Balancers

Inherited from the battery cell equalization concept, differential power processing (DPP) converters have been adopted as an option to implement DMPPT with reduced power loss [5][12]. In this thesis, the DPP is called a current balancer to distinguish it from a voltage balancing converter. Different from a conventional DPP based DMPPT architecture, the proposed architecture utilize a series connected partial power converter instead of a full power processing central converter to complete the MTTP algorithm [4].

DPP converters can be used at different stages, such as on the PV sub-string, PV panel and even PV cell level to implement different level MPPT. The power differences between their associated PV elements are processed by compensating the current difference between each. Various electrical connections between converters, different converter topologies and control strategies have been used.

I. PV-DC Bus connection type

In the typical PV to dc bus connection shown in Fig. 4-7, the input of each DPP converter is connected to one PV module and the output is connected between the DC bus and ground. The DPP converter can add or subtract current to maintain module level DMPPT during mismatched conditions.

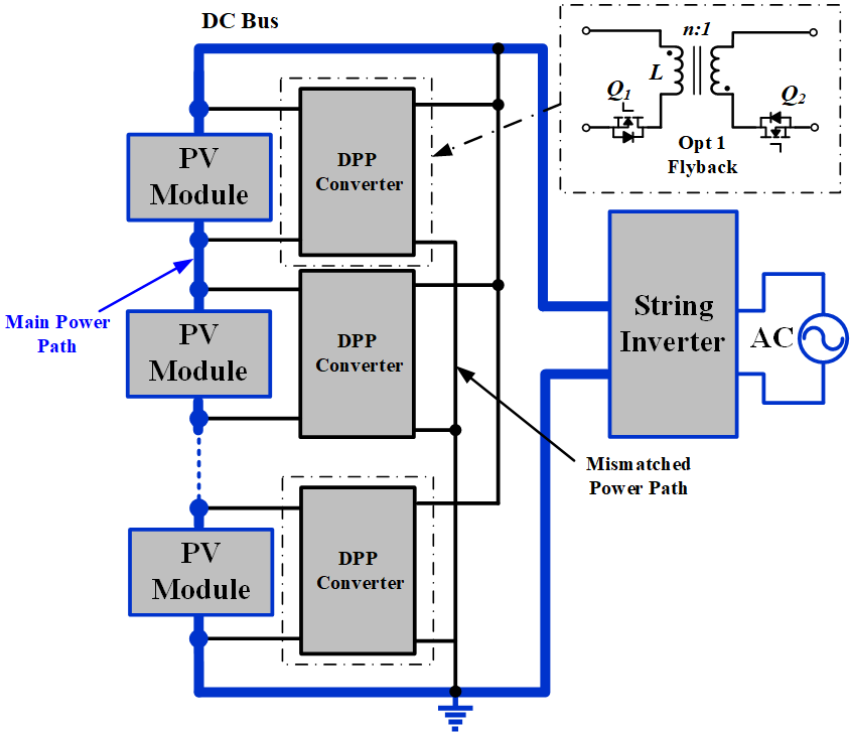


Fig. 4-7 DPP converter in PV-DC bus connection type.

The converter topology shown in Fig. 4-7 is an isolated flyback converter with bidirectional input/output current capability. The implementation proposed in [5] uses *n*-1 buck-boost converter topologies on a PV string of *n* modules. Each buck-boost converter caters for its associated PV element and all other PV elements, and its implementation requires a complicated control strategy. The recommended topology is isolated with no direct connecting between the negative input and output.

The main limitation of a bidirectional flyback based architecture is the converter output current coupling with the PV string current, which imposes control design complexity. To simplify the architecture, other unidirectional topologies, such as isolated LLC resonant converters and sepic converters, have been used. However, these converters cannot implement real module level MPPT. Compared with

bidirectional converters, more power is processed by a unidirectional converter which reduces system efficiency.

Another method uses a boost converter series connected with the PV string to decouple the string current from the converter output current [13]. The control design is simplified and less power is processed by this variation.

The main challenges for a PV-DC bus architecture are a high voltage gain ratio and difficulty in scaling up power ratings. String series connected dc-dc converters can simplify the control design but may introduce control redundancy.

II. PV-PV connection type

With PV-PV connection, each DPP converter connects two adjacent PV modules and the MPPT duty ratio is controlled by one PV module.

This kind of architecture is commonly used. As shown in Fig. 4-8, for a PV string with n PV modules, there are n-1 DPP converters. MPPT of the n^{th} PV module is performed by the string inverter [4].

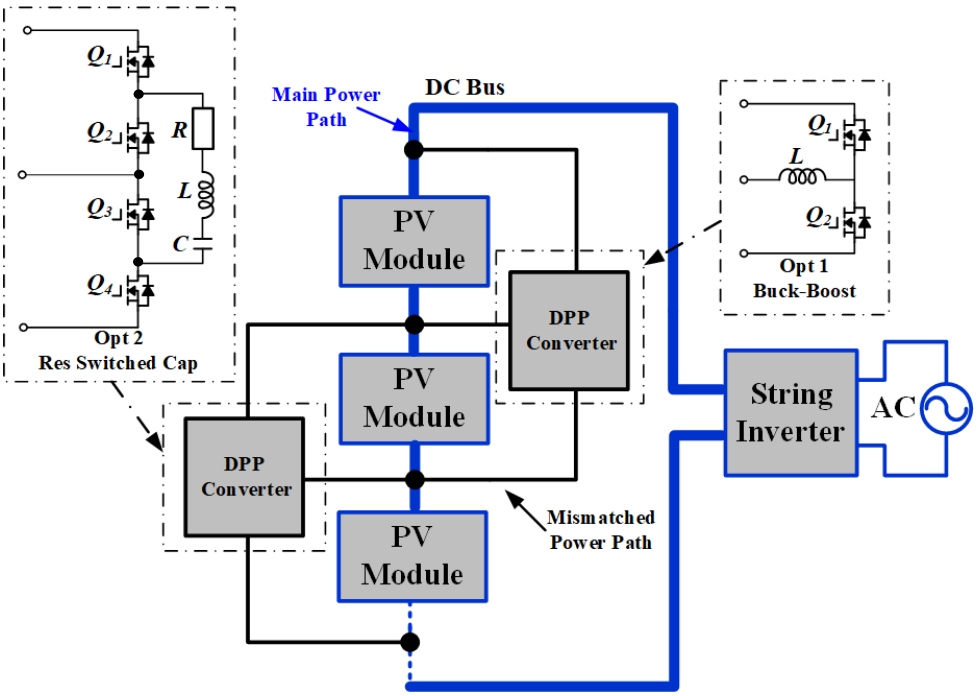


Fig. 4-8 DPP converter in PV-PV connection type.

The most widely deployed DPP converter for PV-PV connection is the bidirectional buck-boost topology, while an alternative is the resonant switched converter [5], [14], [15]. These two representative topologies are illustrated in Fig. 4-8. As for DPP converters for the PV-DC bus, suitable converters for a PV-PV architecture should have the ability to supply or remove current from their associated PV elements to compensate any mismatch. The control design should also consider converter coupling. The optimum PV string current is unique for a given condition, with proper controller design, and extracts the maximum available PV power.

Compared with the PV-DC bus converter, a non-isolated and more compact topology is used for the PV-PV converter. The voltage rating is at the PV module level, not the dc bus. It is assumed the cost can be reduced while the system efficiency can be increased.

Various MPPT algorithms and control strategies have been proposed and verified to increase control accuracy and assist scalability for large-scale power system. The voltage balancing or voltage reference based control algorithm is simple but can only achieve near MPPT. P&O or hill climbing algorithms can approach exact MPPT. Distributed MPPT is implemented at DPP converter level and string inverter level respectively and the control strategy needs coordinated speed and information sharing. Usually string inverter MPPT is slower than DPP MPPT.

In additional to PV-Bus and PV-PV connection types, another variation for PV-Bus connection is a PV-IP (Isolated Port) architecture, where an isolated bus is used to optimize the extracted PV power. The DPP converter for this architecture should also be isolated and bidirectional and the input and output power for the isolated bus must balance. These imposes controller design complexity and may not achieve exact DMPPT during all string current conditions.

Based on the previous discussion, the PV-PV architecture current balancer approach is a reasonable choice for the proposed architecture. The voltage balancer can replace the string inverter to achieve MPPT tracking for all PV modules. Then several PV strings can be parallel connected for large power output.

4.2.4 A Representative Circuit Schematic

An implementation of the proposed DMPPT architecture is illustrated in Fig. 4-9, and is used to illustrate the operating principle with two PV modules series connected to form a PV string. The dc bus voltage is set to the sum of the MPP voltages of the series PV modules at a 1 sun condition (AM1.5, 1000W/m^2 at 25 °C). A flipped semi-quasi-Z source converter (G4)[16] with bipolar voltage output ability is the series voltage balancer and a buck-boost converter is used as a shunt current balancer.

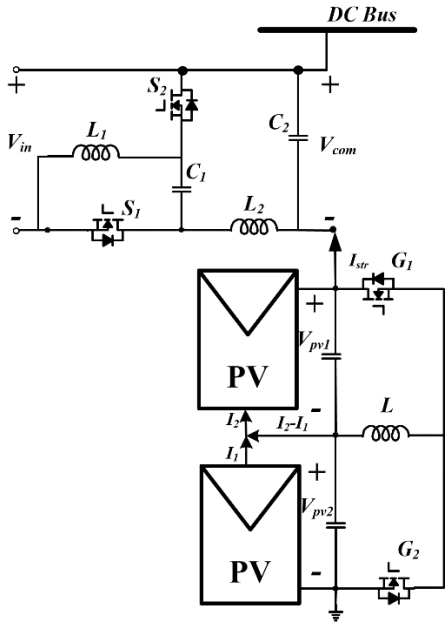


Fig. 4-9 Implemented topology scheme example.

To improve conversion efficiency, the voltage balancing converter can be sourced by an isolated step-down dc-dc converter fed from the dc bus. With distinct current variations under MPPT, the resultant voltage shift is marginal in response to changes in irradiance or temperature, which means the voltage balancer can effectively compensate PV string voltage deviations at a low power.

In Fig. 4-9, the average inductor current of the buck-boost converter can be considered a controllable current source that compensates MPP current difference of the neighbouring PV element. Generally, the duty ratio of a buck-boost current compensator can be expressed by its two adjacent PV voltages as in equation (2).

$$D_i = \frac{V_{PV,i}}{V_{PV,i} + V_{PV,i+1}} \tag{2}$$

where $V_{PV,i}$ represents the voltage across the i_{th} PV module (i is a positive integer). By controlling the duty ratio D_i, the i_{th} PV module can operate at its maximum power output point. In the shuffling D-MPPT architecture, the number of the current balancing converters is one less than the number of PV units. This is why a central converter must be included to act as a global MPPT unit and it must process all the PV power. In the new architecture, the voltage balancer acts as the last MPPT unit of the overall PV string. Hence, the number of MPPT units equals the number of PV modules so per module per MPPT can only be achieved with partial power dc-dc converters. The converters only process the mismatched power between PV modules, so power rating and equipment cost are reduced.

For PV string output voltage V_{string}, common dc bus voltage V_{dc}, and G4 converter input voltage V_{in}, the voltage compensator duty ratio is:

$$D_c = \frac{V_{in} - V_{string}}{2(V_{dc} - V_{string}) - V_{in}} \tag{3}$$

Various MPPT algorithms can be applied and the efficient perturb-and-observe (P&O) method is chosen. The control challenge is that all the modules of one string cannot be decoupled from one another, so the variation of one module's MPP will influence the whole string's operation. Applying Kirchhoff's Current Law, the current relationship is:

$$I_{PV,i} = I_{PV,i+1} - I_{L,i} + D_{i-1}I_{L,i-1} + (1 - D_{i+1})I_{L,i+1} \tag{4}$$

where the i_{th} PV module current is i_{PV}, i and I_L, i is the buck-boost converter inductor current. For control simplification, each i_{th} PV module is controlled by the i_{th} current balancer, and the n^{th} module is controlled by the n^{th} voltage balancer. The control objective is to make each PV module operate at its local MPP. PV module voltages and currents are measured periodically for the MPPT algorithm to generate a controller reference. Because the PV module *I-V* curve has a one-to-one mapping function, the reference can be the desired voltage or current.

In this application, distributed proportional integral (PI) controllers are used to vary the duty ratio of the switches. Since it is difficult to decouple the PV modules, the integral speed decreases from the 1st controller for the first buck-boost converter to the n^{th} controller designed for the G4 converter. When the i_{th} PV module is perturbed

and controlled to find its MPP, its neighbouring $(i+1)_{th}$ PV module is a stable dc input source. The control speed of the top flipped G4 converter is the slowest.

When tracking the *n*th PV module MPP, the remaining *n*-1 PV modules are regarded as operating at their individual MPPs, during which the G4 converter's output voltage is controlled to source the difference between the dc bus and the string. In this architecture, the per string per central converter structure has been replaced by the voltage balancer. Thus, one PV string can realize local control and distributed protection without the necessity of string communications.

4.3 EMT Modelling for a Large-Scale PV Power System

A large-scale PV power system based on the proposed DMPPT architecture is built by electromagnetic transient (EMT) modelling, for further analysis. Various modelling options for the proposed large scale DMPPT architecture are reviewed and compared. EMT model detail is described along with the applied MPPT algorithm and control strategy.

4.3.1 Comparison of the different modelling techniques

The most accurate modelling for power electronic converters is practical physical models with full details mimicking conduction and switching states. Large computation resource is necessary and long simulation time is expected. For some large-scale power systems, it is impractical to establish full scale physical switching models with detailed dynamics. Accurate modelling is used when transient response analysis is required [17].

Although transient response and dynamic details can be captured by detailed physical modelling, it is inefficient and time consuming for large scale PV system modelling if hundreds or even thousands of power devices are used.

High computing power, larger memory and long simulation time are main barriers for implementing detailed physical switching models in large power systems. To reduce simulation time, state space averaging modelling is widely used for pulse width modulated (PWM) switching converters for ac modelling and controller design which was first introduced as a unified modelling approach in [18]. By combining the averaging technique and small signal equivalence, numerical equations and low frequency linear circuit models can be obtained. The switching actions introduce both

zeros and poles to the final output transfer function for feedback control analysis. The detailed description of state space averaging can be found in [19] [20]. Small ripple perturbation is applied to get the final model which includes steady state DC models and dynamic AC small signal models.

In applications small ripple conditions cannot be satisfied; it is difficult to apply conventional averaging models. A more general averaging modelling approach is proposed in [21] to be applied in broader applications including resonant converters which may not satisfy small ripple restrictions.

The simplified average modelling methodology can usually simulate dynamic and static behaviour during normal operating conditions. However, it is difficult to analyse details during abnormal power faults for its independence at every level [22]. To trade-off between the required dynamics and efficient simulation time in large-scale power systems, electromagnetic transient (EMT) modelling is selected as a candidate in this thesis for large scale PV system for comprehensive simulation of normal and faulty operating conditions. The implementation of EMT modelling for the proposed PV system is discussed in the following section. The validity and scalability of the models are demonstrated.

4.3.2 An Efficient EMT model

Most EMT models are designed based on Dommel's algorithm [23]. By applying the trapezoidal integration method, each device element can be converted into a Norton current sourced or Thévenin voltage sourced equivalent circuit. The electrical characters for each node at the present time step is calculated with the previous time step value. The accuracy of EMT model is decided by numerical integration time steps.

In Fig. 4-11 (a), one PV string is illustrated with *n*-1 current balancers realized by buck-boost converters. One dc-dc converter is series connected as a voltage balancer to compensate the voltage difference between the PV string and the DC bus. Because EMT modelling is only implemented for the current balancers, details of the voltage balancer are not drawn.

To obtain the required EMT model, the mathematical model for each PV module in a string should be derived first. The PV module is modelled as a voltage controlled

current source. The output current and voltage of each PV module is used as the input for the current balancer.

I. Mathematical model for PV module

The equivalent circuit for a basic PV cell can be used to give the mathematical model of a PV module as shown in Fig. 4-10 [24]. This circuit consists mainly of a current source determined by sun irradiance and a parallel connected diode which generates dark current. These two parts dominate the *I-V* output of the PV module. The photo current I_{ph} and diode reverse saturation current I_d are influenced by the PV module temperature. The series resistance R_s represents the internal loss and shunt resistance R_{sh} mimics the influence of ground leakage current. Usually, the impact of low series resistance and high shunt resistance values can be ignored to yield a simplified PV cell model. Detailed mathematical model is simulated in Matlab Simulink [25] to operate with the given EMT model for the proposed architecture.

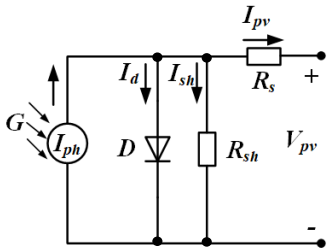


Fig. 4-10 PV module equivalent circuit.

II. EMT model for current balancers

Taking the i^{th} current balancer as an example, the switches S_{1_i} and S_{2_i} are a complementary pair and controlled by gate signal g_i (1=on, 0=off). As shown in Fig. 4-11 (b), the switches in the buck-boost converter cell are replaced by switched resistors R_{1_i} and R_{2_i} in the EMT simulation based equivalent circuit. R_{on} and R_{off} are resistance values during the on and off states of switching devices.

$$R_{1\_i} = g_i R_{on} + (1 - g_i) R_{off}$$
$$R_{2\_i} = (1 - g_i) R_{on} + g_i R_{off} \quad (5)$$

The small capacitance parallel connected with each PV cell is represented by a Norton equivalent circuit in Fig. 4-11 (b). The voltage V_{c_i} across the capacitance is

equal to the single PV cell voltage V_{pv_i} which is calculated by the EMT mathematical model. To mimic the current balancing of the buck-boost converter, the current through the inductor is represented by current source i_{L_i} in the EMT model.

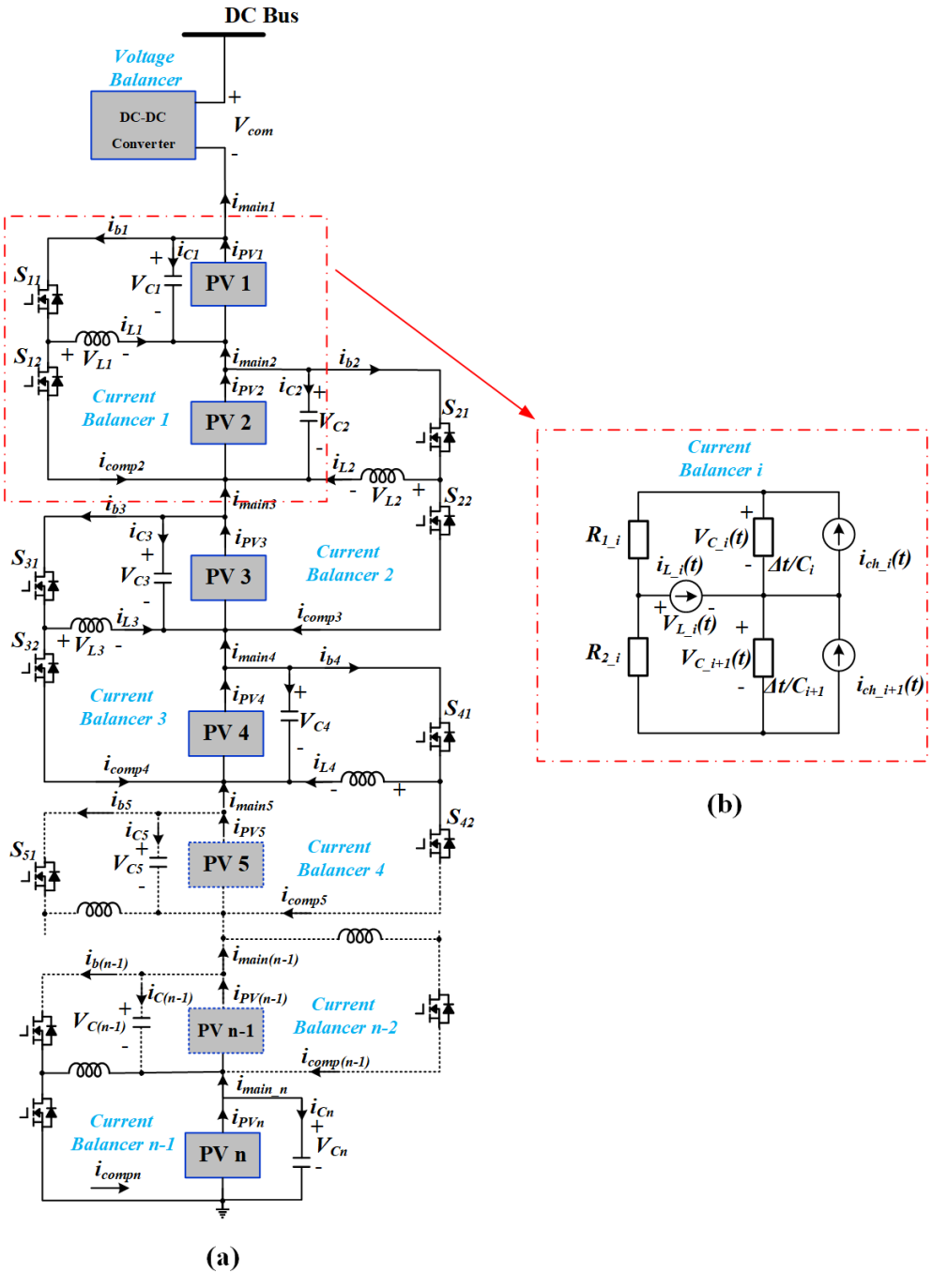


Fig. 4-11 EMT Model for one representative current balancer.
(a) One PV string with current balancer realized by buck-boost converter and
(b) EMP representation for each buck-boost converter.

The current and voltage values of the inductor at the present time step can be calculated by the state values of the capacitance and inductance at the previous time step, as given in equation (6).

$$V_{L\_i}(t) = \frac{V_{C\_i}(t-\Delta t)}{R_{1\_i}} - \frac{V_{C\_i+1}(t-\Delta t)}{R_{2\_i}} - \frac{i_{L\_i}(t-\Delta t)}{1/R_{1\_i} + 1/R_{2\_i}}$$
$$i_{L\_i}(t) = i_{L\_i}(t-\Delta t) + V_{L\_i}(t)\frac{\Delta t}{L} \tag{6}$$

The PV string with *n* PV modules, consists of *n*-1 current balancing converters and one single voltage balancing converter. As indicated in Fig. 4-11 (a), current i_{main} mimics the contribution of each PV module to the PV string and current i_{comp} is the compensating current from the lower half of the buck-boost converter to its associated PV module. Initially the current i_{main_1} is equal to the PV string current flowing into the DC bus and i_{comp_1} is zero. They are used as mediate variables for state values calculation which are given in equations (6) and (7).

$$i_{comp\_1} = 0$$
$$i_{main\_1}(t) = I_{o\_dc}(t-\Delta t)$$
$$i_{comp\_i+1}(t) = \frac{V_{L\_i}(t) + V_{C\_i+1}(t-\Delta t)}{R_{2\_i}} \tag{7}$$
$$i_{main\_i+1}(t) = I_{o\_dc}(t-\Delta t) + i_{comp\_i+1}(t)$$

The voltage V_{C_i} across the capacitor is the same as the PV module voltage V_{PV_i}. In this EMT model, the PV module is treated as a voltage controlled current source and the current i_{PV_i} of each PV module is obtained by a mathematical PV model. The virtual current source i_{ch_i} is applied to represent the influence of the parallel connected buck-boost converter.

$$i_{ch\_i}(t) = \frac{V_{C\_i}(t-\Delta t)}{\Delta t}C + i_{pv\_i}(t-\Delta t) - i_{main\_i}(t) - \frac{V_{C\_i}(t-\Delta t) - V_{L\_i}(t)}{R_{1\_i}} \tag{8}$$

$$V_{C\_i}(t) = V_{PV\_i}(t) = \frac{\Delta t}{C} i_{ch\_i}(t)$$

The time step Δt for the discrete state variables for EMT modelling is restricted by the PWM frequency of the buck-boost converter. Hence, the simulation time of EMT cannot be decreased significantly. There is a trade-off between accuracy of dynamic modelling and reduced simulation time. In this EMT model, the time step is selected to be 1/100th the switching frequency.

Simulation performance comparison between the EMT model and a physical switching model will be given in the next section. It is found that the EMT model can save on simulation time and computation resource. Especially in the large power scale D-MPPT architecture in this thesis, where single PV modules are controlled independently, and many devices are incorporated. The flexibility and scalability of the applied EMT model is also validated to show significant improvement.

4.3.3 MPPT Implementation and Control Strategy

The P&O MPPT algorithm is selected to give the voltage or current references of each PV module, for its simplicity and high accuracy [26]. A fixed perturb value is applied and an additional PI controller is used to force the dc-dc converter to track the generated voltage or current reference. The other function of the PI controller is to enhance stability and minimize oscillation during MPPT tracking.

The numbering order of PV modules in a PV string is 1 to *n* from top (dc bus end) to bottom (0V reference). As shown in Fig. 4-12 (b), the output voltage and output current of the first PV module is sensed for a P&O MPPT module that generates a switching signal for the voltage balancer. For 2nd to n^{th} PV modules, the 1st to n-1th current balancers are used for their MPPT implementation. Hence, each dc-dc converter corresponds to DMPPT realization for a single PV module.

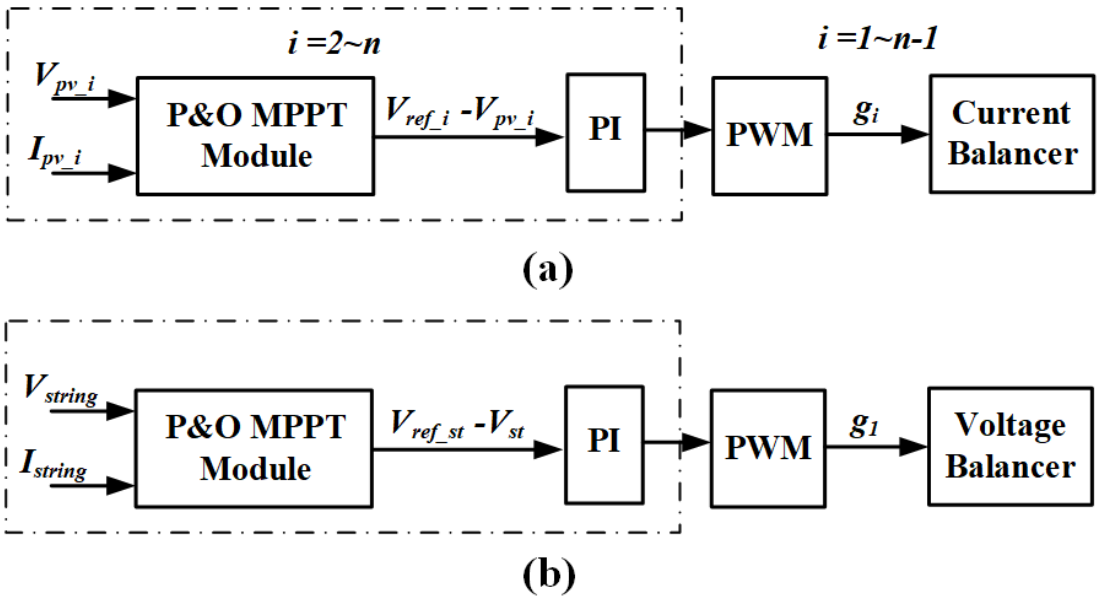


Fig. 4-12 P&O MPPT algorithm and PI control for switching signal generation.

In the proposed architecture, the i^{th} PV module is treated as the voltage source for the i^{th} current balancing converter, and the switching of the i^{th} converter regulates the i+1^{th} PV module to obtain maximum PV energy output. The main challenge for MPPT design is the interaction between the dc-dc converters.

The MPPT perturb values and the PI control parameters are designed to give good DMPPT performance [27], [28]. In this thesis, the first PV module MPPT is applied to get the PV output current reference but not the voltage reference to regulate the series connected voltage balancer, which proves to be a satisfactory solution.

4.4 Simulation Verification and Performance Evaluation

4.4.1 A Simple Two-Module PV System with Bipolar Output Voltage Balancer

To verify the proposed architecture, the simplest implementation is one PV string with two PV modules. A switched simulation model is built based on the circuit schematic as shown in Fig. 4-9.

The module type is 1SolTech 1STH-250-WH with its *I-V* and *P-V* curves plotted in Fig. 4-13. At T=25°C, the parameters of each PV module are V_{mpp}=30.7V and I_{mpp}=8.15A @1000W/m^2, and V_{mpp}=30.5V and I_{mpp}=4.06A@500W/m^2. The dc bus voltage is set to the sum of the two module MPP voltages which is 61.4V @1000W/m^2.

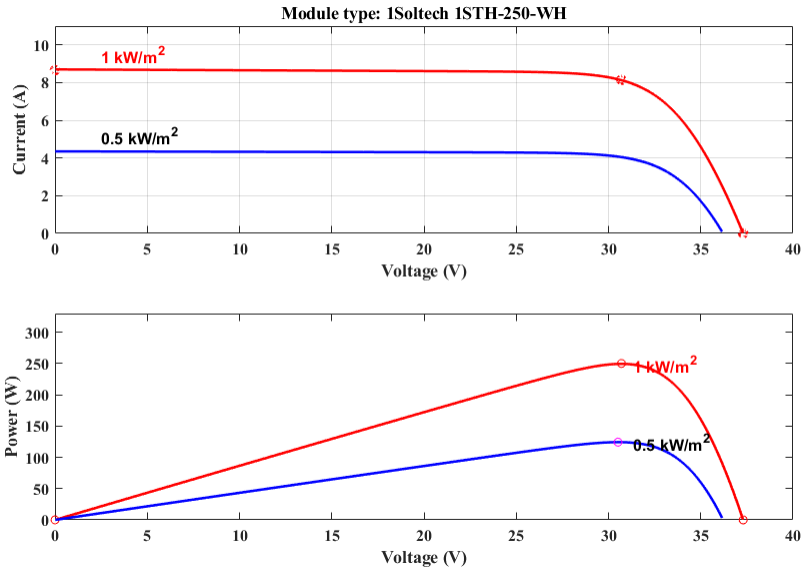


Fig. 4-13 *I-V* and *P-V* characteristics of PV module.

To observe balancer performance, the sun irradiance of PV module #1 varies from 500W/m^2 to 1000W/m^2 at t=0.5s, while PV module #2 maintains 1000W/m^2 irradiance. Fig. 4-14 shows satisfactory MPPT tracking. From Fig. 4-13, when the sun irradiance varies at 0.5s, the MPP voltage V_1 changes slightly (from 30.7V to 30.5V), while the MPP current drops from 8.15A to 4.06A. In Fig. 4-14, the proposed solution acquires MPPT performance. The MPP voltages and currents are obtained and fast tracking is obtained when the variation occurs.

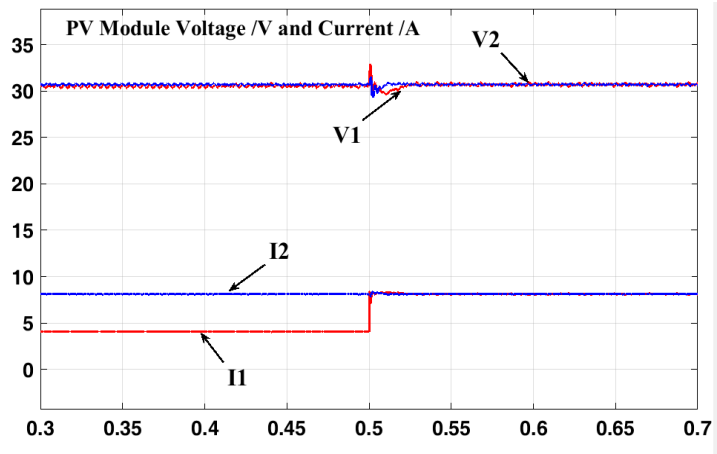
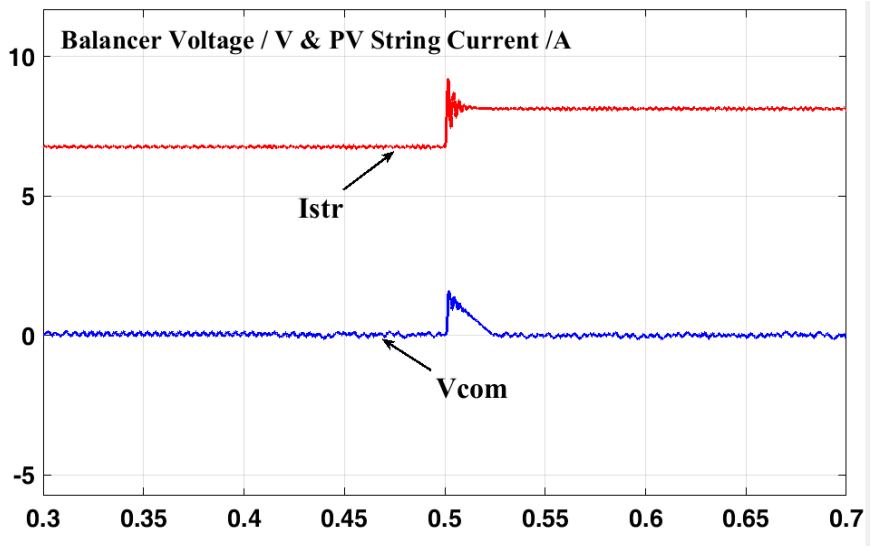
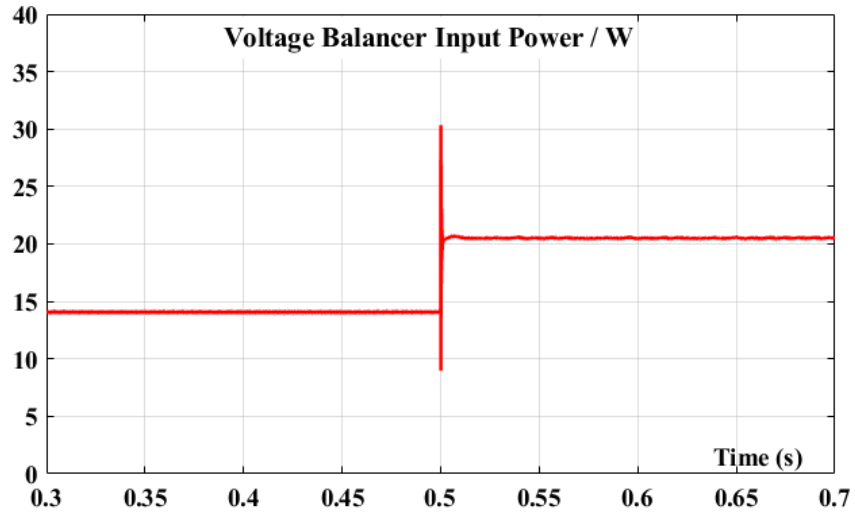


Fig. 4-14 PV module voltages and currents at MPP.

The PV string output current is shown in Fig. 4-15 (a), and because of the balancing converters, enables MPP currents from the two modules. Hence the whole PV string can still generate maximum energy output. Because the MPP voltages differ fractionally, the voltage balancer output voltage is approximately zero with minimal variation, as in Fig. 4-15 (a). The input power of the G4 converter increases from 14W to 20W in Fig. 4-15 (b), while the string's MPP power varies from 500W to 374W during this period. The input power of G4 increased as the voltage balancer needs to output a higher voltage to compensate the difference of the fixed DC bus and the PV string voltage. By voltage balancer compensation, the MPPT of the whole string can be guaranteed and the DC bus voltage is a fixed value. These values establish that the voltage balancer operates as a partial power converter.



(a)

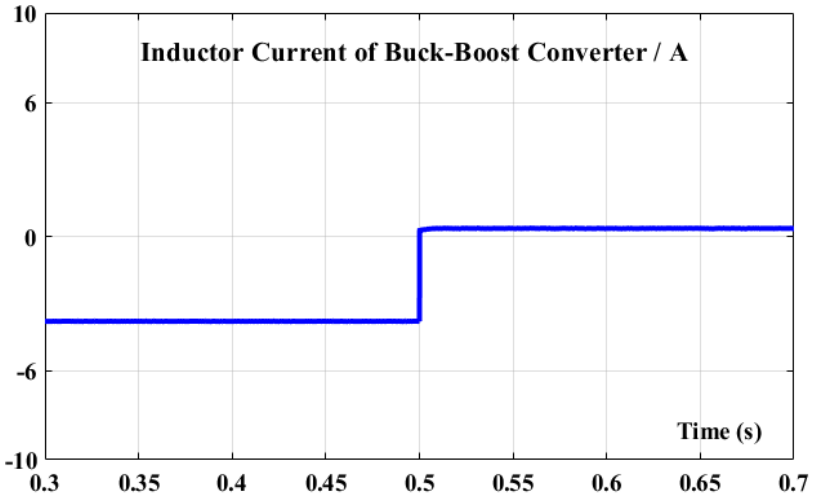


(b)

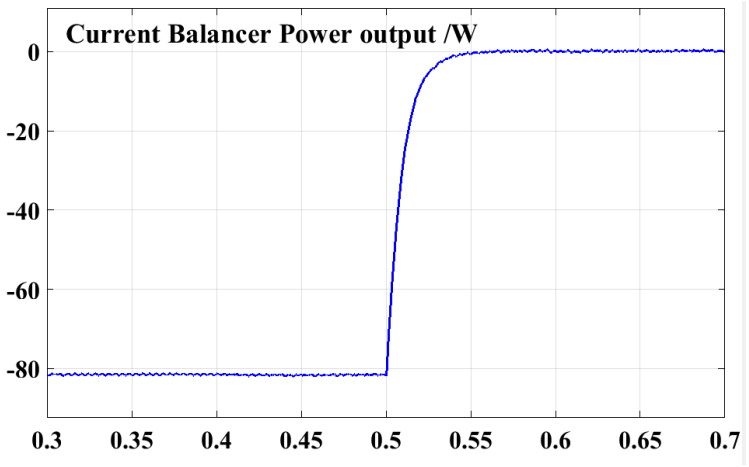
Fig. 4-15 Voltage balancer performance.
(a) Voltage balancer output voltage and PV string current and
(b) Power processed by voltage balancer

The mismatch in MPP currents I1 and I2 is compensated by the associated current balancer with its power output shown in Fig. 4-16 (b). For the disturbance step, the balancing current in Fig. 4-16 (a) is not exactly zero after 0.5s, but the current input is 0.15A when the two modules operate at the same condition. For the large MPP current variation of PV module #1, the power processed by current balancer is about 80W before 0.5s which is still much less than the PV string's MPP power of 500W

during this time. When the MPP currents match, the current balancer processes approximately zero output, resulting in a significant power loss reduction.



(a)



(b)

Fig. 4-16 Current balancer performance.
(a) Compensating current supplied by the current balancer and
(b) Power processed by the current balancer.

Based on simulation, the proposed architecture achieves partial power processing while retaining the DMPPT mechanism. Without mismatch, the auxiliary processors deliver (consume) neglected power and the full PV power flows through

the PV string without processing. The main power flow path is minimally affect by the associated converters, even under mismatched conditions.

4.4.2 Single PV String Power System Modelling

A single PV string with more PV modules is modelled in Matlab Simulink to further observe DMPPT performance. The PV string consists 5 series connected PV modules, hence four associated shunt current balancers. The unipolar buck converter is series connected to the dc bus to act as the voltage balancer. The EMT model is compared with the physical switched device model to observe the module level DMPPT efficiency.

I. PV Module Characteristics

Each PV module is realized by 3 series connected commercial modules, 1SolTech 1STH-250-WH. The PV module characteristics are shown in Fig. 4-17 and Fig. 4-18 with varying sun irradiance and temperature. At T=25°C, the parameters of each PV module are V_{mpp}=30.7V and I_{mpp}=8.15A @1000W/m^2 sun irradiance.

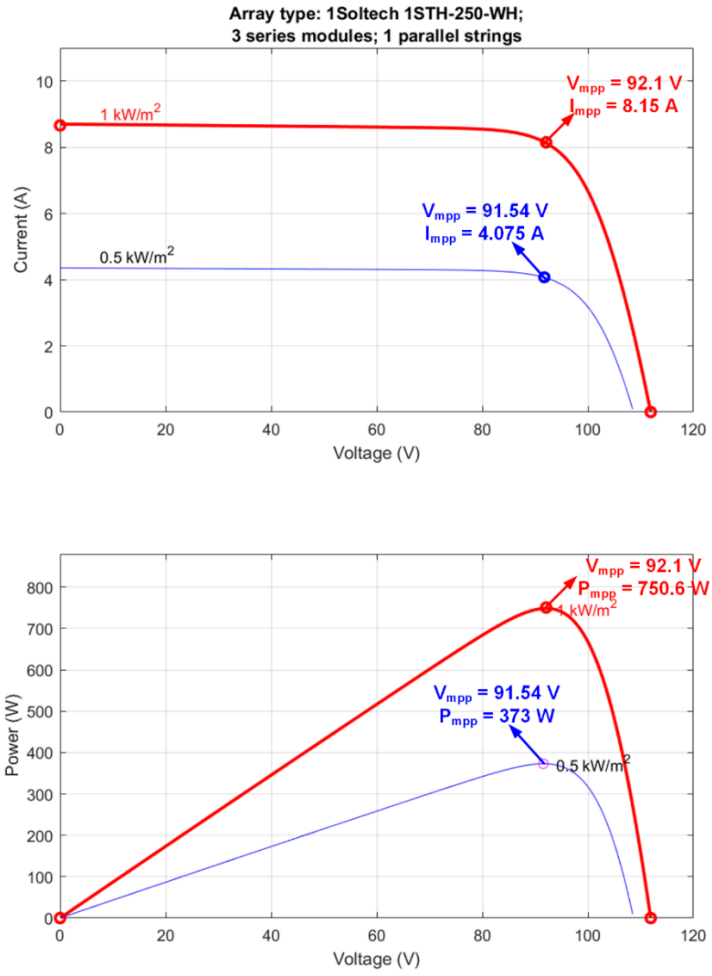


Fig. 4-17 *I-V* and *P-V* characteristics of PV module varying with sun irradiance.

In Fig. 4-17, the MPP current and MPP power decreases to around half when the sun irradiance drops from 1000W/m^2 to 500W/m^2. But the MPP voltage changes little which means it is reasonable for one voltage balancer to compensate the voltage difference between the PV string and dc bus.

The temperature influence on the PV characteristics is mainly on the MPP voltage which decreases from 92.1V to 75.37V as the PV module temperature increases from 25°C to 65°C at 1000W/m^2 sun irradiance.

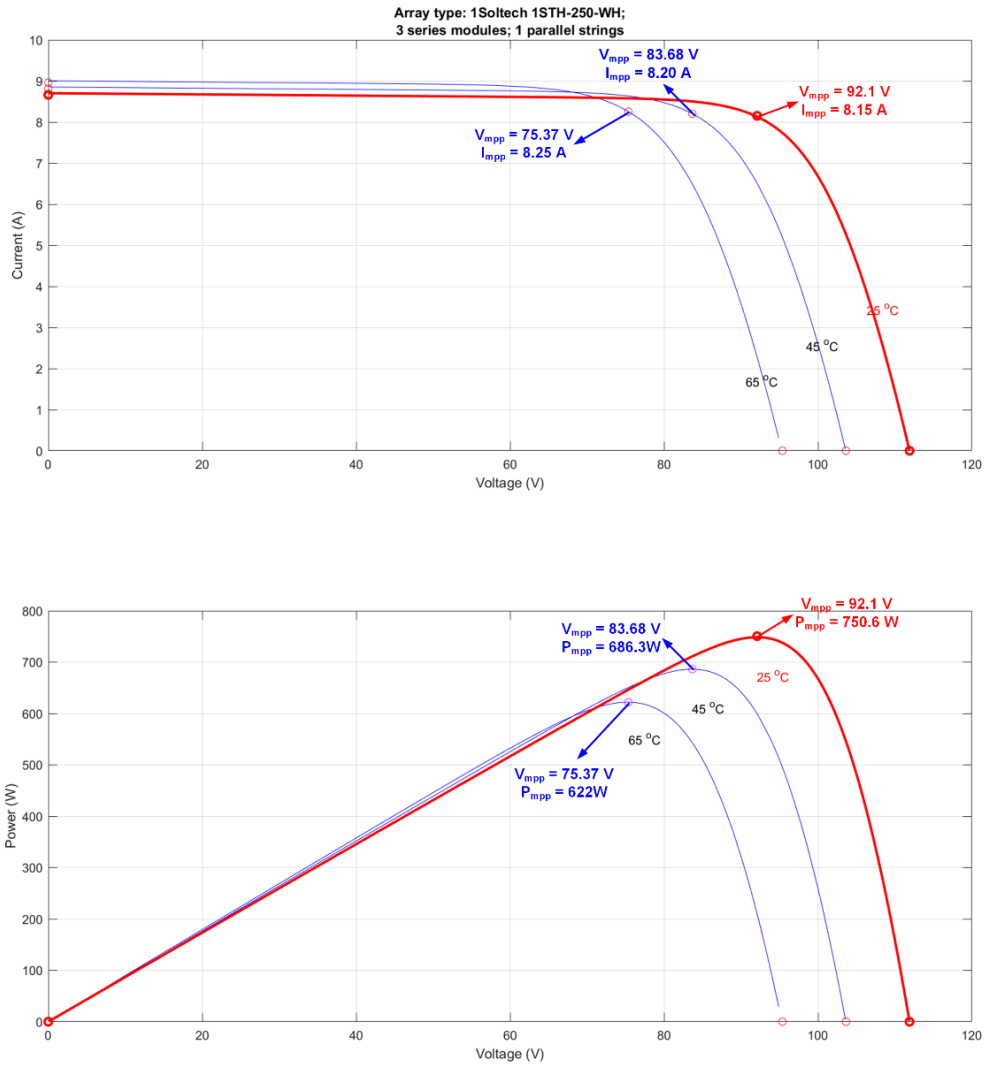


Fig. 4-18 *I-V* and *P-V* characteristics of PV module varying with temperature.

II. Modelling Comparison with a Unipolar Output Voltage Balancer

The single PV string system is integrated into a 460V ac grid through a central inverter. Each PV string consists of five PV modules, and the MPP power output for each PV module is 750W. The simulation results by EMT and the switched model use Simulink for comparison.

In the physical switched model for a 3.75kW PV string, each current balancer is realized with detailed switched devices. The PV module is simulated by Simulink with a five-parameter circuit model. By default, there is an inner algebraic loop within the

diode model of the PV model. Because a detailed power electronic converter is implemented, this loop is broken to speed up simulation.

In the EMT model for the same configuration, the current balancer is realized with its appropriate EMT model and the PV module is realized with a mathematical model. Except for the difference in modelling of the PV module and the current balancer, all other settings are the same for the EMT and switched simulation model. It is anticipated that the EMT model can accelerate the simulation speed and produce accurate simulation results under uniform and mismatched conditions.

For this single PV string system, the voltage balancer is realized with a unipolar buck converter which is sourced by an external isolated 50V DC supply. In both EMT and the switched model, the voltage balancer employs detailed switching devices. When the environmental factors change, as discussed, the PV string voltage will decrease, and the unipolar buck converter compensates the relatively small voltage decrease, with a reduced cost. The current balancer is realized by a simple buck-boost converter and the capacitance parallel connected to each PV module is 25uF. The DC bus voltage is approximately equal to the PV string voltage at standard sun irradiance and temperature. The specification for simulation modelling is listed in Table 4-1.

Table 4-1 Specification for Simulation of Single PV String Power System

Parameters		Values	
Simulink Discrete Sample time		1.25μs	
Standard Sun irradiance		1000W/m^2	
Standard temperature		25°C	
Single PV module V_{mmp}		92.1V	
Single PV module I_{mmp}		8.15A	
Single PV module P_{mmp}		750W	
Series connected PV module number		5	
Single PV String V_{mmp}		460V	
Single PV String I_{mmp}		8.15A	
Single PV String P_{mmp}		3750W	
Isolated DC Voltage for voltage balancer		50V	
DC Bus Voltage Level		485V	
Central Inverter Switching Frequency		20kHz	
AC grid Voltage level		416V line-to-line RMS	
Transformer Ratio		260/416	
Voltage balancer (Buck)		Current balancer (Buck-Boost)	
Parameters	Values	Parameters	Values
Inductance	500μH	Inductance	500μH
Capacitance	10μF	Capacitance	100μF
Switching Frequency	20kHz	Switching Frequency	20kHz

III. Performance Evaluation with Different Mismatch Conditions

With no mismatch, all the PV modules should operate at their specified maximum values at 1000W/m^2 sun irradiance, which is 750W for each PV module. Partial shading is one the primary causes for mismatch between PV modules. In this thesis, different partial shading conditions are investigated to observe the performance of the current and voltage balancers.

The voltage balancer output is 25V with no mismatch. When the sun irradiance decreases, the PV string voltage will decrease which will be compensated by the voltage balancer.

1. Partial shading of a single module

Supposing only one module is partly shaded at any time and the temperature is 25°C in this case study. The initial sun irradiance is 1000 W/m^2 for all the PV modules. The full simulation time is 2 seconds, and only one module will be in a partial shaded condition in this time period.

In the first scenario, the sun irradiance drops from 1000W/m^2 (MPP power 750W) to 500W/m^2 (MPP power 373W) at 1 second for modules 1 to 5 respectively. The MPP output power for each module after partial shading is shown in Table 4-2.

Table 4-2 PV modules outputs for single module partial shading condition

Mismatch module	PV module MPP power (Actual output / Ideal output) after mismatch / W									
	Switched Model					EMT Model				
	1	2	3	4	5	1	2	3	4	5
Module 1	372.45	747.05	747.96	748.14	748.04	373.1	748.7	748.7	748.7	749.1
Module 2	748.68	372.84	748.02	748.11	747.95	748.8	373	748.1	748.3	748.8
Module 3	748.68	748.63	372.92	748.05	748.34	748.8	748.6	373	748.5	749
Module 4	748.08	748.05	748.52	372.93	748.39	748.7	748.6	748.5	372.9	748.3
Module 5	748.24	748.18	747.76	746.62	372.24	748.8	748.6	748.4	748.2	372.2

By comparing simulation results of both the physical switched model and the EMT model, module level MPPT can be achieved at a high efficiency for both models. The average ratio of the actual MPP power and the ideal MPP power is over 99.5% for all modules. The EMT model simulation results match well with the physical model simulation results. However, the EMT simulation time is much less than the physical time. For the 3750W PV string and the 2 seconds simulation time setting, the EMT

model takes around 26 seconds and physical model takes over 4 minutes. The solver mode can also be a cause for this time difference. To get accurate simulation results, a continuous mode is chosen for the physical mode.

The PV module MPP power is illustrated in Fig. 4-19 showing the simulation results by the EMT model when the sun irradiance for module 3 drops from 1000W/m^2 to 500W/m^2.

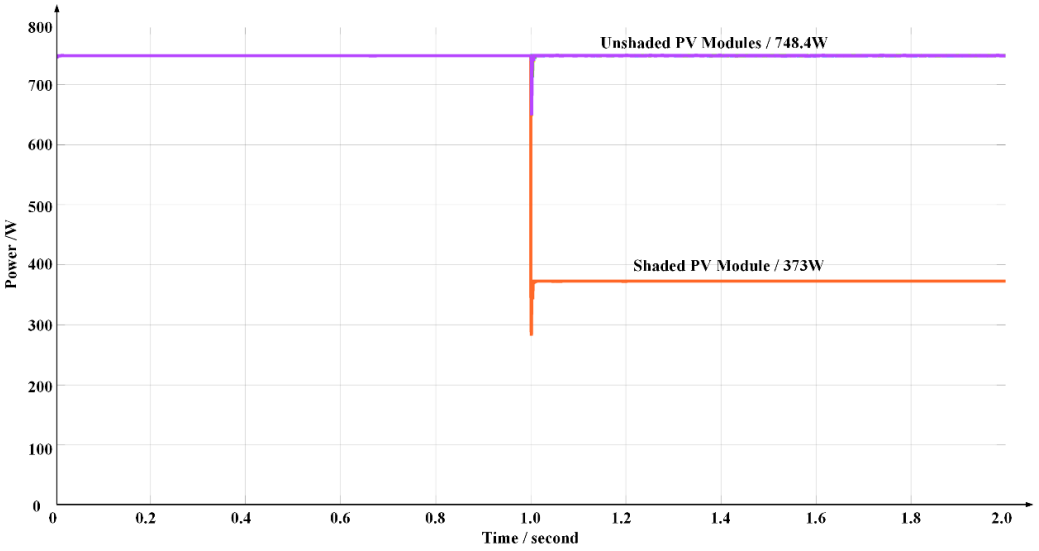


Fig. 4-19 PV modules outputs simulated by EMT model when single module partially shaded and sun irradiance drops from 1000W/m^2 to 500W/m^2.

In the second scenario, one module within the PV string is seriously shaded; the sun irradiance is 100 W/m^2 after 1 second simulation time. Thus, the ideal MPP power for the shaded PV module is 70W. The simulation result from the EMT model is shown in Fig. 4-20 and the shaded module is module 1. The figure shows that high MPPT tracking accuracy can be achieved even in this harsh partial shaded condition. In the following sections, module level DMPPT ability is observed with several shaded modules in a string to further verify the proposed design.

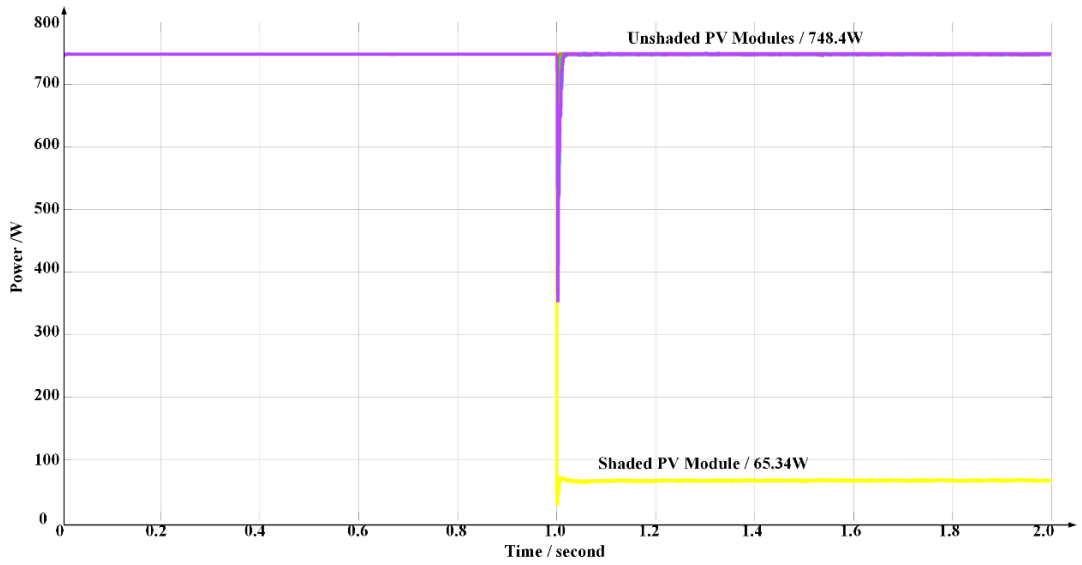


Fig. 4-20 PV modules outputs simulated by EMT model with single module significantly partially shaded and sun irradiance drops from 1000W/m^2 to 100W/m^2

2. Partial shading of several modules

In this case study, several different modules are partially shaded in a string after 1 second. The full simulation period is 2 seconds, and the starting sun irradiance is 1000W/m^2 for each PV module at 25°C. For the first scenario, the sun irradiance drops to 500W/m^2 for the shaded modules. The MPP power for each module after the mismatch is shown in Table 4-3 with a comparison of EMT model and switched model. Both models show a reasonably high MPPT tracking efficiency for different shading combinations at this mismatching condition.

Table 4-3 PV modules outputs when partial shading condition happened for several modules

Mismatch module	PV module MPP power (Actual output / Ideal output) after mismatch / W									
	Switched Model					EMT Model				
	1	2	3	4	5	1	2	3	4	5
Module 1,2	372.8	372.7	747.5	748.2	748.3	373	373.1	748.4	748.5	749.2
Module 1,3	372	747.5	372.3	748	748.4	372.8	747.8	372.6	748.4	748.9
Module 3,4	748.6	749	373	373	748.7	748.7	748.9	373.1	372.9	748.4
Module 1,2,3	371.8	372.5	372.2	747.5	748.1	372.9	372.8	372.7	747.8	748.3
Module 2,3,4	748.4	372.8	373	373	748.3	748.3	373	373	373	748.6
Module 1,5	373	748	748.3	748.6	373	372.9	748.3	748.6	748.9	373

To observe details of the PV modules outputs, the waveforms of the power outputs of the shaded modules are depicted with switched and EMT models in the following section.

In this mismatch condition, the sun irradiance of PV modules #1 and #3 varies from 1000W/m^2 to 500W/m^2 at t=2s within the 5 seconds simulation period, while the other PV modules remain at 1000W/m^2 irradiance. From manufacturer's data sheets, the MPP is 92.1V and 8.15A for each PV module at 1000 W/m^2 sun irradiance.

The physical switched model simulation result is shown in Fig. 4-21, where the module output voltage and output current are around 91.5V to 92.3V and 8.12A to 8.18A separately in uniform conditions. When mismatch occurs at 2s, the output current of module #1 drops to 4.1A and the output current of module #3 changes to 4.06A. The output current of the other three PV modules remains at about 8.15A with negligible variation.

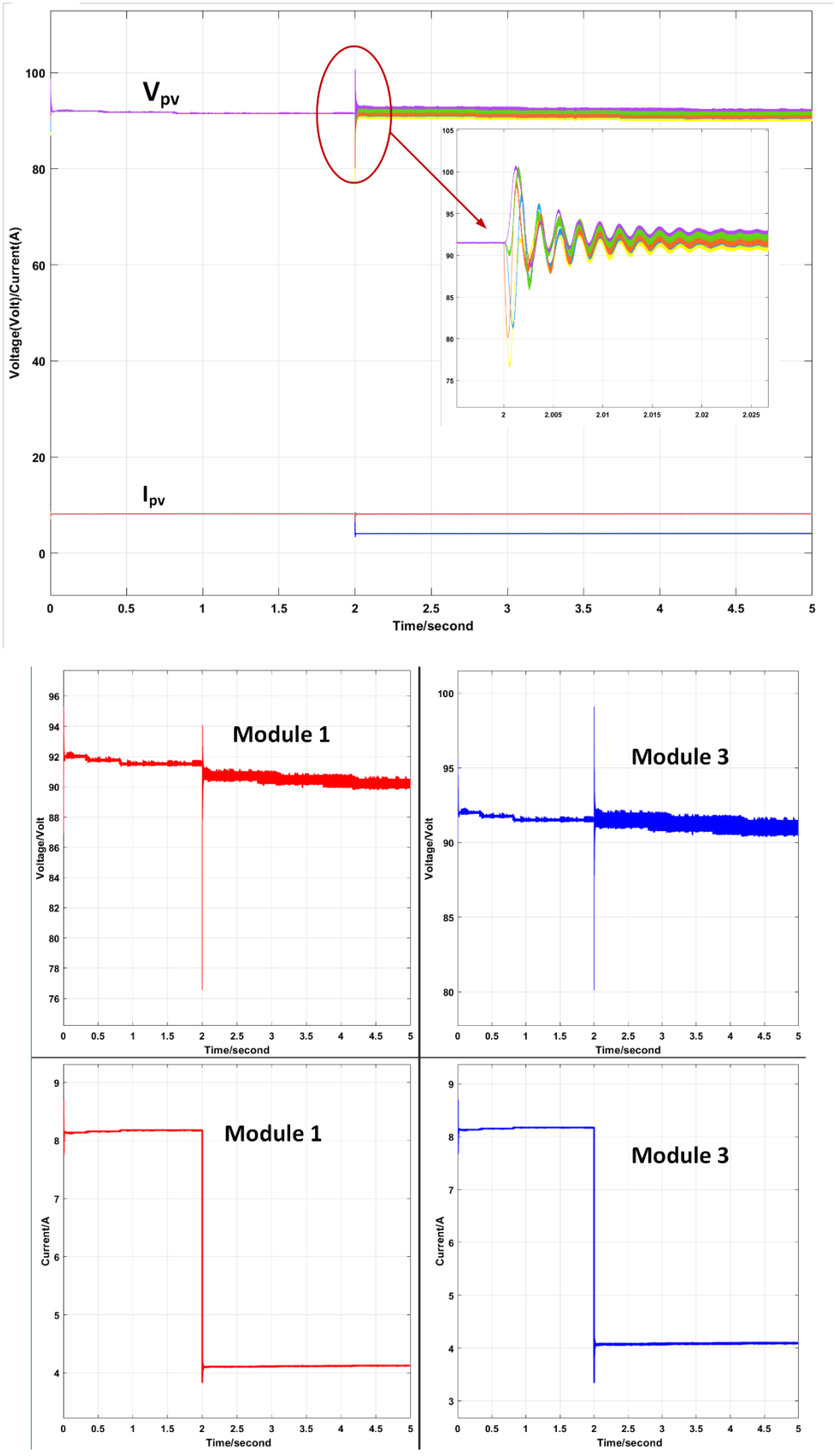


Fig. 4-21 PV module output voltage and current with variation in sun irradiance for detailed switched model simulation.

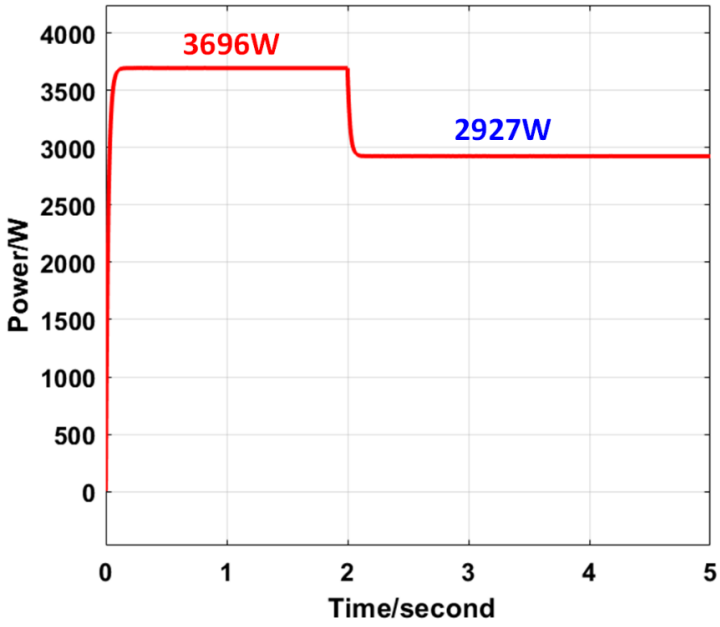


Fig. 4-22 Single PV string output power for Switched Device model.

The complete string output power is shown in Fig. 4-22. The theoretical PV string MPP power at 1000W/m^2 is 3750W and the simulated output power with the proposed DMPPT architecture is 3696W which means a 98.56% MPPT conversion efficiency. If a PV module is partially shaded with 500 W/m^2 sun irradiance, the MPP module output power is 373W. In the specified mismatching condition (2 shaded modules), the MPP power should be 2996W and the proposed architecture delivers 2972W. The MPPT efficiency during sun irradiance variation is 99.19%. Thus, MPP voltages and currents are obtained with fast tracking during normal and mismatched conditions, for the proposed architecture and MPPT algorithm.

For the same mismatching condition, the EMT model simulation results are shown in Fig. 4-23 and Fig. 4-24. The power output curve for the whole string in Fig. 4-23 shows MPPT efficiency. For a uniform normal operating condition, the efficiency is 99.81% and the efficiency is 99.90% with modules 1 and 3 mismatch. The output voltage and current for each PV module in Fig. 4-23 demonstrates that the correct maximum power points are rapidly identified after sun irradiance variation.

Compared with the detailed switched model, the EMT model gives satisfactory simulation results with only negligible differences, while the simulation time for the EMT model is reduced. For the single string system, a 5 seconds simulation period for

the switched model takes 65 seconds and EMT only takes 42 seconds for the same computing resource. It can be anticipated that the EMT model will be much faster and save computing resources when simulating larger power scale PV systems. In the following section, a 45kW PV power system with the proposed architecture is analysed with the EMT simulation model.

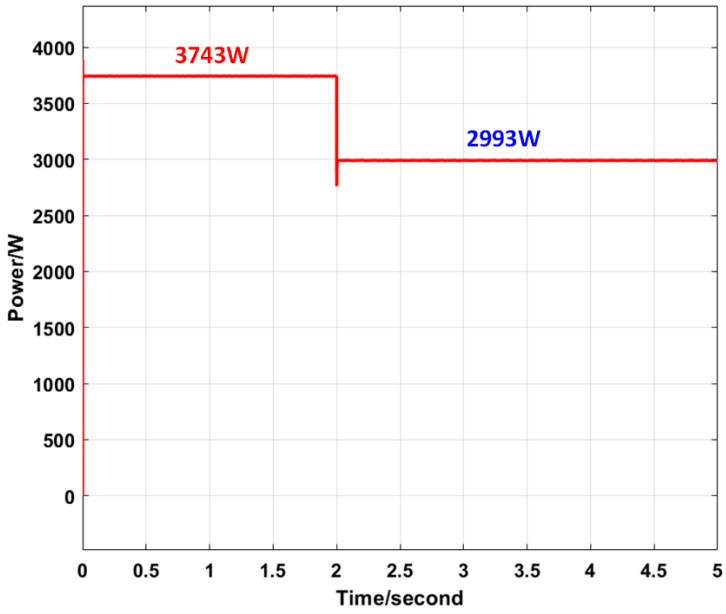


Fig. 4-23 Single PV string output power for EMT model.

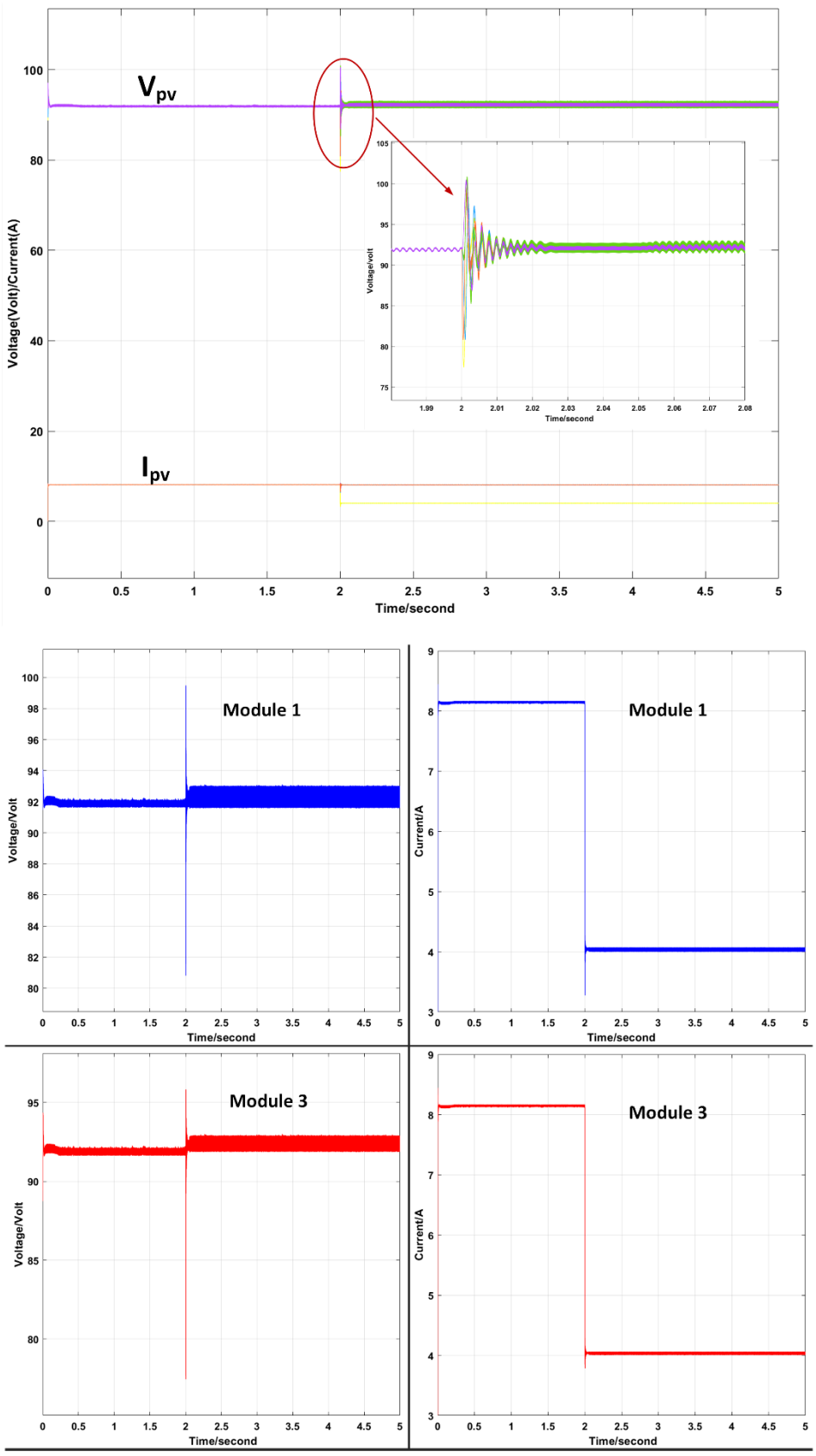


Fig. 4-24 PV module output voltage and current with variation in sun irradiance for EMT simulation model.

It has been established that the EMT model attains as accurate simulation results as the switched model. A harsh mismatch condition is simulated with the EMT model to observe DMPPT performance. The sun irradiance of modules 1, 2 and 3 change at a time point to 100W/m2. The MPP power of each module is shown in Fig. 4-25. The whole string MPP power reduces from 3570W to only 1710W; half the power is lost. The unshaded two PV modules output near 750W and the shaded three modules output over 96% of the desired MPP power. This established that the proposed design can still achieve high module level DMPPT in a harsh shaded condition.

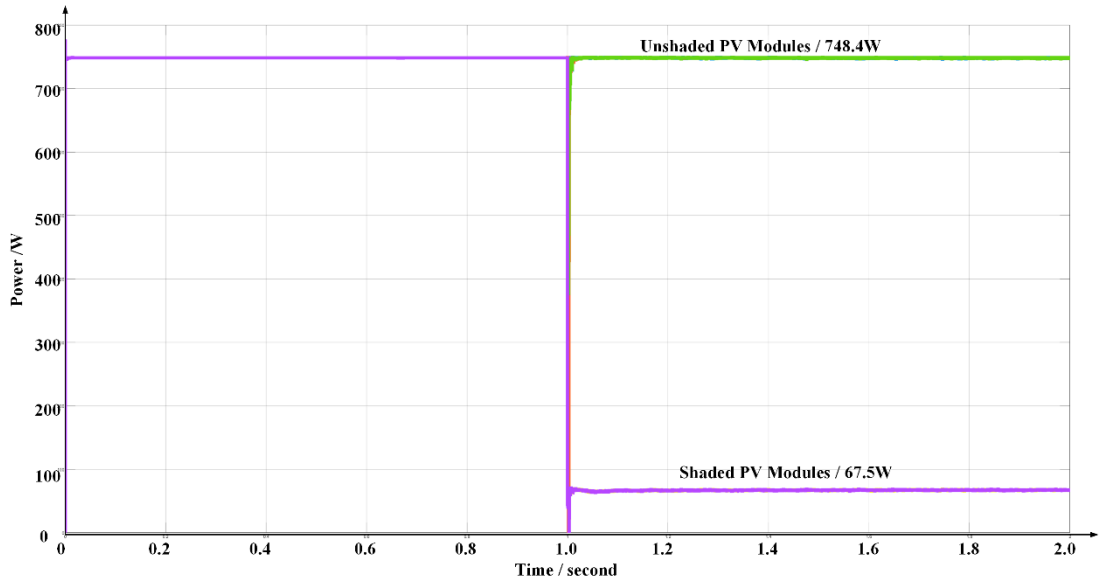


Fig. 4-25 PV module output for mismatch happens at three modules at the same time

4.4.3 Multi-String Multi-Inverter PV Power System

To further evaluate the performance of the proposed architecture in a more complex power system, a 45kW PV system is modelled using the EMT method. The block diagram is shown in Fig. 4-26 with three 15kW central inverters connected in parallel to the ac grid. Each 15kW inverter is sourced by four PV strings within which the proposed architecture is applied. All the partial power converters have the design specifications in Table 4-1.

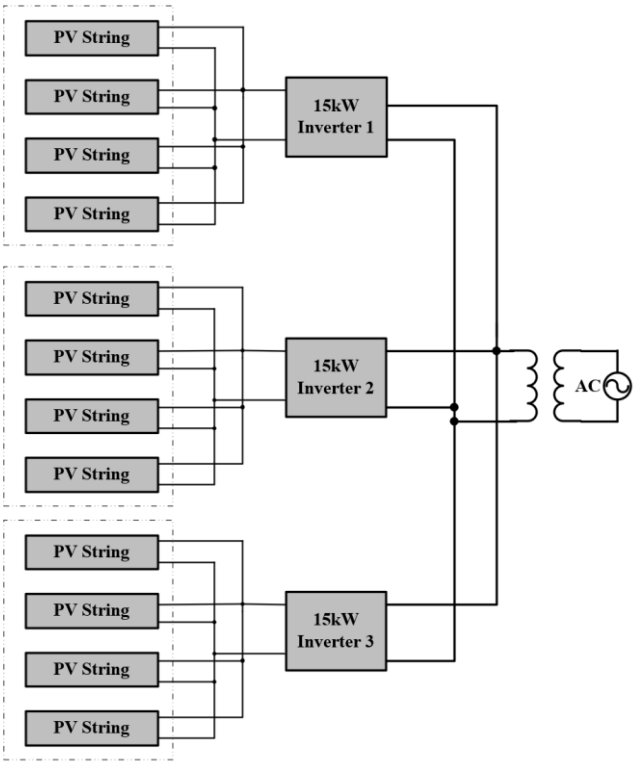


Fig. 4-26 45kW PV DMPPT power system with 12 PV strings connected in parallel.

To observe DMPPT efficiency, two partial shading conditions are subjected to the simulated PV system at 0.2s for PV string #2 and 1s for PV string #5 to #8 separately. The mismatching condition and simulated MPP power results are list in Table 4-4. The simulated power is close to the desired available MPP power for the mismatched PV string. The power output curve for the whole system is shown in Fig. 4-27. The energy conversion efficiency is satisfactory and verifies the effectiveness of the proposed distributed control and MPPT algorithm. Compared with conventional DMPPT architectures, 12 PV strings only require three central grid integrated inverters. A single-string single-inverter configuration is avoided which means a significant cost and size reduction.

Table 4-4 PV string generated power output variation under specified mismatching conditions

PV String No.	Mismatching Condition	Available MPP Power	Simulated MPP Power	MPPT efficiency
#2	at 0.2s, Sun Irradiance for PV Module 2 drops from 1000 W/m^2 to 500 W/m^2	3373W	3368W	99.86%
#5-#8	at 1s, Sun Irradiance for all PV modules inside the PV string drops from 1000 W/m^2 to 500 W/m^2	1865W	1865W	100%

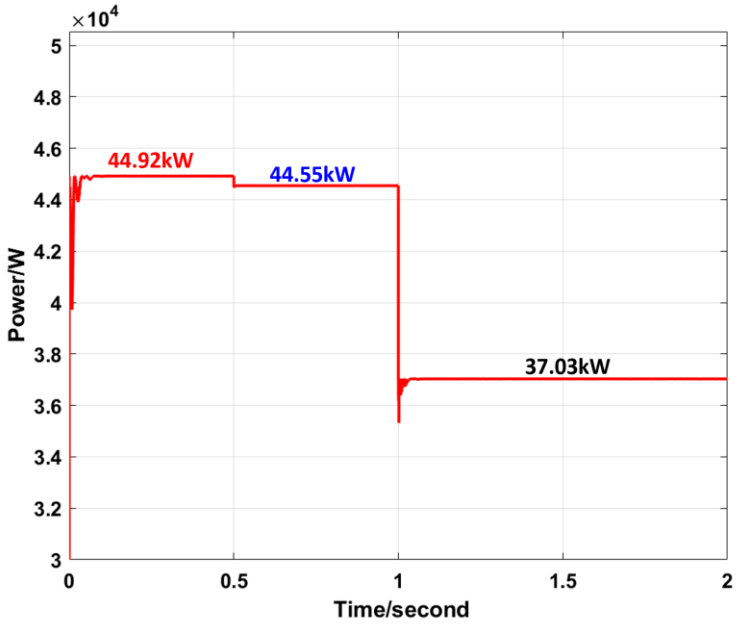


Fig. 4-27 45kW PV power system output with sun irradiance variation.

4.5 Summary

This chapter presented a new D-MPPT architecture based on partial power processing converters for parallel-connected PV strings. The operating principles and converter design requirements were presented. Based on the voltage and current balancing concept, a set of typical converter candidates were analysed with possible

implementing methodologies. The features for their application in the proposed architecture were given for a comprehensive comparison and design guide. A representative circuit diagram was discussed to provide an example for possible distributed control design and MPPT implementation.

The proposed architecture is intended for medium to large scale PV systems. To verify the design feasibility, several modelling methodologies were reviewed. An efficient EMT model was applied with conceptual analysis and mathematical expression. The applied control strategy and MPPT algorithm were applied to design three different power level PV systems. From the simplest two module system to a complicated 45kW multi-string multi-inverter system, the adopted architecture was established to have efficient and effective DMPPT ability. Simulation results confirm the feasibility of the proposed approach.

4.6 References

[1] D. Shmilovitz and Y. Levron, "Distributed Maximum Power Point Tracking in Photovoltaic Systems - Emerging Architectures and Control Methods," *Autom. – J. Control. Meas. Electron. Comput. Commun.*, vol. 53, no. 2, 2012.

[2] J. R. R. Zientarski, M. L. da S. Martins, J. R. Pinheiro, and H. L. Hey, "Evaluation of Power Processing in Series-Connected Partial-Power Converters," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 7, no. 1, pp. 343–352, 2019.

[3] M. Kasper, D. Bortis, and J. W. Kolar, "Classification and Comparative Evaluation of PV Panel-Integrated DC–DC Converter Concepts," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2511–2526, 2014.

[4] H. Jeong, H. Lee, Y. Liu, and K. A. Kim, "Review of Differential Power Processing Converter Techniques for Photovoltaic Applications," *IEEE Trans. Energy Convers.*, vol. 34, no. 1, pp. 351–360, 2019.

[5] P. S. Shenoy, K. A. Kim, B. B. Johnson, and P. T. Krein, "Differential Power Processing for Increased Energy Production and Reliability of Photovoltaic Systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2968–2979, 2013.

[6] Y. Nimni and D. Shmilovitz, "A returned energy architecture for improved

photovoltaic systems efficiency," in *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*, 2010, pp. 2191–2194.

[7] H. Zhou, J. Zhao, and Y. Han, "PV Balancers: Concept, Architectures, and Realization," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3479–3487, 2015.

[8] D. Shmilovitz, "Time variable transformers operating at a near-unity transfer ratio and some possible applications," *IEE Proc. - Electr. Power Appl.*, vol. 151, no. 2, pp. 161–168, 2004.

[9] J. R. R. Zientarski, M. L. d. S. Martins, J. R. Pinheiro, and H. L. Hey, "Series-Connected Partial-Power Converters Applied to PV Systems: A Design Approach Based on Step-Up/Down Voltage Regulation Range," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7622–7633, 2018.

[10] Y. Wang, A. Darwish, D. Holliday, and B. W. Williams, "Plug-In Repetitive Control Strategy for High-Order Wide-Output Range Impedance-Source Converters," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6510–6522, 2017.

[11] M. Uno and T. Shinohara, "Module-Integrated Converter Based on Cascaded Quasi-Z-Source Inverter With Differential Power Processing Capability for Photovoltaic Panels Under Partial Shading," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 11553–11565, 2019.

[12] T. Kamezawa *et al.*, "Photovoltaic system with generation control circuit," in *Proceedings of the IEEE International Conference on Industrial Technology (ICIT'96)*, 1996, pp. 242–246.

[13] Y. Jeon, H. Lee, K. A. Kim, and J. Park, "Least Power Point Tracking Method for Photovoltaic Differential Power Processing Systems," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1941–1951, 2017.

[14] S. Qin, S. T. Cady, A. D. Domínguez-García, and R. C. N. Pilawa-Podgurski, "A distributed approach to MPPT for PV sub-module differential power processing," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 2778–2785.

[15] J. T. Stauth, M. D. Seeman, and K. Kesarwani, "Resonant Switched-Capacitor Converters for Sub-module Distributed Photovoltaic Power Management,"

IEEE Trans. Power Electron., vol. 28, no. 3, pp. 1189–1198, 2013.

[16] R. Tymerski and V. Vorperian, "Generation, Classification and Analysis of Switched-Mode DC-to-DC Converters by the Use of Converter Cells," in *INTELEC '86 - International Telecommunications Energy Conference*, 1986, pp. 181–195.

[17] G. P. Adam and B. W. Williams, "Half- and Full-Bridge Modular Multilevel Converter Models for Simulations of Full-Scale HVDC Links and Multiterminal DC Grids," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 2, no. 4, pp. 1089–1108, 2014.

[18] R. D. Middlebrook and S. Cuk, "A general unified approach to modelling switching-converter power stages," in *1976 IEEE Power Electronics Specialists Conference*, 1976, pp. 18–34.

[19] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2ed ed. Springer, 2001.

[20] S. Cuk, "Modeling, analysis, and design of switching converters," Jan. 1977.

[21] S. R. Sanders, J. M. Noworolski, X. Z. Liu, and G. C. Verghese, "Generalized averaging method for power conversion circuits," in *21st Annual IEEE Conference on Power Electronics Specialists*, 1990, pp. 333–340.

[22] U. N. Gnanarathna, A. M. Gole, and R. P. Jayasinghe, "Efficient Modeling of Modular Multilevel HVDC Converters (MMC) on Electromagnetic Transient Simulation Programs," *IEEE Trans. Power Deliv.*, vol. 26, no. 1, pp. 316–324, 2011.

[23] W. Dommel, "Digital Computer Solution of Electromagnetic Transients in Single- and Multiphase Networks," *IEEE Trans. POWER Appar. Syst.*, no. 4, pp. 388–399, 1969.

[24] S. Pukhrem, "A PHOTOVOLTAIC PANEL MODEL IN MATLAB/SIMULINK." 29-Apr-2013.

[25] M. Villalva, J. Gazoli, and E. Filho, "Comprehensive Approach to Modeling and Simulation of Photovoltaic Arrays," *Power Electron. IEEE Trans.*, vol. 24, pp. 1198–1208, Jun. 2009.

[26] A. K. Abdelsalam, A. M. Massoud, S. Ahmed, and P. N. Enjeti, “High-Performance Adaptive Perturb and Observe MPPT Technique for Photovoltaic-Based Microgrids,” *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1010–1021, 2011.

[27] C. Olalla, D. Clement, M. Rodriguez, and D. Maksimovic, “Architectures and Control of Submodule Integrated DC-DC Converters for Photovoltaic Applications,” *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2980–2997, 2013.

[28] Y. Levron, D. R. Clement, B. Choi, C. Olalla, and D. Maksimovic, “Control of Submodule Integrated Converters in the Isolated-Port Differential Power-Processing Photovoltaic Architecture,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 2, no. 4, pp. 821–832, 2014.

CHAPTER 5

Plug-in Repetitive Control Strategy for Impedance Source Converters: an Islanded Mode Case Study

In this chapter, a modified plug-in repetitive control scheme is presented for HOWO-ISCs with accurate reference tracking (hence low distortion), fast dynamic response, and enhanced robustness. By using zero-phase-shift finite impulse response filters in both the internal model of the repetitive controller and its compensation network, the proposed method achieves zero steady-state error and an extended closed-loop bandwidth. For HOWO-ISC cases, this method outperforms conventional proportional-integral (PI) control, which has considerable steady-state error. It also eliminates the need for parallel loops of several frequencies when proportional resonant control or orthogonal transformation based PI schemes are used to remove lower order distortion.

The design process and performance analysis of the proposed repetitive control strategy are based on a modified three-phase HOWO-ISC configuration with a reduced number of switches. The islanded mode is selected as the case for control implementation. Simulation and experimental results confirmed the feasibility and effectiveness of the proposed control approach.

5.1 Background

Chapter 2 highlighted that HOWO-ISC based inverters have transfer functions giving low bandwidth, a penalty of increased passive elements and right-half-plane zeros, which result in lower order distortion of the ac output power. Specifically, high-order wide-output (HOWO) ISC topologies have non-minimum phase characteristics with extra phase lagging effects, which imposes limitation on the control design for achieving high loop-gain (low tracking error) and sufficient stability margin [1]. Hence, a reliable control strategy with accurate reference tracking ability is demanded for ISCs, which enables them to precisely execute the system level command for power flow regulation in an interconnected energy network, such as those involving maximum power point tracking [2].

In an ac system, conventional instantaneous value based proportional-integral (PI) control cannot achieve zero steady-state tracking error. Thus, PI control in the synchronous reference frame (SRF) using frequency decoupling, is employed [3] in the three-phase SQZS converter. However, to cancel the resonant peak in the transfer function, the active bandwidth needs to be reduced to a low level which weakens the dynamic performance. Also, parallel control loops for each frequency are adopted to guarantee output power quality, which leads to undesirable interaction between the different loops due to the frequency decoupled model approximation. Similarly, to save on mathematical transformations, parallel proportional resonant (PR) control loops are applied to the Ćuk type three-phase inverter in [4] to achieve sufficient harmonic rejection. Since each PR control loop targets only a specific frequency component, multiple control loops are needed, where the loops may interact. This complicates the controller and its efficiency. Nonlinear schemes such as sliding-mode control have been employed in differential mode sepic and Ćuk converters [5][6]. The target variable usually cannot be directly controlled; so a proper sliding surface, combining several state variables, has to be selected. High-pass filters are required to derive the transient signal of the control input in a time-variant ac system. Also, the sliding surface coefficient is influenced by parameter mismatch and load variation, which affects the practical performance.

Repetitive control, based on the internal model principle, is able to attenuate periodic disturbances, and has been adopted in power electronic converter applications

[2], [7]–[11]. In [8], plug-in repetitive control is directly adopted for the SPWM two-level inverter in an uninterruptable power supply (UPS), to ensure low distortion, robust output voltage. In [9], parallel plug-in repetitive control with reduced data memory is used in a bridgeless rectifier topology. The modular multilevel converter (MMC) circulating current can also be eliminated by repetitive control [10][11]. However, unlike the mentioned topologies, HOWO-ISC transfer functions usually have right-half-plane (RHP) zeros, time-variant zero-pole locations, and high resonant peaks. These factors impose higher demand on the design of the digital filter and compensator parameters over that for a lower order converter model.

This chapter presents a generic design of a digital plug-in repetitive control strategy for a family of HOWO ISCs with emphasis on the analysis of the zero-phase-shift (ZPS) filter and compensation network to achieve an extended closed loop bandwidth (improved dynamic response) and minimized reference tracking error. In the proposed strategy, an inner PI control loop and a zero-phase-shift (ZPS) finite impulse response (FIR) compensator are employed to stabilize the converter model plant with improved error convergence speed. Another ZPS low-pass FIR filter is incorporated in the internal model feedback path of the repetitive controller to attenuate the high frequency gain. In this manner, robustness of the overall system is ensured.

The islanded mode SQZS converter has a higher order transfer function than in a grid-connected mode due to the pole caused by the output capacitor [12]. This will compensate the internal model design for the repetitive controller [9]. Unlike the SSTP configuration with zero-sequence component cancellation, the FSTP converter requires phase independent control for distortion immunity over the full baseband range, including the zero-sequence harmonics. Based on these two points, the islanded mode SQZS FSTP inverter is used as the illustrative case study to verify the repetitive controller design.

This chapter is organized as follows: A representative ISC based inverter is discussed in section 5.2 with operational principle analysis and small signal modelling. Then the design process of the proposed control strategy is described in section 5.3 using a selected case study with a novel three-phase SQZS converter configuration having a reduced number of switches. Simulation and experimental verification form

section 5.4, and finally, outcomes and observations are highlighted in section 5.5, in summary.

5.2 Operation of the Four-Switch Three-Phase SQZS Inverter

In this section, the operation principle of a three-phase inverter with reduced switches is analysed. Based on the generic SQZS converter configuration, this four-switch inverter offer boosting output voltage ability. Thus, voltage utilization of the dc input supply can be improved which is useful for PV application. By using small signal analysis, modelling and control requirements are given.

5.2.1 Operation Principle of the FSTP Inverter

The FSTP SQZS inverter can be depicted as in Fig. 5-1, where two SQZS converter output terminals and the dc negative (zero) reference are connected to a three-phase balance load. In this arrangement, the total device and passive component count is reduced. If V_{dc} is the dc input voltage, V_m is the peak value of the desired output phase voltage, and ω is angular fundamental frequency; in order to achieve the output voltage as in (1), the modulation references for the two SQZS converters are expressed by (2).

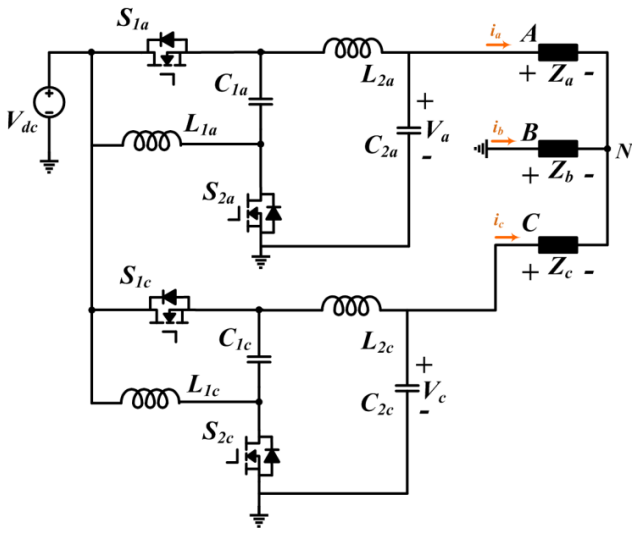


Fig. 5-1. SQZS-based FSTP Inverter.

From Fig. 5-1, the two SQZS converter output voltages in the FSTP configuration are equal to the line-to-line voltages V_{AB} and V_{CB}, respectively. With the voltage gain of the SQZS topology, its maximum ac output voltage magnitude is V_{dc};

thus, in an FSTP arrangement, the peak phase voltage V_m is $0.5774V_{dc}$, which is higher than $½V_{dc}$ in the conventional three-phase two-level inverter (using six switches, without triplen injection, but the same as with triplen/SMV injection). Also, compared to the sepic based FSTP inverter [5], this scheme has a pure sinusoidal ac common mode voltage (no dc component) between its ac side neutral point and the dc-link negative terminal. This eases the insulation design for an interfacing transformer in a grounded system.

$$\begin{cases} V_{AN}(t) = V_m \sin \omega t \\ V_{BN}(t) = V_m \sin(\omega t - \frac{2}{3}\pi) \\ V_{CN}(t) = V_m \sin(\omega t + \frac{2}{3}\pi) \end{cases} \quad (1)$$

$$\begin{cases} V_a(t) = \sqrt{3}V_m \sin(\omega t + \frac{1}{6}\pi) \\ V_c(t) = \sqrt{3}V_m \sin(\omega t + \frac{1}{2}\pi) \end{cases} \quad (2)$$

In contrast to SSTP inverters, where the zero sequence components cannot propagate onto the line-to-line voltage, their FSTP counterparts require each converter output voltage to be a purely fundamental component. This requires the control strategy of ISC based single-phase or FSTP configurations to have sufficient harmonic rejection over all baseband frequencies.

5.2.2 Modelling of the SQZS converter

The SQZS converter topology is redrawn in Fig. 5-2, where L_1 (with parasitic resistance r_1) and C_1 form the impedance source network; L_2 (with parasitic resistance r_2) and C_2 form the second order output filtering stage; V_{dc} is the input voltage and R is the load impedance in an islanded mode. The two switches operate in a complementary manner with the duty cycle of S_1 as the control input, which can be decoupled into a steady-state value δ plus its small perturbation $\Delta\delta$ in classical small signal dynamic analysis.

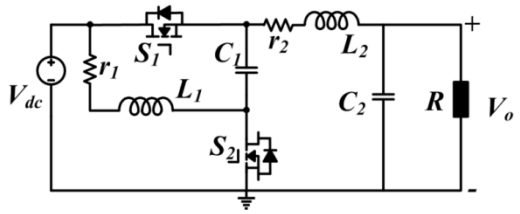


Fig. 5-2. SQZS converter topology.

Then linearizing, the generic small-signal transfer function G(s) of the SQZS converter is (3), where Δv_o represents the small voltage increment caused by the duty cycle perturbation $\Delta\delta$ around the steady-state value.

Similarly, applying this perturbing and linearization method to the steady-state equation of the voltage transfer ratio M and duty cycle δ in (4), the dynamic relationship between Δm and $\Delta\delta$ is as in (5). Therefore, to view the voltage transfer ratio as the controller output signal, the equivalent plant of the SQZS converter for control design can be rearranged as in (6) and Fig. 5-3. Then the dc steady-state gain of the plant transfer function $G_{vm}(s)$ (s=0) becomes independent of duty cycle variation (neglecting inductor parasitic resistance).

$$
\begin{aligned}
&G(s) = \frac{\Delta v_o(s)}{\Delta\delta(s)} = \frac{V_{dc}}{\delta}\frac{A_0 + A_1 s + A_2 s^2}{B_0 + B_1 s + B_2 s^2 + B_3 s^3 + B_4 s^4} \\
&A_0 = \delta R - M(\delta - 1)r_1 \\
&A_1 = C_1 R r_1 - M(\delta - 1)L_1 \\
&A_2 = C_1 L_1 R \\
&B_0 = \delta^2(R + r_1 + r_2) - (2\delta - 1)r_1 \\
&B_1 = \delta^2(C_2 R r_2 + L_2) + (\delta - 1)^2(C_2 R r_1 + L_1) + C_1 r_1(R + r_2) \\
&B_2 = \delta^2 C_2 R(L_1 + L_2) - (2\delta - 1)C_2 L_1 R + C_1 L_1(R + r_2) \\
&+C_1 L_2 r_1 + C_1 C_2 R r_1 r_2 \\
&B_3 = C_1 C_2 R L_1 r_2 + C_1 C_2 R L_2 r_1 + C_1 L_1 L_2 \qquad B_4 = C_1 C_2 L_1 L_2 R
\end{aligned}
\tag{3}
$$

$$
\delta = \frac{1}{2 - M} \tag{4}
$$

$$
K(s) = \frac{\Delta\delta(s)}{\Delta m(s)} = \delta^2 \tag{5}
$$

$$
G_{vm}(s) = \frac{\Delta v_o(s)}{\Delta m(s)} = K(s) \cdot G(s) = \delta^2 G(s) \tag{6}
$$

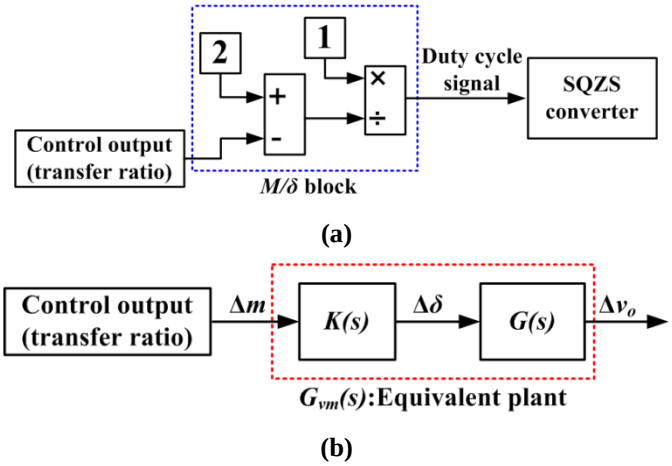


Fig. 5-3. Relationship between voltage transfer ratio and duty cycle in SQZS converter: (a) the signal transformation and (b) small-signal equivalent plant for controller design.

In quasi-steady-state analysis of the SQZS inverter, the voltage transfer ratio M should be modulated as a pure sinusoidal waveform as in (7), where A_m is the ratio of the converter ac side voltage magnitude (line-to-line voltage for the FSTP inverter) over the dc-link voltage. Then, from (4), the duty cycle can be estimated by (8) when ignoring the internal inertia of the SQZS converter.

$$M(t) = A_m \sin \omega t \tag{7}$$

$$\delta(t) = \frac{1}{2 - M(t)} = \frac{1}{2 - A_m \sin \omega t} \tag{8}$$

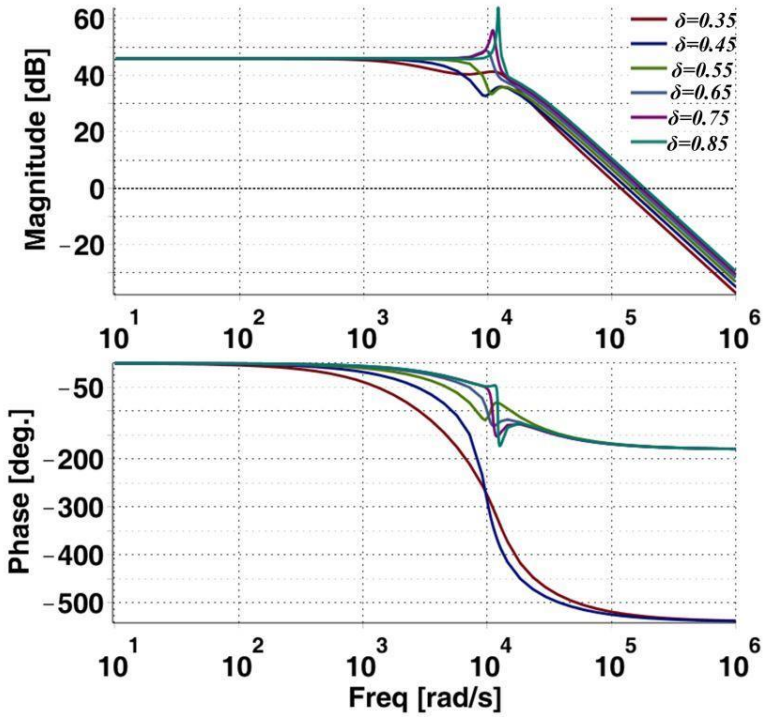
The passive element parameters of the SQZS converter are usually determined by the voltage and current peak ripple constraints, as discussed in [13][4][5]. With these principles, the FSTP SQZS inverter specification for this study is shown in Table 5-1.

In Table 5-1, with the shown dc-link and ac side line-to-line voltages, $A_m = 0.8$; hence, the duty cycle of each SQZS converter module varies approximately between 0.36 and 0.83, based on (8). Then, by substituting the parameters in Table 5-1 and varying the steady-state duty cycle δ, a family of Bode plots and pole-zero plots for the transfer function $G_{vm}(s)$ result as in Fig. 5-4.

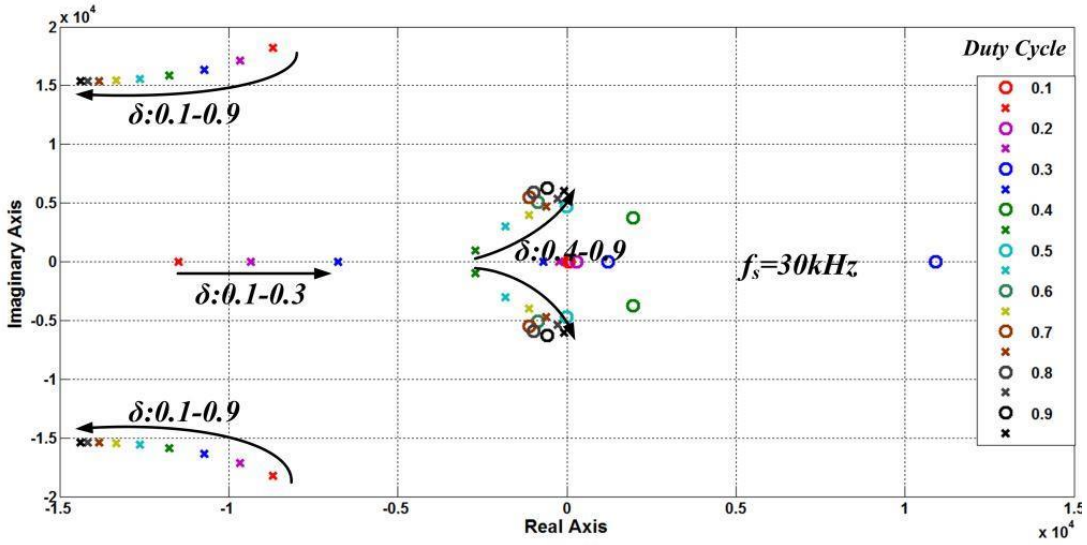
Table 5-1. Rated Values for the FSTP SQZS Inverter.

Power rating	P	2	kW
Per phase load	R	2.5	Ω
Input dc voltage	V_{dc}	125	V
AC line-to-line peak voltage	$\sqrt{3}V_m$	100	V
Inductor	L_1 and L_2	0.5	mH
Capacitor	C_1 and C_2	10	μF
Switching frequency (sampling frequency)	f_s	30	kHz
Fundamental frequency	f_o	50	Hz

From Fig. 5-4(b), when the duty cycle is less than ½, RHP zeros emerge, leading to non-minimal phase system performance with significant phase delay, as shown by the phase-frequency Bode plots in Fig. 5-4(a). Thus, a phase-leading compensation network is required to increase the phase margin and improve the dynamic response [14]. Also, in the amplitude-frequency Bode plots of Fig. 5-4(a), the resonant peak increases with increasing duty cycle.



(a)



(b)

Fig. 5-4. SQZS inverter characteristics with duty cycle variation:
(a) Bode plots of $G_{vm}(s)$ and (b) pole-zero map.

This time-varying performance with duty cycle is in-line with the topologically asymmetrical operation of the SQZS inverter (also other ISCs) for generating bipolar voltage. For example, in the SQZS inverter, the positive voltage level is generated directly by the dc-link; while the negative level is derived from the energy stored in the impedance network.

From (6), by using the transformation block K(s), the dc steady-state gain of $G_{vm}(s)$ is independent of the δ variation compared to (3); however, the gain of $G_{vm}(s)$ in the low frequency range ($s \neq 0$) is of concern for a dc-ac inverter system and changes with duty cycle variation. Consequently, the SQZS converter (and other ISCs) has a time-variant gain effect on the modulating signal along a fundamental period, which means lower order harmonic distortion will appear if the modulating signal is purely the fundamental component. But the real SQZS duty cycle trajectory should deviate from (8) if a pure fundament output voltage is generated.

Thus, the SQZS control strategy (and other HOWO-ICSs) should have sufficient harmonic rejection ability to ensure power quality. In this chapter, repetitive control with periodic disturbance attenuation is adopted to address this problem. Compared to its application in the two-level converter (such as in UPS [8]), the challenge of using this method in a HOWO-ISC is mainly the design of the digital ZPS filter and

compensation network for a time-variant plant, which can stabilize the converter and increase the effective closed-loop bandwidth. The detailed analysis and design procedure are based on the FSTP SQZS inverter.

5.3 Design of Plug-in Repetitive Controller

In this section, based on the design specification illustrated on section 3.3, a digital repetitive control is implemented for the FSTP SQZS inverter. The FSTP inverter requires independent control of the two converter modules to ensure voltage reference tracking as in (2), but only one inverter needs to be considered in the control design process. Fig. 5-5 illustrates the proposed digital plug-in repetitive control strategy for the SQZS inverter with V_d representing all external disturbances. The proposed control scheme employs a repetitive controller outer layer and a PI controller in the inner layer.

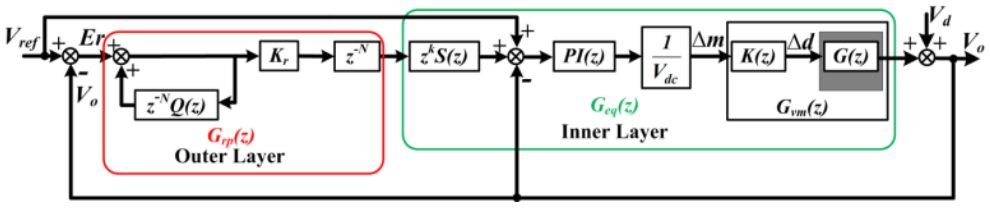


Fig. 5-5. Proposed Plug-in Repetitive Control Scheme.

Theoretically, an ideal plant for repetitive control should have an amplitude gain close to unity (0dB) in the low frequency range (before the cut-off frequency) and then rapidly fall off, monotonically [11]. Therefore, the inner PI controller in Fig. 5-5 is adopted to stabilize the converter transfer function $G_{vm}(z)$. However, PI control is not able to achieve zero steady-state error for the ac signal; thus, the fundamental error and lower order harmonic distortion (baseband frequency range) cannot be eliminated. Also, since the converter model in the negative half cycle has RHP zeros as in Fig. 5-4(b), its dynamic response with only PI control is slow. To provide sufficient closed-loop bandwidth as well as harmonic rejection capability, a FIR ZPS compensator $S(z)$ and an outer layer repetitive controller with a FIR ZPS low-pass filter $Q(z)$, are employed in Fig. 5-5 to provide fast and accurate voltage reference tracking [8].

5.3.1 Compensation Network for Modifying the Converter Plant

In Fig. 5-5, the inner layer compensates the converter plant (close to the ideal case), for the outer layer repetitive controller.

By forward difference mapping from the *s*-domain to the *z*-domain, the discrete transfer function of the normal PI controller can be transformed into (9), where T_s is the sampling (switching) period. Then, if $G_{vm}(z)$ represents the *z*-plane transformed version (forward difference mapping) of the transfer function $G_{vm}(s)$ in (6), its closed-loop *z*-domain transfer function $G_p(z)$ with PI control is expressed by (10). To suppress the resonant peak of $G_{vm}(z)$ in Fig. 5-4(a) over the full duty cycle range, the PI control parameters should be sufficiently small due to the RHP zeros when the duty cycle falls below ½; hence the dynamic response of the inner closed-loop is slow. For the specification in Table 5-1, the PI parameters are selected as P=0.4, I=600, which sets the cross-over frequency of the open loop transfer function $G_{vm}(z)PI(z)$ to about 200Hz, ensuring sufficient stability margin to adapt to a wide load range variation and other disturbances. Then, the amplitude Bode plot of the inner closed-loop system $G_p(z)$, with dc-link voltage normalization, drawn in Fig. 5-6, still has high resonant peaks and is not a qualified plant for repetitive control.

$$PI(z) = P + I \times T_s \frac{1}{z-1} \tag{9}$$

$$G_P(z) = \frac{G_{vm}(z) \cdot PI(z) / V_{dc}}{1 + G_{vm}(z) \cdot PI(z) / V_{dc}} \tag{10}$$

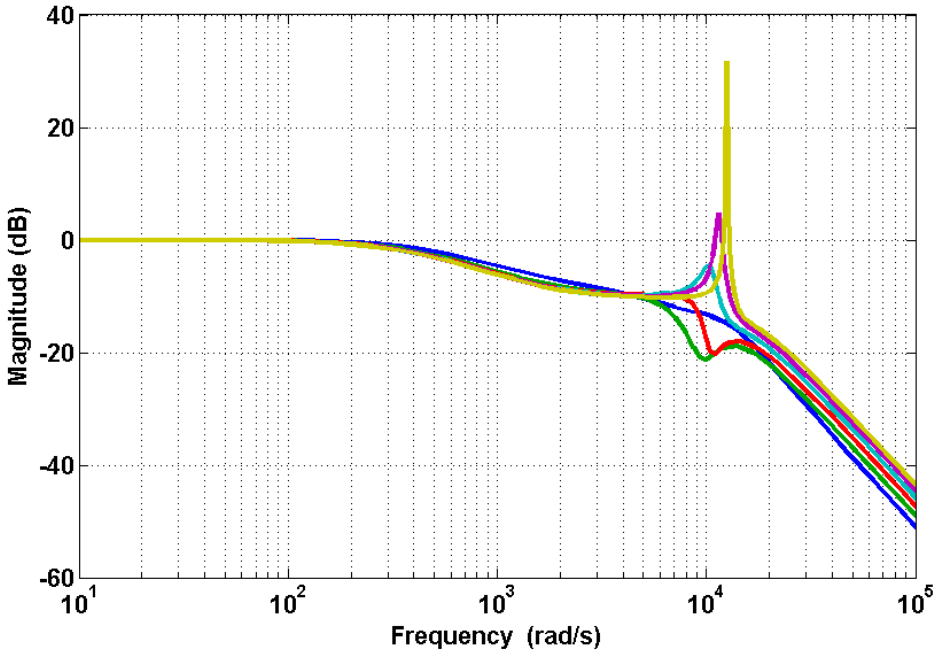


Fig. 5-6. Magnitude Bode plot of $G_p(z)$ with only PI control.

To eliminate the high resonant peaks of $G_p(z)$ for large duty cycles, an additional compensator is required. Considering the low phase margin caused by the RHP zeros and the floating position of the resonance peak due to its time-variant performance, the traditional second-order low-pass filter with additional phase delay and a fixed resonance frequency ZPS notch filter is not applicable to the SQZS inverter [8]. Instead, to mitigate a set of resonant peaks for a wide duty cycle range in the SQZS inverter without deteriorating the phase margin (dynamic performance), a *m* order FIR ZPS compensator $S(z)$ as in (11) with no phase lag, is employed. For the design case of Table 5-1, the resonance frequencies vary approximately between 1.5kHz and 2kHz as in Fig. 5-4(a); thus, a 17 order FIR ZPS filter $S(z)$ with a cut-off frequency of 1.5kHz is designed in MATLAB to suppress the resonance peak to below 0dB. The $S(z)$ parameters for this case are listed in Table 5-2.

$$S(z) = \sum_{i=0}^{m} a_i (z^i + z^{-i}) \tag{11}$$

Table 5-2. Coefficients a_i for the FIR ZPS compensator $S(z)$ in (11), m=17

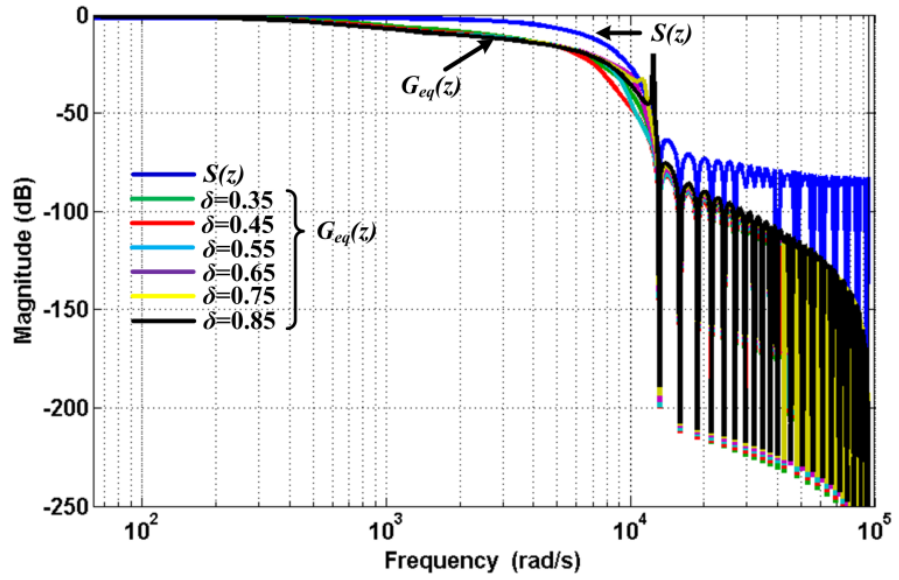
a_0=0.02442; a_1=0.00104; a_2=0.00196;
a_3=0.00329; a_4=0.00508; a_5=0.00736;
a_6=0.01015; a_7=0.01343; a_8=0.01714;

a_9=0.02120; a_{10}=0.02548;a_{11}=0.02985;
a_{12}=0.03413; a_{13}=0.03816; a_{14}=0.04174;
a_{15}=0.04472; a_{16}=0.04697; a_{17}=0.04836.

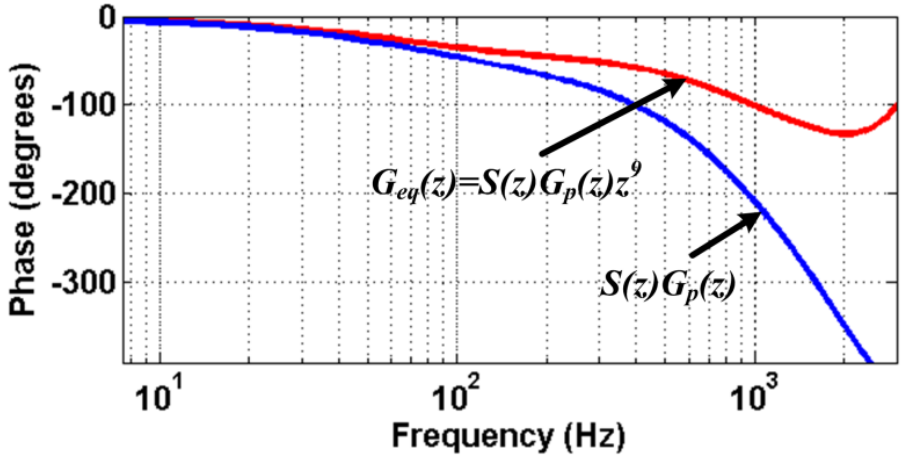
Further, to achieve sufficient phase margin and a fast dynamic response, a k step leading unit z^k is inserted to compensate the phase-lag, particularly for the RHP zeros. Due to the data storage of repetitive control, this leading unit will not result in a non-causal system and allows a faster PI controller to improve the dynamic performance. Then, the SQZS inverter repetitive control plant can be expressed by (12), in which stability is guaranteed and the transient performance is enhanced. Specifically, k is selected to be 9 in this design case.

$$G_{eq}(z) = z^k S(z) G_p(z) \tag{12}$$

With all parameters now known in this case study, the amplitude Bode plots of $G_{eq}(z)$ change with duty cycle δ can be displayed as in Fig. 5-7(a), where all the resonant peaks have been suppressed below 0dB. Also, the phase responses of the original plant $G_{vm}(s)$ in Fig. 5-4(a) reveal that the most severe phase lag occurs at the smallest duty cycle, which is approximately 0.33 in this case ($1 \geq \delta \geq ⅓$ then $+1 \geq M \geq -1$). The phase responses of $G_{eq}(z)$ with k=9 and $S(z)G_p(z)$ without phase-leading compensation are both displayed in Fig. 5-7(b), where the leading unit z^k is able to significantly increase the phase margin to realize an improved closed-loop bandwidth. A compensated equivalent plant suitable for repetitive control can now be achieved, as in (12).



(a)



(b)

Fig. 5-7. Compensation effects: (a) magnitude response of $G_{eq}(z)$ and $S(z)$; (b) phase compensation at δ=0.35.

5.3.2 Internal Model Design for Plug-in Repetitive Control

The repetitive controller with a fast feed-forward path is shown in the outer layer of Fig. 5-5 . The discrete implementation of the internal model of repetitive control is expressed by (13), where K_r is the gain coefficient to adjust the tracking error convergence rate and Q(z) is a low-pass filter to guarantee stability at high frequencies [15]. By periodic integration, any repeatable disturbances can be accumulated in the output; thus high gains for these periodic signals can be achieved in (13), where N is the number of sampling points within one fundamental period.

$$G_{rp}(z) = \frac{z^{-N}K_r}{1-Q(z)z^{-N}} \tag{13}$$

Based on Fig. 5-5 and (13), for the modified plant $G_{eq}(z)$, the voltage tracking error $Er(z)$ is expressed in (14). To ensure repetitive controller stability, the condition in (15) should be satisfied according to the small gain theorem [16]. This reveals that the magnitude of $\left|H(e^{j\omega T_s})\right|$ should always be less than unity when ω changes from zero to πf_s (Nyquist frequency).

$$Er(z) = \frac{(1-G_p(z))(z^N-Q(z))}{z^N-[Q(z)-K_rG_{eq}(z)]}V_{ref}(z) - \frac{(1-G_p(z))(z^N-Q(z))}{z^N-[Q(z)-K_rG_{eq}(z)]}V_d(z) \tag{14}$$

$$\begin{aligned}\left|H(e^{j\omega T_s})\right| &= \left|Q(e^{j\omega T_s}) - K_rG_{eq}(e^{j\omega T_s})\right| \\ &= \left|Q(e^{j\omega T_s}) - e^{j\omega kT_s}K_rS(e^{j\omega T_s})G_p(e^{j\omega T_s})\right| < 1 \\ &\text{where } \omega \in [0, \frac{\pi}{T_s}], T_s = \frac{1}{f_s}\end{aligned} \tag{15}$$

In practice, to ensure sufficient stability margin, $Q(z)$ can be selected as a close-to-unity constant (such as 0.95) or a low-pass filter, which is able to ensure sufficiently high magnitude gain in $G_{rp}(z)$ within the baseband. Thus, provided the reference voltage V_{ref} and disturbance V_d are both purely repetitive as in (16), by viewing $Q(z)$ as 1 in the low frequency range and substituting it into (14), the tracking error $Er(z)$ can be expressed by (17). This means that after each fundamental period, the magnitude of error $Er(z)$ can be attenuated to $H(z)$ times its previous value. Therefore, to ensure stability and increase the convergence rate, $H(z)$ must fall within the unity circle and should be as small as possible.

$$\begin{cases} z^{-N} \cdot V_d(z) = V_d(z) \\ z^{-N} \cdot V_{ref}(z) = V_{ref}(z) \end{cases} \tag{16}$$

$$z^N \cdot Er(z) = H(z) \cdot Er(z) \tag{17}$$

In the frequency domain, (14) can be rewritten as (18) with $T\left(e^{j\omega T_s}\right)$ being expressed by (19). By decreasing the magnitude of the term $T\left(e^{j\omega T_s}\right)$, the harmonic rejection ability can be enhanced, and the steady-state error of the repetitive controller is minimized. Specifically, zero steady-state error can be achieved at frequency ω, where $Q\left(e^{j\omega T_s}\right) = 1$.

$$\left|Er(e^{j\omega T_s})\right| = \left|T(e^{j\omega T_s})\right|.\left|\left(1 - G_p(e^{j\omega T_s})\right)V_{ref}(e^{j\omega T_s})\right| - \left|T(e^{j\omega T_s})\right|.\left|\left(1 - G_p(e^{j\omega T_s})\right)V_d(e^{j\omega T_s})\right| \quad (18)$$

$$T(e^{j\omega T_s}) = \frac{1-Q(e^{j\omega T_s})}{1-H(e^{j\omega T_s})} \quad (19)$$

For better convergence performance, $Q(z)$ should not introduce any additional phase delay into the control loop. Therefore, for low distortion in the SQZS converter output voltage, a FIR structure ZPS low-pass filter is designed for $Q(z)$ with a 3kHz cut-off frequency, for the case in Table 5-1. The expression of $Q(z)$ is indicated in (20) with the coefficients calculated in MATLAB, listed in Table 5-3.

$$Q(z) = \sum_{i=0}^{n} b_i(z^i + z^{-i}) \quad (20)$$

Table 5-3. Coefficients b_i for the FIR ZPS low-pass filter $Q(z)$ in (20), n=6.

b_0=0.59961; b_1=0.21864; b_2=-0.01795;
b_3=0.0063; b_4=-0.00624; b_5=0.0008;
b_6=0.00007.

To highlight the effect of $Q(z)$, the stability constraint of (15) is plotted in Fig. 5-8, where the vector $H(e^{j\omega T_s})$ should not exceed the unity circle. Due to the design demand, in low frequency range, $Q(e^{j\omega T_s})$ should be close to 1 as interpreted by the solid line in Fig. 5-8. Also, with the compensated converter plant of (12), $K_r G_{eq}(e^{j\omega T_s})$ maintains an approximate unity magnitude gain (when K_r=1) and small phase delay within the baseband frequency range. These imply that $\left|H(e^{j\omega T_s})\right|$ is sufficiently small and the repetitive controller can achieve steady-state error mitigation and fast convergence in its effective bandwidth. For the specific case in Table 5-1, the designed gain of the FIR ZPS filter $Q(e^{j\omega T_s})$ in (20) and Table 5-3 can be maintained as 0.98 up to 2 kHz, which is satisfactory to ensure sufficient lower order harmonic rejection. With increasing frequency, the phase delay of $G_{eq}(e^{j\omega T_s})$ increases, while its magnitude decreases. This makes the $K_r G_{eq}(e^{j\omega T_s})$ vector rotate closer to the imaginary axis, as shown by the dashed line in Fig. 5-8. Due to the high frequency attenuation effect of $Q(z)$, the unity circle around the terminal of vector $Q(z)$ moves left (dashed line) with an increase of frequency, which helps maintain the stability margin by ensuring sufficient distance from $H(e^{j\omega T_s})$ to the new circle (dashed line).

For the spectrum range above the cut-off frequency, the magnitude of $G_{eq}(z)$ falls off rapidly, as in Fig. 5-7.

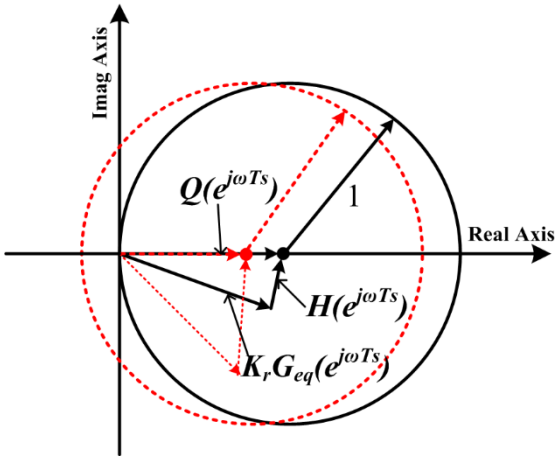


Fig. 5-8. Operational stability explanation.

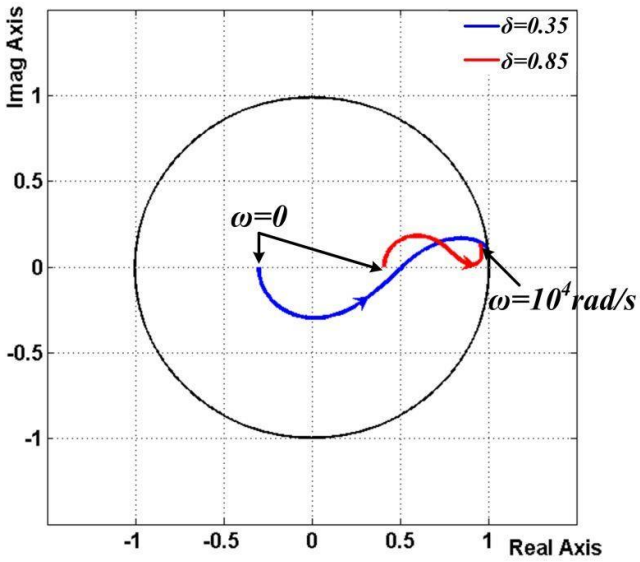


Fig. 5-9. Vector $H(e^{j\omega T_s})$ locus.

The proportional gain of the repetitive controller K_r is usually a real number less than 1. A larger K_r produces faster error convergence but less stability margin, as it will determine the length of $K_rG_{eq}(e^{j\omega T_s})$ (thus, also $H(e^{j\omega T_s})$) in Fig. 5-8. The trajectory of $H(e^{j\omega T_s})$ in the complex plane is drawn in Fig. 5-9 for K_r=1 at the operational points of minimum and maximum duty cycle δ. The stability margin is guaranteed with the selected control parameters for the SQZS inverter design case defined in Table 5-1.

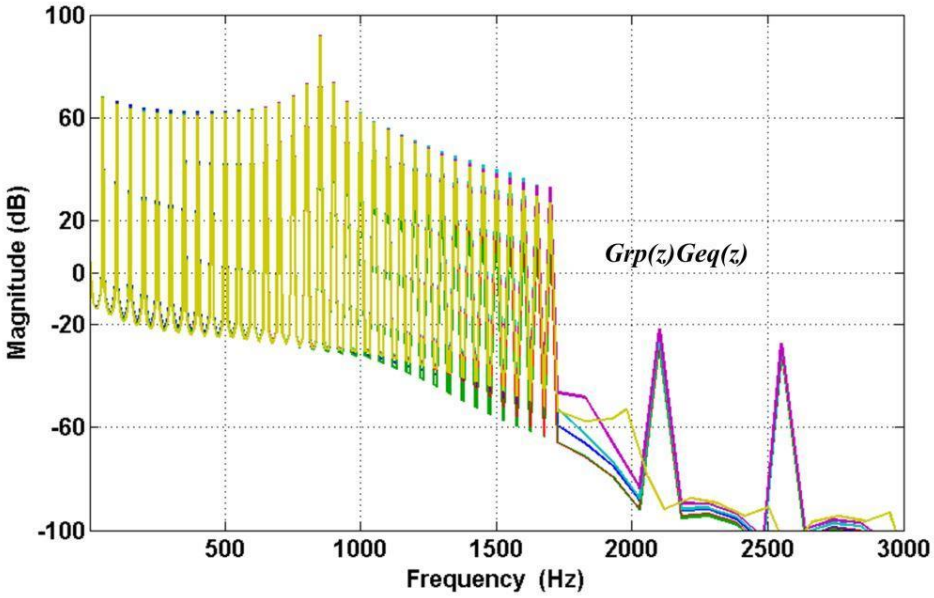


Fig. 5-10. Open loop gain $G_{rp}(z)G_{eq}(z)$ amplitude response.

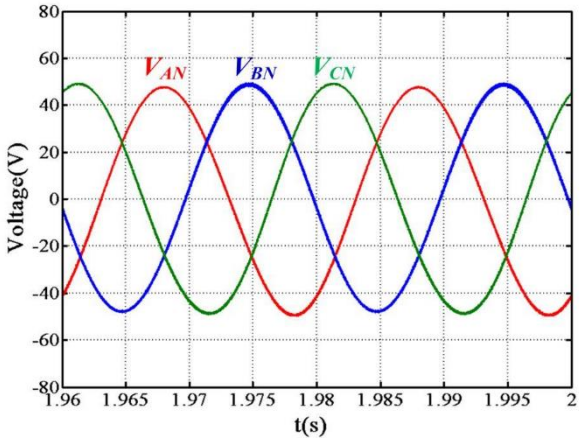
With all the design parameters known, the discrete open loop transfer function of the SQZS inverter with the proposed plug-in repetitive control strategy can be expressed as $G_{rp}(e^{j\omega T_s})G_{eq}(e^{j\omega T_s})$, and its amplitude gains under the full duty cycle variation range are shown in Fig. 5-10 (K_r= 1). The repetitive controller can attenuate the lower order distortion in the baseband by increasing its open loop gain at integer times the fundamental frequency. Due to the use of FIR ZPS compensator $S(z)$ and low-pass filter $Q(z)$, high frequency disturbance can be suppressed significantly. The effective bandwidth is extended compared to conventional methods, as shown in Fig. 5-10.

5.4 Simulation and Experiment Verification

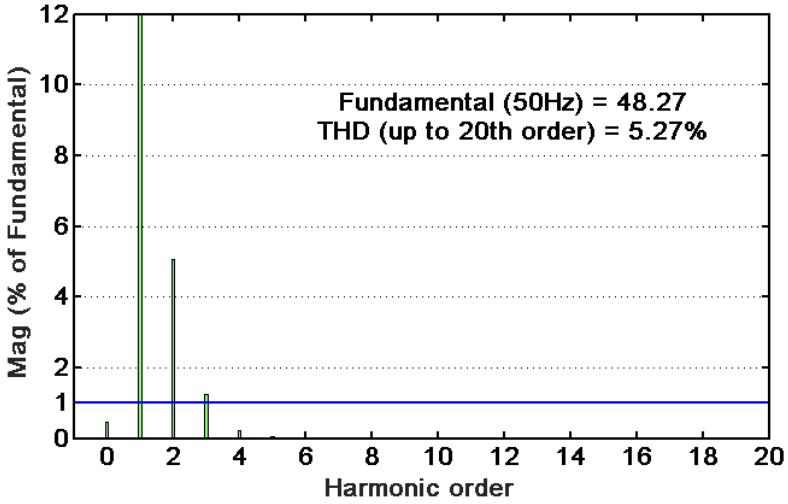
To validate the proposed control scheme, simulation and experimentation on the FSTP SQZS inverter are performed.

5.4.1 Simulation Tests

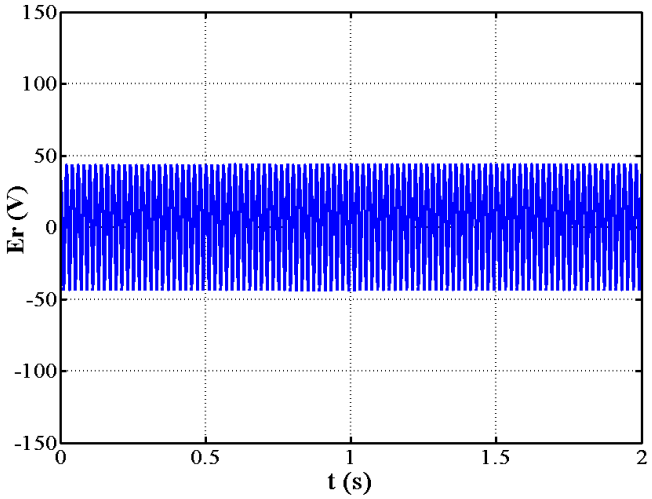
The simulation model of the topology in Fig. 5-1 is based on the specification in Table 5-1; thus, the desired output line-to-line voltage peak value is 100V (57.7V phase voltage) from the FSTP SQZS inverter. Initially, it operates with only the inner PI controller of Fig. 5-5, with parameters P=0.4 and I=600, which is achieved by considering the relative stability indicators.



(a)



(b)



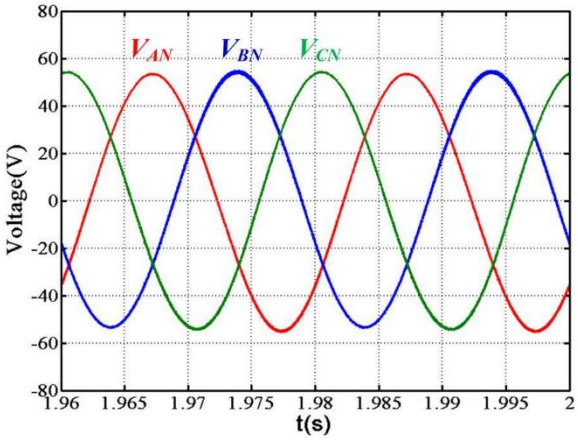
(c)

Fig. 5-11. FSTP-SQZS inverter with PI controller:

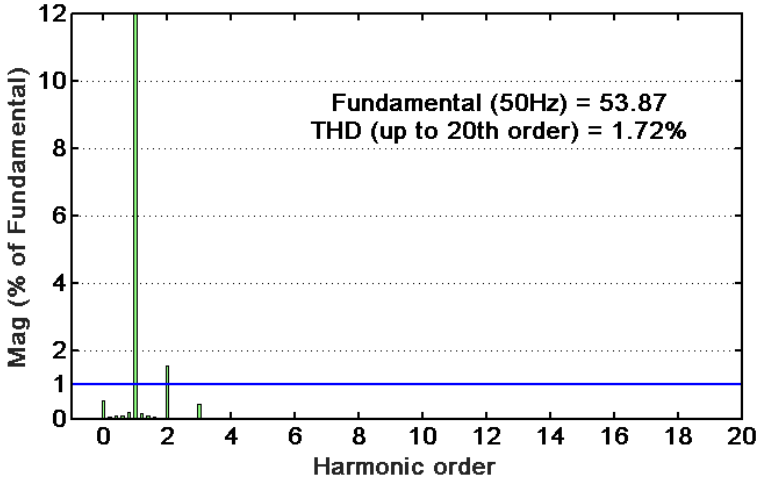
(a) output phase voltage waveforms, (b) fundamental magnitude and low order harmonic distribution for phase A output voltage; and (c) steady state error caused by PI control.

The results in Fig. 5-11 show considerable fundamental component tracking error and low order harmonic distortion (mainly 2nd order); and the calculated baseband (up to 20th order) total harmonic distortion (THD) is 5.3%. This is consistent with the theoretical analysis of the PI controlled SQZS converter with low bandwidth and non-uniform gains at different operating points.

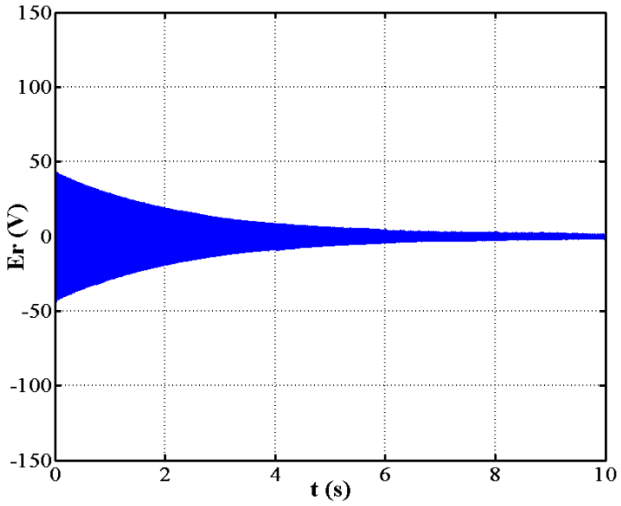
To eliminate the low order harmonic distortion and improve the reference tracking accuracy, repetitive control is employed, initially without compensator $S(z)$ but the PI parameters remain the same. The repetitive controller has a magnifying effect on the magnitude gain, including the resonant peaks. Due to the absence of $S(z)$, the proportional gain of the internal model K_r has to be decreased to guarantee stability. In this case, K_r is chosen to be 0.01. From Fig. 5-12(b), increased fundamental voltage magnitude and reduced 2nd order harmonic distortion can be achieved. However, in Fig. 5-12(c), the error convergence rate is relatively slow due to small K_r.



(a)



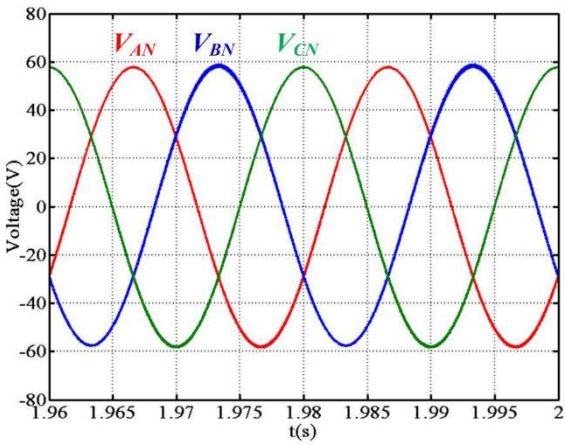
(b)



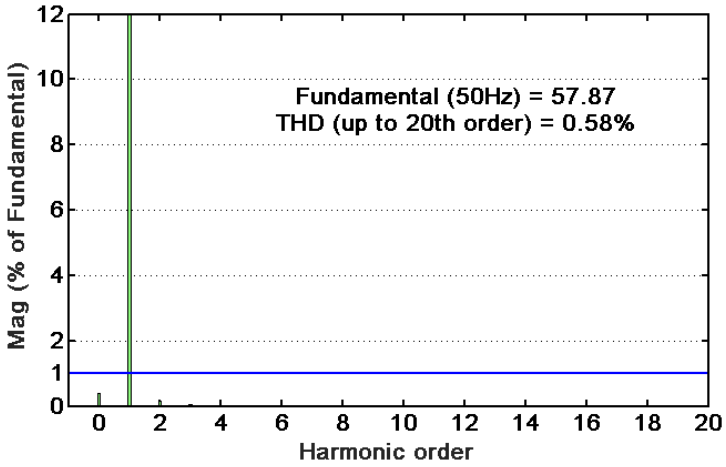
(c)

Fig. 5-12. FSTP-SQZS inverter using repetitive control without compensator $S(z)$ and K_r=0.01: (a) output phase voltage waveforms, (b) fundamental magnitude and low order harmonic distribution for phase A output voltage; and (c) error convergence process.

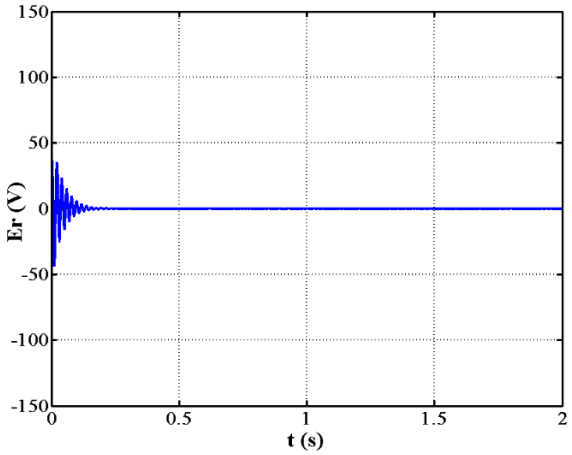
By incorporating compensator $S(z)$ into the control loop, the proportional gain K_r of the repetitive controller is increased. With $S(z)$ based on Table 5-2 and K_r=0.8, Fig. 5-13(b) shows that the fundamental voltage is able to precisely track the reference and low order harmonic components can be eliminated; hence, almost zero steady-state-error is obtained; and the error convergence rate significantly improves with a settling time of less than 0.2s, as illustrated in Fig. 5-13(c).



(a)

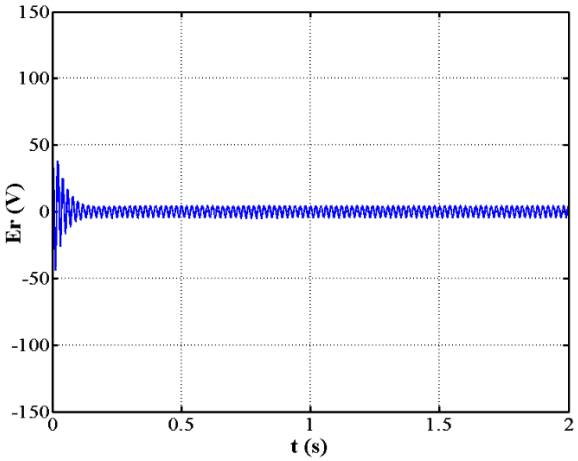


(b)

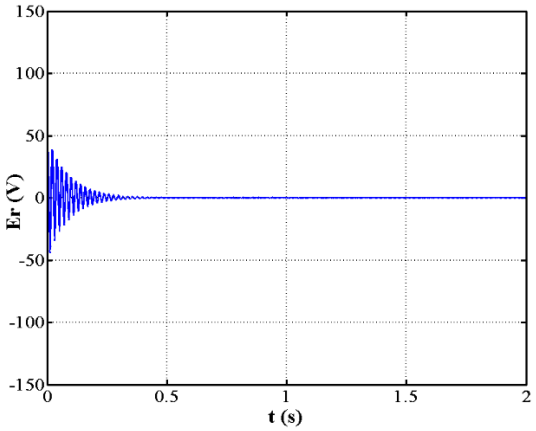


(c)

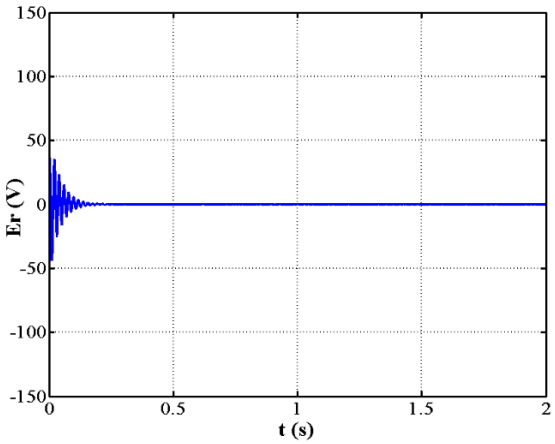
Fig. 5-13. FSTP-SQZS inverter using the proposed repetitive control scheme including $S(z)$ and K_r=0.8: (a) output phase voltage waveforms; (b) fundamental magnitude and low order harmonic distribution for phase A output voltage; and (c) error convergence process.



(a)



(b)



(c)

Fig. 5-14. Error convergence comparison for the plug-in repetitive controller with different parameters: (a) $Q(z)$=0.95, K_r=0.8, (b) Q(z) is low-pass filter, K_r=0.4, and (c) $Q(z)$ is low-pass filter, K_r=0.8.

The impact of K_r and Q(z) is analysed with the error convergence process in Fig. 5-14, where it is deduced that a higher K_r shortens the settling time, but its maximum value is restricted by the stability constraint shown in Fig. 5-8. When Q(z) is 0.95, zero steady state error cannot be achieved due to its attenuation effects on the low frequency loop gains, which finally degrades the ability for lower order harmonic rejection. Comparison between Fig. 5-14(a) and (c) reveals that $Q(z)$ significantly influences the steady-state error.

5.4.2 Experimental Results

A MOSFET based SQZS FSTP inverter is used for practical operational validation purposes. Due to the high voltage stress on the power switches in the SQZS converter (and other ISCs), the dc-link voltage and ac line-to-line peak voltage are scaled down to 40V and 32V (power rating is 200W) respectively, while the other parameters are maintained as in Table 5-1. With this arrangement, the original pole-zero positions of the SQZS converter design case are unchanged. Since the control design diagram in Fig. 5-5 has a $1/V_{dc}$ stage to normalize the converter model to unity (with 0dB open-loop gain in the baseband), the previously selected parameters for the PI controller, $S(z)$, phase-leading compensator, and the internal model ($Q(z)$ and K_r), remain valid (provided the $1/V_{dc}$ stage is included).

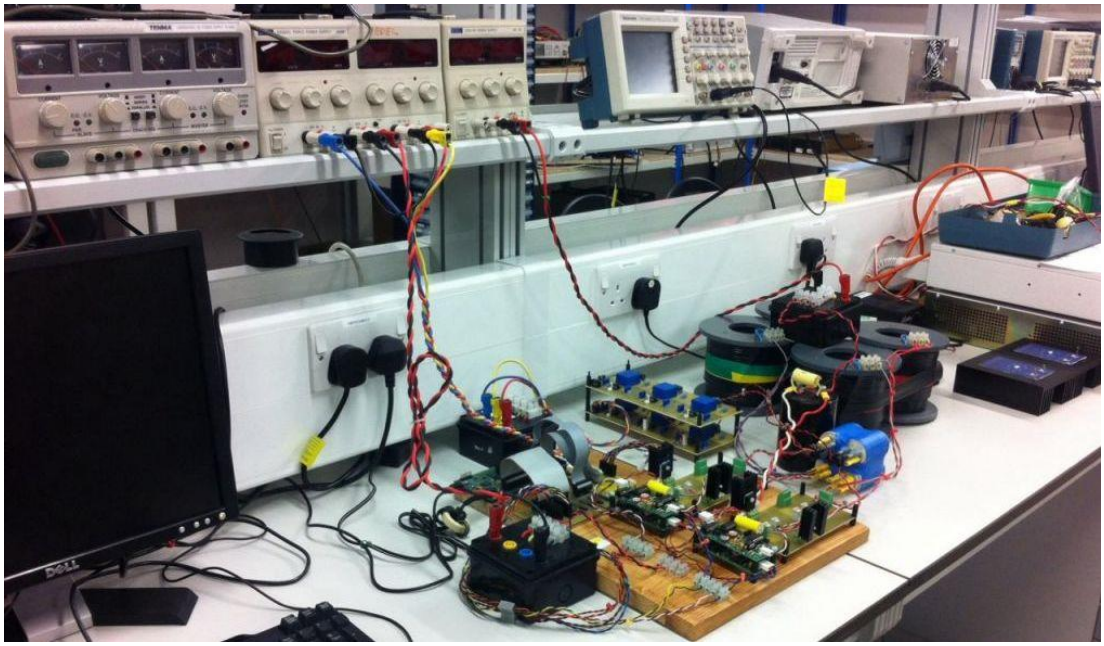
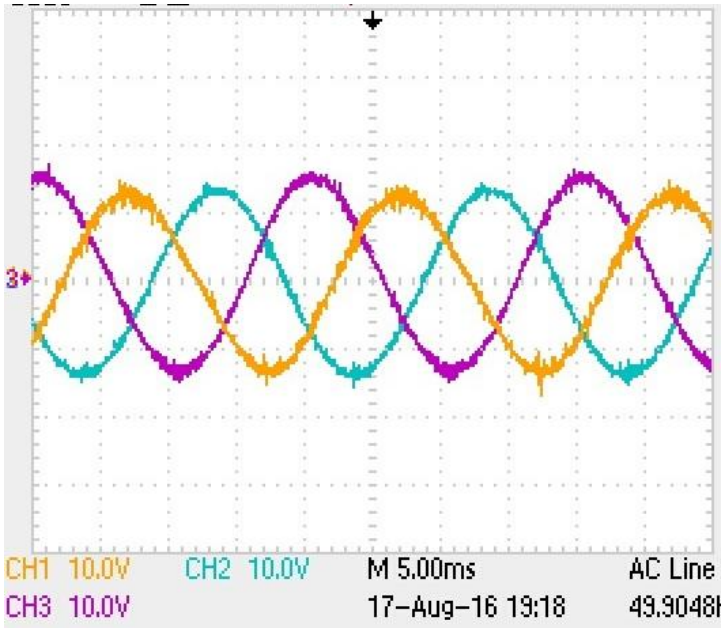
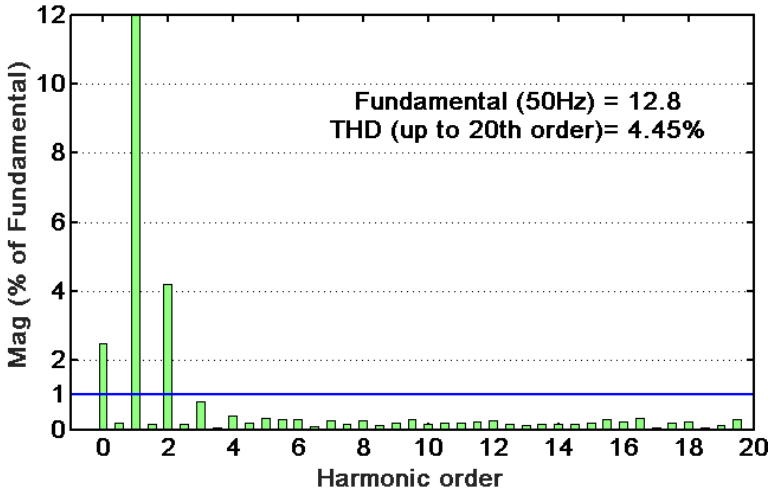


Fig. 5-15. Photograph of the experimental rig.

The control strategy of the FSTP SQZS inverter is realized in a Texas Instrument TMS320F280335 DSP platform with a sampling frequency equal to the switching frequency (30 kHz). The power switches are RFP4668PBF MOSFETs and the overall experiment setup is shown in Fig. 5-15.



(a)



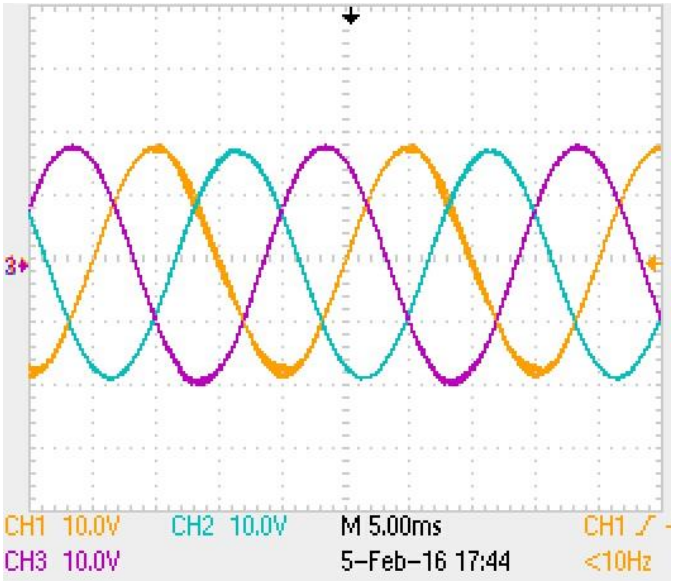
(b)

Fig. 5-16. Experimental results with conventional PI control: (a) three-phase output voltage and (b) fundamental magnitude and low order harmonic distribution for phase A output voltage.

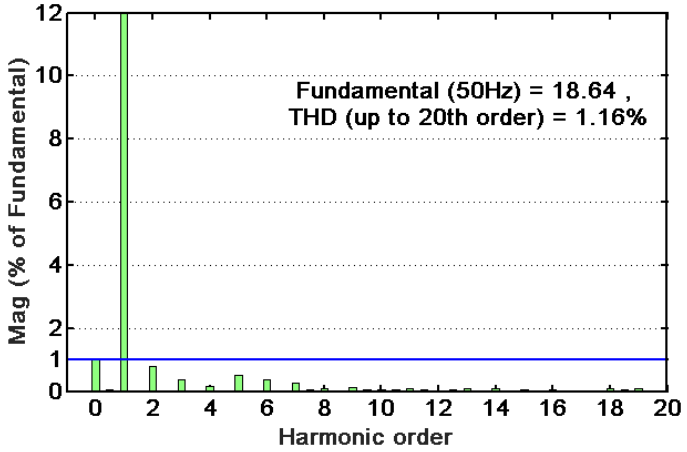
Initially, conventional PI control for the FSTP SQZS inverter is tested with the results in Fig. 5-16, where the achieved fundamental magnitude is much lower than the desired reference. Also, due to an inadequate bandwidth, the voltage waveform deviates from a pure sinusoid due to considerable 2^{nd} order harmonics.

Next, the three-phase output voltage and FFT analysis with the proposed repetitive control and 2.5Ω resistive load are given in Fig. 5-17, where all low

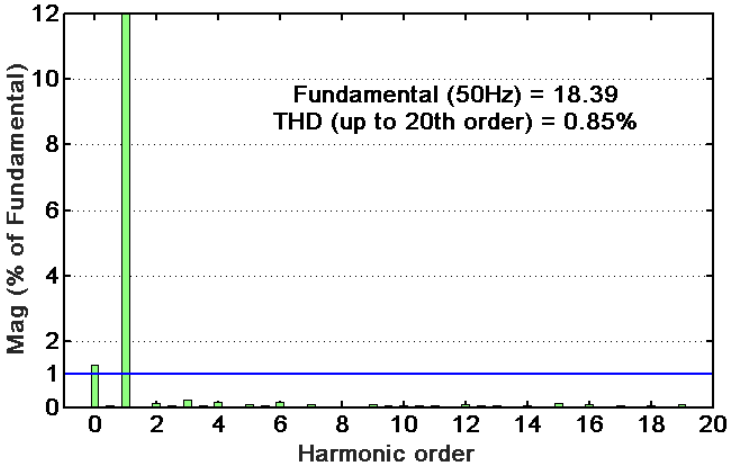
harmonic components are less than 1% of the fundamental except a residual dc component due to the transducer zero-point 1% calibration error.



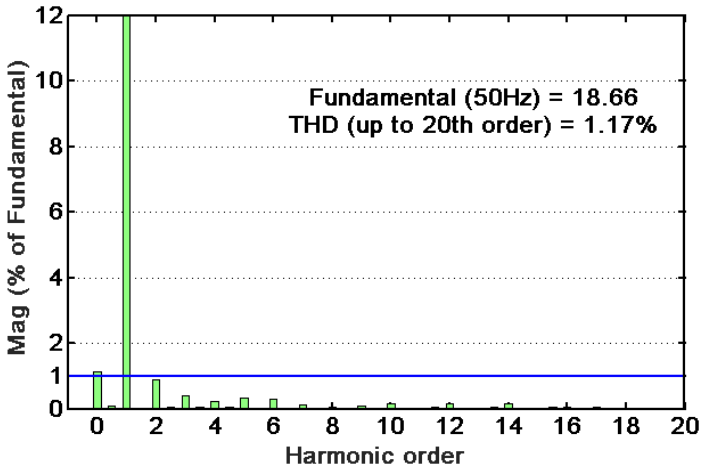
(a)



(b)



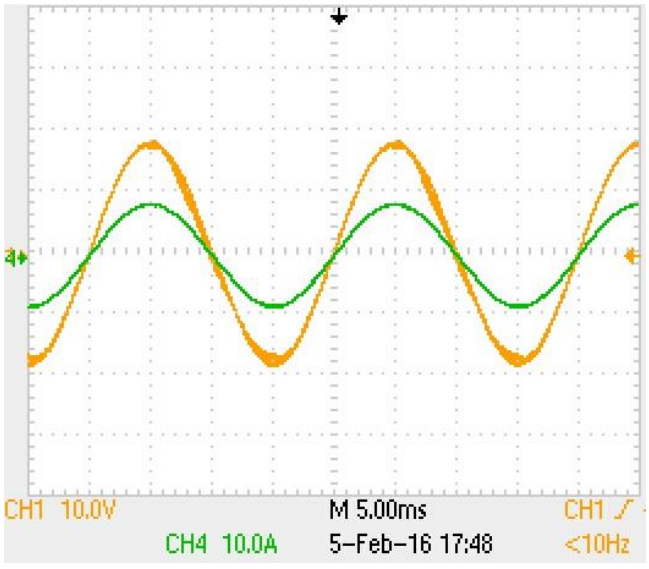
(c)



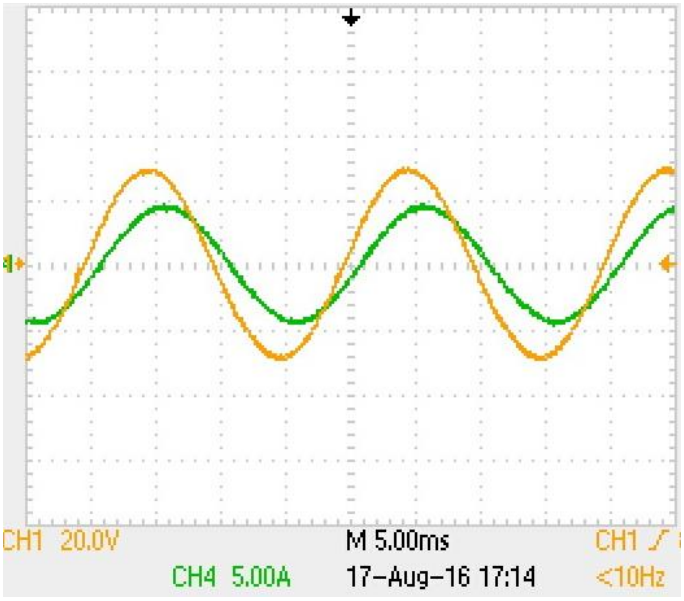
(d)

Fig. 5-17. Experiment results using proposed repetitive control strategy for FSTP-SQZS inverter: (a) three-phase output voltages; and fundamental magnitude and low order harmonic distribution for the output voltages of (b) phase A; (c) phase B; and (d) phase C.

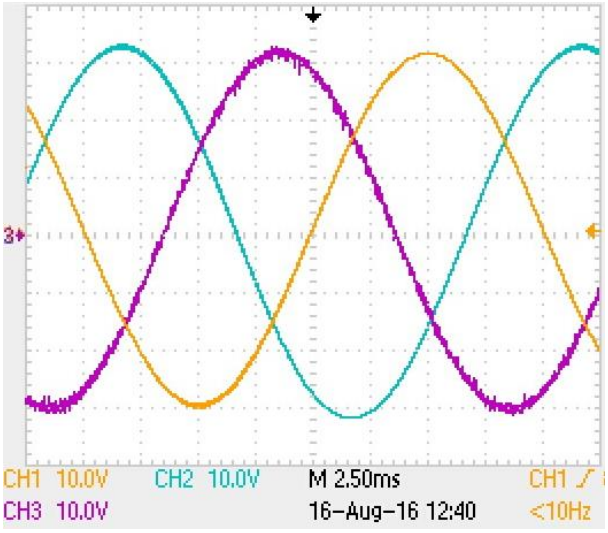
Fig. 5-18 shows the output voltage and current waveforms under different load conditions. In Fig. 5-18(a), the single-phase output voltage with 2.5Ω resistive load is displayed; and Fig. 5-18(b) shows the line-to-line voltage and line current with a 5Ω plus 10mH inductive series load. For an unbalanced load, the three-phase line-to-line voltage in Fig. 5-18(c) is able to maintain balanced; while the load current becomes unbalanced as in Fig. 5-18(d). To examine the dynamic performance of using the proposed repetitive controller, Fig. 5-18(e) demonstrates the transient performance of the SQZS inverter output voltage when the load is step changed from 6Ω to 3Ω. The converter output voltage quickly tracks the reference.



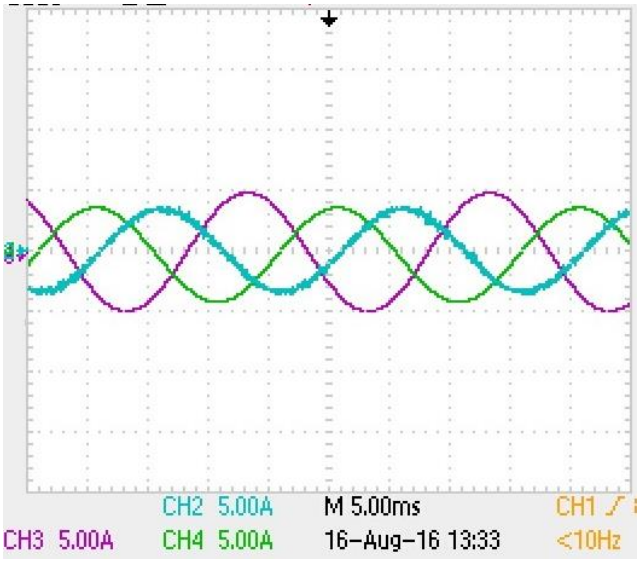
(a)


CH1 20.0V
M 5.00ms
CH1
CH4 5.00A
17-Aug-16 17:14
<10Hz

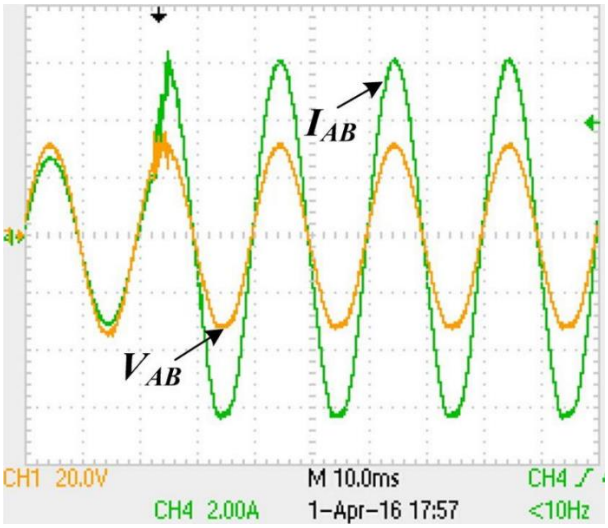
(b)


CH1 10.0V
CH2 10.0V
M 2.50ms
CH1
CH3 10.0V
16-Aug-16 12:40
<10Hz

(c)



(d)



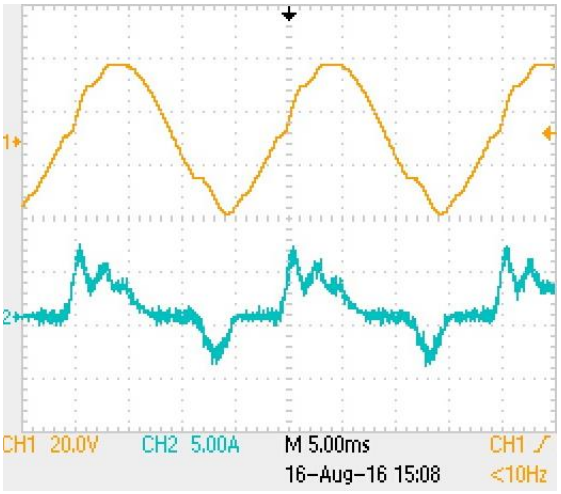
(e)

Fig. 5-18. FSTP-SQZS inverter with different load conditions: (a) phase voltage and current with 2.5Ω load; (b) line-to-line voltage and converter output current with 5Ω+10mH load; (c) balanced three-phase line-to-line voltage with unbalanced load (5.6Ω for phase A and C, 3Ω for phase B); (d) three-phase unbalanced current; and (e) voltage transient performance during load step change (6Ω to 3Ω).

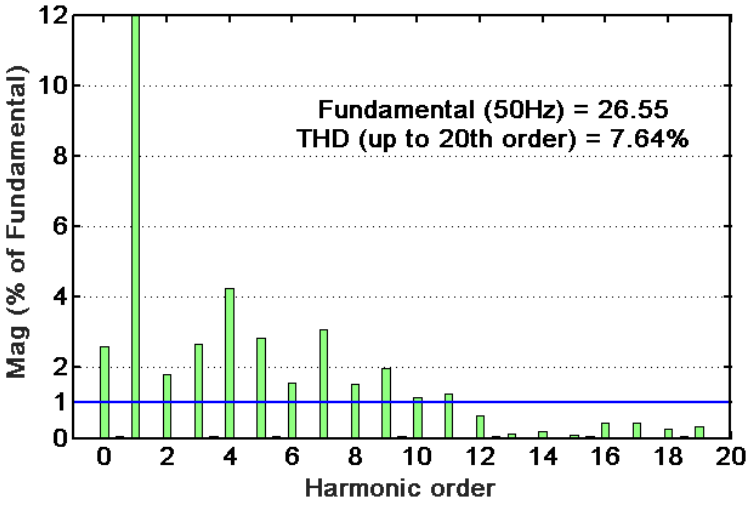
These experimental results imply that both the steady-state and dynamic performance of the SQZS inverter can be improved by using the proposed plug-in repetitive control scheme with a ZPS compensation network.

Fig. 5-19(a) and (b) show the output voltage and current waveforms of the SQZS inverter using PI control under a typical rectifier nonlinear load. Due to limited bandwidth and poor harmonic rejection ability, the output voltage deviates from its

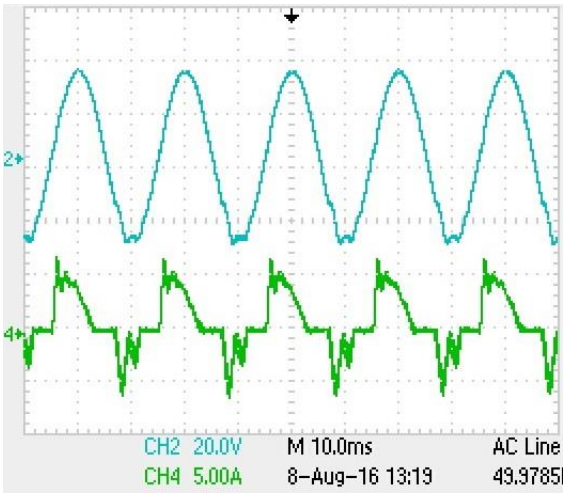
reference with inadequate fundamental component magnitude and significant low order harmonics. In Fig. 5-19(c) and (d), with the proposed repetitive control strategy, the desired fundamental magnitude is maintained, and the dominant low order harmonics are suppressed.



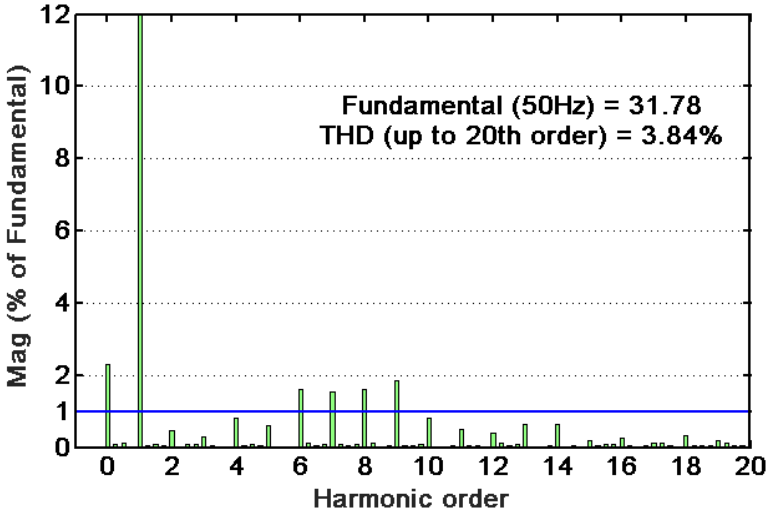
(a)



(b)



(c)



(d)

Fig. 5-19. Experiment results with a nonlinear load (diode rectifier with 300μF capacitor and 10Ω resistor): for PI control (a) voltage and current waveforms; and (b) fundamental magnitude and low order harmonic distribution; and with repetitive control (c) voltage and current waveforms; and (d) fundamental magnitude and low order harmonic distribution.

5.5 Summary

In this chapter, a generic digital plug-in repetitive control strategy has been proposed for a series of high-order wide-output range impedance source converters (HOWO-ISCs). A four-switch three-phase (FSTP) semi-quasi-Z-source (SQZS) islanded mode inverter was adopted as a representative case study. The time-variant characteristics for HOWO-ISCs with non-uniform gains in their transfer function over a fundamental period were analysed, which leads to inherent lower order harmonic distortion in the output voltage during open-loop operation.

The proposed repetitive control strategy eliminates the reference tracking error for the HOWO-ISCs using a single loop, which outperforms conventional proportional-integral (PI) and proportional-resonant (PR) methods with multiple parallel loops for suppressing all low order harmonics. In the proposed scheme, with the designed finite impulse response (FIR) zero-phase-shift (ZPS) compensator and phase-leading unit, an extended bandwidth is obtained by overcoming the initial phase-lag caused by right-half-plane (RHP) zeros. Also, the internal model of the repetitive control unit offers increased loop gain with a wide frequency range. Therefore, accurate reference tracking, fast convergence rate, and robust stability can be achieved. A design procedure for the proposed controller has been presented for a FSTP-SQZS islanded inverter, which has been validated by simulation and experimental results.

References

[1] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, G. E. Town, and S. Yang, "Impedance-Source Networks for Electric Power Conversion Part II: Review of Control and Modulation Techniques," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1887–1906, Apr. 2015.

[2] Ying-Yu Tzou, Rong-Shyang Ou, Shih-Liang Jung, and Meng-Yueh Chang, "High-performance programmable AC power source with low harmonic distortion using DSP-based repetitive control technique," *IEEE Trans. Power Electron.*, vol. 12, no. 4, pp. 715–725, Jul. 1997.

[3] P. Li, G. P. Adam, Y. Hu, D. Holliday, and B. W. Williams, "Three-Phase AC-Side Voltage-Doubling High Power Density Voltage Source Converter With Intrinsic Buck–Boost Cell and Common-Mode Voltage Suppression," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5284–5298, 2015.

[4] A. Darwish, A. M. Massoud, D. Holliday, S. Ahmed, and B. W. Williams, "Single-Stage Three-Phase Differential-Mode Buck-Boost Inverters With Continuous Input Current for PV Applications," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8218–8236, Dec. 2016.

[5] M. S. Diab, A. Elserougi, A. M. Massoud, A. S. Abdel-Khalik, and S. Ahmed, "A Four-Switch Three-Phase SEPIC-Based Inverter," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4891–4905, 2015.

[6] J. Knight, S. Shirsavar, and W. Holderbaum, "An improved reliability cuk based solar inverter with sliding mode control," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 1107–1115, Jul. 2006.

[7] Keliang Zhou and Danwei Wang, "Digital repetitive learning controller for three-phase CVCF PWM inverter," *IEEE Trans. Ind. Electron.*, vol. 48, no. 4, pp. 820–830, Aug. 2001.

[8] Kai Zhang, Yong Kang, Jian Xiong, and Jian Chen, “Direct repetitive control of SPWM inverter for UPS purpose,” *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 784–792, May 2003.

[9] Y. Cho and J. Lai, “Digital Plug-In Repetitive Controller for Single-Phase Bridgeless PFC Converters,” *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 165–175, Jan. 2013.

[10] M. Zhang, L. Huang, W. Yao, and Z. Lu, “Circulating Harmonic Current Elimination of a CPS-PWM-Based Modular Multilevel Converter With a Plug-In Repetitive Controller,” *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 2083–2097, Apr. 2014.

[11] L. He, K. Zhang, J. Xiong, and S. Fan, “A Repetitive Control Scheme for Harmonic Suppression of Circulating Current in Modular Multilevel Converters,” *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 471–481, Jan. 2015.

[12] S. Sajadian and R. Ahmadi, “Model Predictive Control of Dual-Mode Operations Z-Source Inverter: Islanded and Grid-Connected,” *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 4488–4497, May 2018.

[13] D. Cao, S. Jiang, X. Yu, and F. Z. Peng, “Low-Cost Semi-Z-source Inverter for Single-Phase Photovoltaic Systems,” *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3514–3523, Dec. 2011.

[14] H. L. Broberg and R. G. Molyet, “A new approach to phase cancellation in repetitive control,” in *Proceedings of 1994 IEEE Industry Applications Society Annual Meeting*, 1994, vol. 2, pp. 1766–1770 vol.3.

[15] A. Garcia-Cerrada, O. Pinzon-Ardila, V. Feliu-Batlle, P. Roncero-Sanchez, and P. Garcia-Gonzalez, “Application of a Repetitive Controller for a Three-Phase Active Power Filter,” *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 237–246, Jan. 2007.

[16] Keliang Zhou and D. Wang, “Digital repetitive controlled three-phase PWM rectifier,” *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 309–316, Jan. 2003.

CHAPTER 6 Conclusions

6.1 General Summary

As an energy source with infinite reserve, solar energy is a demanded topic in academia and industry to help solve the global fossil fuel energy crisis. Large scale grid integrated PV power systems are the main player in the global electricity market. To increase the energy conversion efficiency in conventional centralised PV systems, implementation of distributed maximum power point tracking approaches is a promising solution. High equipment cost is the main barrier for the development of conventional large scale DMPPT PV systems. To implement DMPPT technologies efficiently in large scale PV systems, some general problems have been analysed, and present solutions have been reviewed. In this thesis, a novel DMPPT architecture with partial power processing converters was presented, with a distributed control strategy for better balance between cost and efficiency.

Impedance source converters with voltage boosting ability are widely used in PV systems. A general problem is the low order distortion when applied in ac applications. Another topic in this thesis is the application of plug-in repetitive control to solve this general problem.

Chapter one presented background to the development of photovoltaic renewable energies around the world. The state-of-the-art PV technologies, especially for the PV materials, were reviewed and compared. New PV materials are waiting to help improve competitiveness for PV electricity in the global market. Grid integrated PV systems are the main player in the PV industry and can be classified by different standards such as by power level, inverter type, and MPPT implementation. The future trend is to deploy MPPT with finer granularity which means research is needed at the

module level and even cell level DMPPT architectures. The main challenges for wider deployment of PV generators were presented and thesis research objectives were listed.

Chapter two reviewed conventional distributed maximum power point tracking architectures for which full power processing PV module integrated converters are used. PV module integrated converters are categorised into two types according to the converter power portion processed. The different architectures can be further divided according to the connection types.

Compared with the partial power processing conversion type, the full power processing conversion type is more readily controlled and many mature architectures have been previously designed. The most important international standards and requirements for grid-integrated PV power systems were discussed, including possible influences on normal operation of the utility grid. Based on these requirements, a set of typical parallel connected micro-inverter topologies and series connected module converter topologies were reviewed. For single phase PV applications, parallel connection types are widely used, and the issue of power decoupling was analysed. Isolated topologies can provide adequate amplification for low PV voltage and avoid grounding issues. Many novel transformerless step-up topologies have been introduced in the past to pursue higher efficiency and lower cost. Typical representative transformerless converters were compared. For series connected module level PV systems, cascaded dc-dc and dc-ac converters are mainly applied in higher voltage level three-phase or single-phase PV systems. Control features and MPPT implementation have also been discussed. All the converters reviewed must deal with all the power generated by the PV modules which is the main reason for high equipment cost in these conventional DMPPT architectures.

The operation principles of impedance source converters have also been reviewed. The main constraints for higher order wide output ISCs were discussed. To solve the general problem for controller design for this type of converters, a repetitive control strategy is given in chapter five of the thesis.

Chapter three reviewed typical partial power processing DMPPT architectures. The non-linear output characteristic of PV cells is analysed with mathematical illustration. Then the mismatch loss mechanism is illustrated for series and parallel connected PV cells to highlight the necessity for a distributed MPPT design. The main

MPPT techniques used in mismatched conditions were compared and the main goal was to comprehensively review three different partial power processing MPPT architectures.

The concept of partial power processing DMPPT is discussed and architectures based on this concept were reviewed. These existing architectures are classified into two groups according to their balancing differential converters. The main drawback is an inverter per string structure which hampers scalability and cost reduction.

Chapter four introduced a novel DMPPT architecture based on only partial power processing converters. By combining voltage and current balancers in one PV string, the per PV string per central converter configuration is avoided. Thus, several parallel connected PV strings can be integrated onto ac grid via one central inverter. The possible converters which can be utilized as auxiliary processors were reviewed in terms of the required connecting types. No mismatch - no power processing has been realized with a distributed control strategy. A developed EMT model is used for performance evaluation. The simulation results verified the proposed novel architecture, which shows satisfactory DMPPT ability.

Chapter five investigated controller design for impedance source converters with high-order wide-output features. Compared with conventional two-level converters, these high order converters have advantages when applied in PV inverters to achieve voltage boosting with either output voltage polarity. Improved dc-link voltage utilization is anticipated. The intrinsic passive impedance network within this kind of converter imposes low order distortion of the ac output power which gives rise to control difficulties. A generic plug-in digital repetitive control scheme was presented for HOWO-ISCs to solve the prominent second harmonic problem. The islanded mode is selected as the case in this chapter to implement the proposed control methodology. Simulation and experimental validation of a topology based on a semi-quasi Z source converter establishes accurate reference tracking, fast dynamic response, and enhanced robustness.

6.2 Author's contribution and future research plan

The main contribution and significance of this thesis can be summarised as:

- A novel DMPPT architecture was presented to realize module level MPPT with only partial power processing converters. For each PV string, the string inverter is replaced by a voltage balancing converter with a reduced power rating. Several PV strings can be parallel connected to one central inverter for expanded power scalability. Distributed control and MPPT are realized.
- A modified generic digital control method was developed for impedance sourced converters which can be used in PV applications for their voltage boosting abilities. The low order harmonic problems were solved with simulation and experimental verification.

Based on the achieved research, some recommendations for future research are:

- The family of impedance source converter usually suffers from high voltage stress on a single switch, and a sufficiently high switching frequency is needed to achieve a wide control design flexibly such as the repetitive controller. These imply that the silicon power switches will incur relatively high losses. Future approaches will be adopting the silicon carbide MOSFET to boost the power efficiency of such converters, and its grid-connection mode will also be tested.
- Analysis of incorporating energy storage devices into the proposed DMPPT architecture and experimental testing, can be carried out. Additionally, the system performance can be evaluated if the DMPPT partial power converters are applied and integrated in at PV cell level.

Appendices

Appendix A. Test Rig Details for FSTP-SQZS Inverter

I. The DSP control system

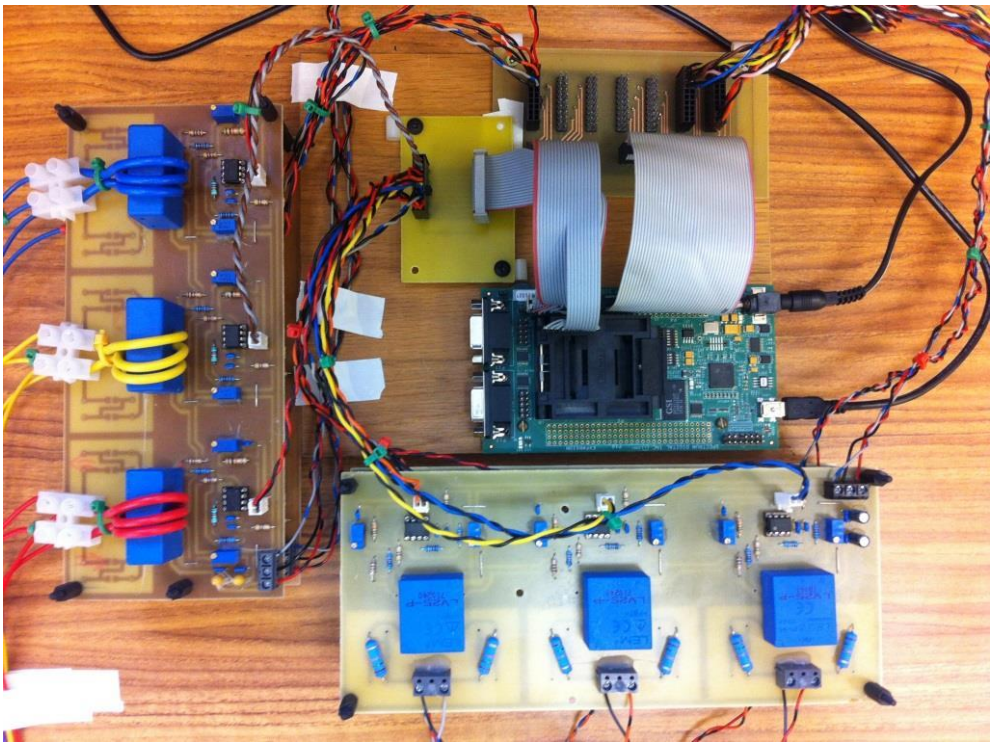


Fig.A-1. The TMS320F28335 DSP platform.

As in Fig.A-1, the Texas Instrument (TI) TMS320F28335 is adopted to implement the plug-in repetitive control method and generate the PWM signals for the FSTP-SQZS inverter.

II. The sensor system

The voltage and current sensor boards are shown in Fig.A-2 and Fig.A-3, respectively. For the voltage transducer, the measurement resistance R-meas should be in the range of 100 to 350 ohms for a DC circuit supply of ±15V. A value of 150 ohms ± 1% is used. The transducer primary current is taken as 10mA by selecting suitable resistors. While for the current transducer, the measurement resistance R-meas should be in the range of 50 to 150 ohms for a DC circuit supply of ±15V, and a value of 100 ohms ± 1% is a used. A signal calibration circuit in Fig.A-4 based on the op-amp NE5534 is employed on both boards following the transducer outputs.

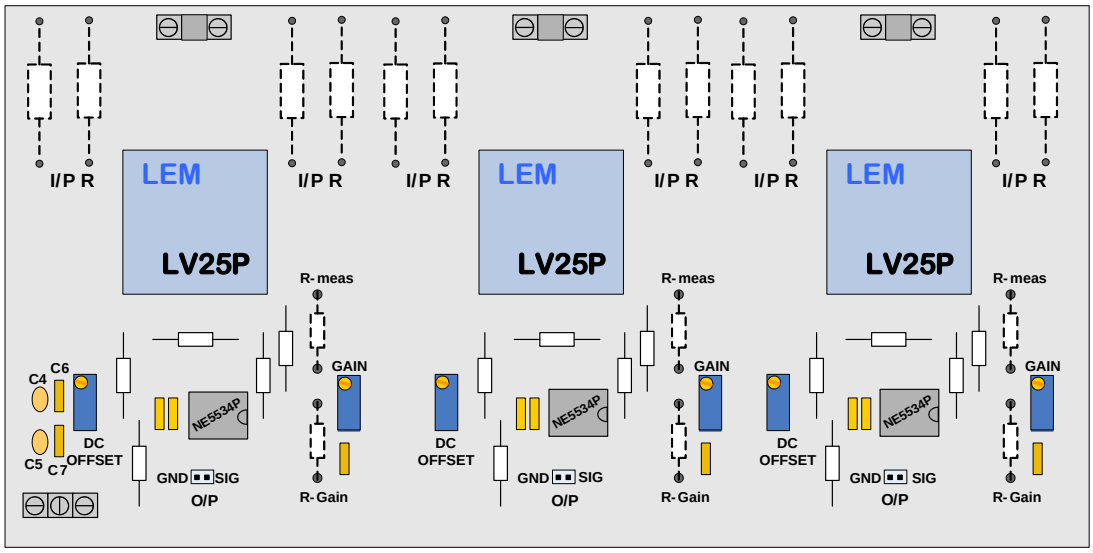


Fig.A-2. LV25P voltage transducer and signal calibration board (2 out of 3 channels are used).

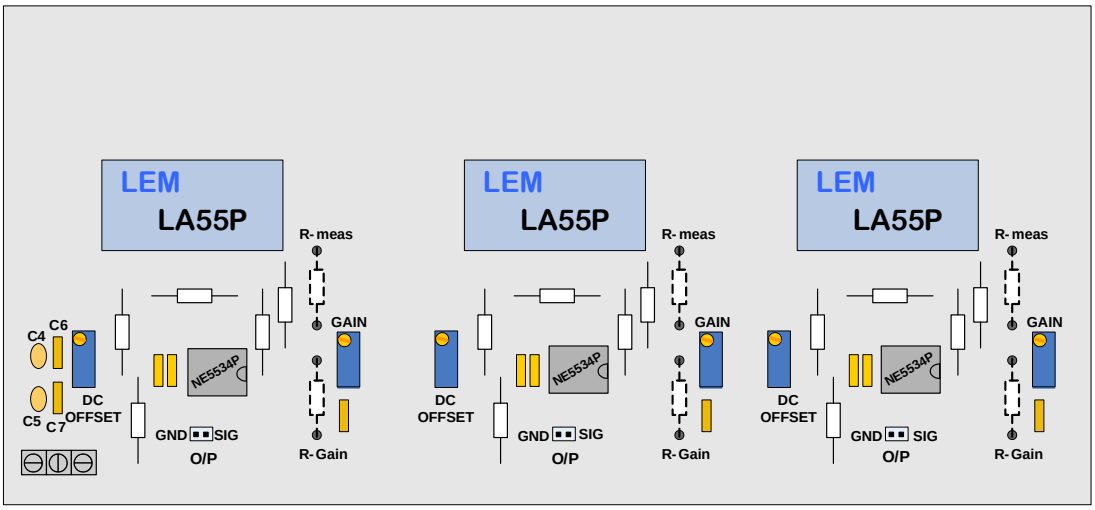


Fig.A-3. LA55P current transducer and signal calibration board (2 out of 3 channels are used).

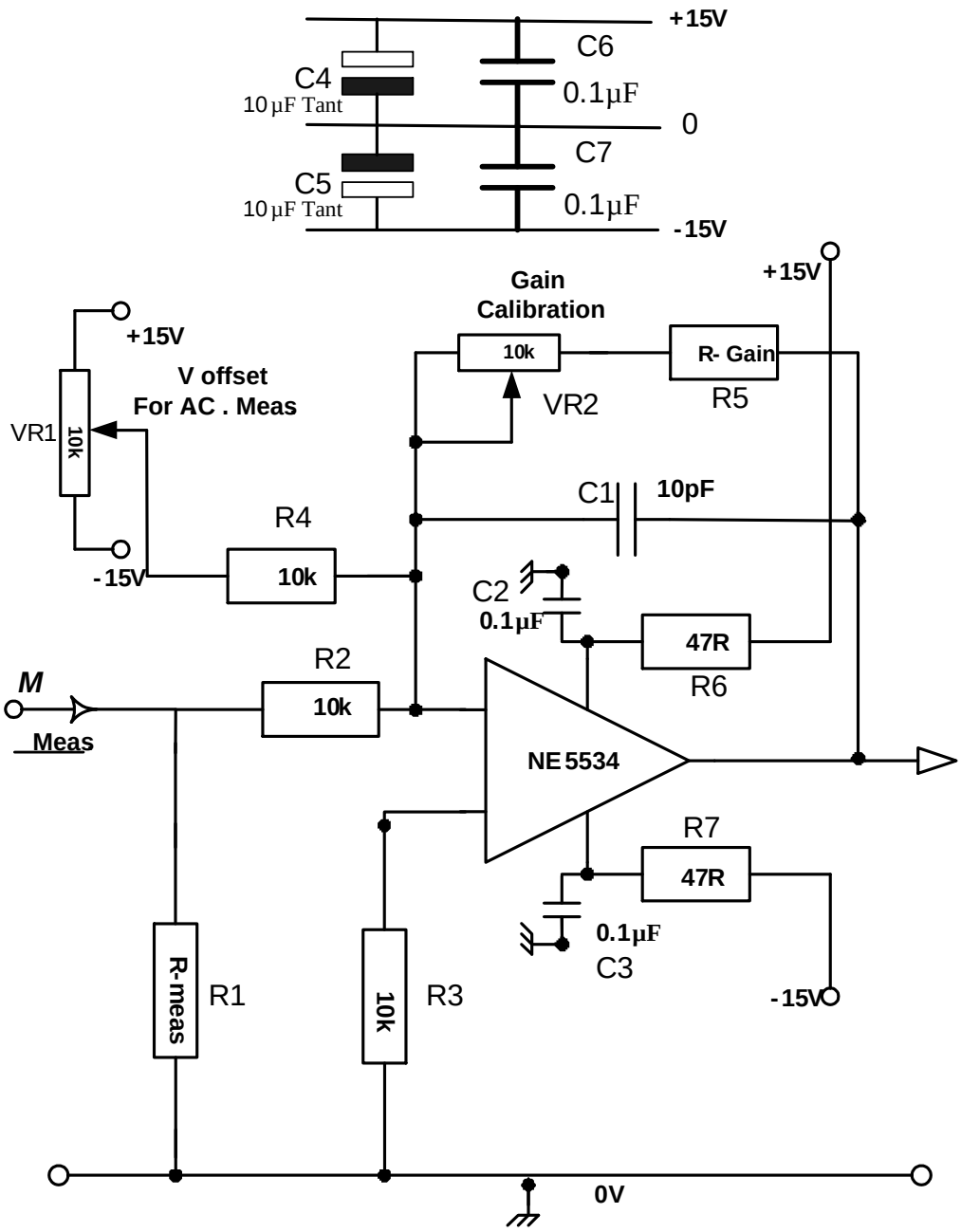


Fig.A-4. Amplifier circuit for signal calibrations in both transducer boards.

III. The overall setup of test rig

Fig.A-5 shows the overall test rig for the FSTP-SQZS inverter with plug-in repetitive control strategy. It consists of:

- TMS320F28335 DSP controller
- Two SQZS inverter legs with impedance source networks
- Common DC-link capacitor

- Gate drivers
- Voltage and current transducer
- Resistive and diode-rectifier loads
- Auxiliary voltage source

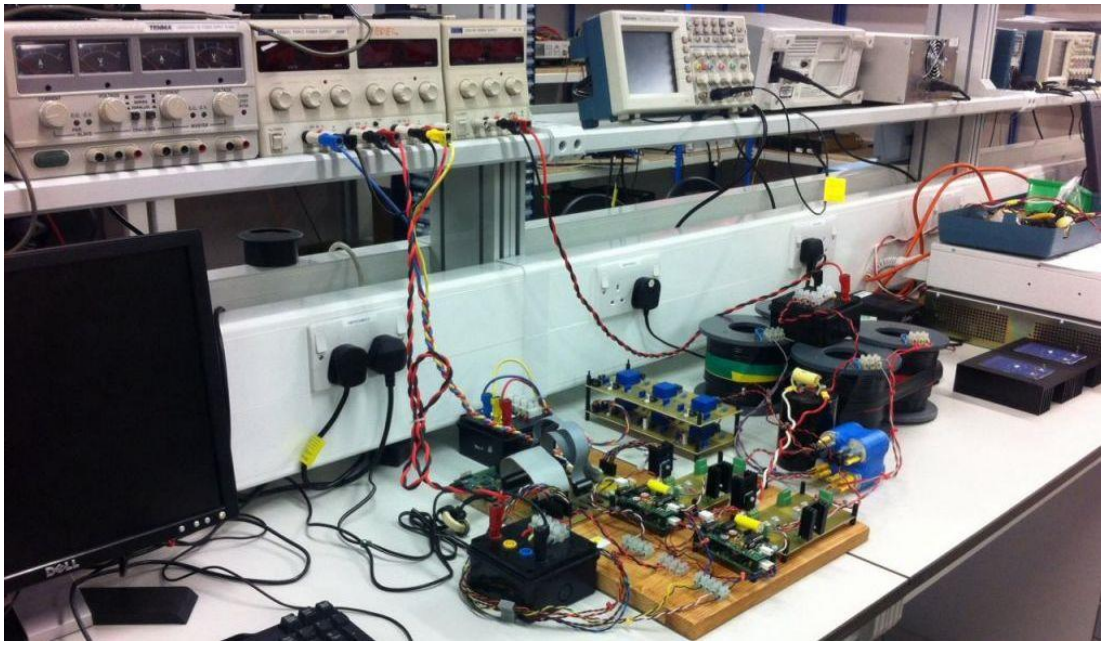


Fig.A-5. The photo of the test rig for FSTP SQZS inverter.

Appendix B. Sample Code for Verifications

The EMTP model for buck-boost converters in a PV string

```
function [Vcx,Vc,iL,Power] = DMPP(Vc_t,iL_t,dt,cap,ind,Ron,Roff,g,Io,ipv) % Vc_t is the previous value of each PV panel, Io is total output current = imain(1)

N = length(ipv);

% N PV modules in series, from top to bottom, noted as 1 - N
%     1
%     2
%     3
%     ...
%     N-2
%     N-1
%     N
% the 1st panel is the input of a buck-boost differential power regulator with its output into panel 2
% then, panel 2 is the input of another buck-boost feeding panel 3
% .....
% finally, the N-1 is the input of last buck-boost compensating panel N
% the left uncompensated panel (panel 1 in previous settings) is controlled by an extral
% central converter or balancer (partial power)


icomp = zeros(1,N);  % icomp is the input compensation current contributed by previous buck-boost differential power regulator
                % so, icomp(1)always 0
                % positive direction is flowing into PV panels

imain = zeros(1,N); % positive direction defined from bottom to top, imain(1) equals to output current to the external dc-dc, Io

Vc = zeros(1,N); % Vpv

% ipv = zeros(1,N);  direct output current of PV panels, from bottom to top

iL = zeros(1,N-1); % buck-boost inductor current, iL(N) is always 0, positive direction is flowing into PV panels

Rsw1 = zeros(1,N-1); % resistance of input side switch in the buck-boost

Rsw2 = zeros(1,N-1);

Power = zeros(1,N); % power output of each PV panel

Vx = zeros(1,N-1);

Vcx = zeros(1,N);

%*****************
icomp(1) = 0; % just emphasize, no actural change after initilization of icomp=zeros(1,N)
imain(1) = Io;
% Vc(1) = 30.7*3;



for ii = 1:N-1
```

```
   % ipv(ii) = Vc_t(ii); % PV modeing function %*****************************%

    Rsw1(ii) = g(ii)*Ron+(1-g(ii))*Roff; % if g(ii)==1...

    Rsw2(ii) = (1-g(ii))*Ron+g(ii)*Roff; % if g(ii)==1...

    Vx_temp = (Vc_t(ii)/Rsw1(ii)-Vc_t(ii+1)/Rsw2(ii)-iL_t(ii))/(1/Rsw1(ii)+1/Rsw2(ii));

    iL(ii) = iL_t(ii)+dt/ind*Vx_temp; % backward

    icomp(ii+1) = (Vx_temp+Vc_t(ii+1))/Rsw2(ii);

    imain(ii+1) = Io+icomp(ii+1); %imain(ii)+icomp(ii+1)-icomp(ii);%imain(ii)+icomp(ii+1)-
icomp(ii);

    ic_temp = ipv(ii)-imain(ii)-(Vc_t(ii)-Vx_temp)/Rsw1(ii); % capacitor current only stored
temporarily

    Vc(ii) = Vc_t(ii)+dt/cap*ic_temp; % backward

    Vcx(ii) = Vc(ii)+ic_temp*0.01;

    Power(ii) = Vcx(ii)*ipv(ii);

    Vx(ii) = Vx_temp;

end

%ipv(N) = Vc_t(N); %*************************PV model

Vc(N) = Vc_t(N)+dt/cap*(ipv(N)-imain(N));

Vcx(N) = Vc(N)+ic_temp*0.01;

Power(N) = Vcx(N)*ipv(N);
```

Appendix C. Perturb and Observe or Hill-Climbing algorithm

The power and voltage relationship of a typical PV module is shown in Fig.A-6. The peak power needs to be found with a MPPT algorithm. Perturb and observe (P&O) or so called hill-climbing method is based on observation of the P-V curve. When the PV module operating point is at the left of the MPP, the output voltage or current needs to move up-right to the MPP as shown in Fig.A- 6. Otherwise, the operating point needs to move in the up-left direction. The final objective is to set the output power at the maximum point.

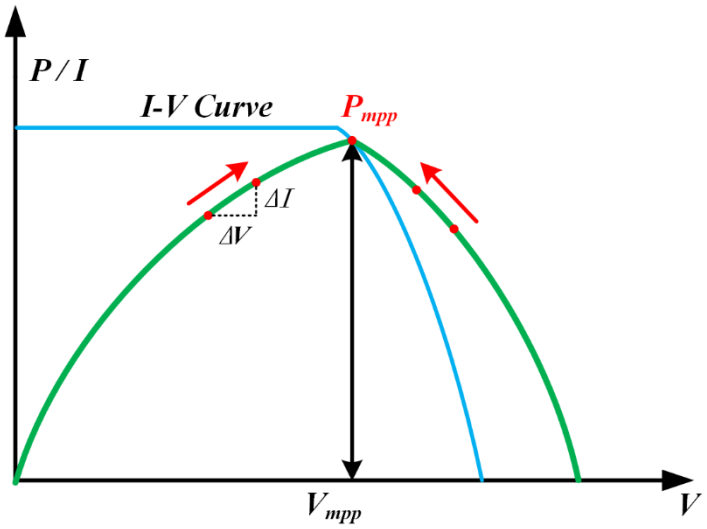


Fig.A- 6 Power-voltage curve of a PV module.

To implement P&O in a PV system, sensors are required to measure the PV module output voltage and current at specified time intervals. Then the calculated power and present voltage or current are compared with the previous values. The operation mechanism is described by the following equations.

A fixed perturbation value ΔV is defined previously according to system features. If the measured power is larger than the previous power value and the PV voltage is larger than the previous voltage measurement; then the operation point is at the left of the MPP, hence the reference voltage to the controller is achieved by adding the perturb value ΔV. The other conditions can be derived similarly.

$$V_{PV}^{*}(t) = V_{PV}(t - \Delta t) + \Delta V \quad (1)$$

$$\left.\begin{matrix} P_{PV}(t) > P_{PV}(t-\Delta t) & V_{PV}(t) > V_{PV}(t-\Delta t) \\ P_{PV}(t) < P_{PV}(t-\Delta t) & V_{PV}(t) < V_{PV}(t-\Delta t) \end{matrix}\right\}$$

$$V_{PV}^{*}(t) = V_{PV}(t-\Delta t) - \Delta V$$

$$\left.\begin{matrix} P_{PV}(t) > P_{PV}(t-\Delta t) & V_{PV}(t) < V_{PV}(t-\Delta t) \\ P_{PV}(t) < P_{PV}(t-\Delta t) & V_{PV}(t) > V_{PV}(t-\Delta t) \end{matrix}\right\} \quad (2)$$

The reference voltage V_{PV}^{*} is given to a control loop to adjust the PV module output voltage and usually a PI controller is used. Another direct method is to oscillate the converter duty cycle for fast tracking P&O. The PV converter duty cycle is increased or decreased at a specific perturbation value according to the *P-V* characteristics. The main problem for P&O is confliction between fast tracking and steady state oscillation. Large perturb values mean a faster MPPT tracking speed which is desirable for PV with an intermittent nature. However, lower steady state oscillation needs smaller perturbation for higher PV efficiency. There is a trade-off between dynamics and steady state operation for P&O algorithms.

From Fig.A- 6, the rate of PV power variation decreases while the operation point approaches the MPP. To improve fixed P&O performance, several adaptive P&O strategies have been proposed. The main concept is to adjust the perturb value according to the power change rate for fast tracking at large power varying conditions. When the MPP is achieved, the active P&O decreases the perturb value to reduce steady state oscillations. By using adaptive P&O, a generic design frame can be established without dependence on a specific PV system feature.

At present, P&O based MPPT is the most widely used commercial technique for simplicity and ease of implementation. Different methods have been analysed to realize adaptive tracking for better performance.

Appendix D. List of Figures

Appendix E. List of Tables

Appendix F. Publication Output

Journal Publications

1. **Y. Wang**, A. Darwish, D. Holliday and B. W. Williams, "Plug-In Repetitive Control Strategy for High-Order Wide-Output Range Impedance-Source Converters," in IEEE Transactions on Power Electronics, vol. 32, no. 8, pp. 6510-6522, Aug. 2017, doi: 10.1109/TPEL.2016.2615689.

   Abstract: High-order wide-output (HOWO) impedance-source converters (ISCs) have been presented for ac inverter applications that require voltage step-up ability. With intrinsic passive impedance networks as energy sources, these converters are able to achieve voltage boosting with either polarity, leading to improved dc-link voltage utilization compared with the conventional two-level converter. However, HOWO-ISCs suffer from transfer functions giving low bandwidth, a penalty of increased passive devices and right-half-plane zeros, which result in lower order distortion of the ac output power. In this paper, a modified plug-in repetitive control scheme is presented for HOWO-ISCs with accurate reference tracking (hence low distortion), fast dynamic response, and enhanced robustness. By using zero-phase-shift finite impulse response filters in both the internal model of the repetitive controller and its compensation network, the proposed method achieves zero steady-state error and an extended closed-loop bandwidth. For HOWO-ISC cases, this method outperforms conventional proportional-integral (PI) control, which has considerable steady-state error. It also eliminates the need of parallel loops for several frequencies when proportional resonant control or orthogonal transformation-based PI schemes are used to remove lower order distortion. The design process and performance analysis of the proposed repetitive control strategy are based on a novel three-phase HOWO-ISC configuration with a reduced number of switches. Simulation and experimental results confirm the feasibility and effectiveness of the proposed control approach.

Conference Papers

2. **Yachao Wang,** D. Holliday and B. Williams, "Parallel Connected D-MPPT Architecture for PV System with Partial Power Processing Converters," in 9th

IET International Conference on Power Electronics, Machines and Drives (PEMD), pp. 1-5, Liverpool, 17-19, Apr. 2018.

Abstract: This paper proposes a new photovoltaic energy conversion architecture that can achieve distributed maximum power point tracking (D-MPPT) with only partial power processing converters. Featuring both the voltage and current compensation abilities, the per module per MPPT structure has been obtained without involving full power processing central converters. A flexible higher dc voltage power interface to the inverter stage or other dc power network is achieved with flexible plug-and-play performance for the streaming power conversion units. Based on the 'no mismatch, no processing' principle, a cost reduction can be expected with lower electrical rating and smaller size for the PV module integrated converters (MIC). The power balancing principle, MIC operating mechanism, control strategy and performance evaluation are analysed. Simulation results verify the feasibility of the proposed approach.

3. A. Darwish, **Yachao Wang**, D. Holliday and S. Finney, "Operation and control design of new Three-Phase inverters with reduced number of switches," 2016 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), Anacapri, 2016, pp. 178-183, doi: 10.1109/SPEEDAM.2016.7525993.

   Abstract: DC/AC inverter topologies having reduced numbers of switches to reduce costs, total inverter size and switching losses have previously been proposed. In addition, these topologies reduce the likelihood of semiconductor switch damage, and have lower common-mode currents. This paper proposes new designs for inverters with reduced switch numbers. For three-phase systems, the proposed inverters use four switches instead of the six used in the traditional three-phase Voltage Source Inverter (VSI). Compared to the traditional Four-Switch Three-Phase (FSTP) inverter, the proposed FSTP inverters improve the voltage utilisation factor of the input dc supply, without the need for triplen injection. Sliding-mode control is used to demonstrate the dynamic response and robustness of the inverters. Also the paper presents new single-phase inverters with two switches instead of the four used in the traditional VSI. The capability of suppressing the 2nd order current harmonic from the input dc side is discussed.

The basic structures of the proposed inverters and their operation, switch ratings, controller design with supporting mathematical equations, and MATLAB/SIMULINK results are presented. Practical results, based on laboratory prototype circuitry controlled using a Texas Instruments TMSF280335 DSP, are presented to demonstrate the design flexibility and operation of the proposed topologies.