University of Strathclyde
Department of Electronics and Electrical Engineering

Toroidal Field Power Supply for the Spherical Tokamak Power Plant

Ziyad M. Shafik
B.Sc, M.Sc

A thesis presented in fulfilment of the requirements for the Degree of Doctor of Philosophy.

2011

Acknowledgement

Completing a PhD is a lengthy journey. I would not have sanely succeeded without the invaluable support, guidance, patience and encouragement of my supervisors, Prof. B. W. Williams and Dr. S. J. Finney.

Gratitude must be also given to the Strathclyde University academic members and technical staff for their continuous support and assistance during the different stages of my PhD. Sincere acknowledgements is given to Dr. John Fletcher for providing the cryogenic testing equipment used as part of my experimental testing. Special appreciation is also given to Dr. T C. Lim for the long discussions during my experimental tests, and undeniably to Mr. Charles Croser for his efforts and help in implementing my main test rig.

I would also like to give my special thanks to Dr. Ahmed Massoud for his constant encouragement during my first year, Dr. Mahmoud Masoud for his support during my third year, and Dr. Khaled Hany for his patience during my writing up year.

My endless indebtedness and love goes to my mother for her continuous support and reassurance, not forgetting my brother and sister.

My final acknowledgments go to Culham Science Centre for funding this research programme, and for the numerous personnel I got to meet during my visits to Culham, especially John Hay and Stephen Shaw.

Dedication

To the memory of my father …

Table of Contents

Abstract

This thesis studies the realisation of a high-current low-voltage DC power supply, for supplying the spherical tokamak power plant toroidal field coils, with a total current of 32 MA at 8V. The system is required to provide high efficiency conversion, high reliability, and a reduced footprint.

Conventional rectification, adopting diodes, fails to provide high efficiencies, due to the relatively increased voltage-drop to output-voltage ratio at low output voltages, caused by the high nominal forward voltage of diodes. The rectifier circuit topology also affects the conversion efficiency. Topologies employing one rectifying switch per path are preferred. Supply frequency step-down transformers, as well as filtering components are considered the bulkiest system elements. Hence, utilising a high frequency conversion stage is preferred for obtaining a reduced converter footprint. A double-stage AC/DC converter system is selected, with parallel connected high frequency DC/DC converters at the final stage, namely ZVS phase-shift PWM DC/DC converters as a base design, to achieve the final current rating requirement. The converter utilises synchronous rectification, to improve the efficiency of the output low-voltage rectifying stage.

A lab-scaled converter, to study the performance of the selected topology, is presented. The DC/DC converter delivers 1 kA at approximately 8V, is supplied from a 600 V DC supply, and utilises the lowest loss system components. The ZVS MOSFET inverter loss, operating at 14 kHz, is predominantly resistive/conduction losses. A nanocrystalline transformer core is adopted, to provide a highly efficient magnetic conversion. A control-driven synchronous rectifier is used for the final stage, with improved control over self-driven techniques, increasing the rectification efficiency. Liquid nitrogen cooling is investigated to possibly reduce the on-resistance of MOSFET devices. Finally, a scaled-up 10 kA module design is discussed, with a possible modification to the presented system. Chip-level MOSFET paralleling is realised for reducing the difficulties of paralleling a large number of devices. Common current reference control, for the parallel converter operation, is presented, and shows the effectiveness for providing balanced current sharing in case of different converter parameters.

Preface

High-current low-voltage rectifiers are employed in applications such as linear regulator circuits used for microprocessor and telecommunication systems, automotive power supplies, electrolytic applications, lead acid battery charging systems, particle accelerators, and various applications adopting superconducting magnets. Fusion reactors are recently added to such applications, with the highest current requirements of all applications. This research aims at selecting the most suitable power supply system topology, for a fusion power plant, requiring a total DC current of 32 MA, at approximately 8 V.

The thesis is presented in eight chapters:

Chapter one gives an introduction to fusion energy, showing the basic design aspects of the spherical tokamak power plant. Similar applications utilising high-current low-voltage power supplies are reviewed, to select a suitable power supply topology for this specific application. A double stage conversion process is chosen, comprising a conventional high voltage diode rectification, followed by parallel connected DC/DC converter modules, adopting low-voltage synchronous rectification.

Chapter two starts with the theory of operation, design procedures, and power loss analysis associated with ZVS phase-shift PWM converters. A design outline for a lab-scaled converter is presented, aided with simulation results.

Chapter three investigates the possible efficiency improvement of applying liquid nitrogen cooling to MOSFET devices, since MOSFETs are utilised in the inverter and rectifier sides. Basic theoretical analysis justifying the reasons of device channel on-resistance reduction at cryogenic temperatures is presented. Experimental testing of selected devices, covering high to low voltage device range, is conducted to decide whether an overall efficiency gain is achieved.

Chapter four presents a brief overview of high frequency transformer design. A nanocrytalline cored, high-current, step-down transformer design, to be utilised in the DC/DC converter is also presented, aided with analytical analysis and FEA simulations.

Chapter five describes the basic operation of synchronous rectification, and studies the parallel operation of MOSFETs, as a large number of devices are connected in parallel

to achieve the required current rating. An electro-thermal device model is developed, to show the effect of parameter variation on current sharing. The model is used to verify the steady-state device temperatures for the 10 parallel connected devices, synchronous rectifier, adopted in the DC/DC converter circuit.

Chapter six presents the experimental testing and small-signal system modelling of the high-current low-voltage DC/DC converter. Open-loop and close-loop experimental results are presented. Loss distribution through the various system components is highlighted. A control technique, improving the efficiency of the synchronous rectification, over the self-driven techniques is developed.

Chapter seven investigates the scaled-up converter module design. A 10 kA module is proposed, to take the advantage of using higher power semiconductor devices, offering lower conduction losses. A chip-level, paralleled MOSFET module is presented, to reduce the possible difficulties of paralleling a large number of MOSFET devices, and improve current sharing. Parallel converter operation is also discussed, showing that a common current reference control technique is basically suitable for providing balanced current sharing, in case of different converter parameters.

Chapter eight presents the conclusions, author's contribution, and possible future research.

Chapter 1

Introduction

The growing demand for energy is leading to an exponential depletion of the finite fossil fuel reserves. Alternative sources of energy are being considered to avoid a determined energy crisis, added to the world's current attention to the dangers of increased carbon dioxide levels, which contributes to global warming. Renewable energy using natural resources, such as hydropower, wind energy, solar energy, geothermal, biofuels, and tidal energy are currently being used/developed, but only contribute to 19% of the global energy demands [1.1]. However, renewables are mostly cyclic sources and are not continuously available, and most conversion processes result in poor efficiencies. Current research strategies are directed towards improving the efficiency of different renewable energy sources, and finding new alternative methods to produce energy. Fusion energy is considered a promising alternative source of energy to the radioactive waste producing nuclear fission process. Attempts at controlling fusion reactions started during the 1940s, when the first experimental fusion reactor was patented by the United Kingdom Atomic Energy Authority (UKAEA) [1.2].

A design for a power plant based on the spherical tokamak (ST) is being currently developed at Culham Centre for Fusion Energy (CCFE) [1.3]. A Component Test Facility (CTF) based on the spherical tokamak design is also being developed to explore the scientific concepts and provide a testing facility for research related to materials and components used.

1.1 Fusion energy and tokamaks

Fusion is the process that powers the sun, in which hydrogen nuclei collide and release massive amounts of energy [1.4]. Fusion research is aimed at reproducing this process through a smaller and safer method, in order to fulfil the growing energy needs. Basically, the concept behind the fusion reaction is to get two or more atoms close together, overcoming the repulsive electrostatic forces due to the nuclei charges, so that the nuclei will pull together using their strong nuclear force, and fuse into one larger atom. The two fused nuclei generally form a single nucleus with a slightly smaller mass

for the fusion of light atoms (with atomic mass below that of iron). The mass difference is released as an enormous amount of energy, according to Einstein's mass-energy equivalence formula ($E = mc^2$) [1.5]. In order to bring the nuclei into close proximity and overcome the electrostatic forces of similar charges, an external source of energy must be supplied, basically heat energy. Atoms are extensively heated until reaching the plasma state, in which electrons are separated, forming a gas consisting of independently moving charged particles [1.4], [1.5]. Extremely high temperatures are required for the nuclei to successively collide and fuse, which is directly proportional to the total atomic charge. Hydrogen atoms, having the smallest nuclear charge, require the lowest temperatures. Helium also possesses the lowest mass per nucleon, and is energetically-wise preferred as a fusion product. Consequently, current experimental fusion reactions combine isotopes of hydrogen (deuterium and tritium) to form isotopes of helium (3He or 4He), producing energy and neutrons [1.5]. This mixture is heated to a temperature of approximately 100 million degrees Celsius to successfully produce a thermonuclear fusion reaction [1.6]. A diagram showing the reaction process is given in Figure 1.1.

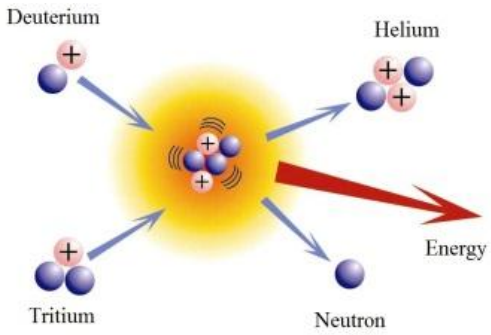


Figure 1.1: Fusion of deuterium and tritium atoms forming a helium atom [1.6]

Plasma, consisting of positive and negative charged particles (nuclei and electrons), is a good electrical conductor and can be readily influenced by magnetic fields. Hence, it can be contained inside a vessel, keeping the high temperature mixture away from the containing vessel walls. The most popular device for magnetic plasma confinement is the tokamak reactor, which is a toroidal vacuum chamber supplied with strong magnetic fields to confine and shape the plasma within the torus [1.7]. A basic structure for a tokamak is shown in Figure 1.2, in which two magnetic fields are used for controlling and shaping the plasma: toroidal and poloidal magnetic fields, giving a resultant helical

magnetic field. The inner poloidal field coils are also used to pass high currents through the plasma by transformer action, increasing the plasma temperature and aiding the other plasma heating methods (neutral beam injection and radio frequency heating) to attain the required temperatures. Other fusion energy concepts include the stellarator, the spherical tokamak, and inertial confinement fusion [1.7].

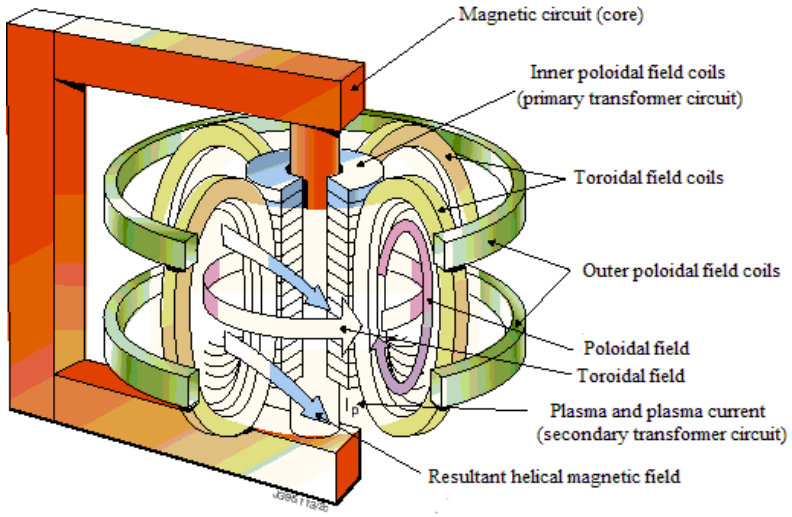


Figure 1.2: Basic structure of a tokamak fusion reactor, showing the toroidal and poloidal field coils, and the ohmic heating circuit (the magnetic core is only used for illustration) [1.7]

Many magnetic confinement based fusion reactors have been built since the early 1970s, in which the main goals are obtaining a stable and sustainable reaction, and the successful utilisation through a commercial power plant [1.6]. Energy extraction from the reactor is achieved by surrounding the plasma by a lithium blanket, which absorbs neutron energy and breeds tritium fuel. Extracted heat then undergoes the same cycle as existing power plants: heat is used to produce steam to drive turbines connected to generators. A simple diagram for a complete fusion energy power plant is shown in Figure 1.3. The basic advantages of fusion power plants over their nuclear fission predecessors are [1.6], [1.8]:

- The fusion reaction produces helium, with no resultant atmospheric pollution.
- Deuterium and tritium mixture, the fuel likely to be used for fusion energy, are both forms of hydrogen and are abundant materials. Deuterium can be readily extracted from ordinary water, while tritium is produced inside the fusion power plant from the lithium blanket, in which lithium is also abundant.

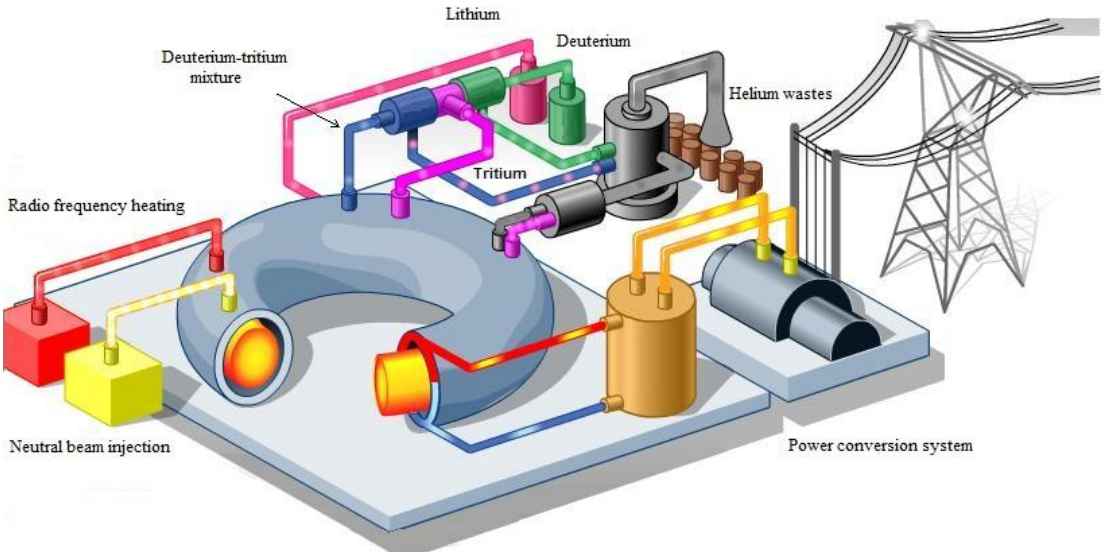


Figure 1.3: Basic structure of a fusion power plant

- One kilogram of fusion fuel produces the same amount of energy as approximately 10,000,000 kilograms of fossil fuels, which makes fusion energy very efficient.
- Fusion energy produces no long-lived radioactive waste. All irradiated plant components are safe to dispose within 100 years.
- The cost of fusion generated electricity is predicted to be comparable to fossil fuel or fission generated electricity.

Most fusion research concentrates on conventional tokamak designs possessing D-shaped plasma. The Joint European Torus (JET) at CCFE is considered the most successful fusion experiment for such reactors. The spherical reactor design provides a more compact device, in which the first spherical tokamak, START (Small Tight Aspect Ration Tokamak), was successfully designed and built. MAST (Mega-Amp Spherical Tokamak), a larger version of START, was also built following the impressive results obtained from START [1.6], [1.7].

Many other fusion experiments and fusion reactor prototypes have been successfully built in many other countries, to explore different concepts. Significant progress has been achieved, which lead to planning for the construction of a larger and more powerful fusion device: The International Thermonuclear Experimental Reactor (ITER), with an expected completion time during 2018. ITER is a joint project between many

countries, and is designed to produce 500MW of fusion power, compared to the current world record of 16 MW achieved by JET. The first commercial demonstration fusion power plant named DEMO is expected to follow the research of ITER, to bring fusion energy to commercial markets [1.7].

1.2 The spherical tokamak power plant

The main objective for achieving a successful fusion power plant is to deliver more fusion power than that required to heat the plasma. The hot fuel is kept away from the reactor walls by strong magnetic fields, which aids maintaining the high plasma temperatures. However, sustaining a stable fusion reaction itself is considered a complex issue. Minor perturbations in the plasma (for example, due to the interaction between the plasma particles and the magnetic enclosure) may lead to different instabilities, such as severe electromechanical forces, hence impairing the confinement and reducing the fusion yield. Plasma stability is an important factor in the operation of magnetically confined fusion. Plasma may be treated as a fluid, the stability of which may be analysed using magnetohydrodynamics (MHD) [1.9]. According to MHD stability calculations, low aspect ratio tokamak designs allow higher plasma pressure for a given magnetic field, leading to higher fusion power density [1.10]. This offers the possibility of achieving a reduced core power plant for the same total fusion power compared to conventional large aspect ratio designs.

The main confinement field for the spherical tokamak power plant (STPP) is produced by a single turn toroidal field coil, consisting of a water cooled solid centre rod and 16 water cooled return limbs. Each of these limbs is connected to 2 MA power supplies, which are located circumferentially around the power core. The massive current requirement (total of 32 MA passing through the central rod) is mandatory to produce the main toroidal confinement field, due to the fact that a single turn coil is used. Plasma shape and positioning is achieved by the aid of poloidal and divertor coils. A helium cooled lithium blanket surrounding the plasma is used for extracting the neutron energy released. Additional detailed descriptions for the operation, design parameters, and main concept are presented in references [1.3], [1.10], and [1.11]. A 3D view for the ST power plant, showing the single turn toroidal field coils, is shown in Figure 1.4.

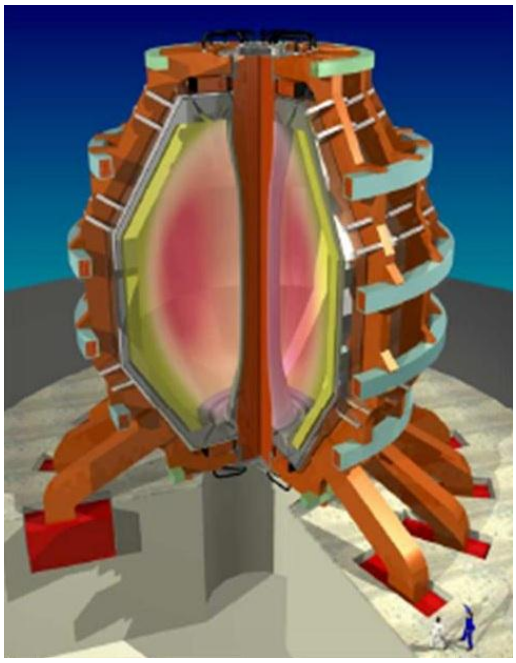


Figure 1.4: Spherical tokamak power core 3D view [1.3]

The realisation of the ST design requires research and development in many areas, including plasma physics, power supply and electrical engineering, as well as material technologies. A reduced scale fusion reactor, a component test facility (CTF), is due for construction before proceeding with the actual spherical power plant [1.8]. The toroidal field (TF) coils for both the STPP and CTF are similar since both are single turn water cooled copper coils. The main system parameters and power supply requirements for both cases are shown in Table 1.1. The water cooled central rod is however subject to excessive neutron irradiation, increasing its resistivity over time. The output voltage of the TF power supplies is then required to be gradually increased, compensating for the increased load resistance and maintaining total current at the required value. The initial resistance and final resistance values at which the central rod has to be replaced are also given in Table 1.1.

Table 1.1: STPP and CTF power supply requirements [1.8]

	STPP	**CTF**
Number of turns	1	1
Number of return limbs	16	10
Initial resistance of centre rod (μΩ)	0.1644	0.45
Final resistance of centre rod (μΩ)	0.1808	0.495
Resistance of TF limbs and feeders (μΩ)	0.0832	0.45
Continuous DC current (MA)	32	10.5
Total required voltage (V)	7.92-8.45	9.45-9.92
Power dissipated in TF coils (MW)	253-270	99.2-104

1.3 The toroidal field power supply

A low-voltage high-current power supply system, based on conventional rectifying techniques, has been proposed in [1.3] as a baseline option. The proposed distribution power system is shown in Figure 1.5. Power is drawn either from a single step-down 400/22 kV, 400 MVA transformer, or directly from generator terminals at 22 kV. Power at 22 kV is distributed through 16 feeder breakers to 25 MVA step-down regulator transformers, with on-load tap changers providing 20% voltage regulation. Each regulating transformer supplies four thyristor phase angle controllers, feeding a pair of 250 kA converter modules, with each converter module assembled with two 125 kA rectifier modules, one on each side of the transformer. The lowest loss power circuit topology is used, with the secondary windings of the converter transformers connected in a half-wave double-star/inter-star configuration.

The lowest loss semiconductors are also employed (i.e. large 100 mm diameter thin-slice silicon diodes). Each rectifier module comprises two 3-phase diode modules forming 6 pulse groups. Plus and minus 15 degrees phase-shift windings, on alternative converter pairs, ensure balanced 12 pulse operation. Each group of eight converter modules are connected in parallel and feed a single pair of 2 MA radial bus bars. The ratings of the main system components are summarised in Table 1.2.

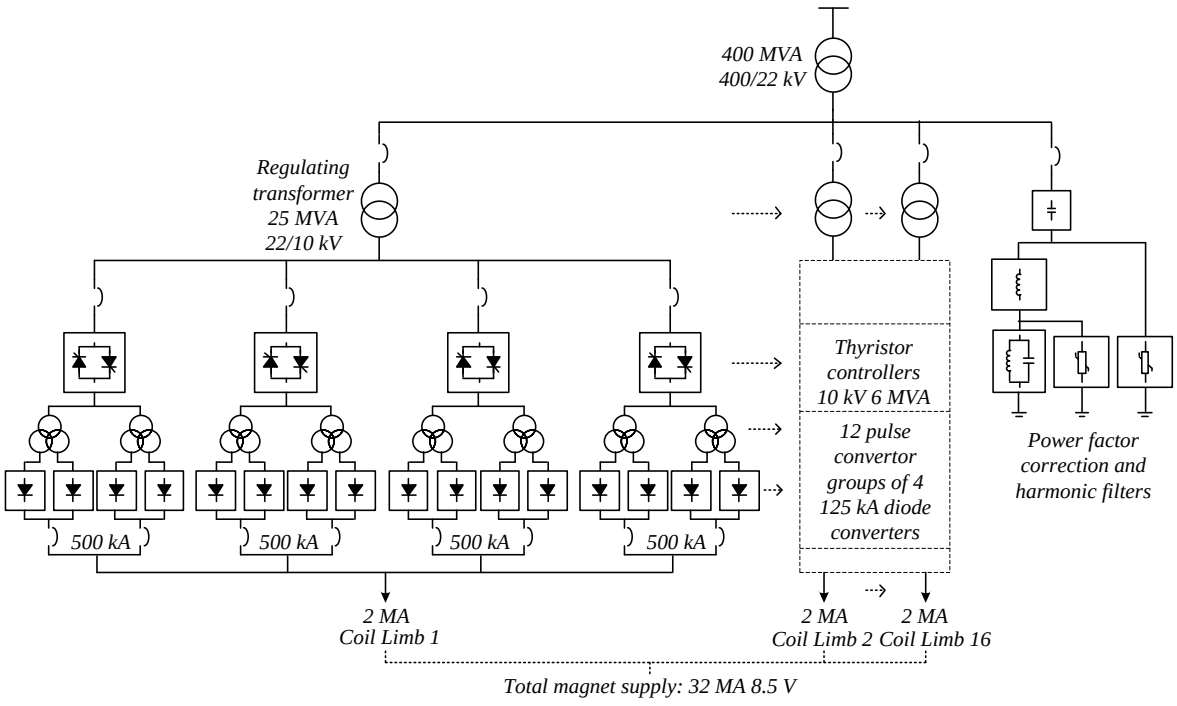


Figure 1.5: Toroidal field coil power supply baseline design [1.3]

Table 1.2: Power system component ratings

Component	Quantity	Power Ratings
Supply transformer	1	3 Phase, 400 MVA, 400/22 kV, star/delta
Regulating transformers	16	3 Phase, 25 MVA, 22/10 kV, star/delta
Thyristor controllers	64	3 Phase, 6 MVA, 10 kV, 350 A
Converter transformers	128	3 Phase, 3 MVA, 10 kV/10 V, Interstar/double star
Rectifiers	128	2x 2.125 MW, 125 kA, 200 V, 6 pulse

The electrical efficiency of the complete power system has been estimated to be approximately 67 % at full-load current, which relatively, is much lower than that achieved for other converter applications with higher output voltage requirements [1.3]. An estimate for the total system power loss, starting from the regulating transformers, shows that the low-voltage transformer-rectifier modules contribute highly to the reduced system efficiency, as shown in Table 1.3.

Table 1.3: Estimated system power loss and efficiency [1.3]

System component	Power Loss (MW)
Regulating transformers	3.6
Thyristor controllers	5.6
Transformer rectifier modules	122
Total TF coil power	254-270
Input power at 22 kV bus bars	385-401
Efficiency	66-67%

1.4 AC/DC conversion systems

AC/DC conversion systems may be basically classified into single-stage and double-stage conversion systems [1.12]. Single-stage converters comprise simple transformer rectifier units, in which a half-wave or full-wave rectifier circuit topology is used. Lower output current/voltage ripple may be achieved by having multiple phase shifted transformer secondary outputs, by using appropriate phase shifting. Single-stage rectification may be then subcategorised, based on the semiconductor device used, into diode rectification, thyristor rectification, and active rectification. Output voltage control may be achieved in the case of thyristor and active rectification, while thyristor phase control and/or regulating transformers are used in the case of diode rectification. Active rectification has the added advantage of drawing power from the utility grid at unity power factor and minimum harmonic distortion. For double-stage conversion, the system consists of a conventional transformer rectifier unit followed by a switched

mode power supply, connected through a DC link capacitor. The switched mode power supply topology may be a DC/DC or DC/AC/DC conversion process, based on the application requirements. Chopper circuits are an example of DC/DC converter topologies, while an inverter-transformer-rectifier unit is considered a typical example of DC/AC/DC conversion topologies. The basic classification of AC/DC conversion systems is illustrated in Figure 1.6. Circuit diagrams showing the different rectification topologies are shown in Figures 1.7 to 1.10 [1.13].

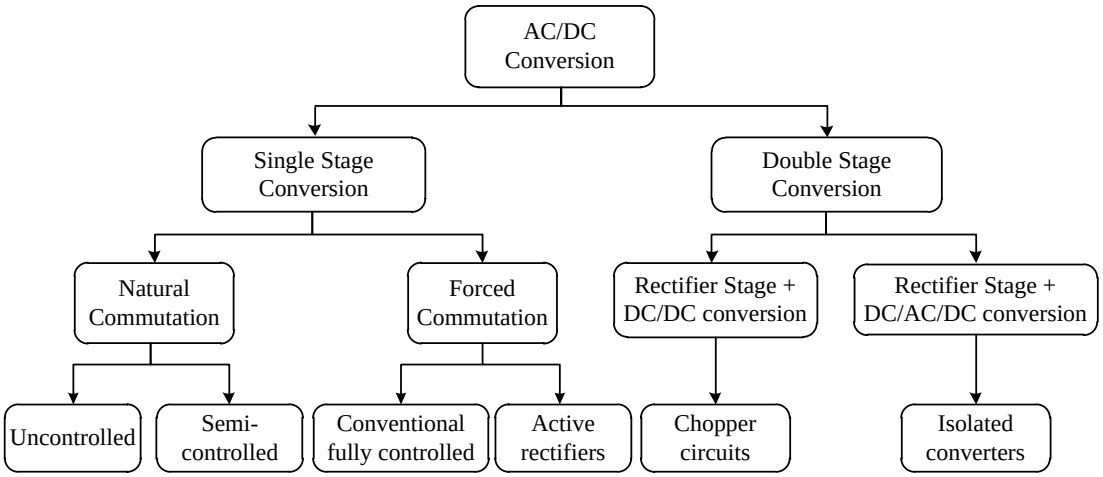


Figure 1.6: Basic classification of AC/DC conversion systems

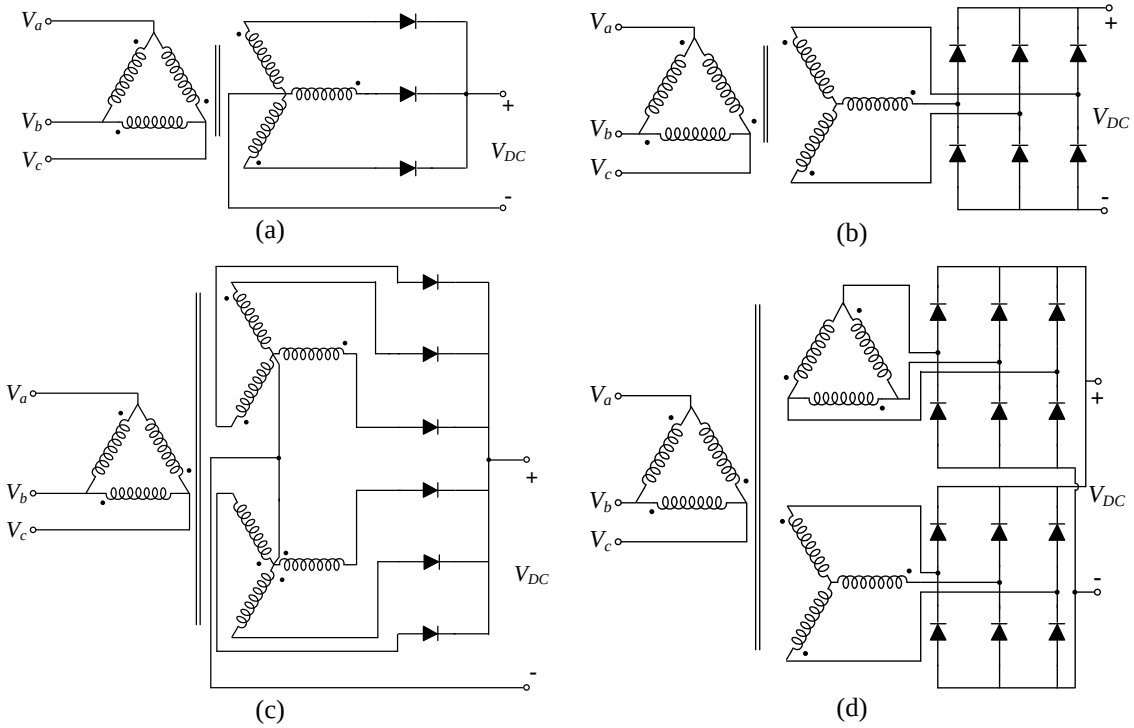


Figure 1.7: Basic diode rectification circuit topologies showing 3 pulse and 6 pulse half-wave rectifiers in (a) and (c), 6 pulse and 12 pulse full-wave rectifiers in (b) and (d) respectively

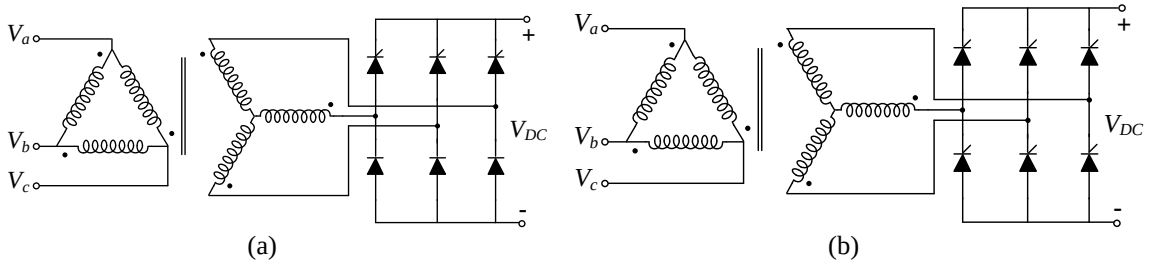


Figure 1.8: Examples of semi-controlled and fully-controlled line commutated converters as shown in (a) and (b) respectively

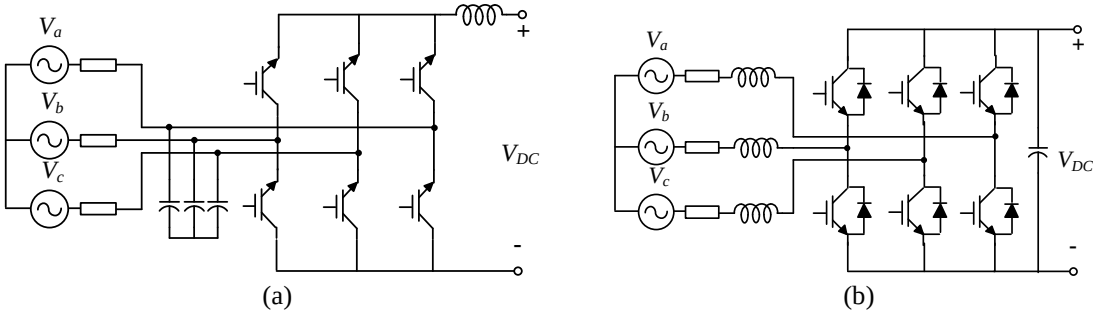


Figure 1.9: Basic active rectification topologies showing the voltage source and current source rectifiers in (a) and (b) respectively

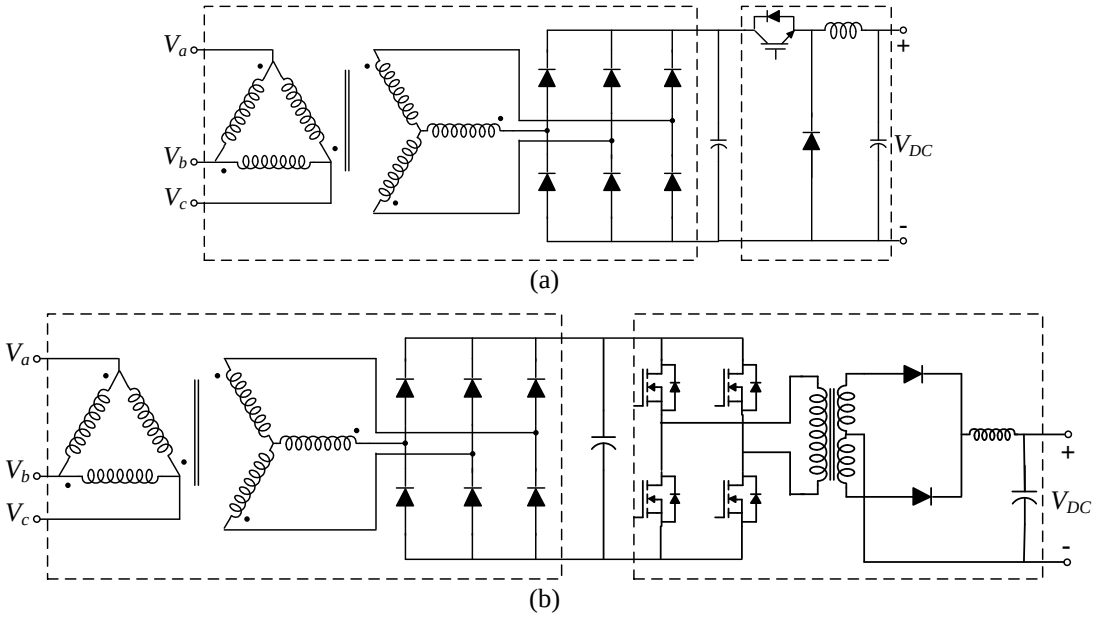


Figure 1.10: Examples of double stage rectification showing a full bridge rectifier followed by a buck converter, and a full bridge rectifier followed by an isolated DC/AC/DC converter, in (a) and (b) respectively

The rectification topology choice is usually determined by the application requirements (voltage/current ripple, volume, power rating, etc…). Electrolytic applications which require high DC currents in the order of kilo Amperes, and DC voltage levels of a few hundred volts, usually employ thyristor based configurations [1.14]. Single-stage full-bridge or half-bridge rectifier configurations, with 12 pulse outputs are typically used. Alternative rectifier configurations have been proposed to improve efficiency and reduce supply harmonic content. Most are double stage converters utilising the use of voltage source inverters to modulate the voltage delivered to a step down transformer before the final rectifying stage [1.15]. For the rectifying stage, a current rating requirement of the rectifying devices exceeds the capability of single device packages, wherein parallel connected devices and parallel connected converters are used. Similarly, 12 pulse full-bridge thyristor rectifiers are proposed for supplying the HELIAS stellarator fusion reactor superconducting coils, at current and voltage levels of 16 kA and 300 V respectively [1.16]. However, for lower voltage levels, as required by the EAST tokamak toroidal field coils (20 V, and 16 kA), half-wave rectification with a double star configuration is used [1.17].

Superconducting magnets utilised in the Large Hadron Collider also require high DC currents at very low voltages. A 20 kA, 6 V, power supply is presented in [1.18]. The system is based on the double-stage conversion topology, in which a ZVS phase-shift PWM inverter is used to supply a centre tapped rectifier transformer at 20 kHz. A modular approach is used, where several converters are parallel connected to provide the required current, as well as redundancy. Transformer primaries are connected in series, while secondary circuits are connected in parallel to insure current sharing. Parallel connected Schottky diodes are used in the rectification stage due to their lower voltage drop, compared to conventional diodes. The use of a high frequency conversion stage permits the use of reduced size magnetic components, namely transformers and filtering components [1.19]. The basic high frequency rectifying topologies for high-current low-voltage requirements are those utilising only one rectifying device per path, such as centre tapped full wave rectifiers. Current-doubler, current-tripler, and n-tupler topologies reduce the transformer secondary winding losses by using additional inductors in the secondary rectifying circuits, as presented in [1.20], [1.21], and [1.22]. However, it may be inadequate at extremely high current requirements due to the relative difficulty of obtaining high current inductors. A similar application in which a

20 MA current at 20 V supplies a single-turn toroidal field coil of the spherical tokamak, wherein a synchronous rectifier using power MOSFET devices, at 50 Hz, is proposed [1.23]. The voltage drop across MOSFET devices is much lower than that of diodes, hence significantly improves converter efficiency. Paralleling MOSFETs is also discussed to achieve further conduction loss reduction, due to the resistive characteristics of MOSFET devices during their on-state. Additional device on-state resistance reduction can be achieved by using liquid nitrogen cooling [1.24], [1.25]. A bidirectional MOSFET switching element utilised in a full-bridge converter is also proposed as a solution in [1.25].

1.5 PhD Objectives

The main objective of this PhD is to study the realisation of a high-current low-voltage AC/DC converter system, for supplying the spherical tokamak toroidal field coils. Based on the brief review presented in the previous section for similar applications, a double stage conversion system is chosen. The high frequency DC/AC/DC conversion stage can then be placed in close proximity to the TF coils, minimising high current bus bar lengths and the associated losses. The use of high frequency transformers minimises the final stage converter footprint. Centre-tapped half-wave rectification is employed due to the low output voltage requirements. Parallel connected modules are to be used for achieving the required final current ratings. A zero voltage switching (ZVS) phase shift PWM inverter topology is used for the DC/AC conversion stage as a basic approach to minimise switching power loss. Based on the available laboratory bench power supply ratings, a DC link voltage of 600 V is assumed for implementing a lab-scaled experimental setup. The design, simulation, and implementation of a centre tapped, high current, high frequency transformer is also carried out. Synchronous rectification is the best solution for minimising the low voltage rectification power loss. This research is basically focusing on the second conversion stage, and reducing the low voltage rectification power loss, for which the following key research points are considered:

- The design, analysis and implementation of a MOSFET based, 600 V, phase-shift PWM, zero voltage switching converters, as part of the DC/DC converter under study.

- Investigate the cryogenic operation of MOSFET devices, to conclude if liquid nitrogen cooling would offer significant on-resistance reduction for either the low-voltage or high-voltage, commercially available MOSFET devices.
- Design and implement a high-current low-voltage centre tapped transformer based on the lowest loss core materials available, as high frequency transformers are not available as standard wound components.
- Study the parallel operation of MOSFET devices, and design a high current synchronous rectifier module. An output current of 1 kA at 8.5 V is the target design ratings, based on the available VA ratings available for the lab power supplies. The output power rating of the converter is considered adequate for representing a lab scaled high-current low-voltage DC/DC converter.

References

[1.1] REN21, *"Renewables 2010 Global Status Report"*, http://www.ren21.net, 2010.

[1.2] G. Thompson, M. Blackman, *"British Patent 817681 Haines MG 1996"*, Plasma Phys. Control. Fusion, 38, p. 643, 1946.

[1.3] G. Voss, A. Bond, J. Hicks, H. Wilson, *"Development of the spherical tokamak power plant"*, Fusion Engineering and Design, Volume 63, pp. 65-71, 2002.

[1.4] G. McCracken, P. Stott, *"Fusion: the energy of the universe"*, Academic Press, ISBN: 012481851X, 2005.

[1.5] Wikipedia, *"Fusion power"*, http://en.wikipedia.org/wiki/Fusion_power, Last update in 2010.

[1.6] CCFE, *"Introduction to Fusion"*, Culham Centre for Fusion Energy Website, http://www.ccfe.ac.uk/introduction.aspx, Last update in 2009.

[1.7] EFDA, *"Introduction to Fusion"*, European Fusion Development Agreement Website, http://www.efda.org/fusion_energy/introduction_to_fusion.htm, Last update in 2010.

[1.8] *"Private communication with CCFE personnel"*.

[1.9] L. Solov'ev, *"The Theory of Hydromagnetic Stability of Toroidal Plasma Configurations"*, Soviet Physics JETP, Volume 26, pp. 400-407, 1968.

[1.10] G. Voss, S. Allfrey, A. Bond, Q. Huang, P. Knight, V. Riccardo, H. Wilson, *"A conceptual design of a spherical tokamak power plant"*, Fusion Engineering and Design, Volume 51, pp. 309-318, 2000.

[1.11] J. Hicks, *"Toroidal field system for tight aspect ratio tokamak reactors"*, Fusion Engineering and Design, Volume 18, pp. 227-232, 1991.

[1.12] A. Siebert, A. Troedson, S. Ebner, *"AC to DC power conversion now and in the future"*, IEEE Transactions on Industry Applications, Volume 38, pp. 934-940, 2002.

[1.13] M.H. Rashid, F.L. Luo, *"Power electronics handbook: devices, circuits, and applications"*, Academic Press, ISBN: 9780120884797, 2006.

[1.14] E. Wiechmann, P. Aqueveque, *"Filterless high current rectifier for electrolytic applications"*, IEEE Industry Applications Conference Record of the Fourtieth IAS Annual Meeting, Volume 1, pp. 198-203, 2005.

[1.15] P. Aqueveque, E. Wiechmann, R. Burgos, *"On the efficiency and reliability of high-current rectifiers"*, IEEE Industry Applications Conference, 41st IAS Annual Meeting., Volume 3, pp. 1290-1297, 2006.

[1.16] J. Skiles, R. Kustom, K. Ko, V. Wong, K. Ko, F. Vong, K. Klontz, *"Performance of a power conversion system for superconducting magnetic energy storage (SMES)"*, IEEE Transactions on Power Systems, Volume 11, pp. 1718-1723, 2002.

[1.17] X. Liu, J. Jiang, L. Xu, Y. Liao, *"Power supply for the superconducting TF magnet system of EAST"*, Nuclear Fusion, Volume 46, pp. 90-93, 2006.

[1.18] H. Jørgensen, F. Bordry, A. Dupaquier, G. Fernqvist, *"High Current, Low Voltage Power Converter [20kA, 6V]: LHC Converter Prototype"*, Sixth European Particle Accelerator Conference, Volume 1, pp. 2059-2061, 1998.

[1.19] P. Dahono, M. Firmansyah, Y. Pramasti, *"A high-current low-voltage DC power supply"*, IEEE 4th International Conference on Power Electronics and Drive Systems, Volume 2, pp. 517-521, 2001.

[1.20] P. Alou, J. Oliver, O. Garcia, R. Prieto, J. Cobos, *"Comparison of current doubler rectifier and center tapped rectifier for low voltage applications"*, IEEE Twenty-First Annual Applied Power Electronics Conference and Exposition, Volume 1, pp. 7-13, 2006.

[1.21] J. Lee, B. Kwon, *"DC–DC converter using a multiple-coupled inductor for low output voltages"*, IEEE Transactions on Industrial Electronics, Volume 54, pp. 467-478, 2007.

[1.22] L. Yao, H. Mao, I. Batarseh, *"A rectification topology for high-current isolated DC-DC converters"*, IEEE Transactions on Power Electronics, Volume 22, pp. 1522-1530, 2007.

[1.23] T. Matsukawa, M. Shioyama, J. Nomura, C. Neumeyer, S. Tsuji-Iio, R. Shimada, *"Synchronous rectifier using power-MOSFET for high current AC/DC converter system"*, IEEE 19th Symposium on Fusion Engineering, Volume 1, pp. 80-83, 2002.

[1.24] T. Matsukawa, H. Chikaraishi, Y. Sato, R. Shimada, M. Ishida, *"Synchronous AC/DC Converter Using Advanced Unipolar Power Electronics Device"*, IEEE/NPS Twenty-First Symposium on Fusion Engineering, Volume 1, pp. 1-4, 2006.

[1.25] T. Matsukawa, K. Shimada, M. Shioyama, S. Nomura, C. Neumeyer, S. Tsuji-Iio, R. Shimada, *"Low voltage, high current DC power supply with self commutated converter using power-MOSFET"*, IEEE 18th Symposium on Fusion Engineering, Volume 1, pp. 137-140, 2002.

Chapter 2

Zero Voltage Switching Phase-Shift PWM Resonant Converter

The conventional hard switched full-bridge converters prevent the realisation of high efficiencies at high switching frequencies, due to the excessive switching losses. Zero voltage switching (ZVS) phase-shift PWM resonant topologies have been widely used in high power density converters, wherein the switching losses are almost eliminated.

This chapter presents the basic theory, design procedures, and power loss analysis associated with zero voltage switching (ZVS) phase shift (PS) PWM resonant converters. The design outline for the 600 V, 12 kW, resonant converter utilised in the high-current low-voltage power supply is also presented, supported by Matlab Simulink simulations.

2.1 Background

Resonant converters are widely used in low to medium power applications. The main advantage behind such applicability is the reduced switching losses, wherein higher switching frequencies can be adopted compared to conventional hard switched PWM converters. Moreover, volume reduction in various magnetic/passive components can be achieved. Switches are turned on and off near zero crossings of tank circuit voltage or current waveforms, which are respectively defined as zero voltage switching (ZVS) and zero current switching (ZCS), wherein output voltage is basically controlled by varying the switching frequency (i.e. is load current dependant). However, resonant converter operation cannot be optimised for wide loading ranges and significant currents may circulate through the tank elements at light loads, leading to poor efficiencies. Moreover, quasi-sinusoidal waveforms exhibit higher peak values than equivalent rectangular waveforms, which may increase conduction losses and component stresses to larger extent than that of switching losses in high power applications [2.1]. It is difficult to optimise filter components used in conventional resonant converters, due to the fact that a wide frequency range is required for operation [2.2]. However, other topologies such as quasi-resonant, multi-resonant, and constant frequency resonant techniques offer solutions to the large frequency range variations and component stresses, with different design complexity levels, as presented in [2.3], [2.4], [2.5], and

[2.6]. For high power applications, partial resonant converters are of advantage, in which the resonant elements resonate partially; during the switching transient only, and are not involved in the primary power transfer [2.7]. This overcomes the high resonant tank VA ratings required in conventional resonant and quasi resonant converters. Additionally, such topologies can utilise circuit parasitic elements (switching device output capacitance and transformer leakage inductance), specifically for the phase-shift PWM ZVS topology. ZVS is achieved for all full bridge converter switches by adopting the resonant discharge of the switching device output capacitance and the transformer leakage inductance.

ZVS phase-shift (PS) PWM converters operate at constant frequency, while the output voltage may be regulated by phase shifting the leading and lagging bridge legs to adjust the primary duty cycle. However, such a topology also suffers some limitations, such as narrow ZVS range, duty cycle loss, secondary rectifier voltage ringing, and large circulation energy. The ZVS range can be extended by employing different auxiliary circuits [2.8], [2.9], [2.10], and [2.11]. A saturable reactor can be used instead of the traditional linear inductor, or transformer equivalent leakage inductance, to reduce the duty cycle loss and circulating energy [2.12]. Overshoot and voltage ringing across the rectifier diodes can be reduced by using dissipative clamps [2.13], low-loss active clamps [2.14], commutating aid circuits [2.15], or by employing a two inductor rectifier [2.16].

ZVS PS PWM is more suitable for use with MOSFET switches than for IGBTs. However, it is desirable to use IGBTs, due to their lower conduction losses and higher power density modules, especially for high voltage applications. The ZVS range of the lagging bridge leg is limited when using IGBTs, unless the leakage inductance is large [2.17], [2.18]. Moreover, IGBTs exhibit current tailing during turn off, which limits the maximum operating frequency to about 20-30 kHz [2.19]. Additional capacitors are required in parallel with the IGBTs to reduce the turn off switching loss, which may reduce the ZVS range of the converter. However, applying active and passive auxiliary circuits has been proposed in different topologies to achieve ZCS for the lagging leg [2.20], [2.21], which adds complexity to the converter circuit, as well as extra switching devices, and associated losses.

2.2 Theory of operation

A full-bridge converter circuit is shown in Figure 2.1. The basic principle of ZVS is to introduce a delay interval between the turn-off and turn-on of switches in each bridge arm, during which, resonance occurs between the transformer leakage inductance and the corresponding switch output capacitance. This dead-time delay interval is conventionally used to avoid short circuit resulting from unintentional simultaneous conduction of switches in the same arm. However, during this short interval, the corresponding switch output capacitance is completely discharged, and the anti-parallel diode is forced into conduction.

Turn-off ZVS is mainly achieved by the presence of the snubber/output capacitance, as it slows down the drain source voltage rise. Moreover, the overlapping between the rising drain source voltage and the decreasing drain current is small, due to the fast response of MOSFET devices.

Output duty cycle variation is achieved by providing phase-shifting between the turn-on of diagonally opposite switches. The mechanism by which ZVS is achieved is different for both bridge arms. During the analysis it is assumed that no additional circuit components are added. The transformer leakage inductance is used as the resonant inductor and the device output capacitance is utilised as the snubber capacitance. The following analysis is for the general converter case, where an output LC filter is used. This analysis is considered valid in the case of removing the output capacitance, by considering the instantaneous output voltage, which would be represented by a series of square pulses having the same average voltage per cycle.

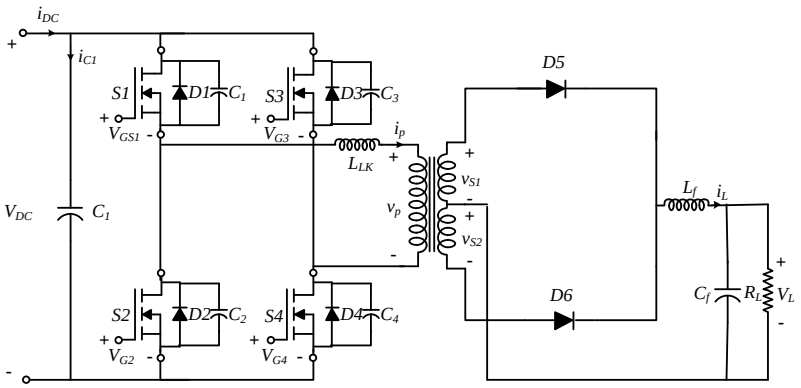


Figure 2.1: Full bridge ZVS phase shift PWM converter circuit

2.2.1 Gate signal generation

A ramp waveform, with an instantaneous value of t_{ramp}, which resets at the end of the required switching period T is used as a reference signal for generating the required gate pulses. Given that t_{LL} is the left leg transition delay, t_{RL} is the right leg transition delay, and t_{PS} is the time/phase shift between both bridge legs, the turn-on conditions for each switch are given in Table 2.1, and illustrated in Figure 2.2.

Table 2.1: Turn-on conditions for gate signal generation

Switch	Turn-on conditions
S1	$\frac{T}{2} \geq t_{ramp} \geq t_{LL}$
S2	$T \geq t_{ramp} \geq t_{LL} + \frac{T}{2}$
S3	$t_{PS} + t_{RL} \geq t_{ramp} \geq \frac{T}{2} + t_{PS}$
S4	$t_{PS} \geq t_{ramp} \geq \frac{T}{2} + t_{PS} + t_{RL}$

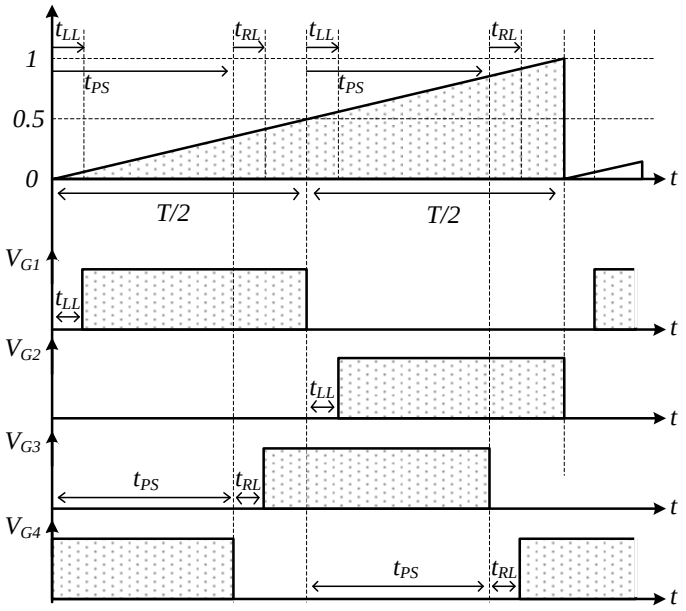


Figure 2.2: Reference ramp signal and generated gate pulses

2.2.2 Modes of operation

The three main modes of operation shown in Figure 2.3 can be assessed by observing the primary current waveform, as follows:

a. Power delivery mode: (t_0 - t_1, t_6 - t_7, ...)

The power delivery mode is the time interval in which either pair of the diagonally opposite switches *S1* and *S4*, or *S2* and *S3*, are both turned on. This time interval is directly proportional to the introduced phase shift, and is equal to $D_{eff} \times T/2$, where D_{eff} is the effective primary voltage duty cycle.

b. Freewheeling mode: (t_2 - t_3, t_8 - t_9, ...)

This is the time interval in which each of the vertically opposite switches *S1* and *S3*, or *S2* and *S4* are in the on-state. This interval is inversely proportional to the applied phase shift, and is equal to $(1-D) \times T/2$, where D is the applied primary duty cycle. During this interval, the primary current freewheels through the corresponding MOSFET switches. Switch and circulation path conduction losses, as well as the reflected load, cause this current to ramp down.

c. Slew mode: (t_3 - t_6, t_9 - t_{12}, ...)

The slew mode is the time interval in which the primary current reverses direction, and is equal to $\Delta D \times T/2$, where ΔD is the duty cycle loss due to this process. It is directly proportional to the load current and total reflected leakage inductance L_{lk} and inversely proportional to the supply voltage V_{DC} ($V_{DC} = L_{lk}\,\Delta i/\Delta t$).

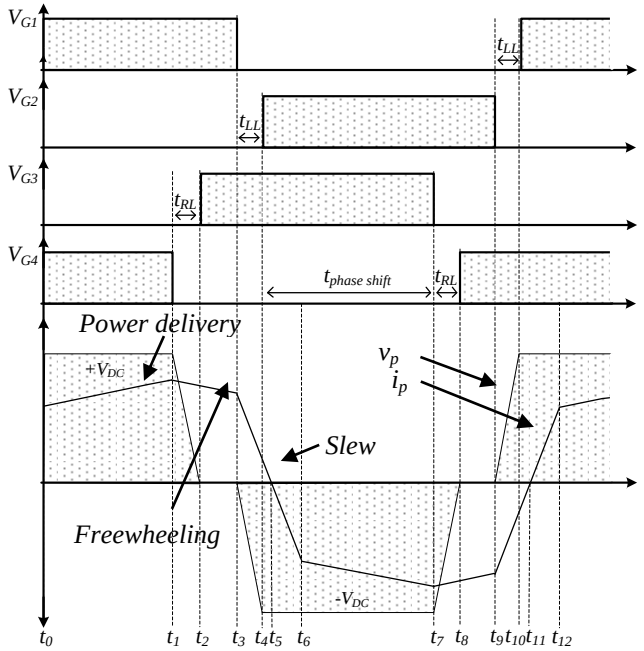


Figure 2.3: Gate signals and transformer primary voltage and current

2.2.3 The resonant cycle

With a sufficiently large transition delay between the upper and lower bridge leg switches, resonant oscillation between the output capacitance and series leakage inductance is observed. The upper and lower switches (*S1* and *S2*) gate signals and lower switch source drain voltage are shown in Figure 2.4. The amplitude of the resonant cycle is directly proportional to the load current and the energy stored in the leakage inductance. This amplitude decreases exponentially until it settles at half the supply voltage (each device per branch, during open circuit, supports half the supply voltage). The main requirement is to turn-on the switch at the instance where the peak resonant cycle voltage reaches zero, thus the switch can be turned on at zero voltage. At this instant, the minimum load for achieving ZVS is defined. However, at higher loads, the peak value may be much higher and current starts flowing through switch *S2* body diode, and the source-drain voltage is clamped to the body diode voltage drop. In this case, the energy stored in the leakage inductance is much larger than that required to discharge the output capacitance, and circulates through the body diode into the supply.

Switch *S2* turn-on should occur at the minimum point where the source-drain voltage reaches zero, at full load. However, this leads to the loss of ZVS under other loading conditions. Turn-on should be selected at the minimum load value which leads to the peak resonant voltage waveform reaching zero. As *S1* is turned off, the primary current forces *D2* to turn-on by discharging the output capacitance of *S2*, during the resonant cycle. This is only achieved if the energy stored in the leakage inductance at this point is greater than that stored in the resonant capacitor:

$$\frac{1}{2}L_{lk}i_p^2 \geq \frac{1}{2}C_rV_{DC} \tag{2.1}$$

The resonant frequency is defined as:

$$f_r = \frac{1}{2\pi\sqrt{L_rC_r}} \tag{2.2}$$

where L_r is the resonant inductance (transformer leakage inductance), and C_r is the resonant capacitance. Given that C_{oss} is the device output capacitance and C_p is the transformer primary winding capacitance (which can be neglected since $C_p \ll 2C_{oss}$),

and taking into account that two output capacitances are present, effectively connected in parallel, the resonant capacitance C_r is:

$$C_r = 2C_{oss} + C_p \cong 2C_{oss} \tag{2.3}$$

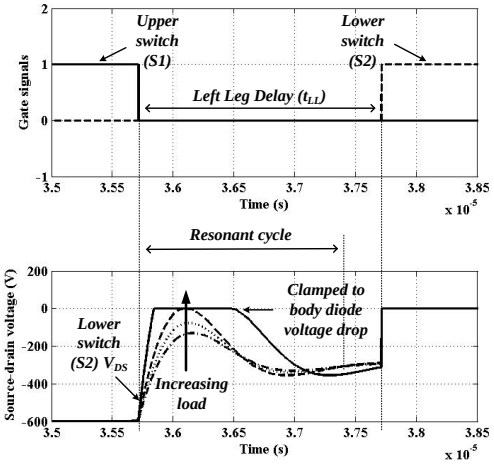


Figure 2.4: Large left leg transition delay (between *S1* and *S2*) showing the resonant waveform across *S2*

2.2.4 Circuit analysis

a. Power delivery interval (t_0 - t_1)

Switches *S1* and *S4* are switched on during this interval as shown in Figure 2.5a, and power is transferred to the load through diode *D5*. The transformer primary voltage and current are:

$$v_p(t) = V_{DC} \tag{2.4}$$

$$i_p(t) = \frac{N_s}{N_p} i_L(t) \tag{2.5}$$

where $i_L(t)$ is the instantaneous filter inductor current, N_s is the secondary transformer winding turns, and N_p is the primary transformer winding turns. Assuming linearly increasing current, the primary current can be expressed as:

$$i_p(t) = i_1 + \left(\frac{v_s - v_{Load}}{L_f}\right)\left(\frac{N_s}{N_p}\right)t \tag{2.6}$$

where i_1 is the initial primary current at the beginning of the power delivery period and $(v_s - v_{Load})/L_f$ is the filter inductor current slope (where v_s is the transformer secondary voltage and v_{Load} is the load voltage), referred to the primary side by multiplying by N_s / N_p.

b. Right leg transition interval ($t_1 - t_2$)

The equivalent circuit showing the active components through this period is illustrated in Figure 2.5b. Switch *S4* is turned off, and resonance occurs between the reflected inductance and the associated output capacitances. The output capacitance C_4 is charged from *0* to V_{DC}, while the output capacitance C_3 is discharged from V_{DC} to *0*. Consequently, the body diode of *S3* is turned on. Since the output capacitance of the switch is small, the primary current can be assumed to be constant during this interval, and the capacitor voltages can be expressed as:

$$v_{C3}(t) = V_{DC} - \frac{1}{C_r}\int_{t_1}^{t} i_p(\tau)\,d\tau \cong V_{DC} - \frac{n i_L(t_1)}{C_r}(t - t_1) \tag{2.7}$$

$$v_{C4}(t) = \frac{1}{C_r}\int_{t_1}^{t} i_p(\tau)\,d\tau \cong \frac{i_p(t_1)}{C_r}(t - t_1) = \frac{n i_L(t_1)}{C_r}(t - t_1) \tag{2.8}$$

where *n* is the transformer turns ratio (N_s/N_p). It is clear that charging and discharging the output capacitances C_3 and C_4 is predominantly controlled by the load current. This period should be adequately adjusted to assure *S3* ZVS turn-on in the next period. The transformer primary voltage can also be assumed to decay linearly to zero according to:

$$v_p(t) = V_{DC} - v_{c4}(t) \tag{2.9}$$

c. Freewheeling interval ($t_2 - t_3$)

S3 is turned on at zero voltage, since the body diode starts conducting during the previous interval. However, the body diode *D3* continues to share the primary current. No voltage is applied to the transformer primary winding, with current circulating through *S1*, *S3*, and *D3* as shown in Figure 2.5c. Hence, the secondary winding voltages are zero, and load current circulates through diodes *D5* and *D6*. Using linear approximations, and given that i_2 is the initial primary current at which this interval starts, the primary current can be obtained similar to Equation (2.6):

$$i_p(t) = i_2 - \left(\frac{v_{Load}}{L_f}\right)\left(\frac{N_s}{N_p}\right)t \tag{2.10}$$

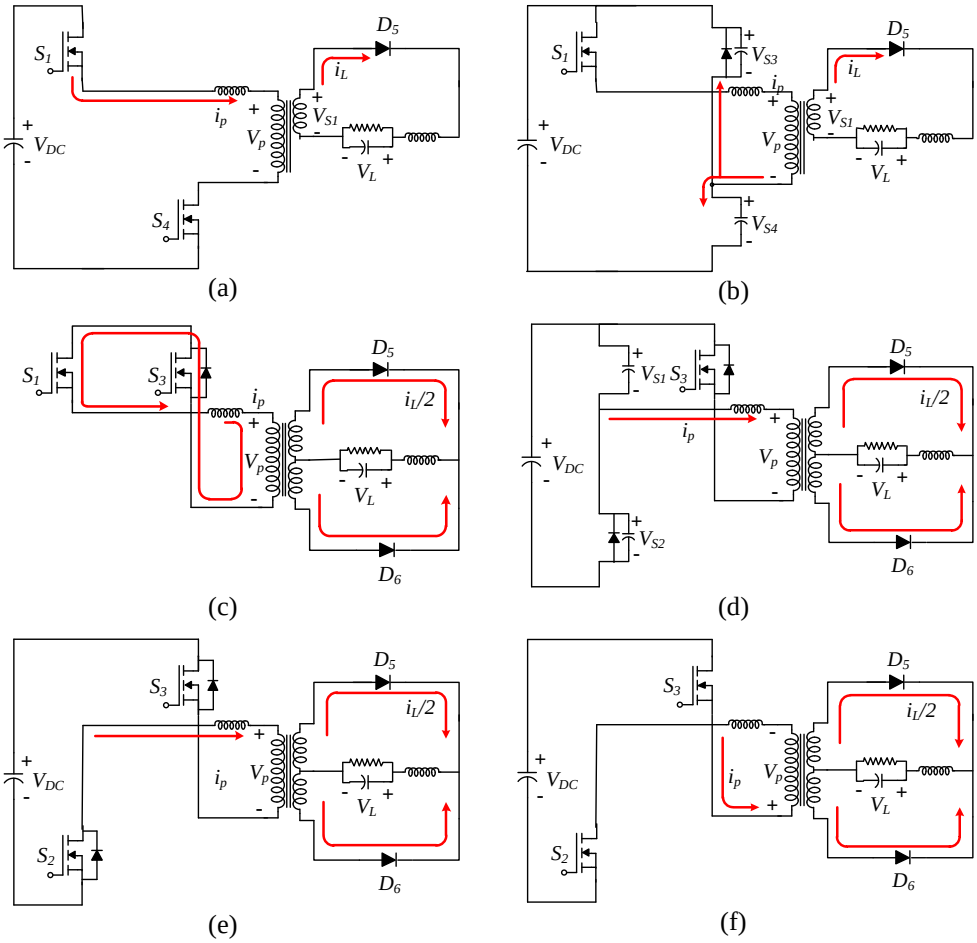


Figure 2.5: Equivalent circuit showing the conducting switching through: (a) Power delivery interval (t_0 - t_1), (b) Right leg transition interval ($t_1 – t_2$), (c) Freewheeling interval ($t_2 – t_3$), (d) Left leg transition interval ($t_3 – t_4$), (e) Slew interval ($t_4 – t_5$), and (f) Slew interval ($t_5 – t_6$)

d. Left leg transition interval ($t_3 – t_4$)

S1 is turned off at the beginning of this interval. The energy stored in the leakage inductance is used to charge C_1 from *0* to V_{DC}, and discharge C_2 from V_{DC} to *0*, as shown in Figure 2.5d. This forces the body diode *D2* to conduct. By using linear approximations, the capacitance voltages are:

$$v_{C1}(t) = \frac{1}{C_r}\int_{t_3}^{t} i_p(\tau)\,d\tau \cong \frac{i_p(t_3)}{C_r}(t - t_3) \tag{2.11}$$

$$v_{C2}(t) = V_{DC} - \frac{1}{C_r}\int_{t_3}^{t} i_p(\tau)\,d\tau \cong V_{DC} - \frac{i_p(t_3)}{C_r}(t - t_3) \tag{2.12}$$

The transformer primary voltage is:

$$v_p(t) = -v_{C1}(t) \tag{2.13}$$

The transformer primary voltage starts rising from 0 to $-V_{DC}$ at the end of this interval, while the primary current starts to decay governed by the leakage inductance, given that i_3 is the initial primary current at which this interval starts:

$$i_p(t) = i_3 - \left(\frac{V_{DC}}{L_{lk}}\right)t \tag{2.14}$$

e. Slew interval ($t_4 - t_5$)

This interval initiates when *S2* is turned on under a ZVS condition. The transformer primary voltage is $-V_{DC}$, and the primary current continues to decay according to Equation (2.14). Secondary winding voltages remain zero, since primary current did not reverse direction. Load current continues circulating through the two rectifier switches as shown in Figure 2.5e, and no power is delivered to the load (from the primary side). Body diodes *D2* and *D3* continue to share the primary current with switch *S2* until current reversal.

f. Slew interval ($t_5 - t_6$)

This interval is the same as the previous one, except that the primary current has reversed direction as shown in Figure 2.5f. Primary current flows through switches *S2* and *S3* respectively. This period terminates when the excess energy stored in the leakage inductance is all returned to the supply. Then a power delivery interval takes place, repeating the same sequence of intervals for the negative half cycle, which are shown in Figure 2.6.

2.2.5 Selecting the delay intervals

a. Left leg transition delay (t_{LL}):

Turn-on ZVS is achieved for the left leg switches *S1* and *S2* by switching the corresponding switch at the peak instant of the resonant waveform. That is, at one quarter of the resonant period:

$$t_{LL} = \frac{\pi}{2}\sqrt{L_r C_r} \tag{2.15}$$

b. Right leg transition delay (t_{RL}):

During this transition, both the energy stored in the transformer leakage inductance and the load inductance is used to achieve ZVS for switch *S3*. By substituting $v_{c3}(t_2) = V_{DC}$ in Equation (2.8):

$$\Delta t_{23} = t_{RL} = \frac{V_{DC}}{i_p} C_r \tag{2.16}$$

To ensure ZVS operation, the right leg transition delay should be selected to be greater than Δt_{23}, say twice this value [2.22]:

$$t_{RL} = \frac{2V_{DC}C_r}{i_{max}} \tag{2.17}$$

where i_{max} is to be substituted with the peak primary current. In this case ZVS operation may be lost at light loads.

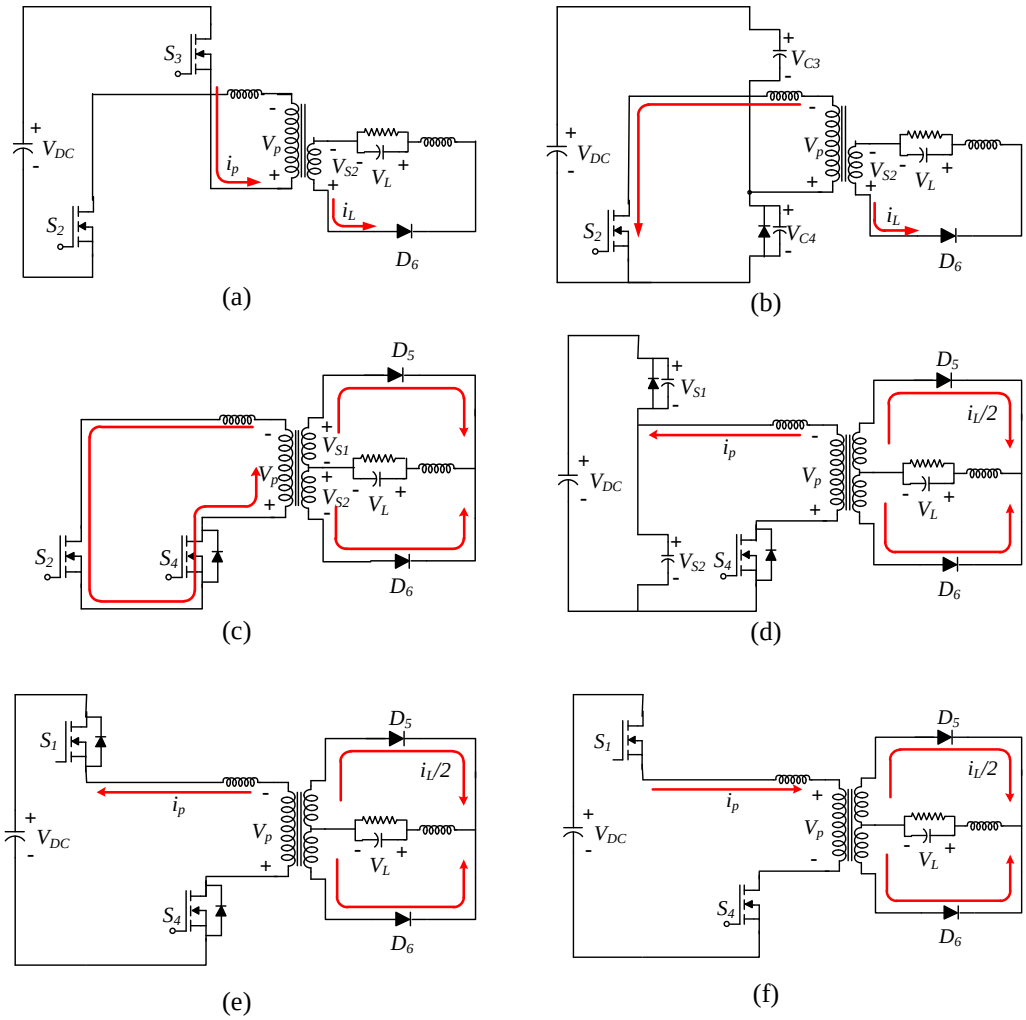


Figure 2.6: Equivalent circuit showing the conducting switching through: (a) Power delivery interval ($t_6 - t_7$), (b) Right leg transition interval ($t_7 - t_8$), (c) Freewheeling interval ($t_8 - t_9$), (d) Left leg transition interval ($t_9 - t_{10}$), (e) Slew interval ($t_{10} - t_{11}$), and (f) Slew interval ($t_{11} - t_{12}$)

To maintain a wider ZVS range, the right leg transition interval can be chosen at the minimum primary current required to achieve ZVS. That is, when the energy stored in the leakage inductance is equal to the energy stored in the resonant capacitance:

$$\frac{1}{2}C_r V_{DC}^2 = \frac{1}{2}L_r i_{min}^2 \tag{2.18}$$

$$i_{min} = \sqrt{\frac{C_r V_{DC}^2}{L_r}} \tag{2.19}$$

where i_{min} is the minimum primary current at which ZVS occurs. A more accurate approach to calculate the minimum current, is to consider the capacitance variation with source to drain voltage in calculating the stored energy, which is given by [2.23]:

$$i_{min} = \sqrt{\frac{C_r \left(V_{OSS}\right)^{1/2} \left(V_{DC}\right)^{3/2}}{L_r}} \tag{2.20}$$

where V_{OSS} is the drain-source voltage at which the device output capacitance is given in the manufacturer's datasheet. However, when the right leg delay is calculated at the minimum primary current, additional power loss due to current circulating in the device body diode should be considered. The right leg delay is chosen according to Equations (2.16), (2.17) and (2.20):

$$t_{RL,min} \le t_{RL} \le t_{RL,max} = \frac{2V_{DC}C_r}{i_{max}} \le t_{RL} \le \frac{V_{DC}C_r}{i_{min}} \tag{2.21}$$

2.2.6 The effective duty cycle

During the slew interval, no energy is transferred to the load until the primary current reverses direction. This interval mainly depends on the reflected leakage inductance. During this interval, the load current circulates through both rectifier diodes since the transformer secondary voltage is zero. The primary duty cycle, as shown in Figure 2.7, may be defined as:

$$D = D_{eff} + \Delta D \tag{2.22}$$

where D is the primary voltage duty cycle (defined from 0 to 1), D_{eff} is the reflected effective secondary duty cycle, and ΔD is the duty cycle loss. The voltage across the leakage inductance can be approximated as:

$$V_{DC} = L_{lk}\frac{\Delta i_{slew}}{\Delta t} = L_{lk}\frac{i_3 + i_1}{\Delta D\, T/2} \tag{2.23}$$

Hence, the duty cycle loss is:

$$\Delta D = \frac{2L_{lk}}{V_{DC}} f_s (i_3 + i_1) \tag{2.24}$$

where f_s is the switching frequency. The currents i_3 and i_1 can be obtained from the secondary side inductor current:

$$i_3 = \left(I_{Load} + \frac{\Delta i_1^{'}}{2} - \Delta i_2^{'} \right) \frac{N_s}{N_p} \tag{2.25}$$

$$i_1 = \left(I_{Load} - \frac{\Delta i_1^{'}}{2} \right) \frac{N_s}{N_p} \tag{2.26}$$

where:

$$\Delta i_1^{'} = \frac{v_s - V_{Load}}{L_f} D \frac{T}{2} \tag{2.27}$$

$$\Delta i_2^{'} = \frac{V_{Load}}{L_f} (1 - D) \frac{T}{2} \tag{2.28}$$

by substituting into Equation (2.24):

$$\Delta D = \frac{2L_{lk}}{V_{DC}} f_s \left(2I_{Load} - \frac{V_{Load}}{L_f} (1 - D) \frac{T}{2} \right) \frac{N_s}{N_p} \tag{2.29}$$

The voltage transformation ratio for the DC/DC converter, neglecting inverter and rectifier switch voltage drops, can be approximated as:

$$\frac{V_{load}}{V_{DC}} = \frac{N_s}{N_p} D_{eff} \tag{2.30}$$

By substituting into Equation (2.29), and neglecting the term containing $(1 - D)$, since it is much smaller than $2I_{Load}$:

$$\therefore \Delta D = \frac{2L_{lk}}{V_{DC}} f_s \left(2I_{Load} \right) \frac{N_s}{N_p}$$

by substituting for the input voltage V_{DC} using Equation (2.30):

$$\therefore \Delta D = D_{eff} \frac{4I_{Load} L_{lk}}{V_{Load}} f_s \left(\frac{N_s}{N_p} \right)^2 \tag{2.31}$$

by substituting into Equation (2.22), given that $R_{Load}^{'} = (V_{Load} / I_{Load}) \times (N_p / N_s)^2$, the effective duty cycle is:

$$D_{eff} = \frac{D}{\left(1 + \frac{4L_{lk}}{R_{Load}^{'}} f_s\right)} \tag{2.32}$$

where $R_{Load}^{'}$ is the load resistance referred to the primary side. Secondary side voltage, filter inductor current, load current, and load voltage are shown in Figure 2.7.

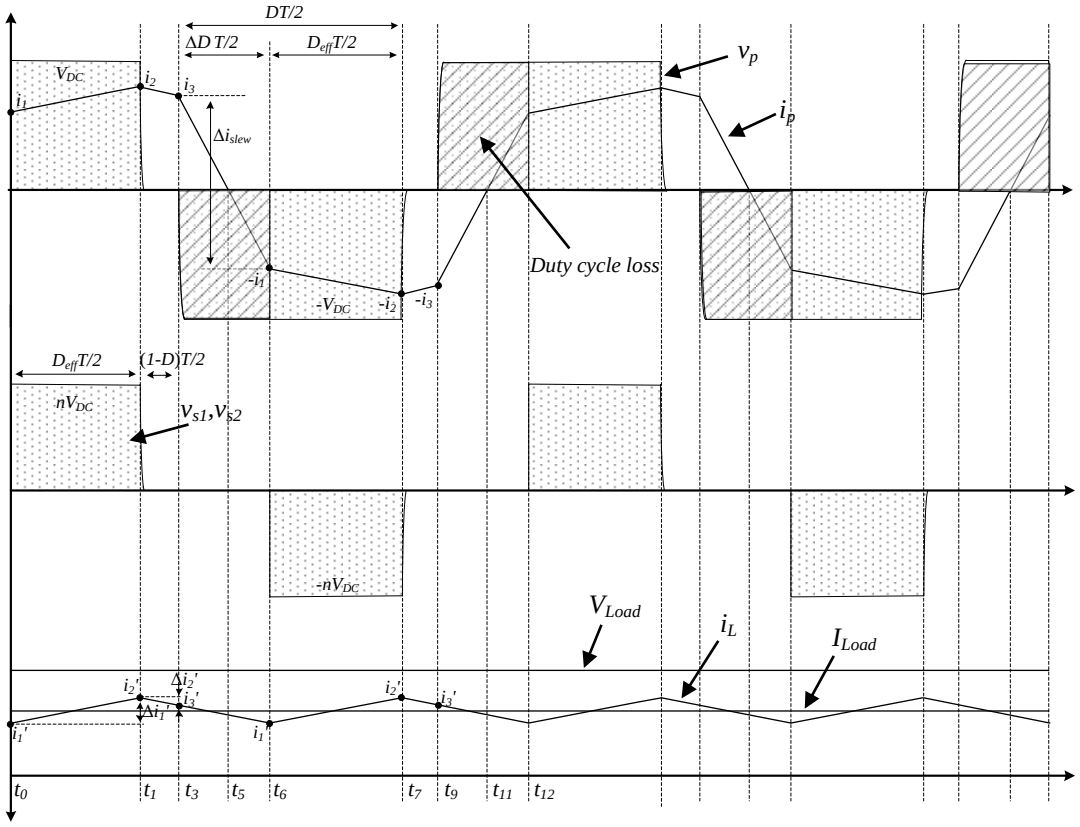


Figure 2.7: Primary voltage, primary current, transformer secondary voltage, filter inductor current, load voltage and load current waveforms, showing the duty cycle loss and the effective secondary duty cycle

2.2.7 Rectifier side ringing

The transformer leakage inductance, secondary winding capacitance, and the diode reverse recovery characteristics cause voltage ringing across each rectifier switch, with a resonating frequency of:

$$f_{rr} = \frac{1}{2\pi\sqrt{\left(N_s / N_p\right)^2 L_{lk} C_{rr}}} \tag{2.33}$$

where C_{rr} is the total secondary transformer winding and rectifier diode capacitances. This ringing can be adequately damped by using snubber circuits, or by using clamping circuits if snubber circuit power loss is too high.

2.2.8 Power loss analysis

Since all switches are turned on with ZVS conditions, the conduction power loss through each switch is only considered, and is calculated by substituting into:

$$P_{cond} = i_{rms}^2 R_{ds(on)} \tag{2.34}$$

The RMS current through each switch can be calculated by integrating the current waveforms in each interval, as illustrated in Appendix A1. Hence, the power losses in switches *S1* and *S2* are:

$$P_{S1,S2} = 2\left[\begin{array}{l}\left(i_1^2 + \frac{\Delta i_1^2}{3} + i_1\Delta i_1\right)D_{eff} + \left(i_2^2 + \frac{\Delta i_2^2}{3} - i_2\Delta i_2\right)(1-D) \\ +\left(\frac{1}{2}\times\frac{{i_3}^2}{3}\right)\frac{\Delta D}{2} + \left(\frac{i_1^2}{3}\right)\frac{\Delta D}{2}\end{array}\right]R_{ds(on)} \tag{2.35}$$

Noted that the primary current is shared between the switch and the body diode until current reversal during the interval ΔD_1. It is assumed that current is shared equally between the two devices. Similarly, for the right leg switches *S3* and *S4*:

$$P_{S3,S4} = 2\left[\begin{array}{l}\left(i_1^2 + \frac{\Delta i_1^2}{3} + i_1\Delta i_1\right)D_{eff} + \left(\frac{1}{2}\times\left(i_2^2 + \frac{\Delta i_2^2}{3} - i_2\Delta i_2\right)\right)(1-D) \\ +\left(\frac{1}{2}\times\frac{{i_3}^2}{3}\right)\frac{\Delta D}{2} + \left(\frac{i_1^2}{3}\right)\frac{\Delta D}{2}\end{array}\right]R_{ds(on)} \tag{2.36}$$

where it is assumed that the body diode equally shares the current with each switch in the intervals ΔD_1 and $(1-D)$. The power loss through the body diodes can be calculated by substituting into:

$$P_{diode} = V_{on} i_{av} \tag{2.37}$$

where V_{on} is the diode forward voltage drop, and i_{av} is the average current through the diode. Body diodes *D1* and *D2* power losses are:

$$P_{D1,D2} = 2V_{on}\left(\frac{i_3}{2}\right)\Delta D_1 \tag{2.38}$$

similarly, body diodes *D3* and *D4* power losses are:

$$P_{D3,D4} = 2V_{on}\left[\left(\frac{i_2 + i_3}{2}\right)(1-D) + \left(\frac{i_3}{2}\right)\Delta D_1\right] \tag{2.39}$$

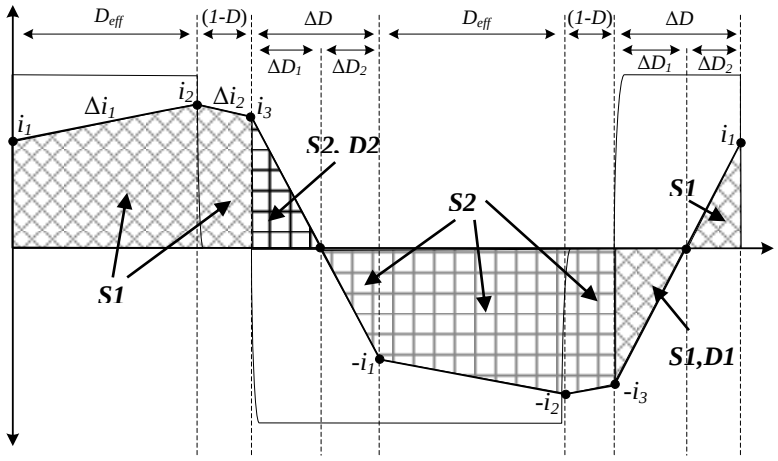
The intervals through which each switch and/or body diode is conducting during the positive and negative half cycles are given in Tables 2.2 and 2.3 respectively, and illustrated in Figures 2.8a and 2.8b.

Table 2.2: Switches and antiparallel diodes in conduction mode during the positive half cycle intervals

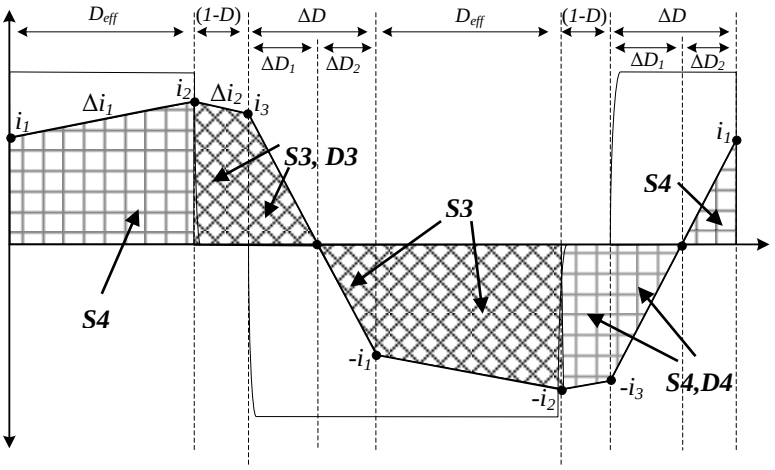
	Positive half-cycle			
Interval	**Power delivery**	**Freewheeling**	**Slew**	
Duration	D_{eff}	$1-D$	$\Delta D_1 = \Delta D/2$	$\Delta D_2 = \Delta D/2$
Switches in conduction	S_1, S_4	S_1, S_3	S_2, S_3	
Anti-parallel diodes in conduction	-	D_3	D_2, D_3	-

Table 2.3: Switches and antiparallel diodes in conduction mode during the negative half cycle intervals

	Negative half-cycle			
Interval	**Power delivery**	**Freewheeling**	**Slew**	
Duration	D_{eff}	$1-D$	$\Delta D_1 = \Delta D/2$	$\Delta D_2 = \Delta D/2$
Switches in conduction	S_2, S_3	S_2, S_4	S_1, S_4	
Anti-parallel diodes in conduction	-	D_4	D_1, D_4	-



(a)



(b)

Figure 2.8: primary current showing conduction through (a) left leg and (b) right leg switches

2.3 ZVS phase-shift PWM DC/DC converter design

Design data used for the DC/DC converter are given in Table 2.4. The MOSFET device IXFN32N120 is used, with rated voltage and current of 1200 V, 32 A respectively, and on-resistance of 0.35 Ω. The device datasheet is given in Appendix A. Noting that at the time of conducting the survey for device selection, the selected 1200 V MOSFET device showed the lowest on-resistance against amongst other lower voltage devices.

Table 2.4: Given data for the DC/DC converter circuit

Specification	Value
Input voltage (V_{DC})	600 V
Transformer turns ratio (N_p/N_s)	54:1
Transformer Leakage inductance (L_{lk})	43 µH
Filter Inductor (L_f)	250 nH
Load resistance (R_{Load})	0.0095 Ω
Operating frequency (f_s)	14 kHz

Two devices are used in parallel to reduce the conduction power loss and heat sinking requirements, and hence twice the effective switch output capacitance (2000 pF) is used as the resonant capacitance (and neglecting the transformer primary inter-winding capacitance). The transformer leakage inductance (43 µH) is used as the resonant inductance. The left leg delay, according to Equation (2.15), is:

$$t_{LL} = \frac{\pi}{2}\sqrt{L_r C_r} = 0.65\,\mu s \tag{2.40}$$

The minimum primary current to achieve zero voltage switching according to Equation (2.20), is:

$$i_{min} = \sqrt{\frac{C_r \left(V_{OSS}\right)^{1/2} \left(V_{DC}\right)^{3/2}}{L_r}} = 2.61A \tag{2.41}$$

The effective secondary duty cycle, at full primary duty cycle ($D = 1$), according to Equation (2.32), is:

$$D_{eff} = \frac{D}{\left(1 + \frac{4L_{lk}}{R'_{Load}} f_s\right)} = 0.92 \tag{2.42}$$

The rectifier switches are assumed to provide a voltage drop of 0.15 V, using synchronous rectification with 10 MOSFET devices in parallel per branch (each device having an on-resistance of 1.5 mΩ, and carrying approximately 100 A). The load voltage is:

$$V_{Load} = V_{DC} \times \frac{N_s}{N_p} \times D_{eff} - 0.15 = 10.07V \tag{2.43}$$

To calculate the conduction power loss, the current values (i_1, i_2, and i_3) and the current differences (Δi_1 and Δi_2) must be calculated. These are obtained by calculating the filter inductor current ripple using Equations (2.27), (2.28), and substituting ($D = 1$):

$$\Delta i'_1 = \frac{v_s - V_{Load}}{L_f} D_{eff} \frac{T}{2} = 136.5A \tag{2.44}$$

$$\Delta i'_2 = \frac{V_{Load}}{L_f}\left(1 - D\right)\frac{T}{2} = 0 \tag{2.45}$$

The currents i_1 and i_2 are:

$$i'_1 = I_{Load} - \frac{\Delta i'_1}{2} = \frac{V_{Load}}{R_{Load}} - \frac{\Delta i'_1}{2} = 992\,A \tag{2.46}$$

$$i'_2 = I_{Load} + \frac{\Delta i'_1}{2} = \frac{V_{Load}}{R_{Load}} + \frac{\Delta i'_1}{2} = 1128.5A \tag{2.47}$$

$$i'_3 = i'_2 - \Delta i'_2 = 1128.5A \tag{2.48}$$

Hence, the primary side currents (i_1, i_2, i_3, Δi_1, and Δi_2) are:

$$i_1 = 18.37\,A \tag{2.49}$$

$$i_2 = i_3 = 20.90A \tag{2.50}$$

$$\Delta i_1 = 2.52\,A \tag{2.51}$$

$$\Delta i_2 = 0 \tag{2.52}$$

Substituting into Equations (2.35), (2.36), (2.38) and (2.39), the total conduction power loss is:

$$P_{loss} = 127.4W \tag{2.53}$$

2.4 Simulation results

The Matlab Simulink model used for obtaining the simulation results is given in the Appendix. The left leg delay according to Equation (2.15) is:

$$t_{LL} = \frac{\pi}{2}\sqrt{L_r C_r} = 0.65\,\mu s \tag{2.54}$$

The right leg transition delay is chosen according to Equation (2.17):

$$t_{RL} = \frac{2V_{DC}C_r}{i_3} = 0.23\,\mu s \tag{2.55}$$

Gate signals for left and right arm switches, showing each bridge-arm transition delays at full primary duty-cycle (that is, zero phase shift between the leading and lagging bridge legs), are shown in Figure 2.9a and 2.9b respectively.

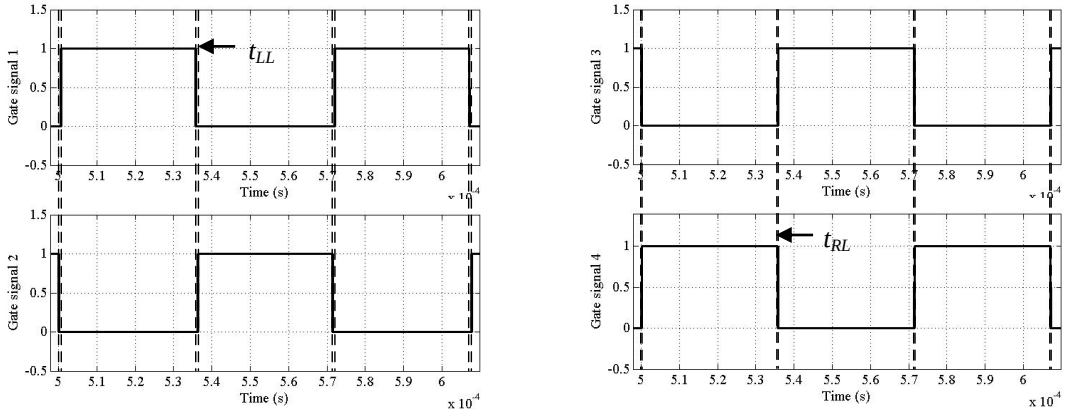
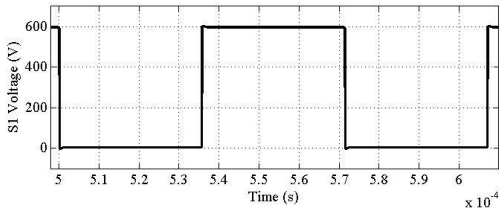
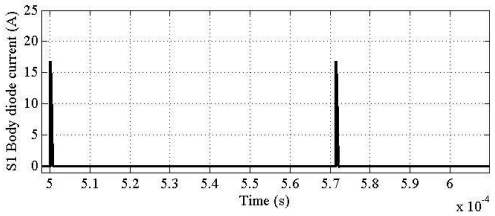


Figure 2.9: Gate signals to the (a) left bridge leg and (b) right bridge leg switches, showing the left leg and right leg transition delays

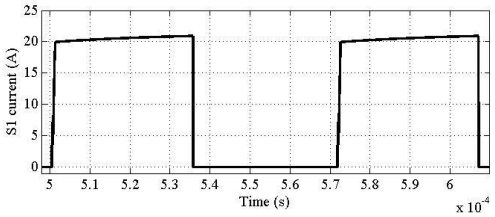
During the right leg and left leg delay intervals, the body diodes of the respective switches are forced to conduct. This is shown for switches *S1* and *S2* in Figure 2.10a and 2.10b respectively, and for switches *S3* and *S4* in Figure 2.10c and 2.10d respectively, where the voltage drop across the switches, body diode current conduction, and main switch currents are plotted for each switch.



(i) Voltage drop across S1

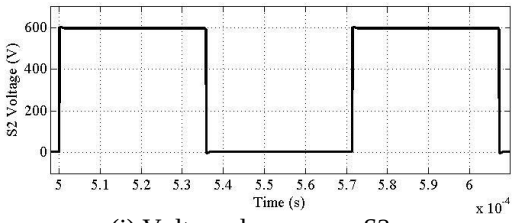


(ii) S1 body diode current

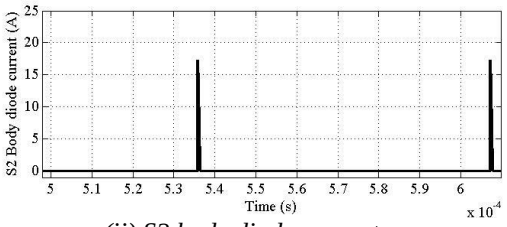


(iii) S1 current

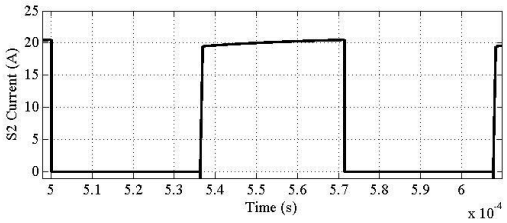
(a)



(i) Voltage drop across *S2*

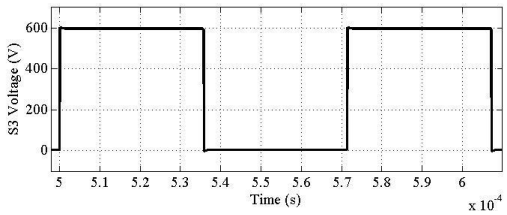


(ii) S2 body diode current

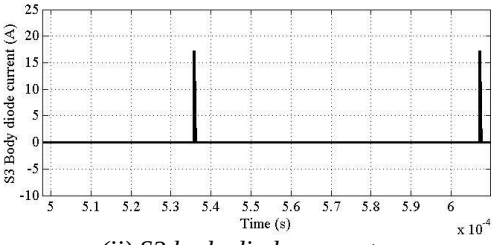


(iii) S2 current

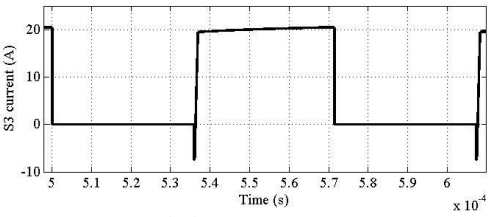
(b)



(i) Voltage drop across S3

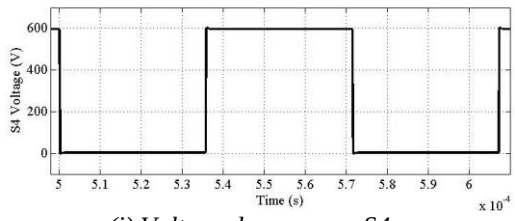


(ii) S3 body diode current

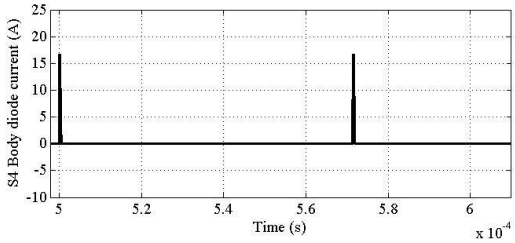


(iii) S3 current

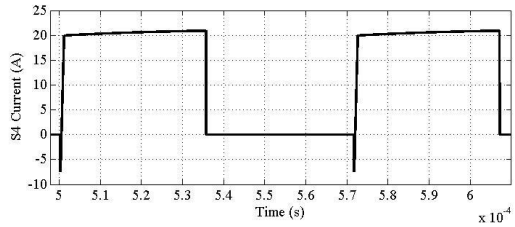
(c)



(i) Voltage drop across S4



(ii) S4 body diode current



(iii) S4 current

(d)

Figure 2.10: Zero voltage switching operation; (i) switch voltage, (ii) switch body diode current, and (iii) main switch current, for switches (a) *S1*, (b) *S2*, (c) *S3*, and (d) *S4*

Primary voltage and current waveforms are shown in Figure 2.11, parts a and b, respectively. Transformer secondary voltage duty cycle loss is observed in Figure 2.11c, during which the primary current reverses direction and the secondary voltage is zero. Filter inductor current is also shown in Figure 2.12. Finally, load voltage and current are shown in Figure 2.13a and 2.13b respectively.

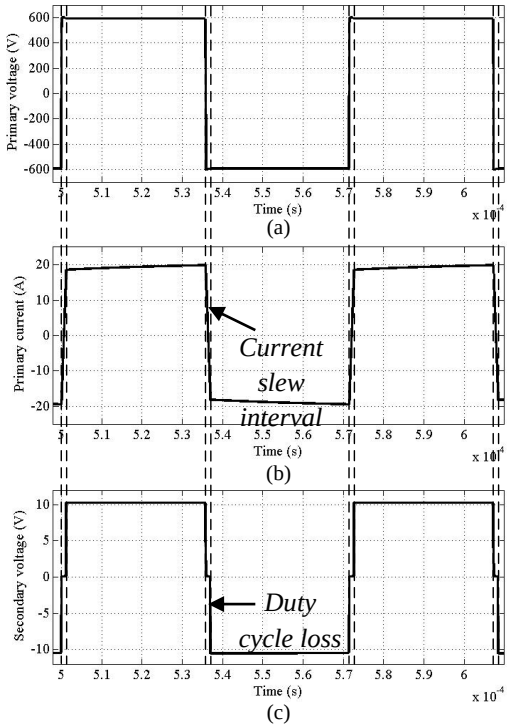


Figure 2.11: Inverter output at full duty cycle; (a) transformer primary voltage, (b) current, and (c) secondary voltage, showing the secondary side duty cycle loss

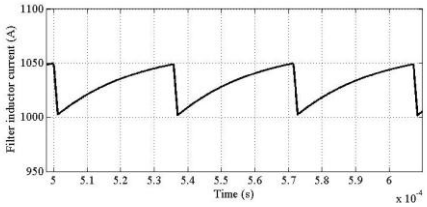


Figure 2.12: Filter inductor current

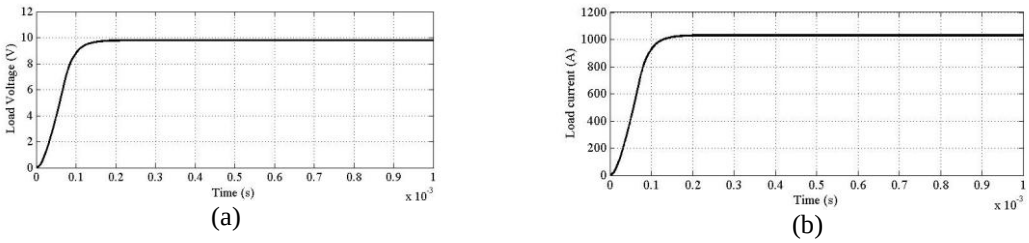


Figure 2.13: (a) Load voltage, and (b) load current

The effective secondary duty cycle obtained by simulation is approximately 0.88, while the total bridge power loss is approximately 143.1 W.

2.5 Summary and discussion

The ZVS phase shift PWM topology has been briefly discussed. Various design considerations, power loss analysis, as well as expressions for the different variables required for obtaining a successful design are also presented. Finally, the initial design of the 600 V, 14 kHz inverter, to be utilised in the high-current low-voltage DC/DC converter is presented, showing various design procedures, power loss analysis, and simulation results.

References

[2.1] R.W. Erickson, D. Maksimovic, *"Fundamentals of Power Electronics, Second Edition"*, Kluwer Academic Publishers, ISBN: 0-7923-7270-0, 2004.

[2.2] J.A. Sabate, V. Vlatkovic, R.B. Ridley, F.C. Lee, B.H. Cho, *"Design considerations for high-voltage high-power full-bridge zero-voltage-switched PWM converter"*, Fifth Annual Applied Power Electronics Conference and Exposition, APEC '90., pp. 275 - 284, 1990.

[2.3] M.M. Jovanovic, F.C.Y. Lee, D.Y. Chen, *"A zero-current-switched off-line quasi-resonant converter with reduced frequency range: analysis, design, and experimental results"*, IEEE Transactions on Power Electronics, Volume 4, pp. 215 - 224 1989.

[2.4] I.J. Pitel, *"Phase-Modulated Resonant Power Conversion Techniques for High-Frequency Link Inverters"*, IEEE Transactions on Industry Applications, Volume 22, pp. 1044 - 1051, 1986.

[2.5] W.A. Tabisz, F.C.Y. Lee, *"Zero-voltage-switching multiresonant technique-a novel approach to improve performance of high-frequency quasi-resonant converters"*, IEEE Transactions on Power Electronics, Volume 4, pp. 450 - 458, 1989.

[2.6] F.-S. Tsai, P. Materu, F.C.Y. Lee, *"Constant-frequency clamped-mode resonant converters"*, IEEE Transactions on Power Electronics, Volume 3, pp. 460 - 473, 1988.

[2.7] I.-D. Kim, E.-C. Nho, G.-H. Cho, *"Novel constant frequency PWM DC/DC converter with zero voltage switching for both primary switches and secondary rectifying diodes"*, IEEE Transactions on Industrial Electronics, Volume 39, pp. 444 - 452, 1992.

[2.8] R. Ayyanar, N. Mohan, *"Novel soft-switching DC-DC converter with full ZVS-range and reduced filter requirement. I. Regulated-output applications"*, IEEE Transactions on Power Electronics, Volume 16, pp. 184 - 192, 2001.

[2.9] R. Ayyanar, N. Mohan, *"Novel soft-switching DC-DC converter with full ZVS-range and reduced filter requirement. II. Constant-input, variable-output applications"*, IEEE Transactions on Power Electronics, Volume 16, pp. 193 - 200, 2001.

[2.10] D.-Y. Lee, B.-K. Lee, S.-B. Yoo, D.-S. Hyun, *"An improved full-bridge zero-voltage-transition PWM DC/DC converter with zero-voltage/zero-current switching of the auxiliary switches"*, IEEE Transactions on Industry Applications, Volume 36, pp. 558 - 566, 2000.

[2.11] P.K. Jain, W. Kang, H. Soin, Y. Xi, *"Analysis and design considerations of a load and line independent zero voltage switching full bridge DC/DC converter topology"*, IEEE Transactions on Power Electronics, Volume 17, pp. 649 - 657, 2002.

[2.12] J.M. Zhang, X.G. Xie, X.K. Wu, Z. Qian, *"Comparison study of phase-shifted full bridge ZVS converters"*, IEEE 35th Annual Power Electronics Specialists Conference, PESC '04, Volume 1, pp. 533 - 539, 2004.

[2.13] R. Redl, L. Balogh, D.W. Edwards, *"Optimum ZVS full-bridge DC/DC converter with PWM phase-shift control: analysis, design considerations, and experimental results"*, Ninth Annual Applied Power Electronics Conference and Exposition, APEC '94., pp. 159 - 165, 1994.

[2.14] J.A. Sabate, V. Vlatkovic, R.B. Ridley, F.C. Lee, *"High-voltage, high-power, ZVS, full-bridge PWM converter employing an active snubber"*, Sixth Annual Applied Power Electronics Conference and Exposition, APEC '91, pp. 158 - 163, 1991.

[2.15] R. Redl, N.O. Sokal, L. Balogh, *"A novel soft-switching full-bridge DC/DC converter: analysis, design considerations, and experimental results at 1.5 kW, 100 kHz"*, IEEE Transactions on Power Electronics, Volume 6, pp. 408 - 418, 1991.

[2.16] N.H. Kutkut, D.M. Divan, R.W. Gascoigne, *"An improved full-bridge zero-voltage switching PWM converter using a two-inductor rectifier"*, IEEE Transactions on Industry Applications, Volume 31, pp. 119 - 126, 1995.

[2.17] J.-G. Cho, J.A. Sabate, G. Hua, F.C. Lee, *"Zero-voltage and zero-current-switching full bridge PWM converter for high-power applications"*, IEEE Transactions on Power Electronics, Volume 11, pp. 622 - 628, 1996.

[2.18] J.-G. Cho, J.-W. Baek, C.-Y. Jeong, D.-W. Yoo, K.-Y. Joe, *"Novel zero-voltage and zero-current-switching full bridge PWM converter using transformer auxiliary winding"*, IEEE Transactions on Power Electronics, Volume 15, pp. 250-257, 2000.

[2.19] J.G. Cho, *"IGBT based zero voltage transition full bridge PWM converter for high power applications"*, IEE Proceedings - Electric Power Applications, Volume 143, pp. 475 - 480, 1996.

[2.20] J.G. Cho, J.A. Sabate, F.C. Lee, *"Novel full bridge zero-voltage-transition PWM DC/DC converter for high power applications"*, Ninth Annual Applied Power Electronics Conference and Exposition, APEC '94, Volume 1, pp. 143 - 149, 1994.

[2.21] X. Feng, X. DianGuo, L. YuXiu, *"A novel zero-voltage and zero-current-switching full-bridge PWM converter"*, The 29th Annual Conference of the IEEE Industrial Electronics Society, IECON '03, Volume 1, pp. 383 - 390, 2003.

[2.22] B.-R. Lin, K. Huang, D. Wang, *"Analysis and implementation of full-bridge converter with current doubler rectifier"*, IEE Proceedings - Electric Power Applications, Volume 152, pp. 1193 - 1202, 2005.

[2.23] D.J. Hamo, *"A 50W, 500kHz, Full-Bridge, Phase-shift, ZVS isolated DC to DC converter using the HIP4081A"*, Intersil Intelligent Power - AN9506, 1995.

Chapter 3

Cryogenic Operation of MOSFETs

Several semiconductor devices have been tested at cryogenic temperatures to show potential benefits, such as the possibility of operating at higher frequencies, reduced power loss, and improved reverse recovery characteristics. MOSFET devices have shown the best operation improvements, mainly due to the on-resistance reduction. However, most reported experiments are carried out on discrete devices, and no complete experimental survey on commercially available devices is available. Additionally, devices are not specified by the manufacturer to operate at cryogenic temperatures.

This chapter presents an experimental survey of MOSFET device on-resistance reduction factors for 16 commercially available MOSFET devices, covering most voltage and current ratings, to show the most suitable devices for such operation. Applicability to the high voltage inverter devices or to the low voltage synchronous rectifier devices, as well as considerations for attaining a reliable operation, are then discussed.

3.1 Background

Many applications require cryogenic cooling, such as applications integrating superconducting materials (superconducting power transmission and distribution, high temperature superconducting transformers, superconducting motors and generators, energy storage systems based on superconducting inductors or cooled capacitors, and superconducting coils or magnets used in magnetic resonance imaging medical equipment and magnetically levitated trains). While other applications require electronic components to operate at cryogenic temperatures, such as outer space applications, military surveillance systems, and supercomputers. This started questioning for the possibility of using cryogenically cooled power electronic devices, and what performance benefits may be gained. In such operating conditions, power circuits are expected to operate with improved efficiency and reliability due to lower junction temperatures, and reduced overall footprint due to the improved thermal conductivity of silicon, as well as packaging materials [3.1].

The operating characteristics for different semiconductor devices have been previously reported at cryogenic temperatures, in which a few improvements contributing to the overall performance are discussed.

Silicon pn junction diodes exhibit increased forward voltage as the temperature decreases from 300K to 77K, decreased breakdown voltage, and reduced reverse leakage current and output capacitance. The forward voltage increases by approximately 40% at 1 A for a 200 V silicon diode as shown in [3.2]. Silicon diodes poses high temperature sensitivity and wide operating temperature ranges, which is achieved by carefully adjusting the doping profiles to minimise freezout effects, hence are typically used as temperature sensors in cryogenic thermometry in the range of 500K to 1.4K [3.3], [3.4]. The forward voltage for germanium power diodes also increase with decreased temperature, but is much less than that for Si power devices. A 100 V Ge diode shows half the forward voltage drop of that for a similar Si diode at 77K, as shown in [3.5]. The peak reverse recovery current for the Ge diode is also reduced to nearly half its value at 77K compared to that at 300K. However, reverse characteristics are similar for both Si and Ge diodes, as both show reduced peak reverse recovery current, reverse leakage current and breakdown voltage as temperature decreases to 77K. However, germanium based devices are usually preferred for power applications operating at cryogenic temperatures down to 20K, due to the higher electron and hole mobilities and lower dopant freezout temperatures compared to that of silicon devices, and more importantly due to their lower forward voltage drops [3.5].

Cryogenically cooled P-i-N power diodes show an increased forward voltage drop at low current densities, while it decreases when operated at currents exceeding rated value. The forward voltage of a 1200 V P-i-N diode increases by 20% as the temperature decreases from 300K to 77K and operated at rates current (4 A), while it decreases by 15% with the decrease in temperature when operated at 2.5 times rated current (10 A). Both cases showed approximately the same forward voltage drop at 77K. Moreover, reduced reverse recovery characteristics (reduced peak reverse current and di/dt) are obtained at 77K, hence cryogenically cooled P-i-N diodes can be operated at higher switching frequencies as well as higher current densities [3.6].

Silicon Schottky barrier diodes are reported to exhibit an increased forward voltage drop of up to 50% at 77K, and a dramatically reduced reverse leakage current [3.2]. The ideal

breakdown voltage of silicon Schottky diodes is predicted to increase to approximately twice their value at room temperature compared to that at 77K [3.7]. Silicon carbide Schottky diodes which are best suited for high voltage applications (due to their lower switching losses and reverse recovery characteristics) also show increased forward voltages at lower temperatures, and reduced reverse leakage currents. Forward voltage drop increased by 43% and 53% for 300 V and 600 V devices respectively as shown in [3.8]. However, no significant change with temperature is typically observed for SiC Schottky diode switching losses, and such devices are best operated at high temperatures [3.9].

Bipolar junction transistors (BJTs) suffer from decreased current gains, and increased base-emitter and collector-emitter voltage drops at 77K. Collector-emitter breakdown voltage increases, while collector-base breakdown voltage decreases as the temperature is reduced from 300K to 77K. A 500 V, 4 A BJT is operated at 77K in [3.10], during which the current gain decreased by 13 times, collector-base breakdown voltage decreased by 1.2 times, collector-emitter breakdown voltage increased by 1.2 times, and a 3.5 times reduction in fall times is achieved. BJTs may be optimised for 77K operation by reducing the emitter doping concentration and increasing the emitter area to reduce bandgap narrowing effects and maintain a constant gain for different collector currents at the same collector emitter breakdown voltage. An optimised BJT for 77K operation has 2.5 times die area, while switching times decreased by 12 times, compared to 300K optimised devices [3.10]. As mentioned, germanium device are more suitable for operation at cryogenic temperatures lower than 77K. A 50 V, 5 A SiGe heterojuction bipolar transistor, in conjunction with a SiGe diode, used in a boost power converter, showed a conversion efficiency of 90% at 40K compared to 75% at room temperature [3.11].

MOSFET devices have gained considerable attention due to their improved performance at cryogenic temperatures. The reduced on-state channel resistance is the main improvement, which is due to the increase in carrier mobilities at lower temperatures [3.12]. Moreover, carrier freezout does not occur at cryogenic temperatures below 40K due to the vertical field caused by the gate voltage across the channel, which ionises the frozen-out channel carriers [3.13]. However, this is not the case for high voltage devices in which the channel resistance is dominated by the drift region resistance, and carrier freezout is observed at temperatures below 30K [3.14].

Reported channel resistance reductions are 21, 13, 11, 3.33, 2.14, 7.25, and 1.2 times for 1000 V, 700 V, 500 V, 250 V, 50 V, 30 V, and 16 V devices respectively in [3.12], [3.15], [3.16], [3.17], and [3.18]. The on-resistance reduction is higher for high-voltage devices due to the high drift region mobility temperature dependence [3.17]. An increase in the MOSFET device transconductance of 2-3 times at 77K is also noted in [3.12]. Device switching losses are also reported to decrease in both hard switching and soft switching topologies [3.19]. This is mainly contributable to the reduction in recovery characteristics of the device body diode in soft switching, and reduced device output capacitance in hard switching [3.17]. Significant reduction in reverse recovery times, and turn off current slopes are also shown in [3.20].

The downsides for MOSFET device cryogenic operation are decreased breakdown voltage and increased threshold voltage. A larger gate voltage may be required to form the inversion layer, so as to overcome the increased threshold voltage. Threshold voltages are reported to increase by approximately 1 V at 77K [3.12]. While breakdown voltages are reported to decrease by 19 to 23% in [3.20]. However, the overall device characteristics at 77K are considered to provide significant improvement. Applications such as resonant converters and high-current low-voltage synchronous rectification are reported to achieve higher conversion efficiencies at cryogenic temperatures [3.18], [3.21], [3.22], [3.23], [3.24], and [3.25].

IGBTs have similar device structures to MOSFETs, and are expected to achieve similar performance at cryogenic temperatures. The IGBT, during the on-state, is modelled as a MOSFET device feeding the base current of a p-n-p transistor [3.26].The forward voltage drop for a 600 V n-channel IGBT decreased until the temperature reached 195K and then increased [3.26]. This is due to the merged characteristics of the MOSFET and BJT devices. Conduction losses for punch through (PT) and non-punch through (NPT) 1200 V, 600 A IGBTs are observed to decrease as the temperature decreases from 300K to 250K, remaining near constant in the range 250K to 70K, and increase rapidly below 70K [3.27]. Increased threshold voltage at low temperatures is also reported, which is due to the reduction in the intrinsic carrier concentrations. Turn-off times decrease by a factor of 4 [3.28]. However, improvements in MOSFET device characteristics show better power saving benefits than IGBTs [3.29].

3.2 MOSFET device modelling

MOSFET devices are either n-channel or p-channel, which are subcategorised into depletion mode (normally on) and enhancement mode (normally off). However, the review presented in the following sections focuses on n-channel enhancement mode devices.

3.2.1 Basic device structures

The planar structure was the first form MOSFET devices, which evolved from the successful manufacture of JFETs. The manufacturing process basically starts by forming the silicon dioxide insulating layer on top of the p-type silicon crystalline slice by using a thermal process. Impurities with controlled levels of doping are then inserted either by diffusion or by ion implantation into photolithographic windows etched through the oxide layer, forming the source and drain n-regions. Finally, a conducting film is added and etched to form a pattern of source, drain, and gate interconnections on the surface [3.30]. A cross section view of one device cell is shown in Figure 3.1.

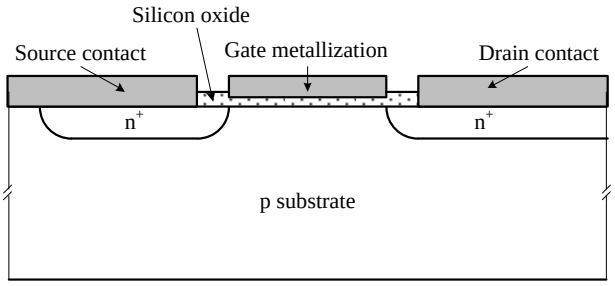


Figure 3.1: Planar MOSFET device structure

This device structure is widely used for NMOS and CMOS integrated components. For power applications, many individual planar devices are connected in parallel during the metallisation process. However, such a structure is not suitable for high voltage and high power applications, due to [3.30]:

- The drain-source spacing has to be increased to obtain high blocking voltage capabilities.
- Source, drain and gate connections are on the surface, which also complicates the metallisation process.
- The two previous points cause a low utilisation factor of utilised silicon die area.

However, the vertical MOSFET structure avoids the disadvantages mentioned above, in which the substrate material forms the drain contact, allowing current to flow vertically through the device [3.31]. A cross section view of a vertical double diffused device structure (VDMOS) is shown in Figure 3.2. The higher voltage blocking capability is obtained by increasing the thickness and reducing the doping level of the drift region.

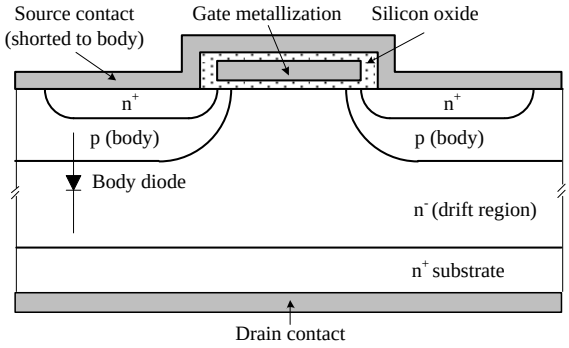


Figure 3.2: Vertical MOSFET (VDMOS) device structure

The on-resistance of VDMOS structures increases significantly for higher voltage devices, where the drift region contributes a major portion of the overall resistance. The drift region resistance contributes nearly 95% of the total on-resistance of 600 V devices, while almost 30% of 30 V devices [3.32]. However, the CoolMOS^{TM} structure presents a lower on-resistance device structure design, which is lower by a factor of 5 compared to VDMOS devices [3.33]. This is achieved by processing additional vertical p-stripes into the drift region and increasing the doping level by an order of magnitude. During reverse bias, a lateral electric field is built up, which drives the charge towards the contact regions, and the drift region acts as a voltage sustaining layer of a P-i-N structure [3.32]. A cross section view of a CoolMOS^{TM} cell structure is shown in Figure 3.3.

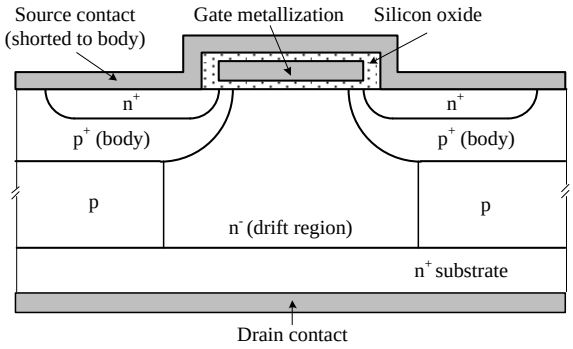


Figure 3.3: CoolMOS^{TM} device structure

3.2.2 MOSFET device operation

The basic operation of a power MOSFET depends on the formation of a conductive path between the n+ source and drift regions, due to the gate induced electric field. A MOSFET device is judged by the total current path resistance (on-resistance) during its on-state, the drain current rate of change with the gate bias rate of change (transconductance), and the device voltage blocking capability during the off-state [3.12]. However, a trade-off between on-resistance and breakdown voltage is due to the increased drift region thickness for higher blocking voltage requirements. The on-resistance, threshold voltage, transconductance, and breakdown voltage are all temperature dependant parameters. However, only on-resistance is considered during the analysis, as it is the parameter that contributes significantly to the device power loss, for the considered application.

3.2.3 Device on-resistance variation with temperature

The relation between on-resistance per unit area (R_{on}) and breakdown voltage (BV), for power MOSFET devices, is given by [3.34]:

$$R_{on} = 4.74 \times 10^{-9} BV^{2.5} \tag{3.1}$$

while, for CoolMOS^{TM} device structure [3.35]:

$$R_{on} = 2.6 \times 10^{-7} C_p BV \tag{3.2}$$

where C_p is the device cell pitch, and BV is the device breakdown voltage. This shows that CoolMOS^{TM} devices have lower on-resistance for the same breakdown voltage, at a given cell pitch. However, more specific relations are required to study temperature variation effects on channel resistance. The channel resistance of various MOSFET structures can be analysed by considering the basic n-channel lateral MOSFET structure. The structure consists of an n+ source and drain regions diffused into a p base region. The contact of the p-base region is also connected to the source contact, to account for breakdown voltage reductions caused by the internal parasitic bipolar transistor. When a positive gate bias (V_g), above the threshold voltage for the MOS structure (V_{th}), is applied to the gate electrode, an inversion layer is formed below the

gate to create the n-channel. Assuming a uniformly distributed charge across the channel, the charge in the channel under the gate is [3.34]:

$$Q = C_{ox}(V_g - V_{th}) \tag{3.3}$$

where C_{ox} is the oxide layer capacitance. A finite voltage drop, which opposes the applied gate bias, occurs across the channel due to its finite resistance. Consequently, the charge distribution across the inversion channel decreases linearly towards the drain end. Consider an elemental segment dx of the channel, located at a distance x from the source n+ region as shown in Figure 3.4. The resistance of this segment is [3.34]:

$$dR = \frac{dx}{W_{ch}\mu_{ni}Q(x)} \tag{3.4}$$

where W_{ch} is the channel width orthogonal to the cross section view, μ_{ni} is the inversion layer electron mobility, and $Q(x)$ is the charge in the inversion layer at this point [3.34]:

$$Q(x) = C_{ox}(V_g - V_{th} - V(x)) \tag{3.5}$$

and $V(x)$ is the local potential caused by the finite channel resistance at this point. The voltage drop across the element due to the channel current flow is:

$$dV = I_D dR \tag{3.6}$$

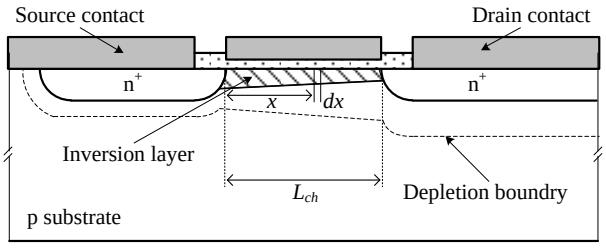


Figure 3.4: Lateral MOSFET structure showing the formed inversion layer

by substitution:

$$\int_0^{L_{ch}} I_D dx = W_{ch}\mu_{ni}C_{ox}\int_0^{V_D}(V_g - V_{th} - V)dV \tag{3.7}$$

where L_{ch} is the channel length.

By integrating, the drain current is [3.34]:

$$I_D = \frac{W_{ch}\mu_{ni}C_{ox}}{2L_{ch}}(2(V_g - V_{th})V_D - V_D^2) \tag{3.8}$$

which describes the device *I-V* characteristics in the saturated current regime of operation. When the drain bias voltage becomes very small compared to the gate voltage, the second term becomes negligible, and the device enters the linear regime of operation, described by:

$$I_D = \frac{W_{ch}\mu_{ni}C_{ox}}{L_{ch}}((V_g - V_{th})V_D) \tag{3.9}$$

where, the channel resistance can be defined as [3.34]:

$$R_{ch} = \frac{V_D}{I_D} = \frac{L_{ch}}{W_{ch}\mu_{ni}C_{ox}(V_g - V_{th})} \tag{3.10}$$

For a VDMOSFET structure, the on resistance is defined as the total resistance to current flow between the drain and source electrodes, which is described as [3.12], [3.34]:

$$R_{on} = R_{SC} + R_{n^+} + R_{ch} + R_A + R_{JFET} + R_D + R_{SUB} + R_{DC} \tag{3.11}$$

where R_{SC} is the source contact resistance, R_{n+} is the n^+ source region resistance, R_{ch} is the channel resistance, R_A is the accumulation region resistance, R_{JFET} is the JFET region resistance, R_D is the drift region resistance, R_{SUB} is the substrate resistance, and R_{DC} is the drain contact resistance; as shown in Figure 3.5.

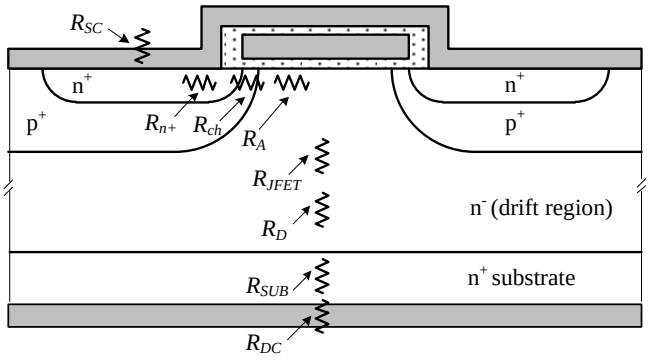


Figure 3.5: Power VDMOS structure showing the various internal resistances

The source contact resistance is determined by dividing the specific contact resistance by the contact area, and is given by [3.34]:

$$R_{sc} = \frac{2\rho_c}{W_{ch}(L_c - L_s)} \tag{3.12}$$

where L_c is the contact window length, and L_s is the n+ source ion implant window length. The n+ source region resistance is determined by the sheet resistance of the n+ diffusion (ρ_{n+}), and its length (L_{n+}) [3.34]:

$$R_{n+} = \rho_{n+} \frac{L_{n+}}{W_{ch}} \tag{3.13}$$

The channel resistance (R_{ch}) is determined as in the case of the lateral MOS structure [3.34]:

$$R_{ch} = \frac{L_{ch}}{W_{ch}\mu_{ni}C_{ox}(V_g - V_{th})} \tag{3.14}$$

where L_{ch} is usually defined as the difference between the p base depth and the n+ source junctions below the gate [3.34]:

$$L_{ch} = x_{jp} - x_{jn+} \tag{3.15}$$

where x_{jp} is the p base region junction depth, and x_{jn+} is the n+ source region junction depth. The accumulation resistance is defined as [3.34]:

$$R_A = \frac{L_A}{W_{ch}\mu_{nA}C_{ox}(V_g - V_{th})} \tag{3.16}$$

where μ_{nA} is the accumulation layer mobility. The JFET region resistance is [3.34]:

$$R_{JFET} = \frac{x_{jp}}{W_{ch}q\mu_{nB}N_D(L_g - 2x_{jp} - 2L_o)} \tag{3.17}$$

where μ_{nB} is the bulk mobility, q is the electron charge, N_{DJ} is the JFET doping concentration, L_g is the polysilicon gate length, and L_o is the zero bias depletion length of the JFET region.

The drift region resistance is given by [3.34]:

$$R_D = \frac{t}{W_{ch} q \mu_{nB} N_D (L_{cell} - a)} ln(\frac{L_{cell}}{a}) \tag{3.18}$$

where L_{cell} is the total cell length, and a is given by [3.34]:

$$a = L_g - 2x_{jp} - 2L_o \tag{3.19}$$

The substrate resistance is given by [3.34]:

$$R_{SUB} = \rho_{SUB} t_{SUB} \tag{3.20}$$

where ρ_{SUB} is the resistivity of the n+ substrate and t_{SUB} is the substrate thickness. The drain contact resistance can be similarly obtained by multiplying the material resistivity by the contact thickness. A titanium contact layer with a coating of nickel and silver is normally used. The dimensions used for the different resistances are shown in Figure 3.6.

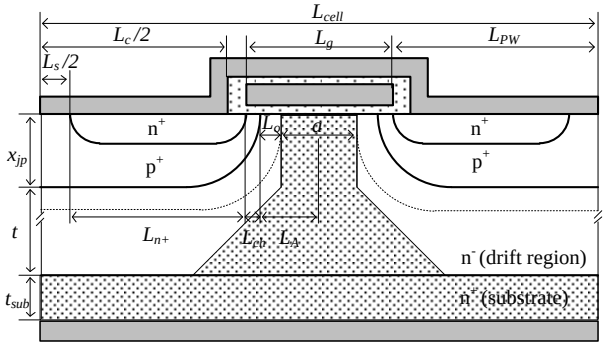


Figure 3.6: Power VDMOSFET structure showing the different dimensions used for the on-resistance analysis

The MOSFET on-resistance decreases with decreased temperature, due to the increase in electron mobilities at low temperatures. This is mainly due to the reduction in photon scattering, which is the dominant scattering mechanism in silicon. The temperature dependence for channel mobility (μ_{ni}), accumulation layer mobility (μ_{nA}), and bulk mobility (μ_{nB}) can be defined by the following relations [3.12]:

$$\mu_{ni} = 357(\frac{T}{300})^{-1.26} \qquad cm^2/V.\sec \tag{3.21}$$

$$\mu_{nA} = 757(\frac{T}{300})^{-0.81} \qquad cm^2 / V.\sec \tag{3.22}$$

$$\mu_{nB} = 1350(\frac{T}{300})^{-2.42} \quad T \succ 200K \tag{3.23}$$

$$\mu_{nB} = 3601(\frac{T}{300})^{-2} \qquad 77K \le T \le 200K \tag{3.24}$$

The drift region resistance contributes the major part of the total on-resistance for high voltage devices. Increasing the layer thickness and decreasing the doping concentration are used to increase the voltage blocking capability. However, the bulk mobility has a higher temperature sensitivity than other mobilities, with a greater reduction in the equivalent resistance for the higher voltage devices, due to the fact that this region is lightly doped. The on-resistance for CoolMOS^{TM} device structures is similar to the on-resistance of VDMOS structures, except that the drift region resistance is reduced due to the higher doping concentrations, with an approximately halved cross section area [3.36]. Hence, on-resistance reduction with temperature is expected to be less than that of VDMOS devices.

3.3 Experimental results

Experimental testing at liquid nitrogen temperature (77K) is carried out on various commercially available power MOSFET devices, with voltage ratings ranging from 24 V to 1500 V. Device datasheets are given in the Appendix. A cryogenic cooling system was built, consisting of a CryoTel^{TM} CT free-piston Stirling cold head provided by Sunpower Ltd, which provides a maximum cooling power of 30W. The cold head is placed inside a vacuum chamber to eliminate possible heat loading caused by convection, to obtain a fast cooling time constant, and to minimise air condensation. A schematic diagram for the cooling system and associated system component datasheets are given in the Appendix. The current ratings for the tested devices range from 160 A for the low voltage devices to 4 A for high voltage devices. Testing is carried out at low operating currents, to prevent self-heating of the devices and limit the heat load on the cooling head. Device self-heating increases device junction temperature, hence on-resistance measurements will not be at the required temperature. The cooling system operates in closed loop operation, where the temperature of the cold tip is measured to maintain a constant temperature of 77K over the heat loading range. The drain current is

measured for each device using a clamp meter, connected to the power circuit terminals. The device voltage drop is measured with two wires connected to the drain and source terminals using another feedthrough, to minimise the error in measurement caused by the voltage drop across the power terminals. A schematic diagram for the test circuit, and connections through the chamber are shown in Figure 3.7.

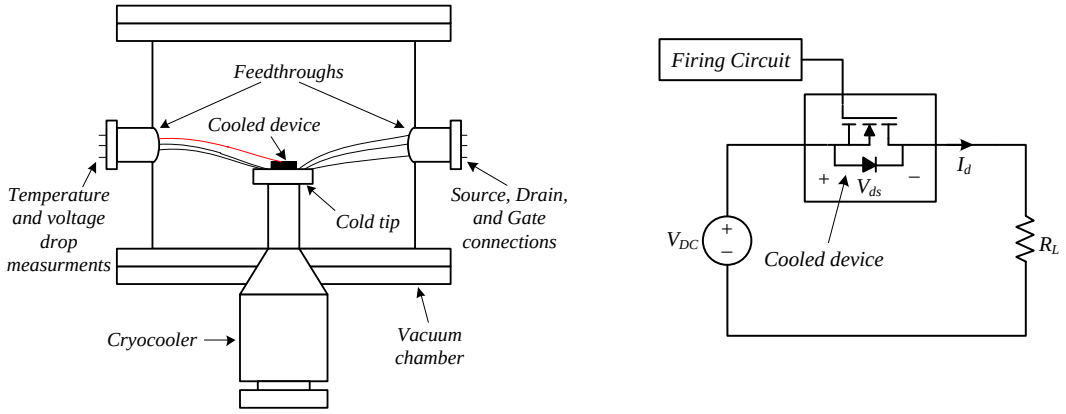


Figure 3.7: Cryogenic cooling setup: (a) Schematic diagram for the cooling head placed inside the vacuum chamber, showing power and measurement connections, and (b) circuit diagram for on-resistance measurement

The on-resistance is calculated at 77K by dividing the measured device voltage drop (V_{ds}) by the measured drain current (I_d). On-resistance measurements at 77K are compared with the expected on-resistance at 400K, which is the normal operating temperature of power devices, to obtain the on-resistance reduction factors. Experimental results are shown in Table 3.1, in which the voltage rating, current rating, measured on-resistance at 77K, expected on-resistance at 400K, and the on-resistance reduction factor are shown for each device. Reduction factors are plotted for each device in Figure 3.8, in which the CoolMos devices are highlighted in darker colour. 16 different devices where successfully tested. More detailed test results are given in Appendix B. The highest on-resistance reduction factors (F) are obtained for the high voltage devices, with reduction factors decreasing as the voltage rating decreases. This is mainly due to the lightly doped and thick layer drift region, which contributes to a major part of the total on-resistance of high voltage VDMOS devices. However, the high voltage CoolMOS^{TM} devices, which have lower on-resistance values, show lower reduction factors as expected, due to the higher drift region doping concentrations. Low voltage devices show the lowest on-resistance reduction factors as observed.

Table 3.1: Voltage rating, current rating, expected on-resistance at 400K, measured on-resistance at 77K, and on-resistance reduction factors for the tested MOSFET devices

	MOSFET	Vds(V)	Id(A)	Rds(400K)	Rds(77K)	F
1	**STP4N150**	1500	4	7.5 Ω	0.3744 Ω	20.03
2	**2SK3745LS**	1500	2	18.5 Ω	1.0286 Ω	17.98
3	**IXFK20N120**	1200	20	1.39 Ω	0.2567 Ω	5.41
4	**IXFN32N120**	1200	32	0.7875 Ω	0.108 Ω	7.2
5	**FQA11N90C**	900	11	2.09 Ω	0.07643 Ω	27.34
6	**IXKC25N80**	800	25	0.225Ω	0.0484 Ω	4.6
7	**IPP60R299**	650	11	0.49 Ω	0.05775 Ω	8.48
8	**FQP5N50**	500	5	2.52 Ω	0.1285 Ω	19.61
9	**IRFP340**	400	11	0.9625 Ω	0.05301 Ω	18.16
10	**FDPF33N25**	250	22	0.1739 Ω	0.01716 Ω	10.13
11	**IRFP4668**	200	130	14.4 mΩ	2.064 mΩ	9.62
12	**IRF510**	100	5.6	0.864 Ω	0.1554 Ω	5.56
13	**IRFb3207**	75	180	5.58 mΩ	1.745 mΩ	3.19
14	**IRLIZ34N**	55	22	52.5 mΩ	9.495 mΩ	5.53
15	**IRF4004**	40	350	1.8225 mΩ	0.489 mΩ	3.73
16	**IRF1324S7**	24	430	1.04 mΩ	0.528 mΩ	1.96

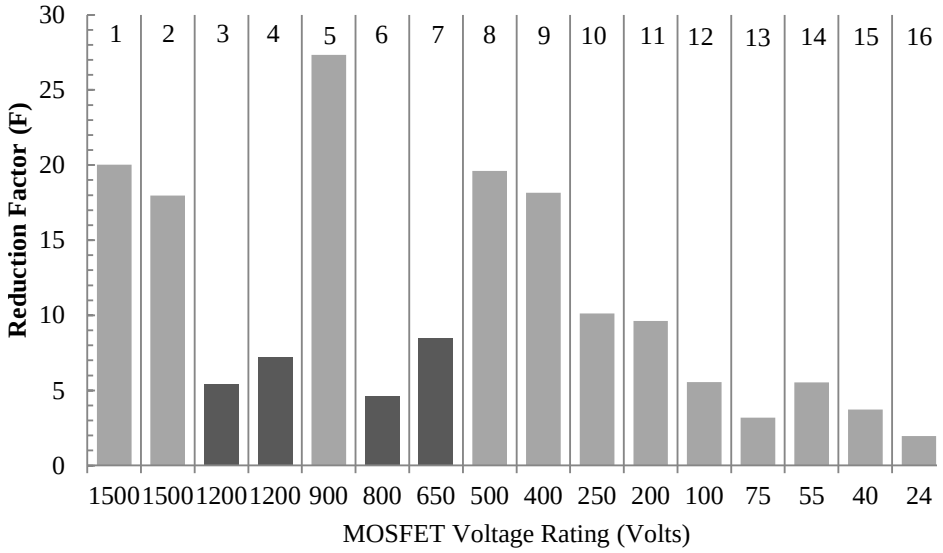


Figure 3.8: On-resistance reduction factors versus the device voltage rating

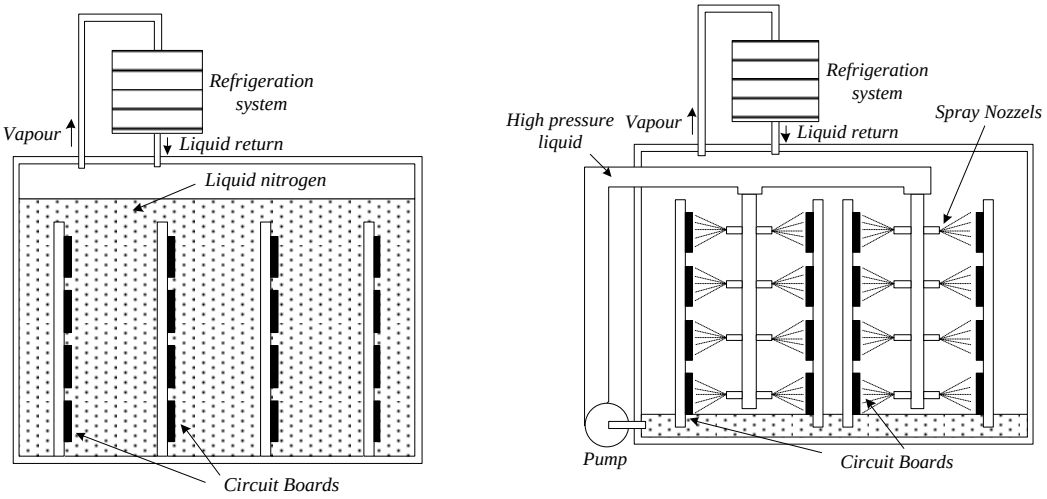
3.4 Power loss reduction and cooling penalty

To satisfy the main objective of cryogenic cooling that of improved overall system efficiency, the cooling penalty should be taken into account. The obtained on-resistance reduction factors, which show the amount of power loss reduction, must be greater than that required to produce refrigeration, in order to achieve energy saving. The ideal Carnot refrigeration efficiency, which is the ratio between the cooling power rate to the ideal power required to produce refrigeration (P), at the normal boiling point of liquid nitrogen (77K) in reference to room temperature (300K), is [3.23]:

$$\eta = \frac{Q}{P} = \frac{T_c}{T_h - T_c} = \frac{77}{300 - 77} = 0.3477 \tag{3.25}$$

This means that the ideal power required to produce 1W of cooling power at 77K, using liquid nitrogen, is $1/0.3477 = 2.88$ W. Liquid nitrogen can be produced in large quantities with 50% of the ideal Carnot cycle efficiency [3.23]. That is an inefficiency of $2.88/0.5 = 5.76$ W/W. An inefficiency factor of 8 to 10 W/W can be assumed by considering transportation, storage, and leakage losses. Therefore, cryogenic power cooling is considered beneficial for MOSFET devices with on-resistance reduction factors greater than 8 to 10, in which energy saving is possible. High voltage VDMOS devices, starting at 250 V devices, are thus considered the best candidates for cryogenic operation. However, the 650V and 800V CoolMOS^{TM} devices, and the 1200 V HiPerFET^{TM} show low on-resistance reduction factors, and will not provide significant energy saving in the case of cryogenic operation.

The previous method used for cryogenic testing of MOSFETs is not suitable for high power applications, due to the high cost, complexity, and low cooling power produced. Due to the high heat fluxes produced by MOSFET devices, two techniques can be adopted: direct immersion in a liquid nitrogen bath and liquid nitrogen spray cooling. The first cooling method can be expected to handle device heat dissipations up to 300 kW/m^2, while the second method can remove heat dissipations up to 1500 kW/m^2 [3.37]. These two cryogenic cooling techniques are shown in Figure 3.9.



(a) (b)

Figure 3.9: Cryogenic cooling methods: (a) immersion cooling and (b) spray cooling

3.5 Summary and discusion

MOSFET device operation at liquid nitrogen temperature is discussed through this chapter. The device on-resistance value at 77K is compared to the expected application operating temperature of 400K to obtain the on-resistance reduction factor. An experimental study on different MOSFET device voltage and current ratings showed that low-voltage devices exhibit the lowest on-resistance reduction factor (approximately 3 times), while it increased to 27 times for the high voltage devices. Applicability to the high voltage devices with reduction factors over 10 is considered advantageous even when taking the cooling power requirements into account (an inefficiency factor of 10 W/W) and an overall system efficiency increase is attained. However, it is not of benefit for the CoolMOS and HiperFET devices. None of the tested devices is rated for operation at temperatures below -50 ^{o}C, as specified by the manufacturer's datasheets. However, no device failure was observed among the tested devices. Failures in device internal and external connections are expected with increased thermal cycling, due to the difference in thermal expansion coefficients, and mechanical properties of the used materials. Special device packaging is then required for obtaining a failure free and reliable operation.

References

[3.1] R. Singh, B.J. Baliga, *"Cryogenic operation of p-i-n power rectifiers"*, Proceedings of the 5th International Symposium on Power Semiconductor Devices and ICs, ISPSD '93, pp. 193-198, 1993.

[3.2] K.B. Hong, R.C. Jaeger, *"Experimental survey of semiconductor power device operation at low temperature"*, Proceedings of the Workshop on Low Temperature Semiconductor Electronics, pp. 99-103, 1989.

[3.3] Y.M. Shwarts, V.N. Sokolov, M.M. Shwarts, I.A. Fedorov, E.F. Venger, *"Advanced silicon diode temperature sensors with minimized self-heating and noise for cryogenic applications"*, The Third International EuroConference on Advanced Semiconductor Devices and Microsystems, ASDAM'00, pp. 351-354, 2000.

[3.4] Y.M. Shwarts, M.M. Shwarts, S.V. Sapon, *"A new generation of cryogenic silicon diode temperature sensors"*, International Conference on Advanced Semiconductor Devices and Microsystems, ASDAM'08, pp. 239-242, 2008.

[3.5] R. Ward, W. Dawson, L. Zhu, R. Kirschman, O. Mueller, M. Hennessy, E. Mueller, R. Patterson, J. Dickman, A. Hammoud, *"Power diodes for cryogenic operation"*, IEEE 34th Annual Power Electronics Specialist Conference, PESC '03, pp. 1891-1896, 2003.

[3.6] R. Singh, B. Baliga, *"Cryogenic operation of P---i---N power rectifiers"*, Solid-State Electronics, Volume 37, pp. 1833-1839, 1994.

[3.7] B.J.B. Ranbir Singh, *"Cryogenic Operation of Silicon Power Devices - Power Electronics and Power Systems"*, Kluwer Academic Publishers, ISBN: 9780792381570, 1998.

[3.8] M. Shanbhag, T. Chow, *"Cryogenic operation of 4H-SiC Schottky rectifiers"*, Proceedings of the 14th International Symposium on Power Semiconductor Devices and ICs, pp. 129-132, 2002.

[3.9] B. Ozpineci, L. Tolbert, *"Characterization of SiC Schottky diodes at different temperatures"*, IEEE Power Electronics Letters, 1, pp. 54-57, 2003.

[3.10] R. Singh, B. Baliga, *"Cryogenic operation of power bipolar transistors"*, Solid-State Electronics, 39, pp. 101-108, 1996.

[3.11] R. Ward, W. Dawson, L. Zhu, R. Kirschman, G. Niu, R. Nelms, O. Mueller, M. Hennessy, E. Mueller, R. Patterson, *"SiGe Semiconductor Devices for Cryogenic*

Power Electronics–IV", Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, APEC'06, 2006.

[3.12] R. Singh, B. Baliga, *"Power MOSFET Analysis/Optimization for Cryogenic Operation Including the Effect of Degradation in Breakdown Voltage"*, Proceedings of the 4th International Symposium on Power Semiconductor Devices and ICs, ISPSD'92, pp. 339-344, 1992.

[3.13] S. Voges, M. Du Plessis, *"The Effect of the Vertical Electric Field on Freeze-out in MOS-Structures"*, Proceedings of the Workshop on Low Temperature Semiconductor Electronics, pp. 38-42, 1989.

[3.14] R. Karunanithi, A. Raychaudhuri, Z. Szücs, G. Shivashankar, *"Behaviour of power MOSFETs at cryogenic temperatures"*, Cryogenics, Volume 31, pp. 1065-1069, 1991.

[3.15] O. Mueller, *"Cryogenic MOSFET power conversion"*, Proceedings of the Workshop on Low Temperature Semiconductor Electronics, pp. 94-98, 1989.

[3.16] H. Ye, C. Lee, R. Simon, P. Haldar, M. Hennessy, E. Mueller, *"Liquid nitrogen cooled integrated power electronics module with high current carrying capability and lower on resistance"*, Applied Physics Letters, Volume 89, pp. 192107-192107-3, 2006.

[3.17] K. Shenai, *"Performance potential of low-voltage power MOSFET's in liquid-nitrogen-cooled power systems"*, IEEE Transactions on Electron Devices, Volume 38, pp. 934-936, 1991.

[3.18] R. Kawanami, T. Ishigohka, *"Low Temperature Characteristics of MOSFET Targeting Low-Voltage High-Current Power Source for Superconducting Magnets"*, IEEE Transactions on Applied Superconductivity, Volume 16, pp. 1630-1633, 2006.

[3.19] H. Li, D. Liu, C. Luongo, *"Investigation of potential benefits of MOSFETs hard-switching and soft-switching converters at cryogenic temperature"*, IEEE Transactions on Applied Superconductivity, Volume 15, pp. 2376-2380, 2005.

[3.20] O. Mueller, *"Properties of high-power Cryo-MOSFETs"*, Thirty-First IAS Annual Meeting, IAS'96, Conference Record of the IEEE Industry Applications Conference, pp. 1443-1448, 1996.

[3.21] B. Ray, S. Gerber, R. Patterson, I. Myers, *"77 K operation of a multi-resonant power converter"*, 26th Annual IEEE Power Electronics Specialists Conference, PESC'95, 1, pp. 55-60, 1995.

[3.22] A. Gardiner, S. Johnson, E. Schempp, *"Operation of power electronic converters at cryogenic temperatures for utility energy conditioning applications"*, IEEE Proceedings of the 31st Intersociety Energy Conversion Engineering Conference, IECEC 96. , pp. 2209-2214, 1996.

[3.23] O. Mueller, K. Herd, *"Ultra-high efficiency power conversion using cryogenic MOSFETs and HT-superconductors"*, 24th Annual IEEE Power Electronics Specialists Conference, PESC '93, pp. 772-778, 1993.

[3.24] T. Matsukawa, M. Shioyama, C. Neumeyer, S. Tsuji-Iio, R. Shimada, *"Operational loss reduction using power-MOSFET for magnetic field coil power supplies of nuclear fusion experimental machine"*, IEEE Transactions on Applied Superconductivity, Volume 12, 2002.

[3.25] Y. Kondo, S. Fukano, A. Ninomiya, T. Ishigohka, *"Cryogenic Low-Voltage/High-Current DC Power Source Using Multi-Parallel-Connected MOSFETs"*, IEEE Transactions on Applied Superconductivity, Volume 19, pp. 2337-2340, 2009.

[3.26] T. Chow, K. So, D. Lau, *"Performance of 600-V n-channel IGBTs at low temperatures"*, IEEE Electron Device Letters, Volume 12, pp. 498-499, 1991.

[3.27] A. Caiafa, A. Snezhko, J. Hudgins, E. Santi, R. Prozorov, *"IGBT operation at cryogenic temperatures: Non-Punch-Through and Punch-through comparison"*, IEEE 35th Annual Power Electronics Specialists Conference, Volume 4, pp. 2960-2966, 2004.

[3.28] R. Singh, B. Baliga, *"Cryogenic operation of asymmetric n-channel IGBTs"*, Solid-State Electronics, Volume 38, pp. 561-566, 1995.

[3.29] O. Mueller, *"Cryo-MOSFET and IGBT: a Comparison"*, Proceedings of the Second European Workshop on Low Temperature Electronics, pp. 219-224, 1996.

[3.30] V. Benda, J. Gowar, D. Grant, *"Power semiconductor devices: theory and applications"*, John Wiley & Sons Inc, ISBN: 9780471976448, 1999.

[3.31] Y. Tarui, Y. Hayashi, T. Sekigawa, *"Diffusion self-aligned metal-oxide-semiconductor transistor--a new approach for a high-speed device"*, Proceedings of the 1st Conference on Solid State Devices, pp. 105-110, 1969.

[3.32] L. Lorenz, G. Deboy, A. Knapp, M. Marz, *"COOLMOS—A new milestone in high voltage power MOS"*, IEEE 11th International Symposium on Power Semiconductor Devices and ICs, ISPSD '99, pp. 3–10, 1999.

[3.33] X. Chen, J. Sin, *"Optimization of the specific on-resistance of the COOLMOS"*, IEEE Transactions on Electron Devices, 48, pp. 344-348, 2002.

[3.34] B. Baliga, *"Fundamentals of power semiconductor devices"*, Springer Verlag, ISBN: 9780387473130, 2008.

[3.35] P.N. Kondekar, C.D. Parikh, M.B. Patil, *"Analysis of breakdown voltage and on resistance of super junction power MOSFET CoolMOS using theory of novel voltage sustaining layer"*, IEEE 33rd Annual Power Electronics Specialists Conference, PESC'02, Volume 4, pp. 1769-1775, 2002.

[3.36] P. Kondekar, M. Patil, C. Parikh, *"Analysis and design of superjunction power MOSFET: CoolMOS™ for improved on resistance and breakdown voltage using theory of novel voltage sustaining layer"*, IEEE 23rd International Conference on Microelectronics, MIEL'02, pp. 209-212, 2002.

[3.37] L. Chow, M. Sehmbey, J. Beam, *"Thermal management issues in cryo-electronics"*, IEEE Proceedings of the 31st Intersociety Energy Conversion Engineering Conference, IECEC 96, Volume 2, pp. 1367-1372, 2002.

Chapter 4

Nanocrystalline Core Based Transformer Design

Transformers are considered critical components that strongly influence high power converter dynamics, efficiency, and size. High-frequency power transformers are not available as standard wound components, and must be designed during the converter design process. The choice of core material significantly influences the overall transformer volume. Soft-magnetic properties contribute the main restrictions during the design process, as well as the available core geometries.

This chapter presents the design and implementation procedures for the high frequency transformer utilised in the high-current low-voltage DC/DC converter under study. Different core materials are first compared to select the appropriate core for this particular application. Leakage inductance calculation for a basic two winding transformer, and the effect of increased leakage on circuit performance are presented. Other design issues such as loss mechanisms in transformer windings and the core, termination, and implementation considerations are also discussed. Finite element analysis (2D and 3D) is carried out in addition to analytical calculations, in order to validate the design.

4.1 Background

Transformer operation is based on the theory of electromagnetism, discovered by Hans Christian Orsted in 1820 [4.1], and electromagnetic induction, discovered by Michael Faraday and Joseph Henry in 1831 [4.2]. Their discoveries are considered one of the most important basic laws of physics, upon which different electromagnetic devices are based. Discoveries continued thereafter, which lead to the first commercially used transformer, produced by George Westinghouse in 1886 [4.3]. The first resonant transformer for generating very high voltages at high frequencies was invented by Nikola Tesla in 1891 [4.4]. Transformers have been widely used since then for voltage step-up and step-down in electrical power transmission and different circuit applications such as measurement, audio circuits, and isolation requirements. Electrical applications have grown through the years in demand for different voltage/current levels, smaller volume, higher power density, lower output ripple, lower EMI, and higher efficiency

systems, which lead to the development of power converters capable of operating at higher frequencies. However, even with advancements in circuit topologies, challenges still exist due to the large footprint occupied by magnetic elements/components. Magnetic core materials represent the main restrictions in regards to volume reduction, as well as electromagnetic interference (EMI) and efficiency. A core material offering an ideally infinite permeability, saturation flux density, resistivity, and zero hysteresis loss would be an optimum choice. However, core materials have no such properties, and the design engineer is restricted to specific values.

A core is used in transformers to reduce the magnetic flux path reluctance, and to confine/guide the magnetic flux within this specified path [4.5]. The effect of magnetic fields produced by electric currents is concentrated within the core, and the magnetic field is then increased by a large factor if compared to that without a core. The main core material characteristics influencing the design and performance of transformers may be summarised as follows:

- Magnetic core geometry
- Air gap presence (only for inductors)
- Relative permeability
- Saturation flux density
- Resistivity
- Curie temperature
- Laminations and insulation dielectric loss
- Hysteresis and eddy current losses per unit volume

These core properties apply to both conventional 50 Hz and higher frequency transformers. The basic core geometries for conventional 50 Hz transformers are the core and shell type constructions [4.6]. Such geometries are also used for high frequency designs, while other geometries exist such as the toroidal shape and different planar geometries. The move towards planar structures in switched mode power supplies has provided lower profile designs, reduced high frequency winding losses, and the possibility of obtaining precise leakage inductance values [4.7]. Optimised low profile magnetic designs can have better volumetric efficiency and higher power density [4.8]. The ease of interleaving due to the use of PCB windings allows for leakage minimisation and control [4.9]. PCB windings also present an easily implementable

method for manufacturing. It is also clear that planar structures have lower core temperatures due to the larger surface area to volume ratio. However, planner structures possess a large footprint area, increased parasitic capacitance, low window utilisation factor, and are limited to certain applications, core materials, and ratings [4.7].

High frequency power transformer design has attained considerable attention over the past decade. High frequency operation adds additional considerations to the design process. The design constraints that should be considered are:

- Core loss (hysteresis and eddy loss)
- High frequency winding loss (skin and proximity losses)
- Temperature rise
- Winding layout, insulation, and termination
- Transformer parasitic components (leakage inductance and distributed capacitance)
- Cross regulation between multiple primaries and/or multiple secondaries

Core loss has been adequately modelled for sinusoidal and non-sinusoidal excitations [4.10], [4.11]. Winding skin and proximity losses can be minimised for simple winding structures by using stranded conductors, referred to as Litz wire [4.12]. For multi-layered windings, proximity loss can be reduced by properly interleaving the primary and secondary windings [4.13]. In the case of using foil windings; the high frequency winding losses can be reduced by optimum thickness selection [4.14]. Various design considerations and procedures have been discussed in [4.15]. Design optimisation has also been well presented in the literature. Optimisation based on finding the operating flux density where the core and winding losses are minimum is presented in [4.16], [4.17], [4.18], based on the minimum volume and power loss in [4.19], minimum weight in [4.20], and considering the maximum temperature rise in [4.16], [4.17], [4.18], [4.21], and [4.22].

Transformer parasitic elements, specifically leakage inductance, may be considered the largest single factor in degrading the performance of switch mode power supplies. It directly affects the application circuit losses, load regulation, and cross regulation for transformers with multiple outputs [4.23]. Minimisation of the leakage inductance is there for required. However, the leakage inductance is utilised in some resonant circuits,

and should be predefined according to the circuit requirements to avoid the addition of an extra inductive-component/circuit-element. The leakage inductance is a representation of imperfect magnetic coupling between transformer windings, caused by increased insulation thickness and/or winding miss-arrangement. The limitations introduced by its presence (internal losses and/or voltage drops) are considered an important design aspect for both 50 Hz and high frequency transformers.

The leakage impedance (which consists of resistive and reactive components) is usually determined using the standard transformer short circuit test. However, extensive research has been presented to evaluate its value analytically. A method for calculating winding resistance and leakage inductance variation with frequency, for single layer, multilayer, and sectionalised windings is presented in [4.24]. The DC values of the resistance and leakage inductance are first calculated, and then multiplied by the appropriate AC/DC factors to obtain the corresponding AC values. This method is widely used and has been extended to different winding types and configurations, specifically for the winding resistance [4.12], [4.25], [4.26], [4.27], [4.28], [4.29]. These factors basically compensate for skin and proximity effects. The leakage inductance can also be calculated using the magnetic flux linkage, reluctance, magnetic energy, small signal, or vector magnetic potential methods [4.5].

4.2 Objectives

The main objectives of this chapter may be summarised as follows:

- Design a high efficiency, low volume, high frequency power transformer satisfying the specifications listed in Table 4.1.
- Provide an implementable high current secondary winding and termination.
- Maintain a reduced volume design through the use of appropriate core materials.
- Model the transformer using analytical and FEA simulation techniques, and estimate core and winding losses.
- Estimate the leakage inductance for proper circuit application.
- Discus the effect of secondary winding termination on the reflected leakage inductance.

Table 4.1: Transformer specifications

Specification	Value
Peak primary voltage	600 V
Rectifier output voltage	8 V
Rectifier RMS current	1000 A
Primary winding configuration	Single Winding Input
Secondary winding configuration	Centre-tapped secondary
Operating frequency	$10kHz \leq f \leq 20kHz$
Operating duty cycle	98%
Volume requirements	Minimum Volume Design
Efficiency restrictions	$95\% \geq \eta \geq 98\%$

The transformer output voltage shall be specified during the design process, according to the leakage inductance and rectifier diode voltage drops. The operating frequency is specified as a range in order to select the appropriate operating frequency during the design process. This reduces the design constraints for selecting the core dimensions; specifically the cross sectional area for a certain geometry, which may lead to a more compact design.

4.3 High frequency transformer modelling

Magnetic devices, such as inductors and transformers, are widely used in different switching converter circuits. The design of such devices cannot be isolated from the converter design itself. Transformer operation and characteristics can be predicted before implementation through proper analysis and modelling. Prior knowledge of transformer non-ideal parameters is also a better approach for design optimisation rather than testing physical implementations. This also permits for circuit simulation of the power supply performance, which may reveal performance limitations attributable to the transformer design. Transformers are represented by an equivalent circuit model, in which the circuit elements can be directly related to transformer physical design, which may be modified in order to improve circuit performance. A two winding transformer equivalent circuit is shown in Figure 4.1. The circuit consists of the transformer loss components (primary and secondary copper winding resistances (R_1, R_2), equivalent core loss resistance (R_C), an ideal transformer with a specific turns ratio (N_1:N_2), and the different transformer parasitic reactive components (primary and secondary leakage inductances (L_{l1},L_{l2}), core magnetising inductance (L_M), and winding parasitic capacitances (C_1, C_2, and C_{12})).

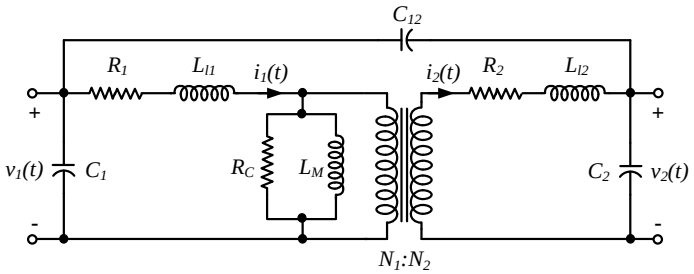


Figure 4.1: Two winding high frequency transformer equivalent circuit

4.3.1 Magnetising inductance

An approximate equivalent circuit representation for a two winding transformer, including the magnetising inductance is shown in Figure 4.2. The magnetising inductance models core magnetisation properties. A transformer saturates when the magnetic flux density exceeds the core material saturation flux density, at which the impedance of the magnetising inductance decreases, and the magnetising current increases dramatically.

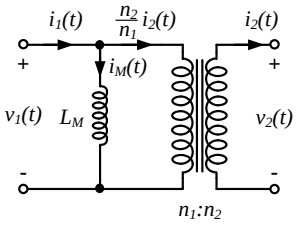


Figure 4.2: Transformer model including the magnetising inductance

Transformer saturation is a function of the applied volts-seconds ($V = N\,d\phi/dt$), not the primary or secondary currents. To avoid core saturation, the flux density should be decreased by increasing the number of turns, or by increasing the core cross sectional area ($V_1 = 4.44 N_1 B_{\max} A_c f_s$). It should be noted that the addition of an air gap to the core has no effect on the saturation level of conventional transformers, and is not employed in conventional designs. An air gap only decreases the magnetising inductance and increases the magnetising current, and affects the output characteristics of the transformer. The magnetising inductance and equivalent core loss resistance, model the non-ideal core properties. While the primary and secondary circuits are coupled through the basic ideal transformer equation:

$$\frac{v_1}{v_2} = \frac{i_2}{i_1} = \frac{N_1}{N_2} \tag{4.1}$$

4.3.2 Magnetic cores

The main purpose of the magnetic core is to provide a low reluctance magnetic path, to ease flux linkage, or magnetic coupling between two or more windings. The link between different windings through the specified magnetic path also provides electrical isolation between windings, and enables the adaptation of different voltage levels by adjusting the turns ratio. Magnetic cores are comprised of materials which can be readily magnetised and demagnetised. An AC waveform is required to continuously transfer energy through the core. The material response is represented by the *B-H* curve shown in Figure 4.3, which is characterised by the relative permeability, according to $B = \mu_o \mu_r H$.

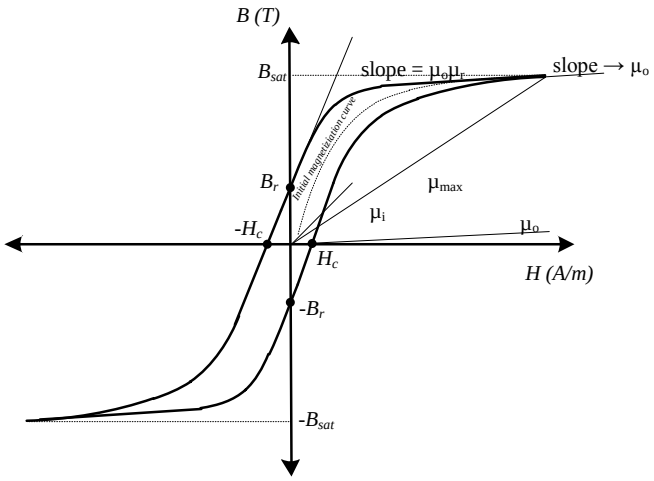


Figure 4.3: Hystresis B-H curve of a magnetic core material

No material can be completely demagnetised after magnetisation, and a residual flux B_r is retained. A reverse magnetic field intensity; the coercive force H_c, must be applied to remove this residual flux. The area enclosed by the *B-H* curve cycle represents the amount of unrecovered energy, known as the hysteresis core loss. The area of the *B-H* loop is narrow for soft magnetic materials, but widens as the frequency increases, due to eddy currents.

a. Core power loss

Increased core temperature due to core losses is one of the most important limitations in high frequency applications. Almost all magnetic materials are electrical conductors; hence eddy currents are induced due to the presence of changing magnetic fields. The total core loss is the sum of both hysteresis and eddy current losses.

i. Hysteriss core loss

Hysteresis loss is the energy required to align, rotate and reverse, etc…, the magnetic moments of the core material domains [4.5]. This loss component cannot be predicted from core material properties, and is usually calculated for a certain core material by experimental curve fitting. The area enclosed by the hysteresis curve represents the hysteresis loss per cycle. For an inductor excited by the periodical voltage $v(t)$, and current $i(t)$ having a frequency *f*, the energy delivered to the inductor over one cycle is:

$$W = \int_0^T v(t)\, i(t)\, dt \tag{4.2}$$

substituting $B(t)$ for $v(t)$ using Faraday's law, and $H(t)$ for $i(t)$ using Ampere's law:

$$W = \int_0^T \left(nA_c \frac{dB(t)}{dt} \right) \left(\frac{l_m H(t)}{n} \right) dt$$

$$= V_c \int_0^T H dB \tag{4.3}$$

where n is the inductor number of turns, A_c is the effective core cross section area, l_m is the core mean magnetic path length, and $V_c = A_c l_m$ is the effective core volume. Hence, the hysteresis power loss, where f_s is the supply frequency, is:

$$P_h = f_s V_c \int_0^T H dB \tag{4.4}$$

ii. Eddy current core loss

Almost all magnetic core materials are electrical conductors, and are placed directly in time varying magnetic fields. According to Faraday's law, this flux induces a voltage which is directly proportional with the excitation frequency. As a result, circulating eddy currents circulate in the core material, with paths, in planes normal to the core magnetic flux. Considering only the resistive component of the core impedance, the eddy current losses are directly proportional to frequency squared. Eddy currents cause heating of the core material. Eddy current losses are reduced by using a core material of higher resistivity and/or manufacturing the core in powder form or thin laminated sheets.

iii. Total core losses

Several empirical equations are used to model core losses in magnetic cores. The classical approach which separates the per unit volume loss components and models each term individually is [4.11], [4.30]:

$$P_v = P_h + P_c + P_e = k_h f B_m^{\beta} + k_c \left(f B_m \right)^2 + k_e \left(f B_m \right)^{1.5} \tag{4.5}$$

where P_v is the total core loss per unit volume, P_h is the hysteresis power loss, P_c is the eddy current loss, P_e is the lamination dielectric material power loss, (k_h, k_c, k_e, β) are the corresponding loss coefficients, f is the operating frequency, and B_m is the maximum operating flux density. However, only the eddy current loss of the three components can be calculated. It is difficult to accurately calculate the other loss components, and are determined experimentally [4.31]. The Steinmetz equation is widely used for evaluating the core losses in iron cored ferrite materials [4.32]:

$$P_v = C_m f^{\alpha} B_m^{\beta} \tag{4.6}$$

Where C_m, α, and β are real empirical parameters ($1 < \alpha < 3$, and $2 < \beta < 3$) obtained from experimental measurement under sinusoidal excitation [4.11]. For non-sinusoidal excitations, a modified Steinmetz equation was developed [4.31]:

$$P_v = C_m f_r f_{eq}^{\alpha - 1} B_m^{\beta} \tag{4.7}$$

Where f_{eq} is the equivalent frequency of the non-sinusoidal waveform, and f_r is the repeated frequency. The empirical parameters are usually provided by the core manufacturer, and in some cases loss density curves are given at different frequencies to calculate these parameters by curve fitting.

b. Core materials

Magnetic materials termed ‘soft’ can be readily magnetised and demagnetised, hence can be used to transfer or store magnetic energy in circuits with time-varying waveforms. ‘Hard’ magnetic materials are used as permanent magnets in applications such as brushless and synchronous electric motors [4.5]. Soft magnetic materials are

either ferromagnetic materials based on iron and nickel, or ferrimagnetic materials, which are based on ceramic oxides of metals (ferrites). Ferromagentic materials include steel, iron powders, alloy powders, and the recently developed nanocrystalline materials. While, ferrimagnetic materials are considered a subgroup of ferromagnetic materials, and are compounds of iron oxide (Fe_2O_3) mixed with one or more oxides of bivalent transition metals such as (FeO, NiO, ZnO, MnO, CuO, BaO, CoO and MgO) [4.33]. Magnetic cores ideally possess a high permeability, high saturation flux density, and high resistivity. Silicon steel, which is widely used in 50 Hz transformers, exhibits the highest saturation flux densities (1.5 - 2 T). It is manufactured in the form of thin laminations or ribbons as standard, to reduce eddy currents. The addition of other materials, such as molybdenum and cobalt, increase the resistivity of the core and reduce the core losses. This also reduces the saturation flux density due to the reduced iron content, which defines the basic trade off between saturation flux density and core losses [4.13]. Typical applications of silicon steel iron cores are 50/60 Hz power transformers, aircraft and marine transport power supplies which operate at 400 Hz, and electric motors, generators, and filter inductors operating below frequencies of a few kHz.

Iron alloys such as nickel-iron have typical saturation flux densities of (0.8 – 1.5 T) depending on the percentage of iron. Such alloys are used for frequencies up to 20 kHz, due to their high permeability. However, nickel iron alloys have poor mechanical properties. Typical applications include current transformers, linear transformers, pulse transformers, saturable reactors, dc-dc converters, and magnetic amplifiers. Cobalt iron alloys have the highest saturation flux densities (2.4 T), and are typically used in space applications, and magnetic amplifiers.

Ferrite cores, which are ceramic materials, are most commonly used for high frequency applications. Ferrites exhibit the lowest saturation flux density of all common magnetic materials (0.25 – 0.5 T), but show comparably low hysteresis and eddy current losses. Manganese-zinc ferrite cores are typically used for frequencies up to 1 MHz, while nickel-zinc ferrite can be used for even higher frequencies. Ferrite cores are used in a wide verity of applications such as high frequency power transformers, pulse transformers, current transformers, common-mode chokes, resonant inductors, high impedance filters, and sensors.

Powdered iron and molybdenum permalloy powder cores posses a saturation flux density of (0.6 – 0.8 T), exhibit significantly lower losses than laminated ferrous alloy cores, and relatively low permeability [4.13]. Powdered iron cores are used for frequency up to 100 MHz. However, amorphous alloys posses a saturation flux densities in the range of (0.8 – 1.5 T), and exhibit lower hysteresis and eddy current losses than ferrous alloys, but higher than ferrites.

Nanocrystalline cores combine the high saturation flux density of silicon steels and the low losses of ferrites giving potential for higher power density magnetic designs[4.34]. A 3.5 factor decrease in volume has been achieved compared to a ferrite based design, for a 300 kW, 200 kHz, high voltage design [4.35], [4.36]. Other designs and associated analysis showing the increased utilisation of nanocrystalline cores in various applications are given in references [4.37], [4.38], [4.39], [4.40], [4.41], and [4.42]. Applications in the frequency range of 150 kHz, such as current transformers and common mode EMI filters, are well suited. Table 4.2 shows the frequency range of different magnetic materials, and shows a comparison between the different materials in terms of permeability, saturation flux density, power loss, Curie temperature, and maximum operating temperature [4.5].

Table 4.2: Ribbon thickness t, relative permeability μ_r, saturation flux density B_s, coercivity H_c, core losses P_{fe}, saturation magnetostriction λ_s, Curie temperature T_c, operating temperature T_{op}, and typical operating frequencies f_{op} for common iron alloys, permalloys, amorphous alloys, nanocrystalline alloys, and ferrite soft magnetic materials

Material	t **(**μm**)**	μ_r		B_s **(**T**)**	H_c	P_{fe} **(**W/kg**)** [(d)]		λ_s **(**10^{-6}**)**	T_c **(**^oC**) / T_{op} (**^oC**)**	f_{op}
		1 kHz	**100** kHz		**(**A/m**)**	**20** kHz	**100** kHz			
3% Silicon Steel	50	2700	800	1.9 [(b)]	2.7	-	1098 [(b)]	-0.8	750/150	50 – 1000 Hz
6.5% Silicon Steel	50	1200	800	1.3 [(a)] - 1.88 [(b)]	1.2	80 [(a)]	770 [(b)]	-0.1	700/150	50 – 3000 Hz
50% - 60% Ni – Fe Permalloy	25 - 50	2000	-	1.2 [(b)] 1.5 [(b)]		45 [(b)]	200 [(a), (c)]	25	500/130	50 – 20000 Hz
80% Ni – Fe Permalloy	30	50000	5000	0.74 [(b)] - 0.8 [(b)]	0.5 – 2.4	14 [(b)]	90 [(a), (c)]	1	460 – 480/130	
Fe-based Amorphous alloy	25	8000	5000	1.5 [(b)] – 1.56 [(b)]	2.4	18 [(b)]	50 [(a)]	25	415/150	0.4 – 250 kHz
Co-based Amorphous alloy	25	150000	18000	0.55 [(b)]	0.3	5 [(b)]	35 [(a)]	<0.2	180/120	
73.5% Fe – 15.5 Si Nanocrystalline	20	110000	30000	1.23 [(b)]	0.4	4 [(b)]	35 [(a)]	~0	570/150	0.4 – 150 kHz
73.5% Fe – 13.5% Si Nanocrystalline	17-18	100000	20000	1.24 [(b)] – 1.7 [(b)]	0.5	3 [(b)]	38 [(a)]	2.1	570/150	
Low loss MnZn Ferrite	-	2400	2400	0.49 [(b)]	12	17 [(b)]	85 [(a)] – 125 [(b)]	-0.6	220/100	10 – 2000 kHz
NiZn Ferrite	-	10-1500	30000	0.24 [(a)] – 0.38 [(b)]	30	20 [(b)]	-	-7.8	200/100	0.2 – 100 MHz

[(a)] At $T_{op} = 100\ ^oC$.
[(b)] At $T_{op} = 25\ ^oC$.
[(c)] Lower bound due to eddy losses.
[(d)] At $B_{op} = 0.2\ T$.

4.3.3 Leakage inductance

Leakage inductance represents the magnetic flux induced through the winding conductors and the associated gaps, which does not link another winding via the core, as shown in Figure 4.4. The total magnetic flux ϕ of the transformer consists of the mutual flux ϕ_M which is the common flux between the two windings, and the leakage flux ϕ_l:

$$\phi = \phi_M + \phi_{l1} + \phi_{l2} \tag{4.8}$$

Where ϕ_{l1} is the primary side leakage flux, and ϕ_{l2} is the secondary side leakage flux. The magnetic flux induced by the primary current i_1 consists of the primary leakage flux ϕ_{l2} and the mutual flux ϕ_{l2}:

$$\phi_{11} = \phi_{l1} + \phi_{21} \tag{4.9}$$

Similarly, for the magnetic flux induced by the secondary current i_2:

$$\phi_{22} = \phi_{l2} + \phi_{12} \tag{4.10}$$

However, the total magnetic flux in the primary winding induced by i_1 and i_2, and similarly for the secondary winding is:

$$\phi_1 = \phi_{11} + \phi_{12} \tag{4.11}$$

$$\phi_2 = \phi_{22} + \phi_{21} \tag{4.12}$$

The flux linkage in the primary and secondary windings are then:

$$\lambda_1 = N_1\phi_1 = N_1\phi_{11} + N_1\phi_{12} \tag{4.13}$$

$$\lambda_2 = N_2\phi_2 = N_2\phi_{22} + N_2\phi_{21} \tag{4.14}$$

Hence, by Faraday's law, the voltages across the primary and secondary windings are:

$$v_1 = \frac{d\lambda_1}{dt} = N_1\frac{d\phi_{11}}{dt} + N_1\frac{\phi_{12}}{dt} = L_{11}\frac{di_1}{dt} + L_{12}\frac{di_2}{dt} \tag{4.15}$$

$$v_2 = \frac{d\lambda_2}{dt} = N_1 \frac{d\phi_{22}}{dt} + N_1 \frac{\phi_{21}}{dt} = L_{22} \frac{di_2}{dt} + L_{21} \frac{di_1}{dt} \tag{4.16}$$

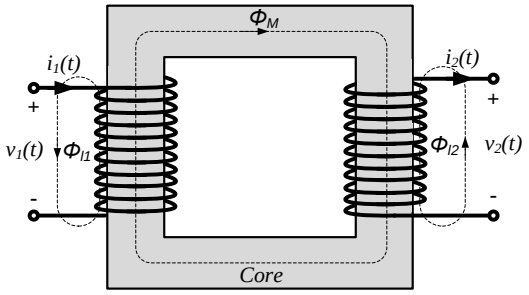


Figure 4.4: Leakage flux in the transformer windings

The presence of the magnetising and leakage inductances cause the terminal voltage ratio ($v_1 : v_2$) differ from the ideal turns ratio ($n_1 : n_2$). The terminal equations of the two winding transformer shown can then be expressed as follows:

$$\begin{bmatrix} v_1(t) \\ v_2(t) \end{bmatrix} = \begin{bmatrix} L_1 & M \\ M & L_2 \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_1(t) \\ i_2(t) \end{bmatrix} \tag{4.17}$$

L_1 and L_2 are the primary and secondary self-inductances:

$$L_1 = L_{11} = L_{l1} + M \tag{4.18}$$

$$L_2 = L_{22} = L_{l2} + M \tag{4.19}$$

where $M = L_{12} = L_{21}$ is the mutual inductance:

$$M = \frac{N_1 N_2}{\mathfrak{R}} = k\sqrt{L_1 L_2} \tag{4.20}$$

where the coupling coefficient k is a measure of the magnetic coupling between the two coils, and lies in the range $0 \le k \le 1$.

a. Leakage inductance calculation

Transformer primary and secondary windings are practically wound as close as possible to minimise leakage fields. The leakage inductance represents the energy stored within the volume of windings, associated insulation, and air gaps. It can be directly calculated by estimating the total magnetic energy stored, using an MMF diagram. A common arrangement is to have the secondary winding surround the primary winding as shown in Figure 4.5.

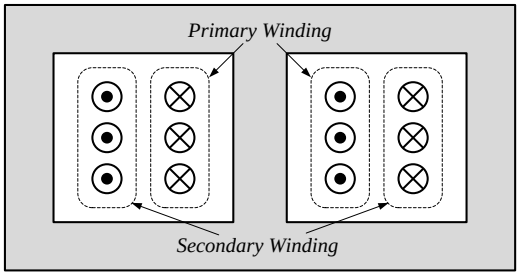


Figure 4.5: Example of a common winding arrangement in a two winding transformer

To calculate the leakage inductance for the shown transformer winding arrangement, the following assumptions are introduced [4.43]:

1. Winding turns are uniformly distributed along each layer, which gives a linear ampere-turns distribution.
2. The core is assumed to possess an infinite permeability. That is, it requires no magnetising MMF; primary and secondary MMFs exactly balance each other.
3. A layer consisting of n_x turns of round wire, of diameter d, carrying a current $i(t)$ can be approximately modelled as a single turn of foil, of thickness t, which carries the current $n_x i(t)$, having the same winding breadth. This does not affect the MMF distribution.

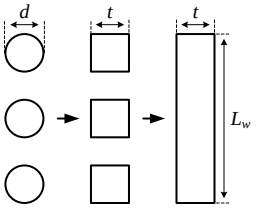


Figure 4.6: Approximating a layer of round conductors as a single foil winding

$$t = \sqrt{\pi}\,\frac{d}{2} \tag{4.21}$$

4. All windings are of equal heights/widths. That is, no radial flux is produced, and all the flux is axial along the windings width.
5. Flux fringing at winding ends is compensated by the Rogowski factor k_r, for which an equivalent winding height is calculated as follows [4.43]:

$$L_w^{'} = \frac{L_w}{k_r} \tag{4.22}$$

$$k_r = 1 - \frac{1 - e^{-\pi L_w / t_{total}}}{\pi L_w / t_{total}} \tag{4.23}$$

where t_{total} is the total winding thickness, including any insulation gaps.

According to these assumptions, the leakage inductance can be estimated by only considering the window cross section. The resultant MMF diagram for the two winding arrangement is shown in Figure 4.7.

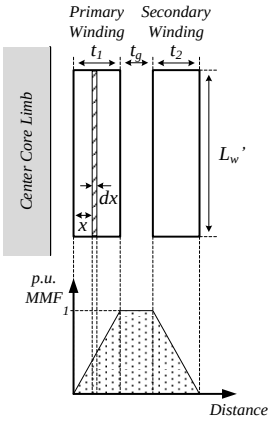


Figure 4.7: MMF Diagram for the equivalent two winding arrangement

The leakage field energy due to the primary winding current:

$$W = \frac{1}{2} L_l i_1^2 \tag{4.24}$$

where L_l is the total leakage inductance referred to the primary side, and i_1 is the primary current. This energy can be calculated by using a differential approach; starting with considering the energy per unit volume. For a magnetic field, in a medium with linear magnetic characteristics ($B = \mu_o H$), when the flux density is increased from 0 to B, the energy stored is:

$$w = \int_0^B H \cdot dB = \int_0^B \frac{B}{\mu_o} \cdot dB = \frac{1}{2\mu_o} B^2 = \frac{1}{2} \mu_o H^2 = \frac{1}{2} BH \tag{4.25}$$

Copper and insulation materials have no magnetic properties, hence the relative permeability is unity. For a cylindrical equivalent winding shape, the differential energy (dW) for a cylindrical ring of height ($L_w^{'}$), thickness (dx), and diameter ($d_1 + 2x$), where d_1 is the internal cylinder diameter, is:

$$dW = \frac{1}{2} \mu_o H_x^2 \times dV \tag{4.26}$$

where dV is the differential volume of the cylindrical ring:

$$dV = \pi \left(d_1 + 2x \right) L_w^{'} dx \tag{4.27}$$

By applying Ampere's law, the MMF at any point is dominated by the total Ampere turns enclosed within the flux path. Hence, the magnetic field enclosed by a flux contour, at the distance *x* with reference to the inside winding diameter is:

$$H_x = \frac{(N_1 i_1)_x}{L_w^{'}} \tag{4.28}$$

Since the MMF distribution is linear, the Ampere-turns at any distance x can be calculated using a simple straight line equation:

$$(N_1 i_1)_x = \frac{N_1 i_1}{t_1} x \tag{4.29}$$

hence:

$$H_x = \frac{N_1 i_1}{t_1 L_w^{'}} x \tag{4.30}$$

By substituting Equation (4.27) and (4.30) into (4.26), the primary winding leakage energy is:

$$W_1 = \int_0^{t_1} \frac{1}{2} \mu_o \times \left(\frac{N_1 i_1}{t_1 L_w^{'}} x \right)^2 \times \pi \left(d_1 + 2x \right) L_w^{'} dx$$

$$= \frac{\mu_o \pi N_1^2 i_1^2}{2 L_w^{'}} \frac{t_1}{3} \left(d_1 + \frac{3}{2} t_1 \right) \tag{4.31}$$

Similarly, for the insulation gap between the primary and secondary windings, where the MMF is constant; the cylindrical ring differential volume at a distance *x* from the gap starting position is:

$$dV = \pi \left(d_g + 2x \right) L_w^{'} dx \tag{4.32}$$

where d_g is the inside diameter of the insulation gap. The magnetic field is constant at any point within the insulation gap:

$$H_x = \frac{N_1 i_1}{L_w^{'}} \tag{4.33}$$

Hence, the energy stored is:

$$W_g = \int_0^{t_g} \frac{1}{2} \mu_o \times \left(\frac{N_1 i_1}{L_w^{'}} \right)^2 \times \pi \left(d_g + 2x \right) L_w^{'} dx$$

$$= \frac{\mu_o \pi N_1^2 i_1^2}{2L_w^{'}} t_g \left(d_g + t_g \right) \tag{4.34}$$

Similarly, for the secondary winding:

$$W_2 = \int_0^{t_2} \frac{1}{2} \mu_o \times \left(\frac{N_1 i_1}{t_2 L_w^{'}} x \right)^2 \times \pi \left(d_2 + 2x \right) L_w^{'} dx$$

$$= \frac{\mu_o \pi N_1^2 i_1^2}{2L_w^{'}} \frac{t_2}{3} \left(d_2 + \frac{3}{2} t_2 \right) \tag{4.35}$$

The total energy stored is then:

$$W = W_1 + W_g + W_2$$

$$= \frac{\mu_o \pi N_1^2 i_1^2}{2L_w^{'}} \left(\frac{t_1}{3} \left(d_1 + \frac{3}{2} t_1 \right) + t_g \left(d_g + t_g \right) + \frac{t_2}{3} \left(d_2 + \frac{3}{2} t_2 \right) \right) \tag{4.36}$$

and the leakage inductance, referred to the primary side, is:

$$L_l = \frac{2W}{i_1^2}$$

$$= \frac{\mu_o \pi N_1^2}{L_w^{'}} \left(\frac{t_1}{3} \left(d_1 + \frac{3}{2} t_1 \right) + t_g \left(d_g + t_g \right) + \frac{t_2}{3} \left(d_2 + \frac{3}{2} t_2 \right) \right) \tag{4.37}$$

Equation (4.37) represents an estimated leakage inductance value for the two concentric winding arrangement, which is directly related to the physical dimensions of the windings. The same procedures can be repeated for different winding arrangements with multiple layers.

b. Effect of leakage inductance on circuit performance

Increased leakage inductance directly affect different power converter circuit performance aspects. As mentioned, the leakage field is represented by an additional inductance in series with each winding, which may be combined into one inductance in series with the primary winding. This inductance reduces the primary current rate of change, and reduces the effective secondary voltage duty cycle. A centre tapped rectifier circuit is shown in Figure 4.8a. The circuit has an input voltage of 120 V, an output voltage of 5 V, and operates at 10 kHz. An equivalent circuit, where the ideal transformer is replaced with an equivalent circuit referred to the secondary side, is

shown in Figure 4.8b. Winding resistances, self-inductances, as well as transistors and diodes voltage drops are neglected to simplify the analysis. The leakage inductance is placed on the secondary side, in series with each winding as shown. The converter is operated with a primary duty cycle of 90%. Consider the ideal case, where zero leakage inductance is assumed, the total secondary duty cycle is the same as the primary side. Any leakage inductance reduces the primary current rate of change as observed in Figure 4.9b. The total effective secondary duty cycle is reduced as shown in Figure 4.9c. The output voltage of the converter drops from 5.4 V to 3.9 V when a leakage inductance of 20 µH is introduced, as shown in Figure 4.9d. The output voltage reduction is directly proportional to the load current. Increased leakage inductance significantly affects load regulation, and must be carefully considered in the design process.

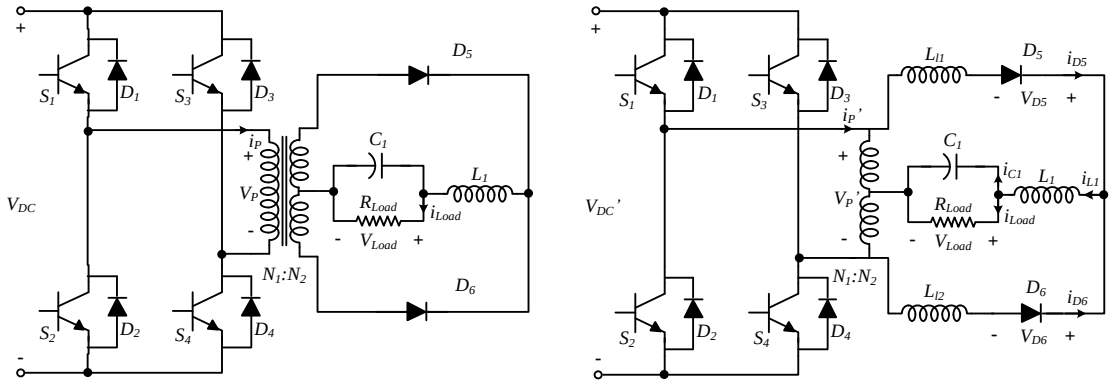


Figure 4.8: (a) Centre tapped rectifier, (b) replacing the ideal transformer by the equivalent circuit model

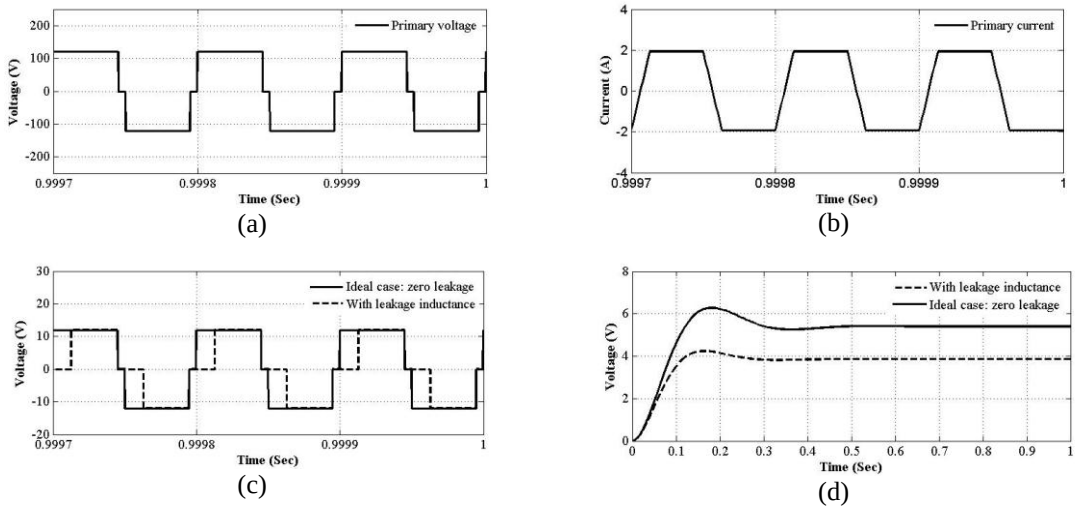


Figure 4.9: (a) Primary voltage with an operating duty cycle of 90%, (b) primary current, (c) secondary voltage in the ideal case with zero leakage and case where the leakage inductance is present, and (d) the average output voltage in both cases

c. Leakage Inductance Minimisation

It has been shown in the previous section, that the leakage inductance directly affects power converter performance. Increased values can lead to poor load regulation, limit the maximum frequency of operation, generate voltage spikes across the main switches, and increase the switching losses of the converter [4.44], [4.45]. Leakage inductance minimisation is mandatory in the majority of power electronic applications. Referring to Equation (4.37), minimum leakage inductance can be achieved by increasing the winding breadth $L_w^{'}$, and/or reducing the insulation thickness between the windings. However, such modifications are subject to restriction on the core geometry, insulation materials used, as well as the manufacturing process. Reduction of the winding thickness is also possible, but is subject to copper loss restrictions. Reducing the number of turns can also lead to increased core loss, and core saturation if not carefully considered. Interleaving is a common technique to reduce the leakage inductance, and minimise the high frequency winding losses. Primary and secondary windings are equally divided in to multiple sections connected in series, with each primary and secondary section placed simultaneously over each other as shown in Figure 4.10. The resultant peak per unit MMF for each corresponding section is reduced by a factor *k*, which is the total number of winding sections. The total leakage inductance for the *k*-section interleaved configuration can be similarly calculated as described previously, specifically:

$$L_{lk} = \sum_{j=1}^{k} \frac{\mu_o \pi N_1^2}{j^2 L_w^{'}} \left(\frac{t_1}{3} D_1 + t_g D_g + \frac{t_2}{3} D_2 \right) \tag{4.38}$$

where D_1, D_g, and D_2 are the mean diameters of the primary winding, gap, and secondary winding respectively.

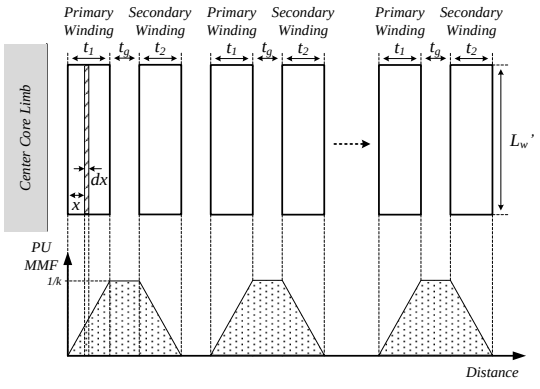


Figure 4.10: Interleaved winding configuration for the two winding transformer

The amount of leakage inductance reduction can be plotted against the number of interleaved sections as shown in Figure 4.11, by dividing equations (4.37) and (4.38):

$$Amount\,of\ Reduction = \frac{L_{lk}}{L_l} = \sum_{j=1}^{k} \frac{1}{j^2} \tag{4.39}$$

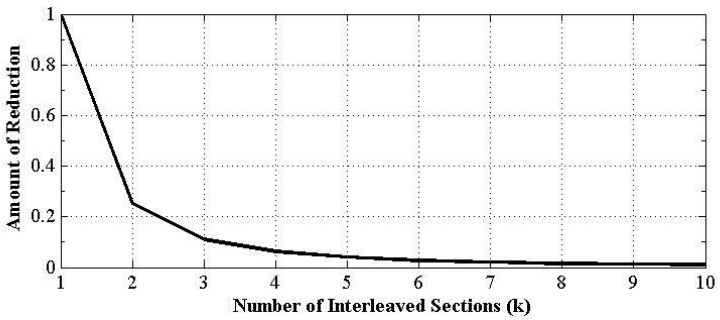


Figure 4.11: Reduction in transformer leakage inductance versus the number of interleaved sections

The total leakage inductance is reduced to 0.25 of its original value by dividing the windings into two interleaved sections. However, the number of obtainable interleaved sections strictly depends on the available core window area.

4.3.4 Winding resistance

Windings are commonly copper conductors, for which the resistance can be calculated by using the specific resistivity of copper at a certain temperature. However, at high frequency operation, skin and proximity effects increase the winding resistance.

a. DC winding resistance

The DC winding resistances can be calculated as follows:

$$R_{p,DC} = \frac{\rho (MLT)_p N_1}{A_{c1}} \tag{4.40}$$

$$R_{s,DC} = \frac{\rho (MLT)_s N_2}{A_{c2}} \tag{4.41}$$

where ρ is the specific resistivity of copper, $(MLT)_p$ and $(MLT)_s$ are the mean length per turn for the primary and secondary windings respectively, A_{c1} and A_{c2} are the primary and secondary conductor cross sectional areas respectively, N_1 and N_2 are the primary and secondary number of turns respectively.

b. AC winding resistance

The effective winding resistance for high frequency current carrying conductors can be significantly more than the equivalent DC resistance. Eddy currents are generated within the conductors, and suffer the phenomena of 'skin effect'. For windings with multiple consecutive layers, proximity effect losses must be also considered.

c. Skin effect

The skin effect is defined as the tendency of an alternating current to flow on the surface of conductors. Specifically, the current passing through the conductor induces a magnetic flux, which induces circulating currents that oppose the main conductor current. These currents reduce the current density in the centre of the conductor, and increase the current density near the surface of the conductor. The conductor current distribution can be found by solving Maxwell's equations for a sinusoidal current of frequency *f*. For an infinite thick plate, the current density *J* decreases exponentially with the depth *d* from the surface according to the following relation:

$$J = J_s e^{-d/\delta} \tag{4.42}$$

where δ is known as the skin or penetration depth; the depth at which the current density decays to $1/e$ of the current density at the surface J_s. The skin depth for a copper conductor at $100^o C$ is given by[4.13]:

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} = \frac{75}{\sqrt{f}} mm \tag{4.43}$$

Winding conductors are chosen to have a diameter or thickness less than or equal to the skin depth at the given operating frequency, to reduce the skin effect losses and improve copper usage. This can be achieved by using Litz wire for round conductors, and multiple laminated foil conductors for high current windings. Litz wire is a stranded conductor, with all strands individually insulated, and twisted together or laid side-by side, in which each individual strand diameter is less than the skin depth.

d. Proximity effect

Consider the m-layer primary transformer winding shown in Figure 4.12, in which all layers are in close proximity to one another, and are connected in series. Currents tend to flow on the surface where the field intensity is greatest. The current flowing through the first layer induces a flux in the space between the first and second layer, which induces a current on the adjacent side of the second layer that tends to oppose this flux. If the conductors are closely spaced, and $\delta \gg t_1$, the induced current will be equal and opposite to the current *i*(*t*). This circulating current adds-up to the current flowing on the other side of the second layer. For an RMS current *I* flowing through all the layers, the power loss in each layer is [4.13]:

$$P_1 = I^2 R_{AC} \tag{4.44}$$

$$P_2 = P_1 + (2i)^2 R_{AC} = 5i^2 R_{AC} \tag{4.45}$$

$$P_3 = (2i)^2 R_{AC} + (3i)^2 R_{AC} = 13i^2 R_{AC} \tag{4.46}$$

$$P_n = ((n-1)i)^2 R_{AC} + (ni)^2 R_{AC} = (2n^2 - 2n + 1) i^2 R_{AC} \tag{4.47}$$

The total power loss for the m-layer winding is[4.13]:

$$P = i^2 R_{AC} \sum_{n=1}^{m} (2n^2 - 2n + 1)$$

$$= i^2 R_{AC} \frac{m}{3} (2m^2 + 1) \tag{4.48}$$

The skin effect causes the copper loss in layer 1 to be equal to the loss in a conductor of thickness delta with uniform current density. Therefore the AC resistance may be approximated as [4.13]:

$$R_{AC} = \frac{t_1}{\delta} R_{DC} \tag{4.49}$$

Compared to the DC or low frequency power loss $P_{DC} = mI^2 R_{DC}$, the proximity effect increases the copper loss by a factor [4.13]:

$$\frac{P}{P_{DC}} = \frac{1}{3} \left(\frac{t_1}{\delta} \right) (2m^2 + 1) \tag{4.50}$$

The winding power loss can be increased with the increased number of layers. However, this example does not quantify the proximity behaviour for $t_1 \sim \delta$, as winding conductors are never practically chosen with $\delta \gg t_1$. An exact calculation method for the resistance reduction factors considering both skin and a proximity effect is given in the next section for foil and Litz wire conductors.

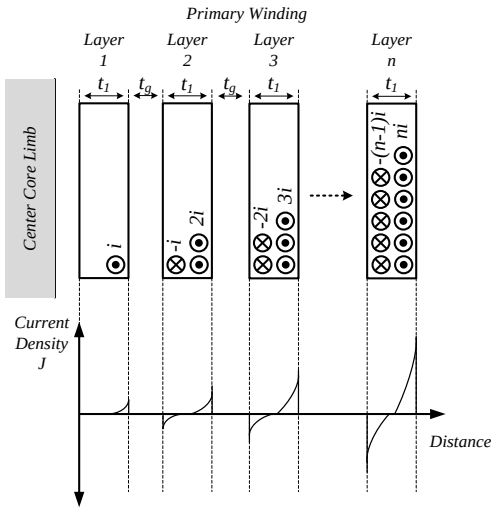


Figure 4.12: Illustration of skin and proximity effects in a multiple layer winding

c. Foil winding resistance considering skin and proximity effects

Magnetic field and MMF distribution across the windings are no longer assumed to be linearly distributed across the winding thickness, and follow a current distribution due to skin and proximity effects as shown in Figure 4.13. The foil winding consists of m layers, each of thickness t and breadth $L_w^{'}$. The current density distribution, and hence the power loss can be obtained from the MMF distribution across the windings, as will be shown briefly.

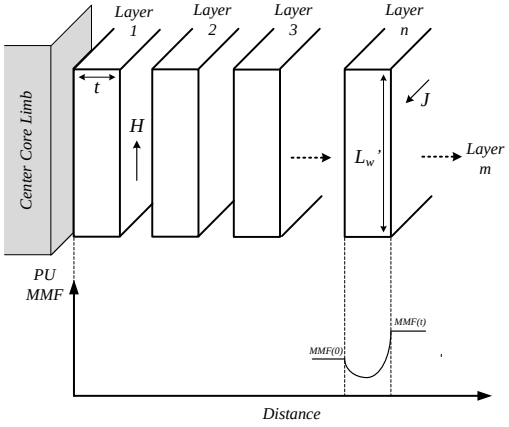


Figure 4.13: Parallel foil conductor winding

The n^{th} layer magnetic field intensity can be obtained by considering Maxwell's equations describing the inductor [4.5]:

$$\nabla \times E = \mu_o \frac{\partial H}{\partial t} \tag{4.51}$$

$$\nabla \times H = \sigma E \tag{4.52}$$

A solution can be obtained under the following assumptions [4.5]:

a. Windings consist of straight and parallel foil conductors, neglecting curvature, edge, and end effects
b. The net charge density of the conductor is zero
c. The core is ideal
d. A sinusoidal current is flowing through the winding conductors ($i = I_m cos\omega t$), which produces an alternating magnetic flux density ($B = B_m cos(\omega t + \varphi_B)$) parallel to the foil windings

The electric and magnetic fields contain only *y* and *z* components, respectively:

$$H = H(x) = H_z = H_z(x) \tag{4.53}$$

$$E = E(x) = E_y = E_y(x) \tag{4.54}$$

Therefore Maxwell's equations in phasor form become:

$$\frac{\partial E_y}{\partial x} = -j\omega\mu_o H_z \tag{4.55}$$

$$-\frac{\partial H_z}{\partial x} = \sigma E_y \tag{4.56}$$

Substituting (4.56) into (4.55) yields the second order differential equation known as the Helmholtz equation [4.5]:

$$\frac{\partial H^2}{\partial x^2} = j\omega\mu_o\sigma H \tag{4.57}$$

The solution of this equation is:

$$H(x) = H_1 e^{\gamma x} + H_2 e^{-\gamma x} \tag{4.58}$$

where H_1 and H_2 are complex constants, and γ is the complex propagation constant:

$$\gamma = \sqrt{j\omega\mu_o\sigma} = \sqrt{\frac{j\omega\mu_o}{\rho}} = \frac{1+j}{\delta} \tag{4.59}$$

and δ is the skin depth given by:

$$\delta = \frac{1}{\sqrt{\pi f \mu_o \sigma}} = \sqrt{\frac{\rho}{\pi f \mu_o}} \tag{4.60}$$

The current density in the n[th] layer can be obtained by substituting into:

$$J(x) = \frac{E(x)}{\rho} \tag{4.61}$$

where:

$$E(x) = -\rho \frac{dH}{dx} \tag{4.62}$$

and the power loss is defined as:

$$P(x) = \rho |J(x)|^2 \tag{4.63}$$

Solving to find the n[th] layer power loss density, yields [4.46]:

$$P = R_{DC} \frac{t}{\delta N_l} \left\{ \left[MMF^2(0) + MMF^2(t) \right] G_1 - 4MMF(0) MMF(t) G_2 \right\} \tag{4.64}$$

$$G_1 = \frac{\sinh\left(\frac{2t}{\delta}\right) + \sin\left(\frac{2t}{\delta}\right)}{\cosh\left(\frac{2t}{\delta}\right) - \cos\left(\frac{2t}{\delta}\right)} \tag{4.65}$$

$$G_2 = \frac{\sinh\left(\frac{t}{\delta}\right)\cos\left(\frac{t}{\delta}\right) + \cosh\left(\frac{t}{\delta}\right)\sin\left(\frac{t}{\delta}\right)}{\cosh\left(\frac{2t}{\delta}\right) - \cos\left(\frac{2t}{\delta}\right)} \tag{4.66}$$

N_l is the number of turns per layer, and R_{DC} is the layer DC resistance. Substituting equation (4.64) for each layer boundary conditions and summing the results in order to obtain the total m layers winding loss, as given in Appendix C. The winding resistance ratio factor due to proximity and skin effects is expressed as [4.13]:

$$F_R = \frac{P}{P_{DC}}$$

$$= \frac{R_{AC}}{R_{DC}} = \frac{t}{\delta} \left(\frac{\sinh\left(\frac{2t}{\delta}\right) + \sin\left(\frac{2t}{\delta}\right)}{\cosh\left(\frac{2t}{\delta}\right) - \cos\left(\frac{2t}{\delta}\right)} + \frac{2}{3}\left(m^2 - 1\right) \frac{\sinh\left(\frac{t}{\delta}\right) - \sin\left(\frac{t}{\delta}\right)}{\cosh\left(\frac{t}{\delta}\right) + \cos\left(\frac{t}{\delta}\right)} \right) \tag{4.67}$$

This expression is plotted against t/δ, for different number of layers, in Figure 4.14, which shows the increased resistance factor due to the increased proximity effect losses as the number of layers increases.

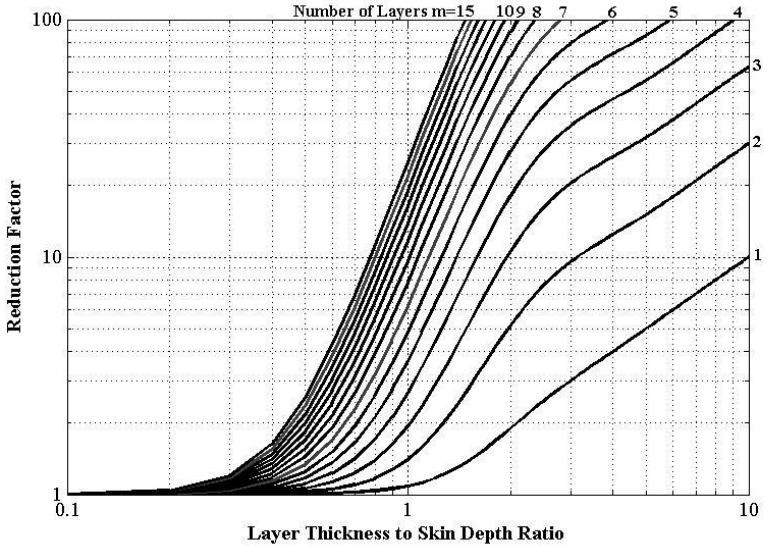


Figure 4.14: Plots of the resistance reduction factor (F_R) versus the layer thickness to skin depth ratio (t/δ), for multiple number of layer (m = 1 − 15)

The first term in Equation (4.67) represents the winding resistance ratio due to the skin effect, while the second term represents the winding resistance ratio due to the proximity effect. Therefore:

$$F_R = F_S + F_P \tag{4.68}$$

where the skin effect factor, which depends on t/δ, is:

$$F_S = \frac{t}{\delta}\frac{\sinh\left(\frac{2t}{\delta}\right)+\sin\left(\frac{2t}{\delta}\right)}{\cosh\left(\frac{2t}{\delta}\right)-\cos\left(\frac{2t}{\delta}\right)} \tag{4.69}$$

and the proximity effect factor, which depends on both the number of layers m and t/δ, is:

$$F_P = \frac{2t}{3\delta}\left(m^2-1\right)\frac{\sinh\left(\frac{t}{\delta}\right)-\sin\left(\frac{t}{\delta}\right)}{\cosh\left(\frac{t}{\delta}\right)+\cos\left(\frac{t}{\delta}\right)} \tag{4.70}$$

Orthogonality exists between both skin and proximity effects, in which each can be separately obtained and then added, under the assumption that the magnetic field applied due to other conductors (proximity effect) is uniform across the conductor cross section [4.28]. Equation (4.67) can also be modified and extended to other winding conductor shapes, such as square, and round conductors by using a square to round conversion to obtain approximate analytical expressions for the winding resistance [4.5]. However, this introduces some approximation errors, especially at high frequencies [4.28].

d. Litz wire resistance considering skin and proximity effects

The equivalent resistance of a Litz wire winding can be obtained by first considering the skin effect in a round conductor. The current density through an infinitely long solid round conductor shown in Figure 4.15 is described by a modified Bessel ordinary differential equation with a complex argument in cylindrical coordinates [4.5]:

$$\frac{d^2J}{dr^2}+\frac{1}{r}\frac{dJ}{dr}-k^2J=0 \tag{4.71}$$

and:

$$k=\frac{1+j}{\delta} \tag{4.72}$$

where k is defined as a complex propagation constant. Solving Equation (4.71) and substituting to obtain the skin effect factor [4.25]:

$$F_S=\frac{\alpha_o}{2}\frac{ber(\alpha_o)bei'(\alpha_o)-bei(\alpha_o)ber'(\alpha_o)}{\left[ber'(\alpha_o)\right]^2+\left[bei'(\alpha_o)\right]^2} \tag{4.73}$$

where:

$$\alpha_o=\frac{\sqrt{2}r_o}{\delta} \tag{4.74}$$

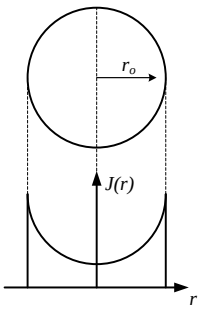


Figure 4.15: Current distribution across an infinitely long round wire

The kelvin functions ($ber(\alpha_o)$, $bei(\alpha_o)$) are represented by an equivalent series expansion of:

$$ber(\alpha_o) = \sum_{n=0}^{\infty}\left(\frac{(-1)\alpha_o^{4n}}{2^{4n}\left[(2n)!\right]^2}\right)$$

$$bei(\alpha_o) = \sum_{n=0}^{\infty}\left(\frac{(-1)\alpha_o^{2(2n+1)}}{2^{2(2n+1)}\left[(2n+1)!\right]^2}\right)$$

Using the orthogonality approach as described in [4.28], the resistance ratio for *m* layers considering both skin and proximity effects, is:

$$F_R = \frac{\alpha_o}{2}\left[\begin{array}{l}\dfrac{ber(\alpha_o)bei'(\alpha_o) - bei(\alpha_o)ber'(\alpha_o)}{\left[ber'(\alpha_o)\right]^2 + \left[bei'(\alpha_o)\right]^2} \\ -2\pi(2m-1)^2\dfrac{ber_2(\alpha_o)ber'(\alpha_o) + bei_2(\alpha_o)bei'(\alpha_o)}{\left[ber(\alpha_o)\right]^2 + \left[bei(\alpha_o)\right]^2}\end{array}\right] \qquad (4.75)$$

In Litz wire windings, the proximity effect may be further divided into strand level and bundle level effects. Bundle level effects depend on the pattern of twisting and are not directly affected by the number and/or the diameter of individual strands, and thus are not considered in the power loss analysis [4.47]. Skin effect may be neglected within individual strands, as strands diameters are usually chosen to be less than the actual skin depth. The strand level proximity effect due to external magnetic fields caused by currents in all other strands, neglecting the skin effect within individual strands, results in the approximated resistance ratio [4.5]:

$$F_R = \frac{R_{AC}}{R_{DC}} = 1 + \frac{\pi^2 f^2 \mu_o^2 n^2 N^2 d_l^2}{192\rho^2 b_c^2} \qquad (4.76)$$

N is the total number of turns, *n* is the number of strands, d_l is the diameter of each strand without insulation, ρ is the resistivity of copper, and b_c is the core window area breadth. This equation is equal to the first term of the Bessel function solution expansion, combined with the assumption of a trapezoidal field distribution [4.47].

e. Winding power loss for non-sinusoidal currents

High frequency transformers used in PWM DC/DC converters are subject to non-sinusoidal winding currents. Such currents may be of a continuous or pulsating nature, depending on the specific application. However, by using a Fourier analysis/expansion,

the fundamental component, associated harmonics, and DC component (if present) can be obtained as follows:

$$i = I + \sum_{n=1}^{\infty} I_{mn} \cos\left(n\omega t + \varphi_n\right) = I + \sqrt{2}\sum_{n=1}^{\infty} I_n \cos\left(n\omega t + \varphi_n\right) \tag{4.77}$$

where I is the winding DC component, I_{mn} is the maximum amplitude of the n[th] harmonic, and $I_n = \sqrt{2} I_{mn}$ is its equivalent RMS value. The winding power loss due to the DC currents, and associated harmonics is then [4.5]:

$$P = I^2 R_{DC} + \sum_{n=1}^{\infty} I_n^2 R_n \tag{4.78}$$

$$= I^2 R_{DC} + I_1^2 R_1 + I_2^2 R_2 + I_3^2 R_3 + \ldots$$

$$= I^2 R_{DC}\left[1 + \frac{R_1}{R_{DC}}\left(\frac{I_1}{I}\right)^2 + \frac{R_2}{R_{DC}}\left(\frac{I_2}{I}\right)^2 + \frac{R_3}{R_{DC}}\left(\frac{I_3}{I}\right)^2 + \ldots\right]$$

$$= I^2 R_{DC}\left[1 + \sum_{n=1}^{\infty} F_{Rn}\left(\frac{I_n}{I}\right)^2\right] \tag{4.79}$$

where F_{Rn} is the equivalent nth harmonic resistance to DC resistance ratio. The equivalent skin depth for the nth harmonic is:

$$\delta_n = \sqrt{\frac{\rho}{\pi \mu_o n f}} = \frac{\delta_1}{\sqrt{n}} \tag{4.80}$$

where δ_1 is the skin depth at the fundamental frequency f. The equivalent nth harmonic resistance ratio for foil conductors can then be obtained for each individual harmonic component by substituting into (4.76):

$$F_{Rn} = \frac{R_n}{R_{DC}} = \frac{\sqrt{n}t}{\delta}\left(\begin{array}{l} \dfrac{\sinh\left(\dfrac{2t\sqrt{n}}{\delta}\right) + \sin\left(\dfrac{2t\sqrt{n}}{\delta}\right)}{\cosh\left(\dfrac{2t\sqrt{n}}{\delta}\right) - \cos\left(\dfrac{2t\sqrt{n}}{\delta}\right)} \\ \\ + \dfrac{2}{3}\left(m^2 - 1\right)\dfrac{\sinh\left(\dfrac{t\sqrt{n}}{\delta}\right) + \sin\left(\dfrac{t\sqrt{n}}{\delta}\right)}{\cosh\left(\dfrac{t\sqrt{n}}{\delta}\right) - \cos\left(\dfrac{t\sqrt{n}}{\delta}\right)} \end{array}\right) \tag{4.81}$$

In the case of Litz wire windings, and specifically for square wave current waveforms, an approximate value for the total RMS AC to DC resistance ratio is presented in [4.47]:

$$F_{R,RMS} = 1 + \left(F_R\left(f_1\right) - 1\right)\frac{f_{eff}^2}{f_1^2} \tag{4.82}$$

Where f_{eff} is the effective frequency for the nonsinusoidal waveform, and f_1 is the fundamental frequency. A square wave with finite sloping edges leads to a finite value of f_{eff}, which is:

$$f_{eff} = 2 f_1 \sqrt{\frac{6}{\Delta(3 - 4\Delta)}} \tag{4.83}$$

where Δ is the transition time as a fraction of the total period. This expression is valid provided there is no significant harmonic current for which the wire diameter is large compared to the skin depth. Based on the rule of thumb that the highest important harmonic number is given by $n = 0.35/\Delta$, a rough check on this would be to calculate the skin depth for a maximum frequency of $f_{max} = 0.35 f_1/\Delta$, and then to compare it to the wire diameter. If there are significant harmonics for which the skin depth is small compared to the wire diameter, an exact solution is preferred [4.47].

4.4 Design criteria

The transformer design process involves not only obtaining the leakage inductance or turns ratio, but is subject to many other constraints. The core must be chosen according to window area requirements. Core magnetic properties and power loss must also be considered. The maximum flux density must not saturate the core, and the core magnetic characteristics must meet the required specifications. Window area requirements are subject to the required conductor cross section area, considering the insulation fill factor. Winding restrictions may result in a larger window area requirement, due to the use of interleaving, for reducing the leakage inductance and/or the proximity effect losses. Other design restrictions such as the requirement of a minimum total power loss, minimum volume, specific leakage inductance, and implementation difficulties also govern the design process. Basic design methods presented in many texts include the area product, k_g, and k_{gfe} methods. For the area product method, the core geometry for a two winding transformer is selected based on the required core area product, presented by:

$$A_p = A_c W_a \tag{4.84}$$

Where A_c is the core cross sectional area, and W_a is the core window area. The required core window area is:

$$W_a = \frac{1}{k_u}\left(N_1 A_1 + N_2 A_2\right) \tag{4.85}$$

Where k_u is the window utilisation factor, N_1 and N_2 are the primary and secondary number of turns, A_1 and A_2 are the primary and secondary cross section areas:

$$A_1 = \frac{I_1}{J}, A_2 = \frac{I_2}{J} \tag{4.86}$$

Where I_1 and I_2 are the primary and secondary RMS currents, and J is the required primary and secondary conductor current density. This design methodology can be applied to most high frequency transformer designs, such as the design presented in [4.15]. A better approach is to use the k_g method. The geometrical constant k_g which is a measure of the effective magnetic size of the core, for which a desired magnetising inductance, maximum operating flux density, and total DC copper loss are achieved, is [4.13]:

$$k_g = \frac{A_c^2 W_A}{MLT} \tag{4.87}$$

where MLT is the average mean length per turn for all windings. A core must be chosen to satisfy the following condition [4.13]:

$$k_g \geq \frac{\rho L_M^2 I_{tot}^2 I_{M,max}^2}{B_{max}^2 k_u P_{cu}} \tag{4.88}$$

where L_M is the required magnetising inductance referred to the primary side, I_{tot} is the total winding currents referred to the primary side, I_M is the peak magnetising current referred to the primary side, B_{max} is the maximum operating flux density, k_u is the winding fill factor, and P_{cu} is the desired allowable total copper loss.

The k_{gfe} method is a modification to the k_g method, in which both the copper and core loss are used as constraints. The optimum operating flux density is obtained where both the core and DC copper losses are minimised. A core is selected according to the following condition [4.13]:

$$k_{gfe} \geq \frac{\rho \lambda_1^2 I_{tot}^2 k_{fe}^{2/\beta}}{4 k_u P_{tot}^{(\beta+2/\beta)}} \tag{4.89}$$

Where k_{fe} and β are material constants which are obtained from the manufacturers datasheets, and λ_1 is the applied primary volt seconds. However, the minimum loss approach can be applied without the need to evaluate the geometrical constants k_g and k_{gfe}. The process basically depends on selecting a core geometry which accommodates the transformer windings, and operates at the optimum flux density which minimises the core and winding losses. Different approaches applying this method are given in [4.16], [4.17], [4.18], and [4.22]. An added minimum volume constraint is also used in [4.19]. The design process is not restricted to certain procedures, but however is directed with the some design constraints, which are common to all designs.

4.5 Nanocrystalline transformer design

The requirement is to design a high frequency centre-tapped transformer with the specifications in Table 4.1. The transformer is utilised in the high-current low-voltage DC-DC converter under study, which supplies a continuous 1000 A DC current at 8 V. A higher transformer output voltage (> 8 V) must be specified in order to account for the rectifier diode and leakage inductance voltage drops. The operating frequency is not restricted to a specific value, but however is specified to be in the range between 10 to 20 kHz. This gives flexibility in order to fulfil the minimum volume restriction.

4.5.1 Primary and secondary winding conductors

Based on the lowest loss density and highest flux swing among the different core materials, the design is to be based on a nanocrystalline core material. The core material Nanoperm®, with a saturation flux density of 1.2 T, is selected based on availability considerations. A single turn foil winding is the optimum choice for the 1000 A high current secondary windings. Specifying a secondary voltage of 11 V, to compensate for the rectifier diode and leakage inductance voltage drop, gives a primary number of turns (approximated to the nearest integer) of:

$$N_1 = \frac{V_1}{V_2} N_2 = \frac{600}{11} \times 1 \cong 54 \tag{4.90}$$

The primary RMS current is then:

$$I_1 = \frac{N_2}{N_1} I_2 = \frac{1}{54} \times 1000 = 18.5\,A \tag{4.91}$$

The secondary winding consists of two single-turn secondary windings to be connected as a centre tapped configuration. The selection of winding conductors is based on a current density J of 3 A/mm^2 (as specified from the AWG standard for continuous current in copper conductors). The primary and secondary conductor cross sectional areas are:

$$A_1 = \frac{I_1}{J} = \frac{18.52}{3} = 6.17\,mm^2 \tag{4.92}$$

$$A_2 = \frac{I_2}{J} = \frac{1000}{3} = 333.3mm^2 \tag{4.93}$$

For centre tapped rectifier operation, each secondary winding carries half the total secondary RMS current. Hence, each secondary winding is constructed with half the required conductor cross section area. However, increasing the conductor cross section area reduces the winding DC power loss, and is permissible if excess window area is available. The skin depth at 20 kHz is:

$$\delta = \frac{75}{\sqrt{f}} = \frac{75}{\sqrt{20000}} = 0.53mm \tag{4.94}$$

Litz wire with individual strand diameters less than the skin depth are used for the primary winding conductor, and foil windings with a thickness less than the calculated skin depth are used for the single turn secondary windings. The dimensions of the secondary winding conductors are to be chosen after selecting the appropriate core geometry. However, using a window utilisation factor k_u of 0.4 [4.16], the required window area is:

$$W_A = \frac{N_1 A_p + 2N_2 A_s}{k_u} = \frac{54 \times 6.17}{0.3} + \frac{2 \times 1 \times 166.665}{0.4} = 1943.9\,mm^2 \tag{4.95}$$

4.5.2 Core and winding geometry

To choose an appropriate core geometry, a minimum window area and a cross sectional area must both be specified. Using the empirical transformer EMF equation obtained from Faraday's law ($E_1 = k_f B_{op} A_c f N_1$); where k_f is the form factor (k_f = 4.44 for sine wave and k_f = 4 for square wave operation), A_c is the core cross sectional area, f is the operating frequency, E_1 is the primary voltage, and N_1 is the primary number of turns; the operating flux density B_{op} is:

$$B_{op} = \frac{E_1}{k_f A_c f N_1} = \frac{600}{4 \times A_c \times f \times 54} \tag{4.96}$$

To choose a core that satisfies minimum volume requirements governed by the smallest window area, as well as the core cross sectional area governed by the maximum operating flux density ($B_{op} \leq \pm 0.8 B_{sat}$), the main restrictions are:

$$W_A \geq 1943.9 mm^2 \tag{4.97}$$

$$B_{op} \leq \pm 0.96 T \tag{4.98}$$

$$10 kHz \leq f \leq 20 kHz \tag{4.99}$$

The maximum operating flux density of $0.8 B_{sat}$ is selected to account for material differences, different quadrant *BH* characteristics and possible temperature variations of B_{sat}. Equation (4.96) is plotted for the available core dimensions provided by the manufacturer. M142 satisfies all inequalities, hence is selected for this design. A minimum operating frequency of 14 kHz is specified to avoid core saturation.

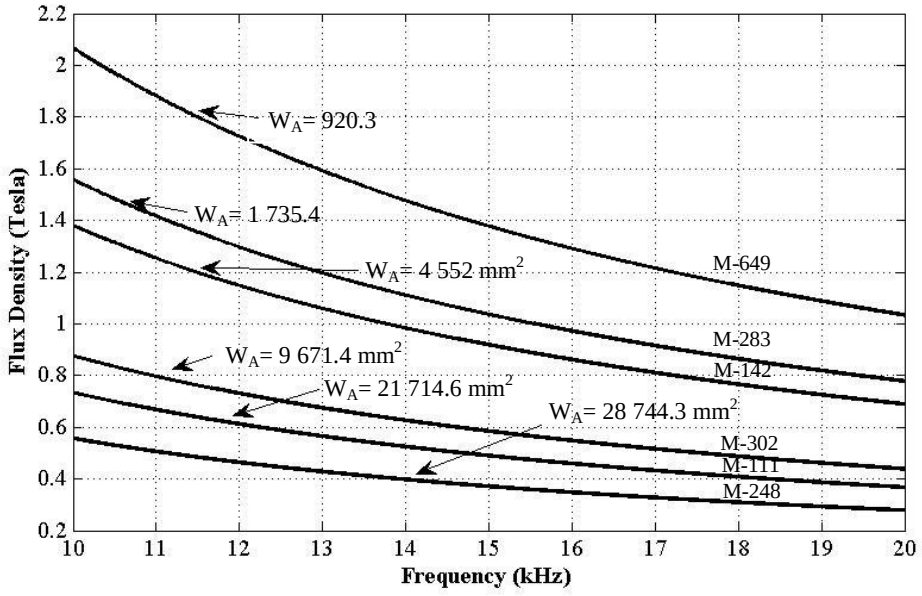


Figure 4.16: Operating flux density versus the operating frequency for the available core dimensions, showing the window area for each core

Based on the calculated skin depth, using Equation (4.94), the primary and secondary winding conductor specifications, and the effective utilisation factor, are listed in Table 4.3. Windings are arranged on the core as shown in Figure 4.17. The primary winding is divided between the two oval core limbs, with 27 turns on each side, connected in series. For the secondary winding, 5 parallel connected foil windings are placed over the

primary winding on each side, and are to be connected in series with a centre-tap termination.

Table 4.3: Primary and secondary conductors specifications, and the effective window utilisation factor

Primary Conductor	Litz wire ($diameter = 0.4mm$) 46 strands	$A_p = 5.78mm^2$
Secondary Conductor	Copper sheet ($Thickness = 0.45mm$) 5 parallel connected sheets per winding	$A_s = 225mm^2$
Effective Utilisation Factor	$k_u = \frac{54 \times 5.8 + 2 \times 225}{4552} = 0.17$	

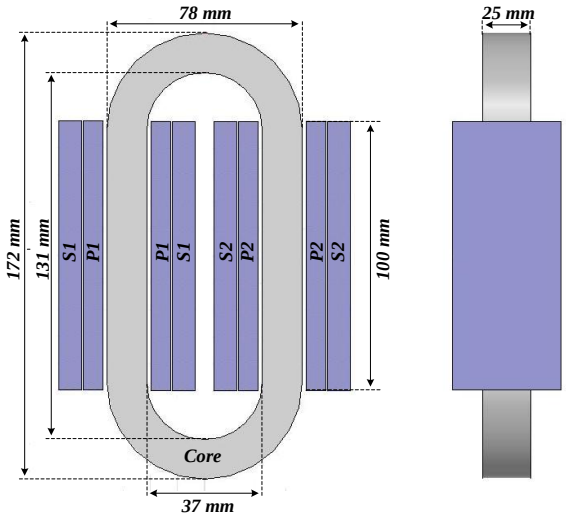


Figure 4.17: Front and side view of primary and secondary winding arrangement, and core dimensions

4.5.3 Leakage inductance calculation

The leakage inductance is calculated based on the energy stored within the windings, insulation and air gaps volume. For centre tapped operation, the total leakage inductance referred to the primary side is the sum of the primary to half secondary and the primary to full secondary leakage components. The primary to full secondary leakage represents the cross coupling between the two single turn secondary windings connected with a centre tap, in which current commutation occurs during each half cycle of operation. The MMF distribution for calculating the primary to half secondary leakage is shown in Figure 4.18.

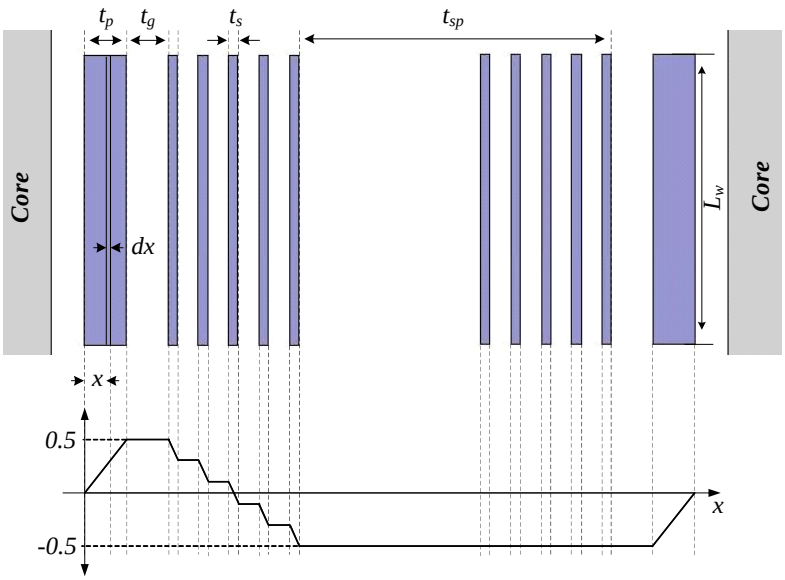


Figure 4.18: MMF distribution across the transformer windings for calculating the primary to secondary leakage inductance

For a rectangular winding with insulation, the energy stored in each winding and insulation section, based on the same method presented earlier, is:

$$W_{p1} = \frac{\mu_o N_1^2 I_1^2 t_p}{8L_w^{'}}\left(\frac{c_p}{3} + 2t_p\right) \tag{4.100}$$

$$W_{g1} = \frac{\mu_o N_1^2 I_1^2 t_g}{8L_w^{'}}\left(c_{g1} + 4t_g\right) \tag{4.101}$$

$$W_s = \frac{\mu_o N_1^2 I_1^2 t_s}{2k^2 L_w^{'}}\sum_{n=1}^{k}\left[c_{sn}\left(\begin{array}{c}\left((n-1)-\frac{k}{2}\right)^2 \\ +\left((n-1)-\frac{k}{2}\right)+\frac{1}{2}\end{array}\right)+t_s\left(\begin{array}{c}4\left((n-1)-\frac{k}{2}\right)^2 \\ +\frac{16}{3}\left((n-1)-\frac{k}{2}\right)+2\end{array}\right)\right] \tag{4.102}$$

$$W_{gs} = \frac{\mu_o N_1^2 I_1^2 t_{gs}}{8L_w^{'}}\sum_{n=1}^{k-1}\left(\frac{n}{k}-\frac{1}{2}\right)^2\left(c_{gn} + 4t_g\right) \tag{4.103}$$

$$W_{g2} = \frac{\mu_o N_1^2 I_1^2 t_{sp}}{8L_w^{'}}\left(c_{g2} + 4t_{sp}\right) \tag{4.104}$$

$$W_{p2} = \frac{\mu_o N_1^2 I_1^2 t_p}{8L_w^{'}}\left(\frac{c_p}{3} + \frac{2t_p}{3}\right) \tag{4.105}$$

where W_{p1} is the energy stored in the first part of the primary winding, W_{g1} is the energy stored in the insulation gap between the primary and secondary windings, W_s is the energy stored in the secondary foil winding, W_{gs} is the energy stored in the insulation

between the individual foil copper conductors, W_{g2} is the energy stored in the gap between the second primary and secondary windings, and W_{p2} is the energy stored in the second primary winding section. A cross sectional view of one core limb with primary and secondary winding is shown in Figure 4.19 for illustration. Winding and insulation thickness, and other associated variables are listed in Table 4.4.

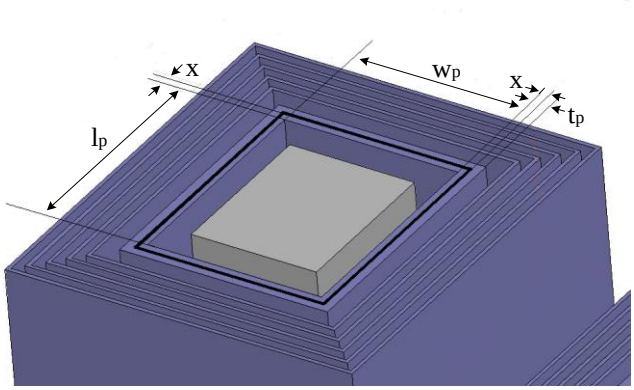


Figure 4.19: Cross section view of primary and secondary windings on one core limb

Table 4.4: Parameter definitions for winding geometry

Variable	Description	Value
t_p	Primary winding thickness	2 *mm*
t_g	Primary to secondary insulation gap thickness	2 *mm*
t_s	Individual secondary sheet thickness	0.45 *mm*
t_{gs}	Insulation thickness between secondary winding sheets	1 *mm*
t_{sp}	Distance between secondary and second primary winding section	25.75 *mm*
L_p	Primary winding cross section length	20.5 *mm*
W_p	Primary winding cross section width	25 *mm*
c_p	Primary winding inner circumference	$2L_p + 2W_p$
c_g	Primary to secondary gap inner circumference	$2L_g + 2W_g$
c_s	Secondary winding inner circumference	$2L_s + 2W_s$
c_{sn}	nth secondary winding layer inner circumference	$c_s + 8(n-1)(t_s + t_{gs})$
c_{gsn}	nth secondary interlayer gap inner circumference	$c_s + 8t_s + 8(n-1)(t_s + t_{gs})$
c_{sp}	secondary to second primary section gap inner circumference	c_g

The energy stored in each winding section is calculated using a Matlab m-file program, which is given in Appendix C4. The calculated primary to half secondary leakage inductance is:

$$L_{primary-half\ secondary} = 2 \times \frac{W_{total}}{I_1^2} = 46.4\,\mu H \tag{4.106}$$

Similarly, the MMF distribution for calculating the primary to full secondary leakage inductance is shown in Figure 4.20.

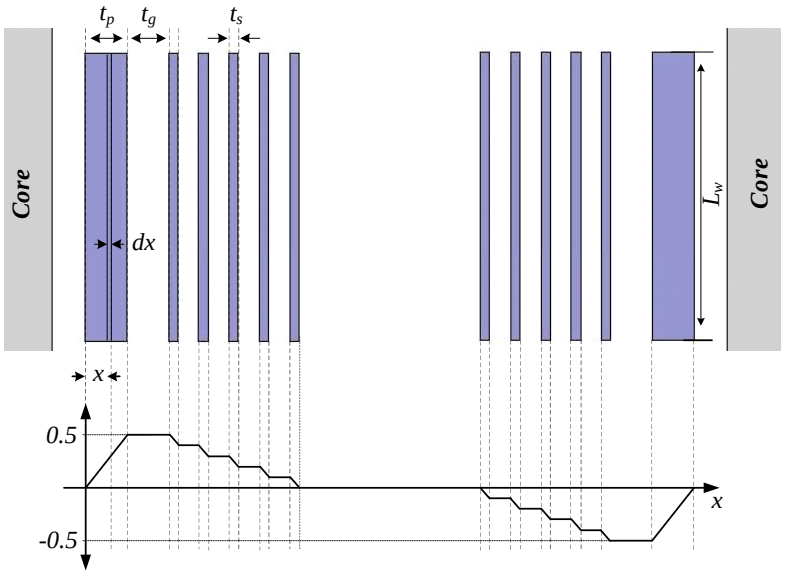


Figure 4.20: MMF distribution across the transformer windings for calculating the primary to secondary leakage inductance

The leakage energy stored in the primary winding W_{p1} and W_{p2}, and primary to secondary insulation gaps W_{g1} and W_{g2} are the same as calculated earlier. However the leakage energy stored in both secondary windings W_{s1} and W_{s2}, as well as the interlayer insulations W_{gsn1} and W_{gsn2}, are:

$$W_{s1} = W_{s2} = \frac{\mu_o N_1^2 I_1^2 t_s}{8k^2 L_w^{'}} \sum_{n=1}^{k} \left[\begin{array}{c} c_{sn} \left(\begin{array}{c} \left((n-1)-k\right)^2 \\ +\left((n-1)-k\right)+\frac{1}{3} \end{array} \right) \\ +t_s \left(\begin{array}{c} 4\left((n-1)-k\right)^2 \\ +\frac{16}{3}\left((n-1)-k\right)+2 \end{array} \right) \end{array} \right] \tag{4.107}$$

$$W_{gs1} = W_{gs2} = \frac{\mu_o N_1^2 I_1^2 t_{gs}}{8L_w^{'}} \sum_{n=1}^{k-1} \left(\frac{n}{k} - 1 \right)^2 \left(c_{gsn} + 4t_{gs} \right) \tag{4.108}$$

Thus the primary to full secondary leakage inductance referred to the primary side is:

$$L_{primary-full\ secondary} = 2 \times \frac{W_{total}}{I_1^2} = 8.7\,\mu H \tag{4.109}$$

and the total leakage inductance is:

$$L_{total} = L_{primary-half\ secondary} + L_{primary-full\ secondary} = 55.1\,\mu H \tag{4.110}$$

4.5.4 Power loss analysis

a. Core power loss

Core loss is calculated based on a modified power loss equation provided by the manufacturer, which accounts for the input voltage form factor, given by [4.48]:

$$P_{fe} = C_m F^x f^y B^z \tag{4.111}$$

where:

$$C_m = P_o \times \left(\frac{1}{F_o}\right)^x \times \left(\frac{1}{f_o}\right)^y \times \left(\frac{1}{B_o}\right)^z \tag{4.112}$$

The constants F_o, f_0, and B_o are the initial form factor, frequency, and magnetic flux density, at which the power loss P_o is calculated, while F, f, and B are the applied voltage form factor, frequency, and magnetic flux density respectively. The parameters x, y, and z are also provided. Parameter values and an estimate for the core power loss are shown in Table 4.5.

Table 4.5: Core power loss calculation according to the manufacturer's equation

Parameter Values (provided by the manufacturer)	**Core Power Loss**
P_o = 80 W/kg F_o = 1.11 f_o = 100 kHz B_o = 0.3 T x = 1.6 y = 1.8 z = 2	$C_m = 80 \times \left(\frac{1}{1.11}\right)^{1.6} \times \left(\frac{1}{100 \times 10^3}\right)^{1.8} \times \left(\frac{1}{0.3}\right)^2$ $= 7.52 \times 10^{-7}\ kg^{-1}$ $P_{fe} = C_m \times (1)^{1.6} \times \left(14 \times 10^3\right)^{1.8} \times (0.96)^2$ $= 20.13 W/kg$

The core weight is calculated using the material properties (given in Appendix C2), and the selected core volume:

$$M = k_v V \rho_{fe} = 0.8 \times \left(7.74 \times 10^{-5}\, m^3\right) \times \left(7350\, kg/m^3\right) = 0.57\, kg \tag{4.113}$$

where k_v is a volume correction factor to account for insulation thickness and laminations. The estimated maximum core power loss is thus:

$$P_{fe} = 11.47 W \tag{4.114}$$

b. Winding power loss

The primary winding DC resistance, which is calculated for each limb separately, is:

$$R_{DC,1} = \frac{\rho_{cu}\left(MLT\right)_p N_1}{A_{c,1}} = \frac{1.73\times10^{-8}\times107\times10^{-3}\times27}{46\times\pi\left(0.4\times10^{-3}/2\right)^2} = 8.65m\Omega \tag{4.115}$$

The AC to DC resistance ratio at 14 kHz for the chosen Litz wire, to account for the skin and proximity effects, is:

$$F_R = \frac{R_{AC}}{R_{DC}} = 1+\frac{\pi^4 f^2\mu_o^2 n^2 N^2 d_l^6}{192\rho^2 b_c^2} \tag{4.116}$$

$$=1+\frac{\pi^4\times\left(14\times10^3\right)^2\times\left(4\pi\times10^{-7}\right)^2\times46^2\times27^2\times\left(0.4\times10^{-3}\right)^6}{192\times\left(1.73\times10^{-8}\right)^2\times\left(100\times10^{-3}\right)^2} = 1.33 \tag{4.117}$$

However, due to the fact that the current is non-sinusoidal, an effective AC to DC ratio factor is calculated based on Equation (4.82), for an equivalent square wave primary current. Using the calculated leakage inductance, the primary current transition time is calculated from:

$$\because L_{lk} = \frac{V}{\Delta i/\Delta t} \tag{4.118}$$

$$\therefore \Delta t = \frac{\Delta i\times L_{lk}}{V} = \frac{37.04\times55.43\times10^{-6}}{600} = 3.4\,\mu sec \tag{4.119}$$

And the transition time as a fraction of the total period Δ is:

$$\Delta = \frac{3.4\,\mu sec}{71.43\,\mu sec} = 0.04 \tag{4.120}$$

The effective frequency is then:

$$f_{eff} = \frac{f_1}{\pi}\sqrt{\frac{6}{\Delta(3-4\Delta)}} = 2\times14\times10^3\sqrt{\frac{6}{0.04(3-4\times0.04)}} \cong 22.3kHz \tag{4.121}$$

The equivalent resistance ratio factor is:

$$F_{R,RMS} = 1+\left(F_R\left(f_1\right)-1\right)\frac{f_{eff}^2}{f_1^2} = 1+\left(1.3315-1\right)\times\left(\frac{22.3}{14}\right)^2 = 2.51 \tag{4.122}$$

The total primary resistance is:

$$R_{AC,1} = 2\times R_{DC,1}\times F_{R,RMS} = 43.4m\Omega \tag{4.123}$$

And the primary winding power loss is:

$$P_1 = I_1^2 R_{AC,1} = 14.87W \tag{4.124}$$

For the expected secondary winding current waveform, the Fourier series expansion RMS currents generated using Matlab are shown in Table 4.6.

Table 4.6: Harmonic power loss in secondary winding according to the calculated resistance ratio

Harmonic (kHz)	RMS Current (A)	R_{AC}/R_{DC}	R_{AC} ($\mu\Omega$)	Power Loss (W)
0	409.01	1	11.38	1.9
1 (Fund. 14)	426.03	1.69	19.3	3.49
2 (28)	115.28	3.69	42	0.56
3 (42)	86.57	6.77	77	0.58
4 (56)	81.51	10.62	120.9	0.8
5 (70)	8.79	14.94	170	0.01
6 (84)	42.84	19.43	221.1	0.41
7 (98)	12.18	23.88	271.8	0.04
8 (112)	14	28.15	320.3	0.06
9 (126)	8.82	32.15	365.8	0.02
13 (182)	4.25	45	512.1	0.01
14 (196)	4.62	47.51	540.6	0.02
16 (224)	6.03	51.85	590	0.03
Total power loss per secondary winding P_2				7.93 W

Therefore, the transformer winding total power loss is:

$$P_{cu} = P_1 + 2P_2 = 30.73W \tag{4.125}$$

4.6 Finite element analysis using Maxwell 2D and 3D simulator

4.6.1 2D finite element analysis

Transformer design and operation is first collaborated using Maxwell 2D and 3D simulators, before implementation. Maxwell 2D is only used to check the maximum operating core flux density, to verify that core saturation does not occur. The winding arrangement and maximum core flux density are shown in Figure 4.21.

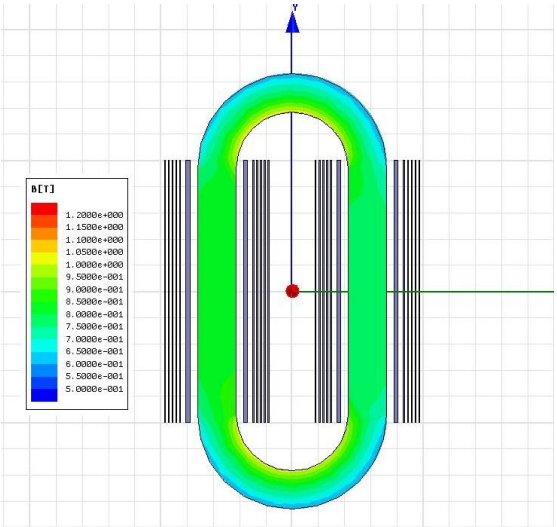


Figure 4.21: Maximum operating flux density through the core

4.6.2 3D finite element analysis

a. Transient analysis

The Maxwell finite element analysis simulator links the transformer model to a circuit simulator, for assessing the transformer transient response. The circuit diagram used in conjunction with the Maxwell simulator for transient analysis is shown in Figure 4.22.

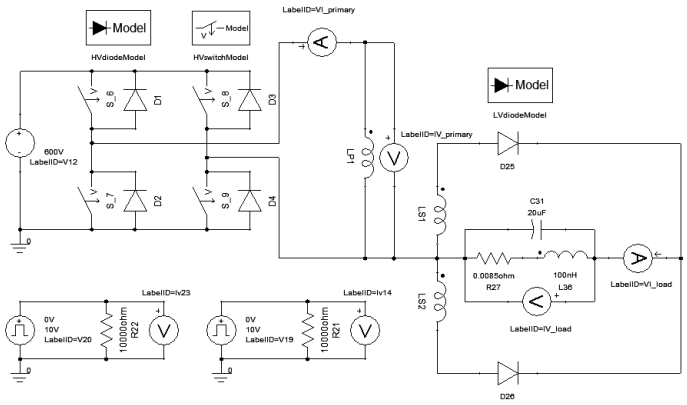


Figure 4.22: DC/DC converter schematic using Maxwell circuit editor

The transformer core and windings are captured in the geometry editor as shown in Figure 4.23. Copper material properties are then assigned to the windings, while the Nnoperm® core material properties obtained from the manufacturer, are added to the core model. The primary winding current and voltage for one cycle is shown in Figure 4.24, with a primary voltage duty cycle of 98%. Centre tapped secondary winding voltages and currents are shown in Figure 4.25. Currents are measured through individual sheet layers to show the current distribution due to proximity effects as shown in Figure 4.25c and Figure 4.25d for secondary windings 1 and 2 respectively. The output load voltage and current are shown in Figure 4.26, while the copper and core losses are shown in Figure 4.27.

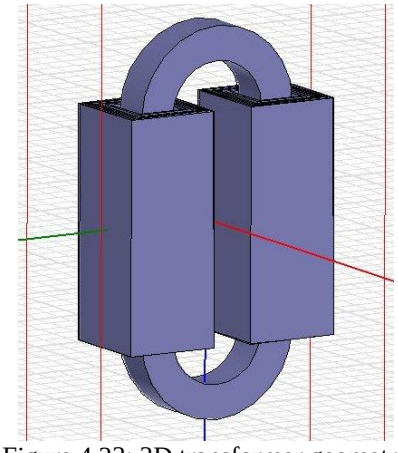


Figure 4.23: 3D transformer geometry

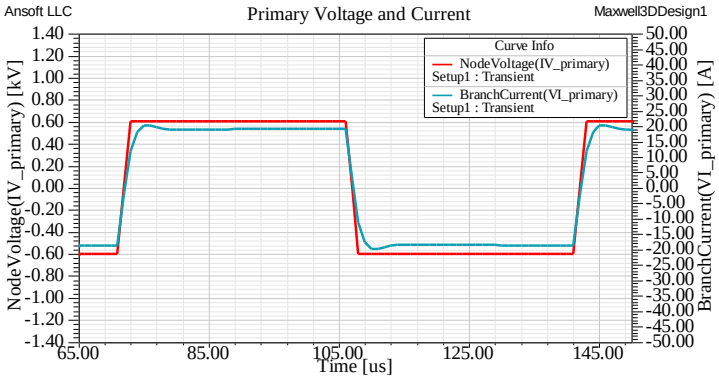


Figure 4.24: Transformer primary winding voltage and current

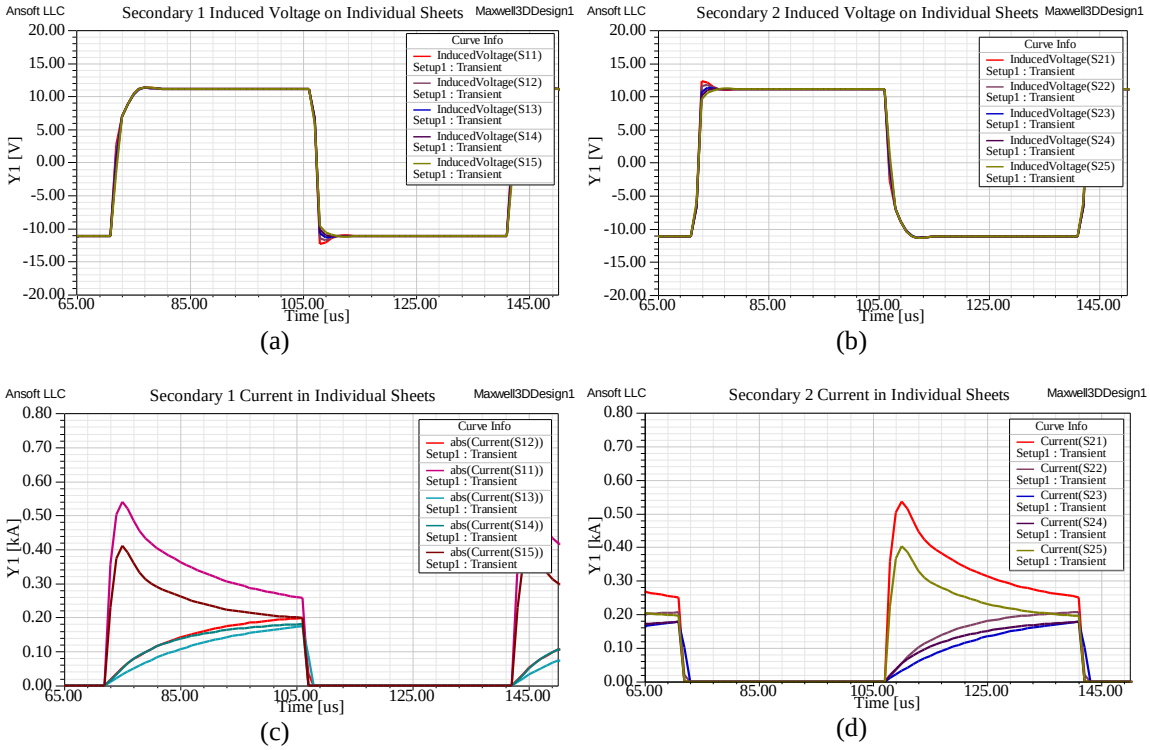


Figure 4.25: (a) Secondary winding 1 voltage, (b) secondary winding 2 voltage, (c) individual sheet currents for secondary winding 1, and (c) individual sheet currents for secondary winding 2

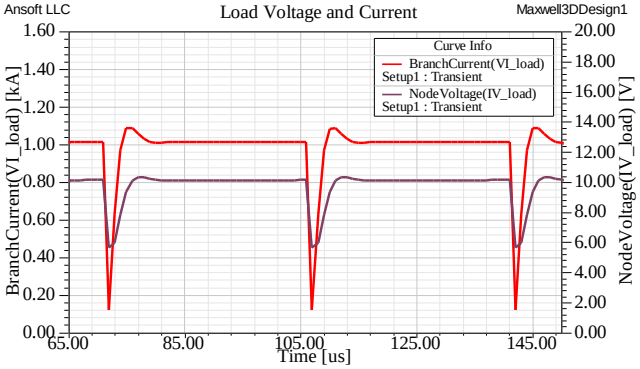


Figure 4.26: Load voltage and current

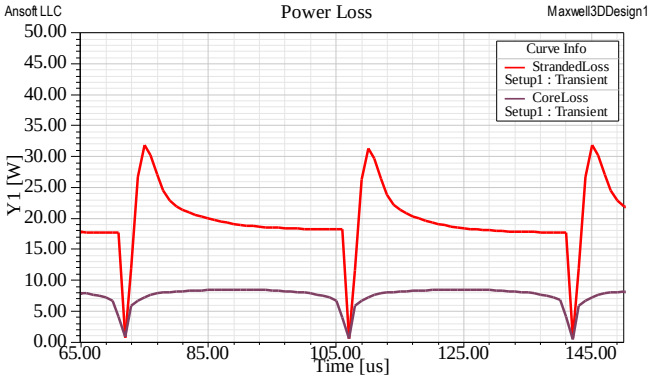


Figure 4.27: Core and winding power loss

b. Leakage Inductance Calculation

Eddy current analysis simulations are carried out for the transformer core and winding geometry shown in Figure 4.23. The leakage inductance is calculated by calculating the winding terminal inductance while all secondary windings are short circuited. Two simulations are performed to calculate the total leakage inductance; the first with one secondary shorted to calculate the primary to one secondary leakage inductance, and the other with both secondary windings shorted to calculate the primary to full secondary leakage inductance component. Simulation results are shown in Table 4.7.

Table 4.7: Leakage inductance simulation results

Primary to one secondary leakage inductance	37.84 μH
Primary to full secondary leakage inductance	5.17 μH
Total leakage inductance	43.02 μH

c. Effect of Bus-Bar Terminals

High current bus-bar terminals are used for connecting the transformer secondary winding to the rectifier circuit. The inductances of the terminals, as well as the rectifier circuit layout add to the leakage inductance of the transformer, and can severely affect circuit performance. The winding arrangement with the added secondary termination is shown in Figure 4.28.

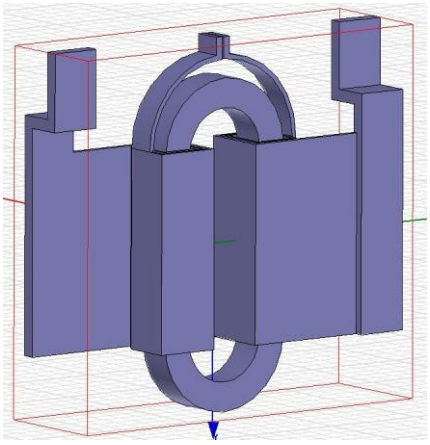


Figure 4.28: 3D transformer geometry with secondary winding with bus-bar terminals

The increase in leakage inductance can be directly observed through the primary current waveform as shown in Figure 4.29. The transition time taken to reverse the current direction is increased from 3.4 μs to 7 μs, which is due to the presence of nearly twice the leakage inductance compared to the transformer without the bus-bar terminals. The effective secondary voltage duty cycle is also reduced for both secondary windings as shown in Figure 4.30a and 4.30b respectively. The power loss is also increased due to the solid copper conductors, as shown in Figure 4.32. Eddy current analysis leakage inductance results are shown in Table 4.8.

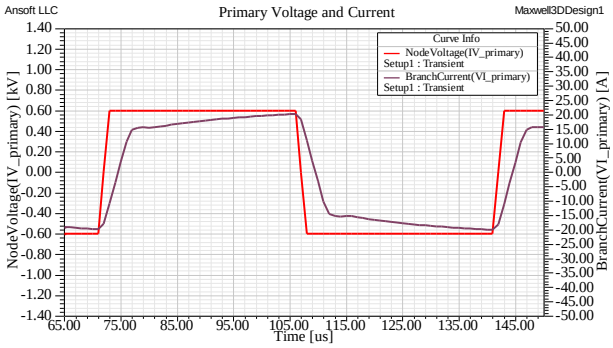
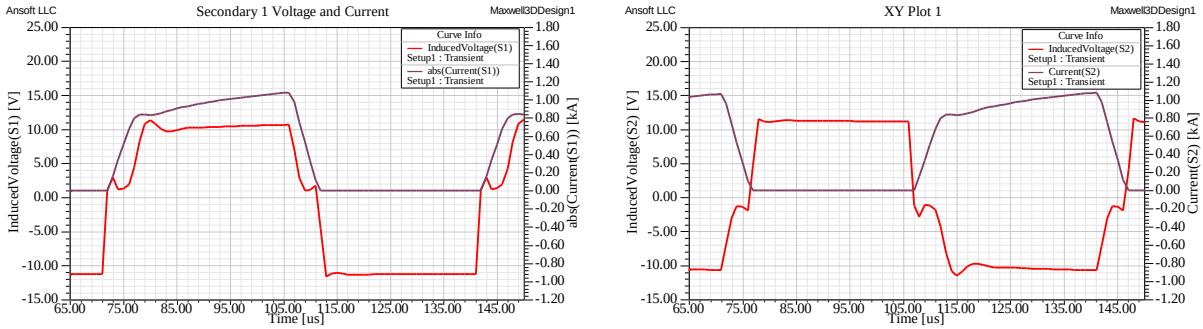


Figure 4.29: Primary winding voltage and current



(a) (b)

Figure 4.30: (a) Secondary winding 1 voltage and current, and (b) Secondary winding 2 voltage and current

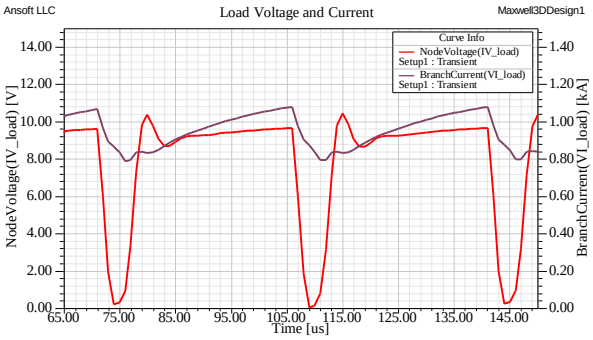


Figure 4.31: Load voltage and current

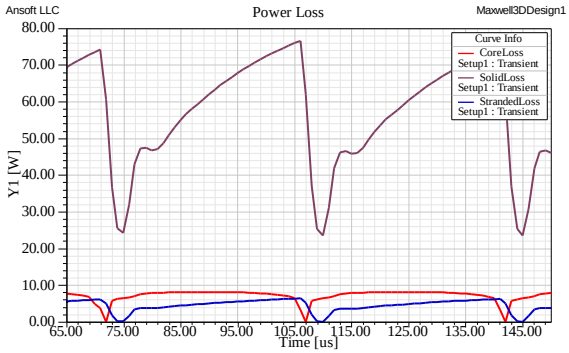


Figure 4.32: Core and winding power loss

Table 4.8: Transformer leakage inductance for the case of added secondary bus-bar terminals

Primary to one secondary leakage inductance	73.6 μH
Primary to full secondary leakage inductance	20 μH
Total leakage inductance	93.6 μH

4.7 Summary and discussion

A high frequency (14 kHz) nanocrystalline core based transformer design has been presented. Nanocrystalline materials can significantly reduce overall transformer volume due to higher saturation flux density, which results in fewer winding turns for a given voltage. Thin copper sheets are used for the high current secondary windings. Different power loss components were analytically estimated. Leakage inductance was calculated based on an energy storage approach, which is directly related to the winding arrangement and geometry. Bus bars are used to provide high current winding terminations, which increase the reflected leakage inductance to the primary side. Finally, finite element analysis simulations validated the design. Comparison between calculations and FEA simulation results are shown in Table 4.9.

Table 4.9: Comparison between calculations and FEA simulation results for different power loss components and leakage inductance calculations

	Calculations	**FEA Simulation without bus bar terminals**	**FEA simulation with bus bar terminals**
Primary winding power loss	14.87 W	21 W combined	8 W
Secondary winding power loss	15.86 W		59 W
Core power loss	11.5 W	9.1 W	7.1 W
Total losses	42.2 W	30.1 W	74.1 W
Leakage inductance	55.1 µH	43.02 µH	93.6 µH

References

[4.1] R.S. Elliott, *"The History of Electromagnetics as Hertz would Have Known It"*, IEEE Transactions on Microwave Theory and Techniques, Volume 36, pp. 806-823, 1988.

[4.2] R.M. Del Vecchio, B. Poulin, P.T. Feghali, D.M. Shah, R. Ahuja, *"Transformer Design Principles, with Applications to Core-Form Power Transformers"*, CRC Press, ISBN: 9781439805824, 2002.

[4.3] J.W. Coltman, *"The Transformer"*, Scientific American, Volume 258, pp. 89-95, 1988.

[4.4] *"Building the World's Largest Tesla Coil - History and Theory"*, Proceedings of the Twenty-Second Annual North American Power Symposium, pp. 128-135 1990.

[4.5] M.K. Kazimierczuk, *"High-Frequency Magnetic Components"*, John Wiley and Sons, Ltd, ISBN: 978-0-470-71453-9, 2009.

[4.6] J.H. Harlow, *"Electric Power Transformer Engineering"*, CRC Press, ISBN: 0-8493-1704-5, 2004.

[4.7] C. Quinn, K. Rinne, T. O'Donnell, M. Duffy, C.O. Mathuna, *"A Review of Planar Magnetic Techniques and Technologies"*, Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition, Volume 2, pp. 1175-1183, 2001.

[4.8] S. Ramakrishnan, R.L. Steigerwald, J.A. Mallick, *"A comparison study of low-profile power magnetics for high-frequency, high-density switching converters"*, Twelfth Annual Applied Power Electronics Conference and Exposition, Volume 1, pp. 388-394, 1997.

[4.9] N. Dai, A.W. Lofti, C. Skutt, W. Tabisz, F.C. Lee, *"A comparative study of high-frequency, low-profile planar transformer technologies"*, Ninth Annual Applied Power Electronics Conference and Exposition, Volume 1, pp. 226-232, 1994.

[4.10] A.J. Moses, J. Leicht, *"Power loss of non oriented electrical steel under square wave excitation"*, IEEE Transactions on Magnetics, Volume 37, pp. 2737-2739, 2001.

[4.11] D. Lin, P. Zhou, W.N. Fu, Z. Badics, Z.J. Cendes, *"A dynamic core loss model for soft ferromagnetic and power ferrite materials in transient finite element analysis"*, IEEE Transactions on Magnetics, Volume 40, pp. 1318-1321, 2004.

[4.12] C.R. Sullivan, *"Optimal choice for number of strands in a litz-wire transformer winding"*, IEEE Transactions on Power Electronics, Volume 14, pp. 283-291, 2002.

[4.13] R.W. Erickson, D. Maksimovie, *"Fundamentals of Power Electronics"*, Kluwer Academic Publishers, ISBN: 9780792372707, 2001.

[4.14] W.G. Hurley, E. Gath, J.G. Breslin, *"Optimizing the AC resistance of multilayer transformer windings with arbitrary current waveforms"*, IEEE Transactions on Power Electronics, Volume 15, pp. 369-376, 2000.

[4.15] J.C. Fothergill, P.W. Devine, P.W. Lefley, *"A novel prototype design for a transformer for high voltage, high frequency, high power use"*, IEEE Transactions on Power Delivery, Volume 16, pp. 89-98, 2001.

[4.16] W.G. Hurley, W.H. Wolfle, J.G. Breslin, *"Optimized transformer design: inclusive of high-frequency effects"*, IEEE Transactions on Power Electronics, Volume 13, pp. 65-659, 1998.

[4.17] W.G. Hurley, *"Optimizing core and winding design in high frequency transformers"*, IEEE International Power Electronics Congress Technical Proceedings, CIEP '96, pp. 2-13, 1996.

[4.18] G. Gu, Q. Li, *"Optimization design of transformer used in switching power supply with high power density"*, IEEE 6th International Power Electronics and Motion Control Conference, IPEMC '09, pp. 1250-1253, 2009.

[4.19] H.R. Karampoorian, G. Papi, A. Zadehgol, *"Volume and loss optimization of high frequency transformer for compact switch mode power supply considering corrected waveform factor"*, IEEE Power India Conference, pp. 110-116, 2006.

[4.20] R.B. Ridley, C. Zhou, F.C.Y. Lee, *"Application of nonlinear design optimization for power converter components"*, IEEE Transactions on Power Electronics, Volume 5, pp. 29-40, 1990.

[4.21] R. Petkov, *"Optimum design of a high-power, high-frequency transformer"*, IEEE Transactions on Power Electronics, Volume 11, pp. 33-42, 1996.

[4.22] G. Callander, A. Gardiner, S. Johnson, *"Analytical minimal loss design of transformers for high frequency switch mode convertors"*, Tenth Annual

Applied Power Electronics Conference and Exposition, APEC '95, pp. 361-366, 1995.

[4.23] J. Lloyd H. Dixon, *"The Effects of Leakage inductance on Switching Power Supply Performance"*, Unitrode Power Supply Design, Application Note, 1990.

[4.24] P.L. Dowell, *"Effects of eddy currents in transformer windings"*, Proceedings of the Institution of Electrical Engineers, Volume 113, pp. 1387-1394, 1966.

[4.25] X. Nan, C.R. Sullivan, *"An improved calculation of proximity-effect loss in high-frequency windings of round conductors"*, IEEE 34th Annual Power Electronics Specialist Conference, PESC '03., 2003.

[4.26] A.D. Podoltsev, I.N. Kucheryavaya, B.B. Lebedev, *"Analysis of effective resistance and eddy-current losses in multiturn winding of high-frequency magnetic components"*, IEEE Transactions on Magnetics, Volume 39, pp. 539-548, 2003.

[4.27] J.A. Ferreira, *"Ånalytical computation of AC resistance of round and rectangular litz wire windings"*, IEE Proceedings Electric Power Applications, Volume 139, pp. 21-25 1992.

[4.28] J.A. Ferreira, *"Improved analytical modeling of conductive losses in magnetic components"*, IEEE Transactions on Power Electronics, Volume 9, pp. 127-131, 1994.

[4.29] J. Schutz, J. Roudet, A. Schellmanns, *"Modeling Litz wire windings"*, IEEE Industry Applications Conference. Thirty-Second IAS Annual Meeting, IAS '97, 1997.

[4.30] G. Bertotti, *"General properties of power losses in soft ferromagnetic materials"*, IEEE Transactions on Magnetics, Volume 24, pp. 621-630, 1988.

[4.31] J. Reinert, A. Brockmeyer, R.W. De Doncker, *"Calculation of Losses in Ferro- and Ferrimagnetic Materials Based on the Modified Steinmetz Equation"*, IEEE Thirty-Fourth IAS Annual Meeting Conference, Volume 37, pp. 1055-1061, 1999.

[4.32] C.P. Steinmetz, *"On the Law of Hysteresis"*, Procedings of the IEEE, Volume 72, pp. 197-221, 1984.

[4.33] B.W. Williams, *"Principles and Elements of Power Electronics: Devices, Drivers, Applications, and Passive Components"*, Published by Barry W. Williams, ISBN: 978-0-9553384-0-3, 2006.

[4.34] A. Makino, T. Hatanai, Y. Naitoh, T. Bitoh, A. Inoue, T. Masumoto, *"Applications of Nanocrystalline Soft Magnetic Materials Fe-M-B (M=Zr, Nb) Alloys NANOPERM"*, IEEE Transactions on Magnetics, Volume 33, pp. 3793-3798, 1997.

[4.35] W. Shen, F. Wang, D. Boroyevich, C.W. Tipton, *"High-Density Nanocrystalline Core Transformer for High-power High-Frequency Resonant Converter"*, IEEE Transactions on Industry Applications, Volume 44, pp. 213-222, 2008.

[4.36] W. Shen, F. Wang, D. Boroyevich, C.W. Tipton, *"High Power Density Nanocrystalline Core Transformer Design for Resonant Converter Systems"*, Fourtieth IAS Annual Meeting Industry Applications Conference, Volume 3, pp. 2216-2222, 2005.

[4.37] M. Giesselmann, T. Vollmer, R. Edwards, T. Roettger, M. Walavalkar, *"Compact HV-DC Power Supply"*, Proceedings of the IEEE International Power Modulators and High Voltage Conference, pp. 242-245, 2008.

[4.38] R.C. Edwards, M.G. Giesselmann, *"Characterization of a High Power Nanocrystalline Transformer"*, IEEE 34th International Conference on Plasma Science, pp. 869-869, 2007.

[4.39] W.A. Reass, S.E. Apgar, D.M. Baca, D.L. Borovina, J.T. Bradle, III, J.D. Doss, J.M. Gonzales, R.F. Gribble, T.W. Hardek, M.T. Lynch, D.E. Rees, P.J. Tallerico, P.G. Trujillo, D.E. Anderson, D.A. Heidenreich, J.D. Hicks, V.N. Leontiev, *"Design, status, and first operations of the Spallation Neutron Source polyphase resonant converter modulator system"*, Proceedings of the Particle Accelerator Conference, 1, pp. 553-557, 2003.

[4.40] S.K. Mazumder, *"Hybrid modulation and new technologies for high-frequency high-power multiphase power system"*, 34th Annual Conference of IEEE Industrial Electronics, pp. 435-441, 2008.

[4.41] W.A. Reass, D.M. Baca, R.F. Gribble, D.E. Anderson, J.S. Przybyla, R. Richardson, J.C. Clare, M.J. Bland, P.W. Wheeler, *"High-Frequency Multimegawatt Polyphase Resonant Power Conditiong"*, IEEE Transactions on Plasma Science, 33, pp. 1210-1219, 2005.

[4.42] D. Vinnikov, J. Laugis, I. Galkin, *"Middle-Frequency Isolation Transformer Design Issues for the High-Voltage DC/DC Converter"*, IEEE Power Electronics Specialists Conference, pp. 1930-1936, 2008.

[4.43] S.V. Kulkarni, S.A. Khaparde, *"Transformer Engineering Design and Practice"*, Marcel Dekker, Inc., ISBN: 0-8247-5653-3, 2005.

[4.44] W.G. Hurley, D.J. Wilcox, *"Calculation of Leakage Inductance in Transformer Windings"*, IEEE Transactions on Power Electronics, Volume 9, pp. 121-126, 1994.

[4.45] Z. Ouyang, O.C. Thomsen, M. Andersen, *"The Analysis and Comparison of Leakage Inductance in Different Winding Arrangements for Planar Transformer"*, International Conference on Power Electronics and Drive Systems, PEDS 2009, pp. 1143-1148, 2009.

[4.46] J.P. Vandelac, P.D. Ziogas, *"A novel approach for minimizing high-frequency transformer copper losses"*, IEEE Transactions on Power Electronics, Volume 3, pp. 266-277, 1988.

[4.47] C.R. Sullivan, *"Optimal choice for the number of strands in a litz-wire transformer winding"*, IEEE Transactions on Power Electronics, Volume 14, pp. 283-291, 1999.

[4.48] Private Communication with Magnetec Gmbh.

Chapter 5

Synchronous Rectification and Parallel Operation of MOSFETs

High current density is demanded in many power electronic applications. MOSFET devices are typically used in high frequency converters to attain a low switching loss, and in rectifiers requiring low conduction losses as synchronous rectifiers. For high output current requirements paralleling more MOSFETs is employed to meet the required ratings. Proper modelling is required to effectively study the current sharing between parallel connected devices, and specify safe margins for a reliable operation.

In this chapter, a Matlab based MOSFET device model is presented. The effect of increased common source and drain inductances, plus including junction capacitances variation with source drain voltage, are first analysed. The model is enhanced by including a thermal network to update temperature dependant device parameters. Simulation for two parallel connected devices with drain, then common source inductance mismatch are discussed. The model is extended to n-devices to show the effect of drain and common source inductance mismatch for a large number of paralleled devices. Finally, the model is utilised in a 1 kA synchronous rectifier design, with 10 parallel connected devices.

5.1 Background

Synchronous rectification is used in applications requiring low output voltage and high efficiency, where the forward voltage drop when using a diode rectifier is considered significant [5.1]. The diode rectifier losses in low voltage rectifiers contribute to a major part of the overall converter losses. MOSFET devices possess resistive characteristics in the conduction mode [5.2]. The effective on-resistance for newly developed low voltage MOSFETs can be less than 1 mΩ, with current ratings up to 430 A in a single module, which can be adequately utilised in low-voltage high-current circuit applications requiring high efficiencies. The ratio between the voltage drop across the rectifying device and the output voltage is an important aspect of low voltage requirements. The application of synchronous rectification to forward converters has been broadly introduced and analysed for output voltages of 1.5 V to 5 V. Efficiency improvement

over Schottky diodes due to the lower conduction loss has been reported for output currents up to 15 A, and switching frequencies below 800 kHz [5.3], [5.4]. At higher frequencies and output currents, body diode conduction and reverse recovery loss increase dramatically, and MOSFET advantages diminish [5.5]. However, synchronous MOSFETs with added parallel connected Schottky diodes is reported to improve efficiencies for converters operating up to 10 MHz, provided the interconnecting parasitic inductance is minimised [5.6].

Full-wave rectification methods are used for higher power requirements and better transformer utilisation. The centre tapped topology is proffered for low voltage requirements, as only one device voltage drop is present per rectification path. Hence, higher efficiencies can be obtained over the full bridge configuration [5.7]. However, current doubler and tripler topologies result in lower transformer secondary currents (and hence, losses), by sharing the current with added inductors [5.8], [5.9].

Device paralleling is used when current requirements cannot be met with a single device package. Paralleling can be also used for reducing the on-resistance of the rectifying path, since MOSFET devices possess resistive characteristics.

MOSFETs may be represented by an equivalent temperature dependant resistance for studying the parallel operation at low switching frequencies, where only the conduction losses are to be considered [5.10]. Analysis at higher switching frequencies can be approximated by an added branch inductance, to approximate the turn-on current transients [5.11]. Including different device parasitic components, such as channel capacitances and terminal inductances (drain, gate and common source inductances), give more accurate results to the device switching behaviour. Minimisation of these inductances is required to obtain optimum switching performance. Trade-offs are between switching overshoot and oscillations, and the associated switching loss [5.12].

In case of paralleled devices, drain and common source inductance mismatch, as well as device specific parameters (such as the threshold voltage, transconductance, on-resistance, and junction capacitances), cause current sharing imbalance which may be maintained at suitable levels through power circuit design and parameter screening [5.13]. The use of individually adjusted gate decoupling resistors can also effectively reduce the imbalance in certain cases [5.14]. Series balancing resistors may be used to

equalise conduction currents, but is not a practical solution in case of high current devices [5.15]. The use of coupled inductors in individual device current paths forces the current sharing without introducing excessive conduction power loss, and is a possible solution for reducing the current imbalance in case of unmatched device parameters [5.16].

MOSFET devices parameters are temperature dependant, which should be included in device models to provide realistic simulations and ease circuit design. Different approaches to include electro-thermal device behaviour in device models are presented in [5.17], [5.18], [5.19], [5.20], [5.21], and [5.22]. For circuit design engineers, using accessible device datasheet curves for different parameter variations with temperature is considered better. Parameter variations which are included in most device datasheets are on-resistance, threshold voltage, and breakdown voltage.

Asymmetrical layout or unequal interconnecting paths, lead to different branch inductances. This causes different transient current sharing and steady state device temperatures. Devices in such conditions are subject to different electrical and thermal stresses, and may lead to device failure [5.23]. Device breakdown voltage is inversely proportional to the on-resistance, and cannot be neglected in the case of low voltage applications where the device is chosen for low power loss considerations [5.24], [5.25]. An easily modified, yet accurate approach to simulate devices in such conditions is required.

5.2 Synchronous rectification

Synchronous rectifiers utilise MOSFETs which are switched ON and OFF in synchronism with the supply to obtain the same rectifying action as diodes. A basic half-wave synchronous rectifier circuit is shown in Figure 5.1. The main current conduction path is from the source terminal to the drain terminal [5.26], which is in the same conducting direction as the internal body diode during the positive half cycle. The gate signal is synchronised with the supply; that is, the MOSFET device is turned on during the positive half cycle, and turned off during the negative half cycle.

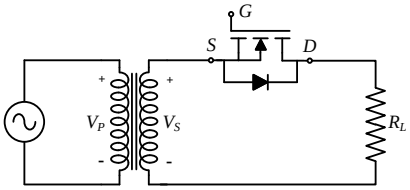


Figure 5.1: Basic half-wave synchronous rectifier

The main advantage of using the MOSFET is the low forward voltage drop, which is considered significant in low output voltage requirements. Synchronous MOSFETs where first introduced in forward buck converter circuits, in which the freewheeling diode is replaced with a MOSFET device as shown in Figure 5.2a. synchronous rectification is also applied to centre tapped rectifiers as shown in Figure 5.2b. The same concept is also applied to other circuit topologies used for low output voltage requirements, such as the current doubler and tripler circuits shown in shown in Figure 5.2c and Figure 5.2d respectively; these take the advantage of the synchronous MOSFET lower forward voltage drop. However, the centre tapped topology remains the better choice for extremely high output current requirements, to avoid extra circuit components. Centre tapped rectification with an output current of 20 MA is proposed in [5.27], where device paralleling is used to achieve the required ratings.

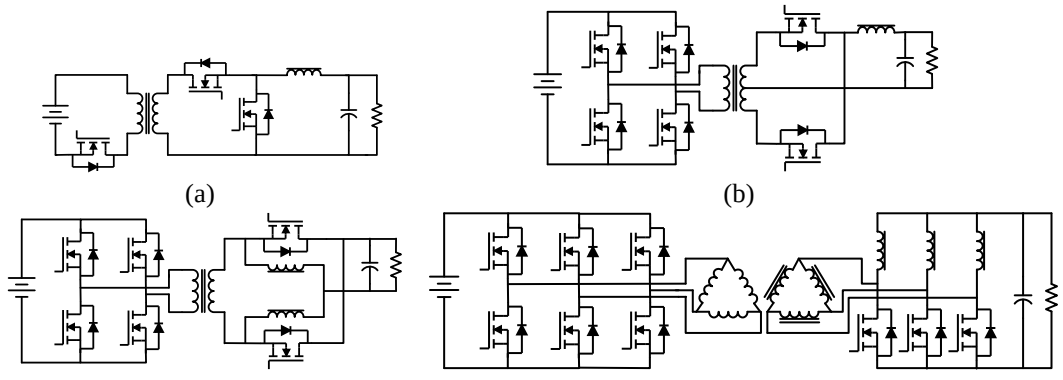
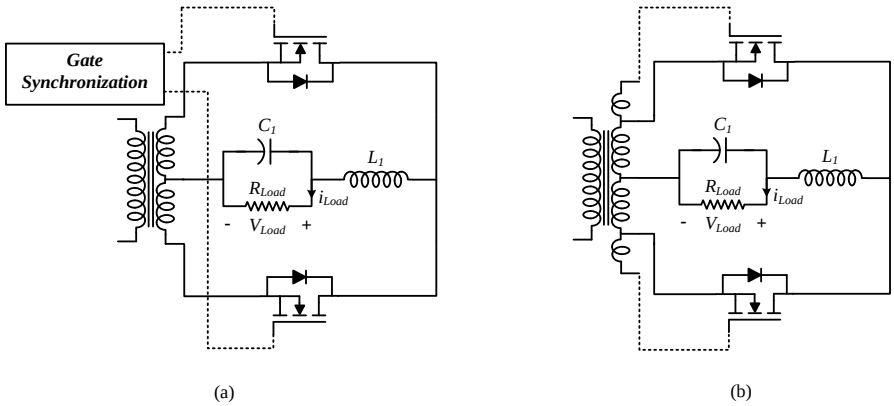


Figure 5.2: Isolated switched mode synchronous rectifier circuit configurations used for low-voltage requirements: (a) forward converter, (b) centre tapped rectifier, (c) current doubler rectifier, and (d) current tripler dc/dc converter

Typically, two driving strategies are used for isolated converters: self-driven methods, which obtain the driving signal directly from the secondary side of the transformer, either through the same or an auxiliary winding, and control driven methods, in which

gate signals are obtained from the primary side controller [5.28]. The two control techniques are illustrated in Figure 5.3.



(a) (b)

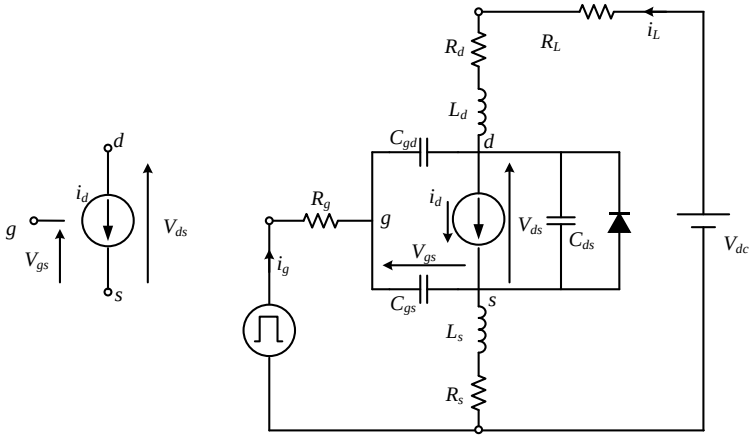
Figure 5.3: (a) Control-driven, and (b) self-driven synchronous rectification

The presence of a parasitic body diode in parallel with the MOSFET makes it impossible to control the turn off while conducting in the forward direction. Parasitic body diode conduction must be avoided as it produces much higher switching losses and voltage drop. When the supply is in the positive direction, the gate signal must be accurately timed to avoid body diode conduction. Body diode conduction may be observed during the switching transition times. However, the gate signals should be adjusted to minimise these periods.

5.3 MOSFET device model for circuit analysis

MOSFETs are voltage controlled devices in which the gate voltage controls turn-on and turn-off. A slow gate voltage rise results in delayed turn-on, and vice versa. For power electronic applications at a switching frequency of a few tens to several hundred kilohertz, the switching times are dominated by the equivalent circuit model parameters and circuit layout parasitic components [5.17]. The basic equivalent circuit model is shown in Figure 5.4a, in which the device is basically represented by a current source. The equivalent circuit including the device parasitic components affecting the device transient behaviour is shown in Figure 5.4b. The device is connected to a resistive load, while the inductive load part may be included into the drain inductance. The device input capacitance ($C_{iss}= C_{gs} + C_{gd}$) and the total gate circuit resistance ($r_s + R_g$) produce the device turn-on delay. The output capacitance ($C_{oss}= C_{ds} + C_{gd}$) is charged and discharged during turn-on and turn-off. The reverse transfer capacitance ($C_{rss}= C_{gd}$),

known as the Miller capacitance, couples the drain source voltage (V_{ds}) to the gate voltage (V_{gs}). These capacitances are nonlinearly inversely proportional to the drain-source voltage. Including this nonlinearity gives more accurate switching loss calculations. The common source and drain inductances (L_s and L_d) are also critical parameters which shape the gate-source voltage, slow down the rise and fall of the drain-source voltage and drain current (i_d), and directly affect device switching losses.



(a) (b)

Figure 5.4: Basic equivalent MOSFET model (a), and equivalent circuit including model parasitic components

The MOSFET switching dynamics are governed by the following simplified conditions for the controlled current source shown in the equivalent circuit model [5.2]:

$$i_d = \begin{cases} 0 & V_{gs} < V_{th} \\ g_{fs}\left(V_{gs} - V_{th}\right) & V_{gs} > V_{th} \text{ and } g_{fs}(V_{gs} - V_{th}) < \dfrac{V_{ds}}{R_{ds(on)}} \\ \dfrac{V_{ds}}{R_{ds(on)}} & V_{gs} > V_{th} \text{ and } g_{fs}(V_{gs} - V_{th}) > \dfrac{V_{ds}}{R_{ds(on)}} \end{cases} \tag{5.1}$$

where g_{fs} is the device transconductance, $R_{ds(on)}$ is the effective channel resistance through the saturation region, and V_{th} is the threshold voltage. The equivalent circuit may then be modelled by a set of differential equations, to aid the analysis. By using Kirchhoff's voltage and current laws for the input loop:

$$V_{gs} = V_g - i_g R_g - L_s \frac{d\left(i_g + i_L\right)}{dt} - \left(i_g + i_L\right) R_s \tag{5.2}$$

$$i_g = C_{iss} \frac{dV_{gs}}{dt} - C_{rss} \frac{dV_{ds}}{dt} \tag{5.3}$$

Equation (5.2) is the gate circuit voltage loop equation, and shows the effect of the common source inductance on the gate circuit. Equation (5.3) shows the effects of both the input capacitances and the reverse transfer capacitance on the switching dynamics. For the output voltage loop:

$$V_{ds} = V_{dc} - i_L \left(R_L + R_d\right) - L_D \frac{di_L}{dt} - L_s \frac{d\left(i_g + i_L\right)}{dt} - \left(i_g + i_L\right) R_s \tag{5.4}$$

$$i_L = i_d + C_{oss} \frac{dV_{ds}}{dt} - C_{rss} \frac{dV_{gs}}{dt} \tag{5.5}$$

Equations (5.1) to (5.5) are modelled using Matlab Simulink, to show the effect of common source and drain inductances variation on the switching performance. The device used for simulations is the IRFP4668PBF, with a current and voltage ratings of 130 A and 200 V respectively, as shown in Appendix D. The device model is used to switch on and off a 1 Ω resistive load at 10 kHz, and 100 V. Two cases are studied, one with a fixed drain inductance value while increasing the common source inductance value, and the other with a fixed common source inductance value while increasing the drain inductance. However, the common source and drain inductances are not only determined by package values, but also include the circuit layout and current path parasitic inductances.

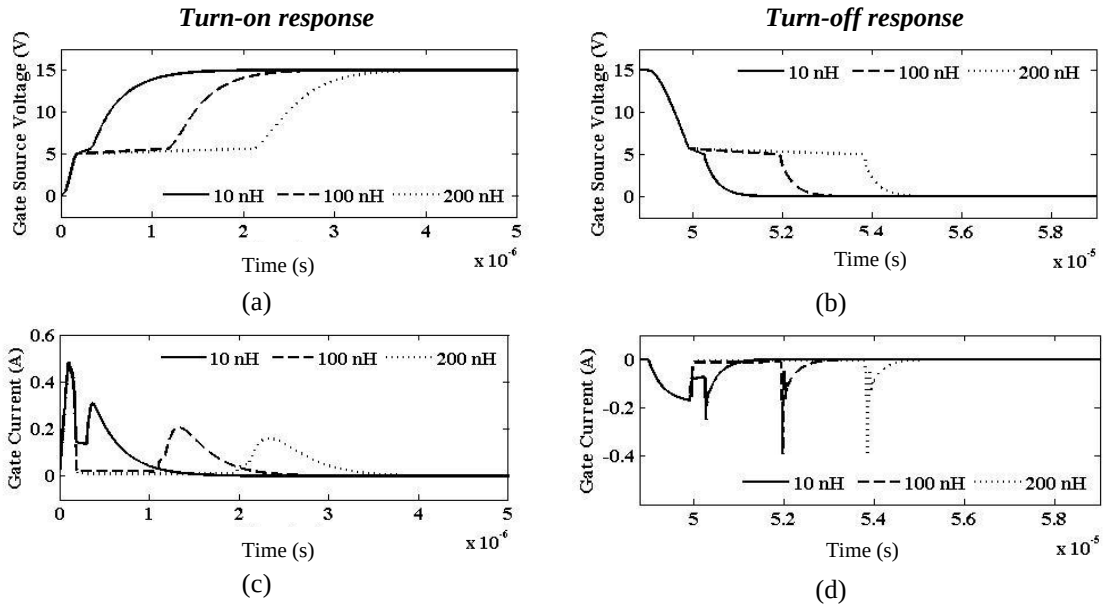
5.3.1 Effect of increased common-source inductance

The device is simulated with a common source inductance of 10, 100, and 200 nH, and a fixed drain inductance of 10 nH. The increase in common source inductance reflects the change in gate and load current as described by (5.2), hence slows down the gate voltage rise and fall during device turn-on and turn-off as shown in Figures 5.3a and 5.3b respectively.

The effect of charging and discharging the input capacitance and the change in the drain source voltage on the gate current is described by Equation (5.3). Gate current waveforms at turn-on and turn-off are shown in Figure 5.3c and Figure 5.3d respectively. Faster device turn-on leads to higher gate current peak values, while peak turn off gate current remains virtually the same.

Increased common-source inductance slows down the source drain voltage as described by Equation (5.4), and reflect on the gate current and gate-source voltage. The drain current is also affected in the active and saturation regions, since it is a function of the gate-source and drain-source voltages respectively. The effect of increased common source inductance on the drain-source voltage and drain current waveforms during turn-on and turn-off are shown in Figure 5.5 parts e to h respectively. Slower voltage and current changes are observed.

Device output capacitance charge and discharge during turn-on and turn-off is included in Equation (5.5), which has a direct effect on the drain-source voltage as shown. The drain current maps the same response due to the fact that most of the switching period occurs in the saturation region, which is represented by the resistive characteristics of the device as given in Equation (5.1), and is shown in Figures 5.5g and 5.5h for turn-on and turn-off respectively. Device turn-on and turn-off power losses increase with increased common-source inductance, due to the larger drain current and source-drain voltage overlap period, as shown in Figure 5.5i and 5.5j respectively.



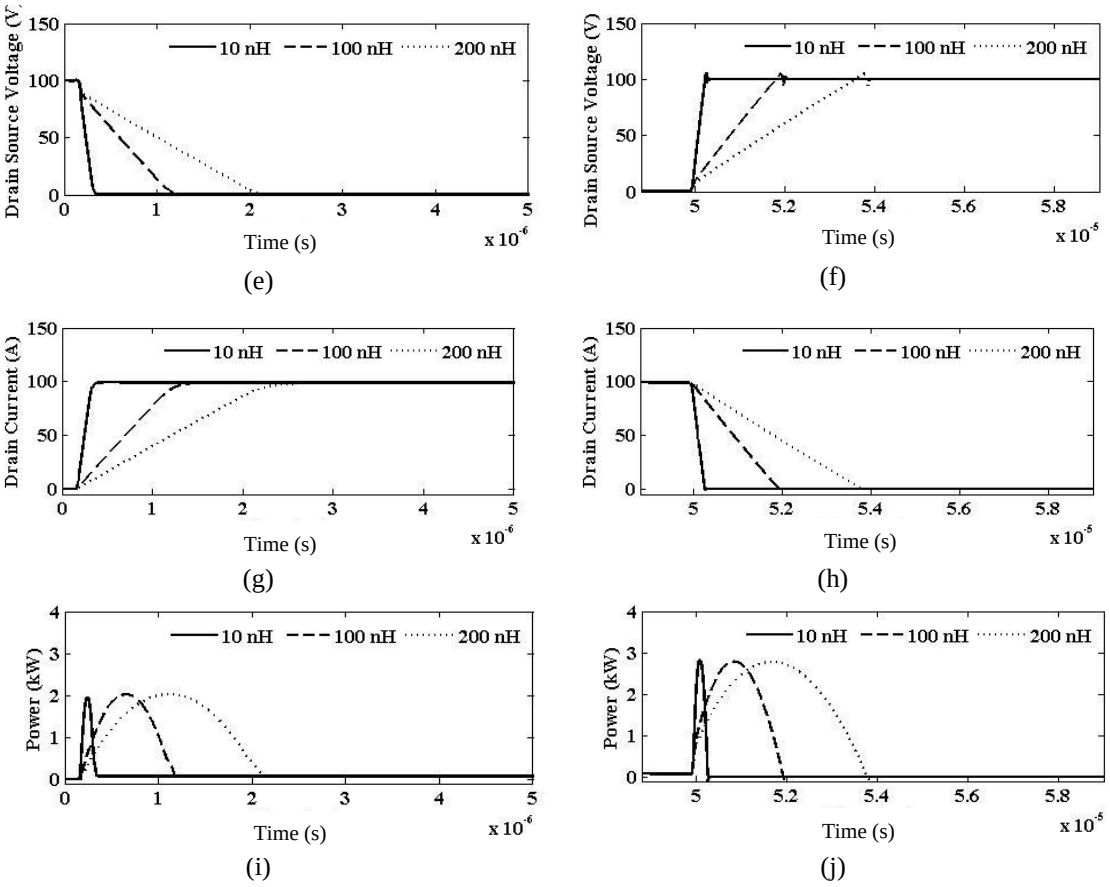


Figure 5.5: The effect of increased common source inductance, with drain inductance kept at 10 nH, on: (a) turn-on and (b) turn-off gate-source voltage, (c) turn-on and (d) turn-off gate current, (e) turn-on and (f) turn-off drain-source voltage, (g) turn-on and (h) turn-off drain current, and (i) turn-on, (j) turn-off power loss

5.3.2 Effect of increased drain inductance

An increased drain inductance has an opposite effect during the turn-on transient of the gate-source voltage, as shown in Figure 5.6a. Increased drain inductance slows down the load current as shown in Figures 5.6g and 5.6h, which is reflected by a higher rate of change in the gate-source voltage as described by Equation (5.2). While at turn-off, drain-source voltage oscillations observed in Figure 5.6f are reflected onto the gate current (Figure 5.6d) and onto the gate-source voltage as shown in Figure 5.6b. The turn-off drain-source voltage oscillations are clamped to the breakdown voltage value by the internal avalanche capability of the device. Reduced rate of change in drain turn-on and turn-off currents are shown in Figures 5.6g and 5.6h respectively. Turn-on power loss decreases with increased in drain inductance as shown in Figure 5.6i, due to the faster drain-source voltage response. However, turn-off losses increase dramatically as shown in Figure 5.6j.

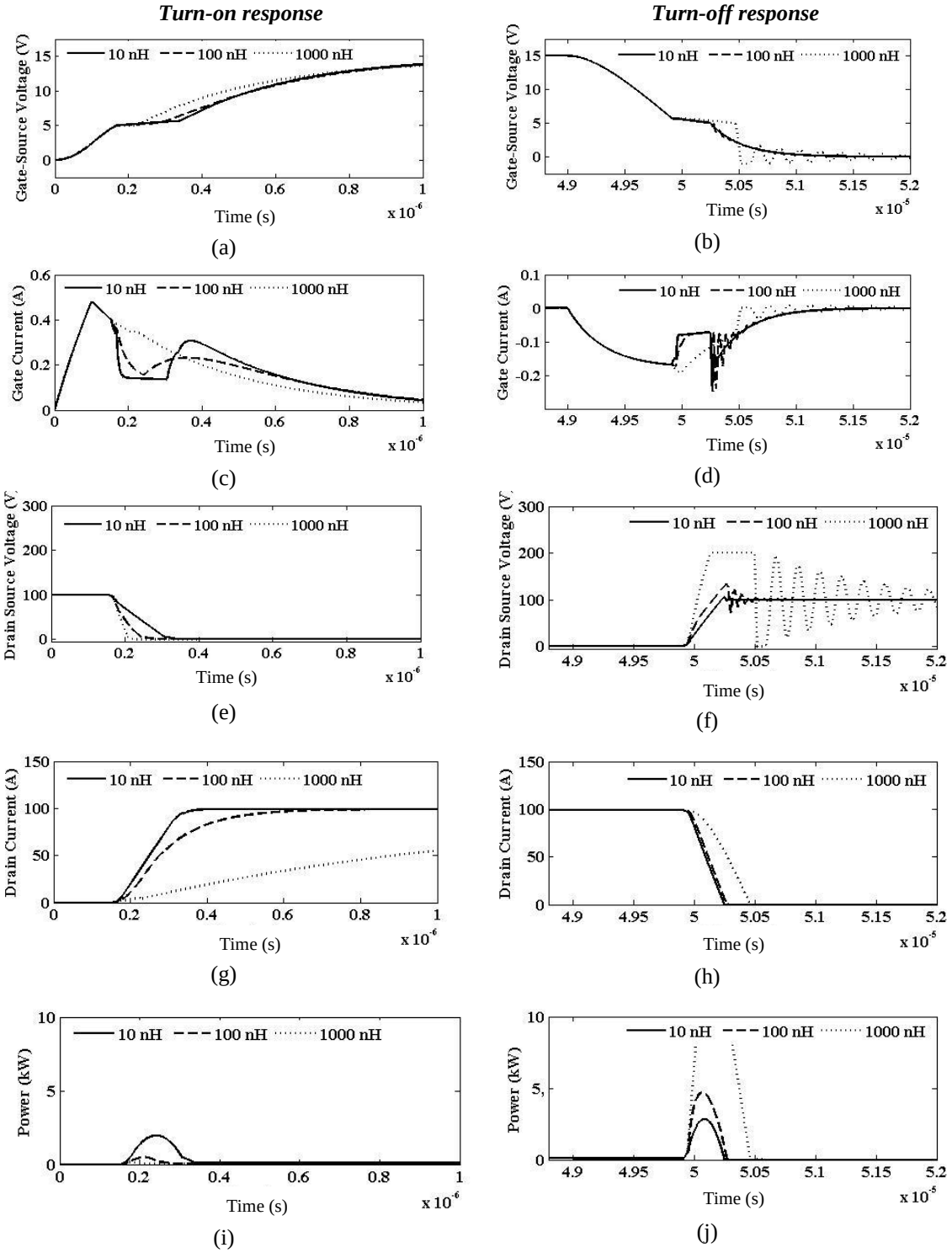
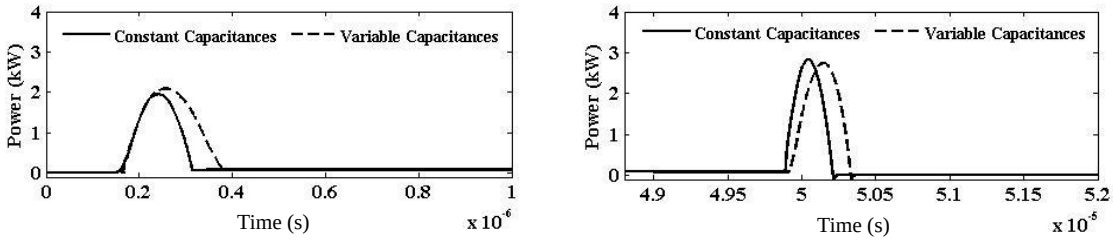


Figure 5.6: The effect of increased drain inductance, with common source inductance kept at 10 nH, on: (a) turn-on and (b) turn-off gate-source voltage, (c) turn-on and (d) turn-off gate current, (e) turn-on and (f) turn-off drain-source voltage, (g) turn-on and (h) turn-off drain current, and (i) turn-on and (j) turn-off power loss

5.3.3 Effect of junction capacitance nonlinearity

Parasitic capacitances directly influence the device model switching waveforms and switching losses [5.29]. Modelling the capacitance variation with drain-source and gate source voltages is complicated, and requires experimental parameter extraction. Different approaches are presented in references [5.30], [5.31], and [5.32]. However, the simplest approach is to use the data given in the manufacturer's datasheets. The capacitance (C_{iss}, C_{oss}, and C_{rss}) variation with the drain-source voltage range are extracted from the manufacturer's datasheet curves as given in Appendix D1, and used in lookup tables to update the capacitance value during simulation. The increase in input capacitance increases the gate-source voltage time constant, and directly affects drain current and drain-source voltage, which cause an increase in turn-on and turn-off losses as shown in Figures 5.7a and 5.7b respectively.



(a) (b)

Figure 5.7: The effect of including the junction capacitances variation with the drain-source voltage on (a) turn-on power loss, and (b) turn-off power loss

5.3.4 Electro-thermal device model

MOSFET device parameters such as the on-resistance, threshold voltage, breakdown voltage, and transconductances are temperature dependant. With most circuit simulators providing results at fixed static temperatures, transient switching behaviour and steady state power loss estimation becomes inaccurate, but is a prime requirement for successful heat sink design.

Electrothermal modelling has been given significant consideration. Different temperature dependant device models using different circuit simulators have been developed. A physical device model formulated as a set of algebraic and partial differential equations, representing the internal dependencies of temperature and electrical variables implemented in spice3 is presented in [5.17]. A spice based model

which includes the electron mobility, drain resistance, threshold voltage, and breakdown voltage temperature dependences is presented in [5.18]. Additional subcircuits which model the model parameters temperature variation, which are not included in the intrinsic spice model, are added as shown in [5.19] and [5.20], and also accounting for capacitance nonlinearities with the drain-source voltage, while VHDL-AMS code is presented in [5.21]. A device model developed in Ansoft Simplorer is presented in [5.22]. The temperature dependant parameters considered in the current Matlab model are the device on-resistance and threshold voltage. The curves given in the datasheet are used as lookup tables according to the instantaneous junction temperature, as shown in Figure 5.8. The device junction temperature is calculated based on the following equivalent thermal model, with a forced air-cooled heat sink:

$$T_j = T_a + \varphi_1 r_1 + \varphi_2 r_2 + \varphi_3 (r_3 + r_{pad} + r_{sink}) \tag{5.6}$$

$$\varphi_1 = P_{loss} - c_1 \frac{dT_j}{dt} \tag{5.7}$$

$$\varphi_2 = \varphi_1 - c_2 \frac{d}{dt}(T_j - \varphi_1 r_1) \tag{5.8}$$

$$\varphi_3 = \varphi_2 - c_3 \frac{d}{dt}(T_j - \varphi_1 r_1 - \varphi_2 r_2) \tag{5.9}$$

where (r_1, r_2, r_3, c_1, c_2, and c_3) are the device equivalent series-connected RC-network components determining the device thermal response, r_{pad} is the thermal pad thermal resistance, r_{sink} is the heat sink thermal resistance, (T_j and T_a) are the junction and ambient temperatures respectively, and (φ_1, φ_2, and φ_3) are the heat flow rates passing through (r_1, r_2, and r_3).

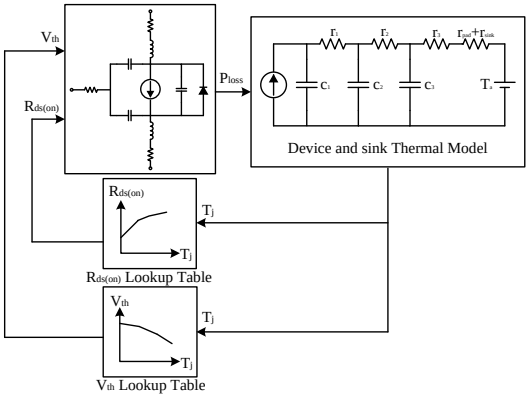


Figure 5.8: Electro-thermal MOSFET model block diagram representation for updating the on-resistance and threshold voltage values

The device thermal parameters are also obtained from the manufacturer's datasheet. Simulation results for the device switching on a resistive load at 10 kHz, 100 V, 100 A, and with equal common source and drain inductances of 10 nH is shown in Figure 5.9. On-resistance, threshold voltage, and instantaneous junction temperature variation with time, in which the junction temperature reaches an average steady state value of 65 ^{o}C, are shown in Figures 5.9a, 5.9b, and 5.9c respectively, with a heat sink thermal resistance of 0.3 ^{o}C/W.

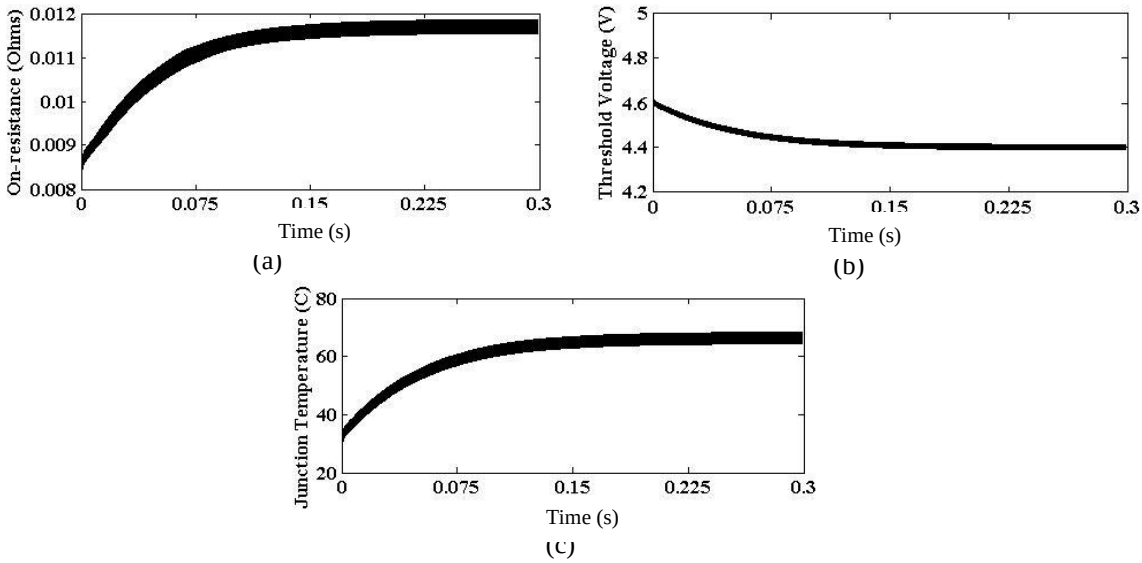


Figure 5.9: MOSFET device electrothermal model (a) transient and steady state junction temperature, (b) varied value of on-resistance until reaching steady state, and (c) varied value of threshold voltage until reaching steady state

5.4 Parallel operation of MOSFETs for higher current output

Paralleling MOSFETs and the associated issues have been widely addressed in the literature, [5.13], [5.14], [5.15], and [5.16] . Dynamic and steady state current sharing between paralleled MOSFETs is directly affected by device parameters and parasitic circuit components. Parallel operation is basically investigated by using the equivalent circuit model, assuming devices are turned on using the same gate signal. The equivalent circuit for two parallel connected devices is shown in Figure 5.10. Based on the equivalent circuit model, the main causes of current imbalance between paralleled devices are:

- Device parameter mismatch, such as the on-resistance ($R_{ds(on)}$), threshold voltage (V_{th}), transconductance (g_{fs}), and parasitic capacitance (C_{ds}, C_{gs}, and C_{ds}).

- Gate drive circuit component mismatch, such as the decoupling resistors (R_{g1} and R_{g2}), and gate loop inductance (L_{s1} and L_{s2}).
- Power circuit drain inductance (L_{d1} and L_{d2}), and common source inductance (L_{s1} and L_{s2}) mismatch due to asymmetrical component layout.

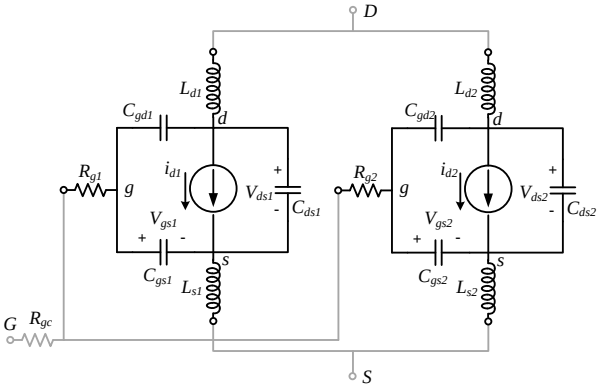


Figure 5.10: The equivalent circuit representation for two parallel connected MOSFET devices

Different device on-resistance causes differences in steady state current sharing. However, thermal runaway conditions do not occur due to the on-resistance positive temperature coefficient. Transconductance and threshold voltage parameter mismatch, as well as differences in drain and common source inductances cause differences in transient current sharing. Gate decoupling resistors (R_{g1} and R_{g2}) are used to adjust the current imbalance caused by difference in Miller capacitances, and parasitic oscillations between paralleled devices [5.13]. Parasitic oscillations may also be eliminated by using ferrite beads [5.33]. However, parasitic oscillations are considered potentially severe for devices paralleled by the manufacturer at the chip level [5.34].

Dynamic and steady state current imbalance is limited over a wide operating range. However, differences in current sharing may lead to excessive thermal stressing and operation beyond the SOA for individual devices, especially in case of a large number of parallel connected devices [5.13]. Device parameter mismatch may be restrained to suitable levels by employing parameter screening, and using devices from the same production batch. Gate drive and power circuit current imbalance causes may be reduced by symmetrical device layout, minimising connection paths, and proper gate drive circuit design. Moreover, thermal coupling reduces thermal stresses between parallel connected devices, and aids current balancing [5.24].

5.4.1 Modelling of two parallel connected devices

Thermal design is an important issue, especially in the case of parallel connected MOSFETs. Parameter mismatch may cause different steady-state device temperatures, and unequal current sharing. Devices having higher junction temperatures carry less current due to their on-resistance positive temperature coefficient. The threshold voltage and device transconductance decrease with increased temperature. Differences in steady state or transient junction temperature would eventually cause one device to turn-on before the other devices causing thermal stresses, even if all gate signals are matched. Breakdown voltage, like the on-resistance, has a positive temperature coefficient. The device with the highest temperature will have the highest breakdown voltage. Breakdown voltage is not considered a critical parameter as long as the appropriate safe margins are used in device rated voltage selection.

However, to investigate the parallel operation of thermally coupled devices, the model previously presented is extended to two parallel connected devices. The equivalent circuit for the devices, showing the interaction between the model and equivalent thermal circuit, is shown in Figure 5.11. The model is developed to investigate the effects of circuit layout on dynamic and steady-state current sharing, which is mainly affected by differences in common source and drain inductances.

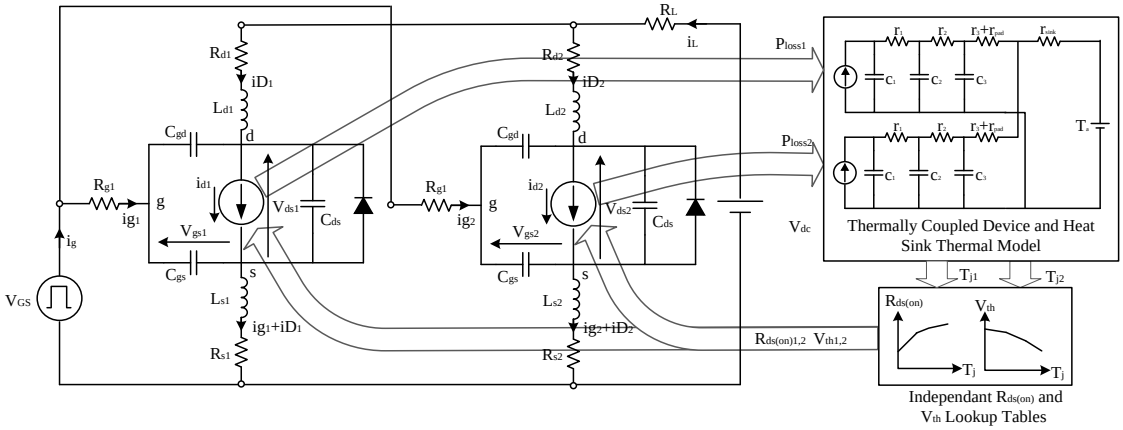


Figure 5.11: Equivalent circuit and thermal coupling model for two parallel connected MOSFETs

The two parallel connected devices are represented by the following differential equations:

$$V_{gs1} = V_g - i_{g1}R_{g1} - L_{s1}\frac{d\left(i_{g1}+i_{D1}\right)}{dt} - \left(i_{g1}+i_{D1}\right)R_{s1} \tag{5.10}$$

$$V_{gs2} = V_g - i_{g2}R_{g2} - L_{s2}\frac{d\left(i_{g2}+i_{D2}\right)}{dt} - \left(i_{g2}+i_{D2}\right)R_{s1} \tag{5.11}$$

$$i_{g1} = C_{\text{iss}1}\frac{dV_{gs1}}{dt} - C_{rss1}\frac{dV_{ds1}}{dt} \tag{5.12}$$

$$i_{g2} = C_{\text{iss}2}\frac{dV_{gs2}}{dt} - C_{rss2}\frac{dV_{ds2}}{dt} \tag{5.13}$$

$$V_{ds1} = V_{dc} - \left(i_{D1}+i_{D2}\right)R_L - i_{D1}R_{d1} - L_{d1}\frac{di_{D1}}{dt} - L_{s1}\frac{d\left(i_{g1}+i_{D1}\right)}{dt} - \left(i_{g1}+i_{D1}\right)R_{s1} \tag{5.14}$$

$$V_{ds2} = V_{dc} - \left(i_{D1}+i_{D2}\right)R_L - i_{D2}R_{d2} - L_{d2}\frac{di_{D2}}{dt} - L_{s2}\frac{d\left(i_{g2}+i_{D2}\right)}{dt} - \left(i_{g2}+i_{D2}\right)R_{s2} \tag{5.15}$$

$$i_{D1} = i_{d1} + C_{oss1}\frac{dV_{ds1}}{dt} - C_{rss1}\frac{dV_{gs1}}{dt} \tag{5.16}$$

$$i_{D2} = i_{d2} + C_{oss2}\frac{dV_{ds2}}{dt} - C_{rss2}\frac{dV_{gs2}}{dt} \tag{5.17}$$

The parallel connected devices are thermally coupled on a common heat sink represented by the following differential equations:

$$T_{j1} = T_a + \varphi_{11}r_{11} + \varphi_{12}r_{12} + \varphi_{13}r_{13} + \varphi_4(r_{pad} + r_{sink}) \tag{5.18}$$

$$T_{j2} = T_a + \varphi_{21}r_{21} + \varphi_{22}r_{22} + \varphi_{23}r_{23} + \varphi_4(r_{pad} + r_{sink}) \tag{5.19}$$

$$\varphi_{11} = P_{loss1} - c_{11}\frac{dT_{j1}}{dt} \tag{5.20}$$

$$\varphi_{21} = P_{loss2} - c_{21}\frac{dT_{j2}}{dt} \tag{5.21}$$

$$\varphi_{12} = \varphi_{11} - c_{12}\frac{d}{dt}(T_{j1} - \varphi_{11}r_{11}) \tag{5.22}$$

$$\varphi_{22} = \varphi_{21} - c_{22}\frac{d}{dt}(T_{j2} - \varphi_{21}r_{21}) \tag{5.23}$$

$$\varphi_{13} = \varphi_{12} - c_{13}\frac{d}{dt}(T_{j1} - \varphi_{11}r_{11} - \varphi_{12}r_{12}) \tag{5.24}$$

$$\varphi_{23} = \varphi_{22} - c_{23}\frac{d}{dt}(T_{j2} - \varphi_{21}r_{21} - \varphi_{22}r_{22}) \tag{5.25}$$

$$\varphi_4 = \varphi_{13} + \varphi_{23} \tag{5.26}$$

The two devices are used to switch a resistive load at 5 kHz, 150V, and 150A, with each device to carry half the total load current. Two different simulation cases allow the study of current sharing, where drain and common source inductance mismatch are considered. The first, in which devices 1 and 2 have equal drain inductances (10 nH) and common source inductances of 10 nH and 20 nH respectively. The second case is for the two devices having equal common source inductance (10 nH) and drain inductances of 10 nH and 100 nH respectively.

a. Case 1:

During the first cycle of operation, the increased common source inductance of device 2 leads to delayed turn-on. Hence device 1 turn-on first and carries a higher transient current. Device 2 then turn-on and starts sharing the load current as shown in Figure 5.12a. By the end of the first load cycle, both devices conduct equal current since both junction temperatures are almost equal.

The turn-on power loss of device 1 is higher due to the increased turn-on transient current, as shown in Figure 5.12b. The turn-off loss of device 2 is higher, due to the extended turn-off time caused by the increased common source inductance, as shown in Figure 5.12c. Junction temperatures for both devices during the first few cycles are shown in Figure 5.12d. Device 1 exhibits a higher initial junction temperature, due to the increased turn-on losses which increases its on-resistance, hence decreasing its current. More current then starts to flow through the other device. Device 2 exhibits a higher turn-off loss than device 1, which is much greater than the increased turn-on loss of device 1, and contributes to further increase in its junction temperature. This situation continues until an equilibrium state is reached. At steady state, device 1 attains a lower

junction temperature as shown in Figure 5.12e, although it carries more transient turn-on current. The threshold voltage of device 2 becomes lower than device 1, hence it turns-on slightly faster. At steady state, the transient current in device 1 decreases compared to that at startup. Further increase in device 2 common source inductance increases the turn-on loss of device 1. It will also dramatically increase the turn-off loss of device 2, to an extent that increases its overall junction temperature more than device 1. Device 2 threshold voltage decreases, turning on device 1 first, which reduces device 1 turn-on loss.

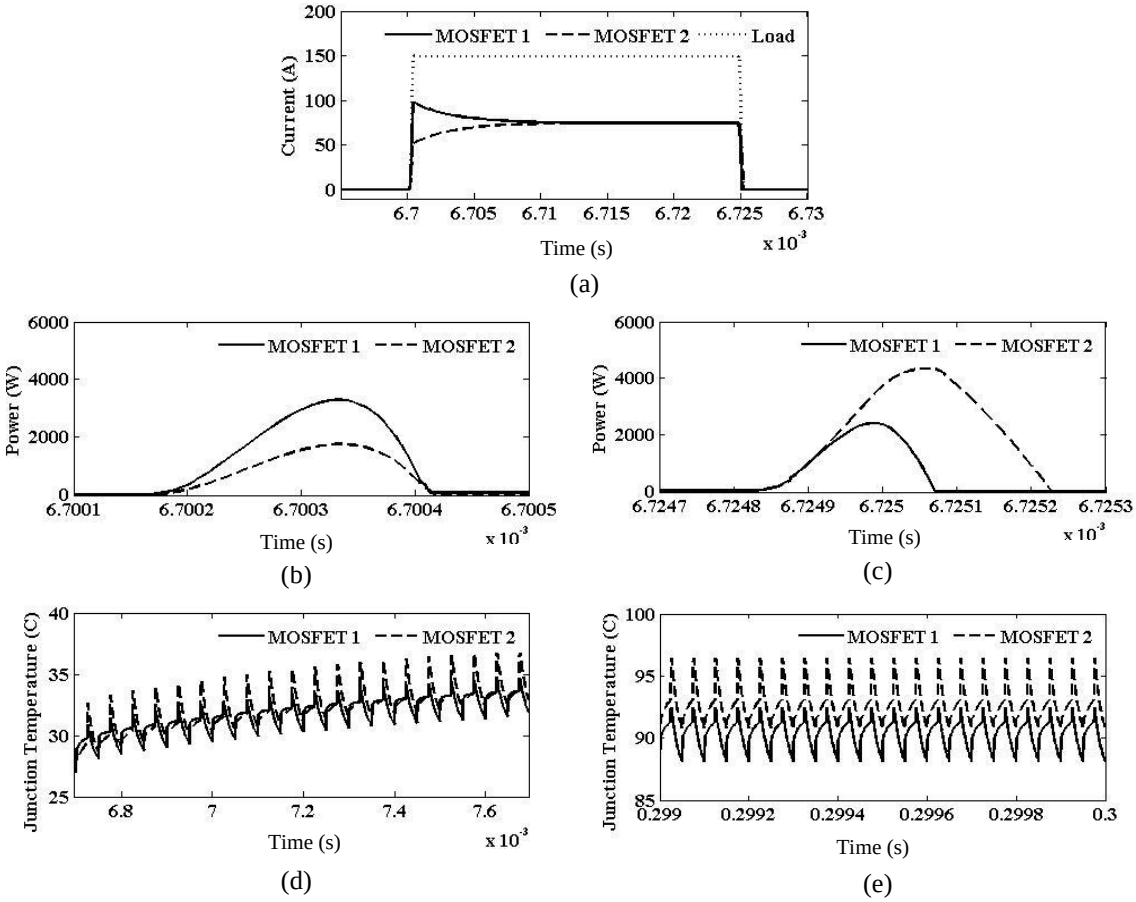


Figure 5.12: (a) First cycle device and load currents, (b) turn-on loss, (c) turn-off loss, (d) junction temperature during the first few cycles, and (e) at steady state operation, for a common source and drain inductances of 20 and 10 nH respectively.

b. Case 2:

With both devices having equal common source inductance (10 nH), and a drain inductance of 10 nH and 100 nH, for devices 1 and 2 respectively, an increase in device 1 turn-on current is also observed as shown in Figure 5.13a. Device 2 exhibits higher

turn-off loss as shown in Figure 5.13b, but less than device 1 turn-on loss. The increased turn-on loss of device 1 increases its junction temperature, hence increases its on-resistance. This causes increased steady-state conduction loss. Device 1 junction temperature then starts to rise as shown in Figure 5.13c. At steady state, device 1 attains a higher junction temperature as shown in Figure 5.13e, which is the opposite to the case where device 2 has higher common source inductance.

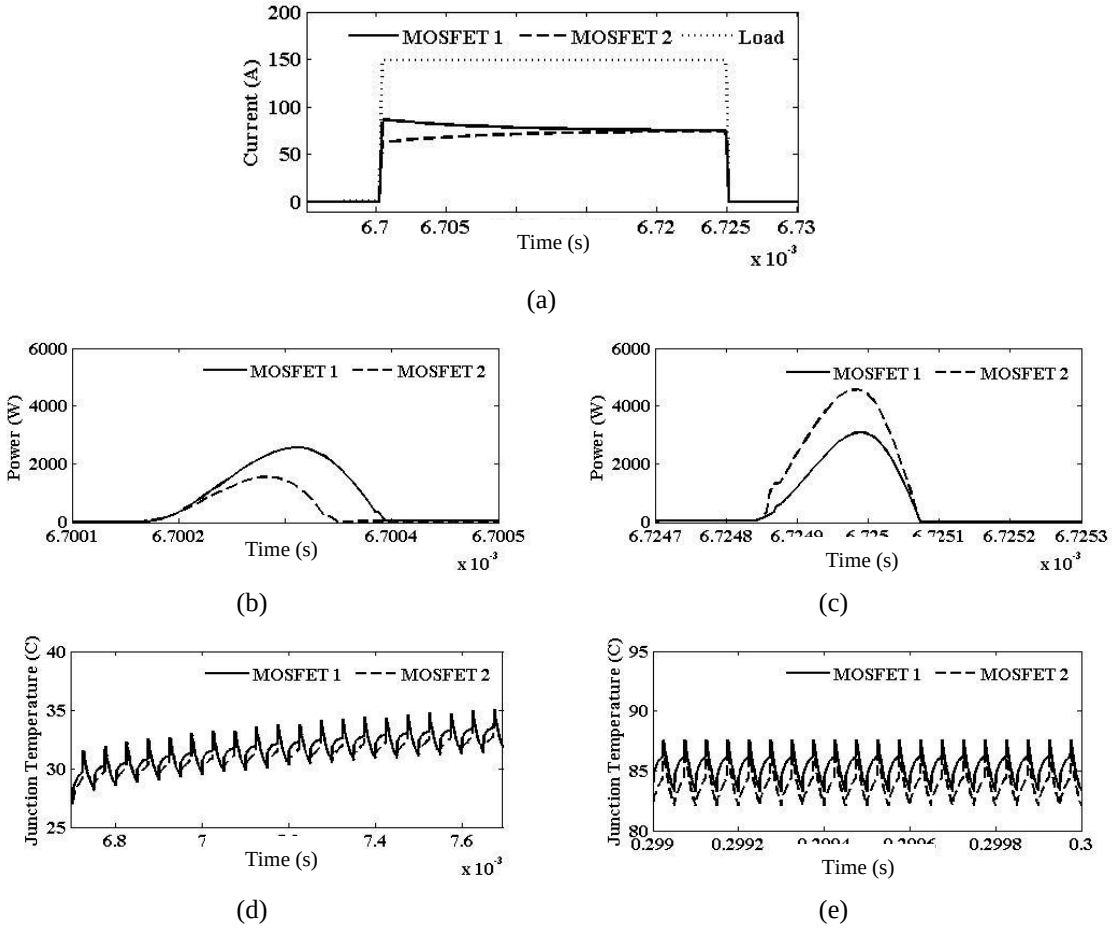


Figure 5.13: (a) First cycle device and load currents, (b) turn-on loss, (c) turn-off loss, (d) junction temperature during the first few cycles, and (e) at steady state operation, for common source and drain inductance of 10 and 100 nH respectively

5.4.2 Modelling n-parallel connected devices

The model can be extended to n-devices in parallel as follows:

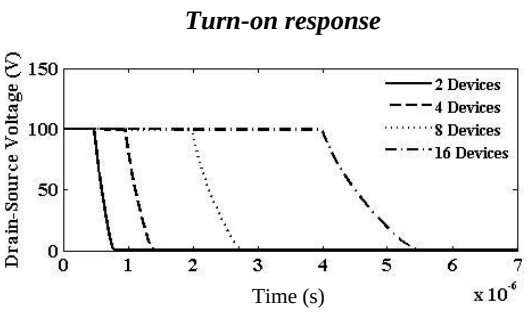
$$V_{gsn} = V_g - i_{gn}R_{gn} - L_{sn}\frac{d\left(i_{gn}+i_{Dn}\right)}{dt} - \left(i_{gn}+i_{Dn}\right)R_{sn} \tag{5.27}$$

$$i_{gn} = C_{issn}\frac{dV_{gsn}}{dt} - C_{rssn}\frac{dV_{dsn}}{dt} \tag{5.28}$$

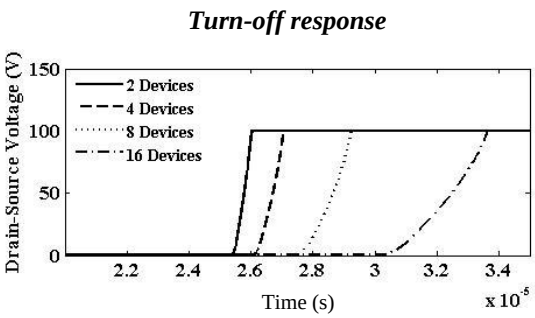
$$V_{dsn} = V_{dc} - \sum_{i=1}^{n} i_{Di}R_L - i_{Dn}R_{dn} - L_{dn}\frac{di_{Dn}}{dt} - L_{sn}\frac{d\left(i_{gn}+i_{Dn}\right)}{dt} - \left(i_{gn}+i_{Dn}\right)R_{sn} \tag{5.29}$$

$$i_{Dn} = i_{dn} + C_{ossn}\frac{dV_{dsn}}{dt} - C_{rssn}\frac{dV_{gsn}}{dt} \tag{5.30}$$

Adding more devices in parallel is suitable for reducing the total conduction loss. While accounting for the increased circuit time constant due to the added junction capacitances of paralleled devices, switching delays are extended. For the ideal case where all devices are matched, and devices are arranged in a symmetrical layout for obtaining equal drain and common source inductances, using the same gate circuit configuration provided it can supply the required current. Increase in the terminal drain-source voltage turn-on and turn-off switching times is shown in Figures 5.14a and 5.14b respectively, for 2, 4, 8, and 16 devices in parallel. The same is observed for the load current as shown in Figures 5.14c and 5.14d, which contributes to the increase in the total switching loss as shown in Figures 5.14e and 5.14f. However, this can be solved by reducing the gate drive circuit output resistance.



(a)



(b)

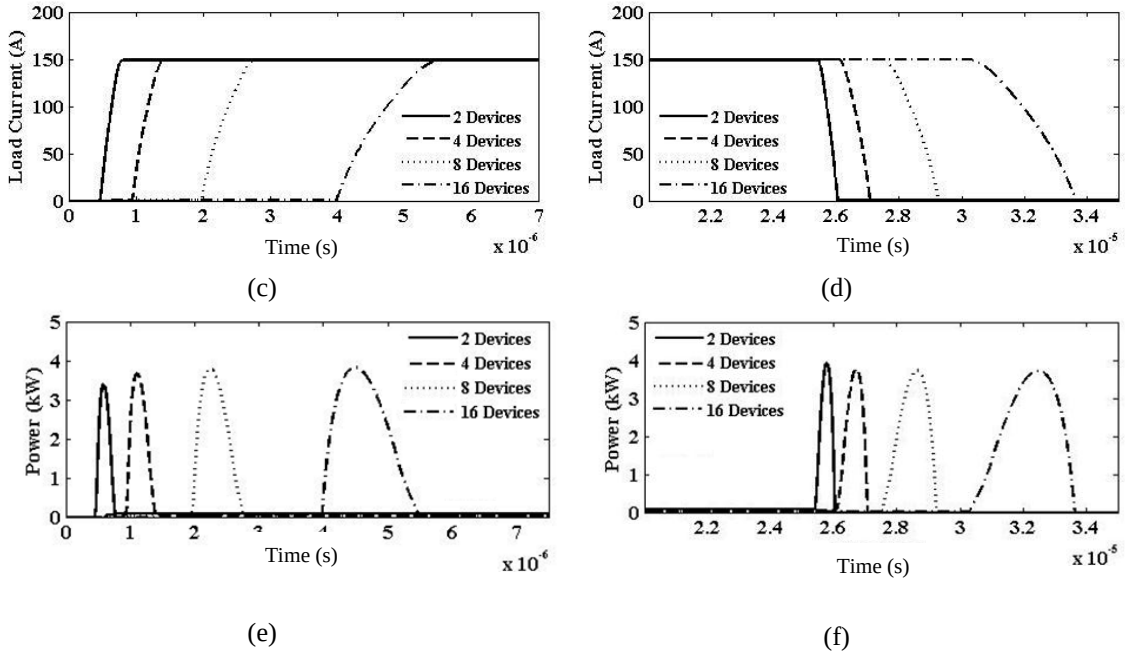


Figure 5.14: The effect of increase in number of paralleled devices on the switching waveforms, and the total power losses: (a), (b) Terminal drain-source voltage during turn-on and turn-off, (c) and (d) load current during turn-on and turn-off, (e) and (f) total turn-on and turn-off power loss

Paralleling may be used for reducing the conduction power loss at the same current rating in a specific application. In this case the current sharing imbalance due to any circuit parameter mismatch is below the current rating of the individual device. Hence, transient imbalance does not cause any thermal or electrical stresses on the device. However, in case of paralleling for higher current handling, the mismatched device may be subjected to severe electrical and thermal stresses. Considering the case of 16 parallel connected devices, where one device has a drain inductance of 10 nH and the other devices have 20 nH drain inductances. The mismatched device will turn-on faster than the other devices, and will carry a much higher transient current, as shown in Figure 5.15.

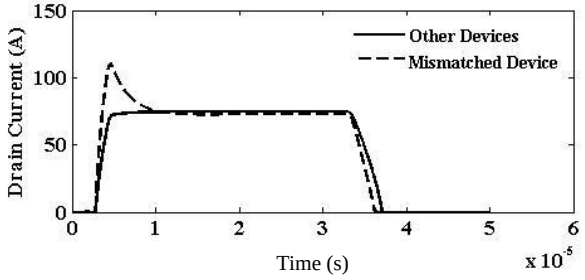


Figure 5.15: Conduction current for 16 parallel connected devices, with one device having a drain inductance of 10 nH, and the other 15 devices having a drain inductance of 20 nH

5.5 Synchronous rectifier module design (1000 A, 12 V)

A survey was carried out in order to select an appropriate device for the required synchronous rectifier ratings. The device IRF1324S-7PPbF is chosen, with a maximum rated current and voltage of 429 A and 24 V respectively, as shown in Appendix B. However, the device package limitation current is 160 A. 10 devices are connected in parallel per rectifier branch. Using the typical on-resistance stated in the datasheet (1 mΩ), the total rectifier power dissipation is:

$$P = 10 \times I^2 R_{on} = 10 \times (100)^2 \times 1 \times 10^{-3} = 100 \text{ W}$$

The selected device is only available in an SMD package. Bus bars must be used due to the high total current, which cannot be conducted by printed circuit board tracks. To avoid damaging the devices due to overheating in case of soldering directly on the bus bars, the devices are soldered first on a thin copper sheet. The sheet is then assembled onto bus bars using multiple screws, to assure good connectivity between the bus bars and the copper sheet. For connecting the devices in centre tapped rectifier configuration, the drain of all devices are connected on a common bus bar which provides the output terminal, while the source terminal for each of the two rectifier branches is connected to two different bus bars, then connected to the transformer secondary terminals. The common drain bus bar, to which the back plate of the devices is connected, is to be connected to a heat sink to dissipate the produced heat energy. A graphite based thermal compound (R_{th} = 0.01 ^{o}C/W) is used, to assure good thermal and electrical conductivity between the copper sheet and the cooled bus bar (see Appendix for photographs of the arrangement).

Considering Figure 5.16 for selecting the appropriate heat sink, the required thermal resistance can be calculated as follows:

$$P_{D1} + P_{D2} = \frac{T_j - T_a}{R_{sa} + R_a + R_b + R_c + (R_{jc1} \,||\, R_{jc2})}$$

$$\therefore R_{sa} = \frac{T_j - T_a}{P_{D(total)}} - (R_a + R_b + R_c + (R_{jc1} \,||\, R_{jc2}))$$

where P_{D1} and P_{D2} are the average power dissipation in the positive and negative rectifier half cycles, T_{j1} and T_{j2} are the junction temperatures, R_{jc1} and R_{jc2} are the respective junction to case thermal resistances, R_{sa} is the heat sink thermal resistance, R_a is the bus bar thermal resistance, R_b is the graphite compound thermal resistance, and R_c is the copper sheet thermal resistance.

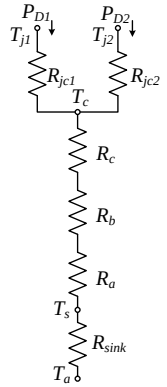


Figure 5.16: Equivalent thermal resistances of the arrangement

For an operating junction temperature of $T_j \leq 150^{\circ}\text{C}$, the required thermal resistance is:

$$R_{sa} \leq \frac{150-25}{100} - (0.04 + 0.01 + 0.55 + 0.025)$$

$$R_{sa} \leq 0.625\,^{\circ}\text{C/W}$$

A heat sink with a thermal resistance of $0.175\,^{\circ}\text{C/W}$ is selected, which results in a junction temperature of:

$$T_j = P_{D(total)} \times \left(R_{sa} + R_a + R_b + R_c + \left(R_{jc1} \,||\, R_{jc2}\right)\right) + T_a$$

$$= 105\,^{\circ}\text{C}$$

which is lower than the 175°C maximum junction temperature specified in the datasheet. The Matlab Simulink model developed previously is used to verify the operating average junction temperature. The drain-source resistance steady state value is 1.175 mΩ, as shown in Figure 5.17a. Each device per rectifier branch generates a switching power loss of 2.46 W, and a conduction power loss of 11.75 W per half cycle, as shown in Figure 5.17b. The steady-state junction temperature settles at 138.75 °C as shown in Figure 5.17c. Simulation results give more precise temperature values, due to the fact that the increase in device resistance due to the increase in junction temperature is considered. This contributes to the actual increased junction temperature than that obtained when considering a constant on-resistance value.

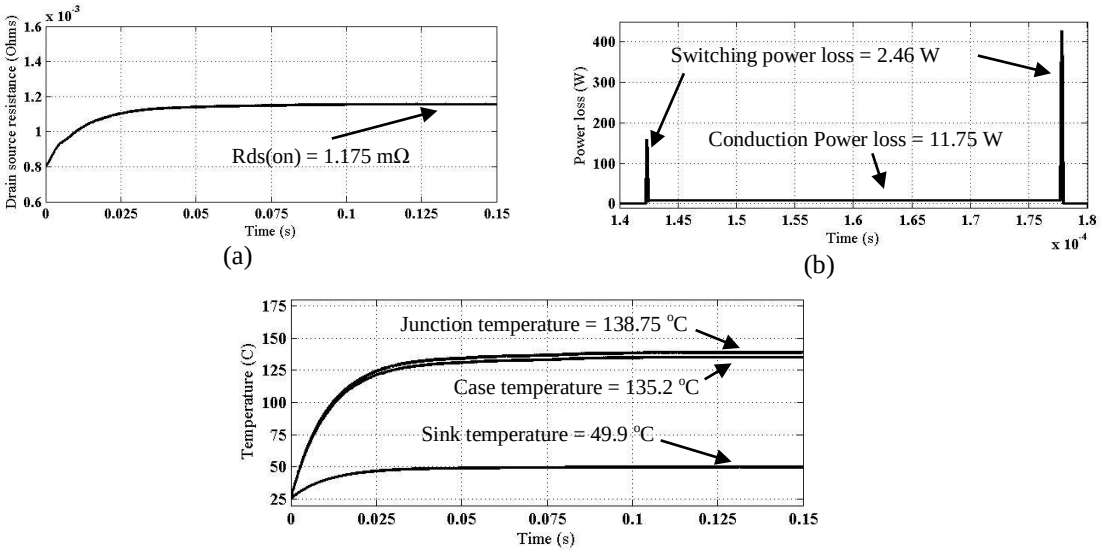


Figure 5.17: Electrothermal simulation results for the designed synchronous rectifier, (a) on-resistance, (b) power loss in each device, and (c) junction, case, and sink temperatures

5.6 Summary and discussion

The main principle of synchronous rectification has been discussed within this chapter. The MOSFET device is used as the switching element instead of conventional diode rectification. The device is switched on in synchronism with the supply. Two control toplogies were presented (self-driven and control-driven topologies), to successfully provide synchronisation and avoid body diode conduction. Parallel connected devices are used for the realisation of high power synchronous rectification. Inspite of the ease of paralleling due to the resistive nature of MOSFETs, balanced current sharing must be guaranteed to avoid individual device thermal stressing. An Electrothermal model was developed to study the effects of current imbalance, due to drain and common source inductance mismatch, in which device parameter mismatches are generated. Finally, a high current synchronous rectifier was designed (1000 A, and 12 V), and an electrothermal model was used to obtain and verify steady state operation aspects.

References

[5.1] B. Yang, J. Zhang, *"Effect and utilization of common source inductance in synchronous rectification"*, Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, APEC 2005, Volume 3, pp. 1407-1411, 2005.

[5.2] D.A. Grant, J. Gowar, *"Power MOSFETs Theory and Applications"*, John Wiley and Sons, ISBN: 9780471828679, 1989.

[5.3] J. Blanc, *"Practical application of MOSFET synchronous rectifiers"*, 13th International Telecommunications Energy Conference, INTELEC '91, pp. 495-501, 1991.

[5.4] O. Djekic, M. Brkovic, *"Synchronous rectifiers vs. Schottky diodes in a buck topology for low voltage applications"*, 28th Annual IEEE Power Electronics Specialists Conference, PESC '97, Volume 2, pp. 1374-1380, 1997.

[5.5] N. Yamashita, N. Murakami, T. Yachi, "Conduction power loss in MOSFET synchronous rectifier with parallel-connected Schottky barrier diode", IEEE Transactions on Power Electronics, Volume 13, pp. 667-673, 1998.

[5.6] M.M. Jovanovic, M.T. Zhang, F.C. Lee, "Evaluation of synchronous-rectification efficiency improvement limits in forward converters", IEEE Transactions on Industrial Electronics, Volume 42, pp. 387-395, 1995.

[5.7] M.I. Mihaiu, *"Toward the "ideal diode" using power MOSFET in full wave synchronous rectifiers for low voltage power supplies"*, International Symposium on Power Electronics, Electrical Drives, Automation and Motion, SPEEDAM 2008, pp. 1384 -1387, 2008.

[5.8] P. Alou, J.A. Oliver, O. Garcia, R. Prieto, J.A. Cobos, *"Comparison of current doubler rectifier and center tapped rectifier for low voltage applications"*, Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, APEC '06 , pp. 744-750, 2006.

[5.9] M. Xu, J. Zhou, F.C. Lee, "A current-tripler dc/dc converter", IEEE Transactions on Power Electronics, Volume 19, pp. 693-700, 2004.

[5.10] T. Lopez, R. Elferich, *"Static paralleling of power MOSFETs in thermal equilibrium"*, Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, APEC '06, pp. 841-847, 2006.

[5.11] T. Lopez, R. Elferich, *"Current Sharing of Paralleled Power MOSFETs at PWM Operation"*, 37th IEEE Power Electronics Specialists Conference, PESC '06, pp. 1-7, 2006.

[5.12] Y. Xiao, H. Shah, T.P. Chow, R.J. Gutmann, *"Analytical Modelling and Experimental Evaluation of Interconnect Parasitic Inductance on MOSFET Switching Characteristics"*, Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, APEC '04, pp. 516-521, 2004.

[5.13] J.B. Forsythe, *"Paralleling of Power MOSFETs for Higher Power Output"*, International Rectifier Application Note.

[5.14] H. Wang, F. Wang, *"MOSFETs Paralleling Operation for High Power Density Converters"*, 41st IAS Annual Meeting of the IEEE Industry Applications Conference, pp. 2284-2289, 2006.

[5.15] B. Abdi, A.H. Ranjbar, K. Malekian, J. Milimonfared, G.B. Gharehpetian, *"Problems Associated With Parallel Performance of High Current Switches and their Remedy"*, International Symposium on Power Electronics, Electrical Drives, Automation and Motion, SPEEDAM, pp. 1379 - 1383, 2008.

[5.16] F. Chimento, A. Raciti, A. Cannone, S. Musumeci, A. Gaito, *"Parallel Connection of Super-Junction MOSFETs in a PFC Application"*, IEEE Energy Conversion Congress and Exposition, ECCE '09, pp. 3776-3783, 2009.

[5.17] J. Bielefeld, G. Pelz, H.B. Abel, G. Zimmer, "Dynamic SPICE-simulation of the electrothermal behavior of SOI MOSFET's", IEEE Transactions on Electron Devices, Volume 42, pp. 1968-1974, 1995.

[5.18] Ž. Jakopović, V. Šunde, Z. Benčić, "Electro-Thermal Modelling and Simulation of a Power-MOSFET", AUTOMATIKA: Journal for Control, Measurement, Electronics, Computing and Communications, Volume 42, pp. 71-77, 2001.

[5.19] C. Leonardi, A. Raciti, F. Frisina, R. Letor, S. Musumeci, *"A new power MOSFET model including the variation of parameters with the temperature"*, Proceedings of the Second IEEE International Caracas Conference on Devices, Circuits and Systems, pp. 261-266, 1998.

[5.20] G. Chindris, O. Pop, G. Alin, F. Hurgoi, *"New Pspice Model for Power MOSFET Devices"*, 24th International Spring Seminar on Electronics Technology: Concurrent Engineering in Electronic Packaging, pp. 158-162, 2001.

[5.21] H. Dia, J.B. Sauveplane, P. Tounsi, J.-M. Dorkel, *"Temperature-Dependant POWER MOSFET Model for Switching Application"*, 15th International Workshop on Thermal Investigations of ICs and Systems, THERMINIC'09, 2009.

[5.22] Z. Jakopovic, V. Sunde, Z. Bencic, *"Electrothermal Modeling and Simulation With Simplorer"*, IEEE International Conference on Industrial Technology, Volume 2, pp. 1141-1145, 2004.

[5.23] G.H. Sarma, G. Nitin, Ramanan, Manivannan, K. Mehta, A. Bhattacharjee, *"Reliability Studies on High Current Power Modules With Parallel MOSFETs"*, IEEE European Microelectronics and Packaging Conference, EMPC '09, pp. 1-7, 2009.

[5.24] J. Chen, S. Downer, A. Murray, D. Divins, *"Analysis of Avalanche Behaviour of Paralleled MOSFETs"*, SAE World Congress, 2004.

[5.25] C. Buttay, T.B. Salah, D. Bergogne, B. Allard, H. Morel, J.-P. Chante, "Avalanche Behaviour of Low-Voltage Power MOSFETs", IEEE Power Electronics Letters, Volume 2, pp. 104-107, 2004.

[5.26] T. Matsukawa, H. Chikaraishi, Y. Sato, R. Shimada, M. Ishida, *"Synchronous AC/DC Converter Using Advanced Unipolar Power Electronics Device"*, Twenty-First IEEE/NPS Symposium on Fusion Engineering, pp. 1-4, 2005.

[5.27] T. Matsukawa, M. Shioyama, J. Nomura, C. Neumeyer, S. Tsuji-Iio, R. Shimada, *"Synchronous rectifier using power-MOSFET for high current AC/DC converter system"*, 19th Symposium on Fusion Engineering, pp. 80-83, 2002.

[5.28] T. Qian, W. Song, B. Lehman, *"Self-Driven Synchronous Rectification Scheme for Wide Range Application of DC/DC Converters with Symmetrically Driven Transformers"*, 37th IEEE Power Electronics Specialists Conference, PESC '06, pp. 1-6, 2006.

[5.29] L. Aubard, G. Verneau, J.C. Crebier, C. Schaeffer, Y. Avenas, *"Power MOSFET switching waveforms: an empirical model based on a physical analysis of charge locations"*, IEEE 33rd Annual Power Electronics Specialists Conference, PESC '02, Volume 3, pp. 1305-1310, 2002.

[5.30] K. Gauen, *"The effects of MOSFET output capacitance in high frequency applications"*, Conference Record of the 1989 IEEE Industry Applications Society Annual Meeting, Volume 2, pp. 1227-1234, 1989.

[5.31] C.K. Ong, P.O. Lauritzen, I. Budihardjo, *"A mathematical model for power MOSFET capacitances"*, 22nd Annual IEEE Power Electronics Specialists Conference, PESC '91, pp. 423-429, 1991.

[5.32] H. Gaffur, S. Yoon, *"Test structures for extraction of MOSFET capacitances"*, Proceedings of the 1994 International Conference on Microelectronic Test Structures, ICMTS '94, pp. 12-14, 1994.

[5.33] P.E. Jonathan Dodge, *"Eliminating parasitic oscillation between parallel MOSFETs, Application note"*, www.microsemi.com, 2004.

[5.34] J.G. Kassakian, D. Lau, "An analysis and experimental verification of parasitic oscillations in parralleled power MOSFET's", IEEE Transactions on Electron Devices, pp. 959-963, 1984.

Chapter 6

System Modelling and Experimental Validation

Each part of the designed DC/DC converter presented in the previous chapters has been carefully chosen to provide the highest overall efficiency. A ZVS phase shift PWM inverter operating at 14 kHz, with paralleled MOSFET devices significantly reduces both conduction and switching losses. The low loss nanocrystalline cored transformer designed and utilised, results in a highly efficient magnetic design. Synchronous rectification is used rather than conventional diode rectification to significantly reduce the voltage drop across the rectifying devices, which severely affects the overall efficiency with low output voltage requirements.

This chapter presents the experimental results for the high-current low-voltage DC power supply, delivering a load current of 1 kA at an average output voltage of approximately 8 V. The block diagram in Figure 6.1 highlights the basic system components.

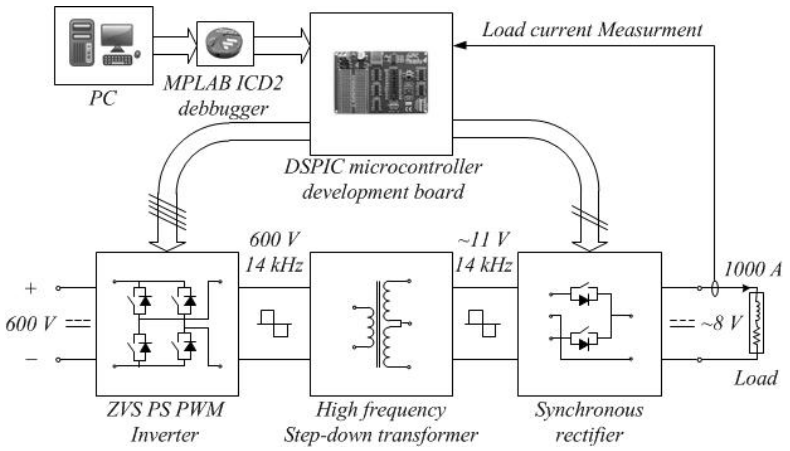


Figure 6.1: Block diagram showing the main system components

6.1 Load bank design

A high-current load bank is built for studying DC/DC converter operation and analysis. The bank consists of eleven 1 kW coil resistors, connected in parallel, giving a total power handling capability of approximately 11 kW. Each individual resistance value is 0.12 Ω, with a rated current of 91 A, as shown in the device datasheet in Appendix F. Resistance is adjusted using the movable contact terminals to achieve the load value

which gives a total load current of 1000 A at approximately 8 V, to simulate a similar case to the actual application requirements. Each resistor also possesses finite inductance, with the measured values presented in Table 6.1. The DC/DC converter is operated at continuous conduction mode through all duty cycle values due to the fact that the load time constant ($L/R \cong 0.375ms$) is much larger than the switching period ($1/f_s = 71.43\mu s$).

Table 6.1: Load bank measured resistance and inductance values

	1 Resistor	**Total Load Bank**
Measured resistance	85 mΩ	7.7 mΩ
Measured inductance	32 µH	2.9 µH

6.2 Open loop system operation

The system is first analysed in open loop operation. Matlab® Simulink simulations are also presented based on the system parameters obtained in the previous chapters, for comparison and validation of the design procedures. A schematic diagram for the open loop system is shown in Figure 6.2. Inverter and synchronous rectifier gate signals are generated from a DSP control board (DSPIC30F2020) with 6 output PWM channels, with pairs configured in complementary mode. Left leg and right leg delays are properly adjusted to achieve inverter ZVS operation. The gate signals for each rectifier side are synchronised with the leading inverter output voltage edges, for the positive and negative half cycles respectively.

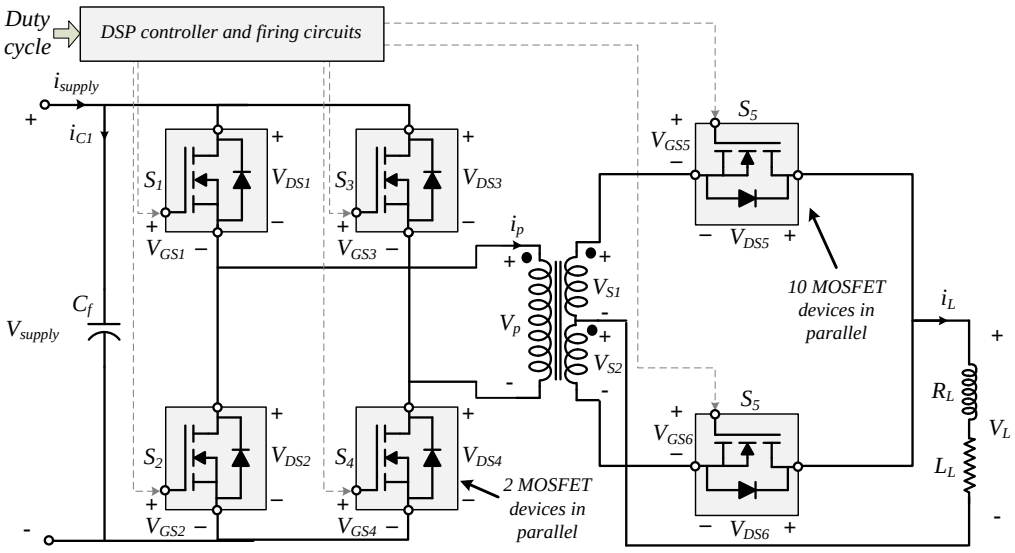


Figure 6.2: Open loop system schematic diagram

The DC/DC converter is utilised as a high current source for an inductive load; hence no output filter inductance is required. The addition of a load side smoothing capacitor would require a high peak capacitor current rating (1000 A), which can only be obtained by paralleling metallised polypropylene capacitors. These would significantly increase the converter volume. Consequently, no filter capacitors are used in order to minimise the overall converter footprint.

6.2.1 Simulation results

Simulations presented in the previous chapters are mainly focused on the independent design, analysis and operation of each system part. However, the ZVS inverter operation presented in Chapter 2 showed the operation for a resistive load through a load-end LC filter. Simulation results for an inductive RL load, where the DC/DC converter is utilised as a high current source, are presented in this section. Converter operation can be considered to be similar to the previous case, except that no output voltage smoothing is needed. Equal full-bridge ZVS left-leg and right-leg transition delays are adopted for simplifying the analysis.

Circuit simulations are carried out at 75% and 100% primary voltage duty cycle using Matlab Simulink. The full-bridge ZVS design procedures are presented earlier in Chapter 2, and will be verified experimentally in the next section. Input voltage and current to the converter are shown in Figures 6.3a and 6.3b, transformer primary voltage and current are shown in Figures 6.3c and 6.3d, and transformer secondary voltages and currents are shown in Figures 6.3e, 6.3f, 6.3g, and 6.3h, for both cases respectively. The leakage inductance is considered as an added series inductance, which may be placed as one inductance in series with the primary winding, or as two inductances each placed in series with each secondary winding. Two 64 nH inductances are added in series with the secondary windings (equal to that obtained experimentally in the next section), while no primary leakage is considered in the simulation model. The synchronous rectifier bus bar circuit inductance is also considered in the simulation. A series inductance with the value of a 20 nH, as part of the total 64 nH winding leakage. The total leakage inductance referred to the primary side is 93.6 µH, which is the same as obtained in Chapter 4. The effective secondary voltage duty cycle in this case is, therefore approximately 81%. A significantly large total leakage inductance is obtained due to the fact that each secondary winding leakage inductance, added to the secondary circuit bus

bar inductance, is multiplied by the squared of the turns ratio. The presence of a small inductance of 64 nH in series with each secondary winding has a significant effect at high currents. The effect of a high leakage inductance can be observed by the presence of a finite current slope during current rise and decay on each secondary winding, which is reflected to the primary winding current during primary current reversal.

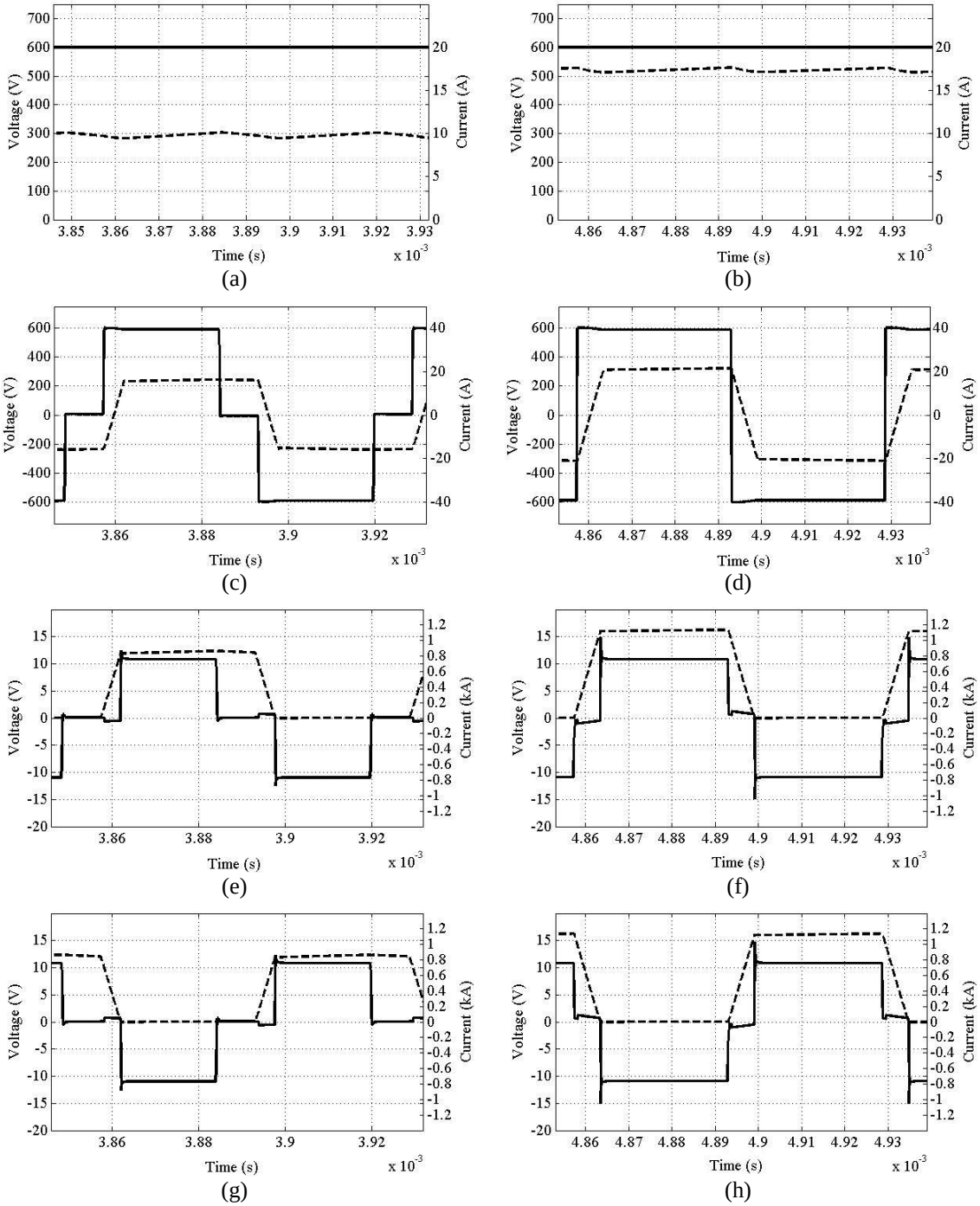


Figure 6.3: Simulation results for DC/DC converter operation showing the supply voltage and current in (a) and (b), transformer primary voltage and current in (c) and (d), secondary winding s1 voltage and current in (e) and (f), and secondary winding s2 voltage and current in (g) and (h), for 75% and 100% primary voltage duty cycles respectively.

The synchronous rectifier gate signals are synchronised with the positive and negative leading edge of the primary voltage waveform, for the positive and negative half cycle rectifier sides respectively. The secondary winding voltage is delayed by a time interval equal to the time required for the primary current to reverse direction, during which the secondary current circulates through both rectifier sides; hence forcing the device internal body diode to conduct, thereby providing ZVS operation for both rectifier side switches. Synchronous rectifier gate signals and drain-source voltages, for 75% and 100% primary duty cycle, and for both the positive and negative half cycles, are shown in Figures 6.4a, 6.4b, 6.4c, and 6.4d respectively.

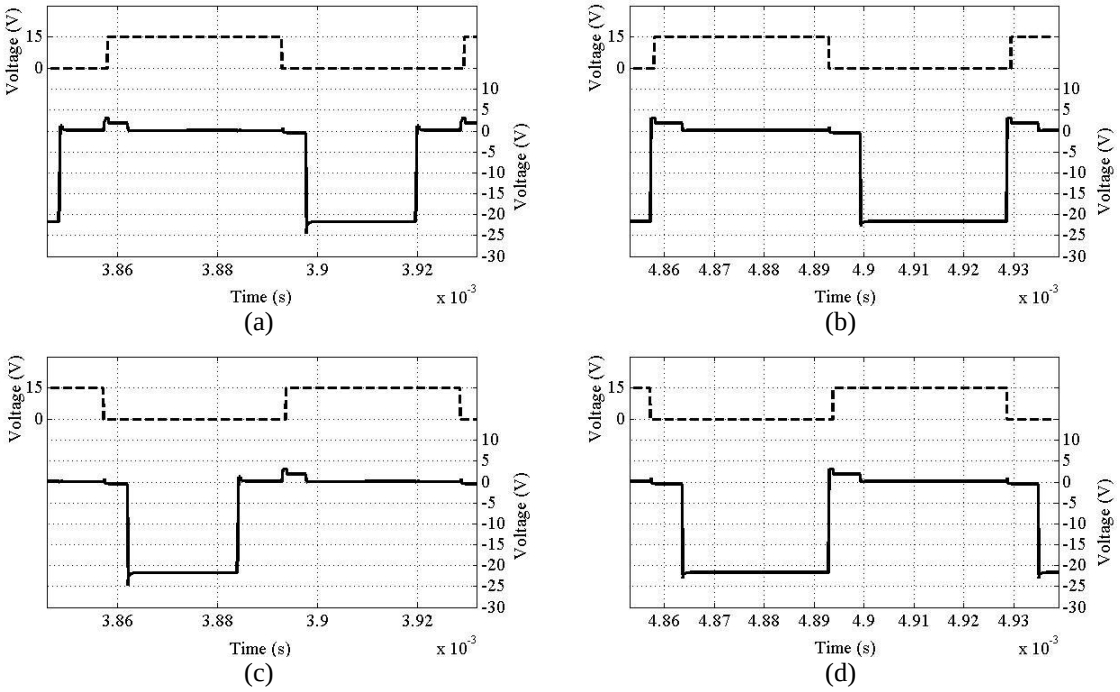


Figure 6.4: DC/DC converter operation showing the positive half cycle synchronous rectifier gate signal and drain source voltage in (a) and (b), and the negative half cycle synchronous rectifier gate signal and drain source voltage in (c) and (d), at 75% and 100% primary voltage duty cycle respectively

The DC/DC converter output voltage is equivalent to a train of voltage pulses, at a period much smaller than the output RL load time constant, hence resulting in a continuous output current with a ripple current of approximately 20 A at full primary duty cycle. Load voltage and current at 75% and 100% primary voltage duty cycle are shown in Figures 6.5a, 6.5b, 6.5c and 6.5d respectively.

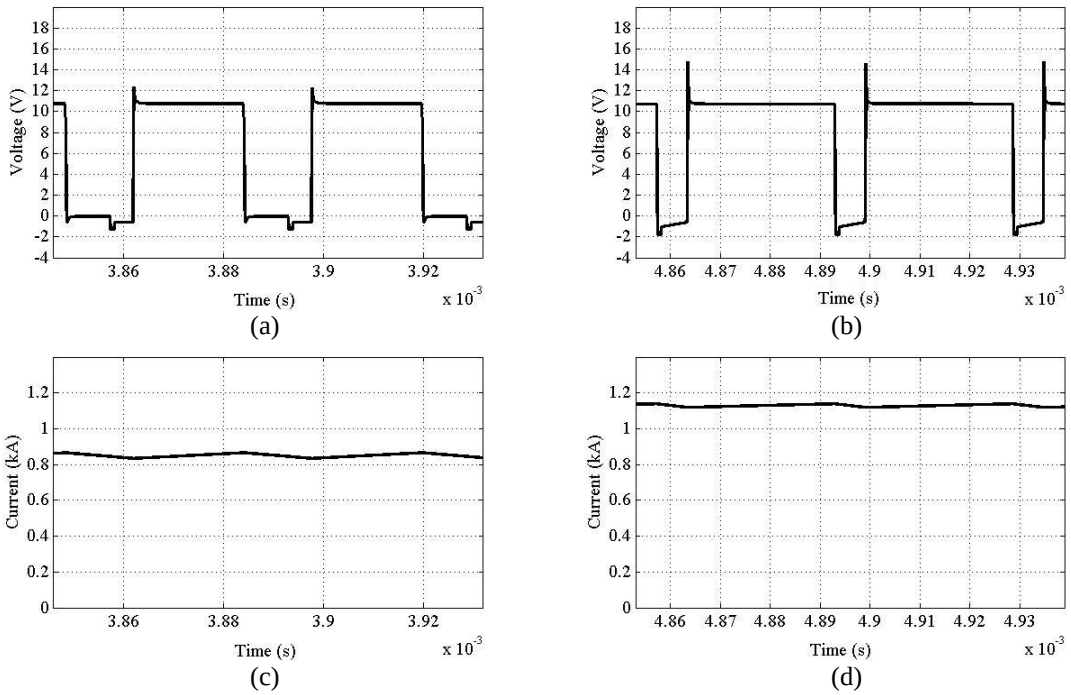


Figure 6.5: DC/DC converter operation showing load voltage at 75% and 100%primary voltage duty cycle in (a) and (b), and load current at 75% and 100% primary voltage duty cycle in (c) and (d)

Power loss calculations based on the analysis presented in Chapter 2, considering inverter and synchronous rectifier steady state junction temperatures, are performed using a Matlab m-file given in Appendix F1. The expected loss distribution through each system part, and the expected overall converter efficiency, are shown in Table 6.2.

Table 6.2: Loss distribution and Efficiency obtained by calculations and Matlab simulations

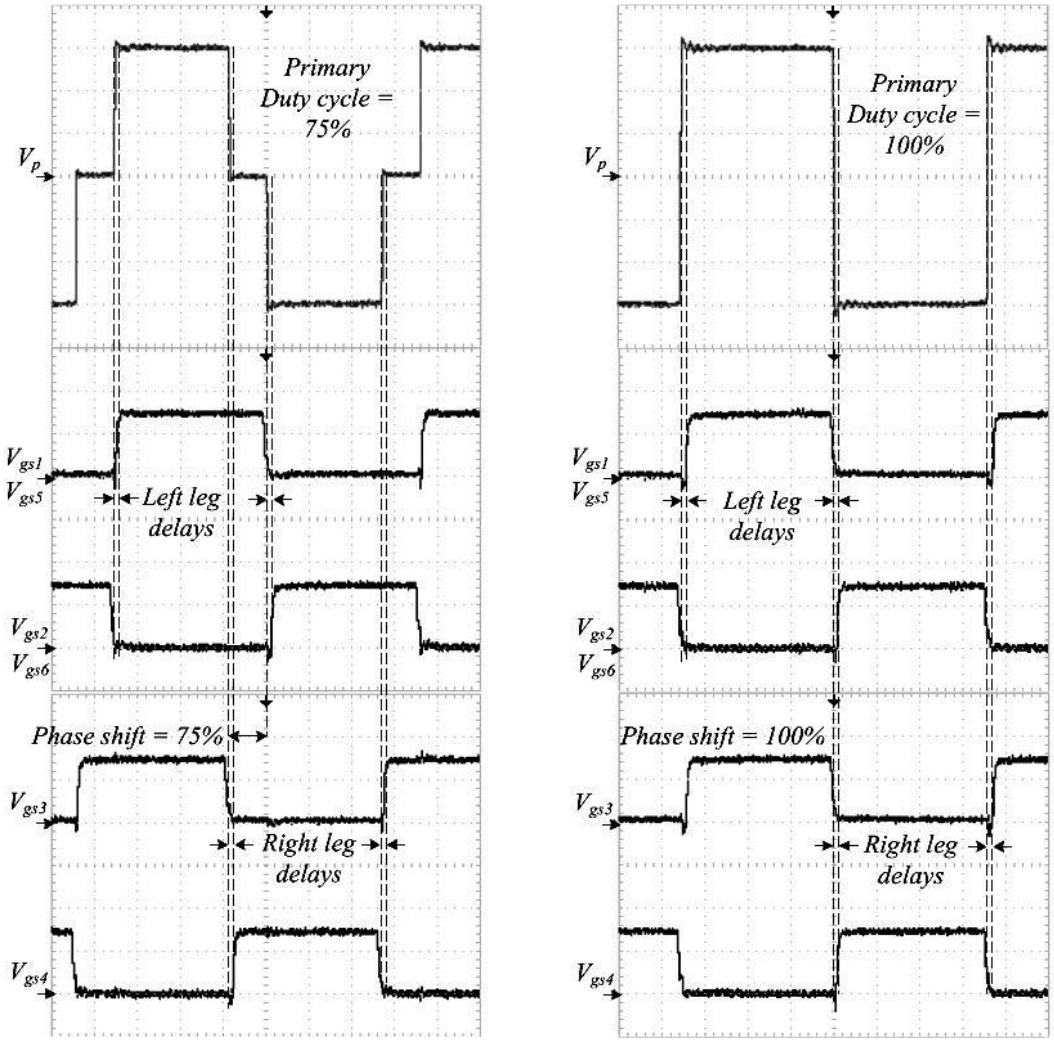
	Calculations	**Matlab simulation**
Inverter power loss	186.8 W [(a)]	186.2 W
Transformer power loss	74.1 W [(b)]	14 W
Synchronous rectifier power loss	257 W [(a)]	257 W
Load power	10.23 kW [(c)]	9.93 kW
Efficiency	95.2%	95.6%

[(a)] Power loss is calculated based on the expected device junction temperature
[(b)] FEA transformer power loss obtained in Chapter 4
[(c)] Load power based on the effective average output voltage

A minimum primary current of 1.7 A is required for obtaining zero voltage switching, based on the analysis presented in Chapter 2. Consequently, the converter operates under ZVS condition in the range, approximately, 10% to 100% load. The significantly wide ZVS range versus load is mainly due to the high transformer leakage inductance.

6.2.2 Experimental validation

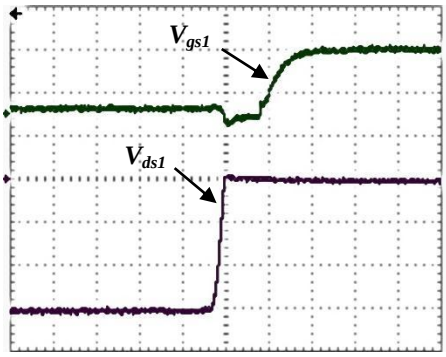
Experimental validation for the DC/DC converter, in open loop control, is performed in two steps; first with 5 load resistors connected (approximately half load operation), and the second with 11 load bank resistors (full load operation). At each step, the converter operation is presented at 75% and 100% primary voltage duty cycle. The supply voltage is manually increased from 0V to 600V in each case, as a safety consideration. All waveforms to be presented are steady state waveforms, for which the converter input voltage is 600V, the switching devices, and various circuit components are at constant and steady state temperatures. The inverter output voltage and gate signals, showing the ZVS left-leg and right-leg transition delays, in which the device body diode is forced to conduct, at 75% and 100% phase-shift, are shown in Figures 6.6a and 6.6b respectively.



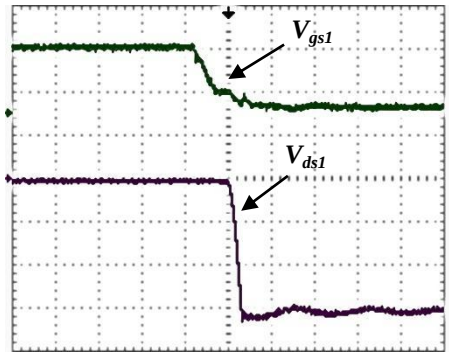
(a) (b)

Figure 6.6: Gate signal synchronisation for ZVS inverter operation and synchronous rectifier at (a) 50% and (b) 100% primary duty cycles

The gate-source and drain-source voltage waveforms are observed for each MOSFET, to verify zero voltage switching operation. The drain-source voltage for each switch falls to the ($I_pR_{ds(on)}$) value before the corresponding gate signal is applied. The gate signal is then applied after assuring that the body diode is in complete conduction; that is after the introduced left-leg or right-leg delays as explained in Chapter 2. Turn-on and turn-off waveforms for *S1*, *S2*, *S3*, and *S4* are shown in Figures 6.7a, 6.7b, 6.7c, and 6.7d respectively.

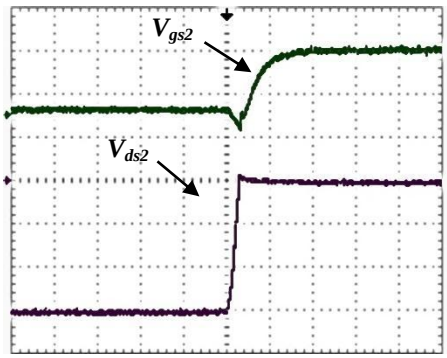


(i) V_{gs1}: 10 V/div, V_{ds1}: 200 V/div, t: 1 µs/div

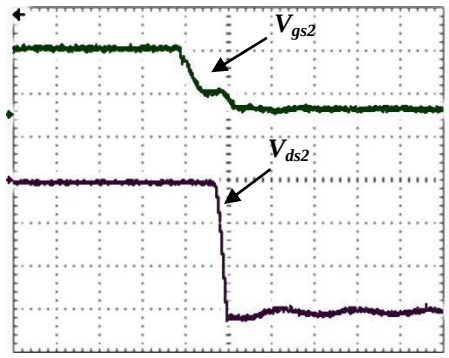


(ii) V_{gs1}: 10 V/div, V_{ds1}: 200 V/div, t: 1 µs/div

(a) S1 turn on and turn off waveforms in (i) and (ii) respectively

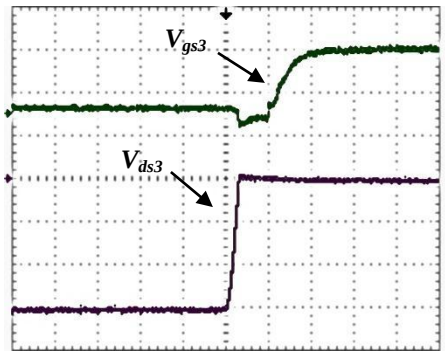


(i) V_{gs2}: 10 V/div, V_{ds2}: 200 V/div, t: 1 µs/div

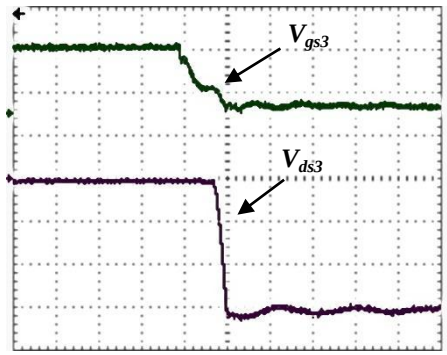


(ii) V_{gs2}: 10 V/div, V_{ds2}: 200 V/div, t: 1 µs/div

(b) S2 turn-on and turn-off waveforms in (i) and (ii) respectively

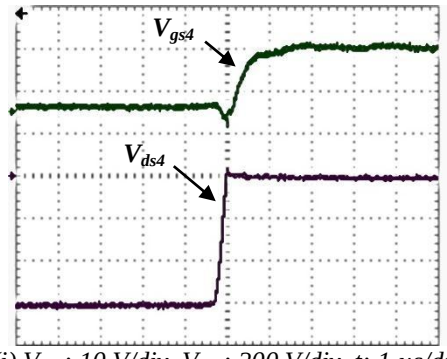


(i) V_{gs3}: 10 V/div, V_{ds3}: 200 V/div, t: 1 µs/div

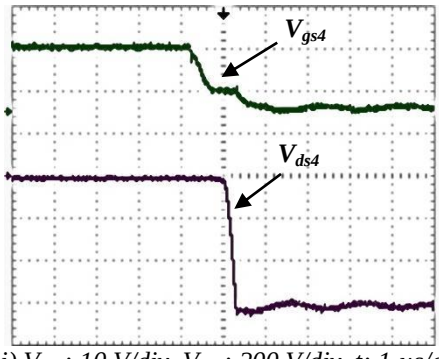


(ii) V_{gs3}: 10 V/div, V_{ds3}: 200 V/div, t: 1 µs/div

(c) S3 turn-on and turn-off waveforms in (i) and (ii) respectively



(i) V_{gs4}: 10 V/div, V_{ds4}: 200 V/div, t: 1 µs/div



(ii) V_{gs4}: 10 V/div, V_{ds4}: 200 V/div, t: 1 µs/div

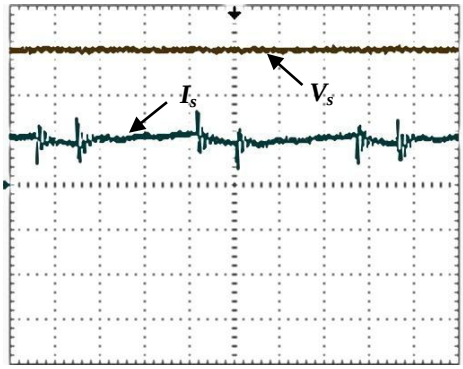
(d) S4 turn-on and turn-off waveforms in (i) and (ii) respectively

Figure 6.7: Turn on and turn off waveforms for inverter switches (a) S1, (b) S2, (c) S3, and (d) S4, showing the gate signal and the voltage across each MOSFET (V_{ds}) respectively, at the lowest operating load for achieving ZVS operation

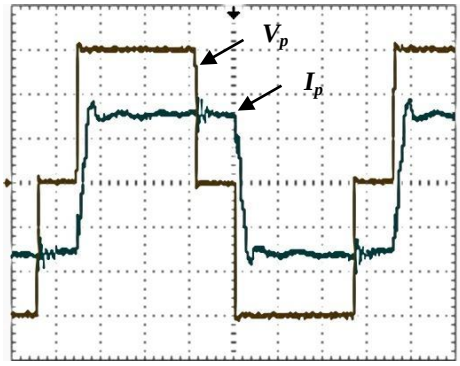
i. Half load operation (5 resistors connected in parallel)

The circuit is first tested at approximately half load, with 5 resistors connected in the load bank. The average load voltage and current at 100% primary duty cycle are approximately 9.63 V and 551 A, and approximately 6.96 V and 398 A at 75 % primary duty cycle respectively. Supply voltage and current, transformer primary voltage and current, secondary winding *S1* voltage, secondary winding *S2* voltage, the positive half cycle synchronous rectifier gate-source voltage and drain-source voltage, the negative half cycle synchronous rectifier gate-source voltage and drain source voltage, load voltage, and load current waveforms are shown in Figures 6.8 and 6.9 for 75% and 100% primary voltage duty cycles, respectively.

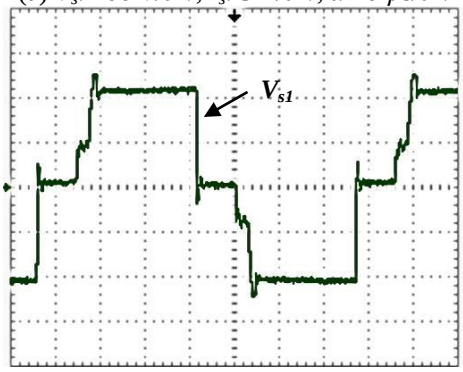
- ***75% primary duty cycle***



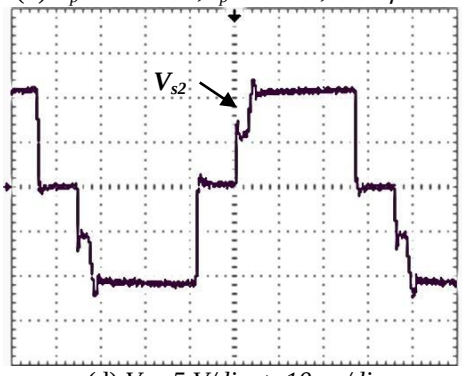
(a) V_s: *200 V/div,* I_s*: 5 A/div, t: 10 µs/div*



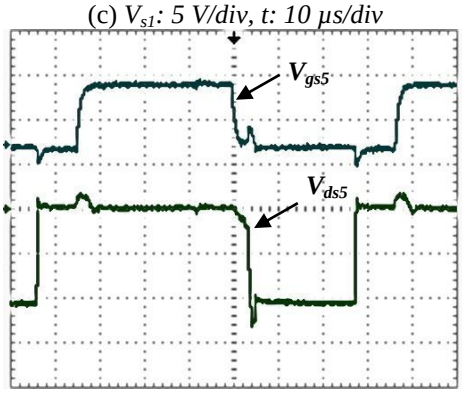
(b) V_p: *200 V/div,* I_p*: 5 A/div, t: 10 µs/div*



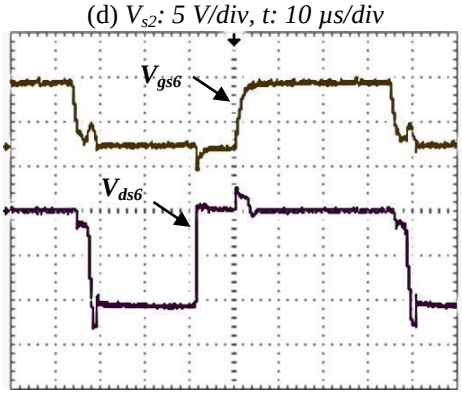
(c) V_{s1}*: 5 V/div, t: 10 µs/div*



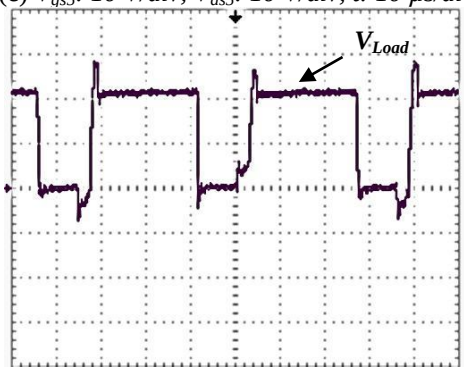
(d) V_{s2}*: 5 V/div, t: 10 µs/div*



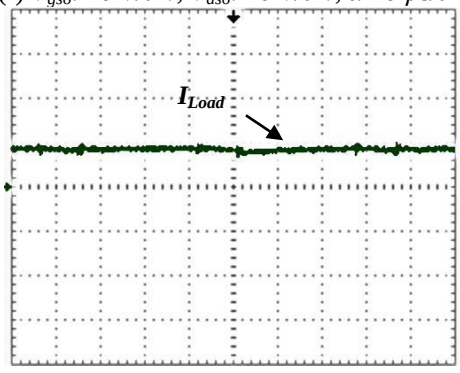
(e) V_{qs5}*: 10 V/div,* V_{ds5}*: 10 V/div, t: 10 µs/div*



(f) V_{gs6}*: 10 V/div,* V_{ds6}*: 10 V/div, t: 10 µs/div*



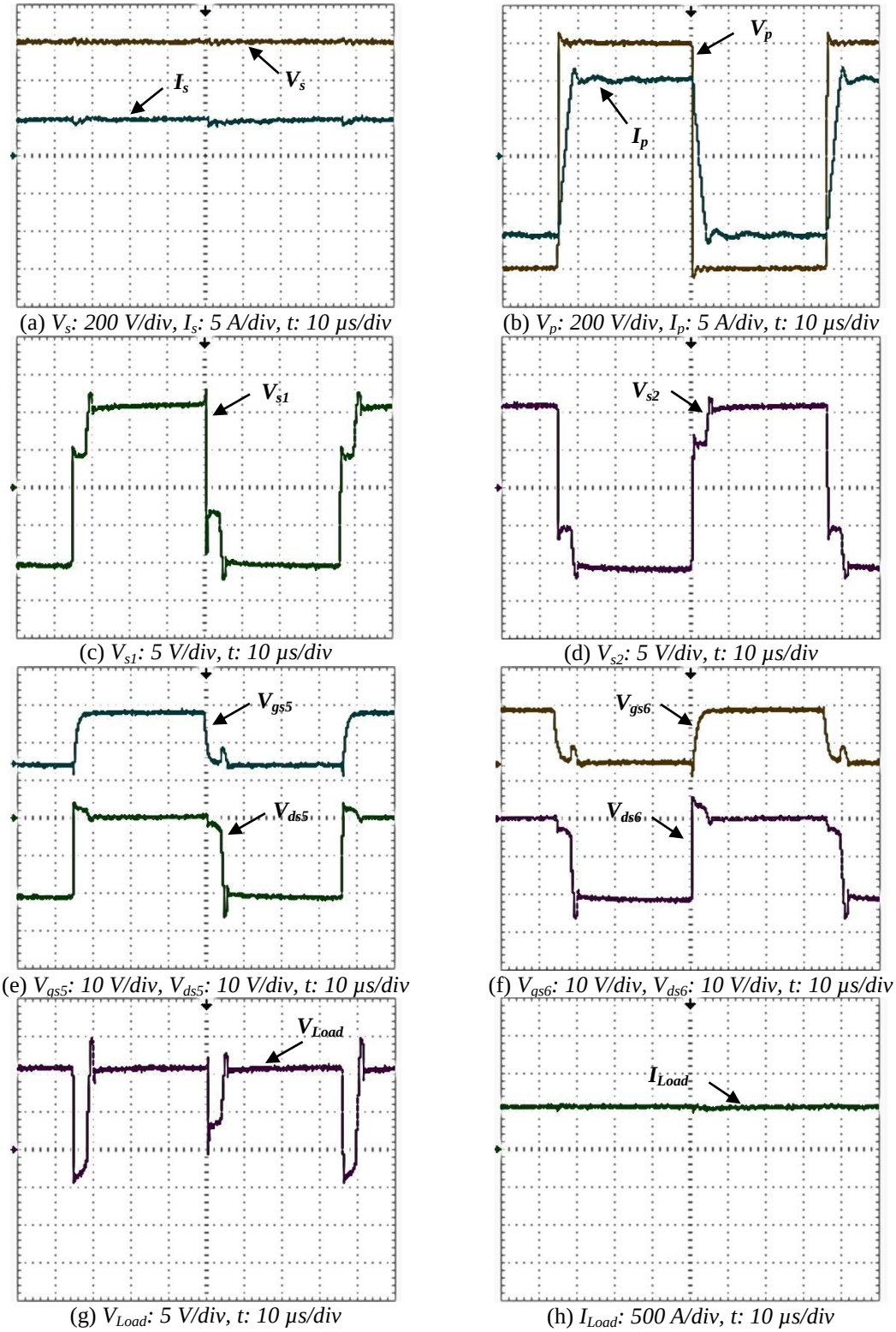
(g) V_{Load}*: 5 V/div, t: 10 µs/div*



(h) I_{Load}*: 500 A/div, t: 10 µs/div*

Figure 6.8: One cycle of operation, at 75% primary duty cycle, showing: (a) supply voltage V_s and current I_s, (b) transformer primary voltage V_p and current I_p, (c) secondary voltage V_{s1}, (d) secondary voltage V_{s2}, (e) synchronous rectifier positive half cycle gate source voltage V_{gs5} and drain source voltage V_{ds5}, (f) synchronous rectifier negative half cycle gate source voltage V_{gs6} and drain source voltage V_{ds6}, (g) load voltage V_{Load} and (h) load current I_{Load}

- ***100% primary duty cycle***



(a) V_s: *200 V/div,* I_s: *5 A/div, t: 10 µs/div*

(b) V_p: *200 V/div,* I_p: *5 A/div, t: 10 µs/div*

(c) V_{s1}: *5 V/div, t: 10 µs/div*

(d) V_{s2}: *5 V/div, t: 10 µs/div*

(e) V_{gs5}: *10 V/div,* V_{ds5}: *10 V/div, t: 10 µs/div*

(f) V_{gs6}: *10 V/div,* V_{ds6}: *10 V/div, t: 10 µs/div*

(g) V_{Load}: *5 V/div, t: 10 µs/div*

(h) I_{Load}: *500 A/div, t: 10 µs/div*

Figure 6.9: One cycle of operation, at 100% primary duty cycle, showing: (a) supply voltage V_s and current I_s, (b) transformer primary voltage V_p and current I_p, (c) secondary voltage V_{s1}, (d) secondary voltage V_{s2}, (e) synchronous rectifier positive half cycle gate source voltage V_{gs5} and drain source voltage V_{ds5}, (f) synchronous rectifier negative half cycle gate source voltage V_{gs6} and drain source voltage V_{ds6}, (g) load voltage V_{Load} and (h) load current I_{Load}

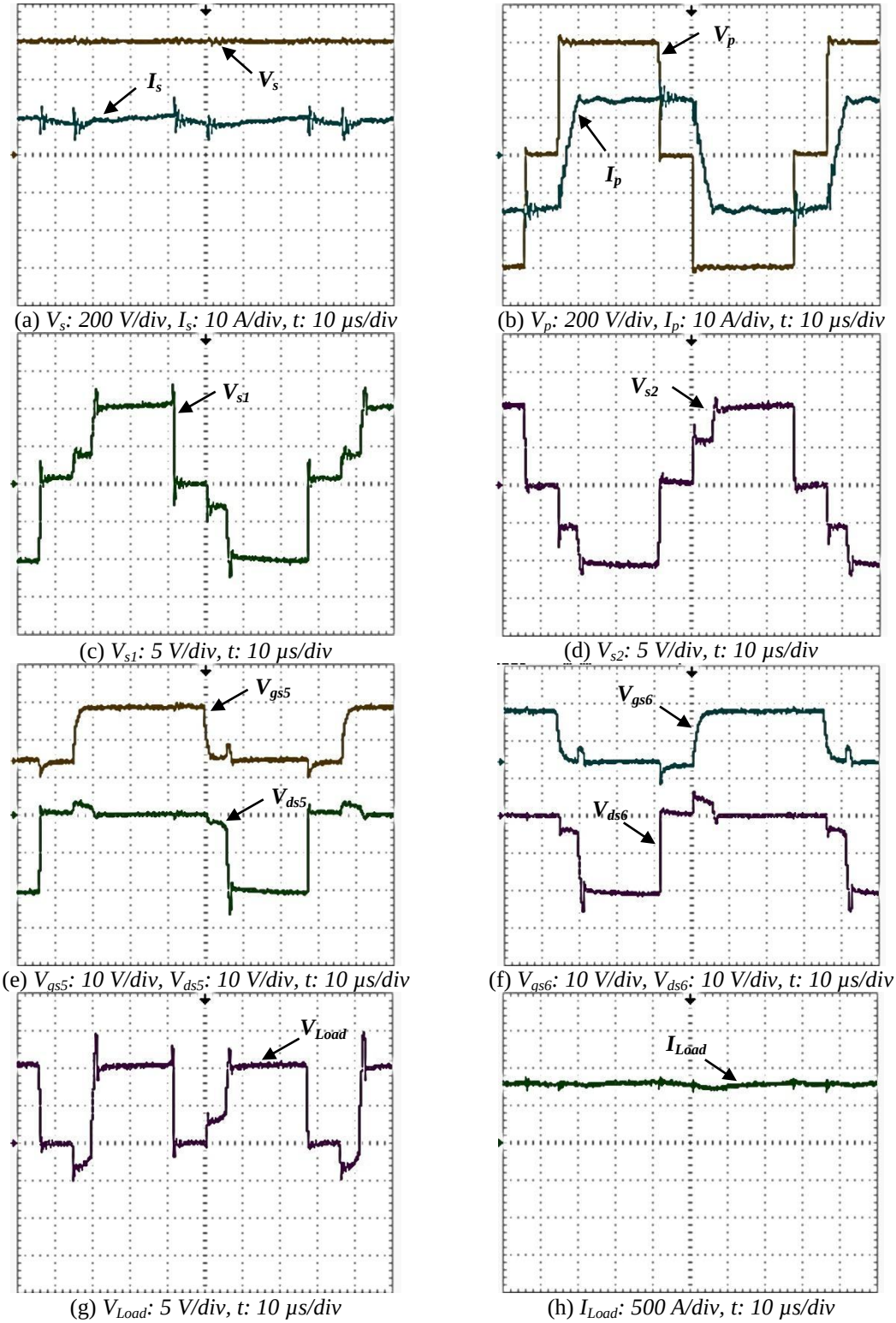
ii. Full load operation (11 resistors connected in parallel)

DC/DC converter operation is next tested at full load, with 11 resistors connected in the load bank, to compensate for the reduced average output voltage caused by the increased duty cycle loss at full loading conditions. The average load voltage and current at 100% primary duty cycle are approximately 8.33 V and 1036 A, and 5.86 V and 729 A at 75 % primary duty cycle respectively. Supply voltage and current, transformer primary voltage and current, secondary winding *S1* voltage, secondary winding *S2* voltage, the positive half cycle synchronous rectifier gate-source voltage and drain-source voltage, the negative half cycle synchronous rectifier gate-source voltage and drain source voltage, load voltage, and load current waveforms are shown in Figures 6.10 and 6.11 for 75% and 100% primary voltage duty cycles respectively.

The total leakage inductance referred to the primary side can be calculated from the transformer primary current. By substituting into $V = L\,di/dt = L\,\Delta i/\Delta t$, with Δi equal to the difference in current values during the current rise or fall interval Δt, a leakage inductance of approximately 134.2 µH is obtained, compared to a value of 93.6 µH obtained by FEA simulations. The obtained leakage inductance, referred to the primary side, is the sum of the transformer leakage inductance, the termination bus bar inductance, and the synchronous rectifier bus bar stray inductance (which was not incorporated during simulations).

The total leakage inductance, referred to the primary side, is approximately half the inductance of each secondary winding. This is only the case when the load current is circulating through both rectifier sides, during commutation. The resultant inductance is halved as the two windings are effectively paralleled during commutation.

- ***75% primary duty cycle***



(a) V_s: 200 V/div, I_s: 10 A/div, t: 10 µs/div

(b) V_p: 200 V/div, I_p: 10 A/div, t: 10 µs/div

(c) V_{s1}: 5 V/div, t: 10 µs/div

(d) V_{s2}: 5 V/div, t: 10 µs/div

(e) V_{qs5}: 10 V/div, V_{ds5}: 10 V/div, t: 10 µs/div

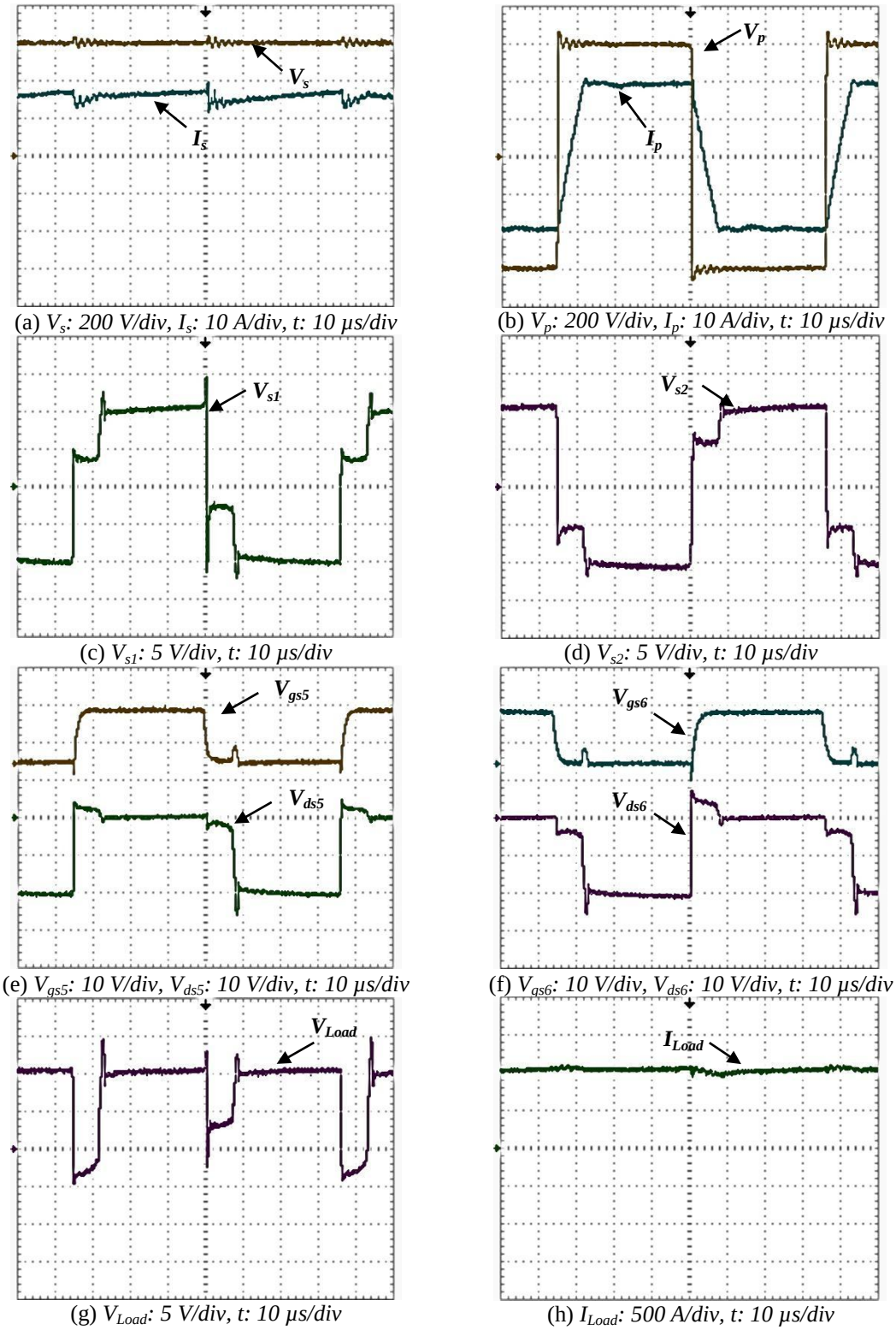
(f) V_{qs6}: 10 V/div, V_{ds6}: 10 V/div, t: 10 µs/div

(g) V_{Load}: 5 V/div, t: 10 µs/div

(h) I_{Load}: 500 A/div, t: 10 µs/div

Figure 6.10: One cycle of operation, at 75% primary duty cycle, showing: (a) supply voltage V_s and current I_s, (b) transformer primary voltage V_p and current I_p, (c) secondary voltage V_{s1}, (d) secondary voltage V_{s2}, (e) synchronous rectifier positive half cycle gate source voltage V_{gs5} and drain source voltage V_{ds5}, (f) synchronous rectifier negative half cycle gate source voltage V_{gs6} and drain source voltage V_{ds6}, (g) load voltage V_{Load} and (h) load current I_{Load}

- ***100% primary duty cycle***



(a) V_s: *200 V/div,* I_s: *10 A/div, t: 10 µs/div* (b) V_p: *200 V/div,* I_p: *10 A/div, t: 10 µs/div*

(c) V_{s1}: *5 V/div, t: 10 µs/div* (d) V_{s2}: *5 V/div, t: 10 µs/div*

(e) V_{gs5}: *10 V/div,* V_{ds5}: *10 V/div, t: 10 µs/div* (f) V_{gs6}: *10 V/div,* V_{ds6}: *10 V/div, t: 10 µs/div*

(g) V_{Load}: *5 V/div, t: 10 µs/div* (h) I_{Load}: *500 A/div, t: 10 µs/div*

Figure 6.11: One cycle of operation, at 100% primary duty cycle, showing: (a) supply voltage V_s and current I_s, (b) transformer primary voltage V_p and current I_p, (c) secondary voltage V_{s1}, (d) secondary voltage V_{s2}, (e) synchronous rectifier positive half cycle gate source voltage V_{gs5} and drain source voltage V_{ds5}, (f) synchronous rectifier negative half cycle gate source voltage V_{gs6} and drain source voltage V_{ds6}, (g) load voltage V_{Load} and (h) load current I_{Load}

It is observed that the converter output voltage is asymmetrical during the duty cycle loss intervals. This is caused by the difference in the transformer secondary windings leakage inductance. Matlab Simulink circuit simulations for two cases verifying the effect of different secondary winding leakage inductances are shown in Figure 6.12 and 6.13 respectively. The first case represents the ideal case with equal secondary windings leakage inductance, while the second case is the actual case where the first secondary winding possesses 15 nH more leakage inductance, and the other secondary winding has a 15 nH less leakage inductance. Hence, the total leakage inductance referred to the primary side, still adds to 93.6 µH, as with the first case.

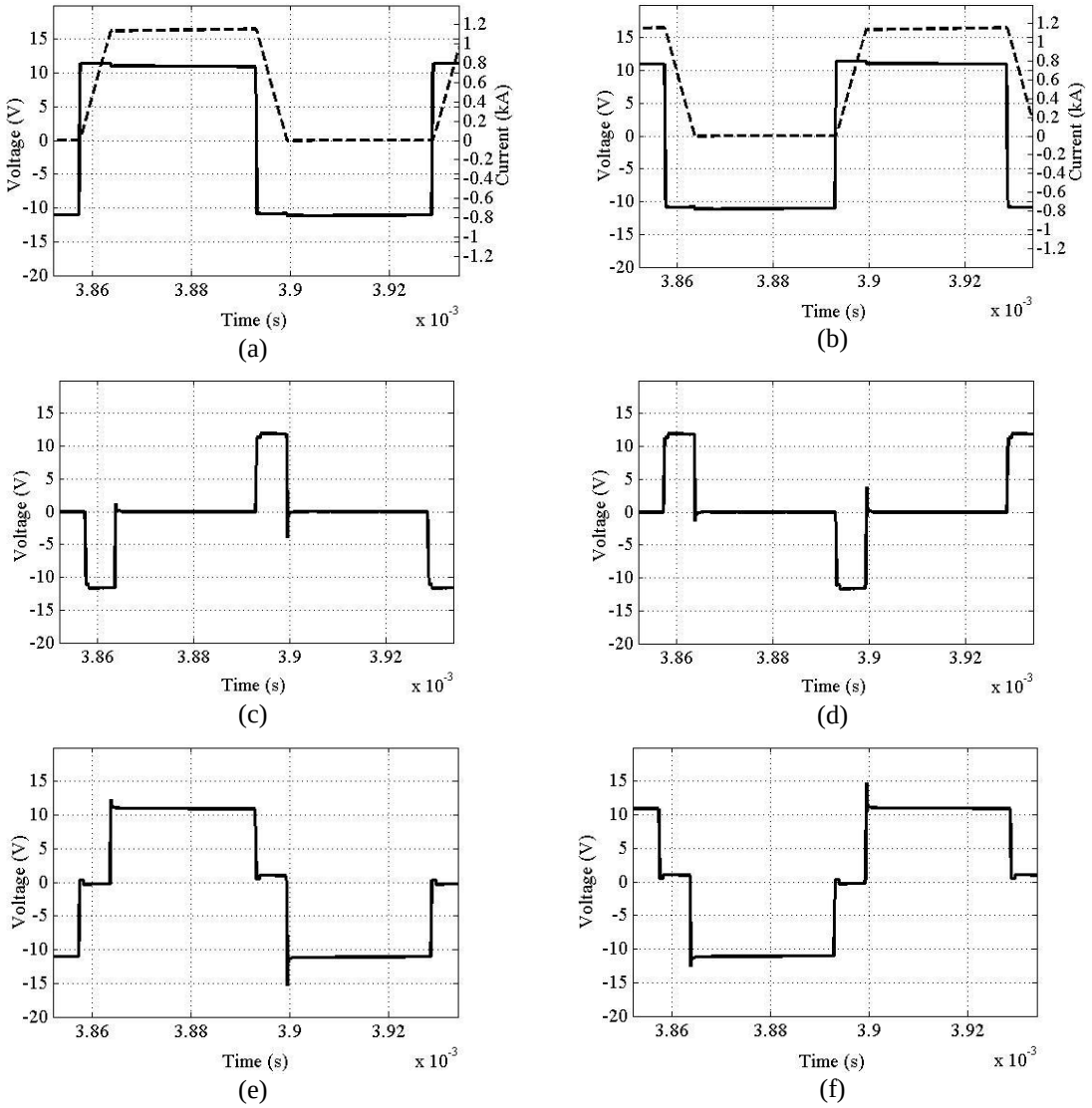


Figure 6.12: The ideal case where the secondary windings leakage inductance is equal: (a) secondary windings voltage V_{S1} and current, (b) secondary winding voltage V_{S2} and current, (c) voltage across the first secondary winding leakage inductance, (d) voltage across the second secondary winding leakage inductance, (e) total secondary winding voltage V_{S1}, and (f) total secondary winding voltage V_{S2}

Ideally, the secondary winding voltage is equal to the primary voltage multiplied by the turns ratio. Adding the effect of the secondary winding leakage inductance, the total secondary winding voltage is the sum of both the secondary winding voltage, and the voltage across the added equivalent series inductance. The voltage across the leakage inductance is a squared voltage pulse opposing the primary voltage during the linearly increasing and decreasing winding currents, causing an approximately zero output voltage during current rise and fall. However, the voltage across each secondary inductance is different with unequal winding inductances, as shown in Figures 6.13c and 6.13d respectively, which explains the asymmetrical secondary winding voltages, and consequently an asymmetrical output voltage.

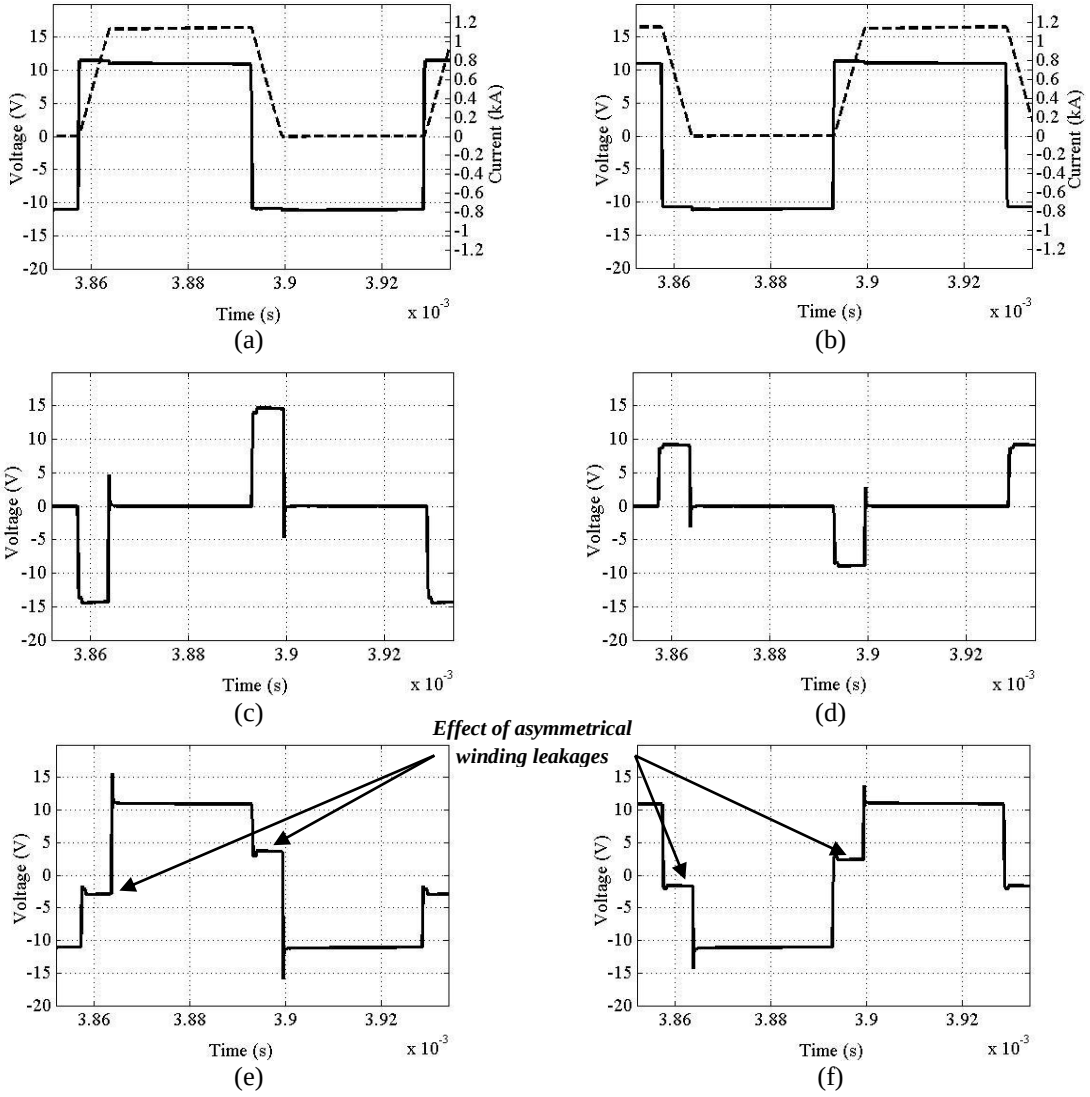
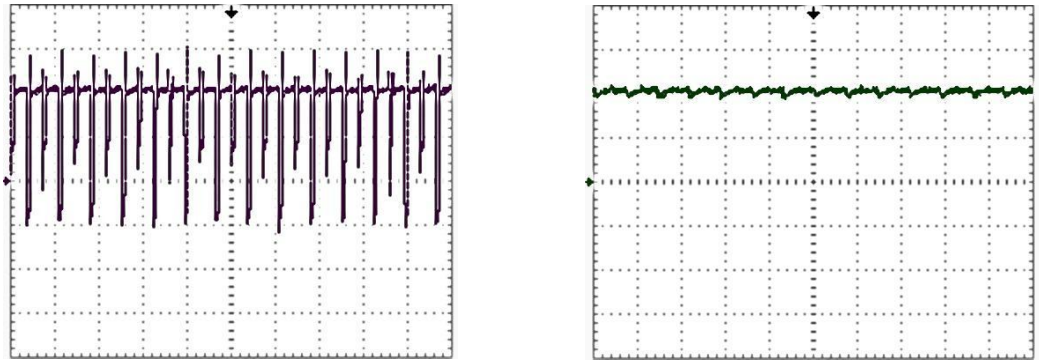


Figure 6.13: The actual case where the leakage inductance of the first secondary winding is increased by 15 nH, and the second secondary winding leakage inductance is reduced by 15 nH: (a) secondary voltage V_{S1} and current, (b) secondary voltage V_{S2} and current, (c) voltage across the first secondary winding leakage inductance, (d) voltage across the second secondary winding leakage inductance, (e) total secondary winding voltage V_{S1}, and (f) total secondary winding voltage V_{S2}

6.2.3 Converter steady-state operation, effective output voltage and efficiency

The DC/DC converter steady state output voltage, for approximately 10 cycles, is shown in Figure 6.14a, which is equivalent to a train of voltage pulses for a time period much less than the load time constant. The resultant steady state current is shown in Figure 6.14b.



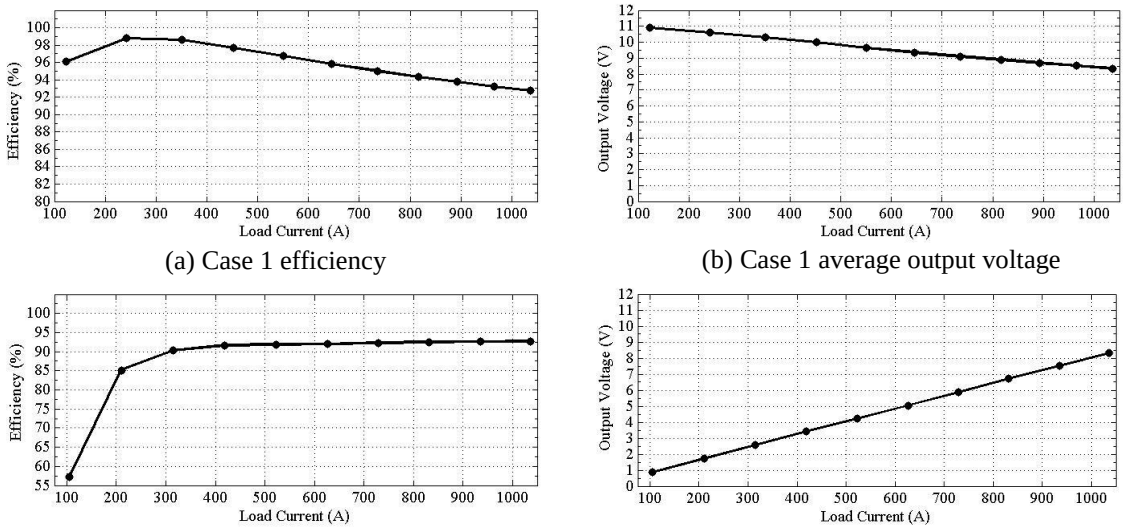
(a) V_{load}*: 5 V/div, t: 100 µs* (b) I_{load}*: 500 A/div, t: 100 100 µs*

Figure 6.14: 14 cycles at steady state operation showing (a) the output load voltage and (b) load current

The overall converter efficiency is first plotted against load current while varying the load resistance in 11 steps (the total parallel resistors in the load bank), at full primary duty cycle, as shown in Figure 6.15a. Maximum converter efficiency is achieved at full primary duty cycle at any loading condition, due to the minimisation of circulating currents during freewheeling intervals. Output voltage versus load current is shown in Figure 6.15b, in which the effective secondary duty cycle is reduced with increased loading. The efficiency at constant maximum load, and varying the primary duty cycle from 10% to 100% in 10% steps, is shown in Figure 6.15c. The corresponding output load voltage is shown in Figure 6.15d. During the first case, it is observed that a maximum efficiency of 98.8% is achieved at approximately 242A. However, the full load efficiency, at full primary duty cycle, is approximately 92.7%.

The reduced efficiency than that previously calculated, and obtained by simulation, is mainly due to larger leakage inductance. The obtained leakage inductance of 134.2 µH gives an effective secondary duty cycle of approximately 75% at full primary duty cycle, resulting in a lower average output voltage and current. However, the actual device junction temperatures are lower than those calculated, resulting in lower power loss in the MOSFETs used in both the inverter and the synchronous rectifier. A comparison between the expected and obtained power loss distribution is shown in

Table 6.3. The estimated transformer power loss is considered a combined transformer, termination, and bus bar power loss, which explains the much higher estimated value than that obtained by FEA.



(a) Case 1 efficiency

(b) Case 1 average output voltage

(c) Case 2 efficiency

(d) Case 2 average output voltage

Figure 6.15: Steady state operation efficiency and average output voltage (a) Efficiency versus load current, (b) output voltage versus load current at 100% duty cycle and increasing load, (c) Efficiency versus load current, and (d) output voltage versus load current at constant full load while varying the primary duty cycle from 10 to 100%

Table 6.3: Calculated and estimated (based on the experimental results) power loss distribution

	Calculations	**Estimated based on experimental Results**
Inverter power loss	186.84 W [(a)]	140.2 W [(d)]
Transformer power loss	74.1 W [(b)]	282 W [(e)]
Synchronous rectifier power loss	256.98 W [(a)]	252.3 W [(d)]
Load power	10.23 kW [(c)]	8.63 kW
Efficiency	95.2%	92.75%

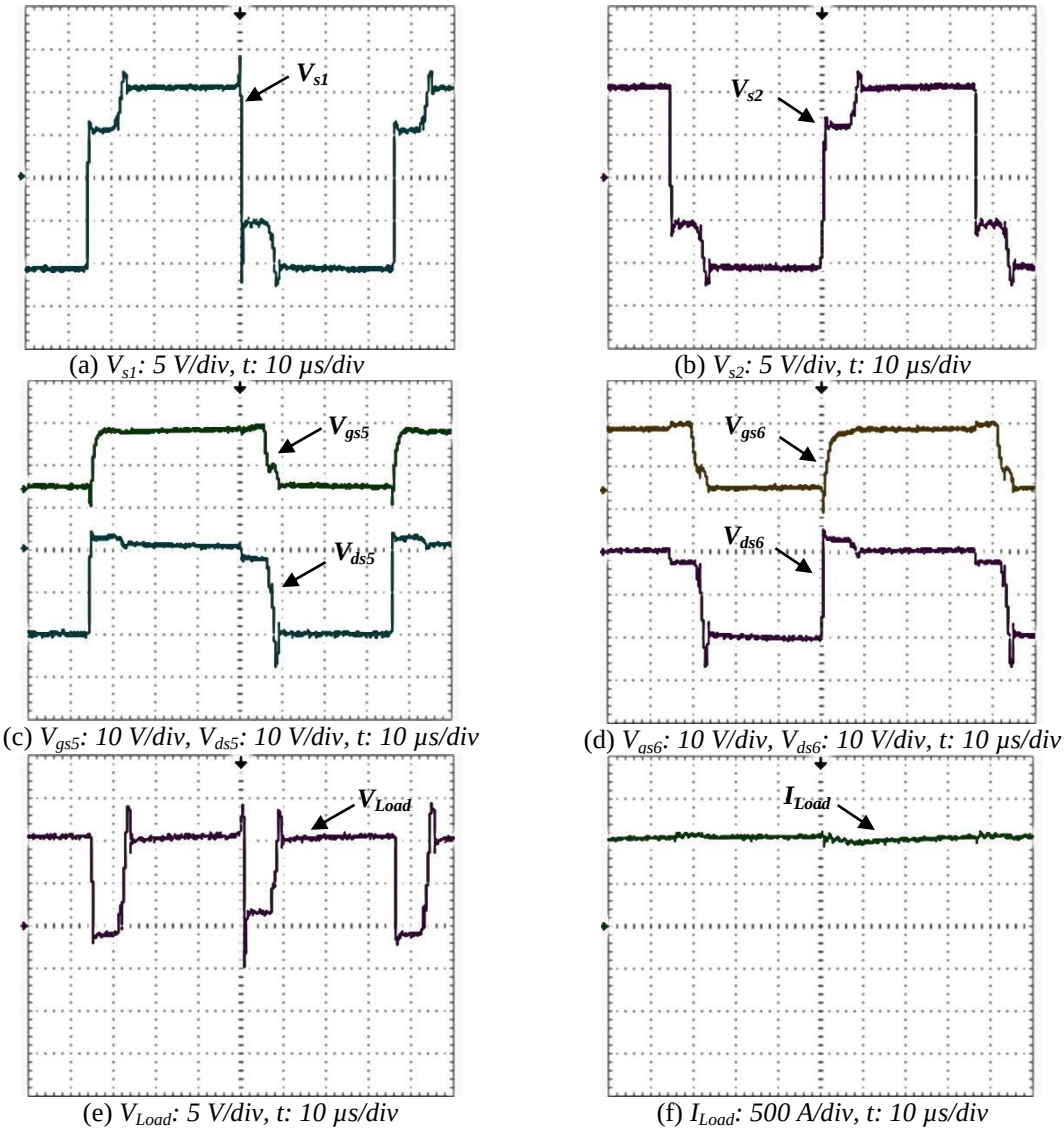
[(a)] Power loss is calculated based on the expected device junction temperature
[(b)] FEA transformer power loss obtained in Chapter 4
[(c)] Load power based on the effective average output voltage
[(d)] Based on the obtained experimental primary current waveform
[(e)] Estimated combined transformer, termination resistances and bus bar losses

6.2.4 Synchronous rectifier efficiency improvement

The synchronous rectifier power loss is approximately 257 W as shown in Table 6.2. This power loss is the sum of MOSFET conduction power loss of 45.6 W during the on interval, and the body diode power loss of 71.4 W during the freewheeling interval, per rectifier branch. The diode conduction loss can be reduced by introducing a gate signal overlap between the two rectifier sides, during the freewheeling intervals, hence minimising circulation currents through the synchronous rectifier device body diode.

However, the freewheeling interval varies with loading conditions. A large freewheeling interval is obtained at lower primary duty cycles and low load currents, and a minimum freewheeling interval of $(1-D_{eff})$ is obtained at full load current. Knowing the total leakage inductance, the overlap interval can be properly adjusted according to the primary duty cycle value. A power loss of 53 W through the MOSFET, and 0.4 W through the device body diodes is obtained per rectifier branch, by properly adjusting the overlap intervals and adding approximately 1 μs dead times, after and before the start and finish of the freewheeling intervals, which avoids secondary winding short circuit. The overall expected efficiency is 96.5% in this case; that is 1.3% increase compared to when no overlap is used.

Applying the proposed control to the experimental arrangement, a total efficiency of 93.5% at full load is obtained. That is, an increase of approximately 0.75%. Experimental results showing the secondary winding voltages, gate source voltages, drain source voltages, load voltage, and load current for the positive and negative synchronous rectifier half cycles are shown in Figure 6.16, with a total converter efficiency of 93.5%.



(a) V_{s1}: 5 V/div, t: 10 µs/div (b) V_{s2}: 5 V/div, t: 10 µs/div

(c) V_{gs5}: 10 V/div, V_{ds5}: 10 V/div, t: 10 µs/div (d) V_{as6}: 10 V/div, V_{ds6}: 10 V/div, t: 10 µs/div

(e) V_{Load}: 5 V/div, t: 10 µs/div (f) I_{Load}: 500 A/div, t: 10 µs/div

Figure 6.16: Synchronous rectifier operation with conduction overlap during the freewheeling interval at full load primary voltage duty cycle: (a) secondary winding voltage, (b) secondary winding voltage, (c) gate source voltage and drain source voltage for the positive half cycle synchronous rectifier, (d) gate source voltage and drain source voltage for the negative half cycle synchronous rectifier, (e) load voltage, and (f) load current

6.3 Closed loop system operation

Appropriate system modelling is required to obtain the required closed loop controller design. However, the DC/DC converter is considered a nonlinear dynamic system, due to the presence of switching devices. Averaging small signal methods are commonly used to linearize the converter model around a certain operating point in the continuous time domain. Linear control techniques, such as Bode plots, root locus, etc., can then be used to design the required closed loop controller response [6.1].

A general unified state space averaging approach for modelling the power stages of switching converters was first introduced in [6.2]. The approach is based on replacing the state space descriptions of the switching intervals by an equivalent averaged model over a single switching period, resulting in a single continuous state space system representation, which can then be approximated in a linear small signal model. A method to model nonlinear zero current and zero voltage switching elements for PWM and quasi resonant converters using a three terminal equivalent lumped model is presented in [6.3]. Small signal analysis can also be applied to find the equivalent system control-to-output transfer function for different PWM DC/DC converters, such as the buck, boost and buck-boost converters. The time averaging equivalent circuit approach is used for the modelling and analysis of PWM DC/DC converters in both continuous and discontinuous conduction modes [6.4].

The small signal equivalent circuit model for the buck converter is derived in [6.5]. A small signal model may be derived for the phase shifted PWM converter based on the buck converter circuit topology, due to the fact that the converter is equivalent to two interleaved buck converters [6.6]. Satisfactory results using the averaged and small signal models are obtained and presented in many publications. The small signal and transient analysis of a zero voltage switched phase shifted PWM converter based on the averaged switch model is presented in [6.7]. A digital controller based on the small signal model of a phase shifted PWM converter is implemented and presented in [6.8].

Unlike buck converters, a reduced effective duty cycle (D_{eff}) is transferred to the secondary side of the converter, which is a function of the leakage inductance, input voltage, inductor current, and the switching frequency. Hence, the derived small signal system model depends on the leakage inductance (L_{lk}), the switching frequency (f_s),

and the perturbations of the filter inductor current ($\tilde{i}_L$), input voltage ($\tilde{v}_{in}$), and the primary voltage duty cycle ($\tilde{d}$), contributing to the small signal model effective duty cycle ($\tilde{d}_{eff}$). For the system being linearized around a certain effective duty cycle (D_{eff}) and inductor current (I_L), the effective duty cycle and inductor current can then be represented as the sum of both the large signal and small signal quantities [6.6]:

$$i_L = I_L + \tilde{i}_L \tag{6.1}$$

$$d_{eff} = D_{eff} + \tilde{d}_{eff} \tag{6.2}$$

The small signal equivalent circuit model for the phase shifted PWM converter is shown in Figure 6.17, as given in reference [6.6] but without the output filter capacitor. The circuit is composed of added voltage and current sources representing the perturbations causing the small signal duty cycle modulation ($\tilde{d}$), small signal duty cycle modulation due to the change of the filter inductor current ($\tilde{d}_i$), and small signal duty cycle modulation due to the change of input voltage ($\tilde{d}_v$).

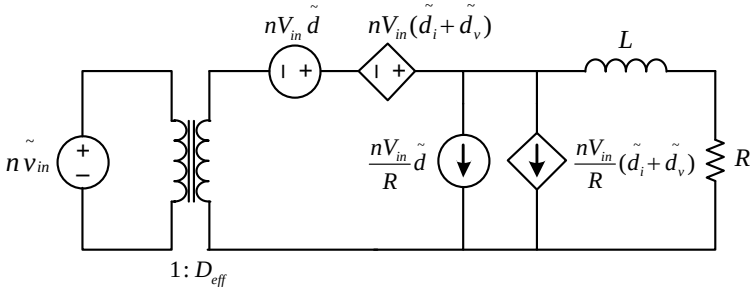


Figure 6.17: The phase shifted PWM converter small signal equivalent circuit model

The duty cycle modulation due to the change in filter inductor current is given by [6.6]:

$$\tilde{d}_i = -\frac{4n^2 L_{lk} f_s}{nV_{in}} \tilde{i}_L \tag{6.3}$$

As shown in Chapter 2, the effective duty cycle is inversely proportional to the load current, in which an increase in load current causes a reduction in the effective duty cycle. This clarifies the presence of the negative sign. The duty cycle modulation due to the change in input voltage is given by [6.6]:

$$\tilde{d}_v = -\frac{4n^2 L_{lk} f_s}{V_{in}^2} \tilde{v}_{in} \tag{6.4}$$

The total change in the small signal effective duty cycle is then:

$$\tilde{d}_{eff} = \tilde{d} + \tilde{d}_i + \tilde{d}_v \tag{6.5}$$

A state space circuit representation may be obtained using the small signal equivalent circuit model. The voltage loop equation for Figure 6.17 is:

$$nD_{eff}\,\tilde{v}_{in} + nV_{in}\,\tilde{d} + nV_{in}(\tilde{d}_i + \tilde{d}_v) = L\frac{d\,\tilde{i}_L}{dt} + \tilde{i}_L R \tag{6.6}$$

Solving for $\frac{d\,\tilde{i}_L}{dt}$:

$$\frac{d\,\tilde{i}_L}{dt} = \left(\frac{nD_{eff}}{L}\right)\tilde{v}_{in} + \left(\frac{nV_{in}}{L}\right)\tilde{d} + \left(\frac{nV_{in}}{L}\right)\tilde{d}_i + \left(\frac{nV_{in}}{L}\right)\tilde{d}_v - \left(\frac{R}{L}\right)\tilde{i}_L \tag{6.7}$$

and by substituting Equations (1) and (2) into (3):

$$\frac{d\,\tilde{i}_L}{dt} = \left(-\frac{R+R_d}{L}\right)\tilde{i}_L + \left(\frac{nD_{eff} + R_d I_L/V_{in}}{L}\right)\tilde{v}_{in} + \left(\frac{nV_{in}}{L}\right)\tilde{d} \tag{6.8}$$

where:

$$R_d = 4n^2 L_{lk} f_s \tag{6.9}$$

Hence, the state space representation for the first order system, where the system state vector is $x(t) = \left[\tilde{i}_L\right]$, the input vector is $u(t) = \begin{bmatrix}\tilde{d} \\ \tilde{v}_{in}\end{bmatrix}$, and the output vector is $y(t) = \left[\tilde{i}_L\right]$, is:

$$\begin{aligned} \dot{x} &= \left[-\frac{R+R_d}{L}\right]x + \begin{bmatrix}\frac{nV_{in}}{L} & \frac{nD_{eff} + R_d I_L/V_{in}}{L}\end{bmatrix}u \\ y &= [1]\,x \end{aligned} \tag{6.10}$$

Assuming constant converter input voltage, and neglecting the small signal input voltage perturbations ($\tilde{v}_{in}$), the system is transformed to a single input, single output system with a control to output transfer function given by:

$$G_{id}(s) = \frac{\tilde{i}_L(s)}{\tilde{d}(s)} = \frac{nV_{in}/(R+R_d)}{sL/(R+R_d)+1} \tag{6.11}$$

The Bode plot for the open loop system is shown in Figure 6.18, where the system parameters used are shown in Table 6.4.

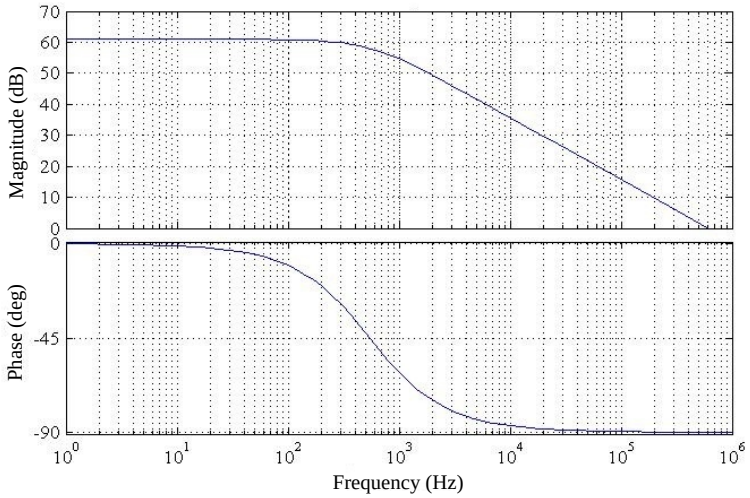


Figure 6.18: Control-to-output transfer function Bode plot

Table 6.4: System parameters used for obtaining the Bode plots

System parameter	Value
Turns ratio (n)	1/54
Input voltage (V_{in})	600 V
Leakage inductance (L_{lk})	115 µH
Switching frequency (f_s)	14 kHz
Load resistance (R)	7.72 mΩ
Load inductance (L)	2.9 µH

The open loop system gain and time constant are given by:

$$k = \frac{nV_{in}}{(R+R_d)} = 1118.3 \tag{6.12}$$

$$\tau = \frac{L}{(R+R_d)} = 292.8\mu s \tag{6.13}$$

The main requirement of closed loop control is to track a given output reference. A classical PI controller is used, which is generally sufficient for first order systems, and is considered appropriate due to the fact that no complicated control is required. A basic block diagram for the closed loop system is shown in Figure 6.19. The controller gains adopted can be readily tuned using the rules of Ziegler and Nicholas [6.9].

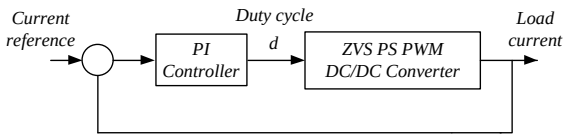
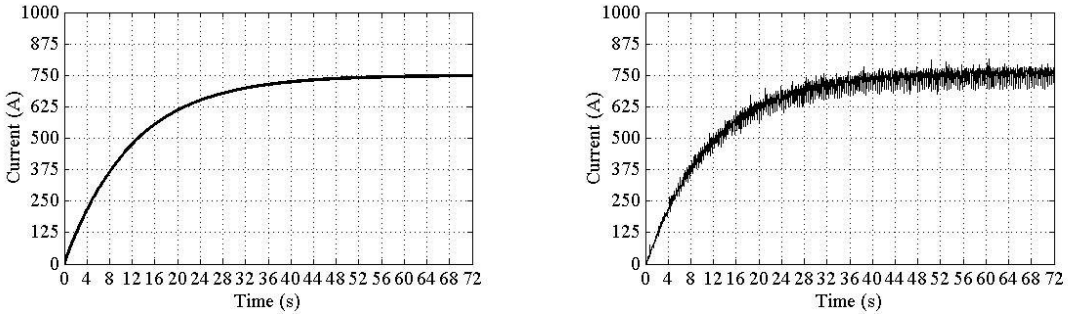


Figure 6.19: Basic block diagram for the closed loop system

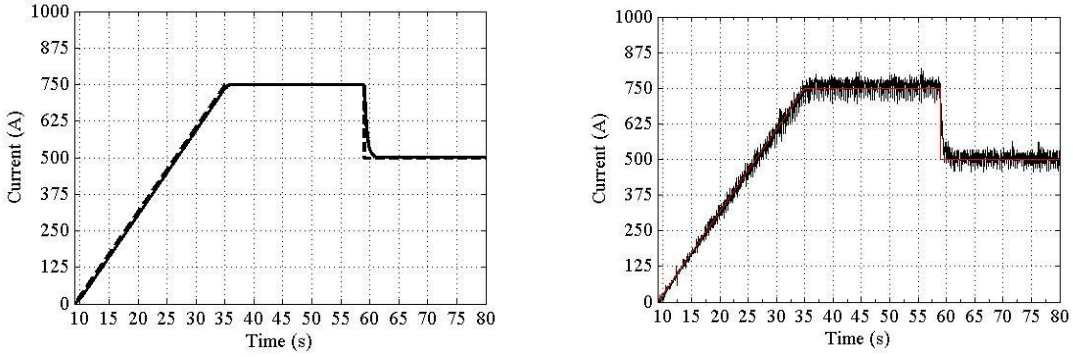
The system is initially tested at a reduced response, increasing the system time constant to avoid mechanical and electrical stresses generated due to the high secondary current. Simulations based on the small signal modelling and the experimental results for closed loop current control, at a constant current reference of 750 A, are shown in Figures 6.20a and 6.20b respectively. The adopted PI controller gains (K_P and K_i) are given in Appendix F4.



(a) (b)

Figure 6.20: Closed loop system load current response by (a) simulation results based on the small signal model, and (b) experimental results

A second experimental test is carried out, where the output current is first increased using a given ramping up current reference from 0 to 750 A, increasing linearly with a rate of 30 A per second. A step change for the current reference to 500 A is then applied after approximately 25 seconds. Current reference signal and converter response obtained by simulations, and obtained experimentally are given in Figure 6.21.



(a) (b)

Figure 6.21: Closed loop system response for the DC/DC converter showing the current reference signal compared to (a) the output current obtained by the small signal model based simulations, and (b) the output current obtained by experimental results

6.4 Summary and discussion

Experimental validation for the designed 1 kA, ZVS phase-shifted PWM converter was successfully presented through this chapter. Open loop system analysis was first performed to show the system characteristics at different operating conditions. Power loss analysis showing the loss distribution through the various system components showed that relatively large power loss is obtained within the secondary circuit bus bars and termination. However, a converter efficiency of 92.75% is initially achieved, with the synchronous rectifier gate signals being synchronised with the inverter left-leg gate signals. An efficiency improvement of approximately 0.75% is achieved by introducing conduction overlap for the opposite synchronous rectifier half cycles, avoiding MOSFET body diode conduction during the freewheeling intervals. Finally, the converter was modelled using the averaged small signal equivalent circuit model, obtaining an equivalent linearized model to apply a conventional PI closed loop current control. Experimental results for the closed loop system response showed good convergence with the small signal modelling based simulation results.

References

[6.1] F. Musavi, K. Al-Haddad, H.Y. Kanaan, *"A novel large signal modelling and dynamic analysis of paralleled DC/DC converters with automatic load sharing control"*, IEEE International Conference on Industrial Technology, ICIT'04, Volume 1, pp. 536-541, 2004.

[6.2] S. Cuk, R. Middlebrook, *"A general unified approach to modelling switching DC-to-DC converters in discontinuous conduction mode"*, International Journal of Electronics, Volume 1, pp. 36-57, 1977.

[6.3] V. Vorperian, R. Tymerski, F.C.Y. Lee, "Equivalent circuit models for resonant and PWM switches", IEEE Transactions on Power Electronics, Volume 4, pp. 205-214, 1989.

[6.4] J. Xu, *"DC and AC small signal analysis of zero-current quasi-resonant buck converter"*, IEEE International Symposium on Circuits and Systems, pp. 684-687, 2002.

[6.5] N. Mohan, T. Undeland, W. Robbins, *"Power Electronics: Converters, Applications, and Design"*, Wiley New York, ISBN: 0471584088, 1995.

[6.6] V. Vlatkovic, J. Sabate, R. Ridley, F. Lee, B. Cho, "Small-signal analysis of the phase-shifted PWM converter", IEEE Transactions on Power Electronics, Volume 7, pp. 128-135, 2002.

[6.7] F. Tsai, "Small-signal and transient analysis of a zero-voltage-switched, phase-controlled PWM converter using averaged switch model", IEEE Transactions on Industry Applications, Volume 29, pp. 493-499, 2002.

[6.8] P. Kocybik, K. Bateson, *"Digital control of a ZVS full-bridge DC-DC converter"*, IEEE Tenth Annual Applied Power Electronics Conference and Exposition, APEC '95, pp. 687-693, 2002.

[6.9] K. Ogata, *"Modern control engineering"*, Prentice Hall, ISBN: 0136156738, 2009.

Chapter 7

10 kA DC/DC Converter Design and Parallel Converter Operation

Parallel connected DC/DC converters must be used to satisfy the main requirement of supplying the toroidal field coil current of 32 MA. A lab-scaled prototype DC/DC converter, showing the possibility of achieving a high efficiency conversion system through recent advances in magnetic and semiconductor technologies, was designed, modelled and successfully implemented in the previous chapters. The applicability of synchronous rectification to high current rectifiers, by using parallel connected MOSFET, was also verified to improve the efficiency of low output voltage and high power requirements.

This chapter presents scaled up design for the 1 kA DC/DC converter system presented, with an output current capability of 10 kA per module. The transformer design is first discussed, including methods for leakage inductance minimisation. Chip level MOSFET device paralleling is proposed to reduce the large number of paralleled devices adopted in the synchronous rectifier, and minimise possibilities for current imbalance. Finally, the parallel operation of two DC/DC converter modules, using common current reference control, is presented.

7.1 10 kA DC/DC converter design

A 10 kA secondary current module rating is specified based on the maximum achievable current rating per transformer, which is directly related to the available core window area, and the chosen conductor current density. Specifying the high-voltage side voltage rating involves multiple basic trade-offs. Utilising a high frequency converter design allows for the parallel connected converter modules to be located close to the load coils, due to the reduced converter footprint, hence reducing high current bus bar lengths. A basic schematic diagram for the proposed system configuration is shown in Figure 7.1, in which 200 parallel connected modules are connected in parallel to supply each 2 MA limb current, for the ST fusion reactor.

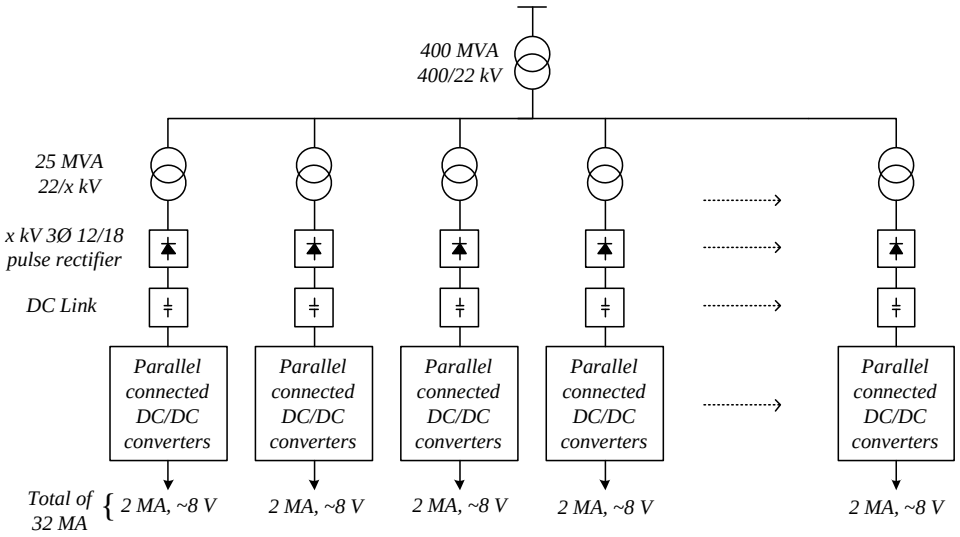


Figure 7.1: Basic schematic diagram for the proposed toroidal field power supply

The 25 MVA, 22/*x* kV, transformers may be located remote from the reactor due to their large volume. The 12 or 18 pulse diode rectifiers may then be also placed with the transformers, considering the obtained DC link voltage resulting from the rectification ratio in each case (for example: the DC link voltage is equal to 1.39*x* kV in case of a 12 pulse rectifier). The DC link voltage is then required to be transmitted through relatively high-current bus-bars, to the final stage: low-voltage high-current, parallel connected DC/DC conversion. A high DC link voltage level must be selected to minimise high current transmission and associated losses. Voltage levels of 600 and 900 V are first introduced to provide a design base for comparison of the different power loss contributions to the various system components, based on the chosen DC link voltage.

7.1.1 Transformer design

The transformer design presented in this chapter is based on the commercially available oval core dimensions. Only basic calculations are discussed. The full design procedures, analysis, and full FEA simulations can be similarly performed as presented in Chapter 4. The largest oval nanocrystalline core provided by Magnetec® is shown in Appendix G. The core window area, where A and C are core dimensions defined in Appendix G1, is:

$$W_A = C\left(A-C\right)+\pi\left(\frac{C}{2}\right)^2 = 28744.3mm^2 \tag{7.1}$$

Applying a window utilisation factor of 0.3 for the primary Litz winding, and 0.4 for the secondary foil windings, the window area should satisfy the following equation:

$$W_A \geq \frac{N_1 A_1}{0.3} + \frac{2N_2 A_2}{0.4} \tag{7.2}$$

where A_1 and A_2 are the primary and secondary winding conductor cross section areas respectively. A single turn secondary winding is used for the high current secondary winding. Specifying a secondary voltage of 12 V gives an initial safe margin (approximately 25%) accounting for the rectifying switch voltage drop and secondary voltage duty cycle loss. For the case where the primary voltage is 900 V, the turns ratio is:

$$\frac{N_1}{N_2} = \frac{I_2}{I_1} = \frac{JA_2}{JA_1} = \frac{A_2}{A_1} = \frac{75}{1} \tag{7.3}$$

where J is the specified conductor current density. By solving Equations (7.2) and (7.3), the primary and secondary conductor cross section areas, are:

$$A_1 \leq 46mm^2$$

$$A_2 \leq 3449.3mm^2$$

Using a conductor current density of 3 A/mm2, the primary and secondary rated currents are:

$$I_1 \leq 138A$$

$$I_2 \leq 10.35kA$$

Using the core net nanocrystalline cross section area of 520 mm^2 (core datasheet given in Appendix G), and an operating flux density of ($0.8B_{sat}$ = 0.96 T), the minimum operating frequency which insures operation within the linear *BH* region, and provides sufficient safe margin for B_{sat} reduction due to material defects and temperature variations, is:

$$f \geq \frac{V_1}{4B_{op}A_{fe}N_1} \geq 6001Hz$$

Calculations are similarly performed for the 600 V primary voltage design. The basic transformer specifications for both cases are shown in Table 7.1.

Table 7.1: Basic transformer design specifications

Primary/secondary voltage	900/12 V	600/12 V
Primary/secondary current	133.3/10 000 A	200/ 10 000 A
Turns ratio	75:1	50:1
Frequency	6 kHz	6 kHz

7.1.2 Leakage inductance minimisation

Transformer leakage inductance is a critical design parameter. It should be noted that it is not necessary to eliminate the leakage inductance. However, it should be limited to an acceptable specific value, which results in the maximum ZVS range, without significantly increasing the secondary voltage duty cycle loss to a level which reduces the average output voltage to less than the required value. It has been concluded in the previous chapter that not only the transformer design specifies the total leakage inductance referred to the primary side. Termination bus bars, as well as secondary circuit layout stray inductances are also added to the total reflected leakage.

For the centre tapped transformer design previously presented, each secondary winding is linked to half of the primary winding placed underneath it on each core limb, and is linked to the other half of the primary winding through the core window breadth. The part which is linked through the core window breadth contributes to a large portion of the leakage flux. Reduced leakage is obtained by dividing each of the secondary windings into two series parts, with each placed on one limb, to provide better primary to secondary coupling. Interleaving the primary and secondary windings may be used to achieve further leakage inductance reduction.

A comparison between the simple primary-secondary arrangement, the winding arrangement where each secondary is placed on both limbs through two series windings in a sandwich arrangement (where the primary is placed between the two secondary winding sections), and a two layer interleaved configuration is shown in Figure 7.2. This figure shows the winding arrangement on the core in each case and connection for each winding section. Primary to one secondary and secondary to secondary MMF diagrams across the windings are also shown for each case respectively.

The total leakage inductance in each case, referred to the primary side, may be calculated following the procedures in Chapter 4. 3D geometry models used for the transformer transient response simulation using FEA for each case, with and without the bus bar terminations, are shown in Figure 7.3.

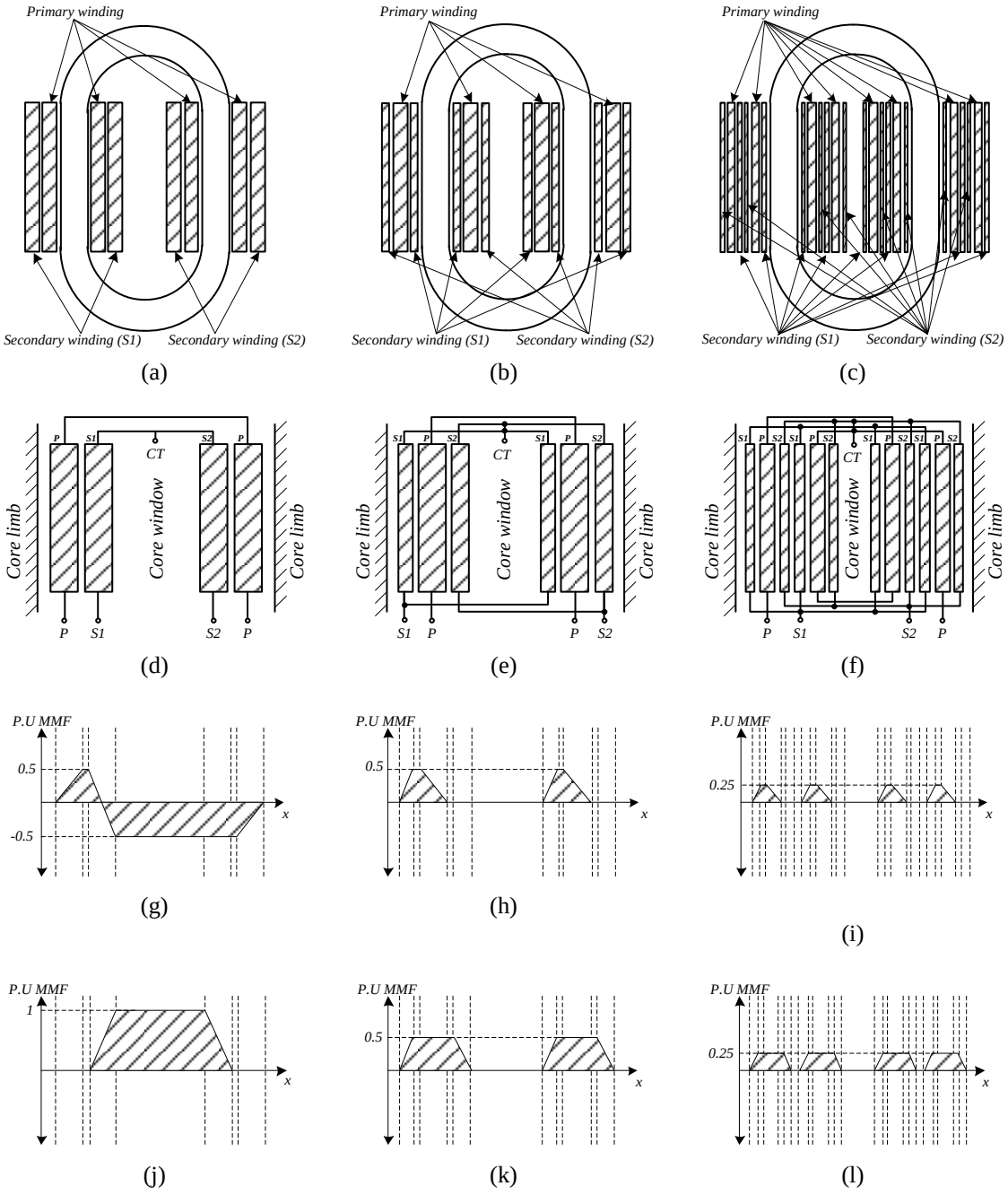


Figure 7.2: Comparison between the three winding arrangement cases; (a) case 1: basic primary secondary arrangement, (b) case 2: sandwich primary secondary arrangement, and (c) interleaved sandwich primary secondary arrangement, showing the winding connection in (d), (e), and (f), the primary to one secondary MMF in (g), (h), and (i), and the secondary to secondary MMF in (j), (k), and (l), for each case respectively

FEA simulations are carried out to estimate the leakage inductance in each case. Interleaving in this case is equivalent to dividing the secondary winding inductance into multiple secondary windings, with their inductance being paralleled and referred to the primary side. This significantly reducing the total reflected inductance to the primary

side. Simulation results for each case, with and without bus bar terminations, in both cases where the primary voltage is 600 and 900 V, is shown in Table 7.2.

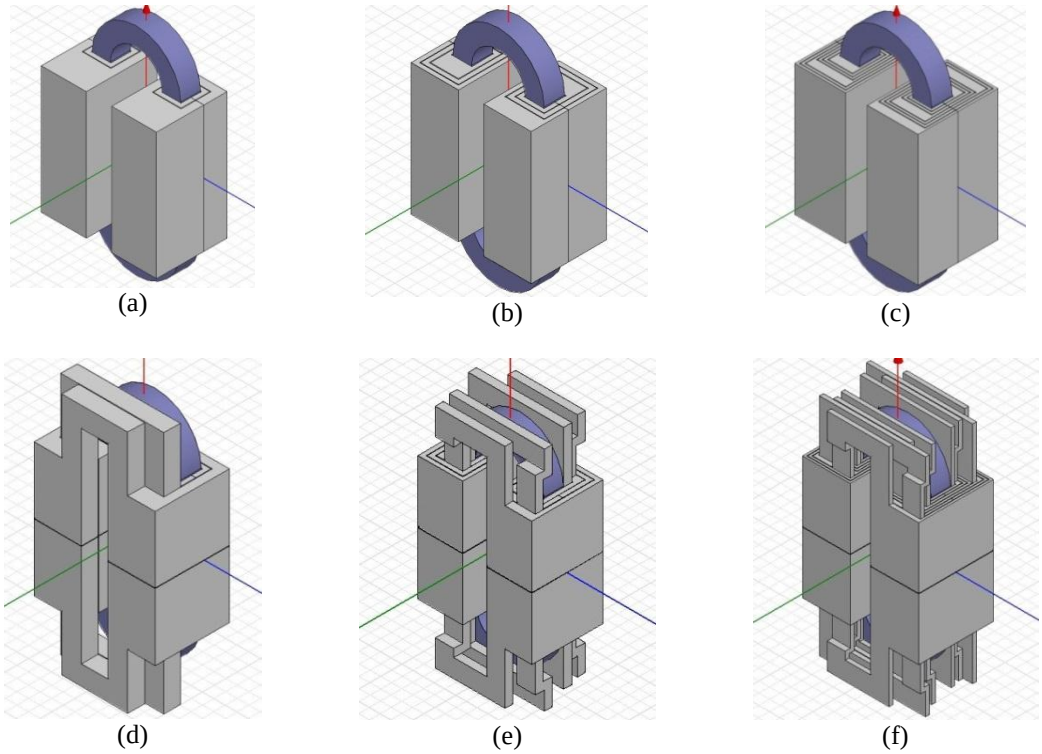


Figure 7.3: 3D transformer models used for FEA in each case: (a) simple primary secondary winding arrangement, (b) sandwich primary secondary windings, (c) interleaved sandwich primary and secondary windings, and the same configurations with added bus bar termination in each case in (d), (e), and (f) respectively

Table 7.2: Transformer leakage inductance obtained by FEA simulation for the simple primary secondary configuration, sandwich primary secondary configuration, and interleaved sandwich primary secondary configuration, for the 600 V and 900 V designs.

Primary voltage		**Case 1**	**Case 2**	**Case 3**
600 V	L_{lk} **(without terminals)**	19.6 μH	7.6 μH	3.9 μH
	L_{lk} **(with terminals)**	43.4 μH	18.5 μH	8.9 μH
900 V	L_{lk} **(without terminals)**	45.5 μH	17.8 μH	9.16 μH
	L_{lk} **(with terminals)**	114.18 μH	43.37 μH	21.1 μH

It is observed that the 600 V transformer design always possesses a lower leakage inductance. The reflected bus-bar terminals stray inductance is increased for the higher voltage design, mainly due to the increased turns ratio. However, significant reduction is achieved in both cases by interleaving. Moreover, the 900 V design shows reduced power loss, by approximately 20 %, due to the lower primary winding current.

7.1.3 Phase-shift PWM ZVS converter

ZVS phase-shift PWM converter operation is analysed at both operating voltages. A leakage inductance which gives the same effective secondary duty cycle, is used both cases, to compensate for the difference in primary current values and primary turns ratio, and to obtain a fair comparison. Both converters operate at an 87% primary voltage duty cycle, and delivering 10 kA at 8.5 V.

The MOSFET inverter uses the low on-resistance (0.35 Ω) IYXS HiPerFET^{TM}, 1200 V, 32A, power MOSFET devices, in which 8 parallel devices per switch are used to achieve the required current rating (200 A). The higher voltage inverter is restricted to IGBT devices, since suitable power MOSFET technology is currently limited to blocking voltages of 1200 V. However, IGBT semiconductor technology is continuously improving. A newly developed, 1700 V, 200 A, trench gate IGBT, utilising the light punch through carrier stored chips, offers the same collector-emitter saturation voltage ($V_{CE(sat)}$) of equivalent IGBT 1200 V devices at the same current rating [7.1]. Basic power loss calculations are performed for both cases and the results are shown in Table 7.3.

Table 7.3: power loss comparison between the 600 V and 900 V inverters, utilising 1200 V MOSFETs and 1700 V IGBT respectively

	1200 V, 32A, MOSFETs	**1700 V, 200 A, IGBTs**
Total number of devices	32	4
Conduction power loss	3164 W [(a)]	759 W [(a)]
Switching power loss	-	1104 W [(b)]
Total power loss	3164 W	1863 W

[(a)] Conduction power loss at T_j = 125 ^oC

[(b)] Worst case turn-off switching power loss based on datasheet E_{off}, at T_j = 125 ^oC and V_{cc} = 1000 V

Lower power loss is achieved with the IGBT inverter, which is mainly due to the lower IGBT conduction losses. Phase shifted ZVS PWM basically eliminates turn-on power loss and significantly reduces device turn off loss, which is negligible for the MOSFET devices at low switching frequencies. Significant turn-off power loss is obtained with IGBTs due to the IGBT turn-off tail current [7.2]. However, zero current switching (ZCS) techniques are considered more suitable for IGBT, in which the device current is forced to zero before turning off the device [7.3], [7.4]. However, an alternative resonant inverter configuration, in which half the supply voltage is applied across the transformer, as shown in Figure 7.4, may be used [7.5]. This configuration has the

advantage of reducing the number of switches used. More research on this point is left for future research.

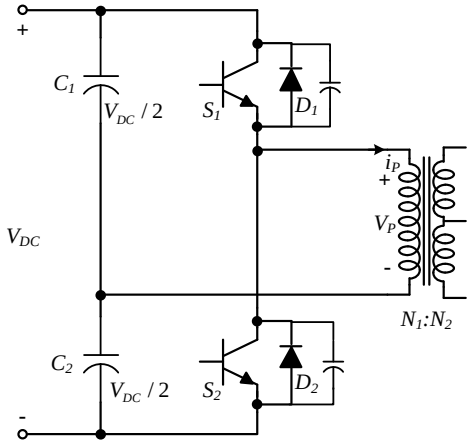


Figure 7.4: Alternative half-bridge configuration with half the line voltage across the transformer

The on-resistance of high voltage MOSFETs may be effectively reduced by using liquid nitrogen cooling, as concluded in Chapter 3. However, the 1200 V, 32 A, 0.35Ω, MOSFET showed significant on-resistance increase on testing the device at relatively low currents (1 to 11A), at 77k. The on-resistance increased with the increase in current due to channel self-heating effects, causing an increase in junction temperature. Identically to this condition, a reduction factor of approximately 7 is achieved at approximately 166K. This device possesses the lowest on-resistance compared to other devices in the 1200 V range. This can be achieved by lightly doping the drift region, and adding more p stripes, as shown in Chapter 3, which significantly reduces the drift region resistance and gives higher voltage blocking capabilities. Hence, the lightly doped drift region causes carrier freezout at 77K for this device. Additional research on this point is also left for future research.

7.1.4 Synchronous rectification and chip level MOSFET paralleling

Paralleling a large number of power MOSFETs is required to satisfy the synchronous rectifier current rating of 10 kA. The latest high current MOSFET (Infineon, 0.95 mΩ, 30V), in which the maximum operating current is package limited to 180 A, is chosen. The centre tapped synchronous rectifier would require approximately 100 parallel connected devices per rectifier branch for each device to carry 100 A during each rectification half cycle, and obtain an effective voltage drop of approximately 0.1 V.

Paralleling such large number of devices introduces possible circuit layout and current path length differences, which may lead to current sharing imbalance between devices. Acceptable transient and steady state current imbalance levels are achieved, even with high device parameter and circuit layout mismatches, as discussed earlier in Chapter 5 [7.6]. However, the different generated thermal stresses may lead to one device failure among the paralleled devices, leading to converter disconnection, and reducing system reliability.

This section realises a MOSFET module with multiple parallel interconnected dies within the same package. Chip level paralleling is already used in high voltage IGBT modules to achieve high power levels as discussed in [7.7] and [7.8]. Device parameter screening and symmetric device layout would then be carried out by the manufacturer, hence reducing and simplifying the overall converter design and implementation times. A 3D view for the MOSFET package (IPB180N03S4L, 0.95 mΩ, 30 V, 180 A), showing device terminals and internal device die, is shown in Figure 7.5.

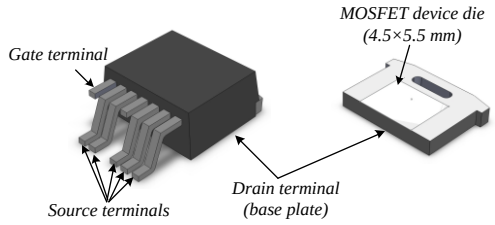


Figure 7.5: IPB180N03S4L 30 V MOSFET device package and internal die

An IGBT module with multiple internally interconnected dies is shown in Appendix G, along with the device datasheet. Based on the same IGBT module base plate dimensions and available internal space for die placement, a similar MOSFET module is proposed and shown in Figure 7.6, in which 48 internal chip dies are connected in parallel. Unlike the original MOSFET device package, the base plate cannot be used as the drain terminal due to manufacturing difficulties. Dies must be first soldered on a thin conducting plate, insulated from the base plate. Source and drain terminals are then connected to copper plates interconnected to the final bus-bar module terminals. Symmetric interconnections within the module must be assured for equal current path inductance and resistance, and consequently equal current sharing between the paralleled dies within the package. MOSFET on-resistance positive temperature coefficient helps ensure current sharing, especially since devices are thermally coupled.

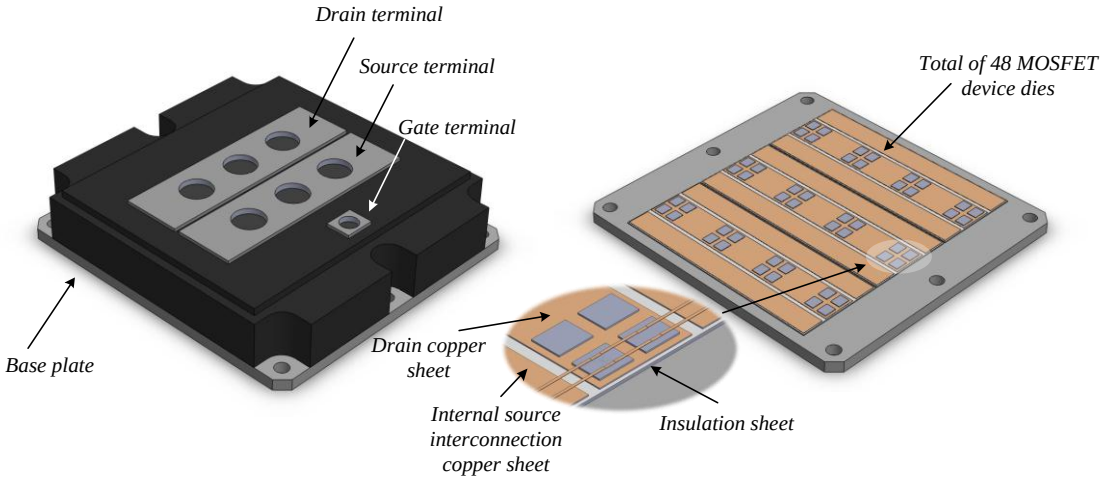


Figure 7.6: The proposed high current MOSFET device package with 48 parallel connected dies

According to the maximum power dissipation of a single die package of 250 W, the total maximum power dissipation for the 48 paralleled die module is 12 kW, provided that the case temperature is maintained at $25^{o}C$. The base plate spreads the heat power giving a maximum power dissipation of approximately 71 W/cm^2, which significantly less than the theoretical forced air cooling limit of 150 W/cm^2, and can be handled by conventional cooling methods [7.9] ,[7.10].

Power loss is similarly calculated as previously presented, with overlapping gate signals to circulate the load current through the MOSFET device rather than the body diode during the freewheeling intervals. The 10 kA synchronous rectifier, utilising 2 modules per rectifier branch, has a total power loss of approximately 850 W.

7.1.5 Overall converter operation and losses

A comparison between the 10 kA converter module total power loss distribution and expected efficiency, for the 600 V and 900 V designs, is shown in Table 7.4.

Table 7.4: Power loss distribution and expected efficiency for the 10 kA DC/DC converter

	600 V design	**900 V design**
Inverter power loss	3164 W	1863 W
Transformer power loss	565 W	469 W
Synchronous rectifier power loss	850 W	850 W
Power output	85 kW	85 kW
DC/DC converter efficiency	94.8 %	96.4%

7.2 Parallel converter operation

The modular power system approach, in which individual lower power converter modules are connected in parallel to achieve the required total power rating, is widely used in distributed power systems, and offers several advantages over a single high power system [7.11]. Higher system reliability is achieved by introducing a certain level of redundancy, in the case of individual converter failure and disconnection [7.12], [7.13]. Moreover, the standardisation of components leads to a significant reduction in design and manufacturing time and cost. Equal voltage and/or current sharing must be achieved to avoid higher transient and steady state electrical and thermal stresses on individual converters. The basic configurations for paralleled output connected converters are the input series and input parallel configurations [7.14]. The input series connection offers the advantage of using lower voltage devices on the high voltage side and having lower conversion ratios for individual converters. However, due to the large number of required converters for this specific application, the input parallel connection is only considered. The operation of input and output parallel connected converters may be analysed based on the linearized converter model presented in Chapter 6. However, the full model is used in which the input voltage perturbations are considered, in which the operation of two converters with different DC input voltage can be analysed. This may be a result of being fed from different DC link capacitors. The state-space representation of the DC/DC converter is given by Equation (6.10). Simulation for two parallel connected 10 kA DC/DC converters based on small signal modelling is carried out using MATLAB®, supplying a total load current of 20 kA. A block diagram representation for open loop operation is shown in Figure 7.7.

Two cases are studied, the first where Converter I DC link voltage is 850 V, while the other converter is fed from 900 V. The second case shows the effect of different converter parameters, in which Converter I possesses an increased transformer leakage inductance. The Matlab Simulink model and system parameters used for both cases are given in the Appendix. Simulation results for both cases are shown in Figures 7.9a and 7.9c respectively, in which converter II must provide more current to compensate for the output voltage reduction of converter I. The overloaded operation of Converter II causes increased thermal stresses on the converter components, which may lead to converter disconnection.

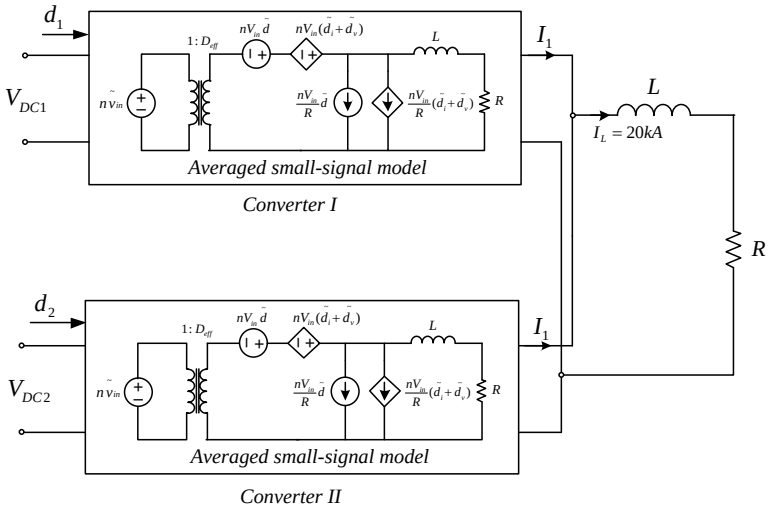


Figure 7.7: Block diagram representation for the open loop operation of two parallel connected converters, using the equivalent averaged small-signal model

Current-control closed-loop operation can effectively provide reliable parallel converter operation in this case. A block diagram for the closed loop system is shown in Figure 7.8, where individual current loops are used for each converter. A common reference current is supplied to individual converters. Simulation results show equal converter current sharing for both cases, where converters are supplied with different DC link voltages and different converter parameters, as shown in Figures 7.9b and 7.9d respectively.

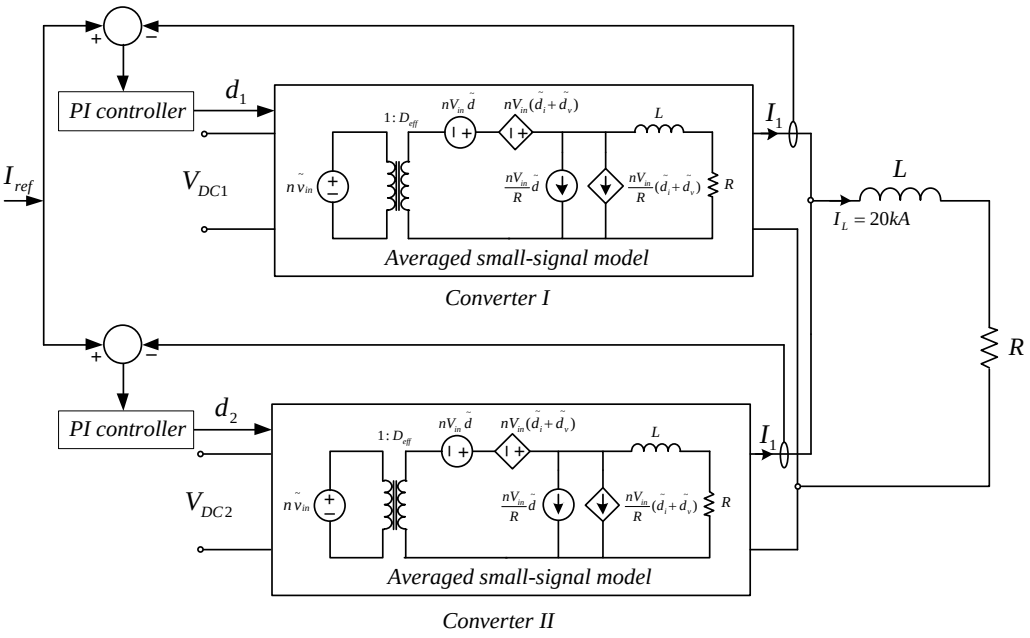


Figure 7.8: Common current reference closed loop control of two parallel connected converters

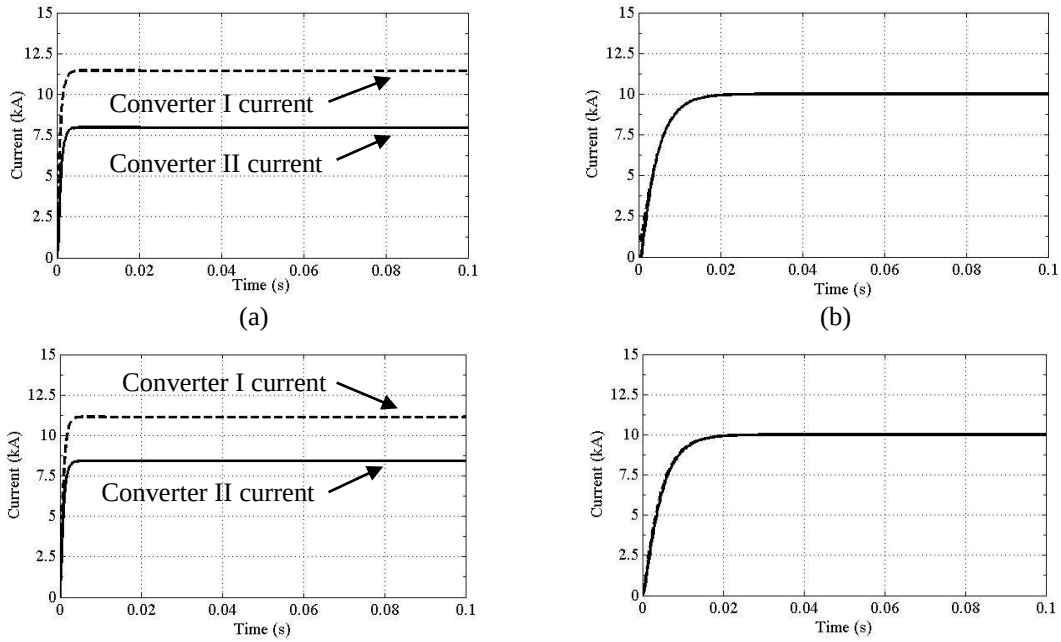


Figure 7.9: Simulations results for the open loop operation of two parallel connected converters supplying a load current of 20 kA, with different DC link voltages and different converter parameters in (a) and (c), and in case of common current reference closed loop operation in (b) and (d) respectively

7.3 Summary

The up-scaled 10 kA DC/DC converter design, based on the 1 kA design presented in the previous chapters, was briefly analysed. The current rating is chosen based on the achievable transformer design according to commercially available core dimensions. Interleaving must be used to reduce transformer leakage inductance, due to its significant effects on the scaled-up converter. Power loss was analysed for DC link voltages of 600 and 900 V. Parallel connected converters must be used to satisfy current requirements. Simple common current reference control is proposed, and is shown to provide balanced converter current sharing in the case of different DC link voltages, as well as different converter parameters.

References

[7.1] N. Clark, J. Donlon, "*NEW 1700V A-SERIES IGBT MODULES WITHS CSTBT AND IMPROVED FWDi*", Powerex Semiconductors, Application note.

[7.2] Q. Jinrong, A. Khan, I. Batarseh, "*Turn-off switching loss model and analysis of IGBT under different switching operation modes*", IEEE 21st International Conference on Industrial Electronics, Control, and Instrumentation, Volume 1, pp. 240-245, 1995.

[7.3] R.L. Steigerwald, R.W. De Doncker, H. Kheraluwala, "*A comparison of high-power DC-DC soft-switched converter topologies*", IEEE Transactions on Industry Applications, Volume 32, pp. 1139-1145, 1996.

[7.4] W. Konrong, F.C. Lee, H. Guichao, D. Borojevic, "*A comparative study of switching losses of IGBTs under hard-switching, zero-voltage-switching and zero-current-switching*", 25th Annual IEEE Power Electronics Specialists Conference, PESC'94, Volume 2, pp. 1196-1204, 1994.

[7.5] L. Hui, P. Fang Zheng, J.S. Lawler, "*A natural ZVS medium-power bidirectional DC-DC converter with minimum number of devices*", IEEE Transactions on Industry Applications, Volume 39, pp. 525-535, 2003.

[7.6] J. Forsythe, "*Paralleling of power MOSFETs for higher power output*", International Rectifier, Application Note.

[7.7] A. Wintrich, J. Nascimento, M. Leipenat, "*Influence of parameter distribution and mechanical construction on switching behaviour of parallel IGBT*", IEEE Proceeding of the Power Conversion Intelligent Motion Conference, PCIM'06, pp. 511-516, 2006.

[7.8] M. Bäßler, M. Münzer, S. Burkert, "*Research of Current Distribution in IGBT Modules with Multiple Chips in Parallel*", Power Conversion Intelligent Motion Europe, pp. 1-4,2005.

[7.9] W. Huang, M. Stan, S. Gurumurthi, R. Ribando, K. Skadron, "*Interaction of scaling trends in processor architecture and cooling*", 26th Annual IEEE Semiconductor Thermal Measurement and Management Symposium, SEMI-THERM'10, pp. 198-204, 2010.

[7.10] W. Nakayama, "*Exploring the limits of air cooling*", Electronics Cooling, Volume 12, pp. 1-10, 2006.

[7.11] L. Shiguo, Y. Zhihong, L. Ray-Lee, F.C. Lee, "*A classification and evaluation of paralleling methods for power supply modules*", 30th Annual IEEE Power Electronics Specialists Conference, PESC'99, Volume 2, pp. 901-908, 1999.

[7.12] L. Thorsell, P. Lindman, "*Reliability analysis of a direct parallel connected redundant power system based on highly reliable DC/DC modules*", IEEE 10th International Telecommunications Energy Conference, INTELEC'88, pp. 551-556, 1988.

[7.13] T.F. Wu, K. Siri, C.Q. Lee, "*Reliability improvement in parallel connected converter systems*", IEEE International Conference on Industrial Electronics, Control and Instrumentation, IECON'91, Volume 1, pp. 429-434, 1991.

[7.14] R. Giri, R. Ayyanar, N. Mohan, "*Common duty ratio control of input series connected modular DC-DC converters with active input voltage and load current sharing*", Eighteenth Annual IEEE Applied Power Electronics Conference and Exposition, APEC '03, Volume 1, pp. 322-326, 2003.

Chapter 8

Conclusion

8.1 General conclusion

A high-current low-voltage DC power supply, with a total output current of 32 MA at approximately 8.5 volts, is required to supply the spherical tokamak power plant (STPP), single-turn toroidal field coil. The toroidal field coil consists of 16 coil limbs, connected to a central rod, forming the doughnut shaped magnetic confinement chamber, with the supply divided into 16 converter modules, each supplying 2 MA current. The same design is to be applied to a component test facility (CTF), based on the same spherical tokamak power plant concept, which is due for construction before proceeding with the actual power plant. Similarly, the component test facility utilises a single turn toroidal field coil, comprising 10 coil limbs, with a total central rod current of 10.5 MA, requiring a converter output voltage of approximately 10V. High efficiency, reliability, and reduced converter footprint, are the basic design constraints for the required power supply system. A basic AC/DC converter configuration, based on conventional rectifying techniques, was first introduced as a possible approach. However, the baseline design, utilising 12-pulse, half-wave, diode rectifiers at supply frequency, possesses a low efficiency (approximately 67%) and a relatively impractical footprint requirement. Exploring different converter topologies is thus mandatory.

Conventional diode rectification is considered inadequate for low output voltage requirements because of high conversion efficiency restrictions. A typical 1.3V, high power diode, forward voltage drop, results in a rectifier stage conversion efficiency of approximately 85% at an output voltage of 8.5V. Synchronous rectification is widely used in low-power low-voltage rectifier circuits (being initially introduced in buck rectifiers), and is similarly applied to the required power supply system. Employing a high frequency transformer can significantly reduce the overall converter footprint, as 50 Hz transformers are considered the bulkiest system component. A modular approach is used, in which multiple low power rating converters are connected in parallel. This can significantly increase system reliability by providing multiple redundant standby modules.

Based on the previous discussion, a double-stage conversion system is proposed. The high-voltage stage is a conventional step-down full-bridge rectifier, delivering an output voltage of 600V to 900V. The second stage is a high frequency DC/AC/DC converter, utilising a ZVS phase-shift PWM inverter, a high frequency transformer, and a synchronous rectifier. Parallel connected modules are to be used for obtaining the total required current rating. A lab-sized prototype design, delivering 1kA at 8V, operating at 14 kHz, was successfully designed, analysed, and implemented, to validate the basic system requirements.

8.2 Author's contribution

The thesis outcomes can be enumerated as follows:

- The basic operation of the ZVS phase-shift PWM, adopting MOSFET devices, is analysed. Analytical expressions for the conduction power loss through the MOSFET device and body diode are derived. MOSFET devices are particularly attractive for this specific application. However, this is not the case for higher voltage, and higher power requirements. It has been shown that using IGBTs for a 900V inverter design results in higher system efficiency, compared to a 600V design utilising MOSFET devices, at the same power rating.
- Liquid nitrogen cooling is not considered beneficial with low on-resistance, advanced vertical power MOSFET structure devices (CoolMOS, or HyperFET devices). A cryogenic testing experimental setup was built. The on-resistance reduction factors at 77K, compared to 400K, are obtained for selected devices covering most device breakdown voltages (which is proportional to the on-resistance). High voltage devices showed the highest on-resistance reduction factors. Power saving is only achieved for devices with reduction factors higher than that required for cooling the devices down to 77 K (i.e. devices with a reduction factor higher than 10), which are the devices suited for low power, high frequency applications.
- A nanocrystalline cored, high frequency transformer has been successfully designed, and experimentally tested. Nanocrystaline magnetic materials possess lower core loss and higher saturation flux density compared to the conventionally used ferrite cores. Hence, a reduced volume, and higher efficiency design is obtained. A centre-tapped transformer is implemented using

an oval core shape, in which each half secondary winding is placed on one core limb. Experimental results showed the necessity of reducing the secondary termination bus-bar lengths, which significantly increases the total reflected leakage inductance to the primary side, and directly affects circuit operation. Symmetrical bus-bar connections and secondary circuit layout are also mandatory for symmetrical operation in positive and negative half cycle rectifier operation.

- A Matlab based electro-thermal device model was developed for studying the parallel operation of MOSFET devices. The model was used to estimate the transient and steady-state current sharing characteristics in the case of different device parameters. Acceptable current mismatch levels are typically obtained, provided that paralleled devices are thermally coupled, arranged symmetrically such that equal drain and common-source inductances are obtained, and are triggered using the same gate signal.
- A 1kA synchronous rectifier was implemented, using parallel connected, surface-mount, MOSFET device packages. Ten devices are directly connected to the secondary circuit bus-bars, as the total secondary current is beyond the capability of printed circuit boards.
- A control-driven synchronisation technique was developed for the MOSFET rectifier, which delivers higher efficiency than self-driven techniques. Both MOSFET rectifier half-cycles are turned-on during the half-wave rectifier commutation period, such that load current circulates through the MOSFET devices rather than body diodes. The commutation period is a function of the total reflected leakage inductance, load resistance, and primary voltage duty-cycle.
- An up-scaled 10 kA converter design was presented, taking the advantage of using lower loss, higher power devices, reducing the number of parallel converters required to achieve a certain total output current.
- A design for a MOSFET device package, with 48 parallel connected device dies was presented. Chip-level paralleling is typically used for high power IGBT packages. The package simplifies paralleling a large number of MOSFET devices.

- Finally, a common current reference control technique was briefly presented for parallel connected converter module operation. It is shown that this control technique is adequate to provide current sharing, even with different individual converter parameters (such as the input voltage or transformer leakage inductance).

8.3 Future research

Further experimental research can be carried out using lab-scaled converter designs, which includes:

- Investigate other inverter topology configurations, such as the half-bridge resonant configuration discussed in a previous chapter, which halves the number of devices used.
- Rearrange the transformer secondary termination bus-bars, to minimise the total reflected leakage inductance. A possible improvement can be achieved by using an interleaved winding configuration.
- Verify the parallel operation of converter modules using the proposed common current reference control.
- Contacting regional industrial prototyping companies for implementing a prototype MOSFET device package, with multiple parallel interconnected device-dies.

Appendix A: ZVS Phase-Shift PWM Resonant Converter

A1. RMS primary transformer current through each sub-interval:

The RMS current during each sub-interval (power delivery, freewheeling, and slew) can be calculated by integrating the linearly approximated current shown in Figure A1.

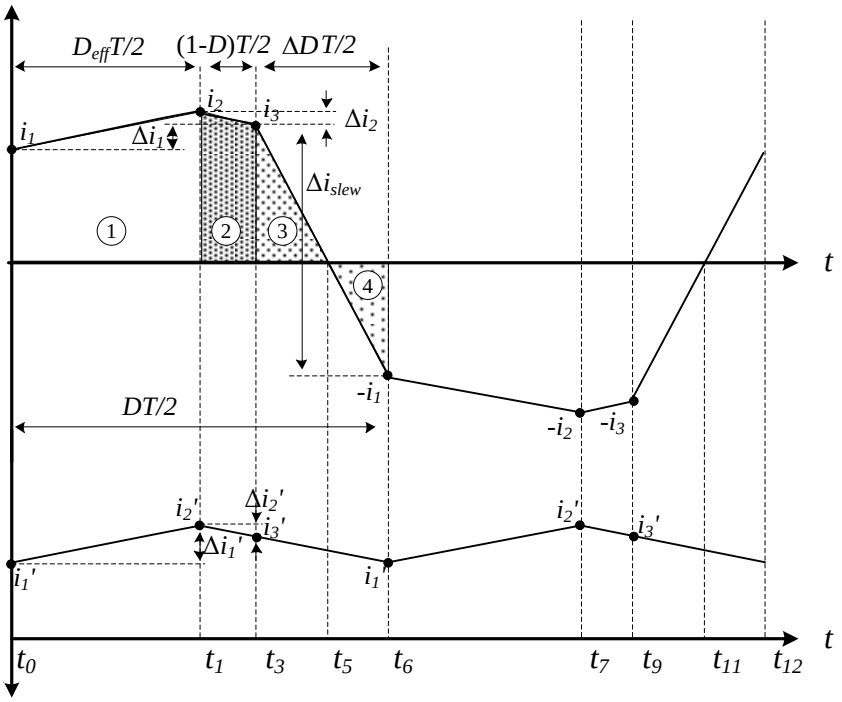


Figure A1: Primary transformer and filter inductor currents

$$i_{rms} = \sqrt{\frac{1}{period}\int_0^{period} \left(i(t)\right)^2 dt}$$

For interval 1:

$$i(t) = i_1 + \left(\frac{\Delta i_1}{D_{eff}\,T/2}\right)t$$

$$\therefore i_{rms} = \sqrt{\frac{1}{D_{eff}\,T/2}\int_0^{D_{eff}T/2}\left(i_1 + \left(\frac{\Delta i_1}{D_{eff}\,T/2}\right)t\right)^2 dt}$$

$$= \sqrt{\frac{1}{D_{eff}\,T/2}\int_0^{D_{eff}T/2}\left(i_1^{\,2} + \left(\frac{2i_1\Delta i_1}{D_{eff}\,T/2}\right)t + \left(\frac{\Delta i_1}{D_{eff}\,T/2}\right)^2 t^2\right)dt}$$

$$= \sqrt{\frac{1}{D_{eff}\,T/2}\left(i_1^{\,2} t + \left(\frac{2 i_1 \Delta i_1}{D_{eff}\,T/2} \right) \frac{t^2}{2} + \left(\frac{\Delta i_1}{D_{eff}\,T/2} \right)^2 \frac{t^3}{3} \right)_0^{D_{eff}\,T/2}}$$

$$= \sqrt{i_1^{\,2} + i_1 \Delta i_1 + \frac{\Delta i_1^{\,2}}{3}}$$

Similarly, for interval 2:

$$i(t) = i_2 - \left(\frac{\Delta i_2}{(1-D)T/2} \right) t$$

$$\therefore i_{rms} = \sqrt{\frac{1}{(1-D)T/2} \int_0^{(1-D)T/2} \left(i_2 - \left(\frac{\Delta i_2}{(1-D)T/2} \right) t \right)^2 dt}$$

$$= \sqrt{\frac{1}{(1-D)T/2} \int_0^{(1-D)T/2} \left(i_2^{\,2} - \left(\frac{2 i_2 \Delta i_2}{(1-D)T/2} \right) t + \left(\frac{\Delta i_2}{(1-D)T/2} \right)^2 t^2 \right) dt}$$

$$= \sqrt{\frac{1}{(1-D)T/2} \left(i_2^{\,2} t - \left(\frac{2 i_2 \Delta i_2}{(1-D)T/2} \right) \frac{t^2}{2} + \left(\frac{\Delta i_2}{(1-D)T/2} \right)^2 \frac{t^3}{3} \right)_0^{(1-D)T/2}}$$

$$= \sqrt{i_2^{\,2} - i_2 \Delta i_2 + \frac{\Delta i_2^{\,2}}{3}}$$

Assuming that ΔD is equally divided for intervals 3 and 4, interval 3 instantaneous current can be expressed as follows:

$$i(t) = i_3 - \left(\frac{i_3}{\Delta D\,T/4} \right) t$$

$$\therefore i_{rms} = \sqrt{\frac{1}{\Delta D\,T/4} \int_0^{\Delta D T/4} \left(i_3 - \left(\frac{i_3}{\Delta D\,T/4} \right) t \right)^2 dt}$$

$$= \sqrt{\frac{1}{\Delta D\,T/4} \int_0^{\Delta D T/4} \left(i_3^{\,2} - \left(\frac{2 i_3^2}{\Delta D\,T/4} \right) t + \left(\frac{i_3^2}{(\Delta D\,T/4)^2} \right) t^2 \right) dt}$$

$$= \sqrt{\frac{1}{\Delta D\,T/4} \left(i_3^2 t - \left(\frac{2 i_3^2}{\Delta D\,T/4} \right) \frac{t^2}{2} + \left(\frac{i_3^2}{(\Delta D\,T/4)^2} \right) \frac{t^3}{3} \right)_0^{\Delta D T/4}}$$

$$= \sqrt{\frac{i_3^{\,2}}{3}}$$

For interval 4:

$$i(t) = \left(\frac{-i_1}{\Delta DT/4} \right) t$$

$$\therefore i_{rms} = \sqrt{\frac{1}{\Delta DT/4} \int_0^{\Delta DT/4} \left(\left(\frac{-i_1}{\Delta DT/4} \right) t \right)^2 dt}$$

$$= \sqrt{\frac{1}{\Delta DT/4} \left(\left(\frac{i_1^2}{(\Delta DT/4)^2} \right) \frac{t^3}{3} \right)_0^{\Delta DT/4}}$$

$$= \sqrt{\frac{i_1^{\,2}}{3}}$$

A2. MOSFET device technical datasheet (only first page is shown):

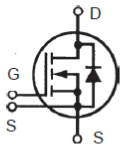
IXYS Advanced Technical Data

HiPerFET™ Power MOSFETs

IXFN 32N120

V_{DSS} = 1200V
I_{D25} = 32A
$R_{DS(on)}$ = 0.35Ω

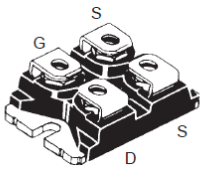
N-Channel Enhancement Mode
Avalanche Rated, High dv/dt, Low t_{rr}



Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	1200	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ	1200	V
V_{GS}	Continuous	±30	V
V_{GSM}	Transient	±40	V
I_{D25}	T_C = 25°C, Chip capability	32	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	128	A
I_{AR}	T_C = 25°C	32	A
E_{AR}	T_C = 25°C	64	mJ
E_{AS}	T_C = 25°C	4	J
dv/dt	$I_S \le I_{DM}$, di/dt ≤ 100 A/µs, $V_{DD} \le V_{DSS}$, $T_J \le$ 150°C, R_G = 2 Ω	15	V/ns
P_D	T_C = 25°C	780	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
V_{ISOL}	50/60 Hz, RMS t = 1 min $I_{ISOL} \le$ 1 mA t = 1 s	2500 3000	V~ V~
M_d	Mounting torque Terminal connection torque	1.5/13 1.5/13	Nm/lb.in. Nm/lb.in.
Weight		30	g

Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_{DSS}	V_{GS} = 0 V, I_D = 3 mA	1200			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 8 mA	2.5		5.0	V
I_{GSS}	$V_{GS(th)}$ = ±30 V_{DC}, V_{DS} = 0			±200	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS} = 0 V, T_J = 25°C			50	µA
	$V_{DS} = V_{DSS}$, V_{GS} = 0 V, T_J = 125°C			3	mA
$R_{DS(on)}$	V_{GS} = 10 V, $I_D = 0.5 \bullet I_{D25}$ Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %			0.35	Ω

miniBLOC, SOT-227 B (IXFN)
E153432



G = Gate D = Drain
S = Source TAB = Drain

Either Source terminal at miniBLOC can be used as Main or Kelvin Source

Features
- International standard package
- miniBLOC, with Aluminium nitride isolation
- Low $R_{DS(on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
- Fast intrinsic Rectifier

Applications
- DC-DC converters
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- Temperature and lighting controls

Advantages
- Easy to mount
- Space savings
- High power density

A3. Relevant device characteristics used in the analysis:

- $R_{DS(on)}$ (on-resistance) versus T_j (junction temperature):

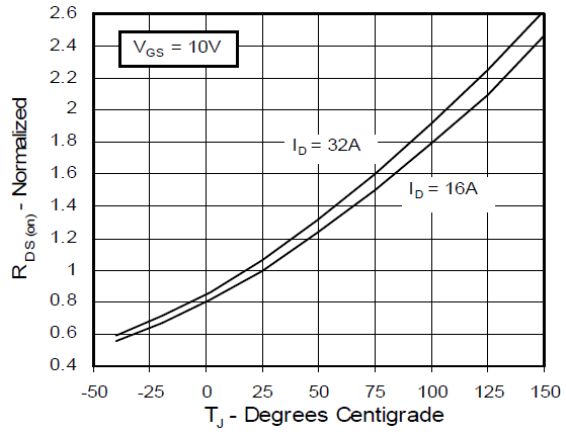


Figure A2: Normalised device on-resistance versus the junction tmperature

- Junction capacitances:

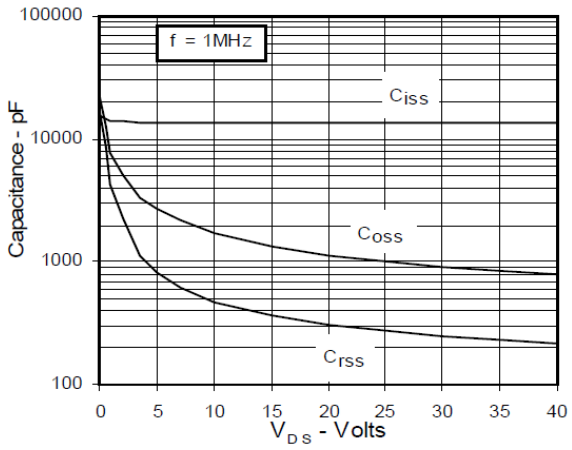
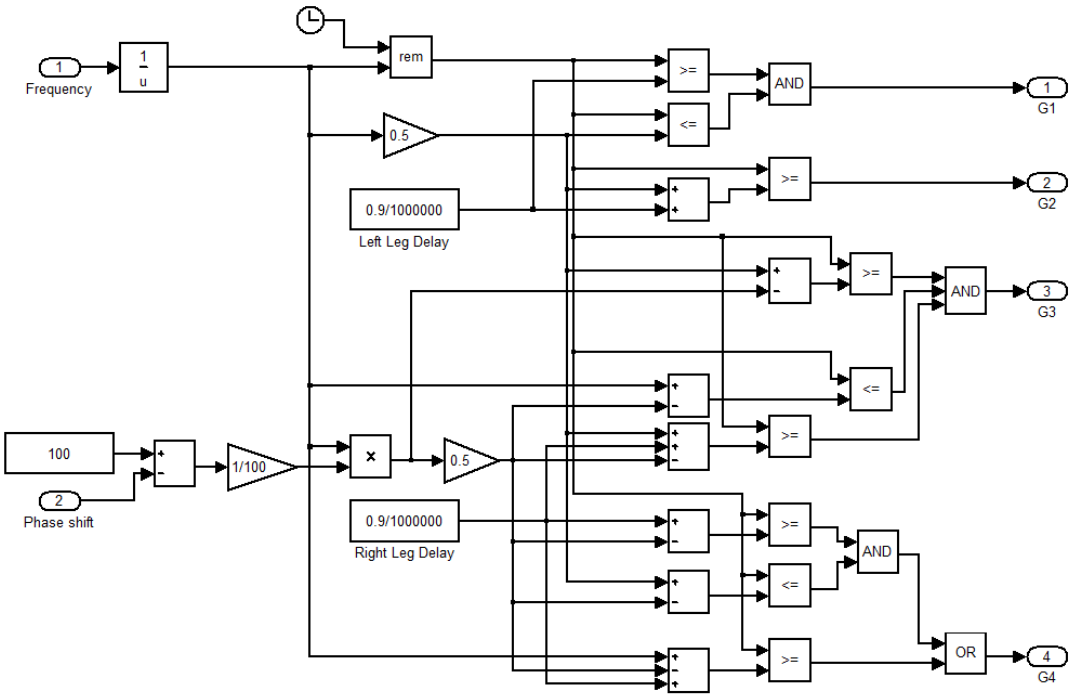


Figure A3: Device junction capacitances versus the device drain-source voltage

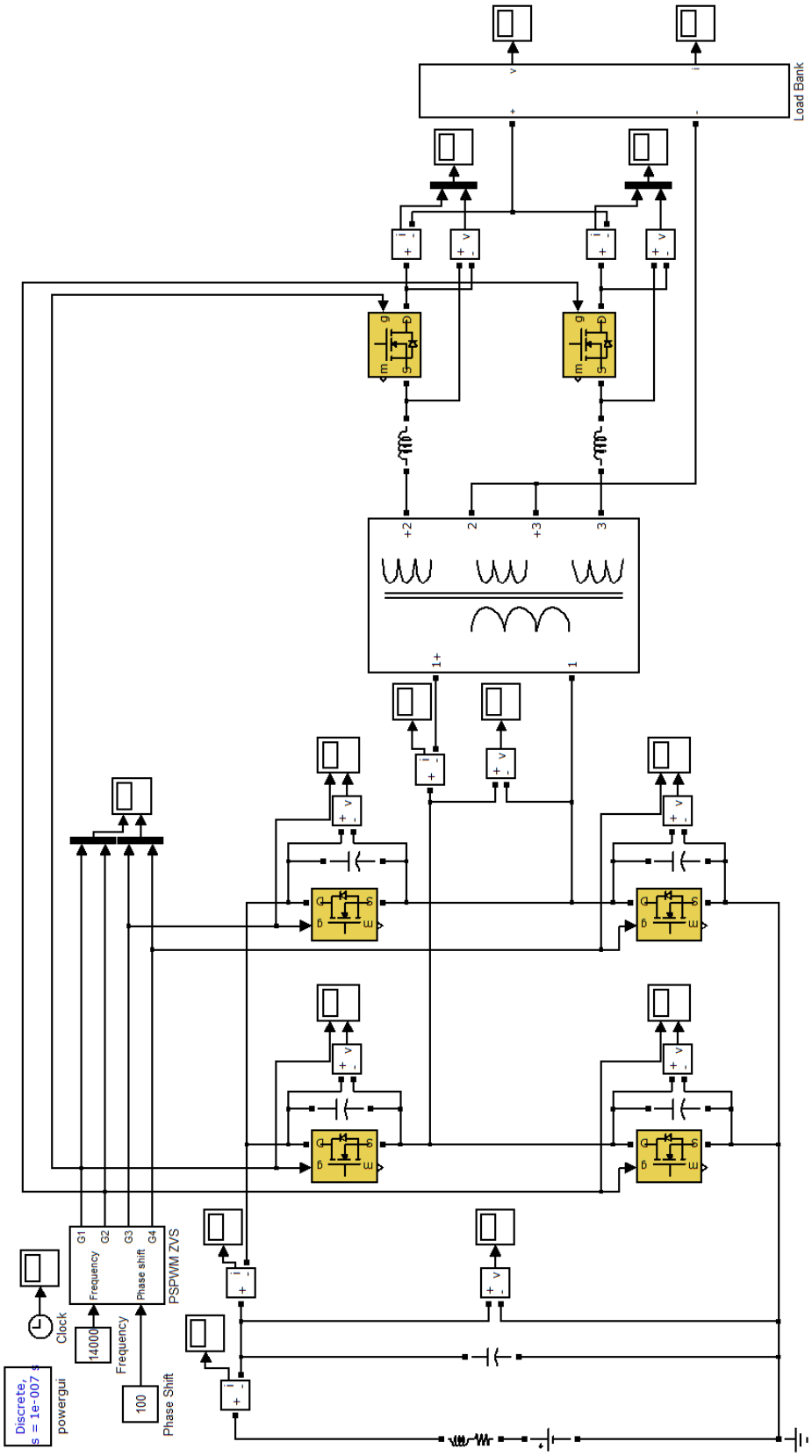
Output capacitance value used for design procedures	C_{oss} = 1000pF

A4. Matlab Simulink model, for the ZVS phase-shift PWM converter:

- Gate signal generation block:

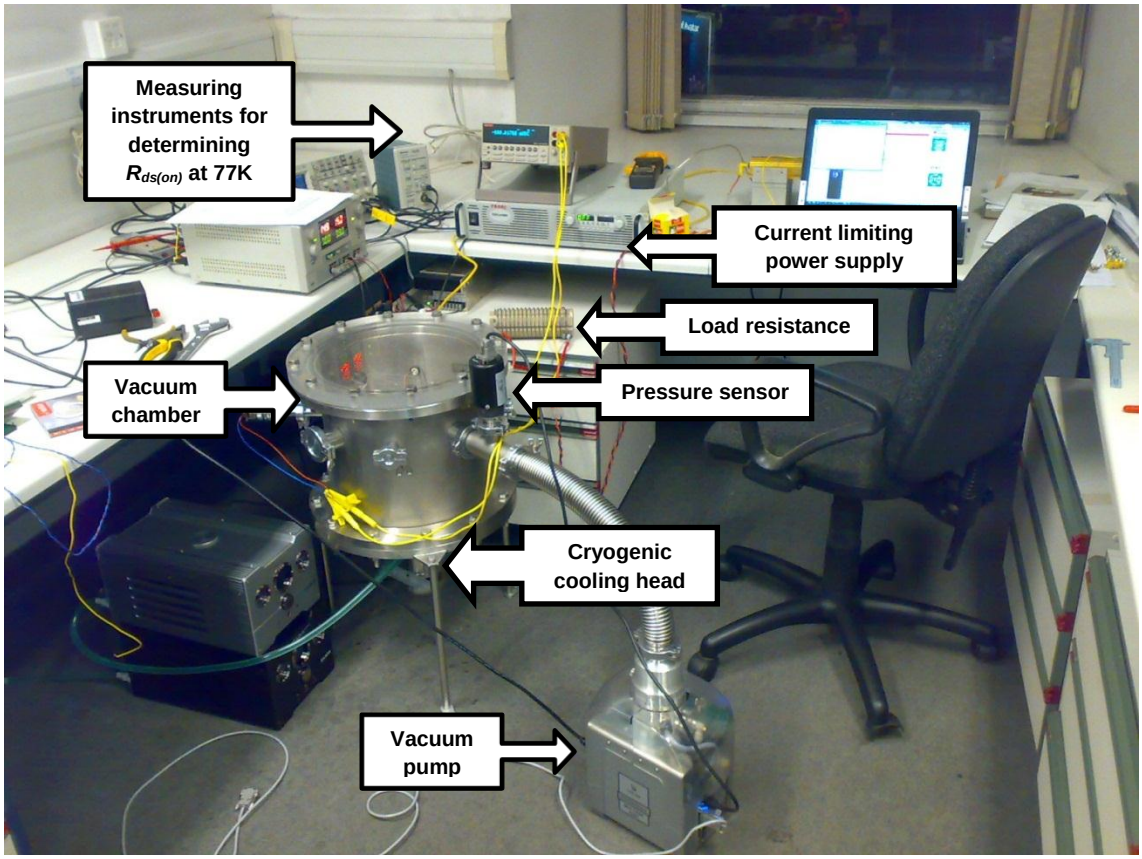


- Simulink model block diagram:



Appendix B: Cryogenic Operation of MOSFETs

B1. Cryogenic testing system:



Note: Devices are first tested at room temperature to verify the on-resistance quoted in the device datasheet, and verify that no measurement errors are obtained.

B2. MOSFET device testing at 77K (detailed experimental results):

- Device 1: STP4N150 (1500V, 4A)

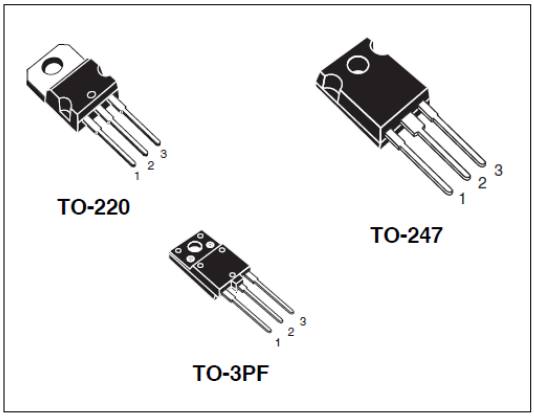
STFW4N150
STP4N150, STW4N150

N-channel 1500 V, 5 Ω, 4 A, PowerMESH™ Power MOSFET
in TO-220, TO-247, TO-3PF

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D	Pw
STFW4N150	1500 V	< 7 Ω	4 A	63 W
STP4N150	1500 V	< 7 Ω	4 A	160 W
STW4N150	1500 V	< 7 Ω	4 A	160 W

- 100% avalanche tested
- Intrinsic capacitances and Qg minimized
- High speed switching
- Fully isolated TO-3PF plastic packages
- Creepage distance path is 5.4 mm (typ.) for TO-3PF



Application

- Switching applications

Description

Using the well consolidated high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of very high voltage Power MOSFETs with outstanding performances. The strengthened layout coupled with the company's proprietary edge termination structure, gives the lowest $R_{DS(on)}$ per area, unrivalled gate charge and switching characteristics.

Figure 1. Internal schematic diagram.

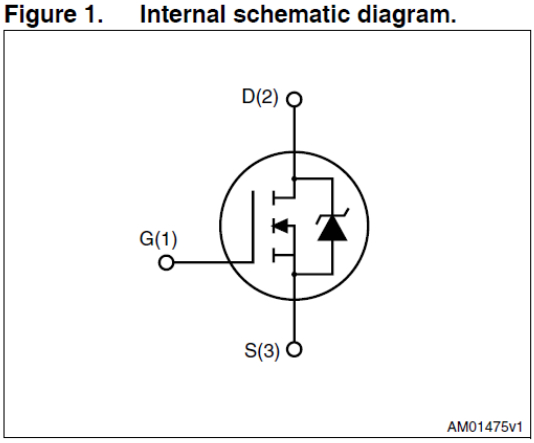


Table 1. Device summary

Order codes	Marking	Package	Packaging
STFW4N150	4N150	TO-3PF	Tube
STP4N150	P4N150	TO-220	Tube
STW4N150	W4N150	TO-247	Tube

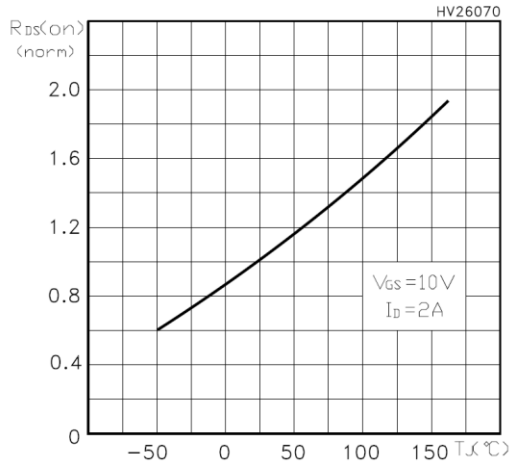


Figure B1: Normalized device on-resistance versus junction temperature

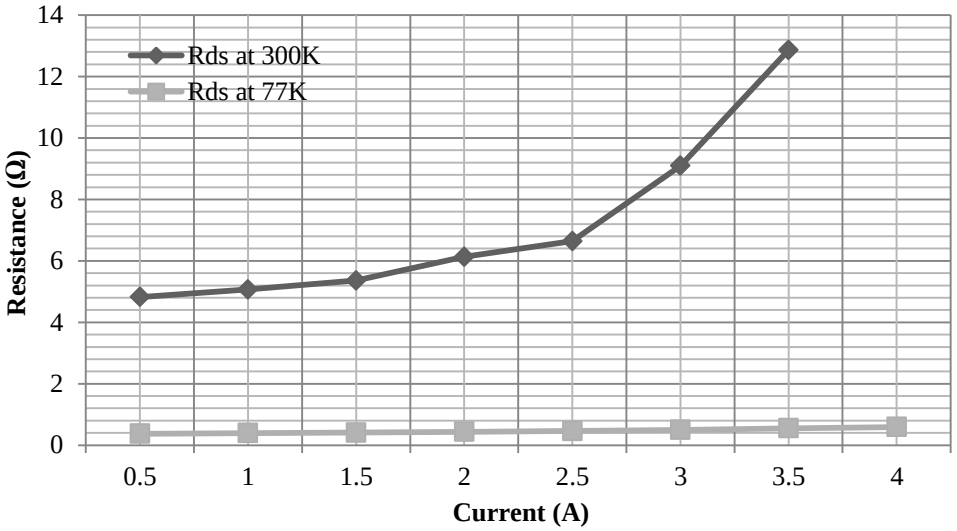


Figure B2: On-resistance measurements obtained by experimental results at 300K and 77K

Table B1: On-resistance at 400K, 77K, and the obtained reduction factor

$R_{ds(on)}$ at 400K	7.5 Ω
$R_{ds(on)}$ at 77K	0.3744 Ω
Reduction factor (F)	20.03

- Device 2: 2SK3745LS (1500V, 2A)

SANYO Semiconductors
DATA SHEET

2SK3745LS — N-Channel Silicon MOSFET High-Voltage, High-Speed Switching Applications

Features

- Low ON-resistance, low input capacitance, ultrahigh-speed switching.
- High reliability (Adoption of HVP process).
- Micaless package facilitating mounting.
- Avalanche resistance guarantee.

Specifications

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DSS}		1500	V
Gate-to-Source Voltage	V_{GSS}		±20	V
Drain Current (DC)	I_D*		2	A
Drain Current (Pulse)	I_{DP}		4	A
Allowable Power Dissipation	P_D		2.0	W
		Tc=25°C	35	W
Channel Temperature	Tch		150	°C
Storage Temperature	Tstg		-55 to +150	°C
Avalanche Energy (Single Pulse) *1	E_{AS}		42	mJ
Avalanche Current *2	I_{AV}		2	A

*Shows chip capability

*1 V_{DD}=99V, L=20mH, I_{AV}=2A

*2 L≤20mH, single pulse

Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=1mA, V_{GS}=0V	1500			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=1200V, V_{GS}=0V			100	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}= ±16V, V_{DS}=0V			±10	μA
Cutoff Voltage	$V_{GS(off)}$	V_{DS}=10V, I_D=1mA	2.5		3.5	V
Forward Transfer Admittance	|yfs|	V_{DS}=20V, I_D=1A	0.7	1.4		S
Static Drain-to-Source On-State Resistance	$R_{DS(on)}$	I_D=1A, V_{GS}=10V		10	13	Ω

Marking : K3745

Continued on next page.

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

N1505QB MS IM TB-00001890 No.8635-1/4

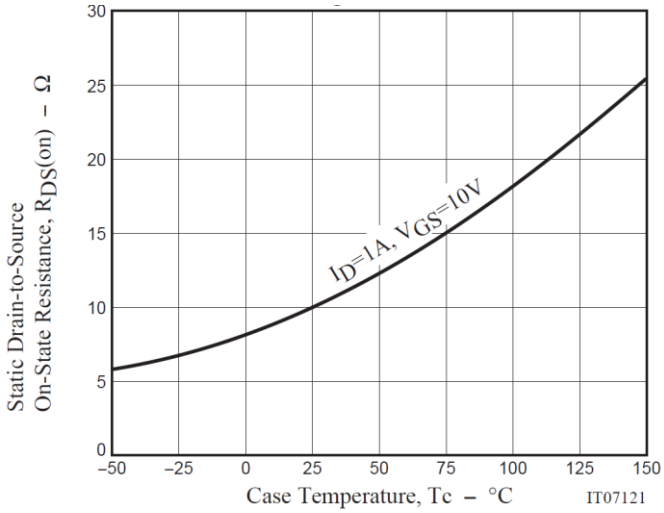


Figure B3: Normalized device on-resistance versus junction temperature

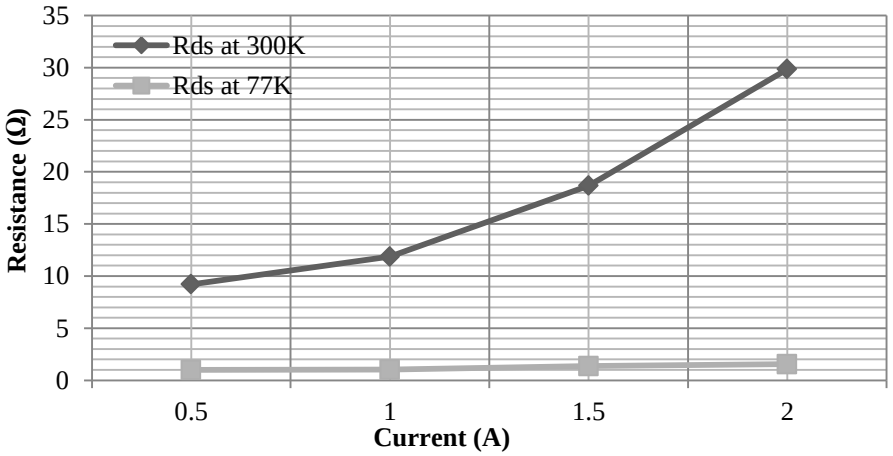


Figure B4: On-resistance measurements obtained by experimental results at 300K and 77K

Table B2: On-resistance at 400K, 77K, and the obtained reduction factor

$R_{ds(on)}$ at 400K	18.5 Ω
$R_{ds(on)}$ at 77K	1.0286 Ω
Reduction factor (F)	17.98

- Device 3: IXFK20N120 (1200V, 20A)

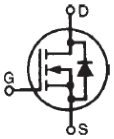
IXYS **Advanced Technical Information**

HiPerFET™ Power MOSFETs

IXFK 20N120
IXFX 20N120

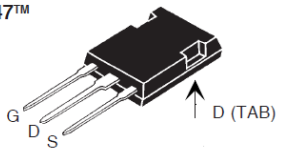
V_{DSS} = 1200 V
I_{D25} = 20 A
$R_{DS(on)}$ = 0.75 Ω

$t_{rr} \leq 300$ ns

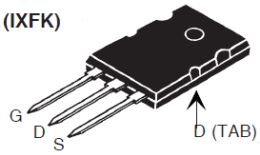


Symbol	Test Conditions		Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C		1200	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ		1200	V
V_{GS}	Continuous		±30	V
V_{GSM}	Transient		±40	V
I_{D25}	T_C = 25°C		20	A
I_{DM}	T_C = 25°C, Note 1		80	A
I_{AR}	T_C = 25°C		10	A
E_{AR}	T_C = 25°C		40	mJ
E_{AS}	T_C = 25°C		2	J
dv/dt	$I_S \leq I_{DM}$, di/dt ≤ 100 A/µs, $V_{DD} \leq V_{DSS}$ $T_J \leq 150$°C, R_G = 2 Ω		5	V/ns
P_D	T_C = 25°C		780	W
T_J			-55 ... +150	°C
T_{JM}			150	°C
T_{stg}			-55 ... +150	°C
T_L	1.6 mm (0.063 in.) from case for 10 s		300	°C
M_d	Mounting torque	TO-264	0.9/6	Nm/lb.in.
Weight		PLUS 247		6 g
		TO-264		10 g

PLUS 247™ (IXFX)



TO-264 AA (IXFK)



G = Gate D = Drain
S = Source TAB = Drain

Features
- International standard packages
- Low $R_{DS(on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
  - easy to drive and to protect
- Fast intrinsic rectifier

Applications
- DC-DC converters
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- AC motor control
- Temperature and lighting controls

Advantages
- PLUS 247™ package for clip or spring mounting
- Space savings
- High power density

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_{DSS}	V_{GS} = 0 V, I_D = 1mA		1200			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 8mA		2.5		4.5	V
I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0				±100	nA
I_{DSS}	$V_{DS} = V_{DSS}$ V_{GS} = 0 V	T_J = 25°C			100	µA
		T_J = 125°C			2	mA
$R_{DS(on)}$	V_{GS} = 10 V, $I_D = 0.5 \bullet I_{D25}$ Note 2				0.75	Ω

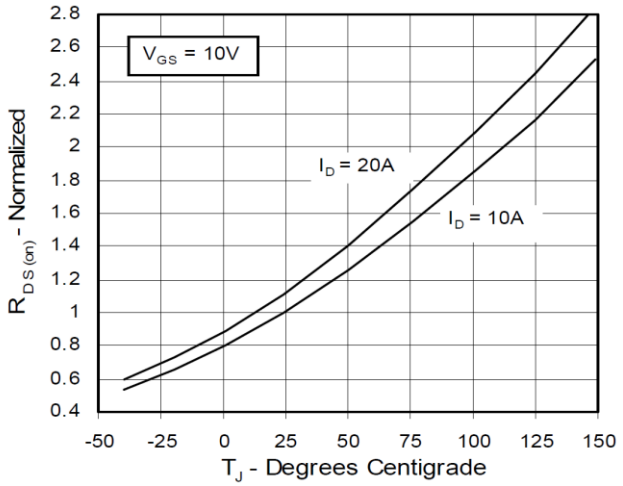


Figure B5: Normalized device on-resistance versus junction temperature

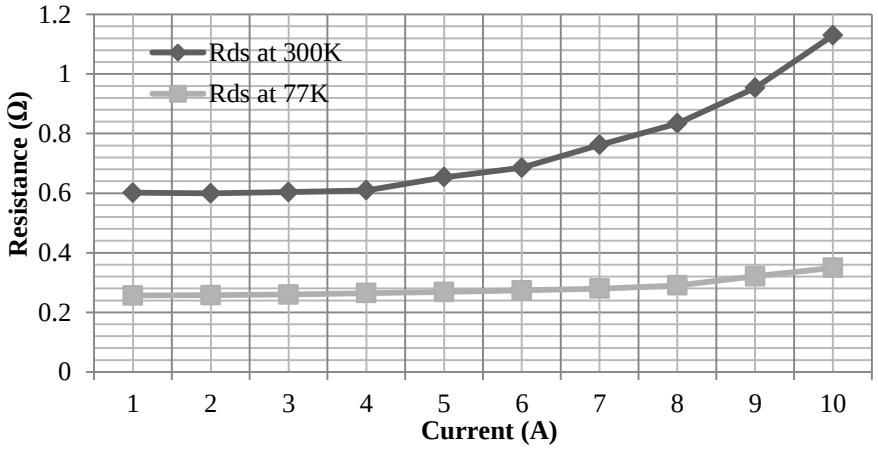


Figure B6: On-resistance measurements obtained by experimental results at 300K and 77K

Table B3: On-resistance at 400K, 77K, and the obtained reduction factor

$R_{ds(on)}$ at 400K	1.39 Ω
$R_{ds(on)}$ at 77K	0.2567 Ω
Reduction factor (F)	5.41

- FQA11N90C (900V, 11A):

FAIRCHILD
SEMICONDUCTOR®

FQA11N90C

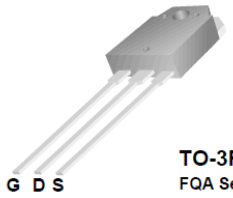
900V N-Channel MOSFET

General Description

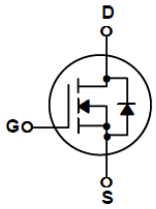
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies.

Features

- 11A, 900V, $R_{DS(on)}$ = 1.1Ω @V_{GS} = 10 V
- Low gate charge (typical 60 nC)
- Low Crss (typical 23 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



TO-3P
FQA Series



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter		FQA11N90C	Units
V_{DSS}	Drain-Source Voltage		900	V
I_D	Drain Current - Continuous (T_C = 25°C)		11.0	A
	- Continuous (T_C = 100°C)		6.9	A
I_{DM}	Drain Current - Pulsed	(Note 1)	44.0	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	960	mJ
I_{AR}	Avalanche Current	(Note 1)	11.0	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	30	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.0	V/ns
P_D	Power Dissipation (T_C = 25°C)		300	W
	- Derate above 25°C		2.38	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	0.42	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink	0.24	--	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	40	°C/W

Rev. A, December 2002

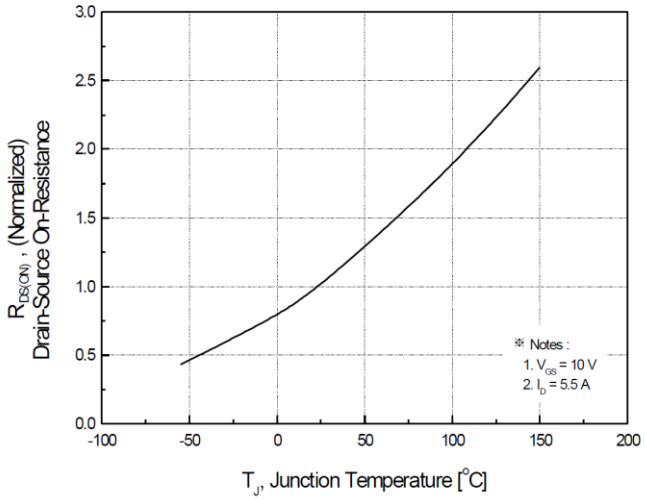


Figure B7: Normalized device on-resistance versus junction temperature

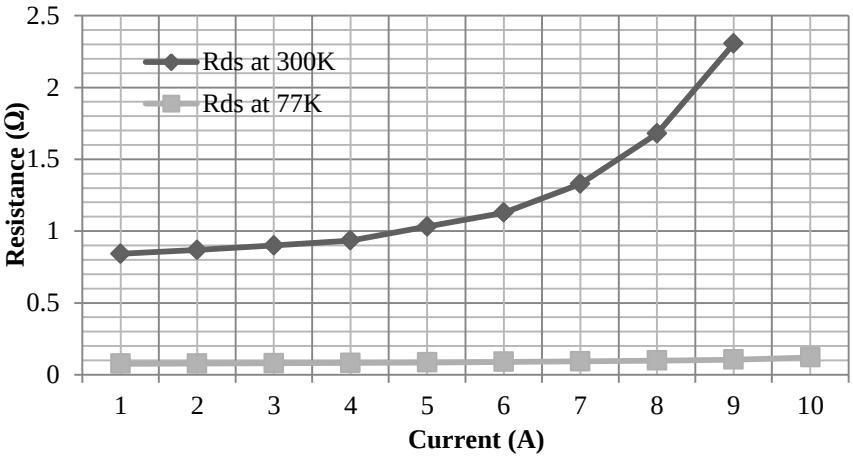


Figure B8: On-resistance measurements obtained by experimental results at 300K and 77K

Table B4: On-resistance at 400K, 77K, and the obtained reduction factor

$R_{ds(on)}$ at 400K	2.09 Ω
$R_{ds(on)}$ at 77K	0.07643 Ω
Reduction factor (F)	27.34

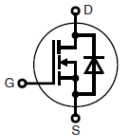
- Device 5: IXKC25N80 (800V, 25A)

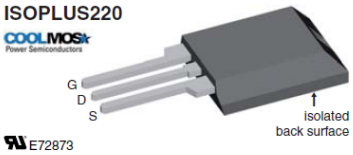
IXYS **IXKC 25N80C**

CoolMOS™ [1] Power MOSFET ISOPLUS™ Package

N-Channel Enhancement Mode
Low R_{DSon}, high V_{DSS} MOSFET
Electrically Isolated Back Surface

I_{D25} = 25 A
V_{DSS} = 800 V
$R_{DS(on)\ max}$ = 150 mΩ





MOSFET			
Symbol	**Conditions**	**Maximum Ratings**	
V_{DSS}	T_{VJ} = 25°C	800	V
V_{GS}		± 20	V
I_{D25} I_{D90}	T_C = 25°C T_C = 90°C	25 18	A A
E_{AS} E_{AR}	$T_{J\,start}$ = 25°C; single pulse; I_D = 3.4 A $T_{J\,start}$ = 25°C; repetitive; I_D = 17 A	670 0.5	mJ mJ
dV/dt	$V_{DS} < V_{DSS}$; I_F = 35 A; T_{VJ} = 150°C d_{iR}/dt = 100 A/µs	6	V/ns

Symbol	Conditions		Characteristic Values (T_{VJ} = 25°C, unless otherwise specified) min.	typ.	max.	
R_{DSon}	V_{GS} = 10 V; I_D = I_{D90}			135	150	mΩ
$V_{GS(th)}$	V_{DS} = V_{GS}; I_D = 2 mA		2		4	V
I_{DSS}	V_{DS} = V_{DSS}; V_{GS} = 0 V	T_{VJ} = 25°C T_{VJ} = 125°C			50 250	µA µA
I_{GSS}	V_{GS} = ± 20 V; V_{DS} = 0 V				±200	nA
C_{iss} C_{oss} C_{rss}	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz			4600 2500 120		pF pF pF
Q_g Q_{gs} Q_{gd}	V_{GS} = 0 to 10 V; V_{DS} = 640 V; I_D = I_{D90}			180 20 80		nC nC nC
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	V_{GS} = 10 V; V_{DS} = 640 V; T_{VJ} = 125°C I_D = 35 A; R_G = 2.2 Ω			25 25 75 10		ns ns ns ns
R_{thJC}					0.5	K/W

Features

- Silicon chip on Direct-Copper-Bond substrate
  - high power dissipation
  - isolated mounting surface
  - 2500 V electrical isolation
- 3rd generation CoolMOS™ [1] power MOSFET
  - high blocking capability
  - lowest resistance
  - avalanche rated for unclamped inductive switching (UIS)
- Low thermal resistance due to reduced chip thickness
- Low drain to tab capacitance (<30 pF)

Applications

- Switched mode power supplies (SMPS)
- Uninterruptible power supplies (UPS)
- Power factor correction (PFC)
- Welding
- Inductive heating

Advantages

- Easy assembly: no screws or isolation foils required
- Space savings
- High power density

[1] CoolMOS™ is a trademark of Infineon Technologies AG.

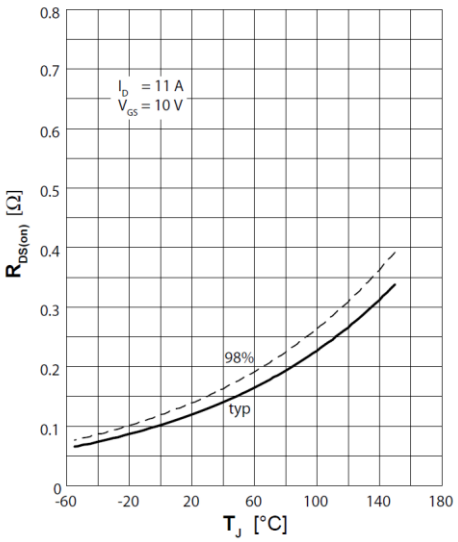


Figure B9: Normalized device on-resistance versus junction temperature

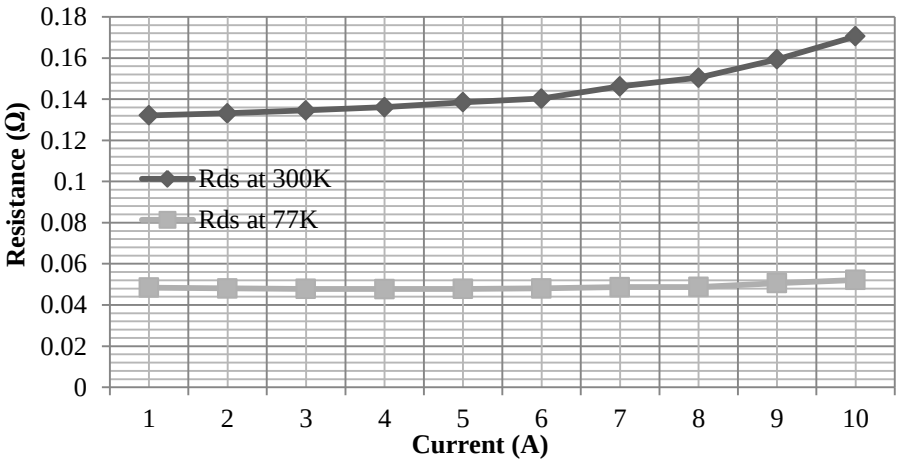


Figure B10: On-resistance measurements obtained by experimental results at 300K and 77K

Table B5: On-resistance at 400K, 77K, and the obtained reduction factor

$R_{ds(on)}$ at 400K	0.225 Ω
$R_{ds(on)}$ at 77K	0.0484 Ω
Reduction factor (F)	4.6

- Device 6: IPP60R299 (650V, 11A)

CoolMOS™ Power Transistor

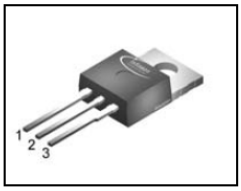
Features

- Lowest figure-of-merit $R_{ON}xQ_g$
- Ultra low gate charge
- Extreme dv/dt rated
- High peak current capability
- Qualified according to JEDEC[1] for target applications
- Pb-free lead plating; RoHS compliant

Product Summary

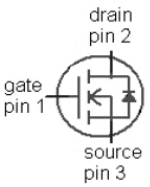
V_{DS} @ $T_{j,max}$	650	V
$R_{DS(on),max}$	0.299	Ω
$Q_{g,typ}$	22	nC

PG-TO220



CoolMOS CP is specially designed for:

Hard switching SMPS topologies



Type	Package	Ordering Code	Marking
IPP60R299CP	PG-TO220	SP000084280	6R299P

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C	11	A
		T_C=100 °C	7	
Pulsed drain current[2]	$I_{D,pulse}$	T_C=25 °C	34	
Avalanche energy, single pulse	E_{AS}	I_D=4.4 A, V_{DD}=50 V	290	mJ
Avalanche energy, repetitive t_{AR}[2),3)]	E_{AR}	I_D=4.4 A, V_{DD}=50 V	0.44	
Avalanche current, repetitive t_{AR}[2),3)]	I_{AR}		4.4	A
MOSFET dv/dt ruggedness	dv/dt	V_{DS}=0...480 V	50	V/ns
Gate source voltage	V_{GS}	static	±20	V
		AC (f>1 Hz)	±30	
Power dissipation	P_{tot}	T_C=25 °C	96	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
Mounting torque		M3 and M3.5 screws	60	Ncm

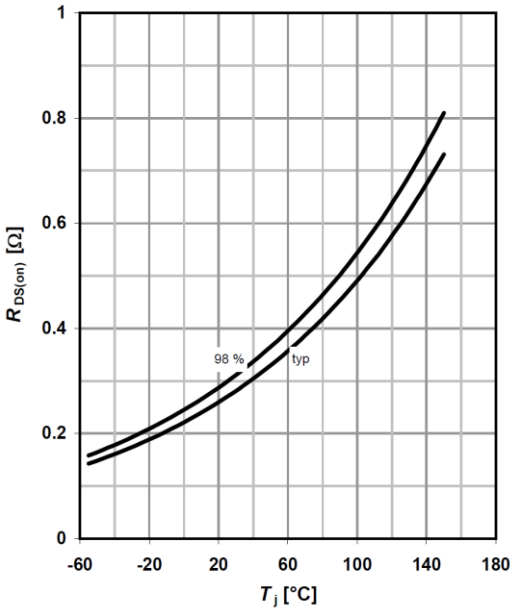


Figure B11: Normalized device on-resistance versus junction temperature

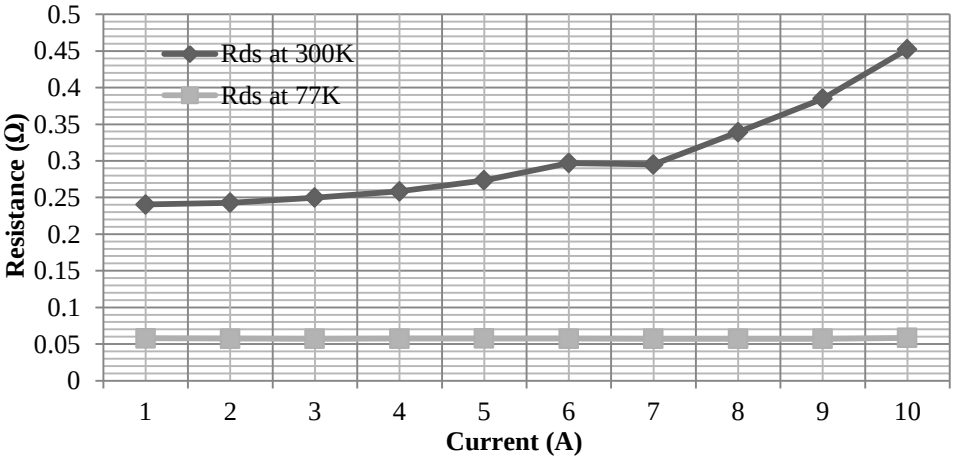


Figure B12: On-resistance measurements obtained by experimental results at 300K and 77K

Table B6: On-resistance at 400K, 77K, and the obtained reduction factor

$R_{ds(on)}$ at 400K	0.49 Ω
$R_{ds(on)}$ at 77K	0.05775 Ω
Reduction factor (F)	8.48

- Device 7: FQP5N50 (500V, 5A)

FAIRCHILD SEMICONDUCTOR®

QFET™

FQP5N50C/FQPF5N50C

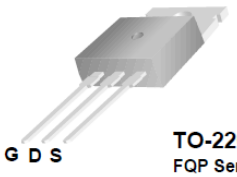
500V N-Channel MOSFET

General Description

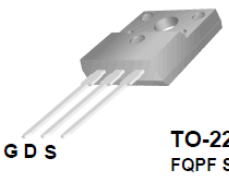
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology.

Features

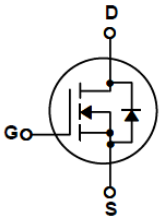
- 5A, 500V, $R_{DS(on)}$ = 1.4 Ω @V_{GS} = 10 V
- Low gate charge (typical 18nC)
- Low Crss (typical 15pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



TO-220
FQP Series



TO-220F
FQPF Series



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter		FQP5N50C	FQPF5N50C	Units
V_{DSS}	Drain-Source Voltage		500		V
I_D	Drain Current - Continuous (T_C = 25°C)		5	5 *	A
	- Continuous (T_C = 100°C)		2.9	2.9 *	A
I_{DM}	Drain Current - Pulsed	(Note 1)	20	20 *	A
V_{GSS}	Gate-Source Voltage		± 30		V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	300		mJ
I_{AR}	Avalanche Current	(Note 1)	5		A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	7.3		mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5		V/ns
P_D	Power Dissipation (T_C = 25°C)		73	38	W
	- Derate above 25°C		0.58	0.3	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300		°C

* Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FQP5N50C	FQPF5N50C	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.71	3.31	°C/W
$R_{\theta JS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	°C/W

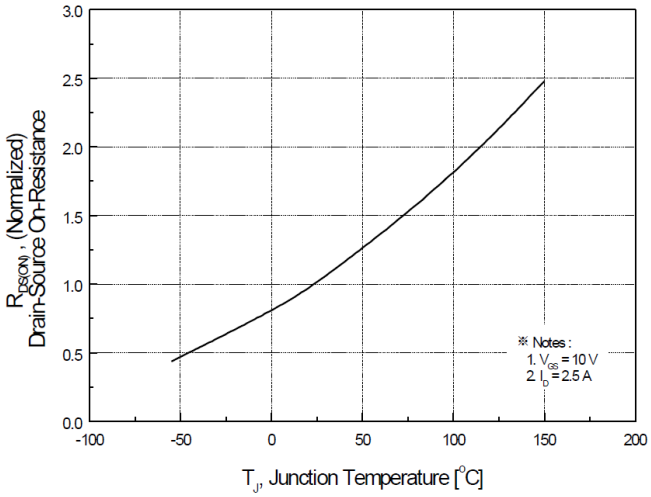


Figure B13: Normalized device on-resistance versus junction temperature

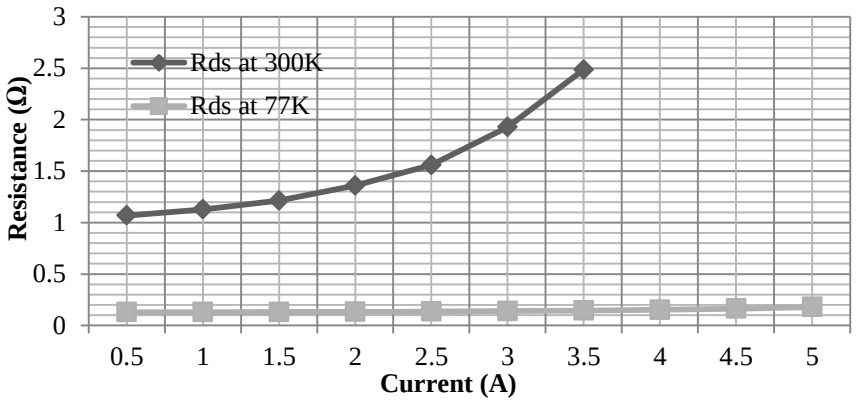


Figure B14: On-resistance measurements obtained by experimental results at 300K and 77K

Table B7: On-resistance at 400K, 77K, and the obtained reduction factor

$R_{ds(on)}$ at 400K	2.52 Ω
$R_{ds(on)}$ at 77K	0.1285 Ω
Reduction factor (F)	19.61

- Device 8: IRFP340 (400V, 11A)

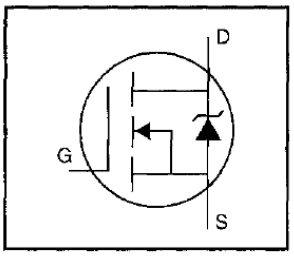
International
IOR Rectifier

PD-9.456C

IRFP340

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



V_{DSS} = 400V

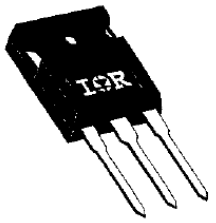
$R_{DS(on)}$ = 0.55Ω

I_D = 11A

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247 package is preferred for commercial–industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole. It also provides greater creepage distance between pins to meet the requirements of most safety specifications.



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10 V	11	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10 V	6.9	
I_{DM}	Pulsed Drain Current ①	44	
P_D @ T_C = 25°C	Power Dissipation	150	W
	Linear Derating Factor	1.2	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	480	mJ
I_{AR}	Avalanche Current ①	11	A
E_{AR}	Repetitive Avalanche Energy ①	15	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	0.83	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	40	

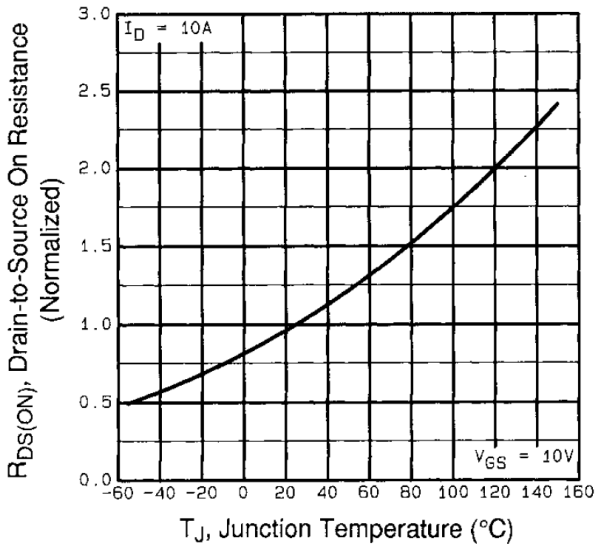


Figure B15: Normalized device on-resistance versus junction temperature

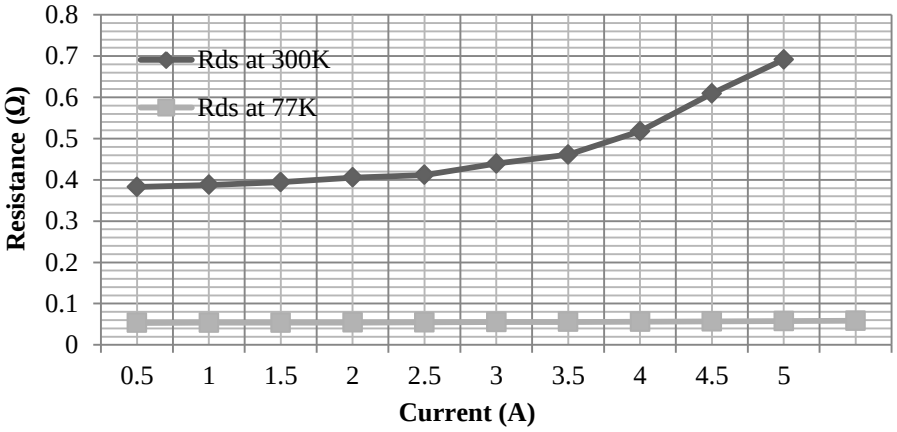


Figure B16: On-resistance measurements obtained by experimental results at 300K and 77K

Table B8: On-resistance at 400K, 77K, and the obtained reduction factor

$R_{ds(on)}$ at 400K	0.9625 Ω
$R_{ds(on)}$ at 77K	0.05301 Ω
Reduction factor (F)	18.16

- Device 9: FDPF33N25 (250V, 22A)

FAIRCHILD SEMICONDUCTOR®

May 2006

UniFET™

FDPF33N25

250V N-Channel MOSFET

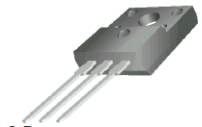
Features

- 20A, 250V, $R_{DS(on)}$ = 0.094Ω @V_{GS} = 10 V
- Low gate charge (typical 36.8 nC)
- Low C_{rss} (typical 39 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

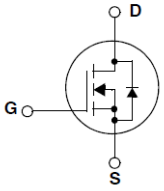
Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.



TO-220F
FDPF Series



Absolute Maximum Ratings

Symbol	Parameter		FDPF33N25	Unit
V_{DSS}	Drain-Source Voltage		250	V
I_D	Drain Current - Continuous (T_C = 25°C) - Continuous (T_C = 100°C)		20 12	A A
I_{DM}	Drain Current - Pulsed	(Note 1)	80	A
V_{GSS}	Gate-Source voltage		±30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	918	mJ
I_{AR}	Avalanche Current	(Note 1)	20	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	9.4	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P_D	Power Dissipation (T_C = 25°C) - Derate above 25°C		94 0.76	W W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Min.	Max.	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	1.32	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	°C/W

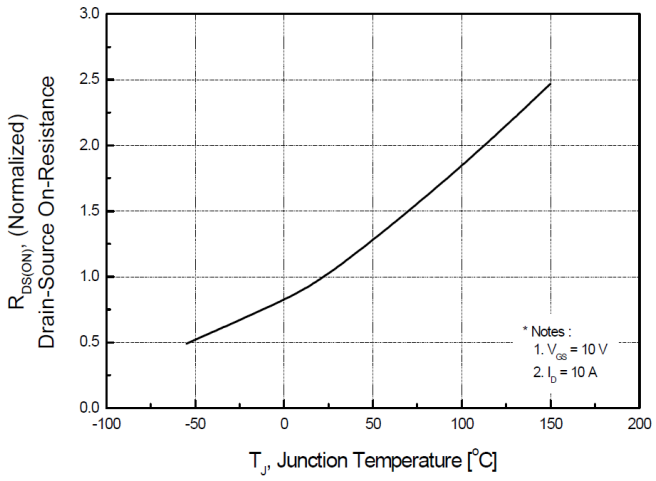


Figure B17: Normalized device on-resistance versus junction temperature

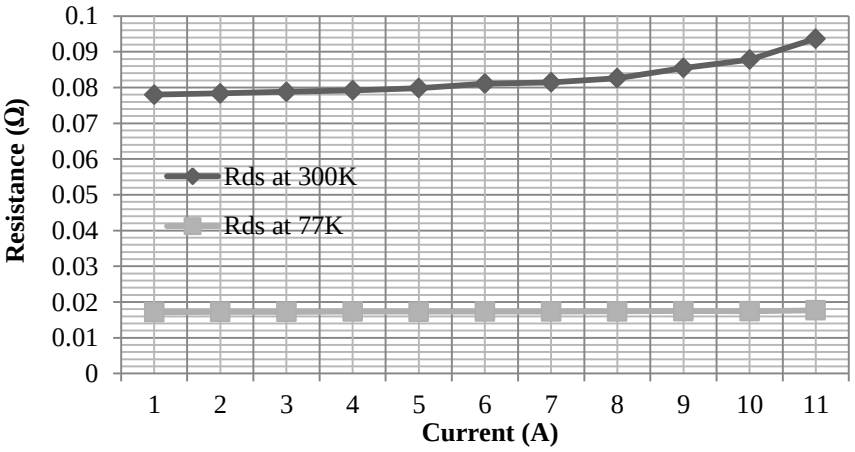


Figure B18: On-resistance measurements obtained by experimental results at 300K and 77K

Table B9: On-resistance at 400K, 77K, and the obtained reduction factor

$R_{ds(on)}$ at 400K	0.1739 Ω
$R_{ds(on)}$ at 77K	0.01716 Ω
Reduction factor (F)	10.13

- Device 10: IRFP4668 (200V, 130A)

International
IOR Rectifier

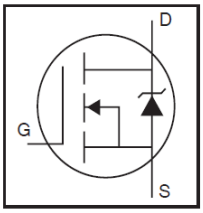
PD -97140

IRFP4668PbF

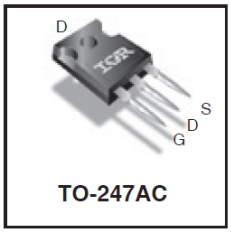
HEXFET® Power MOSFET

Applications
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free



V_{DSS}	200V
$R_{DS(on)}$ typ.	8.0mΩ
max.	9.7mΩ
I_D	130A



TO-247AC

G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	130	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	92	
I_{DM}	Pulsed Drain Current ①	520	
P_D @T_C = 25°C	Maximum Power Dissipation	520	W
	Linear Derating Factor	3.5	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery ③	57	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Avalanche Characteristics

$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ②	760	mJ
I_{AR}	Avalanche Current ①	See Fig. 14, 15, 22a, 22b,	A
E_{AR}	Repetitive Avalanche Energy ④		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	—	0.29	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient ⑦⑧	—	40	

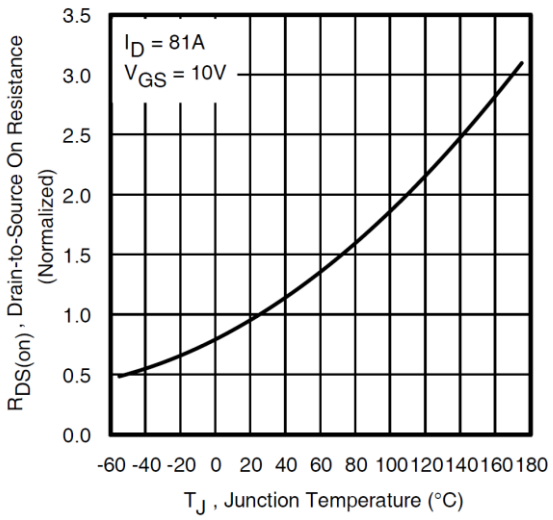


Figure B19: Normalized device on-resistance versus junction temperature

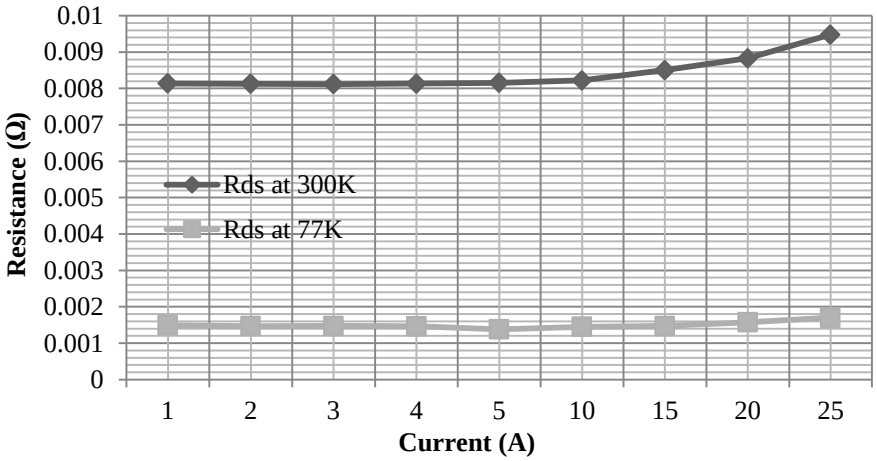


Figure B20: On-resistance measurements obtained by experimental results at 300K and 77K

Table B10: On-resistance at 400K, 77K, and the obtained reduction factor

$R_{ds(on)}$ at 400K	14.4 mΩ
$R_{ds(on)}$ at 77K	2.064 mΩ
Reduction factor (F)	9.62

- Device 11: IRF510 (100V, 56A)

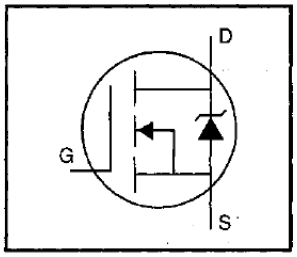
International
IOR Rectifier

PD-9.325Q

IRF510

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- 175°C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



V_{DSS} = 100V

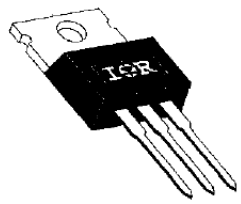
$R_{DS(on)}$ = 0.54Ω

I_D = 5.6A

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10 V	5.6	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10 V	4.0	
I_{DM}	Pulsed Drain Current ①	20	
P_D @ T_C = 25°C	Power Dissipation	43	W
	Linear Derating Factor	0.29	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	100	mJ
I_{AR}	Avalanche Current ①	5.6	A
E_{AR}	Repetitive Avalanche Energy ①	4.3	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	3.5	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

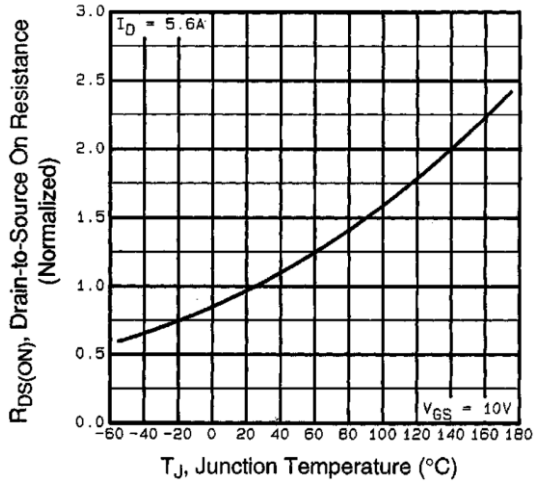


Figure B21: Normalized device on-resistance versus junction temperature

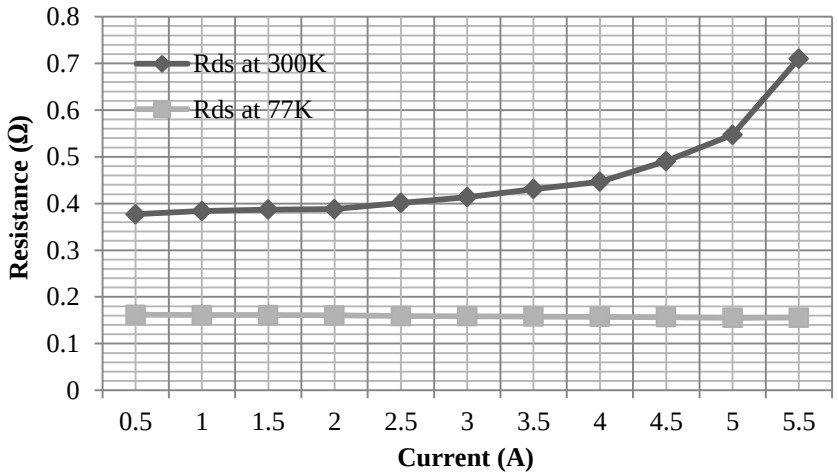


Figure B22: On-resistance measurements obtained by experimental results at 300K and 77K

Table B11: On-resistance at 400K, 77K, and the obtained reduction factor

$R_{ds(on)}$ at 400K	0.864 Ω
$R_{ds(on)}$ at 77K	0.1554 Ω
Reduction factor (F)	5.56

- Device 12: IRFB3207 (75V, 180A)

International
IOR Rectifier

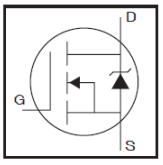
PD - 96893A

IRFB3207
IRFS3207
IRFSL3207

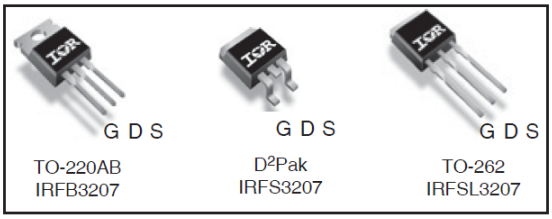
HEXFET® Power MOSFET

Applications
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits
- Worldwide Best $R_{DS(on)}$ in TO-220
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability



V_{DSS}		75V
$R_{DS(on)}$	typ.	3.6mΩ
	max.	4.5mΩ
I_D		180A



TO-220AB IRFB3207 | D²Pak IRFS3207 | TO-262 IRFSL3207

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	180①	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	130①	
I_{DM}	Pulsed Drain Current ②	720	
P_D @T_C = 25°C	Maximum Power Dissipation	330	W
	Linear Derating Factor	2.2	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dV/dt	Peak Diode Recovery ④	5.8	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Avalanche Characteristics

$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ③	910	mJ
I_{AR}	Avalanche Current ①	See Fig. 14, 15, 16a, 16b,	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑨	—	0.45	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface , TO-220	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, TO-220 ⑨	—	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) , D^2Pak ⑧⑨	—	40	

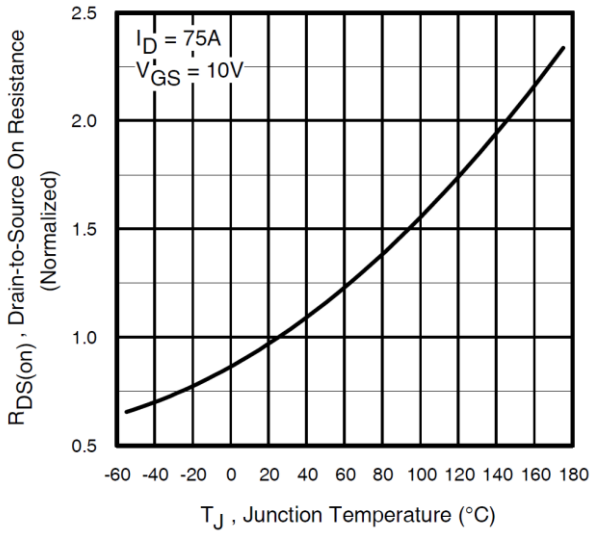


Figure B23: Normalized device on-resistance versus junction temperature

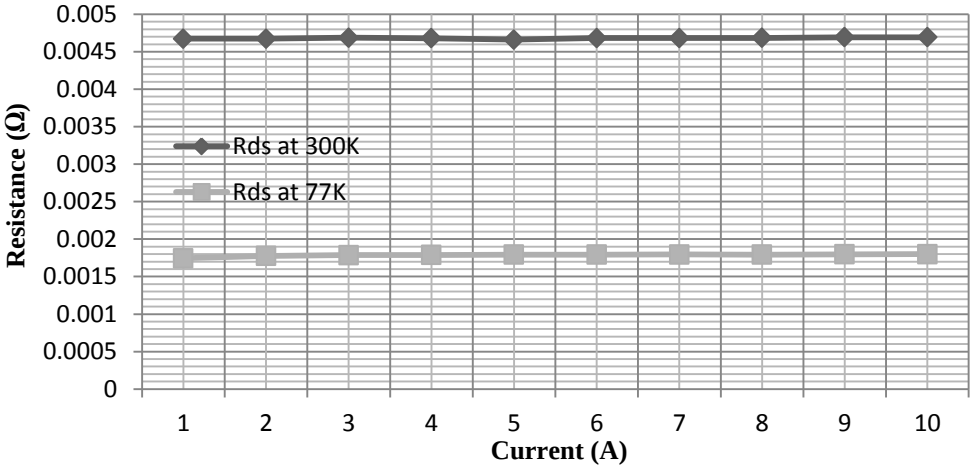


Figure B24: On-resistance measurements obtained by experimental results at 300K and 77K

Table B12: On-resistance at 400K, 77K, and the obtained reduction factor

$R_{ds(on)}$ at 400K	5.58 mΩ
$R_{ds(on)}$ at 77K	1.745 mΩ
Reduction factor (F)	3.19

- Device 13: IRLIZ34N (55V, 22A)

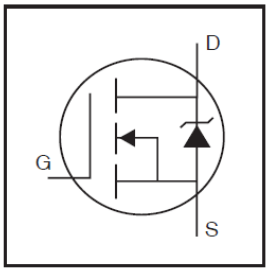
International
IOR Rectifier

PD - 95455

IRLIZ34NPbF

HEXFET® Power MOSFET

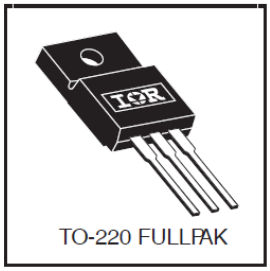
- Logic-Level Gate Drive
- Advanced Process Technology
- Isolated Package
- High Voltage Isolation = 2.5KVRMS ⑤
- Sink to Lead Creepage Dist. = 4.8mm
- Fully Avalanche Rated
- Lead-Free



V_{DSS} = 55V

$R_{DS(on)}$ = 0.035Ω

I_D = 22A



TO-220 FULLPAK

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	22	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	15	
I_{DM}	Pulsed Drain Current ⑤⑥	110	
P_D @T_C = 25°C	Power Dissipation	37	W
	Linear Derating Factor	0.24	W/°C
V_{GS}	Gate-to-Source Voltage	±16	V
E_{AS}	Single Pulse Avalanche Energy ②⑥	110	mJ
I_{AR}	Avalanche Current①⑥	16	A
E_{AR}	Repetitive Avalanche Energy①⑥	3.7	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑥	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	———	———	4.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient	———	———	65	

6/23/04

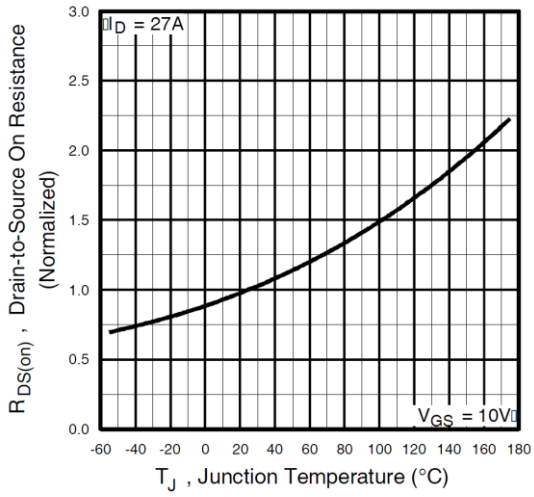


Figure B25: Normalized device on-resistance versus junction temperature

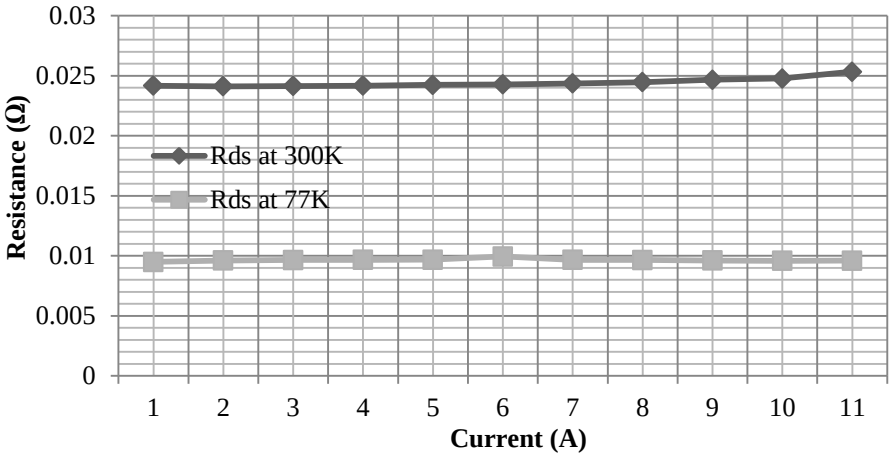


Figure B26: On-resistance measurements obtained by experimental results at 300K and 77K

Table B13: On-resistance at 400K, 77K, and the obtained reduction factor

$R_{ds(on)}$ at 400K	52.5 mΩ
$R_{ds(on)}$ at 77K	9.495 mΩ
Reduction factor (F)	5.53

- Device 14: IRF4004 (40V, 350A)

International
IOR Rectifier

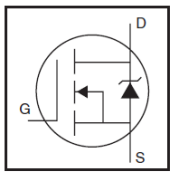
PD - 97323

IRFP4004PbF

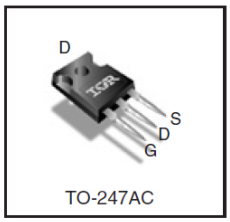
HEXFET® Power MOSFET

Applications
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability



V_{DSS}	40V
$R_{DS(on)}$ typ.	1.35mΩ
max.	1.70mΩ
$I_{D\ (Silicon\ Limited)}$	350A①
$I_{D\ (Package\ Limited)}$	195A



TO-247AC

G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, VGS @ 10V (Silicon Limited)	350①	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	250①	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Wire Bond Limited)	195	
I_{DM}	Pulsed Drain Current ②	1390	
P_D @T_C = 25°C	Maximum Power Dissipation	380	W
	Linear Derating Factor	2.5	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ④	2.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Avalanche Characteristics

$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ③	290	mJ
I_{AR}	Avalanche Current ②	See Fig. 14, 15, 22a, 22b	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑨	—	0.40	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient ⑧⑨	—	40	

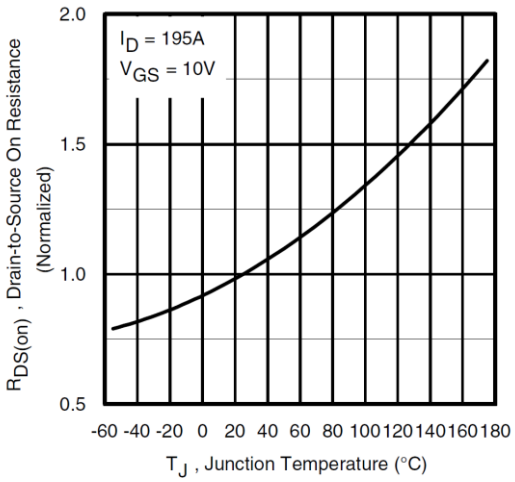


Figure B27: Normalized device on-resistance versus junction temperature

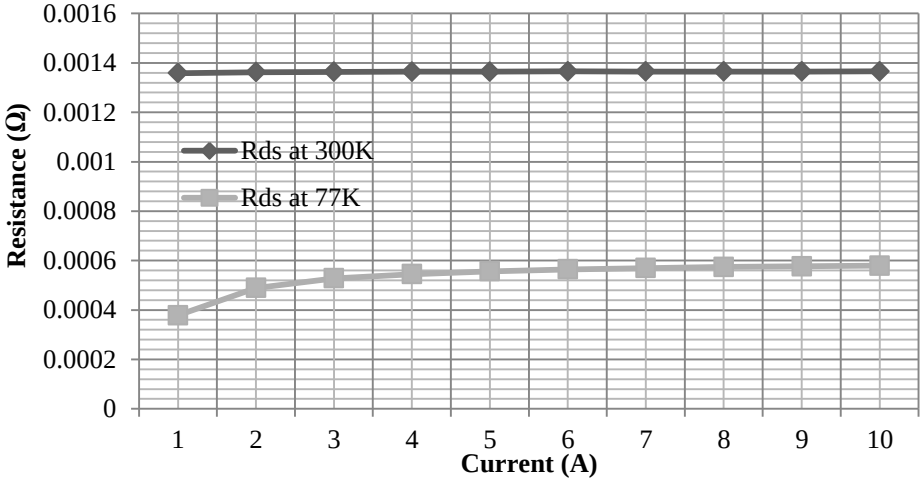


Figure B28: On-resistance measurements obtained by experimental results at 300K and 77K

Table B14: On-resistance at 400K, 77K, and the obtained reduction factor

$R_{ds(on)}$ at 400K	1.8225 mΩ
$R_{ds(on)}$ at 77K	0.489 mΩ
Reduction factor (F)	3.73

- Device 15: IRF1324S7 (24V, 429A)

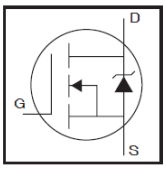
International
IOR Rectifier

PD - 97263

IRF1324S-7PPbF

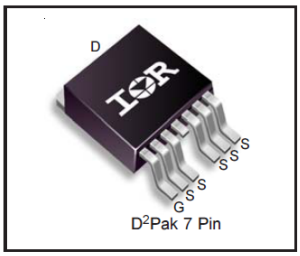
HEXFET® Power MOSFET

Applications
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits



V_{DSS}		24V
$R_{DS(on)}$	typ.	0.8mΩ
	max.	1.0mΩ
I_D		429A

Benefits
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free



D^2Pak 7 Pin

G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	429①	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	303①	
I_{DM}	Pulsed Drain Current ②	1640	
P_D @T_C = 25°C	Maximum Power Dissipation	300	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ④	1.6	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Avalanche Characteristics

$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ③	230	mJ
I_{AR}	Avalanche Current ①	See Fig. 14, 15, 22a, 22b,	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑨	—	0.50	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) , D^2Pak ⑧⑨	—	40	

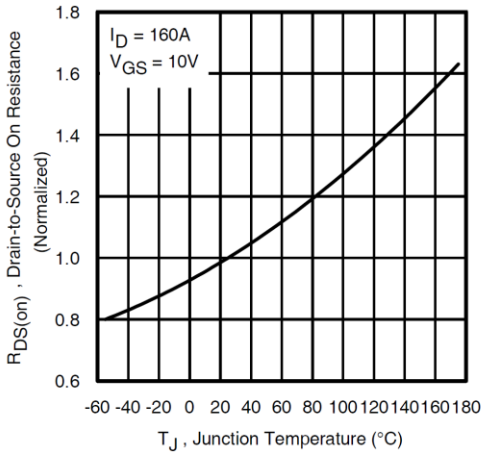


Figure B29: Normalized device on-resistance versus junction temperature

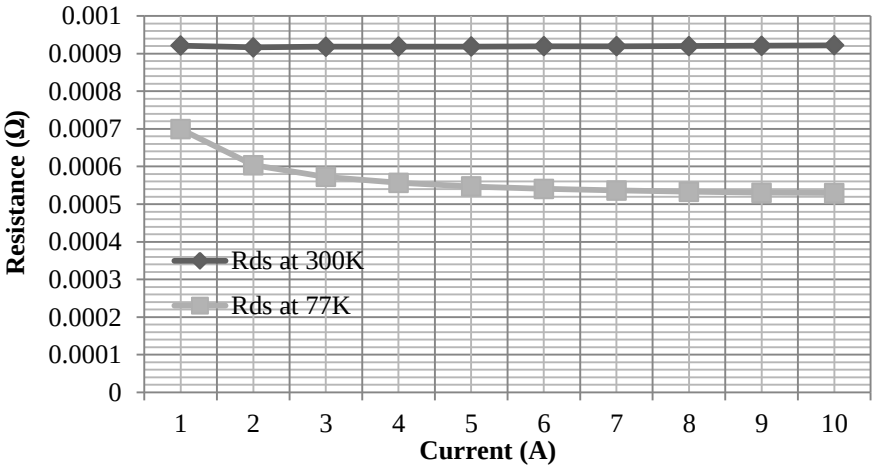


Figure B30: On-resistance measurements obtained by experimental results at 300K and 77K

Table B15: On-resistance at 400K, 77K, and the obtained reduction factor

$R_{ds(on)}$ at 400K	1.04 mΩ
$R_{ds(on)}$ at 77K	0.528 mΩ
Reduction factor (F)	1.96

Appendix C: Nanocrystalline Transformer Design Data

C1. The total m layer winding power loss due to skin and proximity effects:

The following analysis is given in reference [4.13]. Given that the copper power loss per layer, after solving Maxwell's equations to obtain the current density distribution, is:

$$P = R_{DC}\frac{t}{\delta N_l^{\,2}}\left\{\left[MMF^2(0)+MMF^2(t)\right]G_1 - 4MMF(0)\,MMF(t)G_2\right\}$$

where N_l is the number of turns in the layer, and R_{DC} is the DC resistance of the layer, and the functions G_1 and G_2 are:

$$G_1 = \frac{\sinh\left(\frac{2t}{\delta}\right)+\sin\left(\frac{2t}{\delta}\right)}{\cosh\left(\frac{2t}{\delta}\right)-\cos\left(\frac{2t}{\delta}\right)}$$

$$G_2 = \frac{\sinh\left(\frac{t}{\delta}\right)\cos\left(\frac{t}{\delta}\right)+\cosh\left(\frac{t}{\delta}\right)\sin\left(\frac{t}{\delta}\right)}{\cosh\left(\frac{2t}{\delta}\right)-\cos\left(\frac{2t}{\delta}\right)}$$

For a winding carrying a current of *I*:

$$MMF(t) - MMF(0) = N_l I$$

Defining m as the ratio of the *MMF* at *t* to the layer ampere-turns $N_l I$, hence:

$$\frac{MMF(0)}{MMF(t)} = \frac{m-1}{m}$$

The power dissipated in the layer is then:

$$P = I^2 R_{DC}\frac{t}{\delta}\left[\left(2m^2-2m+1\right)G_1 - 4m\left(m-1\right)G_2\right]$$

And the resistance ratio due to skin and proximity effects is:

$$F_R = \frac{P}{P_{DC}} = \frac{t}{\delta}\left[\left(2m^2-2m+1\right)G_1 - 4m\left(m-1\right)G_2\right]$$

The total increase in winding resistance for M layers is:

$$F_R = \frac{1}{M}\sum_{m=1}^{M}\left(\frac{t}{\delta}\left[\left(2m^2-2m+1\right)G_1 - 4m\left(m-1\right)G_2\right]\right)$$

$$= \frac{1}{M}\frac{t}{\delta}\sum_{m=1}^{M}\left(m^2\left(2G_1-4G_2\right) - m\left(2G_1-4G_2\right)+G_1\right)$$

The summation can be expressed in closed form, with help of the identities:

$$\sum_{m=1}^{M} M = \frac{M(M+1)}{2}$$

$$\sum_{m=1}^{M} M^2 = \frac{M(M+1)(2M+1)}{6}$$

which leads to:

$$F_R = \frac{t}{\delta}\left(G_1 + \frac{2}{3}(M^2-1)\left(G_1-2G_2\right)\right)$$

For the term $\left(G_1-2G_2\right)$:

$$G_1 - 2G_2 = \frac{\sinh\left(\frac{2t}{\delta}\right)+\sin\left(\frac{2t}{\delta}\right)}{\cosh\left(\frac{2t}{\delta}\right)-\cos\left(\frac{2t}{\delta}\right)} - 2\frac{\sinh\left(\frac{t}{\delta}\right)\cos\left(\frac{t}{\delta}\right)+\cosh\left(\frac{t}{\delta}\right)\sin\left(\frac{t}{\delta}\right)}{\cosh\left(\frac{2t}{\delta}\right)-\cos\left(\frac{2t}{\delta}\right)}$$

$$= \frac{\sinh\left(\frac{2t}{\delta}\right)+\sin\left(\frac{2t}{\delta}\right)-2\sinh\left(\frac{t}{\delta}\right)\cos\left(\frac{t}{\delta}\right)-2\cosh\left(\frac{t}{\delta}\right)\sin\left(\frac{t}{\delta}\right)}{\cosh\left(\frac{2t}{\delta}\right)-\cos\left(\frac{2t}{\delta}\right)}$$

By using the following trigonometric relations:

$$\cosh(2a) = 2\cosh^2(a)-1$$

$$\cos^2(2a) = 2\cos^2(a)-1$$

$$2\sinh(a)\cosh(a) = \sinh(2a)$$

$$2\sin(a)\cos(a) = \sin(2a)$$

$$\therefore G_1 - 2G_2 = \frac{2\sinh\left(\frac{t}{\delta}\right)\cosh\left(\frac{t}{\delta}\right) + 2\sin\left(\frac{t}{\delta}\right)\cos\left(\frac{t}{\delta}\right) - 2\sinh\left(\frac{t}{\delta}\right)\cos\left(\frac{t}{\delta}\right) - 2\cosh\left(\frac{t}{\delta}\right)\sin\left(\frac{t}{\delta}\right)}{2\cosh^2\left(\frac{t}{\delta}\right) - 1 - 2\cos^2\left(\frac{t}{\delta}\right) + 1}$$

$$= \frac{\sinh\left(\frac{t}{\delta}\right)\cosh\left(\frac{t}{\delta}\right) + \sin\left(\frac{t}{\delta}\right)\cos\left(\frac{t}{\delta}\right) - \sinh\left(\frac{t}{\delta}\right)\cos\left(\frac{t}{\delta}\right) - \cosh\left(\frac{t}{\delta}\right)\sin\left(\frac{t}{\delta}\right)}{\cosh^2\left(\frac{t}{\delta}\right) - \cos^2\left(\frac{t}{\delta}\right)}$$

$$= \frac{\left[\sinh\left(\frac{t}{\delta}\right) - \sin\left(\frac{t}{\delta}\right)\right]\left[\cosh\left(\frac{t}{\delta}\right) - \cos\left(\frac{t}{\delta}\right)\right]}{\left[\cosh\left(\frac{t}{\delta}\right) + \cos\left(\frac{t}{\delta}\right)\right]\left[\cosh\left(\frac{t}{\delta}\right) - \cos\left(\frac{t}{\delta}\right)\right]}$$

$$= \frac{\sinh\left(\frac{t}{\delta}\right) - \sin\left(\frac{t}{\delta}\right)}{\cosh\left(\frac{t}{\delta}\right) + \cos\left(\frac{t}{\delta}\right)}$$

Hence:

$$\therefore F_R = \frac{R_{AC}}{R_{DC}} = \frac{t}{\delta}\left(\frac{\sinh\left(\frac{2t}{\delta}\right) + \sin\left(\frac{2t}{\delta}\right)}{\cosh\left(\frac{2t}{\delta}\right) - \cos\left(\frac{2t}{\delta}\right)} + \frac{2}{3}\left(M^2 - 1\right)\frac{\sinh\left(\frac{t}{\delta}\right) - \sin\left(\frac{t}{\delta}\right)}{\cosh\left(\frac{t}{\delta}\right) + \cos\left(\frac{t}{\delta}\right)}\right)$$

C2. Material properties of Nanoperm® (obtained from manufacturer's website):

Table C1: Nanoperm material properties

Saturation flux density (B_{sat})	1,2 T
Saturation magnetostriction	< 0,5 ppm
Specific electrical resistivity	115 µOhmcm
Density	7,35 g/cm3
Curie temperature (T_c)	600 °C
Min. operational temperature (T_{min})	- 40 °C
Max. operational temperature (T_{max})	+ 120 (180) °C
Core losses (0.3T/100kHz,sine) (P_v)	< 110 W/kg
Tape thickness (d)	17 / 23 µm
Grain size (typ.)	10 nm
Permeability (μ)	20.000 - 200.000
Alloy composition	$Fe_{73,5}\,Cu_1\,Nb_3\,Si_{15,5}\,B_7$

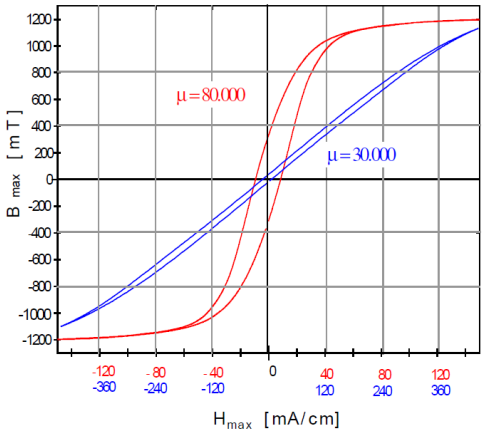


Figure C1: Hysteresis curves

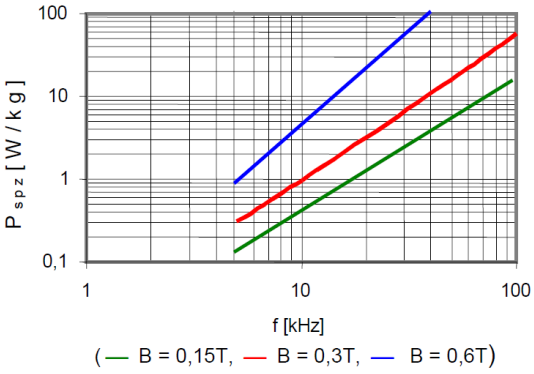


Figure C2: Core power loss curves

C3. M142 core data:

FORM Identifier: F 108 Revision: 03 Page: 1/1	Product specification for inductive components	MAGNETEC GmbH Industriestrasse 7 D-63505 Langenselbold

☐

Client:	MAGNETEC GmbH	Magnetec P/N:	M-142	Magnetec A/N:	12138
Client's P/N:	/	PS Index:	07	PS Revision:	06
Subject:	EMC Wandler			Type:	E

1. Mechanical Outline

Nominal core dimensions:

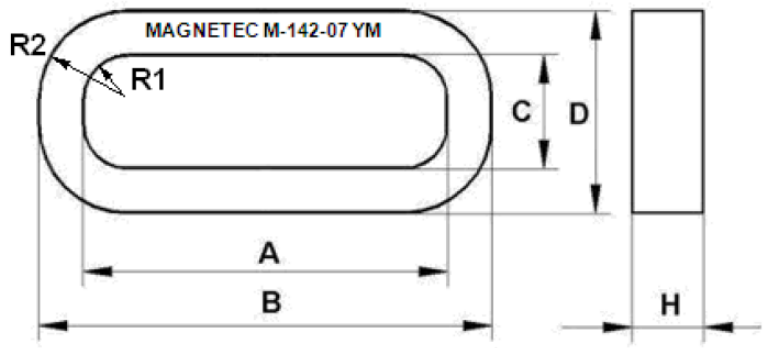
133 x 104 x 20

Finished product dimensions:

OD ≤ **172,0 (B) / 78,0 (D)**
ID ≥ **131,0 (A) / 37,0 (C)**
H ≤ **25,0**

[dimensions] = mm

R1 = 18,9 / R2 = 38,6



2. Core data

Core material:	NANOPERM®	L_{Fe} = 37,0 cm	A_{Fe} = 2,1 cm^2
Nominal values:	Permeability level	@ frequency	@ H peak
	~30.000	10 kHz	3,0 mA/cm

3. Inspection values

	Measured value	Measurement limits	Frequency	Ieff x N [mA x turn]
	AL [µH]	16,0 - 32,0	10 kHz	80

4. Core finishing

Type:	**Cased, with glued case**
Marking:	**MAGNETEC M-142-07 YM**
Packaging:	**4 pcs. per layer; 3 layers per carton box; PU = 12 pcs.**

5. Comments:

☒ **Marking date code (YM) acc. to IEC 62 5.1; YM = production year and month**
☒ **RoHS compliant according to directive 2002/95/EC**

Index / Revision	Alteration	Date
05 / 04	Milled case	05.07.2005
06 / 05	Moulded case / PU = 12 pcs.	10.11.2008
07 / 06	Glued case instead of taped one	21.06.2010

Created:	Zs. Eperjesi 21.06.2010	Approved (Techn):	F. Zámborszky 25.06.2010	Approved (Quality):	V. Káposztás 25.06.2010	Released:	F. Rauscher 25.06.2010

C4. Matlab Program for calculating the transformer winding power loss:

```
%-------------------------------------------------------------------------
%--------------- Transformer power loss calculations ---------------------
%-------------------------------------------------------------------------
u0=4*pi*10^-7
rou=1.73*10^-8;
freq=14*10^3;
%--------------------------
%primary winding: (litz wire)
%--------------------------
N1=27;
ns=46;
dc1=0.4e-3;
bc=100e-3;
MLT1=107e-3;
%--------------------------
Fr_pri=1+(((pi^4)*(freq^2)*(u0^2)*(N1^2)*(ns^2)*(dc1^6))/(192*(rou^2)*(bc^2)))
%--------------------------
delta=3.4e-6*freq;
f_eff=(freq/pi)*sqrt(6/(delta*(3-(4*delta))))
Fr_pri_rms=1+((Fr_pri-1)*((f_eff^2)/(freq^2)))
%--------------------------
Rdc1=rou*MLT1*N1/(ns*pi*((dc1/2)^2))
Rac1=Rdc1*Fr_pri_rms*2
%--------------------------
P1=(18.52^2)*Rac1
%--------------------------
%secondary winding: (parallel foil windings)
%--------------------------
h=0.45e-3;      %foil thicknes
b=100e-3;       %winding hieght
Skin_Depth=75e-3/sqrt(freq);
A=h/Skin_Depth
m=5;
cs1=2e-3*((25+4+4)+(20.5+4+4));

MLT2=cs1+2*(8*1e-3)+2.5*8*(0.45e-3);
Rdc2=rou*MLT2/(m*0.45*100e-6)
for n=1:1:16;

Fs_sec(n)=A*sqrt(n)*((sinh(2*A*sqrt(n))+sin(2*A*sqrt(n)))/(cosh(2*A*sqrt(n))-
cos(2*A*sqrt(n))));
    Fp_sec(n)=(2*A*sqrt(n)/3)*(((m^2)-1)*((sinh(A*sqrt(n))-
sin(A*sqrt(n)))/(cosh(A*sqrt(n))+cos(A*sqrt(n)))));
end
Fr_sec_n=Fs_sec+Fp_sec
Rac2n=Rdc2*Fr_sec_n
I=[426.03 115.28 86.57 81.51 8.79 42.84 12.18 14 8.82 0 0 0 4.25 4.62 0 6.03];
P2_n=Rac2n.*(I.^2)
P2_dc=(409.01^2)*Rdc2
P2=2*(P2_dc+sum(P2_n))
```

C5. Initial transformer testing:

- *RLC meter measurements:*

Open-circuit, short-circuit, and DC measurements are conducted using the FLUKE™ RLC meter shown below. The device applies a sinusoidal voltage to the measuring terminals and analyses the drawn current.

Table C1: Transformer open circuit, short circuit and DC measurement results using the RLC meter

Open-circuit measurements (at 14 kHz)	
$R_c = 5.85k\Omega$	$L_m = 67mH$
Short-circuit measurements (at 14kHz)	
$R = 25.24\Omega$	$L = 286.3\mu H$
DC measurements	
$R_p = 31m\Omega$	$R_s = 50\mu\Omega$

The short circuit inductance measurement is equivalent to the sum of primary and secondary leakage inductances. A higher obtained value, compared to experimental values obtained in Chapter 6, is due to the measurement error caused by the added short circuit wire inductance. However, based on the obtained DC resistances (and multiplying by the AC/DC resistance factors obtained earlier), the transformer primary winding power loss is 26.6 W, and the power loss in each secondary winding is 50.9 W, giving a total copper power loss of 128.5 W.

- *Open circuit operation, with 600 V, 14 kHz, input voltage:*

The circuit is tested at full primary voltage duty cycle. The input transformer current, primary voltage, and secondary voltage waveforms are shown below.

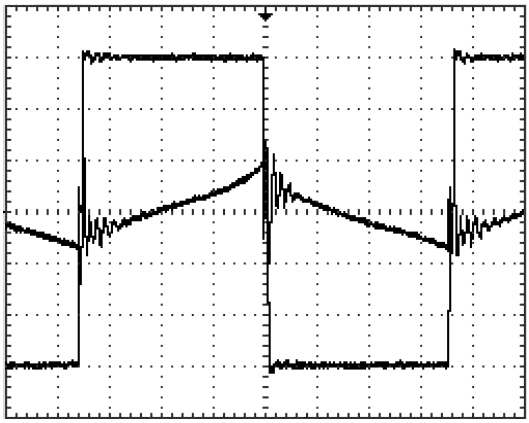


Figure C3: Transformer primary voltage and current (V_p*: 200 V/div,* i_p*: 250 mA/div, t: 10 µsec/div*)

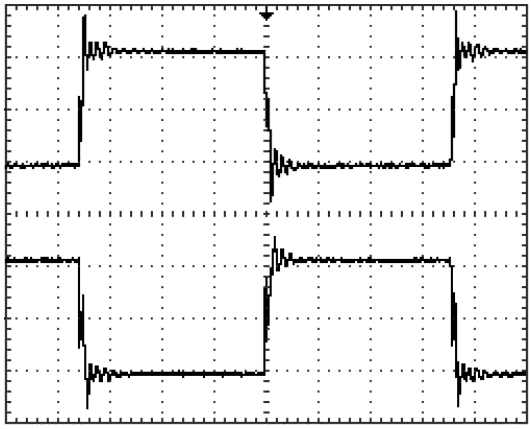


Figure C4: Transformer secondary voltages (V_{s1}*: 10 V/div,* V_{s2}*: 10 V/div, t: 10 µsec/div*)

The transformer draws an RMS current of 127 mA, while the RMS input voltage is 590 V. The input transformer current and voltage waveforms in this case can be used to obtain the transformer core losses (P_c). Using Fourier analysis, and considering odd harmonics due to half wave symmetry, the no-load transformer power loss due to fundamental (14 kHz) and odd harmonic components, up to the 21st harmonic, as calculated using Matlab, is 14.96 W. The transformer equivalent core loss resistance (R_c) and magnetizing inductance (L_m), as shown in the no-load equivalent circuit model shown in Figure C5, can be calculated as follows:

$$i_c = \frac{P_c}{v_{rms}} = \frac{14.96}{590} = 25.35mA$$

$$\therefore R_c = \frac{v_{rms}}{i_c} = \frac{590}{25.35\times10^{-3}} = 23.27k\Omega$$

$$i_m = \sqrt{i_{rms}^2 - i_c^2} = 124.44mA$$

$$\therefore L_m = \frac{v_{rms}}{2\pi f i_m} = 53.92mH$$

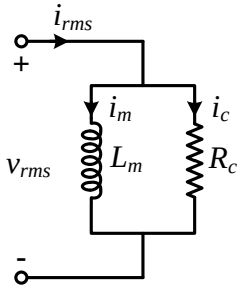


Figure C5: Transformer open-circuit equivalent circuit

Appendix D: Electro-thermal MOSFET Simulation Model

D1.Technical datasheet for device used in the analysis:

International
IOR Rectifier

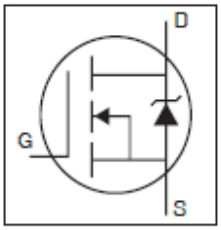
PD -97140

IRFP4668PbF

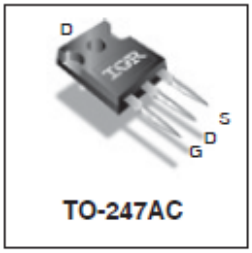
HEXFET® Power MOSFET

Applications
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free



V_{DSS}	200V
$R_{DS(on)}$ typ.	8.0mΩ
max	9.7mΩ
I_D	130A



TO-247AC

G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

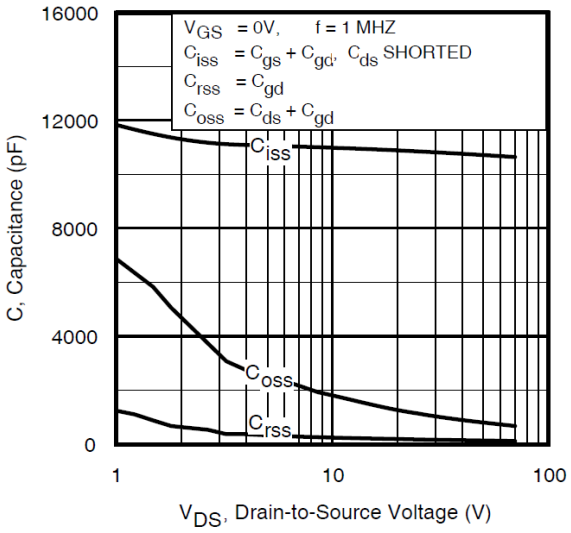
Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	130	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	92	
I_{DM}	Pulsed Drain Current ①	520	
P_D @T_C = 25°C	Maximum Power Dissipation	520	W
	Linear Derating Factor	3.5	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery ③	57	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

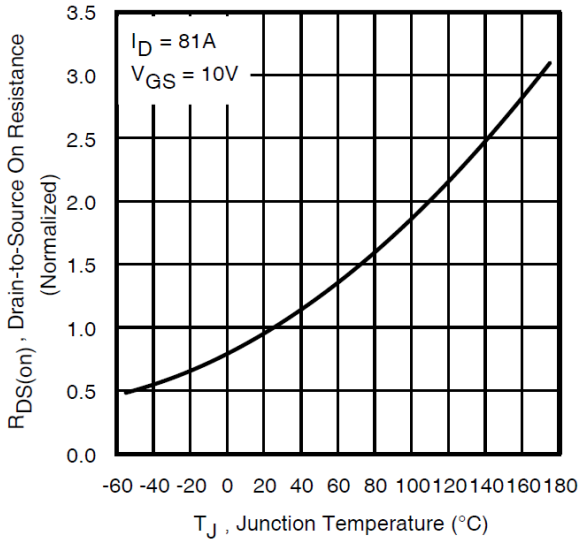
Avalanche Characteristics

$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ②	760	mJ
I_{AR}	Avalanche Current ①	See Fig. 14, 15, 22a, 22b,	A
E_{AR}	Repetitive Avalanche Energy ④		mJ

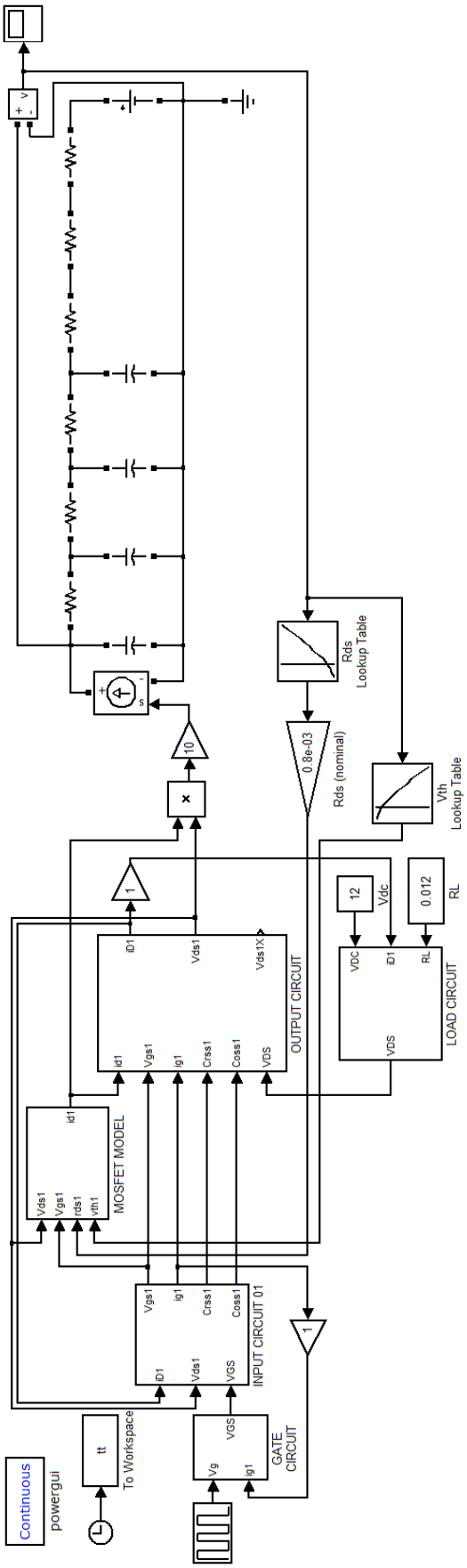
Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	—	0.29	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient ⑦ ⑧	—	40	


16000
12000
8000
4000
0
1
10
100
V_{GS} = 0V, f = 1 MHZ
C_{iss} = C_{gs} + C_{gd}, C_{ds} SHORTED
C_{rss} = C_{gd}
C_{oss} = C_{ds} + C_{gd}
C_{iss}
C_{oss}
C_{rss}
C, Capacitance (pF)
V_{DS}, Drain-to-Source Voltage (V)


3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-60 -40 -20 0 20 40 60 80 100120140160180
I_D = 81A
V_{GS} = 10V
$R_{DS(on)}$, Drain-to-Source On Resistance (Normalized)
T_J , Junction Temperature (°C)

D2. Simulink Electro-thermal Model:



Appendix E: 1 kA Synchronous Rectifier Module

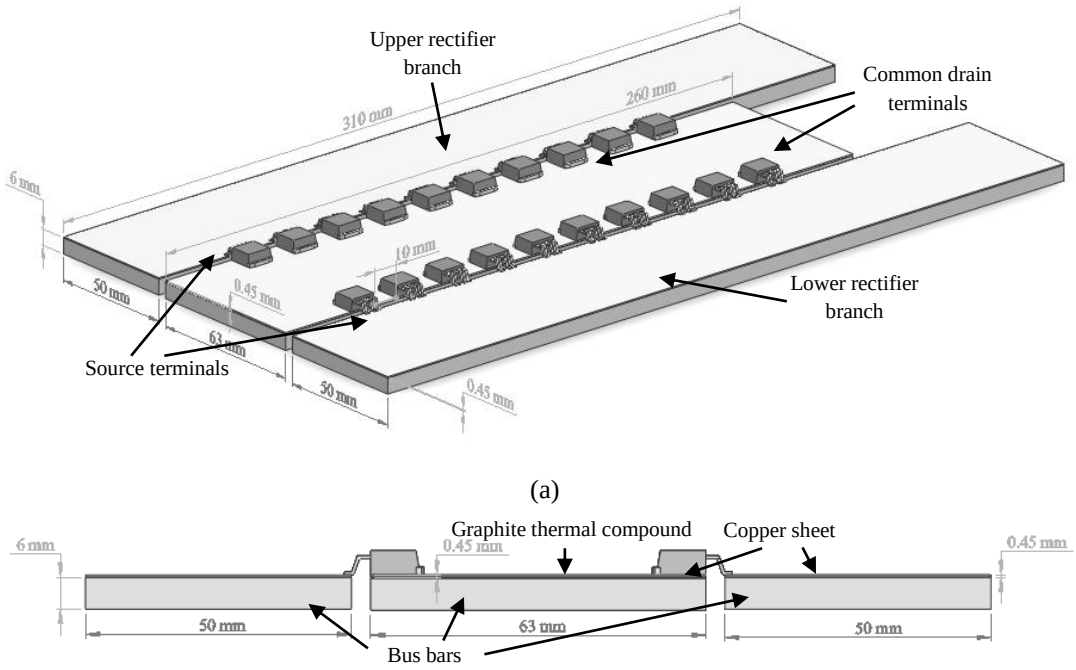


Figure E1: Synchronous rectifier assembly (a) 3D view of the bus bar arrangement, and (b) cross section view

Appendix F: Experimental Test Rig, Hardware and Software

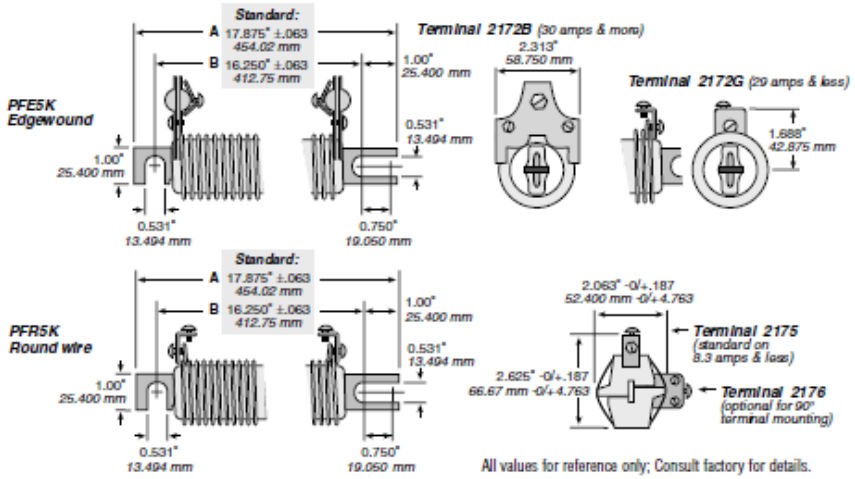
F1. Matlab m-file program for calculating the inverter and synchronous rectifier power loss:

```
n_turns = 54;
f_s = 14000;
v_p = 600;
L_lk = 135e-06;
L_load = 32e-03/11;
R_load = 0.085/11;
duty_cycle = (1)/2;
v_rec_drop = 0.1;
R_ds_on = 1.6*0.35/2;
V_on = 1.3;
%-------------------------------
d_eff = duty_cycle/(1+((4*L_lk*f_s)/(R_load*(n_turns^2))));
%-------------------------------
V_load = ((600/n_turns)*d_eff)-v_rec_drop;
%-------------------------------
I_load = V_load/R_load
%-------------------------------
d_i1_dash = ((600/n_turns)-V_load)*d_eff/(2*f_s*L_load);
%-------------------------------
d_i2_dash = V_load*(1-duty_cycle)/(2*L_load);
%-------------------------------
i1_dash = I_load - (d_i1_dash/2);
%-------------------------------
i2_dash = I_load + (d_i1_dash/2);
%-------------------------------
i3_dash = I_load + (d_i1_dash/2) - d_i2_dash;
%-------------------------------
i1 = i1_dash/n_turns;
i2 = i2_dash/n_turns;
i3 = i3_dash/n_turns;
d_i1 = d_i1_dash/n_turns;
d_i2 = d_i2_dash/n_turns;
%-------------------------------
P_S1_S2 = 2*((((i1^2) + ((d_i1^2)/3) + (i1*d_i1))*d_eff)+ ...
       (((i2^2) + ((d_i2^2)/3) - (i2*d_i2))*(1-duty_cycle))+ ...
       (((i3^2)/6)*(duty_cycle-d_eff)/2)+ ...
       (((i1^2)/3)*(duty_cycle-d_eff)/2))*R_ds_on;
P_S3_S4 = 2*((((i1^2) + ((d_i1^2)/3) + (i1*d_i1))*d_eff)+ ...
       (((i2^2) + ((d_i2^2)/3) - (i2*d_i2))*(1-duty_cycle)/2)+...
       (((i3^2)/6)*(duty_cycle-d_eff)/2)+ ...
       (((i1^2)/3)*(duty_cycle-d_eff)/2))*R_ds_on;
P_D1_D2 = 2*V_on*i3*(duty_cycle-d_eff)/4;
P_D3_D4 = 2*V_on*((((i2+i3)/2)*((1-duty_cycle)))+(i3*(duty_cycle-d_eff)/4));
%-------------------------------
P_inv_total = P_S1_S2 + P_S3_S4 + P_D1_D2 + P_D3_D4

P_synch_total = 2*((I_load^2)*(d_eff/2))*0.8/(1000*10)+...
    + V_on*(((((i1_dash)/2))*((1-d_eff)/2))+((((i2_dash)/2))*((1-d_eff)/2)))
```

F2. Load bank technical datasheet:

PFE and PFR Series

Powr-Rib® Edgewound
Edgewound and Round Wire



All values for reference only; Consult factory for details.

Designed in both Edgewound and Round Wire formats, these rugged resistors can handle 700 to 1000 Watts of power. Specify our Edgewound design for very low resistance and high power capacity. When higher resistance with lower power capacity is required use our Round Wire design.

Constructed of a heavy resistance alloy mounted on ceramic insulators and supported by a metal mounting bracket. Metal parts, except for the resistance element, are heavily plated to prevent oxidation at high operating temperatures and to prevent corrosion. The mounting bar is slotted on each end to facilitate installation. Edgewound units provide clamp-type terminals, permitting a reliable connection which can be moved along the resistive element to obtain intermediate values.

ORDERING INFORMATION

RoHS Compliant

P F E 5 K R 1 0 0 E

Style	# of Sections	Tolerance	Ohms
PFE = Edgewound PFR = Roundwire	2 5 3 6 4 7 8	K = 10%	R100 = 0.10 1R00 = 1.0 10R0 = 10

STANDARD PART NUMBERS

EDGEWOUND Ohms		Part #	Amps
0.1	✔	PFE5KR100E	100
0.12	✣	PFE5KR120E	91
0.14	✔	PFE5KR140E	89
0.16	✣	PFE5KR160E	78
0.18	✣	PFE5KR180E	75
0.22	✔	PFE5KR220E	68
0.25	✔	PFE5KR250E	63
0.3	✣	PFE5KR300E	57
0.33	✔	PFE5KR330E	54
0.37	✔	PFE5KR370E	50
0.5	✔	PFE5KR500E	47
0.6	✔	PFE5KR600E	43
0.67	✔	PFE5KR670E	41
0.75	✔	PFE5KR750E	39
1	✔	PFE5K1R00E	33
1.3	✔	PFE5K1R30E	29
1.6	✔	PFE5K1R60E	26
2.2	✔	PFE5K2R20E	18.4
2.8	✔	PFE5K2R80E	16.3
3.5	✔	PFE5K3R50E	14.6
4.5	✔	PFE5K4R50E	12.7
5.4	✔	PFE5K5R40E	11.8
6.8	✔	PFE5K6R80E	10.3
8.5	✔	PFE5K8R50E	9.4

ROUNDWIRE Ohms		Part #	Amps
11	✔	PFR5K11R0E	8.3
13	✔	PFR5K13R0E	7.6
17	✔	PFR5K17R0E	6.6
20	✔	PFR5K20R0E	5.9
25	✔	PFR5K25R0E	5.1

✔ = Standard values
✣ = Non-standard values subject to minimum handling charge per item.

Check product availability at
www.ohmite.com

SPECIFICATIONS

Electrical

Current Rating: Continuous duty as listed on following page.

Wattage Rating: 700 to 1,000 (up to 1,600 watts on special order)

Resistance Tolerance: ±10% standard, ±5% available

Terminals: Clamps, movable along resistor wire for setting intermediate resistance values on Edgewound units (current must be derated in proportion).

Temperature Coefficient:
±300 ppm/°C for resistors 50 amps and more
±500 ppm/°C for resistors 47 amps or less

Ohmic Values: See chart on following page.

Mounting: Metal mounting bar is slotted on each end to facilitate installation.

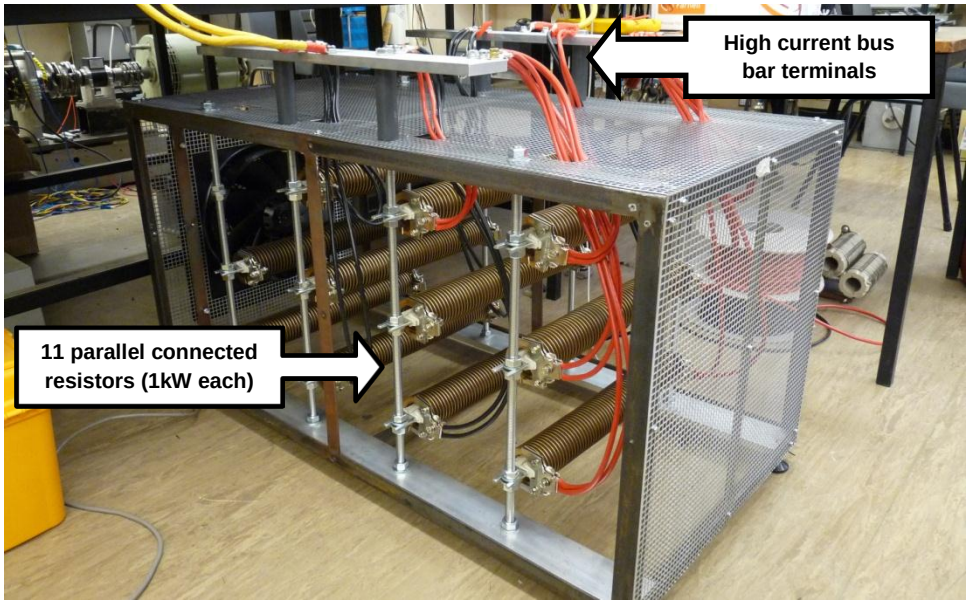
Edgewound units have clamp-type terminals which permits a reliable connection and can be moved along the resistive element to obtain intermediate values.

Ordering Information

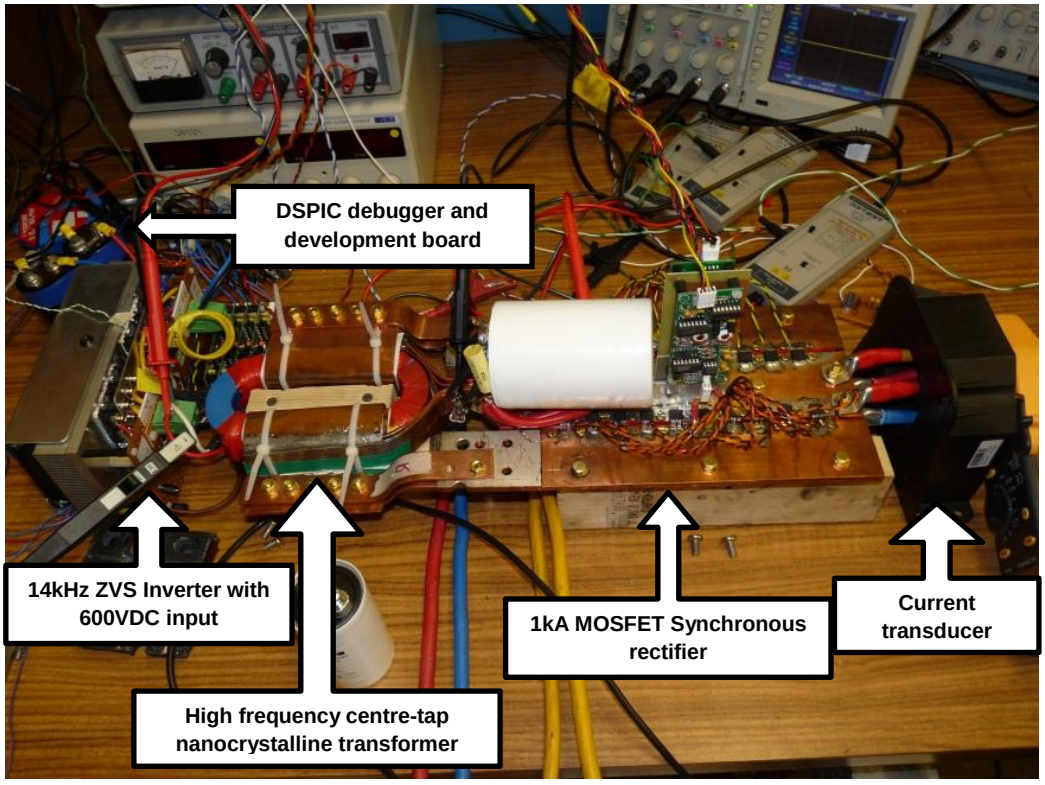
See Part Number chart for standard resistance values when ordering.

Our Tech Center is open 10am to 2pm CT Tuesdays and Thursdays, just call 866-9-OHMITE

F3. Load bank:



F4. Test Rig:



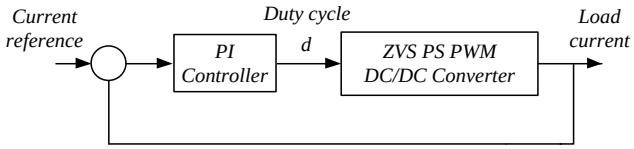
F5. Microchip MPLAB C-code:

- *Open-loop program:*

```
int i = 0;        // variable for to be incremented from 0 to 49
unsigned int x;
unsigned int temp;
/*****************************************************************/

/*************************** FUNCTIONS ***************************/
/*                     PWM INITIALIZATION FUNCTION                */

void init_pwm(void)
{
/* ~~~~~~~~~~~~~~~~~~~~~~~~~~~~ PWM 1 ~~~~~~~~~~~~~~~~~~~~~~~~~~~~ */

IOCON1bits.PENH = 1;    // PWM1H is controlled by PWM module
IOCON1bits.PENL = 1;    // PWM1L is controlled by PWM module
IOCON1bits.PMOD = 0;    // select complementary PWM mode

PDC1 = 22857;     // duty cycle = PDC1*1.5625 nsec = 35.7140 usec
DTR1 = 675;       // PWMH dead time = DTR1*1.5625 nsec = 0.8984 usec
ALTDTR1 = 675;    // PWML dead time = DTR1*1.5625 nsec = 0.8984 usec
PHASE1 = 22857;         // Phase shift = 0

/* ~~~~~~~~~~~~~~~~~~~~~~~~~~~~ PWM 2 ~~~~~~~~~~~~~~~~~~~~~~~~~~~~ */

IOCON2bits.PENH = 1;    // PWM2H is controlled by PWM module
IOCON2bits.PENL = 1;    // PWM2L is controlled by PWM module
IOCON2bits.PMOD = 0;    // select complementary PWM mode

PDC2 = 22857;     // duty cycle = PDC2*1.5625 nsec = 35.7140 usec
DTR2 = 675;       // PWMH dead time = DTR2*1.5625 nsec = 0.8984 usec
ALTDTR2 = 675;    // PWML dead time = DTR2*1.5625 nsec = 0.8984 usec
PHASE2 = 0;       // Phase shift = maximum = 22857 - 575 = 22282

/* ~~~~~~~~~~~~~~~~~~~~~~~~~~~~ PWM 3 ~~~~~~~~~~~~~~~~~~~~~~~~~~~~ */

IOCON3bits.PENH = 1;    // PWM3H is controlled by PWM module
IOCON3bits.PENL = 1;    // PWM3L is controlled by PWM module
IOCON3bits.PMOD = 0;    // select complementary PWM mode
PWMCON3bits.DTC = 1;    // negative deadtime

PDC3 = 22857;     // duty cycle = PDC3*1.5625 nsec = 35.7140 usec
DTR3 = 3125;      // PWMH dead time = DTR3*1.5625 nsec = 0.8984 usec
ALTDTR3 = 3425;   // PWML dead time = DTR3*1.5625 nsec = 0.8984 usec
PHASE3 = 22857-675;     // Phase shift = 0

/* ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ */

PTPER = 45714;    // PWM period = PTPER*1.5625 nsec = 71.4281 usec
PTCONbits.PTEN = 1;     // enable PWM module

/* ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ */
}

/*                     ADC INITIALIZATION FUNCTION                */

void init_adc(void)
{
ADCONbits.ADSIDL = 0;         // operate in idle mode
```

```
ADCONbits.FORM = 1;     // output in fractional format
ADCONbits.EIE = 1;      // generate interrupt after first conversion
ADCONbits.ORDER = 0;    // even analogue channel is converted first
ADCONbits.SEQSAMP = 1;  // sample at the start of second conversion
ADCONbits.ADCS = 2;                 // Fadc/8
ADPCFG = 0xFFFC;        // AN0 and AN1 set to analogue inputs
ADCPC0bits.IRQEN0 = 1;  // enable interrupt after AN0 and AN1 complete
ADCPC0bits.SWTRG0 = 1;        // start conversion of AN0 and AN1
ADCPC0bits.TRGSRC0 = 0xc;     // select timer1 match as trigger source

TMR1 = 0;                     // reset timer
PR1 = 45714;                  // match period every one complete cycle
IFS0bits.T1IF = 0;            // clear timer1 interrupt flag
IEC0bits.T1IE = 0;            // disable timer1 interrupt request


IFS0bits.ADIF = 0;      // clear ADC conversion interrupt flag status
IEC0bits.ADIE = 1;      // enable ADC conversion complete interrupt
ADCONbits.ADON = 1;           // turn on the ADC module
T1CONbits.TON = 1;            // turn on timer1

/* ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ */
}

/*********************************************************************/

/********************** INTERRUPT FUNCTIONS ***********************/
/*                           ADC INTERRUPT                           */

void __attribute__((interrupt, no_auto_psv)) _ADCInterrupt()
{
IFS0bits.T1IF = 0;      // clear timer1 interrupt flag
IFS0bits.ADIF = 0;      // clear ADC interrupt flag
ADSTATbits.P0RDY = 0;   // clear ADSTAT bit
if (i<50)         // save 50 samples of measured waveform in the array
      {           // for plotting
      PORTDbits.RD0 = 1;
      inputsignal[i] = ADCBUF0;
      PORTDbits.RD0 = 0;
      i = i+1;
      }
if (i>49)
      {
      i = 0;
      }
}

/*********************************************************************/

/************************** MAIN FUNCTION ***************************/

int main(void)
{
init_pwm();             // initialize PWM module
init_adc();             // initialize ADC module
while(1)                // infinite loop doing nothing
      {
      }
}
/*********************************************************************/
```

- *Closed-loop program:*



$K_P = 0.0001$

$K_I = 0.4$

```
/***************************** LIBRARY FILES ************************/

#include "p30f2020.h"
#include <dsp.h>
#include <stdlib.h>

/********************************************************************/

/************************* CONFIGURATION BITS ***********************/

_FOSCSEL(PRIOSC_PLL)
_FOSC(CSW_FSCM_OFF & OSC2_IO &HS)
_FPOR(PWRT_OFF)
_FGS(CODE_PROT_OFF)
_FBS(BSS_NO_FLASH)
_FICD(ICS_PGD1)

/********************************************************************/

/******************** GLOBAL VARIABLES AND ARRAYS *******************/

#define max_phase_shift  22857
#define FCY 10000000UL

#include "c://program files (x86)/Microchip/mplab
30/support/generic/h/libpic30.h"

fractional inputsignalsave[10];
int i = 0;

unsigned int k = 0;
unsigned int t = 0;
unsigned int f = 0;

tPID fooPID;
fractional abcCoefficient[3] __attribute__ ((section(".xbss, bss,
xmemory")));

fractional controlHistory[3] __attribute__ ((section(".ybss, bss,
ymemory")));

fractional kCoeffs[] = {0,0,0};

unsigned int phaseshift = 0;
```

```
unsigned int phaseshiftsave[10];
fractional ref_sig = 0.1;
float ref_sig_inc = 0;

/*****************************************************************/

/*************************** FUNCTIONS ***************************/
/*                     PWM INITIALIZATION FUNCTION                */

void init_pwm(void)
{

/* ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ PWM 1 ~~~~~~~~~~~~~~~~~~~~~~~~~~ */
IOCON1bits.PENH = 1;    // PWM1H is controlled by PWM module
IOCON1bits.PENL = 1;    // PWM1L is controlled by PWM module
IOCON1bits.PMOD = 0;    // select complementary PWM mode

PDC1 = 22857;     // duty cycle = PDC1*1.5625 nsec = 35.7140 usec
DTR1 = 675;       // PWMH dead time = DTR1*1.5625 nsec = 0.8984 usec
ALTDTR1 = 675;    // PWML dead time = DTR1*1.5625 nsec = 0.8984 usec
PHASE1 = 0;             // Phase shift = 0

/* ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ PWM 2 ~~~~~~~~~~~~~~~~~~~~~~~~~~ */

IOCON2bits.PENH = 1;    // PWM1H is controlled by PWM module
IOCON2bits.PENL = 1;    // PWM1L is controlled by PWM module
IOCON2bits.PMOD = 0;    // select complementary PWM mode

PDC2 = 22857;     // duty cycle = PDC1*1.5625 nsec = 35.7140 usec
DTR2 = 675;       // PWMH dead time = DTR1*1.5625 nsec = 0.8984 usec
ALTDTR2 = 675;    // PWML dead time = DTR1*1.5625 nsec = 0.8984 usec
PHASE2 = 0;             // Phase shift = 0

/* ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ PWM 3 ~~~~~~~~~~~~~~~~~~~~~~~~~~ */

IOCON3bits.PENH = 1;    // PWM1H is controlled by PWM module
IOCON3bits.PENL = 1;    // PWM1L is controlled by PWM module
IOCON3bits.PMOD = 0;    // select complementary PWM mode

PDC3 = 22857;     // duty cycle = PDC1*1.5625 nsec = 35.7140 usec
DTR3 = 675;       // PWMH dead time = DTR1*1.5625 nsec = 0.8984 usec
ALTDTR3 = 675;    // PWML dead time = DTR1*1.5625 nsec = 0.8984 usec
PHASE3 = 0;             // Phase shift = 0

/* ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ */

PTPER = 45714;    // PWM period = PTPER*1.5625 nsec = 71.4281 usec
PTCONbits.PTEN = 1;     // enable PWM module

}
/* ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ */
/*                     ADC INITIALIZATION FUNCTION                */
/* ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ */

void init_adc(void)
{
ADCONbits.ADSIDL = 0;         // operate in idle mode
ADCONbits.FORM = 1;           // output in fractional format
ADCONbits.EIE = 1;      // generate interrupt after first conversion
ADCONbits.ORDER = 0;    // even analogue channel is converted first
ADCONbits.SEQSAMP = 1;  // sample at the start of second conversion
```

```
ADCONbits.ADCS = 2;           // Fadc/8
ADPCFG = 0xFFFC;              // AN0 and AN1 set to analogue inputs
ADCPC0bits.IRQEN0 = 1;  // enable interrupt after AN0 and AN1 complete
ADCPC0bits.SWTRG0 = 1;        // start conversion of AN0 and AN1
ADCPC0bits.TRGSRC0 = 0xc;     // select timer1 match as trigger source

TMR1 = 0;                     // reset timer
PR1 = 45714;                  // match period every one complete cycle
IFS0bits.T1IF = 0;            // clear timer1 interrupt flag
IEC0bits.T1IE = 0;            // disable timer1 interrupt request

T1CONbits.TCKPS = 0x2;
IFS0bits.ADIF = 0;      // clear ADC conversion interrupt flag status
IEC0bits.ADIE = 1;      // enable ADC conversion complete interrupt
ADCONbits.ADON = 1;           // turn on the ADC module
T1CONbits.TON = 1;            // turn on timer1

/* ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ */

}

/*****************************************************************/

/*********************** INTERRUPT FUNCTIONS ************************/
/*                           ADC INTERRUPT                          */

void __attribute__((interrupt, no_auto_psv)) _ADCInterrupt()
{
IFS0bits.T1IF = 0;
IFS0bits.ADIF = 0;            // clear ADC interrupt flag
ADSTATbits.P0RDY = 0;         // clear ADSTAT bit

fooPID.measuredOutput = ADCBUF0/2;

PID(&fooPID);

phaseshift = __builtin_mulsu(fooPID.controlOutput, max_phase_shift) >>
15;

PHASE1 = phaseshift;
PHASE3 = phaseshift;

if (phaseshift > 22857)
      {
      phaseshift = 22857;
      }
if (phaseshift < 0)
      {
      phaseshift = 0;
      }
if (i<10)
      {
      PORTDbits.RD0 = 1;
      phaseshiftsave[i] = phaseshift;
      inputsignalsave[i] = ADCBUF0;
      PORTDbits.RD0 = 0;
      i = i+1;
      }
if (i>9)
      {
      i = 0;
```

```
      }

      }

/*********************************************************************/

/************************** MAIN FUNCTION ***************************/

int main(void)
{
fooPID.abcCoefficients = &abcCoefficient[0];
fooPID.controlHistory = &controlHistory[0];
PIDInit(&fooPID);
kCoeffs[0] = Q15(0.00001);
kCoeffs[1] = Q15(0.4);
kCoeffs[2] = Q15(0);
PIDCoeffCalc(&kCoeffs[0], &fooPID);
fooPID.controlReference = Q15(0.00000001);
init_pwm();
init_adc();
delay_ms(1000);

while(f<1)
{
if ((k<65530) && (f<1))
      {
      k++;
      }
if ((k = 65530) && (f<1))
      {
      k=0;
      t++;
      }
if ((t = 65530) && (f<1))
      {
      k=0;
      ref_sig_inc = ref_sig_inc+0.000001;
      fooPID.controlReference = Q15(ref_sig_inc);
      }
if ((ref_sig_inc>0.6066611842) && (f<1))
      {
      f=2;
      }
      }
delay_ms(delay_interval_1);
ref_sig_inc = 0.4044407894;
fooPID.controlReference = Q15(ref_sig_inc);
while(1)
      {
      }

}

/*********************************************************************/
```

Appendix G: 10kA DC/DC converter design

G1. Nanocrystalline core used for the design:

FORM Identifier: F 108 Revision: 03 Page: 1/1	Product specification for inductive components	MAGNETEC GmbH Industriestrasse 7 D-63505 Langenselbold

☐

Client:	MAGNETEC GmbH	Magnetec P/N:	M-248	Magnetec A/N:	12386
Client's P/N:	/	PS Index:	04	PS Revision:	02
Subject:	EMC Wandler			Type:	E

1. Mechanical Outline

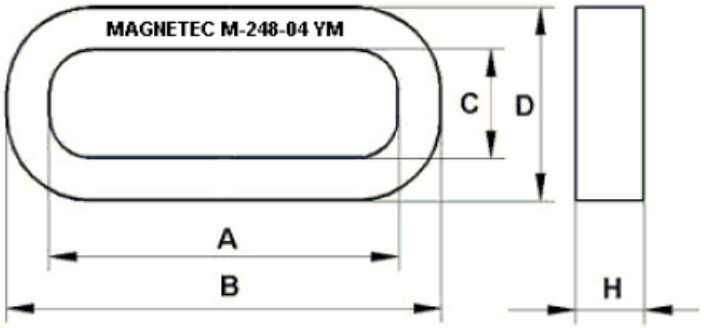
Nominal core dimensions:

300 x 254 x 30

Finished product dimensions:

OD ≤ 392,0 (B) / 160,0 (D)
ID ≥ 326,0 (A) / 94,0 (C)
H ≤ 36,0

[dimensions] = mm



2. Core data

Core material:	NANOPERM®	L_{Fe} = 87,1 cm	A_{Fe} = 5,2 cm²
Nominal values:	Permeability level	@ frequency	@ H peak
	~30 000	10 kHz	3,14 mA/cm

3. Inspection values

	Measured value	Measurement limits	Frequency	leff x N [mA x turn]
	AL [µH]	15,8 - 31,5	10	185

4. Core finishing

Type:	Cased
Marking:	MAGNETEC M-248-04 YM
Packaging:	1 pcs. per layer; 5 layers per carton box; PU = 5 pcs.

5. Comments:

☒ Marking date code (YM) acc. to IEC 62 5.1; YM = production year and month
☒ RoHS compliant according to directive 2002/95/EC

Index / Revision	Alteration	Date
04 / 01	Product specification / Moulded case	12.12.2006
04 / 02	PU = 5 pcs.	17.07.2009

Created:	F. Zámborszky 17.07.2009	Approved (Techn):	J. Nyéki 21.07.2009	Approved (Quality):	V. Káposztás 21.07.2009	Released:	F. Rauscher 21.07.2009

G2. High power IGBT module with internal parallel connected device dies:

MITEL SEMICONDUCTOR

GP600DHB16S

Powerline N-Channel IGBT Module

Supersedes March 1997 version, DS4335 - 5.6

DS4335 - 5.7 December 1998

APPLICATIONS

- High Power Switching.
- Motor Control.
- UPS.
- AC And DC Servo Drive Amplifiers.

TYPICAL KEY PARAMETERS

V_{CES}	1600V
$V_{CE(sat)}$	3.5V
$I_{C(CONT)}$	600A
$I_{C(PK)}$	1200A

FEATURES

- n - Channel.
- Enhancement Mode.
- High Input Impedance.
- High Switching Speed.
- Latch-Free Operation.
- Low Forward Voltage Drop.
- Isolated Base.

CIRCUIT

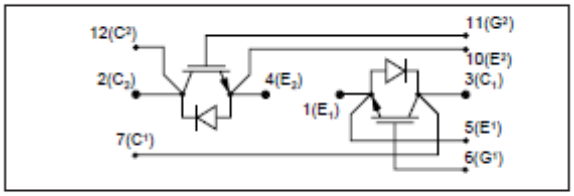


Fig.1 Half bridge circuit diagram

PACKAGE OUTLINE

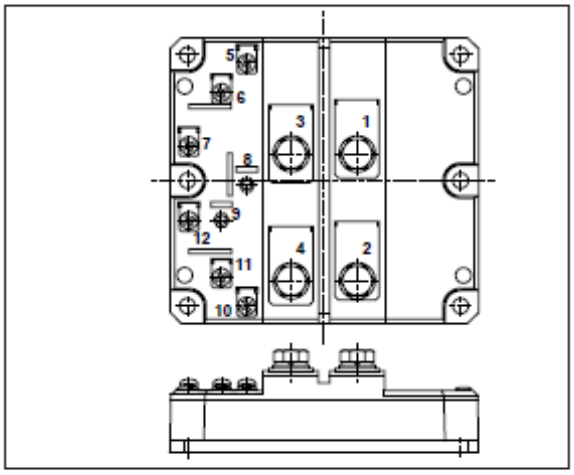


Fig. 2 Outline type code: D.
See package details for further information.

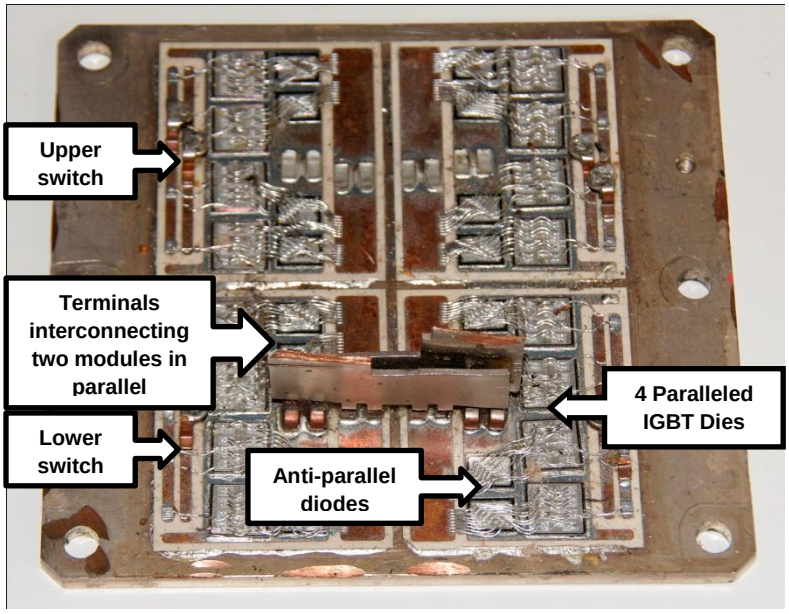
RATINGS

T_{case} = 25°C unless stated otherwise.

Symbol	Parameter	Test Conditions	Max.	Units
V_{CES}	Collector-emitter voltage	V_{GE} = 0V	1600	V
V_{GES}	Gate-emitter voltage	-	±20	V
I_C	Collector current	DC, T_{case} = 25°C	600	A
$I_{C(PK)}$		1ms, T_{case} = 25°C	1200	A
P_{max}	Maximum power dissipation (per arm)	T_{case} = 25°C (Transistor)	4150	W
V_{isol}	Isolation voltage	Commoned terminals to base plate. AC RMS, 1 min, 50Hz	3400	V

Caution: These devices are sensitive to electrostatic discharge. Users should observe proper ESD handling precautions.

G3. Internal structure for a high power IGBT module:



Appendix H: Author's Publications

1. Shafik, Z. M. ; Ahmed, K. H. ; Finney, S. J. ; Williams, B. W. ;

Nanocrystalline cored transformer design and implementation for a high current low voltage dc/dc converter

This paper appears in: Power Electronics, Machines and Drives (PEMD 2010), 5th IET International Conference on

ABSTRACT

Transformers are considered critical components that influence high power converter dynamic response, efficiency, and size. High permeability nanocrystalline cores are being increasingly utilized in designs due to their high saturation flux density, high power density, and lower power loss, for a given volume. This paper presents the design and implementation of a high frequency nanocrystalline cored transformer operating at 14 kHz, and used in a high current low voltage dc-dc converter with a 600 V input, and an 8 V, 1000 A output requirement. Power loss analysis and leakage inductance calculation are derived to evaluate the transformer performance. Simulation and experimental results are also presented to validate the design.

2. Shafik, Z.M. ; Masoud, M.I. ; Fletcher, J.E. ; Finney, S.J. ; Williams, B.W. ;

Efficiency improvement techniques of high current low voltage rectifiers using MOSFETs

This paper appears in: Universities Power Engineering Conference (UPEC), 2009 Proceedings of the 44th International

ABSTRACT

This paper presents techniques for loss minimization in ultra-high current low-voltage power supplies. The use of synchronous rectification using MOSFETs offers the advantage of reducing the conduction losses significantly compared to conventional rectification, with the possibility of achieving almost zero conduction losses through parallel connection. The design considerations for paralleling MOSFETs are briefly discussed, as paralleling is required for satisfying the high current requirements. Moreover, cryogenic operation of MOSFETs offers further reduction of the conduction losses. MOSFETs with various ratings are tested to evaluate the reduction in the on-resistance at liquid nitrogen temperature compared to the normal operating temperature. An estimate for the rectifier power losses including the cooling power is compared in order to show if it is advantageous for this specific application.