University of Strathclyde

Design, implementation, and applications of a novel isolated D2 dc to dc converter

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June, 2024

This thesis is the result of author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

Acknowledgement

I would like to thank Prof. Barry W. Williams and Prof. Jiang Wei for their continuous guidance, advice, and knowledge sharing; without whom, this research would not have been possible.

I also would like to thank Dr Mohamed Atef Elgenedy, Dr Neville McNeill and Dr Shuren Wang for their support and advice throughout my PhD study.

Finally, sincere relief goes to myself, for my persistence, striving, and fight against pain through this period.

List of Symbols

Symbol	Term	Unit
B_s	Magnetic Flux Density	T
C	Capacitance	F
δ	Duty Cycle	
f_s	frequency	Hz
H	Magnetic Field	A/m
η	Efficiency	
I_{in}	Input Current	A
I_o	Output Current	A
I_{Lo}	Current flowing in inductor L_o	A
k	Transformer Coupling Coefficient	
L_i	Input Inductance	H
L_o	Output Inductance	H
M	Mutual Inductance	H
n	Transformer Turns Ratio	
n	Phase number	
N_1	Transformer Primary side turns	
N_2	Transformer Secondary side turns	
N_P	Transformer Primary side turns	
N_S	Transformer Secondary side turns	
P_{in}	Input Power	W
P_o	Output Power	W
P_{rated}	Rated Power	W
S	Light Intensity	W/m^2
T	Temperature	℃
T_s	Switching Time Period	s
R_o	Output Resistance	Ω
R_{load}	Resistive Load Resistance	Ω
V_{in}	Input Voltage	V
V_o	Output Voltage	V
V_{Co}	Output Capacitor Voltage	V
V_{C1}	C_1 Voltage	V
V_{C2}	C_2 Voltage	V
V_S	Voltage Power Supply	V

List of Abbreviations

Abbreviation	Term
ac	alternative current
CCM	Continuous Conduction Mode
dc	direct current
DCM	Discontinuous Conduction Mode
DPDT	Double-pole double-throw
DSP	Digital Signal Processor
EMF	Electromagnetic Force
EMI	Electromagnetic Interference
HFT	High frequency transformer
IGBT	Insulated Gate Bipolar Transistor
mmf	Magnetomotive Force
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
PI	Proportional Integral
PID	Proportional Integral Derivative
PLL	Phase Locked Loop
PS	Power System
PV	Photovoltaic
PWM	Pulse Width Modulation
RMS	Root Mean Square
SiC	Silicon Carbide
SOC	State of Charge
SOE	State of Energy
SOH	State of Health
SPDT	Single-pole Double-throw
VSC	Voltage Source Converter

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Abstract

Power converters play a pivotal role in renewable energy power generation systems, with their significance increasing utilization and broad application in areas such as photovoltaics, fuel cells, uninterruptible power supplies, and electric vehicles. The advent of sustainable charging methodologies derived from renewable energy sources paves the way for future interfaces that are not only sustainable but also render distributed energy resources eco-friendly. An optimal converter is characterized by a wide conversion ratio, cost-effectiveness, minimal voltage stress on switches, simplicity, galvanic isolation, and high-efficiency performance. These attributes enable the converter's economic viability in various systems, including charging systems, inversion, and green energy resources like solar energy conversion. This research aims to explore these aspects in depth, contributing to the body of knowledge in this rapidly evolving electric power conversion field.

This study introduces an electrically isolated D2 dc to dc converter; an innovative derivation from the traditional single switch D2 converter, designed to fulfil the requirements of sustainable distributed systems. Comprehensive models of the proposed converter, including circuit and mathematical models, a simulation model, and a hardware platform, confirm these aspects. The converter topology is implemented in a photovoltaic system for maximum power point tracking and energy storage device charging. It accommodates three dc/dc application scenarios: low power conversion, input-parallel output-series cascaded and interleaved parallel connections, each governed by their respective modulation strategies and control methods. This research exploration of these aspects contributes to the evolving field of sustainable energy conversion.

This thesis presents three variations derived from the isolated D2 converter, for active power factor correction, namely, the isolated D2 converter, the bridgeless isolated D2 converter, and the interleaving isolated D2 converter. Each of these converters successfully achieves the power factor correction objectives of maintaining a stable output voltage, ensuring a near unity factor, and minimizing harmonic current. After

analysis and comparison, the interleaving converter emerges as a superior choice, demonstrating the most advantageous characteristics among the three power factor correction converters.

A single-phase inverter is derived from the proposed isolated D2 converter for inversion applications. The inverter is sinusoidally modulated with second-order generalized integrator phase lock loop, generating a standard sinusoidal voltage waveform. The output voltage and current from the inversion process align with the requirements of distributed resources. This innovative approach to inversion offers the potential for efficient energy conversion in distributed systems, including both single and three phase system.

This research encompasses the realization of dc/dc application converters, power factor correction converters, and inverters on both software and hardware platforms. The features and characteristics of these elements are observed, compared, and analysed. The isolated D2 converter, the focus of this research, demonstrates wide and effective applicability in isolated dc/dc, ac/dc, and dc/ac applications, exhibiting commendable performance when properly utilized. Given its robustness, the isolated D2 converter with continuous input and output current converter, is posited as a promising converter topology for future energy resources.

Keywords: An isolated D2 converter; dc/dc applications; Active power factor correction; Single-phase inversion

CHAPTER 1 Introduction

This thesis is concerned with the efficient and simple energy conversion between two dc voltage sources or a dc source and a dc load. A so-called dc to dc (dc/dc) converter can be stand alone or part of a larger electric power conversion system. This introduction focuses on describing many of the known dc/dc converters, and the numerous systems they form part of. The thesis, hence, introduction, is biased towards transformer isolated converters and low semiconductor switching component count, which yield high electric power conversion efficiency. Basic converter configurations are initially considered, and with this appreciation, followed by typical dc/dc converter applications.

1.1 dc/dc Converter Classification

Depending on whether there is an electrical connection between dc/dc converters, they can be divided into two categories: either isolated or non-isolated dc/dc converters. Each category employs distinct methodologies to enhance converter characteristics and features. As shown in Fig. 1.1, there are many commonly used derivations of dc/dc converters.

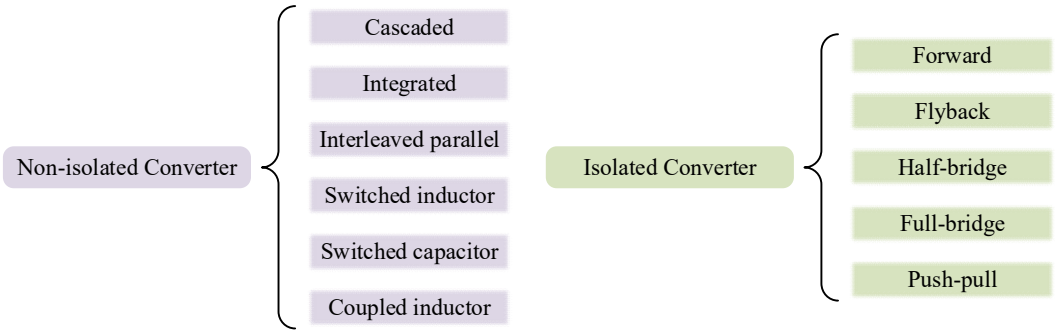


Fig. 1.1 dc/dc converter categories and derivations

The concern and focus of this thesis is ***isolated*** switched mode dc/dc conversion, which provides galvanic electrical isolation (generally a transformer) between the input energy dc source and the dc load and provides flexible dc gain for dedicated applications. Generally, the voltage transfer ratio is determined and controlled by the transformer ratio, n, and switch on-state duty cycle, δ. Non-isolated dc/dc converters generally have a simple topology, convenient control, low cost, and high reliability and stability.

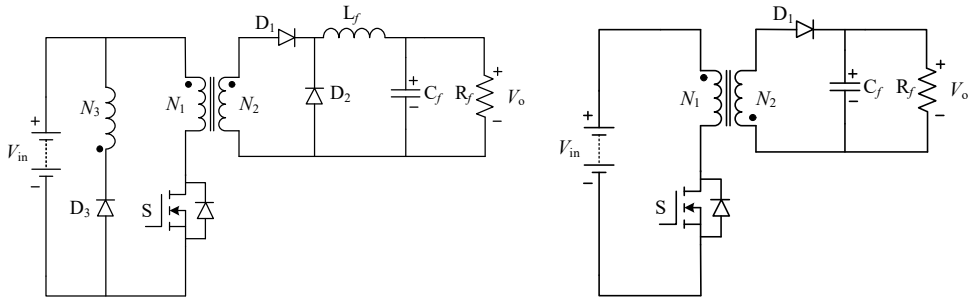
The isolation (between the input source and output load) is usually achieved by a dc/ac/dc conversion sequence using two sequential stages: dc/ac conversion and ac/dc conversion. Coupled inductors or ac transformers are used for the galvanic isolation. Isolation may be required for safety, voltage level shifting and grounding purposes. Isolation can protect low-voltage circuitry from high voltage stress in high voltage systems, particularly in applications demanding a high voltage transfer ratio. Isolated structures can provide different platforms of grounding in the interconnection of dc networks.

1.2 Isolated dc/dc Converters

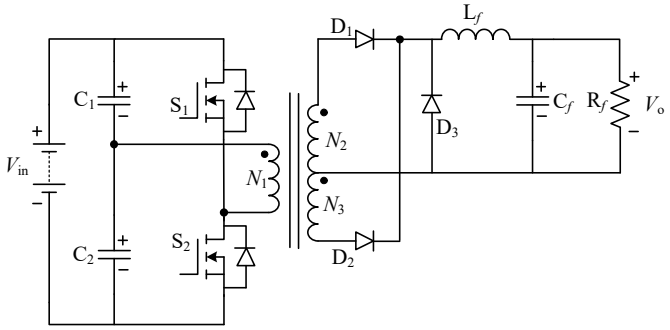
The common isolated dc/dc converter circuits (with one magnetic component) include,

forward and flyback, push-pull, half-bridge and full-bridge circuits [1], [2]. Isolated type converters can adjust the turns ratio to vary the output voltage range and can avoid high active switch losses due to high duty cycle values. However, increasing the turn ratio can affect the coupling factor of the transformer. The existence of parasitic parameters that cannot be ignored, such as leakage inductance and distributed capacitance, can render low efficiency in high-voltage gain applications.

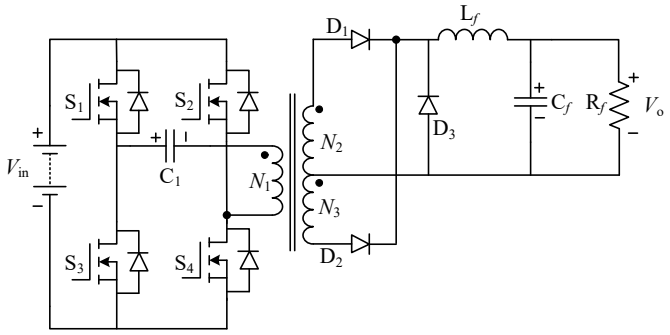
The single switch flyback dc/dc converter in Fig. 1.2 (b) evolves from the buck/boost dc converter and is one of the simplest isolated dc/dc converters [1]. Its main power circuit consists of four components. The transformer of the flyback dc/dc converter is actually a coupled inductor, and the core of the magnetic material used in the transformer can have an air gap to ensure that the core does not saturate at maximum load current. The flyback conversion circuit refers to the excitation direction into the primary of the transformer, which is the opposite to the excitation direction out of the transformer. That is, the core stores energy taken from the primary side EMF source when the switch is ON, stores it, and releases that energy on the secondary side, with the core retaining a dc level of energy (under a continuous inductor current condition). An air gap allows more magnetic energy storage. Flyback conversion has high conversion efficiency, can provide multiple outputs, and the circuit has few components. If a suitable control circuit is added, a high efficiency, low consumption, and stable output power supply can be achieved.



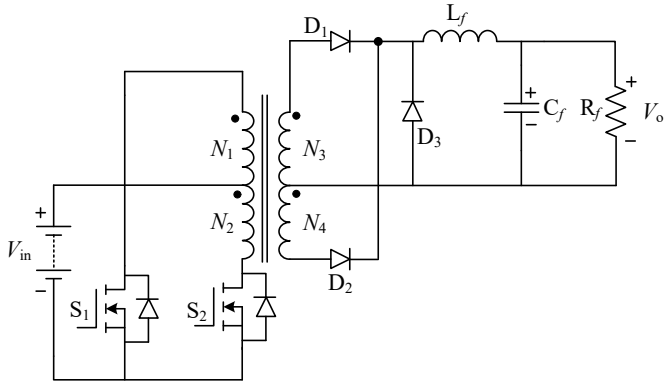
(a) Forward dc/dc converter (b) Flyback dc/dc converter



(c) Half-bridge dc/dc converter



(d) Full-bridge dc/dc converter



(e) Push-pull dc/dc converter

Fig. 1.2 Common isolated dc/dc converters [1]

The single switch, isolated, Forward dc/dc converter in Fig. 1.2a is derived by inserting a transformer into the basic Buck dc/dc converter [1]. The Forward converter transfers energy directly from the input to the output through the transformer when the switch is turned ON. When the switch is turned OFF, the secondary winding of the transformer will provide electrical energy to the output through an external diode. It usually operates in a continuous conduction mode. The most significant difference between the forward

dc/dc converter and the Flyback dc/dc converter is that the transformer primary relative to the secondary winding, which are opposite (dot orientation). N_3 is a flux reset winding, which is used to demagnetize the core when the switch is off; preventing core saturation. The transformer of the Flyback converter needs to support energy storage and release and is usually designed with an air gap. The transformer design of Forward converters focuses on direct energy transfer, with less demand for air gaps. Flyback converters are typically used for low-power applications; Forward converters are suitable for applications that require high power and efficiency.

The half-bridge dc/dc converter in Figure 1.2c [1] is composed of a half-bridge inverter, centre tapped dc link capacitors, and an output rectifier filter element. The characteristics of the half-bridge dc/dc converter are: (1) the transformer input voltage is half the working voltage of the switching components. (2) the primary winding of high-frequency transformers has no central tap in the primary winding.

The full-bridge dc/dc converter in Fig. 1.2d [1] is composed of a single-phase full-bridge inverter and an output rectifier filter circuit. The circuit is composed of four switches, and its transformer only has one primary winding. Through rotation of forward and reverse voltage, two opposite magnetic fluxes result from the primary winding of the transformer, which results in the need for full wave rectification in the secondary winding to obtain output dc energy. Soft switching the full-bridge converter circuit improves its electrical performance, conversion efficiency, and reliability compared to hard-switching power supplies.

The full-bridge converter circuit has the following advantages: (1) load current sharing technology, and the power supply adopts current sharing technology, which is easy to expand. There are various methods to achieve modular expansion and load equalization. Controls of the full-bridge topology include zero voltage pulse width modulation and soft switching phase shift control.

The Push-pull dc/dc converter in Fig. 1.2e is composed of an output rectifier filter that utilises two complementary controlled switches. It uses pulse width modulation and transformer isolation. It connects the centre tap of the transformer to the positive of the input power supply, and the other ends are respectively connected to the drains of the

switch transistors. Consequently, through coupling, the switches experience at least twice the dc supply voltage. But, at low voltages, it can be more cost effective than half-bridge and full-bridge conversion power supplies. The centre tapped secondary in the three bridge circuits can be replaced by a single winding with a full-bridge diode rectifier.

1.3 Converter Analysis

To design a converter, it is necessary to quantify many of the circuit characteristics, such as the ac and dc currents flowing through its circuit elements, the voltages across these elements, the input-to-output voltage transfer ratio as a function of switch on-state duty cycle, δ, etc.

The basic principle of a state space averaging method is to take the inductor current and capacitor voltage as state variables, within the topology basic circuit components, according to the state of the power switch. The dc/dc converter contains nonlinear components such as power switches and diodes, making the system nonlinear. However, when the converter operates near a stable operating point, the relationship between the small signal perturbations of the circuit state variables is linear. Therefore, the nonlinear dc/dc converter can be decomposed into a linear system for analysis through the state space averaging method.

In PWM-switched dc/dc converters, the input voltage V_s can be regarded as a power source, and the driving signal of the switch base/gate can be considered as a signal source. Both switches and diodes operate within a large range of their characteristic curves, so switch-mode power converters are highly nonlinear. For simplicity, first consider switches and diodes as ideal switches, ignoring their conduction voltage drop and off-state leakage current while also ignoring their switching process, which means that switching action is considered instantaneous. Then, a PWM-type dc/dc converter operating in continuous conduction mode (inductor current never falls to zero) can be represented by two linear non-time-varying circuits. The state space equations are:

$0 < t < \delta T_s$

$$\dot{x} = A_1 x + B_1 V_s \tag{1-1a}$$

$$y = C_1^T x \tag{1-1b}$$

$\delta T_s < t < T_s$

$$\dot{x} = A_2 x + B_2 V_s \tag{1-2a}$$

$$y = C_2^T x \tag{1-2b}$$

where x is a state variable; A_1, B_1, A_2, B_2, $C_1{}^T$, and $C_2{}^T$ are the coefficient matrix, and δ is the on-state duty cycle of the power switch.

The state space averaging method can provide an analytical form of the dynamic characteristics of dc/dc converters, enabling the analysis of such switch regulation systems using linear system theory. In the state space averaging method, the solution is not based on the instantaneous values of each variable in the circuit but on the average value. The purpose of this method is to obtain mathematical expressions describing the steady-state and dynamic small signal characteristics of the circuit by providing the coefficient matrices A_1, B_1, A_2, B_2, $C_1{}^T$, and $C_2{}^T$ of the state equation under two switch states and then obtain a unified low-frequency small signal equivalent circuit model.

The piecewise linear equations of PWM switching converters shown in equations (1-1) and (1-2) are exact. To obtain the state space average equation that describes its steady-state and dynamic small signal characteristics, the following steps are needed: averaging, adding a disturbance, and linearization.

1.4 The Isolated Ćuk

Numerous (thirty) two inductor, single switch dc/dc converters exist [1], [2]. An example is the Ćuk converter, C5, (and its isolated variation) since it shares the same component count, transfer function, and similar two inductor operation mechanisms as the D2 converter [2], which is the research subject of this thesis.

1.4.1 Non Isolated Ćuk [1]

There are many single switch dc/dc converter circuits (33 in total [2], See Appendix A for the 33 known single switch dc to dc converters and their alphanumeric classification), including three basic circuits with one inductor: Buck (A1), Boost (A2), Buck/Boost (A5) converters, and commonly, with two inductors: Ćuk (C5), Sepic (G5), and Zeta (G6). The Ćuk converter is the most common two inductor dc/dc converter.

(notation is per [2])

Fig.1.3 shows the evolution of the Ćuk converter. A Buck converter is preceded by a boost converter, with intermediate capacitor decoupling, as shown in Fig. 1.3a. In Fig. 1.3b, the switch-and-diode pair is replaced by a single DPDT switch, and C_1 is retained for energy storage. As with the Buck-Boost, output voltage polarity inversion allows further simplification. As indicated in Fig. 1.3c, the DPDT switch and shunt capacitor network can be replaced by an SPDT switch and a series capacitor. A practical realization of this new circuit is shown in Fig. 1.3 (d): namely the Ćuk converter [138].

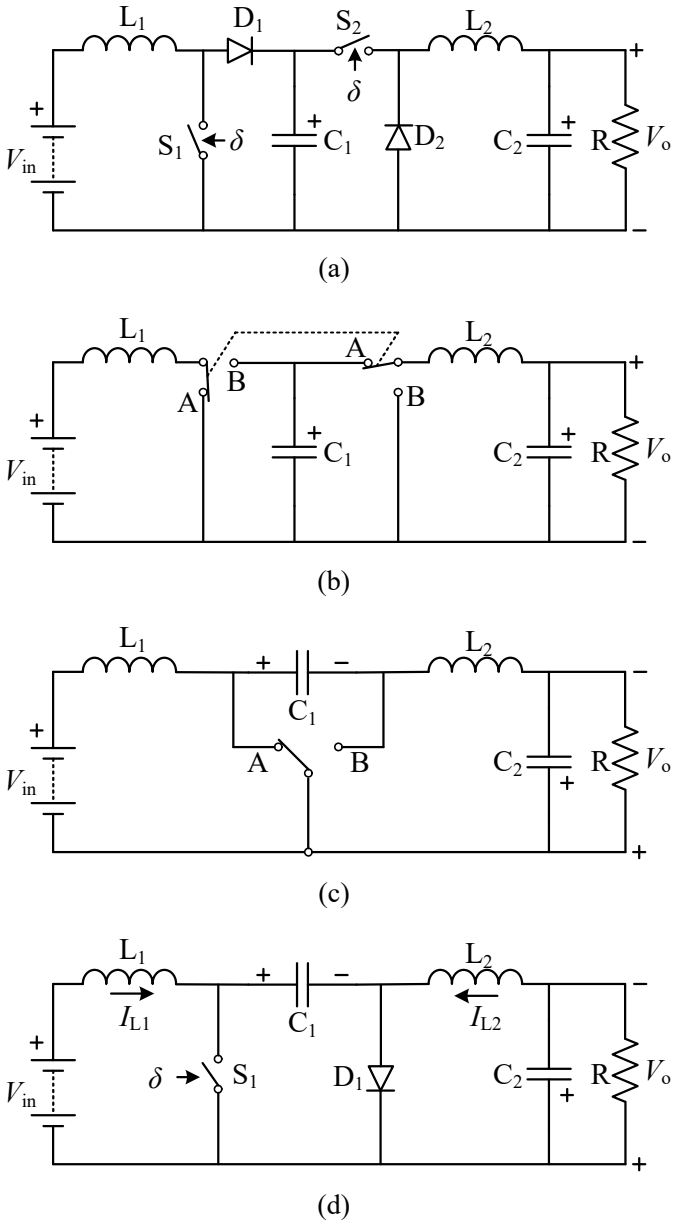


Fig. 1.3 Evolution of the Ćuk converter

(1) Compared with Buck, Boost and Buck-Boost converters, the Ćuk circuit has the

advantage of both continuous input and output current due to the inductor component at the input and output port.

(2) Unlike Buck and Boost converters (but like the Buck/Boost), the voltage transfer ratio of the Ćuk offers output voltage higher and lower than the input voltage.

(3) Compared with the Buck and Buck-Boost converter, the switch transistor emitter of Ćuk is grounded (with respect to the input and output). Thus, the driving circuit is simpler.

(4) Compared with a Buck converter with an input C filter and a Boost with an output C filter (4 components), the number of components is the one more (a second L).

1.4.2 Isolated Ćuk Converter

The transformer isolated Ćuk converter is shown in Fig. 1.4.

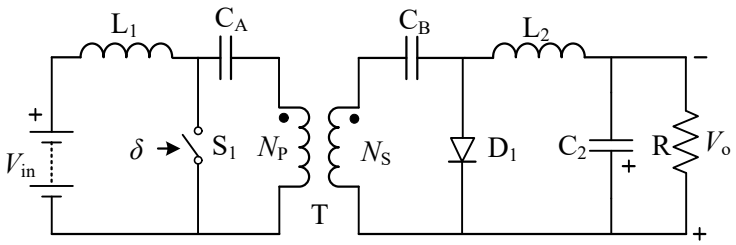


Fig. 1.4 The isolated Ćuk converter [2]

The isolated Ćuk converter transfer ratio is

$$\frac{V_o}{V_{in}} = -\frac{N_S}{N_P}\frac{\delta}{1-\delta} \tag{1-3}$$

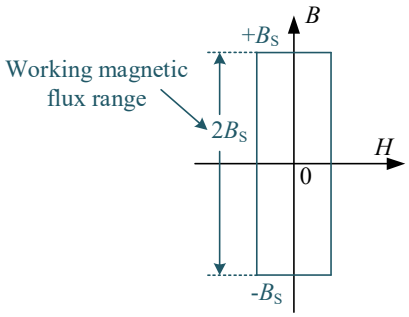


Fig. 1.5 Working magnetic flux range of the isolated Ćuk converter

This circuit has all the advantages of a Ćuk circuit. The magnetic state of the transformer core, as seen in Fig. 1.5, changes from - B_S to +B_S in the first part of a cycle and then from + B_S to - B_S in the second part of the cycle (with zero average current,

hence no net stored energy per cycle), fully utilizing the core volume capability. Therefore, at the same output power, the magnitude of the isolation transformer used is minimised, and the transformer design is that of a standard transformer. The two capacitors also act to blocking dc from the transformer.

1.5 Other Isolated Single Switch Converters [2]

Like the Ćuk converter (C5), the Zeta (G6) and Sepic (G6) converters can be transformer isolated, as shown in Fig. 1.6. The Zeta and Sepic converters offer other isolation methods. They not only can be isolated with a transformer (zero average current) and extra capacitor like the Ćuk converter (Fig 16 parts d, e, f) but can isolated by changing an existing inductor into a coupled circuit (dc biased average current) as in Fig 1.6 parts g and h, (with the capacitor retained as is).

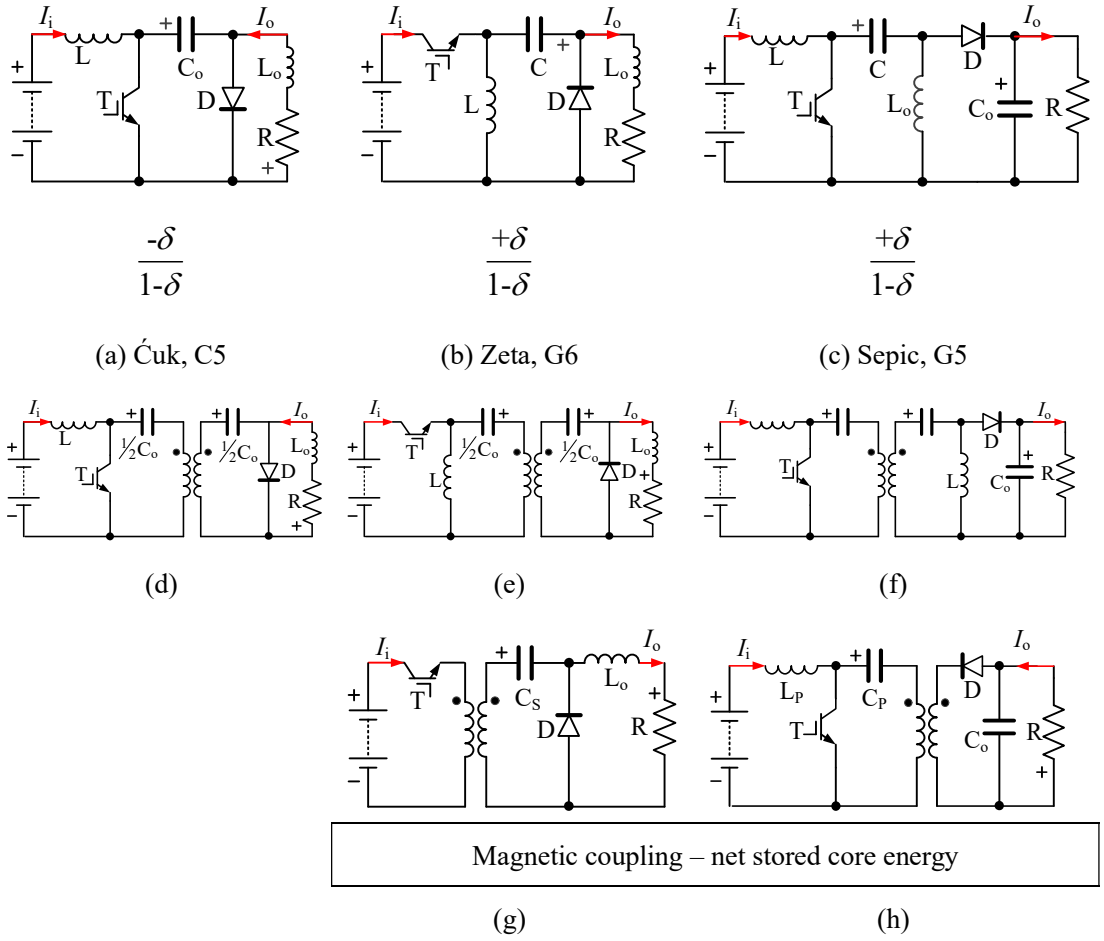


Fig 1.6 Isolation version of various single switch, two inductor dc/dc converters [2]

(a), (d) Ćuk C5, (b), (e), (g) Zeta G6, and (c), (f), (h) Sepic G5.

The main contribution of this thesis stems from the application of the two coupling methods available to the Sepic and Zeta (but not the Ćuk) converters. Specifically, any converter where energy is transmitted through

i. a ***series capacitor***, without any alternative shunt energy bypass paths, can have the series capacitor split into two with a transformer connected to the reference level.

ii. a ***shunt inductor*** connected to the input/output reference, can have that inductor replaced by a coupled magnetic circuit connected to the reference level.

If the above-mentioned transformations are carried out for both capacitors and inductors, it could render 30 different dc/dc converters [2], such topological conditions exist only in the D2 dc/dc converter, in Fig. 1.7.

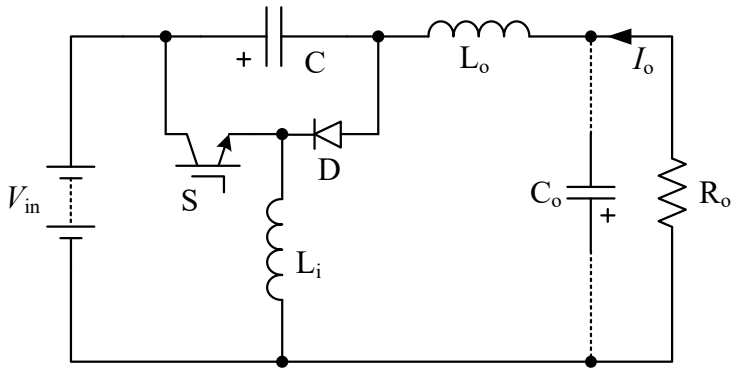


Fig. 1.7 D2 topology [2]

1.6 Other Transformer Variations (Isolation and Non-single Switch)

A novel modulation scheme for a bidirectional isolated pulse width modulation active-clamp (PAC)-Ćuk converter, in Fig 1.8, is presented in [3], where the optimality between the duty cycles and the ZVS constraints is simple to compute.

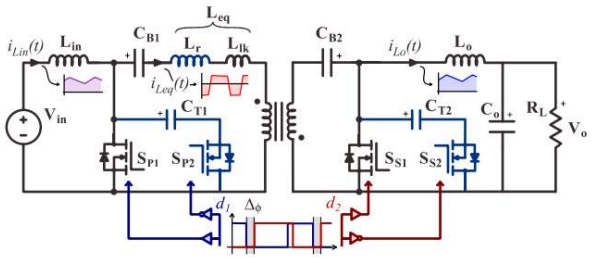


Fig. 1.8 Bidirectional PAC-Ćuk converter topology [3]

Paper [4] presents design guidelines of a bidirectional isolated Ćuk converter with an active-snubber circuit, Fig. 1.9, which is used as a cell level tester for multiple automotive dc energy storage devices (ESDs), such as ultracapacitors, Li-ion batteries,

and NiMH batteries.

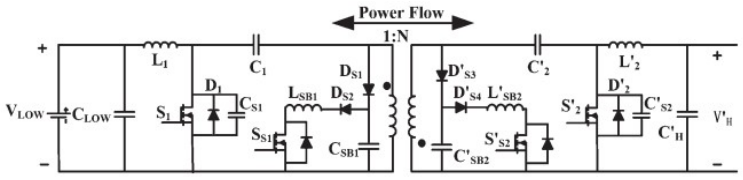


Fig. 1.9 Designed bidirectional isolated dc/dc converter [4]

A silicon-carbide (SiC)-based dc/dc converter [5], in Fig. 1.10 is developed for a manned solar aircraft for supply delivery in remote locations. The isolated Ćuk topology is augmented with a bridge to achieve four quadrant operation and minimize the worst-case processed power.

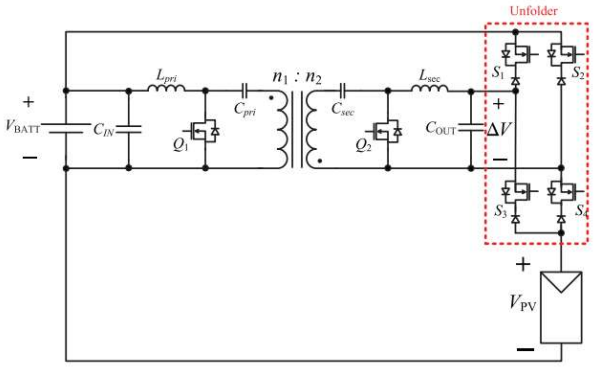


Fig. 1.10 Four-quadrant differential power processing isolated Ćuk converter [5]

A single-stage electric vehicle (EV) battery charger with an isolated bridgeless (BL) Ćuk–single-ended primary inductor converter (Sepic) converter, Fig. 1.11, is developed in [6]. The proposed charger design ensures a discontinuous conduction mode with intrinsic power factor correction (PFC) at ac mains.

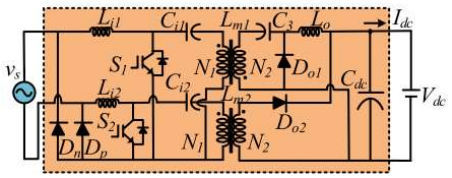


Fig. 1.11 The proposed BL isolated Ćuk-SEPIC converter [6]

Paper [7] presents a power factor correction (PFC)-based bridgeless isolated Ćuk converter-fed brushless dc (BLDC) motor drive, Fig. 1.12. A bridgeless configuration of an isolated Ćuk converter is derived to eliminate the front-end diode bridge rectifier, to reduce conduction losses.

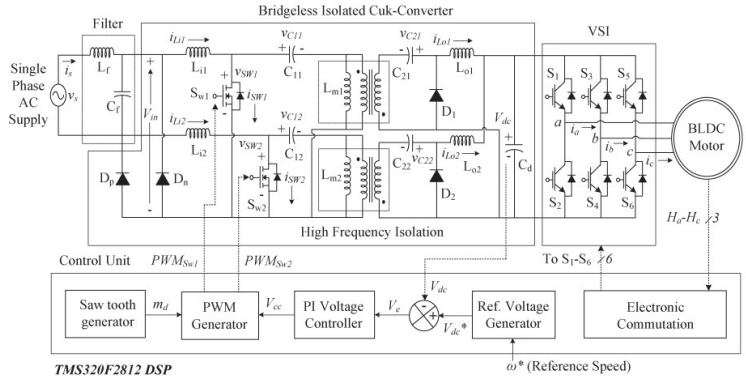


Fig. 1.12 A bridgeless isolated Ćuk converter-fed BLDC motor drive [7]

In paper [8], analysis and design of a three-phase isolated Ćuk-based PFC converter (Fig. 1.13) has been proposed that operates in the discontinuous output inductor current mode to achieve PFC at the three-phase ac input. Advantageously, it uses the existing ac line inductance as the Ćuk input inductor.

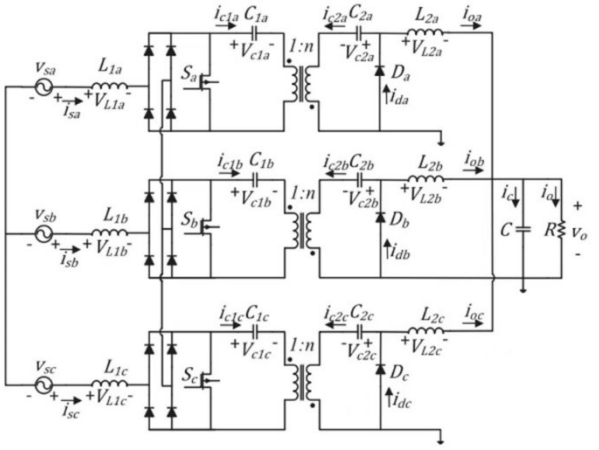


Fig. 1.13 Proposed structure of the three-phase-isolated Ćuk converter [8]

Article [9] discusses the modular three-phase ac/dc converter using single-phase isolated Ćuk rectifier modules, Fig. 1.13, as an effective single-stage solution for three-phase PFC in EV chargers. The converter is essentially the same as that in Fig. 1.14, but does not exploit the existing ac line inductance on the Ćuk input.

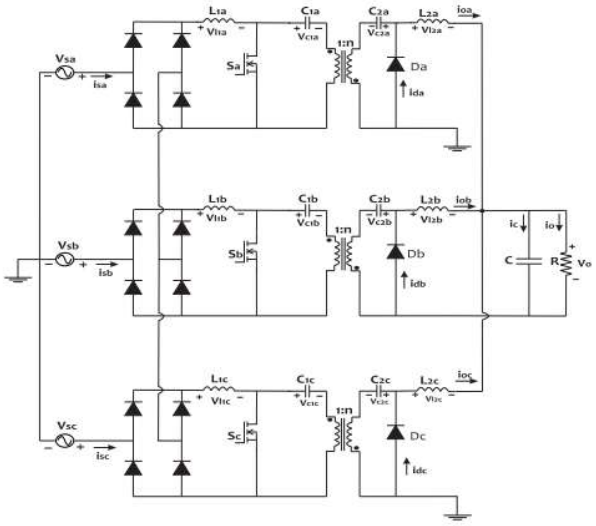


Fig. 1.14 The modular three-phase ac/dc converter using Ćuk rectifier modules [9]

In [10], a novel high voltage gain single-stage dc/ac converter, Fig. 1.15, is proposed for distributed energy resources. A Flyback-type auxiliary circuit is integrated with an isolated Ćuk-derived voltage source inverter to achieve a much higher voltage gain.

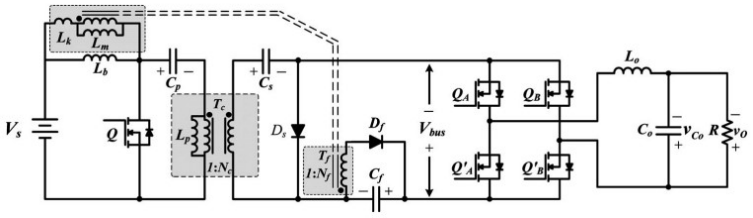
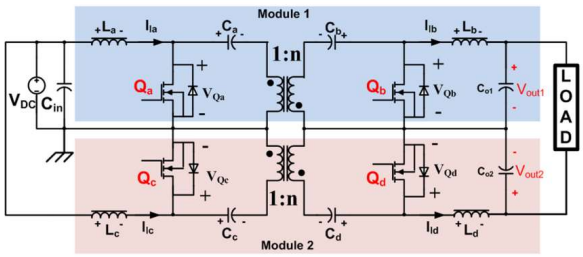
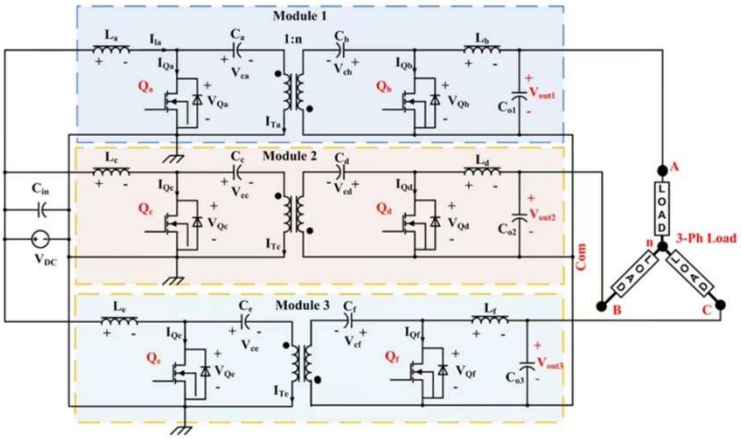


Fig. 1.15 Circuit configuration of the proposed single-stage inverter [10]

In [11], a modular control approach has been proposed for a single- and three-phase differential-mode Ćuk inverter (DMCI), Fig. 1.16, operating with a proposed discontinuous modulation scheme that offers tangible performance benefits over a conventional continuous modulation scheme.



(a) Single-phase DMCI



(b) Three-phase DMCI

Fig. 1.16 Circuit configuration of the proposed Ćuk inverter [11]

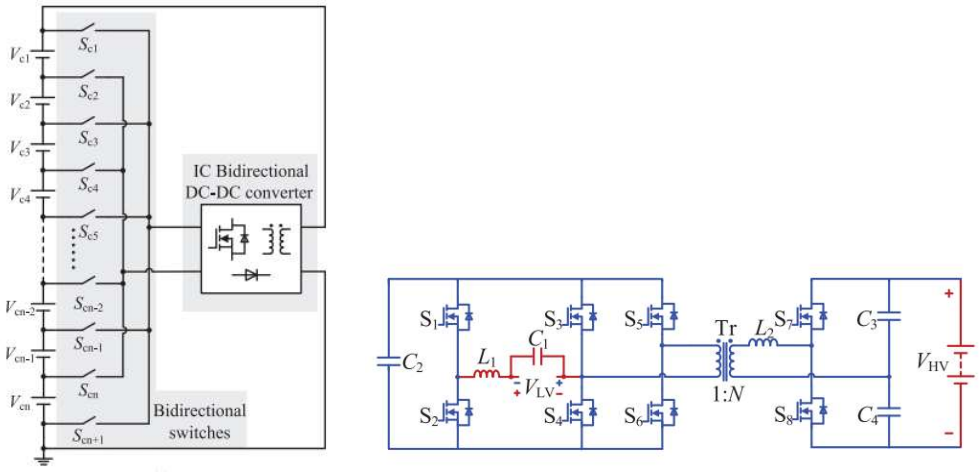
As has been discussed, the isolated Ćuk converter topology can be applied in many applications requiring isolation. It can achieve a high gain voltage with few switches. As an isolated dc/dc converter with its duality, it qualifies for the bidirectional flowing energy (two switches). So, isolated Ćuk converters are often used for EV charging and ac/dc microgrids. The isolated Ćuk can also be used as a single and three-phase PFC circuit, for isolation security.

1.7 Isolated Cascaded and Parallel Converters

1.7.1 Cascaded and Integrated

Cascading involves integrating two or more dc/dc converters, that is, merging the same structural parts and connecting different structural parts in series or parallel, thereby improving the voltage gain or output quality of the dc/dc converter.

In [12], an isolated bidirectional dc/dc converter (Fig. 1.17) with an integrated cascade structure is proposed for a centralized charge equalization system. The integrated cascade structure enables higher integration and higher reliability, and this converter solves the problem of achieving equalization with low cost and small volume for a long series-connected battery string.



(a) (b)

Fig. 1.17 Topology derivation of BBLLC

(a) The architecture based on an integrated cascade (IC) bidirectional dc/dc converter (b) Proposed integrated cascade bidirectional dc/dc converter. [12]

In [13] a novel integrated cascade bidirectional dc/dc converter is presented (in Fig 1.18) for optimizing a centralized charge equalization system. It attains outstanding performance in terms of equalization efficiency, modularity, impact on SOH and control complexity, and addresses the dilemma of achieving equalization with low cost and small size, for a long series battery string.

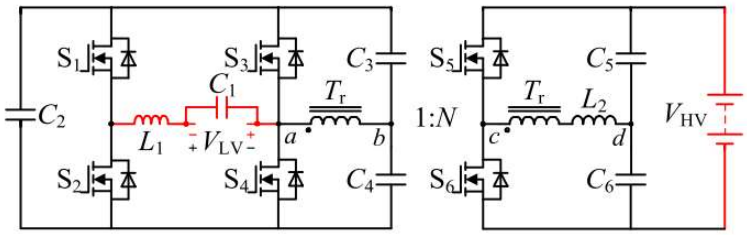


Fig. 1.18 Integrated cascade bidirectional dc/dc converter in [13]

Paper [14] investigates the unbalanced operating principle of a cascaded Modular multilevel converter–bidirectional dc/dc converter (MMC-BDC). The power range of the SMs is further deduced, and a fast-balancing charging method based on the power range analysis is put forward to balance the SOC of ESEs quickly and smoothly.

The current ripple of the combined Ćuk dc converter is reduced, the voltage stress is further reduced, and the degree of component damage is reduced. The Buck-Boost dc converter is combined with the zeta dc converter, where the input terminals of the two

converters are connected in parallel, and the output terminals are connected in series，resulting in an increase in voltage gain and a decrease in voltage stress. Combining two Zeta dc/dc converters increases voltage gain and reduces the volume of the dc converter, but the reduction is not ideal, further improving efficiency [15][16].

From this summary, cascaded and integrated converters can be applied in battery chargers, MMC, balancing charge, low current ripple, high voltage gain, etc.

1.7.2 Interleaved Parallel

Interleaved parallel connection is mainly used in high-power applications, as the input and output currents and ripple generated under high-power conditions are relatively large. Current ripple affects the reliability and stability of the converter and its performance and lifespan. In order to reduce current ripple, increase response speed, and reduce inductance volume, interleaved parallel connection technology can be adopted.

Reference [17] presents an optimized design process of high-power multi-phase interleaved bidirectional (non-isolated) Boost converters (Fig. 1.19). Generalized methods are developed for calculating the minimum inductance and capacitance required for a variety of phase numbers and different switching frequencies, which simplifies the design process.

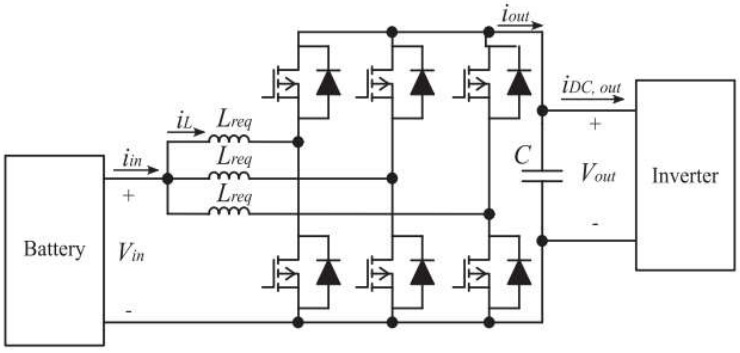


Fig. 1.19 Three-phase interleaved bidirectional synchronous Boost converter circuit for HEV application in [17]

An interleaved parallel LLC converter (Fig. 1.20) is proposed as a dc/dc converter for a digital off-board charger in accordance with the high output power requirements of modern electric vehicle chargers. The proposed converter utilizes a hybrid control strategy of pulse frequency modulation (PFM) and PWM that can increase the

adjustable output voltage range, and a smooth target voltage can be achieved [18].

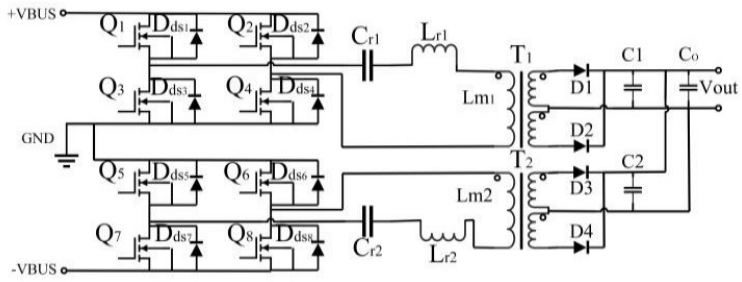


Fig. 1.20 Schematic diagram of the converter in [18]

To increase the maximum transmission power, [19] proposes a novel interleaved parallel bidirectional DAB converter, Fig.1.21.

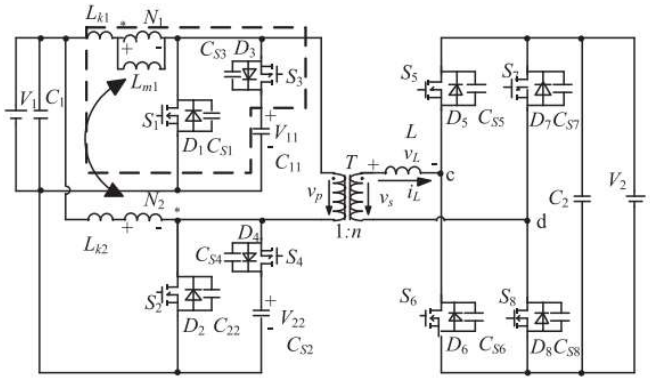


Fig. 1.21 Interleaved parallel bidirectional DAB converter topology in [19]

The effect of the interleaved carriers on the harmonic performance of the parallel connected VSCs is analysed in [20]. The closed-form analytical harmonic solution for the two paralleled interleaved VSCs, modulated by asymmetrical regular sampled DPWM1, is derived, and the reduction in the magnitude of some of the harmonic components is demonstrated in [20].

In some applications that require high-power converters to adapt to the large input current, the input inductance also needs to be increased, to avoid increasing the input current ripple. The use of an interleaved parallel structure converter topology can have two current ripples interleaved and superimposed. The duty cycle of the two phases of switch signals in the interleaved parallel converters is the same, with a phase difference of 180°, as can be achieved in Fig. 1.22. This reduces the input current ripple and output voltage ripple while reducing losses caused by inductance hysteresis. The basic interleaved parallel Boost converter topology has the advantage of a small input current

ripple, although it has a moderate impact on voltage. Fig. 1.23 shows an isolated dual inductor interleaved parallel converter, which can increase voltage gain and form an isolated structure but cannot flexibly adjust the duty cycle.

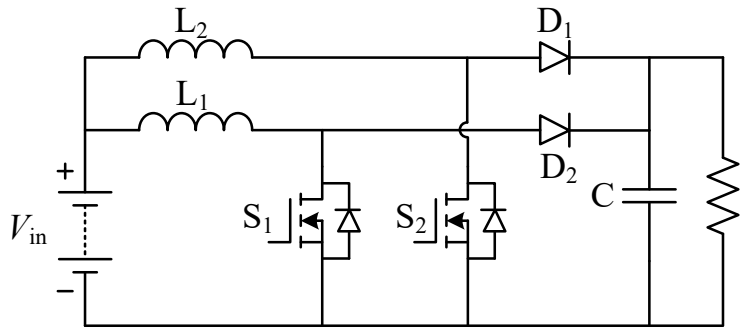


Fig. 1.22 Basic interleaved parallel Boost converter

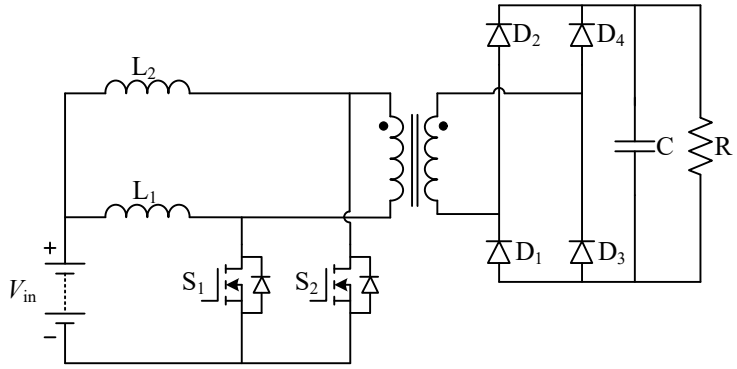


Fig. 1.23 Isolation type dual inductance interleaved parallel Boost converter

1.8 Example Isolated dc/dc Converter Applications

In this thesis, in later chapters, the proposed dc/dc isolated topology is investigated in three dc/dc applications: i. maximum power point track in photovoltaic power systems, ii. Input-parallel output-series, and iii. interleaved parallel technology. The next subsections provide the necessary overview background for the associated thesis chapter. Commensurate with the isolated converter bias of the research presented in this thesis, only isolated circuits and techniques are considered.

1.8.1 PV: MPPT

The power produced by PV systems is influenced by radiation and temperature, resulting in a constantly changing maximum power point that needs to be continuously monitored [21], [22], [23]. Various maximum power point tracking (MPPT) controls and their algorithms have been developed for PV systems [24]-[30]. Traditional MPPT methods in the literature include Perturb & Observe (P&Q), Incremental Conductance

(INC), Hill Climbing (HC), Constant Voltage (CV), Constant Current (CC), Fractional Open Circuit Voltage (FOCV), Adaptive Reference Voltage (ARV), Parasitic Capacitance (PC), Fractional Short Circuit Current (FSCC), Ripple Correlation Control (RCC), dc-link Capacitor Drop, On-Line MPP, Lookup Table, and Linearization-based methods [31], [32]. Among these methods, P&Q and INC methods have been extensively studied [33]-[36].

Modified INC is proposed to detect the occurrence of partially shaded conditions and enhance the tracking speed [37]. An advanced MPPT algorithm based on P&O and INC algorithms proposed in [38] provides fast-tracking of the MPP and detects any change in operating conditions while operating in a steady state. In [39], a fixed-step-size INC MPPT with a direct control method based on the Ćuk converter was employed. Paper [40] introduces an improved INC algorithm based on the mathematical residue theorem, and the improved INC overcomes the disadvantage of oscillation around the reference point. The paper [41] proposes a novel design of a fuzzy logic-based algorithm for varying the step size of the INC MPPT method for PV. MPPT efficiency is improved, and it enhances the output dc power and reduces the convergence time to reach steady state with intermittent environmental conditions. A novel self-adaptive INC provides quick tracking ability and reaches oscillation-free steady-state conditions [42]. Various INC MPPT methods on the charging of a battery load sourced from solar panels are analysed and compared. A superior MPPT tracking system uses a variable step size method [43].

A modified P&O MPPT algorithm is proposed to avoid drift problems [44]. The P&O algorithm was used to improve the MPP tracking rate [45]. Article [46] proposes a fixed zone P&O (FZPO) technique to achieve improved steady-state efficiency and fast and drift-free MPPT PV systems without additional sensors. A modified P&O technique was proposed to improve MPPT algorithm performance, which can deal with irradiance fluctuation during non-peak hours [47]. Paper [48] presents a new MPPT method for PV systems, taking the initial operating point of a PV system, then uses the short-circuit current method and later shifts to the conventional P&O technique. The algorithm does not need any irradiance/temperature sensor and improves stability and power harvesting

from PV modules. In [49], a proportional gain resonant and gain scheduled proportional (PR-P) controller-based variable perturbation size real-time adaptive P&O MPPT algorithm is presented. It resolved the drawbacks of the conventional P&O MPPT method associated with constant perturbation size that leads to poor transient response and high continuous steady-state oscillation.

The INC mainly depends on the slope of the power-voltage (*P-V* curve), whereas P&O has voltage as a control variable. It requires neither sensors for irradiation and temperature nor solar PV knowledge. Every MPPT technique has advantages and limitations, but MPPT requirements can be drafted with numerous parameters like sensors required, hardware implementation, cost viability, tracking speed and tracking efficiency [61].

1.8.2 Input Parallel Output Series (IPOS)

High input and high output voltage applications are emerging. However, the existing switching devices are limited by voltage stress. Several methods solve this issue, including a switch series connection, multilevel converters, and modular series-parallel structures, where modular series-parallel systems are the most popular choice due to the advantages of low cost, simple design process, high modularity, reliability, and redundancy [51] - [54].

Some dc/dc converters are cascaded to obtain high voltage gain with low input current ripple and low component stress. Paper [55] proposes a double IPOS hybrid switched-capacitor Boost converter with low voltage stress, small input current ripple and automatic current balancing. An IPOS multilevel Boost converter is proposed in [56], which has a high voltage gain, low component stress, small input current ripple, and an automatic current balancing function for all input inductor currents. Mixed conduction mode control for a bridgeless Boost PFC converter (IPOS Boost) is proposed to improve its power factor and reduce input current total harmonic distortion (THD_i) in light-load conditions [57]. To control voltage balancing between upper and lower voltages, a high-voltage gain IPOS Boost converter with inherent output voltage balancing capability has been developed [58]. Paper [59] introduces a symmetrical, high step-up, IPOS dc/dc converter based on voltage multiplier cells and active clamp

circuits to obtain a high voltage conversion ratio. With Fig. 1.24, a Ćuk-based modular dc/dc IPOS converter modular configuration can increase the voltage-blocking capability at the output and handle high currents at the converter input [60]. An IPOS partial power converter is considered a promising high-efficiency, high-density solution because only a fraction of power is processed via multistage converters to regulate the output voltage [61].

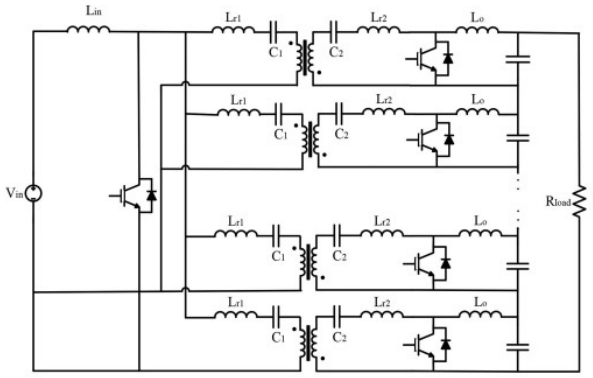


Fig. 1.24 The proposed modular converter with a reduced number of components [60]

A full-bridge is widely used in IPOS applications, especially the dual active bridge (DAB). The IPOS LLC resonant converter in Fig. 1.25, with a coupled transformer and current-sharing capability, is proposed for high-gain, high-efficiency applications [62]. Paper [63] investigates an offshore wind farm based on a modular DAB-isolated dc/dc converter with droop voltage balancing control. The phase-shifted full-bridge based IPOS converter [64] with the modified connection of the output filter, for a wide input voltage variation, reduces filter inductor ripple current. The isolated inverter composed of cascade isolated bridge cells (I-BCs) connected in IPOS, in Fig. 1.26, offers good performance for the PV grid connection [65]. Paper [66] proposes a novel nonlinear control method for the IPOS modular dual active bridge (DAB) dc/dc converter, which regulates the dc bus voltage and individual module voltages simultaneously. The converter in [67] consists of a full-bridge dc/dc converter with active rectifier IPOS connected modules, which achieves zero voltage switching for all primary side switches and zero current switching for all secondary side switches and diodes.

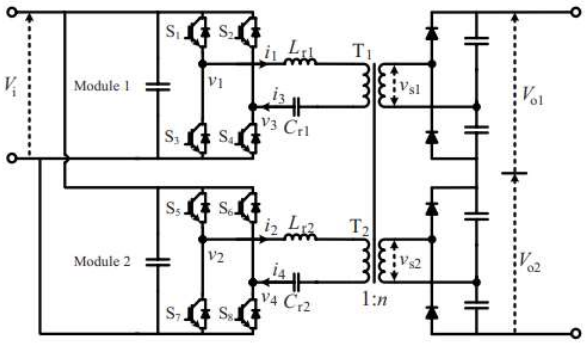


Fig. 1.25 IPOS LLC converter with coupled transformer [62]

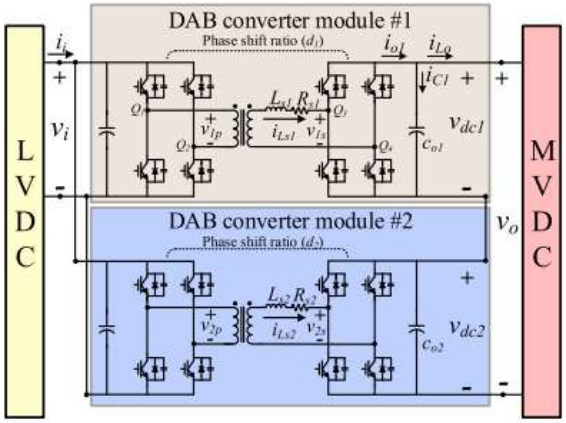


Fig. 1.26 High-frequency-link isolated bridge converter [65]

IPOS systems have an auto-balancing mechanism, so in a dc grid-connected renewable power system, IPOS is used to realize power balancing. An IPOS system can also be applied in large-scale PV generation connected to a HVDC grid. The output voltage of the IPOS system is maintained constant within a modular multilevel converter so can be used to control output current when realizing MPP tracking.

1.8.3 Interleaved Parallel Connections

The interleaved parallel method of converter connection can be applied when the input current is relatively high. This method can improve output voltage, reduce input current pulsation, and increase converter capacity to share power losses, which improves system stability.

Paper [68] analyses interleaved parallel converters, and results show that the superposition of N interleaved triangular waveforms with identical amplitudes and duty ratios is equal to another single triangular waveform whose net amplitude, effective duty ratio, and effective frequency can be specified in terms of the original parameters

in closed form. Some basic dc/dc converters are connected in parallel and operated in an interleaving mode for ripple reduction in the source current and output voltage [69]. This reduces the current ripple, and the proposed interleaved Boost converter can improve the power handling capabilities and increase the overall system rating. Paper [70] presents an optimized design process of high-power multi-phase interleaved bidirectional Boost converters, which offers benefits to hybrid and electric vehicles because higher-voltage propulsion power equates to lower motor losses.

Interleaving of resonant converters reduces the requirement of input and output passive filters, providing better dynamic performance and higher power density. In [71], a novel single-phase interleaved parallel cascaded three-level (IPC-TL) power factor correction (PFC) converter is proposed. It exhibits the merits of lower inductance volt-second and inductor current ripple, lower common-mode noise, and lower control cost compared with the traditional IPC-TL topology. An interleaved LCLC resonant converter has accurate current balancing performance over a wide input voltage range [72]. The n-phase interleaved LLC resonant converter in [73] utilizes existing magnetics of resonant inductors and balances the output, input, and tank currents without increasing the active or passive components and without dedicated controls and expensive sensors. The multiphase interleaved inductive power transfer-based dc/dc converter in Fig. 1.27 is implemented in [74] into an n-phase system, reducing output current ripple[74]. The interleaved parallel LLC converter in [75] is proposed as a dc/dc converter for a digital off-board charger in accordance with the high output power requirements of modern electric vehicle chargers.

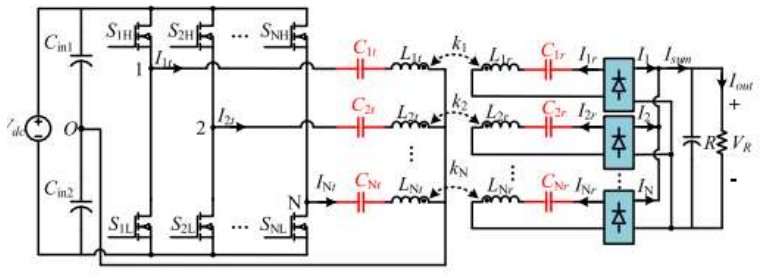


Fig. 1.27 Proposed multiphase IPT based current-source dc/dc converter in [74]

The full-bridge is also cascaded in interleaved parallel, and DAB converters are used in this application for bidirectional power transfer and galvanic isolation. A two-phase

interleaved phase-shift full-bridge converter with transformer winding series-parallel autoregulated current doubler rectifier [76] reduces output filter current ripple and decreases filter size. The interleaved DAB and non-isolated dc/dc structure in Fig. 1.28 has good dynamic characteristics, and the current ripple can be reduced, so an improved battery lifecycle is expected [77].

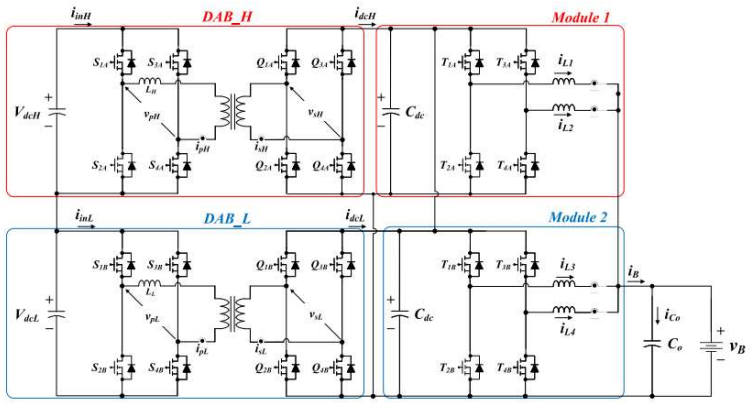


Fig. 1.28 The proposed converter structure in [77]

Interleaved parallel refers to not only converter cascading but also PWM modulation and its strategy. A simple decentralized interleaving PWM approach is proposed for parallel grid-tied converters to reduce switching current ripple at the point of common coupling [78]. Paper [79] proposes an improved interleaved discontinuous PWM method to reduce zero-sequence circulating currents (ZSCC) in paralleled converters and switching losses, with ease of use and scalability. An IPOP three-level dc/dc converter associated with an interleaving control strategy is proposed to minimize and balance capacitor ripple current [80].

Interleaved parallel topologies are based on staggering switch transitions of many parallel converters so that the current ripple of each converter cancels when summed at a common load. Ripple cancellation and interleaving in converter systems and control strategies are widely used in power electronics.

1.9 Other Converter Applications

1.9.1 Power Factor Correction (PFC)

PFC converters with nonlinearities connected to the grid, can degrade ac power quality [81]. The main desired features of a PFC converter are (typically):

- continuous sinusoidal input current;

- THD < 5%;
- $pf \geq 0.9$;
- efficiency ≥ 95% at varying load conditions and line voltage levels;
- flexible step-up and step-down chopper behaviour;
- simplified control of input ac current and output dc voltage;
- reduced semiconductor device, passive elements, filter size, converter size;
- reduced control sensors and simplified control;
- reliability, cost-effective, high power density; and
- reduced Electromagnetic Interface (EMI) noise

In the following subsections, PFC converters are classified into three converter categories: basic dc/dc converter based PFC converter, bridgeless PFC converter, and interleaved PFC converter.

Single-phase PFC stages ideally have three features: operation over a long life span, soft switching at high frequency, and a reasonably low output voltage. These features permit a high power factor, power density and efficiency, and reduced stress on subsequent stages [82]. This category of PFC converter is composed of a diode bridge rectifier (DBR) and a non-isolated single-switch converter, such as Buck, Boost, Buck-Boost, Sepic, Ćuk, and Zeta or combines a DBR and an isolated converter, such as push-pull, half-bridge, full-bridge, multi-level converter and so on [83] - [86].

i. Buck PFC Converter

The Buck PFC converter is an efficient option for low-voltage applications with unlimited lower-limit voltage. However, the input current ripple is high in the Buck PFC converter. The duty cycle is from 0 to 1, which is limited, and its dead-angle issue in the DCM leads to a few applications using the Buck PFC converter.

Paper [91] investigates a six-level flying capacitor multilevel (FCML) Buck PFC converter. It follows portions of the rectified input voltage by swinging at twice-line frequency. A single-phase three-level flying-capacitor PFC rectifier [88] with active pulsating power buffering-embedded switching with a higher pf and a lower THD has reduced voltage and current stress, magnetic and capacitive footprint. A hybrid switched-inductor (HS-L) Buck-type PFC with a coupled inductor can be used to

improve the efficiency of a LED driver [89]. A series-capacitor-based Buck-type PFC converter can achieve ultrahigh step-down conversion ratio, high PF and switch soft turn-on [90]. The Buck PFC converter is usually connected with other components, such as a flying-capacitor, switched-inductor and so on, to avoid its shortcomings and realize a higher power factor.

ii. Boost PFC Converter

Boost converters are widely employed within PFC converters. They can be modified with a switched capacitor converter and voltage multiplier techniques to attain higher output voltage.

The One Cycle Control (OCC) is a viable PFC control strategy for traditional converters used in PFC applications [91]. Boost-type PFC converters can reduce device voltage stress, input current harmonics, sensors and system volume and improve input PF [92], [93] - [95]. A Boost-type PFC converter integrated with a soft switching resonant converter is proposed to achieve higher PF, recycle the transformer leakage inductance, reduce switching losses, and improve efficiency [96].

iii. Zeta and Other PF Correction Converters

A two-switch isolated Zeta PFC converter in Fig. 1.29 is proposed [97] for arc welding, which can reduce switch stress and operate in a DCM to achieve inherent pf correction at the utility. A Zeta PFC converter to yield improved THD of ac mains current with near unity pf under a wide range of input voltages and loads, is proposed in [98]. A modified Sheppard–Taylor PFC converter features zero-voltage turnoff switching and natural purely resistive behaviour at low dc output voltage levels [99]. A senseless multilevel rectifier with PFC can maintain unity PF at the input side, is suitable for medium to high load handling capability and suits electric vehicle chargers, dc conversion stage for drives. and LED driver applications [100].

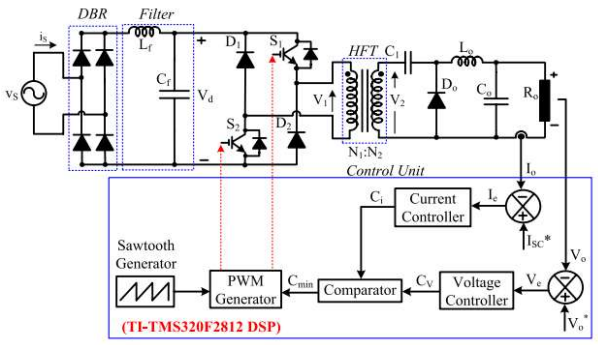


Fig. 1.29 A modified Zeta converter-based AWPS [97]

iv. Combination Converter

Boost and Buck converters are integrated as a PFC converter to obtain high PF and low current harmonics at the input line and regulate the dc link voltage [101]. Paper [102] proposes the Boost-flyback PFC converter in Fig. 1.30 that operates in DCM, which can achieve high PF and high efficiency, reduce switch voltage stress, and provide input-output electrical isolation for safety. A new star PFC architecture combines the Boost converter and half-bridge PFC converter to operate efficiently, leading to high-power density and efficiency [103]. The multitrack PFC architecture in [104] combines a Boost converter and a magnetic isolation stage to reduce the internal device voltage stress and maintain zero-voltage-switching at high frequency.

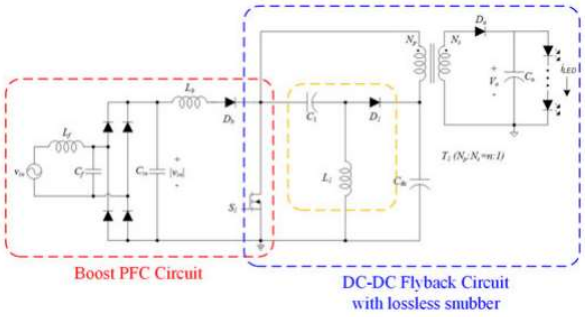


Fig. 1.30 Boost-flyback PFC converter in [101]

The combination PFC converter features two integrated converter characteristics, like electrical isolation for safety, wide operation range and simple control.

v. Interleaved PFC

Compared with the single-phase PFC converter, the interleaved PFC converter can reduce input and output current ripple, reduce switching device current stress, and improve conversion power and power density due to being multi-phase.

An interleaved Boost PFC converter [105] features soft switching, no reverse recovery loss, high efficiency, simple control, and a greater static gain. A ZVS interleaved Boost PFC converter is designed to charge the traction battery of an electric vehicle from the utility mains [106]. The interleaved Boost PFC converter can also improve the efficiency, PF, volume and flux density [107] [108] [109]. The novel two-inductor, interleaved Boost PFC converter in [110] exhibits voltage-doubler characteristics and is suitable for a universal line (90 - 264 V_{RMS}).

Fully utilizing phase-shift can achieve more functions. An interleaved totem-pole bridgeless Boost PFC converter with soft-switching capability can achieve ZVS by applying the phase-shifting control between two PFC converter units, resulting in high efficiency and reduced conduction loss [111]. A new front-end ac/dc bridgeless interleaved PFC topology is proposed in [112] for level II plug-in hybrid electric vehicle battery charging, which reduces charging time[112].

Some unique control methods are applied in interleaved PFC converters, which can generate unexpected results. A digital adaptive current source driver is proposed for the interleaved Boost PFC converter, which optimizes the switching loss and gate drive loss according to different turn-on and turn-off drain currents over a wide load range [113]. A cross-coupled master-slave interleaved control method for BCM PFC converters responds to the disturbance on the PS within one switching cycle [114]. An interleaved isolated PFC converter with an IPOS structure with a wide output voltage range is used to three-phase charge EV [115].

Interleaved PFC converters have many characteristics, such as unity PF, soft switching, no diode reverse recovery loss, auto-balance of currents between the semiconductors, the static gain is twice that of conventional boost, and current or input voltage sensors are not required, that is, no current loop need, so interleaved PFC converters are widely used in high-power requirements, like EV charging.

1.9.2 Single-phase inverter (dc/ac)

In general, single-phase, single-stage inverters are categorized into four topologies: Full-bridge/H-bridge, Buck-Boost, Flyback type chopper and Z-source inverters.

A single-phase H-bridge inverter adapts an active double-frequency power ripple

decoupling method without additional power electronics in [116]. One cycle control (OCC) based on a single-phase H-bridge inverter is applied in PV distributed generation systems for its cost-effectiveness, simple structure, and phase-locked loop-free implementation [117]. In [118], dual-comparison OCC is used for bidirectional power flow in single-phase grid-connected full-bridge converters without any steady-state dc offset and light-load instability, and implements unipolar PWM without a grid voltage sensor. In general, H-bridge-type inverters, usually based on OCC, are applied in small single-phase PV distributed generator systems because of their simplicity, PLL-free structure, grid voltage sensor-less operation, and cost-effectiveness [119].

A new bidirectional single-phase Buck-Boost inverter topology guarantees minimum capacitance requirement, regulates dc-port and ac-port currents, manages mismatch of input and output power, steps up or down the dc voltage in a single power conversion stage, and reduces switching loss and semiconductor device stress [120].

Some novel topologies can be derived as inverters, which can achieve numerous functions. A dual-stage matrix converter for single-phase inversion [121] eliminates the bulky dc-link energy storage element across the intermediate stage, which is suitable for low-power applications. The number of output phases in this converter can be increased by adding the desired number of legs.

i. Single-phase Inversion Control

Phase, amplitude and frequency are significant factors in the control of grid-connected systems inverters, rectifiers and energy restorers [122] - [125]. Numerous control solutions have been proposed, involving discrete Fourier transform (DFT), Kalman filter, least-square estimation, adaptive notch filter (ANF), delayed signal cancellation (DCS), linear observer, harmonic oscillators (linear and nonlinear), PLL, demodulation-based techniques, open-loop techniques, etc.

Paper [126] proposes a linear observer technique to solve phase and frequency estimation problems with the single-phase grid voltage signal in the presence of dc offset and harmonics. To achieve grid synchronization, a state observer-based approach and a frequency adaptation law [127] guarantee estimation error dynamics and global asymptotic convergence of the estimated parameters in the fundamental frequency case.

Of the various techniques, PLL receives widespread attention due to its excellent performance and a simple structure. A new single-phase synchronous reference frame PLL based on DFT offers better harmonics immunity and dc component rejection capacity and incorporates grid frequency variations [128]. A nonadaptive moving average filter (MAF) quadrature signal generator with error compensators, reduces the complexity of conventional MAF and maintains good performance, in [129]. A single-phase, single-loop PLL-based phase shift keying method is employed to detect the phase [130]. The transfer delay-based PLL in [131] removes phase offset and double-frequency ripple errors and is simple and efficient. A Park-based *dq* frame single-phase PLL which removes double-frequency oscillatory, is based on a linearized model [132]. Second-order generalized integrator (SOGI) based PLL restrains the performance under varying frequency and distorted grid voltage conditions [133]. It has been widely discussed and used for its simplicity, good filtering ability, and frequency adaptability. Different techniques of single-phase SOGI-PLL are analysed and compared in [134]. Self-Tuning-SOGI-PLL (SSOGI-PLL) has a good dynamic response to grid voltage sag; Modified-SOGI-PLL (MSOGI-PLL) has a good dynamic response to phase angle change; SOGI-PLL with-a prefilter (SOGI-PLL-WPF) technique suppressed harmonics better; SOGI-PLL-WPF and MSOFI-PLL have a good performance in eliminating dc offset. The SOGI-PLL has a fast dynamic response and improves response time under different grid disturbances [135].

1.10 Thesis Structure and Research Contents

The thesis proposes a new isolated single transformer topology derived from the D2 converter [2]. The main contributions of the thesis are that the mathematical model is built, and core flux ripple cancellation with a single transformer core with four windings is proposed. Practical dc/dc applications based on the proposed topology; super-capacitor charge, PV, IPOS, and interleaving, three cascaded isolated D2 converters in PFC applications and a novel primary side one switch and two switches secondary side inverter derived from the isolated D2 converter are verified through simulation and experimentation.

This thesis is divided into the following six chapters:

This chapter**, Chapter 1**, introduces common isolated and non-isolated converters and additionally presents PWM-type dc/dc converter design progress and general circuit characteristics analysis. Because the proposed isolated D2 converter shares similarities to the Ćuk converter, the evolution, transfer ratio, characteristics, comparison, and applications of Ćuk and isolated Ćuk converters are presented. Three applications applicable to the new isolated D2 converter are introduced (since they are explored in later chapters): dc/dc conversion, power factor correction and single-phase inversion.

Chapter 2 proposes the isolated D2 converter, and includes its derivation, topology, dynamic model and mathematical model. Feasibility analysis is conducted through simulation and experimentation. Attention is given to the transformer hardware structure and design.

Chapter 3 presents the isolated D2 converter in three dc/dc applications: maximum power point tracking, input-parallel output-series cascaded, and interleaved parallel connection. The principles, modulation strategies, and control methods are explained via simulation and experimentation.

Chapter 4 presents the application of power factor correction. The proposed isolated D2 converter in two modes (bridgeless converter and interleaving converter), suppresses harmonic pollution and improves power supply quality.

Chapter 5 presents the isolated D2 application to single-phase inversion (dc/ac), using SPWM modulation and second-order generalized integrator control. Both simulation and experimentation validate that the inverter can generate ac power, in a stand-alone mode, and can be grid connected.

Chapter 6, the conclusions, involves summarised conclusions of the thesis, highlights of the research contribution, plus future research.

CHAPTER 2 The Isolated D2 Converter

This thesis researches a novel one-switch isolated dc/dc converter called an isolated D2 converter. This chapter analyzes the isolated D2 converter in terms of derivation, circuit model, controllability, finite element analysis, and efficiency. Another contribution highlighted in this chapter is that D2 converter isolation can be achieved with a single transformer core with four windings, offering core flux ripple cancellation. The current ripple and flux plots of different transformer coupling orientations are considered.

2.1 Isolated D2 Converter Topology

Analysis starts with, and stems from, consideration of the non-isolated D2 converter.

2.1.1 Isolated D2 Converter Derivation

Ćuk, Zeta and Sepic are basic common (2 inductors and one switch) dc/dc converters. The topologies and voltage transfer ratios were given in Chapter 1, Fig. 1.6. The D2 dc/dc converter has the input inductor L_{in} connected to the negative pole of the dc power supply and the switch S and diode D, are connected as shown in Fig. 1.7 and Fig. 2.1 of this chapter. The output series inductor affords continuous output current possibilities. According to the inductor volt-sec balance, the voltage transmission ratio of D2 is

$$\frac{V_o}{V_{in}} = -\frac{\delta}{1-\delta}$$

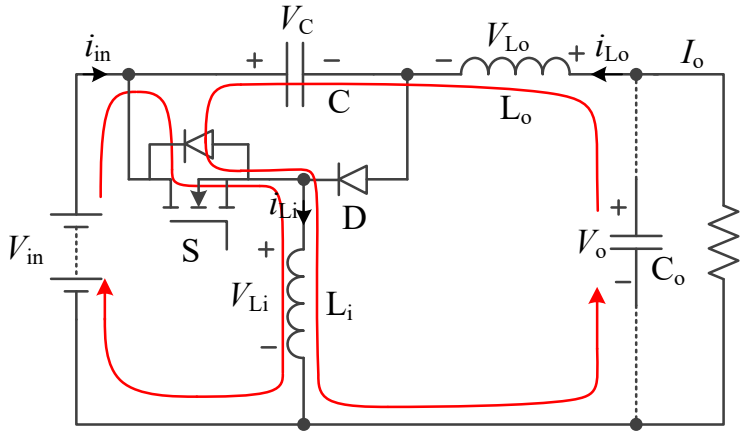
This transfer ratio is established as follows.

When the switch is ON:

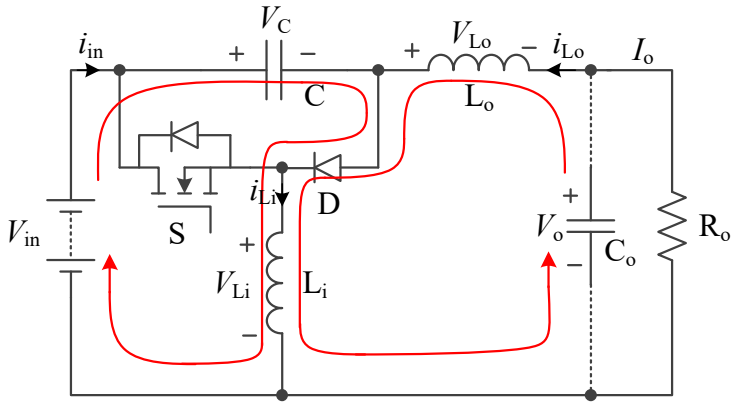
$$\begin{cases} V_{L_i} = V_{in} \\ V_C - V_{L_o} - V_{L_i} = V_o \end{cases} \tag{2-1}$$

When the switch is OFF:

$$\begin{cases} V_{L_i} + V_C = V_{in} \\ V_{L_o} - V_{L_i} = V_o \end{cases} \tag{2-2}$$



(a) Switch ON



(b) Switch OFF

Fig. 2.1 Two states of the D2 converter in CCM

So, when the switch is ON, with on-state duty cycle δ:

$$\begin{cases} V_{L_i} = V_{in} \\ V_C - V_{L_o} - V_{L_i} = V_o \end{cases} \Rightarrow \begin{cases} L_i \dfrac{\Delta i_{L_i}}{\delta T} = V_{in} \\ V_C - L_o \dfrac{\Delta i_{L_o}}{\delta T} - V_{in} = V_o \end{cases} \Rightarrow \begin{cases} \Delta i_{L_i} = \dfrac{V_{in} \bullet \delta T}{L_i} \\ \Delta i_{L_o} = \dfrac{(V_o + V_{in} - V_C) \bullet \delta T}{L_o} \end{cases} \tag{2-3}$$

Assuming continuous inductor L_i current, when the switch is OFF:

$$\begin{cases} V_{L_i} + V_C = V_{in} \\ V_{L_o} - V_{L_i} = V_o \end{cases} \Rightarrow \begin{cases} L_i \dfrac{\Delta i_{L_i}}{(1-\delta)T} + V_C = V_{in} \\ L_o \dfrac{\Delta i_{L_o}}{(1-\delta)T} - L_i \dfrac{\Delta i_{L_i}}{(1-\delta)T} = V_o \end{cases} \tag{2-4}$$

Substituting equation (2-3) into equation (2-4):

$$\begin{cases} L_i \dfrac{\Delta i_{L_i}}{(1-\delta)T} + V_C = V_{in} \\ L_o \dfrac{\Delta i_{L_o}}{(1-\delta)T} - L_i \dfrac{\Delta i_{L_i}}{(1-\delta)T} = V_o \end{cases}$$

$$\Rightarrow \begin{cases} \dfrac{L_i}{(1-\delta)T} \bullet \dfrac{V_{in} \delta T}{L_i} + V_C = V_{in} \\ \dfrac{L_o}{(1-\delta)T} \bullet \dfrac{(V_o + V_{in} - V_C)\delta T}{L_o} - \dfrac{L_i}{(1-\delta)T} \bullet \dfrac{V_{in} \delta T}{L_i} = V_o \end{cases} \tag{2-5}$$

$$\Rightarrow \begin{cases} V_C = \dfrac{1-2\delta}{1-\delta} V_{in} \\ V_C = \dfrac{2\delta - 1}{\delta} V_o \end{cases}$$

Eliminating the capacitor voltage V_c:

$$\frac{1}{1-\delta}V_{\text{in}} = -\frac{1}{\delta}V_{\text{o}}$$

$$\frac{V_{\text{o}}}{V_{\text{in}}} = -\frac{\delta}{1-\delta}$$

According to ac equivalent circuit theory and inductor and transformer coupling (Fig. 2.2), the D2 converter can be converted into an isolated topology. In this thesis, the topology Fig. 2.3 shows the so-called isolated D2 converter. These transformations have been exploited to isolate the Ćuk, Zeta and Sepic converters

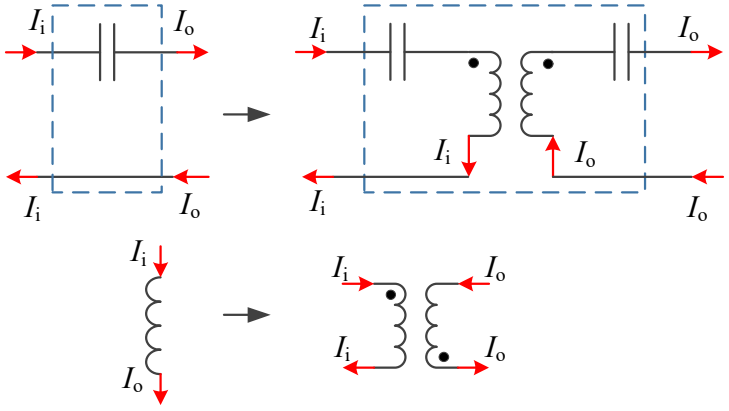


Fig. 2.2 ac equivalent circuits

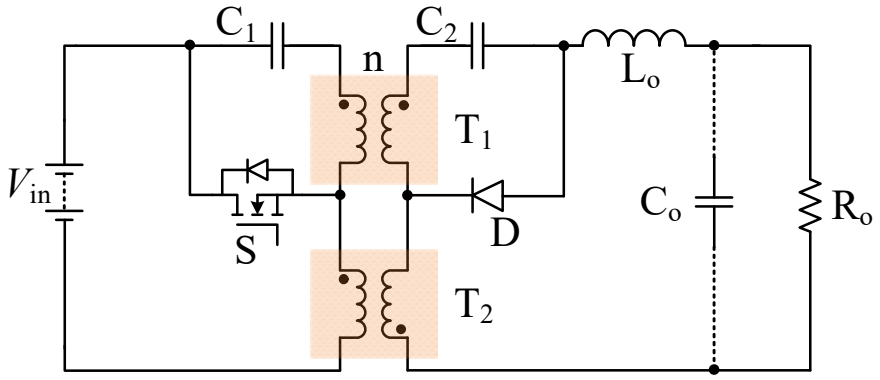
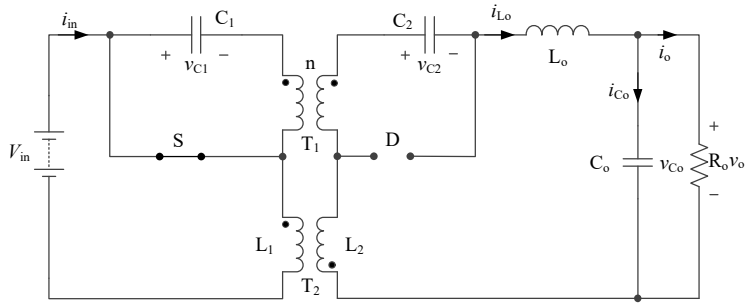


Fig. 2.3 Isolated D2 Converter

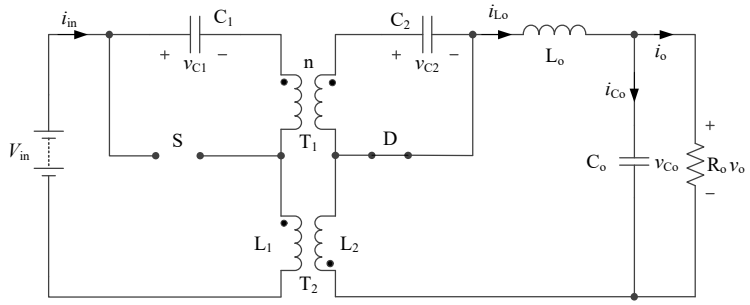
The isolated D2 converter (initially) contains two high-frequency transformers, T_1 and T_2, two coupling dc blocking capacitors, C_1 and C_2, an output inductor L_o, an output filter capacitor C_o, a power diode D and a power switch S. According to volt-sec balance, the transformer isolated D2 converter voltage transmission ratio is

$$\frac{1}{1-\delta}V_{in} = -\frac{1}{n\delta}V_o$$
$$\frac{V_o}{V_{in}} = -\frac{n\delta}{1-\delta} \tag{2-6}$$

2.1.2 Modelling of the Isolated D2 Converter



(a) Switch ON



(b) Switch OFF

Fig. 2.4 Isolated D2 dc/dc converter operation

The operating principle of the isolated D2 dc/dc converter is explained by the switch's ON and OFF positions. When the power switch is ON, T_2 stores energy, and C_1 charges C_2 via the power switch, diode, and high-frequency transformer. L_o transfers its energy to the load via the power diode. When the power switch is OFF, C_1 is charged by T_2 and the input source and C_2 discharges into L_o and the load.

The passive component requirements of the converter can be calculated using (2-7) to (2-11). For a CCM mode (continuous inductor current) of operation, inductor values should be higher than the calculated values to follow [136].

$$T_2 = \frac{R_o(1-\delta)^2}{2\delta f_s n^2} \tag{2-7}$$

$$L_{\mathrm{o}} = \frac{R_{\mathrm{o}}\left(1-\delta\right)^{2}}{2f_{\mathrm{s}}} \tag{2-8}$$

$$C_{1} = \frac{V_{\mathrm{in}} n^{2} \delta^{2}}{\left(1-\delta\right)\Delta V_{\mathrm{C1}} f_{\mathrm{s}} R_{\mathrm{o}}} \tag{2-9}$$

$$C_{2} = \frac{V_{\mathrm{o}}\delta}{\Delta V_{\mathrm{C2}} f_{\mathrm{s}} R_{\mathrm{o}}} \tag{2-10}$$

$$C_{\mathrm{o}} \geq \frac{V_{\mathrm{o}}\left(1-\delta\right)}{8L_{2}\Delta V_{\mathrm{Co}} f_{\mathrm{s}}^{2}} \tag{2-11}$$

In order to derive the state-space mathematical model of the converter, Kirchhoff's voltage and current laws are applied to the switch's ON and OFF circuits separately. The model can be derived for the switch ON position as in (2-12)-(2-17).

$$\frac{\mathrm{d}i_{\mathrm{in}}}{\mathrm{d}t} = \frac{V_{\mathrm{in}}}{L_{1}} \tag{2-12}$$

$$\frac{\mathrm{d}V_{C1}}{\mathrm{d}t} = \frac{-ni_{Lo}}{C_{1}} \tag{2-13}$$

$$\frac{\mathrm{d}i_{Lo}}{\mathrm{d}t} = \frac{-nV_{\mathrm{C1}}}{L_{\mathrm{o}}} - \frac{V_{\mathrm{C2}}}{L_{\mathrm{o}}} - \frac{V_{\mathrm{o}}}{L_{\mathrm{o}}} - \frac{V_{\mathrm{in}}}{L_{\mathrm{o}}} \tag{2-14}$$

$$\frac{\mathrm{d}V_{\mathrm{C2}}}{\mathrm{d}t} = \frac{-i_{\mathrm{Lo}}}{C_{2}} \tag{2-15}$$

$$\frac{\mathrm{d}V_{\mathrm{o}}}{\mathrm{d}t} = \frac{i_{\mathrm{Lo}}}{C_{\mathrm{o}}} - \frac{V_{\mathrm{o}}}{R_{\mathrm{o}}C_{\mathrm{o}}} \tag{2-16}$$

$$\frac{\mathrm{d}V_{\mathrm{o}}}{\mathrm{d}t} = \frac{i_{\mathrm{Co}}}{C_{\mathrm{o}}} \tag{2-17}$$

$$i_{\mathrm{L2}} = i_{\mathrm{Lo}} - i_{\mathrm{Co}} \tag{2-18}$$

$$\begin{bmatrix} \dot{i}_{\text{in}} \\ V_{\text{C1}} \\ i_{\text{Lo}} \\ V_{\text{C2}} \\ V_{\text{o}} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \dfrac{-n}{C_1} & 0 & 0 \\ 0 & \dfrac{-n}{L_{\text{o}}} & 0 & \dfrac{-1}{L_{\text{o}}} & \dfrac{-1}{L_{\text{o}}} \\ 0 & 0 & \dfrac{-1}{C_2} & 0 & 0 \\ 0 & 0 & \dfrac{1}{C_{\text{o}}} & 0 & \dfrac{-1}{R_{\text{o}}C_{\text{o}}} \end{bmatrix} \begin{bmatrix} i_{\text{in}} \\ V_{\text{C1}} \\ i_{\text{Lo}} \\ V_{\text{C2}} \\ V_{\text{o}} \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L_1} \\ 0 \\ \dfrac{-1}{L_{\text{o}}} \\ 0 \\ 0 \end{bmatrix} V_{\text{in}} \tag{2-19}$$

For the switch OFF position, the model can be written as in (2-20)-(2-24).

$$\frac{\mathrm{d}i_{\text{in}}}{\mathrm{d}t} = \frac{-V_{\text{C1}}}{L_1} - \frac{V_{\text{C2}}}{nL_1} + \frac{V_{\text{in}}}{L_1} \tag{2-20}$$

$$\frac{\mathrm{d}V_{\text{C1}}}{\mathrm{d}t} = \frac{i_{\text{in}}}{C_1} \tag{2-21}$$

$$\frac{\mathrm{d}i_{\text{Lo}}}{\mathrm{d}t} = -\frac{V_{\text{o}}}{L_{\text{o}}} - \frac{V_{\text{in}}}{L_{\text{o}}} + \frac{V_{\text{C1}}}{L_{\text{o}}} + \frac{V_{\text{C2}}}{nL_{\text{o}}} \tag{2-22}$$

$$\frac{\mathrm{d}V_{\text{C2}}}{\mathrm{d}t} = \frac{i_{\text{in}}}{nC_2} \tag{2-23}$$

$$\frac{\mathrm{d}V_{\text{o}}}{\mathrm{d}t} = \frac{i_{\text{Lo}}}{C_{\text{o}}} - \frac{V_{\text{o}}}{R_{\text{o}}C_{\text{o}}} \tag{2-24}$$

$$\begin{bmatrix} \dot{i}_{\text{in}} \\ V_{\text{C1}} \\ i_{\text{Lo}} \\ V_{\text{C2}} \\ V_{\text{o}} \end{bmatrix} = \begin{bmatrix} 0 & \dfrac{-1}{L_1} & 0 & \dfrac{-1}{nL_1} & 0 \\ \dfrac{1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & \dfrac{1}{L_{\text{o}}} & 0 & \dfrac{1}{nL_{\text{o}}} & \dfrac{-1}{L_{\text{o}}} \\ \dfrac{1}{nC_2} & 0 & 0 & 0 & 0 \\ 0 & 0 & \dfrac{1}{C_{\text{o}}} & 0 & \dfrac{-1}{R_{\text{o}}C_{\text{o}}} \end{bmatrix} \begin{bmatrix} i_{\text{in}} \\ V_{\text{C1}} \\ i_{\text{Lo}} \\ V_{\text{C2}} \\ V_{\text{o}} \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L_1} \\ 0 \\ \dfrac{-1}{L_{\text{o}}} \\ 0 \\ 0 \end{bmatrix} V_{\text{in}} \tag{2-25}$$

To obtain the converter average state-space model given in (2-27), (2-19) and (2-25) are combined using the condition of (2-26).

$$A = \delta A_1 + (1-\delta) A_2$$
$$B = \delta B_1 + (1-\delta) B_2 \tag{2-26}$$

$$\begin{bmatrix} \dot{i}_{in} \\ V_{C1} \\ i_{Lo} \\ V_{C2} \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & \frac{-(1-\delta)}{L_1} & 0 & \frac{-(1-\delta)}{nL_1} & 0 \\ \frac{1-\delta}{C_1} & 0 & \frac{-n\delta}{C_1} & 0 & 0 \\ 0 & \frac{-n\delta+(1-\delta)}{L_o} & 0 & \frac{-n\delta+(1-\delta)}{nL_o} & \frac{-\delta+(1-\delta)}{L_o} \\ \frac{1-\delta}{nC_2} & 0 & \frac{-\delta}{C_2} & 0 & 0 \\ 0 & 0 & \frac{\delta+(1-\delta)}{C_o} & 0 & \frac{-\delta-(1-\delta)}{R_oC_o} \end{bmatrix} \begin{bmatrix} i_{in} \\ V_{C1} \\ i_{Lo} \\ V_{C2} \\ V_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ \frac{-1}{L_o} \\ 0 \\ 0 \end{bmatrix} V_{in} \tag{2-27}$$

where

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{n}{C_1} & 0 & 0 \\ 0 & \frac{-n}{L_o} & 0 & \frac{-1}{L_o} & \frac{-1}{L_o} \\ 0 & 0 & \frac{-1}{C_2} & 0 & 0 \\ 0 & 0 & \frac{1}{C_0} & 0 & \frac{-1}{R_oC_o} \end{bmatrix} \quad A_2 = \begin{bmatrix} 0 & \frac{-1}{L_1} & 0 & \frac{-1}{nL_1} & 0 \\ \frac{1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{L_o} & 0 & \frac{-1}{nL_o} & \frac{-1}{L_o} \\ \frac{1}{nC_2} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_o} & 0 & \frac{-1}{R_oC_o} \end{bmatrix},$$

$$B_1 = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ \frac{-1}{L_o} \\ 0 \\ 0 \end{bmatrix} \quad B_2 = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ \frac{-1}{L_o} \\ 0 \\ 0 \end{bmatrix} \quad x = \begin{bmatrix} i_{in} \\ V_{C1} \\ i_{Lo} \\ V_{C2} \\ V_o \end{bmatrix} \quad u = \begin{bmatrix} V_{in} \end{bmatrix} \quad C = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & -1 \end{bmatrix} \quad D = \begin{bmatrix} 0 \\ 0 \end{bmatrix}.$$

In order to derive the linear model and transfer function of the isolated D2 converter, small signal analysis of the converter should be conducted. The small signal equivalent model can be obtained in (2-29) by using (2-28).

$$\dot{\tilde{x}} = \left(\delta A_1 + (1-\delta) A_2\right)\tilde{x} + \left[\left(A_1 - A_2\right)\tilde{x} + \left(B_1 - B_2\right)u\right]\tilde{\delta} \tag{2-28}$$

$$\begin{bmatrix} \dot{\tilde{i}}_{\text{in}} \\ \dot{\tilde{V}}_{\text{C1}} \\ \dot{\tilde{i}}_{\text{Lo}} \\ \dot{\tilde{V}}_{\text{C2}} \\ \dot{\tilde{V}}_{\text{o}} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-(1-\delta)}{L_1} & 0 & \frac{-(1-\delta)}{nL_1} & 0 \\ \frac{1-\delta}{C_1} & 0 & \frac{-n\delta}{C_1} & 0 & 0 \\ 0 & \frac{-n\delta+(1-\delta)}{L_{\text{o}}} & 0 & \frac{-n\delta+1+\delta}{nL_{\text{o}}} & \frac{-\delta+(1-\delta)}{L_{\text{o}}} \\ \frac{1-\delta}{nC_2} & 0 & \frac{-\delta}{C_2} & 0 & 0 \\ 0 & 0 & \frac{1}{C_o} & 0 & \frac{-1}{R_{\text{o}}C_{\text{o}}} \end{bmatrix} \times \begin{bmatrix} \tilde{i}_{\text{in}} \\ \tilde{V}_{\text{C1}} \\ \tilde{i}_{\text{Lo}} \\ \tilde{V}_{\text{C2}} \\ \tilde{V}_{\text{o}} \end{bmatrix} + \begin{bmatrix} \frac{nV_{\text{C1}}+V_{\text{C2}}}{nL_1} \\ \frac{-i_{\text{in}}-ni_{\text{Lo}}}{C_1} \\ \frac{n(n-1)V_{\text{C1}}+(-n-1)V_{\text{C2}}}{nL_{\text{o}}} \\ \frac{-i_{\text{in}}-i_{\text{Lo}}}{nC_2} \\ 0 \end{bmatrix} \tilde{\delta} \tag{2-29}$$

After Laplace manipulation of (2-29):

$$\Rightarrow \begin{cases} sI_{\text{in}}(s) = \frac{\delta-1}{L_1}V_{\text{C1}}(s) - \frac{1-\delta}{nL_1}V_{\text{C2}}(s) + \frac{nV_{\text{C1}}+V_{\text{C2}}}{nL_1}\delta(s) \\ sV_{\text{C1}}(s) = \frac{1-\delta}{C_1}I_{\text{in}}(s) - \frac{nd}{C_1}I_{\text{Lo}}(s) + \frac{-I_{\text{in}}-nI_{\text{Lo}}}{C_1}\delta(s) \\ sI_{\text{Lo}}(s) = \frac{-n\delta+(1-\delta)}{L_{\text{o}}}V_{\text{C1}}(s) + \frac{-n\delta+1+\delta}{nL_{\text{o}}}V_{\text{C2}}(s) + \frac{1-2\delta}{L_{\text{o}}}V_{\text{o}}(s) + \frac{n(n-1)V_{\text{C1}}+(-n-1)V_{\text{C2}}}{aL_{\text{o}}}\delta(s) \\ sV_{\text{C2}}(s) = \frac{1-\delta}{nC_2}I_{\text{in}}(s) - \frac{\delta}{C_2}I_{\text{Lo}}(s) - \frac{I_{\text{in}}+I_{\text{Lo}}}{nC_2}\delta(s) \\ sV_{\text{o}}(s) = \frac{1}{C_{\text{o}}}I_{\text{Lo}}(s) - \frac{1}{R_{\text{o}}C_{\text{o}}}V_{\text{o}}(s) \end{cases}$$

the following transfer functions are obtained.

$$\frac{I_{in}(s)}{\delta(s)} = \frac{\begin{array}{l} s^4\frac{nV_{\text{C1}}+V_{\text{C2}}}{nL_1} + s^3[\frac{(1-\delta)(I_{\text{in}}+I_{\text{Lo}})}{n^2C_2L_1} - \frac{(1-\delta)(-I_{\text{in}}-nI_{\text{Lo}})}{C_1L_1} + \frac{nV_{\text{C1}}+V_{\text{C2}}}{nR_{\text{o}}C_{\text{o}}L_1}] \\ +s^2[\frac{(1-\delta)(I_{\text{in}}+I_{\text{Lo}})}{n^2R_{\text{o}}C_2C_{\text{o}}L_1} + \frac{\delta k_1}{n^2C_2L_1L_{\text{o}}} - \frac{(1-\delta)(-I_{\text{in}}-nI_{\text{Lo}})}{R_{\text{o}}C_1C_{\text{o}}L_1} + \frac{\delta k_2}{C_1L_1L_{\text{o}}} - \frac{(1-2\delta)(nV_{\text{C1}}+V_{\text{C2}})}{nC_{\text{o}}L_1L_{\text{o}}}] \\ +s[-\frac{2\delta^2(1-\delta)(I_{\text{Lo}}-nI_{\text{Lo}})}{nC_2C_1L_1L_{\text{o}}} - \frac{(1-\delta)(1-2\delta)(I_{\text{in}}+I_{\text{Lo}})}{n^2C_2C_{\text{o}}L_1L_{\text{o}}} + \frac{\delta k_1}{n^2R_{\text{o}}C_2C_{\text{o}}L_1L_{\text{o}}} \\ +\frac{(1-\delta)(1-2\delta)(-I_{\text{in}}-nI_{\text{Lo}})}{C_1C_{\text{o}}L_1L_{\text{o}}} + \frac{\delta k_2}{R_{\text{o}}C_1C_{\text{o}}L_1L_{\text{o}}}] - \frac{2\delta^2(1-\delta)(I_{\text{Lo}}-nI_{\text{Lo}})}{nR_{\text{o}}C_2C_1C_{\text{o}}L_1L_{\text{o}}} \end{array}}{\begin{array}{l} s^5 + s^4\frac{1}{R_{\text{o}}C_{\text{o}}} + s^3[\frac{(1-\delta)^2}{n^2C_2L_1} + \frac{\delta[-n\delta+(1+\delta)]}{nC_2L_{\text{o}}} + \frac{(1-\delta)^2}{C_1L_1} + \frac{n\delta[-n\delta+(1-\delta)]}{C_1L_{\text{o}}} - \frac{(1-2\delta)}{C_{\text{o}}L_{\text{o}}}] \\ +s^2[\frac{(1-\delta)^2}{n^2R_{\text{o}}C_2C_{\text{o}}L_1} + \frac{\delta[-n\delta+(1+\delta)]}{nR_{\text{o}}C_2C_{\text{o}}L_{\text{o}}} + \frac{(1-\delta)^2}{R_{\text{o}}C_1C_{\text{o}}L_1} + \frac{n\delta[-n\delta+(1-\delta)]}{R_{\text{o}}C_1C_{\text{o}}L_{\text{o}}}] \\ +s[-\frac{(1-\delta)^2(1-2\delta)}{n^2C_2C_{\text{o}}L_1L_{\text{o}}} - \frac{(1-\delta)^2(1-2\delta)}{C_1C_{\text{o}}L_1L_{\text{o}}}] \end{array}} \tag{2-30}$$

$$\frac{V_{C1}(s)}{\delta(s)}=\frac{\begin{array}{l}s^4\frac{(-I_{in}-nI_{Lo})}{C_1}+s^3[\frac{(-I_{in}-nI_{Lo})}{R_oC_1C_o}+\frac{(1-\delta)(nV_{C1}+V_{C2})}{nC_1L_1}-\frac{\delta[n(n-1)V_{C1}+(-n-1)V_{C2}]}{C_1L_o}]\\+s^2[\frac{(1-\delta)^2(I_{Lo}-nI_{Lo})}{n^2C_2C_1L_1}+\frac{\delta[-n\delta+(1+\delta)](I_{Lo}-nI_{Lo})}{nC_2C_1L_o}+\frac{(1-\delta)(nV_{C1}+V_{C2})}{nR_oC_1C_oL_1}\\-\frac{(1-2\delta)(-I_{in}-nI_{Lo})}{C_1C_oL_o}-\frac{\delta[n(n-1)V_{C1}+(-n-1)V_{C2}]}{R_oC_1C_oL_o}]+s[\frac{(1-\delta)^2(I_{Lo}-nI_{Lo})}{n^2R_oC_2C_1C_oL_1}\\+\frac{\delta[-n\delta+(1+\delta)](I_{Lo}-nI_{Lo})}{nR_oC_2C_1C_oL_o}-\frac{(1-\delta)(1-2\delta)(nV_{C1}+V_{C2})}{nC_1C_oL_1L_o}]-\frac{(1-\delta)^2(1-2\delta)(I_{Lo}-nI_{Lo})}{n^2C_2C_1C_oL_1L_o}\end{array}}{\begin{array}{l}s^5+s^4\frac{1}{R_oC_o}+s^3[\frac{(1-\delta)^2}{n^2C_2L_1}+\frac{\delta[-n\delta+(1+\delta)]}{nC_2L_o}+\frac{(1-\delta)^2}{C_1L_1}+\frac{n\delta[-n\delta+(1-\delta)]}{C_1L_o}-\frac{(1-2\delta)}{C_oL_o}]\\+s^2[\frac{(1-\delta)^2}{n^2R_oC_2C_oL_1}+\frac{\delta[-n\delta+(1+\delta)]}{nR_oC_2C_oL_o}+\frac{(1-\delta)^2}{R_oC_1C_oL_1}+\frac{n\delta[-n\delta+(1-\delta)]}{R_oC_1C_oL_o}]\\+s[-\frac{(1-\delta)^2(1-2\delta)}{n^2C_2C_oL_1L_o}-\frac{(1-\delta)^2(1-2\delta)}{C_1C_oL_1L_o}]\end{array}} \tag{2-31}$$

$$\frac{I_{Lo}(s)}{\delta(s)}=\frac{\begin{array}{l}s^4\frac{[n(n-1)V_{C1}+(-n-1)V_{C2}]}{nL_o}+s^3[-\frac{[-n\delta+(1+\delta)](I_{in}+I_{Lo})}{n^2C_2L_o}\\+\frac{[-n\delta+(1-n)](-I_{in}-nI_{Lo})}{C_1L_o}+\frac{[n(n-1)V_{C1}+(-n-1)V_{C2}]}{nR_oC_oL_o}]+s^2[-\frac{[-n\delta+(1+\delta)](I_{in}+I_{Lo})}{n^2R_oC_2C_oL_o}\\+\frac{(1-\delta)k_1}{n^3C_2L_1L_o}+\frac{[-n\delta+(1-\delta)](-I_{in}-nI_{Lo})}{R_oC_1C_oL_o}+\frac{(1-\delta)k_2}{nC_1L_1L_o}]\\+s[-\frac{2\delta(1-\delta)^2(I_{Lo}-\delta I_{Lo})}{n^2C_2C_1L_1L_o}+\frac{(1-\delta)k_1}{n^3R_oC_2C_oL_1L_o}+\frac{(1-\delta)k_2}{nR_oC_1C_oL_1L_o}]-\frac{2\delta(1-\delta)^2(I_{Lo}-nI_{Lo})}{n^2R_oC_2C_1C_oL_1L_o}\end{array}}{\begin{array}{l}s^5+s^4\frac{1}{R_oC_o}+s^3[\frac{(1-\delta)^2}{n^2C_2L_1}+\frac{\delta[-n\delta+(1+\delta)]}{nC_2L_o}+\frac{(1-\delta)^2}{C_1L_1}+\frac{n\delta[-n\delta+(1-\delta)]}{C_1L_o}-\frac{(1-2\delta)}{C_oL_o}]\\+s^2[\frac{(1-\delta)^2}{n^2R_oC_2C_oL_1}+\frac{\delta[-n\delta+(1+\delta)]}{nR_oC_2C_oL_o}+\frac{(1-\delta)^2}{R_oC_1C_oL_1}+\frac{n\delta[-n\delta+(1-\delta)]}{R_oC_1C_oL_o}]\\+s[-\frac{(1-\delta)^2(1-2\delta)}{n^2C_2C_oL_1L_o}-\frac{(1-\delta)^2(1-2\delta)}{C_1C_oL_1L_o}]\end{array}} \tag{2-32}$$

$$\frac{V_{C2}(s)}{\delta(s)}=\frac{\begin{array}{l}-s^4\frac{I_{in}+I_{Lo}}{nC_2}+s^3[-\frac{I_{in}+I_{Lo}}{nR_oC_2C_o}+\frac{(1-\delta)(nV_{C1}+V_{C2})}{n^2C_2L_1}-\frac{\delta[n(n-1)V_{C1}+(-n-1)V_{C2}]}{nC_2L_o}]\\+s^2[-\frac{(1-\delta)^2(I_{Lo}-nI_{Lo})}{nC_2C_1L_1}-\frac{\delta[-n\delta+(1-\delta)](I_{Lo}-nI_{Lo})}{C_2C_1L_o}+\frac{(1-\delta)(nV_{C1}+V_{C2})}{n^2R_oC_2C_oL_1}\\+\frac{(1-2\delta)(I_{in}+I_{Lo})}{nC_2C_oL_o}-\frac{\delta[n(a-1)V_{C1}+(-n-1)V_{C2}]}{nR_oC_2C_oL_o}]+s[-\frac{(1-\delta)^2(I_{Lo}-nI_{Lo})}{nR_oC_2C_1C_oL_1}\\-\frac{\delta[-n\delta+(1-\delta)](I_{Lo}-nI_{Lo})}{R_oC_2C_1C_oL_o}-\frac{(1-\delta)(1-2\delta)(nV_{C1}+V_{C2})}{n^2C_2C_oL_1L_o}]+\frac{(1-\delta)^2(1-2\delta)(I_{Lo}-nI_{Lo})}{nC_2C_1C_oL_1L_o}\end{array}}{\begin{array}{l}s^5+s^4\frac{1}{R_oC_o}+s^3[\frac{(1-\delta)^2}{n^2C_2L_1}+\frac{\delta[-n\delta+(1+\delta)]}{nC_2L_o}+\frac{(1-\delta)^2}{C_1L_1}+\frac{n\delta[-n\delta+(1-\delta)]}{C_1L_o}-\frac{(1-2\delta)}{C_oL_o}]\\+s^2[\frac{(1-\delta)^2}{n^2R_oC_2C_oL_1}+\frac{\delta[-n\delta+(1+\delta)]}{nR_oC_2C_oL_o}+\frac{(1-\delta)^2}{R_oC_1C_oL_1}+\frac{n\delta[-n\delta+(1-\delta)]}{R_oC_1C_oL_o}]\\+s[-\frac{(1-\delta)^2(1-2\delta)}{n^2C_2C_oL_1L_o}-\frac{(1-\delta)^2(1-2\delta)}{C_1C_oL_1L_o}]\end{array}} \tag{2-33}$$

$$\frac{V_o(s)}{\delta(s)}=\frac{\begin{array}{l}s^3\frac{[\delta(n-1)V_{C1}+(-n-1)V_{C2}]}{nC_oL_o}+s^2[-\frac{[-n\delta+(1+\delta)](I_{in}+I_{Lo})}{n^2C_2C_oL_o}\\+\frac{[-n\delta+(1-\delta)](-I_{in}-nI_{Lo})}{C_1C_oL_o}]+s[\frac{(1-\delta)k_1}{n^3C_2C_oL_1L_o}+\frac{(1-\delta)k_2}{nC_1C_oL_1L_o}]-\frac{2\delta(1-\delta)^2(I_{Lo}-nI_{Lo})}{n^2C_2C_1C_oL_1L_o}\end{array}}{\begin{array}{l}s^5+s^4\frac{1}{R_oC_o}+s^3[\frac{(1-\delta)^2}{n^2C_2L_1}+\frac{\delta[-n\delta+(1+\delta)]}{nC_2L_o}+\frac{(1-\delta)^2}{C_1L_1}+\frac{n\delta[-n\delta+(1-\delta)]}{C_1L_o}-\frac{(1-2\delta)}{C_oL_o}]\\+s^2[\frac{(1-\delta)^2}{n^2R_oC_2C_oL_1}+\frac{\delta[-n\delta+(1+\delta)]}{nR_oC_2C_oL_o}+\frac{(1-\delta)^2}{R_oC_1C_oL_1}+\frac{n\delta[-n\delta+(1-\delta)]}{R_oC_1C_oL_o}]\\+s[-\frac{(1-\delta)^2(1-2\delta)}{n^2C_2C_oL_1L_o}-\frac{(1-\delta)^2(1-2\delta)}{C_1C_oL_1L_o}]\end{array}} \tag{2-34}$$

where

$$k_1=[(1-\delta)[n(n-1)V_{C1}+(-n-1)V_{C2}]+[-n\delta+(1+\delta)](nV_{C1}+V_{C2})]$$
$$k_2=[(1-\delta)[n(n-1)V_{C1}+(-n-1)V_{C2}]+[-n\delta+(1-\delta)](nV_{C1}+V_{C2})]$$

In addition, there is an output LC filter in the topology [137],

$$L_o=\frac{1}{4\pi f_cC_o} \tag{2-35}$$

where $f_{sw} >> f_c$, f_{sw} is the switching frequency, and f_c is the cut-off frequency. The LC filter transfer function is:

$$T_{LC}(s)=\frac{V_o}{V_{in}}=\frac{1}{s^2L_oC_o+1} \tag{2-36}$$

The switch average model for the non-isolated D2 is modelled using the software LTspice, and ac scan results follow [138].

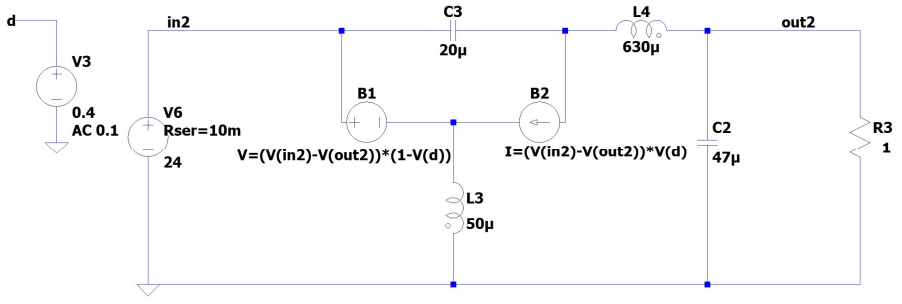


Fig. 2.5 D2 Converter switch average model from LTspice (NON-ISOLATED)

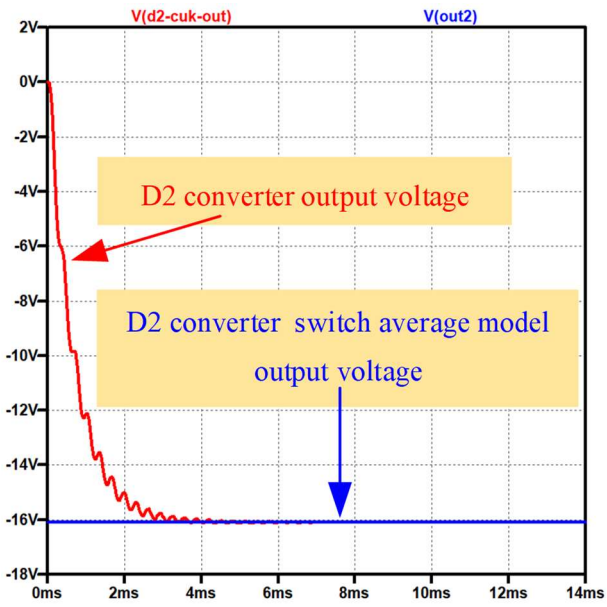


Fig. 2.6 Output voltages of D2 Converter and D2 switch average model (NON-ISOLATED)

The switch average model for the non-isolated D2 is an idealized model, and there is no transient process. The D2 converter circuit simulation model includes components without control, so there are transients during the first 4ms.

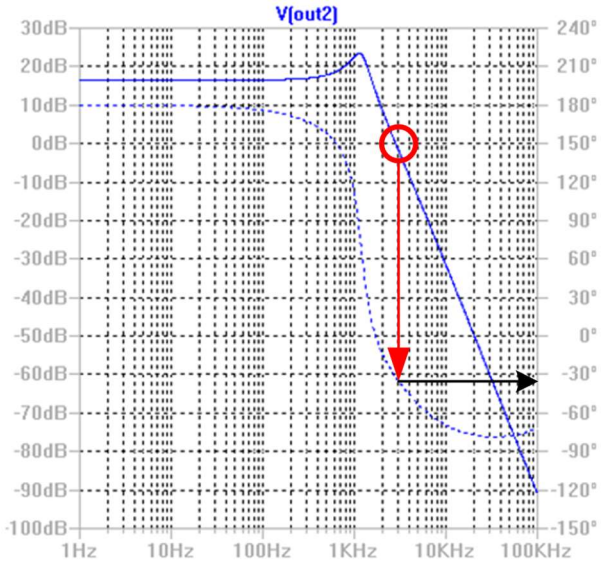


Fig. 2.7 D2 ac scan results (NON-ISOLATED)

The phase margin γ

$$A(\omega_c)=\left|G(j\omega_c)\bullet H(j\omega_c)\right|=1 \tag{2-37}$$

$$\gamma=180°+\angle G(j\omega_c)\bullet H(j\omega_c) \tag{2-38}$$

The phase margin $\Delta\gamma$ in Fig. 2.7 validates D2 converter system stability.

The switch average model of the isolated D2 is modelled using the software LTspice,

and ac scan results follow.

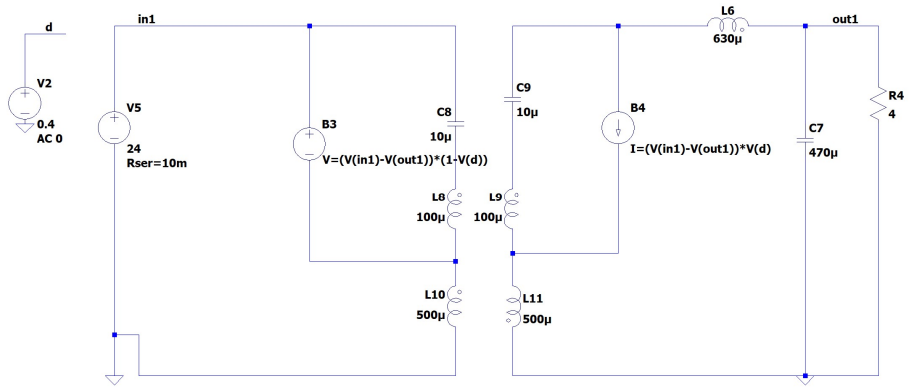


Fig. 2.8 Isolated D2 Converter switch average model on LTspice (ISOLATED)

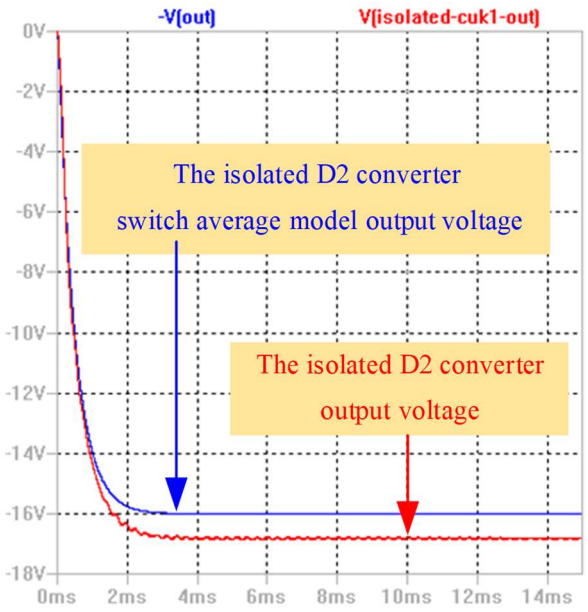


Fig. 2.9 Output voltages of the isolated D2 and the isolated D2 switch average model (ISOLATED)

The transformers in the isolated D2 switch average model and the isolated D2 converter result in the transients. The switch average model for the isolated D2 is an idealized model, and the output voltage value is accurate and consistent with the calculated results. The isolated D2 converter circuit simulation model includes other components without control, so there is an error in the output voltage.

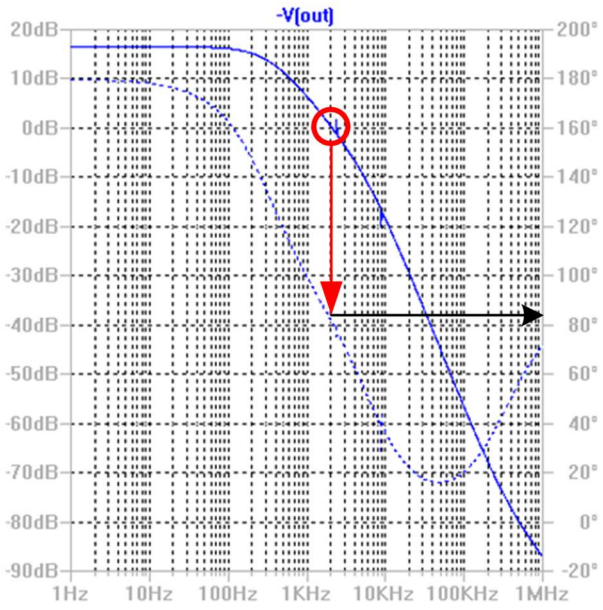


Fig. 2.10 ac scan results of the isolated D2 Converter (ISOLATED)

The phase margin $\Delta\gamma$ from Fig. 2.10 directly, validates that the isolated D2 converter system is stable.

2.2 Isolated D2 Simulation

2.2.1 Resistive Load

The following applications are simulated in the PSIM software because LTspice is particularly suitable for simulating and optimizing analogue circuits, but there may be limitations in handling complex circuits and advanced analytical functions. PSIM software provides a wider range of functionalities and model support, which is suitable for various circuit design needs. Also, a C block module in PSIM is used, and the control circuit completely imitates the analogue-to-digital conversion (A/D) of the actual controller DSP.

TABLE I

SIMULATION ELEMENT VALUES

V_{in}	24 V	T_1, L_{11}: L_{12}	100 µH: 100 µH
R_o	3Ω, 4Ω	T_1, k	0.9
C_1	10 µF	T_1, n	1:1
C_2	10 µF	T_2, L_{21}: L_{22}	500 µH: 500 µH
C_o	470 µF	T_2, k	0.9
L_o	600 µH	T_2, n	1:1
f_s	50 kHz		

First, the open-loop isolated D2 converter is simulated in PSIM software as shown in Fig. 2.11. The duty cycle of the MOSFET is ½, the input voltage is 24 V, and other parameter values are as shown in Table I and Fig. 2.11. According to (2-6), the theoretically calculated value of the output voltage is -24 V, and the output voltage is -24 V in the simulation.

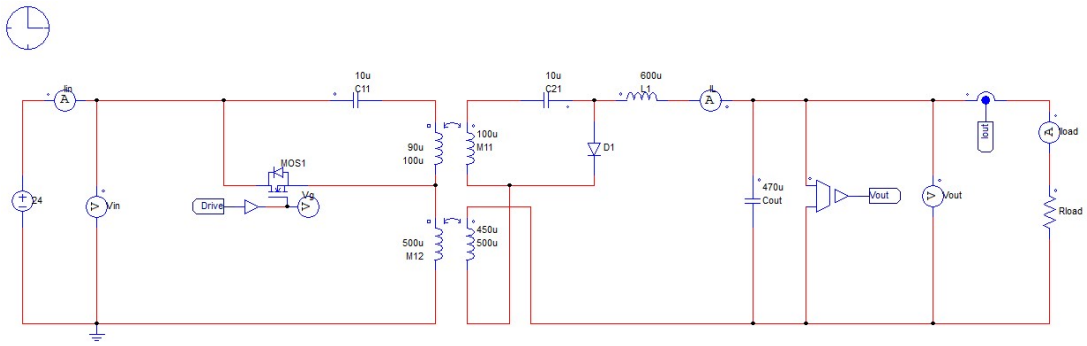


Fig. 2.11 The isolated D2 converter simulation model in PSIM

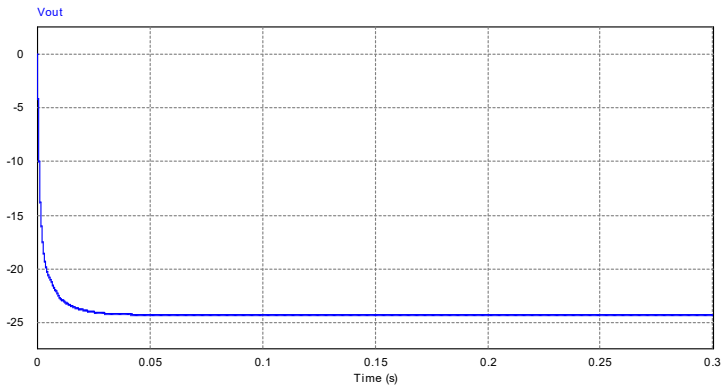


Fig. 2.12 The output voltage of the open-loop isolated D2 converter

When the load is a resistor, the following simulations verify the feasibility of controlling the isolated D2 converter. In the following closed-loop simulation, all the initial capacitor voltages and initial inductor currents are zero.

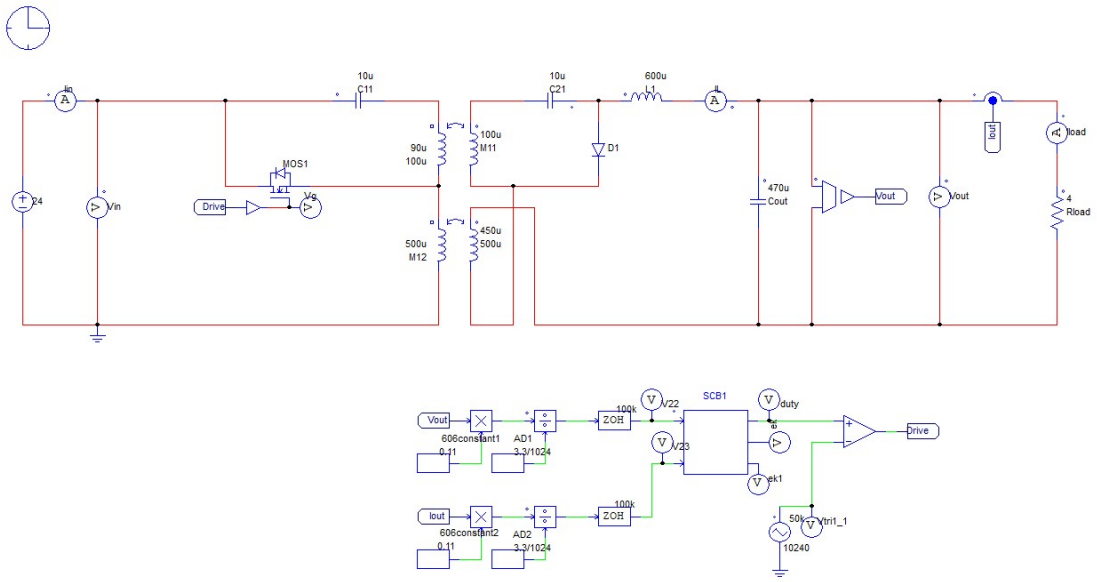


Fig. 2.13 The isolated D2 converter with a close-loop simulation model in PSIM

Both output voltage and output current are controlled (and magnitude limited), and the output is determined at lower power (for reliability).

As an example, if the output voltage reference is -20 V, and the output current reference is -3 A, the output plots in Fig. 2.14 result.

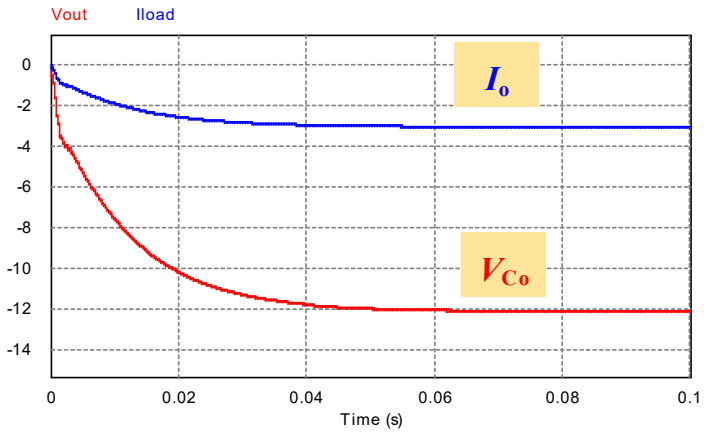


Fig. 2.14 The output voltage and current of the closed-loop isolated D2 converter

(V_o reference is -20 V, I_{load} reference is -3 A)

As seen, with a duty cycle of ⅓. the output current and voltage reach -3 A and -12 V, which equal the output reference values.

Changing the output references to -15 V and -5 A (δ=5/13) , produces the confirmation results in Fig. 2.15 (where the current controller has reached its regulation limit, 4 A).

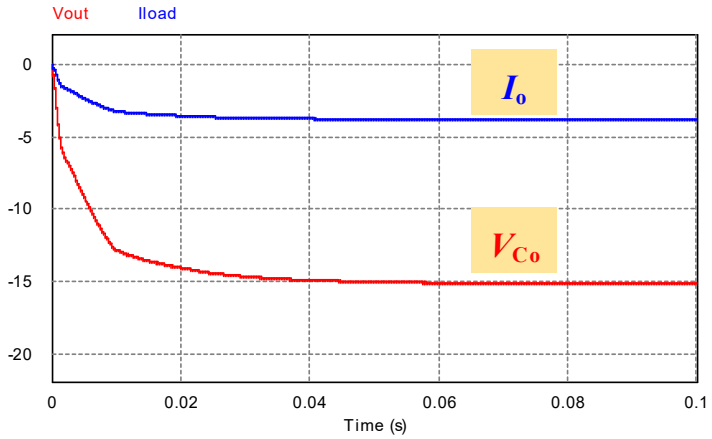


Fig. 2.15 The output voltage and current of the closed-loop isolated D2 converter

(V_o reference is -15 V, I_{load} reference is -5 A)

These simulations verify that the isolated D2 converter complies with the theoretical D2 voltage transmission ratio and can be controlled under different load conditions.

2.2.2 Capacitive Load

When the load is changed to a capacitor, the converter acts as a dc/dc charger [139].

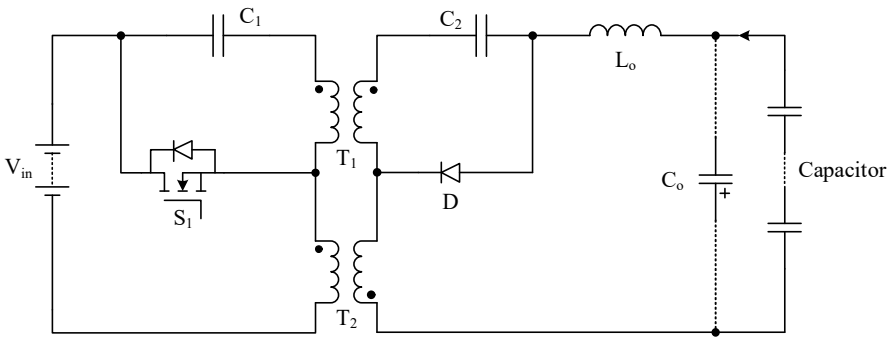


Fig. 2.16 The isolated D2 converter with capacitor load topology

The charging current (limit) is set as 3 A, and the rated voltage of the capacitor is 20 V.

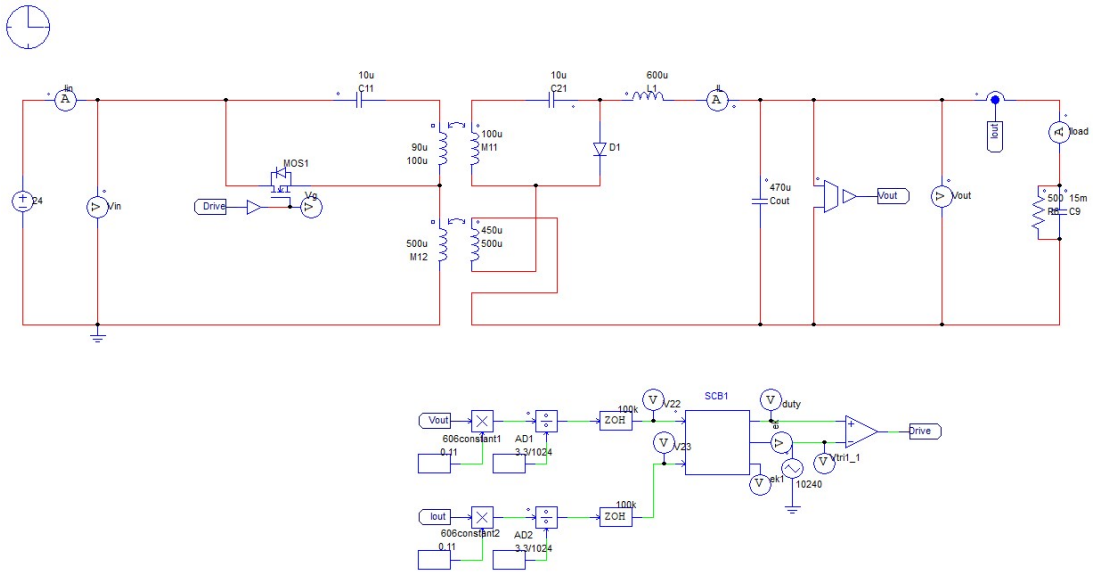


Fig. 2.17 The isolated D2 converter with capacitor load, simulation model

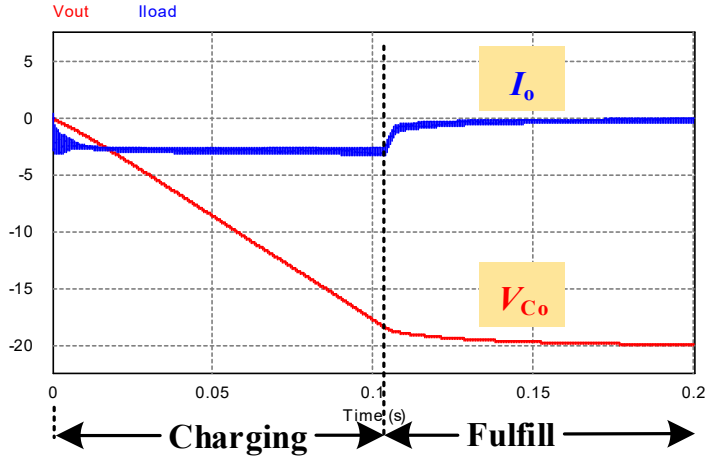


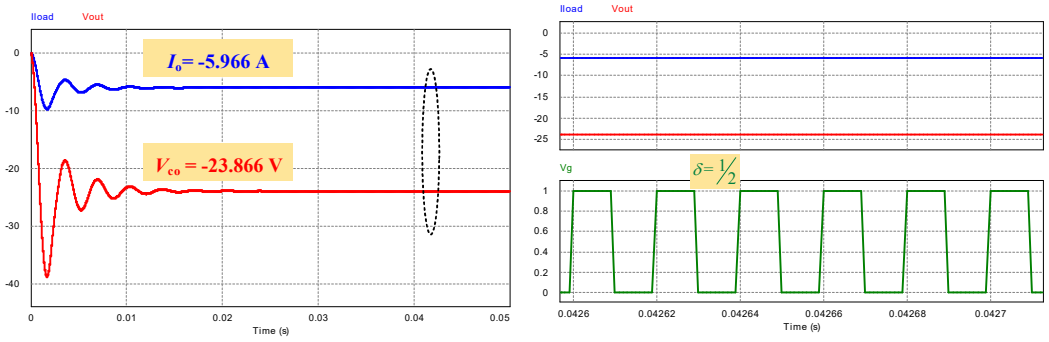
Fig. 2.18 The charging current and capacitor voltage

The charging current is initially controlled at 3 A. When the capacitor voltage is charged to the rated voltage of 20 V, the charging current decreases to 0 A, and then the capacitor voltage is maintained at 20 V.

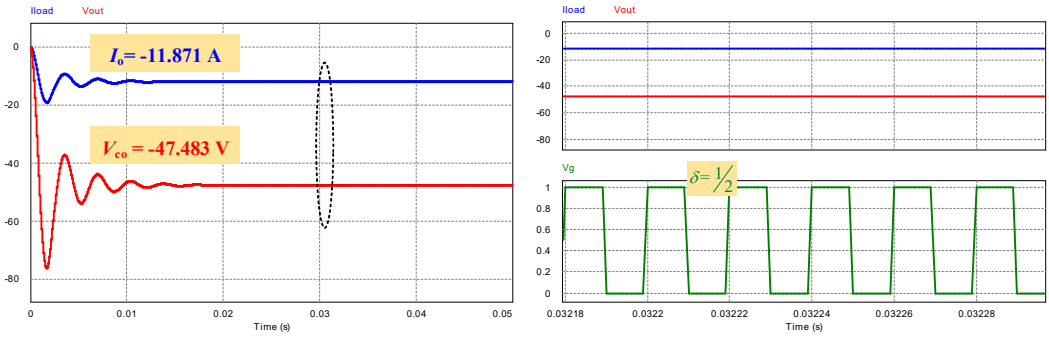
2.2.3 Output Voltage Range

To further verify the isolated D2 converter transmission ratio (2-6), the transformer ratio *n* is changed in the following simulations. The isolated D2 converter steps up the output voltage range when both transformer pair turns ratio remains the same.

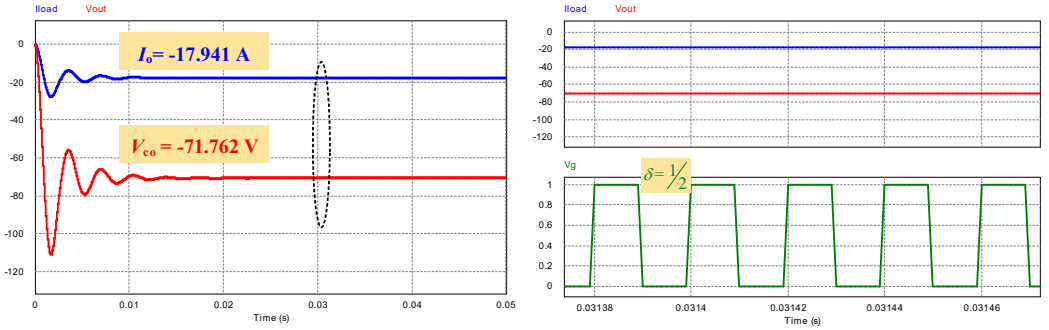
The open-loop isolated D2 converter is simulated in PSIM software. The duty cycle of the MOSFET is ½, the input voltage is 24 V, and other parameter values are as shown in Table I and Fig.2.11 (except transformers parameters).



(a) *n*=1:1



(b) *n*=1:2



(c) *n*=1:3

Fig. 2.19 Different transformer ratios of the isolated D2 converter output waveforms

In these simulations, all the passive components initial values are 0 and not under control, so the initial oscillations exist and take some time (about 0.01s) to reach the steady state. In Fig 2.19, the simulation output results verify that the isolated D2 converter complies with the theoretical D2 voltage transmission ratio and steps up the output voltage range.

2.3 Hardware Platform Design

2.3.1 Schematic and Printed Circuit Board

For experimental research, a two-phase isolated D2 was designed, and the PCB

schematic is shown in Fig. 2.20. An auxiliary power supply for the digital signal processor is incorporated, as shown in Fig. 2.21. With two D2 converters, the hardware can form different topologies for different functions. Fig. 2.22 shows the drive schematic, where the drive principle is based on a Push-pull circuit. Fig. 2.23 shows the drive PCB, PWM from the DSP, and its corresponding drive signals waveforms. Table II shows experimental component values.

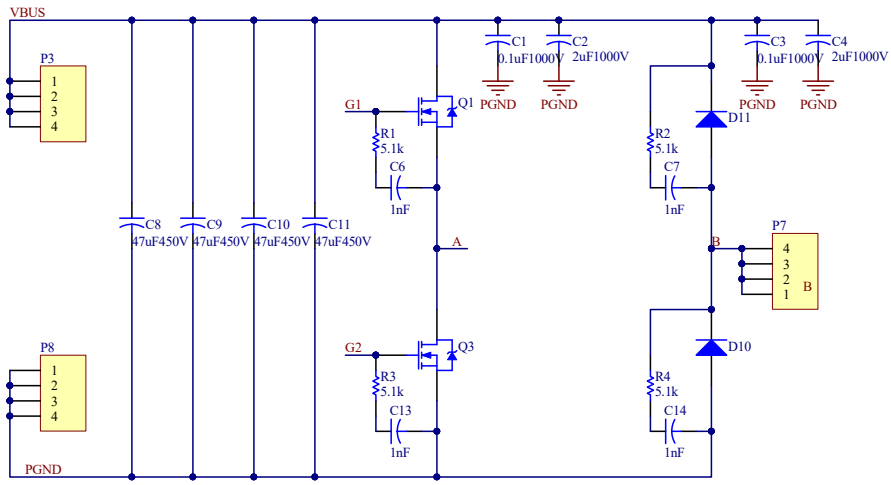


Fig. 2.20 Schematic of the isolated D2 converter

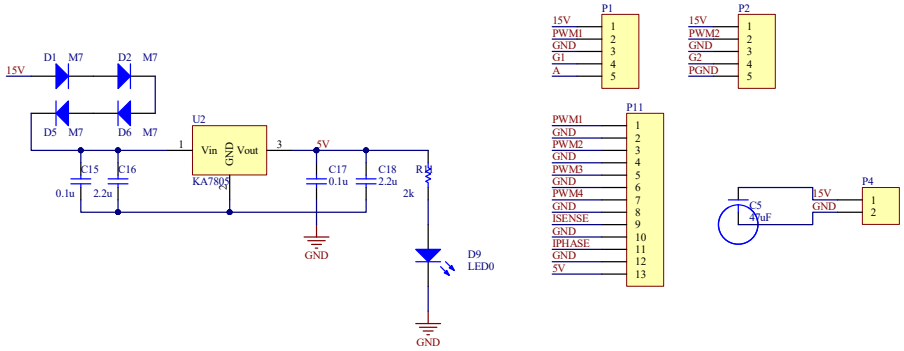


Fig. 2.21 The auxiliary power supply and interface schematic

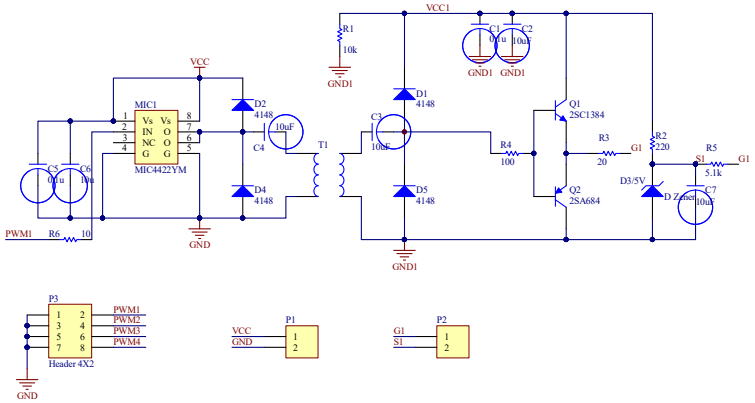


Fig. 2.22 Schematic of the switch drive

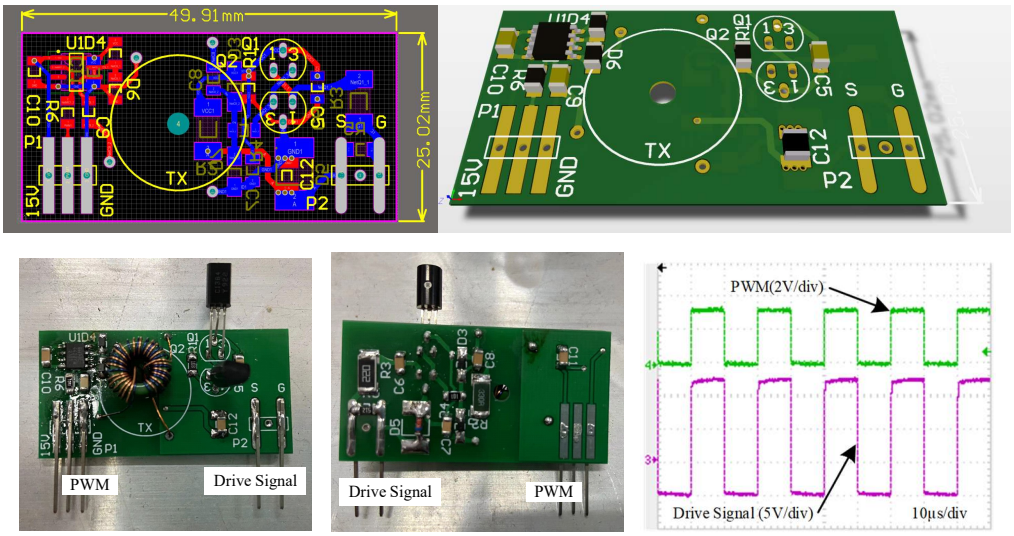


Fig. 2.23 Drive PCB, PWM and drive signals

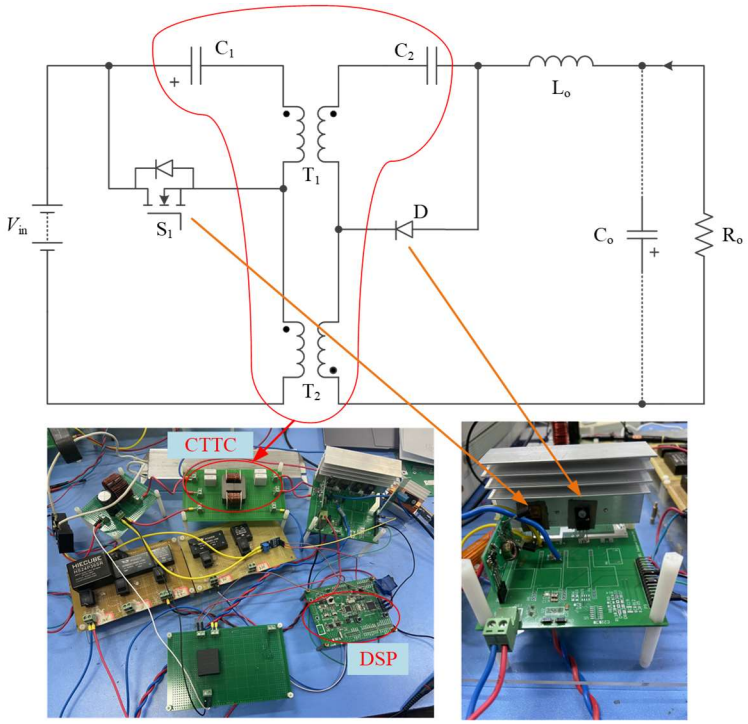


Fig. 2.24 Isolated D2 circuit and its hardware platform

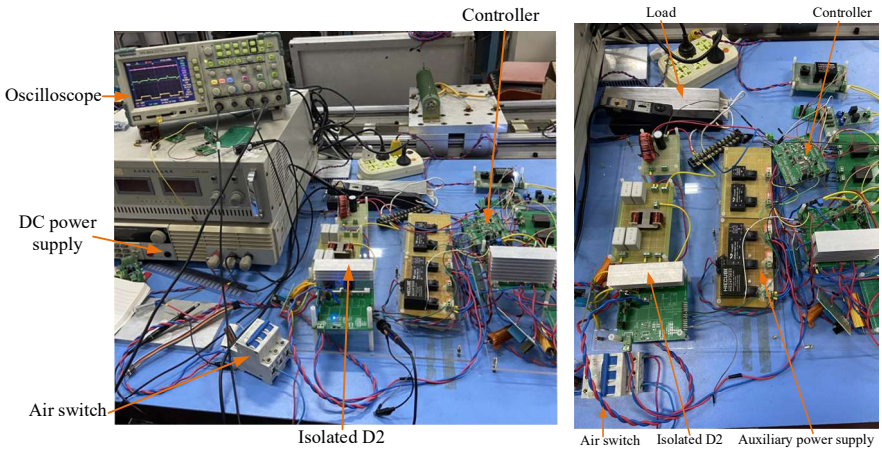


Fig. 2.25 Isolated D2 hardware platform

Fig. 2.24 and Fig. 2.25 show the developed 250 W 60 V isolated D2 hardware platform. The following experimental parameters used this platform.

TABLE II

EXPERIMENTATION ELEMENT VALUES

V_{in}	24 V	T_1, L_{11}: L_{12}	100 μH: 100 μH
$\boldsymbol{R_o}$	10 Ω	$\boldsymbol{T_1}$, $\boldsymbol{k}$	**0.96**
C_1	10 μF	T_1, n	1:1
C_2	10 μF	T_2, L_{21}: L_{22}	500 μH: 500 μH
C_o	470 μF	$\boldsymbol{T_2}$, $\boldsymbol{k}$	**0.98**
L_o	600 μH	T_2, n	1:1
f_s	50 kHz		

2.3.2 Controller Digital Signal Processor

The versatile controller chip dsPIC33FJ64GS606 is used in the following experiments.

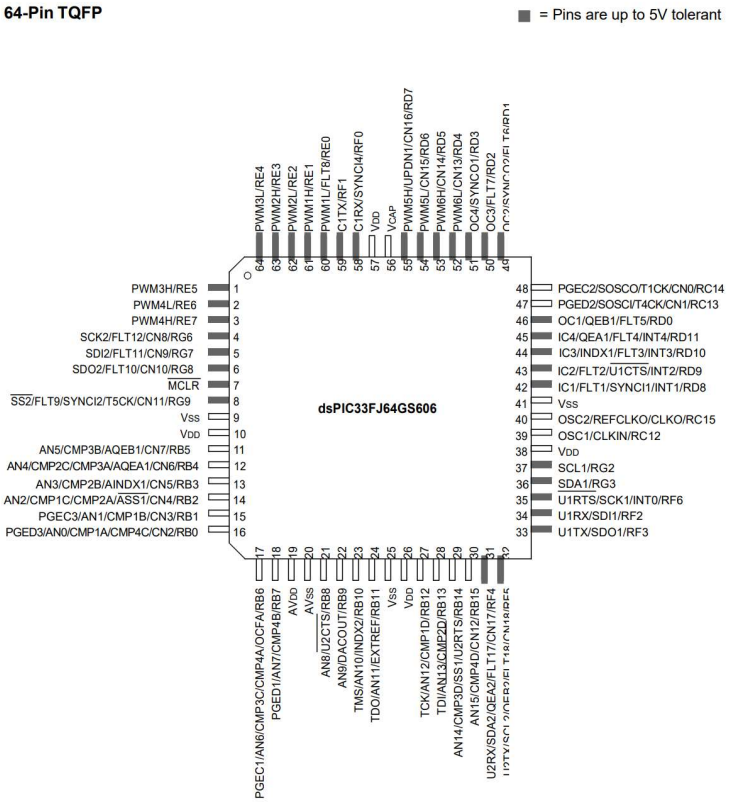


Fig. 2.26 dsPIC33FJ64GS606 pinout

2.4 Isolating Transformers

Initially each of the isolating ac transformations involves separate transformers, T_1 and T_2, each with two windings, figures 2.2 and 2.3. Such an isolated two transformer version of D2 is initially investigated [140].

Subsequently a single core is used to combine the magnetics of the 4 windings (of T_1 and T_2), which offers flux ripple cancellation possibilities [141], [142].

2.4.1 Two Separate Transformers

The isolated D2 converter with two separate transformers is conducted for later comparison with the single core case. Although E-core pairs are used, equally each transformer could be wound on toroidal or C cores. E-core pairs (Fig. 2.27 and 2.28) were adopted to be consistent with the single transformer design that follows after this section.

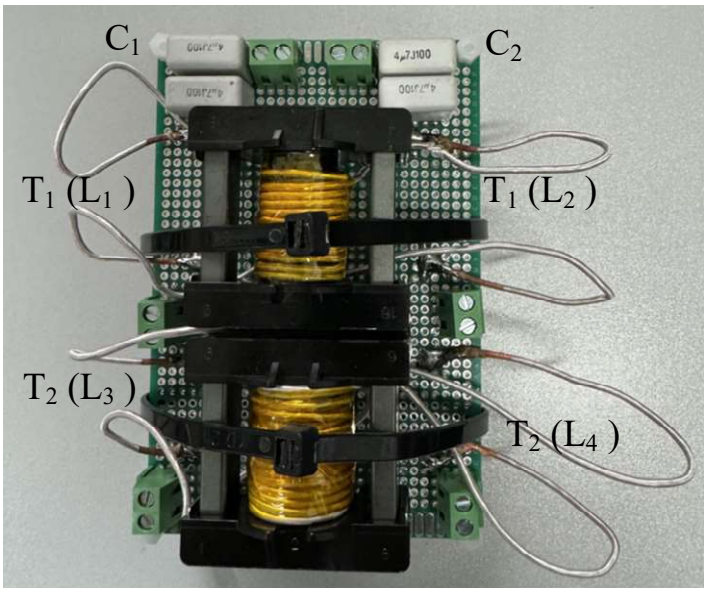
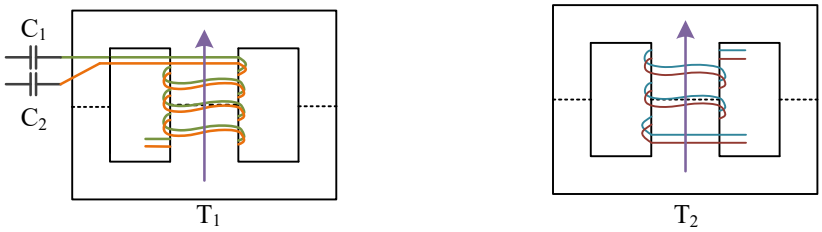


Fig. 2.27 The isolated D2 converter with two separate transformers CTTC hardware

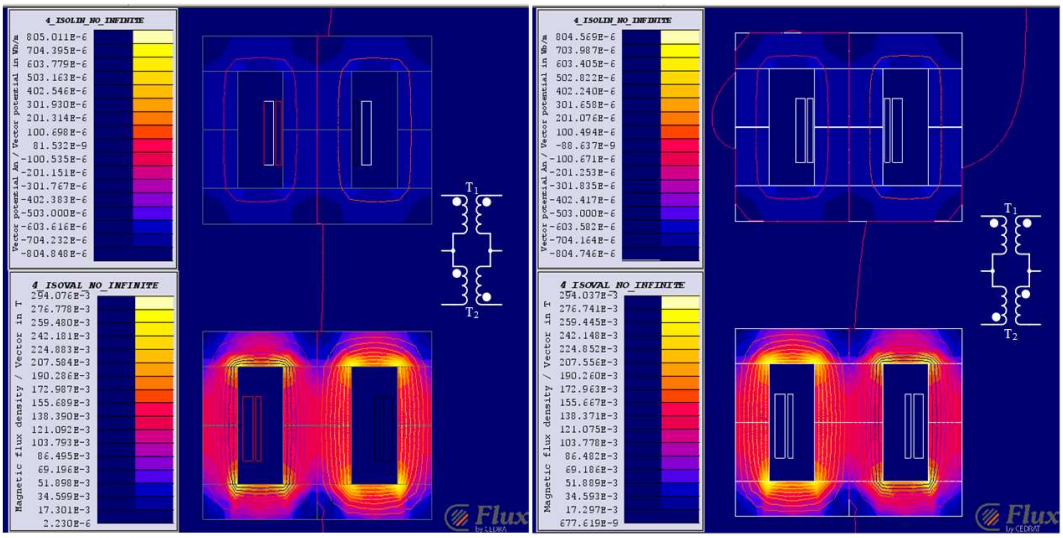
The inductance, mutual inductance, and coupling coefficient of the two separate transformers are measured as: L_1=102.5μH, L_2=102.6μH, L_3=489.3μH, L_4=489.9μH, M_{12}=101.7μH, M_{34}=484.4μH, k_{12}=0.992, k_{34}=0.990. No energy is stored in the T_1 core; but energy is stored in the T_2 core.



(a) No energy stored (b) Energy stored in the core

Fig. 2.28 Flux interaction on two separate transformers

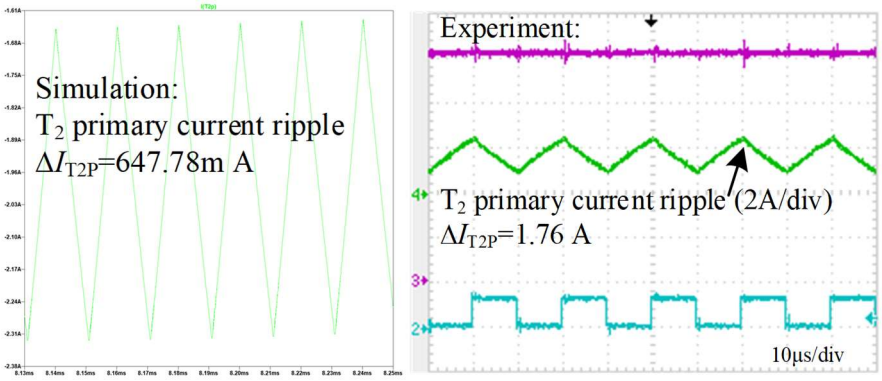
Finite element analysis on the two separate transformers is shown in Fig. 2.29.



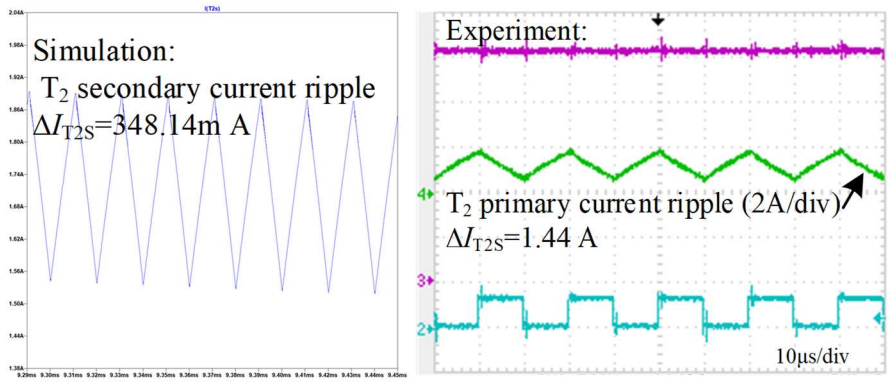
(a) Case 1 (b) Case 2

Fig. 2.29 Finite element analysis on the two separate transformers

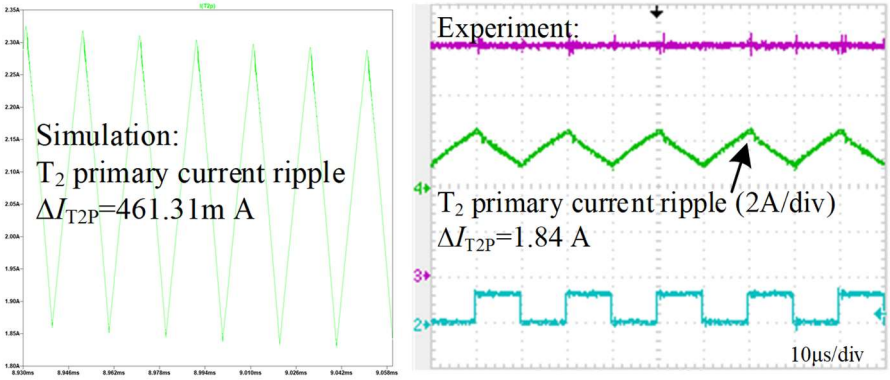
The simulation and practical results of the two core physical orientation cases are the same, as shown in Fig. 2.29. Specifically, core proximity stray flux interaction is nearly non-existent. In the coupled capacitor transformer case, T_1, the average current I is zero. Hence, the core experiences ripple magnetic field intensity ΔH around zero. No energy is stored in the core. In T_2, the core experiences a ripple current around a controlled current. Component H_{dc} is stored in the core. Such core flux conditions are explored in detail in the next section; necessary when using a single core with 4 windings. Experimental results with 2 transformers follow.



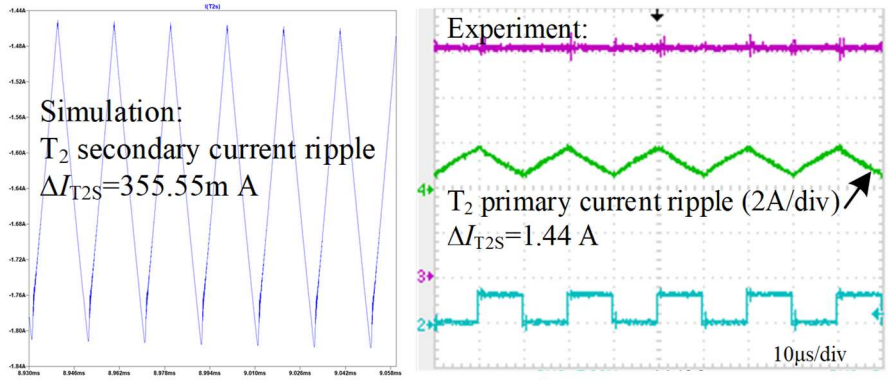
(a) T_2 primary current ripple (dot orientation Case 1)



(b) T_2 secondary current ripple (dot orientation Case 1)



(c) T_2 primary current ripple (dot orientation Case 2)

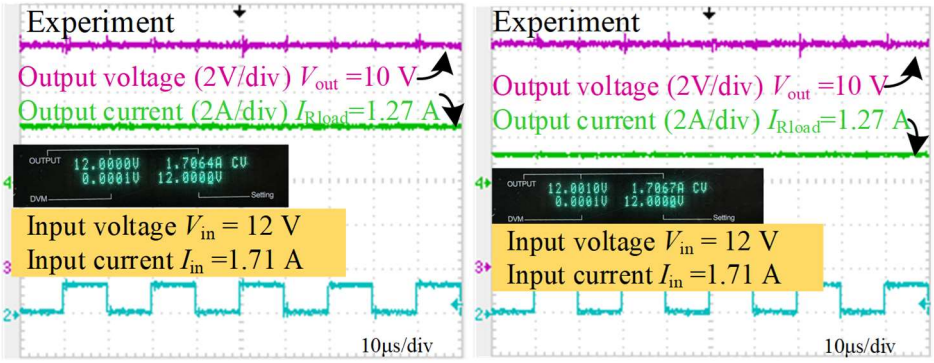


(d) T_2 secondary current ripple (dot orientation Case 2)

Fig. 2.30 Two separate transformers current ripple, for two stray coupling orientations

Fig. 2.30 shows the simulated and experimental ripple current associated with T_2, of the isolated D2 converter, with two separate transformers.

Typical input and output results are shown in Fig. 2.31. These results will be compared with results when a common core is used for T_1 and T_2, (in the next section).



(a) Case 1 (b) Case 2

Fig. 2.31 Input and output *V* and *I* of the isolated D2 converter with two separate transformers

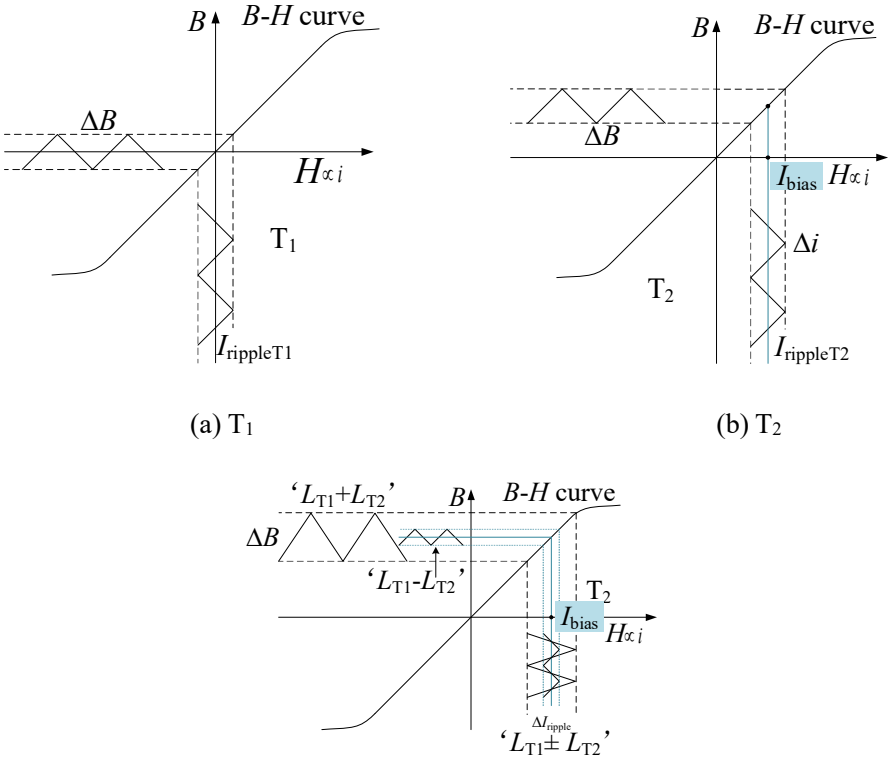
2.4.2 Single Four-winding Transformer

The two transformer isolation techniques used (Fig. 2.2 and Fig. 2.33a) are based on combining those used on the Ćuk (capacitor ac equivalent circuit) and Sepic and Zeta (inductor ac equivalent circuit) converters [1]. Transformer T_2 is used in a current source control mode, thus avoiding core saturation. In the capacitor coupling case, the series capacitors block T_1 from any dc voltage.

In the coupled capacitor case, T_1, the average current I_{ave} is zero (with fixed average dc voltage bias's on the two capacitors). Hence, the core experiences ripple magnetic field intensity ΔH (ripple current $N\Delta i=\Delta H\ell$) around H_{ave} α I_{ave} = 0. No energy is stored in the core. In the case of transformer coupling of the magnetizing inductance, T_2, the core experiences the ripple current (ΔH α Δi) around a controlled current $I_{dc\ bias}$ (hence fixed core H, $H_{dc\ bias}$ α $I_{dc\ bias}$). Component $H_{dc\ bias}$ represents net energy (hence core volume) stored in the core.

Winding pairs are wound on the outer limbs of an E core pair. That is, T_1 is on one outer limb and T_2 is on the other outer limb, with no winding on the center limb.

The core (shared flux paths) condition ($B=\mu H$) is the algebraic sum of the two winding pair mmf induced fluxes, as shown in Fig. 2.32. Depending on the coupling (dot) orientation between T_1 and T_2, ripple flux components are subtractive (tend to cancel) in the center limb, but additive in the outer limbs, or vice versa, specifically, additive in the center and subtractive in the outer limbs (assuming no induced interaction).



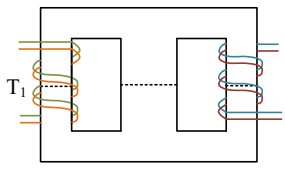
(a) T_1 (b) T_2

(c) T_1 and T_2

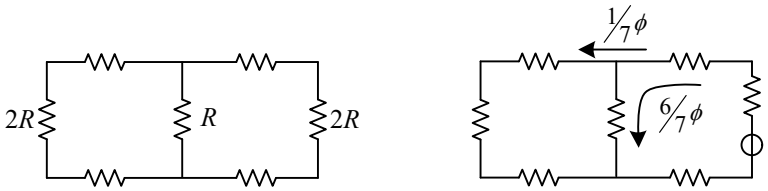
Fig. 2.32 *B-H* curve for D2 isolated converter ripple fluxes

Fig. 2.32 illustrates the *B-H* operating curve for the D2 coupling circuit isolated converter, showing ripple current effects for the transformer: (a) T_1, (b) T_2, and (c) T_1 and T_2 on a single core (outer limbs) connected for additive and subtractive ripple current produced fluxes.

All the inductance, mutual inductance, and coupling coefficient are measured values. M_{12}=112.45μH, M_{13}=39.5μH, M_{14}=46μH, M_{23}=41.5μH, M_{24}=46.5μH, M_{34}=517μH. k_{12}=0.995, k_{13}=0.159, k_{14}=0.179, k_{23}=0.167, k_{24}=0.187, k_{34}=0.943. These values are applied in the flux interaction analysis, finite element analysis, simulation and experiments. The magnetic core model used and its magnetic circuit model are shown in Fig. 2.32.



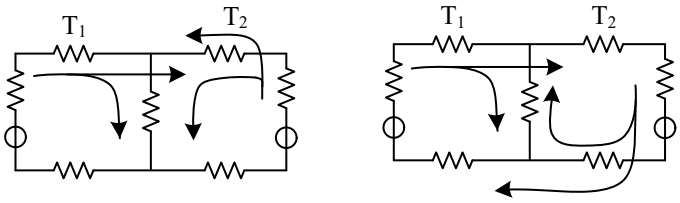
(a) 2E cores approx model



(b) Resistance $R \equiv$ reluctance ($\approx \ell/A$) (c) Flux $\phi \equiv$ current

Fig. 2.33 2E-core magnetic circuit model

Combining actual measurement results (and core dimensions), flux from the outer limb splits $^{6}/_{7}\phi$ into the centre limb and $^{1}/_{7}\phi$ into the other limb. That is, little interaction can be expected in the outer limbs (compared to central limb interaction).

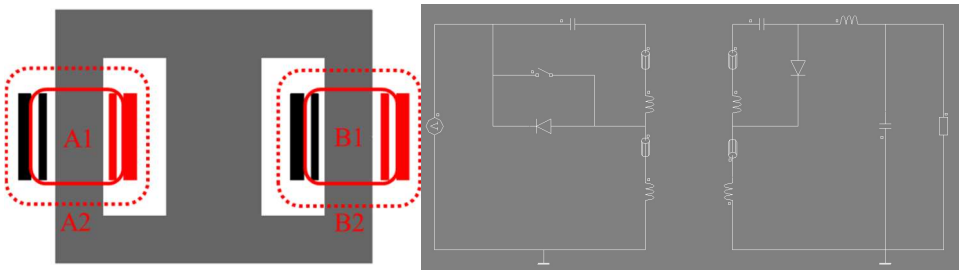


(a) Case 1 (b) Case 2

Fig. 2.34 Two ripple flux cases

In Case 1, the ripple is additive in the centre limb and subtractive in the outer limb (Fig. 2.34a). In Case 2, the ripple flux is subtractive in the centre limb and additive in the outer limb (Fig. 2.34b).

The finite element analysis software flux result is used to observe the magnetic circuit and magnetic field, based on Fig. 2.35.

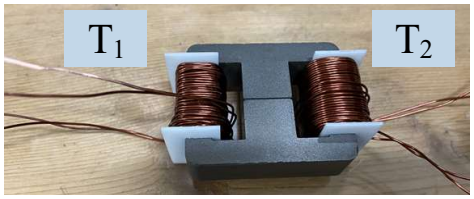


(a) (b)

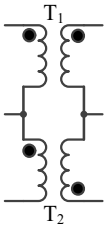
Fig. 2.35 Isolated D2 converter transformer Flux model

(a) E-core and winding arrangement flux model (b) Isolated D2 circuit Flux model

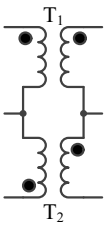
Fig. 2.36 shows the finite element analysis results for the two coupling (dot) orientations between T_1 and T_2 on one core.



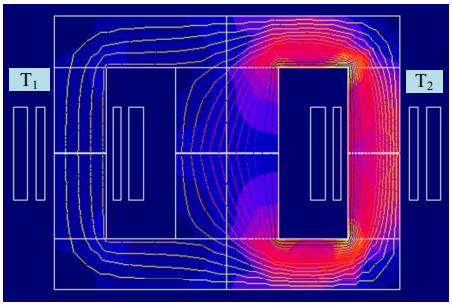
(a) E-core and winding arrangement



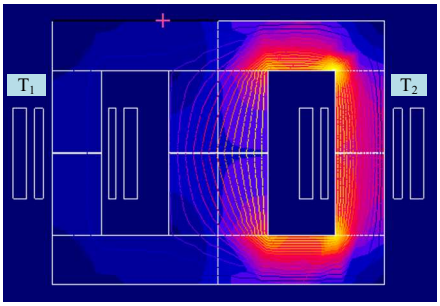
(b) Case 1 transformer



(c) Case 2 transformer



(d) Case 1 flux plot

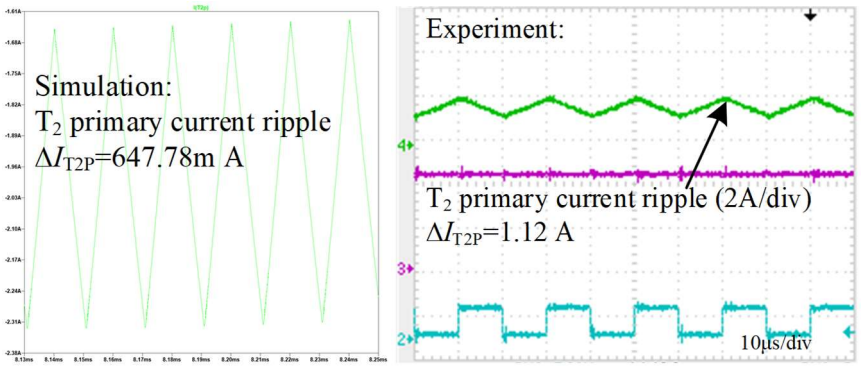


(e) Case 2 flux plot

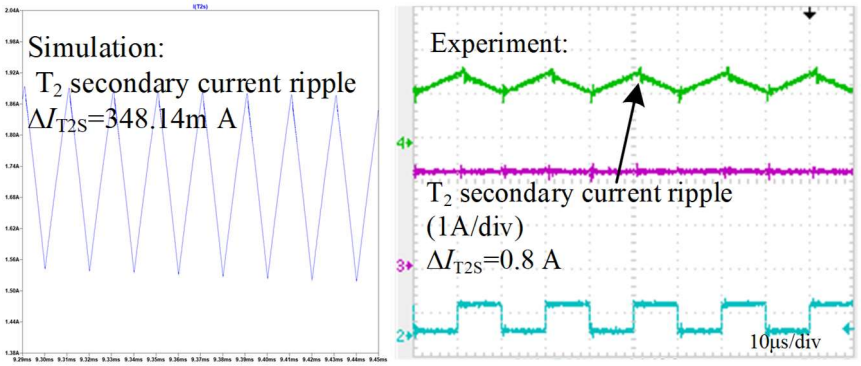
Fig. 2.36 Finite element analysis on the transformer

In general, most fluxes tend to the centre limb rather than interacting with the other limb (winding pair). This is because the reluctance of the centre limb is much lower than the alternate path through a limb with a longer path ℓ and smaller area, A (reluctance, $\Re \alpha \ell/A$), as seen in Fig. 2.33.

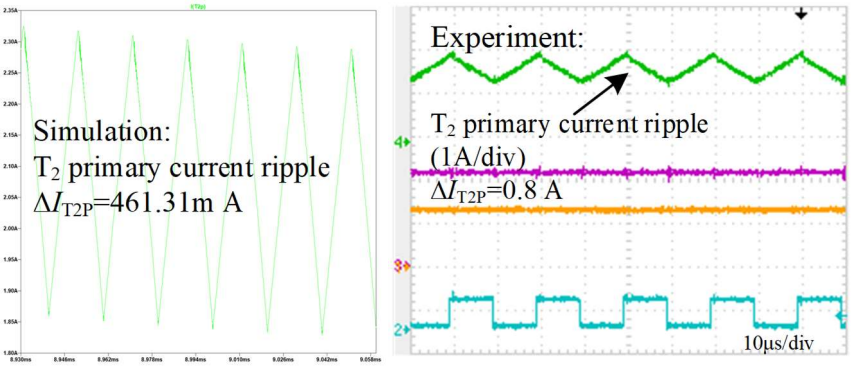
In Fig. 2.36, parts d and e note the flux lines in the left E-core limb, which are associated with T_1. In Fig. 2.36e, the centre limb flux is increased but is not saturated, while importantly, the flux coupled (interaction) between T_2 and T_1 is low. In Fig. 2.36d, flux lines occur around the outer flux path (linking T_1 and T_2), implying flux interaction. In the simulations and experiments (Fig. 2.37), the current ripple through the four windings is monitored.



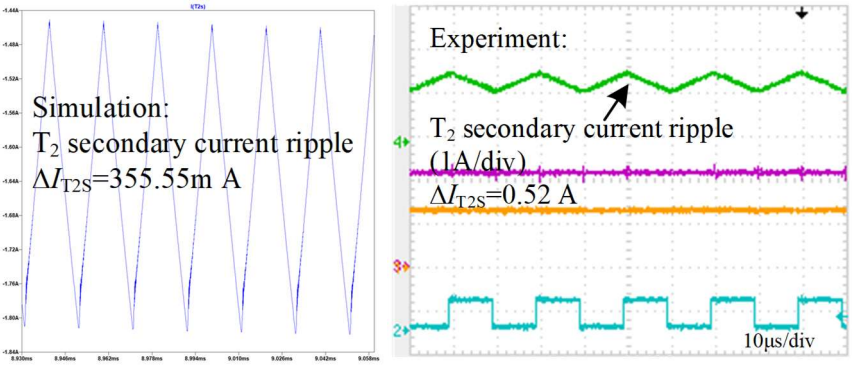
(a) T_2 primary current ripple (dot orientation Case 1)



(b) T_2 secondary current ripple (dot orientation Case 1)

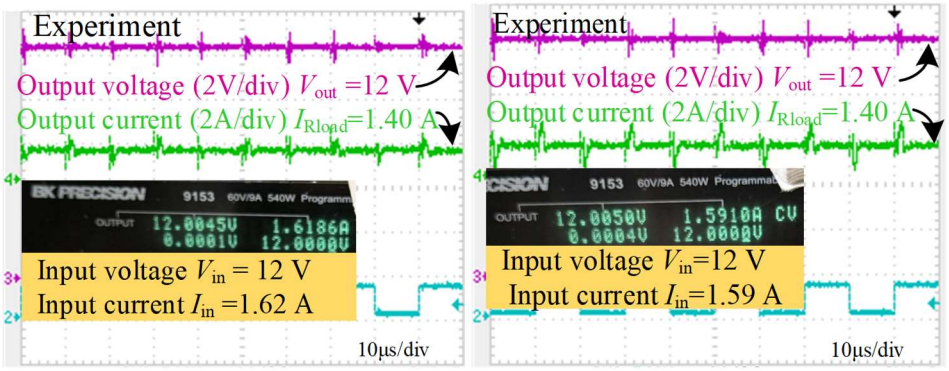


(c) T_2 primary current ripple (dot orientation Case 2)



(d) T_2 secondary current ripple (dot orientation Case 2)

Fig. 2.37 Four-windings transformer current ripple, for two coupling orientations, one core



(a) Case 1 (b) Case 2

Fig. 2.38 Input and output V and I of two coupling orientations, on core

From Fig. 2.38, the isolated D2 efficiency of each coupling orientation is (common core):

$$\eta_{\text{Case1}} = \frac{12\text{V} \times 1.40\text{A}}{12\text{V} \times 1.62\text{A}} \equiv 86.4\% \tag{2-39}$$

$$\eta_{\text{Case2}} = \frac{12\text{V} \times 1.40\text{A}}{12\text{V} \times 1.59\text{A}} \equiv 88.05\% \tag{2-40}$$

As seen in Fig. 2.36, there are more flux lines in the T_1 limb of Case 1 than in Case 2, which is consistent with better efficiency results for Case 2.

From Fig. 2.38, with 2 separate cores, the isolated D2 efficiency of each coupling orientation is:

$$\eta_{\text{SeperateTransformersCase1}} = \frac{10\text{V} \times 1.27\text{A}}{12\text{V} \times 1.71\text{A}} \equiv 62.89\% \tag{2-41}$$

$$\eta_{\text{SeperateTransformersCase2}} = \frac{10\text{V} \times 1.29\text{A}}{12\text{V} \times 1.71\text{A}} \equiv 62.87\% \tag{2-42}$$

In both cases, the efficiency is the same since virtually zero stray fluxes couple the two transformers. So, the simulation, current ripple, flux plots, output waveforms, and efficiency are the same. Compared with the efficiency of the single transformer with four windings, the isolated D2 converter with two separate transformers has lower efficiency. That is, the isolated D2 converter with a single four-winding E-core transformer features better performance. Thus, the 250 W 60 V prototype for experimentation incorporates one transformer with four windings, plus a power supply, DSP, auxiliary power supply, one gate driver, one switch and diode, sensors, capacitors,

load, heat sink, etc.

2.5 Single Core Isolated D2 Experiments

2.5.1 Resistive Load

When the input voltage is 24 V, and the resistive load is 10 Ω, the output voltage and current reference limits are 24 V and 2 A, when the PWM theoretical duty cycle is 0.4545. The experimental output waveforms are seen in Fig. 2.37.

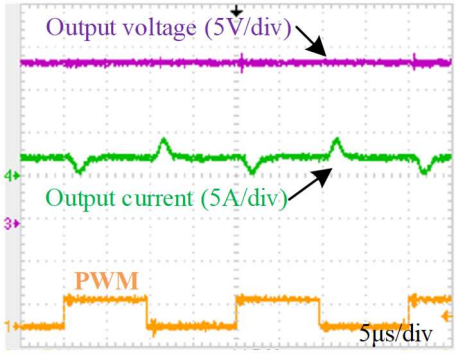


Fig. 2.39 The output voltage, current and PWM of the closed-loop isolated D2 converter

(V_o reference is 24V, I_{load} reference is 2A)

The output current is 2 A, the output current reference value, the output voltage is about 18.8 V, and the duty cycle in the waveforms is 0.46. With a 10 Ω load, current control dominates over voltage control. So, the isolated D2 converter output current can be controlled.

When changing the output voltage and current reference limits to 10 V and 2 A; (the PWM theoretical duty cycle is 0.294), the output waveforms in Fig. 2.40 result.

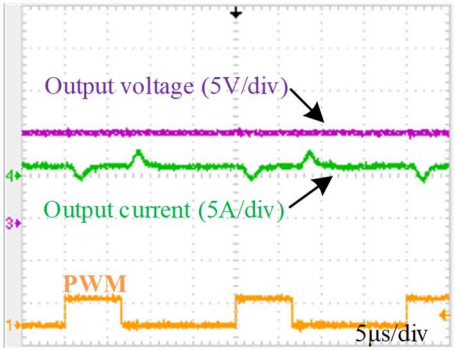


Fig. 2.40 The output voltage, current and PWM of the closed-loop isolated D2 converter

(V_o reference is 10 V, I_{load} reference is 2 A)

The output voltage is 10 V, which is equal to the output voltage reference value, the

output current is 1 A, and the duty cycle in the waveforms is 0.3. So voltage control dominates, confirming the isolated D2 converter output voltage can be controlled.

These current and voltage controlled experiments verify that the isolated D2 converter complies with the D2 voltage transmission ratio and can be controlled under different load conditions.

2.5.2 Capacitive Load

When the load is a super-capacitor, the converter is used as a dc/dc charger, as in Fig. 2.41. The super-capacitor bank rated voltage is 27 V dc and the capacitance is 15 F.

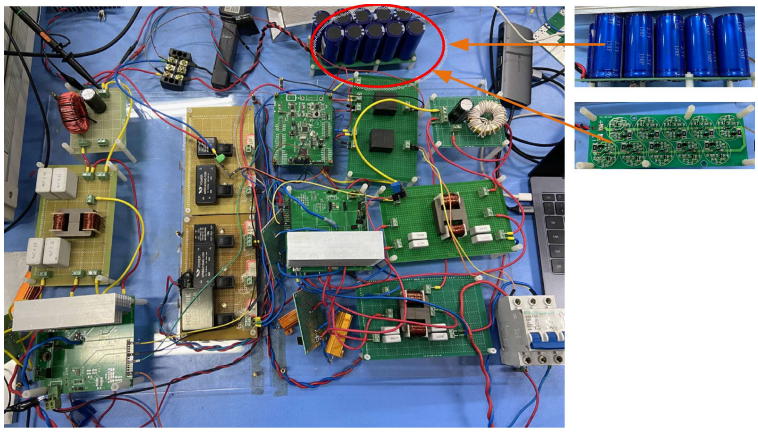
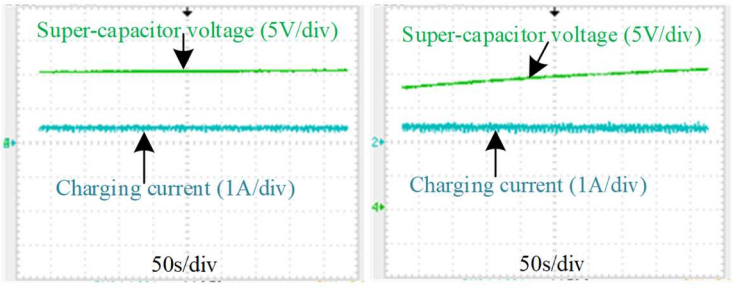
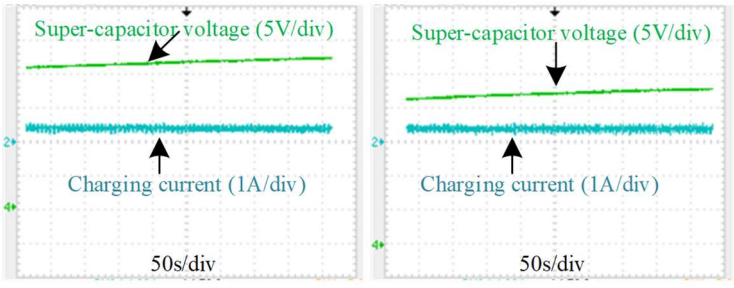


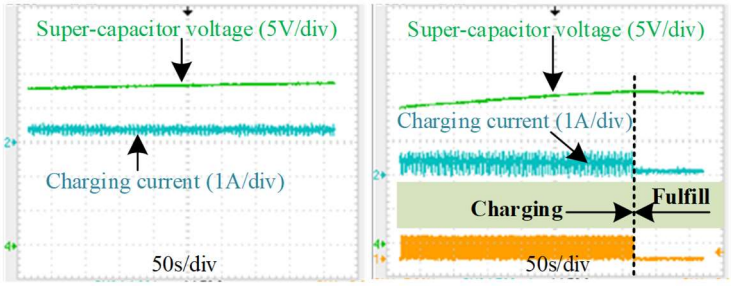
Fig. 2.41 Super-capacitor load, isolated D2 hardware platform



(a) 0-450s (b) 451-900s



(c) 901-1350s (d) 1351-1800s



(e) 1801-2250s (f) 2251-2700s

Fig. 2.42 Super-capacitor charging process

In Fig. 2.42, the charging current is constantly controlled. When the capacitor voltage reaches rated operating voltage, 22.5 V, the charging current decreases to 0 A, and then the voltage is maintained at 22.5 V. Thus, the single core, isolated D2 converter can charge a super-capacitor (highly capacitive load); safely and effectively.

2.6 D1 Converter

All of the 33 single switch (See Appendix A for the 33 known single switch dc to dc converters and their alphanumeric classification), dc to dc converters are reversible[1], that is they offer bidirectional power flow possibilities when two switch and diode pairs are used. With reverse power flow converters D2 becomes converter D1 (figures 2.43 and 2.44). D1 and D2 are the reverse of each other, and the required transformer isolation stages are the same for both. Both have the same voltage transfer function. The D1 converter offers continuous input current (whilst the D2 affords continuous output current) [1]. A particular application may dictate which of the two converters is employed. The basic simulation to follow (Fig. 2.45) confirms the D1 converter operation and its voltage transfer function. The D2 bidirectional mode (that is D1 operation) is exploited in Chapter 5.

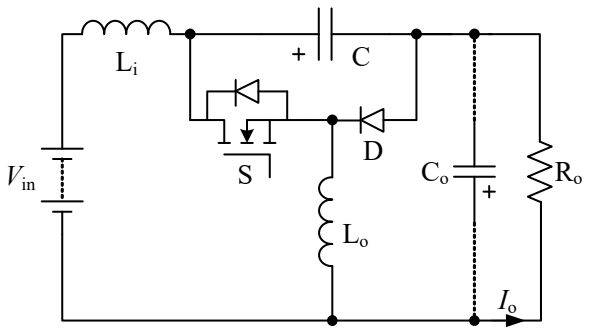


Fig. 2.43 D1 converter topology

The transfer ratio of D1 is the same as the D2 converter [1]:

$$\frac{V_o}{V_{in}} = -\frac{\delta}{1-\delta}$$

The basic non-isolated D1 converter circuit is simulated using PSIM software.

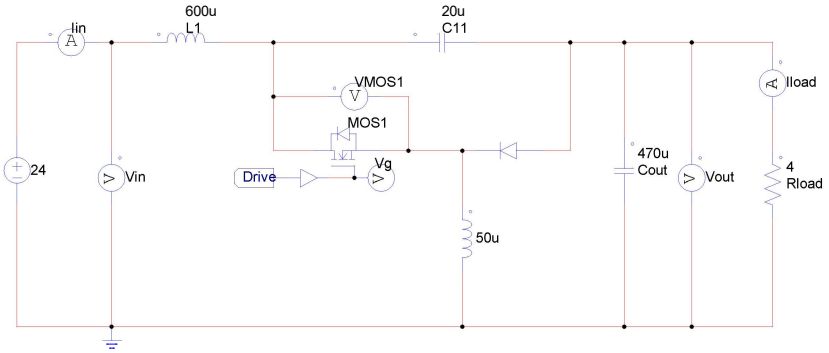


Fig. 2.44 D1 converter simulation model in PSIM

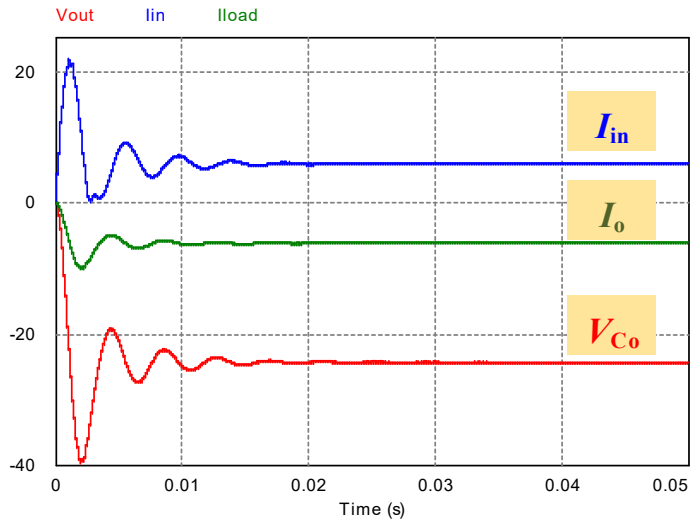


Fig. 2.45 The input current and output voltage waveforms of the D1 converter

When the load is a resistor, the simulation waveforms in Fig. 2.45 verify the transmission ratio of the D1 converter. The input current of the D1 converter can be continuous.

2.7 Summary

This chapter proposes an isolated D2 converter, which was investigated, and its voltage transfer ratio and average model were analysed. The isolated D2 converter with resistive and capacitive loads was simulated in the closed-loop. The simulations verify that the isolated D2 can transfer power, the calculated transfer ratio correctness, its loading capacity and controllability.

An isolated D2 converter hardware platform, comprising a primary circuit, controller, switch gate driver, auxiliary power supply, etc, was used for experimentation. Significantly, the transformer winding and magnetic core in the actual circuit were analysed, and two transformers were wound, one on each outer limb of an E-core pair. Resistive and capacitive loads, in closed-loop control, were investigated. The successful experiments validity the presented analysis of the isolated D2 converter.

CHAPTER 3 Isolated D2 dc/dc Converter Applications

As with any isolated switched mode dc to dc converter, the isolation properties of the proposed D2 converter allow free connection of both the primary and secondary sides in the following configurations: input-parallel output-series (IPOS), input-parallel output-parallel (IPOP), input-series output-parallel (ISOP), input-series output-series (ISOS), and variations with isolated sources, including parallel power processing (PPP). There are three isolated dc/dc applications will be introduced in detail.

3.1 PV Application MPPT

3.1.1 Principle

Photovoltaic power generation systems, renowned for their eco-friendly electricity production devoid of pollution, exhibit inherent characteristics necessitating regulatory intervention. Specifically, the photovoltaic module manifests pronounced nonlinearity in its output and susceptibility to fluctuations induced by external environmental variables. Thus, the incorporation of voltage, current, and power regulators within the interface connecting the photovoltaic module to the load, are imperative to ensure optimal system performance and stability.

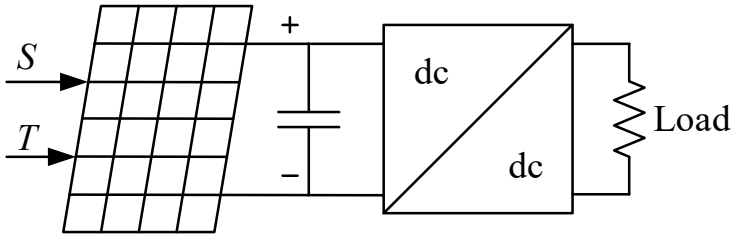


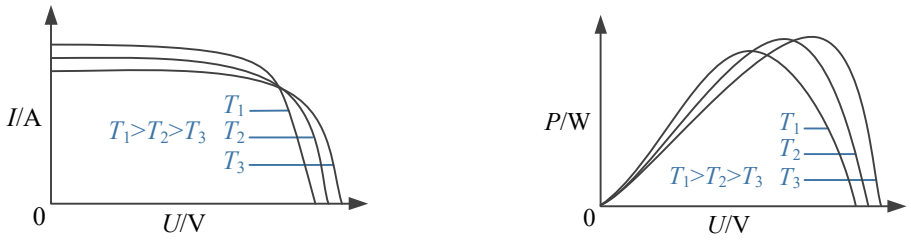
Fig. 3.1 Photovoltaic power generation system

The MPPT system is an electrical system that enables the photovoltaic panel to output maximum electric energy by adjusting the working state of the photo-electrical module. It can effectively store the dc power generated by the solar panel in a battery and can effectively solve the domestic and industrial power consumption issues in remote areas and tourist areas that cannot be covered by the conventional ac power grid. The MPPT controller can detect the generated voltage of the solar panel in real-time and track the maximum voltage, current and power values so that the system can charge the storage battery at the maximum power output. It is the key technology of photovoltaic systems to electrically coordinate solar panels, batteries and loads.

Photovoltaic cells have different output characteristics under different external environmental conditions, such as their parameters affected by light intensity and external temperature. No matter how these external environmental conditions change, photovoltaic cells have only one maximum power point (MPP). So, some topologies and methods can be used to track the MPP.

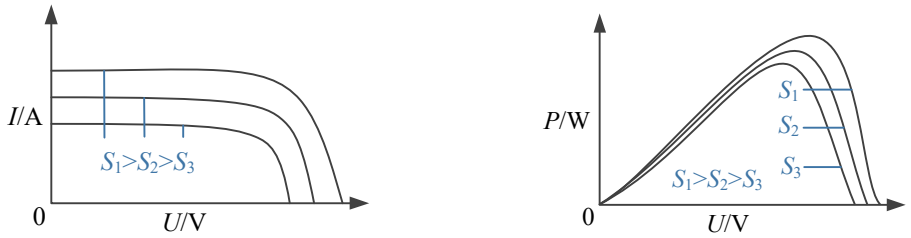
The output power of the photovoltaic cell is related to the working voltage of the MPPT controller. Since the solar cell is influenced by external factors such as light intensity

and temperature, its output power is variable, and a stronger light intensity results in more electricity. PV *I-U* and *P-U* characteristic curves are shown in Fig 3.2 and 3.3 [143].



(a) *I-U* output characteristic curve (b) *P-U* output characteristic curve

Fig. 3.2 Output characteristic curves with constant light intensity



(a) *I-U* output characteristic curve (b) *P-U* output characteristic curve

Fig. 3.3 Output characteristic curves with constant temperature

The photovoltaic power generation system can be represented by the equivalent circuit in Fig. 3.4 [144], [145].

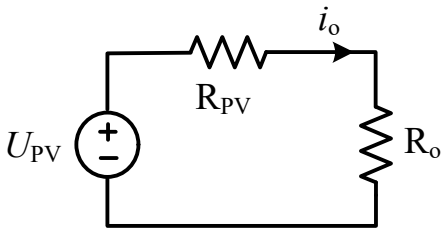


Fig. 3.4 Photovoltaic power generation system equivalent circuit

The power consumed by the resistor R_{load} is:

$$P_o = \left(\frac{U_{pv}}{R_o + R_{pv}} \right)^2 \times R_o \tag{3-1}$$

The derivative of equation (3-1) is:

$$\frac{dP_o}{dR_o} = \left(\frac{U_{pv}}{R_{pv} + R_o} \right)^2 - \frac{2R_o U_{pv}^2}{\left(R_{pv} + R_o \right)^2} = \frac{U_{pv}^2 \left(R_{pv} - R_o \right)}{\left(R_{pv} + R_o \right)^3} \tag{3-2}$$

According to the maximum power transmission theorem, maximum power transmission occurs when the load impedance matches the system's equivalent

impedance. That is, when $R_{pv} = R_o$, the derivative is zero, and the power output is a maximum. Therefore, it is necessary to adjust the equivalent resistance of the dc/dc converter to make it equal to the internal resistance of the photovoltaic cell so as to realize tracking of the MPP.

A converter with MPPT makes full use of the solar cell's capability so that when the solar radiation remains constant, the output power with MPPT will be the highest possible.

With only one switch in a dc/dc converter, control can be simple. There is one capacitor between the photovoltaic panel output and the converter input transmitting energy, which reduces the whole volume and increases power density. If the photovoltaic power generation system is to have no direct electrical connection between the photovoltaic panel side and the power consumption side; the isolated D2 can meet these requirements. The converter can not only stabilize the input voltage and power but also realize MPPT. The isolated D2 converter used in the PV application topology is shown in Fig. 3.5 for a resistive and Fig. 3.6 for a capacitive charging load.

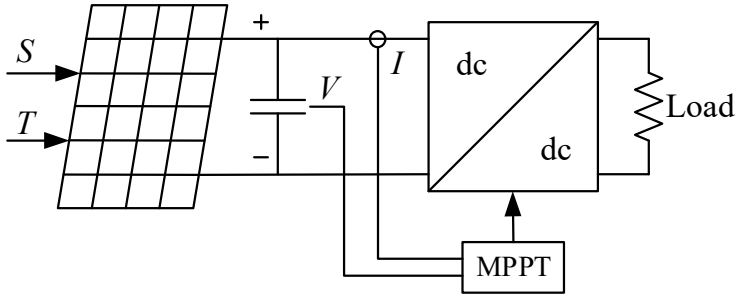


Fig. 3.5 MPPT control frame, resistive load

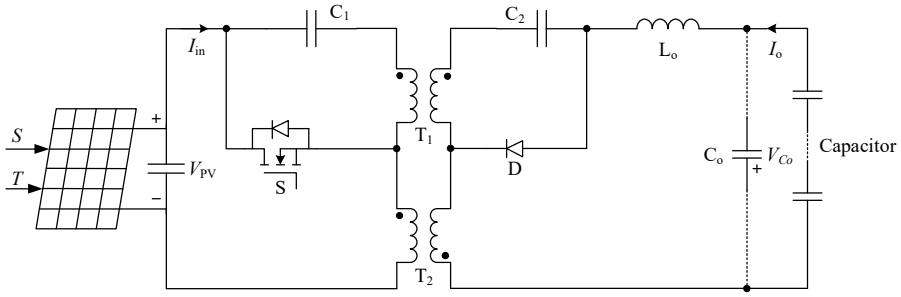


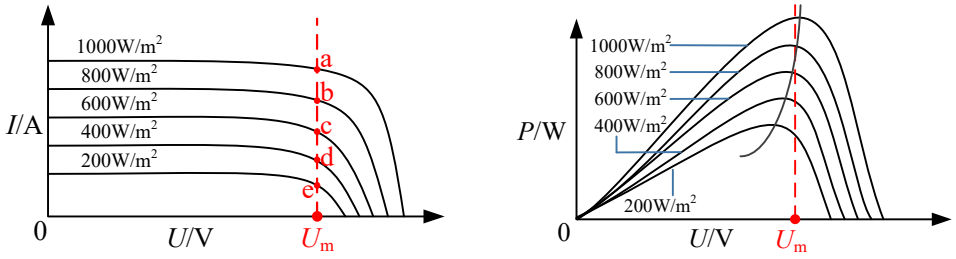
Fig. 3.6 The isolated D2 converter in PV MPPT application, capacitive load

3.1.2 Algorithms

Common MPPT control methods include constant voltage tracking (CVT), perturb and Observe algorithms (P&O) and Incremental conductance (INC).

i Constant Voltage Tracking (CVT)

Constant Voltage Tracking (CVT) [146] uses an approximate proportional relationship between the working voltage of photovoltaic cells at the maximum output power point U_m and its open circuit voltage U_{oc}. Assuming that the PV is in a constant external ambient temperature. Although light intensity has a greater impact on PV output power, it has little impact on the working voltage at the maximum power point. Therefore, it can be considered that the working voltage at the maximum power point of the photovoltaic cell remains unchanged when the external ambient temperature remains unchanged.



(a) *I-U* output characteristic curve (b) *P-U* output characteristic curve

Fig. 3.7 Output characteristic curves with constant temperature and U_m

Fig. 3.7 (a) shows the relationship between the voltage at the maximum power and the open circuit voltage. The abscissa corresponding to points a, b, c, d and e are the working voltage at the maximum power point of the photovoltaic cell under the given working conditions. The voltage of these points are approximately equal; that is, U_m can be assumed constant. When the ambient temperature and light intensity change little, it can be concluded that there is an approximately linear relationship between the voltage U_m at the maximum power point of the photovoltaic cell and the open circuit voltage U_{oc}.

$$U_m = kU_{oc} \tag{3-3}$$

where k is the proportional coefficient, which is less than 1 for different kinds of photovoltaic cells; generally between 0.7 and 0.85.

In Fig. 3.7 (b), when the light intensity changes at constant temperature, the maximum power point is basically around the near vertical red dotted line. So the photovoltaic cell output voltage is fixed to be approximately equal to the voltage value of the maximum power point under this light intensity. When the PV output voltage is assumed constant U_m, (hence constant voltage tracking, CVT), the output power can be regarded as the maximum power point.

The advantage of CVT is that its structure is simple and easy to implement, and the system is stable. Although used in some photovoltaic systems, the unaccounted influence of temperature change on output power results in system energy loss.

ii Perturb and Observe (P&O)

The perturbation observation (P&O) method [147], [148], [149], [150] is a mature algorithm and it is a widely used strategy in MPPT algorithms.

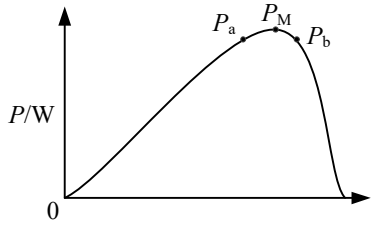


Fig. 3.8 Perturbation observation method (P&O) diagram

The basic principle of the disturbance observation method is that firstly, the output power P_a is measured when the photovoltaic cell functions under a certain reference voltage or current, and then a disturbance is added to the reference voltage or current, such as a forward voltage disturbance; the output power P_b after the disturbance is also measured. Compare P_a with P_b: if

- $P_b > P_a$, the disturbance direction is correct and continue to add disturbance momentum in this direction.
- $P_b > P_a$, the disturbance direction is reversed and the disturbance momentum should be added in the opposite direction.

In this way, the disturbance momentum should be added repeatedly until the PV output power stabilized near the maximum power point.

This method continuously detects the output voltage and current and calculates the output power. Disturb the voltage or current, calculate the value of output power and

then judge the increase or decrease of the power after disturbance so as to change the disturbance direction. In practice, it is difficult to disturb the PV working voltage or current. Generally, the duty cycle of the dc/dc converter is taken as the disturbance, and the output power is changed by changing the dc/dc converter duty cycle.

The advantages of P&O are that the control strategy is relatively simple and easy to implement, and the system hardware is simple.

Continuous disturbance is added to the controlled object. If the external environmental conditions change greatly, disturbance observation failure may result in "misjudgment". The selection of disturbance step size also plays an important role in the disturbance observation method. The larger the disturbance step, the less time it takes for the system to track to the maximum power point, that is, the faster dynamic response speed, but the greater the system oscillation amplitude at the maximum power point, resulting in lower steady-state accuracy, and the greater energy loss. However, if the step size is smaller, the system needs more disturbances and a longer time to track to the maximum power point, but the oscillation amplitude of the system is smaller, and the power loss is lower.

The "misjudgment" and steady-state oscillation of the system are further analyzed in the following subsections.

(1) P&O Misjudgment

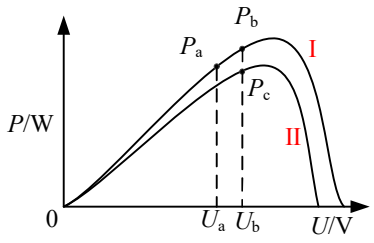


Fig. 3.9 P&O Misjudgment

Assuming that the light intensity changes significantly during the disturbance control process, from curve I to curve II in Fig. 3.9. Before the change, the photovoltaic cell operates at point ‘a’ on curve I, and the output power is P_a. In the next step of disturbance, the forward voltage disturbance is applied to make the output power reach P_b. When the external environmental conditions remain unchanged, the forward voltage

disturbance continues to be applied because the output power P_b after disturbance is larger than the output power P_a. However, when the light intensity changes, which changes the *P-U* characteristic curve from I to II, the measured output power P_c is less than the output power P_a. Therefore, the reverse voltage disturbance will be added in the next disturbance, and the system will "misjudge".

(2) Oscillation Analysis

When the system finally stabilizes near the maximum power point, it swings up and down at the maximum power point, oscillation.

Assuming that the system is at point 'a', the working point voltage is U_a, the corresponding output power is P_a, and this voltage U_a is on the left of the voltage U_m at the maximum power point. The difference between the two voltages is less than or equal to the disturbance step size ΔU, that is, $U_m - U_a \leq \Delta U$. Since $U_a < U_m$ and $P_a < P_m$, the system needs to add disturbance in the direction of power increase, so the working point becomes point 'b', and the corresponding power is P_b. Then, the working point voltage is $U_b = U_a + \Delta U$. Next the values of P_a and P_b are judged to determine the system disturbance direction. Two cases can occur.

Case 1:

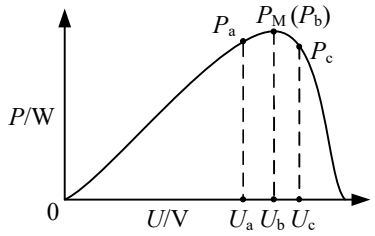


Fig. 3.10 The first case diagram of Oscillation analysis

After disturbance $P_b = P_m > P_a$, the system continues to apply forward disturbance voltage ΔU, then the working point voltage is $U_c = U_b + \Delta U$, and $P_c < P_b$ at this time. Then the system adds the reverse disturbance voltage ΔU, so the working point voltage becomes U_b, and $P_b > P_c$. The system will continue to add the reverse disturbance voltage ΔU, and the working voltage becomes U_a. At this time, $P_a < P_b$. The system will add the forward disturbance voltage ΔU, and in this way, the system will oscillate back and forth between P_a, P_b (P_m) and P_c. Case 1 results in the following energy loss:

$$P_{loss} = 2P_m - P_a - P_b \tag{3-4}$$

Case 2:

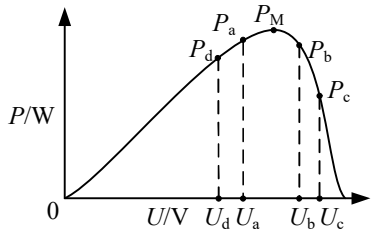


Fig. 3.11 The second case diagram of Oscillation analysis

Case 2 can be divided into three situations.

(a) $P_b > P_a$

At this time, the working point voltage is $U_b = U_a + \Delta U$, $P_b > P_a$, so then,

Add disturbance	Working voltage point	Output power	
forward	U_c (= $U_b + \Delta U$)	P_c (< P_b)	→
reverse	U_b (= U_c - ΔU)	P_b (> P_c)	→
reverse	U_a (= U_b - ΔU)	P_a (< P_b)	→
forward	U_b (= $U_a + \Delta U$)	P_b (> P_a)	→···

In this situation, the power loss is:

$$P_{loss} = 3P_m - P_a - P_b - P_c \tag{3-5}$$

(b) $P_b < P_a$

At this time, the working point voltage is $U_b = U_a + \Delta U$, $P_b < P_a$, so then,

Add disturbance	Working voltage point	Output power	
reverse	U_a (= U_b - ΔU)	P_a (> P_b)	→
reverse	U_d (= U_a - ΔU)	P_d (< P_a)	→
forward	U_a (= $U_d + \Delta U$)	P_a (> P_d)	→
forward	U_b (= $U_a + \Delta U$)	P_b (< P_a)	→···

In this situation, the power loss is:

$$P_{loss} = 3P_m - P_a - P_b - P_d \tag{3-6}$$

(c) $P_b = P_a$

In this situation, the output power oscillates between P_m and P_a. The power loss is:

$$P_{loss} = 2\left(P_m - P_a\right) \tag{3-7}$$

In conclusion, when the light intensity changes suddenly, the system may have a 'misjudgment'. Therefore, the P&O is suitable for small and medium-sized power systems with small or stable changes in the external environment to reduce misjudgment. The system stable oscillation amplitude is related to the disturbance step size. In order to reduce power loss as much as possible, on the premise that the system meets the dynamic response speed, the system disturbance step size should be reduced as much as possible to reduce unnecessary power loss.

iii Incremental Conductance (INC)

The incremental conductance method [38], [151], [152] (INC) is based on the fact that there is only one maximum power point in the *P*-*U* characteristic curve of the PV.

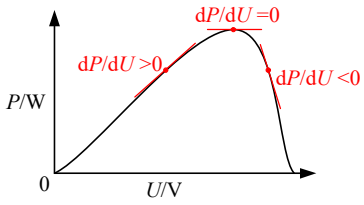


Fig. 3.12 The schematic of INC

From the PV *P*-*U* characteristic curve, the cell output power *P* is a function of its output voltage *U*, and the output current *I* is also a function of the output voltage *U*. The derivative d*P*/d*U* is obtained by deriving the output power *P* from *U*. The relationship between the working voltage and the voltage at the maximum power point is compared by the relationship between the derivative d*P*/d*U* and zero.

When

- d*P*/d*U* > 0, the PV working voltage *U* is on the left side of the voltage U_m at the maximum output power point;
- d*P*/d*U* < 0, the working voltage *U* is on the right side of the voltage U_m; and
- d*P*/d*U* = 0, the working voltage *U* equals the voltage U_m at the maximum output power point.

However, in practice, the relationship between the output voltage *U* and the voltage U_m

is not determined directly by judging the relationship between dP/dU and zero.

PV output power is:

$$P = UI \tag{3-8}$$

Derivative of U is:

$$\mathrm{d}P / \mathrm{d}U = I + U\frac{\mathrm{d}I}{\mathrm{d}U} \tag{3-9}$$

When

- dP/dU > 0, I+UdI/dU > 0, dI/dU > -I/U, then $U < U_m$;
- dP/dU = 0, I+UdI/dU = 0, dI/dU = -I/U, then $U = U_m$; and
- dP/dU < 0, I+UdI/dU < 0, dI/dU < -I/U, then $U < U_m$.

From this analysis, the maximum output power of photovoltaic cells can be found by judging the relationship between dI/dU and -I/U.

If

- dI/dU > -I/U, the working voltage U is less than voltage U_m at the maximum power point, and the PV output voltage should be increased;
- dP/dU = 0, the working voltage U is equal to U_m, and the output voltage should remain unchanged; and
- dP/dU < 0, the working voltage U is greater than U_m, and the PV output voltage should be reduced.

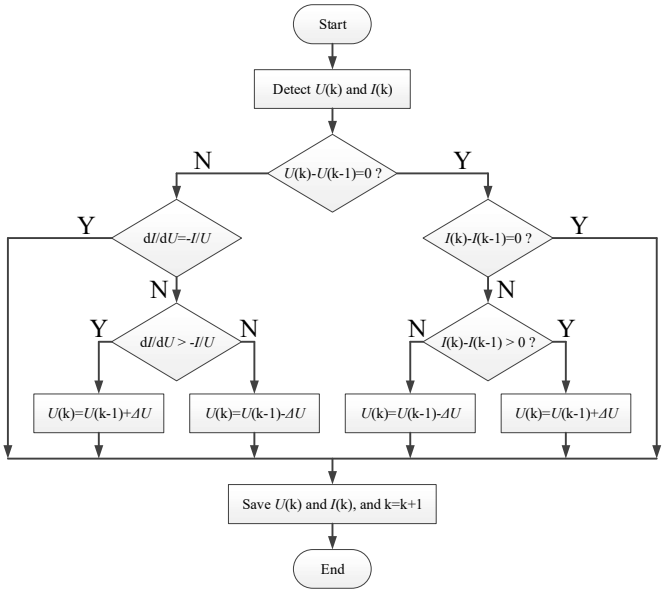


Fig. 3.13 The flow chart of INC

Fig. 3.13 shows a control flow chart for INC, where ΔU represents the disturbance step. INC determines the voltage change by comparing the instantaneous conductance and the PV change of conductance. The previous working voltage and previous output power are not needed, and INC can respond quickly to sudden external environment changes. This method is simple and can improve tracking accuracy and achieve high tracking efficiency.

However, the step size can be problematic. Too large or too small a step will cause power loss, so a fixed step size is not easy to select. The accuracy requirements of the sensor are high, which increases equipment costs. INC cannot inherently prevent oscillations after a sudden change in light intensity.

From the three methods, based on response speed, steady-state accuracy and operability, INC is selected to illustrate the isolated D2 converter in the following simulations and experiments.

3.1.3 MPPT Simulation

i Resistive Load

In PV applications, the isolated D2 converter is used as a dc/dc converter to control PV input voltage and input current to realize MPPT. Time-domain modelling in PSIM is according to Fig. 3.5 and Fig. 3.6.

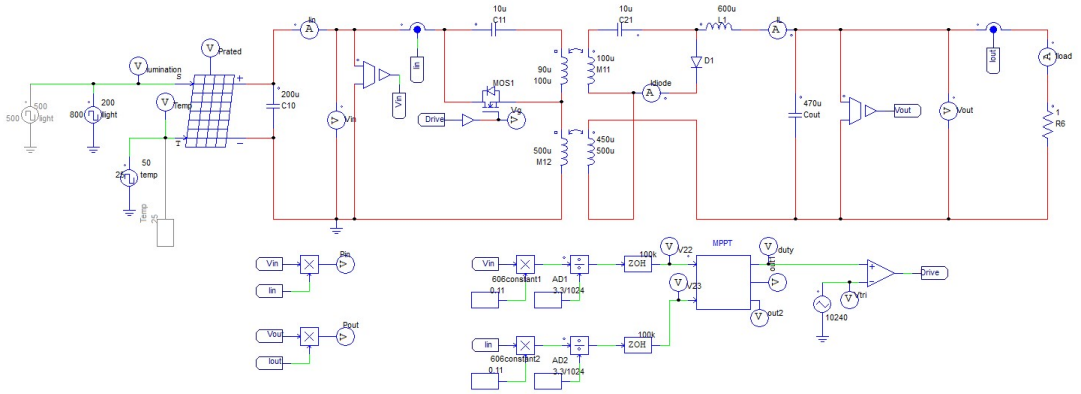


Fig. 3.14 The isolated D2 converter in PV application, simulation model

In the simulation waveforms, the temperature is offset by 800 for observation convenience; external factors light intensity and environment temperature waveforms are shown on the upper part of the oscilloscope plots, and real-time maximum power and power are also shown in the figure.

When the temperature is 25 ℃ continuously, and the light intensity decreases from 1000 W/m^2 to 600 W/m^2, the maximum output power can be tracked.

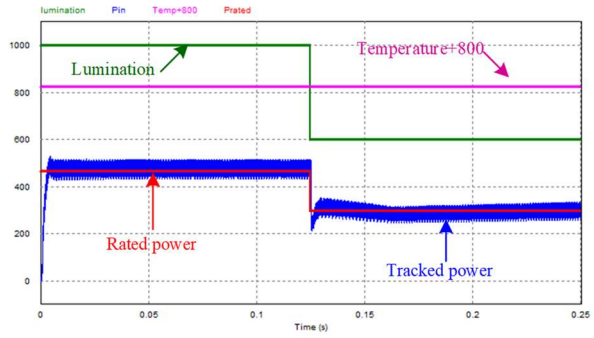


Fig. 3.15 MPPT waveforms (temperature = 25 ℃, light intensity = 1000 W/m^2 → 600 W/m^2)

In Fig 3.15, the red line shows the rated power varying according to the light intensity, and the maximum power is tracked under control. Fig. 3.16 shows the same waveform, but the light intensity varies periodically between 1000 W/m^2 and 600 W/m^2 to verify the function and effectiveness of the isolated D2 converter and MPPT control.

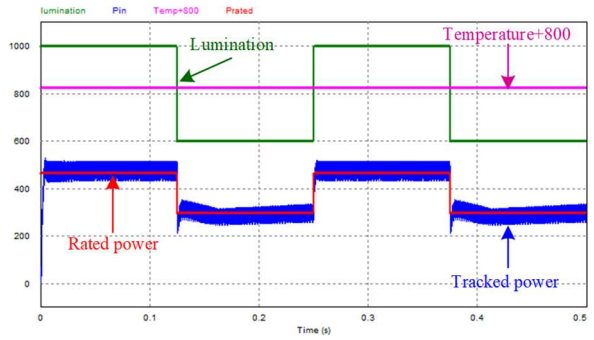


Fig. 3.16 MPPT waveforms (temperature = 25 ℃, light intensity = 1000 W/m^2 ↔ 600 W/m^2)

When the light intensity remains constant, and the temperature changes periodically, the maximum power is tracked in Fig. 3.17.

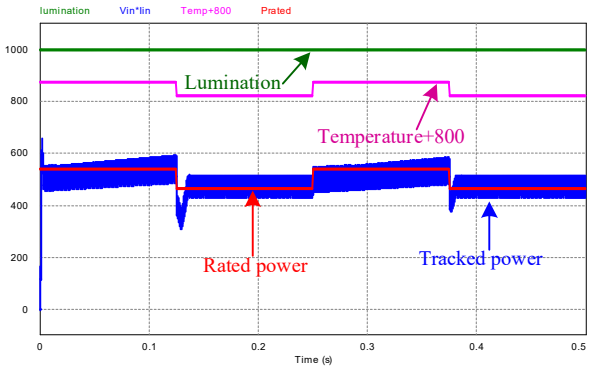


Fig. 3.17 MPPT waveforms (temperature = 25 ℃ ↔ 50 ℃, light intensity = 1000 W/m^2)

Combining the above two situations, both temperature and light intensity change in real time. Fig. 3.18 illustrates that the MPPT control based on the isolate D2 converter is suitable for the PV system application.

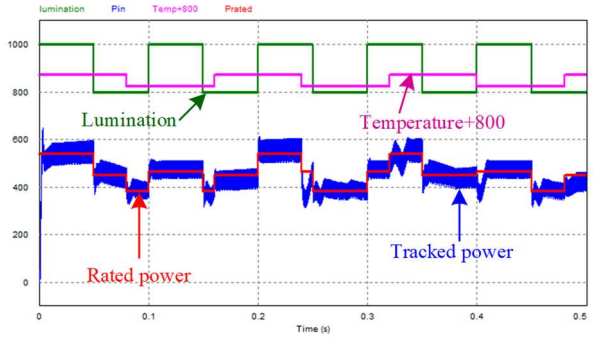


Fig. 3.18 MPPT waveforms

(temperature = 25 °C ↔ 50 °C, light intensity = 1000 W/m^2 ↔ 800 W/m^2)

ii Capacitive Load

In photovoltaic applications, the isolated D2 converter is used as a dc/dc converter to control the input voltage and input current to realize MPPT. The system is used to charge capacitors. The system is different from the isolated converter with resistor load, for the capacitor charging voltage and current should also be under control, and when the capacitor is fully charged, the system should stop any charging.

The topology in Fig. 3.19 shows a capacitor load, such as a super-capacitor.

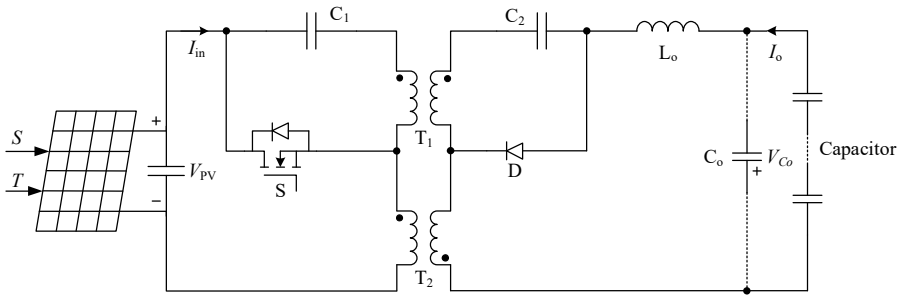


Fig. 3.19 The isolated D2 converter in PV MPPT application with capacitor load

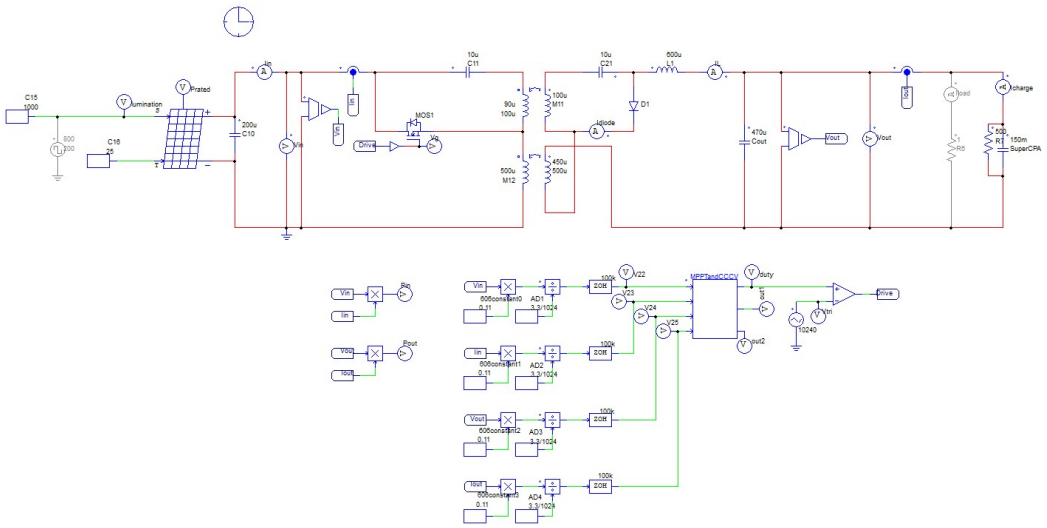


Fig. 3.20 The isolated D2 converter with capacitor load model in the PSIM

In the simulation, the PV panel output voltage and current, and the capacitor charging voltage and current are measured. The light intensity is 1000 W/m^2, the temperature is 25 ℃, the capacitor rated voltage is 30 V, and the initial charging current is 15 A. The MPPT waveform and charging waveform are shown in Fig. 3.21.

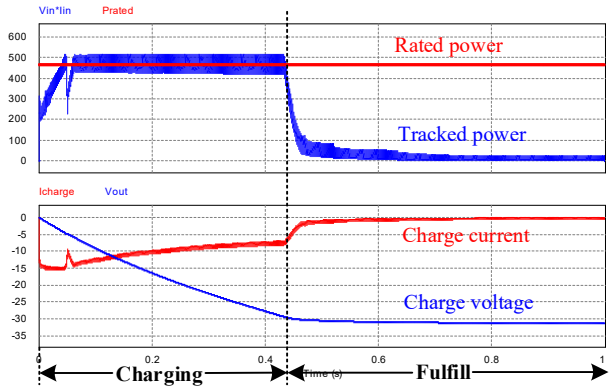


Fig. 3.21 MPPT and Capacitor charging waveforms

(temperature = 25 ℃, light intensity = 1000 W/m^2, rated voltage = 30 V, charging current = 15 A)

MPPT is realized, and when the charge is completed, that is, the capacitor voltage reaches 30 V, MPPT ends, the charging current becomes zero, and the voltage remains at 30 V.

The light intensity varies periodically between 1000 W/m^2 and 800 W/m^2, the temperature is 25 ℃, the capacitor rated voltage is 30 V, and the initial charging current is 15 A, so the MPPT waveform and charging waveform are shown in Fig. 3.22.

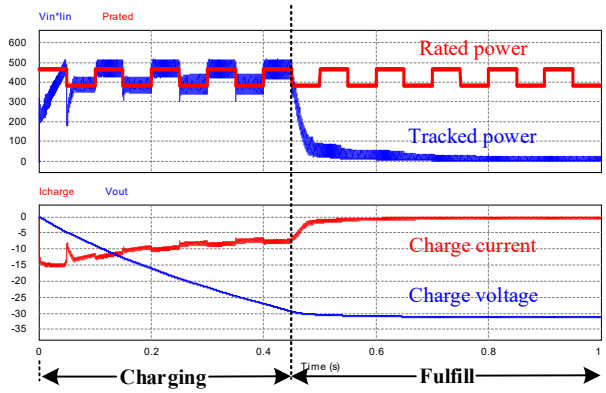


Fig. 3.22 MPPT and Capacitor charging waveforms (temperature = 25 ℃, light intensity = 1000 W/m^2 ↔ 800 W/m^2, rated voltage = 30 V, charging current = 15 A)

The light intensity varies periodically between 1000 W/m^2 and 800 W/m^2, the temperature varies periodically between 25 ℃ and 50 ℃, the capacitor rated voltage is 30 V, and the initial charging current is 15 A; so the MPPT waveform and charging waveform are shown in Fig.3.23.

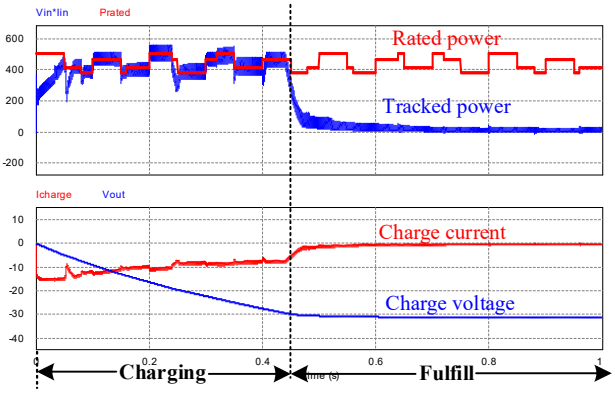


Fig. 3.23 MPPT and Capacitor charging waveforms (temperature = 25 ℃ ↔ 50 ℃, light intensity = 1000 W/m^2 ↔ 800 W/m^2, rated voltage = 30 V, charging current = 15 A)

The isolated D2 converter can realize MPPT and control capacitor charge.

These simulations verify that the topology is able to control the input and output voltage and current and implement the start and stop of the operation, independent of the type of load, with good dynamic response.

3.1.4 MPPT Experimentation

Initially the PV *P-U* output characteristic curve is obtained by testing the output voltage during a day when the light intensity is adequate. During the process, the electronic load voltage is changed and the current is measured so the corresponding power can be

obtained, and then the *P-U* curve is realized.

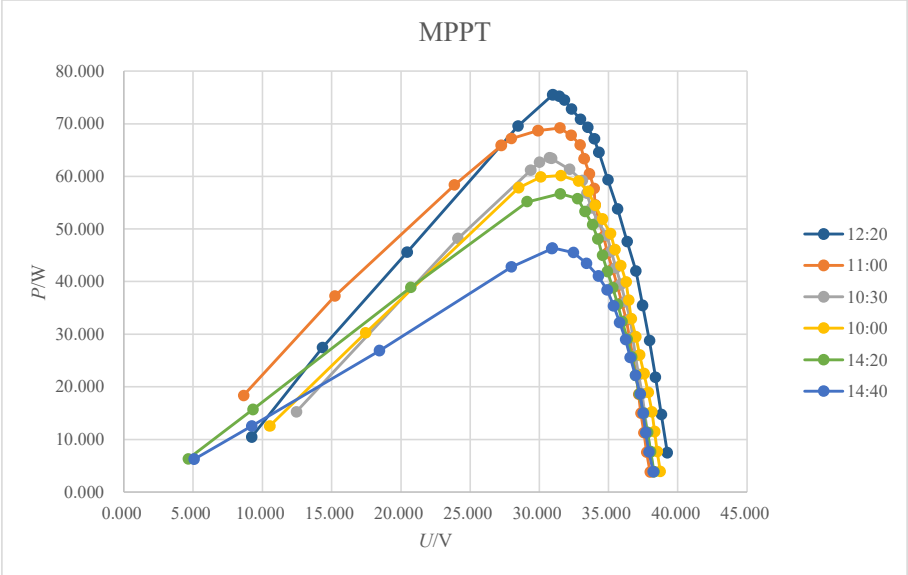


Fig. 3.24 Photovoltaic panel *P-U* output characteristic curves with constant temperature

In Fig. 3.24, the testing time is from 10:00 am to 14:40 pm, the light is sufficient, and the temperature is suitable during this period. In the figure, the PV panel generates higher power when the sun is direct, as opposite to the PV panel around noon (from 10:00 am to 13:00 pm).

The isolated D2 converter hardware used to control the input voltage and input current to realize MPPT is shown in Fig. 3.25.

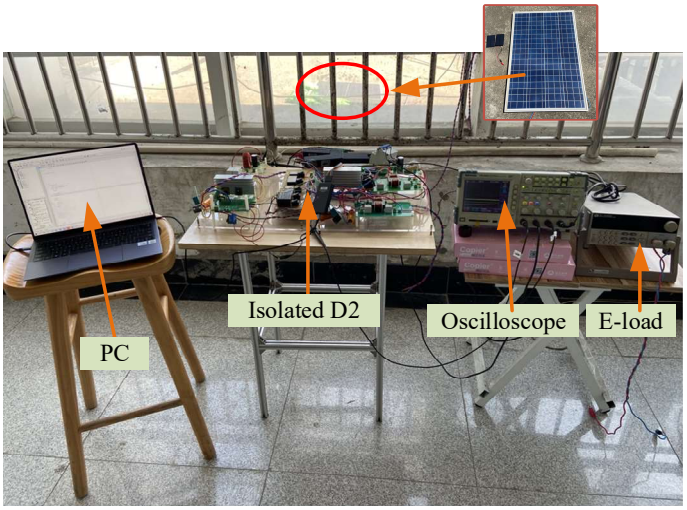
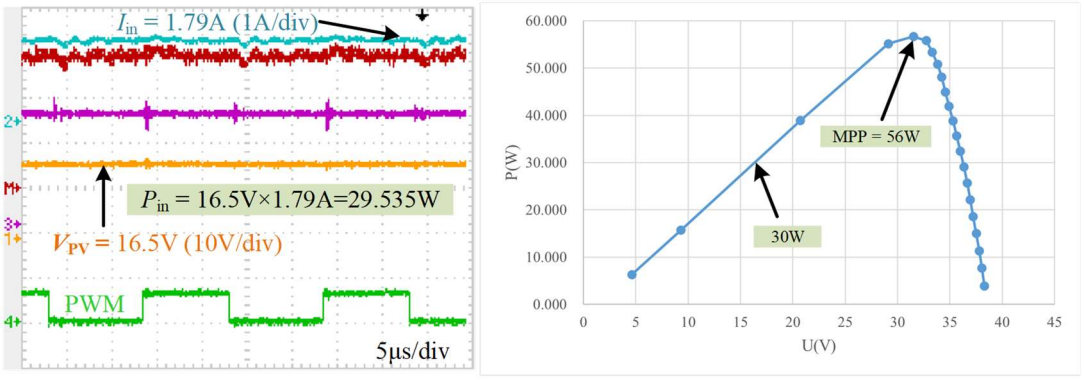
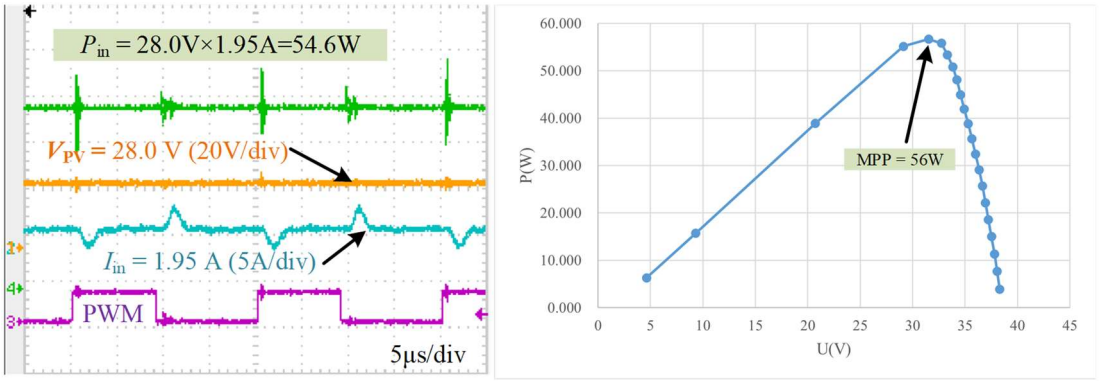


Fig. 3.25 The isolated D2 converter for PV application hardware platform



(a) Open-loop



(b) Closed-loop

Fig. 3.26 The isolated D2 converter MPPT waveforms and maximum point

In the open-loop, when the maximum power is 56W and the tracking power is low, 30 W, the PV panel output voltage is 16.5 V, and the current is 1.79 A, so the output power is 29.5 W (52.7%), and the voltage is not near the MPP voltage.

In the closed-loop, the tracking voltage is 28 V, and the current is 1.95 A, so the tracking power is 54.6 W (97.5%), and the maximum power is tracked.

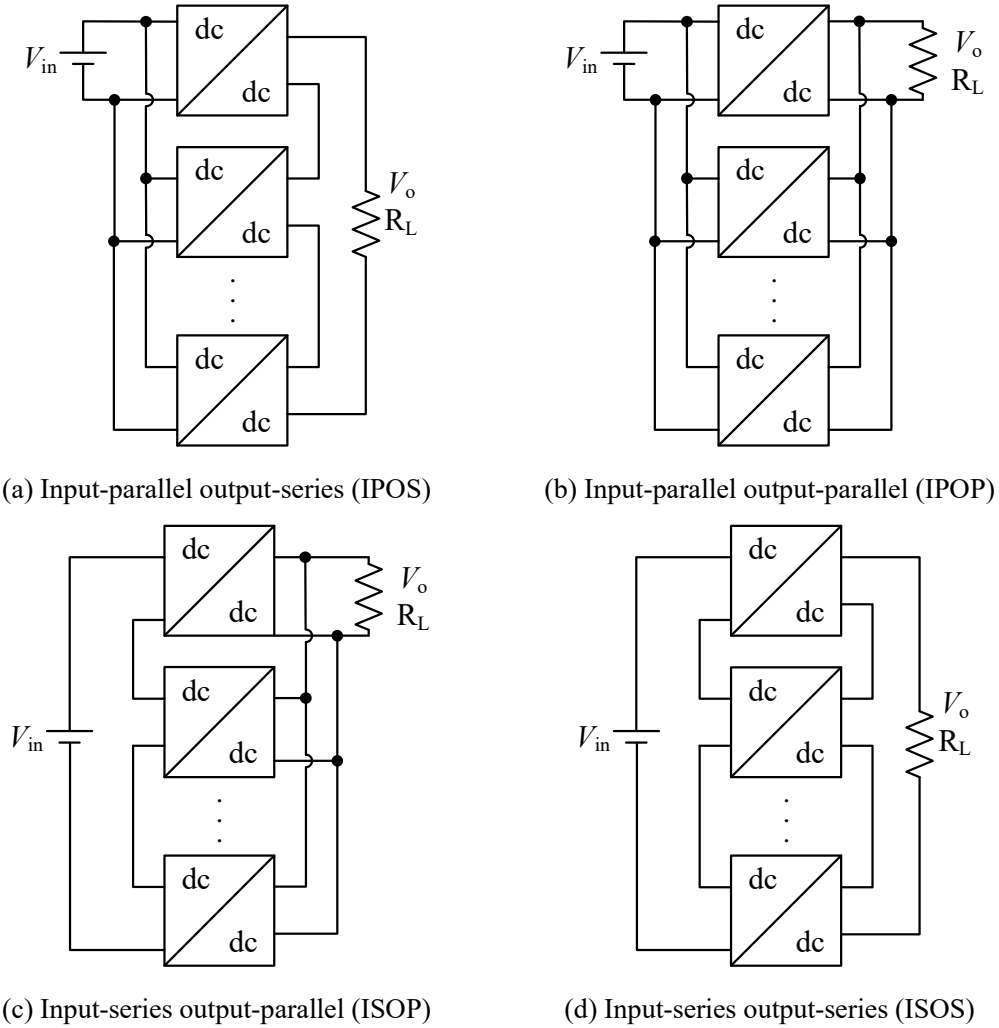
The isolated D2 converter can realize MPPT and verify the topology controls the input and output voltage and current, with good dynamic response. These waveforms illustrate the MPPT control based on the isolate D2 converter is suitable for the PV system application.

3.2 Input-Parallel Output-Series (IPOS) Isolated D2

Because the D2 converter is isolated, the potential of the primary and secondary sides need to be related (electrically).

3.2.1 Input Parallel Output Series Converter

According to the different connection modes of the isolated input and output, modular converters can be divided into the four categories shown in Fig. 2.27 [153] - [160].



(a) Input-parallel output-series (IPOS)

(b) Input-parallel output-parallel (IPOP)

(c) Input-series output-parallel (ISOP)

(d) Input-series output-series (ISOS)

Fig. 3.27 Structure diagram of four series parallel systems

(a) The IPOS converter is mainly suitable for high-power applications, especially for a high transmission ratio between the output voltage and the input voltage. IPOS converter submodules can be input-parallel and output-series to form a high-voltage output system. As an application example where the voltage generated by the photovoltaic panel on the converter input is small, and the system output voltage needs to be high, an IPOS converter can complete the Boost.

(b) IPOP is mainly used in low input voltage and high output current applications, such as uninterruptible power supplies (UPS) and aircraft power supply. The control methods of IPOP converters include centralized control, distributed control and master-slave control. The advantage of the IPOP converter is that with the increase in the number of

parallel sub-modules, the smaller the output ac ripple and the lower the switch current stress.

(c) ISOP converter is composed of submodules connected in input-series and output-parallel. The main advantage of the ISOP converter is that the input-series connection structure can reduce the switch voltage stress. The output current ripple can be reduced, so the filter size can be reduced, and the efficiency and the dynamic characteristics of the system are improved under interleaving control between sub-modules. In the control method, ISOP can realize the natural output current balancing by controlling the input voltage balancing. Some literature proposes the control method of a common duty cycle to realize natural input voltage balance. However, simple control can be affected by the parameter transformation of sub-modules, so cannot achieve accurate voltage balance. Therefore, the most widely used control method is to take the input voltage sampling and add a feedforward loop to realize the input voltage balance.

(d) A ISOS converter is mainly used when the input and output voltage requirements are high, such as with a ship power supply, etc. The ISOP converter is composed of sub-modules connected in input-series and output-series, so the series structure requires voltage-balancing control on both the input and output. The voltage-equalizing mode control of ISOS is similar to that of ISOP. Few ISOS converters are employed.

3.2.2 Advantages of IPOS

Input parallel output series converter has many advantages.

- The input side is a parallel structure. The input current is I_{in}, and the current flowing through the sub-module is I_{in}/n, so the current flowing through the switch is reduced, which can greatly reduce the current stress of each switch.
- The output side is a series structure. The load voltage is V_o, and the output voltage of each sub-module is V_o/n, so the relatively low voltage level of the power switches can be used at the output side, which reduces the selection requirements for the power switch and the costs.
- Compared with the transformer with a high voltage ratio to achieve high voltage step-up, the transformer performance requirements of each sub-module are low in the topology based on IPOS, and the transformer with a small ratio can be selected.

- The IPOS converter can realize modular control. Each slave module output power is 1/n of the total output power, which facilitates the separate design of slave modules and the integrated design of the system.

According to the above analysis and advantages, an IPOS converter is used for dc/dc conversion, and the key point is to control the output voltage of each sub-module on the output side.

3.2.3 IPOS Isolated D2 Converter Example

Two isolated D2 converters form an input-parallel output-series IPOS structure, and the topology is shown in Fig. 3.28. In the topology, the input voltage V_{in} supplies the two isolated D2 converters and the output capacitors are in series. Each converter input voltage is equal to the input voltage V_{in}; each converter input current is half of the total input current; each converter output voltage is half the load voltage; and each output current equals the load current.

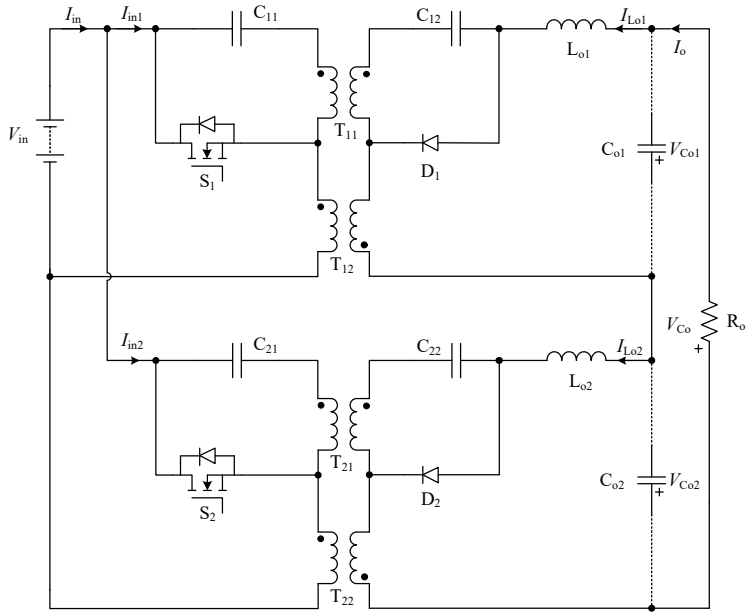


Fig. 3.28 Input-parallel output-series (IPOS) Isolated D2 converter topology

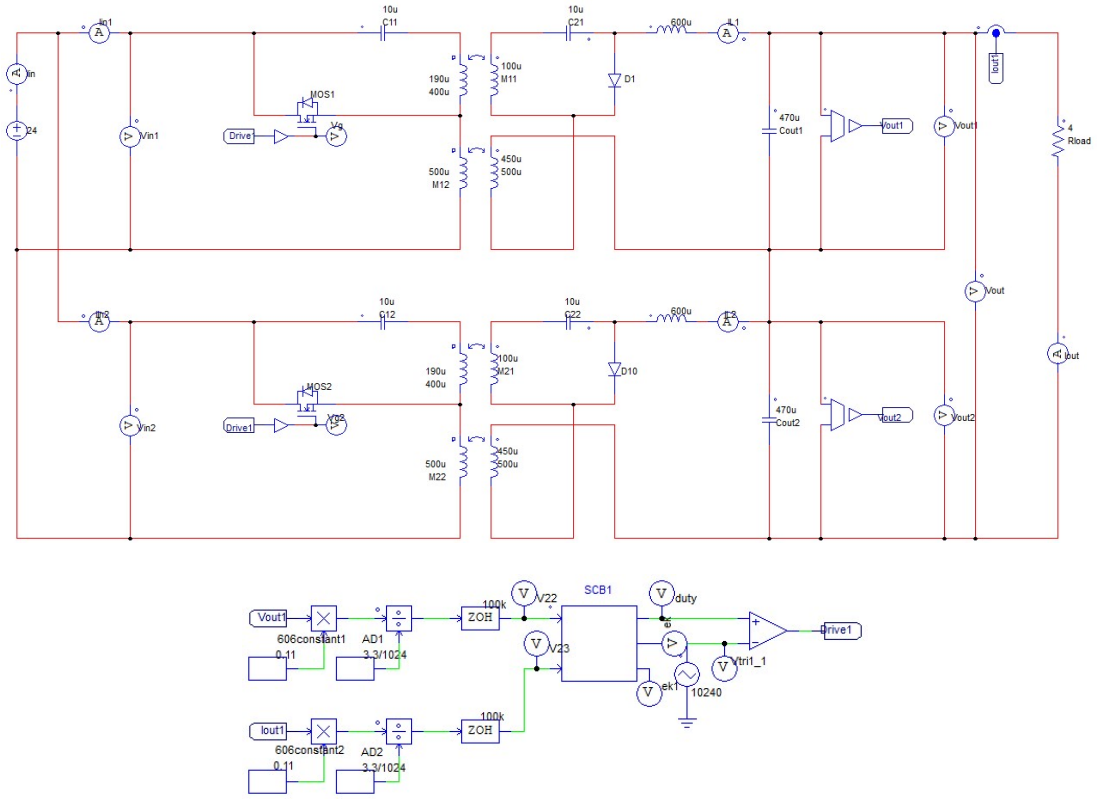


Fig. 3.29 Input-parallel output-series (IPOS) Isolated D2 converter model built in PSIM

IPOS isolated D2 converter PSIM simulation model is shown in Fig.2.29, where the output voltage and current are controlled. The each converter output voltage reference is set as -20 V, and the output current reference is -3 A. The load is 4 Ω, and the system outputs lower power under control, where the output waveforms are shown in Fig. 3.30.

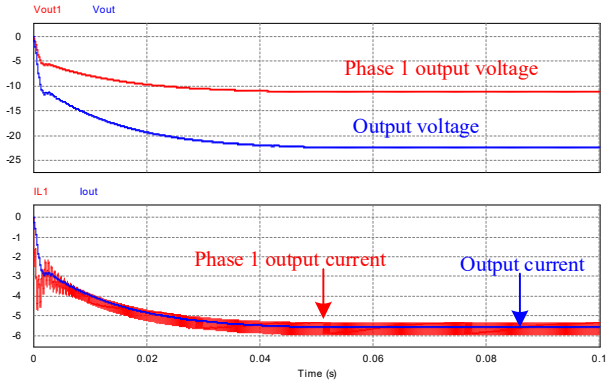


Fig. 3.30 IPOS Isolated D2 converter output voltage and current waveform

(Voltage reference = -20 V, Current reference = -6 A)

The sub-converter output voltage reference is set to -10 V, and the output current reference is set to -6 A. The output waveforms are different from the previous waveforms. One converter output voltage reference is set to -10 V, so the total voltage

is -20 V, and the output power is 100 W, theoretically.

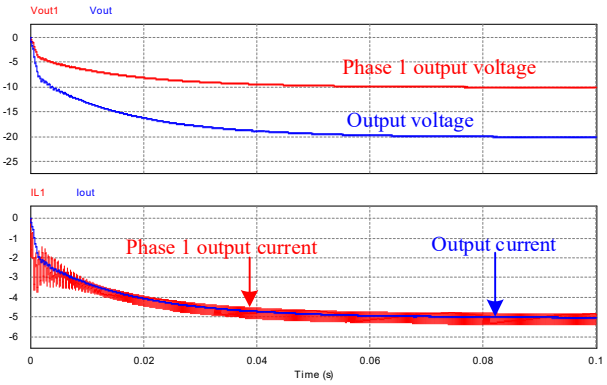


Fig. 3.31 IPOS Isolated D2 converter output voltage and current waveform

(Voltage reference = -10 V, Current reference = -6 A)

In Fig. 3.31, the output voltage and current are controlled, compying with the IPOS characteristics. The voltage and current waveforms confirm that the isolated D2 converter can be cascaded in an input-parallel output-series connection and offers good performance.

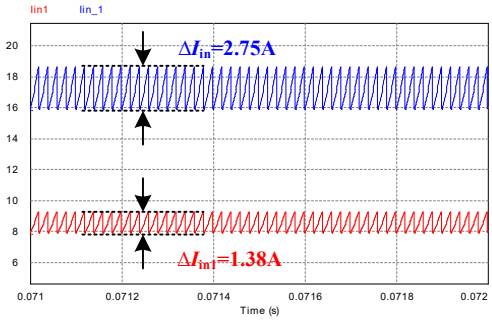


Fig. 3.32 IPOS isolated D2 converter input current ripple

In Fig. 3.32, the current ripple I_{in1} and I_{in2} are 1.38 A, and I_{in} current ripple is 2.75 A, which means each sub-module input current ripple is reduced, and the current flowing through the switch can be reduced, which can reduce the current stress of each switch. Moreover, I_{Lo1}, I_{Lo2} and I_o mean values are 5.566 A, but I_{Lo1} and I_{Lo2} current ripple are 0.571 A, and I_o current ripple is almost 0 A. So that the IPOS isolated D2 converter reduces the output current ripple.

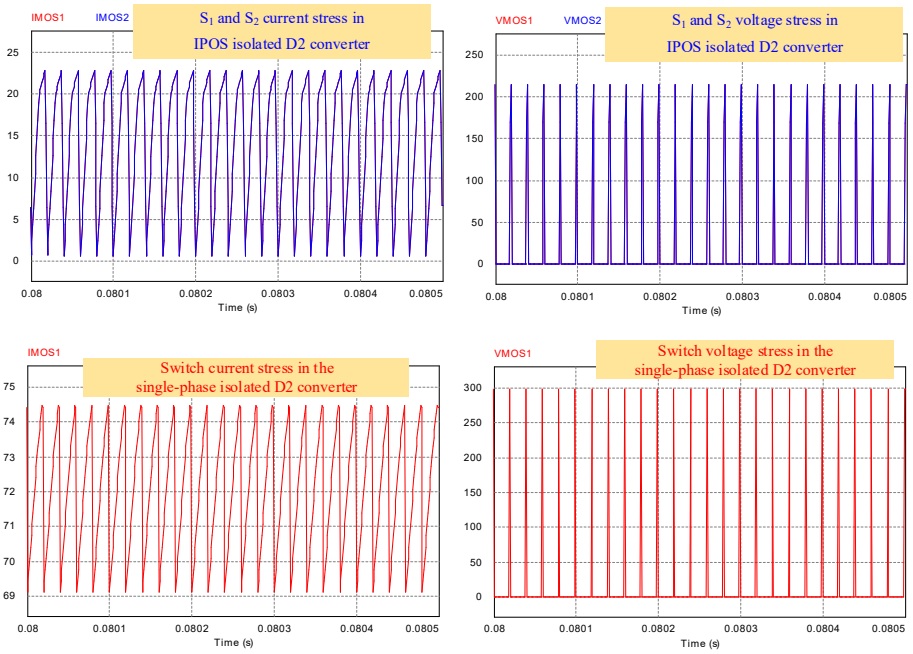


Fig. 3.33 Switch current stress and voltage stress comparison

In Fig. 3.33, in the same condition, the single-stage converter switch current stress is 74.3 A, and in the IPOS converter switch, the current stress is 22.5 A, so the current flowing through the switch is reduced. Also, the single-stage converter switch voltage stress is 300 V, and in the IPOS converter switch voltage stress is 212 V, so the IPOS structure reduces the power switch voltage stress.

Changing the power supply to 220 V dc, in Fig. 3.34, one sub-converter output voltage reference is set as -150 V, and the output current reference is set to -100 A.

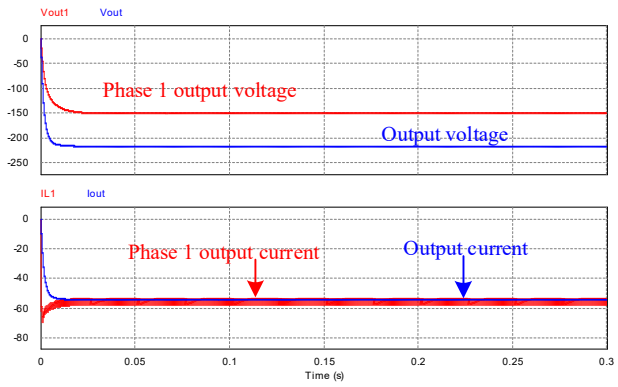


Fig. 3.34 IPOS Isolated D2 converter output voltage and current waveform

(Voltage reference = -150 V, Current reference = -100 A)

These simulation models, control strategies and waveforms verify that the IPOS isolated D2 converter is suitable for high-power applications.

3.2.4 IPOS Isolated D2 Converter Used in PV

As mentioned, the photovoltaic step-up application is suitable for the IPOS converter as a sub-module to complete the boost. A single isolated D2 converter itself is suitable for PV applications, so the IPOS isolated D2 converter simulation model is shown in Fig. 3.35 and Fig. 3.36 built in this section. The dc supply is replaced by a photovoltaic panel.

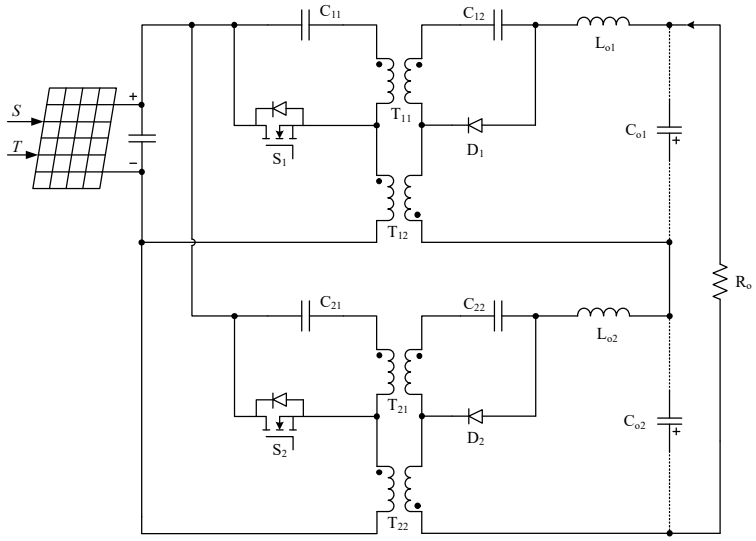


Fig. 3.35 Input-parallel output-series (IPOS) Isolated D2 converter PV application topology

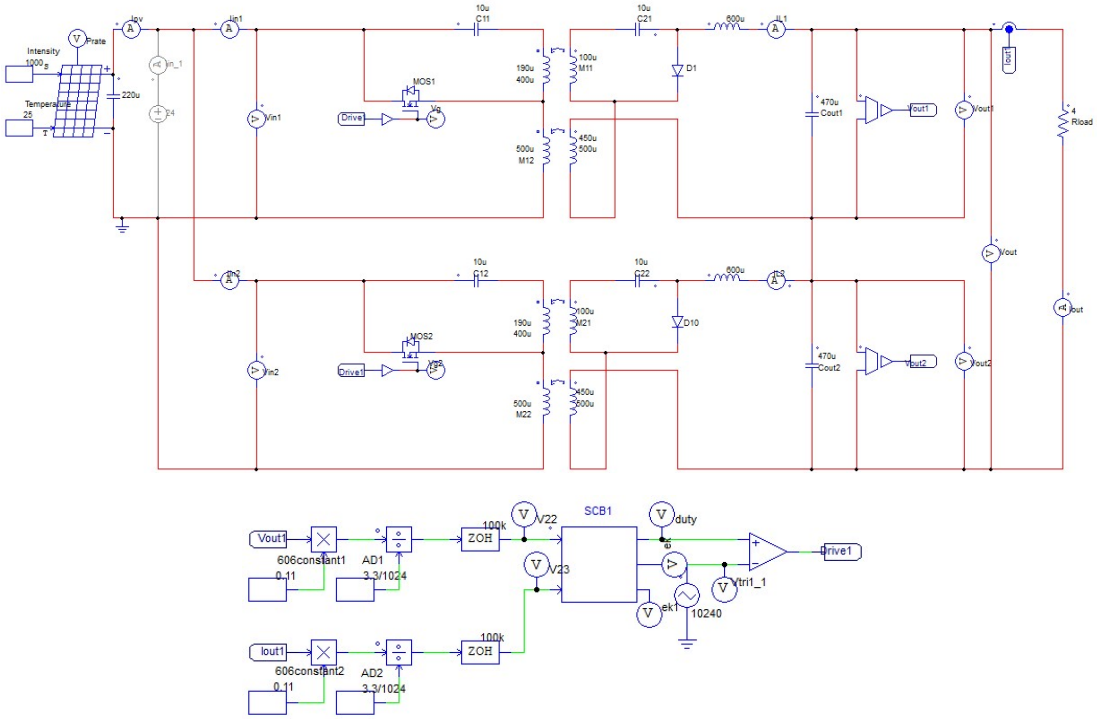


Fig. 3.36 IPOS Isolated D2 converter PV application model built in PSIM

The one sub-converter output voltage reference is set as -25 V, and the output current reference is -5 A.

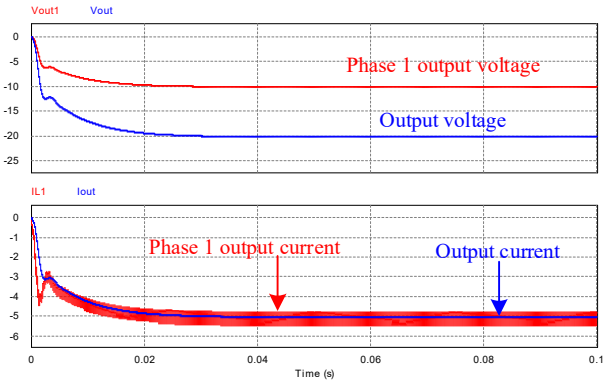


Fig. 3.37 IPOS Isolated D2 converter with PV panel output voltage and current waveform

(Voltage reference = -25 V, Current reference = -5 A)

The output current is -5 A under control, and the output voltage is 4 Ω×-5 A =-20 V.

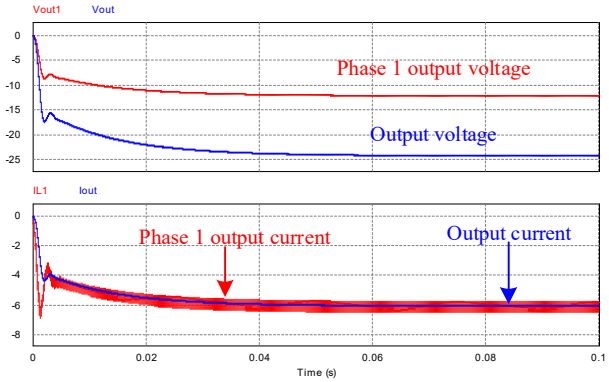


Fig. 3.38 IPOS Isolated D2 converter with PV panel output voltage and current waveform

(Voltage reference = -12 V, Current reference = -8 A)

Changing the references, in Fig. 3.38: each output voltage is -12 V under the control, and the output current is (2×-12 V)÷4 Ω=-6 A.

Thus, the IPOS using the isolated D2 is suited for photovoltaic applications. This application is only implemented through simulation and has not been experimentally validated due to its similarities in hardware with interleaved parallel cascaded introduced in the next section.

3.2.5 IPOS Experimentation

In this IPOS application, the isolated D2 converter controls the two-phase output voltage and two-phase inductor current. To verify the two phases can work

independently, the two transformers turn ratios are wound differently, Phase 1 is 1:1 and Phase 2 is 1:4, respectively. The isolated D2 converter for this IPOS hardware application is shown in Fig. 3.39 and is used to validate the simulations in Fig. 3.37.

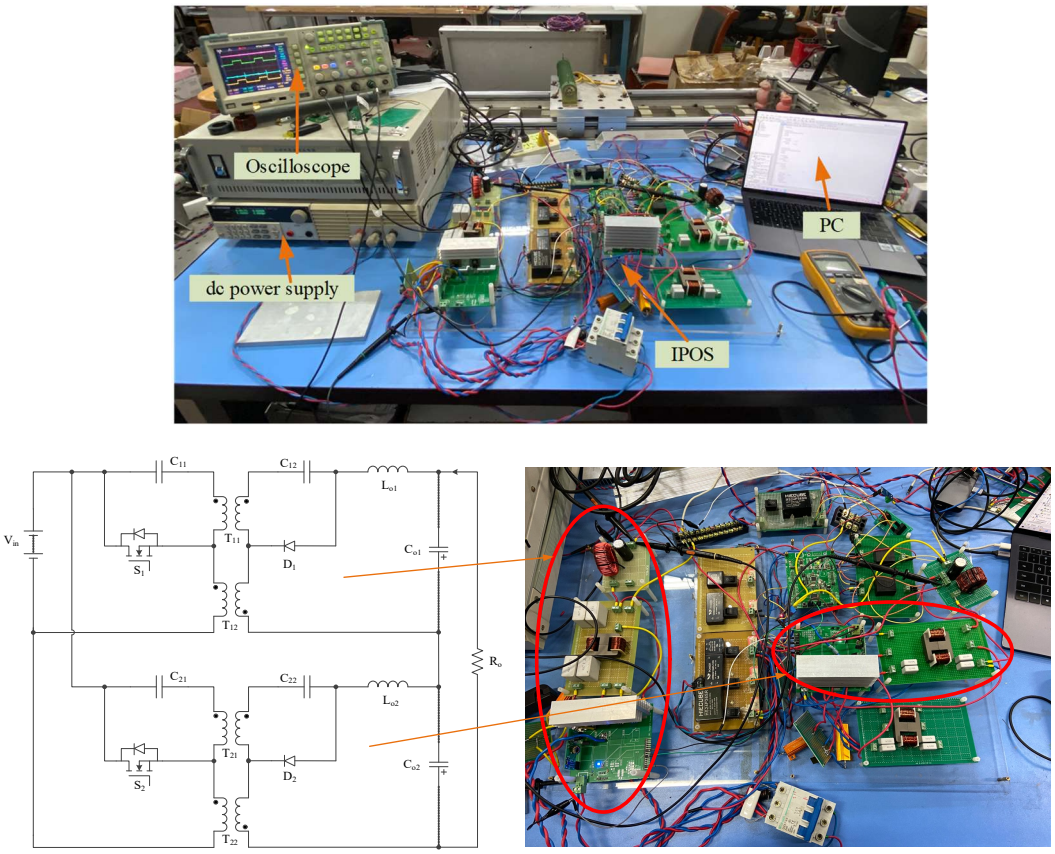


Fig. 3.39 The isolated D2 converter IPOS hardware platform

The IPOS isolated D2 converter open-loop validation experimental results are shown in Fig. 3.40. One stage output voltage (yellow line) is 1.82 V, the other stage output voltage (purple line) is 5.97 V, and the load voltage (green line) is 7.97 V, which satisfies the IPOS output rule.

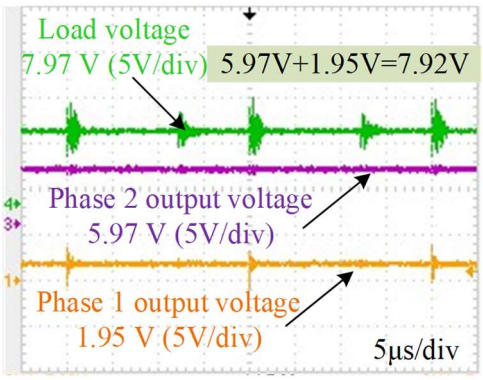


Fig. 3.40 IPOS isolated D2 converter open-loop output voltage waveforms

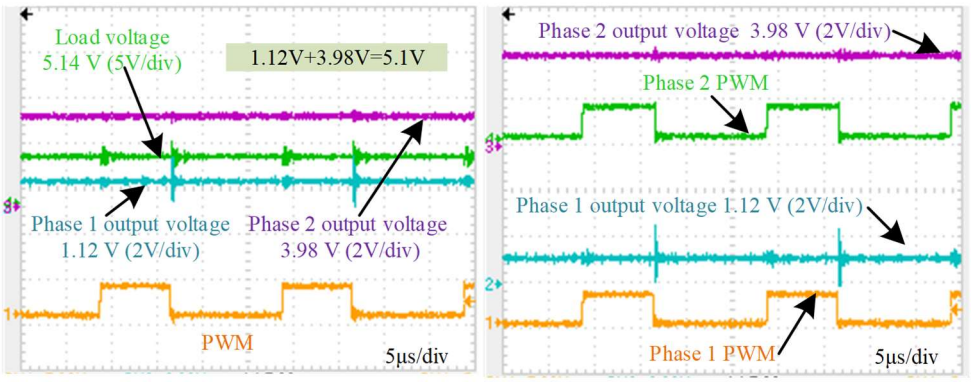


Fig. 3.41 IPOS isolated D2 converter closed-loop output voltage waveforms

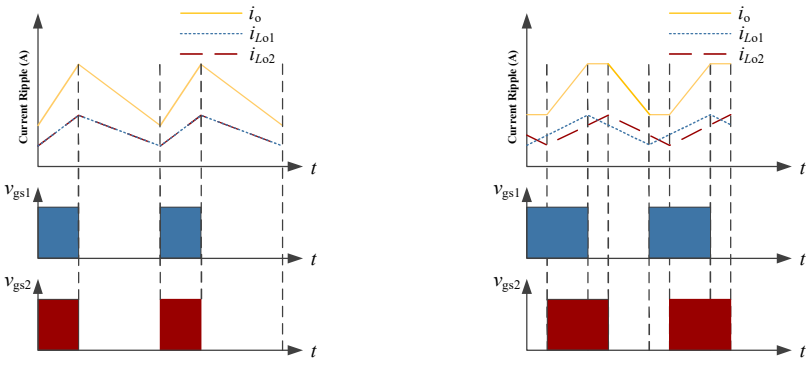
Next, in closed-loop experiments, the IPOS two-stage output voltage and current are controlled. One-stage converter output voltage reference is set as 1 V, and the output current reference is set as 1 A. The load is 8 Ω, and the system outputs lower power under the control, with the output waveforms shown in Fig. 3.41. In addition, with differences in the two transformers, the PWM duty cycles of the two stages are different, which also verifies both isolated D2 converters are controlled.

3.3 Interleaved Isolated D2 Converters

3.3.1 Interleaving Principle

A gradual increase in converter power level poses a challenge to the voltage and current stress of switches. The interleaving technique [70], [72] increases the capacity of the converter by paralleling the multi-stage topology and solves the problems of high stress and insufficient device capacity. Current balancing makes each stage operate under a lower load current, which reduces switch conduction loss. Each stage conducts alternately so that the current of each stage is staggered and then the output superimposed, which not only offsets part of the ripple but also increases the converter working frequency.

The n-(parallel)-stage topology with the same switching frequency is connected in parallel, and the operating modes can be divided into three types: synchronous trigger, independent trigger and interleaving trigger.



(a) Synchronous trigger (b) Independent trigger

Fig. 3.42 Typical waveform diagram of two modes of two-stage parallel operation

Synchronous trigger mode (Fig. 3.42a) refers to when the ON and OFF control signals of n-stages are transmitted out at the same time. The n-stage switches are turned ON and OFF at the same time, the peak and valley values of each stage inductor current are superimposed correspondingly, the total current ripple peak-to-peak value is n times that of one stage current ripple, and the ripple frequency is equal to the switching frequency.

Independent trigger mode (Fig. 3.42b) refers to when the stage of the n-stage topology control signal is random; the switching frequency of each stage is the same, but the starting point of conduction is random. The total current is also randomly superimposed, and the ripple frequency is not fixed.

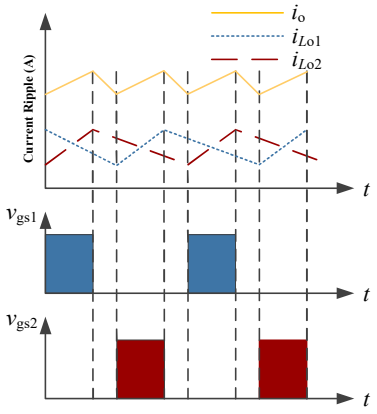


Fig. 3.43 Waveform diagram of interleaving trigger of two-stage parallel operation

Interleaving trigger mode (Fig. 3.43) refers to the control signal phases of n-stage topology that differ by 2π/n, and the currents of each stage are interleaved by 2π/n and then superimposed. The interaction makes the total current ripple peak-to-peak value

less than the current ripple of each stage, and the total current ripple frequency becomes n times one stage current. When the number of parallel stages and duty cycle meet certain conditions, the total current can achieve zero ripple, which is analyzed below.

In summary, the multi-stage parallel topology can employ various control modes, but the interleaving trigger control mode can improve the converter performance to the greatest extent. In the interleaving trigger mode, the equivalent frequency of the converter increases, the current ripple decreases, and the volume of the filter network can also be reduced. Therefore, the parallel isolated D2 converter under interleaving trigger mode will be considered.

3.3.2 Output Inductor Current Ripple Analysis

The basic principle of the interleaving technique is introduced, when it will be seen that different control modes will have different effects on the current ripple. The duty cycle and the number of parallel stages, n, will also affect the current ripple. Fig. 3.44, shows the schematic diagram of a single-cycle inductor current segmentation.

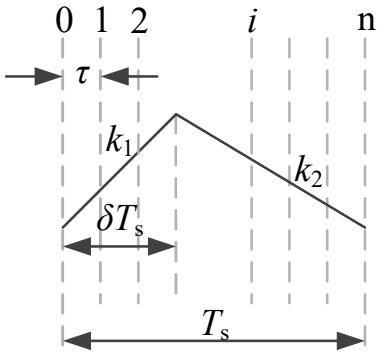


Fig. 3.44 Sectional diagram of single period inductor current

Assumed the converter is composed of an n-stage parallel topology, where the switching cycle period is T_s, and the duty cycle is δ, for all stages. The converter control mode is the interleaving triggering, the working mode of each stage inductance is the continuous current mode (CCM), and the single-stage induced current ripple is ΔI_L. Each cycle T_s is equally divided into n intervals, and the duration of each interval is τ, which is called phase shift time. If the time point is when the inductor changes from the energising state to the de-energising state, Fig. 3.45 is obtained.

According to these assumptions and Fig. 3.45, the following relationships can be

obtained.

$$\tau = \frac{T_s}{\mathrm{n}} \tag{3-10}$$

$$f_s = \frac{1}{T_s} \tag{3-11}$$

$$k_1 = \frac{\Delta I_L}{\delta T_s} \tag{3-12}$$

$$k_2 = -\frac{\Delta I_L}{(1-\delta) T_s} \tag{3-13}$$

where k_1 is the slope of the curve before δT_s, representing the energising rate of the inductor; k_2 is the slope after δT_s, representing inductor de-energising rate.

The period of each stage is the same, T_s, and the converter operates in the interleaving trigger mode. After the inductor current of each stage is superposition, the total current ripple period is equal to the phase shift time τ. Therefore, the variation can be obtained by studying the total current ripple in the interval of phase shift time τ, as shown in fig. 3.45, where there is only one turning point in each phase shift time τ, and the other (n-1) phases are similarly monotonically increasing and decreasing. There may be three cases: when

- $\delta < ½$, the effective waveform increases monotonically;
- $\delta > ½$, the effective waveform decreases monotonically; and
- $\delta = ½$, the equivalent waveform is a horizontal line.

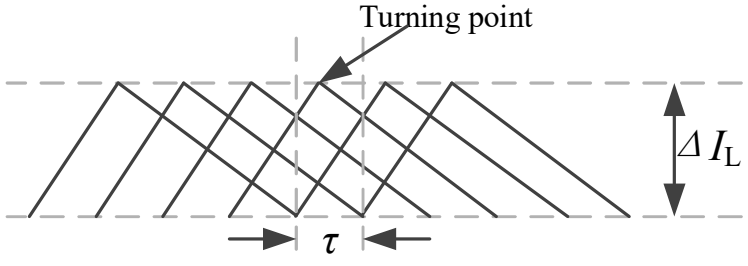


Fig. 3.45 Schematic diagram of n-stage interleaving inductor current

Fig. 3.46 shows the schematic diagram of inductor current ripple synthesis when $\delta < ½$.

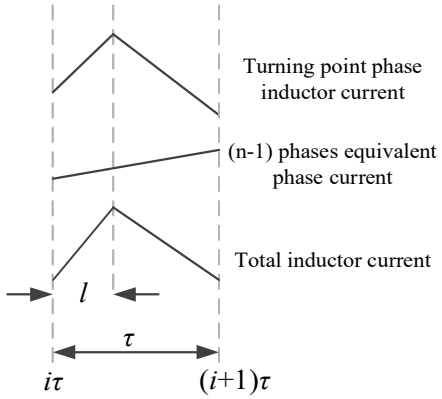


Fig. 3.46 Schematic diagram of inductor current ripple synthesis when $\delta < 0.5$

l is the distance between the turning point and the start of phase shift time τ,

$$l = \delta T_s - i\tau \tag{3-14}$$

After the superposition of n-stage currents, the total current ripple $\triangle I$ is

$$\Delta I = ilk_1 + (\mathrm{n} - i - 1)lk_2 \tag{3-15}$$

After rearranging (2.7), (2.8) and (2.9) in (2.10), the equation (2.11) is obtained.

$$\Delta I = \Delta I_L \left(\delta - \frac{i}{\mathrm{n}} \right) \frac{1 + i - \mathrm{n}\delta}{\delta(1-\delta)} \tag{3-16}$$

where $\dfrac{i}{\mathrm{n}} < \delta < \dfrac{i+1}{\mathrm{n}}, \qquad i = 0,1,2\ldots(\mathrm{n}-1)$.

It can be obtained by normalizing the single-stage current ripple as the pedestal value.

$$K = \frac{\Delta I}{\Delta I_L} = \frac{(\mathrm{n}\delta - i)(1 + i - \mathrm{n}\delta)}{\mathrm{n}\delta(1-\delta)} \tag{3-17}$$

where K is the normalization coefficient, and the total current ripple characteristics diagram can be drawn, as shown in Fig. 3.46. When the number of stages is n = 2, 3, 4, the horizontal axis is the duty cycle δ, and the vertical axis represents the ratio of total current ripple to single-stage current ripple.

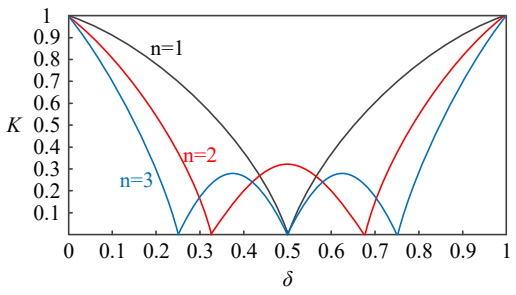


Fig. 3.47 Multi-stage current ripple characteristics in interleaving trigger mode

In Fig. 3.47, the total current ripple is affected by the duty cycle and the number of stages. Also, when the converter is n-stage interleaving parallel, there are n-1 duty cycle points that can achieve zero ripple output.

For n = 2, the interleaving isolated D2 converter topology IPOP is as in Fig. 3.48.

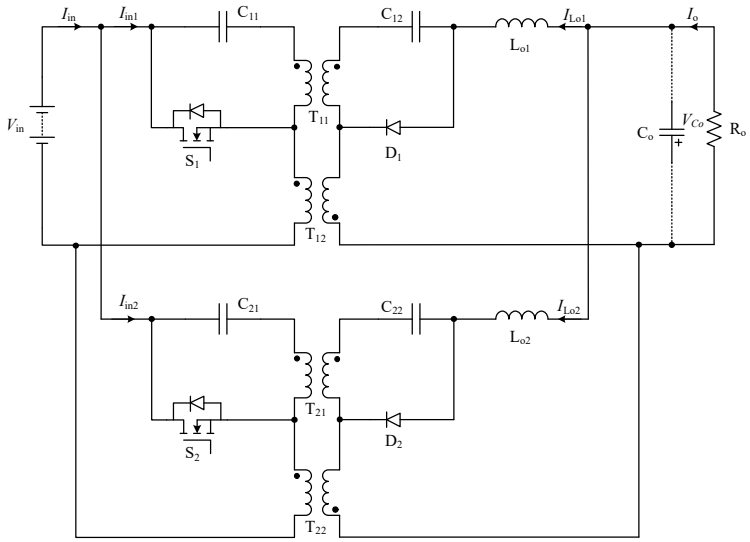
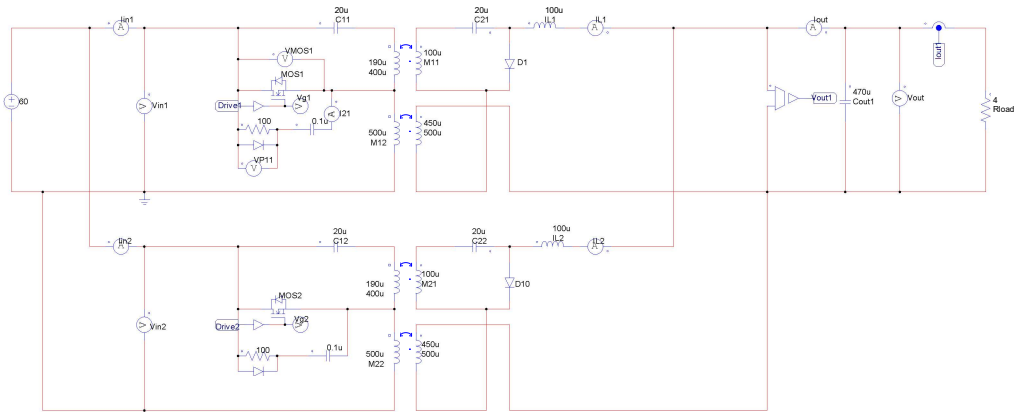


Fig. 3.48 Interleaved isolated D2 converter topology

3.3.3 Interleaved Isolated D2 Simulation

The input voltage is the reference, and the two-stage input current is the controlled variable. According to the analysis and operation modes, in the PSIM model in Fig. 3.49, i_{s1}, i_{s2} and input voltage are sampled; the stage and magnitude of these variables are controlled in the PSIM C block.



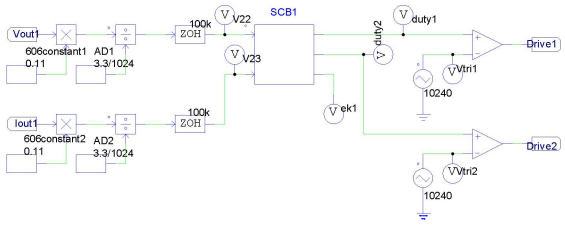


Fig. 3.49 Interleaved isolated D2 converter in the PSIM

In order to observe the effect of interleaving control on inductor ripple current, the output inductance is reduced to 100 μH, while the other component parameters are unchanged. The drive signals of S_1 and S_2, i_{o1}, i_{o2}, and i_o ripple waveforms are shown in Fig. 3.50, where the effect of closed-loop control and simulation components (non-idea transformers, switches, etc.), leads to the output inductor ripple is not a standard current waveform. Although the converter is affected by these practical factors, the interleaving operation still functions. The total inductor current ripple is smaller than that of each stage, and the ripple frequency becomes n times the stage ripple. The current RMS value increases.

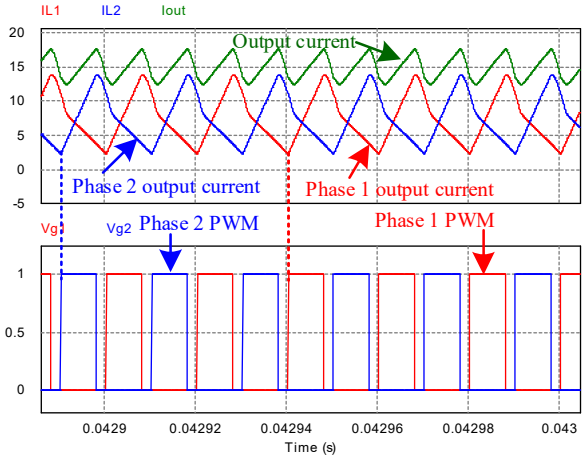


Fig. 3.50 Output current ripple of interleaved isolated D2 converter, simulation

In terms of reducing current ripple, according to (3-17), when the theoretical duty cycle is 0.35 for a two-stage interleaved circuit, the total inductor current ripple is 46.15% for each stage, that is, the normalization coefficient $K = 0.462$.

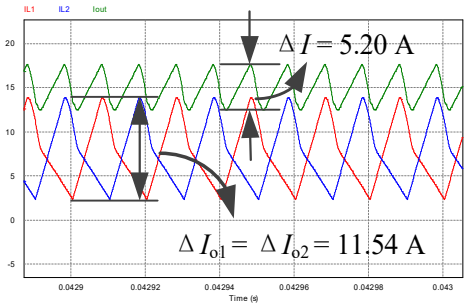
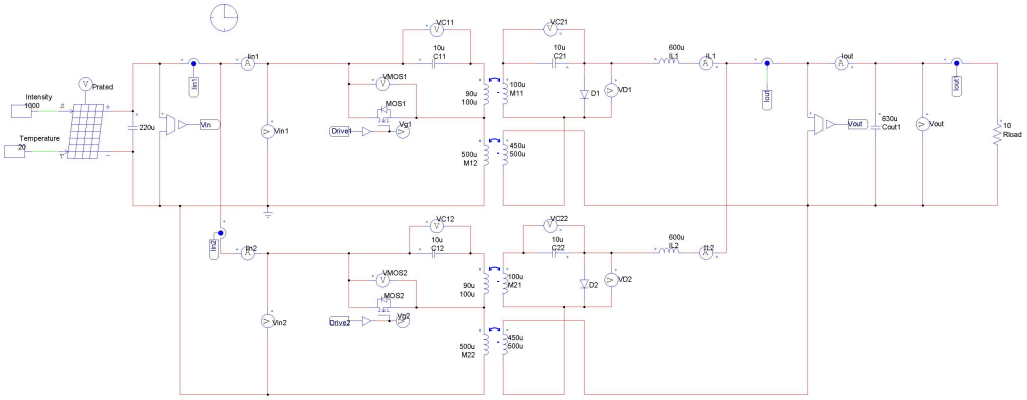


Fig. 3.51 Output current ripple, simulation

In Fig. 3.51, when the load current I_o = 15.0 A, the stage inductor current ripple ΔI_{o1} = ΔI_{o2} = 11.54 A, the total current ripple ΔI = 5.20 A, and the interleaving converter makes ΔI 45.06% of the ΔI_{o1} (or ΔI_{o2}), that is K = 0.451. The total current ripple normalization coefficient K is smaller than the theoretical value of 0.462 because switching loss and conduction losses are considered in the simulation, and the duty cycle is slightly greater than 0.35 after closed-loop control. When the duty cycle of a two-stage interleaved converter is less than 0.5, and the duty cycle increases, the normalization coefficient decreases. Therefore, allowing for practical imperfection, the simulation results validate the theoretical analysis.

Interleaving can also be used in PV applications, and the corresponding circuit simulation is modelled as in Fig. 3.52 (where the dc power supply is replaced by a PV panel).



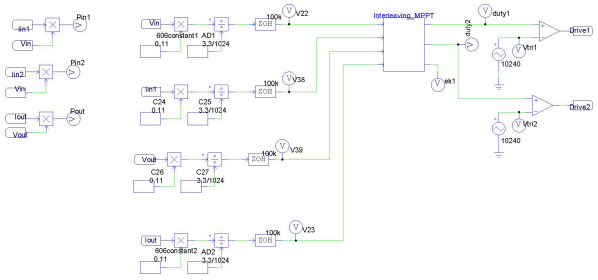


Fig. 3.52 Interleaved isolated D2 converter in PV application model in the PSIM

All the input voltage and current, output voltage and current are sampled during MPPT control. The waveforms in Fig. 3.53 validate the possibility of the isolated D2 converter in the PV application, with MPPT.

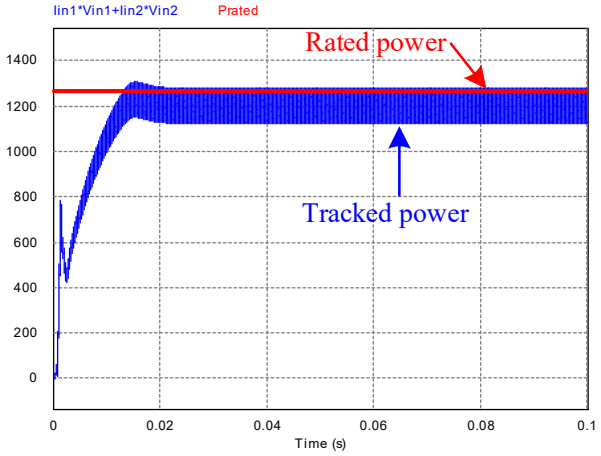


Fig. 3.53 Interleaved isolated D2 with PV panel rated and output power, simulation

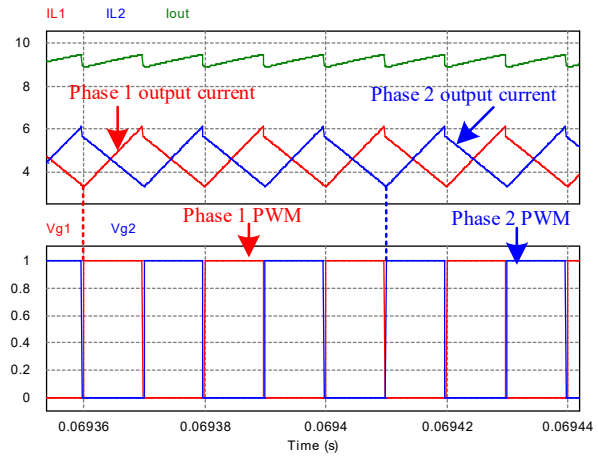
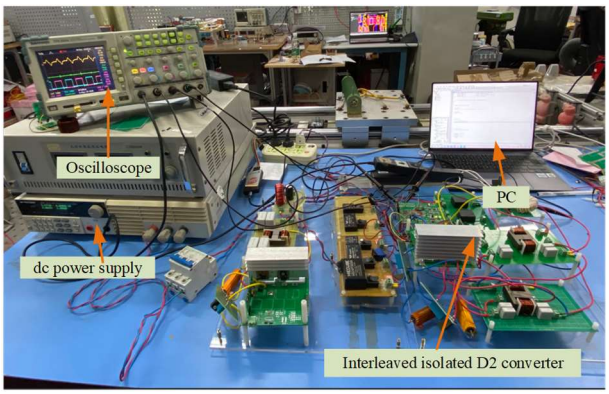


Fig. 3.54 Interleaved two stages current, load current and two stages PWM, simulation

In Fig. 3.54, the output current frequency is twice that of each stage inductor current

and the load current ripple is significantly reduced.

3.3.4 Interleaved Isolated D2 Experimentation



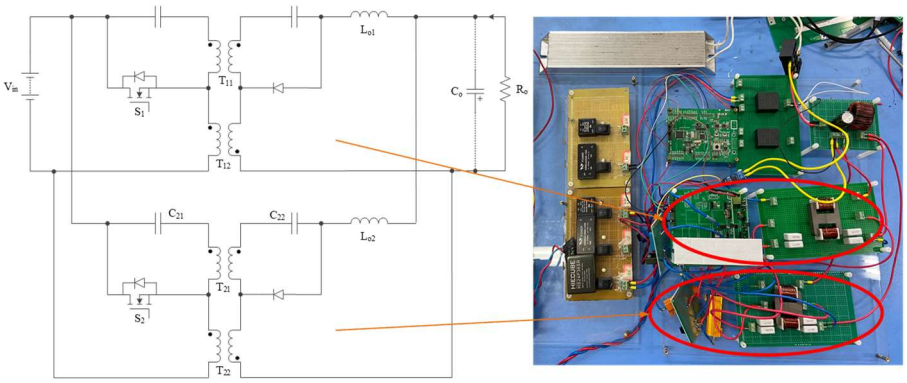
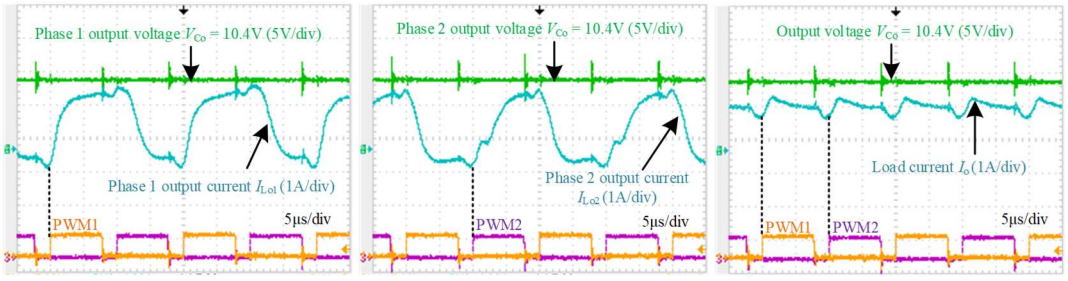


Fig. 3.55 Interleaved isolated D2 converter hardware platform

For this resistive load, interleaving application, the isolated D2 converter is a dc/dc converter to control the two-stage output voltage and two-stage inductor current and the hardware platform is shown in Fig. 3.55. It needs to be emphasized that in order to observe the stage inductor current and load current ripple, the output inductance is (undesirably) reduced to 100 μH.

The interleaving isolated D2 converter closed-loop experiment results are shown in Fig. 3.56, when the output voltage reference is set to 10 V.

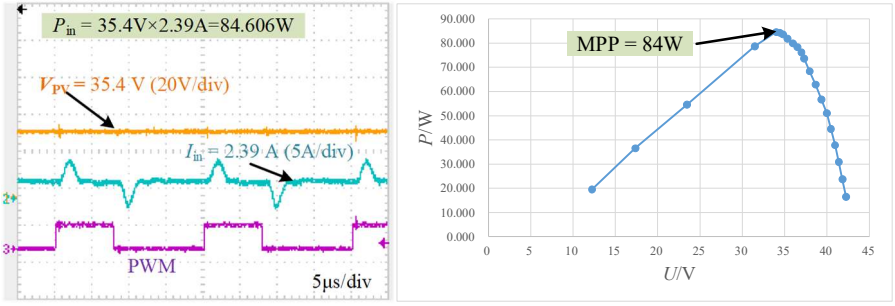


(a) Stage 1 inductor current (b) Stage 2 inductor current (c) Load current

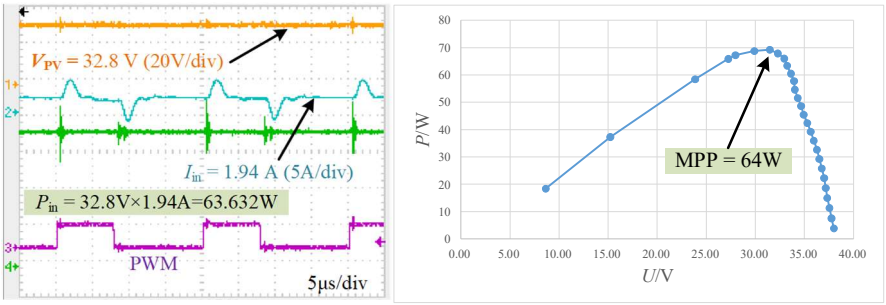
Fig. 3.56 Interleaved isolated D2 inductor and load current waveforms

From Fig. 3.56, when the load current I_o = 1.31 A, the stage inductor current ripple ΔI_{o1} = ΔI_{o2} = 2 A, the total current ripple ΔI = 0.6 A, then the interleaving converter produces ΔI 30% of the ΔI_{o1} (or ΔI_{o2}), that is K = 0.3. The total current ripple normalization coefficient K is smaller than the theoretical value of 0.462 because switching and conducting losses occur, and the duty cycle is slightly greater than 0.35 after closed-loop control. When the duty cycle of a two-stage interleaving converter is less than ½, the duty cycle increases, and the normalization coefficient decreases. Therefore, within acceptable error, the experimental results verify the theoretical analysis on interleaving isolated D2 converters.

The converter is also used in PV applications with MPPT control, where the dc power supply is replaced by a PV panel. Fig 3.57 shows MPPT tracking experimental results for the interleaving isolated D2 converter at different light intensities.



(a) MPP = 84W

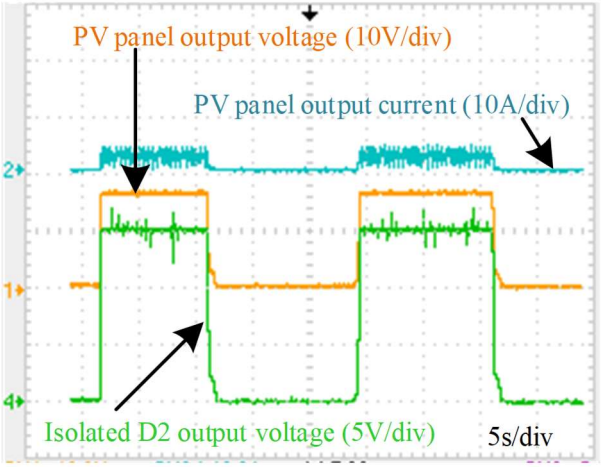


(b) MPP = 64W

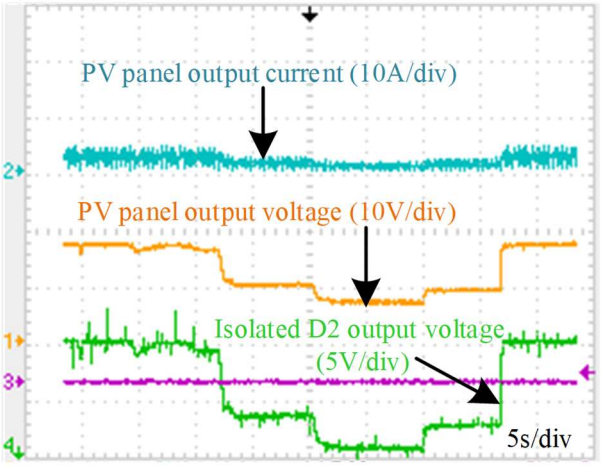
Fig. 3.57 The interleaved isolated D2 converter MPPT waveforms and maximum point

When the maximum power is 85 W, the tracking voltage is 35.4 V, and the current is 2.39 A, so the tracking power is 84.6 W, which nearly equals the maximum power of 85W. When the maximum power is 64 W, the tracking voltage is 32.8 V, and the current is 1.94 A, hence, the tracking power is 63.6 W, so the maximum power is tracked.

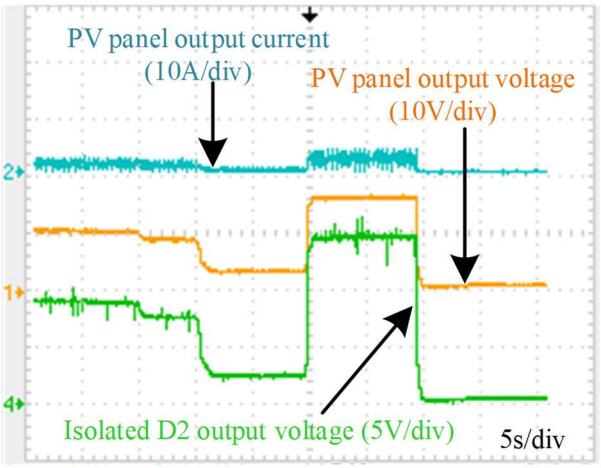
Thus, interleaved isolated D2 converters can realize MPPT, and results establish that the topology controls the input and output voltage and current and that the system has a good dynamic response. Three shading experiments are conducted, as shown in Fig. 3.58. The following waveforms can include most weather change conditions. So, shading experiments also establish the practicability of the isolated D2 topology.



(a) 0% shading → 100% shading → 0% shading → 100% shading



(b) 0% shading → 75% shading → 100% shading → 80% shading→ 0% shading



(c) 50% shading → 75% shading → 0% shading → 100% shading

Fig. 3.58 Shading experiments based on interleaved isolated D2 converter

3.4 Summary

This chapter proposes three dc/dc applications, namely PV, IPOS and interleaving. Principles, algorithms, simulation and experiments of these applications were presented. These three isolated topologies show that the isolated D2 converter can be flexibly cascaded with a wide transmission ratio, continuous input current, low input current ripple, reduced switch stress, output voltage ripple and so on. The applications featuring simple circuits, flexible derivation, easy control, high efficiency, and good dynamics are suitable for low-power applications.

CHAPTER 4 Isolated D2 in an ac to dc Application: PFC

Harmonics refers to the amount of electricity energy larger than the fundamental frequency after Fourier decomposition of periodic non-sinusoidal quantity in electric energy. Total harmonic distortion (THD) can be used to represent the harmonic magnitude and is defined as follows for the ac current and voltage:

$$THD_V = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \times 100\%$$
$$THD_I = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} \times 100\% \quad (4\text{-}1)$$

where V_1 and I_1 represent the fundamental root mean square (RMS) values of voltage and current, respectively, and V_n and I_n represent the nth harmonic RMS of voltage and current, respectively.

Harmonic suppression methods are mainly divided into passive suppression and active suppression. Passive suppression usually involves a passive filter, generally composed of a power capacitor, resistor and reactor according to the demand to provide a low-pass path for harmonics. Passive filters are a common way of reactive power compensation and harmonic suppression because of their simple structure, reliable operation and convenient maintenance. Active suppression uses the power electronic device structure and control strategy to reduce or even eliminate the harmonic so that the input voltage and current phase remain sinusoidal and in phase. This method is also called power factor correction, PFC.

4.1 PFC Principle

The purpose of power factor correction (PFC) technology is to suppress harmonic pollution in the power grid and improve power supply quality. In the power grid network, the distortion of the voltage waveform is usually small, but the distortion of the current waveform causes losses and a non-ideal (non-unity) power factor, PF.

Assuming that the grid voltage is not distorted, PF is defined as:

$$PF = \frac{I_1}{I}\cos\theta_1 = v\cos\theta_1 \tag{4-2}$$

where θ represents the included angle between the fundamental voltage and current, cosθ is the fundamental power factor or displacement factor, and v is the fundamental wave factor expressed by:

$$v = \frac{I_1}{I} = \frac{I_1}{\sqrt{\sum_{n=2}^{\infty} I_n^2}} \tag{4-3}$$

From the simultaneous equations (4-1), (4-2) and (4-3), PF can also be expressed as:

$$\mathrm{PF} = \frac{1}{\sqrt{1+THD^2}}\cos\theta \tag{4-4}$$

The smaller the THD, the greater the power factor, and when the THD is less than 5%, the PF can be as high as 0.999.

PFC technology is divided into two types: active power factor correction (APFC) and passive power factor correction (PPFC).

4.1.1 Passive Power Factor Correction, PPFC

Passive PFC technology [161] realizes power factor correction by reactive power compensation through a passive network composed of inductors and capacitors. Thus, PPFC is a natural rectification technology because of its high efficiency without switching loss, large volume, and the effect of harmonic suppression is not obvious.

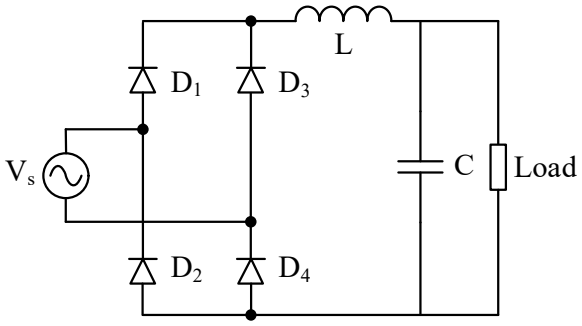
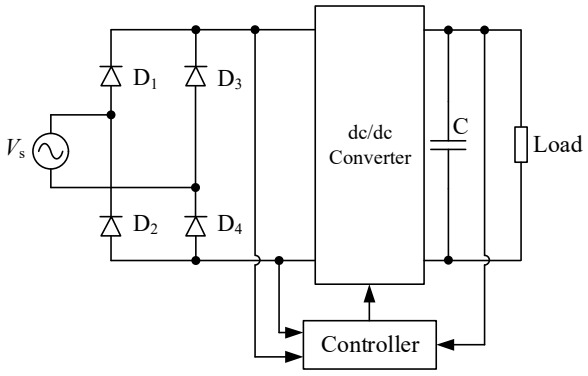


Fig. 4.1 Passive power factor correction circuit

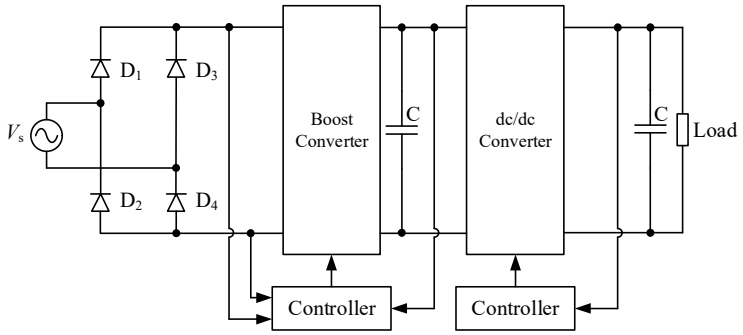
The corrected power factor is low, about 0.91, and the total harmonic content can only be reduced by about 70%, which may be insufficient to meet industrial requirements.

4.1.2 Active Power Factor Correction, APFC

Active PFC is a forced rectification technology [86], [92], [162], [163]. The input current is controlled by a switching process to follow the input voltage and realize power factor correction. The advantages of APFC are stable output voltage, high power factor (near unity) and small harmonic current, but with the disadvantages of complex control and high cost. There are two types of PFC, namely single-stage PFC and two-stage PFC.



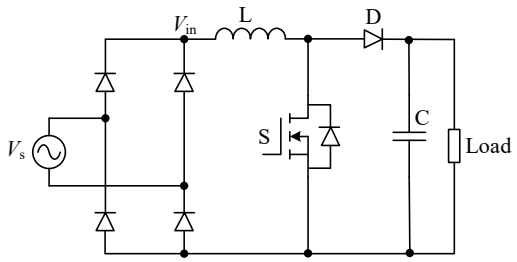
(a) Single-stage PFC



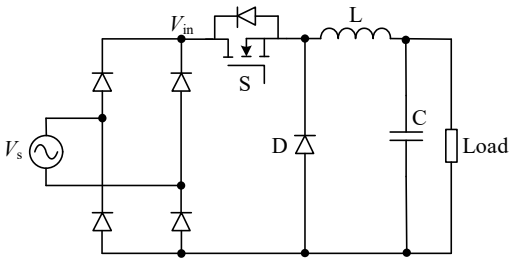
(b) Two-stage PFC

Fig. 4.2 Cascade structures of PFC circuit

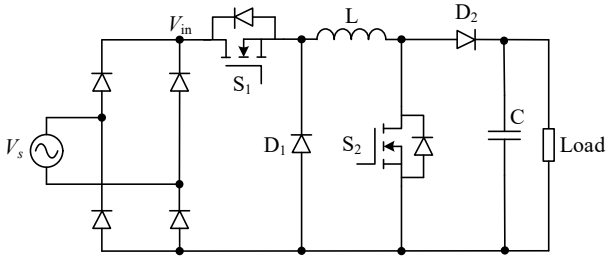
The basic converter topologies such as Boost, Buck, Buck-Boost and Ćuk, which can be used as the main PFC circuit, as shown in Fig. 4.3.



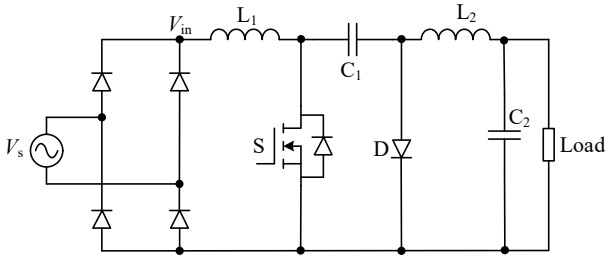
(a) Boost PFC



(b) Buck PFC



(c) Buck-Boost PFC



(d) Ćuk PFC

Fig. 4.3 Four PFC circuits based on Boost, Buck, Buck-Boost and Ćuk converters

The Boost PFC circuit in Fig. 4.3 (a) can boost voltage, so the PFC can work from a wide range of input voltage conditions. The input current is the inductor current, which is continuous and easy to adjust with input voltage change. However, when the Boost circuit works in a DCM mode, the stress of the front-stage EMI filter will be increased. When the voltage crosses zero, the current waveform will be distorted, and the power factor will be affected. The circuit does not offer isolation.

The Buck PFC circuit shown in Fig. 4.3 (b) can step down voltage and reduce the voltage transmission ratio for the later stage. The open circuit protection function can be realized by controlling the switch. The switch voltage stress is the maximum value of the output voltage, which is less than the switch voltage stress of the Boost circuit.

The Buck PFC noise ripple is large, which increases the difficulty of filter design, so in practical applications, Buck PFC is rarely used. The circuit does not offer isolation.

The Buck-Boost PFC circuit is shown in Fig. 4.3 (c), and the input current characteristics are similar to those of the Buck PFC circuit. The switch S_1 will turn off near the zero crossing point of the input voltage, and the power cannot be transmitted to the load, resulting in large harmonics. Also the polarity of the output voltage is opposite to the input voltage. There are two switches in the Buck-Boost PFC circuit, which makes the design of the drive and control circuit more difficult. The circuit does not offer isolation.

The Ćuk PFC circuit is shown in Fig. 4.3 (d) where the circuit structure is complex, the output current ripple can be large, and the reliability is low. So, the Ćuk PFC circuit is used in a few applications. However, the Ćuk can step up and step down the output voltage, and with the input inductor, the input current is continuous and easy to adjust. Also, there is only one switch, simplifying the drive circuits and control strategy. The circuit can offer isolation.

4.2 Different PFC Topologies

There are three PFC schemes:

- the common topology, the ac power is rectified to dc power by a diode bridge, and the isolated D2 is used to complete PFC;
- two isolated D2 converters without a diode bridge; and
- two isolated D2 and a diode bridge, but interleaving is used.

4.2.1 One Isolated D2

Only one isolated D2 is used in PFC to verify the feasibility, with the topology shown in Fig. 4.4. It improves the power factor by controlling the input current waveform to be more sinusoidal and near in phase with the input voltage V_s waveform.

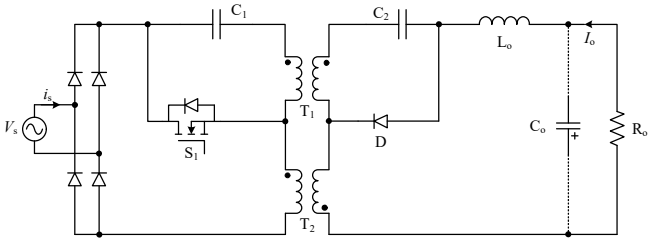


Fig. 4.4 One isolated D2 converter used in PFC

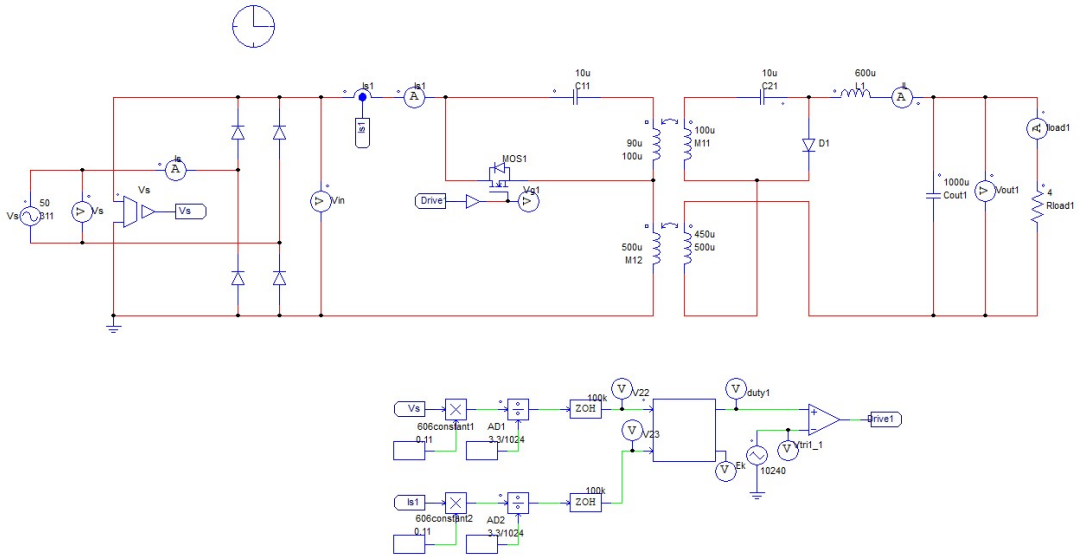


Fig. 4.5 One isolated D2 converter PFC in the PSIM

The input ac voltage is a reference, and the input current is the controlled variable. So the PSIM simulation model, where the input voltage and the rectified current phase are compared in the C block. When the phase difference becomes larger, the duty cycle of the switch is controlled to become smaller, and vice versa. The grid frequency is 50 Hz, and the rated voltage is 220 V ac, giving a peak voltage of 220× √ 2=311 V. The grid voltage and current are shown in Fig. 4.5, where the grid voltage and current are in phase under control.

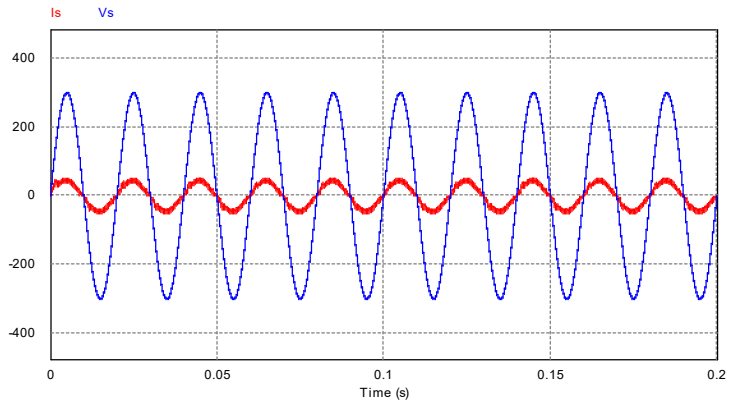
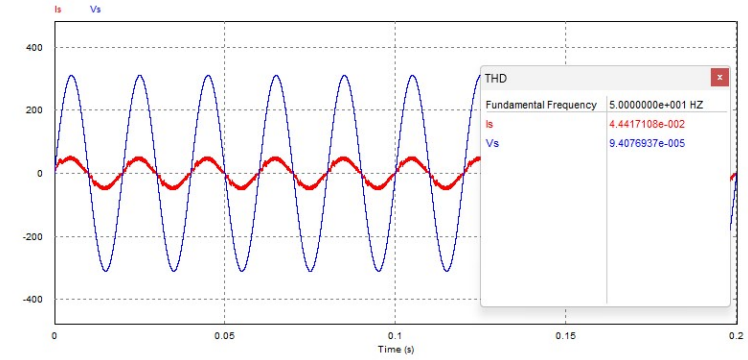
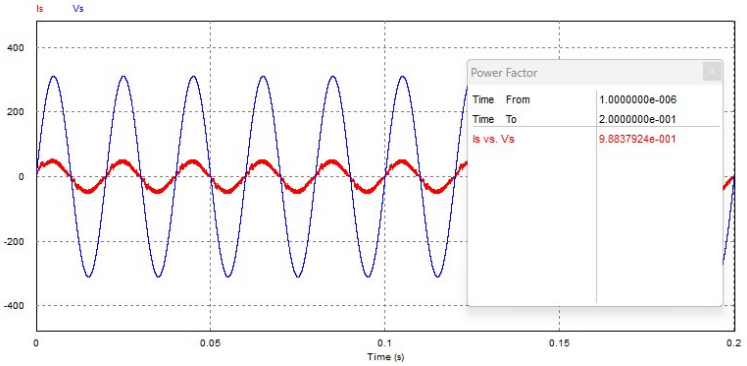


Fig. 4.6 One isolated D2 converter PFC grid ac voltage and current

Two indicators, THD and PF, are calculated and analyzed to demonstrate PFC converter performance. The current THD is 4.441% < 5%, which meets the grid connection requirement of less than 5% for distributed resources. The power factor is 0.988 > 0.95, sufficiently close to 1.



(a) THD



(b) PF

Fig. 4.7 THD and PF of One isolated D2 converter PFC grid voltage and current

The hardware platform is 60 V, 250 W, with the corresponding simulation is shown in Fig.4.8.

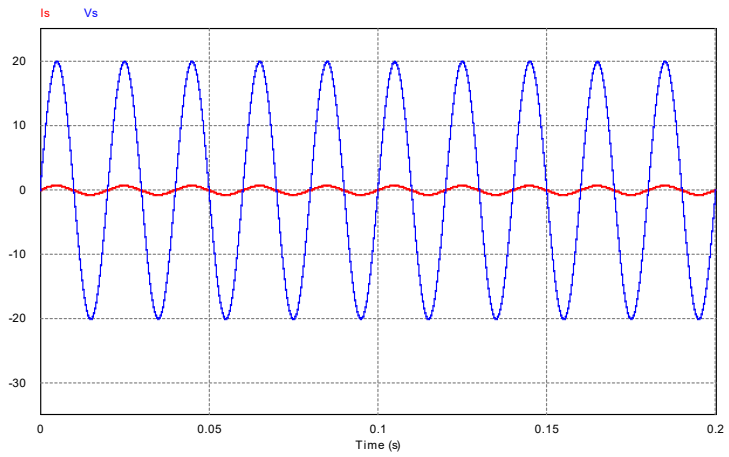
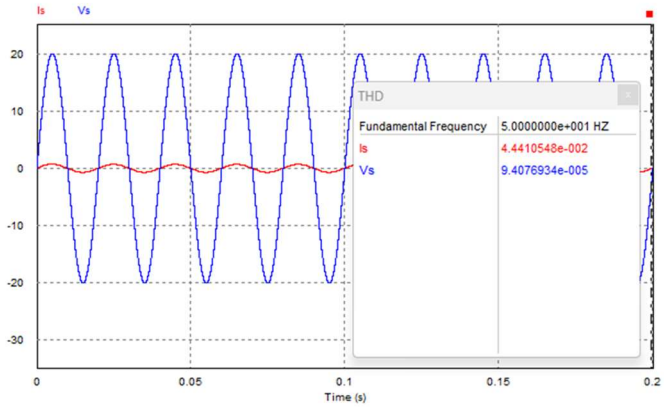
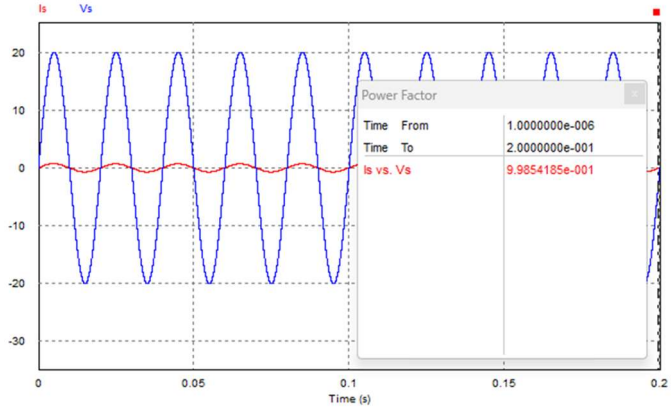


Fig. 4.8 One isolated D2 converter PFC voltage and current (Low power)



(a) THD



(b) PF

Fig. 4.9 THD and PF of One isolated D2 converter PFC voltage and current (Low power)

The current THD is 4.44% < 5%, which meets a grid connection requirement of less than 5% for distributed resources. The power factor is 0.985 > 0.95, close to 1. So, the isolated D2 converter is a suitable choice for PFC.

4.2.2 Bridgeless Isolated D2

i Operational Processes

The bridgeless Buck and Boost PFC converters have a limited voltage conversion ratio (ratio between output and input voltages), i.e., < 1 for the Buck and > 1 for the Boost converters. Isolation of both is problematic. Therefore, these converters cannot be used for a wider range of dc link voltage control. A ***bridgeless*** Buck-Boost converter does not provide high-frequency isolation.

A bridgeless configuration of an isolated D2 converter is derived for the partial or complete elimination of the front-end diode bridge rectifier (DBR), where Fig. 4.10

shows the proposed PFC bridgeless dual isolated D2 converter. It improves the power factor by controlling the input current waveforms to be more sinusoidal and near in phase with the input voltage V_s waveform.

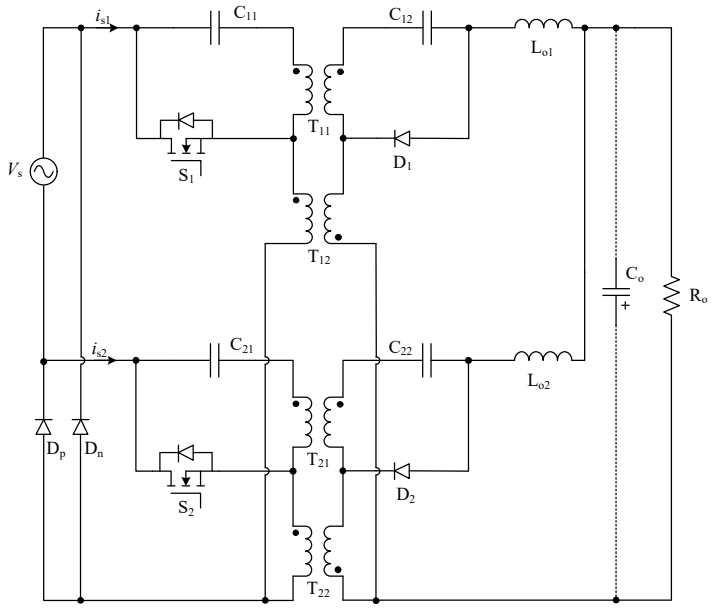
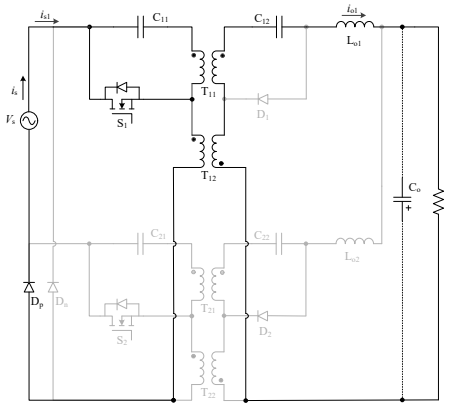
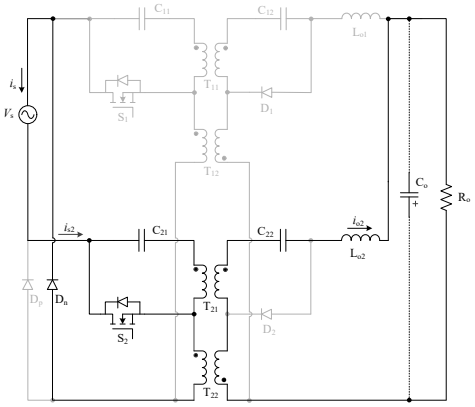


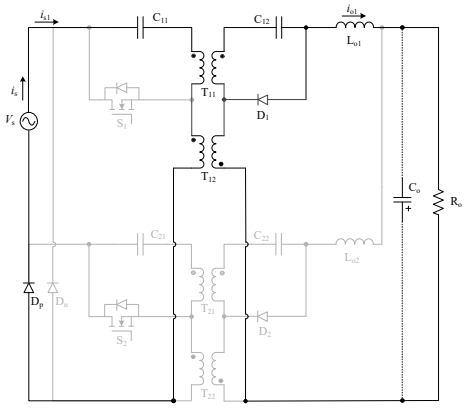
Fig. 4.10 PFC Bridgeless isolated D2 converter used in PFC



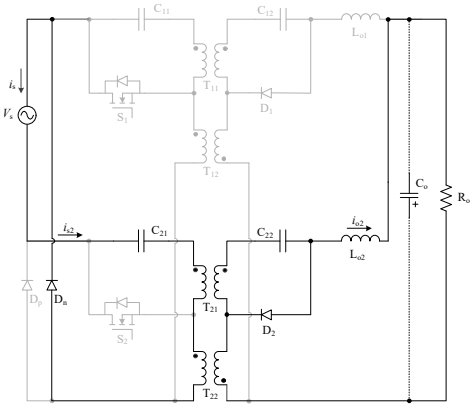
(a) positive half cycle (switch ON)



(c) negative half cycle (switch ON)



(b) positive half cycle (switch OFF)



(d) negative half cycle (switch OFF)

Fig. 4.11 Different modes of operation of bridgeless dual isolated D2 converter

Fig. 4.11 (a) and (b) show two modes of operation of a bridgeless isolated D2 converter in a switching period for the positive half cycle of the supply voltage, and (c) and (d) show two modes of operation in a switching period for the negative half cycle of the supply voltage.

Mode (a): When the switch S_1 is turned **ON**, the input inductor T_{12}, output inductor L_{o1}, and magnetizing inductance of HFT T_{11} start energizing, as shown in Fig. 4.11a. The input side intermediate capacitor C_{11} supplies the energy to the HFT, and the output side intermediate capacitor C_{12} supplies the required energy to the dc link capacitor C_o.

Mode (b): When the switch S_1 is turned **OFF**, the input inductor T_{12}, output inductor L_{o1}, and magnetizing inductance of HFT T_{11} start de-energizing as shown in Fig. 4.11b. The intermediate capacitors C_{11} and C_{12} charge, and the dc link capacitor C_o discharges. Operation for the negative half cycle of the supply voltage is similar.

Initially, the intermediate capacitors C_{11}, C_{12}, C_{21}, and C_{22} are completely discharged and are charged during the operation of the PFC converter. The voltage across the input side intermediate capacitors C_{11} and C_{21} depends upon the instantaneous input voltage; hence, the initial charging of C_{11} and C_{21} is zero. However, the output side intermediate capacitors C_{12} and C_{22} are not completely discharged in a switching period or a half line cycle of the supply voltage due to the voltage maintained at the dc link capacitor C_d.

During the operation of the PFC converter in the positive half cycle, the energy storage components on the primary side of the HFT, the primary of T_{11} and T_{12}, and C_{21}, remain in a non-conducting state and are completely discharged.

ii Simulation

The input voltage is the reference, and the two input currents are the controlled variables. According to the above analysis and operation modes, the PSIM simulation model is shown in Fig. 4.12.

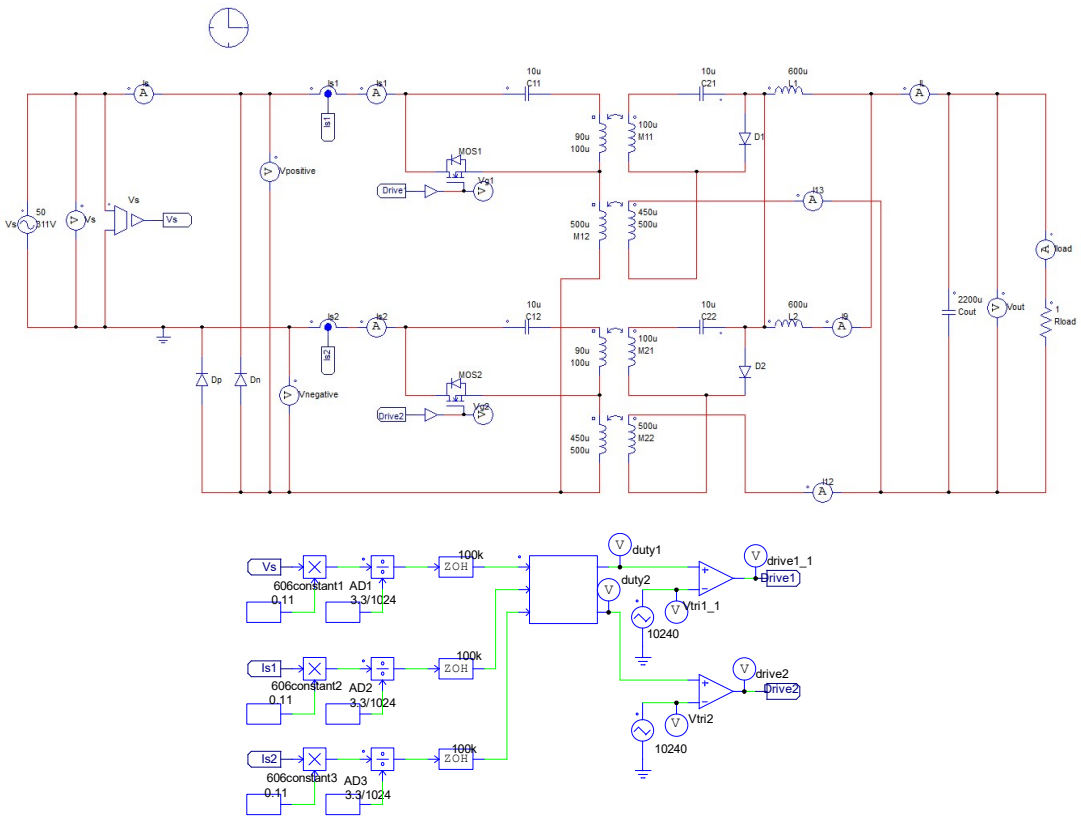


Fig. 4.12 PFC Bridgeless isolated D2 converter in the PSIM

In the simulation, i_{s1}, i_{s2} and input voltage are sampled, the phase and magnitude of these variables are controlled in a PSIM C block PSIM. The grid voltage and current waveforms are shown in Fig. 4.13, where the grid voltage and current are in phase, under the control.

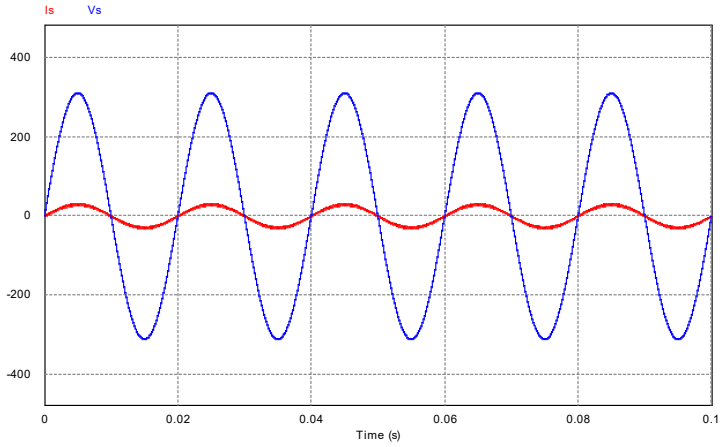
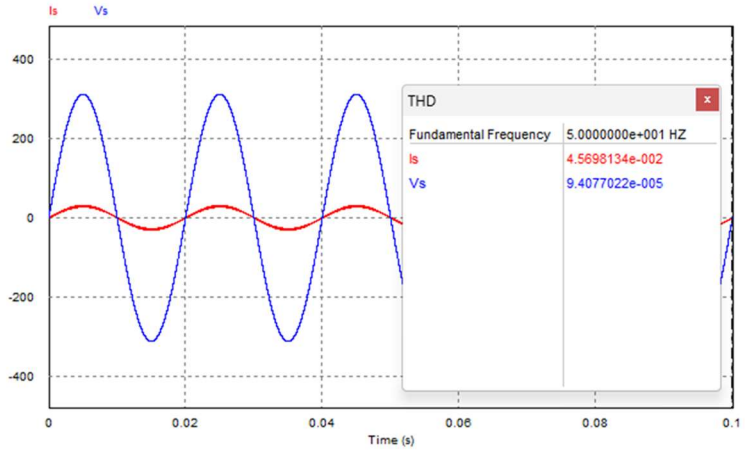


Fig. 4.13 PFC Bridgeless isolated D2 converter grid voltage and current



(a) THD

(b) PF

Fig. 4.14 THD and PF of PFC Bridgeless isolated D2 converter grid voltage and current

The current THD is 4.57% < 5%, which meets the generation requirements. The power factor of this situation is 0.99 > 0.95, close to 1. The low-power simulation is also presented, to correspond to the experimental results to be presented.

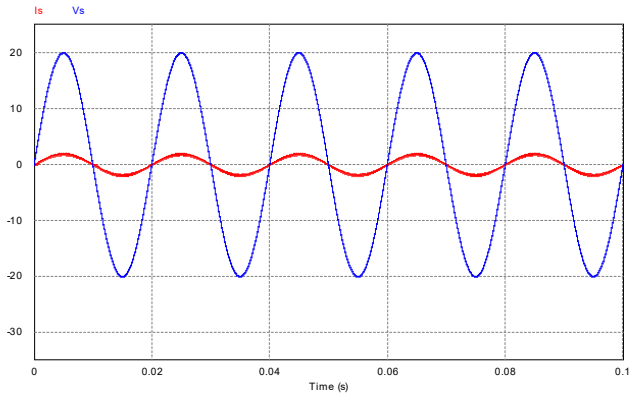
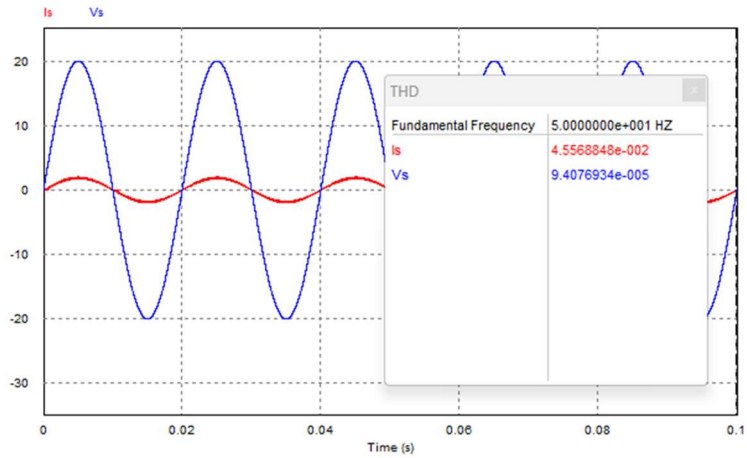
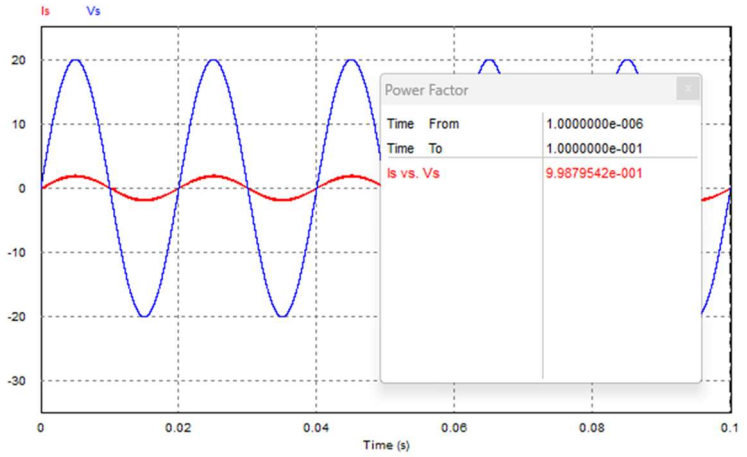


Fig. 4.15 PFC Bridgeless isolated D2 converter voltage and current (Low power)



(a) THD



(b) PF

Fig. 4.16 THD and PF of PFC Bridgeless isolated D2 converter voltage and current (Low power)

The current THD is 4.56% < 5%, and the power factor of this situation is 0.99 > 0.95. So, the PFC Bridgeless isolated D2 converter is suitable for PFC.

4.2.3 Interleaved Isolated D2

Interleaving has many advantages. It can reduce the current ripple volume of energy storage, reduce current stress through shunting, and increase converter heat dissipation capability.

Two interleaved isolated D2 IPOP converters are taken as an example to analyze the operation states under CCM. The equivalent resistance model of the two-phase interleaved technique is used to obtain the current balancing conditions.

i Operational Processes

The main difference between each phase control in an interleaving parallel converter is

that the phase is different. The working process of the two interleaving parallel isolated D2 converters under CCM is analyzed. The two-phase interleaving parallel isolated D2 converter topology is shown in Fig. 4.17. Interleaved isolated D2 PFC improves the power factor by controlling the input current waveform to be more sinusoidal and near in phase with the input voltage V_s waveform.

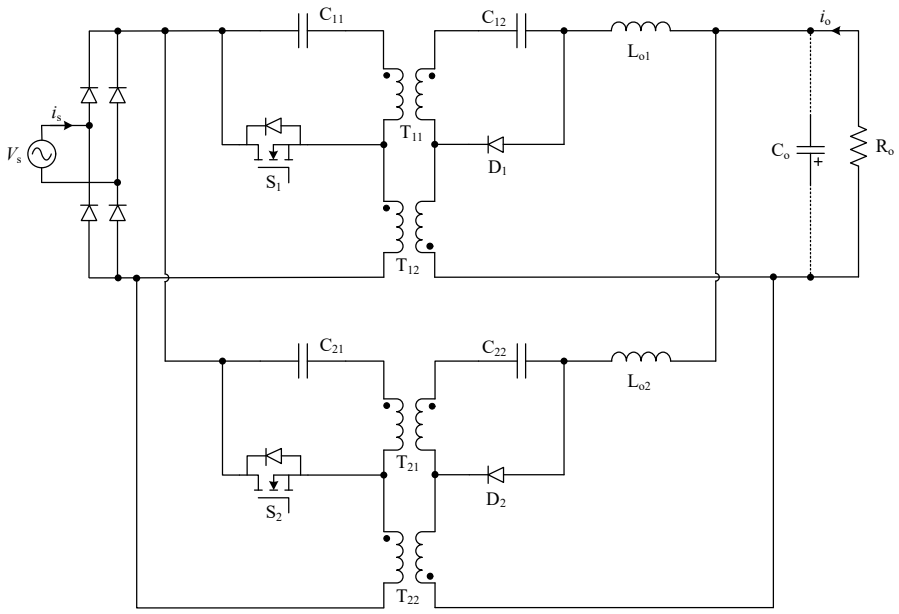
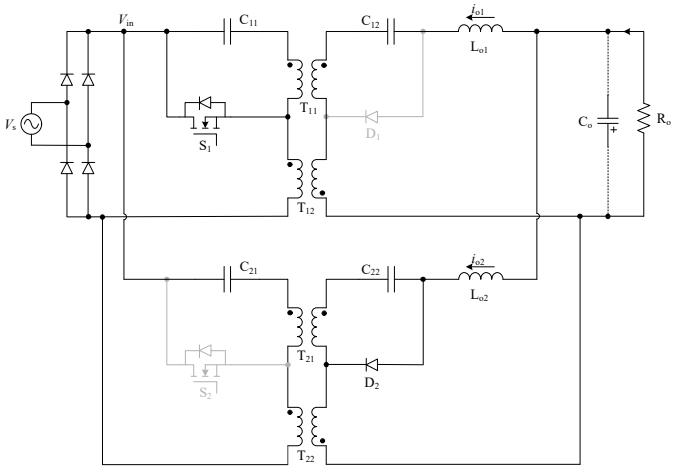
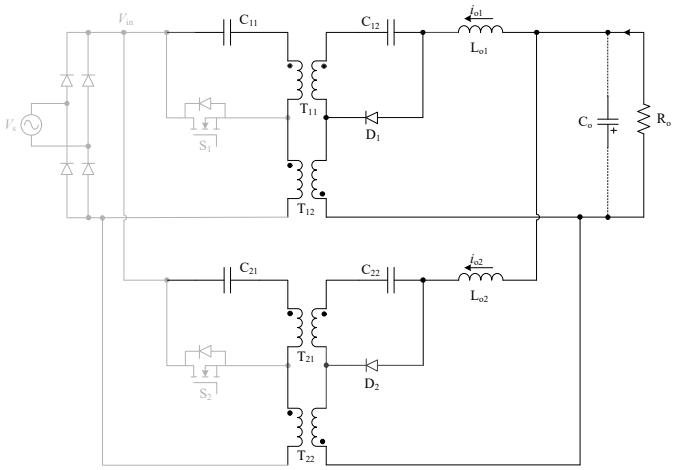


Fig. 4.17 Topology of two-phase isolated D2 converter

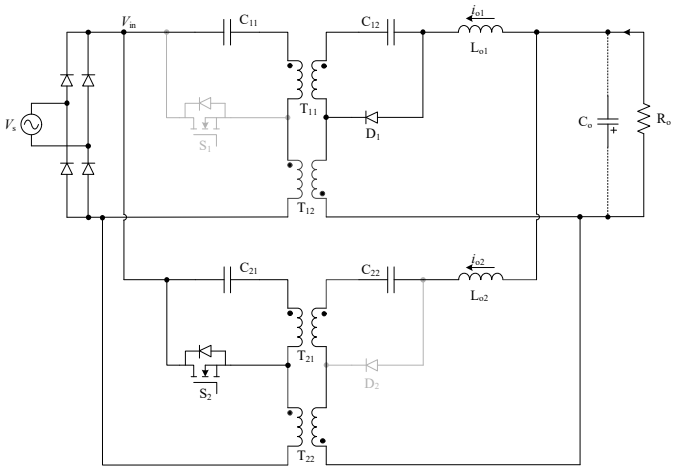
In the interleaving trigger control mode, two sets of switches are interlaced conducted by 180 °, and there are three working modes when duty cycle $\delta \leq ½$, as shown in Fig. 4.18. The two switches, S_1 and S_2, cannot conduct simultaneously.



(a) state 1



(b) state 2



(c) state 3

Fig. 4.18 Working states of two-phase interleaved isolated D2 converter

It is assumed all circuit components of the two D2 converters are identical and the circuit operates in CCM.

State 1: Switch S_1 is turned **ON** and switch S_2 is turned **OFF**, power supply V_{in} energizes inductor L_{o1}, inductor current i_{o1} rises; inductor L_{o2} discharges load through flywheel diode D_2, inductor current i_{o2} decreases; circuit state satisfies:

$$\begin{cases} L\dfrac{\mathrm{d}i_{\mathrm{o}1}}{\mathrm{d}t}=V_{\mathrm{in}} \\ L\dfrac{\mathrm{d}i_{\mathrm{o}2}}{\mathrm{d}t}-V_{\mathrm{C}_{11}+\mathrm{C}_{12}}=-V_{\mathrm{o}} \\ L\dfrac{\mathrm{d}\left(i_{\mathrm{o}1}+i_{\mathrm{o}2}\right)}{\mathrm{d}t}=V_{\mathrm{in}}-V_{\mathrm{o}}+V_{\mathrm{C}_{11}+\mathrm{C}_{12}} \\ C\dfrac{\mathrm{d}u_{\mathrm{c}}}{\mathrm{d}t}=\left(i_{\mathrm{o}1}+i_{\mathrm{o}2}\right)-\dfrac{V_{\mathrm{o}}}{R} \end{cases} \tag{4-5}$$

State 2: Switch S_1 and S_3 are turned **OFF**, inductor L_{o1} and L_{o2} are energized through diode D_1 and D_2 respectively, capacitor C_o is charged, inductor current i_{L1} and i_{L2} decrease; the circuit state is:

$$\begin{cases} L\dfrac{\mathrm{d}i_{\mathrm{o}1}}{\mathrm{d}t}=-V_{\mathrm{o}} \\ L\dfrac{\mathrm{d}i_{\mathrm{o}2}}{\mathrm{d}t}=-V_{\mathrm{o}} \\ L\dfrac{\mathrm{d}\left(i_{\mathrm{o}1}+i_{\mathrm{o}2}\right)}{\mathrm{d}t}=-2V_{\mathrm{o}} \\ C\dfrac{\mathrm{d}u_{\mathrm{c}}}{\mathrm{d}t}=\left(i_{\mathrm{o}1}+i_{\mathrm{o}2}\right)-\dfrac{V_{\mathrm{o}}}{R} \end{cases} \tag{4-6}$$

State 3: Switch S_1 is turned **OFF**, S_3 is turned **ON**, inductor L_{o1} charges capacitor C_o through flywheel diode D_1, inductor current i_{o1} decreases; power supply V_{in} energizes inductor i_{o2}, inductor current i_{o2} rises; the circuit state satisfies:

$$\begin{cases} L\dfrac{\mathrm{d}i_{\mathrm{o}1}}{\mathrm{d}t}=V_{\mathrm{in}} \\ L\dfrac{\mathrm{d}i_{\mathrm{o}2}}{\mathrm{d}t}+V_{\mathrm{C}_{21}+\mathrm{C}_{22}}=V_{\mathrm{o}} \\ L\dfrac{\mathrm{d}\left(i_{\mathrm{o}1}+i_{\mathrm{o}2}\right)}{\mathrm{d}t}=V_{\mathrm{in}}+V_{\mathrm{o}}-V_{\mathrm{C}_{21}+\mathrm{C}_{22}} \\ C\dfrac{\mathrm{d}u_{\mathrm{c}}}{\mathrm{d}t}=\left(i_{\mathrm{o}1}+i_{\mathrm{o}2}\right)-\dfrac{V_{\mathrm{o}}}{R} \end{cases} \tag{4-7}$$

The inductor current ripple ΔI_{o1}, ΔI_{o2} of each phase and the total current ripple ΔI and voltage gain A_V satisfy:

$$\begin{cases} \Delta I_{o1} = \Delta I_{o2} = \dfrac{\left[2\delta V_{in} + (1-\delta)V_o\right]\delta T_s}{(1-\delta)L} \\ \Delta I = \dfrac{\left[2\delta V_{in} + (1-\delta)V_o\right]\delta T_s}{(1-2\delta)L} \\ A_V = \dfrac{V_o}{V_{in}} = -\dfrac{\delta}{1-\delta} \end{cases} \tag{4-8}$$

The dependent variables in (4-8) are the input voltage V_{in} and the output voltage V_o. In (4-4), the current ripple is obtained from dependent variables parallel stage number n and the duty cycle δ. Calculations show that the same ripple normalization coefficients result, that is, ripple results are consistent.

ii Simulation

The input voltage is a reference, and two D2 input currents are the controlled variables. The PSIM simulation model in Fig. 4.19 fulfills the presented analysis and operation modes.

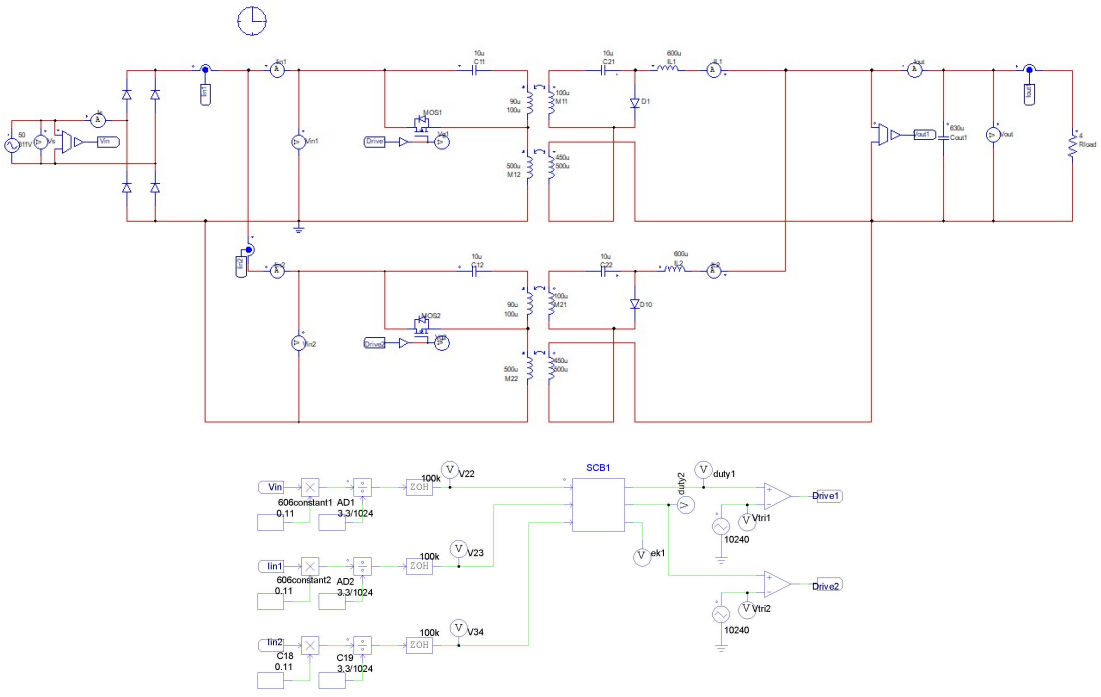


Fig. 4.19 PFC Interleaved isolated D2 converter in the PSIM

In the simulation, i_{s1}, i_{s2} and input voltage are sampled, the phase and magnitude of these variables are controlled in a PSIM C block. The grid voltage and current waveforms are shown in Fig. 4.20.

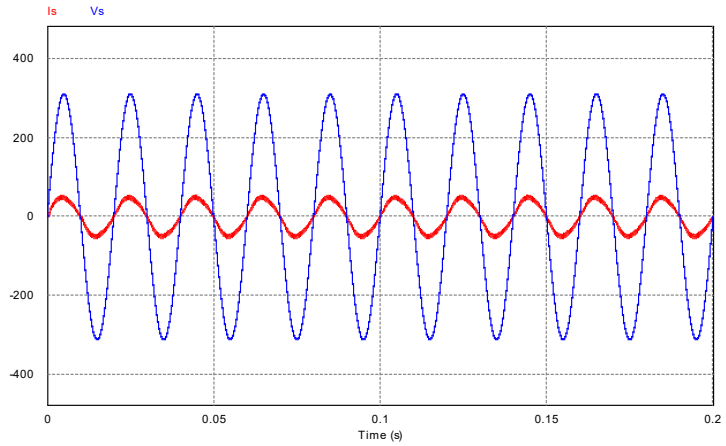
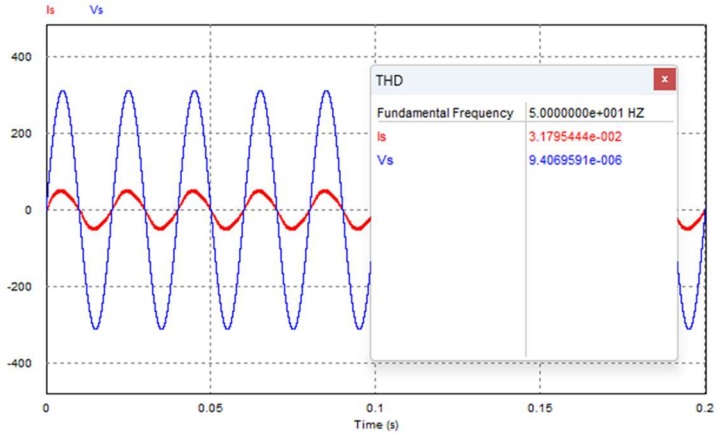
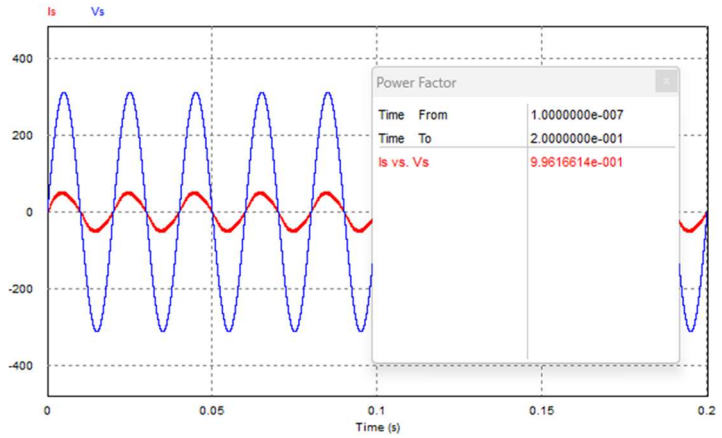


Fig. 4.20 PFC Interleaved isolated D2 converter grid voltage and current

During start-up, the current in the first period is unstable, and the current ripple is large. From the second period, the voltage and current of the grid are in phase and present sinusoidal waveforms that are under control.



(a) THD



(b) PF

Fig. 4.21 THD and PF of PFC Interleaved isolated D2 converter grid voltage and current

The current THD is 3.18% < 5%, and the power factor is 0.96 > 0.95. The low power simulation (results in Fig. 4.22) is also conducted to correspond to the experimental conditions to be presented.

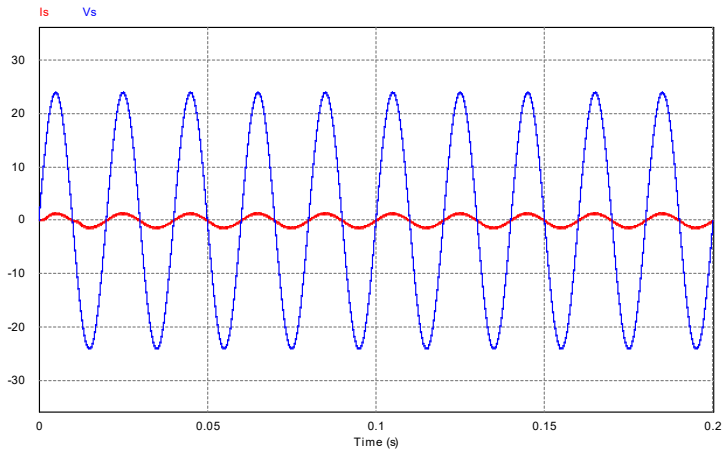
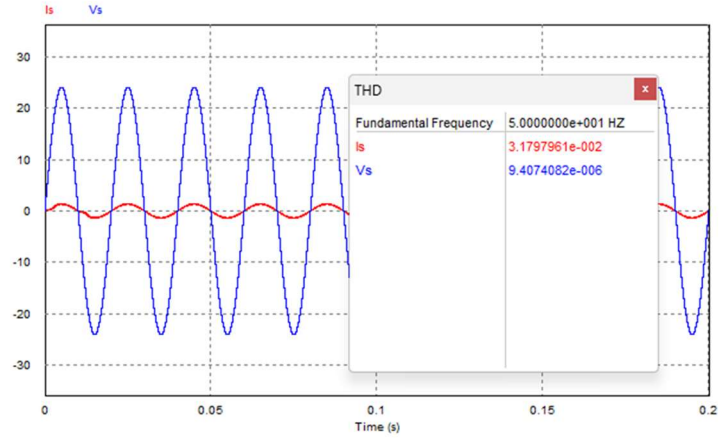
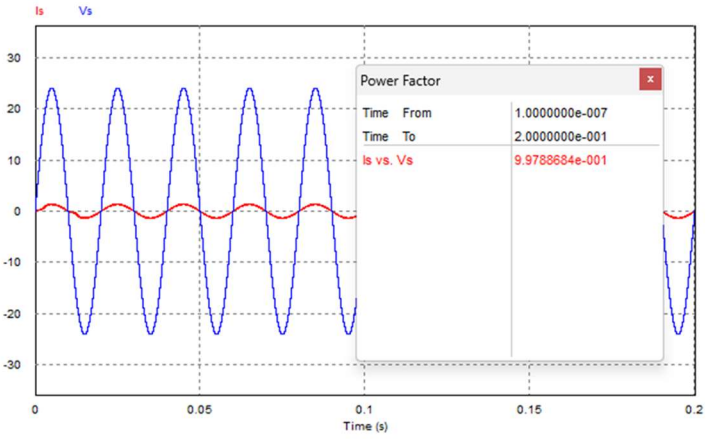


Fig. 4.22 PFC Interleaving isolated D2 converter voltage and current (Low power)



(a) THD



(b) PF

Fig. 4.23 THD and PF of PFC Interleaved isolated D2 converter voltage and current (Low power)

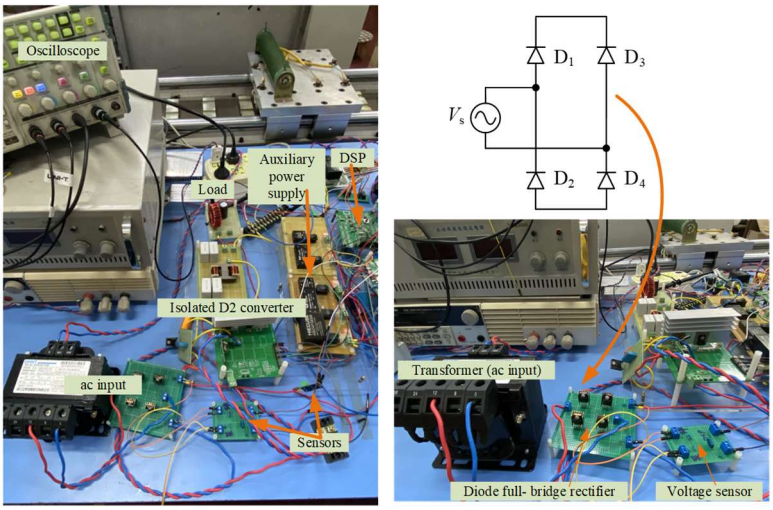
In Fig. 4.23, the current THD is 3.18% < 5%, and the power factor is 0.98 > 0.95. So, the PFC Interleaved isolated D2 converter is suitable for PFC.

4.3 Experimentation

The hardware platforms for three presented PFC topologies based on isolated D2 are shown in figures 4.24, 4.28, and 4.33. The input voltage and current waveform data are imported into MATLAB/Simulink to measure power factor and verify the theory and principles are correct and meet practical requirements.

4.3.1 One Isolated D2

PFC hardware platform with one isolated D2, with a resistive load, is shown in Fig. 4.24.



(a) Hardware platform (b) Input supply and Diode full-bridge

Fig. 4.24 Only one isolated D2 used in the PFC hardware platform

The dc voltage sensor used in the previous chapter experiments is replaced by an ac voltage sensor, where both the voltage sensor and current sensor sample the rectified voltage and current.

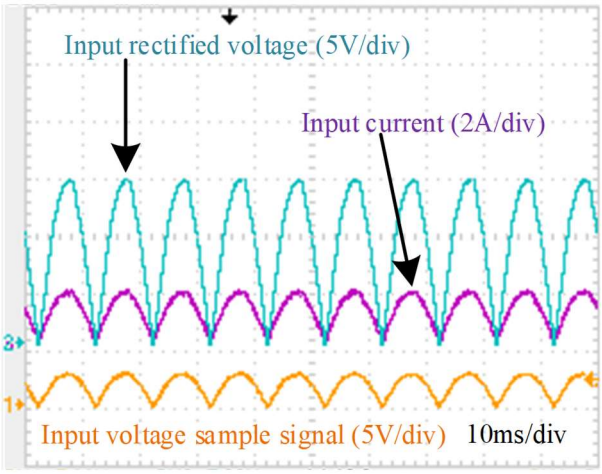


Fig. 4.25 ac voltage and its sample signal

Fig. 4.25 shows the isolated D2 PFC input rectified voltage (blue line) and current (purple line), and the yellow line is the input rectified voltage sample signal, which is between 0 and 3.3 V.

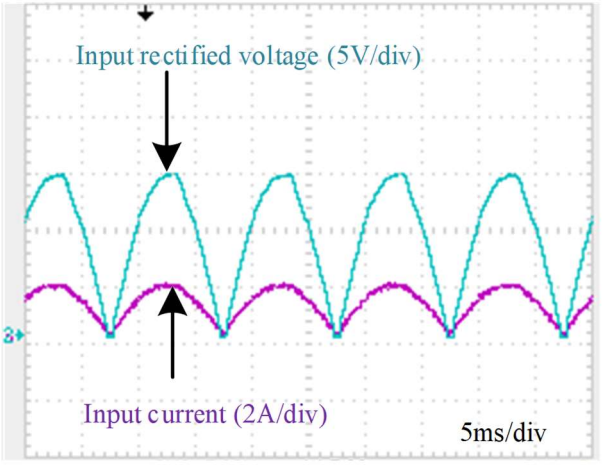
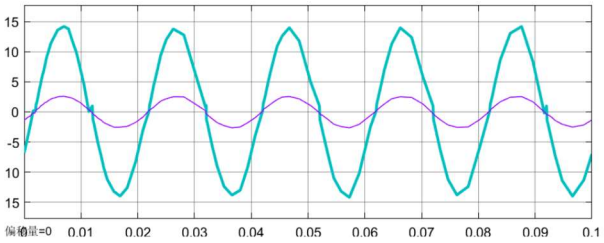
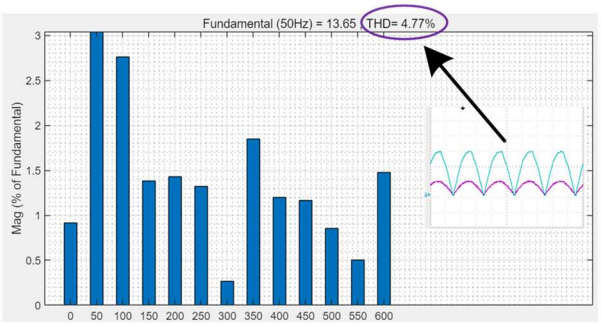


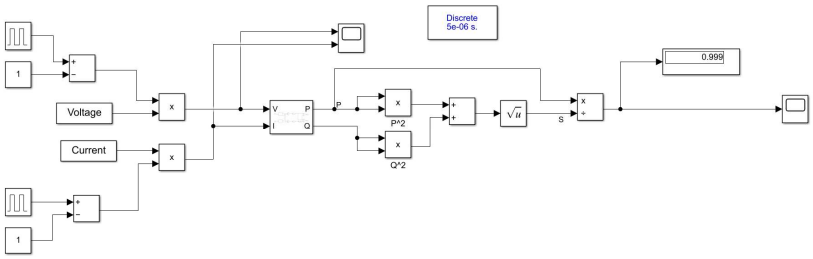
Fig. 4.26 One isolated D2 PFC ac input rectified voltage and current



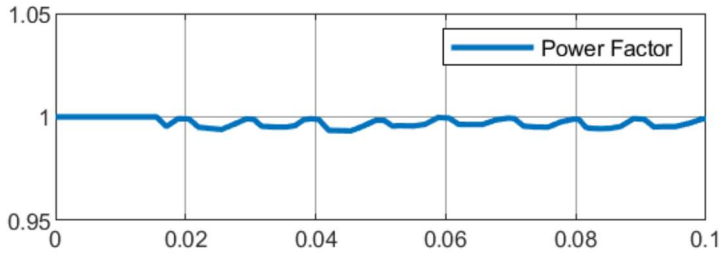
(a) Imported voltage and current waveforms on MATLAB/Simulink



(b) THD FFT on MATLAB/Simulink



(c) PF on MATLAB/Simulink



(d) PF transient waveform

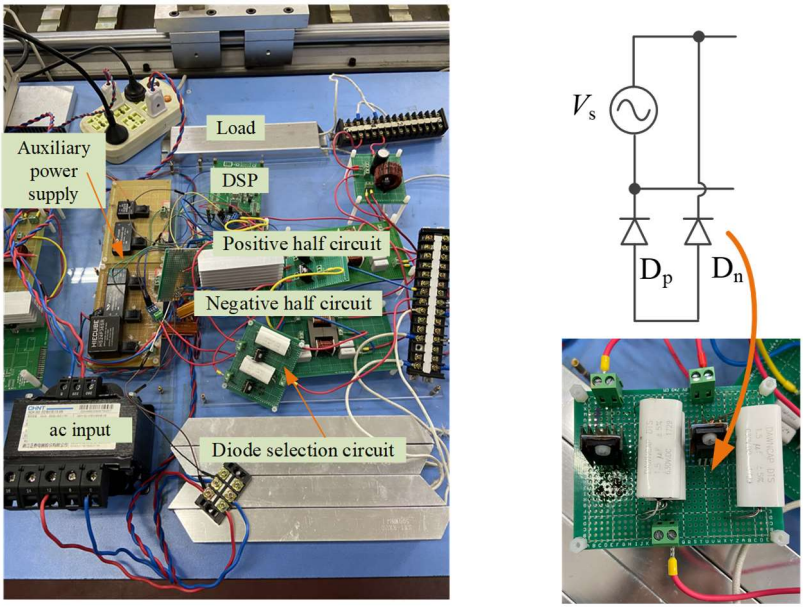
Fig. 4.27 THD and PF of One isolated D2 PFC

From Fig. 4.27, the voltage and current are in phase and under control. The current THD is 4.77%, and the power factor is 0.985. The input voltage and current in this PFC are both on the positive axis. The imported data are multiplied by -1 every other period, simulating the sine wave and then using the FFT tool to calculate THD (Fig. 4.27a and Fig. 4.27c).

The experimental results are distorted, but similar to, the simulation results. The isolated D2 converter is suitable for PFC being consistent with theoretical analysis and simulation verification.

4.3.2 Bridgeless Isolated D2

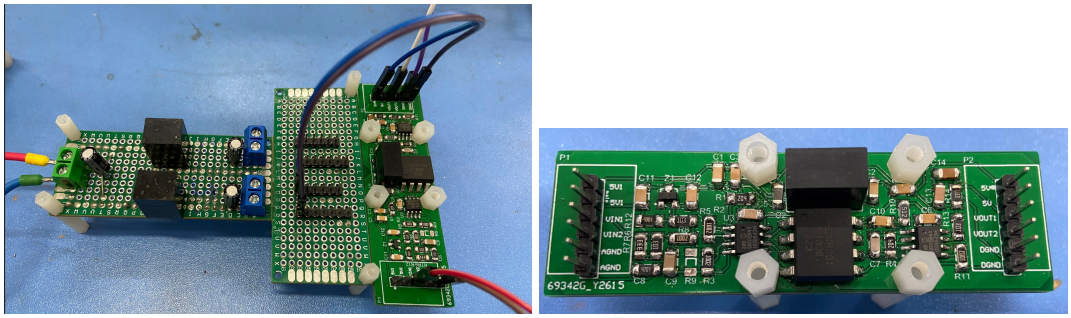
The hardware in Fig.4.28 is the PFC D2 converter circuit in Fig. 4.10.



(a) Hardware platform (b) Diode selection circuit

Fig. 4.28 PFC Bridgeless isolated D2 converter hardware platform

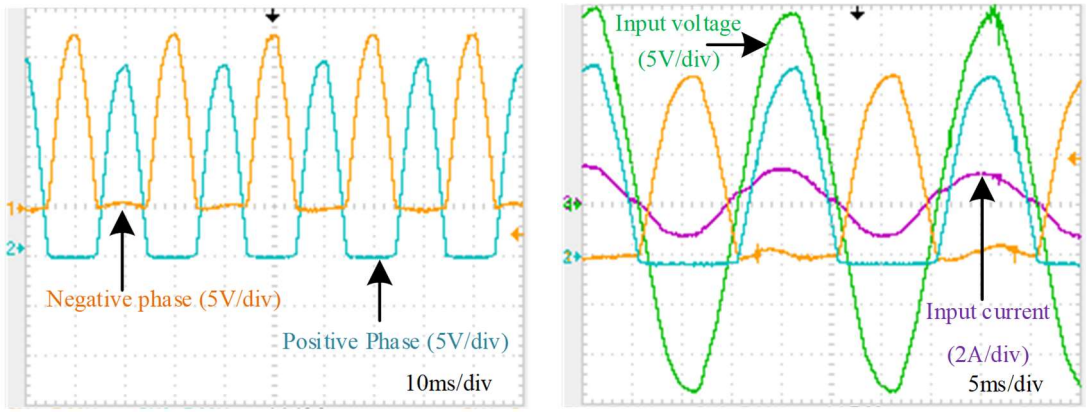
Different from one phase isolated D2 PFC, there are no diode full-bridge rectifier (no rectified voltage), so the ac voltage sensor is replaced by one which can sample negative voltage. The ac voltage sensor is isolated.



(a) ac voltage sensor circuit (b) ac voltage sensor PCB

Fig. 4.29 ac voltage sensor

The input side of PFC bridgeless isolated D2 is a diode select circuit which distinguishes between the 2 D2 input stages. So the output of the diode select circuit is shown in Fig. 4.30a. The yellow and blue lines are the two isolated input stages. In Fig. 4.30b, the green line is ac power input to the diode selection circuit. The purple line is input current, that is, one of PFC controlled variables.



(a) Diode select voltage (b) Input and output of diode selection

Fig. 4.30 Input and output voltage waveforms of diode select circuit

In Fig. 4.31, the input voltage and current are in phase and under control. Due to the input voltage being stepped down by an isolation transformer and the influence of the bridgeless D2 converter, the input voltage waveform oscillates.

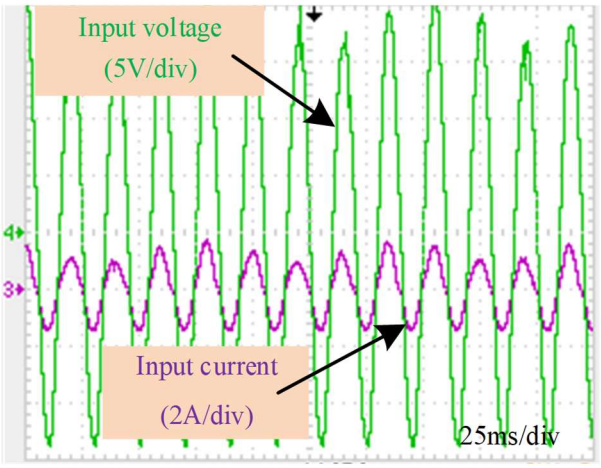
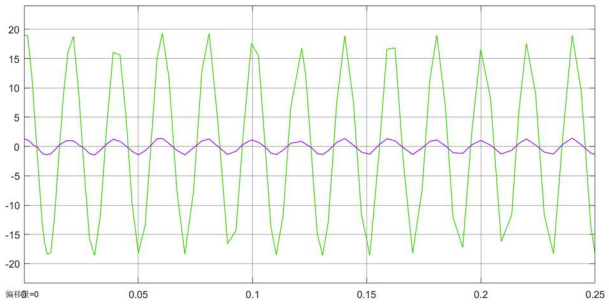
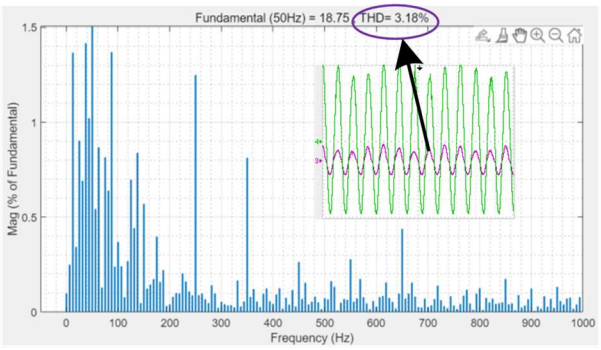


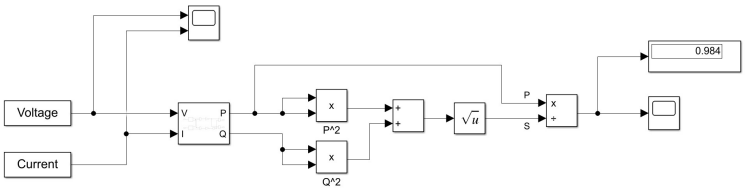
Fig. 4.31 Bridgeless isolated D2 PFC voltage and current



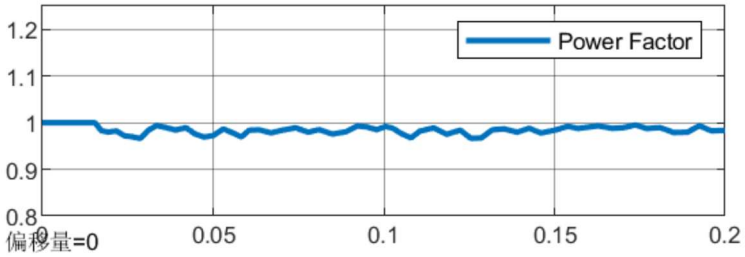
(a) Imported voltage and current waveforms on MATLAB/Simulink



(b) THD FFT on MATLAB/Simulink



(c) PF on MATLAB/Simulink



(d) PF transient waveform

Fig. 4.32 THD and PF of PFC bridgeless isolated D2

From Fig. 4.32, the current THD is 3.18%, and the power factor is 0.98, close to 1. So, the PFC bridgeless isolated D2 converter can be used for PFC. The experimental results are nearly consistent with the PFC bridgeless isolated D2 simulation results, so is a possible choice for PFC.

4.3.3 Interleaved Isolated D2

According to Fig. 4.13, the proposed PFC interleaved isolated D2 converter hardware is shown in Fig. 4.33.

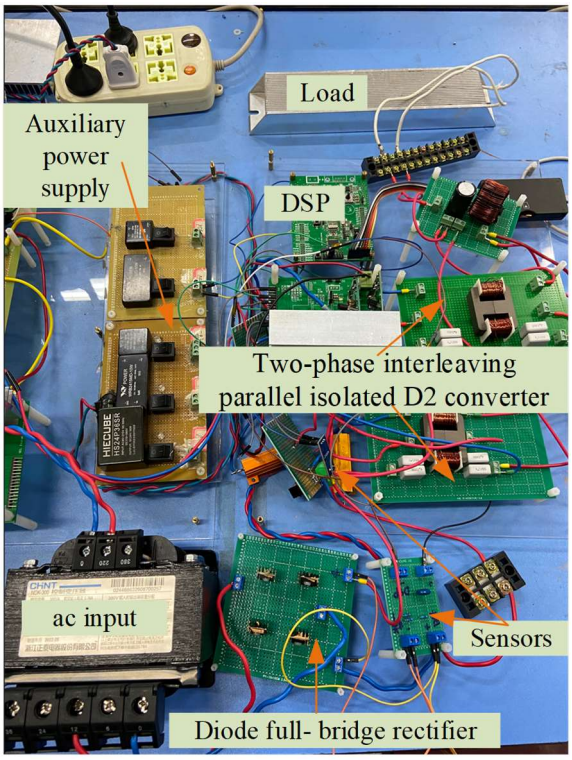


Fig. 4.33 PFC interleaved isolated D2 converter hardware platform

The input voltage is the reference, and two-phase input current are the controlled variables. In accordance with the analysis and operation modes, the ac voltage and current waveforms are shown in Fig. 4.34.

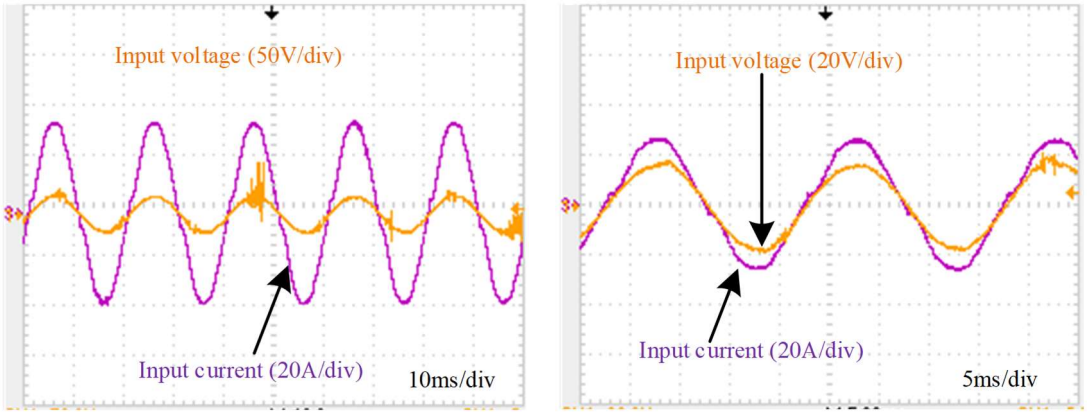


Fig. 4.34 Interleaved isolated D2 PFC voltage and current

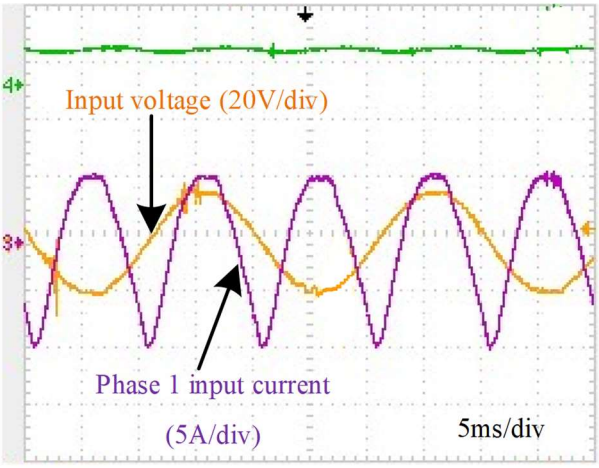
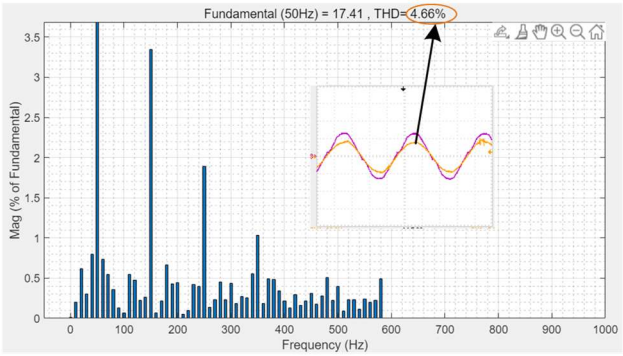
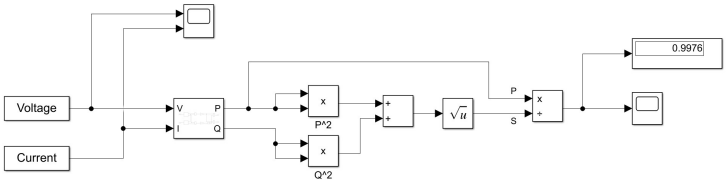


Fig. 4.35 Interleaved isolated D2 PFC voltage and phase current

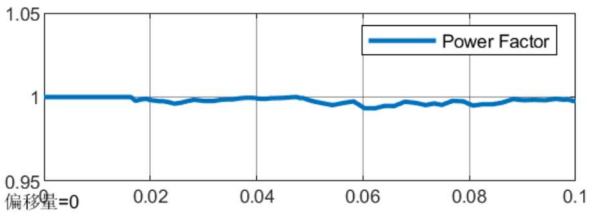
In Fig. 4.35, the yellow line is input voltage and the purple line is one phase input current. The current frequency is twice that of the voltage.



(a) THD FFT on MATLAB/Simulink



(b) PF on MATLAB/Simulink



(c) PF transient waveform

Fig. 4.36 THD and PF of PFC interleaved isolated D2

In Fig. 4.36, the PFC input voltage and current waveform data are imported into

MATLAB/Simulink, and the power factor is calculated: current THD is 4.66% < 5%, and the power factor is 0.998 > 0.95. So the PFC interleaving isolated D2 converter can be used for PFC.

4.4 Summary

This chapter analyzes passive PFC and active PFC, and three PFC topologies all fall into the category of active PFC. The isolated D2 PFC converters can reduce harmonics, step up and down the isolated output voltage. The input current is continuous and easy to adjust with only one switch.

The topologies, operational processes, simulation, hardware platform and experiments for One isolated D2, bridgeless isolated D2, and interleaved isolated D2 are presented in detail. From THD and power factor analysis of simulation results and experiments, the performance of interleaved isolated D2 is optimal.

CHAPTER 5 Single-Phase Inversion: Isolated D2 Inverter

Single-phase dc to ac inversion with electrical isolation is an active research area (for example, in domestic PV applications). The isolated D2 converter has electrical isolation characteristics and can be used for isolated dc to ac applications. As with dc/dc control, only one switch is controlled when based on an orthogonal system, which simplifies control. As with many dc to ac converters, reversible ac to dc conversion is an inherent feature. This chapter investigates the aspect of the D2 related to dc to ac conversion, with power reversibility.

5.1 Circuit Configuration and Modulation

5.1.1 Isolated D2 Inverter Circuit Design

Although the isolated D2 converter is fundamentally a dc/dc converter, the topology can be modified to realize dc/ac inversion (the reversible D2 is a D1 topology, simulated in Chapter 2). On the secondary side of the D2, the diode constrains the voltage and current direction. So, the diode is replaced by two switches to allow reverse voltage and current directions. When two switches are connected in reverse series, their rated voltage is superimposed, allowing them to withstand bidirectional voltages. The two switch output diode replacement is shown in Fig. 5.1, which uses MOSFETs, to exploit the inherent antiparallel diode.

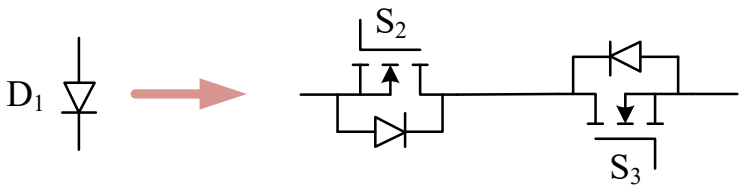


Fig. 5.1 The Diode controllable bidirectional replacement

Fig. 5.2 shows the configuration of the proposed isolated D2 inverter circuit.

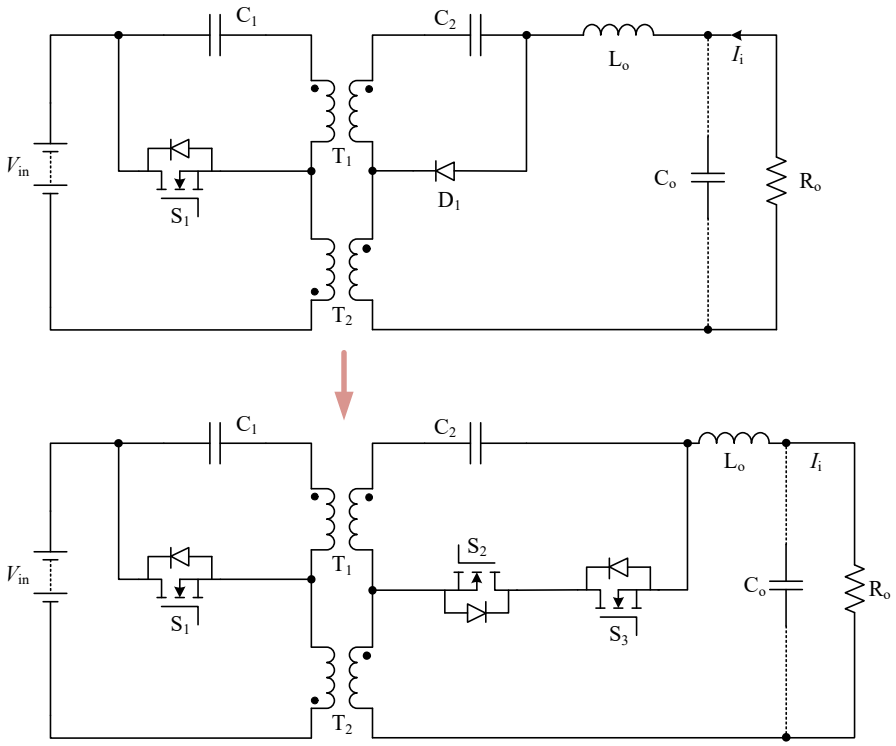


Fig. 5.2 Isolation D2 inverter dc to ac circuit configuration

In this topology, the switch on the primary side is the only switch used to control converter inversion. The two secondary side switches are used to reverse (as director switches) the voltage and current per 100 Hz, resulting in the final 50 Hz alternating current waveform. The secondary two switches are not modulated.

A 60 Vdc/250 W hardware platform will be used.

5.1.2 Modulation Method

Sinusoidal pulse width modulation (SPWM) is selected to control the primary side switch S_1. 50 Hz complementary square wave signals are used to control S_2 and S_3, as shown in Fig. 5.3

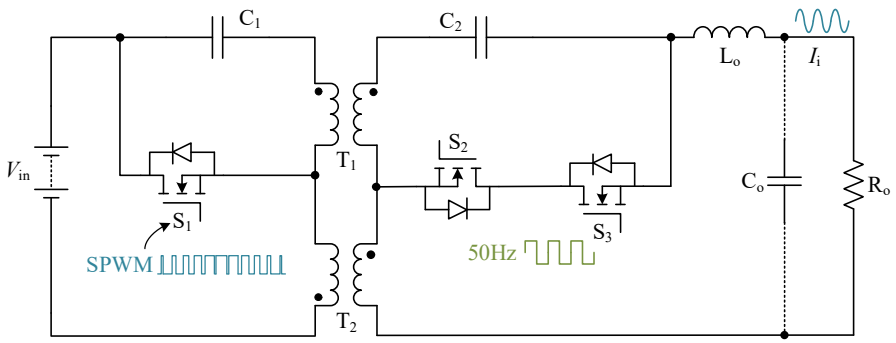
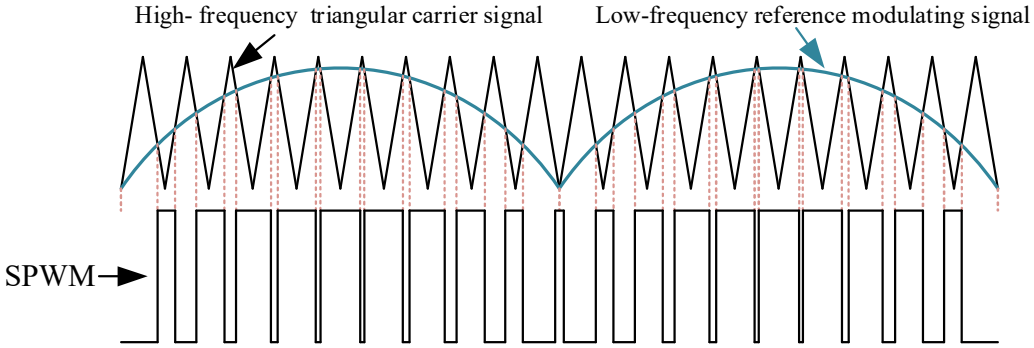
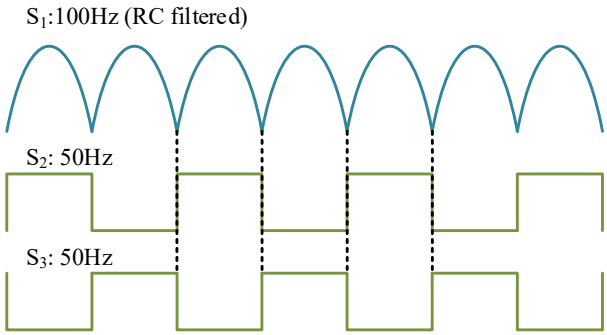


Fig. 5.3 Isolation D2 inverter modulation

S_2 and S_3 are used to 'flip' the output voltage and current waveforms, as shown in Fig. 5.4, which shows the SPWM generation principle in this inversion.



(a) S_1 modulation



(b) Isolated D2 inverter SPWM and 50Hz square wave signals

Fig. 5.4 The isolated D2 inverter modulation

5.2 Control Strategy

5.2.1 Second-Order Generalized Integrator

Second-order generalized integrator (SOGI) is an orthogonal system depicted in Fig. 5.5. As output signals, two sine waves (v' and qv') phase shifted by 90° are generated. The component v' has the same phase and magnitude as the fundamental of the input signal v.

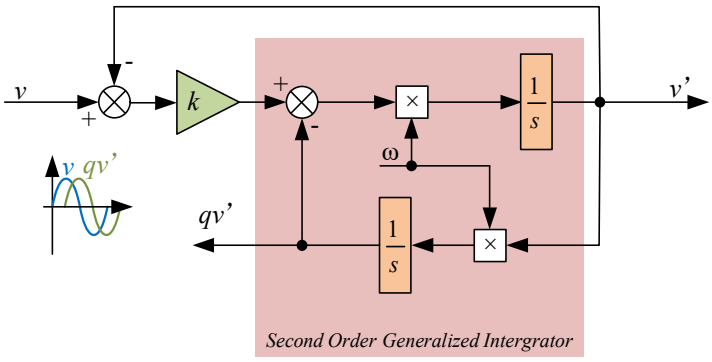


Fig. 5.5 General structure of a single-phase PLL based on SOGI

The structure is defined as:

$$G_{\mathrm{SP-PLL}}(s)=\frac{\omega s}{s^2+\omega^2} \tag{5-1}$$

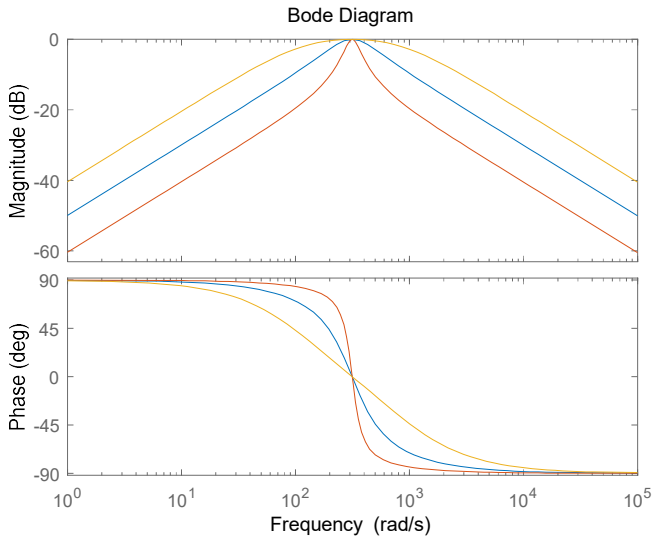
where ω represents the SOGI resonance frequency. The closed-loop transfer functions of the structure are:

$$H_d(s)=\frac{v'}{v}(s)=\frac{k\omega s}{s^2+k\omega s+\omega^2} \tag{5-2}$$

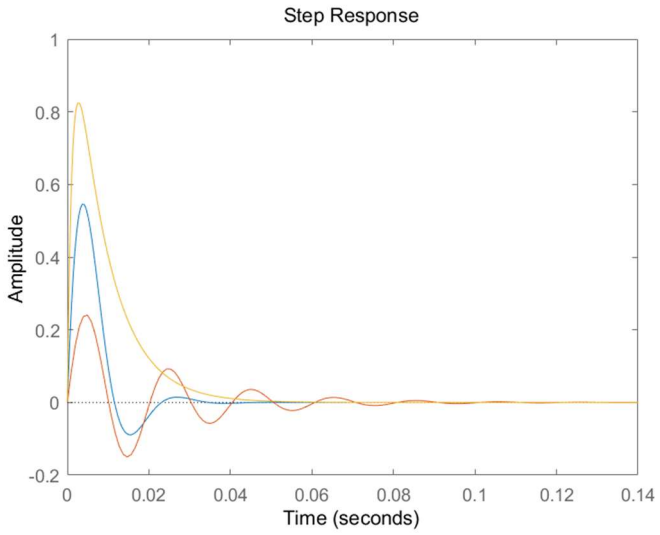
$$H_q(s) = \frac{qv'}{v}(s) = \frac{k\omega^2}{s^2 + k\omega s + \omega^2} \tag{5-3}$$

where k affects the closed-loop bandwidth.

The Bode representation and the step response of the closed-loop transfer function for the proposed structure at different values of gain k are shown in Fig. 5.6 (a) and (b).



(a) Bode plots



(b) Step response

Fig. 5.6 Closed-loop transfer function (H_d) at different values of gain k

The resonance frequency value of the SOGI is adjusted by the provided frequency of the PLL. The method for creating the orthogonal system has advantages compared to other methods (viz. Transport-Delay, Hilbert Transformation, and Inverse Park Transformation). With a simple structure, as seen from Fig. 5.6, three main tasks are

performed: generating the orthogonal voltage system; filtering the orthogonal voltage system without delay; and the structure is frequency adaptive.

In the proposed method, the input signal v is filtered, resulting in orthogonal voltage waveforms, v and qv', due to SOGI resonance at grid frequency ω. The filtering level can be set by gain k. As k decreases, the filter bandpass narrows, resulting in heavy filtering, but the system dynamic response becomes slower, as observed in Fig. 5.6b. From Fig. 5.6a, at resonance frequency, there is no attenuation compared to high attenuation away from this frequency.

Another reason for choosing SOGI is that in this inversion system, the integration and differentiation of sine and cosine are both simple.

5.2.2 Inversion Control

Fig. 5.7 shows the inversion control block diagram in detail and is used to validate its effectiveness and practicability.

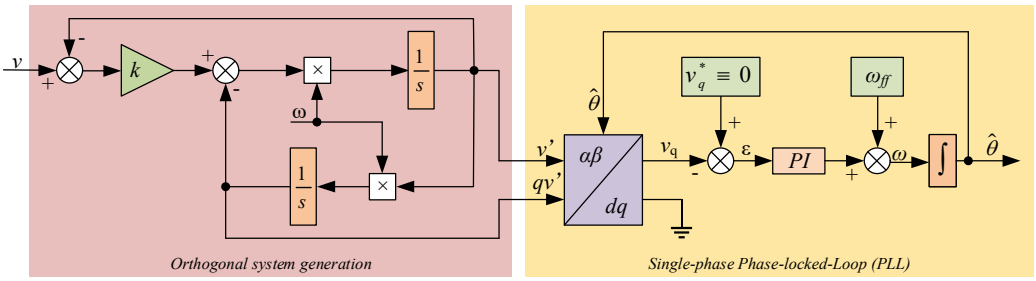
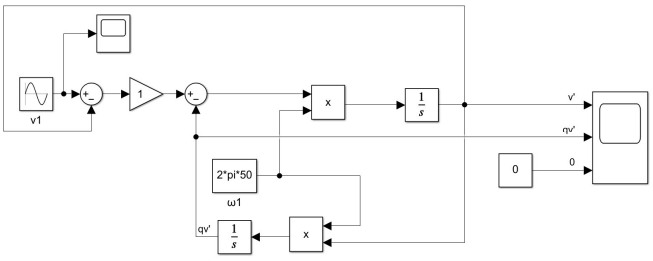
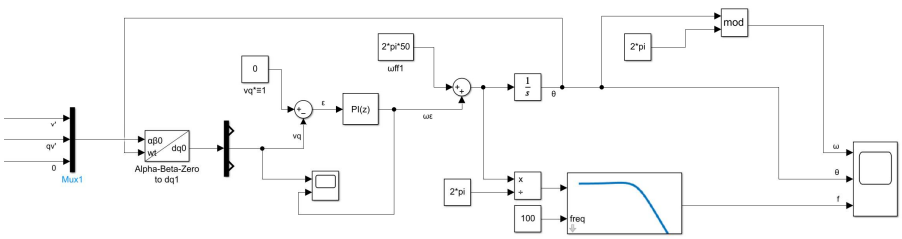


Fig. 5.7 The inversion control block diagram

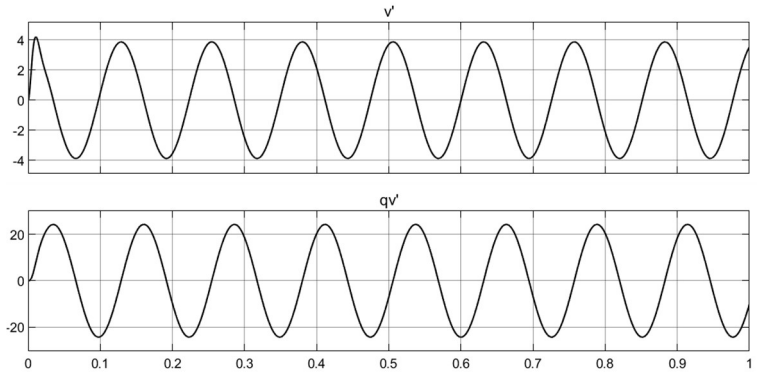


(a) SOGI

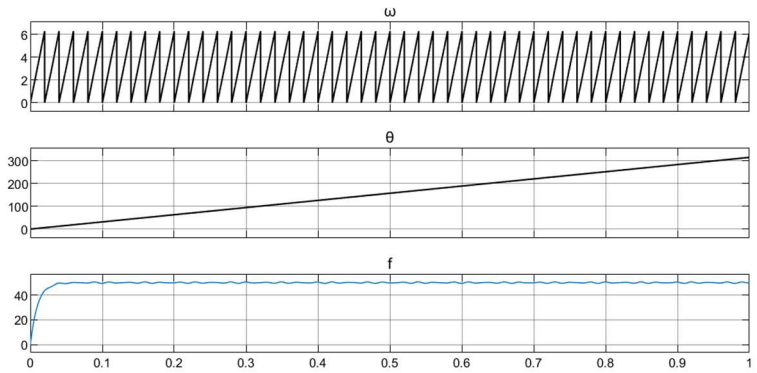


(b) PLL

Fig. 5.8 The single-phase PLL based on SOGI in MATLAB/Simulink



(a) v' and qv'



(b) ω, θ and f

Fig. 5.9 The parameters of the single-phase PLL based on SOGI

The simulation result in Fig. 5.9 verifies that the single-phase PLL based on SOGI functions in the isolated D2 inversion.

5.3 Simulation

SPWM modulation and SOGI control are used for the circuit in figures 5.4b and 5.5, with the simulation model shown in Fig. 5.10.

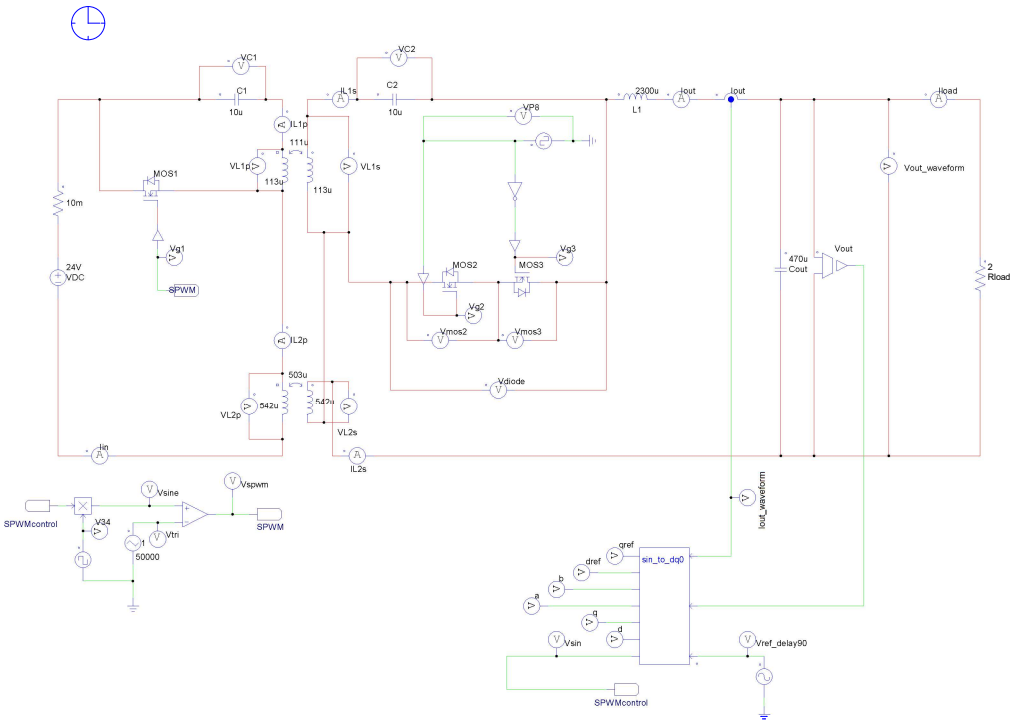


Fig. 5.10 Isolated D2 inverter model in simulation software

In simulation, the input dc power supply is 24 V, output inductance is 2300 μH, output capacitance is 470 μF, resistive load is 2 Ω, and the output ac current maximum value is controlled at 9 A.

The two sine waves in Fig. 5.11 have a phase shift of 90°, where these orthogonal signals, *v*' and *qv*', generated by the control program, are used in the PLL.

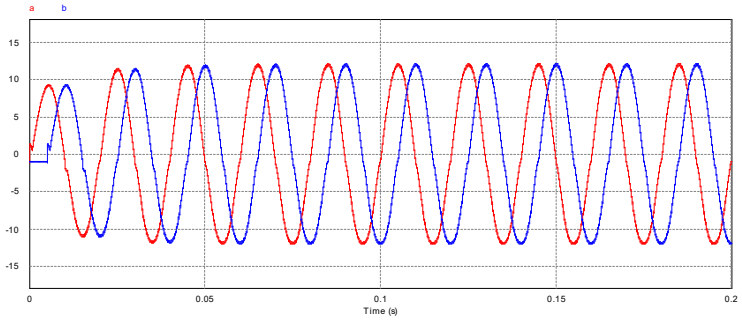


Fig. 5.11 Orthogonal signals *v*' and *qv*' generated from simulation

In Fig. 5.12, the modulation signals of primary switch S_1 are from the single-phase PLL, based on SOGI control after low pass filtering. In the simulation circuit, there are capacitors, transformers, and inductors, which make the circuit not completely dual. Therefore, in the closed-loop control, the modulation waveform of S_1 adjusts itself to make the positive and negative cycles of the output voltage symmetrical. Hence, the

adjacent two modulation waveforms are not the same. Also the basic transfer function of the D2 converter is non-linear. The secondary switches S_2 and S_3 are consistent with Fig. 5.4b. In the simulation, modulation signals stabilize after two cycles, which satisfies the design requirement and validates control effectiveness.

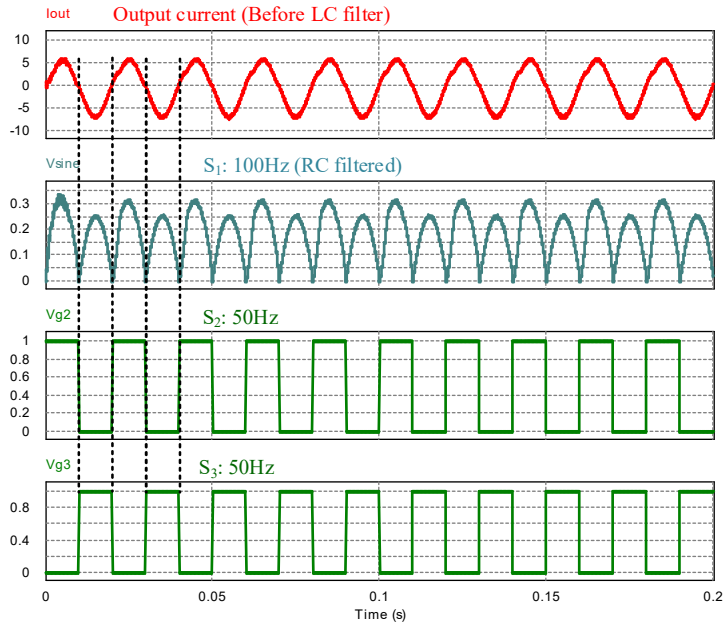


Fig. 5.12 Isolated D2 inverter modulation in simulation (closed-loop)

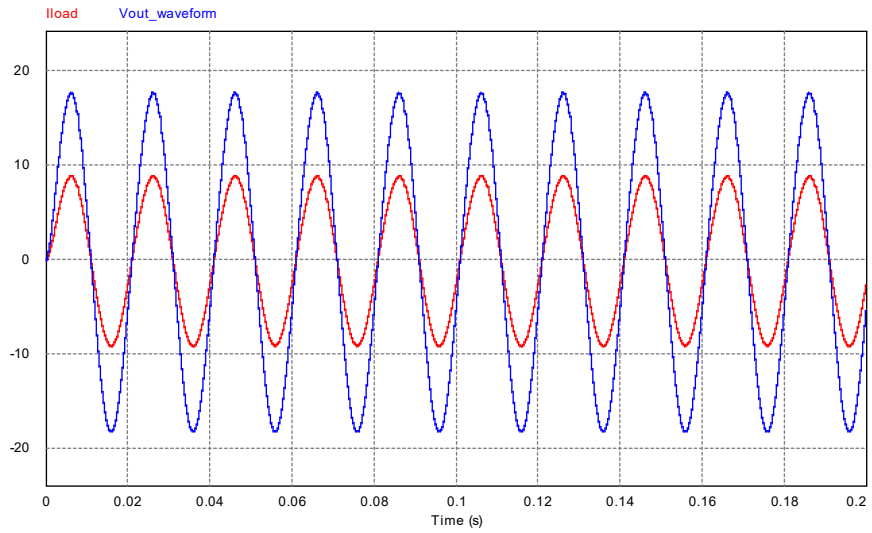
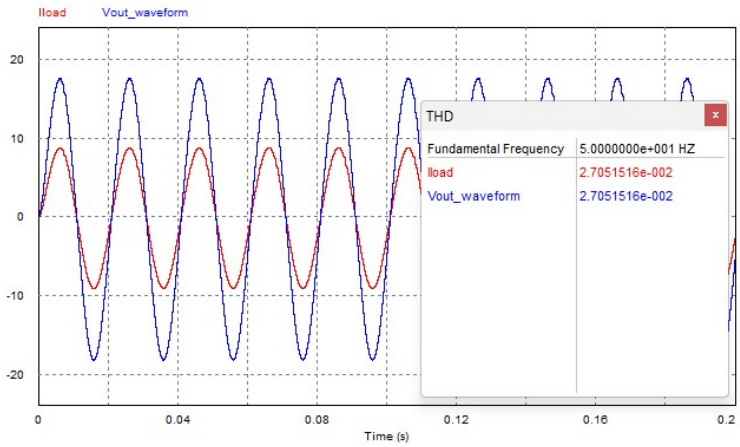
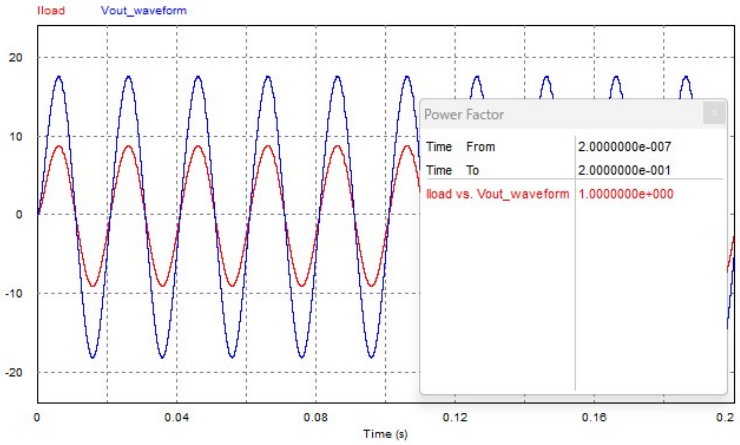


Fig. 5.13 Isolated D2 inverter simulation output waveforms

The current in Fig. 5.13 is controlled as a sine wave with a frequency of 50 Hz and a maximum value of 9 A. The simulation verifies that the isolated D2 can invert the dc supply to the ac side under control, and the output current and voltage waveforms are sinusoidal.



(a) THD



(b) PF

Fig. 5.14 Isolated D2 inverter simulation FFT analysis

Inverter simulation output THDs (from an FFT module), in Fig. 5.14 (a), are 2.71% (current), and is 2.71% (voltage), which meets grid connection requirement of less than 5% for distributed resources. The PF of the inverter is 1, as shown in Fig. 5.14 (b).

The isolated dc to single phase ac inverter features the following performance and advantages.

- From the perspective of circuit complexity and cost, the isolated D2 inverter has three switches. Fewer switches not only simplifies the circuit itself but also means fewer driver circuits.
- Switch stress on the secondary side is reduced; two switches connected in reverse series having a 50% duty cycle.
- From the perspective of generating ac power quality, the THD is relatively low, and the PF approaches unity.

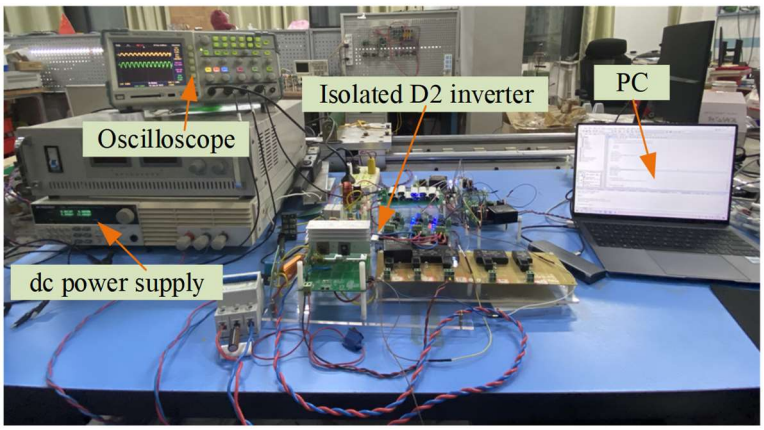
The isolated D2 inverter has the advantages of a simple circuit, simple control, simple modulation, low cost, high-quality electrical energy, and electrical isolation with only three switches.

5.4 Experimentation

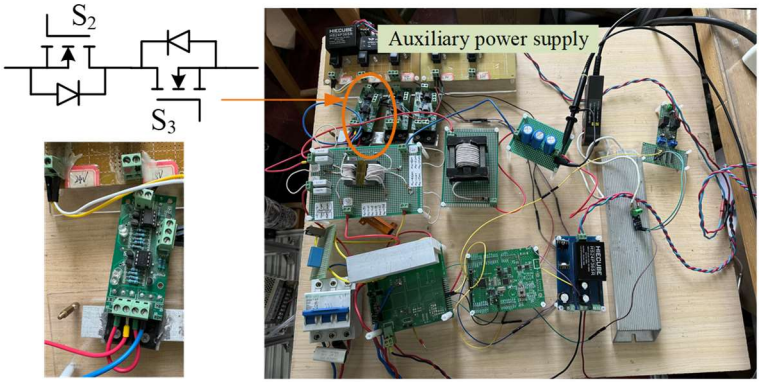
5.4.1 Hardware Platform

The isolated D2 inverters hardware platform is an extension to the isolated D2 dc/dc converter hardware platform. The secondary diode is replaced by two series switches, and dc sensors are replaced by ac sensors, as in Fig. 5.15 (a), while Fig. 5.15 (b) (c) shows the two circuit modifications.

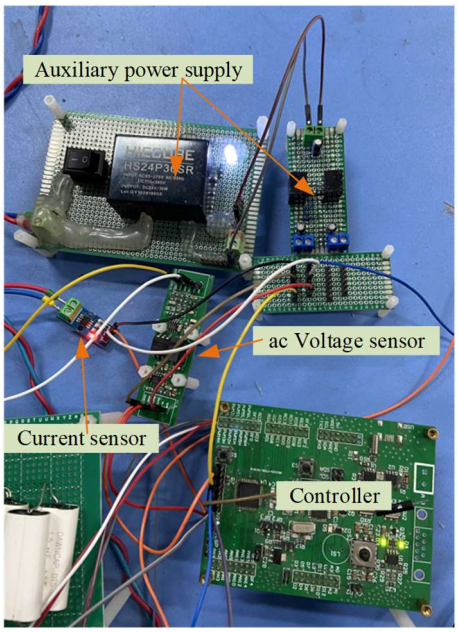
The input dc power supply is 24 V, output inductance is 2300 μH, output capacitance is 470 μF, the resistive load is 8 Ω, and the output ac current maximum value is set to 1.5 A under control.



(a) Hardware platform



(b) Isolated D2 inverter circuit



(c) ac voltage and current sensors

Fig. 5.15 Isolated D2 inverter circuit hardware platforms

5.4.2 Modulation and Control

The inverter modulation is as in as in the simulation. S_2 and S_3 signals are complementary square waves as shown in Fig. 5.16.

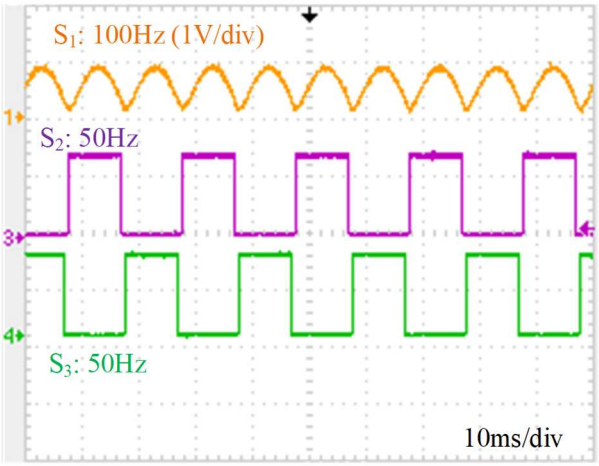


Fig. 5.16 Isolated D2 inverter modulation signals

A single-phase PLL based on the SOGI control program is also typed into the controller so that the final modulated wave is a 100 Hz sine wave.

5.4.3 Experimental Results

First, an open-loop experiment is performed to test and verify the feasibility of the isolated D2 inverter in the hardware platform. In Fig. 5.17, the ac side voltage and

current waveforms have a 50 Hertz fundamental but with distortion harmonics due to the D2 non-linear transfer function.

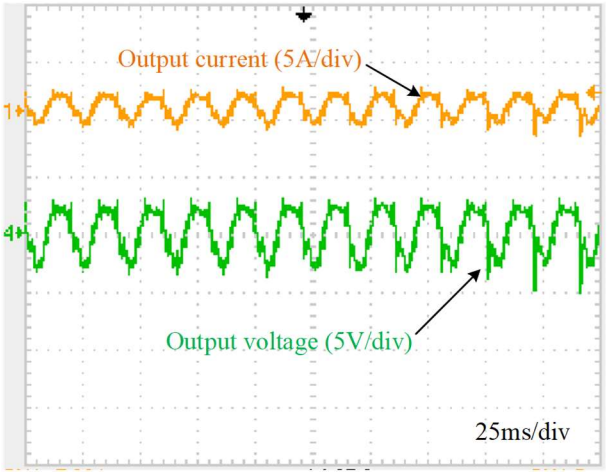
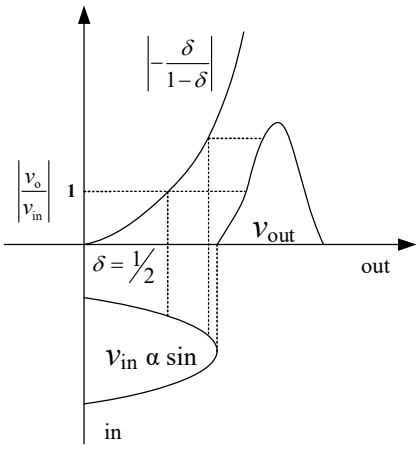
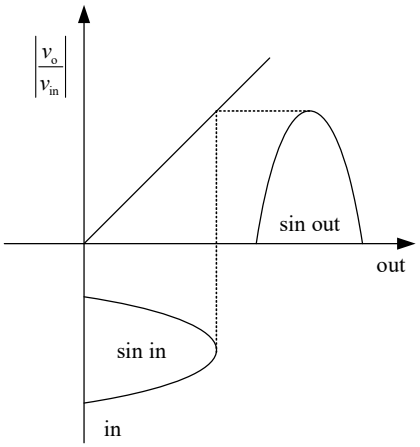


Fig. 5.17 Isolated D2 inverter output waveforms in open-loop

Fig. 5.18 (a) shows the relationship between sin input demand, δ, and hence v_{out}. In the open-loop, the isolated D2 converter transfer ratio is $-\delta/(1-\delta)$, which is a non-linear relationship, so the voltage and current waveforms distort without compensation. If v_{out}/v_{in} is linear, that is, a straight line, as shown in Fig. 5.18 (b), the output voltage and current waveforms would be sinusoidal.



(a) Non-linear



(b) Linear

Fig. 5.18 Isolated D2 inverter output waveforms distortion source

Since achieved open-loop waveforms validate the feasibility of inversion, control is added. Considering the power supply power limit and current value, an 8 Ω resistor is selected as load.

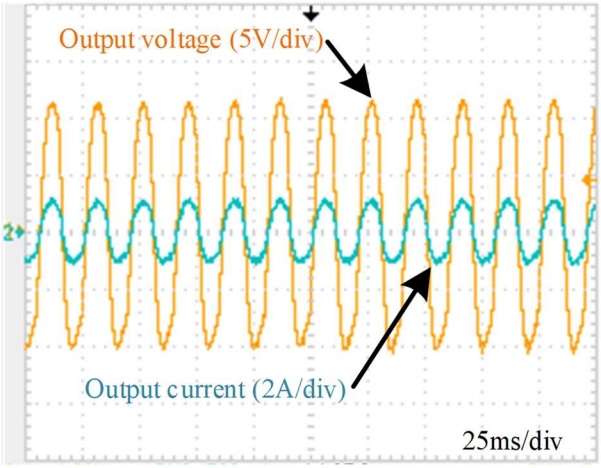
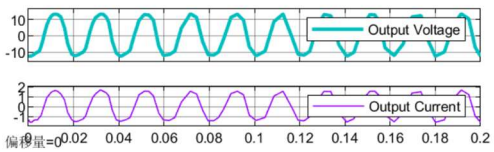
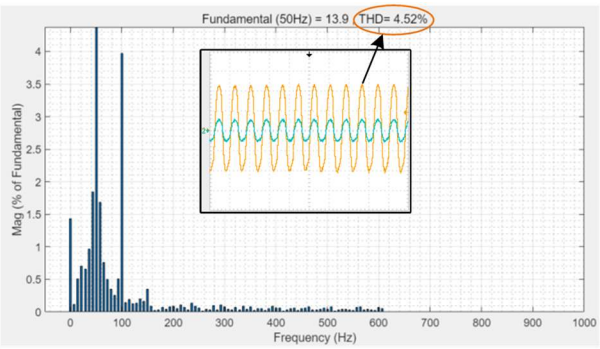


Fig. 5.19 Isolated D2 inverter output waveforms in closed-loop

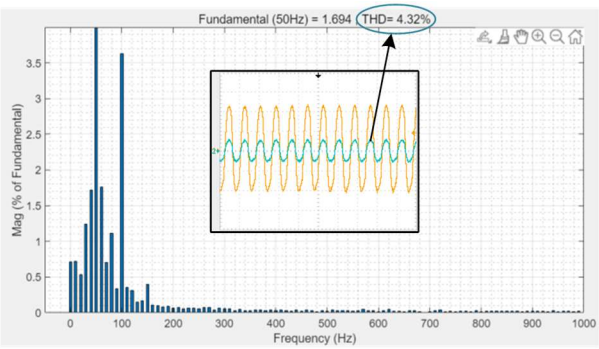
In Fig 5.19, the voltage maximum value is controlled at 12 V, and the current maximum value is 1.5 A, with the current and voltage waveforms being essentially sinusoidal. The output current and voltage waveforms data imported into MATLAB/Simulink give THDs of 4.52% and 4.32% for current and voltage respectively, where both are less than 5%, and the PF is near 1.



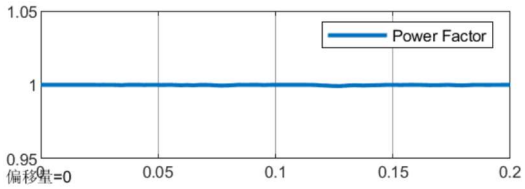
(a) Imported output voltage and current waveforms



(b) THD of the isolated D2 inverter output voltage



(c) THD of the isolated D2 inverter output current



(d) PF of the isolated D2 inverter output

Fig. 5.20 THD and PF of the isolated D2 inverter

Since the isolated D2 inverter can generate ac power that meets grid standards, it is a practical and feasible approach to dc to ac conversion.

5.5 ac/dc Conversion

The isolated D2 converter is a reversible topology, that is, it can perform as a converter (ac/dc) and an inverter (dc/ac), theoretically. The ac side is replaced by a single-phase ac voltage source, with a diode and resistive load on the dc side. This inverse D2 mode, is effectively the isolated D1 converter, introduced in simulation in Chapter 2.

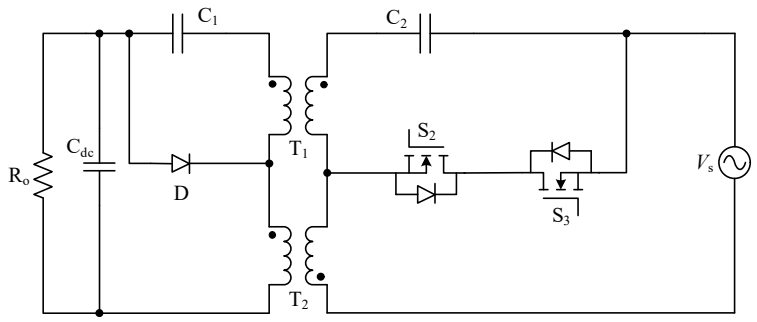


Fig. 5.21 Isolation D2 ac to dc converter

For simulation, Fig.5.22, the ac power supply maximum value is 12 V/50 Hz, the output capacitance is 470 μF, the resistive load is 4 Ω, and the output ac current maximum value is controlled at 2 A.

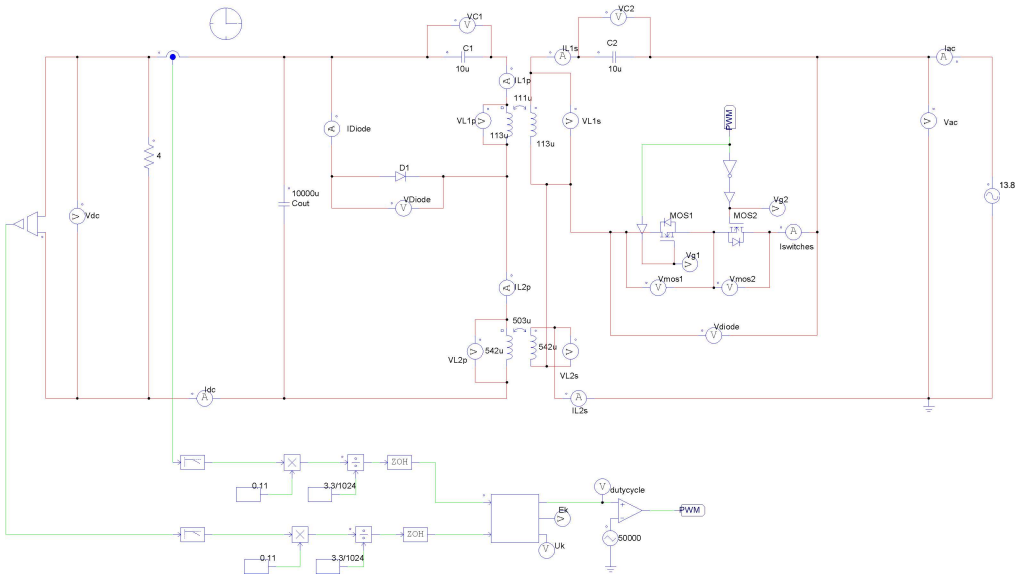


Fig. 5.22 Isolated D2 ac to dc converter model in simulation software

In the simulation, the dc voltage reference is set to -8 V and the current reference is set to -2 A. The ac input voltage and current are in phase, shown in Fig. 5.23.

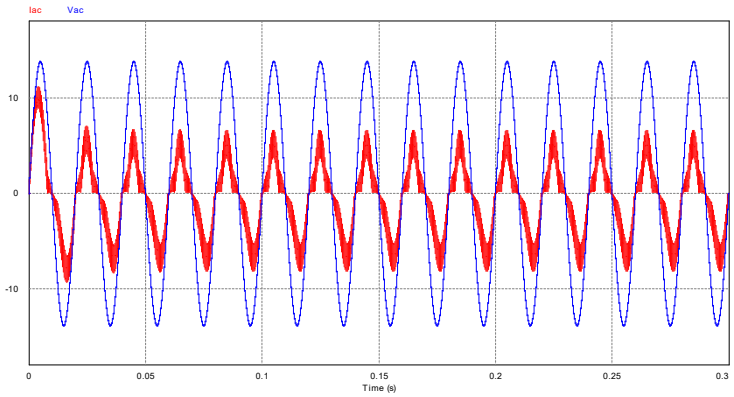
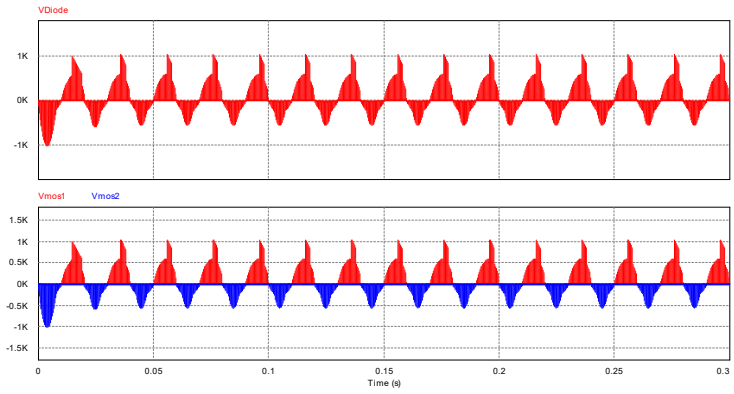
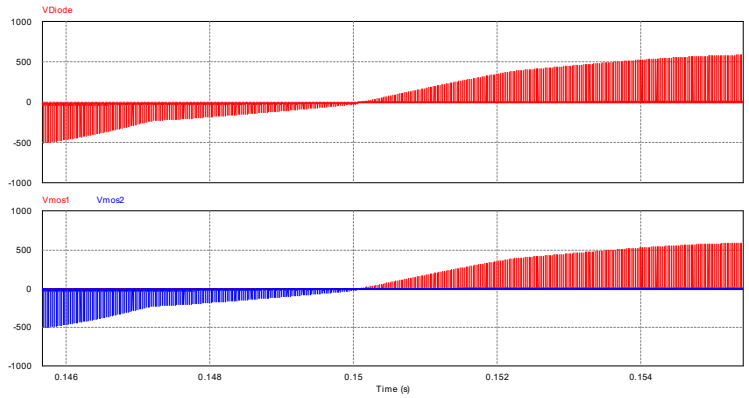


Fig. 5.23 Isolated D2 ac to dc converter simulation input voltage and current waveforms

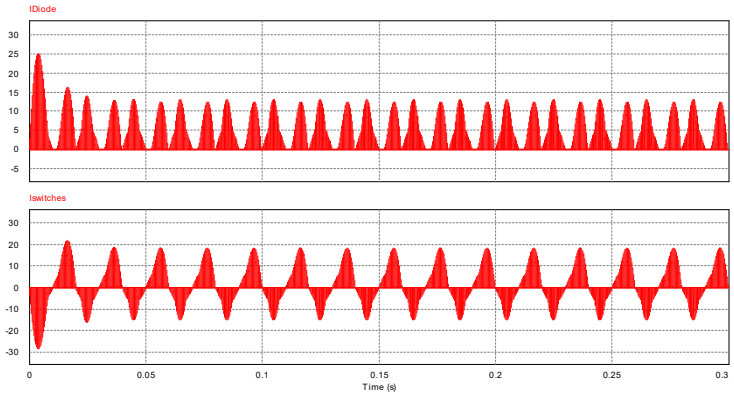


(a) S_1, S_2 and D_1 voltage stress

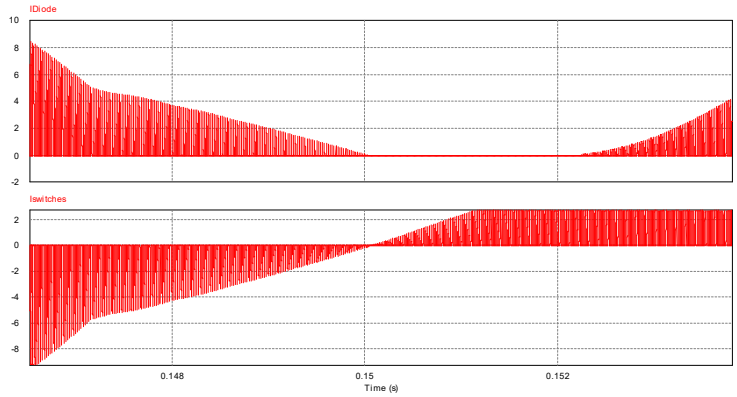


(b) S_1, S_2 and D_1 voltage stress detail view

Fig. 5.24 Isolated D2 ac to dc converter switches voltage stress



(a) S_1, S_2 and D_1 current stress



(b) S_1, S_2 and D_1 current stress detail view

Fig. 5.25 Isolated D2 ac to dc converter switches current stress

From Fig. 5.24 and Fig. 5.25, the topology is symmetry; the sum of the voltage and current stress vector of S_1 and S_2 is equal to that of the dc side diode. The isolated D2 ac to dc converter output waveforms are shown in Fig. 5.26.

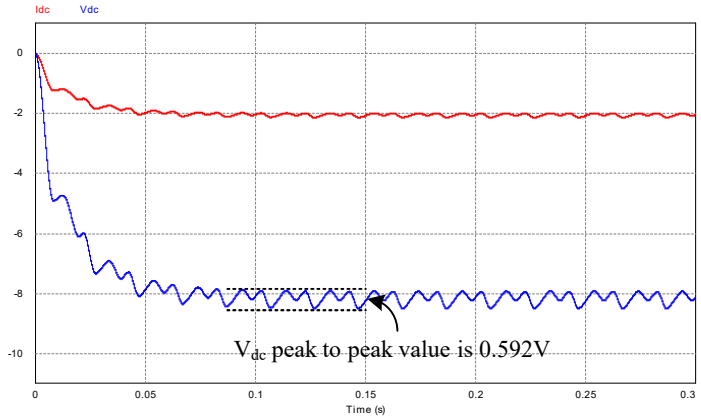


Fig. 5.26 Isolated D2 ac to dc converter simulation output waveforms

The dc output voltage has a second order harmonic component due to the ac supply, as shown in Fig 5.26, where the voltage mean value is controlled at -8 V, and the current mean value is controlled at -2 A. As with all single-phase ac to dc converters, this output ripple is expected since the source energy pulsates at 100 Hz, while the converter transfers energy at the switching frequency. The dc voltage output peak to peak value is 0.592 V and output voltage mean value is 8.144 V, so that the ripple coefficient is

$$\frac{0.592\text{V}}{8.144\text{V}}\times 100\%=7.27\%<10\%.$$

For ac adapters, the qualified ripple coefficient should usually be less than 10 % of the output voltage, and the isolated D2 ac to dc converter meets this requirement. The ripple

can be reduced by increasing the dc output capacitance.

The analysis and simulation establish that the isolated D2 ac to dc converter is viable. The isolated bidirectional D2 circuit is suitable for bidirectional power transmission, with few switches (three). It offers CCM on the input and output so that the converter can be connected to the PV panels, and other renewable energy sources. The isolated D2 converter can realise dc to dc, dc to ac, and ac to dc conversion. Hence, the topology is suitable for distributed energy and microgrid systems. The dc to ac and ac to dc properties, along with isolation, make the topology applicable to EV charging application that requires a back-to-grid feature.

5.6 Summary

This chapter proposed and studied a single-phase dc/ac inverter derived from the isolated D2 converter. The primary switch is modulated by SPWM and controlled by a single-phase PLL based on SOGI. Modulation and control strategies can be used to design and modulate the isolated D2 inverter. Both simulation and experimentation verified the feasibility of the circuit design and validated control accuracy. The proposed inverter can regulate the ac load current and voltage and reduce harmonics with only three switches and electrical isolation, and few converters can realize this function. Also, the ac to dc converter inversed of the isolated D2 inverter was also proposed to verify the flexibility of the isolated D2 inverter.

CHAPTER 6 Conclusion and Future Research

This chapter summarises the general conclusion arising from the research, main contribution by the author, and the envisaged future research in the isolated D2 converter.

6.1 General Conclusions

An isolated D2 topology derived from the D2 converter was investigated. The working principle, circuit model, mathematical model, and applications were researched. Based on the circuit topology and performance, the system framework was designed, its feasibility was modelled and analyzed, and corresponding modulation strategies and control methods were designed. All system simulation models were built in LTSpice or PSIM softwares, and hardware platform construction and experimental verification were completed. The characteristics and practicality of this topology were studied and analyzed. The specific work lists are as follows:

(1) The system was proven stable by analyzing the isolated D2 converter operating principle, switch average model, and state-space mathematical model, calculating the converter transfer ratio, small signal equivalent model, transfer function and the bode plots of the ac scan.

(2) A hardware platform was designed and constructed, and the transformer hardware structure was investigated through simulation, winding methods, experimentation, and finite element analysis these aspects. The isolated D2 converter with resistive load and capacitive load in closed-loop was tested and verified in the PSIM software and hardware platform.

(3) The isolated D2 converter was applied in three dc/dc applications in simulation and experimentation: MPPT in PV systems, IPOS, and interleaved parallel connection. The converter and the interleaving converter can track the MPP rapidly and effectively. The two-phase IPOS isolated converter combining both advantages of IPOS and the isolated D2 was validated. Interleaving technology was employed in the topology and showed good features.

(4) The isolated D2 converter, bridgeless isolated D2 converter and interleaved isolated D2 converter were used in PFC applications. All these three topologies reduced THD and improved PF in simulation and hardware platforms.

(5) A single-phase inverter derivation from the isolated D2 converter was presented, the SPWM operating the only switch that can be modulated was explained, and the inversion control based on SOGI-PLL was employed. Both simulations and

experiments verified the feasibility of the inversion based on the proposed topology.

6.2 Authors Original Contributions

An outline of the novel research realised by this author is as follows:

- ✓ Derived, designed and analysed a novel one-switch ***isolated*** D2 converter and offered core flux ripple cancellation with a single transformer core with four windings in the proposed topology.
- ✓ Proposed practical dc/dc applications; super-capacitor charge, PV, IPOS, and interleaving.
- ✓ Compared and analysed the three cascaded isolated D2 converters in PFC applications.
- ✓ Proposed a novel primary side one switch and two switches secondary side inverter derived from the isolated D2 converter, (only three switches), with galvanic isolation and bidirectionality.
- ✓ Provided comprehensive theoretical, simulation and experimental verification for all the proposed dc/dc, ac/dc and dc/ac conversion applications.

6.3 Future Research

Due to the limitations of simulation conditions and time, the research content is not totally comprehensive. Further research is needed to address the following technical and application issues:

(1) The designed hardware platform requirement was a low power level system and limited load capacity, which makes it impossible to observe the operation of multiphase converters visually. In the future, components with high voltage and current stress can be selected, and multiphase (three) converters can be added for detailed analysis.

(2) The isolated D2 converter systems in this thesis were composed of one converter or two-phase converters, and their performance was analysed. In the future, whether charging or inversion can be quickly restored under faults and after fault elimination, can be analysed. If the response is not fast enough, the control strategies can be

optimized further.

(3) Better (more sophisticated) control strategies should enable lower THD results in dc to ac conversion.

(4) Compare and analyze the isolated D2 converter with other basic one-switch isolated converters existing in detail.

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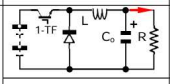
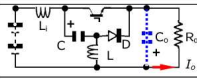
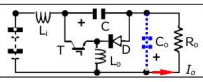
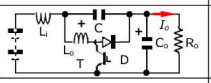
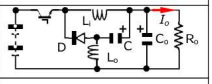
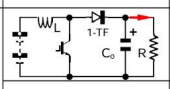
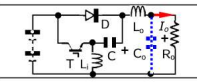
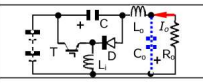
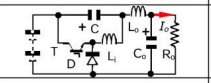
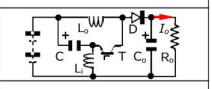
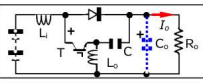
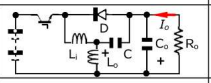
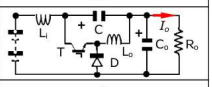
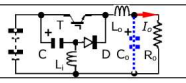
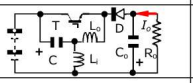
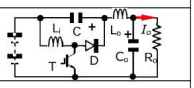
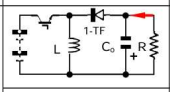
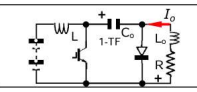
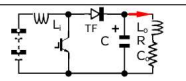
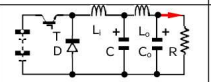
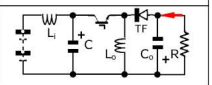
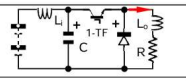
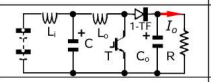
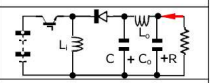
Appendix A 33 Known Single Switch dc to dc Converters and Their Alphanumeric Classification

	A	C	D	E	F
1					
	A1: Buck δ	C1: δ	$-\delta$ /1-δ	1/1-δ	δ
2					
	A2: Boost 1/1-δ	C2: 1/1-δ	$-\delta$ /1-δ	δ	1/1-δ
3					
			1/1-δ	$-\delta$ /1-δ	δ
4					
			δ	$-\delta$ /1-δ	1/1-δ
5					
	A5: Buck-Boost $-\delta$ /1-δ	C5: Cuk $-\delta$ /1-δ	1/1-δ	δ	$-\delta$ /1-δ
6					
			δ	1/1-δ	$-\delta$ /1-δ -ve Luo

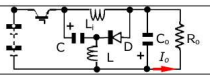
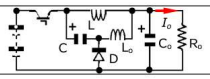
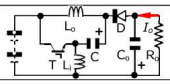
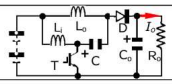
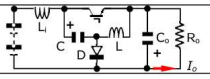
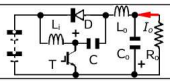
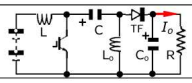
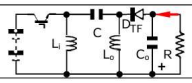
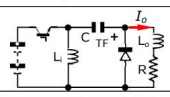
	G	P
1		
	$-\delta$ /1-2δ	P1: δ
2		
	1-2δ /1-δ	P2: 1 /1-δ
3		
	$-\delta$ /1-2δ	
4		
	1-2δ /1-δ	
5		
	sepic δ /1-δ	P5: $-\delta$ /1-δ
6		
	+ve Luo/zeta δ /1-δ	

Fig. A.1. 33 known single switch dc to dc converters and their alphanumeric classification [2]

Appendix B PSIM Software C Block Code

All the simulation controls in the C block code are shown below.

B1. Isolated D2 dc/dc Simulation: Voltage and Current Selection

Variable/Function definitions:

```
#include <Stdlib.h>
#include <String.h>
#include<stdio.h>
#include <math.h>

 int gnInputNodes=0;
 int gnOutputNodes=0;

 int gnStepCount=0;

double Vout, Iout, D;

double Vref, Iref;
double Uk=0, Uk1=0, Ek=0, Ek1=0;
double uk=0, uk1=0, ek=0, ek1=0;
```

RunSimUser Fcn:

```
gnStepCount++;

Vout=in[0];
Iout=in[1];
Vref=-20*0.11/0.0032;
Iref=-3*0.11/0.0032;

Ek=-Vref+Vout;
Uk=Uk1+15*(Ek-Ek1)+0.02*Ek;
Uk1=Uk;
Ek1=Ek;

if(Uk>9728)
       Uk=9728; //0.95
if(Uk<512)
       Uk=512;          //0.05

ek=-Iref+Iout;
uk=uk1+15*(ek-ek1)+0.05*ek;
uk1=uk;
ek1=ek;

if(uk>9728)
     uk=9728;
if(uk<512)
     uk=512;

if(Uk>uk)
       D=uk;
if(Uk<=uk)
       D=Uk;

out[0]=D;
out[1]=ek;
out[2]=Ek;
```

B2. Isolated D2 dc/dc Simulation: MPPT

Variable/Function definitions:

```
#include <Stdlib.h>
#include <String.h>
#include<stdio.h>
#include <math.h>

 int gnInputNodes=0;
 int gnOutputNodes=0;

 int gnStepCount=0;

double Uin=0,Uin 1=0, Iin=0,Iin 1=0, Do=5120;
double biasU=0,biasI=0;
double e=0;

double UKref=1375;       //40V
double UK2=0, UK2 1=0, EK2=0, EK2 1=0;

      float      Ts=1e-5;                  //100k
      double     Kp=5;
      float      Ti=0.0005;
      float      C=Kp*(2*Ti+Ts)/(2*Ti);
      float      D=Kp*(Ts-2*Ti)/(2*Ti);
```

RunSimUser Fcn:

```
gnStepCount++;

Uin=in[0];
Iin=in[1];
biasU=Uin-Uin1;
biasI=Iin-Iin1;

if(gnStepCount%40==0||gnStepCount==1)
{
   if(biasU==0)
   {
      if(biasI>0)
         UKref+=17;          //left: plus 0.5 V
      if(biasI<0)
         UKref-=8;           //right: minus 0.25V
   }
   if(biasU!=0)
   {
      e=Iin+Uin*biasI/biasU;
      if(e<0)
        UKref-=8;           //right: minus 0.25V
      if(e>0)
        UKref+=17;          //left: plus 0.5V
   }

   Uin1=Uin;
   Iin1=Iin;

   if(UKref<515)
      UKref=515;      //15V input
   if(UKref>1891)
      UKref=1891;      //55V input
}

   EK2=Uin-UKref;
   UK2=UK21+C*EK2+D*EK21;

   if(UK2<=100)    //0.01
     UK2=100;
   if(UK2>=9728)//0.95
     UK2=9728;

    UK21=UK2;
    EK21=EK2;
   Do=UK2;

out[0]=Do;
out[1]=UKref;
out[2]=biasI;
```

B3. Isolated D2 dc/dc Simulation: MPPT and CCCV

Variable/Function definitions:

```
#include <Stdlib.h>
#include <String.h>
#include<stdio.h>
#include <math.h>

 int gnInputNodes=0;
 int gnOutputNodes=0;

 int gnStepCount=0;

double Uin=0,Uin1=0, Iin=0, Iin1=0, Do=5120;

double biasU=0,biasI=0;
double e=0;

double UKref=1375;        //40V
double UK=0, UK1=0, EK=0, EK1=0;

      float      Ts=1e-5;                  //100k
      double     Kp=5;
      float      Ti=0.0005;
      float      C=Kp*(2*Ti+Ts)/(2*Ti);
      float      D=Kp*(Ts-2*Ti)/(2*Ti);
```

RunSimUser Fcn:

```
g_nStepCount++;

Uin=in[0];
Iin=in[1];
Uout=in[2];
Iout=in[3];

biasU=Uin-Uin1;
biasI=Iin-Iin1;

if(gnStepCount%40==0||gnStepCount==1)
{

   if(biasU==0)
   {
      if(biasI>0)
         UKref+=17;          //left: plus 0.5 V
      if(biasI<0)
         UKref-=8;           //right: minus 0.25V
      }
   if(biasU!=0)
   {
      e=Iin+Uin*biasI/biasU;
      if(e<0)
        UKref-=8;           //right: minus 0.25V
      if(e>0)
        UKref+=17;          //left: plus 0.5V
   }


   Uin1=Uin;
   Iin1=Iin;

   if(UKref<859)
      UKref=859;      //25V input
   if(UKref>1891)
      UKref=1891;     //55V input
}
```

```
    EK=Uin-UKref;
    UK=UK1+C*EK+D*EK_1;
    if(UK<=100)    //0.01
      UK=100;

    if(UK>=9728)//0.95
      UK=9728;

     UK1=UK;
     EK1=EK;
       Do=UK;

Uoref=-30*0.11/0.0032;
Ioref=-15*0.11/0.0032;

Ek2=-Uoref+Uout;
Uk2=Uk2_1+85*(Ek2-Ek2_1)+0.0002*Ek2;
Uk2_1=Uk2;
Ek2_1=Ek2;

if(Uk2>9728)
       Uk2=9728;        //0.95
if(Uk2<100)
       Uk2=100;         //0.01

ek3=-Ioref+Iout;
uk3=uk31+15*(ek3-ek31)+0.05*ek3;
uk31=uk3;
ek31=ek3;

if(uk3>9728)
      uk3=9728;
if(uk3<100)
      uk3=100;

if((Uk2>uk3)&&(uk3<UK))
       Do=uk3;
if((uk3>Uk2)&&(Uk2<UK))
       Do=Uk2;
if((Uk2>UK)&&(UK<uk3))
       Do=UK;

out[0]=Do;
out[1]=UKref;
out[2]=biasI;
```

B4. Input Parallel Output Series Isolated D2 Converter Control

Variable/Function definitions:

```
#include <Stdlib.h>
#include <String.h>
#include<stdio.h>
#include <math.h>

 int gnInputNodes=0;
 int gnOutputNodes=0;

 int gnStepCount=0;

double Vout, Iout, D;

double Vref, Iref;
double Uk=0, Uk1=0, Ek=0, Ek1=0;
double uk=0, uk1=0, ek=0, ek1=0;
```

RunSimUser Fcn:

```
gnStepCount++;

Vout=in[0];
Iout=in[1];
Vref=-200*0.11/0.0032;
Iref=-100*0.11/0.0032;

Ek=-Vref+Vout;
Uk=Uk1+15*(Ek-Ek1)+0.02*Ek;
Uk1=Uk;
Ek1=Ek;

if(Uk>9728)
       Uk=9728; //0.95
if(Uk<512)
       Uk=512;          //0.05

ek=-Iref+Iout;
uk=uk1+15*(ek-ek1)+0.05*ek;
uk1=uk;
ek1=ek;

if(uk>9728)
     uk=9728;
if(uk<512)
     uk=512;

if(Uk>uk)
       D=uk;
if(Uk<=uk)
       D=Uk;

out[0]=D;
out[1]=ek;
out[2]=Ek;
```

B5. Interleaving Isolated D2 Converter Control

Variable/Function definitions:

```
#include <Stdlib.h>
#include <String.h>
#include<stdio.h>
#include <math.h>

 int gnInputNodes=0;
 int gnOutputNodes=0;

 int gnStepCount=0;

double Vout, Iout, D;

double Vref, Iref;
double Uk=0, Uk1=0, Ek=0, Ek1=0;
double uk=0, uk1=0, ek=0, ek1=0;
```

RunSimUser Fcn:

```
 gnStepCount++;

Vout=in[0];
Iout=in[1];
Vref=-20*0.11/0.0032;
Iref=-3*0.11/0.0032;

Ek=-Vref+Vout;
Uk=Uk1+15*(Ek-Ek1)+0.02*Ek;
Uk1=Uk;
Ek1=Ek;

if(Uk>9728)
       Uk=9728; //0.95
if(Uk<512)
       Uk=512;   //0.05

ek=-Iref+Iout;
uk=uk1+15*(ek-ek1)+0.05*ek;
uk1=uk;
ek1=ek;

if(uk>9728)
     uk=9728;
if(uk<512)
     uk=512;

if(Uk>uk)
       D=uk;
if(Uk<=uk)
       D=Uk;

out[0]=D;
out[1]=D;
out[2]=Ek;
```

B6. Single-phase Isolated D2 Converter PFC

Variable/Function definitions:

```
#include <Stdlib.h>
#include <String.h>
#include<stdio.h>
#include <math.h>

 int gnInputNodes=0;
 int gnOutputNodes=0;

 int gnStepCount=0;

double Vin, Iin;

double Iref=0;
double Uk=0, Uk1=0, Ek=0, Ek1=0;
double Ts=1e-5;

double  Kp=45;
double Ti=0.0005;
double C=Kp*(2*Ti+Ts)/(2*Ti);
double D=Kp*(Ts-2*Ti)/(2*Ti);
```

RunSimUser Fcn:

```
 gnStepCount++;

// In case of error, uncomment next two lines. Set *pnError to 1
// and copy Error message to szErrorMsg
 //*pnError=1;
 //strcpy(szErrorMsg, "Place Error description here.");

Vin=in[0];
Iin=in[1];

Iref=Vin/2.4;
Ek1=Ek;
Ek=Iref-Iin;
Uk1=Uk;
Uk=Uk1+C*Ek+D*Ek1;


if(Uk>9728)
      Uk=9728; //0.95
if(Uk<512)
      Uk=512;          //0.05

out[0]=Uk;
out[1]=Ek;
```

B7. Two-phase Isolated D2 Converter PFC

Variable/Function definitions:

```
#include <Stdlib.h>
#include <String.h>
#include<stdio.h>
#include <math.h>

 int gnInputNodes=0;
 int gnOutputNodes=0;

 int gnStepCount=0;

double Vin, Iin1, Iin2;

double Iref=0;
double Uk=0, Uk1=0, Ek=0, Ek1=0;
double uk=0, uk1=0, ek=0, ek1=0;
double Ts=1e-5;
```

RunSimUser Fcn:

```
 gnStepCount++;

Vin=in[0];
Iin1=in[1];
Iin2=in[2];

if( Vin>0)
{
Iref=Vin/2.4;
Ek1=Ek;
Ek=Iref-Iin1;
Uk1=Uk;
Uk=Uk1+C*Ek+D*Ek1;

if(Uk>9728)
      Uk=9728; //0.95
if(Uk<512)
      Uk=512;          //0.05
}
```

```
if(Vin<0)
{
Iref=-Vin/2.4;
ek1=ek;
ek=Iref-Iin2;
uk1=uk;
uk=uk1+C*ek+D*ek1;


if(uk>9728)
      uk=9728;  //0.95
if(uk<512)
      uk=512;          //0.05
}

out[0]=Uk;
out[1]=uk;
```

B8. Interleaved Isolated D2 Converter PFC

Variable/Function definitions:

```
#include <Stdlib.h>
#include <String.h>
#include<stdio.h>
#include <math.h>

 int gnInputNodes=0;
 int gnOutputNodes=0;

 int gnStepCount=0;

double Vin, Iin1, Iin2;

double Iref=0;
double Uk=0, Uk1=0, Ek=0, Ek1=0;
double uk=0, uk1=0, ek=0, ek1=0;
double Ts=1e-5;
```

RunSimUser Fcn:

```
 gnStepCount++;

Vin=in[0];
Iin1=in[1];
Iin2=in[2];

if( Vin>0)

{Iref=Vin/2.4;
Ek1=Ek;
Ek=Iref-Iin1;
Uk1=Uk;
Uk=Uk1+C*Ek+D*Ek1;

if(Uk>5120)
        Uk=5120; //0.95
if(Uk<512)
        Uk=512;   //0.05

out[0]=Uk;
out[1]=Uk;
}


if(Vin<0)
{
Iref=-Vin/2.4;
ek1=ek;
ek=Iref-Iin2;
uk1=uk;
uk=uk1+C*ek+D*ek1;


if(uk>5120)
        uk=5120;  //0.95
if(uk<512)
        uk=512;           //0.05

out[0]=uk;
out[1]=uk;
}
```

B9. Single-phase Isolated D2 Inverter Control

Variable/Function definitions:

```
#include <Stdlib.h>
#include <String.h>
#include <math.h>

 int gnInputNodes=0;
 int gnOutputNodes=0;

 int gnStepCount=0;

#define pi 3.14159265358979323846264433
float a=0,a1=0;
float b=0;
float d;
float q;
int t1=0;
float sin1[401];
double dref=0;
double qref=-12;

double ed[2];
double Idlimitmax=100;
double Idlimitmin=0;
double delted=0;
double Id=0;
double dkp=0.2;
double dki=0.0000;

double eq[2];
double Iqlimitmax=4995;
double Iqlimitmin=0;
double delteq=0;
double Iq=0;
double qkp;
double qki;
```

RunSimUser Fcn:

```
if(gnStepCount==250)
{

//90° lagging
   t1++;
   sin1[t1]=in[2];
   a=sin1[t1];
   if(t1>100)
     b=sin1[t1-100];
   else
     b=sin1[t1+300];
   if(t1>=400)
     t1=0;
     gnStepCount=0;

//dq
    d=a*cos(100*pi*t1/20000)+b*sin(100*pi*t1/20000);
   q=-a*sin(100*pi*t1/20000)+b*cos(100*pi*t1/20000);

//d control
ed[0]=dref-d;
delted=(dkp+dki)*ed[0]-dkp*ed[1];
ed[1]=ed[0];
Id=Id+delted;


//q control
qkp=dkp;
qki=dki;
eq[0]=qref-q;
delteq=(qkp+qki)*eq[0]-qkp*eq[1];
eq[1]=eq[0];
Iq=Iq+delteq;

a1=Id*cos(100*pi*t1/20000)-Iq*sin(100*pi*t1/20000);
if(t1>=0 && t1<=200 && a1>0.95)
a1=0.95;
if(t1>=0 && t1<=200 && a1<=0)
a1=0;
if(t1<=400 && t1>=200 && a1<=-0.95)
a1=-0.95;
if(t1<=400 && t1>=200 && a1>=0)
a1=0;
out[0]=a1;
}
```

Appendix C Hardware Platform Devices List

TABLE Appendix C Hardware Platform Devices

Component	Device	Main Features
MOSFET	IRF640NPbF	Drain-to-Source Breakdown Voltage V_{DSS}=200V Static Drain-to-Source On-Resistance $R_{DS(on)}$=0.15Ω Continuous Drain Current I_D=18A Gate-to-Source Voltage VGS=±20V
MOSFET Driver	MIC4422	9A-Peak Low-Side MOSFET Driver Supply Voltage V_s=20V Input Voltage V_{in} +0.3V to GND -5V Peak Output Current I_{out} 9A Peak
Diode	V20200G	Dual High Voltage Trench MOS Barrier Schottky Rectifier Trench MOS Schottky technology; Low forward voltage drop, low power losses; High efficiency operation; Low thermal resistance. $I_{F(AV)}$=2×10A V_{RRM}=200V V_F (at IF=10A)=0.71V
Capacitor	Metallized polyester film capacitor	Capacitance: 1.5μF, 4.7μF, 10μF, 22μF and so on Rated Voltage $U_{R,VDC}$=630V, $U_{R,\ VAC}$=220V
Current Sensor	ACS714	Optimized Range, I_p=±5A Sensitive, Sens(Typ)(mV/A)=185 Supply Voltage V_{CC}=8V Output Voltage V_{IOUT}=8V Overcurrent Transient Tolerance I_P=100A
Amplifier	MCP6022	Rail-to-Rail Input/Output Supply Voltage V_{DD}=8V Wide Bandwidth: 10 MHz (typical)

Appendix D Experiments Programs

All the following programs are coded in the dsPIC33FJ32GS606 16-Bit Digital Signal Controller with High-Speed PWM, ADC and Comparators.

D1. Isolated D2 dc/dc Simulation: Voltage and Current selection

D1.1 Variable/Function definitions:

```
#include "p33FJ64GS606.h"
#include "math.h"
#include <stdio.h>
#include <stdlib.h>
/* Configuration Bit Settings */
 FOSCSEL(FNOSC PRIPLL)              /*Primary Oscillator (XT, HS, EC) with PLL*/
 FOSC(FCKSM CSDCMD & OSCIOFNC ON)      /*Both Clock switching and Fail-safe Clock Monitor are disabled*//*OSC2 is general purpose digital I/O pin*/
 FWDT(FWDTEN OFF)                  /*Watchdog timer enabled/disabled by user software*/
 FPOR(FPWRT PWR128 )                /*POR Timer Value:128ms*/
 FICD(ICS PGD1 & JTAGEN OFF)         /*Communicate on PGC1/EMUC1 and PGD1/EMUD1*//*JTAG is disabled*/

void init PWM(void);
void Init ADC(void);

signed long an0,an1,an2,an3;
signed long Iref, IrefDiv=5,I;
signed long ek,ek1=0,uk,uk1=0;
long count=0,refDivCount=0;
```

D1.2 Main Function

```
int main()
{
/* Configure Oscillator to operate the device at 30Mhz,
      Fosc= Fin*M/(N1*N2), Fcy=Fosc/2,
      Fosc= 4*(60)/(2*2)=60Mhz , Fcy = 30Mhz. */
/* Configure PLL prescaler, PLL postscaler, PLL divisor */
    PLLFBD=58;              /* M = PLLFBD + 2 */
    CLKDIVbits.PLLPOST=0;   /* N1 = 2 */
    CLKDIVbits.PLLPRE=0;    /* N2 = 1 */

      builtin write OSCCONH(0x03);         /* New Oscillator/
      builtin write OSCCONL(0x00);         /* Enable Switch */

    while(OSCCONbits.COSC != 0b011);       /* Wait for new Oscillator to become /
    while(OSCCONbits.LOCK != 1);           /* Wait for Pll to Lock */

/* Now setup the ADC and PWM clock for 120MHz   ;  Fvco=Fin*M/N1 ;  Fvco=8*30/2=120MHz    */
    ACLKCONbits.ASRCSEL = 1;
    ACLKCONbits.FRCSEL = 0;
    ACLKCONbits.SELACLK = 1;               /*Fvco*/

    ACLKCONbits.APSTSCLR = 7;              /* Divide Auxiliary clock by 1 */
    ACLKCONbits.ENAPLL = 1;                /* Enable Auxiliary PLL */

    while(ACLKCONbits.APLLCK != 1);        /* Wait for Auxiliary PLL to Lock */

    init PWM();
    PTCONbits.PTEN  = 1;                // Enable the PWM Module

    TRISB=0x0000;
     PORTB=0xFFFF;

Init ADC();
TRISDbits.TRISD3 = 0;       //TEST signal output
LATDbits.LATD3=0;
while(1);

}
```

D1.3 High-frequency PWM Setting

```
void init PWM()
{
   PTPER = 10240;                  /* 40kHz PTPER*/

/* ~~~~~~~~~~~~~~~~~~~~~~~~ PWM Configuration ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ */
   PWMCON1bits.ITB = 0;       /* PHASEx/SPHASEx register provides time base period for this PWM generator*/
   PWMCON1bits.MDCS = 0;   /* MDC register provides duty cycle information for this PWM generator*/

   IOCON1bits.PENH = 1;        /* PWM1H is controlled by PWM module */
   IOCON1bits.PENL = 1;           /* PWM1L is controlled by PWM module */
   IOCON1bits.PMOD = 0;/* PWM I/O */

   PWMCON2bits.ITB = 0;       /* PHASEx/SPHASEx register provides time base period for this PWM generator*/
   PWMCON2bits.MDCS = 0;
   PWMCON2bits.DTC = 0;     //deadtime
   IOCON2bits.PENH = 1;        /* PWM2H is controlled by PWM module */
   IOCON2bits.PENL = 1;           /* PWM2L is controlled by PWM module */
   IOCON2bits.PMOD = 0;
   DTR2 = 50; /* Dead Time value is 100 ns */
   ALTDTR2 = 50;

   PWMCON3bits.ITB = 0;       /* PHASEx/SPHASEx register provides time base period for this PWM generator*/
   PWMCON3bits.MDCS = 0;
   PWMCON3bits.DTC = 0;
   IOCON3bits.PENH = 1;        /* PWM1H is controlled by PWM module */
   IOCON3bits.PENL = 1;           /* PWM1L is controlled by PWM module */
   IOCON3bits.PMOD = 0;
   DTR3 = 50; /* Dead Time value is 100 ns */
   ALTDTR3 = 50;

   PDC1 =5120;                  /* Initial Duty cycle 50% */
   PDC2 =5120;
   PDC3 = 6144;
// /* ~~~~~~~~~~~~~~~~~~~~~~~~ ADC Trigger Configuration ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ */
PWMCON4bits.ITB = 0;              //PTPER provides the PWM time.
   PWMCON4bits.MDCS = 0;
   PWMCON4bits.DTC = 0;
   IOCON4bits.PENH  = 1;              /* PWM1H is controlled by PWM module */
   IOCON4bits.PENL  = 1;              /* PWM1L is controlled by PWM module */
   IOCON4bits.PMOD  = 0;
   PDC4=5120;
  TRGCON4bits.TRGDIV = 1;       /* Trigger interrupt generated once every 2PWM cycle */
  TRGCON4bits.TRGSTRT = 0;      /* Trigger generated after waiting 0 PWM cycles */
PTCONbits.PTEN  = 1;
}
```

D1.4 ADC Setting

```
void Init ADC()
{
   ADCONbits.ADON=0;          //close ADC module
   ADCONbits.SLOWCLK = 1;              //  ACLK for time input       High Frequency Clock input
   ADCONbits.ADCS =1;                 // Clock divider selection =ACLK/2=32MHz
   ADCONbits.FORM = 0;                // Output in Integer Format
   ADCONbits.EIE = 0;                // Enable Early Interrupt
   ADCONbits.ORDER = 0;               // Normal Order of conversion
   ADCONbits.SEQSAMP = 1;              // Simultaneous sampling
   ADCONbits.ASYNCSAMP = 0;             // Asynchronous sampling
//   ADCONbits.SLOWCLK = 1;              // High Frequency Clock input PLL
//   ADCONbits.ADCS =0;                 // Clock divider selection  N=1 64M
   /* For simultaneus sampling total conversion time for one pair is 0.625us */
   ADSTAT = 0;                       /* Clear the ADSTAT register */

   ADCPC0bits.TRGSRC0 = 5;                  /* AN0 and AN1 triggered by PWM2 ????*/
   ADCPC0bits.IRQEN0 = 0;              /* Global ADC interrupt  requested */

   ADCPC0bits.TRGSRC1 = 5;             /* AN2 and AN3 triggered by PWM2 */
   ADCPC0bits.IRQEN1 = 1;

   ADPCFGbits.PCFG0 = 0;              /* AN0 is inverter current sense */
   ADPCFGbits.PCFG1 = 0;              /* AN1 is inverter voltage sense */
   ADPCFGbits.PCFG2 = 0;              /* AN2 is inverter current sense */
   ADPCFGbits.PCFG3 = 0;              /* AN3 is inverter voltage sense */

   TRISBbits.TRISB0=1;//??
   TRISBbits.TRISB1=1;
   TRISBbits.TRISB2=1;
   TRISBbits.TRISB3=1;


   IPC3bits.ADIP = 1;
   IFS0bits.ADIF = 0;                /* Clear AD Interrupt Flag */
   IEC0bits.ADIE = 1;                 /* Enable the ADC Interrupt at the start. */
   ADCONbits.ADON = 1;                  // Enable ADC module
}
```

D1.5 ADC Interrupt (Control Algorithm)

```
void  attribute  ((interrupt, no auto psv))  ADCInterrupt(void)
{


LATDbits.LATD3=~LATDbits.LATD3;

an0=ADCBUF0;
Iref=880; //1.5A*110=165, n=10 (2.79V/8.4225A)/(3.3/1024)=103
an1=ADCBUF1;
Vref=50; //10V*10

//current loop
 ek=Iref-an0;
 uk=uk1+50*(ek-ek1)+0.02*ek;
  Ek=Vref-an1;
  Uk=Uk1+13*(Ek-Ek1)+0.02*Ek;

 if(uk>5000) //5120*1024
    uk=5000;
 if(uk<512) //512*1024
    uk=512;

  //Voltage limit
 if(Uk>5000) //6144*1024
    Uk=5000;
 if(Uk<512) //512*1024
    Uk=512;

    Uk1=Uk;
    Ek1=Ek;

 if(Uk>uk)
 {
       duty=uk;

 }
 if(Uk<=uk)
 {
       duty=Uk;
   }

 PDC2=duty;

ADSTATbits.P0RDY = 0;
ADSTATbits.P1RDY = 0;
 IFS0bits.ADIF = 0;
}
```

D2. MPPT

The variable/Function definitions, main function, high-frequency PWM setting, and ADC setting are nearly the same, so only the control code is shown in the rest of the experiment programs.

```
void  attribute  ((interrupt, no auto psv))  ADCInterrupt(void)
{


LATDbits.LATD3=~LATDbits.LATD3;

an0=ADCBUF0;
an1=ADCBUF1;

// count++;
 ek=an0-an0_b;
 Ek=an1-an1_b;

   if(Ek==0)
   {
      if(ek>0)
         Vref+=17;          //left:plus 0.5 V
      if(ek<=0)
         Vref-=8;           //right:minus 0.25V
   }
   if(Ek!=0)
   {
      e=an0+an1*ek/Ek;
      if(e<=0)
        Vref-=8;           //right:minus 0.25V
      if(e>0)
        Vref+=17;          //left:plus 0.5V

   }
```

```
   an1_b=an1;
   an0_b=an0;

   if(Vref<200)
      Vref=200;      //10V input
   if(Vref>900)
      Vref=900;      //55V input

 //PI
   Ek1=Vref-an1;

   Uk=Uk1+2*Ek1+0.0001*(Ek1-Ek2);
   if(Uk<=500)    //
     Uk=500;

   if(Uk>=9000)//
     Uk=9000;

   Ek2=Ek1;
   Uk1=Uk;

   PDC2=Uk;
   PDC3=10*an1;
   PDC4=duty;
   PDC1=ek*10;

an2=ADCBUF2;
an3=ADCBUF3;

ADSTATbits.P0RDY = 0;
ADSTATbits.P1RDY = 0;
 IFS0bits.ADIF = 0;
}
```

D3. Super Capacitor Charge

```
void  attribute  ((interrupt, no auto psv))  ADCInterrupt(void)
{


LATDbits.LATD3=~LATDbits.LATD3;

 I=ADCBUF3;
 Vo=ADCBUF2;
 Vin=ADCBUF1;

 PDC3=Vo;

 if(Vo>=450)
 {
    PI lock=1;
    //PID Vo();
    PDC2=0;
 }
 if(Vo<450&&PI lock==1)
 {
    PDC2=0;
 }

 if(Vo<450&&PI lock==0)
 {

EK3=Vin-Vinref;
UK3=UK3 1+kp vin*(EK3-EK3 1)+ki vin*EK3;

  if(UK3<50)
    UK3=50;
  if(UK3>1000)
    UK3=1000;

   UK3 1=UK3;

   EK3 1=EK3;
 E=UK3;
```

```
//PID I();
  EK1=E-I;

  UK1=UK1 1+kp iin*(UK1-UK1 1)+ki iin*UK1;

if(UK1<500)
      UK1=500;
   if(UK1>6000)
      UK1=6000;


    UK1 1=UK1;
    EK1 1=EK1;

PID Vo();



if(UK1<=UK2)
{
  PDC1=UK1;
  PDC2=UK1;
}
if(UK1>UK2)
{
 PDC1=UK2;
 PDC2=UK2;

}
  }
ADSTATbits.P0RDY = 0;
ADSTATbits.P1RDY = 0;
 IFS0bits.ADIF = 0;
}
```

D4. IPOS

```
void    attribute   ((interrupt, no auto psv))   ADCInterrupt(void)
{


LATDbits.LATD3=~LATDbits.LATD3;

an0=ADCBUF0;
Iref=828; //1.5A*110=165, n=10 (2.79V/8.4225A)/(3.3/1024)=103

an1=ADCBUF1;
an2=ADCBUF2;
Vref=30;
Vref1=80;

Ek=Vref-an1;
Uk=Uk1+150*(Ek-Ek1)+0.001*Ek;
Uk1=Uk;
Ek1=Ek;

if(Uk>6000)
       Uk=6000; //0.95
if(Uk<512)
       Uk=512;          //0.05


ek=Vref1-an2;
uk=uk1+49.5*(ek-ek1)+0.012*ek;
uk1=uk;
ek1=ek;

if(uk>6000)
     uk=6000;
if(uk<512)
     uk=512;

   PDC2=4000;
   PDC3=uk;

   PDC4=duty;
   PDC1=an1;

ADSTATbits.P0RDY = 0;
ADSTATbits.P1RDY = 0;
 IFS0bits.ADIF = 0;
}
```

D5. Interleaved Isolated D2

```
void  attribute  ((interrupt, no auto psv))  ADCInterrupt(void)
{


LATDbits.LATD3=~LATDbits.LATD3;

an0=ADCBUF0;
Iref=828;
an1=ADCBUF1;
Vref=70;


//current loop
 ek=Iref-an0;

 uk=uk1+15*(ek-ek1)+0.02*ek;

 if(uk>5000) //5120*1024
    uk=5000;
 if(uk<512) //512*1024
    uk=512;


    ek1=ek;
    uk1=uk;

    PDC2=uk;   //4020;
    PDC3=uk;
    PDC4=duty;
    PDC1=ek*10;

an2=ADCBUF2;
an3=ADCBUF3;

ADSTATbits.P0RDY = 0;
ADSTATbits.P1RDY = 0;
 IFS0bits.ADIF = 0;
}
```

D6. Interleaved Isolated D2 PFC

```
void  attribute  ((interrupt, no auto psv))  ADCInterrupt(void)
{


LATDbits.LATD3=~LATDbits.LATD3;

an0=ADCBUF0;//i1
an2=ADCBUF2;//uin


Iref=an2;
Ek=Iref-an0;
Uk=Uk1+38.57*(Ek-Ek1)+0.0003205*Ek;
Ek1=Ek;
Uk1=Uk;

if(Uk>5000)
       Uk=5000; //0.95
if(Uk<512)
       Uk=512;          //0.05

PDC2=Uk;
PDC3=Uk;


ADSTATbits.P0RDY = 0;
ADSTATbits.P1RDY = 0;
 IFS0bits.ADIF = 0;
}
```

D7. Single-phase Isolated D2 PFC

```
void  attribute  ((interrupt, no auto psv))  ADCInterrupt(void)
{

LATDbits.LATD3=~LATDbits.LATD3;

an0=ADCBUF0;//I
an1=ADCBUF1;//U
Iref=an1;

Ek=Iref-an0;
Uk=Uk1+36.25*(Ek-Ek1)+0.00001*Ek;
Uk1=Uk;
Ek1=Ek;

if(Uk>5000)
      Uk=5000; //0.95
if(Uk<512)
      Uk=512;          //0.05

PDC3=Uk;


ADSTATbits.P0RDY = 0;
ADSTATbits.P1RDY = 0;
 IFS0bits.ADIF = 0;
}
```

D8. Bridgeless Isolated D2 PFC

```
void  attribute  ((interrupt, no auto psv))  ADCInterrupt(void)
{


LATDbits.LATD3=~LATDbits.LATD3;

//I
an0=ADCBUF0;//1
an1=ADCBUF1;//2
//U
an2=ADCBUF2;//1

//1
if(an2>776)
{
   Iref1=an2-776;
ek=Iref1-an0;
uk=uk1+2*(ek-ek1)+0.001*ek;
uk1=uk;
ek1=ek;

if(uk>5000)
      uk=5000;  //0.95
if(uk<512)
      uk=512;          //0.05


Iref2=0;
Ek=Iref2-an1;
Uk=Uk1+2*(Ek-Ek1)+0.001*Ek;
Uk1=Uk;
Ek1=Ek;

if(Uk>5000)
      Uk=5000; //0.95
if(Uk<512)
      Uk=512;          //0.05

//PHASE2=-1*uk;
PDC2=uk;
PDC3=Uk;

}
```

```
//2
else{


   Iref2=776-an2;
Ek=Iref2-an1;
Uk=Uk1+2*(Ek-Ek1)+0.001*Ek;
Uk1=Uk;
Ek1=Ek;

if(Uk>5000)
      Uk=5000; //0.95
if(Uk<512)
      Uk=512;          //0.05


   Iref1=0;
ek=Iref1-an0;
uk=uk1+2*(ek-ek1)+0.001*ek;
uk1=uk;
ek1=ek;

if(uk>5000)
      uk=5000;  //0.95
if(uk<512)
      uk=512;          //0.05

//PHASE2=-1*uk;
PDC2=uk;
PDC3=Uk;
}



ADSTATbits.P0RDY = 0;
ADSTATbits.P1RDY = 0;
 IFS0bits.ADIF = 0;
}
```

D9. Single-phase Inversion

D9.1 Sine Table

```
const unsigned int sintable[]={32767,33282,33796,34311,34824,35338,35851,36363,36874,37384,37893,38401,38907,39412,39915,40416,40916,41413,41909,42402,42893,43381,43866,44349,44829,
45306,45780,46251,46719,47182,47643,48100,48553,49002,49447,49888,50324,50757,51185,51608,52027,52441,52850,53254,53653,54047,54436,54820,55198,55570,55937,56298,56653,57002,57346,
57683,58014,58339,58658,58970,59276,59575,59868,60154,60433,60705,60971,61229,61481,61725,61963,62193,62415,62631,62839,63040,63233,63419,63597,63767,63930,64085,64233,64373,64505,
64629,64745,64853,64954,65046,65131,65207,65276,65336,65389,65433,65469,65498,65518,65530,65534,65530,65518,65498,65469,65433,65389,65336,65276,65207,65131,65046 ,64954,64853,64745,
64629,64505,64373,64233,64085,63930,63767,63597,63419,63233,63040,62839,62631,62415,62193,61963,61725,61481,61229,60971,60705,60433,60154,59868,59575,59276,58970,58658,58339,58014,
57683,57346,57002,56653,56298,55937,55570,55198,54820,54436,54047,53653,53254,52850,52441,52027,51608,51185,50757,50324,49888,49447,49002,48553,48100,47643,47182,46719,46251,45780,
45306,44829,44349,43866,43381,42893,42402,41909,41413,40916,40416,39915,39412,38907,38401,37893,37384,36874,36363,35851,35338,34824,34311,33796,33282,32767,32252,31738,31223,30710,30196,29683,29171,28660,28150,2764
1,27133,
26627,26122,25619,25118,24618,24121,23625,23132,22641,22153,21668,21185,20705,20228,19754,19283,18815,18352,17891,17434,16981,16532,16087,15646,15210,14777,14349,13926,13507,13093,
12684,12280,11881,11487,11098,10714,10336,9964,9597,9236,8881,8532,8188,7851,7520,7195,6876,6564,6258,5959,5666,5380,5101,4829,4563,4305,4053,3809,3571,3341,3119,2903,2695,2494,2301,
2115,1937,1767,1604,1449,1301,1161,1029,905,789,681,580,488,403,327,258,198,145,101,65,36,16,4,0,4,16,36,65,101,145,198,258,327,403,488,580,681,789,905,1029,1161,1301,1449,1604,1767,
1937,2115,2301,2494,2695,2903,3119,3341,3571,3809,4053,4305,4563,4829,5101,5380,5666,5959,6258,6564,6876,7195,7520,7851,8188,8532,8881,9236,9597,9964,10336,10714,11098,11487,11881,12280,
12684,13093,13507,13926,14349,14777,15210,15646,16087,16532,16981,17434,17891,18352,18815,19283,19754,20228,20705,21185,21668,22153,22641,23132,23625,24121,24618,25118,25619,26122,26627,
27133,27641,28150,28660,29171,29683,30196,30710,31223,31738,32252,32767};//400
```

D9.2 Inversion Control

```
void    attribute   ((interrupt, no auto psv))  ADCInterrupt(void)//40khz
{



   ADSTATbits.P0RDY = 0;           /* Clear ADC pair ready bit */
   ADSTATbits.P1RDY = 0;
   IFS0bits.ADIF = 0;

 if(t==400)  t=0;
 an0=ADCBUF0;
 sin1[t]=an0;
 a=sin1[t]>>8;

if(t>=100 && t<400)
  b=sin1[t-100]>>8;
if(t<100 && t>=0)
 b=sin1[t+300]>>8;

//dq

if(t<300 && t>=0)
   {
   d=a*(sintable[t+100]-32767)>>8+b*(sintable[t]-32767)>>8;
    q=-a*(sintable[t]-32767)>>8+b*(sintable[t+100]-32767)>>8;
}

if(t>=300 && t<400)
   {
   d=a*(sintable[t-300]-32767)>>8+b*(sintable[t]-32767)>>8;
    q=-a*(sintable[t]-32767)>>8+b*(sintable[t-300]-32767)>>8;
}

//d control
ekd 0=d ref-d;
ukd 0=ukd 1+0.18*ekd 0-0*(ekd 0-ekd 1);
ekd 1=ekd 0;
ukd 1=ukd 0;
```

```
if(t<300 && t>=0)
{
   a1=ukd 1*(sintable[t+100]-32767)>>10-ukq 1*(sintable[t]-32767)>>10;
}
if(t>=300 && t<400)
{
   a1=ukd 1*(sintable[t-300]-32767)>>10-ukq 1*(sintable[t]-32767)>>10;
}
a1=a1>>2;
 PDC6=a1;


if(t<195 && t>=5)
{PDC1=12792;
 PDC2=0;
}
if(t>195 && t<205)
   {PDC1=0;
 PDC2=0;
}
if(t<395 && t>=205)
{
 PDC1=0;
 PDC2=12792;
}
 if(t<400 && t>=395)
{
 PDC1=0;
 PDC2=0;
}
t++;

}
```

Appendix E List of Figures and Tables

E.1 List of Figures

E.2 List of Tables

Appendix F List of Author's Publications

Conference Papers

Jieyun Wang, Wei Jiang, Tianyang Wang, Xiao He, "Wireless Super-capacitor Charger for Linear Motion Transportation," *3rd International Conference on Mechanical, Electrical and Medical Intelligent System* 2019.

Jieyun Wang, Wei Jiang, Barry W. Williams, Seji Hashimoto, "Simulation Research on Three-Phase Isolation Energy Storage Converter for Electric Vehicle", Technology and Social Science 2020.

J. Wang, W. Jiang and B. W. Williams, "Battery Energy Storage Converter for Shipboard Energy Magazine System," *2021 4th IEEE International Conference on Industrial Cyber-Physical Systems (ICPS)*, Victoria, BC, Canada, 2021

Journal Papers

Jieyun Wang, Wei Jiang, Xiangyu Qin and Barry W. Williams. "Design and implementation of a novel isolated D2 dc to dc converter," (under review, related to the thesis work)

Wang, Jieyun, Wei Jiang, Shuren Wang, Jingying Lu, Barry W. Williams, and Qianlong Wang. "A Novel Step Current Excitation Control Method to Reduce the Torque Ripple of Outer-Rotor Switched Reluctance Motors," *Energies* 15, 2022.

Pan, Sisi, Wei Jiang, Ming Li, Hua Geng, and **Jieyun Wang**. "Evaluation of the Communication Delay in a Hybrid Real-Time Simulator for Weak Grids" *Energies* 15, 2022.