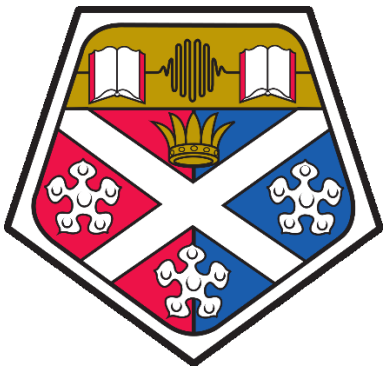

University of Strathclyde

Department of Electronic and Electrical Engineering

High-Voltage Pulse Generators Incorporating Modular Multilevel Converter Sub-Modules

by

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B.Sc. (*first class honors*), M.Sc.

A thesis presented in fulfilment of the requirements for the degree of Doctor of Philosophy

2018

This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of any degree.

Signed: *M. Atef* Date: 10/06/2018

"Over every possessor of knowledge is one [more] knowing"

[Qur-ān, Yusuf 12:76]

"Everything Should Be Made as Simple as Possible, But Not Simpler"

[Albert Einstein]

Dedication

To the ancestors who paved the path before me upon whose shoulders I stand.

To the successors who will benefit from this work.

Acknowledgements

All praise is due to ***Allah***, whose praise cannot be described by those who speak, whose blessings cannot be enumerated by those who count.

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M. Atef

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List of Symbols

C_{SM}	MMC sub-module capacitance	F
C_{Arm}	Arm equivalent capacitance	F
E_L	Energy transferred to load during pulse	J
E_{SM}	SM capacitor energy	J
E_{Arm}	Arm equivalent capacitor energy	J
E_r	Energy dissipated during SM capacitor charging	J
E_s	Energy supplied by the input source during SM capacitor charging	J
D	Converter's duty ratio	J
f_s	Pulse repetition frequency	Hz
i	SM capacitor charging current	A
i_s	HV DC supply input current	A
i_o	Output load current.	A
i_L	Input inductor energising current	A
i_{Arm}	Arm current	A
I_L	Input inductor maximum energising current	A
I_P	Output peak pulse current	A
I_s	Average supply current	A
I_x	SM capacitor peak charging current	A
I_y	SM capacitor peak discharging current	A
I_o	RMS output current	A
L_a	Arm inductance	H
L_s	Input HV DC supply inductance	H
L_i	Input LV DC supply inductance.	H
m	Number of bypassed SMs/arm during multipulse waveform generation	
N	Number of SMs per arm	
n	Transformer turns ratio	
P_L	Load pulse power.	W
r	Inductor internal resistance	Ω
R_L, R	Load Resistance	Ω
T_s, t_s	Pulse repetition time	s
T_Q	PWM carrier repetition time	s
t_p	Positive polarity pulse duration	s
t_n	Negative polarity pulse duration	s
t_{pz}	Positive polarity null load voltage duration	s
t_{nz}	Negative polarity null load voltage duration	s
t_{pl}	Pulse duration	s
t_x	Step voltage-level applying time	s
t_m	pulse plateau time	s
t_L	Inductor energising time	s
t_c	SM capacitor charging time	s
V_s,V_{in}	HV/LV DC input supply voltage	V
V_{SM}	Charged SM capacitor voltage	V

v_P	Output pulse voltage	V
V_P	Output pulse peak-voltage	V
V_p	Positive pulse peak-voltage	V
V_n	Negative pulse peak-voltage	V
V_o	SM capacitor voltage after contributing to pulse generation	V
V_α	SM capacitor voltage drop after contributing to pulse generation	V
γ	Percent SM capacitor voltage ripple	
α	Safety factor, damping factor	
β	Per unit SM capacitor remaining voltage	
δ	Pulse duty ratio	
λ	Voltage boosting ratio	

List of Abbreviations

AC	Alternating current
BMPG	Voltage boost mode pulse generator
BPG	Voltage-boost capability pulse generator
CPG	Clamping pulse generator
DC	Direct current
FB	Full bridge
GPG	Generic pulse waveform generator
HB	Half bridge
HV	High voltage
HVDC	High voltage direct current
IPG	Isolated dc input sources based pulse generator
IGBT	Insulated gate bipolar transistor
MMC	Modular multilevel converter
NLV	Null load voltage
NLC	Nearest level control
PEF	Pulsed electric field
PG	Pulse generator
PI	Proportional integral
PWM	Pulse width modulation
SM	Sub module
SPG	Sequentially charged pulse generator
SMPS	Switched mode power supply
SUPG	Voltage step-up pulse generator
TSPG	Transform based pulse generator with sequentially charged SMs
UPG	Universal pulse waveform generator

Abstract

Recent research established the effectiveness of applying a pulsed electric field to deactivate harmful microorganisms (such as bacteria and E. coli). Successful deactivation is achieved by lethal electroporation; a process that produces electric pores in the biological cell membrane of the harmful microorganisms when subjected to high-voltage (HV) pulses. The HV pulses are designed to create pores beyond a critical size at which the biological cell can reseal. In contrast when applying non-lethal electroporation, the cell-membrane survives after the electroporation process. This is required, for example, when inserting protein cells in the cell-membrane. In both lethal and non-lethal electroporation, HV pulses in the kilo-Volt range (1-100 kV) with durations ranging between nanoseconds and milliseconds are required.

This thesis proposes nine pulse generator (PG) topologies based on power electronic devices and modular multilevel converter sub-modules. The proposed topologies are divided into two main groups namely: PGs fed from a HV DC supply and PGs fed from an LV DC supply. The first group presents a new family of HV DC fed topologies that improve the performance of existing HV DC fed PGs, such as flexible pulse-waveform generation and full utilisation of the DC link voltage. The second group is dedicated to a new family of LV DC fed PG topologies which have flexible pulse-waveform generation, controlled operation efficiency, and high voltage gain.

All the proposed PG topologies share the important aspect in the newly developed HV PGs, that is modularity, which offers redundancy and robust pulse generation operation.

The presented PG topologies are supported by theoretical analysis, simulations, and experimentation.

Contents

Chapter 1

Introduction

This chapter explores the concept, the process and the applications of electroporation. Electroporation pulse generator load modelling and essential background for the following chapters are highlighted. Subsequent thesis chapters are dedicated to high voltage pulse generators.

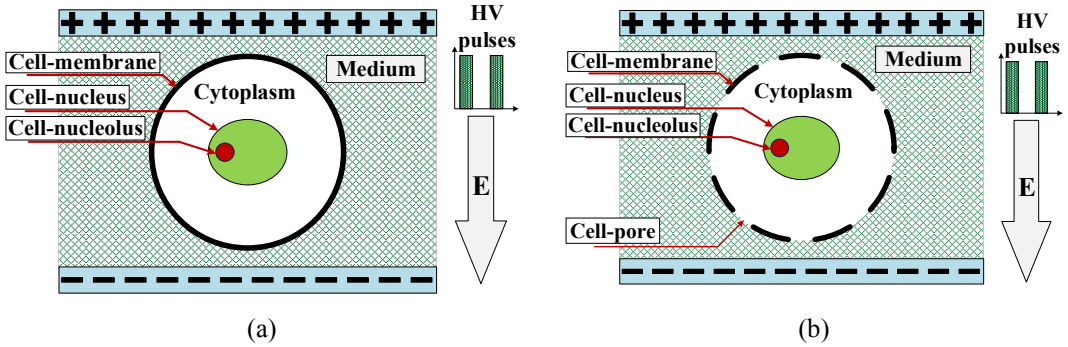
1.1 The Electroporation Process

Electroporation is the process where a biological cell-membrane is subjected to high electric field strength via a train of sufficiently high-voltage (HV) pulses [1]. The applied pulsed electric field (PEF) produces micropores in the cell-membrane as shown in Fig.1.1. In Fig.1.1, a schematic representation of a cell-membrane in a medium is depicted. At the beginning of the electroporation process, Fig.1.1a, the cell is intact, however, after sufficient time of PEF application the pores start to appear in the cell-membrane as shown in Fig.1.1b [1]-[4].

There are two types of electroporation, namely: reversible (or, non-lethal) and irreversible (or, lethal). In reversible electroporation, the cell-membrane survives after the electroporation process and reseals its pores [5]. In contrast, irreversible electroporation is lethal, as the cell-membrane dies [5]. For each cell-membrane, there is a critical electric field E_{cr}, beyond which the cell-membrane cannot reseal if the applied electric field $E > E_{cr}$. Depending on the biological cell characteristics, a suitable PEF can be applied for the suitable electroporation type [6].

In order to create an electric field across the treatment chamber for electroporation, a high voltage for sufficient time should be applied. Recent research confirms the effectiveness of applying HV-pulses in the kilo-volt range (1-100kV) with pulse duration ranges between nanoseconds and milliseconds [7]. Generally, the higher the voltage, the shorter the necessary pulse duration. Then both the energy efficiency and the electroporation criteria are met. Therefore a low power long-time input is used to

provide high-power short-time pulses through power conversion stage for electroporation, as illustrated in Fig.1.2 [8].



(a) (b)

Fig.1.1. Effect of electroporation on a biological cell-membrane. (a) At the beginning of electroporation. (b) After electroporation.

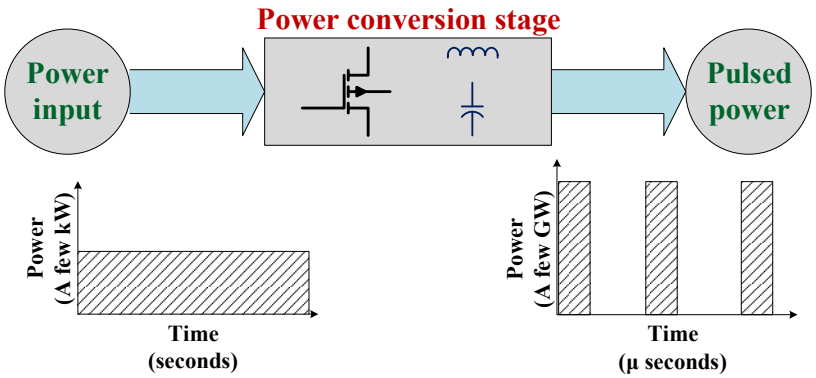


Fig.1.2. Pulsed power energy concept.

1.2 Electroporation Applications

Several applications can benefit from the electroporation process in its lethal and non-lethal forms [9]-[14]. Generating electroporation pulses is primarily controlled by the applied HV across the cell-membrane, pulse-waveform shape, and pulse application time. Therefore, there is a wide range of pulses, where a specific pulse suites a specific application.

1.2.1 Lethal Electroporation Applications

Lethal electroporation targets the deactivation of any parasites, bacteria, and viruses. Two applications are:

- ***Water treatment***: In water treatment, disinfection is a crucial step before piping water to homes and businesses, where a disinfectant (for example, chlorine or chloramine) is added to the water. Alternatively, disinfection can be achieved by applying lethal electroporation to the water [10].
- ***Food Sterilization***: Thermal treatments are used in the food industry for preservation, but with adverse effects on food nutritional values. Therefore, applying PEF with a suitable waveform can preserve food nutritional values and eliminate bacteria and microbes [11].

1.2.2 Non-Lethal Electroporation Applications

Applying non-lethal PEF is required when keeping the biological cell alive, for ecological or treatment reasons. The two examples are:

- ***Bio-fouling prevention***: The bio-fouling phenomenon is evident in water-cooling systems, where an uncontrolled growth of aquatic nuisance species (such as algae, barnacles and Zebra mussels) may clog pipes. For ecological purposes, non-lethal electroporation can be used to prevent bio-fouling. Stunning action can be applied with electrodes placed at the intake of untreated water system and repetitive electrical pulses are applied such that each volume of water that passes between the electrodes is exposed at least once to the electric field [12].
- ***Medical treatment***: Molecular therapies require that the effective drug reaches target cells. This can be achieved by several delivery methods such as injections, inhalations, or creams. The drug agent is more effective when entering the targeted cells, and the cell-membrane is the primary barrier against entry. Non-lethal electroporation creates pores in the cell-membrane which can be utilised for drug insertion [13]-[14].

1.2.3 Pulse Waveform Shapes

Among the wide range of possible HV pulse-waveforms for electroporation; rectangular, exponential, combined narrow and wide pulse duration (or, multipulse) and ramp pulses are commonly used [15], shown in Fig.1.3. The rectangular pulse waveform in Fig.1.3a is the most common pulse waveform due to its effective pulse area compared with the exponential pulse waveform shown in Fig.1.3b.

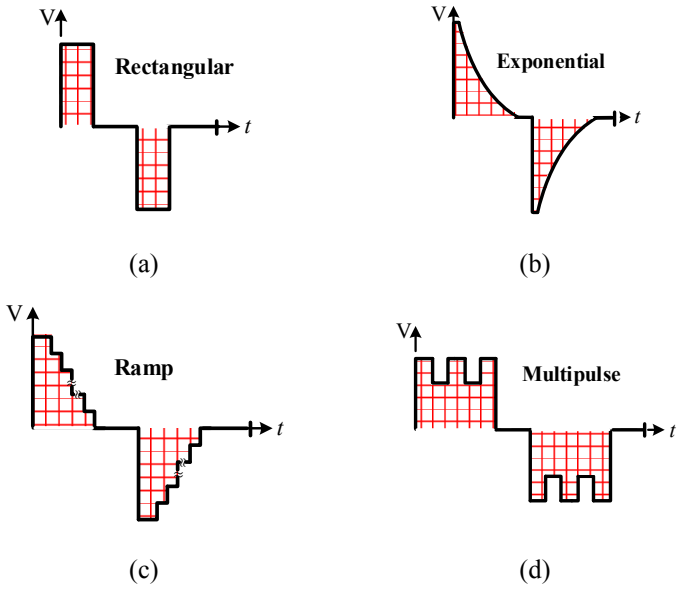


Fig.1.3. Common pulse waveforms in PEF applications.
(a) Rectangular. (b) Exponential. (c) Ramp. (d) Multipulse.

Normally, the exponential waveform is created across the load due to the nature of classical pulse generators (PGs), which is formed of an RC network. With proper selection of RC values, the exponential waveform plateau, rise and tail times are controlled. In recent PGs, exponential waveform characteristics (rise, plateau and tail times) can be imitated by ramping waveforms, shown in Fig.1.3c. Multipulse waveform, shown in Fig.1.3d, formed of wide-pulses combined with a train of narrow pulses is preferred in food sterilization applications in order to minimize the amount of heat generated during electroporation, without altering the food nutrition value [16]-[18].

The HV pulses can be either unipolar or bipolar. Bipolar pulses are advantageous in terms of subjecting the microorganisms under treatment to reversing mechanical stresses in addition to the electrical stresses which expedite the electroporation process [19].

1.3 Electroporation Load Modelling

In order to model the PG load, a breakdown of the treatment chamber elements is essential. As depicted in Fig.1.1, a treatment chamber contains a medium and at least a biological cell. The medium can be described by resistance R_s and a capacitance

C_s which are linearly related to the resistivity of the medium and its dielectric constant, respectively [6]. The biological cell is formed of three substructures, namely: the cell-membrane, the cytoplasm, and the nucleus. Taking the cell substructures into account, the cell interior can be modelled as resistors (R_{c1} and R_{c2}) and the membranes surrounding the cell, modelled as capacitors, C_m. Both elements are in series to resistance describing the cytoplasm outside the nucleus, which again can be modelled by resistor R_n and its surrounding membrane by capacitors C_n [6]. Fig.1.4 shows the detailed electrical model of a biological cell under treatment [6].

Basically, the sample under treatment, along with the medium, are modelled by resistance and capacitance. But its modelling is dependent on the applied PEF duration. For pulse durations comparable to the dielectric relaxation time (which is typically in nanosecond order) of the medium, the capacitive component of the impedance can be neglected [20]. For the assessment of the proposed PGs, the load is described by resistance, since the targeted range of pulse durations is microseconds and longer.

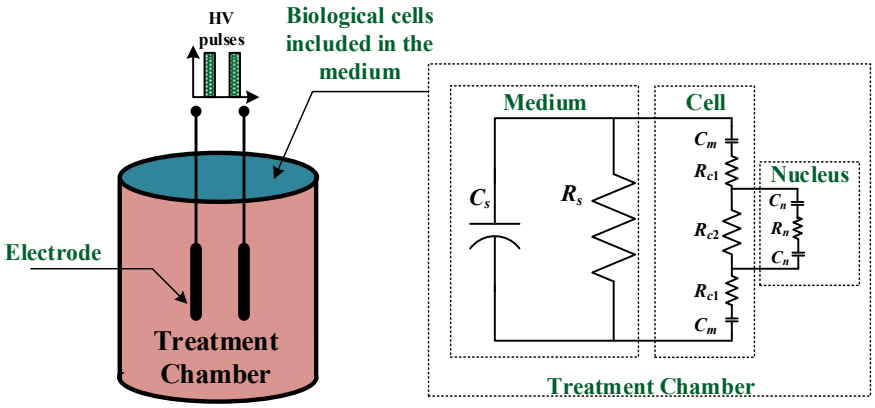


Fig.1.4. Electrical modelling of a biological cell in a medium.

1.4 Research Motivation and Objectives

PEF applications are well-established, where classical methods of HV pulse generation dominate. In classical PGs, charging a group of capacitors in parallel, then discharging them in series, provides the HV pulses between the connection terminals. These PGs are bulky, inflexible, and inefficient. The main generated pulse waveform is either exponential or rectangular and unipolar.

The research in this thesis exploits the evolution of power electronic switches, with their high voltage withstand capability and fast on/off switching operation, to introduce a new family of PGs suitable for electroporation. The main objectives of this thesis are:

- Present scalable, modular, redundant and flexible PGs with a reduced footprint.
- Provide a detailed description of the proposed PG topologies.
- Propose PGs, which can either be fed from an existing HV DC input, or from an LV DC input.
- Establish a generic pulse wave generation methodology suitable for wide ranging pulse generation applications.
- Compare the proposed PGs with state-of-the-art solid-state based PGs and highlight key features and limitations.
- Provide conclusions and recommendations for future extension of the research undertaken in this thesis.

Chapter 2

Review of High-Voltage Pulse Generators

Marx generators, pulse forming networks, and Blumlein lines are commonly used classical high-voltage (HV) pulse generators (PGs). With ongoing HV semi-conductor switch development (silicon and silicon carbide), mainly increased voltage rating and higher switching frequency capability, it is possible to generate HV pulses with power electronics-based converters. This chapter reviews classical PGs and newly developed power electronics based-PGs for electroporation applications.

2.1 Classical High-Voltage Pulse Generators

Classical PGs are mainly based on charging a group of capacitors in parallel then discharging them in series so that a high voltage pulse is developed across the connected load.

2.1.1 Marx Generator

The basic Marx generator was invented by Erwin Marx in 1923. As illustrated in Fig.2.1 it is comprised of a group of N capacitors, C, which are charged in parallel from the input supply V_s through the charging resistor r_c. The switching action takes place with the help of the spark gaps between stages, which have a break down voltage slightly higher than V_s. The HV pulse is formed when cascaded voltage break down of the spark gaps results when connecting the charged capacitors in series [21]-[23]. In order for cascade break down, the first spark gap is intentionally triggered, exposing $2V_s$ voltage across the second spark gap forcing it to conduct. The process continues until all the spark gaps are shorted, hence a voltage pulse of NV_s is impressed across load R.

The basic Marx PG generates unipolar pulses. If bipolar pulses are required, another similar stack fed from $-V_s$ is used and the load is connected differentially between the two stack outputs [24]-[25]. The charging resistors are the control

element in the Marx generator, if faster and shorter pulses are required, the charging resistances are reduced.

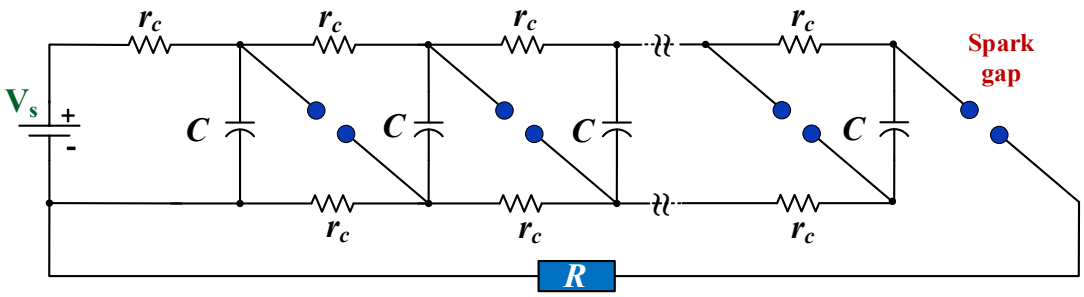


Fig.2.1. Classical Marx generator.

2.1.2 Pulse Forming Network

The nature of the generated HV pulse in a Marx generator is exponential. If near rectangular pulses are required, pulse forming network (PFN) can be used. The PFN is formed of N cascaded LC sections, as illustrated in Fig.2.2, connected to an input voltage source V_s. After storing the energy in the LC branches, an HV switch is closed across the load after disconnecting the input supply, such that the required pulse voltage is delivered [26]-[29].

A PFN mimics lossless transmission lines (TLs), thus the network impedance is

$$Z_o = \sqrt{L/C} \tag{2.1}$$

where Z_o is the PFN characteristic impedance. The pulse duration is calculated from

$$t_p = 2N\sqrt{LC} \tag{2.2}$$

where t_p is the generated pulse duration.

The PFN has the advantage of a simple structure and the ability to generate a near rectangular waveform. The main limitations are the limited pulse width range, (LC value adjustment is required when different pulse characteristics are needed) and the generated pulse peak is half the input supply due to a load matching requirement ($R = |Z_o|$). In order to increase the pulse peak voltage, the PFN can be of several cascade stages in conjunction with a Marx generator [30]-[31]. The pulse edges can be sharpened by allowing the cored inductor component to saturate.

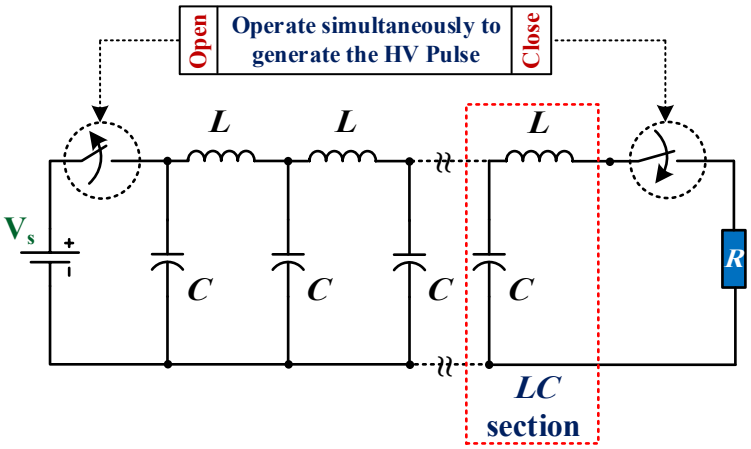


Fig.2.2. Classical PFN layout.

Similar to PFNs, TLs can be used to generate HV pulses, depending on their inherent distributed LC parameters [32]-[34]. However, for near rectangular pulses, load impedance matching is required, hence, the maximum pulse voltage is half the input voltage. A solution for pulse peak voltages equal to the input voltage was provided by Alan Blumlein in 1937. The load is connected in series between two TLs, which are energised by an input voltage at one end. For proper Blumlein line operation, both TLs must be identical and the load impedance must equal twice the characteristic impedance of one line ($R = 2Z_o$) [35]-[37].

2.2 Power Electronics-Based HV Pulse Generators

With the evolution of power electronic switches, with high voltage withstand and fast on/off switching operation, numerous solid-state based HV pulse generators have been proposed. The fast on/off switching of the power electronic switches allows fast charging of the utilised capacitors and narrow output HV pulse generation. Examples of power electronics-based PGs vary from mimicking the classical generators, such as the Marx generator, to emerging new topologies and converters.

An important aspect in the newly developed HV PGs is modularity, which offers redundancy, scalability and robust pulse generation operation. A group of the newly emerged PG topologies exploited the inherent modularity of multilevel converter sub-modules (SMs).

Generally, the power electronics-based PGs can be collated into three main groups, namely: Non modular multilevel converter (MMC) based, MMC-based, and hybrid

topologies. MMC-based refers to topologies that adopt existing MMC phase-legs used in HVDC transmission applications, to HV pulse generation. The hybrid term refers to PGs that incorporate the MMC SMs as a stage of pulse generation within the topology. A comparison between the main features and limitations of the three groups is given in Table 2.1. Generally, MMC-based topologies are fed from an HV DC input whereas the hybrid, and the non MMC-based are fed from a low voltage DC input.

Table 2.1: General Features Comparison of Pulse Generator Topology Groups

Attribute	Non MMC-based	MMC-based	Hybrid
Examples	[38]-[54]	[61]-[63]	[64]-[68]
Features	* No voltage sensors[1] * Simple control * Small footprint[2] * LV DC supply fed	* Scalable * Modular * Redundant * Reduced semiconductor ratings * Generate different pulse waveforms	* MMC modules are connected across the load to form the pulses * No HV switches for HV DC chopping * Moderate footprint * LV DC supply fed
Limitations	* Parameter change sensitivity * Lacks modularity *HV switches * Generated pulses mainly rectangular * Inflexible pulse characterizations	* HV DC supply fed * Essential SM capacitor voltage balancing *Large footprint * Possibly complicated control with sensorless operation	* Different pulse waveforms if SM capacitors are charged independently, otherwise drift in HV levels *Sensors to avoid capacitor voltage drift
[1]Under open loop conditions. [2]In comparison with MMC based PGs.			

2.2.1 Non MMC-Based PG Topologies

The basic approach of non MMC-based PG topologies is to find a way to step up the voltage, thereafter, an HV switch in series with the load chops the HV. The HV switch is normally switched OFF, and is switched ON during pulse generation, as shown in Fig.2.3. As a result, series connection of semiconductor devices is inevitable, which represents the main drawback of such topologies.

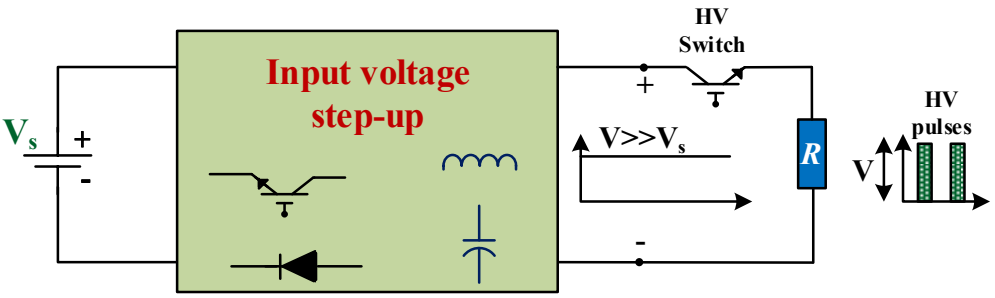


Fig.2.3. Basic concept of non MMC based pulse generators.

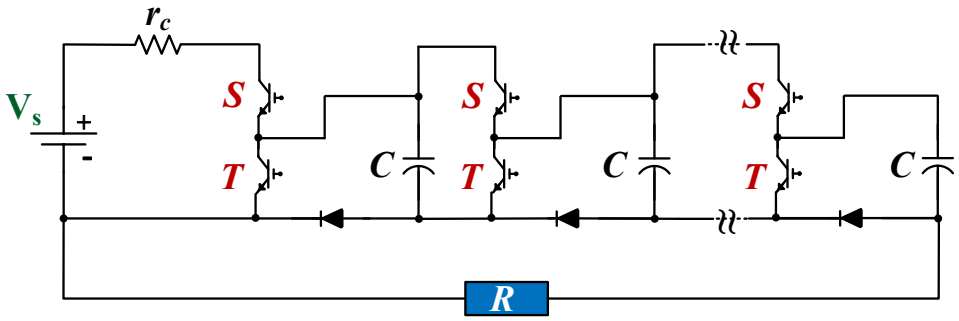


Fig.2.4. Solid-state based Marx generator.

A. Solid-state Marx Generator

Mimicking the classical Marx generator, the solid-state Marx generator has been extensively studied [38]-[42]. The core idea is to replace the spark gaps, shown in Fig.2.1, with power electronic switches such as insulated gate bipolar transistors (IGBTs), as illustrated in Fig.2.4.

A controllable charging/discharging mechanism of the capacitors is obtained, such that switches S allow charging of the capacitors while switches T allow pulse generation across the load. The original topology generates unipolar rectangular pulses, however, in [41], an H-bridge around each capacitor allows bipolar pulse generation. In [42], bipolar pulse generation is achieved by charging two capacitor groups from two DC sources, such that each group is charged to the same voltage but with reverse polarity.

Solid-state Marx PGs have a simple structure, but careful IGBT selection is essential. For example, in Fig.2.4, IGBT ratings are not identical as the current stresses of S switches closer to V_s are higher due to parallel capacitor charging.

B. Switched-Mode Power Supply-Based PGs

Utilising basic switched-mode power supply (SMPS) circuits in HV pulse generation topologies [43]-[51] has been researched. Particular attention has been given to boost, buck-boost and the isolated buck-boost (or the flyback) SMPS circuits, shown in Fig.2.5, due to their voltage step-up capabilities.

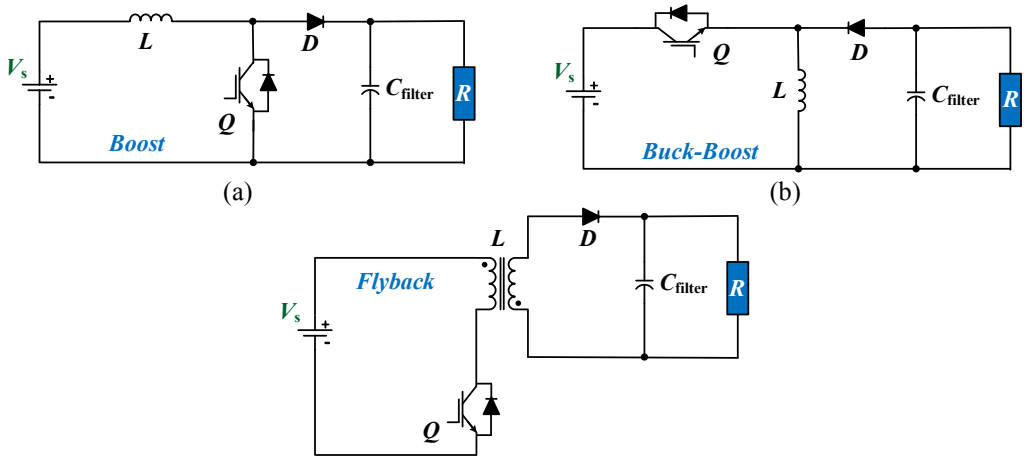


Fig.2.5. Commonly SMPS circuits in HV pulse generation.
(a) Boost. (b) Buck-Boost. (c) Flyback.

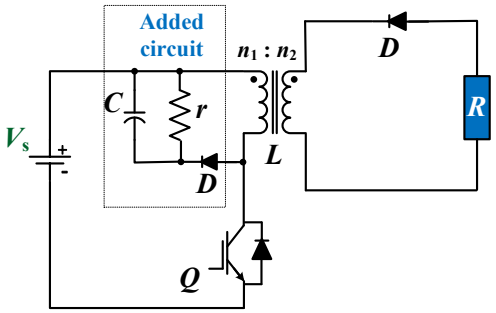


Fig.2.6. Flyback based HV-PG in [47].

In [47], the basic flyback converter shown in Fig.2.5c has been modified by removing the output filter capacitor and adding an RCD circuit across the transformer primary side, as shown in Fig.2.6. Unlike typical DC-DC converter applications, the output voltage is not a constant DC voltage, therefore, in HV pulse generation, the output filter capacitor can be removed. The RCD circuit, the transformer inductance, and the switch Q form a buck-boost converter. The switch Q is operated with a high duty ratio ($0.9 \leq \delta < 1$), when Q is ON, the transformer

primary is exposed to V_s. When Q is OFF, the transformer primary is exposed to $-V_c$ where, V_c is the RCD capacitor voltage such that

$$V_c = \frac{\delta}{1-\delta} V_s \tag{2.3}$$

A negative unipolar HV pulse is generated across load R, with further voltage step up due to the transformer turns ratio, when Q is OFF

$$V_p = \frac{-n_2}{n_1} V_c \tag{2.4}$$

where V_p is the generated pulse voltage across load R. The Q duty ratio must be properly selected, in the high range, such that transformer core reset and the voltage rating of Q alleviate the need of series connection switches.

In [48]-[49], an input buck-boost converter feeds a stack of LV switch–capacitor units at the output stage, as shown in Fig.2.7. With proper control of the series switches Q, an HV pulse is impressed across the load with controllable dv/dt. But a complicated control algorithm is required and only unipolar pulses are generated.

In [50], two boost converters are connected front-to-front while the load is connected differentially between the two outputs as shown in Fig.2.8. The topology can generate bipolar pulses, but requires careful parameter selection.

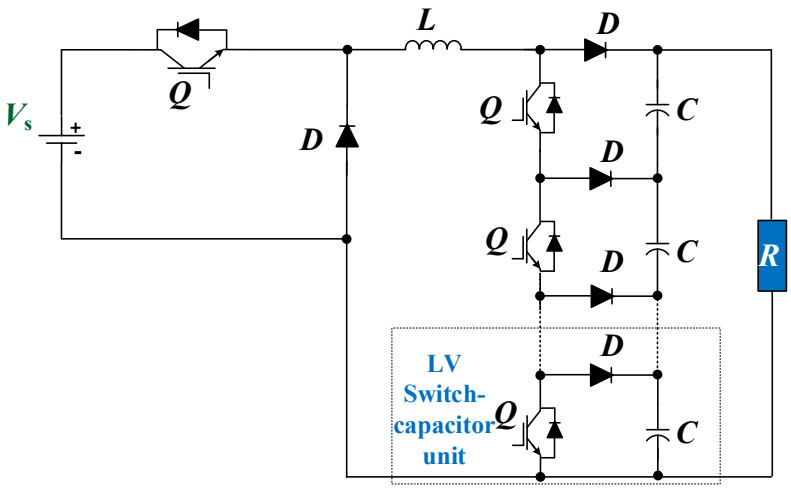


Fig.2.7. The buck-boost converter-based PG in [48]-[49].

In [51], the boost converter-based circuit in Fig.2.9 operates in a discontinuous conduction mode. The load is differentially connected between the input and output. The topology generates unipolar pulses, and no HV switch to create the HV pulses.

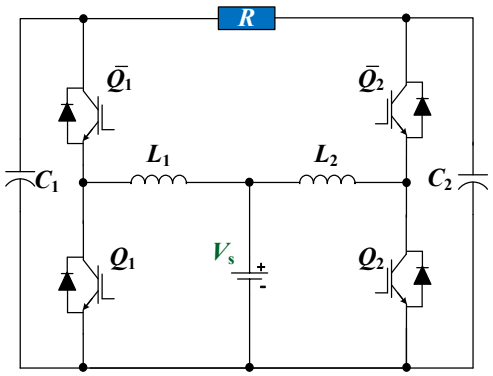


Fig.2.8. Front to front boost converter PG in [50].

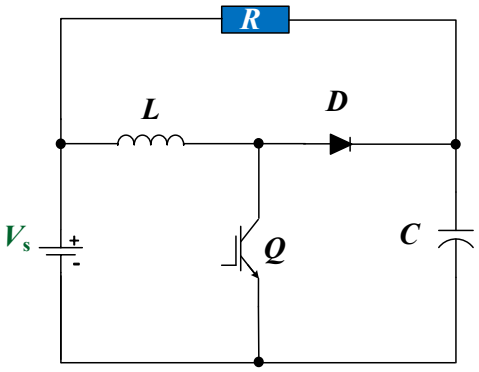


Fig.2.9. Boost converter based PG in [51].

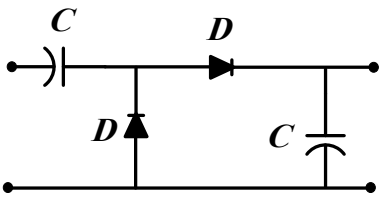


Fig.2.10. Basic CDVM module.

The basic capacitor-diode voltage multiplier (CDVM) module, shown in Fig.2.10, has been incorporated in PG topologies [52]-[54]. Basically, the LV DC input voltage is used to charge the CDVM modules to generate HV DC then a high voltage rated switch is employed to chop the HV DC into unipolar rectangular pulses of the desired rate and width. For bipolar pulses, an H-bridge can be utilised at the output stage. Further voltage boosting can be obtained if the cascaded CDVM modules are preceded by a boost/buck-boost converter.

All the mentioned non-MMC-based PG topologies target unipolar/bipolar rectangular waveform pulse generation. Generation of multipulse waveforms has been addressed in literature by incorporating two converters, one generates the wide pulses and the other generates narrow pulses, then the combination generates multipulse waveforms [16], as shown in Fig.2.11.

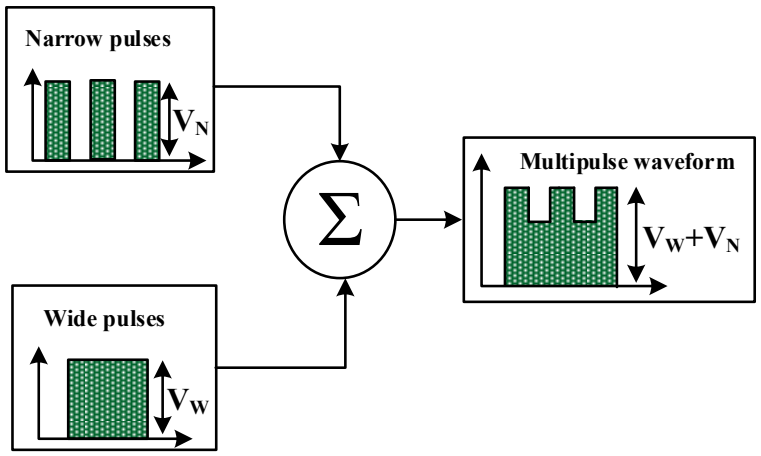


Fig.2.11. Conceptual generation of multipulse waveforms using two rectangular pulse waveforms.

As summarised in Table 2.1 and illustrated through the explored non-MMC-based PGs, the need for an HV switch in the output stage and parameter dependent operation are two limitations. The operation of these PGs is simple and their footprint is small.

2.2.2 MMC Based PG Topologies

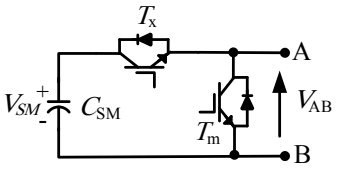
Multilevel voltage source converters (VSCs), such as the diode clamped; flying capacitors, and cascaded full-bridges, are proposed to overcome the main limitations of the two-level VSC in medium-voltage and high-voltage applications [55]; limitations such as bulky input DC capacitor, bulky output ac filter, and high dv/dt. By adding additional levels, the input capacitance is reduced, as is the harmonic filter size (if not eliminated) and the dv/dt problem is mitigated [56].

A. MMC Operation Background

The MMC, an attractive structure multilevel VSC, was invented by Rainer Marquardt in 2001. The MMC hardware structure is based on two SM types, which are the building blocks of MMC topologies, namely: the half-bridge sub-module (HB-SM) and the full-bridge sub-module (FB-SM). Both SM types, along with their switch states, are shown in Fig.2.12 [57]-[60].

The HB-SM, shown in Fig.2.12a, has a capacitor C_{SM} in series with an auxiliary IGBT switch/diode T_x and both are paralleled to a main IGBT switch/diode T_m. Each

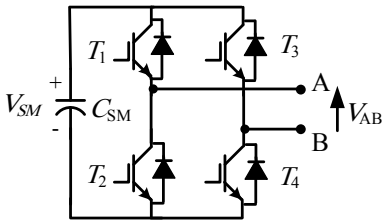
HB-SM can operate in any of three switch states; bypass, insertion and idle. The bypass state (when the main IGBT is ON and the auxiliary IGBT is OFF) implies that the SM is a short circuit and the voltage across the SM terminal V_{AB} is near zero. The insertion state (when the main IGBT is OFF and the auxiliary IGBT is ON) connects the SM-capacitor to V_{AB}, hence, the SM voltage is $V_{AB} = V_{SM}$. The idle state (when both the main and auxiliary IGBTs are OFF) introduces an open circuit (in the direction A to B) across the SM terminal at steady-state, thus, hindering the current flow through the SM terminals (in the direction A to B).



SM Switch States

T_m	T_x	V_{AB}	State
ON	OFF	0	Bypassed
OFF	ON	+ V_{SM}	Inserted
OFF	OFF	Idled	

(a)



FB-SM Switch States

T_1	T_2	T_3	T_4	V_{AB}	State
ON	OFF	ON	OFF	0	Bypassed
OFF	ON	OFF	ON	0	
ON	OFF	OFF	ON	+ V_{SM}	Inserted
OFF	ON	ON	OFF	- V_{SM}	

(b)

Fig.2.12. MMC-SMs. (a) HB-SM. (b) FB-SM.

As illustrated in Fig.2.12b, the FB-SM is formed of four IGBTs/diodes connected to a capacitor. The FB-SM terminals, A and B, are short-circuited (bypassed $V_{AB} = 0$) in two cases when T_1 and T_3 or T_2 and T_4 are switched ON with the other two switches OFF simultaneously. A positive capacitor voltage is applied, $V_{AB} = +V_{SM}$, across terminals A and B when T_1 and T_4 are ON and T_2 and T_3 are OFF. When T_1 and T_4 are OFF and T_2 and T_3 are ON a reverse polarity capacitor voltage appears across terminals A and B, $V_{AB} = -V_{SM}$. Thus, with control of the SM switches, zero, positive, and negative voltages can be applied across terminals AB.

Both SM types have been studied for MMC-based HVDC transmission applications, where the features of each SM type have been elucidated [58]. Whereas

the HB-SM has half the number of semi-conductor switches, the FB-SM can generate a negative voltage at its terminals, which can be used to block HVDC DC fault current.

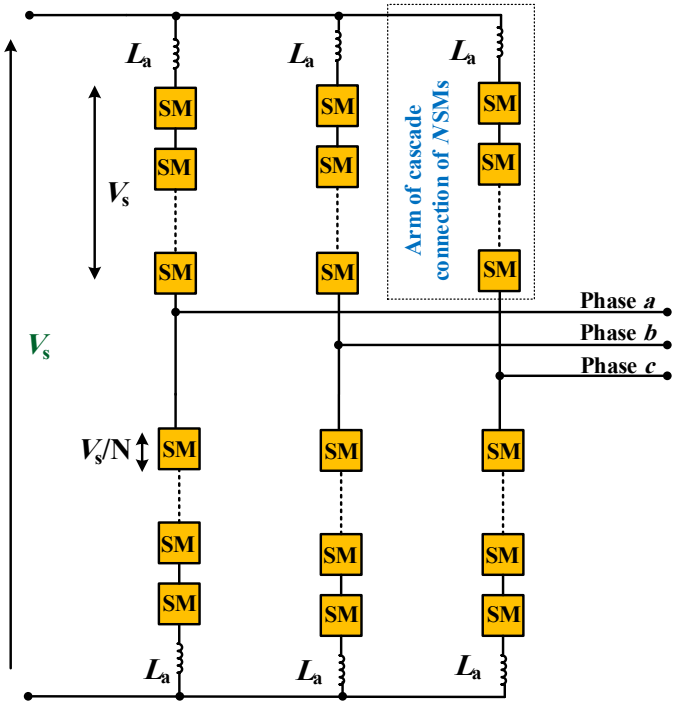


Fig.2.13. Conventional three-phase MMC topology.

The conventional three-phase MMC topology, shown in Fig.2.13, is formed of three phase legs each comprised of two arms of cascade connection of SMs (either HB, FB or both). Each MMC arm has inductor L_a which has two functions, namely: limit arm inrush current during capacitor voltage balancing processes and reduce circulating current between the phases in a three-phase system [55]. Each arm must be able to support the full DC link voltage V_s, thus, for N series SMs per arm, each SM capacitor and switching device must be rated at

$$V_{SM} = \frac{V_s}{N} \tag{2.5}$$

MMC operation necessitates correct insertion/bypass of the SMs by applying modulation techniques while assuring SM capacitor voltage balance. Several MMC modulation techniques have been proposed, such as sinusoidal pulse width modulation (SPWM), space vector modulation (SVM), selective harmonic

elimination (SHE), and nearest-level control (NLC) [59]. The NLC is preferred for a large number of SMs per arm. The NLC approach determines the voltage levels that must be synthesized and the required number of SMs to be inserted for a given voltage step, V_{SM}, by tracking reference signals. The voltage across the upper and the lower arms can be defined as

$$v_{x1} = ½V_s(1 - m\sin(\omega t + \varphi)) \tag{2.6}$$

$$v_{x2} = ½V_s(1 + m\sin(\omega t + \varphi)) \tag{2.7}$$

where v_{x1} and v_{x2} are the upper and lower arm voltages, respectively, m is the modulation index, and φ is the phase shift which is 0°, -120° and 120° for a three phase MMC. Based on the reference arm voltages and the step voltage, the NLC modulation technique is able to determine the number of SMs to be inserted per arm to synthesis the voltage level

$$N_{x1} = round(\frac{v_{x1}}{V_{SM}}) \tag{2.8}$$

$$N_{x2} = round(\frac{v_{x2}}{V_{SM}}) \tag{2.9}$$

where N_{x1} and N_{x2} are the SM number to be inserted in the upper and lower arm, respectively.

Before insertion of the selected SMs to form the required voltage-level with NLC, the SM voltages must be sorted, as it is desired to keep capacitor voltages within a certain band. Therefore, each SM voltage in each arm is continuously measured and compared with other SM voltages in that arm, and the capacitor voltages are sorted (based on magnitude) depending on arm current direction. If the arm current direction indicates SM capacitors discharging, progressively the highest voltage capacitor among the available remaining capacitors is inserted at each voltage level during synthesizing the NLC voltage-levels. Otherwise, the SM capacitors are charged, hence, progressively the lowest voltage capacitor is inserted [60].

B. Phase-leg MMC-Based PG topologies

The main features promoting the MMC for pulse power applications can be summarised as follows:

- inherent capacitor in each MMC-SM.

- structure modularity and redundancy.
- input/output voltage level scalability.
- avoidance of series-connected semi-conductor switches.
- possibility of generating any pulse-waveform by using a suitable reference signal to insert/bypass SMs.

The potential challenges are:

- need for an HV DC input, as the MMC cannot boost the input voltage.
- essential SM capacitor voltage balancing.
- large footprint.

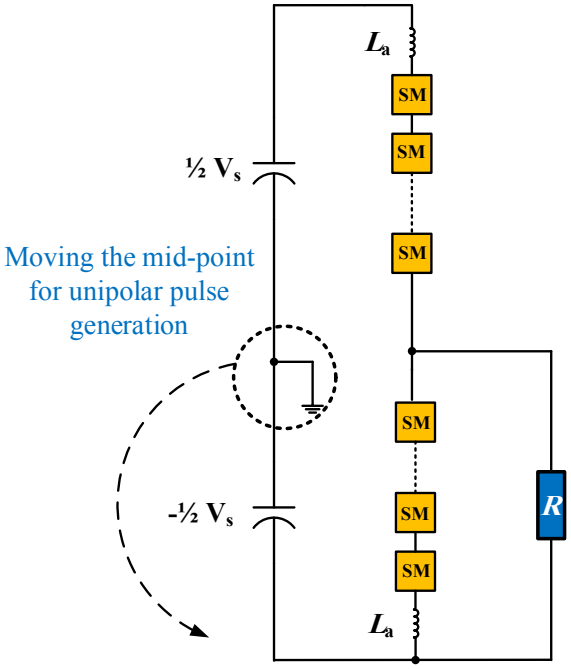


Fig.2.14. Phase-leg MMC based PG topology structure [61]-[63].

By using one phase-leg of a three phase MMC based inverter, shown in Fig.2.13, conventional pulse waveforms can be generated. Changing the modulating reference waveform, which is responsible MMC SM insertion/bypass, allows mimicking of the modulating signal across the load. A phase-leg MMC based PG topology, illustrated in Fig.2.14 fed from HV DC input, V_s, suffers from the following limitations:

- Two bulky capacitors are required to form $\pm ½V_s$ with a mid-point connection.
- generated pulses are bipolar by the default connection, however, for unipolar pulses the reference point is moved to ground. Thus the converter cannot generate both unipolar and bipolar pulses without physically changing the power topology.
- generated bipolar pulse peak voltage is half the HV DC input.

Sensorless SM capacitor voltage balance in MMC based PG topologies are presented in [61]-[63] using HB-SMs. In [61]-[62], the SM-capacitor voltages are balanced by adding a diode between adjacent HB-SMs when employing a specific ON/OFF switching sequence on MMC HB-SM switches.

For converter cost reduction, a conventional phase-leg of MMC HB-SMs is operated in a sensorless mode using phase disposition PWM technique [63]. For each reference pulse waveform, the ON/OFF switching sequence of the SMs is studied, such that the SMs are inserted based on the same loading conditions resulting in balanced capacitor voltages. MMC phase-leg sensorless operation is attractive in terms of reducing hardware costs and complexity. But control complexity is increased as the number of the SMs is increased, and operation is adversely affected under SM failure.

Reference [64] attempts to obtain a pulse peak voltage higher than the input DC link voltage, with phase-leg MMC topology. The two arms of the phase-leg are comprised of a series combination of FB and HB SMs, the pulse peak voltage can be either equal to or integer multiples of the input DC link voltage by selecting the proper FB and HB SMs number per arm. But, the topology requires pre-charging of the SM-capacitors before operation while a complicated balancing algorithm is necessary for a large number of SMs.

2.2.3 Hybrid PG Topologies

MMC based PG topologies alleviates the need for HV switches and avoids the series connection challenges of non MMC-based PG topologies. But the main limitation is the need of an HV DC input and an MMC phase-leg can only generate bipolar pulses with a peak voltage of half the input HV DC. A solution to these limitations involves hybrid PG topologies, in which an LV DC is the input stage followed by a voltage

boosting mechanism. MMC SMs can be either incorporated at the voltage boosting stage or at the HV pulse creation stage, or both. The MMC SMs are employed to store energy in their inherent capacitors, from the input supply, then transfer it to the load during HV pulse generation. Hence, HV pulses are created across the load without semi-conductor series connection, while gaining MMC features such as modularity, scalability, and redundancy.

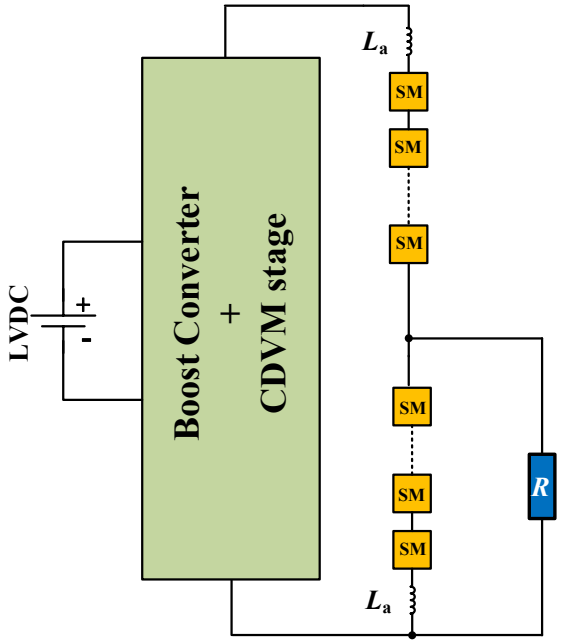


Fig.2.15. Hybrid MMC based PG using boost inverter and CDVM stages to feed an MMC phase-leg [65].

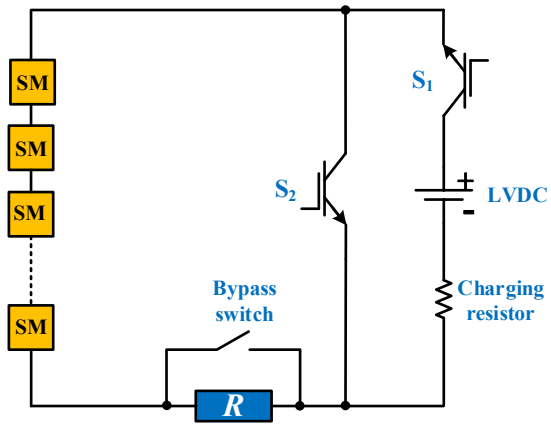


Fig.2.16. Sequential charging MMC SMs fed from an LV DC supply and a charging resistor [66].

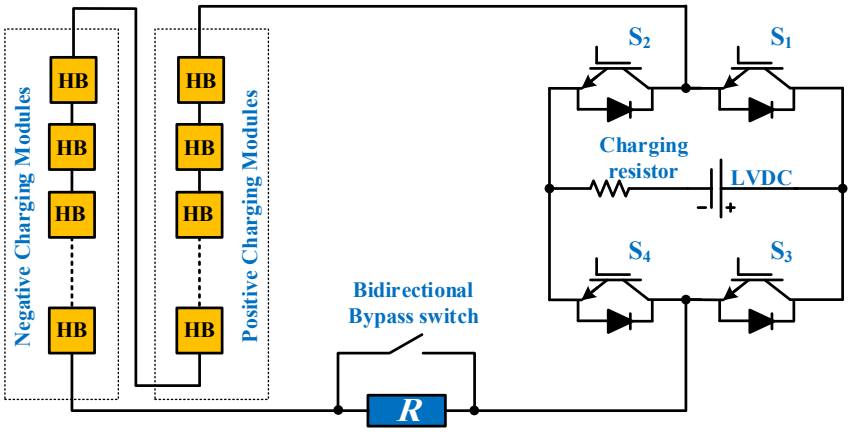


Fig.2.17. Two series groups of MMC HB-SMs charged sequentially to positive and negative voltages by an input H-bridge and LV DC supply and a charging resistor [68].

A boost converter fed from an LV DC source followed by a CDVM stage is proposed in [65] such that HV DC is obtained, as shown in Fig.2.15. The generated HV DC is then applied to the terminals of an MMC phase-leg. MMC SMs are employed to create the HV pulses across the load, hence, a solution for HV DC generation is provided while the MMC phase-leg is operated as in sectionB B2.2.2B.

In [66], a specific number of HB-SMs (according to the required pulse peak voltage) are charged sequentially from an LV DC input then discharged in series across the load, forming unipolar HV pulses, as shown in Fig.2.16. During the progressive sequential SM charging, the SM to be charged is inserted while the other series SMs are bypassed, while the load is bypassed and switches S_1 and S_2 are turned ON and OFF, respectively. During HV pulse generation, all the charged SMs are inserted simultaneously and switches S_1 and S_2 are turned OFF and ON, respectively, thus, a unipolar rectangular HV pulse appears across the load. But the charging mechanism is achieved via a relatively high charging resistances to limit the charging current. Consequently, capacitor charging time is elongated, which limits the pulse generation repetition rate and/or the number of utilised SMs.

In [67], the HB-SMs are replaced with FB-SMs to allow bipolar HV pulse generation across the load. Alternatively, two groups of series connected HB-SMs are employed in [68], such that one group is responsible for generating the positive pulse polarity and the other generates the negative pulse polarity. Charging the HB-

SMs in each group is by using an H-bridge across the LV DC supply and a charging resistor as shown in Fig.2.17.

The MMC sequential charging PG topologies in [66]-[68], utilise a bypass switch across the load during individual SM charging. The bypass switch is comprised of diodes in [66], thyristors in [67], and back-to-back thyristors in [68], respectively. The bypass switches are rated at the HV pulse level.

2.3 Summary

Electroporation applications require HV pulses with specific characteristics, hence, HV PGs are the key element in such applications. This chapter presented the main available topologies for HV pulse generation. Two major PG categories are presented namely: classical PGs and power electronics based PGs, as shown in Fig.2.18. Power electronics-based PGs are collated into three main groups, namely: non MMC-based, MMC-based, and hybrid topologies. The main features and limitations for each category were highlighted.

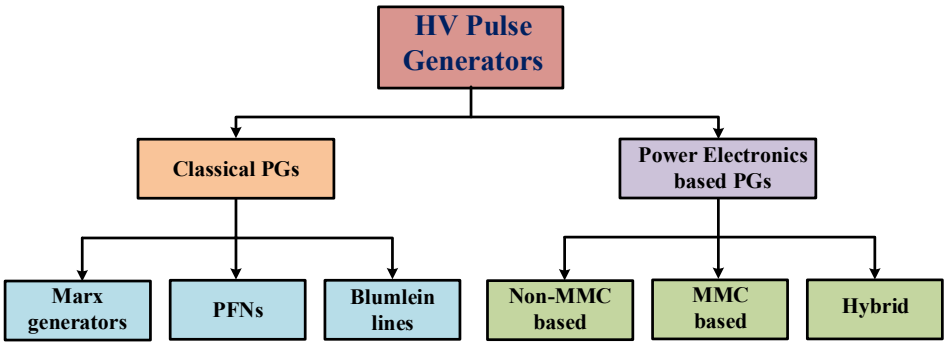


Fig.2.18. Classification of HV PGs in the literature.

Chapter 3

New MMC Based PGs Fed from an HV DC Source

In this chapter, a new family of HV DC fed MMC based PGs is introduced. The proposed topologies address limitations facing existing MMC based topologies. The HV DC source is assumed to exist. The research is focused on generating flexible HV pulses with full utilisation of the input HV DC while assuring SM capacitor voltage balance.

3.1 Clamping Based Pulse Generator

A DC source feeding an H-bridge comprising four semi-conductor switches, generates AC rectangular voltage waveform across the load, as illustrated in Fig.3.1. Turning on Q_1 and Q_2 while turning off Q_3 and Q_4 simultaneously impose $+V_s$ across the load, while $-V_s$ is imposed across the load when Q_1 and Q_2 are turn off while turning on Q_3 and Q_3, simultaneously. This is the basic approach for inverting a DC voltage input to AC with a peak voltage equal to the DC input voltage. But, extending this approach to invert HV DC requires series switch connection forming the H-bridge. Additionally, dynamic and static voltage charging across the switches must be catered for by using snubber circuits.

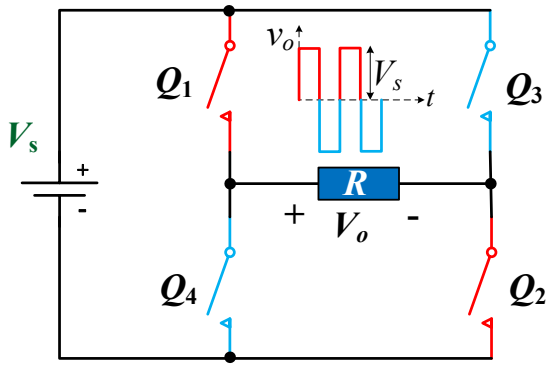


Fig.3.1. Generating AC voltage from DC input voltage using H-bridge circuit.

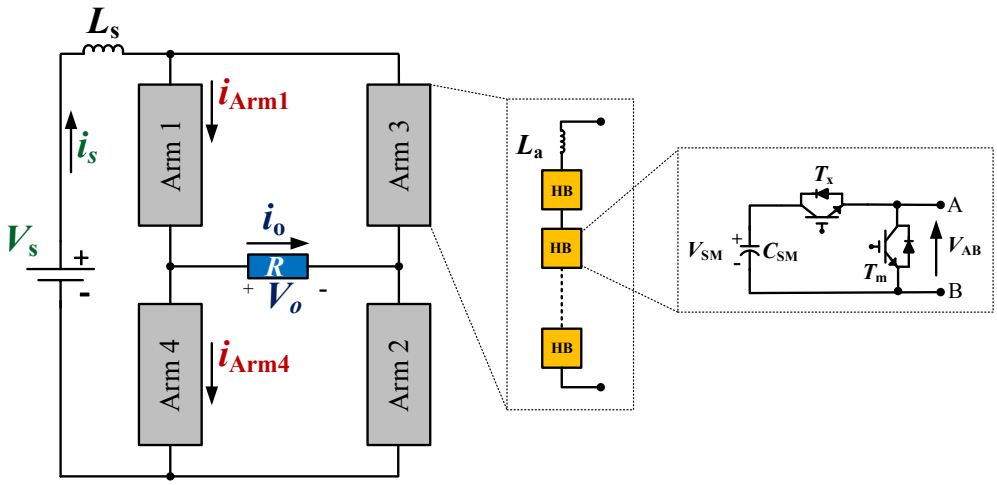


Fig.3.2. Proposed CPG converter topology.

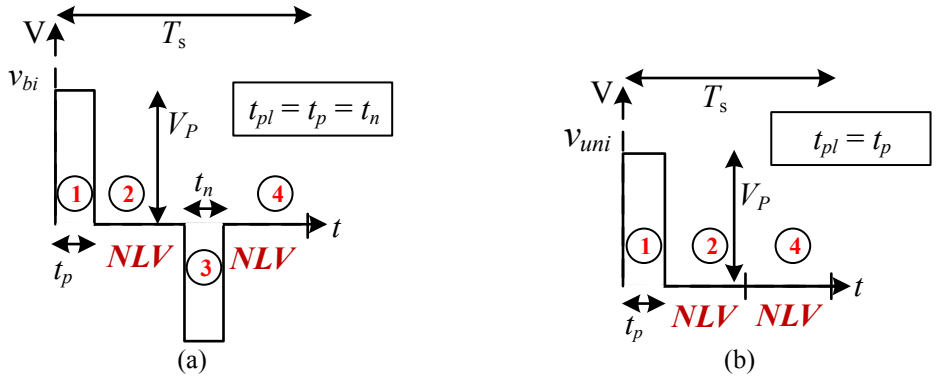


Fig.3.3. Generated HV pulses: (a) Bipolar rectangular. (b) Unipolar rectangular.

3.1.1 Clamping PG Converter Topology

In order to avoid series device connection challenges, a clamp based PG (CPG) topology is proposed to generate rectangular HV pulses based on MMC HB-SMs without voltage sensors as shown in Fig.3.2 [69]. It consists of four MMC arms (Arm z, where $z \in \{1, 2, 3, 4\}$) forming an H-bridge connected to HVDC supply V_s via an inductor L_s. Each arm is of N series connected MMC HB-SMs and an arm inductor L_a to suppress inrush current between SM capacitors during their insertion. Depending on the switching sequence of the complimentary switches T_m and T_x, the SM-terminal voltage V_{AB} is either equal to the capacitor-voltage V_{SM} or zero, as illustrated in the HB-SM switching table in Fig.2.12a.

The proposed converter is capable of generating the rectangular bipolar (v_{bi}) and unipolar (v_{uni}) HV pulses shown in Fig.3.3a and Fig.3.3b, respectively. The

controlling parameters are: repetition time T_s and pulse duration t_{pl}. For flexibility, each pulse polarity has a dedicated pulse duration, t_p and t_n for the positive and negative pulse polarities, respectively. If symmetrical pulse polarity durations are generated as in Fig.3.3a, then $t_p = t_n = t_{pl}$. The generated pulses can be defined by the time durations in (3.1) and (3.2), where each pulse polarity is followed by a null load voltage (NLV) duration (of 0V), for bipolar and unipolar pulses respectively, see Fig.3.3.

$$v_{bi} = \begin{cases} +V_P & , \quad 0 \le t < t_{pl} \\ 0\ (positive\ NLV) & , \quad t_{pl} \le t < ½T_s \\ -V_P & , \quad ½T_s \le t < ½T_s + t_{pl} \\ 0(negative\ NLV) & , \quad ½T_s + t_{pl} \le t < T_s \end{cases} \tag{3.1}$$

$$v_{uni} = \begin{cases} \pm V_P & , \quad 0 \le t < t_{pl} \\ 0\ (positive\ NLV) & , \quad t_{pl} \le t < ½(T_s + t_{pl}) \\ 0(negative\ NLV) & , \quad ½(T_s + t_{pl}) \le t < T_s \end{cases} \tag{3.2}$$

3.1.2 CPG Operating Principle

The same methodology is used to generate unipolar and bipolar rectangular pulses. The only difference is the omission of one polarity during pulse generation. Accordingly, the following discussion will consider bipolar pulse generation to illustrate the basic concept. The load is modelled as a resistive load *R* as illustrated in Chapter 1. For proper operation, each arm should be able to withstand the DC-link voltage V_s, therefore, each SM-capacitor voltage is:

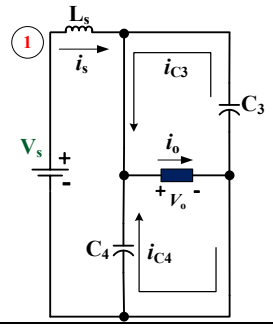
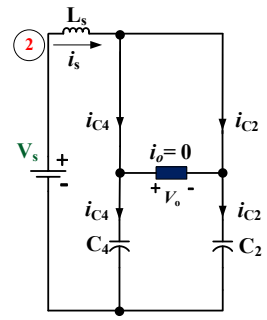
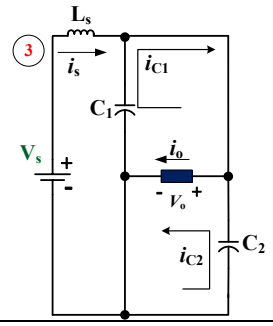
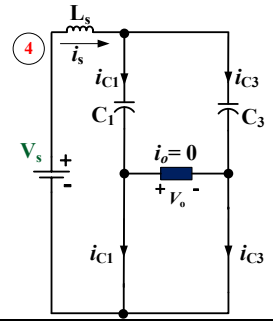
$$V_{SM} = \frac{V_s}{N} \tag{3.3}$$

Table 3.1 shows the circuit configuration and summarises the operating sequence in each period. Generally, during positive pulse generation Arm3 and Arm4 capacitors are inserted to discharge across the load, while Arm1 and Arm2 are inserted during negative pulse generation. The positive and negative NLV durations in (3.1) allow charging of the lower arms and the upper arms, respectively.

The utilised MMC SMs in each arm are all inserted/bypassed simultaneously, therefore, each IGBT switch is subjected only to the SM voltage. Thus, the SM capacitor clamps the IGBT voltage and enforces a symmetrical series voltage

distribution. In both charging and discharging, the arm SM capacitors are inserted together presenting a total capacitance of C_{SM}/N per arm.

Table 3.1: Operating Principle of the CPG

	Circuit configuration	Sequence of operation
Positive Pulse		• Arm3 and Arm4, C_3 and C_4, capacitors are inserted simultaneously while Arm1 and Arm2 are bypassed such that load voltage is $+V_s$. • Load current flows due to a combination of three energy sources; C_3, C_4 and L_s. • C_3 and C_4 discharge during this period.
Positive NLV		• Arm2 and Arm4, C_2 and C_4, capacitors are inserted, Arm1 and Arm3 are bypassed, hence the load voltage is nullified. • The load current is zero. • C_2 and C_4 are charged through L_s during this period.
Negative Pulse		• Arm1 and Arm2, C_1 and C_2, capacitors inserted while Arm3 and Arm4 are bypassed so the load voltage is $-V_s$. • The load current flows due to a combination of three energy sources; C_1, C_2 and L_s. • C_1 and C_2 discharge during this period.
Negative NLV		• Arm1 and Arm3, C_1 and C_3, capacitors are inserted, Arm2 and Arm4 are bypassed, hence, the load voltage is nullified. • The load current is zero. • C_1 and C_3 are charged through L_s during this period.

3.1.3 Analysis and Parameter selection of the CPG

Based on the operating principle in Table 3.1, provided all the arm switches are turned on/off at the same time, the pictorial charging and discharging sequence of the equivalent arm capacitors is shown in Fig.3.4. The instantaneous current flow through the load (i_o), the input inductor (i_s), Arm1 (i_{Arm1}), and Arm4 (i_{Arm4}) are shown in Fig.3.5.

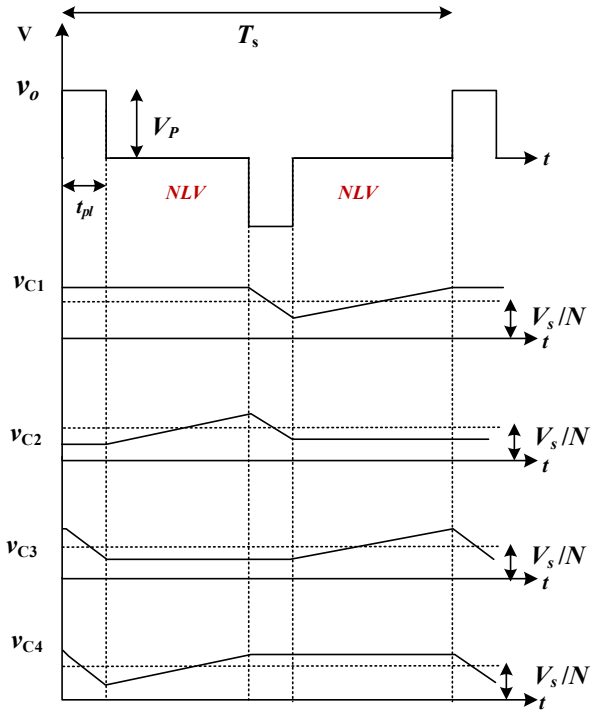


Fig.3.4. Arm equivalent capacitors charging and discharging sequence for generating a bipolar rectangular pulse.

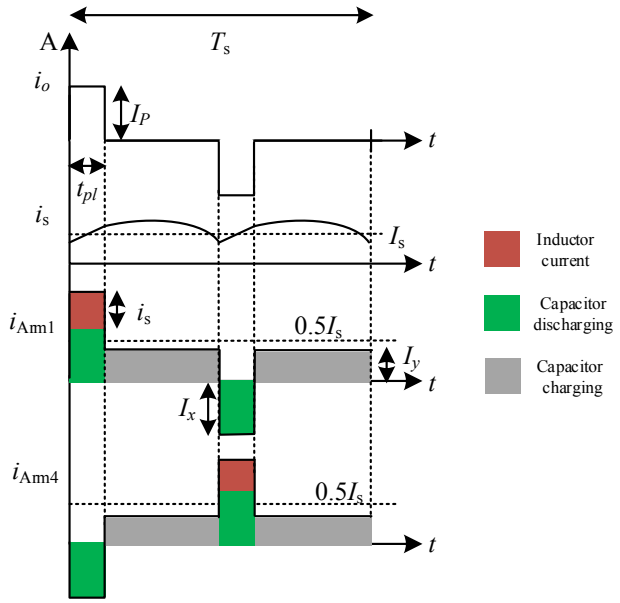


Fig.3.5. Current waveforms through the load, the input inductor, Arm1, and Arm4.

Assuming the voltage and current notations in Fig.3.2 are positive, the load current is

$$i_o = i_{Arm1} - i_{Arm4} = i_{Arm3} - i_{Arm2} \tag{3.4}$$

while the input current i_s is

$$i_s = i_{Arm1} + i_{Arm3} = i_{Arm2} + i_{Arm4} \tag{3.5}$$

During positive pulse generation, the load current is supplied from three energy sources namely: Arm3 capacitors discharge through Arm1; Arm4 capacitors discharge through Arm2; and the input inductor current. During a negative pulse duration the load current is formed from three energy sources namely: Arm1 capacitors discharge through Arm3; Arm2 capacitors discharge through Arm4; and the input inductor current. Denoting the average input current as I_s and neglecting semi-conductor losses:

$$V_s I_s = I_o V_o \tag{3.6}$$

where I_o and V_o are the load rms current and voltage, respectively.

Accordingly, V_o is calculated using Fig.3.3a:

$$V_o = \sqrt{\frac{2t_{pl}}{T_s}} V_P \tag{3.7}$$

Since $I_o = V_P/R$, I_s is

$$I_s = \frac{V_P^2}{V_s}\frac{2\delta}{R} \tag{3.8}$$

where $\delta = t_{pl}/T_s$ is the pulse duty ratio.

From Fig.3.5 and (3.4), the pulse peak current I_P can be expressed as

$$I_P = I_s + 2I_x \tag{3.9}$$

where the capacitors discharging and charging currents are denoted by I_x and I_y respectively. Accordingly, the capacitors current-second (charge) balance yields

$$I_x t_{pl} = I_y(½T_s - t_{pl}) \tag{3.10}$$

From Fig.3.5 and (3.4), the capacitor charging current is

$$I_y = ½ I_s \tag{3.11}$$

Solving (3.9), (3.10) and (3.11) yields

$$I_y = \delta I_P \tag{3.12}$$

$$I_x = (½ - \delta) I_P \tag{3.13}$$

$$I_s = 2\delta I_P \tag{3.14}$$

As the average charge change in any SM capacitor should be zero, examination of either the charging or the discharging period is sufficient. Thus the equivalent arm capacitance C_{Arm} can be defined as

$$C_{Arm} = \frac{I_x \Delta t}{\Delta v} \tag{3.15}$$

where Δt is the discharging current duration and Δv is the peak to peak voltage ripple. Substituting for variables from the previous equations gives

$$C_{Arm} = \frac{(½ - \delta) V_P \, \delta T_s}{R(\gamma V_s)} \tag{3.16}$$

where γ is the percent peak to peak voltage ripple of an arm capacitor. Accordingly the SM capacitance is:

$$C_{SM} = \frac{(½ - \delta) V_P \, \delta T_s}{R(\gamma V_s)} N \tag{3.17}$$

If IGBTs voltage drops and the internal resistance of L_s are neglected, then $V_P \cong V_s$. Then (3.17) reduces to

$$C_{SM} = \frac{(½ - \delta) \, \delta T_s}{\gamma R} N \, \alpha \tag{3.18}$$

where $\alpha \geq 1$ is a factor to account for the neglected losses.

Resonance between the DC link inductor and arm capacitance during charging of either the two upper arms or two lower arms should be avoided. Device switching frequency should be well away from the resonance frequency of the equivalent LC circuits to avoid exciting resonance currents. Therefore, based on the calculated equivalent arm capacitance and the repetition time, an estimation of the inductance of L_s is:

$$L_s > \frac{½T_s^2}{(2\pi)^2 C_{Arm}} \tag{3.19}$$

3.1.4 Simulation Results for the CPG Converter

The CPG topology is MATLAB/Simulink simulated with the parameters in Table 3.2. The capacitance of the SM capacitors is calculated based on (3.18) with $\alpha = 1$, and (3.19) is used to estimate the input inductance. The simulations assess the ability of the PG to generate bipolar and unipolar pulses, and operation with faulty MMC SMs.

The simulation results when generating 10μs bipolar HV pulses at 10kHz are shown in Fig.3.6. The generated pulses are shown in Fig.3.6a, the 4 arms capacitor voltages are given in Fig.3.6b with an expanded view of arms 1 and 3. The response of the capacitor voltages follow the expected response shown in Fig.3.4. As a result, in this case for $T_s = 100\mu s$, each arm capacitor discharges into the load for 10μs, charge for 40μs while their voltage is unchanged for 50μs. Each capacitor voltage oscillates around 1000V, that is V_s/N, with less than 5% voltage ripple, as designed.

The proposed converter is capable of changing the rectangular pulse characteristics without altering the converter topology, specifically, via software control. Using the same specification as in Table 3.2, the converter is programmed to generate 4μs positive unipolar HV pulses and 10μs unipolar HV pulses with negative polarity, all at a 10kHz repetition rate and 10kV peak as shown in Fig.3.7a and Fig.3.7b respectively. It is recommended to assume the widest pulse polarity is t_{pl} during the capacitance sizing stage, see (3.18).

Generating rectangular pulses with different polarity characteristics is possible. Bipolar pulses with different positive and negative durations, 10μs and 4μs respectively, are shown in Fig.3.7c. Combined NLV bipolar pulses are shown in Fig.3.7d such that the positive pulse duration is 10μs and the negative pulse is 4μs. Fig.3.7e shows the flexibility of the concept, with bipolar pulses of a variable repetition frequency. A train of 4μs pulses at 10kHz is combined with a train of 10μs pulses at 5kHz, with a 1200μs repetition time.

Table 3.2: Specification for CPG Simulation and Experimentation

Parameter		Simulation	Experimentation
DC input voltage	V_s	10 kV	250 V
Input inductance	L_s	1.5 mH	0.5 mH
Number of SMs/arm	N	10	3
Repetition time	T_s	100 µs	100 µs
Arm inductance	L_a	15 µH	10 µH
Load resistance	R	1 kΩ	500 Ω
SM capacitance	C_{SM}	1 µF	1 µF
Pulse duration	t_{pl}	10µs and 4µs	10µs and 4µs
Percent voltage ripple	γ	0.05	0.05
Safety factor	α	1	1

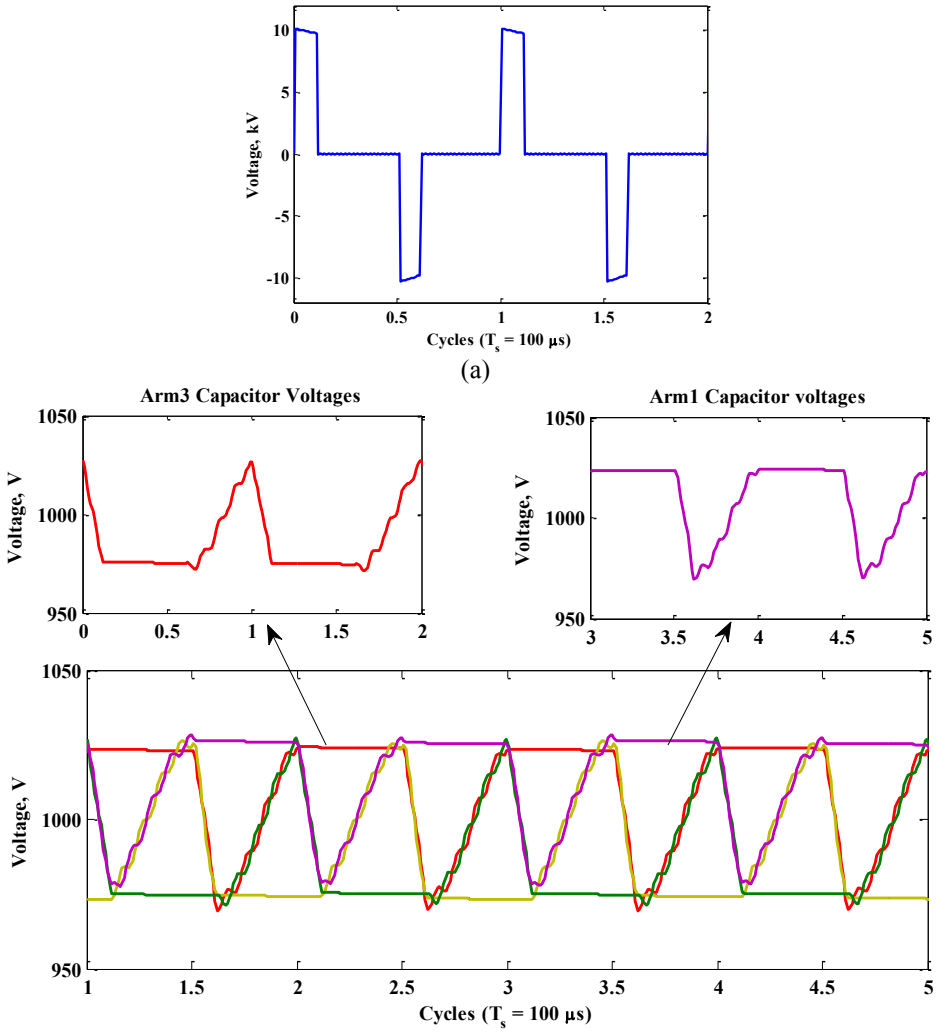


Fig.3.6. Simulation results for bipolar HV pulses, $t_{pl} = 10\mu s$.
(a) Output pulse. (b) 4 arm capacitor voltages with expanded view of Arm1 and Arm3.

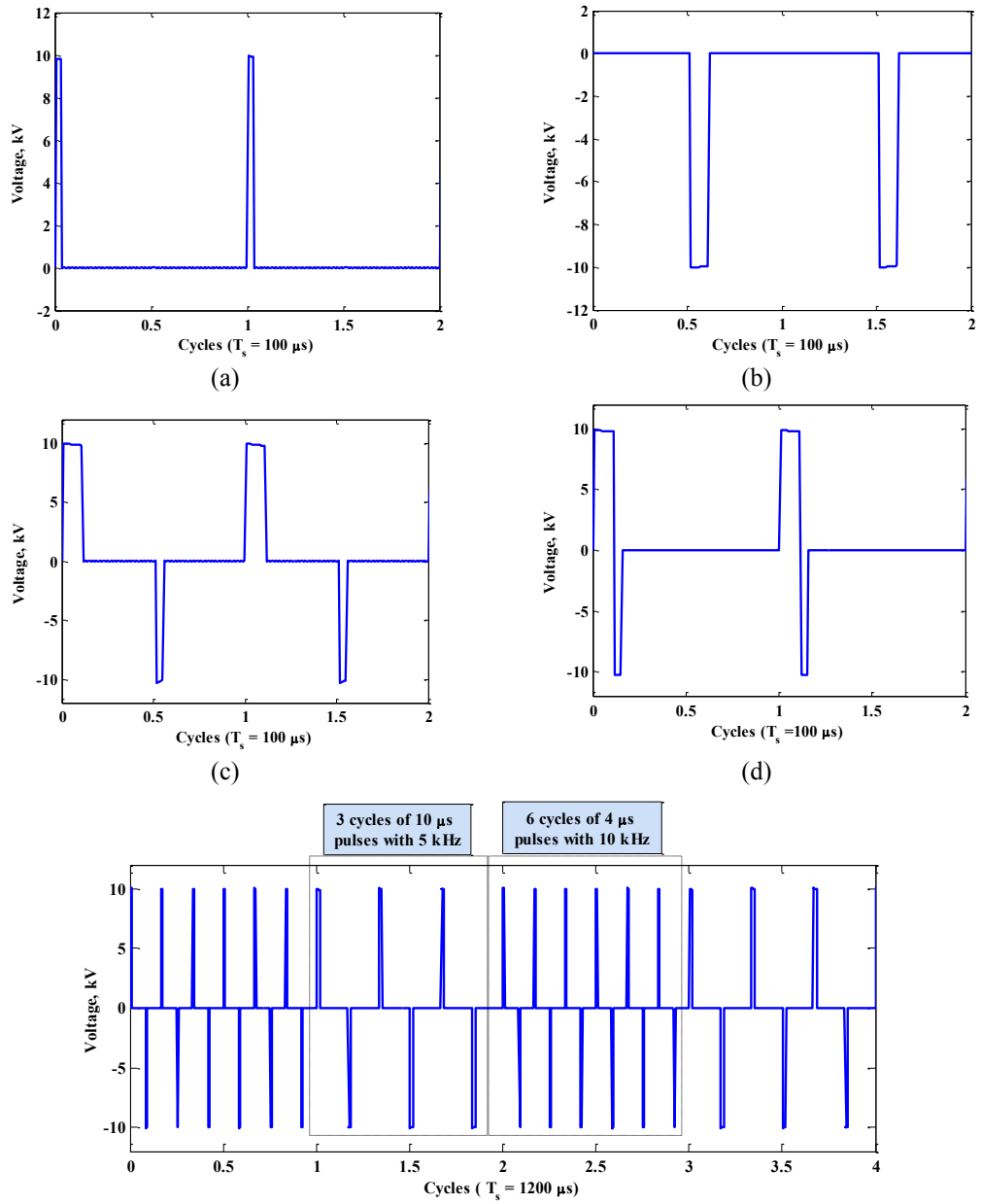


Fig.3.7. Simulation results for output HV pulses with different characteristics.
(a) 4µs positive unipolar. (b) 10µs negative unipolar. (c) Different polarity duration pulses. (d) Combined NLV pulses with different durations. (e) Variable pulse duration and repetition frequency.

The small voltage drop in the pulse peak is due to the decrease in capacitor energy during pulse generation. It is the reciprocal of the SM capacitance, thus the larger the capacitance, the smaller the voltage drop and vice-versa. The ability of the CPG to generate a wide range of rectangular pulses is solely dependent on the speed of the controller in executing the control software instructions, such that the total software

execution time is less than the required pulse repetition time. For high repetition rates and/or short pulse durations, fast semi-conductor switches is mandatory.

The SM capacitors are responsible for clamping the voltage across the module switches to V_s/N without any voltage measurements or control. Thus, if one or more SMs fail, the excess voltage will be shared equally between the healthy SM capacitors. Hence, the new SM voltage V_f under failure is

$$V_f = \frac{V_s}{N - N_f} \tag{3.20}$$

where N_f is the number of faulty SMs. The CPG converter is able to generate the desired bipolar rectangular pulses, shown in Fig.3.6a, with two faulty SMs in Arm1. But, in this case the voltage of each healthy SM in Arm1 will be 1250V; increased from 1000V before the fault. The voltage stress is distributed between the healthy SMs to alleviate the malfunction of the two SMs, as shown in Fig.3.8.

The switches rating should be selected as 50% of its rating value in the datasheets to comply with the failure in time (FIT) effect. For the series connected HB-MMC SMs, practically, as in HVDC transmission applications, there should be redundant SMs that are normally not contributing in the process unless a failure occurs, then they take the place of the malfunctioned SMs. Additionally, if for any reason the number of redundant SMs is not enough, a malfunctioned SM is bypassed, and since the other SMs are also designed based on FIT (half their voltage rating) they can withstand the excess voltage stresses until it is mitigated.

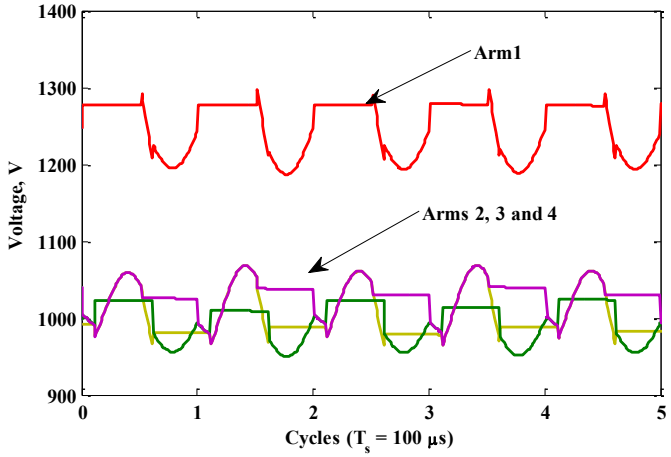


Fig.3.8. Simulation results for the 4 arms capacitor voltages with two faulty SMs in Arm1 during bipolar rectangular pulses generation of $t_{pl} = 10\mu s$.

3.1.5 Experimental Results for the CPG Converter

The proof of concept CPG experimental setup uses ultra-fast IGBT switches (STGW30NC60WD) while the control algorithm is implemented in eZDSP, which is a digital signal processor (DSP) board based on the Texas Instruments TMS320F28335 DSP. The experimental specifications are given in Table 3.2, and the proof of concept experimental rig is shown in Fig.3.9.

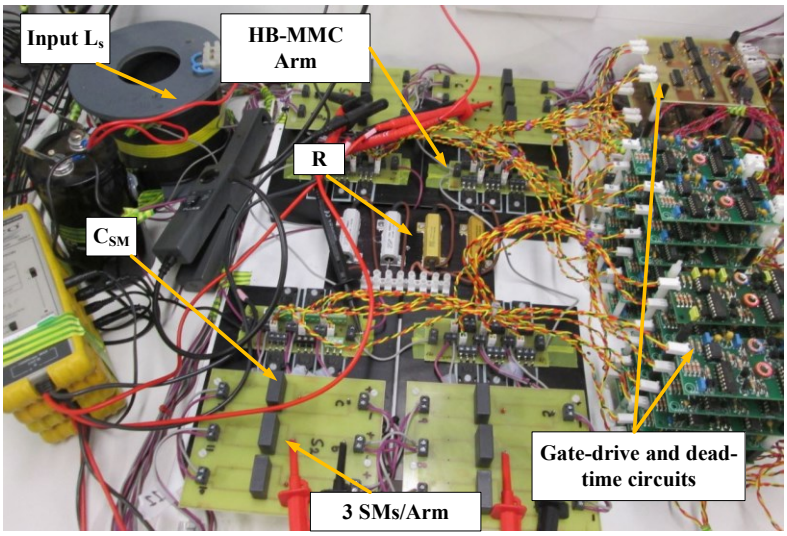


Fig.3.9.The proof of concept CPG experimental rig.

Fig.3.10 shows the experimental bipolar voltage pulses with $t_{pl} = 10\mu s$. The output voltage pulses and the input current through L_s are shown in Fig.3.10a and Fig.3.10b, respectively. The voltages across one capacitor in each of the four arms are given in Fig.3.10c with a shifted-zoomed view of Arm1 and Arm3 capacitor voltages. Since the output pulse peak is 250V, each capacitor voltage should be around 83.3V, as shown in Fig.3.10c.

Generating customised rectangular pulse characteristics is explored in Fig.3.11. Fig.3.11a shows bipolar pulses with positive and negative pulse durations of 8µs and 4µs respectively. Combined NLV duration pulses with positive and negative pulse durations of 8µs and 4µs, respectively, are shown in Fig.3.11b. Unipolar rectangular pulses with a positive polarity of $t_{pl} = 10\mu s$ are shown in Fig.3.11c. In Fig.3.11d, a train of 4µs pulses at 10kHz is combined with a train of 8µs pulses at 2.5kHz, with a 1500µs repetition time.

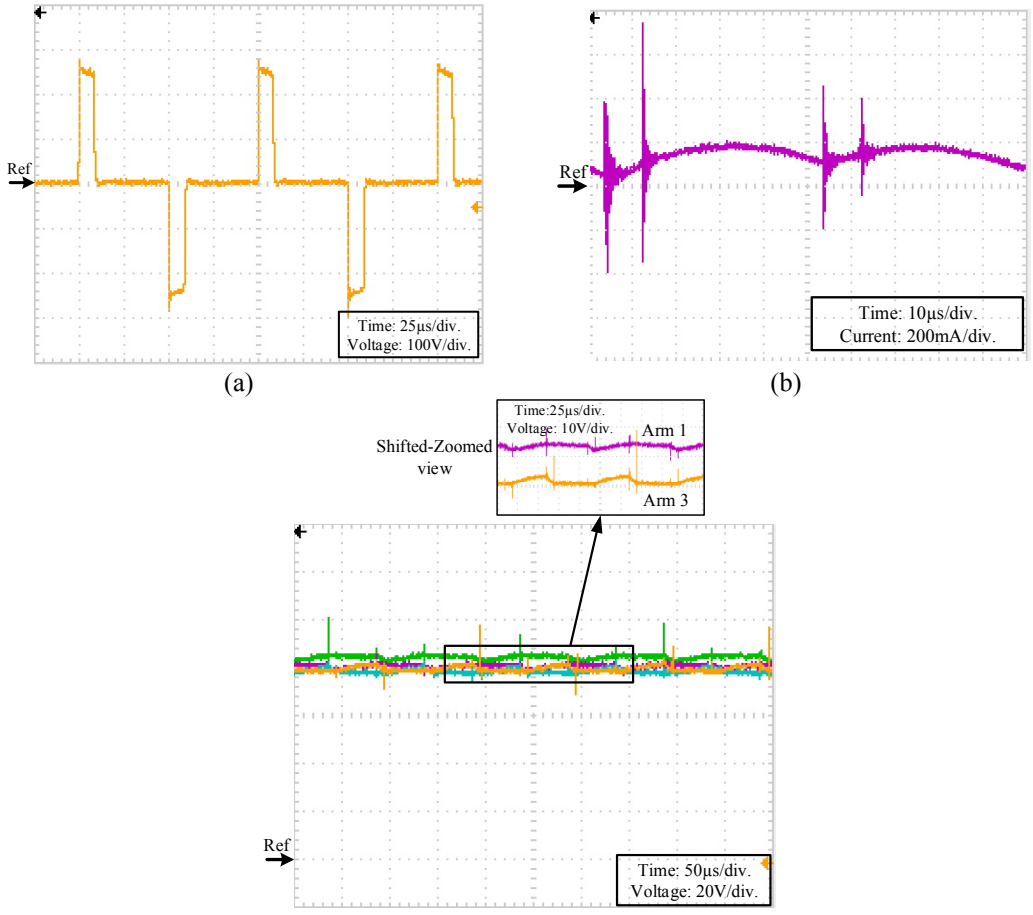


Fig.3.10. Experimental results, $t_{pl} = 10$ µs.
(a) Output bipolar voltage pulses. (b) Input current. (c) One capacitor voltage in each of the 4 arms.

Finally, in order to verify the performance of the proposed topology during MMC SM malfunction, one Arm1 SM is deliberately shorted while generating bipolar pulses of $t_{pl} = 10\mu s$. Again the parameters in Table 3.2 are used with an input voltage of $V_s = 200V$. The output voltage pulses are shown in Fig.3.12a. The faulty arm SM voltages are shown in Fig.3.12b along with one SM voltage in the healthy arm, Arm4. The healthy SM voltages in Arm1 increase to 100V from 66.7V. The voltage across one capacitor in each arm for this case is shown in Fig.3.12c.

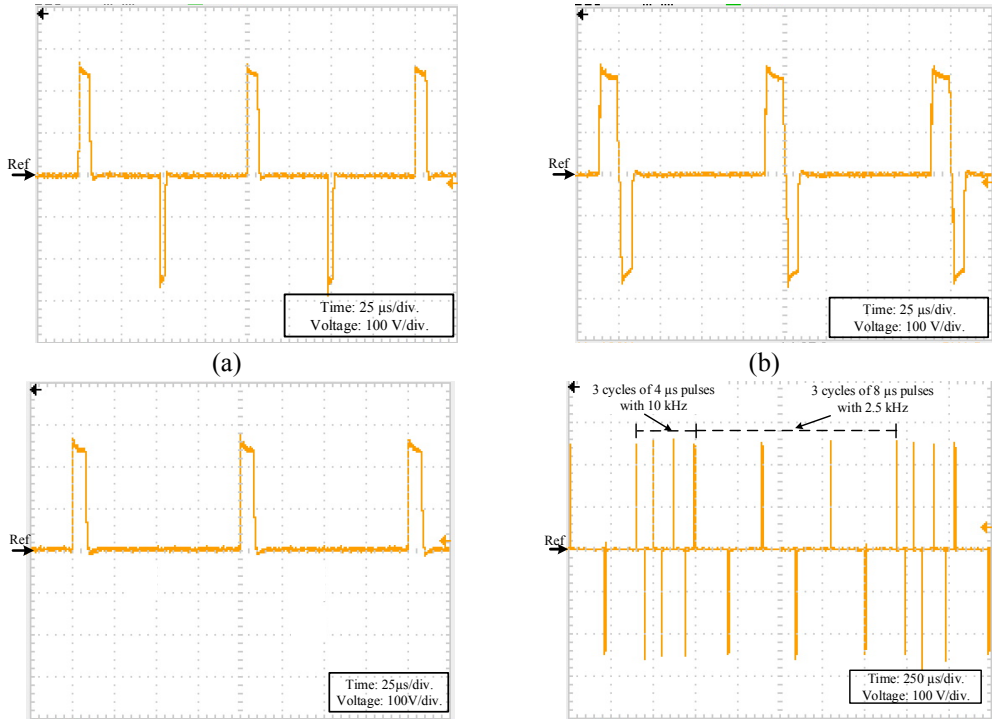


Fig.3.11. Experimental results.
(a) Different duration pulses. (b) Combined NLV pulses with different polarity durations. (c) Unipolar pulses with $t_{pl} = 10\mu s$. (d) Variable pulse duration and repetition frequency.

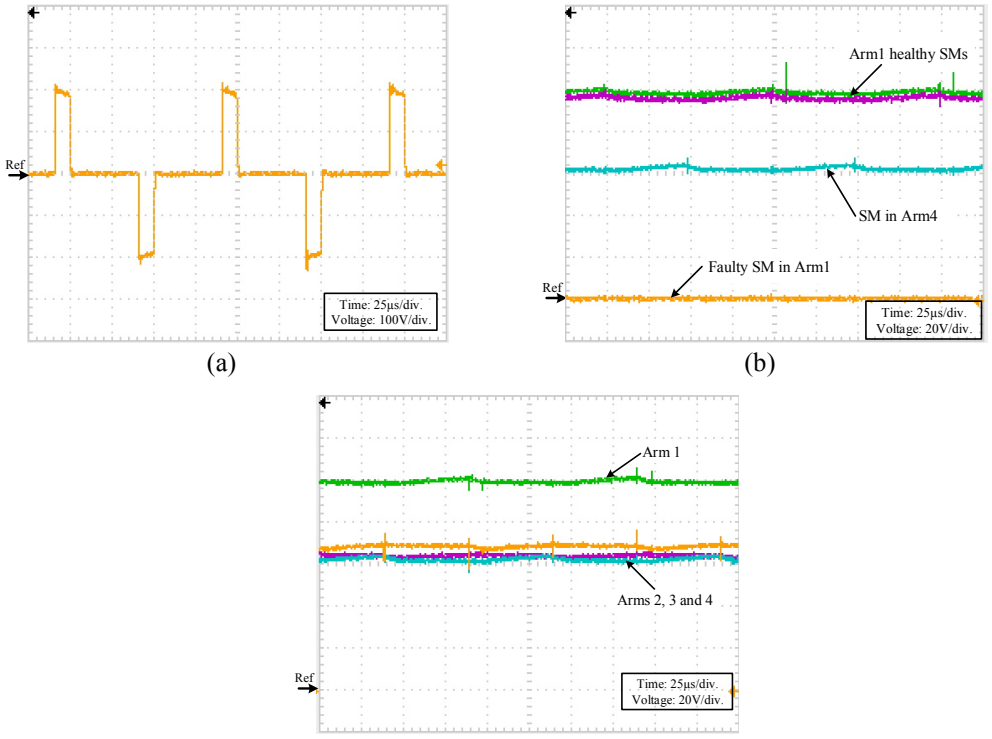


Fig.3.12. Experimental results, when a SM in Arm1 is faulty.
(a) Output bipolar voltage pulses with $t_{pl} = 10\mu s$. (b) Arm1 SM capacitor voltages along with one SM in Arm4. (c) One SM capacitor voltage in each of the 4 arms.

3.2 Generic Pulse Waveform Generator

Despite the flexibility offered by the CPG topology, it is only able to generate rectangular pulse waveforms. If voltage sensors are added to provide individual SM voltage measurement to the controller software, generation of bipolar multilevel pulse-waveforms is possible while maintaining SM capacitors voltage balance. The multilevel pulse-waveform can be manipulated to generate rectangular, ramp and multipulse waveforms by only changing the controller software algorithm, without changing any physical connections in the circuit topology. The feature of generating high frequency rectangular pulses in the CPG can be obtained by disabling the voltage-measurements and operate in the sensorless clamping mode.

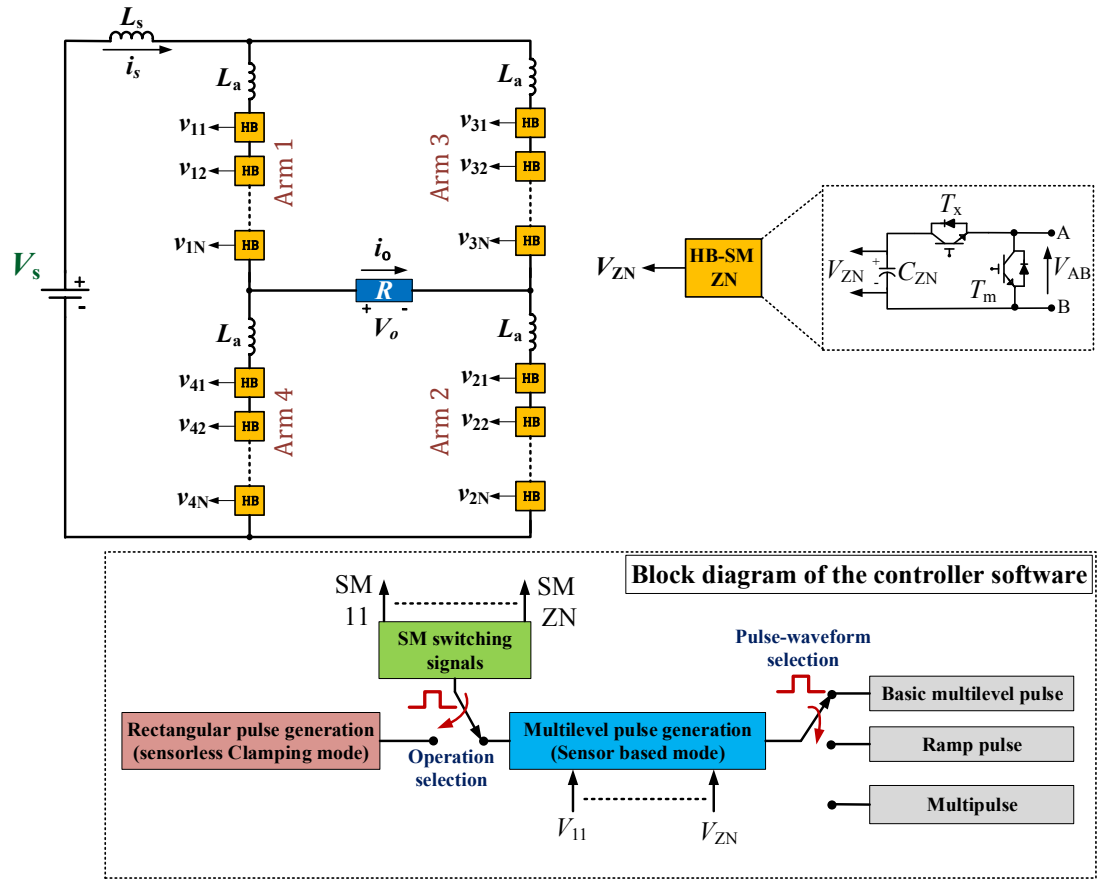


Fig.3.13. GPG topology along with the controller software block diagram.

3.2.1 Generic Pulse Waveform Generator Topology Description

The generic pulse waveform generator (GPG) topology, shown in Fig.3.13, is structured as the CPG topology shown in Fig.3.2. The only hardware difference is adding individual SM voltage sensors to measure V_{ZN}, where Z = 1, 2, 3 and 4 is the

arm number and N is the SM number in arm Z. The measured voltages are fed to the controller to assure capacitor voltage balance around $V_{ZN} = V_s/N$ while generating different waveforms [70].

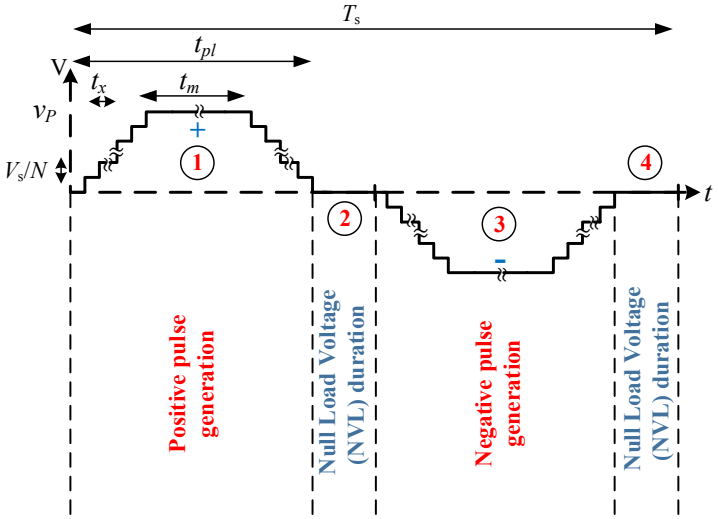


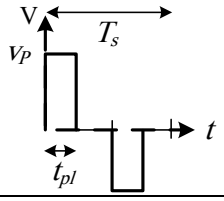
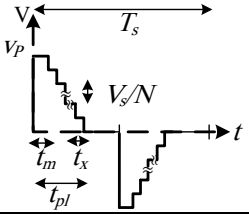
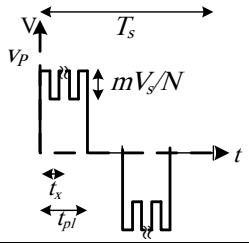
Fig.3.14. Basic multilevel pulse-waveform.

The GPG basic multilevel pulse-waveform v_P is shown in Fig.3.14, and can be defined by four sequential intervals: positive pulse, positive NLV, negative pulse, and negative NLV. Controlling the five parameters defining this basic waveform allows the generation of any desired pulse-waveform. The five parameters are: repetition time T_s, total pulse time t_{pl}, pulse plateau time t_m, SM-voltage step V_s/N, and step voltage-level applied time t_x. There are $N + 1$ voltage levels from the zero voltage-level to the pulse peak voltage V_s (neglecting IGBT ON resistance, diode voltage drops and arm inductor resistance). The positive and positive NLV intervals in the basic waveform (regions 1 and 2 in Fig.3.14, respectively) can be expressed mathematically as in (3.21):

$$v_P = \begin{cases} \sum_{n=1}^{N} \frac{nV_s}{N}, & 0 \le t < Nt_x \\ V_s, & Nt_x \le t < (Nt_x + t_m) \\ \sum_{n=1}^{N} (V_s - \frac{nV_s}{N}), & (Nt_x + t_m) \le t < t_{pl} \\ 0, & t_{pl} \le t < ½T_s \end{cases} \tag{3.21}$$

Mathematically, region 3 is the negative equivalent of region 1, while region 4 is similar to region 2. Accordingly, Table 3.3 defines the emulated conventional electroporation pulse-waveforms generated by the GPG from its basic pulse-waveform controlling attributes.

Table 3.3: Generation of conventional pulse-waveforms from multilevel pulse-waveform

	Waveform	Controlling attributes
Rectangular		With $t_{pl} = t_m$ and $t_x = 0$, all the corresponding arm SMs will be inserted/bypassed simultaneously.
Ramp		By inserting all corresponding SM capacitors for duration t_m, then bypassing them one-by-one gradually to reduce the voltage to zero in Nt_x, hence $t_{pl} = t_m + Nt_x$.
Multipulse		By setting t_{pl} as the wide pulses duration with an amplitude V_s, and the narrow pulses magnitude ($V_s - {mV_s}/{N}$) and duration t_x. m is the number of bypassed SMs in the corresponding arm.

3.2.2 GPG Operating Sequence

To generate the multilevel pulse waveform shown in Fig.3.14, each SM-voltage is continuously measured, compared with other SM-voltages in the corresponding arm, and the capacitor voltage magnitudes are sorted. The highest voltage capacitor among the available capacitors is inserted first at each voltage level during the transition from 0 to $\pm V_s$, while the lowest SM-voltage is bypassed first during the transition from $\pm V_s$ to 0. Thus, if one of the arm N capacitors is inserted, the software algorithm will select from the remaining $N - 1$ capacitors to build the next voltage level and so on, until the desired pulse waveform is created. Hence, the sequence of software algorithm steps in generating the multilevel pulse-waveform,

while assuring capacitors voltage balancing during pulse generation, can be summarised as follows (assuming all the SM-capacitors are charged to V_s/N):

1. The pulse waveform parameters are fed to the software programme namely: repetition time T_s, total pulse time t_{pl}, pulse plateau time t_m, the number of SMs N, step voltage-level, applied time t_x, and the continuous voltage measurement of the N SM-capacitors.
2. To form the first voltage-level (level-1) of the positive pulse, the capacitor voltages of arms 3 and 4 are compared and sorted. Then, the largest capacitor voltages are inserted first to form level-1.
3. After t_x the remaining $(N-1)$ capacitor voltages are compared and the highest capacitor voltages are inserted for t_x to create the second voltage-level.
4. The same process of insertion and voltage comparison is continued until reaching the pulse peak voltage at which all the N SM-capacitors are inserted. Thus the transition from 0 to $+V_s$ is completed.
5. After t_m the transition from $+V_s$ to 0 starts. Based on the measured SM-capacitor voltages the SMs are bypassed one by one, where the lowest SM-voltage it bypassed first.
6. After all arm 3 and 4 SM-capacitors contributed in positive pulse generation, they are connected to the DC supply by bypassing all the N SMs of the arm connected in series with it. Thus they are re-charged to V_s/N. As a result, the load voltage is nulled.
7. After the positive NLV duration, the steps 2 to 6 are repeated for arms 1 and 2 to generate the negative pulse polarity.

Although the default generated pulses are bipolar, the omission of either polarity during pulse generation yields unipolar pulses generation. The circuit configurations of the GPG during bipolar pulse generation are similar to those in Table 3.1.

3.2.3 Simulation Results for the GPG Converter

GPG operation is MATLAB/Simulink simulated with the parameters in Table 3.4, when generating electroporation pulse waveform shapes. By disabling the voltage

sensors, the GPG acts like the CPG generating rectangular waveforms. The individual SM-capacitance C_{ZN} is sized as in (3.18).

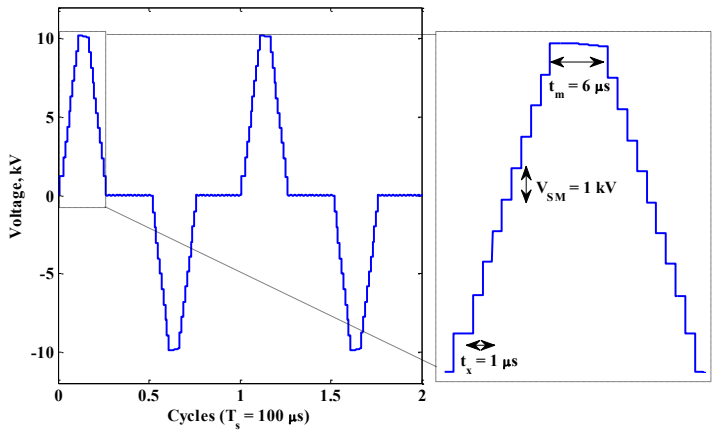
Table 3.4: Specification for GPG Simulation and Experimentation

Parameter		Simulation	Experimentation
DC input voltage	V_s	10 kV	150 V
Input inductance	L_s	1.5 mH	2.5 mH
Number of SMs/arm	N	10	3
Repetition time	T_s	100 μs	1000 μs
Arm inductance	L_a	15 μH	10 μH
Load resistance	R	500 Ω	100 Ω
SM capacitance	C_{SM}	5 μF	15 μF
Percent voltage ripple	γ	0.05	0.05
Safety factor	α	1	1

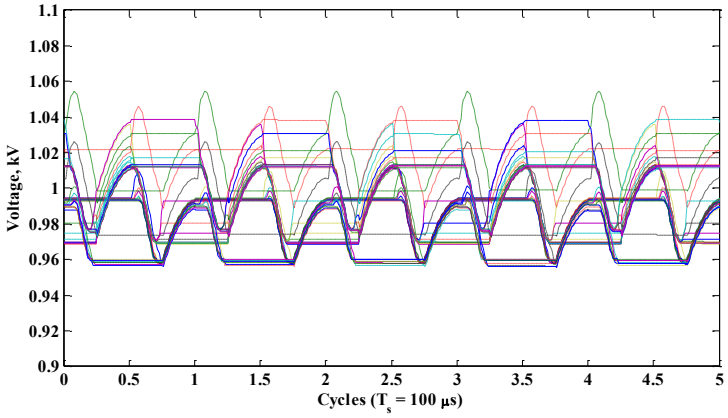
The basic GPG multilevel bipolar pulse-waveform is shown in Fig.3.15a, with $t_x = 1\mu s$ and $t_m = 6\mu s$ at a 10kHz repetition frequency, while the corresponding 40 capacitor voltages in the four arms, fluctuating around 1000V, are shown in Fig.3.15b. Combined NLV durations bipolar multilevel pulses are shown in Fig.3.15a, while unipolar multilevel pulses are shown in Fig.3.15b.

Exploiting the controllability of the basic multilevel pulse-waveform affords the possibility of generating ramp and multipulse pulse-waveforms. Fig.3.16a shows bipolar ramp pulses with $t_x = 1\mu s$ and $t_m = 6\mu s$, while its unipolar version of pulses is depicted in Fig.3.16b. With $m = 5$ and $t_x = 5\mu s$ bipolar multipulse waveforms are shown in Fig.3.16c and a unipolar version is shown in Fig.3.16d.

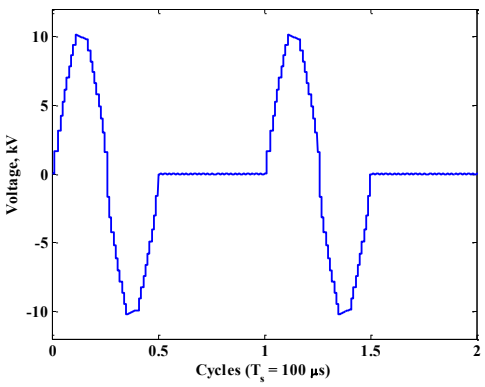
The observed small voltage drop in the pulse peak in the simulation results can be mitigated by using a safety factor $\alpha > 1$ during SMs capacitance selection.



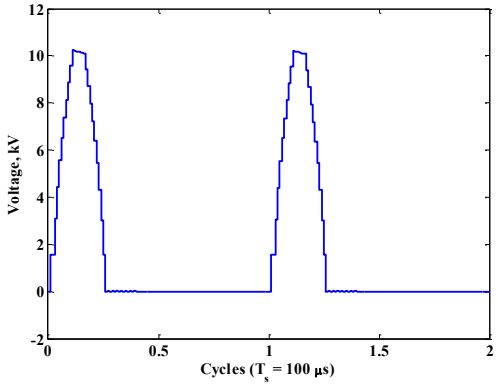
(a)



(b)



(c)



(d)

Fig.3.15. Simulation results of basic GPG multilevel HV pulse-waveform.
(a) Output voltage pulses. (b) 4 arms capacitor voltages. (c) Bipolar combined NLV durations.
(d) Positive unipolar.

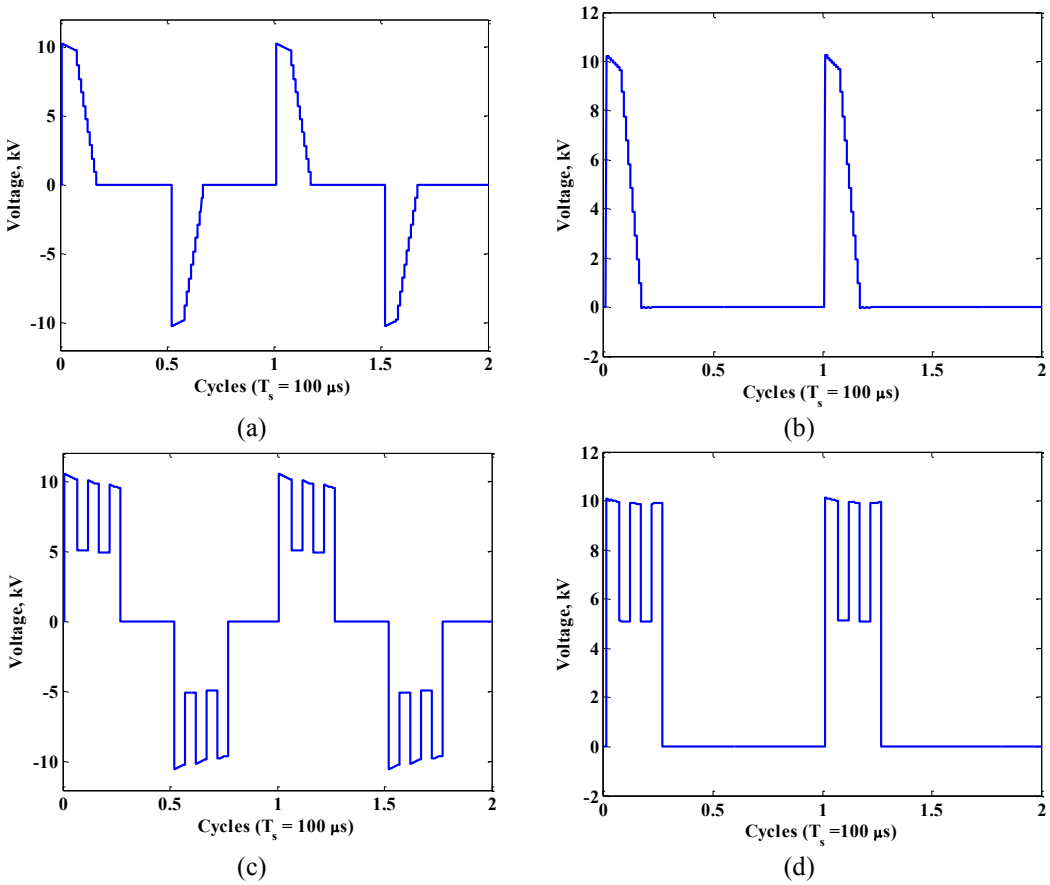


Fig.3.16. Simulation of GPG conventional HV pulses.
(a) Bipolar ramp. (b) Unipolar ramp. (c) Bipolar multipulse. (d) Unipolar multipulse.

3.2.4 Experimental Results for the GPG Converter

A proof of concept experimental rig in Fig.3.17 is used to validate the performance of the GPG and explore its software-algorithm flexibility in producing common PEF pulse-waveforms. Ultra-fast IGBT switches (STGW30NC60WD) are used, while the control algorithm was implemented with Texas Instruments' eZDSP TMS320F28335. The experimental specifications are given in Table 3.4.

The software control code follows the operating sequence detailed in section 3.2.2. Isolated voltage sensors sent capacitor measurements to the DSP via an analogue/digital port (A/D). Based on these measurements, after sorting, the DSP code decides which MMC-SM should be inserted/bypassed, sending a control ON/OFF signal through a DSP digital output port to the corresponding IGBT gate drive. The gate drive circuits (an individual isolated circuit for each IGBT switch) provide isolation between the control stage and the power stage.

The basic multilevel pulse-waveform with four positive and four negative voltage-levels is shown in Fig.3.18a with $t_x = t_m = 40\mu s$ and a 1000µs repetition time. The corresponding voltage across one capacitor in each of the 4 arms is shown in Fig.3.18b, which implies that each voltage level is 50V, so the pulse peak voltage is 150V.

Generating multilevel pulse-waveform with asymmetric positive/negative pulse durations is shown in Fig.3.18c where the positive pulse duration is twice the negative duration, with $t_x = t_m = 40\mu s$. Combined NLV durations bipolar multilevel pulses are shown in Fig.3.18d with $t_x = t_m = 40\mu s$, while negative unipolar multilevel pulses are shown in Fig.3.18e.

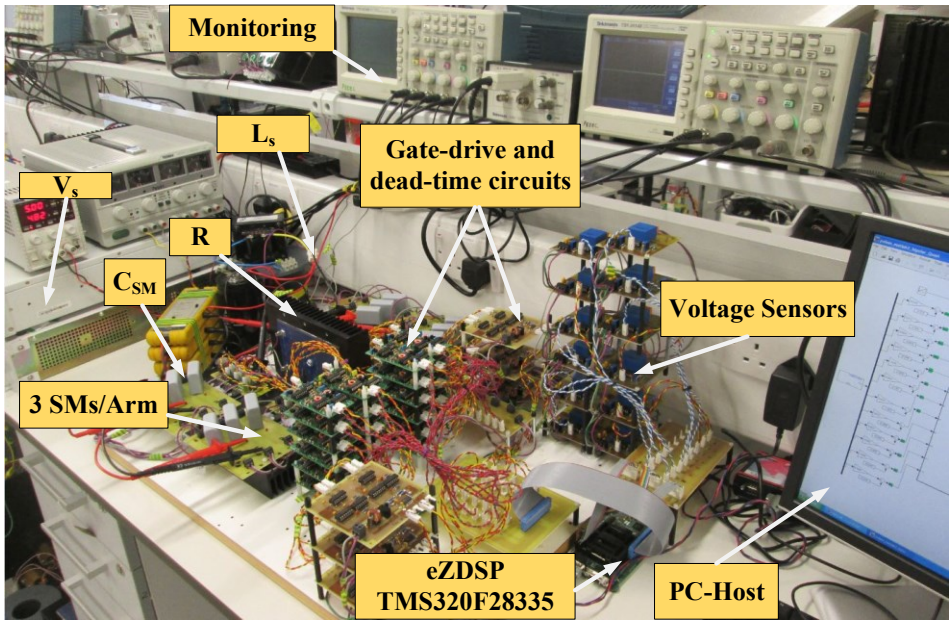


Fig.3.17. The proof of concept GPG experimental rig.

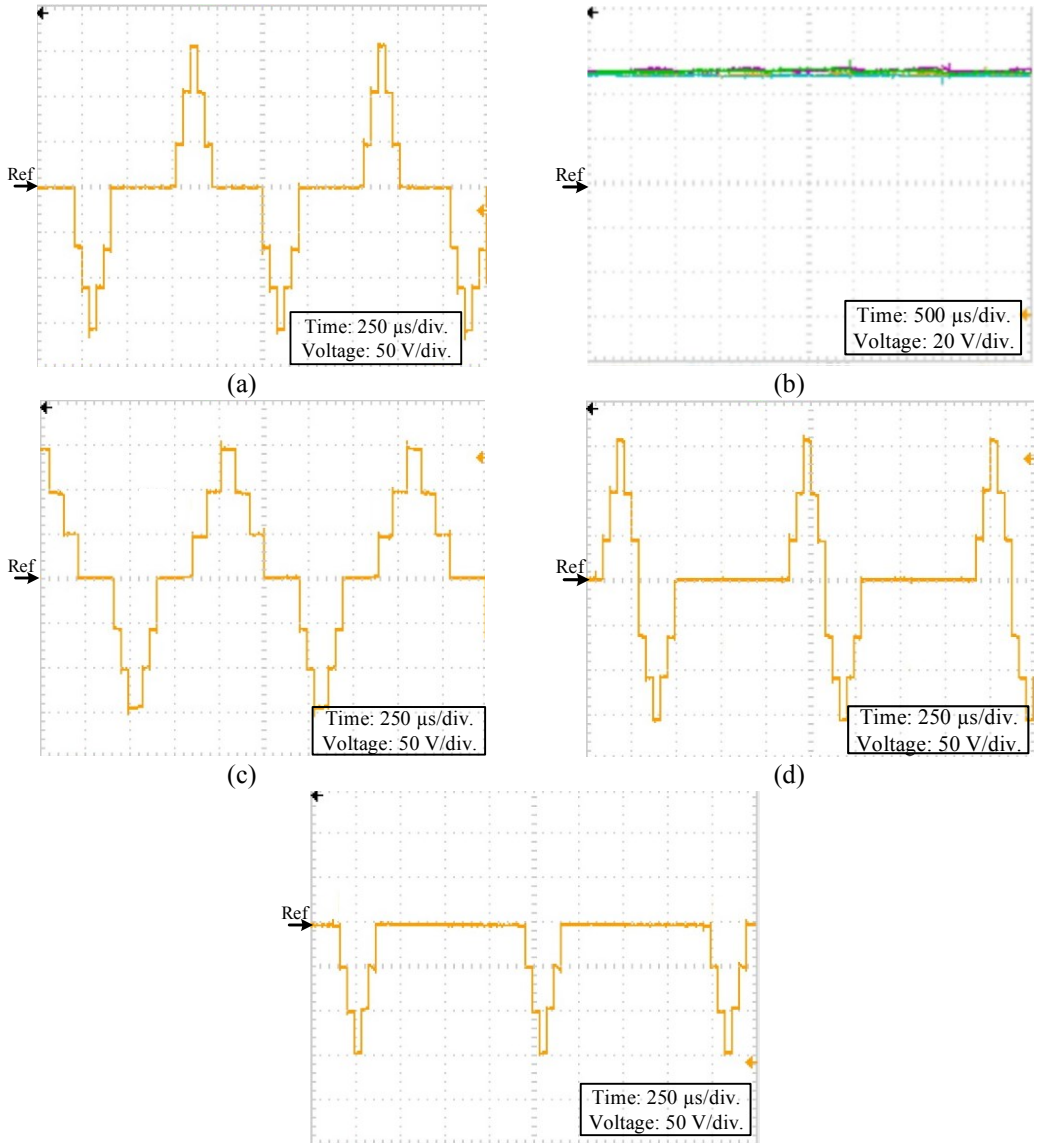


Fig.3.18. Experimental results for GPG basic multilevel pulses generation with different characteristics with voltage-levels of 50V. (a) Output voltage pulses with $t_x = t_m = 40\mu s$. (b) One SM capacitor voltage from each of the 4 arms. (c) Bipolar asymmetrical pulses. (d) Combined NLV symmetrical durations pulses. (e) Negative unipolar pulses.

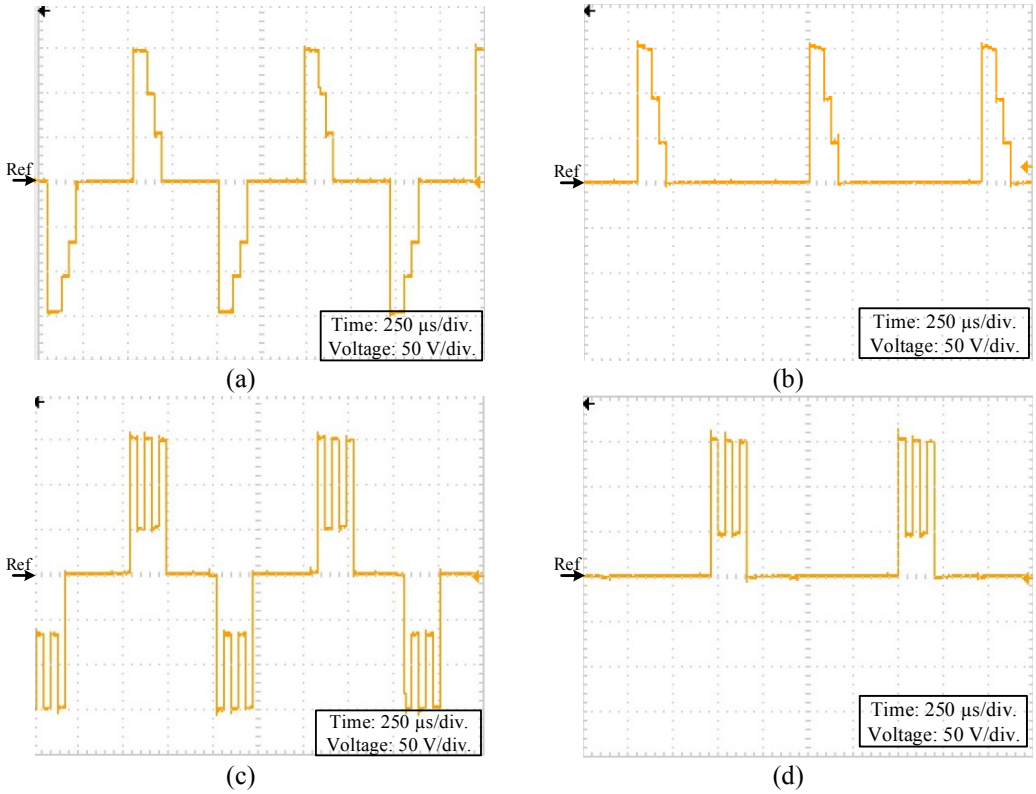


Fig.3.19. Experimental results for GPG conventional pulse waveforms generation with voltage-levels of 50V. (a) Bipolar ramp pulses with $t_x = 40\mu s$ and $t_m = 80\mu s$. (b) Positive unipolar ramp pulses with $t_x = 40\mu s$ and $t_m = 80\mu s$. (c) Bipolar multipulse with $m = 2$ and $t_x = 40\mu s$. (d) Positive unipolar multipulse with $m = 2$ and $t_x = 40\mu s$.

Bipolar ramp pulses with $t_x = 40\mu s$ and $t_m = 80\mu s$ are shown in Fig.3.19a while the unipolar ramp version is shown in Fig.3.19b. Multipulse pulse-waveforms of bipolar and unipolar types with $m = 2$ and $t_x = 40\mu s$ are shown in Fig.3.19c and Fig.3.19d, respectively.

The GPG topology, which originated from the CPG after adding individual SM voltage sensors, can generate a wide range of pulse waveforms with the appropriate software algorithm. Both the CPG and GPG topologies are H-bridge structured which allows full utilisation of the HV DC input. But, the footprint of these topologies can be large and costly, especially the GPG with the added sensors.

3.3 Universal Pulse Waveform Generator

In [71] a new phase-leg structure for MMC based DC-AC converters is presented based on the HVDC dual active bridge (DAB) which acts as a DC-DC transformer in HVDC transmission applications. Each phase-leg [71] consists of two arms. The

upper arm is called the transition arm (formed of series connected MMC SMs) and the lower arm is called the bi-state arm (formed of series connected IGBTs) as shown in Fig.3.20. If the transition arm is replaced by another bi-state arm, the converter acts like two-level converter which generates a square AC voltage waveform.

The transition arm [71] facilitates controlled stepped transitions between the positive and negative HVDC rails when synthesizing the output AC voltage that will be imposed on the DAB AC transformer, hence, a quasi two-level voltage waveform is generated with reduced dv/dt. The dv/dt reduction reduces the voltage stresses on the used AC transformer and the emitted electromagnetic interference (EMI) [72].

By utilising the concept of generating multilevel voltage transitions [72] with some operating modifications, HV pulse generation can be achieved. The proposed PG can generate all the conventional pulse-waveforms, therefore, to distinguish it from the GPG in section 3.2, it is termed the universal pulse waveform generator (UPG).

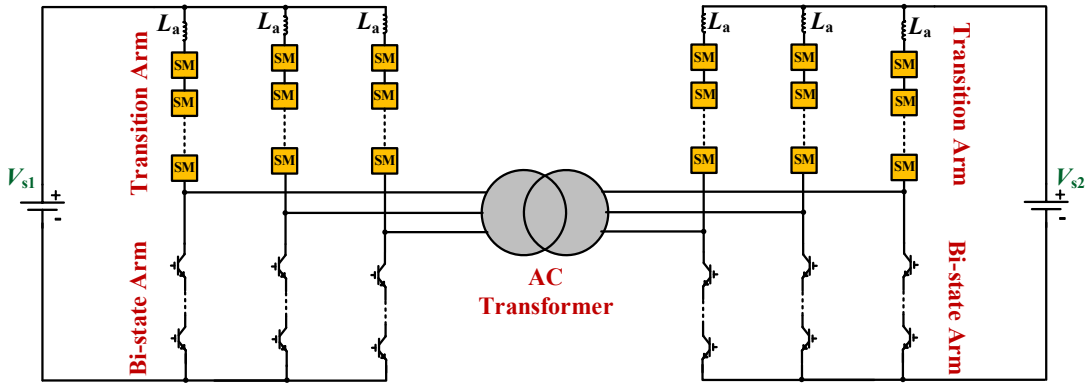


Fig.3.20. Transition arm converter in a dual active bridge application [71].

3.3.1 UPG Topology Description

The UPG converter topology shown in Fig.3.21 consists of four arms forming an H-bridge. The two upper arms, Arm1 and Arm2, are the transition arms formed of N series connected HB-MMC SMs while the two lower arms, Arm3 and Arm4, are the bi-state arms formed by series connected IGBT switches. Each transition arm has a small arm series inductor L_a to suppress the inrush current between SM-capacitors during their insertion process and to control SM capacitor charging when connected to the DC input supply V_s.

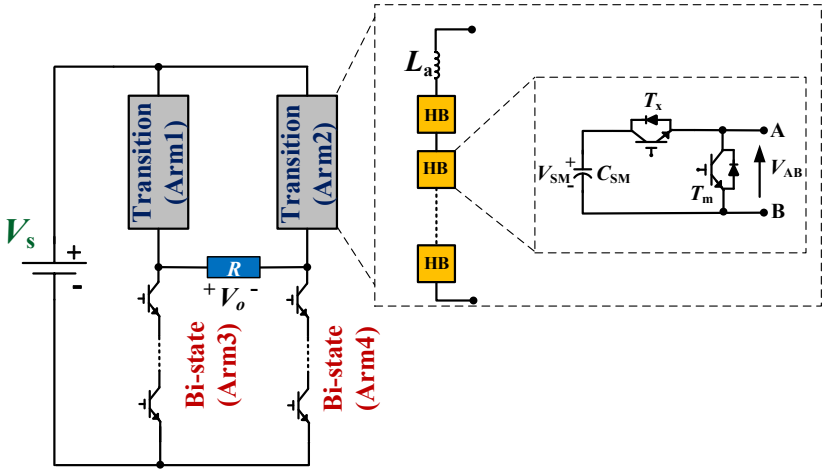


Fig.3.21. UPG converter topology.

Each HB-SM can operate in any of three switch states; bypass, insertion and idle, as shown in Fig.2.12. Therefore, the two transition arms have tri-state modes. Since the two lower arms are formed from series connected IGBTs, they can operate only in bi-state modes (either turned on or off).

For UPG converter operation, each arm must be able to withstand the DC-link voltage V_s. Consequently, the voltage of the HB-MMC SM capacitors in the transition arm should be balanced and the capacitor voltages fluctuate around V_s/N. The MMC sorting and rotating technique is adopted, where each capacitor voltage is continuously measured, compared with other SM capacitor voltages in that corresponding arm, and voltage sorted. The highest voltage capacitor among the available capacitors is inserted first at each voltage level during the transition from 0 to $\pm V_s$, while the lowest SM-voltage is bypassed first during the transition from $\pm V_s$ to 0.

The UPG can generate the basic multilevel pulse-waveform V_P shown in Fig.3.14, with the merit of reduced SMs and voltage sensor numbers in comparison with the GPG. Thus the UPG converter has reduced footprint and cost [73]. As illustrates in Table 3.3, manipulating the multilevel pulse waveform controlling parameters (T_s, t_{pl}, t_m, V_s/N, and t_x) allows the generation of conventional pulse waveforms.

3.3.2 UPG Operation Principle

The UPG generated pulse-waveforms, are normally bipolar, where the SMs in Arm2 are responsible of generating the positive pulse-duration, while the SMs in Arm1 are responsible for generating the negative-pulse duration. Disabling a specific transition arm will lead to generating unipolar pulse-waveforms with the desired polarity.

As discussed, there are four intervals for a bipolar pulse-waveform generation cycle. UPG operation for each interval is shown in Table 3.5 and can be explained as: during the positive pulse generation interval, the two bi-state arms are OFF, Arm1 SMs are bypassed and Arm2 SMs are inserted. Consequently, the equivalent series connected capacitor C_{SM}/n is inserted across the load producing a voltage of $+nV_s/N$, where n is the number of the inserted SMs. Similarly, for negative pulse generation, the two bi-state arms are OFF, Arm2 SMs are bypassed and Arm1 SMs are inserted. Hence, a series connected capacitor C_{SM}/n is inserted across the load producing voltage $-nV_s/N$. During NLV intervals the SM-capacitors of Arm2 or Arm1, for positive or negative pulses respectively, are charged from the DC-link supply, while the load voltage is nulled. The equivalent inserted capacitor C_{SM}/N charges to V_s.

Turning ON/OFF the bi-state arms assured soft-switching operation, zero voltage switching (ZVS), that is, the series-connected switches are switched only when the voltage across the bi-state arm is near zero. After positive/negative pulse polarity generation, charging of Arm2/Arm1 is the next interval which requires turning on the bi-state Arm4/Arm3. During charging of one of the transition arms, the other transition arm is idled, and the charging SM-capacitors are inserted. Therefore, the voltage across the corresponding bi-state arm remains close to zero, hence it can be turned on allowing the input supply to charge the SMs. During the charging interval, the charging transition arm voltage reaches the supply voltage V_s, hence, the voltage difference across the corresponding bi-state arm is zero, and therefore, the bi-state arm can be turned off in a ZVS state.

Idling one transition arm during the NLV intervals (or, the charging interval of the other transition arms) will not prevent charging of its capacitor-SMs, through T_x diode, when starting the converter. At steady-state, the idled arm SM-capacitor voltages are charged to the supply voltage V_s, and since they are not participating in the pulse generation, the arm voltage will not change, hence the idled arm can be viewed as an open circuit during charging of the other transition arm, as shown in Table 3.5.

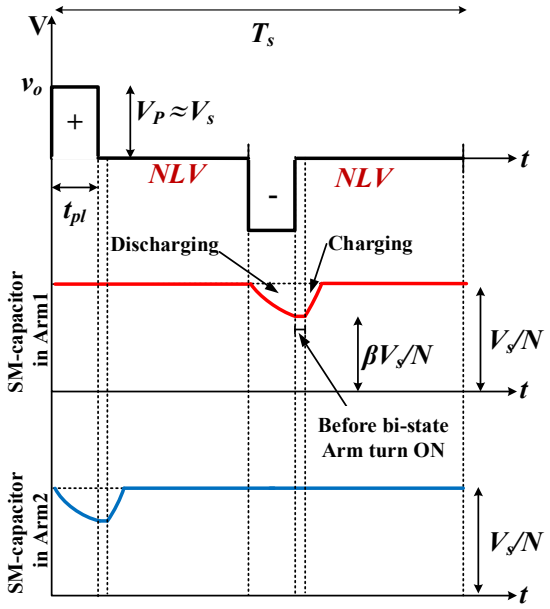
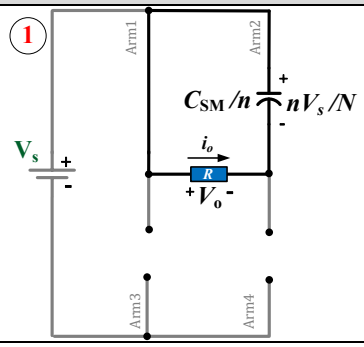
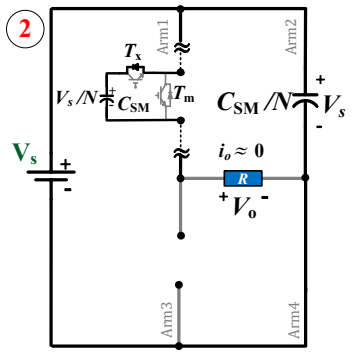
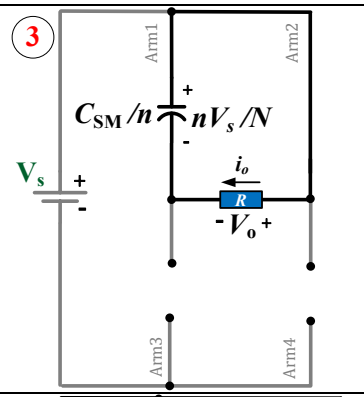
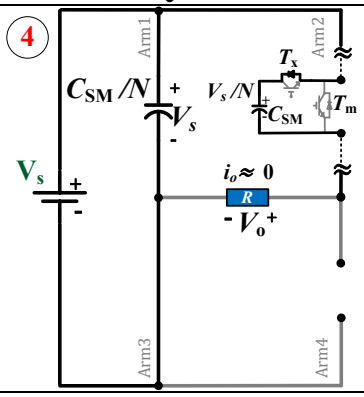


Fig.3.22. Individual SM-capacitors of Arm1 and Arm2 charging and discharging sequence for generating a rectangular bipolar pulse.

Table 3.5: Operating Principle of the UPG

	Circuit configuration	Sequence of operation
Positive Pulse		• bi-state arms are turned OFF. • Transition Arm1 SMs are bypassed to provide a path for transition Arm2 discharging SM-capacitors. • Transition Arm2 SMs are inserted according to the desired pulse-waveform. • A positive pulse is formed across the load.
Positive NLV		• bi-state arms are kept OFF. • All transition Arm2 SM-capacitors are inserted while transition Arm1 is put in idle state. • bi-state Arm4 is turned ON, keeping Arm3 OFF. • Charging the series connected SM-capacitors to the supply voltage. • bi-state Arm4 is turned OFF.
Negative Pulse		• The bi-state arms are kept OFF. • Transition Arm2 SMs are bypassed to provide a path for transition Arm1 discharging SM-capacitors. • Transition Arm1 SMs are inserted according to the desired pulse-waveform. • A negative pulse is formed across the load.
Negative NLV		• bi-state arms are kept OFF. • Transition Arm1 SM-capacitors are inserted while transition Arm2 is put in idle state. • bi-state Arm3 is turned ON, keeping Arm4 OFF. • Charging the series connected SM-capacitors to the supply voltage. • bi-state Arm3 is turned OFF.

3.3.3 UPG Parameters Selection

Since a bipolar rectangular pulse-waveform represents the case where all the SM-capacitors in the transition arms (Arm1 and Arm2) are to be inserted, giving a step from the zero voltage-level to $\pm V_s$, its generation will be considered in the following analysis and when SM-capacitor sizing.

UPG operation for each pulse polarity can be illustrated from an energy conversion perspective. Assume the individual SM-capacitors are pre-charged to V_s/N. During the positive pulse interval some of the energy stored in Arm2 capacitors is transferred to the load during pulse generation time t_{pl}. Hence, Arm2 capacitors partially discharge and their voltage reduces accordingly. This energy reduction is compensated by re-charging Arm2 individual SM-capacitors to V_s/N during the positive NLV interval, as illustrated in Fig.3.22. The same procedures occur during the negative-pulse interval through Arm1 SM-capacitors. Therefore, the energy is transferred from the input DC supply to the load in two stages, first the input DC supply charges the corresponding SM-capacitors, then the charged SM-capacitors partially discharge into the load. The energy transferred to the load E_L during the pulse time is

$$E_L = P_L t_{pl} \tag{3.22}$$

where P_L is the power consumed by the load R during pulse time t_{pl} which can be expressed as

$$P_L = \frac{V_o^2}{R} \tag{3.23}$$

where V_o is the load rms voltage which can be calculated from Fig.3.22 as

$$V_o = \sqrt{\frac{1}{T_s}\int_0^{T_s} v_o^2(t)\, dt} \tag{3.24}$$

thus

$$V_o = \sqrt{\frac{2t_{pl}}{T_s}}V_P \tag{3.25}$$

Neglecting IGBTs voltage drops and the internal resistance of L_a, then $V_P \cong V_s$, hence the load energy per pulse polarity is

$$E_L = \frac{t_{pl}^2 V_s^2}{T_s R} \tag{3.26}$$

The energy transferred to the load is equal to the difference between the initial energy stored in the individual arm capacitors and the energy remaining after pulse generation

$$\Delta E_{SM} = E_{SM}^{i} - E_{SM}^{p} \tag{3.27}$$

where ΔE_{SM} is the energy difference in an individual SM-capacitor in the discharging arm, E_{SM}^{i} is the initial energy stored, and E_{SM}^{p} is the remaining energy per SM capacitor, such that

$$E_{SM}^{i} = ½C_{SM}\frac{V_s^2}{N^2} \tag{3.28}$$

and

$$E_{SM}^{p} = ½C_{SM}\frac{\beta^2 V_s^2}{N^2} \tag{3.29}$$

where β is the per unit remaining capacitor voltage after pulse generation as illustrated in Fig.3.22. Hence:

$$\Delta E_{SM} = ½C_{SM}\frac{V_s^2}{N^2} - ½C_{SM}\frac{\beta^2 V_s^2}{N^2} \tag{3.30}$$

Thus the energy difference in the discharging transition arm of N series SMs is

$$\Delta E_{Arm} = N \times \Delta E_{SM} = ½C_{SM}\frac{(1-\beta^2)V_s^2}{N} \tag{3.31}$$

where ΔE_{Arm} is the energy difference in the arm corresponding to a specific pulse polarity. Neglecting semi-conductor losses, then $\Delta E_{Arm} = E_L$, hence the SM-capacitance is

$$C_{SM} = \frac{2t_{pl}^2 N}{(1-\beta^2)T_s R} \tag{3.32}$$

Denoting $\delta = t_{pl}/T_s$, the pulse on-state duty ratio (3.32) yields

$$C_{SM} = \frac{2N\delta t_{pl}}{(1-\beta^2)R}\alpha \tag{3.33}$$

where $\alpha > 1$ is a safety factor to account for neglected losses. C_{SM} can be tailored to produce an acceptable pulse peak voltage drop for a given load and pulse characteristic (increase C_{SM} to decrease the voltage drop).

The SM-capacitor per unit voltage drop, $(1-\beta)$, specifies the efficiency of the resonate recharging of the SM-capacitors. The resonant losses, related to the throughput power, are approximately the per unit drop, squared, viz. $(1-\beta)^2$. For

example, with 10% capacitor voltage drop, the recharging losses are 1% the average power of the pulse causing the drop. These losses are dissipated in the charging circuit resistance and the bi-state arm devices as on-state losses. These device losses are mitigated by the fact that the bi-state arm devices do not incur switching losses; their switching is at zero voltage, ZVS. Consequently, the total average power P_{tot} associated with the applied HV pulses with repetition frequency f_s, can be calculated as (3.34) for bipolar pulses, and halved for unipolar pulses.

$$P_{tot} = \frac{2t_{pl}^2 V_s^2}{R} f_s^2 \tag{3.34}$$

The arm inductor L_a in series with the MMC SMs in HVDC applications has two functions; suppressing the circulating current between SMs and limiting the DC short circuit current [58]. Although, the proposed UPG converter topology adopts the technology of an MMC-HVDC converter, the operating principle is different, and DC-link short circuit blocking is not relevant. But, small arm inductance is preferred in each transition arm (Arm1 and Arm2) such that the inrush current is suppressed when inserting the SMs in series across the load during discharging or across the DC supply during charging. Resonance between L_a and the arm capacitors should be avoided [70]. Hence, the device switching frequency should be sufficiently distant from the resonance frequency of the equivalent LC circuit to avoid exciting resonance currents. Therefore, based on the designed equivalent arm capacitance and repetition time, an estimation of the inductance of L_a is

$$L_a < \frac{NT_s^2}{(2\pi)^2 C_{SM}} \tag{3.35}$$

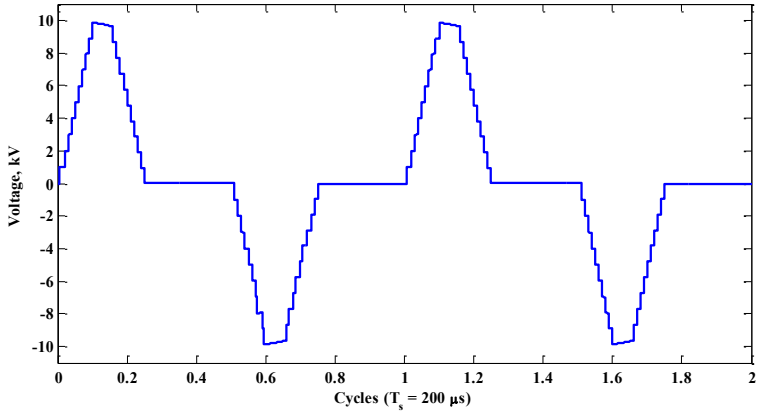
3.3.4 Simulation Results for the UPG Converter

The UPG operation is MATLAB/Simulink simulated, with the parameters given in Table 3.6 for generating electroporation pulse waveform shapes. The SM-capacitance C_{SM} is calculated based on (3.33), while (3.35) is used to estimate the arm inductance L_a. The number of the IGBT switches in bi-state arms Arm3 and Arm4, is $N = 10$. The simulations assess the ability of the UPG to mimic the commonly used pulse-waveforms in PEF applications and the flexibility of the converter to

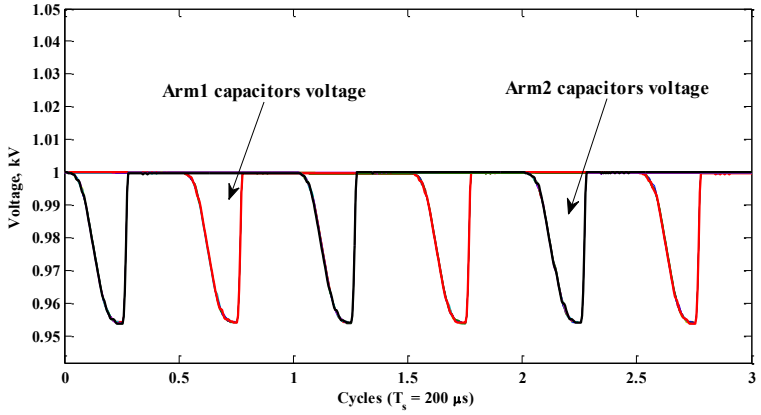
control the generated pulse attributes via controller software-algorithm, without any physical changes to the power topology or the load connection.

Table 3.6: Specification for UPG Simulation and Experimentation

Parameter		Simulation	Experimentation
DC input voltage	V_s	10 kV	150 V
Number of SMs/arm	N	10	3
Repetition frequency	f_s	5 kHz	1.8 kHz
Arm inductance	L_a	2 µH	1 µH
Arm resistance	r_a	0.1 Ω	0.2 Ω
Load resistance	R	1 kΩ	100 Ω
SM capacitance	C_{SM}	5 µF	15 µF
Per unit remaining capacitor voltage	β	0.95	0.9
Safety factor	α	2	2



(a)



(b)

Fig.3.23. Simulation results for basic UPG multilevel pulse-waveform.
(a) Output bipolar HV pulses. (b) Arm1 and Arm2 capacitor voltages.

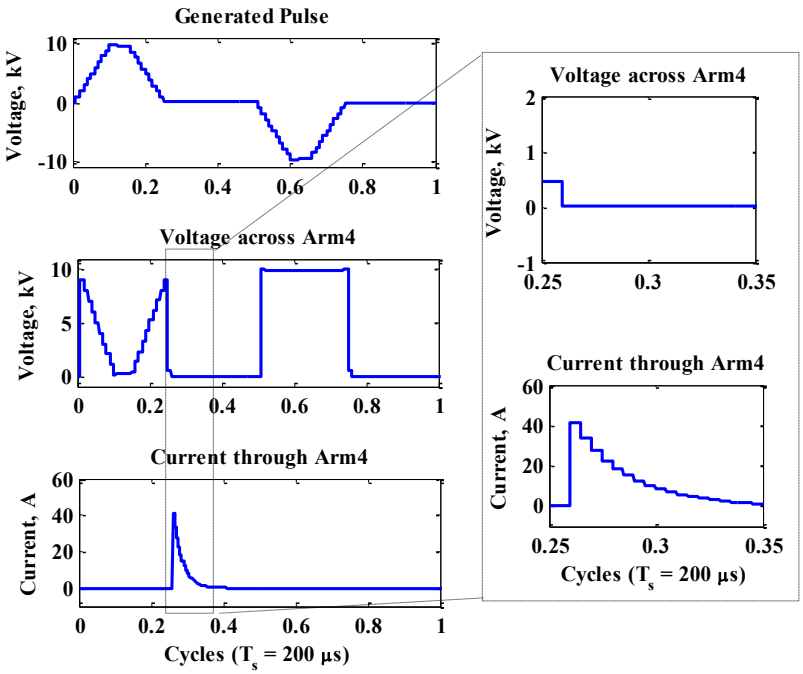
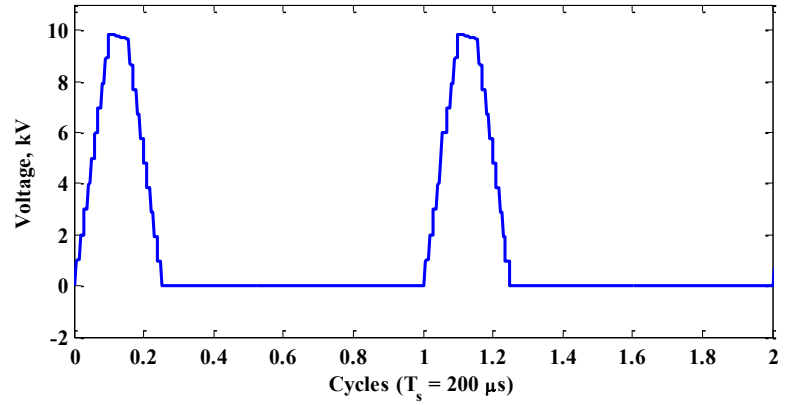


Fig.3.24. Voltage across and current through bi-state Arm4 during positive pulse generation via Arm2 SM-capacitors with zoomed view of Arm4 voltage and current during Arm2 capacitors re-charging.

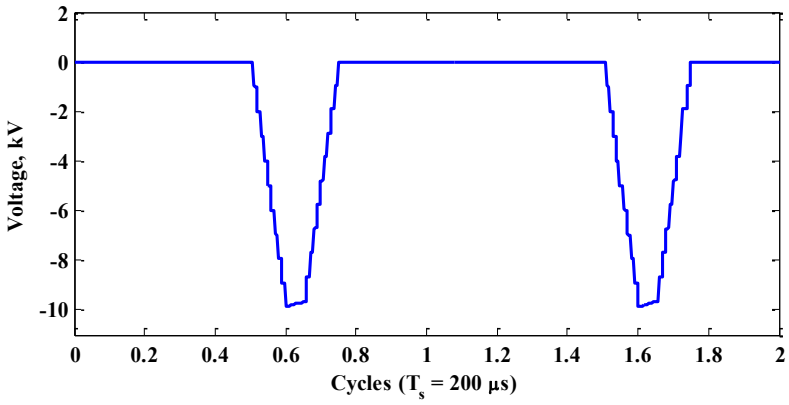
With a repetition frequency of 5kHz, the basic UPG multilevel pulse-waveform is shown in Fig.3.23. Fig.3.23a shows the generated voltage pulse with $t_x = 2\mu s$, $t_m = 14\mu s$ and $t_{pl} = 50\mu s$. The SM-voltages of Arm1 and Arm2 are shown in Fig.3.23b. In Fig.3.23b, Arm2 contributes to the positive pulse generation while Arm1 contributes to the negative pulse generation. The SM-capacitors charge to the 1kV after their voltage has decreased during discharge across the load.

The voltage across and the current through the bi-state Arm4 during one cycle of pulse generation is shown in Fig.3.24. When the voltage across Arm4 is near zero, the bi-state arm switches are turned on allowing capacitor charging current to flow. After the SM-capacitors are charged, the current reaches zero and the voltage across the bi-state arm is zero, hence, the arm switches can be turned off. During negative pulse generation, the bi-state arm is maintained off and its voltage supporting is V_s as shown in Fig.3.24.

Fig.3.25a shows the generation of a positive unipolar multilevel pulse-waveform, while the negative counterpart is depicted in Fig.3.25b. Since the two transition arms can operate independently, not only a certain polarity can be omitted, but it can be generated with different characteristics. For example in Fig.3.26a, the positive pulse is generated with $t_x = 2\mu s$, $t_m = 24\mu s$ and $t_{pl} = 60\mu s$ while the negative pulse is generated with $t_x = 2\mu s$, $t_m = 2\mu s$ and $t_{pl} = 38\mu s$. Since the positive pulse duration is longer, the decrease in the SM voltages of Arm2 is more than that for Arm1, see Fig.3.26b.

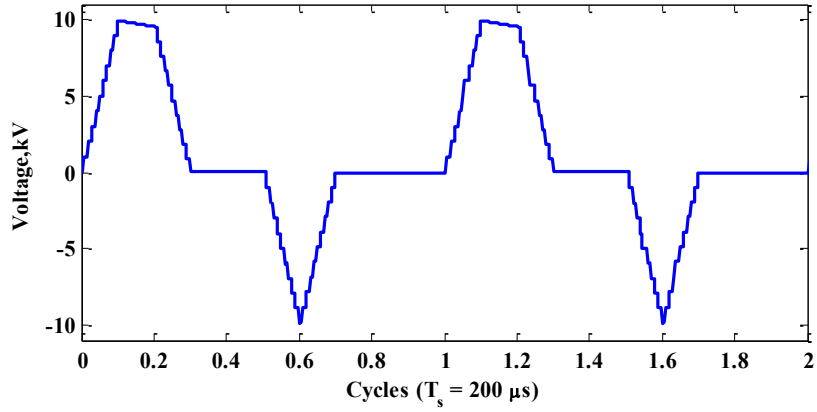


(a)

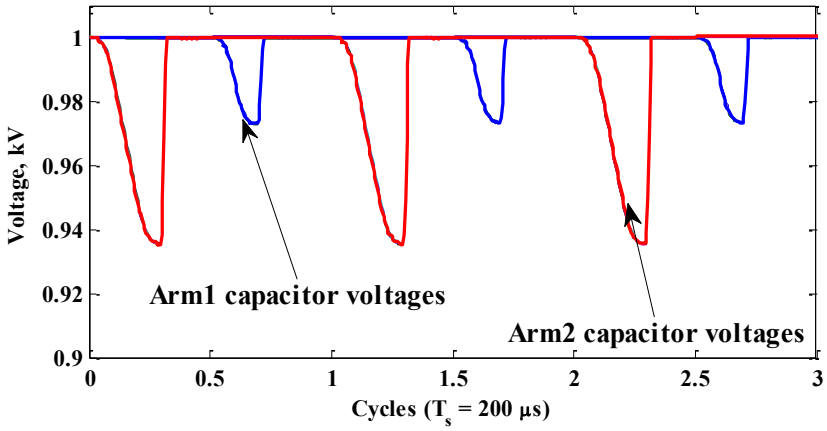


(b)

Fig.3.25. Simulation of unipolar UPG multilevel pulses.
(a) Positive. (b) Negative.



(a)



(b)

Fig.3.26. Simulation of asymmetric bipolar UPG multilevel pulses.
(a) Output bipolar HV pulses and (b) Arm1 and Arm2 capacitor voltages.

With $t_x = 0$ and $t_m = t_{pl} = 10\mu s$, a rectangular pulse can be generated. The simulation results of bipolar rectangular pulses are shown in Fig.3.27a. Generating positive unipolar and combined NLV durations rectangular pulses is explored in Fig.3.27b and Fig.3.27c, respectively, with 10µs positive and negative pulse durations.

The features of controlled dv/dt in the basic generated multilevel pulse waveform and the conventional rectangular pulse waveform can be combined as shown in Fig.3.28a and Fig.3.28b, with a 10kHz repetition frequency. The exploitable lower value of t_x is limited by switching device turn on and off delay times. In Fig.3.28a t_x is 0.1µs (viable with SiC 1700V, 45mΩ MOSFETs, with 50ns turn on and off delays) while t_m is 5µs, hence the total rise time is much shorter than the plateau time. If a faster rise time is required, grouping of the SMs can be employed. As

shown in Fig.3.28b, to achieve a rise time of 0.3µs, the ten SMs are voltage sorted into three groups, two groups of 3 SMs and one group of 4 SMs.

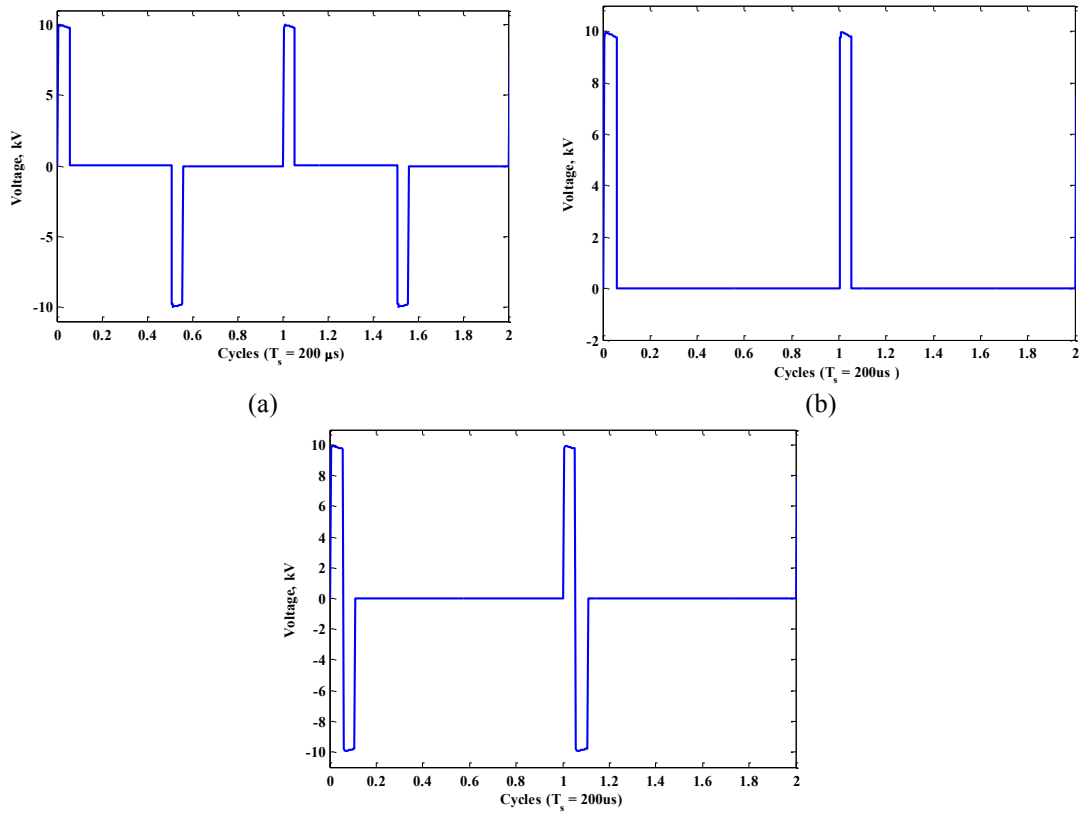
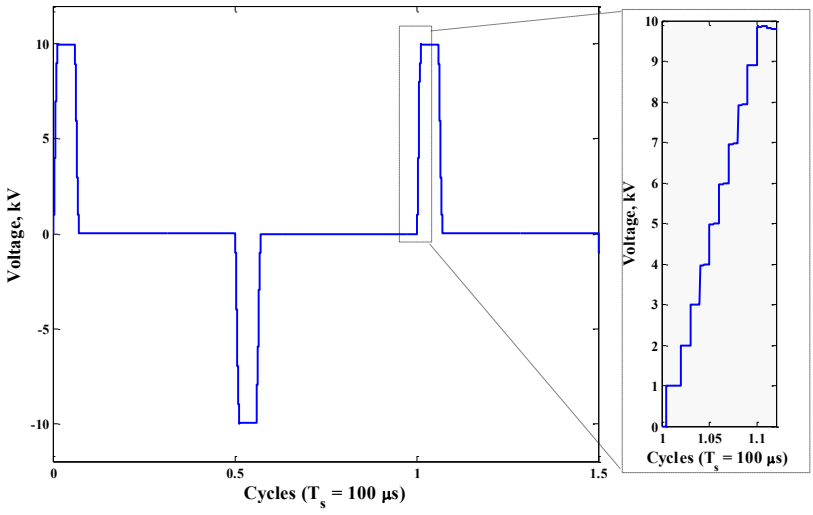
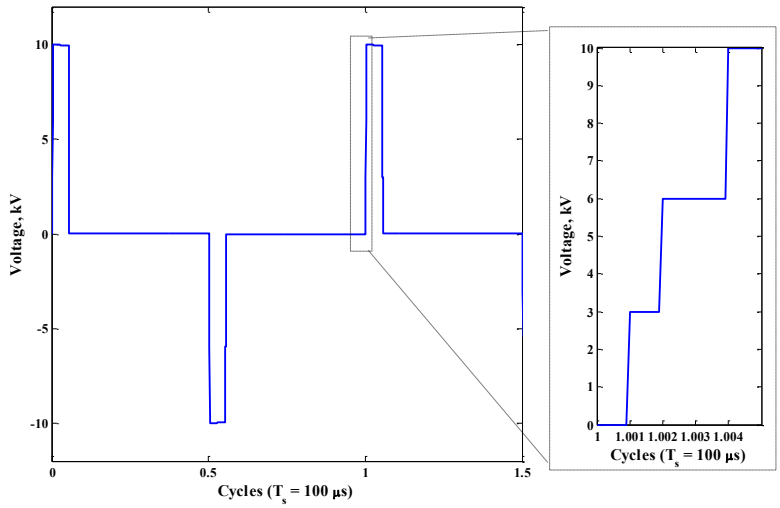


Fig.3.27. Simulation of UPG rectangular output HV pulses.
(a) Bipolar. (b) Positive unipolar. (c) Combined NLV durations.

Exploiting the flexibility afforded by the generated basic multilevel pulse-waveform from the UPG allows ramp generation and combined wide and narrow pulse-waveforms. Such waveforms can be generated with either bipolar or unipolar polarities. With $t_x = 2\mu s$, $t_m = 10\mu s$, Fig.3.29a shows bipolar ramp pulses and Fig.3.29b shows positive unipolar ramp pulses. Consequently, with $m = 5$ and $t_x = 10\mu s$, bipolar combined wide and narrow pulses are shown in Fig.3.29a and the negative unipolar version is shown in Fig.3.29b.



(a)



(b)

Fig.3.28. Simulation of UPG 10 kHz multilevel rectangular HV pulses with $t_x = 0.1\mu s$ and $t_m = 5\mu s$. (a) Without SMs grouping. (b) With SMs grouping.

3.3.5 Experimental Results for the UPG Converter

The proof of concept UPG power circuit from Fig.3.21 shown in Fig.3.30, uses IGBT switches (STGW30NC60WD) for the HB-MMC arms which have antiparallel diodes, while the bi-state arms use Infineon IGW60T120 IGBTs. The control algorithm is implemented with Texas Instruments' eZDSP TMS320F28335 to generate the required gating signals for the UPG switches in the four arms.

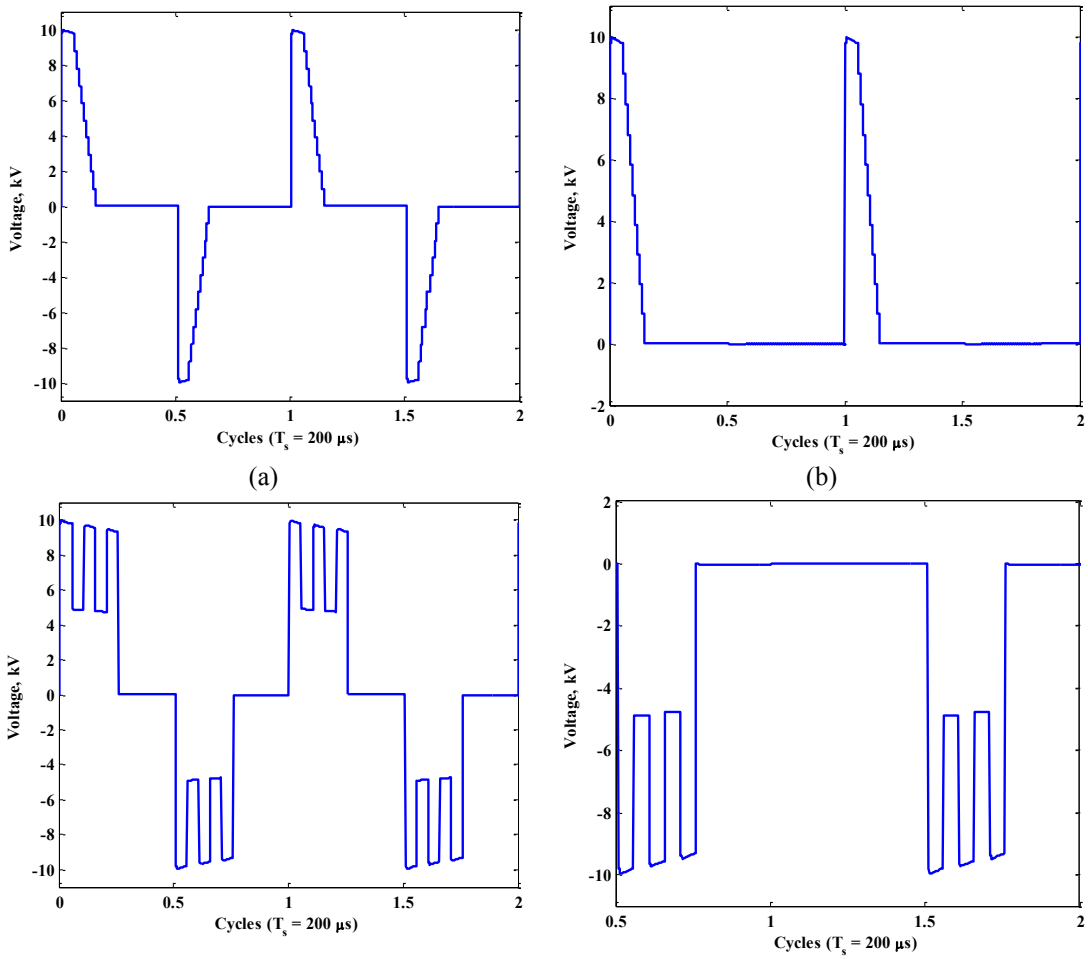


Fig.3.29. Simulation of GPG conventional HV pulses.
(a) Bipolar ramp. (b) Unipolar ramp. (c) Bipolar multipulse. (d) Unipolar multipulse.

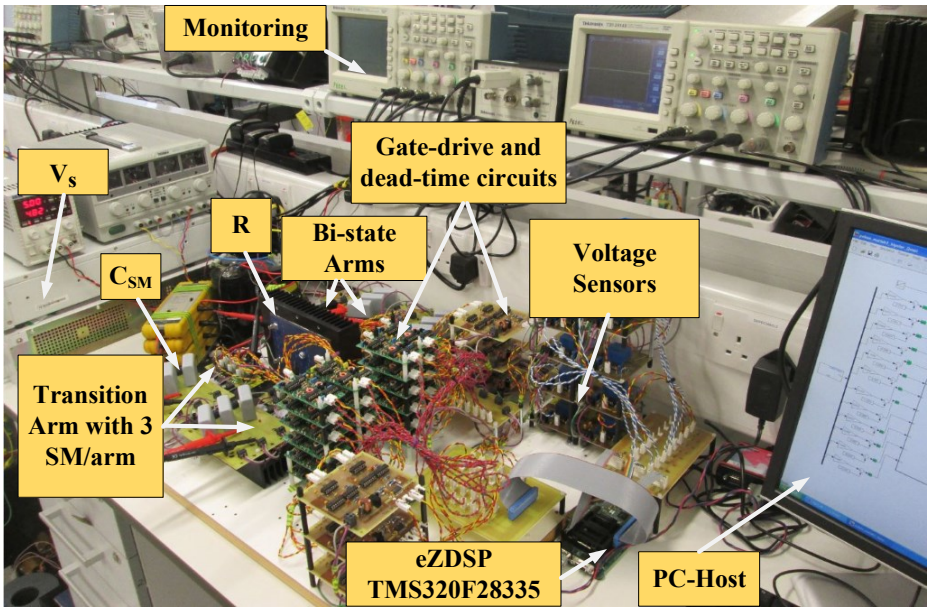


Fig.3.30. The proof of concept UPG experimental rig.

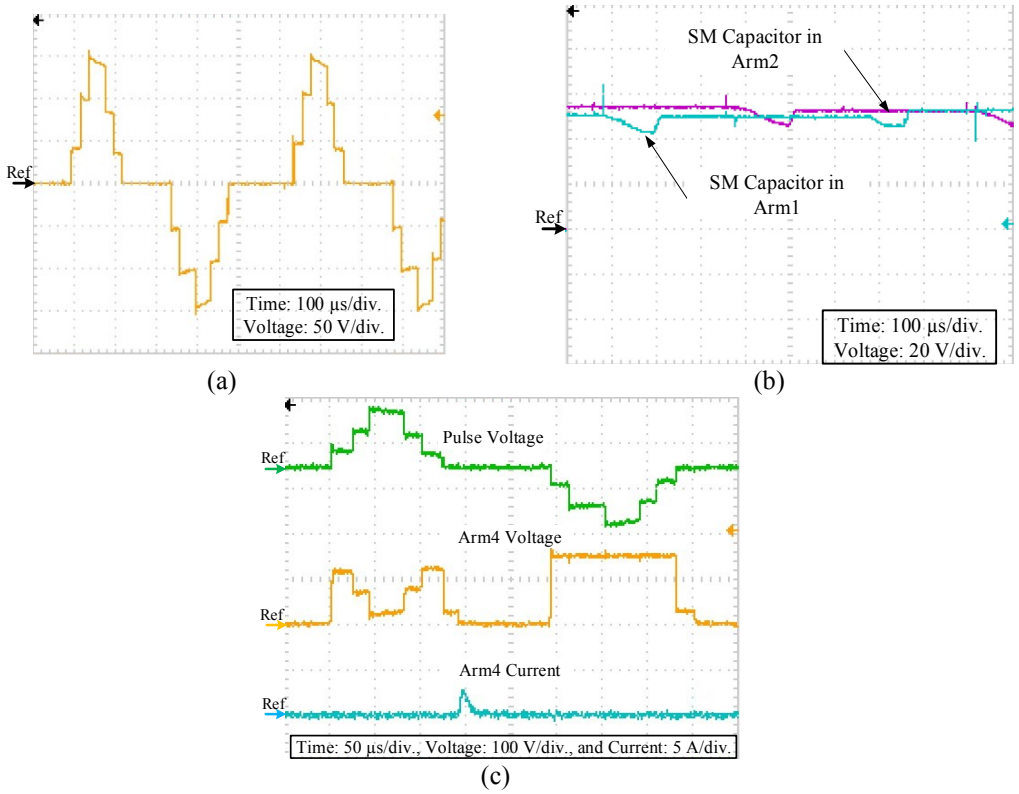


Fig.3.31. Experimental results for UPG basic multilevel pulses generation with a voltage-level of 50V. (a) Output voltage pulses. (b) One SM capacitor voltage from each of the 2 transition arms. (c) Voltage across and current through bi-state Arm4 during one cycle of pulse generation via Arm2 SM-capacitors.

The experimental specifications are given in Table 3.6. The experimentally generated four-level basic multilevel pulse-waveform is shown in Fig.3.31 with a repetition frequency of 1.8kHz. The output voltage pulses are shown in Fig.3.31a with $t_x = 20\mu s$, $t_m = 40\mu s$ and $t_{pl} = 120\mu s$, while the SM-capacitor voltage from Arm1 and Arm2 are in Fig.3.31b. Since the input supply voltage is 150V, the SM-capacitors charge to 50V, then during the associated pulse time the corresponding transition arm capacitors discharge across the load reducing SM-capacitor voltage to 44V. Fig.3.31c shows the waveforms of voltage across and the current through the bi-state arm Arm4 during a complete cycle of the generated pulse. The waveforms reveal that the bi-state arm is turned ON/OFF only when the voltage across the arm is near-zero, thereby yielding ZVS.

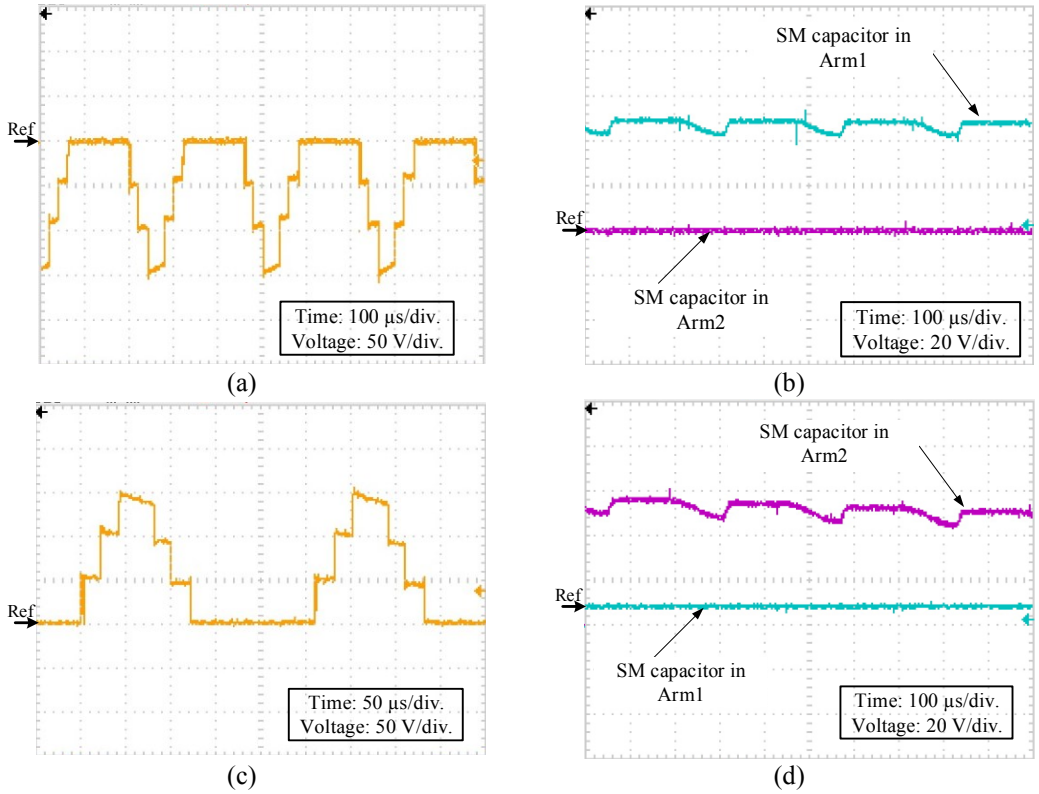


Fig.3.32. Experimental results for UPG unipolar multilevel pulses generation with voltage-level of 50V. (a) Negative polarity pulses. (b) One SM capacitor voltage from each of the 2 transition arms during negative unipolar pulse generation. (c) Positive polarity pulses. (d) One SM capacitor voltage from each of the 2 transition arms during positive unipolar pulse generation.

With $t_x = 20\mu s$, $t_m = 40\mu s$ and $t_{pl} = 120\mu s$ negative plus positive unipolar four-level voltage pulses are shown in Fig.3.32a and Fig.3.32c with a repetition frequency of 3.6kHz, respectively. A SM capacitor voltage from the corresponding arm as well as the deactivated arm during unipolar pulses generation, are shown in Fig.3.32b and Fig.3.32d for the negative and the positive unipolar pulses, respectively. The deactivated arm SM capacitors voltage remain zero, as they are not contributing to the pulse generation.

Generating rectangular pulses with different characteristics is explored in Fig.3.33. Symmetrical rectangular bipolar pulses with $t_m = 20\mu s$ are shown in Fig.3.33a, with SM-capacitor voltages from Arm1 and Arm2 in Fig.3.33b. Positive unipolar pulses with $t_m = 40\mu s$ are shown in Fig.3.33c, while combined symmetric NLV pulses are illustrates in Fig.3.33d. Asymmetric rectangular pulse generation is shown in

Fig.3.33e and Fig.3.33f. Fig.3.33e shows a 40µs rectangular positive pulse followed by a 20µs negative pulse. An asymmetric combined NLV duration rectangular pulse is depicted in Fig.3.33f with positive and negative pulse times of 20µs and 40µs, respectively.

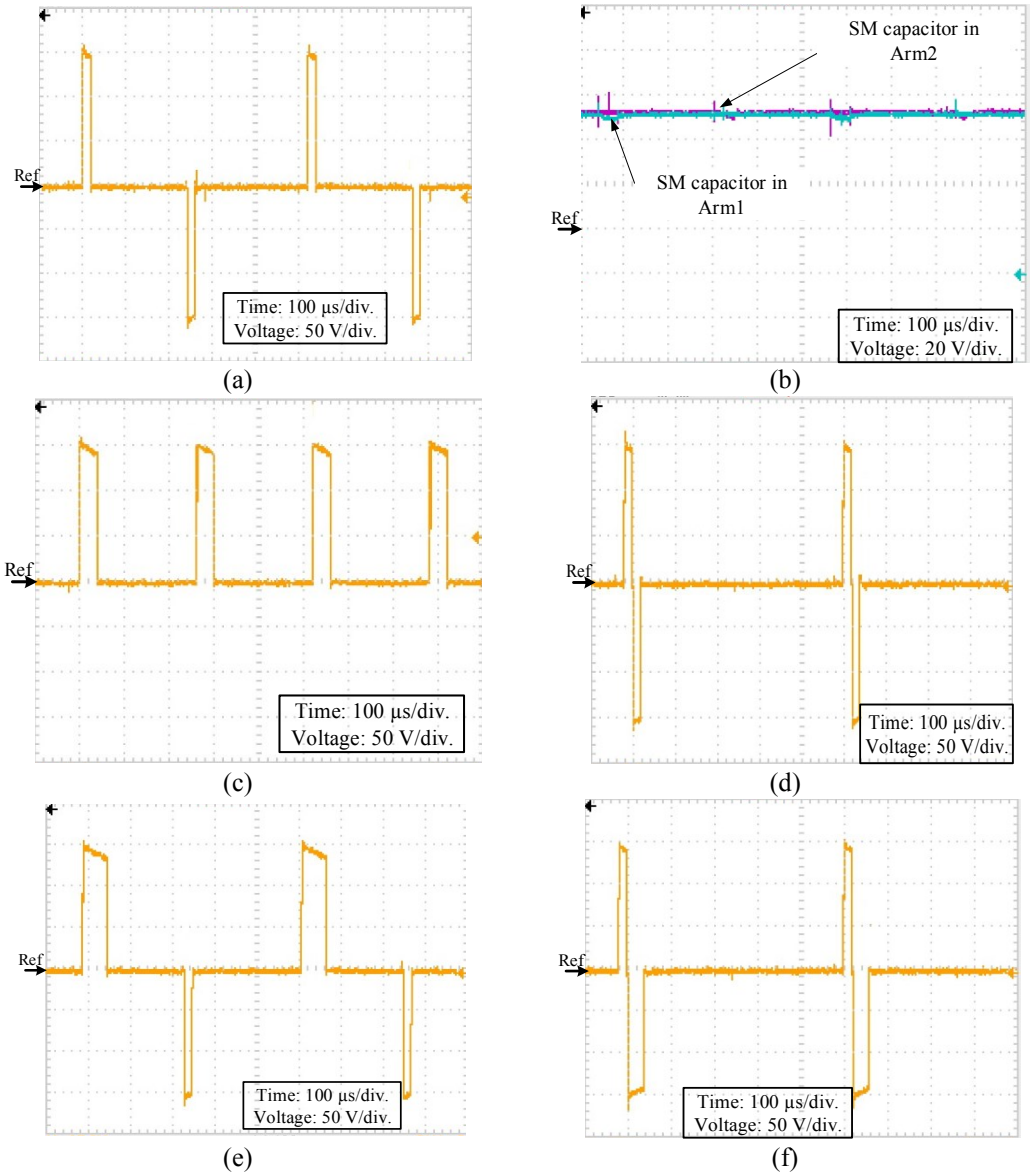


Fig.3.33. Experimental results for UPG rectangular pulses.
(a) Symmetrical bipolar with $t_m = 20\mu s$. (b) SM-capacitor voltage in the 2 transition arms. (c) Positive unipolar with $t_m = 40\mu s$. (d) Combined NLV durations with $t_m = 20\mu s$. (e) Asymmetrical bipolar with positive $t_m = 40\mu s$ and negative $t_m = 20\mu s$. (f) Combined NLV durations with positive $t_m = 20\mu s$ and negative $t_m = 40\mu s$.

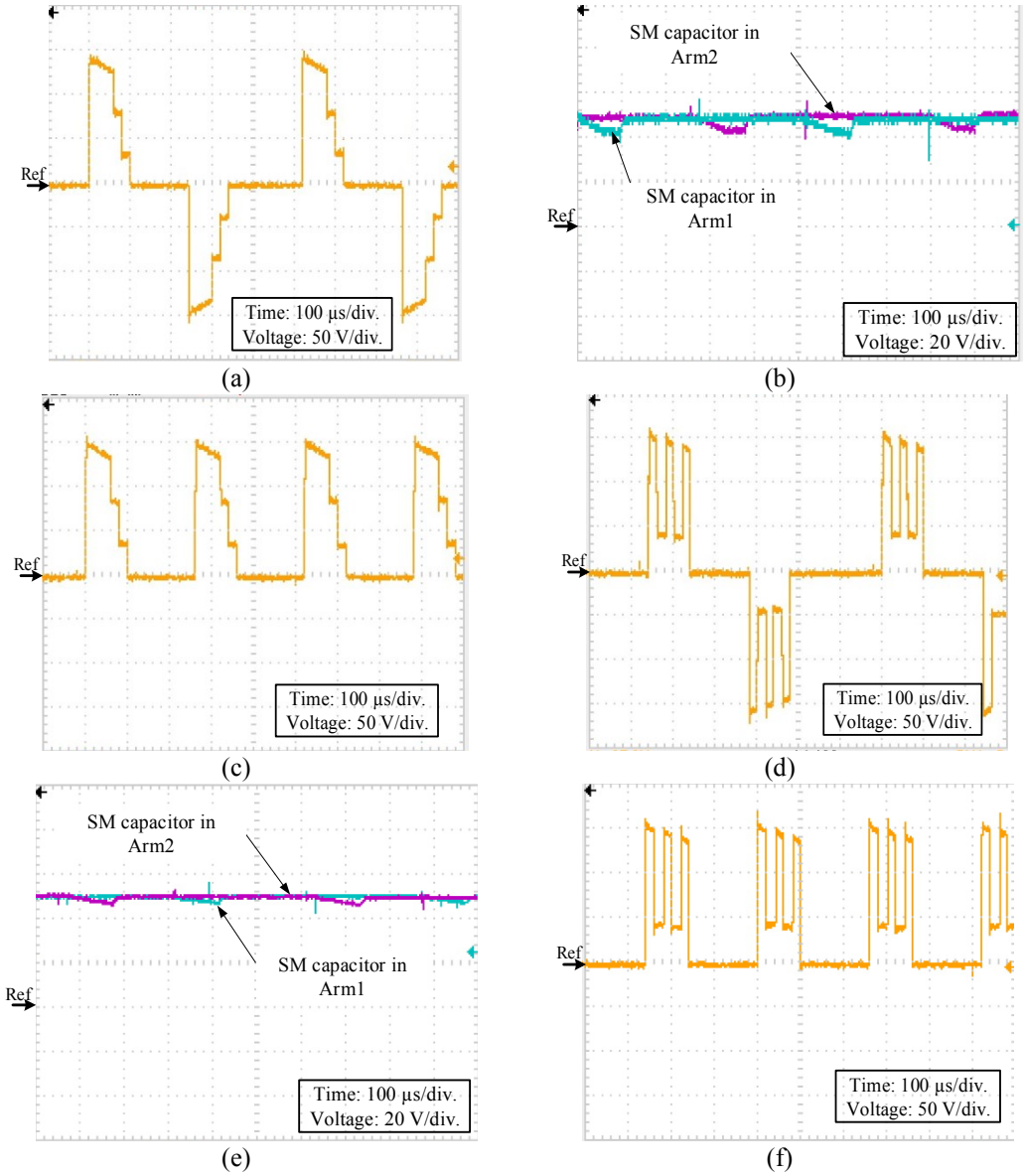


Fig.3.34. Experimental results for UPG conventional electroporation pulses generation. (a) Bipolar ramp pulses with $t_x = 20$ µs and $t_m = 40$ µs. (b) SM-capacitor voltage in the 2 transition arms during bipolar ramp pulse generation. (c) Positive unipolar ramp. (d) Bipolar multipulse with $m = 2$ and $t_x = 20$ µs. (e) SM-capacitor voltage in the 2 transition arms during bipolar multipulse generation. (f) Positive unipolar multipulse.

Bipolar ramp pulses with $t_x = 20\mu s$ and $t_m = 40\mu s$ are shown in Fig.3.34a and a SM-capacitor voltage in the 2 transition arms are shown in Fig.3.34b. The unipolar version is shown in Fig.3.34c. The multipulse waveforms with $m = 2$ and $t_x = 20\mu s$ are shown in Fig.3.34d, Fig.3.34e and Fig.3.34f are bipolar pulses, with SM-capacitors voltage in the 2 transition arms, and the unipolar version of pulses, respectively.

3.3.6 UPG Topology Variations and Limitations

There are UPG topology variations, dependent on the electroporation application requirements.

Arm inductance: The arm inductor L_a is small and may be accounted for by the inherent internal wiring and connection of the SMs. Clamping the inductors with freewheel diodes is possible but the low voltage of the forward biased diode may result in an excessively long L/R reset time constant, which will limit the upper operating frequency. The energy of remaining unclamped stray inductance, rings with the SM capacitors. This ringing represents a small loss.

Elimination of bi-state arm diodes: MMC SM-capacitor recharging involves an *LCR* oscillation, where if underdamped, the current alternately reverses. The damping losses are independent of the circuit quality factor, thus critical damping incurs the lowest stresses, with an acceptable settling time. As such, without current reversal, the bi-state arm diodes across the IGBTs are redundant. To maximize power transfer, any (added and/or exiting) resistance should be in the bi-state arm. Both MMC arm series inductors can be moved to their associated series bi-state arm.

Bi-state arm switches: The switching properties of the bi-state arm devices can be much slower than those necessary for the transition arms (HB-MMC arms). Because their inter DC rail state transitions are at zero current, they can be higher voltage (consequently slower) rated devices, used near their voltage limit. Thus the number of bi-state arm series connected devices can be much less than N, the number MMC SMs in the transition arms. The trade-off of higher voltage devices is higher off-state leakage current, so the parallel connected static voltage sharing resistance is decreased.

Single ended topology: For only unipolar pulses, one leg consisting of one MMC SM arm and one bi-state arm (in either series order across the DC link), can be employed as a single ended chopper, where the load can be across either arm, such that the load can be referenced to either voltage rail. The load across the transition arm is preferred, since this allows the bi-state arm diodes to be removed, provided resonant recharging of the MMC SM capacitors is over-damped. The MMC SM main diodes provide a freewheel path for load circuit trapped energy.

Finally, the ability of the converter to generate high repetition rate pulses only depends on the speed of selected controller in executing the control software instructions, such that the total software execution time is less than the required pulse repetition time. For high repetition rates and/or short pulse durations, the utilisation of fast (short turn on delays) semi-conductor switches is mandatory.

3.4 Summary

This chapter has presented a new three PG topologies based on MMC SMs, namely: the clamping PG (CPG), the generic pulse-waveform PG (GPG), and the universal pulse-waveform PG (UPG). Each of the PGs are in the form of an H-bridge, therefore full utilisation of the input HV DC is possible.

The clamping topology (CPG) operates without voltage sensors and only targets rectangular pulse-waveform generation with flexible characteristics.

By adding voltage sensors to the CPG, the GPG topology is created. This hardware modification allows the controller software to generate multilevel waveforms, which can be manipulated to mimic conventional electroporation pulse waveforms.

The CPG and the GPG form their H-bridge by using four identical MMC arms. But the UPG topology has an H-bridge of two MMC arms with their associated voltage sensors along with two arms of series connected IGBTs. The UPG can generate multilevel pulse waveforms similar to the GPG. Thus, the UPG can generate conventional electroporation pulse waveforms with a reduced number of MMC SMs and voltage sensors.

The three introduced topologies require an HV DC input to operate. The topologies can be supplied from an LV DC input followed by a DC-DC voltage boosting stage or a 12-pulse AC-DC thyristor half-controlled converter which offers soft start up and shut down.

Chapter 4

New Hybrid PGs Fed from an LV DC Source

In this chapter, a new family of hybrid PGs fed from LV DC is introduced. Available hybrid PG topologies generate rectangular pulse waveforms with limited flexibility. The proposed new hybrid topologies improve the performance of the existing sequentially charging topologies. A methodology to generate different pulse waveforms from hybrid topologies is proposed.

4.1 Sequentially Charged MMC HB-SMs PG

One solution to avoid the need of an HV DC supply at the input is provided by sequentially charging the capacitors in the MMC SMs from an LV DC input. After charging the SM capacitors, the HV pulse is generated by inserting (in series) the SMs simultaneously, hence, the HV pulse voltage-gain is related to the number of charged SMs and the voltage of the input LV DC.

4.1.1 Sequentially Charged PG Converter Topology

The proposed sequentially charged PG (SPG) topology, shown in Fig.4.1, is comprised of a combination of two series-connected HB-SM arms (Arm1 and Arm2) and two series-connected IGBT-diode switches (S1 and S2). The arrangement of SMs and series IGBT-diode switches (S1 and S2) is such that the individual capacitors of the upper N series-connected SMs, Arm1, are charged to $+V_s$ through S1 from input supply V_s. The individual capacitors of the lower N series-connected SMs, Arm2, are charged through S2 from the same input supply V_s but in reverse polarity. The charging of each individual capacitor, either in Arm1 or Arm2, from the input supply occurs sequentially via an rL circuit, as shown in the charging equivalent circuit in Fig.4.2. Specifically $N-1$ SMs are bypassed with T_m on, whence the inserted SM with T_x off, charges to V_s. This process of inserting each uncharged SM, with $N-1$ bypassed, eventually charges all N SM capacitors to V_s.

Different bipolar rectangular pulse characterizations can be generated, namely:

- with/without combined periods of positive and negative NLV;
- with different positive and negative voltage-peaks; and
- with different positive and negative durations

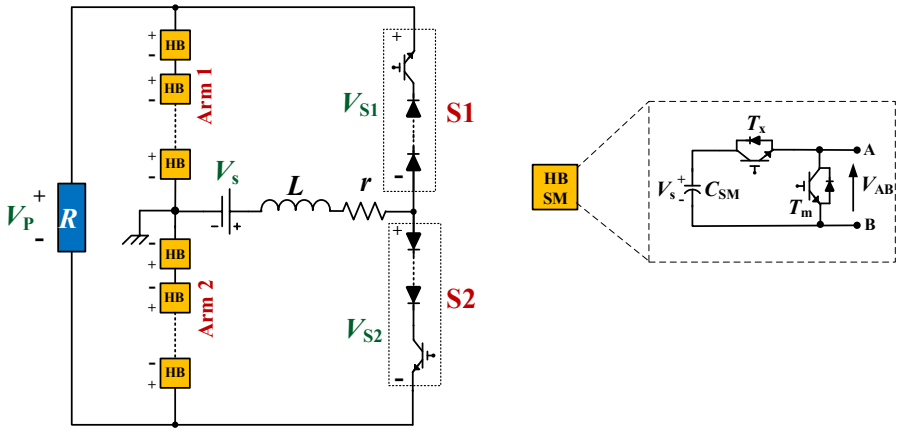


Fig.4.1. Proposed SPG converter topology.

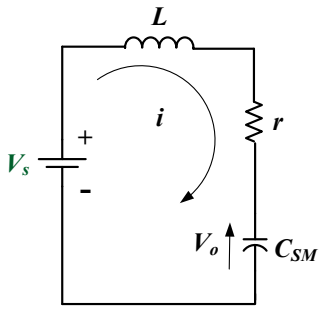


Fig.4.2. SM-capacitor charging process equivalent circuit.

4.1.2 SPG Topology Operating Principle

Generating the bipolar rectangular pulse of peak voltage $V_P = \pm NV_s$, shown in Fig.4.3, by the proposed SPG is achieved via the following stages (assuming all SM capacitors are pre-charged to V_s):

- ***Stage* I**: Arm1 SMs are inserted, and Arm2 SMs are bypassed, while the switches S1 and S2 are off as shown in Fig.4.4a. Thus the load voltage is $+NV_s$ for the required positive pulse time t_p, and the supply V_s is disconnected.
- ***Stage* II**: after contributing to the positive pulse generation; in Arm1, each SM capacitor voltage decreases to V_o (as illustrated in Fig.4.3). Thus, in stage

II each capacitor is charged to V_s sequentially. Arm1 and Arm2 are idled, while S1 and S2 are maintained OFF from stage I, then the first SM in Arm1 is inserted. S1 is turned on (hence, near ZVS is assured) and the charging process, for the charging time (t_c), starts. After t_c, the charged SM is bypassed and the next SM is inserted for charging, etc. After the charging of the last SM capacitor, S1 is turned OFF (hence, ZCS is assured), then the SM is bypassed. During the total charging time of the N sequentially-charged SMs, $t_{pz} = Nt_c$, the load voltage is nulled as shown in Fig.4.4b.

- ***Stage* III**: for a negative pulse period t_n, a negative pulse of peak$-NV_s$ is formed across the load by inserting Arm2 capacitors, while bypassing Arm1 SMs, and maintaining S1 and S2 off as shown in Fig.4.4c.
- ***Stage* IV**: similar to stage III, the negative NLV time $t_{nz} = Nt_c$ is employed to sequentially charge the N individual capacitors of Arm2 SMs through S2, see Fig.4.4d, while imposing a zero voltage across the load. The same approach of turning ON/OFF S1 is repeated for S2 such that ZVS and ZCS are assured at S2 turn ON and OFF, respectively.

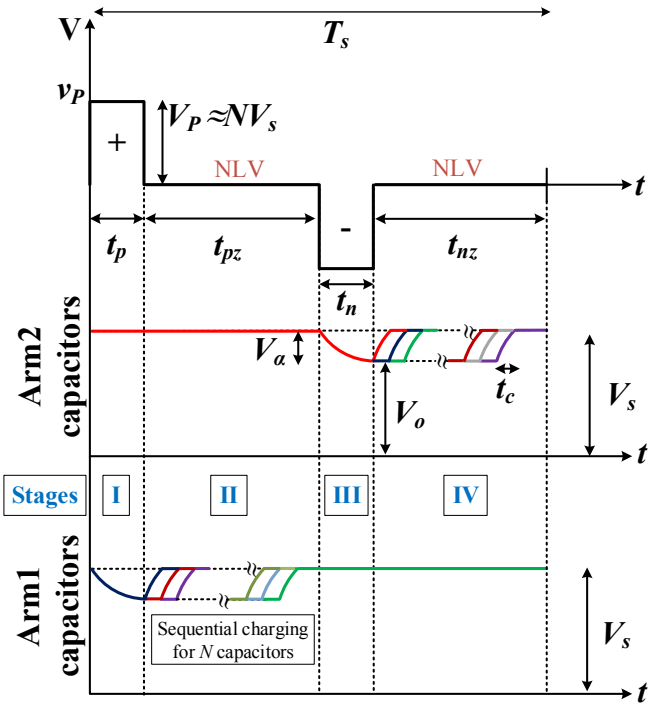


Fig.4.3. SPG generated bipolar rectangular waveform and the corresponding charging/discharging sequence of Arm1 and Arm2 capacitors.

Since the positive and the negative arms of the series-connected HB-SMs are charged independently, generation of symmetrical, as in Fig.4.3, and asymmetrical rectangular bipolar HV pulses is possible as shown in Fig.4.5. As a result, the SPG allows flexible bipolar rectangular HV pulse generation in symmetrical and asymmetrical forms. In Fig.4.5a symmetrical combined NLV duration pulses is shown when the pulse cycle starts with a positive polarity. The asymmetry is not only in the negative (t_n) - positive (t_p) pulse durations as in Fig.4.5b, but also in the negative (V_n) - positive (V_p) pulse magnitudes, as in Fig.4.5c. Fig.4.5d shows combining both asymmetries in a combined NLV pulse when the pulse cycle starts with a negative polarity. As a result of this pulse generation flexibility, if one or more of the SMs fail (then bypassed) the pulse voltage will be asymmetrical (in magnitude). In order to have the same energy content, the pulse width is increased as depicted in Fig.4.5b and Fig.4.5d.

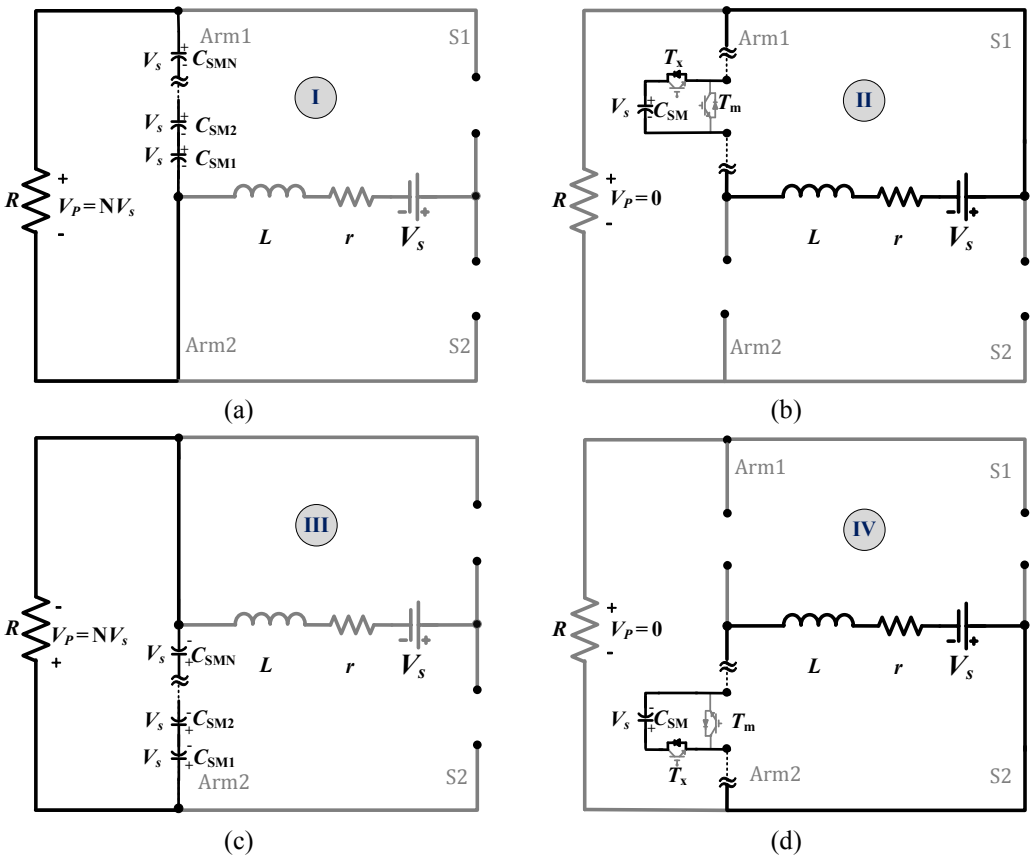


Fig.4.4. SPG circuit configurations during bipolar pulse generation stages.
(a) Stage I. (b) Stage II. (c) Stage III. (d) Stage IV.

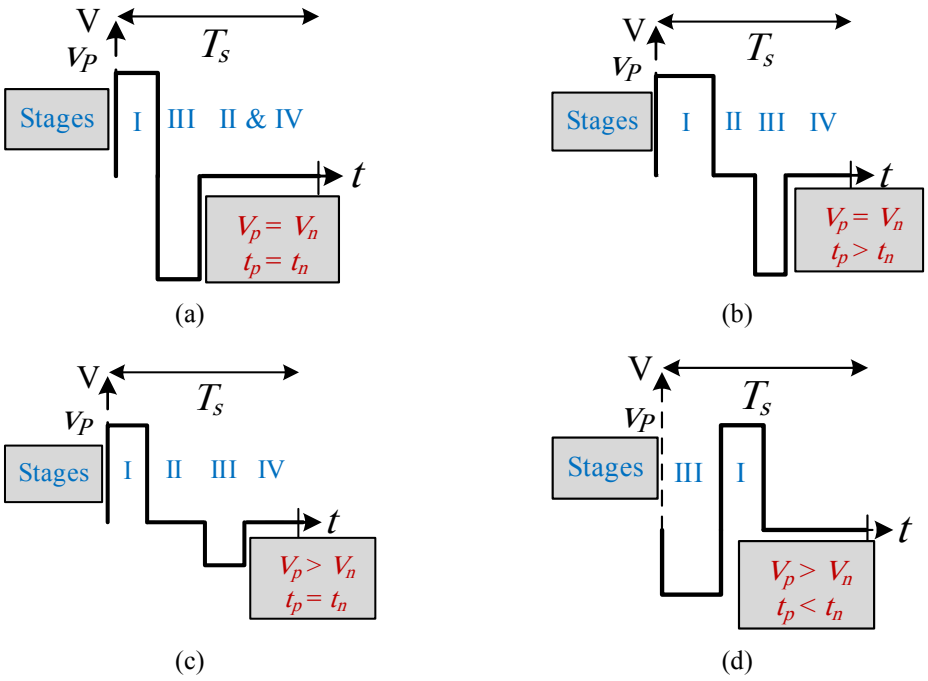


Fig.4.5. Symmetrical and asymmetrical bipolar rectangular pulses.
(a) Symmetrical combined NLV durations when the pulse cycle starts with positive polarity. (b) Duration asymmetry in bipolar rectangular pulses. (c) Magnitude asymmetry in bipolar rectangular pulses. (d) Asymmetrical combined NLV durations when the pulse cycle starts with negative polarity.

The IGBTs in the HB-SMs are rated at the low voltage input DC supply V_s. Although, the IGBTs in S1 and S2 are rated at V_s, during positive and negative pulse generation, a reverse voltage of $(N-1)V_s$ is experienced across S1 and S2, respectively. Therefore a series diode (or series connection of diodes) to block this voltage is necessary. Such series connected blocking diodes experience a static reapplied dv/dt (not conducting when the reverse voltage is applied), hence shunt resistors (to compensate for leakage current variation) and capacitors (to compensate for junction capacitance variation) are sufficient to ensure voltage sharing. Alternatively, any reverse blocking device, such as the IGCT, (series connected) can be utilised for S1 and S2 [74]-[80].

4.1.3 SPG Topology Variations

Fig.4.6a shows another SPG topology variation for generating bipolar pulses with single active switch Q. If unipolar pulses, with a specific polarity, are preferred using

the topology in Fig.4.1, the arm responsible for generating the other pulse polarity is disabled. However, it is more efficient and compact to replace the disabled HB-MMC arm with a single IGBT switch (Q) rated at V_s. Fig.4.6b and Fig.4.6c show the proposed unipolar SPG topologies for positive and negative HV pulse generation, respectively. The switch Q blocks load current during the successive SM capacitor charging sequence. It must be ensured that Q is switched on before any SMs are inserted to generate an output pulse, so as not to exceed its voltage rating.

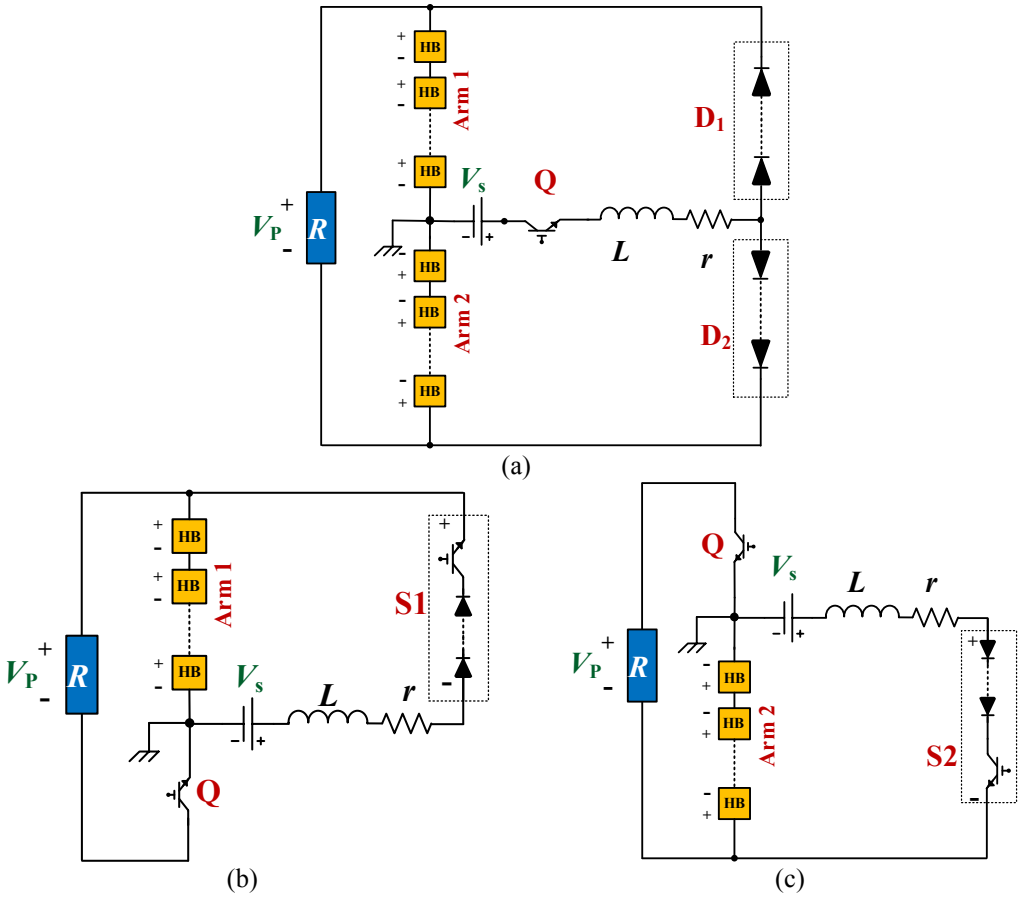


Fig.4.6. Other SPG topologies.
(a) Single switch charging switch SPG. (b) Positive unipolar rectangular pulse generation.
(c) Negative unipolar rectangular pulse generation.

4.1.4 Charging Process Analysis and SPG SM Capacitance Sizing

Consider the charging equivalent circuit in Fig.4.2, where the SM-capacitor is initially charged to V_o such that $V_o < V_s$ and the resultant capacitor voltage drop due to the previous voltage pulse generation is

$$V_\alpha = V_s - V_o \tag{4.1}$$

Applying KVL yields:

$$V_s = ri + L\frac{di}{dt} + \frac{1}{C_{SM}}\int i\,dt \tag{4.2}$$

Differentiate with respect to t and re-arranging terms

$$\frac{d^2i}{dt^2} + \frac{r}{L}\frac{di}{di} + \frac{i}{LC_{SM}} = 0 \tag{4.3}$$

To solve this second-order differential equation; two initial conditions are required. At re-charging, the initial current is zero:

$$i(0) = 0 \tag{4.4}$$

Also, the capacitor voltage is reduced to V_o, after discharging into the load during pulse generation, hence, at $t = 0$ applying KVL to find $\frac{di(0)}{dt}$:

$$ri(0) + L\frac{di(0)}{dt} + V_0 = V_s \tag{4.5}$$

Thus

$$\frac{di(0)}{dt} = \frac{V_s - V_o}{L} = \frac{V_\alpha}{L} \tag{4.6}$$

Generally, the response of $i(t)$ depends on the roots of (4.3). The relation between r, L and C_{SM} that determines the response type and $i(t)$ mathematical expressions are summarised in Table 4.1. In Table 4.1, A_1 and A_2 are constants to be calculated via the circuit initial conditions, $x_1$and x_2 are the roots of the differential equation, which are expressed as in (4.7):

$$x_{1,2} = -\alpha \pm \sqrt{\alpha^2 - \omega_o^2} \tag{4.7}$$

Table 4.1: Relation between r, L and C_{SM} and Response Type

Response type	**Overdamped**	**Critically damped**	**Underdamped**
Condition	$C_{SM} > \frac{4L}{r^2}$	$C_{SM} = \frac{4L}{r^2}$	$C_{SM} < \frac{4L}{r^2}$
Instantaneous current equation	$i(t) = A_1e^{x_1t} + A_2e^{x_2t}$	$i(t) = (A_1 + A_2t)e^{-\alpha t}$	$i(t) = e^{-\alpha t}(A_1cos\omega_d t + A_2sin\omega_d t)$
where $\alpha = \frac{r}{2L}$, $\omega_o = \frac{1}{\sqrt{LC_{SM}}}$ and $\omega_d = \sqrt{\omega_o^2 - \alpha^2}$			

A. Individual SM Capacitor Charging Efficiency

Since a critically damped response represents the margin between the other two response types, it is considered in the following analysis without loss of generality. The current $i(t)$ can be expressed as follows, while accounting for the initial conditions

$$i(t) = \frac{V_\alpha}{L} t e^{-\alpha t} \tag{4.8}$$

The energy dissipated in r (circuit loss component) can be expressed as E_r where

$$E_r = r\int_0^\infty i(t)^2 dt = \frac{rV_\alpha^2}{L^2}\int_0^\infty t^2 e^{-2\alpha t}\, dt \tag{4.9}$$

Integration yields

$$E_r = \frac{rV_\alpha^2}{L^2}\left[\frac{-e^{-2\alpha t}(2\alpha^2 t^2 + 2\alpha t + 1)}{4\alpha^3}\right]_0^\infty \tag{4.10}$$

$$E_r = \frac{rV_\alpha^2}{L^2}\frac{1}{4\alpha^3} \tag{4.11}$$

Since $\alpha = \frac{r}{2L}$, (4.11) yields

$$E_r = \frac{rV_\alpha^2}{L^2}\left(\frac{8L^3}{4r^3}\right) = \frac{2L}{r^2}V_\alpha^2 \tag{4.12}$$

However, for a critically damped response type, $C_{SM} = \frac{4L}{r^2}$; substitution into (4.12) gives

$$E_r = ½C_{SM}V_\alpha^2 \tag{4.13}$$

The energy supplied E_s by the source V_s is

$$E_s = V_s\int_0^\infty i(t)dt = \frac{V_sV_\alpha}{L}\int_0^\infty te^{-\alpha t}\, dt \tag{4.14}$$

Integrating yields

$$E_s = \frac{V_sV_\alpha}{L}\left[\frac{-e^{-\alpha t}(\alpha t + 1)}{\alpha^2}\right]_0^\infty = \frac{V_sV_\alpha}{L}\frac{1}{\alpha^2} \tag{4.15}$$

Similarly, since $\alpha = \frac{r}{2L}$:

$$E_s = \frac{V_sV_\alpha}{L}\left(\frac{4L^2}{r^2}\right) = V_sV_\alpha\frac{4L}{r^2} \tag{4.16}$$

Again, for a critically damped response, $C_{SM} = \frac{4L}{r^2}$; substitution into (4.16) gives

$$E_s = C_{SM}V_sV_\alpha \tag{4.17}$$

The per unit (pu) charging inefficiency (η_{loss}) is expressed as

$$\eta_{loss} = \frac{E_r}{E_s} = \frac{½C_{SM}V_\alpha^2}{C_{SM}V_sV_\alpha} = \frac{½V_\alpha}{V_s} \tag{4.18}$$

Thus, the pu voltage drop determines the inefficient energy ($\%\eta_{loss}$) thus the charging energy efficiency ($\%\eta_{ch}$), is:

$$\%\eta_{loss} = 100 \times ½V_\alpha^{pu} \tag{4.19}$$

$$\%\eta_{ch} = 100 - \%\eta_{loss} \tag{4.20}$$

Regardless the response type (rC or under or over damped rCL), the inefficiency is always only dependant on the capacitor voltage drop (see Appendix B). Inductance does not influence the efficiency, but affects the charging current peak and capacitor charging time.

B. Individual SM Capacitor Charging Time

Generally, for given initial conditions, the overdamped case has the longest charging time while the underdamped case has the fastest charging time. If a fast response, without severe oscillations or ringing, is desired, the critically damped case is used. In this work, the response of the circuit is chosen to be underdamped with near unity damping factor. This provides a fast charging time with acceptable overshoot and negligible oscillation. The underdamped current is expressed as

$$i(t) = \frac{V_\alpha}{\omega_d L} e^{-\alpha t} sin\omega_d t \tag{4.21}$$

After charging an individual SM capacitor, the charging current reduces to zero, hence, the actual charging time t_c^* can be calculated by setting $i(t_c^*) = 0$; solving (4.21) for t_c^* yields:

$$t_c^* = \frac{\pi}{\omega_d} \tag{4.22}$$

Accordingly, the software-controller assigned charging time, t_c, for each SM capacitor must be larger than t_c^* ($t_c > t_c^*$) such that the charging current drops to zero, therefore, assuring ZCS of the IGBT.

C. Individual SM Capacitor Sizing

The energy transferred to the resistive load per pulse polarity is expressed in Chapter 3 as:

$$E_L = \frac{N^2 V_s^2}{R} t_{pl} \tag{4.23}$$

where E_L is the per pulse-polarity load energy and t_{pl} is the pulse-polarity duration. The load energy is transferred from the stored energy in the series inserted SM capacitors during pulse generation, hence

$$½ N C_{SM} V_s^2 (1 - \beta^2) = \frac{N^2 V_s^2}{R} t_{pl} \tag{4.24}$$

where β is the per unit remaining voltage on the SM capacitor after pulse generation. Thus, SM capacitance is

$$C_{SM} = \frac{2N t_{pl}}{(1 - \beta^2) R} \tag{4.25}$$

To account for the neglected voltage drops across the semiconductor switches and parasitic resistances, a safety factor $\alpha \geq 1$ is introduced. Accordingly, the SM capacitance used in the proposed topology is selected based on

$$C_{SM} = \frac{2N t_{pl}}{(1 - \beta^2) R} \alpha \tag{4.26}$$

Table 4.2: Simulation and Experimental Specifications of the SPG

Parameter		Simulation	Experimental
LV DC input voltage	V_s	1 kV	200 V
Load pulse peak voltage	V_P	10 kV	600V
Input inductance	rL	1Ω and 2µH	2 Ω and 6µH
Number of SMs per Arm	N	10	3
Load resistance	R	1 kΩ	500 Ω
SM capacitance	C_{SM}	5 µF	5 µF
Assigned SM charging time	t_c	20 µs	60 µs
Repetition time	T_s	420 µs	400 µs
pu remaining voltage	β	> 0.95	
Safety factor	α	1.3	3.2

4.1.5 Simulation Results for the SPG

Matlab/Simulink simulations are used to assess the viability of the proposed SPG topology, with the specifications in Table 4.2. With a 10μs pulse duration and 10kV pulse peak, symmetrical bipolar voltage pulses are depicted in Fig.4.7. The SM capacitors in Arm1 and Arm2 are sequentially charged through the rL branch to the LV DC supply level $V_s = 1$kV. Fig.4.7a shows the generated pulses across the load while Fig.4.7b and Fig.4.7c illustrate the charging and discharging sequence of the positive and negative SM capacitors, respectively.

The input charging current for one cycle is shown in Fig.4.7d, where the 20 SMs of Arm1 and Arm2 are charged sequentially in the positive and negative NLV periods, respectively. Based on the parameters in Table 4.2, the individual SM capacitor charging current drops to zero after the charging time, $t_c^* = 16.2$μs, as a result, in the controller, the assigned charging time for each SM capacitor is set to $t_c = 20$μs. Thus, after charging the last SM capacitor, switches S1 and S2 can be turned OFF safely at ZCS. The voltage stresses across S1 and S2 are shown in Fig.4.7e and Fig.4.7f.

Symmetrical combined NLV durations are shown with a positive pulse generated first and a negative pulse generated first, with 10μs pulse duration and 10kV pulse peak in Fig.4.8a and Fig.4.8b, respectively.

In Fig.4.9, the generation of asymmetrical bipolar pulses is explored. Bipolar pulses with a positive peak of V_p =10kV and a negative peak of V_n =5kV with 10μs pulse duration for each polarity, are shown in Fig.4.9a. With a 10kV voltage peak, Fig.4.9b shows bipolar pulses of positive pulse duration t_p =15μs and negative pulse duration t_n =5μs. Combined NLV duration pulses of V_p =5kV, t_p =15μs, V_n =10kV, and t_n =5μs are shown in Fig.4.9c. The combined NLV duration pulses ofV_n = 4kV, t_n =15μs, V_p =5kV and t_p = 5μs are shown in Fig.4.9d.

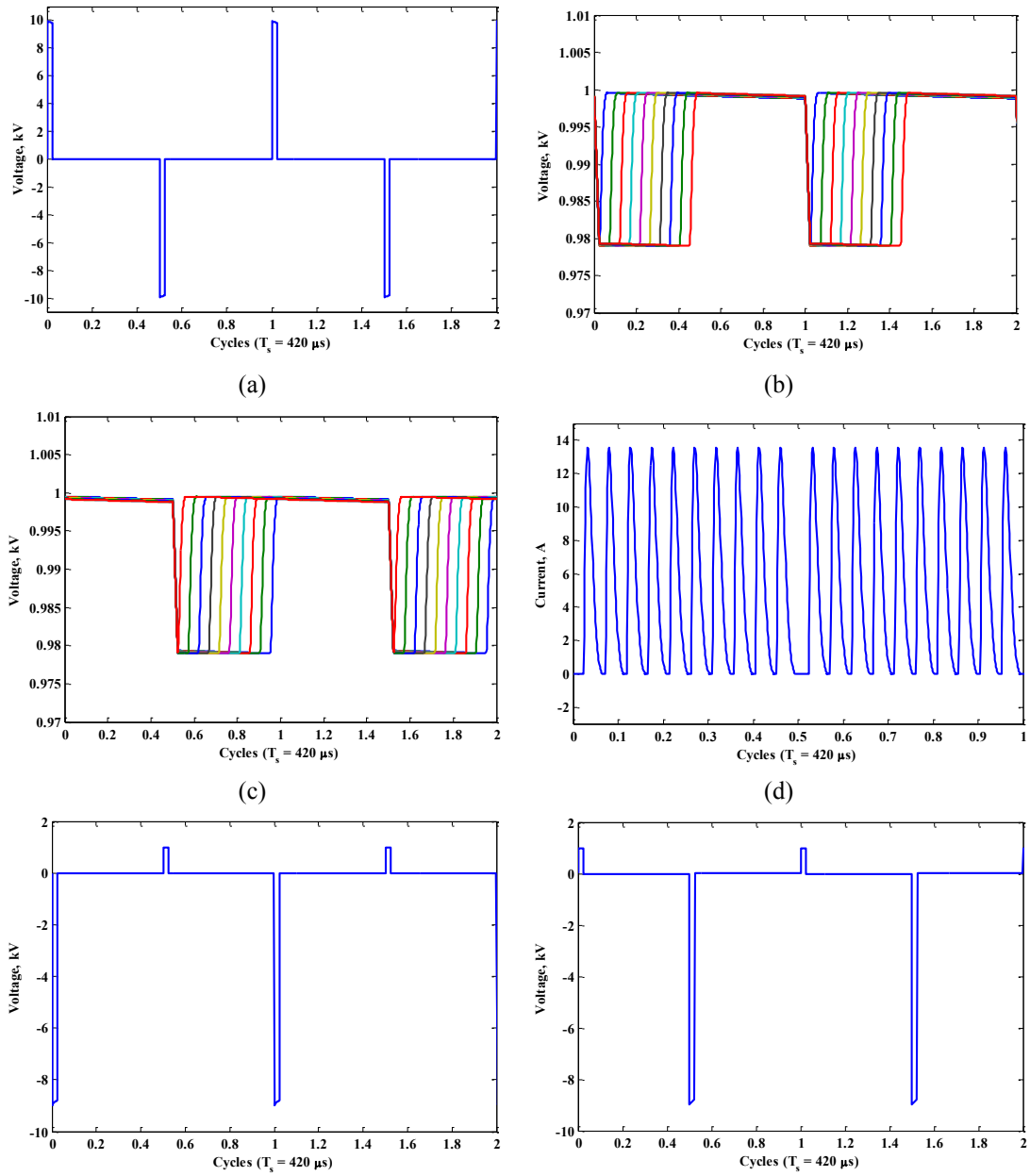
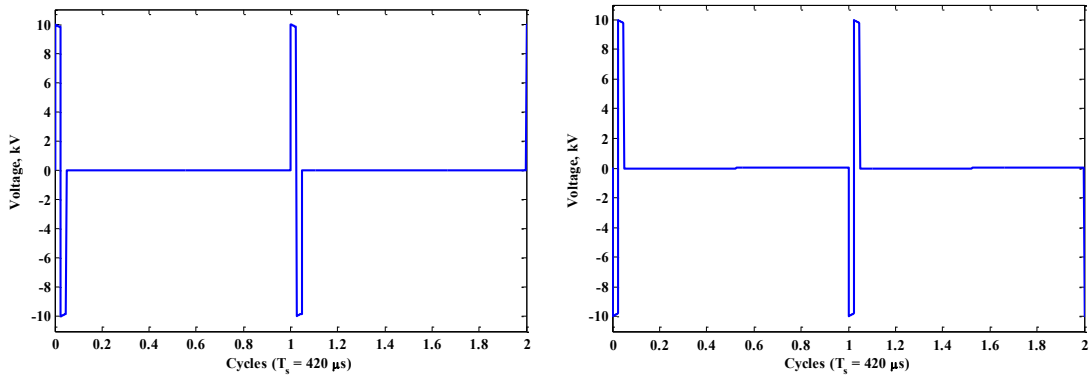


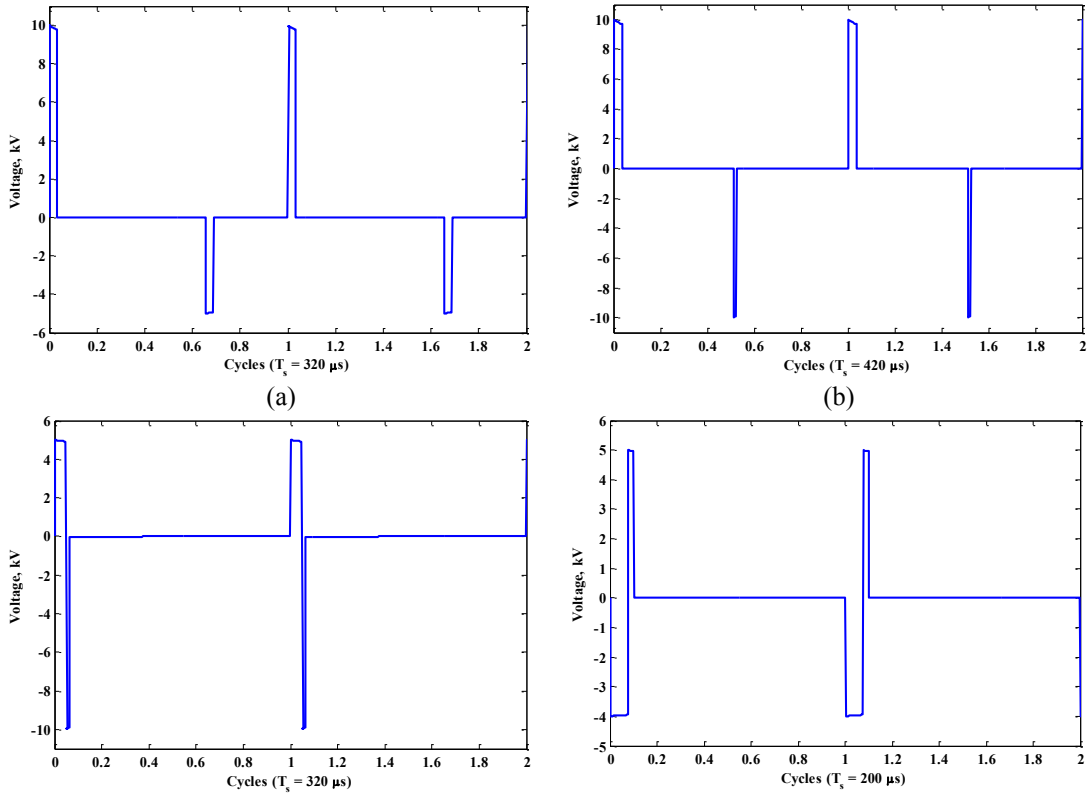
Fig.4.7. Generation of 10 kV peak, 10µs symmetrical bipolar pulses.
(a) Voltage pulses across the load. (b) Ten SM capacitor voltages of Arm1. (c) Ten SM capacitor voltages of Arm2. (d) Input charging current of the SM capacitors.(e) Voltage across S1.(f) Voltage across S2.

With the parameters in Table 4.1 and the unipolar SPG topologies in Fig.4.6, unipolar pulses of peak voltage 10kV, duration 10µs and repetition rate $T_s = 210\mu s$ are generated as shown in Fig.4.10. Fig.4.10a shows unipolar pulses of positive polarity while Fig.4.10b shows negative polarity unipolar pulses.



(a) (b)

Fig.4.8. Generation of 10 kV peak, 10µs symmetrical combined NLV durations bipolar pulses. (a) Positive pulse generated first. (b) Negative pulse generated first.



(a) (b)

(c) (d)

Fig.4.9. Generation of asymmetrical bipolar pulses.
(a) Positive and negative polarities magnitude asymmetry. (b) Positive and negative polarities duration asymmetry (c) Asymmetrical pulses with combined NLV durations when the pulse cycle starts with positive polarity. (d) Asymmetrical pulses with combined NLV durations when the pulse cycle starts with negative polarity.

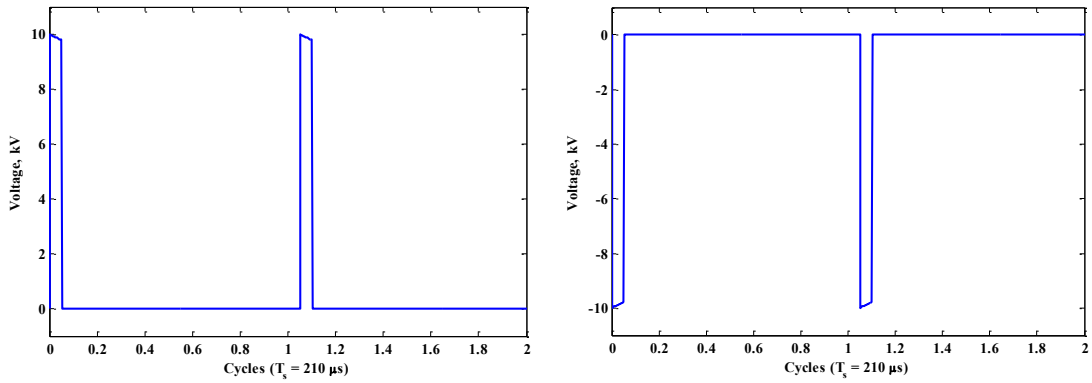


Fig.4.10. Generation of 10 kV peak, 10µs unipolar pulses.
(a) Positive pulse polarity. (b) Negative pulse polarity.

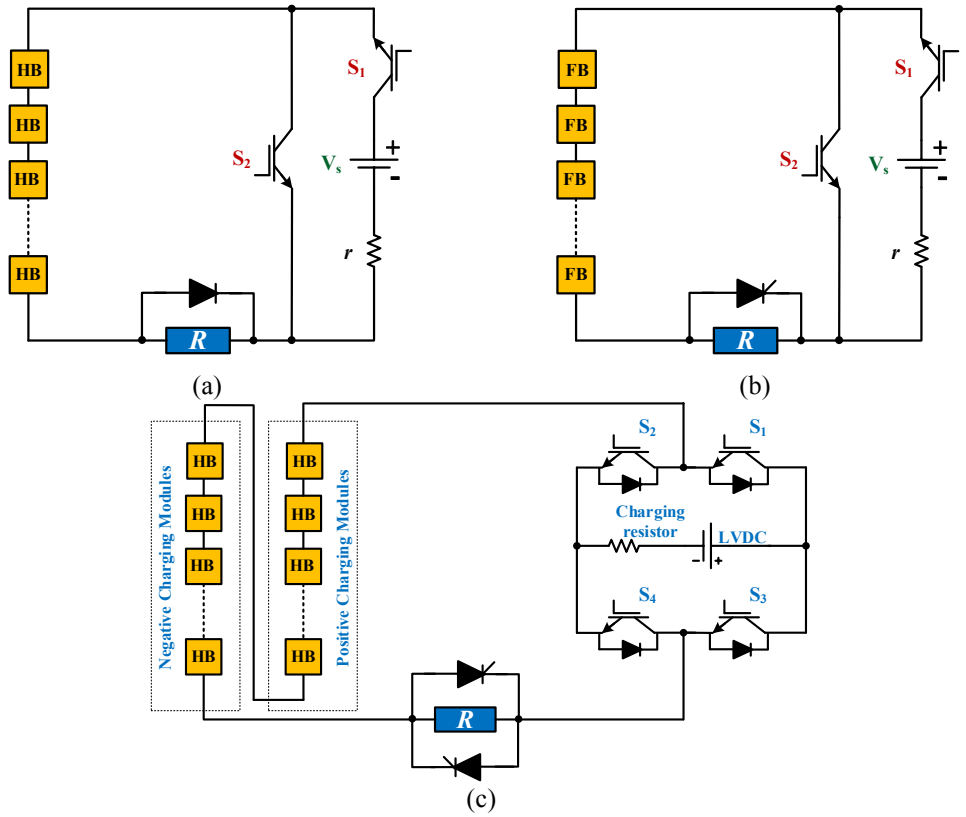


Fig.4.11. Sequential charging topologies compared with the SPG.
(a) Topology in [66]. (b) Topology in [68]. (c) Topology in [67].

Table 4.3 compares the proposed SPG topology and the MMC-based sequential charging topologies using a charging resistor in [66]-[68]. The comparison is based on generating HV pulses with a pulse peak voltage $V_P = 10\text{kV}$, repetition time $T_s = 500\mu\text{s}$ (for unipolar mode $T_s = 250\mu\text{s}$), and pulse duration $t_{pl} = 20\mu\text{s}$ across a $R =$

1kΩ resistive load. The detailed comparison methodology and parameters selection are given in Appendix B.

As shown in Table 4.3 the capacitances in the sequential charging topologies in [66]-[68] are 60% larger than for the proposed SPG topology. But the maximum current of the sequential charging topologies in [66]-[68] is 23.3% lower than in the proposed SPG topology in Fig.4.1 and Fig.4.6a. In the bipolar pulse generation mode, the proposed SPG can have the same repetition time as the unipolar pulse generator, where the charging of one of the upper and one of the lower SMs can overlap, but at the expense of doubling the current drawn from the input supply. This feature is not possible in the PG topologies in [66]-[68] due to their hardware structure.

Table 4.3: Quantitative Comparison between MMC Sequential Charging PGs

	Topology in [66] Fig.4.11a	**Topology in [68] Fig.4.11b**		**Topology in [67] Fig.4.11c**		**Proposed SPG Topology Fig.4.1&Fig.4.6a**	
Charging r/rL	$r = 3.6\ \Omega$	$r = 3.6\ \Omega$		$r = 3.6\ \Omega$		r =1.5Ω &L = 10µH	
SM Capacitance	$C_{SM} = 6.43$ µF	$C_{SM} = 6.43$ µF		$C_{SM} = 6.43$ µF		$C_{SM} = 4$ µF	
Charging time/SM (t_c)♠	$t_c = 23$ µs	$t_c = 23$ µs		$t_c = 23$ µs		$t_c = 22.5$ µs	
Peak charging current	13.8 A	13.8 A		13.8 A		18 A	
Pulse Polarity	Unipolar	Bipolar	Unipolar	Bipolar	Unipolar	Bipolar	Unipolar
Repetition time (T_s)	250 µs	500 µs	250 µs	500 µs	250 µs	500 µs	250 µs
Number of SM/Arm	10	20	10	10		20	10
Type of SMs	Half-Bridge	Half-Bridge		Full-Bridge		Half-Bridge	
Number of Arms	1	2	1	1		2	1
Number of MMC IGBTs rated at LV DC	20	40	20	40		40	20
Number of switches other than MMC IGBTs, and their ratings	2 IGBTs rated at LV DC	4 IGBTs rated at LV DC	2 IGBTs rated at LV DC	2 IGBTs rated at LV DC		1# or 2 IGBTs rated at LV DC.	1# or 2 IGBTs rated at LV DC.
	1 diode rated at HV pulse level (series connection of devices).	2 back to back thyristors rated at HV pulse level (series device connection)	1 thyristor rated at HV pulse level (series device connection)	1 thyristor rated at HV pulse level (series device connection)		2 Diodes rated at the HV pulse level ($N-1$ series device connection)	1 Diodes rated at HV pulse level ($N-1$ series device connection)

♠The charging time of the SPG must consider time for ZVS/ZCS conditions. # see Fig.4.6a for single switch version

4.1.6 SPG Proof of Concept Experimental Results

The proof of concept SPG power circuit of Fig.4.1 uses IGBT switches STGW30NC60WD in the HB-MMC arms, which have antiparallel diodes, while switches S1 and S2 are comprised of Infineon IGW60T120 IGBTs in series with IXYS DSEI30-10A ultrafast power diodes. The software algorithm was implemented in a Texas Instruments (TMS320F28335) DSP to generate the required gating signals for the SPG switches. The experimental specifications are given in Table 4.2 and the proof of concept experimental rig is shown in Fig.4.12.

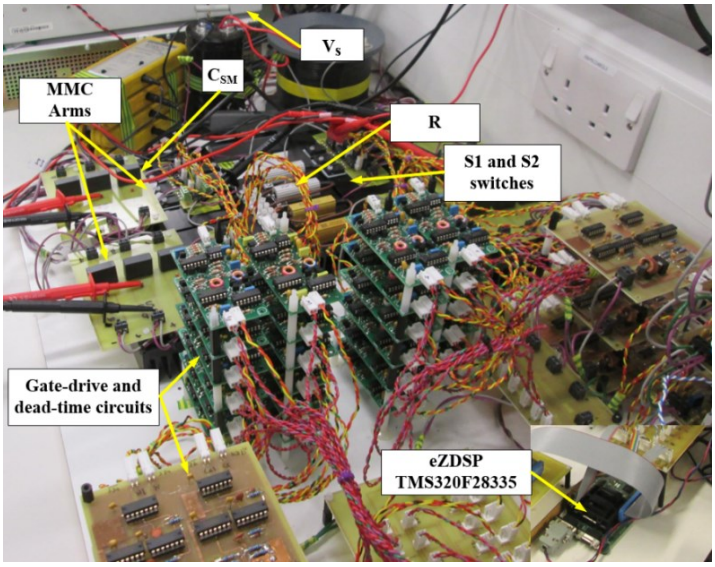


Fig.4.12. The proof of concept SPG experimental rig.

Fig.4.13 shows the generated symmetrical bipolar pulses with a peak-peak voltage of 1.2kV, 20μs pulse duration and $T_s = 400\mu s$ repetition rate. The generated voltage pulses are shown in Fig.4.13a, while Fig.4.13b and Fig.4.13c show the charging and discharging sequence of the positive and negative arm SM-capacitors, respectively. In order to generate a peak voltage of 600V per pulse-polarity, the individual SM capacitors are sequentially charged to the supply voltage $V_s = 200V$. The input charging current is shown in Fig.4.13d with an assigned SM charging time $t_c = 60\mu s$. The voltage waveforms across switches S1 and S2 (V_{S1} and V_{S2}, respectively) are depicted in Fig.4.13e, measured as illustrated in Fig.4.1. During pulse generation each switch opposing to the inserted SM-capacitors is subjected to a reverse voltage of $V_P - V_s = 400V$, while the other switch is subjected to $V_s = 200V$.

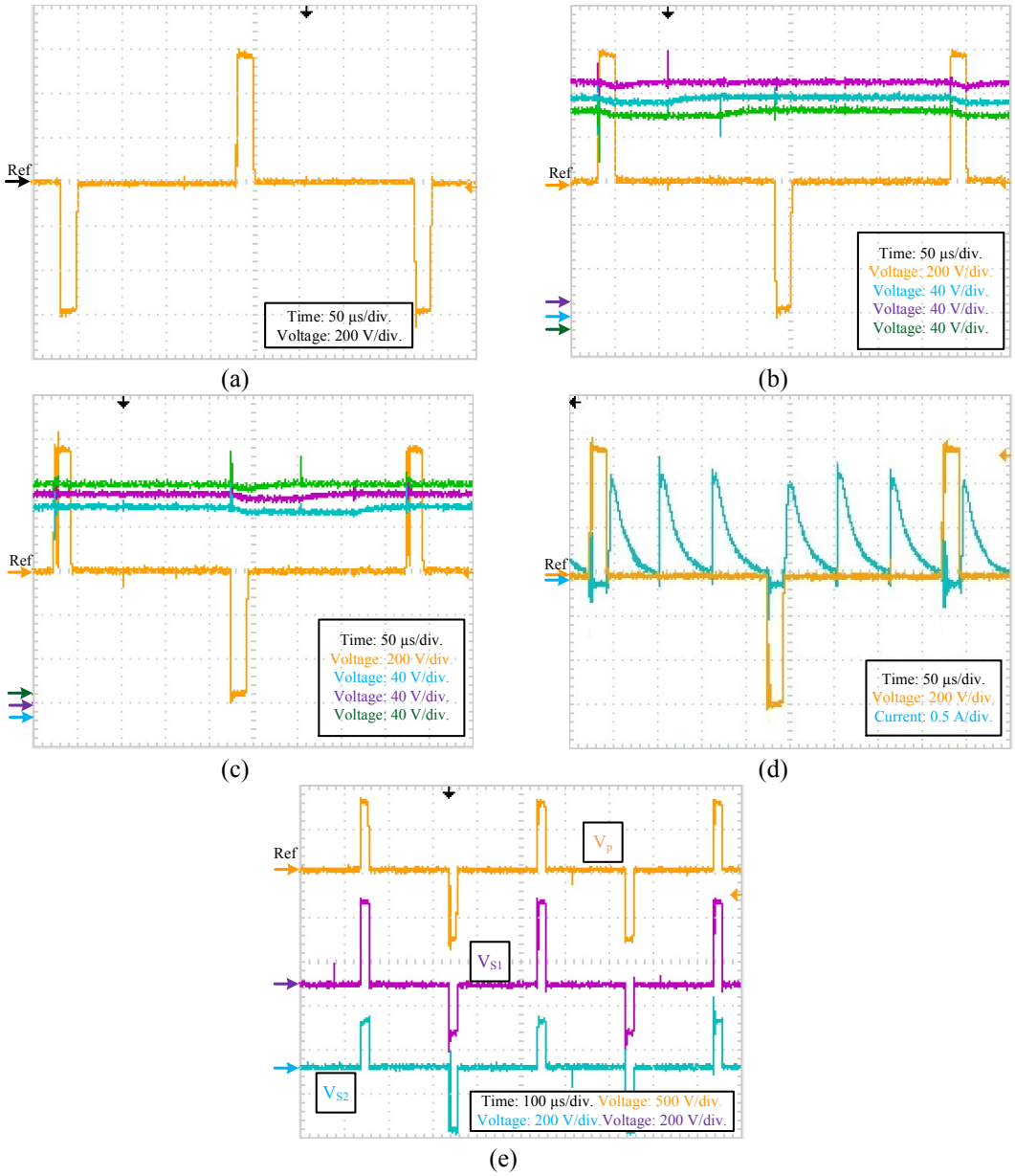


Fig.4.13. Experimental generation of symmetrical bipolar pulses of 1.2 kV peak-peak. (a) Output voltage pulses. (b) Positive arm, Arm1, SM-capacitors voltage charging and discharging sequence. (c) Negative arm, Arm2, SM-capacitors voltage charging and discharging sequence.(d) Input charging current. (e) Voltage waveforms across switches S1 and S2.

Generated asymmetrical bipolar pulses are shown in Fig.4.14. 1.2kV peak-peak, bipolar pulses of $t_p = 20\mu s$ and $t_n = 10\mu s$ are shown in Fig.4.14a. Combined NLV duration bipolar pulses of $V_p = 600V$, $t_p = 10\mu s$, $V_n = 200V$, and $t_n = 20\mu s$ are shown in Fig.4.14b. A pulse duration of 20µs combined NLV duration bipolar pulses of $V_p = 100V$ and $V_n = 400V$ are shown in Fig.4.14c.

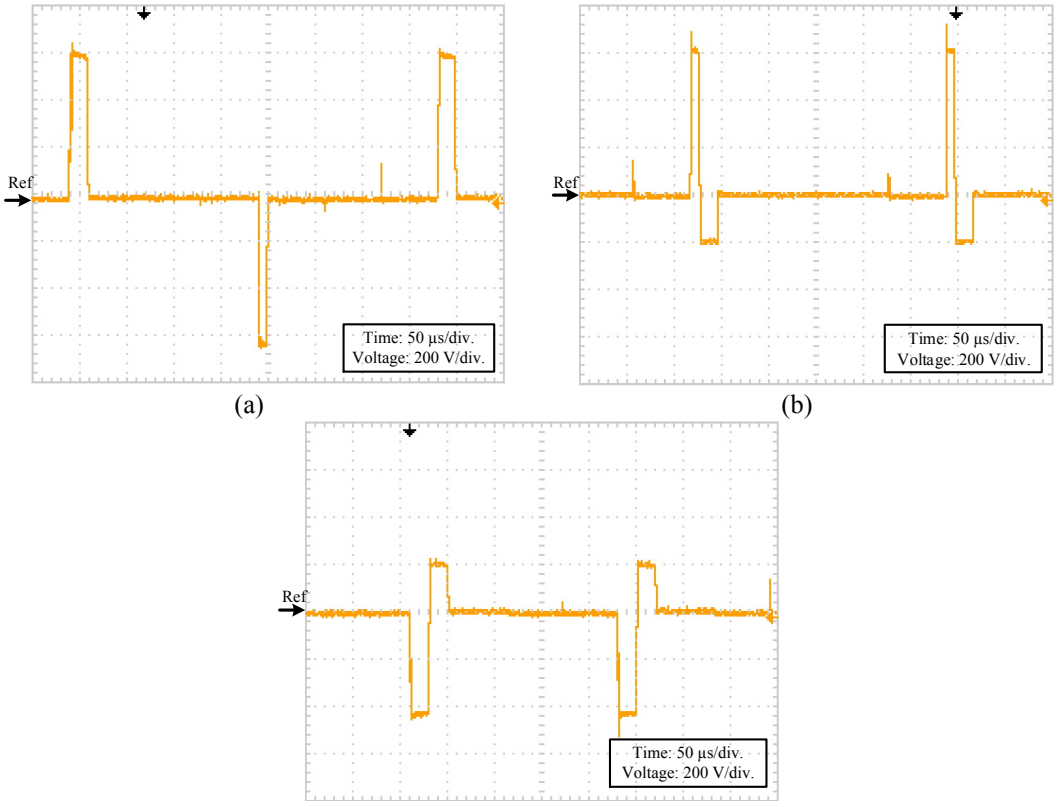


Fig.4.14. Experimental generation of asymmetrical bipolar pulses.
(a) Positive and negative polarity duration asymmetry. (b) Positive and negative polarity magnitude and durations asymmetry with combined NLV durations when pulse cycle starts with positive polarity. (c) Positive and negative polarity magnitude and durations asymmetry with combined NLV durations when the pulse cycle starts with negative polarity.

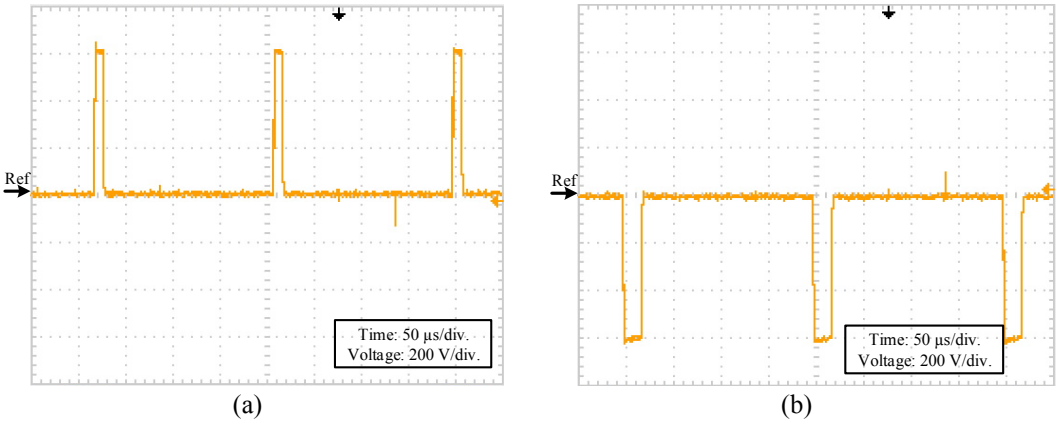


Fig.4.15. Experimental generation of 600V peak unipolar pulses.
(a) Positive pulse polarity of 10µs pulse duration. (b) Negative pulse polarity of 20µs pulse duration.

Unipolar pulses are generated by enabling the appropriate pulse polarity arm only, as shown in Fig.4.15. Positive unipolar pulses are shown in Fig.4.15a with a 600V peak, 10μs pulse duration, and repetition rate of $T_s = 190\mu s$. Fig.4.15b shows 600V negative unipolar pulses, with a pulse duration of 20μs, and a $T_s = 200\mu s$ repetition rate.

4.1.7 Replacing the HB-SMs with FB-SMs

The SPG topology in Fig.4.1 can be formed of N series-connected FB-MMC SMs, which are charged sequentially from an LV DC supply V_s through an rL branch via the reverse blocking switch S as shown in Fig.4.16. With appropriate control of individual FB-SMs, zero voltage, positive and negative voltages can be applied across the load, as illustrated in Fig.2.12b. The topology incorporates two switches, switch S and switch Q. Switch S provides a closed current path during sequential charging the SM capacitors as in the HB-SM based SPG. The switch Q provides a closed current path for the SM capacitors to discharge across the load, R, when forming the required voltage pulse. When S is ON, Q is OFF and vice-versa (and both may be off). The switch S must have a high reverse blocking capability, formed of series connected IGBTs and diodes. (The IGBTs, as do the diodes, experience a static reapplied dv/dt voltage stress, as the supporting voltage is applied with zero device current. As with the series connected diodes, shunt resistors and capacitors are sufficient to ensure voltage sharing). The IGBTs are rated at $(N+1)V_s$ and the diodes are rated at $(N-1)V_s$, hence, unlike the HB-SM based SPG the IGBTs series connection is required. Switch Q is rated at the LV DC supply V_s and is formed of an IGBT Q with anti-parallel diode D_Q to allow bidirectional current flow.

The circuit during each stage of generating bipolar rectangular pulses (depicted in Fig.4.3) is illustrated in Fig.4.17. Fig.4.17a shows the circuit during positive pulse generation (stage I) where individual SM capacitors are inserted in series (by turning on T_1 and T_2 SM switches with T_3 and T_4 switches off) and switch Q is on with its antiparallel diode reverse biased. Fig.4.17b shows the charging current path for individual SM-capacitors (stages II and IV). The load is isolated by Q and has zero-voltage during the SM charging process. Finally, in stage III, a negative voltage can be formed across the load, with SM switches T_1 and T_2 off and T_3 and T_4 switches

on. Switch Q switch is nominally off as its antiparallel diode conducts, allowing a discharging current to flow as shown in Fig.4.17c.

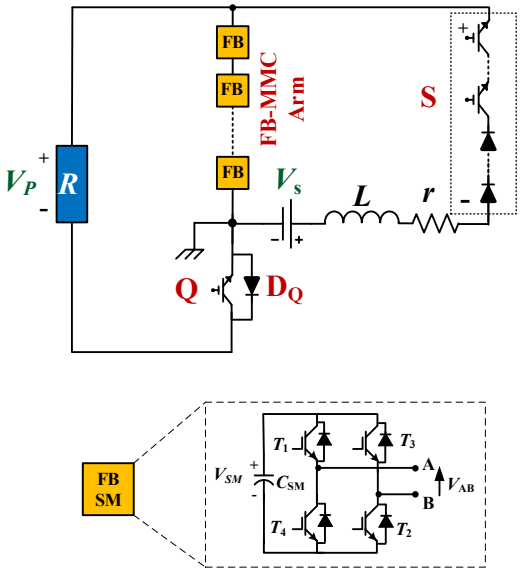


Fig.4.16. SPG Topology based on FB-SMs.

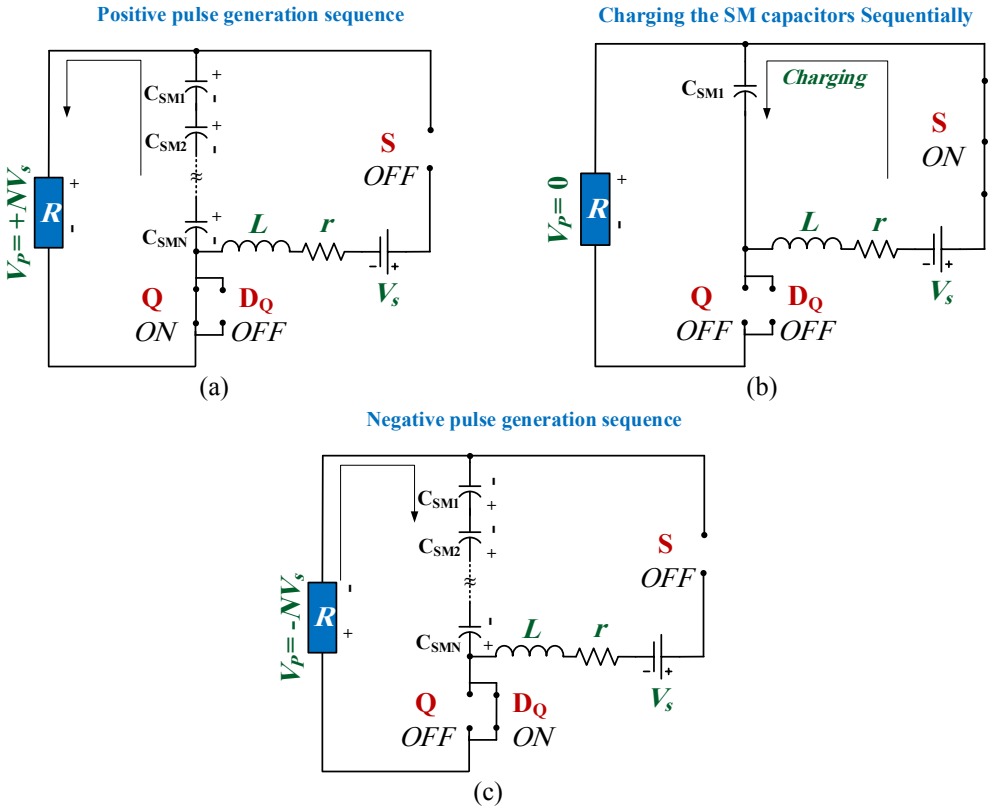


Fig.4.17. FB-SM based SPG circuit configuration during the generation of a bipolar pulse cycle. (a) Stage I. (b) Stages II and IV. (c) Stage III.

The FB-SM based SPG simulation results, when generating bipolar rectangular pulses with $V_s = 1\text{kV}$ and $N = 5$, are shown in Fig.4.18. The pulse peak voltage is 5kV as shown in Fig.4.18a, and the SM capacitor voltages fluctuate around 1kV as expected, see Fig.4.18b. The main drawback in this topology is the resulting $(N + 1)V_s$ voltage stresses across the switch S, thus necessitating series IGBT connection. Similar to the HB-SM based SPG, series diodes are added due to the reverse blocking requirement of the switch S, which has to withstand a reverse voltage of $(N - 1)V_s$. Fig.4.18c shows the voltage across the IGBTs and diodes of switch S are 6kV and -4kV, respectively.

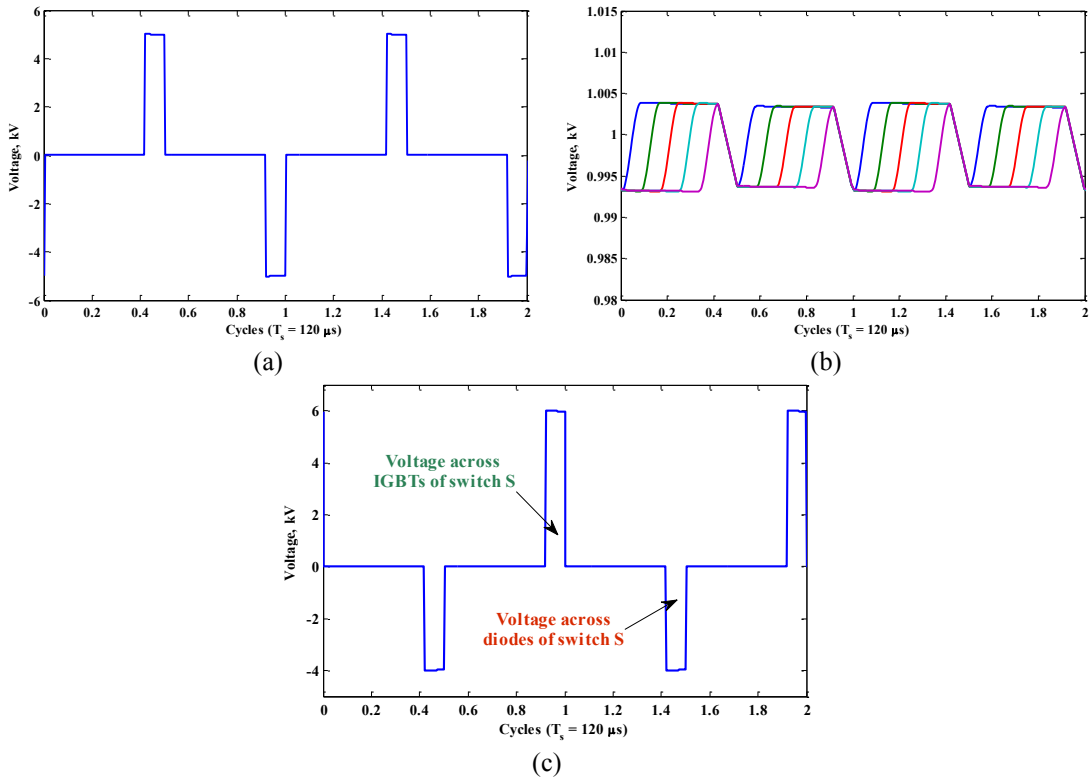


Fig.4.18. FB-SM based SPG generation of 5 kV peak, 10µs symmetrical bipolar pulses. (a) Voltage pulses across the load. (b) Five SM capacitor voltages. (c) Voltage across IGBTs and diodes of switch S.

4.2 SPG Operation in Voltage Boost Mode

In the SPG, the high gain depends on two factors namely: the number of the utilised sub modules and the input DC voltage level. For a low voltage DC input, the number of SMs should be increased. This adversely affects the pulse repetition time, as the individual SMs are charged sequentially, and increases converter footprint. In order

to achieve both a high voltage gain and a high repetition rate, with the same or even reduced SPG footprint, a control variable is added to allow the high voltage generation. The introduced control variable is achieved by allowing the individual SMs to operate in a voltage boost mode, that is, each SM acts as a boost converter when inserted sequentially in series with input DC supply V_s and the energising inductor L_i in Fig.4.19.

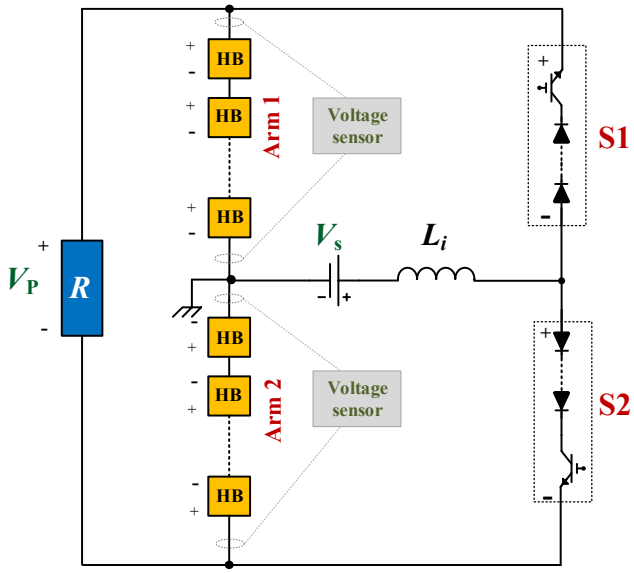


Fig.4.19. Proposed BMPG converter topology.

4.2.1 Voltage Boosting SPG Operation Principle

The same hardware structure proposed for the SPG is adopted in the voltage boost mode pulse generator (BMPG), Fig.4.19. The topology is formed of two series opposing connected MMC HB-SM arms, Arm1 and Arm2, where Arm1 is responsible of generating positive polarity pulses and Arm2 is responsible for negative polarity pulse. The reverse blocking switches S1 and S2 allow individual SM capacitor sequential charging as well as providing a closed loop path to energise the input inductor, L_i, creating a voltage-boost mode for the SM-capacitors. S1 and S2 are exposed to a reverse voltage during pulse generation, hence reverse blocking switches are required similar to the SPG topology in Fig.4.1.

The BMPG topology requires no voltage sensors for generating HV bipolar rectangular pulses. Generation of multilevel pulse waveforms is possible assuming identical SM-capacitors. Practically, capacitances differ, which will eventually lead

to capacitor voltage drift. A remedy is to use a voltage sensor across each arm as illustrated in Fig.4.19. The measured voltage is compared with a reference voltage; a SM capacitor is only re-charged if its voltage is below the reference during its allocated charging time slot, as illustrated in Fig.4.20. An alternative is one voltage sensor across the series combination V_s and L_i, thus avoiding any sensor high voltage requirement. The sensor measurement bandwidth has to be commensurate with the switching frequency of S1/S2 in order to measure the instantaneous voltage of a SM capacitor voltage when S1/S2 is on.

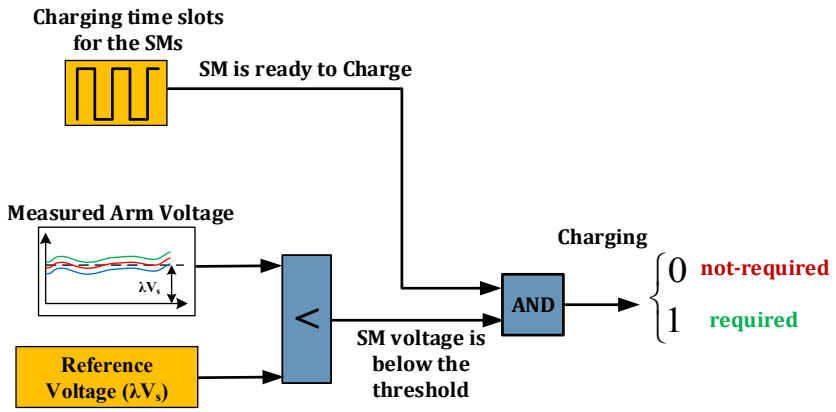


Fig.4.20. Modified SM-capacitors charging mechanism to avoid capacitor voltage drift.

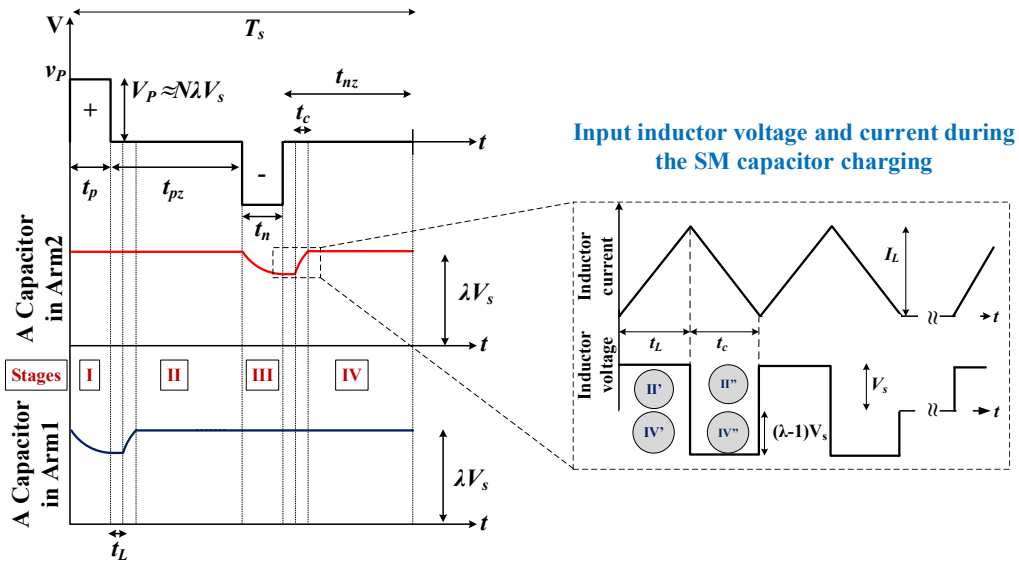


Fig.4.21. Generation of bipolar HV pulses and SM capacitor voltage profile and current through and voltage across the energising input inductor.

A. SM capacitors charging and discharging sequence

In order to generate the required HV pulses across the load R, in Fig.4.21, the following operational sequence assumes the SM-capacitors are pre-charged:

- ***Stage* I**: A positive polarity HV pulse is generated across the load R for the required time t_p by simultaneously inserting the SM capacitors of Arm1 (T_x ON, T_mOFF). During t_p Arm2 SMs are bypassed (T_x OFF, T_m ON) while switches S1 and S2 are both off, as shown in Fig.4.22a.
- ***Stage* II**: Individual SM capacitors of Arm1 are re-charged for the next positive pulse generation for t_{pz}. In creating the voltage boost feature, this stage is divided into two sub-stages (II' and II'').
  - **i)** ***Sub-stage* II'**, in Fig.4.22b, S1 is turned ON and the main switch of a SM in Arm1, T_m, is turned on (as are other T_m in other SMs). Then a current I_L energises the input inductor L_i for a pre-designed time t_L.
  - **ii)** ***Sub-stage* II''**, shown in Fig.4.22c. A switch T_m is turned off and inductor energy diverts current into that SM's capacitor via the diode in antiparallel with T_x. This boost converter action charges the SM capacitor for a pre-designed charging time t_c.

  The two sub-stages are repeated on each arm SM and stage II is completed when each SM capacitor in Arm1 is charged to a DC voltage λV_s, such that λ is the voltage boost factor. The voltage across the load is zero during this SM capacitor charging process, since both switches in the other arm's SMs are off.
- ***Stage* III**: For a negative pulse period t_n, a negative polarity HV pulse of peak $-N\lambda V_s$ is formed across the load by inserting Arm2 capacitors, while bypassing Arm1 SMs, (with S1 and S2 off), as shown in Fig.4.22d.
- ***Stage* IV**: similar to stage II, this stage is divided into IV' as in Fig.4.22e and IV'' as in Fig.4.22f. The individual SM capacitors of Arm2 are re-charged ready for the next negative pulse generation for t_{nz}, while imposing no voltage across the load.

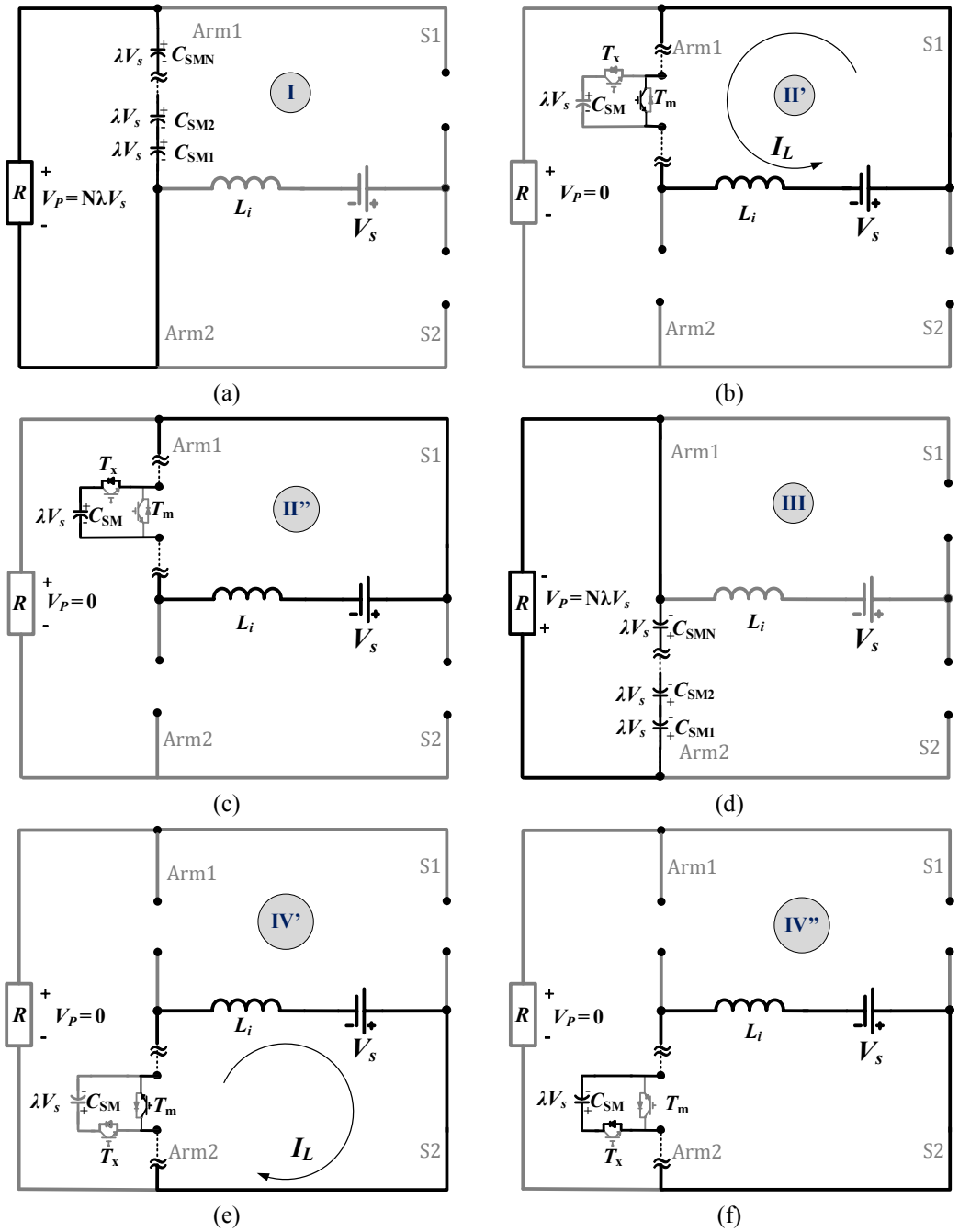


Fig.4.22. BMPG circuit configurations during bipolar pulse generation stages.
(a) Stage I. (b) Stage II'. (c) Stage II". (d) Stage III. (e) Stage IV'. (f) Stage IV".

B. Adjusting the voltage-boost ratio

As illustrated in Fig.4.21, before inserting each SM-capacitor for charging, the input inductor is energised: the charging current i_L will have a current ripple of

$$\Delta I_L = \frac{V_s \Delta t}{L_i} \tag{4.27}$$

where V_s is the LV DC supply voltage and ΔI_L is the current ripple. The inductor voltage, illustrated in Fig.4.21, must obey the voltage-second balance rule:

$$V_s t_L = V_s(\lambda - 1)t_c \tag{4.28}$$

Re-arranging yields:

$$\frac{t_c}{t_L} = \frac{1}{\lambda - 1} \tag{4.29}$$

The software controller determines and assigns the ratio between the time of energising the input inductor, t_L, and the SM capacitor charging time, t_c. For example, if the SM capacitors are to be charged to twice the input LV DC voltage, then $\lambda = 2$ whence $t_L = t_c$ according to (4.29).

C. Input inductor and SM-Capacitance sizes

The minimum inductance is selected to control the current ripple of the charging current of the SM capacitors. Thus the inductance can be estimated from

$$L_i \geq \frac{V_s t_L}{\Delta I_L} \tag{4.30}$$

The SM footprint/volume is dominated by its capacitor size and an estimation of the SM capacitance is as given in (4.26).

The resultant repetition rate of the generated pulses can be calculated from (4.31):

$$T_s = t_p + t_n + 2N(t_L + t_c) \tag{4.31}$$

Table 4.4: Simulation and Experimentation Specifications of the BMPG

Parameter		Simulation	Experimental
LV DC input voltage	V_s	1 kV	50 V
Number of SMs per Arm	N	3	3
Load resistance	R	1 kΩ	500 Ω
Input inductance	L_i	600 µH	650 µH
SM capacitance	C_{SM}	1 µF	10 µF
Assigned SM charging time	t_c	5 µs	20 µs
Pulse duration for both polarities	t_{pl}	5 µs	20 µs
Percent remaining voltage (pu)	β	0.99	

4.2.2 Simulation Results for the BMPG

MATLAB/Simulink simulations are used to assess the viability of the proposed BMPG topology, with the specifications in Table 4.4. With three SMs per arm and an input voltage of 1kV, the BMPG is simulated when charging each SM capacitor to double the input voltage, that is $\lambda = 2$. Fig.4.23a shows the generated bipolar pulses across the load while Fig.4.23b shows the SM capacitor voltages for the Arm1. Since the boost factor is 2, each SM-capacitor is charged to 2kV, and the peak of the generated pulse is 6kV with $T_s = 70\mu s$, as shown in Fig.4.23a. Fig.4.23c shows the input inductor current with equal charging and discharging times, $t_L = t_c$.

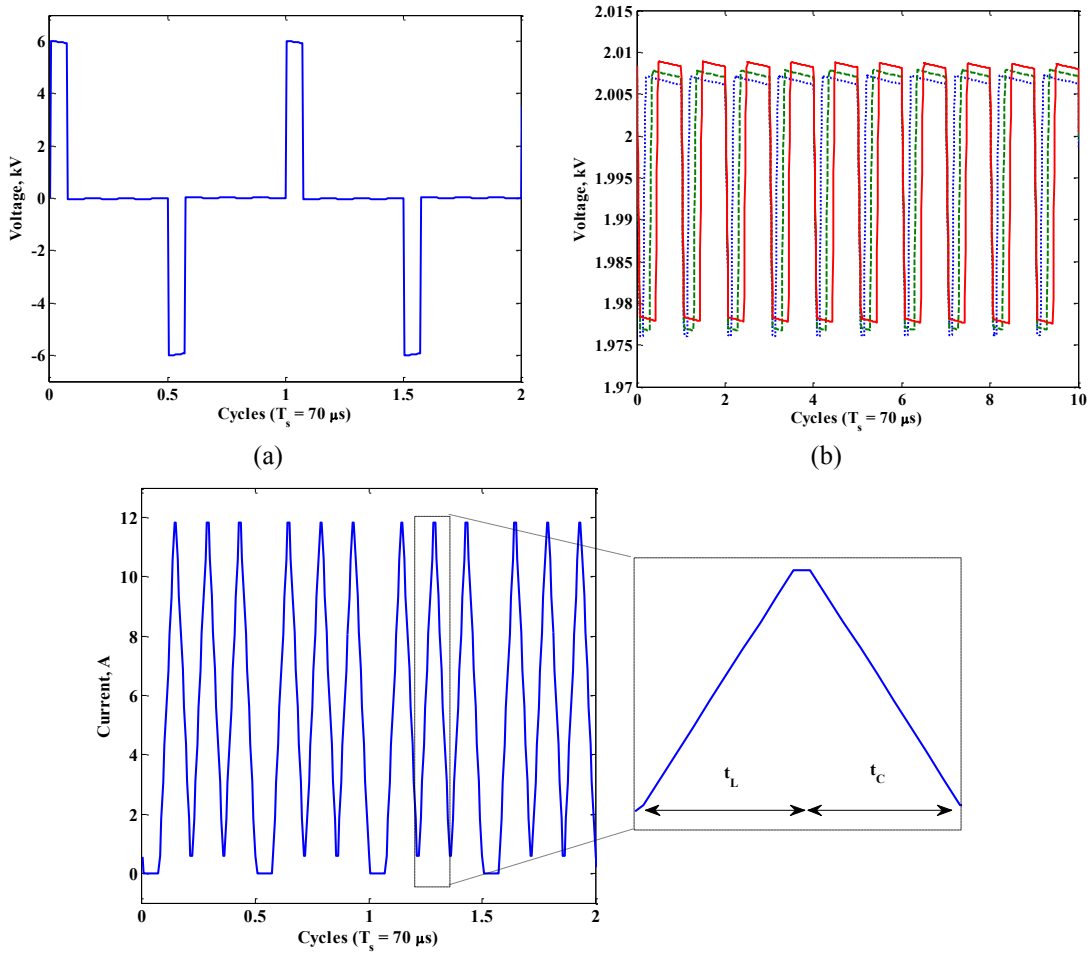


Fig.4.23. Simulation of HV rectangular pulses generated by BMPG with ae boost factor $\lambda = 2$. (a) Voltage pulses. (b) Arm1 SM-capacitor voltages. (c) Input inductor current.

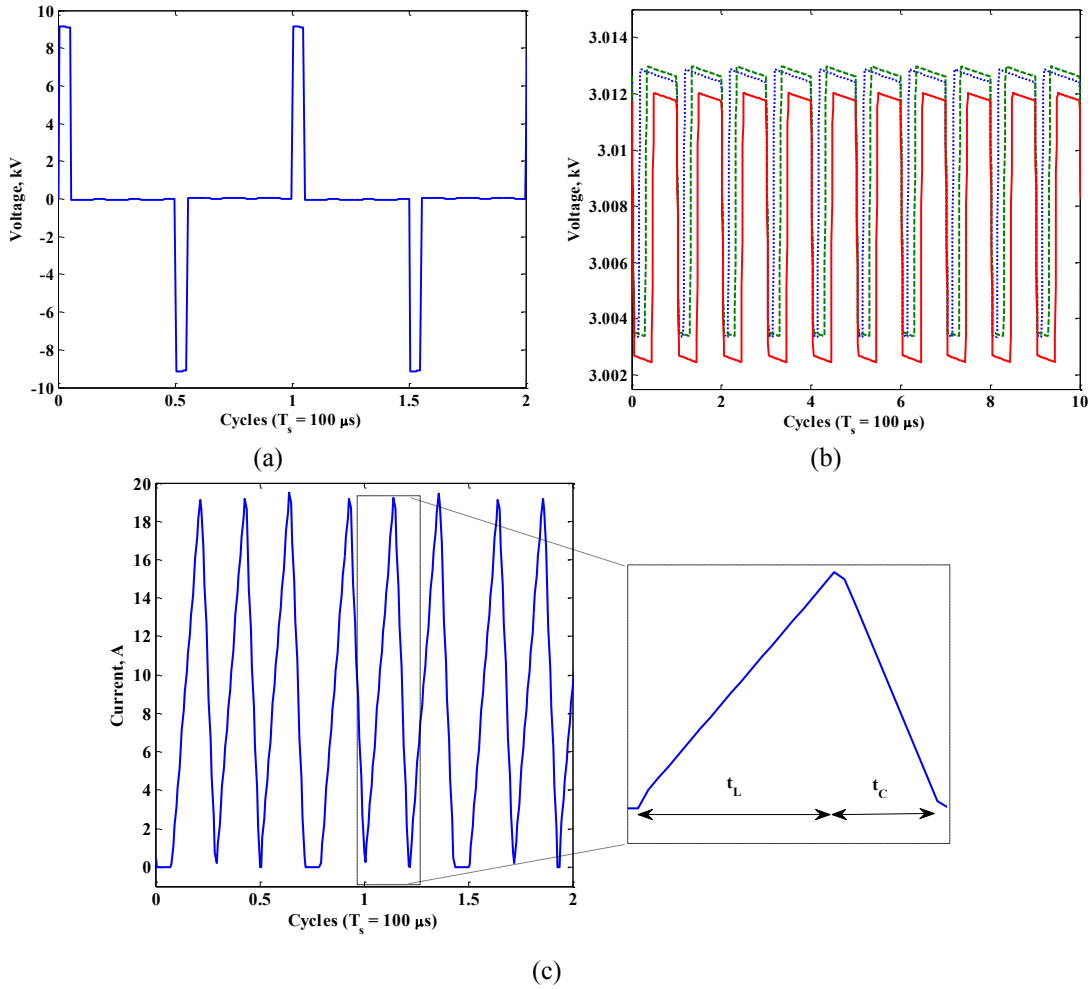


Fig.4.24. Simulation of HV rectangular pulses generated by BMPG for a boost factor $\lambda = 3$. (a) Voltage pulses. (b) Arm1 SM-capacitor voltages. (c) Input inductor current.

For $\lambda = 3$, the energising time of the inductor is increased such that $t_L/t_c = 2$ according to (4.29). For the same parameters, Table 4.4, Fig.4.24a explores the output voltage pulse which has a 9kV peak and $T_s = 100\mu s$ repetition time. The SM capacitor charging voltage is three times the input supply, 3 kV, as shown in Fig.4.24b. The input inductor current is shown in Fig.4.24c.

The proposed charging mechanism (in 4.2.1 A) to avoid capacitor voltage drift shown in Fig.4.20, is simulated when the SM capacitances are mismatched. With $\lambda = 2$ and $V_s = 1$kV, the positive arm is programmed to generate multilevel pulse whereas the negative arm is programmed to generate rectangular pulse. The capacitances of the three SMs either in the upper or the lower arm are mismatched as follows 8µF, 10µF and 12µF (viz. 20% deviation from the nominal of 10µF). Each

SM capacitor is expected to fluctuate around 2kV and the pulse peak-voltage is expected to be 6kV. Fig.4.25a shows the train of the generated pulses before and after applying the proposed controlled charging mechanism. The corresponding SM capacitor voltages of the positive and negative arms are shown in Fig.4.25b and Fig.4.25c, respectively. After activating the proposed charging mechanism, the capacitor voltages balanced regardless their capacitances difference and the experienced voltage drift is alleviated. The simulated capacitance deviation is higher than the practical capacitance values deviation (typically 5% for plastic types), such that the control algorithm is tested at extreme conditions.

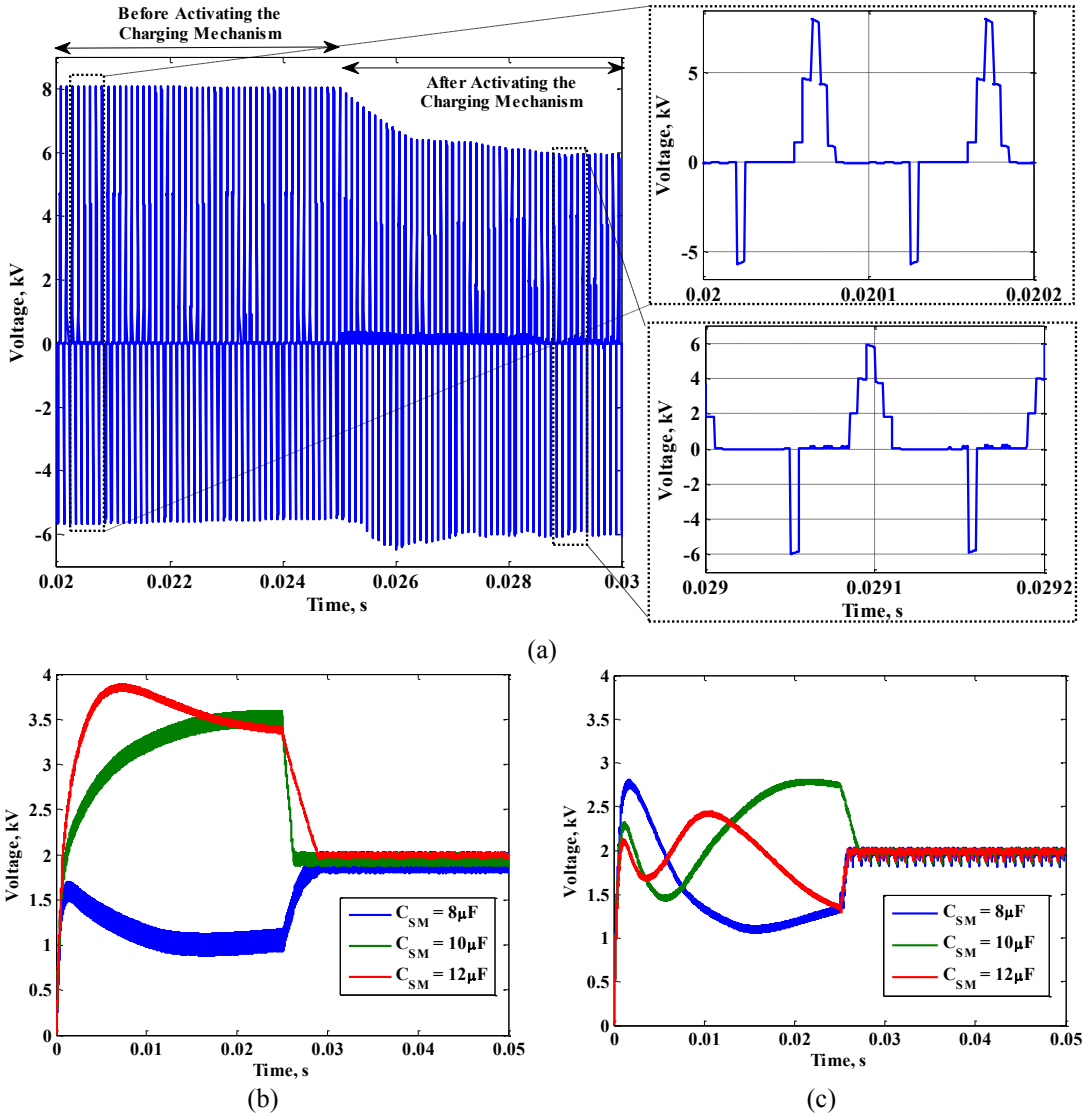


Fig.4.25. Simulation of applying the proposed charging mechanism when $\lambda = 2$.
(a) Voltage pulses. (b) Arm1 SM-capacitor voltages. (c) Arm2 SM-capacitor voltages.

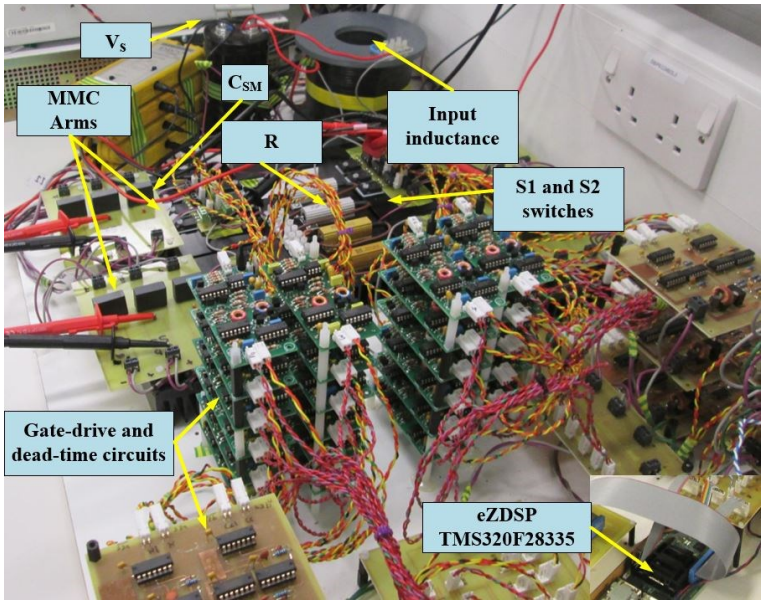


Fig.4.26. BMPG proof of concept experimental set-up.

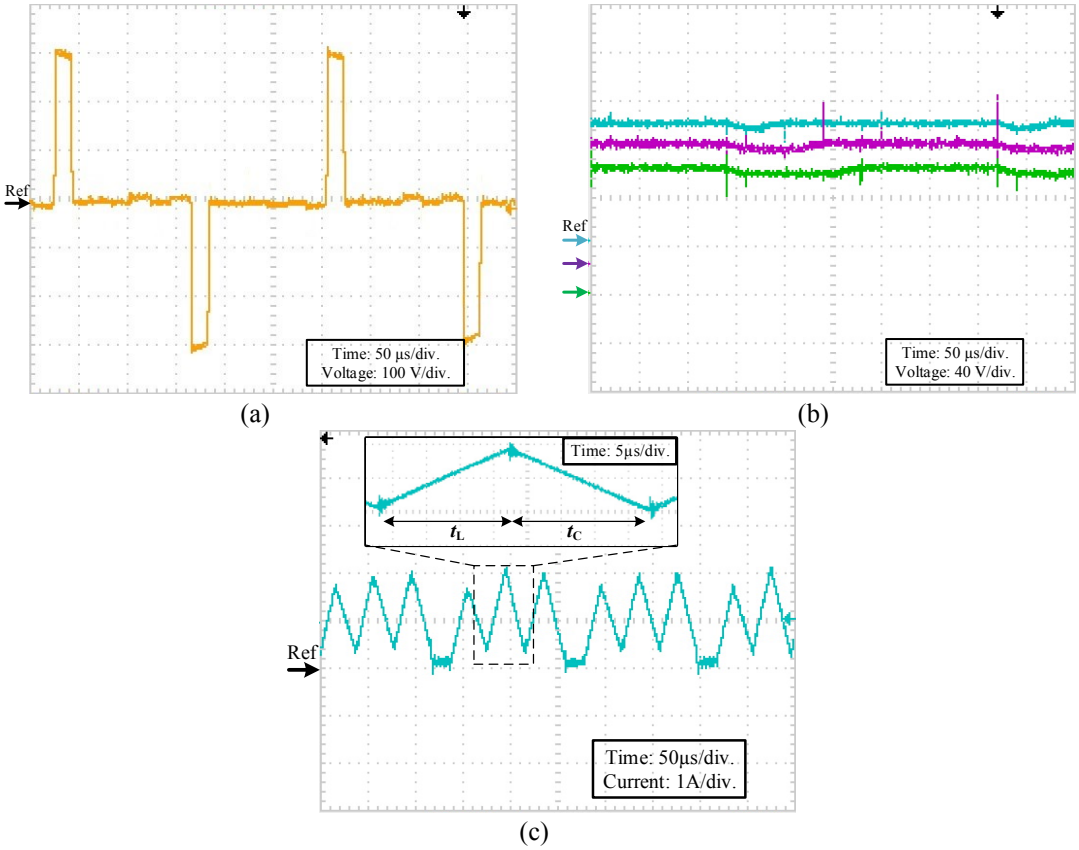


Fig.4.27. BMPG experimental results when $\lambda = 2$.
(a) Voltage pulses. (b) Arm2 SM-capacitor voltages. (c) Input inductor current.

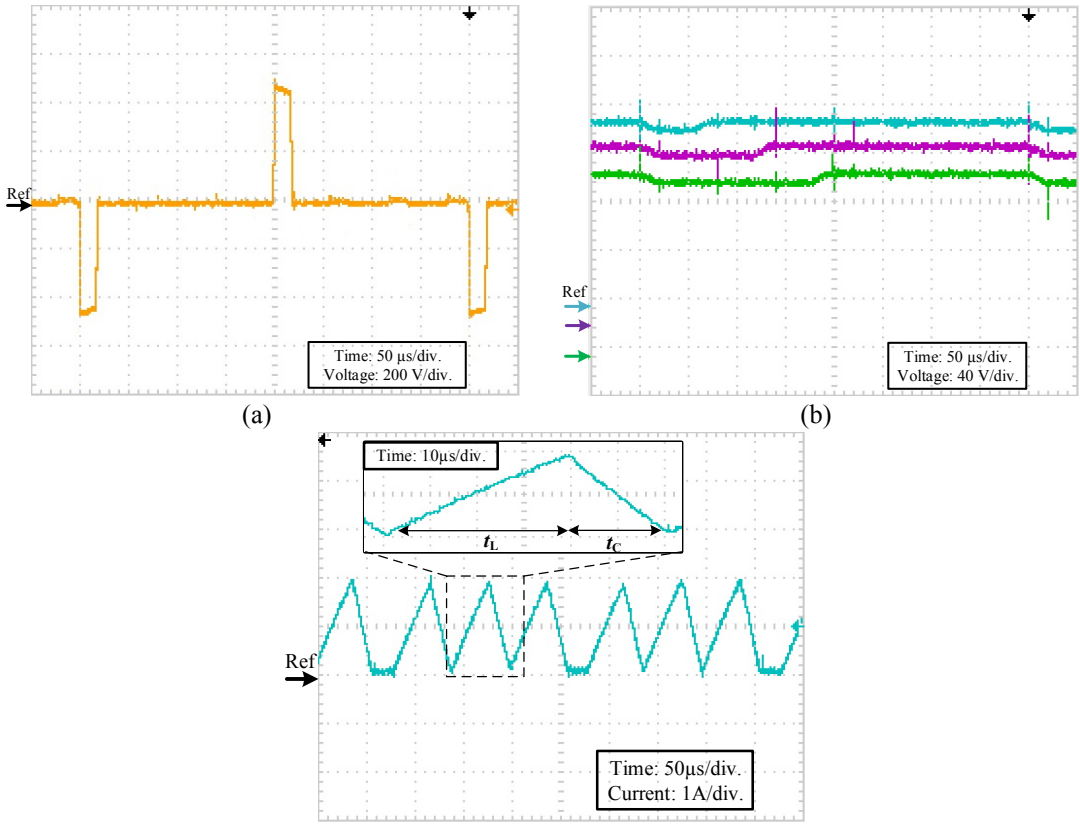


Fig.4.28. BMPG experimental results when $\lambda = 3$.
(a) Voltage pulses. (b) Arm2 SM-capacitor voltages. (c) Input inductor current.

4.2.3 Experimental Results for BMPG

The proof of concept experimental set-up, shown in Fig.4.26, uses IGBTs STGW30NC60WD in Arm1 and Arm2, which have antiparallel diodes, while the reverse blocking switches S1 and S2 are Infineon IGW60T120 IGBTs in series with IXYS DSEI30-10A power diodes.

The experimental results are shown in Fig.4.27 and Fig.4.28 for boost ratios λ =2 and 3, respectively. The generated voltage pulses are shown in Fig.4.27a and Fig.4.28a, where for the same input DC voltage, the output voltage is doubled and tripled. Thus, the pulse peak voltage for $\lambda = 2$ is $V_P = 300\text{V}$ as shown in Fig.4.27a, while $V_P = 440\text{V}$, as shown in Fig.4.28a, for $\lambda = 3$.

The repetition rate is reduced in the tripled case as more time is required to energise the inductor. $T_s = 260\mu s$ when $\lambda = 2$ and $T_s = 400\mu s$ when $\lambda = 3$. For both cases the voltages of Arm2 capacitors are shown in Fig.4.27b and Fig.4.28b for $\lambda = 2$ and $\lambda = 3$, respectively. Individual capacitor voltages are balanced around 150V.

Finally, the inductor input current is depicted in Fig.4.27c and Fig.4.28c for $\lambda = 2$ and 3, respectively. For $\lambda = 2$, the assigned time for energising the inductor and charging the capacitor are equal, while the energising time is double the capacitor charging time when $\lambda = 3$.

The proposed BMPG charging technique allows a reduction in converter size by charging each SM individually to λV_s such that λ is a controllable voltage-boost ratio, then the charged capacitors are inserted in series across the load terminal generating a pulse peak of $\lambda N V_s$. Along with no voltage sensors, reduced converter footprint and flexible HV pulse generation, the proposed converter can utilise commercially available semi-conductors by proper input inductance selection. But for accurate pulse generation the inductance may need adjusting to comply with any new desired current rating.

4.3 Generic HV PG with Voltage Boost Capability

The sequential PG, SPG, topology provides an effective sequential charging technique for the N MMC SM capacitors. Each SM capacitor is charged to the input voltage level V_s, thus, the maximum obtained pulse voltage peak is NV_s. In order to increase the SPG voltage gain, a voltage boost mode of operation was suggested in section 4.2 for the BMPG, hence, the maximum obtained pulse voltage peak is $N\lambda V_s$. These two topologies generate rectangular pulse waveforms with flexible characteristics and without utilising voltage sensors. But, practically, the capacitors are not identical hence the SM capacitor voltages will voltage drift if other conventional pulse waveforms (such as the ramp, multipulse or multilevel) are generated without deployment of individual SM voltage sensors. Although a single voltage measurement transducer can be used the across the series connected V_s and L_i, its necessary bandwidth to sample the capacitor voltage magnitude when the boosting switch is off, may be challenging.

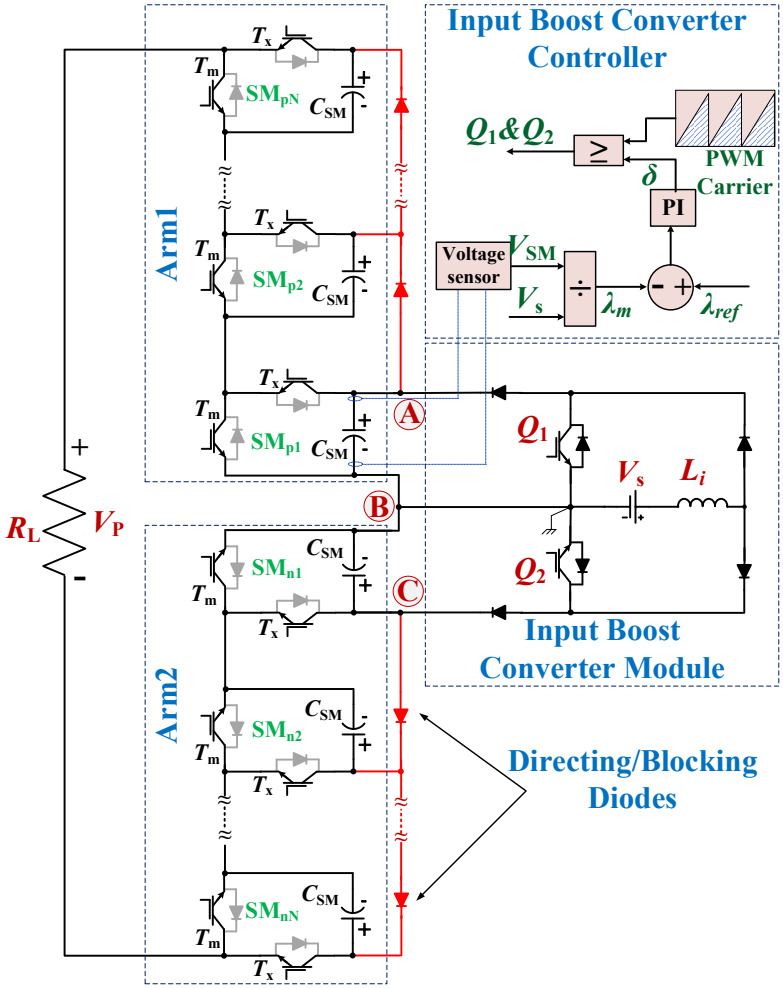


Fig.4.29. The BPG converter topology.

In order to generate the commonly used electroporation pulse waveforms while assuring capacitor voltage balance and high voltage gain, a generic sequential charging HV PG with voltage-boost capability (BPG) is proposed.

4.3.1 Proposed BPG Topology

The proposed bipolar HV PG with voltage-boost capability (BPG), is shown in Fig.4.29. It is formed of three main parts namely: input boost converter module with its controller; upper arm (Arm1); and lower arm (Arm2). The boost converter module has input inductor L_i, two identical IGBTs Q_1 and Q_2, and four directing/blocking diodes (effectively each series diode in $S1$ and $S2$ in Fig.4.1 and in Fig.4.6, is moved to a corresponding voltage level SM thus providing inherent reverse voltage sharing).

The boost module has three terminals: B is common to both arms, and A and C are connected via a diode to the positive terminal of the first SM capacitor in Arm1 and Arm2, respectively.

Arm1 generates positive polarity HV pulses across the load; its first SM capacitor positive and negative terminals are connected to the terminals A and B respectively. Arm2 is responsible for generating the negative HV polarity pulse across the load; its first SM capacitor positive and negative terminals are connected to the terminals C and B respectively. Each arm is formed of series connected MMC HB-SMs. The SMs of Arm1 are denoted SM_{pj}, and the SMs of Arm2 are denoted SM_{nj}, where, p and n denote positive and negative pulses, respectively, and $j \in \{1, 2, \dots, N\}$ where N is the number of SMs per arm. Unlike in the conventional MMC, the SM capacitor positive terminals are connected to each other via external directing/blocking diodes. These diodes allow the input boost converter to charge the required capacitor while blocking current flowing back from higher level SMs, to other capacitors. Each HB-SM is formed of two IGBT switches, T_m and T_x. Control of these two switches, means the SM terminals can either develop zero voltage, (*bypassed*, when T_m is on and T_x is off) or the capacitor voltage, (*inserted*, when T_m is off and T_x is on). In conventional HB-SM based topologies, SM capacitor charging is attained via the antiparallel diode of switch T_x. In the proposed topology, these diodes ensure voltage sharing of the directing/blocking diodes. However, the charging mechanism of the proposed BPG is different than that of the conventional MMC based PG. Here each SM capacitor is charged directly from the input boost converter sequentially via the directing/blocking diodes.

The SMs are constructed such that their capacitor charging is directly from the input boost converter. Directing/blocking diodes are utilised to control the charging process and to prevent the capacitors from undesirably discharging. The diodes enable capacitor voltage balance, direct any overcharging current to achieve voltage balance, and prevent voltage drifting.

The input boost converter duty ratio δ is controlled by a proportional-integral (PI) controller, which the desired boost ratio λ_{ref} as a reference signal, it only requires voltage measurement of one boost converter level SM capacitor, whence a single voltage sensor indirectly controls all SM capacitor voltages. If only symmetrical

pulses are sought, a single sensor is sufficient whilst for asymmetrical pulses two sensors each with a PI controller are required to individually control each arm.

The BPG aims is to provide a robust HV PG that has the following features:

- does not utilise HV series connected devices that are unclamped by a SM;
- fed from LV DC input supply;
- two-controllable gain variables; the boost converter duty ratio and the number of utilised series SMs;
- one modest bandwidth low voltage sensor per arm for SM capacitor voltage balancing;
- two arms of MMC SMs; and
- flexible and controllable PEF waveforms.

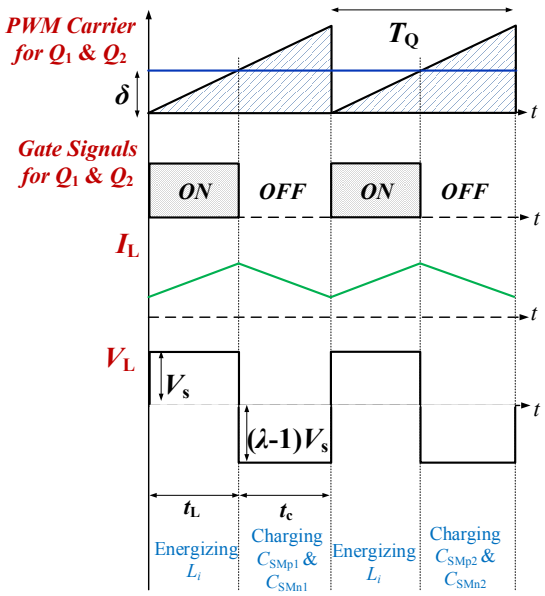


Fig.4.30. Energising sequence of the input inductor by controlling switches Q_1 and Q_2.

Normally, sequentially charged MMC topologies have a relatively low repetition rate, as each individual SM capacitor has to be re-charged after contributing to the HV pulse. Adding a boost converter in the input stage will further increase the repetition time as the charging time of the SM capacitors is divided in two parts, first the boost converter inductor is energised and then the capacitor is charged. To overcome this drawback, the BPG topology only utilises sequential charging when

starting, while charging two SMs simultaneously. After delivery of an HV pulse, with the directing/blocking diodes and the main switch in each SM, all SM capacitors are recharged sequentially in parallel to the desired voltage level. Thus the proposed topology can achieve high repetition rate HV pulses from an LV DC input.

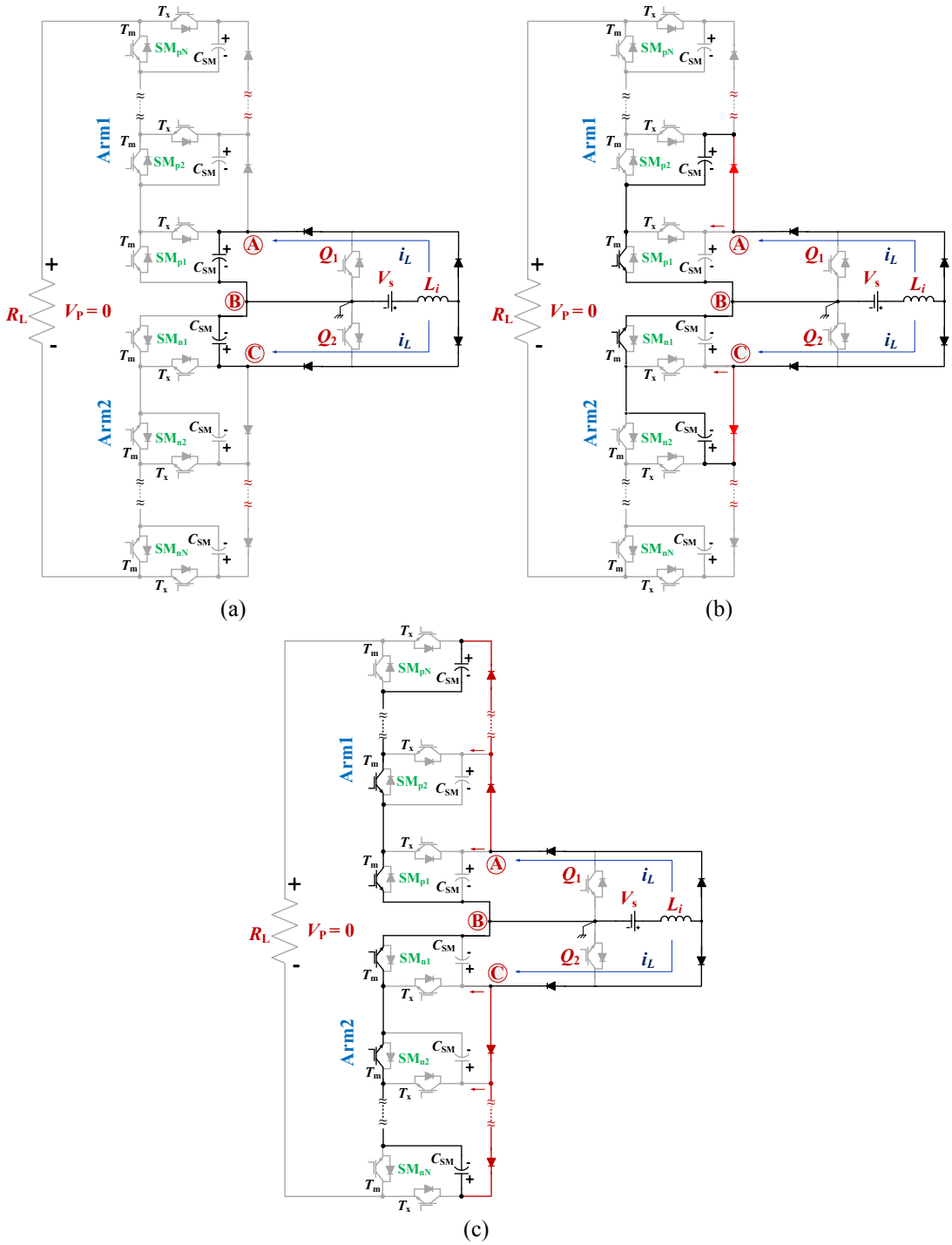


Fig.4.31. SM capacitor charging sequence. (a) First SM. (b) Second SM. (c) Last SM.

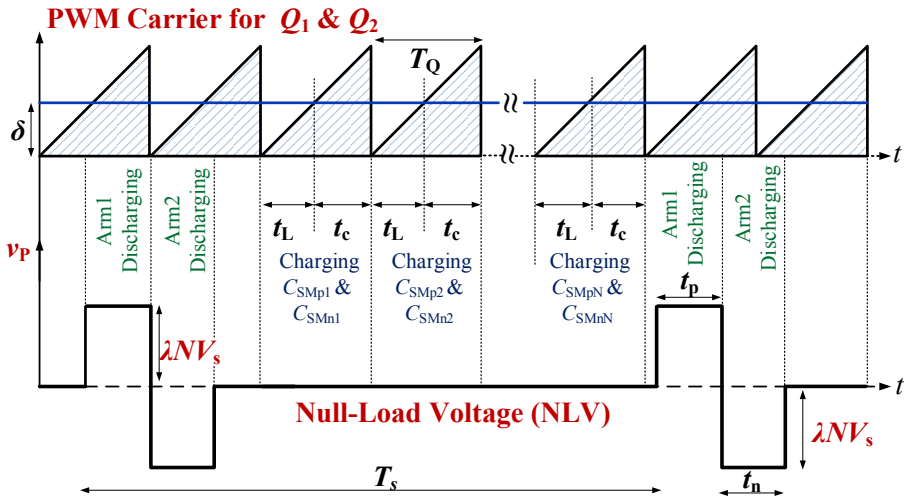


Fig.4.32. Bipolar rectangular pulse generation sequence.

A. SM capacitor charging and discharging sequence

Since the DC charging source is via a boost converter, initial system capacitor charging cannot be controlled by the boost converter. It is therefore assumed the input DC source is controlled ramped from zero voltage, with all switches T_m in both arms, in the on state. As an alternative, a buck boost input stage is offered in Fig.4.35.

The input boost converter is controlled by a PI controller, which generates the required duty ratio δ. This in turn controls Q_1 and Q_2 switch ON/OFF, creating the desired voltage magnitude λV_s across the boost converter terminals as shown in Fig.4.30. Each SM capacitor is sequentially connected across these terminals, starting from the first SM capacitors C_{SMp1} and C_{SMn1}. During the ON time of Q_1 and Q_2 the input inductor L_i is energised for time t_L and during the OFF time the SM capacitors are allowed to charge for time t_c, as shown in Fig.4.31a. Although a single switch in the input boost converter is sufficient, the existence of two switches operating simultaneously means a low switch current rating. After charging C_{SMp1} and C_{SMn1}, the input inductor is re-energised during the ON time of $Q_1$and Q_2. For charging the second level SM capacitors in Arm1 and Arm2, C_{SMp2} and C_{SMn2}, T_m switches in the previously charged SMs are switched ON, hence, the charging current will flow through the directing diodes to charge C_{SMp2} and C_{SMn2}, for t_c as

shown in Fig.4.31b. The sequential charging process is continued until all the SM capacitors in Arm1 and Arm2 are charged to the desired voltage as shown in Fig.4.31c.

After charging all the SM capacitors, HV bipolar pulse generation across the load, as in Fig.4.32, is initiated by allowing Arm1 SM capacitors to discharge into the load (by switching on T_x of Arm1 and switching on T_m of Arm2 simultaneously, see Fig.4.33a). That is, for positive pulses, SMs in Arm1 are inserted, and bypassed in Arm2. For negative pulses, the states are: bypass Arm2 SMs and insert Arm1 SMs, see Fig.4.33c. SM switch operation is complementary.

In practice, with certain provisions to be specified, charging during normal operation can occur with all the MMC-SMs bypassed (T_m on) as shown in Fig.4.34.

Both SM capacitor charging and pulse generation do not involve the antiparallel diode across switch T_x, but it voltage clamps the directing/blocking diodes whence this antiparallel diode is obligatory. Voltage sharing across SMs is inherent in the charging (all SM capacitors charge to a maximum of λV_s) and discharging mechanisms (SM either remain unchanged or discharge to less than λV_s).

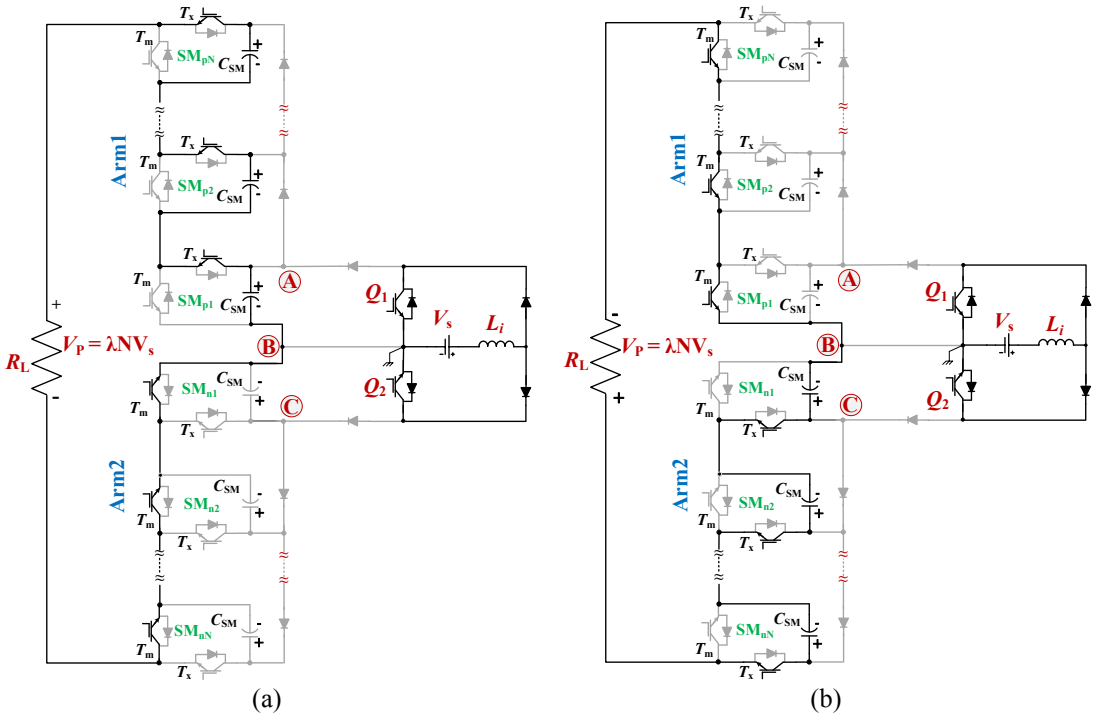


Fig.4.33. Bipolar rectangular pulse generation. (a) Positive pulse. (b) Negative pulse

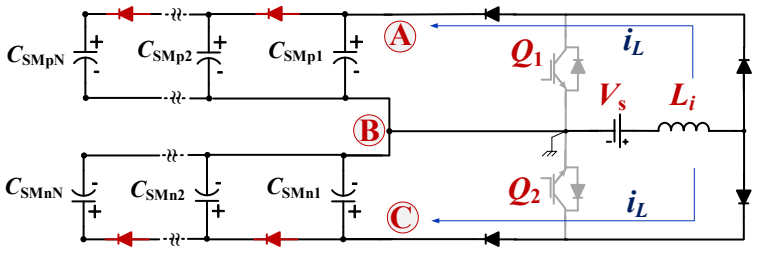


Fig.4.34. Continuous charging for the SM-capacitors.

B. BPG Parameters Estimation

Similar to the BMPG (discussed in section 4.2) and as illustrated in Fig.4.30, before charging the SM capacitors, the input inductor is energised, the current being described by

$$\frac{di_L}{dt} = \frac{V_s}{L_i} \tag{4.32}$$

where V_s is the LV supply voltage. The minimum inductance is selected to control the current ripple of the charging current of the SM capacitors. The inductance can be specified from

$$L_i = \frac{V_s \delta T_Q}{\Delta I_L} \tag{4.33}$$

where ΔI_L is the current ripple.

SM footprint/volume is dominated by its capacitor size. An estimation of SM capacitance is as given in (4.26).

The resultant repetition rate of the generated pulses at the start of charging the SM capacitors sequentially, can be calculated from (4.34):

$$T_s = t_P + t_N + N(t_L + t_c) \tag{4.34}$$

Also, since the energising and charging of the input inductor and the SM capacitor, respectively, occur in time T_Q, which is the repetition rate of the PWM carrier for switches Q_1 and Q_2:

$$T_s = t_P + t_N + NT_Q \tag{4.35}$$

The repetition rate is increased significantly by the parallel charging approach, where the N SMs are charged simultaneously. Thus N is a control variable in continuous operation to specify the desired repetition time T_s. However, for proper

operation, the carrier frequency for the input boost converter must be higher than the generated pulse repetition rate.

C. BPG Topology Variation

With Arm1 and Arm2 intact, the input terminals A, B and C can be connected to a buck-boost converter (instead of a boost converter) as shown in Fig.4.35. This feature is preferred for soft starting from a fixed or uncontrolled DC source. Hence, by utilising the buck-boost converter, the range of the voltage is extended from 0 to λV_s (instead of V_s to λV_s in boost converter case). If soft starting is not required, a boost converter is recommended, since it has a wider control range and less stresses on the input switches, compared to the buck-boost converter [81].

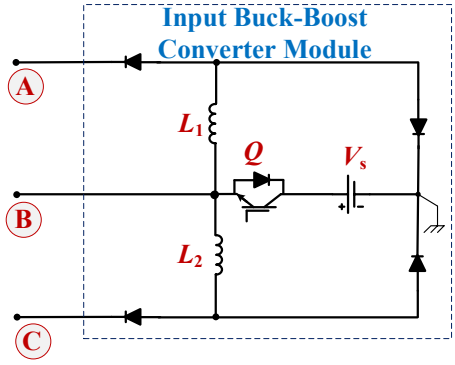


Fig.4.35. Input buck-boost converter module.

Table 4.5: Simulation and Experimentation Specifications of the BPG

Parameter		Simulation	Experimental
LV DC input voltage	V_s	500V	50 V
Number of SMs per Arm	N	5	3
Load resistance	R	500 Ω	500 Ω
SM capacitance	C_{SM}	5 µF	5 µF
Input inductance	L_i	1 mH	3.5 mH
PWM carrier repetition time	T_Q	25 µs	40 µs
Pulse duration for both polarities	t_{pl}	25 µs	50 µs
Percent remaining voltage (pu)	β	0.95	

4.3.2 Simulation Results for the BPG

The proposed BPG, with five SMs per each arm, is Matlab/Simulink simulated with the specifications in Table 4.5.

With a voltage-boost ratio of $\lambda = 2$, a bipolar rectangular pulse waveform of $T_s = 175\mu s$ and symmetrical pulse durations of $t_p = t_n = 25\mu s$ is shown in Fig.4.36a. Each SM capacitor is charged to 1kV as shown in Fig.4.36b, thus with five SMs per arm, the peak voltage of the generated rectangular pulse is 5kV, as shown in Fig.4.36a. The current and the voltage of the input boost converter inductor, shown in Fig.4.36c, for $\lambda = 2$. The inductor energising time is the same as the capacitor charging time. The inductor produces 500V on the capacitor during charging as shown in Fig.4.36c. The controller generated duty ratio δ and the PWM carrier are shown in Fig.4.36d.

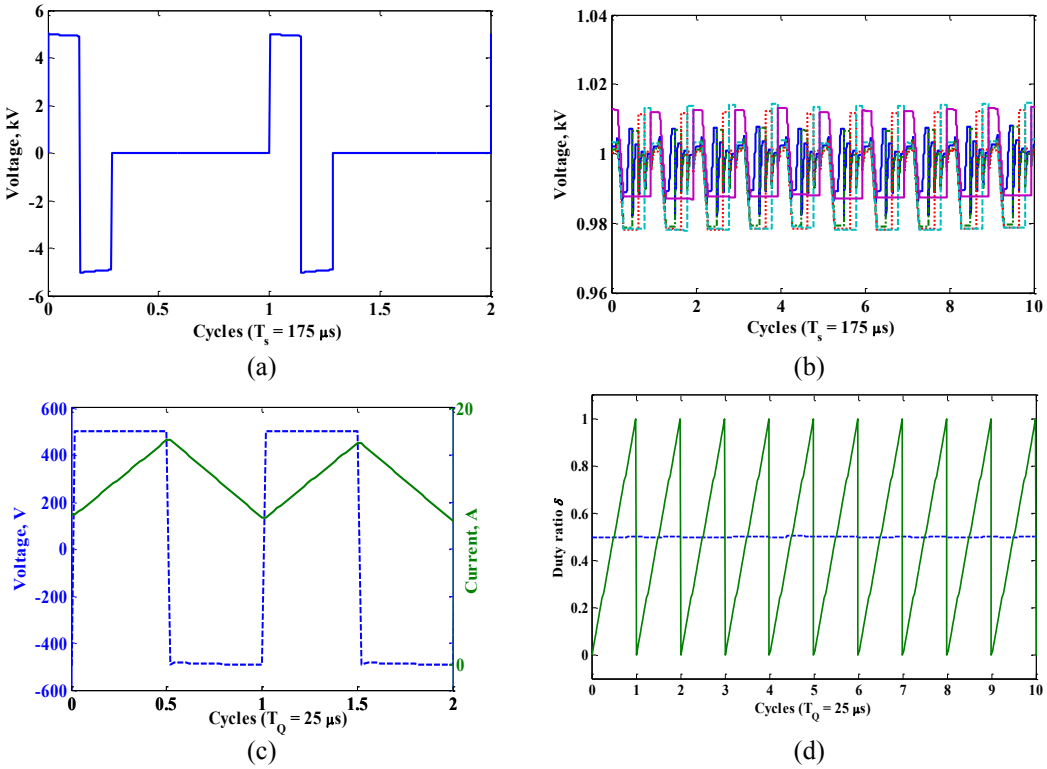
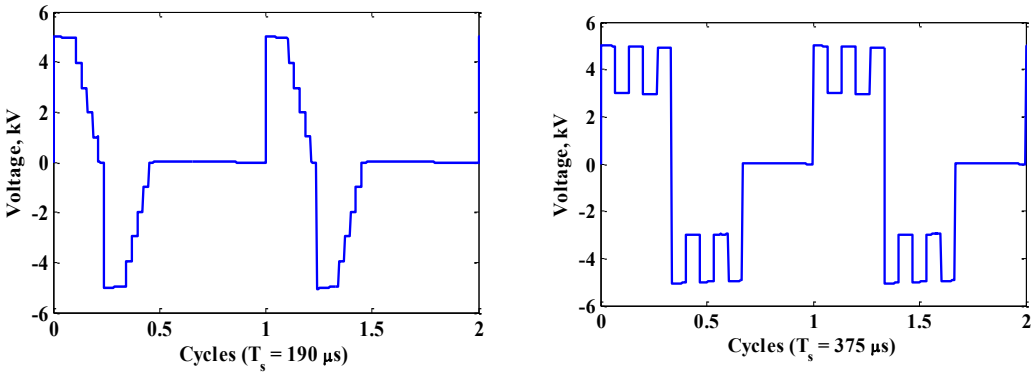
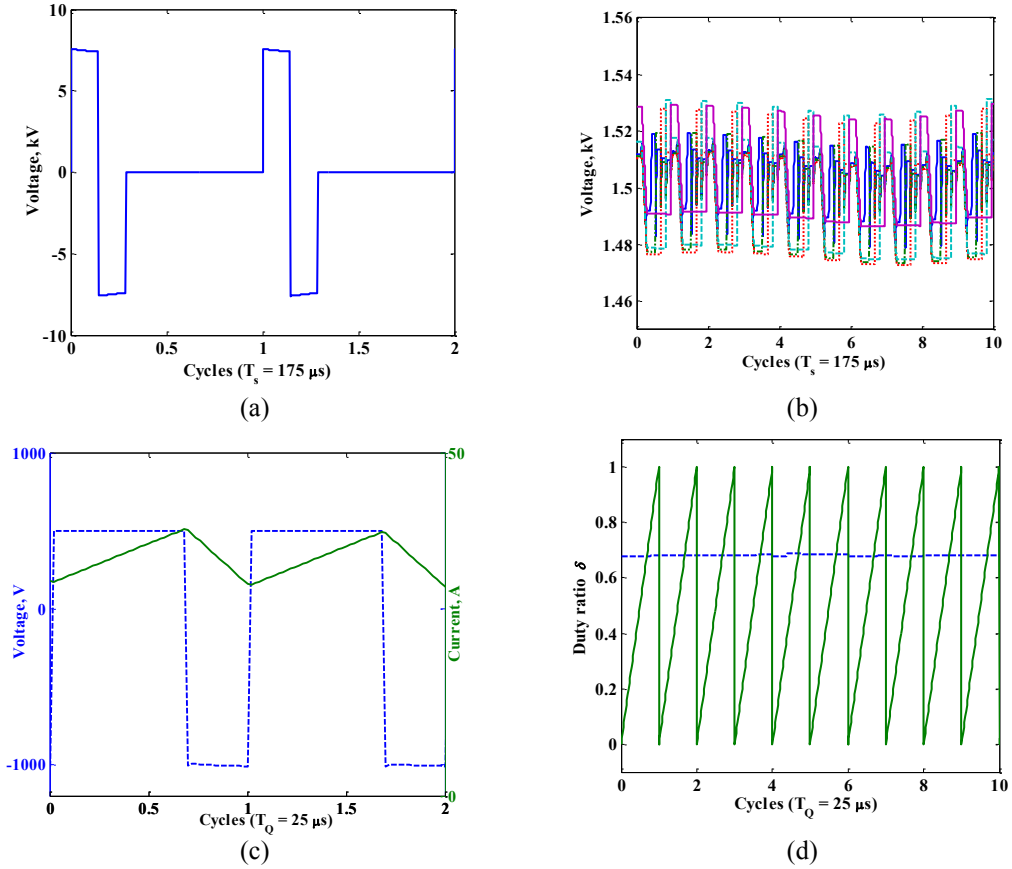


Fig.4.36. Simulation results for BPG generated bipolar rectangular waveform ($\lambda = 2$).
(a) Generated pulses. (b) Arm2 capacitor-voltages. (c) Input inductor voltage and current. (d) Input boost converter duty ratio.



(a) (b)

Fig.4.37. Simulation results for BPG commonly used PEF bipolar pulse waveforms ($\lambda = 2$). (a) Ramp. (b) Multipulse.



(a) (b)

(c) (d)

Fig.4.38. Simulation results for BPG generated bipolar rectangular waveform ($\lambda = 3$). (a) Generated pulses. (b) Arm2 capacitor-voltages. (c) Input inductor voltage and current. (d) Input boost converter duty ratio.

The topology can generate commonly used pulse waveforms, such as the ramp and multipulse. With a voltage-boost ratio of $\lambda = 2$, Fig.4.37a shows a symmetrical bipolar ramp pulse waveform with $T_s = 190\mu s$. The SM capacitors are inserted

simultaneously, hence, a peak voltage of 5kV appears across the load for the required plateau time; Fig.4.37a, 20μs, then the SM capacitors are bypassed progressively (an outer SM before an inner SM, $j = 5, 4, 3, 2, 1$) every 5μs until all are bypassed. In Fig.4.37b, with a voltage-boost ratio of $\lambda = 2$, a symmetrical bipolar multipulse waveform of $T_s = 375\mu s$ is shown. Forming two superimposed pulses of wider and narrow duration is created by inserting all the arm SM capacitors simultaneously, then bypassing some simultaneously. The process is repeated based on the desired narrow pulse repetition time. In Fig.4.37b, the wider pulse repetition time is $375\mu s$, while the narrow pulse repetition time is $50\mu s$ with two SMs bypassed.

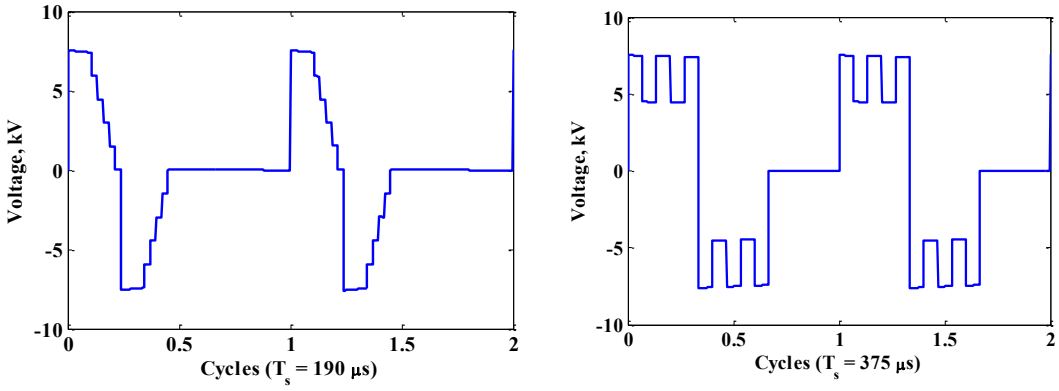
SM insertion and bypassing should comply with:

- an inner capacitor is always inserted before an outer capacitor.
- an outer capacitor is always bypassed before an inner capacitor.

This means an outer capacitor will always retain a higher voltage than an inner capacitor, after pulse generation. Otherwise uncontrolled current flows through the directing diodes to outer SMs when charging.

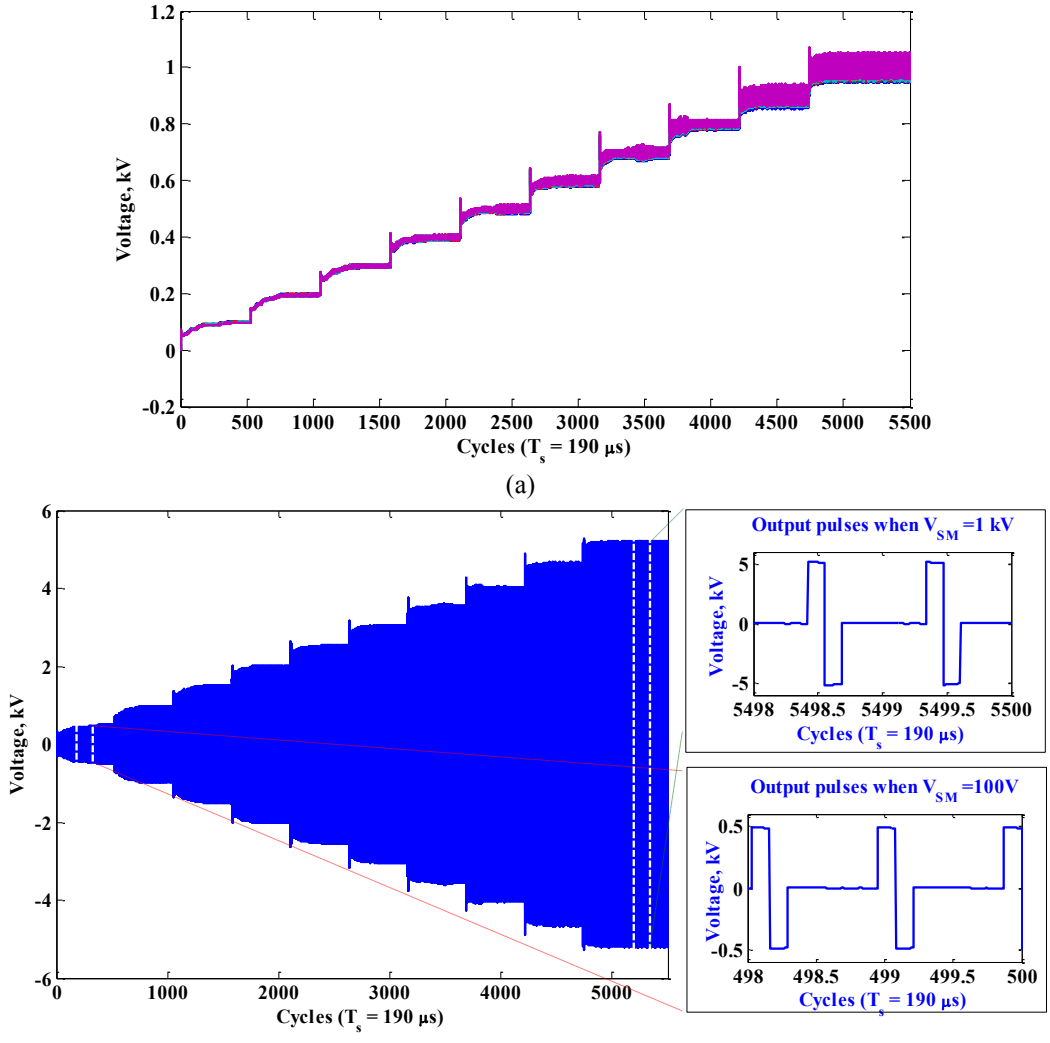
The benefit from applying closed loop control to the input boost converter is to vary the voltage boost ratio and the controller automatically assigns the correct inductor energising time, such that the SM capacitors charge to the desired voltage λV_s. Fig.4.38a shows a bipolar rectangular pulse waveform of 7.5kV peak, $T_s = 175\mu s$ and symmetrical pulse durations of $t_p = t_n = 25\mu s$ when $\lambda = 3$. The SM capacitors are charged to 1.5kV as shown in Fig.4.38b, while the input inductor voltage and current and controller generated duty ratio are in Fig.4.38c and Fig.4.38d, respectively. Generation of bipolar ramp pulses and multipulse waveforms are shown in Fig.4.39a and Fig.4.39b, respectively.

Start-up of the proposed BPG, when a buck-boost converter replaces the input boost converter, is illustrated in Fig.4.40. The input supply is $V_s = 500V$, and the SM-capacitor voltages are ramped from 0 to 1kV in 100V steps, as shown in Fig.4.40a, the first SM capacitor voltage is measured and feed to the controller which in turn controls the duty ratio of the buck-boost converter. The train of the bipolar rectangular pulses generated in this case is shown in Fig.4.40b, where the pulse peak voltage is 500V at the start, and eventually reaches 5kV as commanded.



(a) (b)

Fig.4.39. Simulation results for BPG commonly used PEF bipolar pulse waveforms ($\lambda = 3$). (a) Ramp. (b) Multipulse.



(a)

(b)

Fig.4.40. Simulation results for BPG when a buck-boost converter replacing the input boost converter and the SM-capacitor charging voltage is ramped from 0 to 1 kV. (a) Arm2 capacitor-voltages. (b) Generated bipolar rectangular pulses.

4.3.3 Experimental Results for BPG

The proof of concept experimental set-up shown in Fig.4.41 uses IGBT switches STGW30NC60WD in Arm1, Arm2 and the input boost converter, plus IXYS DSEI30-10A directing/blocking power diodes. Each arm is comprised of three SMs.

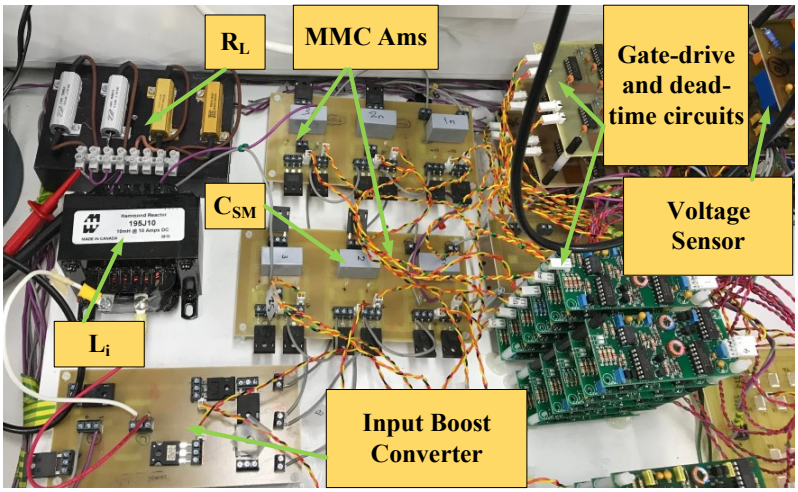


Fig.4.41. The proof of concept BPG experimental rig.

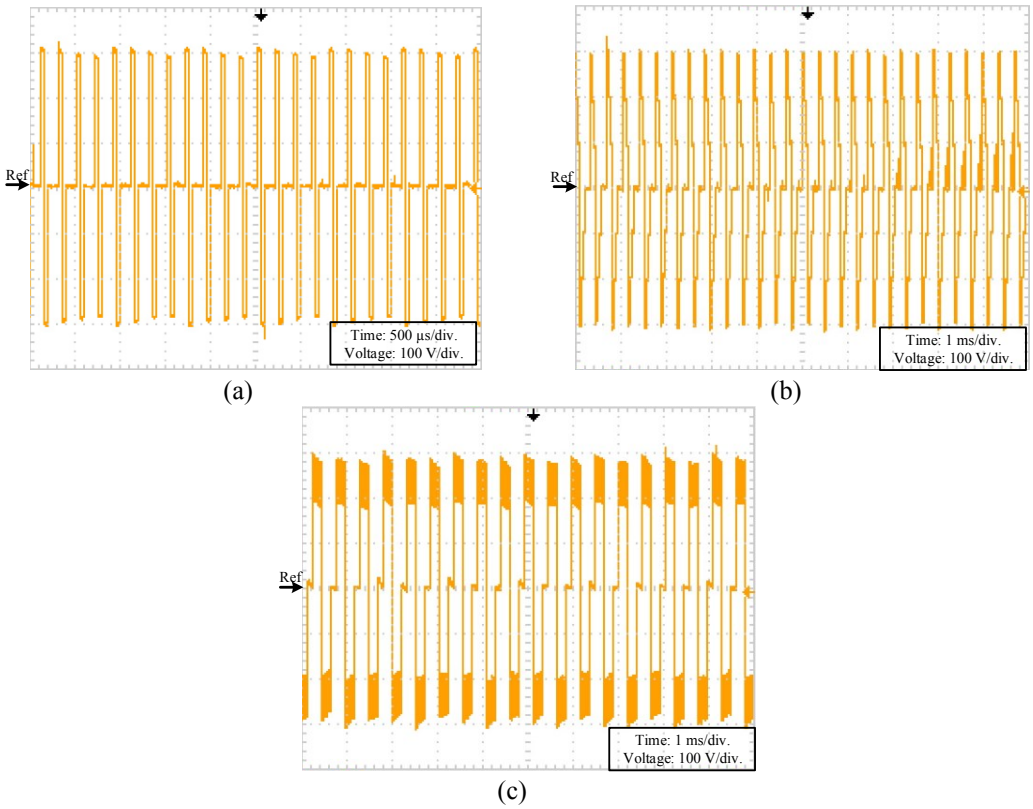


Fig.4.42. BPG experimental results for a train of conventional bipolar PEF pulse waveforms ($\lambda = 2$). (a) Rectangular. (b) Ramp. (c) Multipulse.

With a boost factor of $\lambda = 2$, $V_s = 50\text{V}$ and the specification in Table 4.5, three trains of the conventional PEF pulse waveforms are generated as shown in Fig.4.42. The rectangular pulses with $t_p = t_n = 40\mu\text{s}$ are given in Fig.4.42a. Fig.4.42b shows the ramp pulses with a step-voltage of $20\mu\text{s}$ whereas Fig.4.42c shows the multipulse train when a single SM is bypassed and inserted every $20\mu\text{s}$ to form the short duration pulses. A zoomed view for the three pulse waveforms is depicted in Fig.4.43 along with Arm2 SM capacitor voltages. For the 50V input voltage, each SM capacitor charges to 100 V, as shown in Fig.4.43. Two cycles for the rectangular ($T_s = 200\mu\text{s}$), ramp ($T_s = 360\mu\text{s}$) and the multipulse ($T_s = 520\mu\text{s}$) waveforms are shown in Fig.4.43a, Fig.4.43b and Fig.4.43c, respectively. The input boost-converter voltage and current are shown in Fig.4.43d during rectangular pulses generation.

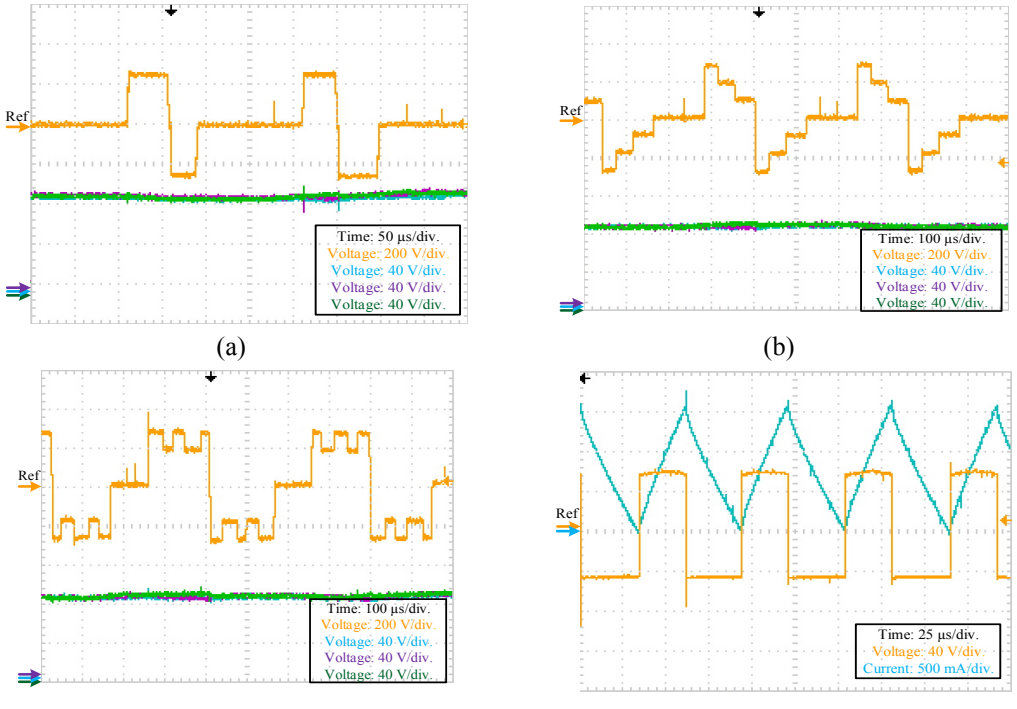


Fig.4.43. BPG experimental results for bipolar PEF pulse waveforms ($\lambda = 2$).
(a) Zoom of rectangular pulses. (b) Zoom of ramp pulses. (c) Zoom of multipulse pulses. (d)Input inductor voltage and current when generating rectangular pulses.

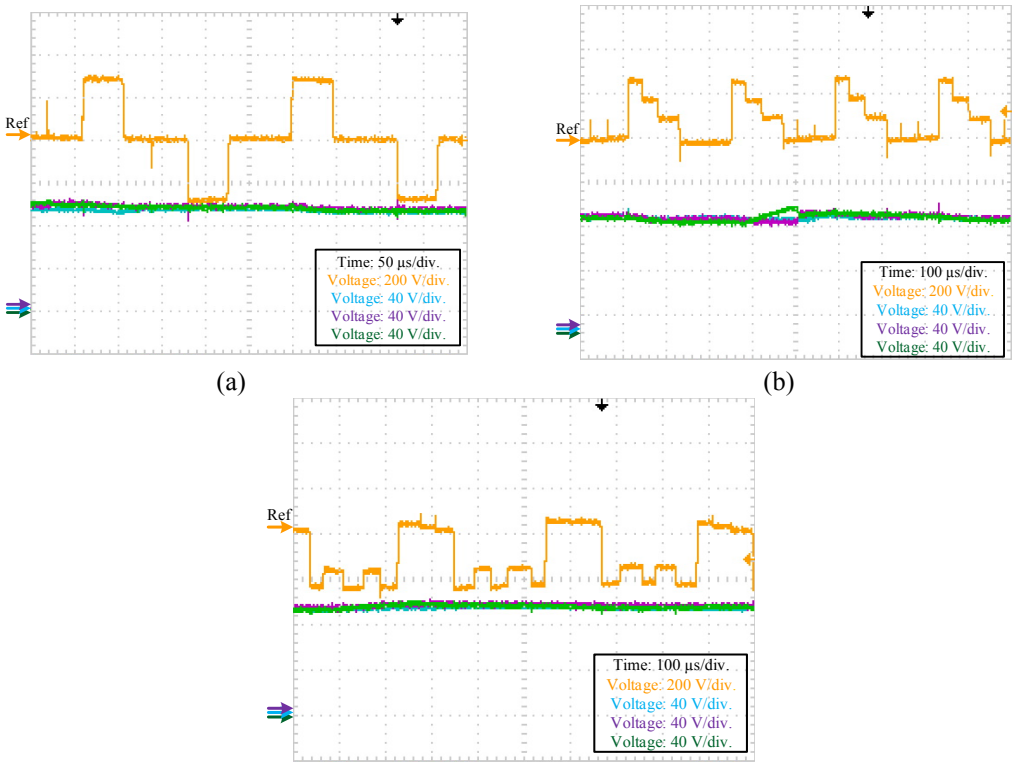


Fig.4.44. BPG experimental results for bipolar pulse waveforms and Arm2 capacitor voltages with $\lambda = 3$. (a) Bipolar rectangular. (b) Positive unipolar ramp. (c) Negative unipolar multipulse.

In order to investigate high gain voltage pulses with low voltage DC input, the input voltage is reduced to 30V with a boost factor $\lambda = 3$. Hence, each SM capacitor is charged to 90V as shown in Fig.4.44 and the pulse peak voltage is 270V. The generated bipolar rectangular pulses with $t_p = t_n = 50\mu s$ and $T_s = 250\mu s$ are in Fig.4.44a, along with Arm2 capacitor voltages.

Not only bipolar pulses can be generated with the BPG, but unipolar pulse generation is possible, by disabling (no arm insertion) the unwanted pulse polarity during pulse generation. This is illustrated in Fig.4.44b and Fig.4.44c for positive unipolar ramp pulses ($T_s = 240\mu s$) and a negative unipolar multipulse ($T_s = 320\mu s$), respectively.

4.4 Summary

In this chapter, a new family of hybrid PGs fed from an LV DC source was introduced. By replacing the capacitor charging resistor with an inductor, the SPG has more degrees of control freedom. Thus, the SM capacitors can charge fast with

controlled input charging current. Both HB and FB SMs can be used in the SPG. But utilising FB-SMs yields increased voltage stresses across the charging IGBT switches, therefore series device connection is inevitable.

The SPG topology can charge each SM capacitor in each arm to the input voltage level but not above. Thus the maximum voltage gain is controlled by the number of SMs. A modification in the SPG charging sequence is made in the BMPG. Specifically the inductor is energised, by proper control of the SMs main IGBTs, then its energy is released to charge the SM capacitor. Adjusting the ratio of the inductor energising time and the capacitor charging time controls the voltage boost ratio. Thus, the BMPG has the boost factor as an added control variable in addition to the number of the utilised SMs, to obtain high gain pulse voltages.

The SPG and the BMPG generate bipolar/unipolar rectangular pulse waveforms with a wide range of characteristics. But, extending their operation range to cover conventional PEF pulse waveforms necessitates SM voltage sensors to assure capacitors voltage balance. Thus, as in MMC PG based topologies, sorting the capacitor voltages is required either by voltage sensors or by a sensorless algorithm. By using a boost converter at the input, one voltage sensor at the boost converter level, and directing/blocking diodes, generation of all needed pulse waveforms is possible. Thus, a generic BPG is obtained while having the same voltage boost capabilities as the BMPG topology. The input boost converter can be replaced by a buck-boost converter, hence giving start up ramp charging of the SM capacitors.

Chapter 5

New HV-PGs Utilising the Transformer

An intuitive way for bipolar HV pulse generation is to utilise a step-up transformer, such that LV bipolar pulses are applied to the transformer LV side. In this configuration, transformer leakage inductance limits the range of the generated pulse durations. Alternatively, transformers can be used in a hybrid PG to provide isolation as well as additional voltage gain. In both transformer utilisation methods the voltage-second balance of each transformer side must be assured, otherwise the core saturates. This chapter explores three new PGs that utilise nano-crystalline core based transformers.

5.1 Transformer Utilisation in a Sequentially Charged SM Topology

To explore the viability of transformer utilisation, a transformer based PG with sequentially charged SMs (TSPG) formed of two parallel phase-legs is proposed (Fig.5.1). One leg is responsible for positive pulse generation while the other leg generates the negative pulse polarity. Each phase-leg contains two series arms, the upper arm is formed of series connected MMC HB-SMs, while the lower arm is formed of series-connected reverse blocking switches [82]-[83]. The SM capacitors are charged sequentially from the LV DC supply through a resistive-inductive (rL) branch such that the input charging current has a slightly underdamped response which allows rapid sequential charging of the SM capacitors. The sequentially-charged SM-capacitors are inserted simultaneously during pulse generation, hence the peak pulse voltage is $\pm NV_s$. The formed bipolar pulses are applied across the load through a step-up nano-crystalline core based transformer with n turns ratio. Accordingly, the generated pulses have a peak voltage of $\pm nNV_s$ as a result of the two-stage magnification. During pulse generation, the LV DC supply is isolated from the upper arm voltage $\pm NV_s$ by the lower arms being in an off state. Also the

charging efficiency can be improved if the rL charging circuit is replaced by an SMPS approach, as utilised in Chapter 4.

5.1.1 TSPG Topology Principle of Operation

The TPG topology is shown in Fig.5.1. The upper arms, Arm1 and Arm2, are formed of N series-connected MMC HB-SMs which are charged sequentially from the LV DC supply V_s through an rL branch via reverse blocking switch S_1 or S_2. During charging of a particular arm's SM capacitors, the other arm SMs are idled. The SM capacitors of the charging arm are charged sequentially by bypassing the other series SMs in the arm while inserting the SM capacitor to be charged. The operating sequence to generate the bipolar rectangular pulses shown in Fig.5.2, is outlined in Table 5.1. Pulse generation is formed of four stages, consecutively, the positive pulse, the positive SM capacitors charging, the negative pulse, and the negative SM capacitors charging. Although a positive pulse can be immediately followed by a negative pulse, followed by sequential recharging of SM capacitor in the two upper arms.

The formed voltage pulse V_t across the primary winding of the transformer is stepped up by transformer turns ratio n before being impressed across the load. Hence, the generated voltage pulse V_P is magnified by the N sequentially charged SMs and the transformer turns ratio n yielding a voltage pulse of peak $\pm nNV_s$ across the load.

Reverse blocking semi-conductor switches are required for S_1 and S_2 which can be an IGBT in series with diodes, as shown in Fig.5.1. This is because during pulse generation, S_1 and S_2 arms are OFF and a reverse voltage of $(N-1)V_s$ is applied across them. The IGBT switch rating is V_s, and since an LV DC input source is used, a single IGBT should be sufficient. Additionally, zero voltage switching (ZVS) is assured during IGBT turn ON/OFF, thus, series connection of IGBTs (if required) or the diode(s) should not present a sharing issue. The static reapplied dv/dt can be catered for by shunt resistors and capacitors.

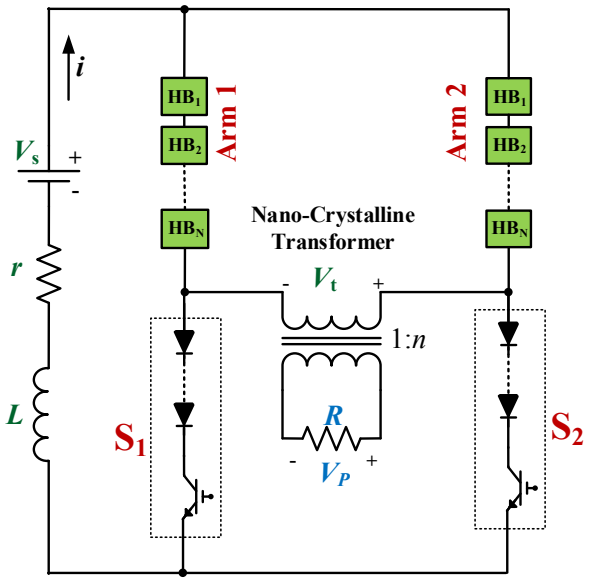


Fig.5.1. The TSPG converter topology.

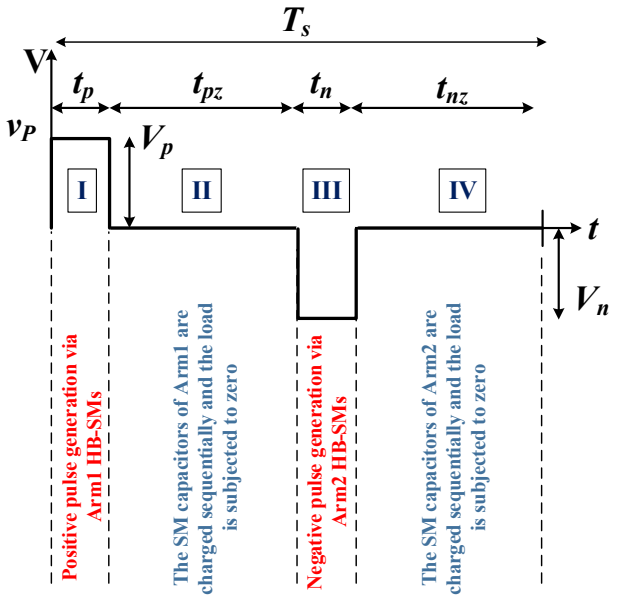


Fig.5.2. Generated bipolar rectangular voltage pulse across the transformer primary.

The properties of the nano-crystalline core material, which is selected in for TSPG topology and the subsequent transformer based topologies, can be summarised as follows:

- 1.2T saturation magnetic flux density (0.4T in ferrite cores, see Fig.5.3).
- High relative permeability (μ_r ranges between 20000 to 70000).

- Negligible magnetising current.
- Zero magnetostriction, hence, reduced noise level during operation.
- Good thermal stability (Curie point at 560°C).
- Low losses at higher frequencies.

Fig.5.3 compares the B-H characteristics of several magnetic materials. Generally, nano-crystalline is preferred (over ferrite) for high-frequency operation due to its high core permeability, hence high magnetizing inductance, high flux density, and near square hysteresis loop [81]. The reduced transformer volume, due to the high-frequency operation, enhances the modularity of the proposed topology.

Two aspects should be considered namely: transformer leakage inductance and core voltage-second balance. The transformer leakage inductance limits the generated duration of the pulses, thus, the leakage should be measured in order to determine the allowable pulse duration range.

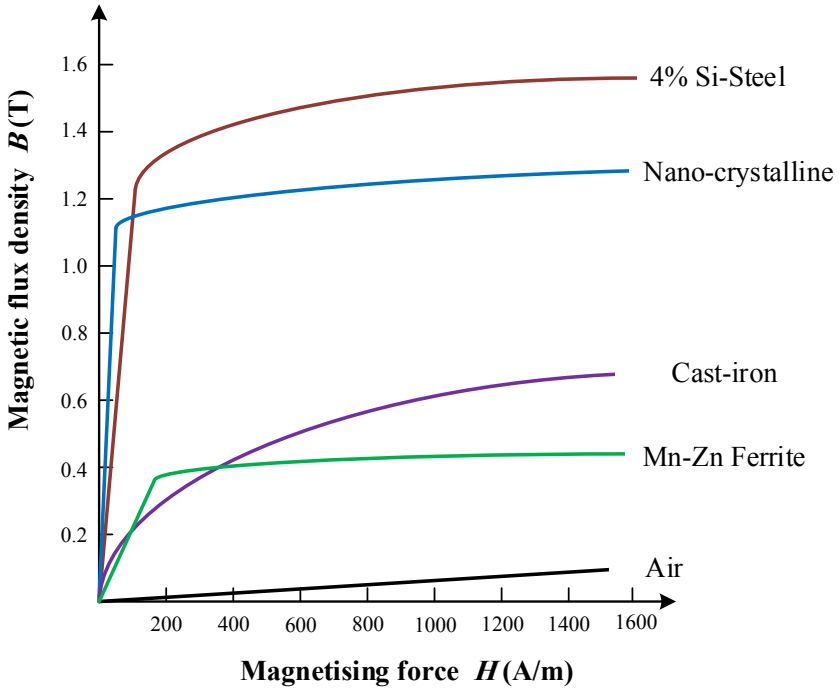
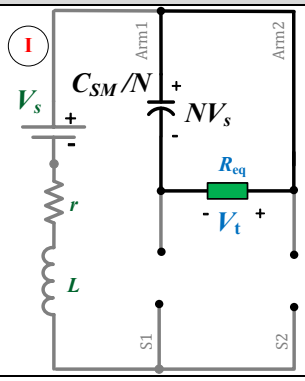
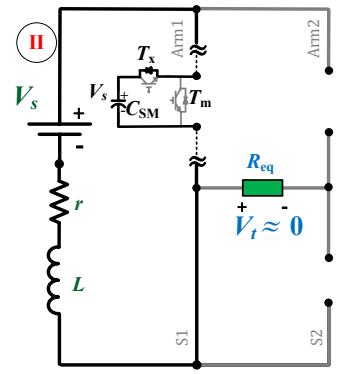
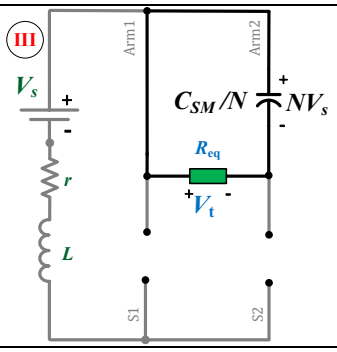
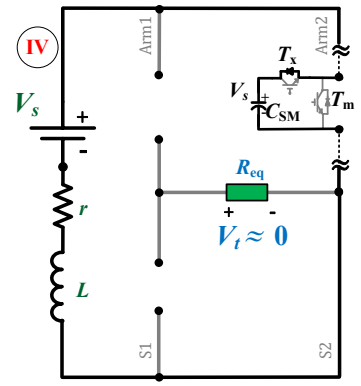


Fig.5.3. Magnetic materials B-H characteristics.

Table 5.1: Operating Principle of the TSPG

	Circuit configuration	Operation Sequence
Positive Pulse		• S_1 and S_2 switches are OFF. • Arm2 SMs are bypassed to provide a path for Arm1 discharging SM capacitors. • A positive pulse of voltage peak V_p is formed across the transformer primary for a duration of t_p.
Arm1 Capacitors Charging		• S_1 is ON (while charging SM capacitors of Arm1) and S_2 is OFF. • Arm1 SM capacitors are inserted sequentially to re-charge Arm1 SM capacitors, each to V_s. • All Arm2 SMs are idle. • To charge Arm1 SMs, the first charging SM is inserted, then S_1 is turned ON (hence, ZVS). • After charging the last SM, S_1 is turned OFF safely since the charging current is zero. • During Arm1 SMs charging duration t_{pz} the transformer primary voltage is nullified.
Negative Pulse		• S_1 and S_2 switches are OFF. • Arm1 SMs are bypassed to provide a path for Arm2 SM capacitors to discharge. • Negative pulse V_n is formed across the transformer primary for duration t_n.
Arm2 Capacitors Charging		• S_1 is OFF and S_2 is ON (while charging SM capacitors of Arm2). • Arm2 SM capacitors are inserted sequentially to re-charge the individual Arm2 SM capacitors to V_s. • All Arm1 SMs are idle. • To allow charging Arm2 SMs, the first charging SM is inserted, then S_2 is turned ON (hence, ZVS). • After charging the last SM, S_2 turns OFF safely since the charging current is zero. • During the Arm2 SMs charging duration t_{nz} the transformer primary voltage is nullified.

Voltage-second balance is assured for symmetrical bipolar pulses, however, asymmetrical pulses must maintain the voltage-second balance (otherwise, the transformer core will accumulate unidirectional flux and saturate). Thus, the following equation should be applied to determine the suitable pulse polarity magnitude and duration while assuring transformer voltage-second balance

$$V_p t_p = V_n t_n \tag{5.1}$$

where V_p and V_n are the peak of the positive and negative pulse polarities while t_p and t_n are the corresponding pulse polarity durations (assuming rectangular pulses as in Fig.5.2).

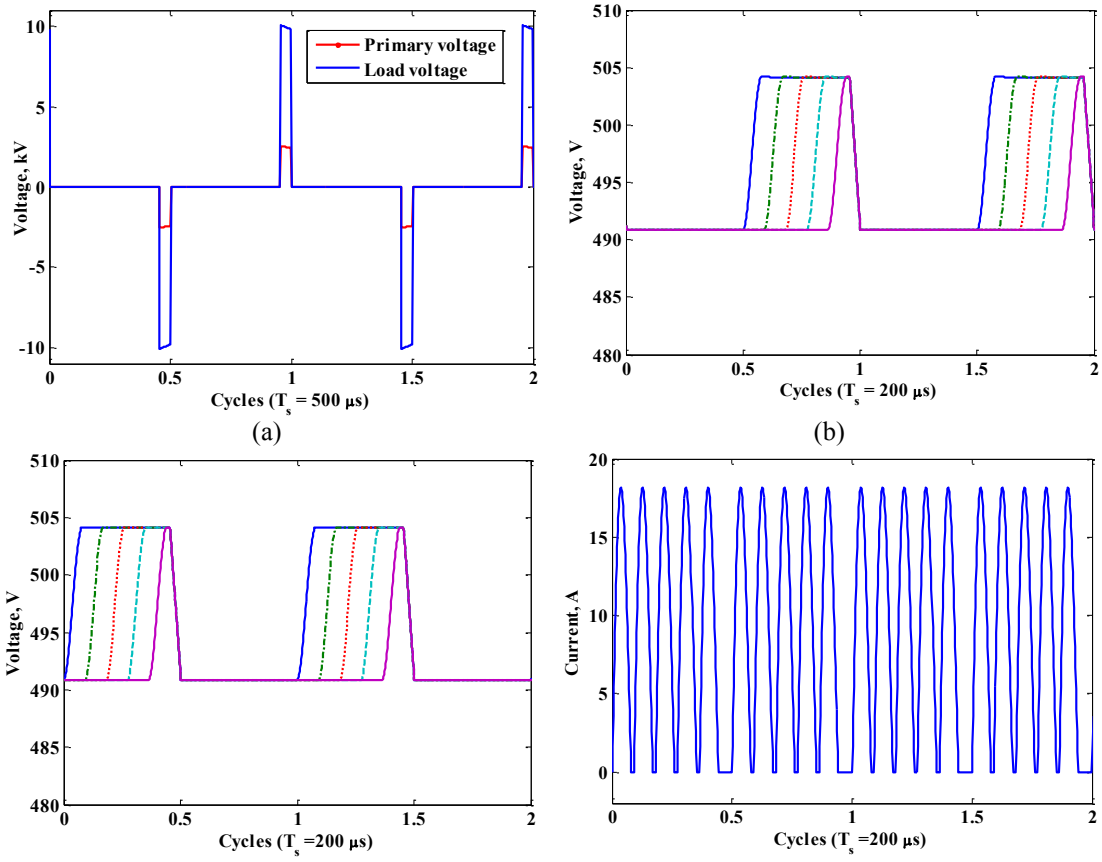


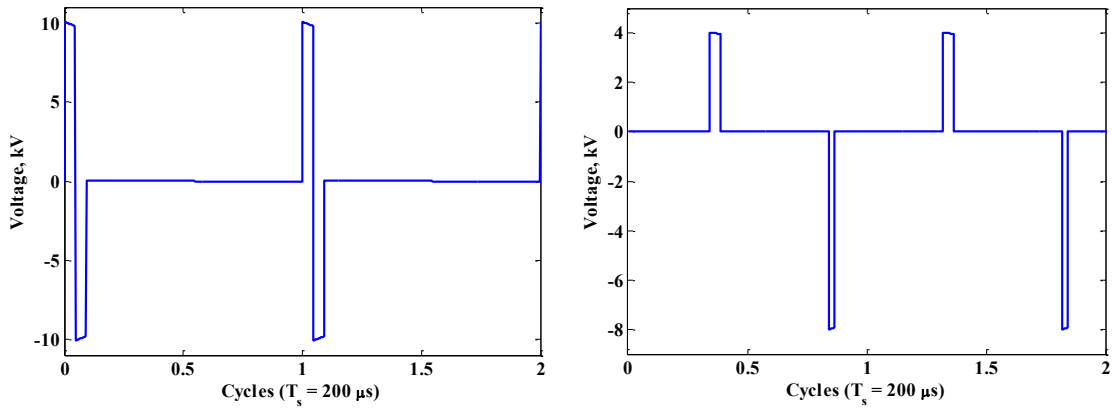
Fig.5.4. TSPG simulation results for generating 10 kV, 10µs bipolar rectangular pulses. (a) Voltage pulses across the transformer primary and the load. (b) Five SM capacitor voltages of the negative pulse, Arm1. (c) Five SM capacitor voltages of the positive pulse, Arm2. (d) Input charging current of the SM capacitors.

5.1.2 TSPG Simulation Results

Matlab/Simulink simulations are used to validate the TSPG topology, with 5 SMs, $n = 4$, $V_s = 500\text{V}$ and a resistive load of 1kΩ. Bipolar rectangular pulses with positive and negative durations of 10µs, voltage pulse peak of 10kV and repetition rate of 5kHz are shown in Fig.5.4a. In Fig.5.4a, the primary voltage of the transformer is 2.5kV, which is the sum of the sequentially charged five SM capacitors, while the voltage across the load is 10kV, since the transformer has $n = 4$. The capacitor voltages of Arm1 and Arm2 are shown in Fig.5.4b and Fig.5.4c, respectively, where each capacitor fluctuates around 500V, with a voltage ripple of less than 5%.

The current flows from the LV DC supply to charge the individual SM capacitors during the charging period as shown in Fig.5.4d. The current falls to zero after the SM capacitors re-charged to 500V with charging time of 14µs.

The flexibility of the TSPG is explored by generating asymmetrical bipolar pulses and combined NLV duration pulses as in Fig.5.5. Fig.5.5a shows asymmetric bipolar pulse with a positive polarity peak of 4 kV and 10µs duration, while the negative pulse polarity has an 8 kV peak and 5µs duration. Combined NLV duration pulses are explored in Fig.5.5b with 10µs pulse durations and 10kV peak voltage.



(a) (b)

Fig.5.5. TSPG simulation results, generation of different bipolar pulse shapes whilst ensuring the transformer voltage-second balance constraint. (a) Combined NLV duration bipolar pulses of 10µs pulse durations and 10 kV peak. (b) Asymmetric bipolar pulses of 10µs positive-pulse duration and 4 kV peak and 5µs negative-pulse duration with 8 kV peak.

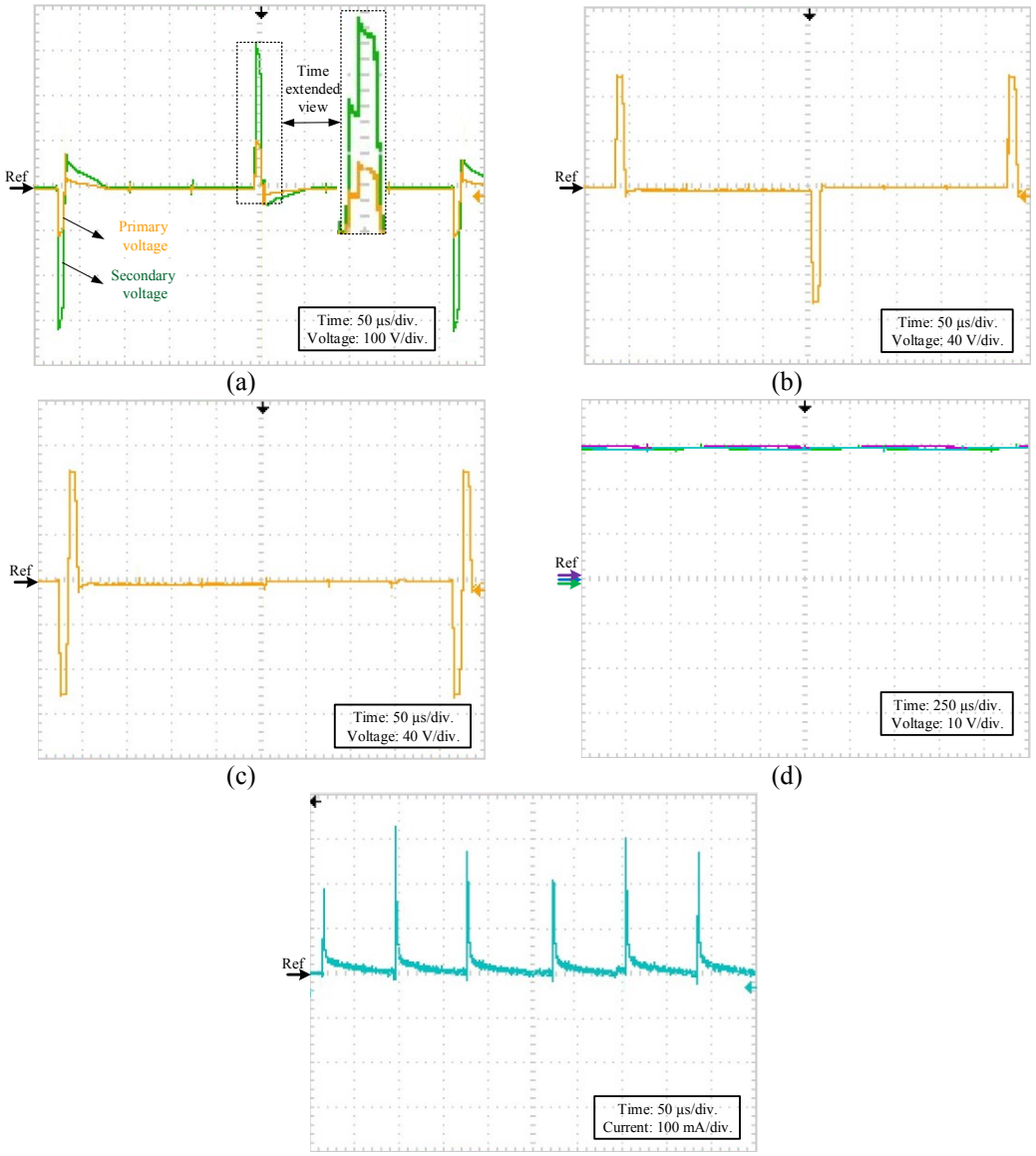


Fig.5.6. TSPG Experimental results. (a) Primary and secondary voltage pulses of non-combined NLV durations bipolar pulses. (b) Primary voltage pulses of non-combined NLV durations bipolar pulses. (c) Primary voltage pulses of combined NLV durations bipolar pulses. (d) Three individual SM capacitors voltage of Arm2. (e) Input charging current.

5.1.3 TSPG Proof of Concept Experimental Results

To test the TSPG converter, the introduced proof of concept experimental rig for the SPG converter (see Fig.4.12) is modified by adding a transformer of $n = 3$, the R load is 1kΩ, and the LV DC input is 30V. Although transformer leakage inductance is ignored in the simulations, its effect is seen in the experimental validation. To minimize transformer flux leakage, the primary is wound over the secondary windings. The experimentally-deduced (see Appendix C) secondary side leakage

inductance L_l, which is in series with the load, is 3.56µH. Therefore for 1kΩ load resistance, the generated pulse requires $\Delta t = L_l/R = 3.56$ns for each voltage polarity to reach its peak value. Thus, for proper operation, the pulse polarity duration time should be larger than Δt. Consequently, microsecond pulse durations can be generated, which is targeted in this thesis.

The primary and secondary voltages of 10µs bipolar pulses and 400µs repetition are shown in Fig.5.6a. The voltage-peak of the generated pulses across the load is 300V since the transformer turns ratio is 3 and the primary voltage is 100V, as in Fig.5.6a. The primary voltage of bipolar pulses with non-combined and combined NLV durations and a peak voltage of 90V are shown in Fig.5.6b and Fig.5.6c, respectively. All SM capacitor voltages in the two MMC arms fluctuate around 33V as shown for Arm2 SM-capacitors in Fig.5.6d. The charging input current is shown in Fig.5.6e for the pulses in Fig.5.6a.

5.2 Transformer Utilisation for Isolated DC Input Sources PG

The topology in this section uses transformers to provide isolated DC sources. The isolated DC input sources PG (IPG) topology is formed of multiple cascading of four series conversion stages as shown in Fig.5.7. The first stage is a relatively low voltage DC input and with conversion stages generates isolated HV pulses across the load. The IPG utilises modular multilevel FB-SMs, thus can generate bipolar voltage pulses. Alternatively, if so an application need, HB-SMs produce unipolar pulses, but with half the number of SM IGBTs. With both SM types, each SM capacitor is charged independently from individually connected circuitry across each SM capacitor. Thus, along with modularity and scalability, the proposed topology alleviates the need of SM capacitor voltage measurement and balancing, as each SM capacitor is constantly charged by its own voltage source circuit. Not only rectangular pulses are possible with the proposed topology, but multilevel pulses with reduced dv/dt are also possible. The utilised FB-SM capacitance is small compared with the capacitances in HVDC transmission applications, which reduces the topology footprint and volume [84].

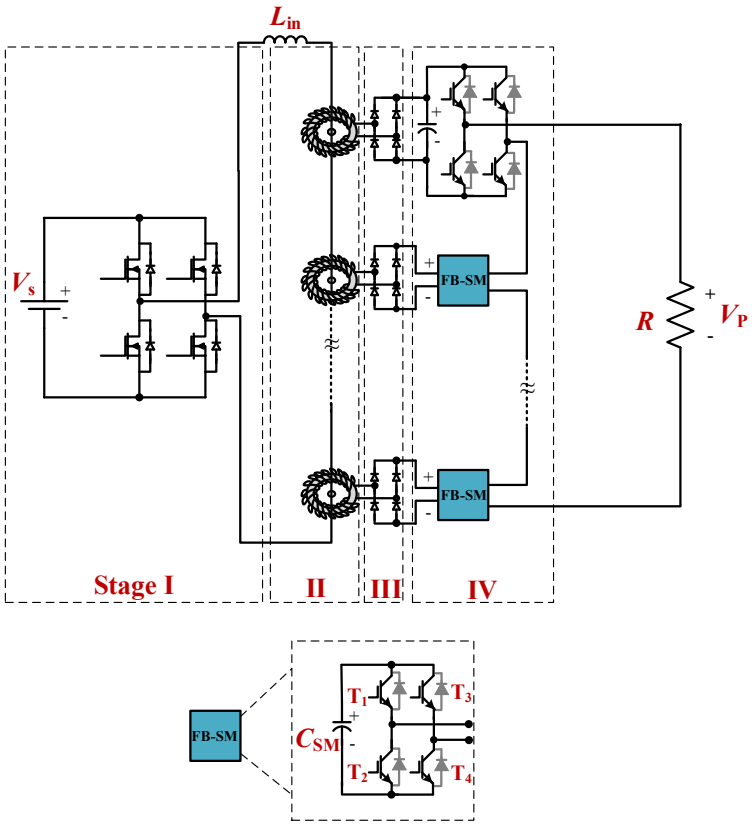


Fig.5.7. The IPG converter topology and its four successive conversion stages, for HV pulse generation.

5.2.1 IPG Converter Topology

The IPG converter topology and the four successive stages for HV pulse generation across a load R, are illustrated in Fig.5.7. Stage-I, the H-bridge inverter, is responsible for converting the LV DC input V_s into a high-frequency square AC voltage of $2V_s$ peak to peak. In Fig.5.7, stage-II is formed of N nano-crystalline core based high-frequency step-up transformers, all with a turns ratio $1:n$. The reduced transformer volume, due to high-frequency operation, enhances topology modularity. The primary of each transformer is a single-turn that is located in the axial centre of each transformer core. A single central turn realizes the necessary HV isolation, creepage and clearance. The peak of the applied high-frequency square AC voltage from stage-I, at the primary of each transformer is V_s/N, while the secondary voltage peak is nV_s/N where N is the number of transformer cores (hence FB-SMs) and n is the number of secondary turns.

The inductor L_{in} in stage-II has a small inductance, typically in the µH range, to limit the input current (thus creating a current source). With a large number of transformers, the total leakage inductance may be sufficient to alleviate the need of L_{in} at the input. In stage-III, the high-frequency square AC voltage of each transformer secondary is rectified through a diode full-bridge rectifier, resulting in a DC voltage of

$$V_{SM} = nV_s/N \tag{5.2}$$

The final stage, stage-IV, consists of the N series connected FB-SMs across the load (usually the treatment chamber). With each FB-SM capacitor C_{SM} directly fed from the output of stage-III, the pulse peak voltage is approximately

$$V_P = nV_s \tag{5.3}$$

The use of FB-SMs allows the generation of both positive and negative output voltage polarities. The anti-parallel diodes across each IGBT switch in the FB-SMs can be omitted because they are not utilised to re-charge the FB-SM capacitors as in HVDC transmission applications. Here each of the N FB-SM capacitors is independently charged by one of the N external isolated DC sources (stage-III in Fig.5.7).

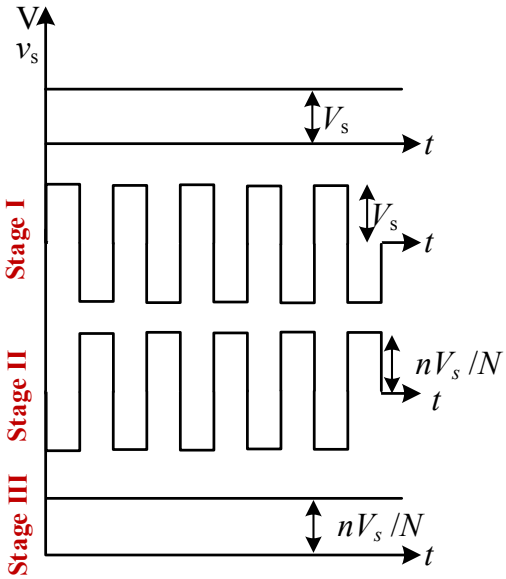


Fig.5.8. Voltage variation through different stages of the IPG topology.

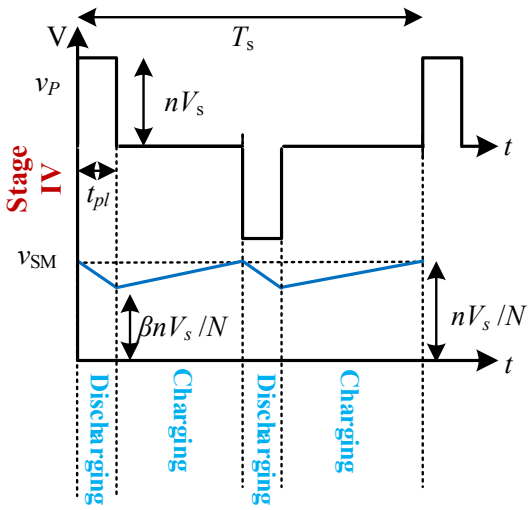


Fig.5.9. IPG Generated rectangular bipolar pulses.

5.2.2 IPG Topology Principle of Operation

The voltage waveforms of the first three stages are illustrated in Fig.5.8. Starting from an LV DC input, V_s, each FB-SM capacitor is charged simultaneously and independently, to a DC voltage of nV_s/N. The FB-SM capacitors are the energy pool that provides the required HV pulse energy (or stage-IV), where, with the aid of the FB-SM voltage clamping configuration, it is possible to connect the charged capacitors in series to create pulses with a peak voltage of $\pm nV_s$, if all the FB-SMs are inserted.

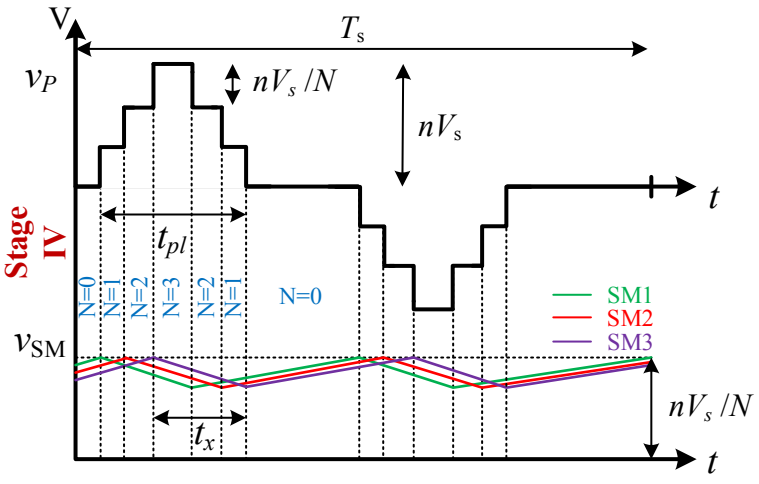


Fig.5.10. IPG Generated multilevel pulses.

Fig.5.9 illustrates the generation of a symmetrical bipolar rectangular pulse-waveform with a repetition time of T_s. At $t = 0$, all the FB-SM capacitors are inserted to form the positive polarity voltage pulse, (by turning on T_1 and T_4 of each FB-SM) for the desired pulse time t_{pl}, thus a peak voltage of $+nV_s$ is impressed across the load. Then the FB-SMs are bypassed, by turning on T_1 and T_3 (or T_2 and T_4) of each FB-SM, for $(½T_s - t_{pl})$ which nulls (zeros) the voltage across the load. The FB-SM capacitors are inserted simultaneously to form the negative polarity voltage pulse, (by turning on T_2 and T_3 of each FB-SM) for the desired pulse time t_{pl}. Then again the SMs are bypassed, by turning on T_1 and T_3 (or T_2 and T_4) of each FB-SM, for the remainder of T_s. During pulse generation, the FB-SM capacitor voltage V_{SM} decreases, as a result of transferring some stored energy to the load. The remaining voltage V_o on each FB-SM capacitor is

$$V_o = \beta n V_s / N \tag{5.4}$$

where β is the percent remaining voltage after pulse generation. After pulse generation, the individual FB-SM capacitors are recharged to their pre-discharging value $V_{SM} = nV_s/N$ through stage-III (although the charging process occurs continuously, even during the pulse).

As the pulse voltage magnitude increases, it is desirable to reduce the PG dv/dt to reduce EMI levels. Generating multilevel pulse waveforms is not possible without assuring balance of the individual SM-capacitor voltages. Generally this can be achieved only by employing sensorless or sensor based techniques. Balancing is possible with the IPG converter without the necessity of sensors or complicated algorithms for sorting the FB-SM capacitor voltages as in HVDC transmission applications. The fact that each FB-SM voltage is restored to its pre-discharging voltage-level immediately after contributing to pulse generation, makes it possible to generate multilevel pulse waveforms, using the first-in first-out (FIFO) principle.

The FB-SM with the lowest capacitor voltage is charged first as the low voltage H-bridge is forced to operate in a current source mode (current limit mode). This is because the current source effectively sees all the SM capacitors in parallel. So energy is always transferred to the capacitor (or all capacitors at initial charging) with the lowest voltage, thus provide auto-voltage regulation. Progressively all the FB-SM capacitors are simultaneously charged in a current limiting mode until each

capacitor voltage reaches nV_s/N that is V_{SM}, when the H-bridge operates in a voltage source mode, with zero current in the primary (and secondary) and V_s/N across each single turn primary. Thus, when a FB-SM is taken out of pulse generation (bypassed) it is automatically charged to the pre-discharge voltage level while waiting for the next pulse generation. In fact the SM charging process is continuous and occurs during pulse generation.

Fig.5.10 illustrates the principle of generating four-level pulses with $N = 3$, rising to the pulse-peak voltage, and its decrease. During voltage increase (at the zero voltage-level $N = 0$), for the first level ($N = 1$) only one FB-SM is inserted, SM1, then for the second level ($N = 2$) SM2 is inserted, adding to SM1, and finally SM3 is inserted, meaning all three SMs source the load, forming the pulse-peak voltage. The transition to zero voltage is controlled by bypassing the first inserted FB-SMs first, based on the FIFO concept as illustrated in Fig.5.10.

5.2.3 IPG Topology FB-SM Capacitance Sizing

In Fig.5.9 and Fig.5.10, after the FB-SM capacitor voltage drops due to transferring some of its stored energy to the load, it is charged to the pre-discharged voltage via the charging circuit in previous stages I, II and III. Thus, if a bipolar rectangular pulse of time t_{pl} is considered (as in Fig.5.9), the energy transferred to the load per pulse polarity, with a small voltage drop, can be expressed as

$$½C_{SM}(V_{SM}^2 - V_o^2)N \approx \frac{V_P^2}{R} t_{pl} \tag{5.5}$$

where V_P is the peak of the of the rectangular pulse across the resistive load R. By neglecting semiconductor voltage drops, from (5.2), (5.3) and (5.4), equation (5.5) yields

$$½C_{SM} \frac{n^2 V_s^2}{N}(1 - \beta^2) = \frac{n^2 V_s^2}{R} t_{pl} \tag{5.6}$$

Re-arranging (5.6), the FB-SM capacitance can be estimated as

$$C_{SM} = \frac{2N t_{pl}}{(1 - \beta^2)R} \alpha \tag{5.7}$$

where $\alpha \geq 1$ is a factor to account for neglected semiconductor voltage drops and circuit parasitic resistances.

Although the estimated value in (5.7) is based on a symmetrical rectangular pulse waveform, it can be used for asymmetrical rectangular pulse waveforms by using the widest pulse polarity as t_{pl}. Additionally, it can be used for the multilevel pulse waveform in Fig.5.10. At the individual FB-SM level, t_{pl} is substituted by t_x where t_x is the total insertion time for each individual FB-SM capacitor based on the discussed FIFO principle of insertion.

5.2.4 IPG Simulation Results

The IPG topology is Matlab/Simulink simulated with the specifications given in Table 5.2. The voltage variation through different stages of the IPG topology is explored in Fig.5.11 while generating symmetrical bipolar pulses of 10µs pulse duration and 5kV pulse peak at a 120µs repetition rate. As explained in Fig.5.8, the LV DC input, shown in Fig.5.11a, is converted by the input inverter to an AC square waveform with repetition time $T_Q = 100\mu s$ in stage-I as shown in Fig.5.11b. In stage-II, the AC voltage created by stage-I is stepped up by the utilised transformer as shown in Fig.5.11c. Fig.5.11d shows the rectified voltage after stage-III feeding the FB-SM capacitor. The generated bipolar rectangular pulses are depicted in Fig.5.11e while the five SM capacitor voltages are shown in Fig.5.11f.

The concept of isolated DC sources feeding the FB-SM capacitors allows different electroporation pulse waveforms generation, as illustrated in Fig.5.12. In Fig.5.12a asymmetrical bipolar rectangular pulses are generated with $T_s = 130\mu s$, positive polarity peak of 3kV and 20µs duration, while the negative pulse polarity has a 5kV peak and 10µs duration.

Table 5.2: Simulation and Experimentation Specifications of the IPG

Parameter		Simulation	Experimental
LV DC input voltage	V_s	100 V	25 V
Number of FB-SMs	N	5	5
Load resistance	R	1 kΩ	500 Ω
Input inductance	L_{in}	2 µH	10 µH
SM capacitance	C_{SM}	5 µF	10 µF
Stage-I inverter frequency	f_Q	10 kHz	16 kHz
Transformers secondary turns	n	10	5
Percent remaining voltage	β	0.98	

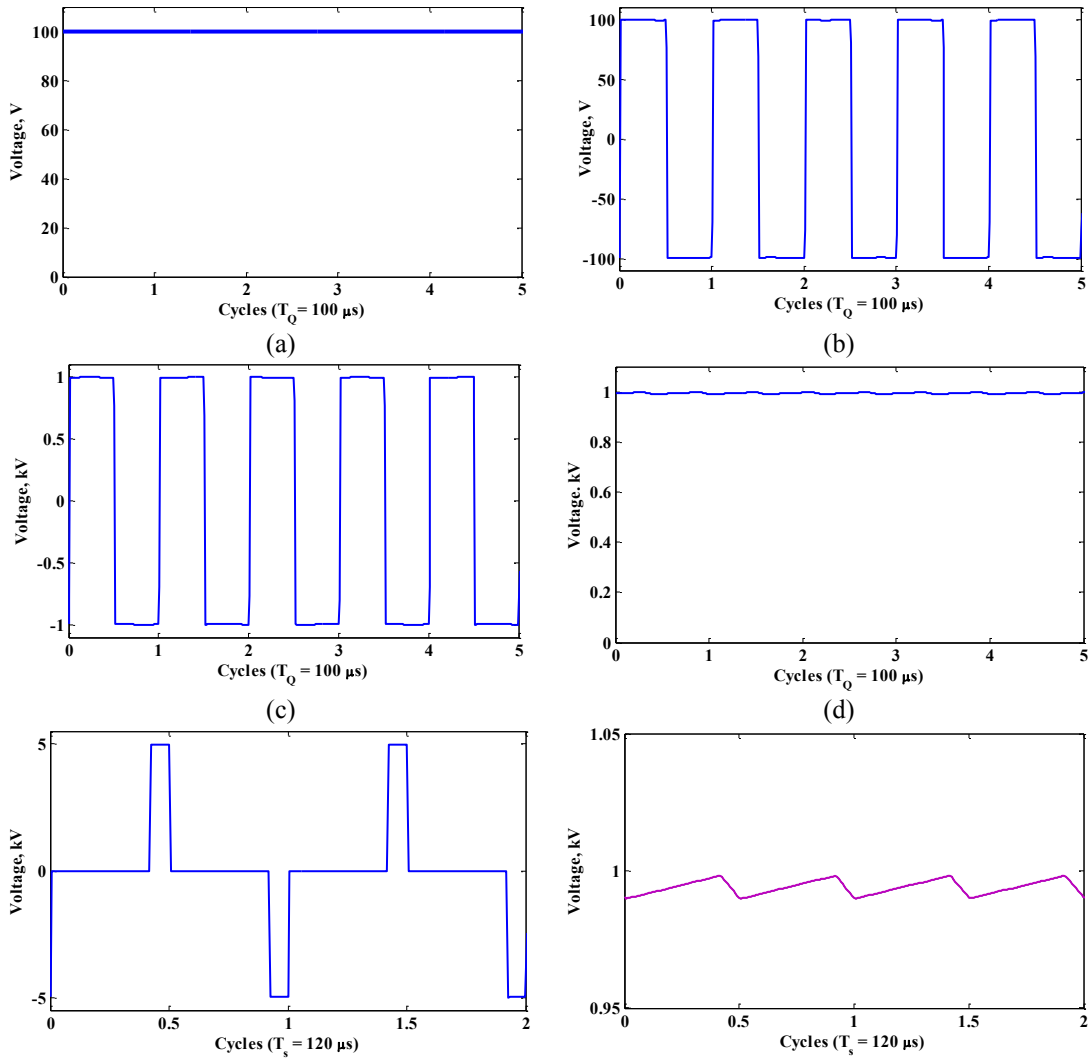


Fig.5.11. IPG Simulation results for symmetrical rectangular pulse.
(a) Input LV DC supply voltage. (b) Stage-I voltage.(c) Stage-II voltage. (d) Stage-III voltage.
(e) Generated pulses.(f) SM capacitor voltages.

During the positive polarity, two SM are bypassed while the five SMs are inserted during the negative pulse duration. Fig.5.12b shows bipolar multilevel pulses with $T_s = 100\mu s$ and pulse duration of 20µs. The multipulse waveform pulses are shown in Fig.5.12c with $T_s = 100\mu s$ and pulse duration of 25µs when one SM is bypassed every 5µs of each pulse polarity generation. Fig.5.12d shows the generation of bipolar ramp pulses with $T_s = 100\mu s$ and pulse duration of 20µs.

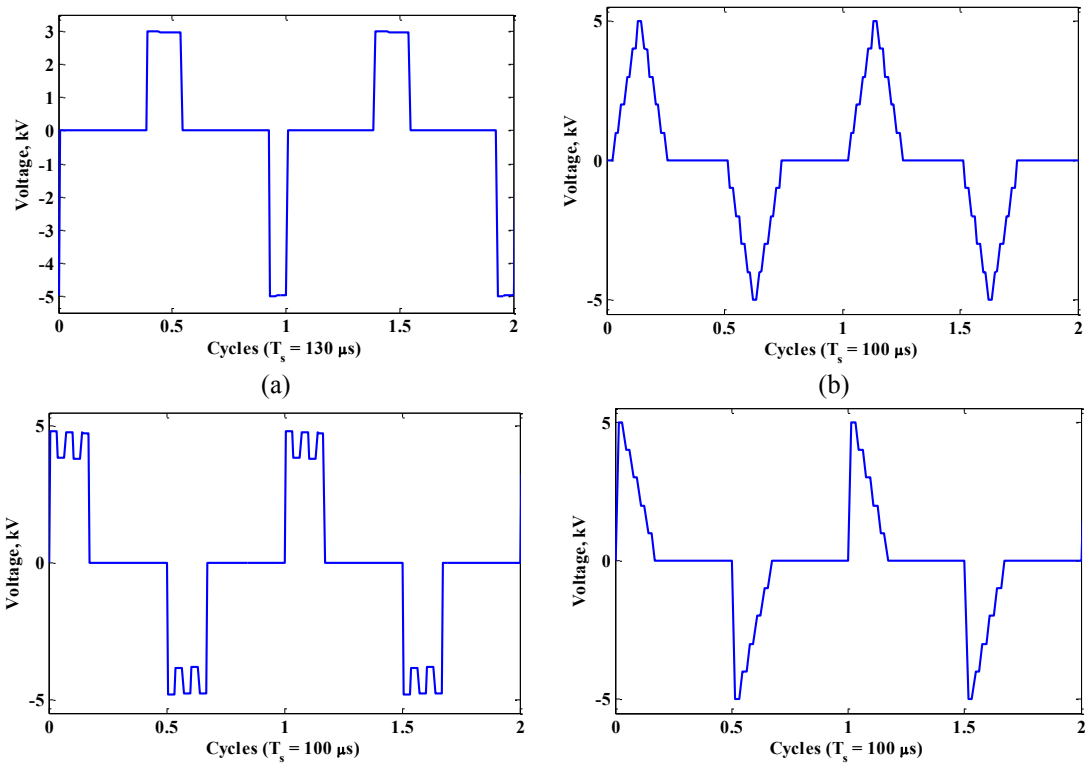


Fig.5.12. IPG Simulation results for different bipolar pulse waveforms.
(a) Asymmetrical rectangular. (b) Multilevel. (c) Multipulse. (d) Ramp.

5.2.5 IPG Proof of Concept Experimental Results

The scaled down experimental set-up used to validate operation and the flexibility of the proposed pulse generator consists of five FB-SMs. The experimental parameters are given in Table 5.2, while Fig.5.13 shows rig details. Stage-I, the H-bridge inverter is shown in Fig.5.13a, a module combining stages II, III and IV is depicted in Fig.5.13b, the five SM are shown in Fig.5.13c and the complete set-up is shown in Fig.5.13d.

With five FB-SMs, the IPG is able to generate a multilevel bipolar pulse waveform of up to six voltage-levels ($N + 1$) in each polarity. A six level bipolar voltage-pulse is shown in Fig.5.14a, where the FB-SM DC voltage is 100V (nV_s/N =100V) for the five FB-SMs successively inserted at 5µs intervals. The 500V peak is for 20µs, when all the FB-SMs are inserted. With the reverse FB-SM sequencing process on the trailing edge, a pulse t_{pl} = 60µs of 500V peak is impressed across the load.

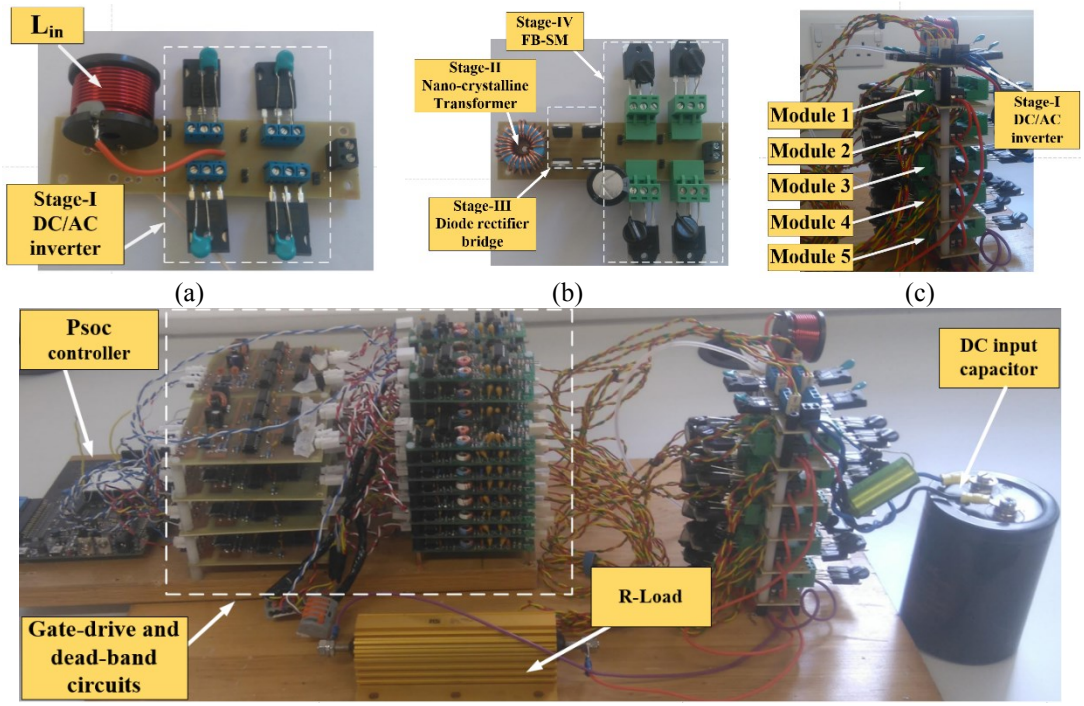


Fig.5.13. IPG proof of concept experimental rig. (a) Stage-I H-Bridge inverter. (b) Modules of stages-II III and IV. (c) Five modules. (d) Experimental test rig.

The voltages of three FB-SM capacitors are shown in Fig.5.14b. The capacitor voltages balance around 100V, and immediately after contributing to pulse-polarity generation, all started to re-charge. The 100V charging level for the FB-SM capacitor is obtained by rectifying the stage-II square AC voltage of each FB-SM. Since the DC voltage input is 25V, the output square AC voltage from stage-I inverter has a peak-voltage of 25V, as shown in Fig.5.15, which also shows the typical primary current of the stage-II transformers.

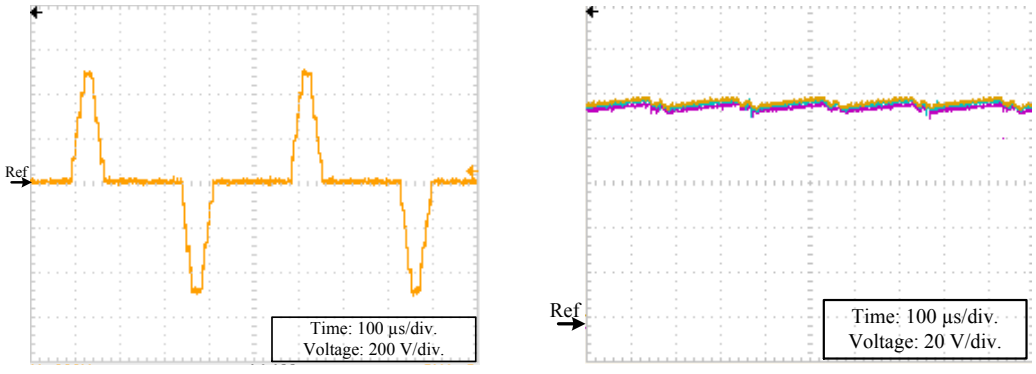


Fig.5.14. IPG Experimental results for the multilevel pulse.
(a) 500V pulse-peak. (b) Three FB-SM capacitor voltages.

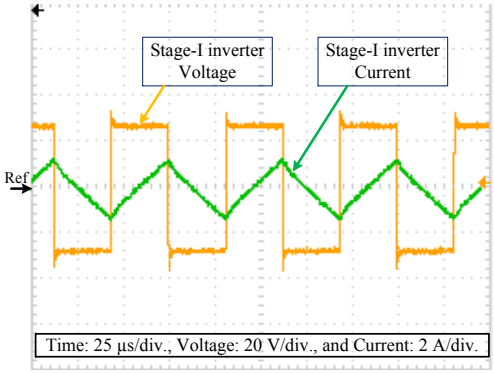
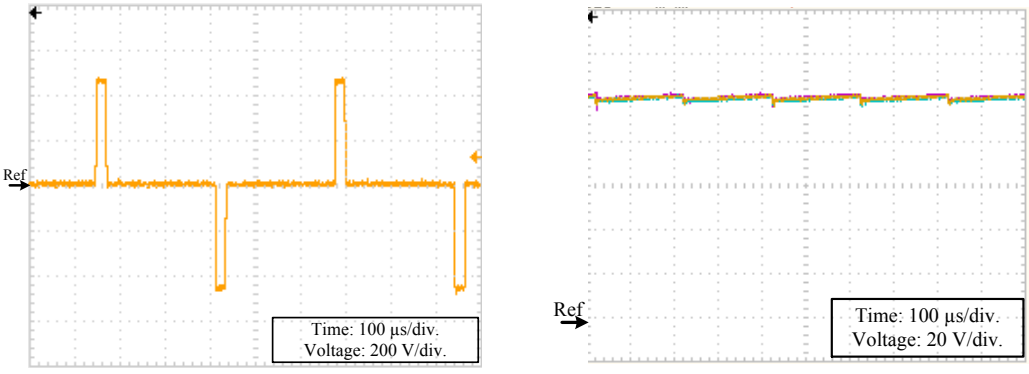


Fig.5.15. IPG Experimental results for the stage-I inverter voltage and current waveforms.



(a) (b)

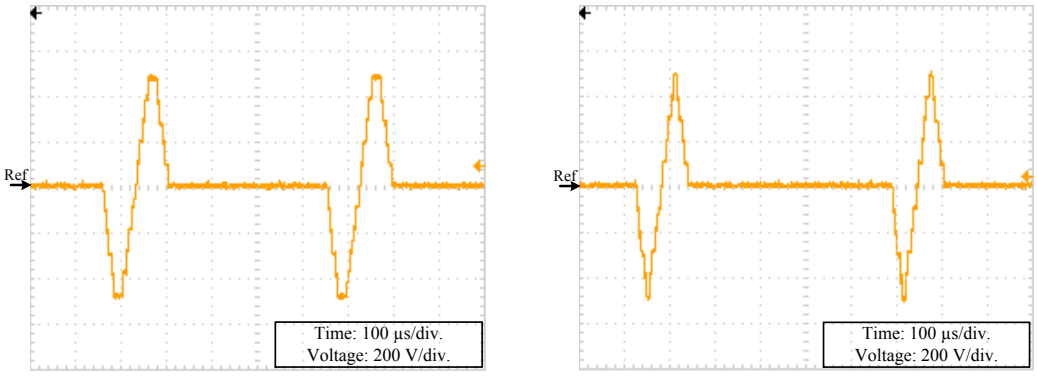
Fig.5.16. IPG Experimental results for the rectangular pulse.
(a) 500V pulse-peak. (b) Three FB-SM capacitor voltages.

By inserting the five FB-SM capacitors simultaneously in series, a rectangular pulse waveform of 20µs is generated from the proposed PG as shown in Fig.5.16a, while the capacitor voltages of three FB-SMs are shown in Fig.5.16b.

The flexibility of inserting and bypassing the FB-SM capacitors without affecting their voltage balance allows generating pulses of combined null load voltage durations. Fig.5.17a and Fig.5.17b show two six-level voltage pulses, where the null load voltage durations between the negative and positive pulse polarities are combined, when the FB-SM capacitors are inserted at the pulse-peak for 20µs and 5µs, respectively.

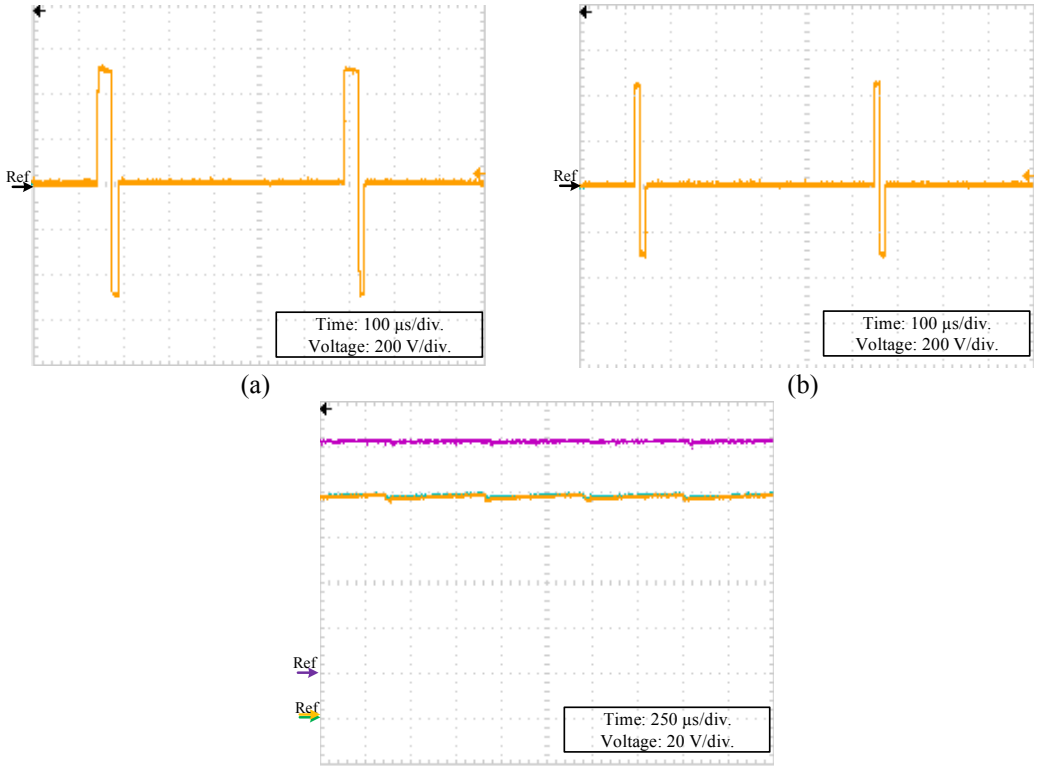
Combined null load voltage durations in the case of rectangular pulses with different positive and negative durations (30µs and 10µs respectively) are shown in Fig.5.18a. Not only different positive and negative pulse durations can be generated by the IPG, but different magnitudes (+500V and -300V) are possible, as shown in Fig.5.18b. In Fig.5.18b, two FB-SMs are bypassed during negative pulse polarity

generation, hence, the peak of the positive-pulse polarity is 500V and the negative-pulse peak is 300V, both of 10µs duration. Fig.5.18c shows the voltages of three FB-SM capacitors, where one is bypassed. In Fig.5.18c, the bypassed FB-SM capacitor voltage is near 100V (as it only contributes to positive pulse generation for 10µs), while the other two capacitors contribute to generating both pulse polarities.



(a) (b)

Fig.5.17. IPG Experimental results for combined NLV multilevel ±500V pulses. (a) With 20µs pulse peak duration. (b) With a 5µs pulse peak duration.

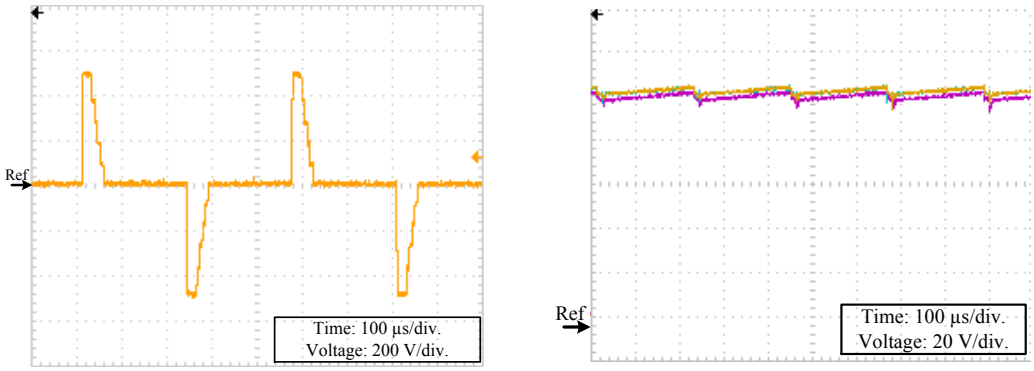


(a) (b)

(c)

Fig.5.18. IPG Experimental results for the combined null-load voltage rectangular voltage pulses. (a) Positive and negative pulse durations of 30µs and 10µs, respectively. (b) Positive and negative pulse peak voltage of +500V and -300V, respectively. (c) Three FB-SM capacitor voltages.

Finally, by inserting all the FB-SM capacitors simultaneously on the rising edge then bypassing them sequentially on the falling edge, the IPG is able to create ramp pulse waveforms (which mimic conventional exponential pulse waveforms). The generated trailing edge ramp pulse waveform is shown in Fig.5.19a and the capacitor voltages of three FB-SM capacitors are shown in Fig.5.19b.



(a) (b)

Fig.5.19. IPG Experimental results for the ramp trailing edge pulse.
(a) 500V pulse. (b) Three FB-SM capacitor voltages.

5.2.6 IPG Topology Aspects and Limitations

The following are the aspects and limitations for the IPG topology for scalability purposes.

A. Transformer Series Primary Isolation Technique Aspects

A key aspect of the IPG, hence an attribute, is that each FB-SM is powered via a separate transformer, but with a single coupled primary source. By using a single primary turn (a common conductor passing through the core longitudinal axis as shown in Fig.5.8), HV properties of isolation and low inter-winding capacitance are obtained.

For scaling to high power, the H-bridge DC to square wave AC generator should operate in two modes. The first mode is a current control mode, $V_{SM} < nV_s/N$, by utilising inductor L_{in} (and its current as feedback) in Fig.5.8 and transformer leakage, and the second mode is as a voltage controller, $V_{SM} = nV_s/N$, by decreasing the switching frequency or bypassing L_{in}.

The current control mode (where the transformer secondary appears to be short-circuited), is used to initially charge the system capacitors from 0V to nV_s/N. The current control mode is key to maintaining FB-SM capacitor voltage balance. In a current control mode, the transformer acts like a current transformer, where $\Sigma ni = 0$ and $V_{SM} < nV_s/N$ conditions dominate. This means all the primary energy is transferred to the FB-SM with the lowest capacitor voltage, since all the capacitors appear to be in parallel to the current source. Thus progressively all the FB-SM capacitors charge to a level where voltage transformer conditions dominate, that is $V_{SM} = nV_s/N$ control ensures all capacitors have the same voltage, but a FB-SM with a voltage higher than nV_s/N receives no charge. Capacitor voltage balance is assured because the lowest voltage FB-SM capacitor(s) will always charge to nV_s/N, while a capacitor voltage(s) $V_{SM} > nV_s/N$ will not increase because the secondary output appears as an open circuit condition.

At modest power levels, a compromise on the magnitude of L_{in} can avoid the need for two mode control of the H-bridge. Specifically inductance large enough to limit peak currents (particularly at system FB-SM capacitor initial charge up), but small enough to minimize the loss at the maximum output voltage (since it adds to transformer leakage inductance), at a given frequency.

B. Factors affecting FB-SM Capacitance Sizing

Basically, HV pulse specification is determined by the application and load requirements. The factors are mainly pulse peak voltage V_P, repetition time T_s, and pulse duration time t_{pl}. Based on these and the load resistance R, the FB-SM capacitance can be estimated from (5.7). However, two factors will affect capacitance, namely:

- The capacitor voltage drop after contributing to the generated pulse and
- The neglected semiconductor voltage drops and circuit parasitic resistances.

These two factors are considered in (5.7) by introducing two variables β and α. β is the per unit remaining capacitor voltage after contributing to the pulse. The voltage across the capacitor will be restored to $V_{SM} = nV_s/N$ after contributing to the pulse (peak voltage nV_s), then this cycle will be continued every T_s. This voltage fluctuation is capacitor voltage ripple. A common practice allows a voltage ripple of

up to 0.1 pu. Consequently, the minimum remaining voltage is 0.9 pu. Thus, the suggested values of β will range from 0.9 pu to 1 pu.

With the selected β, the equivalent capacitance will control the voltage drop. However, the neglected voltage drops and parasitic resistance may affect the designed capacitor voltage drop adversely if not compensated. Accordingly, since all the parameters in (5.7) are fixed, the safety factor α is used to increase the FB-SM capacitance if the drop level is not satisfactory. Initially, the safety factor is set to $\alpha = 1$, the drop value is tested, if not satisfactory, α is increased.

C. Pulse Generation Limitations

The ability of the IPG to generate the required pulse waveforms at high repetition rates depends on the following factors:

- The speed of the selected controller in executing the control software instructions, such that the total software execution time is less than the required pulse repetition time and
- The turn ON/OFF delay times (and mismatch) of the power semi-conductor switches and their gate drives.

Rectangular, as well as ramp pulses, may require accurate turning ON/OFF timing of the semi-conductor switches. Timing deviation may be evident in the practical generation of pulses. A solution is to pre-compensate the gate signal timing by software control such that actual switching OFF/ON timings are matched.

Increasing or decreasing the number of the MMC FB-SMs has no effect on the DC input supply (other than its current rating). Increasing the FB-SM number provides flexibility of pulse waveform generation by creating N levels, and will provide redundant FB-SMs in the case of failure and will allow reducing the voltage rating of the semi-conductor switches. In contrast, the minimum number of FB-SMs is ultimately dependent on the desired HV DC level and the voltage rating of the semi-conductor switches and their turn ON/OFF speeds.

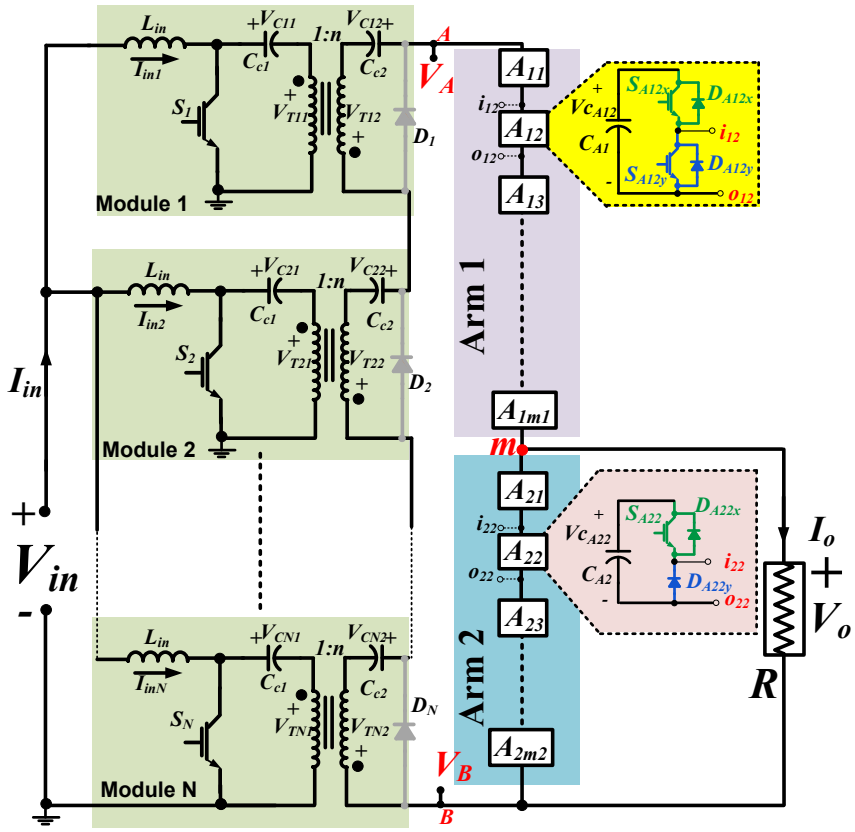


Fig.5.20. The SUPG converter topology.

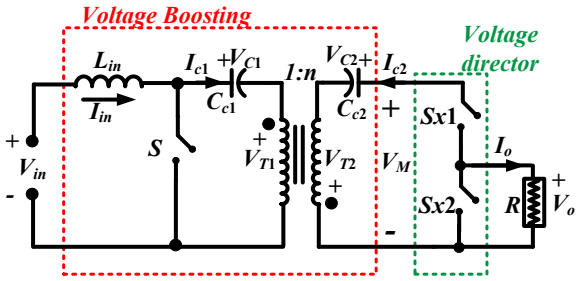


Fig.5.21. The basic VBM.

5.3 Isolated Input-Parallel/Output-Series Voltage Boosting Modules based PG

A unipolar step-up PG (SUPG) fed from an LV DC supply is proposed based on isolated input-parallel/output-series (IPOS) voltage-boosting modules (VBMs) and MMC-SMs, as shown in Fig.5.20. The VBMs, shown in Fig.5.21, are isolated via nano-crystalline core based transformers which have high magnetising inductance and are suitable for high-frequency operation [81]. HV step-up is obtained from three mechanisms: the number of utilised VBMs, the voltage conversion ratio of the individual VBM, and the turns ratios of the step-up isolation transformers. The

generated HV DC from connecting the output of the individual VBMs in series is chopped by employing two arms of series connected MMC-SMs across the load, hence, the SM-capacitors actively clamp the voltage across the semi-conductor switches [85]-[86]. High repetition pulse rates are possible, independent of the employed number of VBMs or MMC-SMs.

5.3.1 Basic Voltage Boosting Module of the SUPG

The basic VBM of the proposed SUPG is shown in Fig.5.21. Unlike conventional DC-DC converters [87], the secondary side switches S_{x1} and S_{x2} are not necessarily operating in a complementary manner. The switching pattern for the VBM devices and the developed circuit configurations are illustrated in Fig.5.22a. The VBM operation is explained as follows:

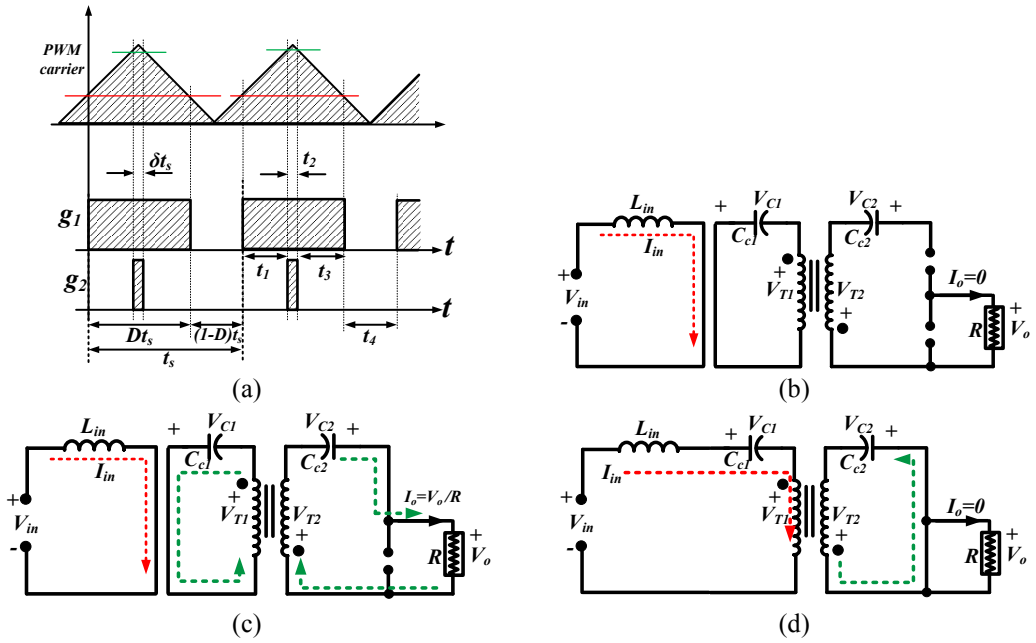


Fig.5.22. Normal VBM operation. (a) Operational states. (b) Circuit configurations during t_1 and t_3. (c) Circuit configurations during t_2. (d) Circuit configurations during t_4.

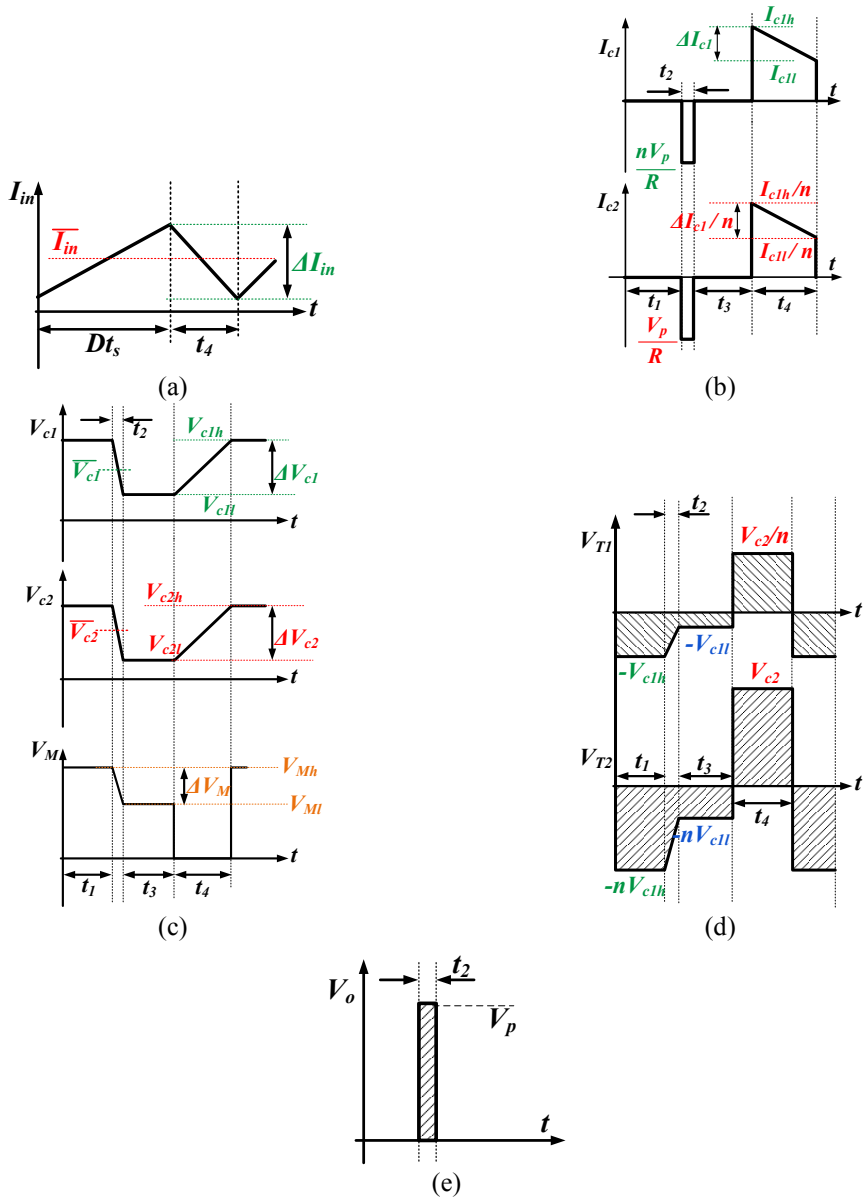


Fig.5.23. Waveforms of basic VBM. (a) Current through the input inductor. (b) Current through C_{c1} and C_{c2}. (c) Voltage across C_{c1} and C_{c2}. (d) Isolation transformer primary and secondary voltages. (e) The output generated pulse.

i) $t_1\ (0 < t < \frac{D-\delta}{2} t_s)$

During period t_1, (Fig.5.22b) the input current I_{in} increases and L_{in} energises, the load is connected to an open circuit, and the voltage of capacitors C_{c1} and C_{c2} are constant. The differential equations that describe the circuit in this period are:

$$\frac{dI_{in}}{dt} = \frac{1}{L_{in}} V_{in} \tag{5.8}$$

$$\frac{dV_{c1}}{dt} = 0 \tag{5.9}$$

$$\frac{dV_{c2}}{dt} = 0 \tag{5.10}$$

$$I_o = 0 \tag{5.11}$$

ii) $t_2 \left(\frac{D-\delta}{2} t_s < t < \frac{D+\delta}{2} t_s\right)$

During t_2, (Fig.5.22c) the input current I_{in} continues to increase while the load is connected to capacitor C_{c2} in series with S_{x1}. This leads to a sudden voltage pulse across the load. Capacitors C_{c1} and C_{c2} discharge as their voltages decrease. The differential equations that describe the circuit in this period are:

$$\frac{dI_{in}}{dt} = \frac{1}{L_{in}} V_{in} \tag{5.12}$$

$$\frac{dV_{c1}}{dt} = \frac{-n}{C_{c1}} I_o \tag{5.13}$$

$$\frac{dV_{c2}}{dt} = \frac{-1}{C_{c2}} I_o \tag{5.14}$$

$$I_o = \frac{nV_{c1} + V_{c2}}{R} \tag{5.15}$$

iii) $t_3 \left(\frac{D+\delta}{2} t_s < t < D t_s\right)$

The same operation is repeated as in period t_1.

iv) $t_4 \left(D t_s < t < t_s\right)$

I_{in} decreases and L_{in} releases energy into the capacitors while the voltages V_{c1} and V_{c2} increase. No voltage is impressed across the load R, see Fig.5.22d. The describing differential equations are:

$$\frac{dI_{in}}{dt} = \frac{1}{L_{in}} V_{in} - \frac{1}{L_{in}} V_{c1} - \frac{1}{nL_{in}} V_{c2} \tag{5.16}$$

$$\frac{dV_{c1}}{dt} = \frac{1}{C_{c1}} I_{in} \tag{5.17}$$

$$\frac{dV_{c2}}{dt} = \frac{1}{nC_{c2}} I_{in} \tag{5.18}$$

$$I_o = 0 \tag{5.19}$$

The voltage and current waveforms of the basic VBM during one complete cycle of pulse generation are depicted in Fig.5.23. Fig.5.23a shows the current through the input inductor. The current through C_{c1} and C_{c2} are shown in Fig.5.23b, while the voltage waveforms across C_{c1} and C_{c2} are shown in Fig.5.23c along with the resultant VBM terminal voltage V_M. The isolation transformer's primary and secondary voltages are shown in Fig.5.23d, while the generated voltage pulse is shown in Fig.5.23e.

Assuming the pulse duty ratio δ is small with respect to the main duty ratio D and solving equations (5.8) to (5.19), the circuit currents and voltages are

$$\bar{I}_{in} = \frac{\delta V_P^2}{R V_{in}} \tag{5.20}$$

$$\Delta I_{in} = \frac{D t_s V_{in}}{L_{in}} \tag{5.21}$$

$$I_{c1h} = \frac{\delta V_P^2}{R V_{in}} + \frac{D t_s V_{in}}{2 L_{in}} \tag{5.22}$$

$$I_{c1l} = \frac{\delta V_P^2}{R V_{in}} - \frac{D t_s V_{in}}{2 L_{in}} \tag{5.23}$$

$$V_P = \frac{n}{1-D} V_{in} \tag{5.24}$$

$$\bar{V}_{c1} = V_{in} \tag{5.25}$$

$$\Delta V_{c1} = \frac{(1-D) t_s \bar{I}_{in}}{C_{c1}} \tag{5.26}$$

$$V_{c1h} = V_{in} + \frac{(1-D) t_s \bar{I}_{in}}{C_{c1}} \tag{5.27}$$

$$V_{c1l} = V_{in} - \frac{(1-D) t_s \bar{I}_{in}}{C_{c1}} \tag{5.28}$$

$$\bar{V}_{c2} = \frac{nD}{1-D} V_{in} \tag{5.29}$$

$$\Delta V_{c2} = \frac{(1-D) t_s \bar{I}_{in}}{n C_{c2}} \tag{5.30}$$

$$V_{c2h} = \frac{nD}{1-D} V_{in} + \frac{(1-D) t_s \bar{I}_{in}}{2 n C_{c2}} \tag{5.31}$$

$$V_{c2l} = \frac{nD}{1-D} V_{in} - \frac{(1-D) t_s \bar{I}_{in}}{2 n C_{c2}} \tag{5.32}$$

$$V_{Mh} = V_{c2h} + nV_{c1h} \tag{5.33}$$

$$V_{Ml} = V_{c2l} + nV_{c1l} \tag{5.34}$$

5.3.2 Structure and Operation of the SUPG Topology

Fig.5.20 shows the proposed SUPG is comprised of the parallel in series out connection of N voltage boosting modules shown in Fig.5.21. Galvanic isolation of the boosting part in the individual VBM enables series connection of N modules, while for HV voltage sharing the initial switches S_{x1} and S_{x2} are replaced by two arms (Arm1 and Arm2) of series connected MMC-SMs. Arm1 is formed of m_1 conventional HB-SMs, while each of the m_2 SMs of Arm2 are formed with two diodes, a switch, and a capacitor.

The basic operation of the proposed SUPG can be described as follows: with the operation sequence shown in Fig.5.22a, switches S_i (where, $i \in \{1, 2, \dots N\}$) are turned on during t_1, t_2, and t_3 and off otherwise, allowing the input inductors to energise. During t_2, the lower switches of the SMs in Arm1 (S_{A1jy} where, $j \in \{1, 2, \dots m_1\}$) are turned on, that is bypassed while the lower diodes in Arm2 (D_{A2ky} where $k \in \{1, 2, \dots m_2\}$) are reverse biased, thus a voltage difference V_{AB} is impressed across the load. During t_4, the lower diodes of the SMs in Arm1 (D_{A1jy} where $j \in \{1, 2, \dots m_1\}$) and Arm2 conduct a charging current of $(I_{in}/n)/N$ through the N charging capacitors C_{c2}.

The diodes D_i prevent unintended series connection of secondary sides of the isolation transformers due to any delay in primary side switch gate signals.

Based on the VBM in section 5.3.1 and assuming that the component values of the N VBMs are identical, the average voltages of the each voltage boosting stage is:

$$\bar{V}_{ci1} = V_{in} \tag{5.35}$$

$$\bar{V}_{ci2} = \frac{nD}{1-D} V_{in} \tag{5.36}$$

Accordingly, the input inductor current of the individual VBMs is:

$$\bar{I}_{in} = \frac{\delta V_P^2}{NRV_{in}} \tag{5.37}$$

The primary and secondary transformer voltages of each VBM are:

$$\bar{V}_{Ti1} = \begin{cases} -V_{in}, & 0 \le t < Dt_s \\ \dfrac{D}{1-D}V_{in}, & Dt_s \le t < t_s \end{cases} \tag{5.38}$$

$$\bar{V}_{Ti2} = \begin{cases} -nV_{in}, & 0 \le t < Dt_s \\ \dfrac{nD}{1-D}V_{in}, & Dt_s \le t < t_s \end{cases} \tag{5.39}$$

During t_2, the midpoint 'm' is connected to the upper point 'A' through semiconductor switches S_{A1jy}. Consequently, a voltage pulse with duty ratio δ and magnitude V_P is impressed across the load R. The pulse peak voltage is:

$$V_P = \sum_{i=1}^{i=N} (V_{ci2} - V_{Ti2}) \tag{5.40}$$

thus

$$V_P = \frac{nN}{1-D}V_{in} \tag{5.41}$$

As concluded from (5.41), the output voltage is amplified by three mechanisms: (i) the N utilised VBMs converters, (ii) transformer turns ratio n, and (iii) the individual VBMs duty ratio D. The average capacitor voltages of the Arm1 and Arm2 SM-capacitors are:

$$V_{cA1j} = \frac{V_P}{m_1} \tag{5.42}$$

$$V_{cA2k} = \frac{V_P}{m_2} \tag{5.43}$$

5.3.3 SUPG Parameters Selection

The main merits of the SUPG are that of obtaining high voltage output pulses with readily available semiconductor technology and a relatively low input voltage; thus modularity, scalability and flexibility features arise. Starting from the load side, the voltage and current stresses of the Arm1 SM switches are:

$$\hat{V}_{SA1jx} = \hat{V}_{SA1jy} = \frac{V_P}{m_1} \tag{5.44}$$

$$\hat{I}_{SA1jy} = \frac{V_P}{R} \tag{5.45}$$

$$\hat{I}_{DA1jy} = \frac{\bar{I}_{in}}{n} \tag{5.46}$$

The current stresses of the clamping switches and diodes (S_{A1jx} and D_{A1jx}) are relatively small and hence, switches with lower current ratings can be used. Similarly, the voltage and current stresses of the Arm2 SMs are:

$$\hat{V}_{SA2kx} = \hat{V}_{SA2ky} = \frac{V_P}{m_2} \tag{5.47}$$

$$\hat{I}_{DA2ky} = \frac{\bar{I}_{in}}{n} \tag{5.48}$$

Assuming a modular design and 'τ' and 'ε' are the voltages and current derating factors of the Arm SMs devices, the number of Arm1 SMs (m_1) should satisfy

$$m_1 \geq \frac{V_P}{\tau V_{rA1}} \tag{5.49}$$

$$I_{rA1} \geq \frac{\bar{I}_{in}}{\varepsilon n} \tag{5.50}$$

where V_{rA1} and $I_{rA1}$are the rated voltage and current of Arm1 devices, respectively. Similarly, the number of Arm2 SMs (m_2) should satisfy

$$m_2 \geq \frac{V_P}{\tau V_{rA2}} \tag{5.51}$$

where V_{rA2} is the rated voltage of Arm2 devices. As they conduct the charging currents of the clamping capacitors, the current ratings of Arm2 SM devices can be small compared to Arm1 device ratings.

Assuming 'μ' and 'σ' are the voltages and current derating factors of the devices in the VBMs, the number of the VBMs (N) should satisfy

$$N \geq \frac{\bar{I}_{in}}{\sigma I_{rM}} \tag{5.52}$$

The maximum duty ratio D_{max} is related to the voltage stresses across the module's devices, viz.:

$$D_{max} \leq \frac{V_{rM} - \mu V_{in}}{V_{rM}} \tag{5.53}$$

where V_{rM} and I_{rM} are the rated voltage and current of the VBM devices, respectively.

The VBMs passive element values are selected in order to keep the ripple current and voltage within certain ranges. The ripple across the different elements can be calculated from [87] as:

$$\Delta V_{c1} = \frac{(1 - D_{max}) t_s \bar{I}_{in}}{N C_{c1}} \tag{5.54}$$

$$\Delta V_{c2} = \frac{(1 - D_{max}) t_s \bar{I}_{in}}{n N C_{c2}} \tag{5.55}$$

$$\Delta I_{in1} = \frac{D_{max} t_s V_{in}}{L_{in}} \tag{5.56}$$

Defining the ripple factors as:

$$x = \frac{\Delta V_{c1}}{\bar{V}_{c1}} \tag{5.57}$$

$$y = \frac{\Delta V_{c2}}{\bar{V}_{c2}} \tag{5.58}$$

$$z = \frac{\Delta I_{in1}}{\bar{I}_{in1}} \tag{5.59}$$

Accordingly, the passive element values should be:

$$C_{c1} \geq \frac{(1 - D_{max})^2 t_s \bar{I}_{in}}{N x V_{in}} \tag{5.60}$$

$$C_{c2} \geq \frac{(1 - D_{max})^2 t_s \bar{I}_{in}}{n^2 N y V_{in}} \tag{5.61}$$

$$L_{in} \geq \frac{N D_{max} t_s V_{in}}{z \bar{I}_{in1}} \tag{5.62}$$

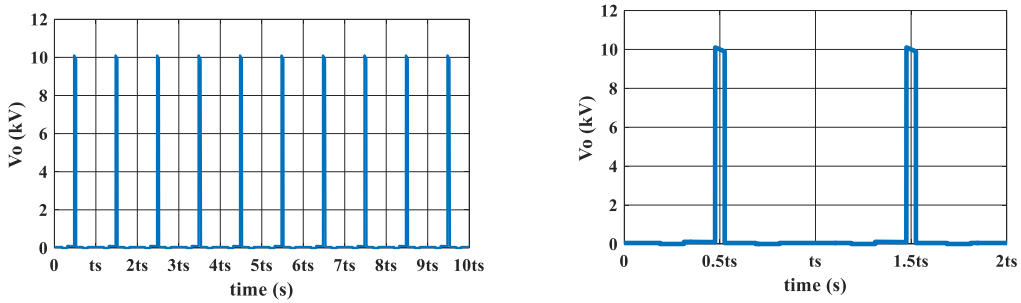
Because energy transfer is conducted through the VBM capacitors C_{c1} and C_{c2}, the SMs capacitance of Arm1 and Arm2 can be relatively small. The upper switches in the SMs (S_{A1jx} and S_{A2kx}) are responsible for discharging the capacitors when their terminal voltages increase above the desired range for any unexpected reason in order to ensure balanced voltages across the cells.

Based on the previous analysis, the parameters of the proposed system are as in Table 5.3 for generating an HV pulse of 10kV peak. For modular design, all the transformers are wound for an isolation and clearance voltage higher than the peak value of the pulses as this stress voltage is experienced by the SM at the highest potential. In addition, if the ground point is moved to the point m, the required

insulation voltage is reduced to half the output voltage, without affecting converter operation.

Table 5.3: SUPG Simulation Parameters Selection for 10kV Pulse Generation

Parameter		Value
Input DC voltage	V_{in}	100V
Output Pulse peak-voltage	V_P	10 kV
Pulse repetition time	t_s	100 µs
Load resistance	R	500 Ω
Maximum pulse duty ratio	δ_{max}	0.1
Maximum input current	I_{in}	200A
Rated voltages of SM devices	V_{rA1} and V_{rA2}	1500V
Rated currents of SM devices	I_{rA1} and I_{rA2}	40A
Rated voltage of VBM devices	V_{rM}	600V
Rated current of VBM devices	I_{rM}	60A
Derating factors of VBMs	μ and σ	0.75
Derating factors of MMC-SMs	τ and ε	0.75
Number of VBMs	N	5
Transformers turns ratio	n	5
Number of SMs in Arm1 and Arm2	m_1 and m_2	9
Maximum duty ratio of VBMs	D_{max}	0.8
Ripple factors	x, y and z	10%, 2% and 10%
VBMs capacitances	C_{c1} and C_{c2}	80µF and 10µF
VBMs inductances	L_{in}	2mH
MMC-SM capacitances	C_{A1} and C_{A2}	2 µF



(a) (b)

Fig.5.24. SUPG simulation results with 10kHz repetition rate and pulse duration of 5µs. (a) Train of pulses. (b) Time expanded view of the pulses train.

5.3.4 SUPG Simulation Results

MATLAB/SIMULINK simulations of the SUPG in Fig.5.20, with the values in Table 5.3, illustrate the operation of the proposed HV topology.

Fig.5.24 shows the load voltage pulses with $\delta = 0.05$ (that is, 5µs pulse time) and when the repetition rate of the output train pulses is equal to the switching frequency of the boosting modules ($f_s = 10$kHz). The generated pulses repetition rate is independent of f_s and can be varied according to the application.

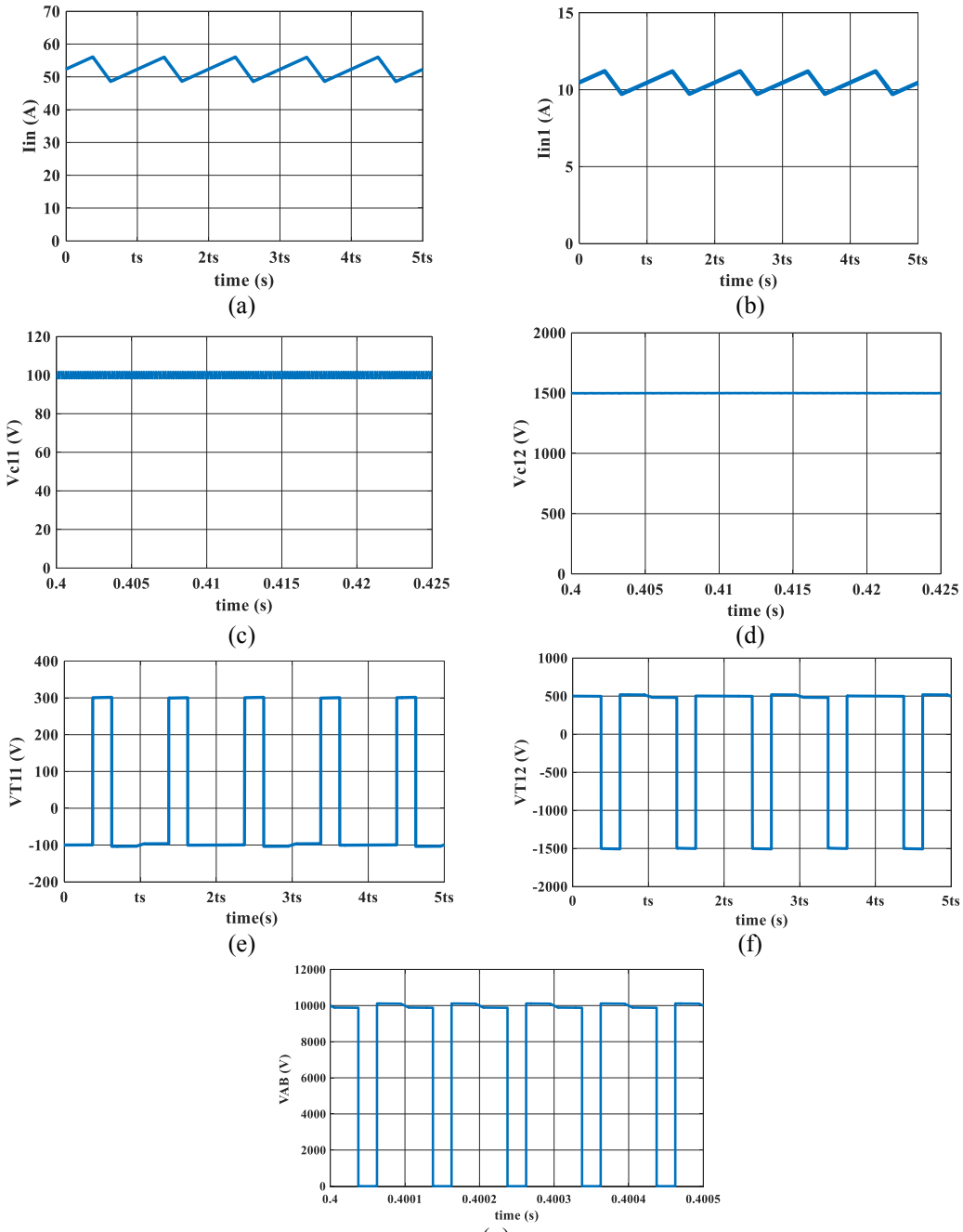


Fig.5.25. SUPG simulation results of current and voltage waveforms at different parts of the SUPG (5kHz repetition rate and pulse duration of 20µs). (a) Total input current drawn from the DC-input supply. (b) First VBM input current. (c) First VBM primary side capacitor voltage (V_{C11}). (d) First VBM secondary side capacitor voltage (V_{C12}). (e) Voltage across the first VBM primary side (V_{T11}). (f) Voltage across the first VBM secondary side (V_{T12}). (g) Total terminal voltage (V_{AB}).

Various performance current and voltage waveforms of the SUPG are depicted in Fig.5.25. Fig.5.25a shows the total input current drawn from the input supply, while the first VBM current is shown in Fig.5.25b with the expected one-fifth the total input current. The capacitor voltages of the primary, V_{C11}, and secondary, V_{C12}, sides of the first VBM are shown in Fig.5.25c and Fig.5.25d, respectively. The voltages across the primary, V_{T11}, and secondary, V_{T12}, of the first VBM are shown in Fig.5.25e and Fig.5.25f, respectively, which confirm transformer volt-second balance. The terminal voltage V_{AB} is shown in Fig.5.25g.

The individual SM voltages in Arm1 and Arm2 are explored in Fig.5.26a and Fig.5.26b, respectively. As mentioned, the generated output pulse train repetition rate not necessarily the same as the VBMs switching frequency. Therefore, Fig.5.26c shows the output voltage pulses with a 5kHz repetition rate and a 20µs pulse duration when the VBMs switching frequency is $f_s = 10$kHz. At start-up of the proposed converter, the duty ratio D can be increased gradually following a first-order capacitive circuit manner until it reaches the final steady-state value in order to ease the charging process of the SM capacitors and avoid exceeding acceptable limits.

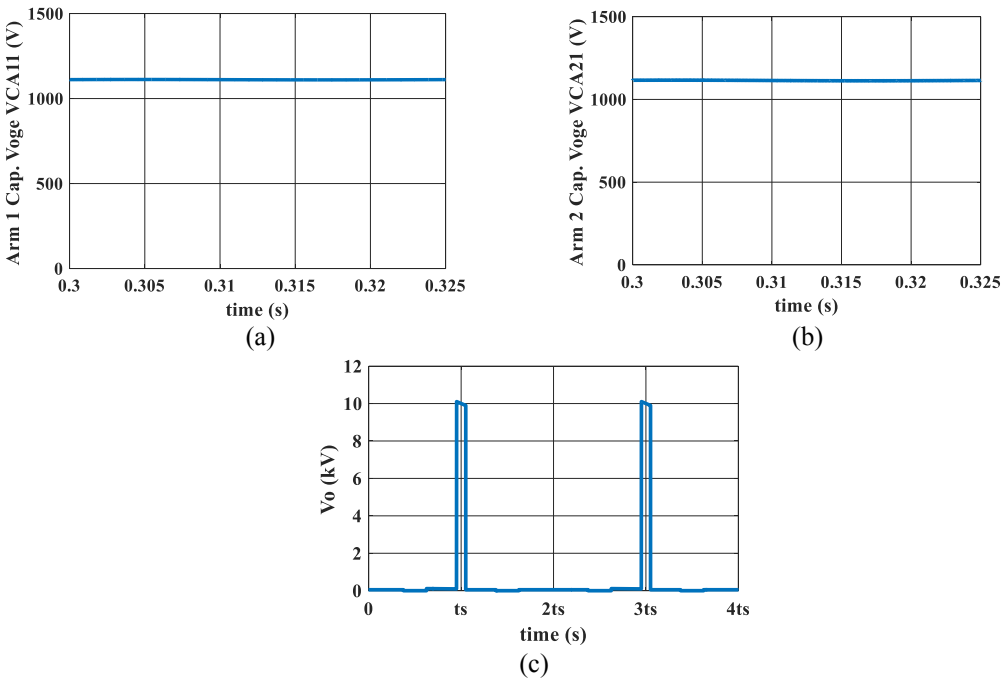


Fig.5.26. SUPG simulation results for 5kHz repetition rate and 20µs pulse duration. (a) First SM capacitor voltage in Arm1. (b) First SM capacitor voltage in Arm2. (c) Output voltage pulses.

Table 5.4: SUPG Experimental Specification

Parameter		Value
Input DC voltage	V_{in}	50 V
Output Pulse peak-voltage	V_P	500 V
Load resistance	R	100 Ω
Maximum pulse duty ratio	δ_{max}	0.1
Number of VBMs	N	2
Transformers turns ratio	n	1
Number of SMs in Arm1 and Arm2	$m_1$andm_2	2
Maximum duty ratio of VBMs	D_{max}	0.8
VBMs capacitances	C_{c1}andC_{c2}	80 µF and 10 µF
VBMs inductances	L_{in}	3.5 mH
MMC-SM capacitances	C_{A1}andC_{A2}	2 µF
IGBT switches part no.	FGY75N60SMD	

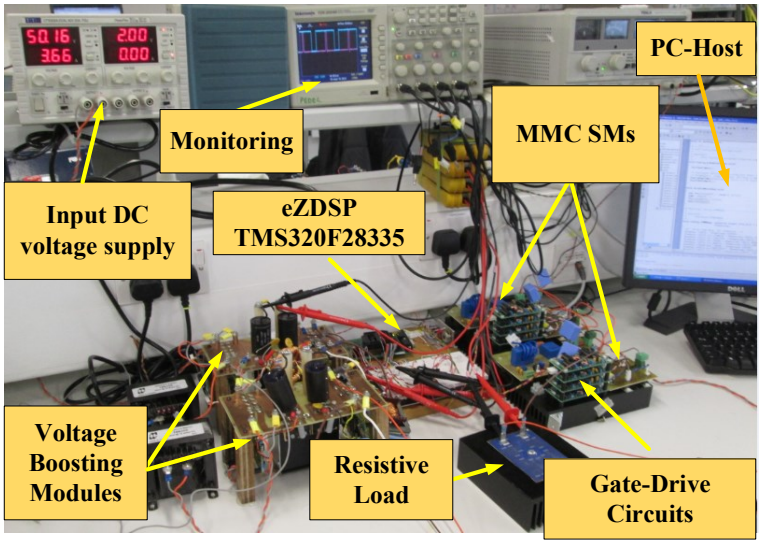


Fig.5.27. The proof of concept SUPG experimental prototype.

5.3.5 SUPG Proof of Concept Experimental Results

To show the operation of the proposed system and validate the mathematical analyses and simulation results, the proof of concept hardware prototype in Fig.5.27 is employed, with the parameters in Table 5.4, and controlled with Texas Instruments TMS320F28335 DSP.

Fig.5.28a shows a train of the experimentally generated output voltage pulses with 500V pulse-peak, 10kHz repetition rate, and 2.5µs pulse duration. A time-expanded view of one pulse cycle is depicted in Fig.5.28b. Fig.5.28c and Fig.5.28d show the total input current drawn from the input supply and the first VBM drawn current.

Since two VBMs are utilised, the first VBM draws one-half the total input current. The first SM-capacitor voltage in Arm1 and Arm2 are explored in Fig.5.28e. The voltages across the primary (V_{T11}) and secondary (V_{T12}) of the first VBM are shown in Fig.5.28h.

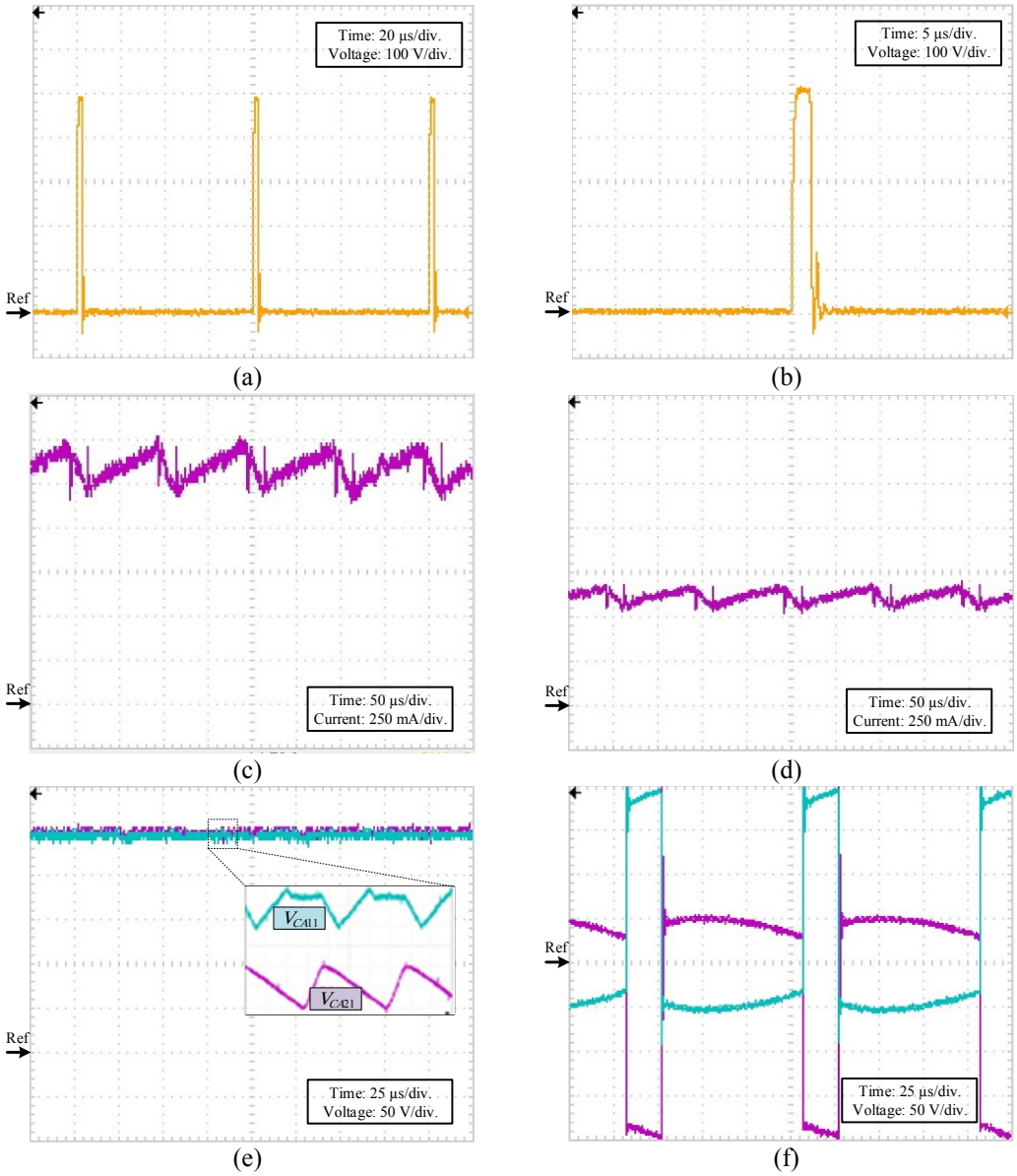


Fig.5.28. SUPG experimental results when generating pulses of 10 kHz repetition rate and pulse duration of 2.5µs. (a) The train of the generated voltage pulses. (b) One cycle of the generated voltage pulses. (c) Total input current drawn from the DC-input supply. (d) First VBM input current. (e) One SM-capacitor voltage in Arm1 and Arm2. (f) Voltage across the first VBM primary and secondary sides.

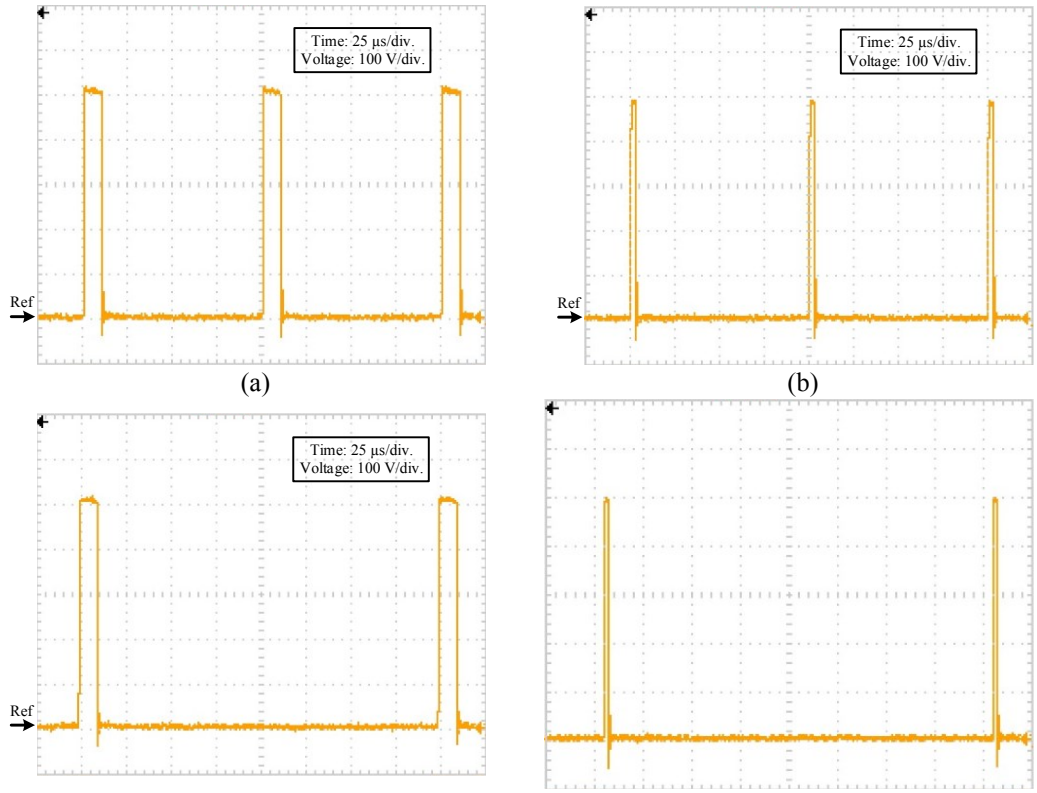


Fig.5.29. SUPG experimental results when generating different pulse repetition-rates and pulse-durations.(a) Train of 10 kHz and 10µs pulses. (b) Train of 10 kHz and 2.5µs pulses. (c) Train of 5 kHz and 10µs pulses. (d) Train of 5 kHz and 2.5µs pulses.

Finally, the flexibility of generating a wide range of different pulse repetition rates and pulse durations are explored in Fig.5.29. With a pulse duration of 10µs and repetition rate of 10kHz, Fig.5.29a shows the generated pulse train. Fig.5.29b explores the train of pulses with the same 10kHz repetition rate, with 2.5µs pulse durations. Fig.5.29c shows pulses with a 5kHz repetition rate and 10µs pulse duration, while Fig.5.29d shows pulses with a 5kHz repetition rate and 2.5µs pulse duration.

The SUPG topology can be extended to generate bipolar voltage pulses, which may be required for some electroporation applications, by forming an H-bridge with two additional MMC arms across the treatment chamber, similar to Fig.3.2.

5.4 Summary

This chapter presented three different PG topologies based on utilising a transformer. In the TSPG topology, an LV input supply is used to charge N SM capacitors

sequentially, like the SPG topology presented in section 4.1. Utilising a step-up transformer with an n turns ratio at the output stage, the output pulse-peak is increased. The generated pulses duration is adversely affected by transformer leakage inductance. The TSPG only generates bipolar pulses that assure transformer voltage-second balance, otherwise the transformer core will saturate. The remaining two topologies, IPG and SUPG, do not utilise a transformer across the load, but are used for isolation and voltage step-up before the pulse generation stage, not across the load. In the IPG, isolated DC sources are formed using transformers to continuously charge FB-SM capacitors. The IPG FB-SMs can generate conventional electroporation pulse waveforms while assuring SM capacitor voltage balance. In the SUPG, several voltage boosting modules are connected in parallel-input series-output form with the aid of transformers. As a result, the SUPG has three voltage step-up mechanisms namely: the duty ratio control of the voltage boosting modules, the turns ratio of the isolation transformers, and the number of voltage boosting modules.

Chapter 6

Conclusion and Future Research

This chapter summarises the general conclusion arising from the research, main contribution by the author, and the envisaged future research in the area of modular HV pulse generator topologies.

6.1 Conclusions

Chapter one summarised the concept and the process of electroporation. The two main types of electroporation along with the related applications were introduced. The electroporation pulse generator load modelling was highlighted and since micro-second pulse durations are considered in this thesis, it was concluded that the electroporation load can be effectively modelled by a resistor.

Chapter two presented a literature review for classical PGs and newly developed power electronics based-PGs for electroporation applications. Power electronics-based PGs were collated into three main groups, namely: non MMC-based, MMC-based, and hybrid topologies. The main features and limitations for each category were highlighted. It was concluded that power electronic PGs offer better pulse shape flexibility than traditional approaches.

Chapter three presented a new family of HV DC fed MMC based PGs. The proposed topologies addressed limitations facing existing MMC based topologies. The research focused on generating flexible HV pulses with full utilisation of the input HV DC while assuring SM capacitor voltage balance. The HV DC source was assumed to exist but AC-DC converter possibilities for the HV DC source were considered in an appendix, Appendix A. It was concluded that the complication of such an HV DC source is a limitation of said PGs.

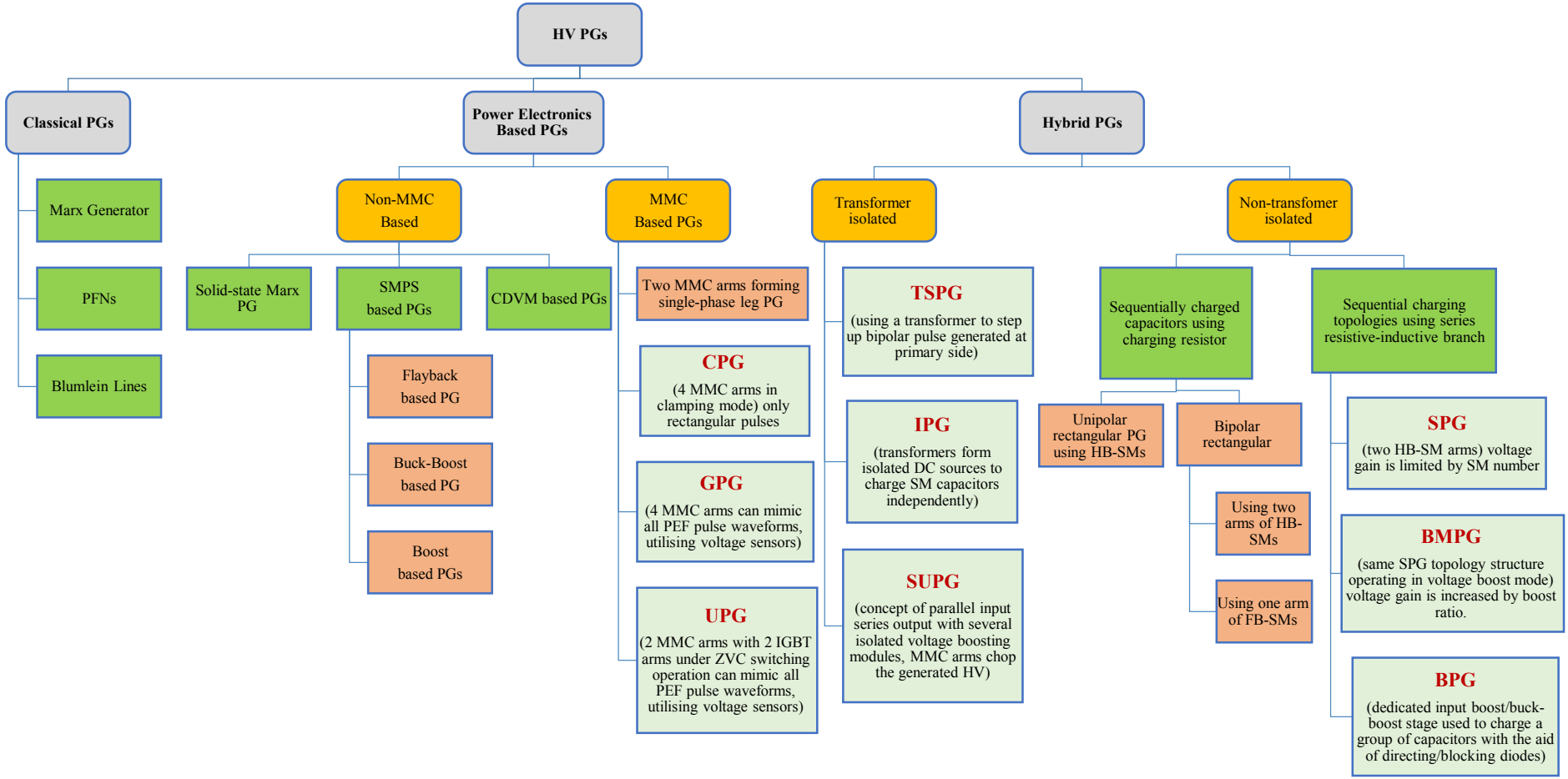


Fig.6.1. Summary of the PG family (author's contribution are the 9 PG blocks with bold red mnemonics).

Chapter four presented a new family of hybrid PGs fed from LV DC. The topologies address the limitations of existing sequentially charging topologies. A methodology to generate different pulse waveforms from hybrid topologies was introduced.

Chapter five explored the possibilities of transformer utilisation in MMC based and hybrid PGs. It was concluded that both saturation and leakage present limitation of a transformer approach.

The block diagram summarising the main family PG groups and family members presented in Fig.2.18 are shown in Fig.6.1. The proposed nine topologies are included among the existing topologies under the appropriate family. Additionally, a comparative matrix summarising the ranking of the proposed PGs in terms of wide range of attributes is given in Table 6.1.

6.2 Author's Contribution

With the aid of Fig.6.1, the main contribution and significance of this thesis can be summarised as:

- New categorisation of existing and the newly emerged PG topologies.
- New PG topologies with three common features namely: scalability, modularity and redundancy, have been proposed.
- Three new MMC based PG topologies (CPG, GPG and UPG) with full utilisation of the HV DC input source, were presented, such that:
  - The three MMC based PG topologies have reduced footprint and flexible pulse waveform generation. Operation under SM failure is assured.
  - The CPG topology is proposed from the GPG topology for applications requiring rectangular pulse waveforms only, therefore, voltage sensors are removed, giving cost and footprint reduction.
  - The proposed GPG and the UPG topologies are able to mimic all conventional electroporation pulse waveforms by only changing the software, without any physical changes to the power circuit.
- Six new PG topologies (SPG, BMPG, BPG, TSPG, IPG and SUPG) were proposed to generate HV pulses from an LV DC input source. These PGs

belong to the hybrid family of PGs. Unlike SPG, BMPG and BPG, the other three PGs utilise transformers, such that:

- The SPG topology presents a more efficient method to charge the SM capacitors sequentially from the LV DC input via an rL branch (rather than a resistor). Therefore fast SM charging is achieved and accordingly fast repetition rates are achievable.
- The BMPG topology is a voltage boost version of the SPG such that further voltage gain is achieved for a given footprint.
- The BPG topology utilising a boost/buck-boost converter to control the charging voltage of the SM capacitors is a variation. The BPG topology with only one voltage sensor at the boost/buck boost converter voltage level can mimic all the conventional electroporation pulse waveforms. It is the only existing PG topology fed from an LV DC input with such capability.
- The TSPG topology is proposed to explore the viability of a step-up transformer across the load. Recommendations for the pulse duration range and pulse waveform shape were presented.
- The IPG and the SUPG topologies utilise transformers to provide isolated DC voltage sources such that when cascaded, an HV DC output is obtained. Unlike the HV switch used in literature to chop the HV and form the pulse, MMC arms are employed.

- Provided comprehensive theoretical, simulation and scaled down experimental verification for all the nine proposed PG topologies.

Table 6.1: Comparative matrix of the proposed PGs

	CPG	**GPG**	**UPG**	**SPG**	**BMPG**	**BPG**	**TSPG**	**IPG**	**SUPG**
Input DC voltage, V_s	HV DC			LV DC					
Number of SMs	$4N$	$4N$	$2N$	$2N$	$2N$	$2N$	$2N$	N	$2m^*$
Total number of IGBTs in the SMs	$8N$	$8N$	$4N$	$4N$	$4N$	$4N$	$4N$	$4N$	$3m$
Type of SMs	HB	HB	HB	HB	HB	HB	HB	FB	HB
Voltage sensors	none	$4N$	$2N$	none	2	2	none	none	none
Other switches	none	none	$2N$-IGBTs	reverse voltage blocking switches rated at the negative pulse peak comprised of one IGBT and series diodes (based on their ratings)				$4N$-diodes 4-IGBTs	N-IGBTs m-diodes
SM capacitors	$4N$		$2N$	$2N$				N	$2m$
Other component	input L		none	input rL element to charge the sm capacitors				input L	$2N$-Cs N-L
Type of pulses	bipolar/unipolar						only bi-polar	bi-polar/ uni-polar	only uni-polar
Pulse waveforms	recta-ngular	all pulse waveforms		rectangular		all	recta-ngular	all	recta-ngular
SM capacitor voltage	V_s/N			V_s	λV_s		V_s	nV_s/N	$\frac{nV_s}{1-D}$
Pulse peak voltage	V_s			NV_s	λNV_s		nNV_s	nV	$\frac{nNV_s}{1-D}$
SM capacitors re-charging	each arm SM capacitors are charged simultaneously			sequentially charged		paral-lel	seque-ntially charg-ed	continuous charging	
Repetition rate	fast			moder-ate	slow	very fast	moder-ate	fast	
Repetition rate flexibility	limited by controller speed and voltage sensors band width			limited by SMs charging time				limited by controller speed	
Control complexity	simple	complex		simple	moderate		simple		mode-rate
Footprint	large		moderate	small				moderate	
Transformer utilisation	none						one with n turns ratio	one** with N secon-daries	N

*In the SUPG topology N is the number of voltage boosting modules and m is the number of SMs per Arm.
**This is a specially wound transformer with one primary turn and N secondaries each of n turns. In all topologies n is the transformer turns ratio.

6.3 Future Research

This thesis proposed a new family of power electronics based PGs. Although the proposed topologies have several distinctive features with respect to existing power electronics based PGs, some recommendations for the future research are:

- Replacing the Si IGBTs within the utilised MMC-SMs with wide band gap semi-conductor devices such as silicon-carbide and gallium nitride. This will enable sub-microsecond pulse durations and fast repetition rates.
- With the utilisation of the wide band gap devices, re-modelling of the electroporation load is necessary. Neglecting load capacitance will not be valid for sub-micro second pulse durations.
- Pulsed current waveforms used for pulsed magnetic fields also represent an extension, where such pulses are required in applications such as magnetic resonance imaging.
- Testing the power system components insulation requires a specific impulse waveform with specific characteristics. A future extension is to promote the flexibility of the proposed topologies to cover this application.

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Appendix A

High Voltage DC Supplies for HV DC Fed PGs

Generally HV PG publications do not address the issue of deriving of the HV DC from the AC grid. This appendix presents some established approaches for the HV DC supply that feeds PGs. The main two challenges for the AC-DC converter are the power factor and current harmonics. The power factor is preferred to be near unity so as to draw zero reactive power drawn from the supply. The current harmonics must comply with current harmonic limits in IEEE Std. 519-1992, summarised in Table A.1.

Table A.1: Current Harmonic Limits

Maximum Harmonic Current Distortion in % of I_L						
Individual Harmonic Order (Odd Harmonics)						
I_{SC} / I_L	h<11	11≤h<17	17≤h<23	23≤h<35	35≤h	TDD
<20*	4.0	2.0	1.5	0.6	0.3	5.0
20<50	7.0	3.5	2.5	1.0	0.5	8.0
50<100	10.0	4.5	4.0	1.5	0.7	12.0
100<1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0
Even harmonics are limited to 25% of the harmonic limits, TDD refers to Total Demand Distortion and is based the average maximum demand current at the fundamental frequency, taken at PCC.						
*All power generation equipment is limited to these values of current distortion regardless of I_{SC}, I_L.						
I_{SC} =Maximum short current at the PCC I_L = Maximum demand load current (fundamental) at the PCC h = Harmonic number						

A.1 24 Pulse Diode Rectifier

A 24 pulse rectifier can have each pulse at 15° to other pulses over a complete power cycle. This has a positive impact on the grid side input current which becomes nearly sinusoidal. Also voltage sharing is afforded by the four rectifiers being fed from their individual AC source. Thus no series connection of semiconductor devices is necessary. The required phase-shift is obtained via a phase-shifting, multi-winding three-phase transformer. The turns ratio between the primary and the secondary side is calculated such that each of the four secondaries have the same AC voltage. Fig.A.1 shows a 24 pulse rectifier along with the primary and secondary winding types to achieve the necessary phase-shifts. (Relays and any soft start resistive circuitry are not shown).

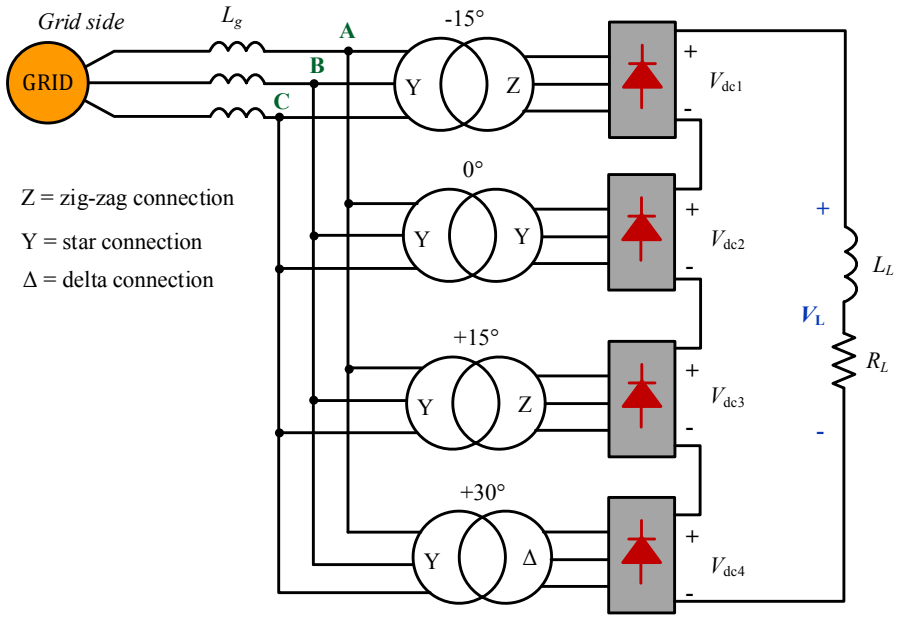

Fig.A.1. Schematic diagram of a 24 pulse rectifier.

The 24 pulse rectifier shown in Fig.A.1 is simulated with input AC supply voltage of 100kV, grid inductance 0.1mH/phase, and resistive load of 50Ω. Fig.A.2 shows the line-to-line secondary voltage of V_{AB} of the four transformers which shows AC voltages of equal magnitudes and 15° phase shifts. The resultant voltage a cross the DC load is shown in Fig.A.3 with 24 pulses per cycle. The resultant output voltage is four times the generated DC voltage by an individual 6-pulse rectifier due to the

series connection ($V_L = V_{dc1} + V_{dc2} + V_{dc3} + V_{dc4}$). The input grid phase voltage and current are shown in Fig.A.4 while the FFT analysis of phase-A current is shown in Fig.A.5. The characteristic harmonics in this spectrum are dominated by the 25th and the 23rd harmonic orders.

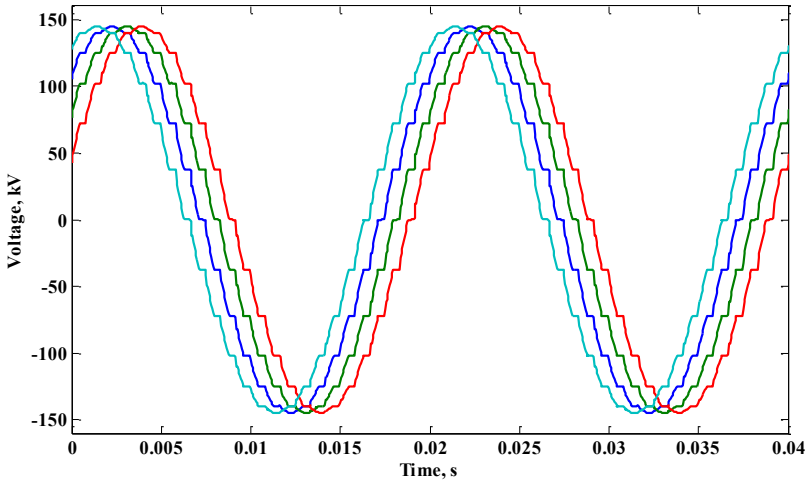

Fig.A.2. Line-to-line secondary voltage V_{AB} of the four transformers.

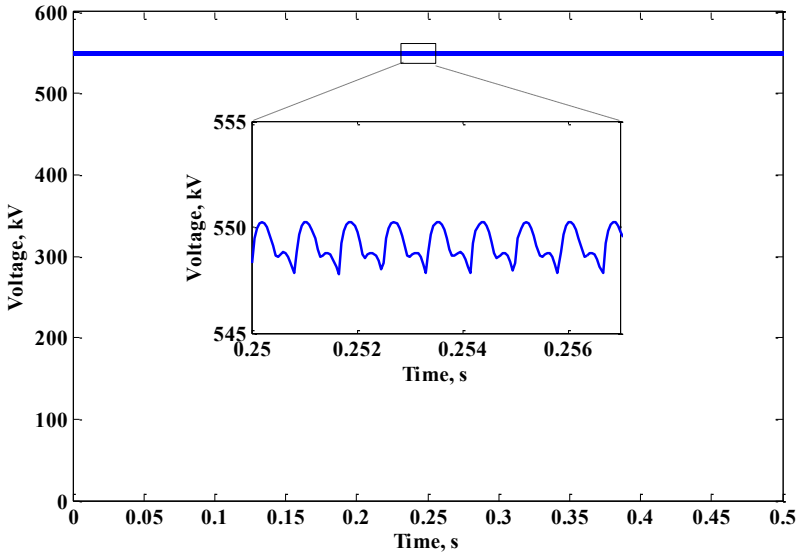

Fig.A.3. Rectifier output DC voltage.

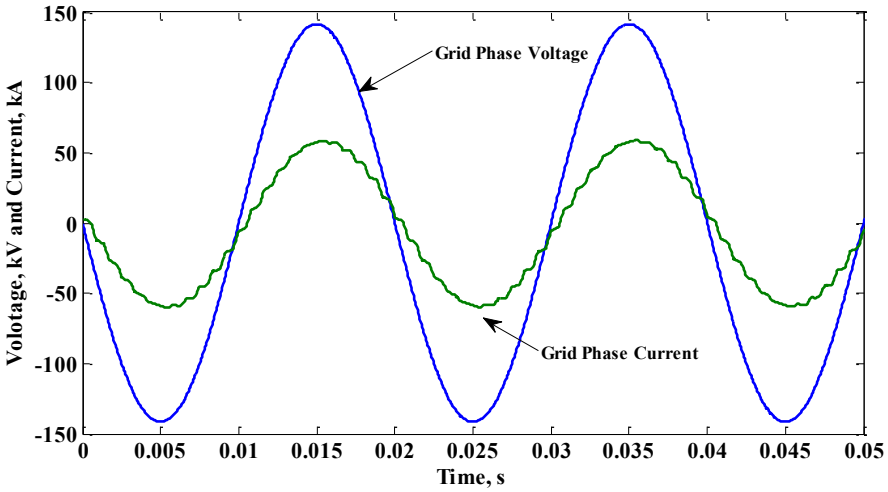

Fig.A.4. Grid phase-A input voltage and current.

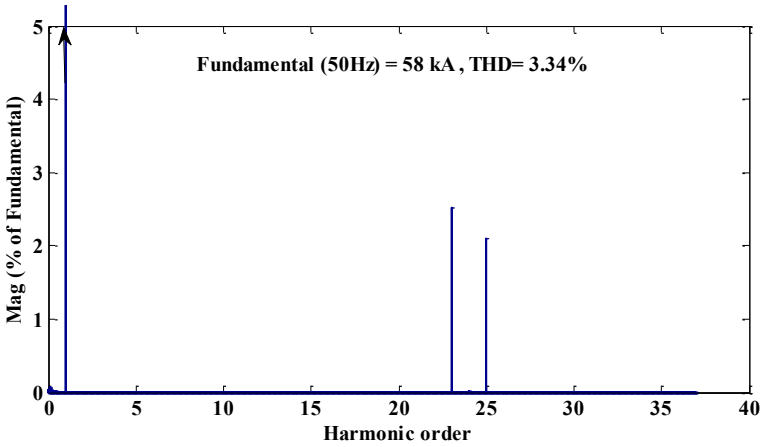

Fig.A.5. FFT analysis up to the 37th harmonic order for phase-A grid current.

As a result, the twenty four pulse rectifier has better than necessary THD results, which alleviate the need of integrating a shunt active filter. Independent of the grid voltage, 100kV AC as used in the presented simulations, the same concept is applicable at other AC voltages, for example 415V AC, depending on the system power rating.

A.2 Fully Controlled and Half Controlled 24 Pulse Rectifier

Replacing the diodes in Fig.A.1 by thyristors is ideal for high powers (thyristor: 8kV, 3.6kA average, 90kA surge), high reliability and low losses. They have a low on-state voltage (1.88V @ 3kA) and switching losses, which results in an AC-DC

converter efficiency of better than 99.5 percent. The thyristor rectifier is line commutated and forms a fully controllable DC voltage source with a small reactor in the DC link (as is used in CSI drives). 12 or 24-pulse rectifier configurations minimize converter harmonic influence on the AC supply system. Also a higher pulse number, hence transformer with phase shifted windings, reduces semiconductor voltage stresses, because rectification is at a lower voltage since the three phase rectified DC outputs are series connected. Half controlled rectifiers can be used since energy reversal, regeneration, is not needed, further improving robustness and reliability. The input rectifier, incorporating application specific AC filtering, can met the most stringent requirements for current and voltage harmonic distortion as defined in Table A.1 and the input power factor can be adjusted by AC shunt capacitors.

A.3 The Power Factor and the Harmonics at Grid Side

The 24 pulse AC-DC controlled rectifier is phase controlled for soft system start up and shut down. The controlled start-up feature can be exploited, at no converter cost, during normal operation, that is, variable DC link voltage. The only penalties are the input power factor and harmonics. Being a 24 pulse converter, the first 6 harmonics are eliminated, 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, 19^{th}, with the first harmonics appearing at the 23^{rd} - 1150Hz and 25^{th} - 1250Hz ($24n\pm1$), at frequencies with magnitudes readily attenuated by AC filters. Another penalty is input power factor deterioration with reducing output voltage $\cos\alpha$ pu (increasing thyristor gating delay, α). With all four converters employing the same firing angle, the lowest frequency input harmonic is the 23^{rd}. With zero delay angles, the reactive power Q component is zero and real power P and the output voltage are a maximum, 1pu. At a 90°angle, the output voltage is zero as is P, but Q is a maximum, 0.25pu. The reactive power (lagging) is $Q=¼\cos\alpha$, so for a 0.5pu link voltage, $\alpha=60°$ $Q=¼\sin60°$, 0.22pu. For a 1MVA drive system, the maximum reactive power Q is 0.22MVAr. Leading compensation capacitance left permanently in circuit, at 1pu link voltage, would compensate lagging power equipment in the vicinity.

A.4 AC-DC Converter with Shunt Active Compensation

An alternative to reduce the THD % and to achieve unity power factor is to utilise an active shunt filter. Fig.A.6 shows a schematic diagram for a grid feeding a conventional three-phase rectifier circuit (which is a nonlinear load), while an active filter is shunted to the grid. The shunt active filter is a voltage source inverter which is controlled to inject current harmonics, due the nonlinear load, so that the current from the grid is purely sinusoidal [88]-[89].

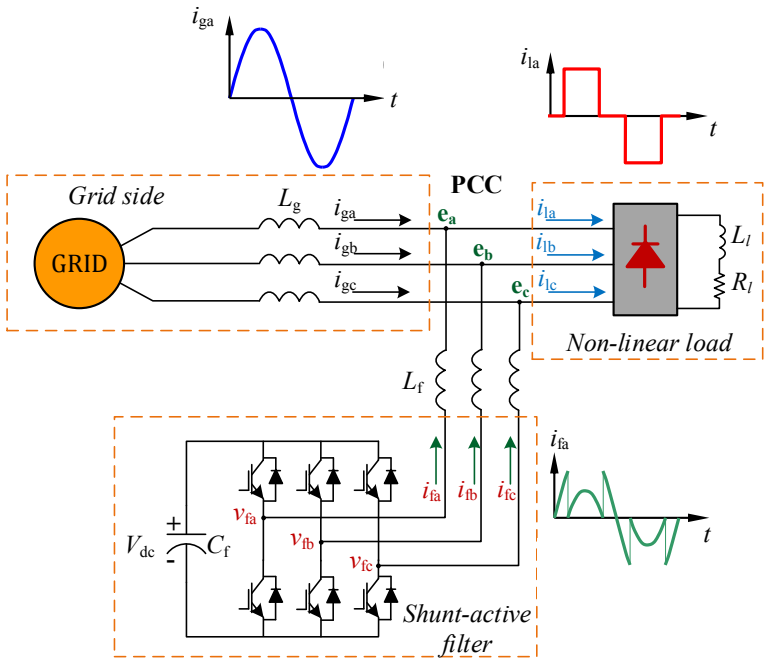

Fig.A.6. A schematic diagram of a shunt active filter connected to a grid feeding a nonlinear load.

Appendix B

Comparison between Sequentially Charged Hybrid PGs and Charging Inefficiency Aspects

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This appendix details a quantitative comparison between the MMC sequential charged PGs in Table 4.3. Also, the effect of the charging response type and the charging element (rL or just r) on the per unit charging inefficiency are investigated.

B.1 Comparison Steps between Sequential Charging Hybrid PGs

The justification of data in comparative, Table 4.3, follows:

- In [66], the authors use a resistor to charge the capacitors sequentially; the topology is shown in Fig.4.11a. It can operate in two modes, fast repetition and slow repetition rate modes. In the slow repetition rate mode, the SM capacitors are charged using the load resistor R (which is in the kΩ range). In contrast, in the fast repetition mode the load resistor is bypassed by diodes (which are rated at the HV level of the generated pulses), and another resistor r (called limiting resistor in the range of Ohms) is inserted during the charging to allow fast charging of the capacitors and hence, a fast repetition rate is achieved.
- In [67], the authors extend the topology of [66] to allow for bipolar pulse generation, as shown in Fig.4.11c.
- In [68], the authors replace the HB-MMC SMs in [66] with FB-MMC SMs to allow bipolar pulse generation as shown in Fig.4.11b.
- HV pulse specification is determined by the application and the load. The specifications are mainly pulse peak voltage V_P, repetition time T_s, and pulse duration time t_{pl}. PG design is based on parameters.

- To comparison the Sequential PG topologies [66]-[68] and the proposed SPG topology, the following specifications are assumed to allow comparison of capacitor size (capacitance) and the required semi-conductor switches:
    - The pulse peak voltage $V_P = 10$kV, the input supply is an LV DC of 1kV, thus the number of MMC-SMs is $N = 10$.
    - SM-capacitor minimum remaining voltage is 95% of the fully charged value, hence $V_\alpha = 50$V.
    - The resistive load is R = 1kΩ.
    - Pulse duration of t_{pl} =20μs, for both bipolar and unipolar modes.
    - The repetition time for all topologies is fixed at $T_s = 500$μs and 250μs for bipolar pulse and unipolar pulses, respectively.
    - Accordingly, the charging time can be calculated from $T_s = x(Nt_c + t_{pl})$, where, $x = 1$ in case of unipolar topologies and $x = 2$ for bipolar topologies. As a result, the charging time is t_c =23μs for all topologies.
    - The current drawn from the supply should not exceed available single semi-conductor switch current rating such that parallel connection is avoided. For the comparison, Infineon IHW30N160R2 IGBTs (30A maximum current and a turn-off delay of 525ns), will be considered.
- The design equations used for the sequential PG topologies [66]-[68] are

$$N_{max} = \sqrt{\frac{(T_s - t_{pl})\, R\, ln(a/b)}{t_{pl} r \ln({}^{(b-1)}/_{(a-1)})}} \tag{B.1}$$

$$C_{SM} = \frac{N t_{pl}}{R\, ln(a/b)} \tag{B.2}$$

$$t_c = r C_{SM} \tag{B.3}$$

where N_{max} is the maximum number of MMC-SMs (the used N SMs must be $\leq N_{max}$), r is the charging resistance, a and b are the upper and lower percentage of the remaining voltage across a SM-capacitor ($b = 0.95$ to comply with 5% minimum remaining voltage, and $a = 0.98$ as suggested in

[66]-[68]), and t_c is the charging time for the SM-capacitor after contributing to the pulse generation.

- The maximum charging current can be calculated for the topologies [66]-[68] as in (B.4)

$$I_{max} = \frac{V_\alpha}{r} \tag{B.4}$$

- In contrast, the SM capacitance in the proposed SPG is based on equation (B.5), with a unity safety factor.

$$C_{SM} = \frac{2Nt_{pl}}{(1-\beta^2)R} \tag{B.5}$$

- The maximum charging current can be calculated for the proposed SPG topology by the following steps

$$i(t) = \frac{V_\alpha}{\omega_d L} e^{-\alpha t}\ sin\omega_d t \tag{B.6}$$

To find the time at which the current reaches its maximum, (B.6) is differentiated and equated to zero,

$$\frac{di}{dt} = \frac{-V_\alpha}{\omega_d L}\alpha\, e^{-\alpha t}\, sin\omega_d t + \frac{V_\alpha}{L} e^{-\alpha t}\, cos\omega_d t = 0 \tag{B.7}$$

$$t_{i\_max} = \frac{\tan^{-1}(\frac{\omega_d}{\alpha})}{\omega_d} \tag{B.8}$$

Substituting (B.8) into (B.6), the maximum current is:

$$I_{max} = i\left(t_{i\_max}\right) = \frac{V_\alpha}{\omega_d L} e^{-\alpha t_{i\_max}}\, sin\omega_d t_{i\_max} \tag{B.9}$$

- Parameter selection steps for the topologies proposed in [66]-[68] and the proposed SPG are illustrated in Table B.1.

Table B.1: Steps for parameter selection based on the design equations for the four topologies

Topologies in [66]-[68]	SPG topology
1. Based on the specified 10 MMC-SMs, the percent capacitor remaining voltage, R load and pulse duration: SM-capacitance is estimated from (B.2). 2. Based on the specified charging time, and step1, the charging resistance r is estimated from (B.3). 3. Once the SM capacitance and the charging resistance are calculated, the maximum charging current is determined based on (B.4).	1. Based on the specified 10 MMC-SMs, the percent capacitor remaining voltage, R load and pulse duration: the SM capacitance is estimated from (B.5). 2. Based on the specified charging time and step1, the damping frequency is estimated from $\omega_d = \frac{\pi}{t_c}$. 3. Accordingly, for determining the two remaining parameters, equation (B.8) is solved iteratively to estimate α and ω_o, while complying with the maximum charging current. 4. Based on step 1 and 3, the three parameters are estimated.

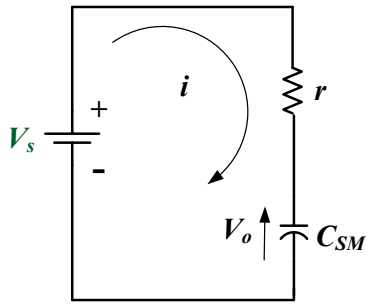

Fig.B.1. Charging process equivalent circuit with a resistor.

B.2 Effect of Charging element and Charging Response Type on Charging Inefficiency

Charging the SM capacitors with an rL or r element, results in the same charging efficiency. To prove this, consider Fig.B.1 in which the SM capacitor is charged through a resistor only. Consider a source V_s and an rC_{SM} load time constant where the capacitor is initially charged to V_o such that $V_o < V_s$. The pu charging loss (inefficiency) is defined as energy E_r lost in the resistor divided by total energy E_s from the DC supply as in Chapter 4

$$\eta_{loss} = \frac{E_r}{E_s} \tag{B.10}$$

Whether the charging circuit is rC or rLC (underdamped, critically-damped or overdamped), the pu charging losses are the same. The presence of L affects the peak charging current and the time to recharge the capacitor. L is thus a free design control variable. $V_\alpha = V_s - V_o$ is the capacitor voltage drop as a result of the previous power pulse. The rC circuit charging current, as a result of the step voltage V_α, is

$$i(t) = \frac{V_\alpha}{r} e^{-t/\tau} \tag{B.11}$$

where $\tau = rC_{SM}$ and the initial current is V_α/r.

The energy E_r dissipated in the resistor is

$$E_r = r\int_0^\infty i(t)^2 dt = \frac{V_\alpha^2}{r}\int_0^\infty e^{-2t/\tau}\, dt \tag{B.12}$$

$$E_r = ½C_{SM}V_\alpha^2 \tag{B.13}$$

The energy $E_s$drawn from the supply V_s is

$$E_s = V_s\int_0^\infty i(t) dt = \frac{V_s V_\alpha}{r}\int_0^\infty e^{-t/\tau}\, dt \tag{B.14}$$

$$E_s = C_{SM}V_s V_\alpha \tag{B.15}$$

The per unit (pu) charging inefficiency (η_{loss}) is

$$\eta_{loss} = \frac{E_r}{E_s} = \frac{½C_{SM}V_\alpha^2}{C_{SM}V_s V_\alpha} = \frac{½V_\alpha}{V_s} \tag{B.16}$$

Thus, the pu voltage drop determines the inefficient energy, $\%\eta_{loss}$ thus the charging energy efficiency $\%\eta_{ch}$, as follows:

$$\%\eta_{loss} = 100 \times ½V_{\alpha}^{pu} \tag{B.17}$$

$$\%\eta_{ch} = 100 - \%\eta_{loss} \tag{B.18}$$

This is the same result obtained in Chapter 4 for charging the SM-capacitors via rL branch.

By utilising the rL branch in the proposed SPG topology, the % inefficiency will always depend on the per-unit % drop of capacitor voltage. Changing the inductance will not affect the calculated efficiency, but it will increase/decrease the charging rate of the capacitors by decreasing/increasing the input charging current. To illustrate this effect, a simulation is used to mimic the charging instant of the SM-capacitor from a certain voltage drop and to calculate the %energy inefficiency. The simulation results are compared with the simulation results at different drop values and at three cases of the circuit response (overdamped, critically-damped and underdamped). The three cases are detailed in Table B.2, Table B.3 and Table B.4 for the overdamped, critically-damped, and underdamped cases respectively.

Table B.2: Overdamped response specifications

Overdamped (the parameters are selected such that $C_{SM} > \frac{4L}{r^2}$) $r = 1\ \Omega$, $C_{SM} = 5$ µF and $L = 1$µH		
Drop value in pu ($V_{\alpha\ pu}$)	$\%\eta_{loss}$ calculated value from (4.19)	$\%\eta_{loss}$ from Simulation results
0.05	2.5%	Fig.B.2
0.1	5%	Fig.B.3
0.2	10%	Fig.B.4
Fig.B.5 shows the capacitor charging current and the capacitor voltage charging from 950 V to 1000 V (i.e. 5% drop).		

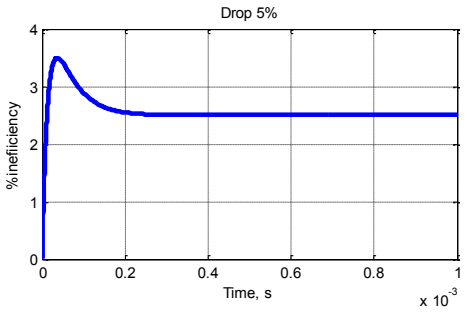

Fig.B.2. % inefficiency at 5% voltage drop.

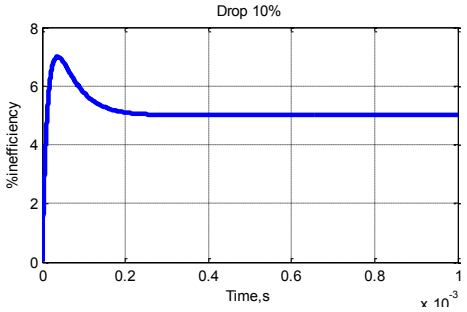

Fig.B.3. % inefficiency at 10% voltage drop.

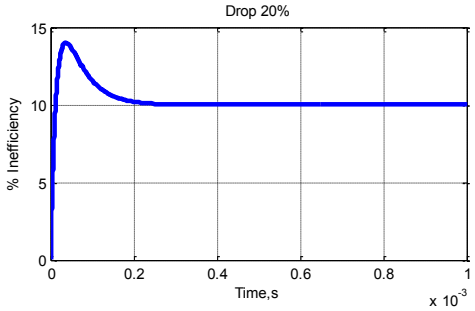

Fig.B.4. % inefficiency 20% voltage drop.

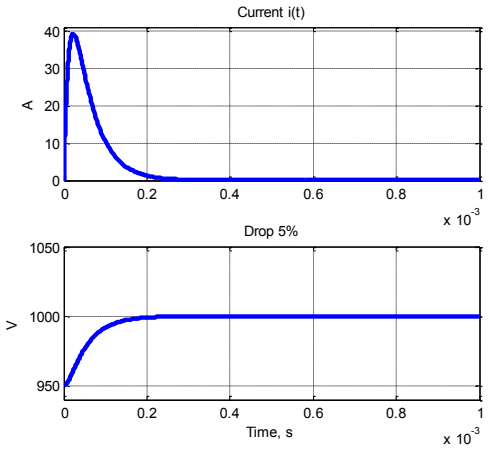

Fig.B.5. Response of current $i(t)$ and capacitor voltage at 5% voltage drop

Table B.3: Critically-damped response specifications

Critically-damped (the parameters are selected such that $C_{SM} = \frac{4L}{r^2}$) $r = 1\Omega$, $C_{SM} = 4\mu F$ and $L = 1\mu H$		
Drop value in pu ($V_{\alpha\, pu}$)	$\%\eta_{loss}$ calculated value from (4.19)	$\%\eta_{loss}$ from Simulation results
0.05	2.5%	Fig.B.6
0.1	5%	Fig.B.7
0.2	10%	Fig.B.8
Fig.B.9 shows the capacitor charging current and the capacitor voltage charging from 900 V to 1000 V (i.e. 10%).		

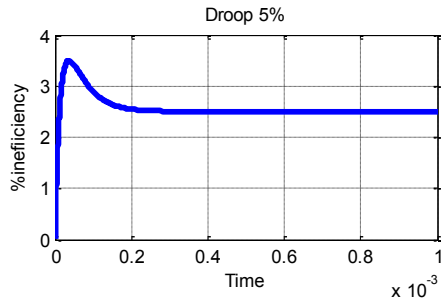

Fig.B.6. % inefficiency at 5% voltage drop.

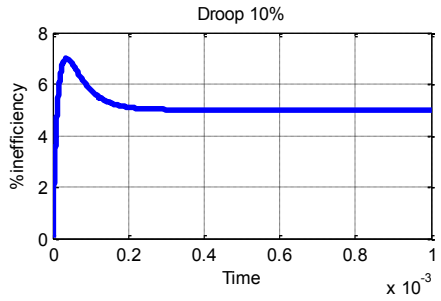

Fig.B.7. % inefficiency at 10% voltage drop.

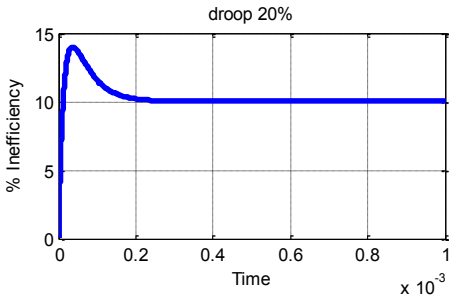

Fig.B.8. % inefficiency 20% voltage drop.

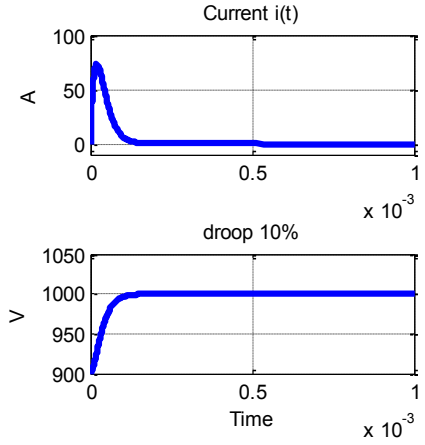

Fig.B.9. The response of the current $i(t)$ and capacitor voltage at 5% voltage drop

Table B.4: Underdamped response specifications

Critically-damped (the parameters are selected such that $C_{SM} = \frac{4L}{r^2}$) $r = 1\Omega$, $C_{SM} = 2\mu F$ and $L = 1\mu H$		
Drop value in pu ($V_{\alpha\, pu}$)	$\%\eta_{loss}$ calculated value from (4.19)	$\%\eta_{loss}$ from Simulation results
0.05	2.5%	Fig.B.10
0.1	5%	Fig.B.11
0.2	10%	Fig.B.12
Fig.B.13 shows capacitor charging current and the capacitor voltage charging from 800 V to 1000 V (i.e. 20% drop).		

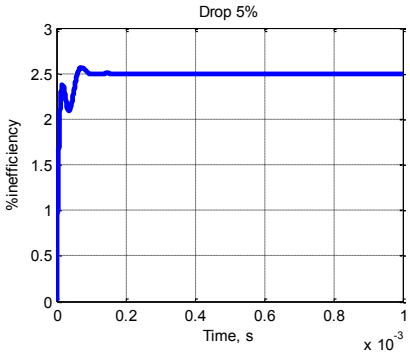

Fig.B.10. % inefficiency at 5% voltage drop.

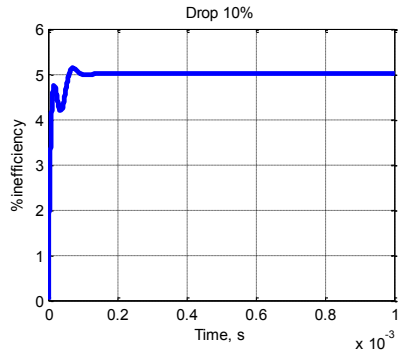

Fig.B.11. % inefficiency at 10% voltage drop.

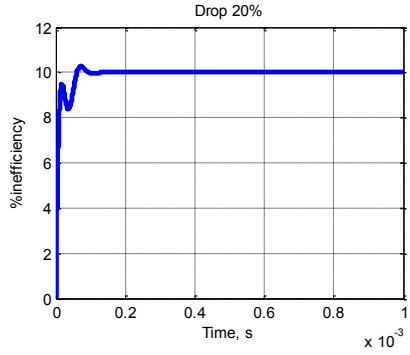

Fig.B.12. % inefficiency 20% voltage drop.

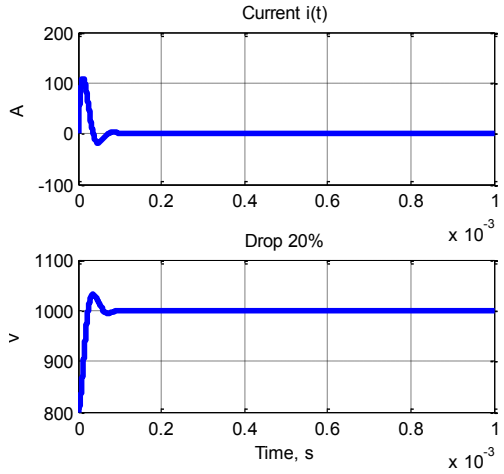

Fig.B.13. The response of the current $i(t)$and capacitor voltage at 5% voltage drop

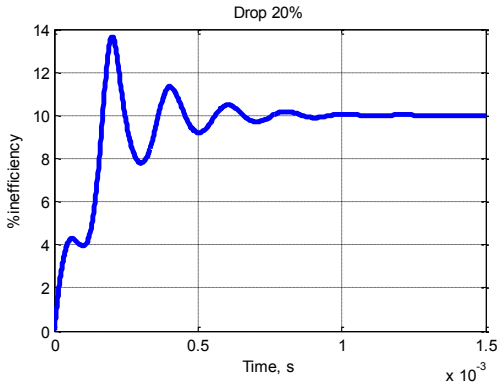

Fig.B.14. % inefficiency 20% voltage drop when L is replaced by $10L$.

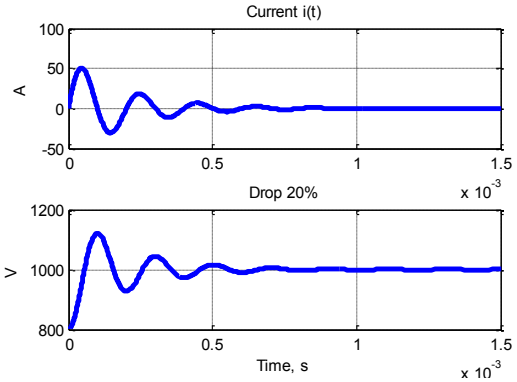

Fig.B.15. The response of the current $i(t)$ and capacitor voltage at 5% voltage drop L is replaced by$10L$.

Finally, to illustrate the inductance effect on the charging time and current, the same parameters of the underdamped case are used, and the value of L is replaced by $10L$. The obtained results are shown in Fig.B.14 and Fig.B.15 at drop of 20%. It is established that increasing the inductance decreases the peak charging current and elongates the charging time

Appendix C

Test Rigs and Software Control

This appendix presents the main utilised hardware elements, along with a sample simulation, and experimental software programmes.

C.1 Digital Signal Processor (DSP)

The DSP is responsible for reading the actual voltage and current waveforms from the measurement devices. Then, the DSP controls the overall operation according to the loaded program in its flash memory. Accordingly, the controller must have features such as a fast calculating processor, sufficient storage memory, compatible and fast analogue to digital converters, and easy programming packages. For these reasons, Texas Instrument (TI) TMS320F28335 floating point DSP is used. The main task of the floating point DSP is to generate the PWM signal for the gate drive circuits which operate the active switches of the different proposed PG power converters. The DSP output port is compatible with the gate drive input voltages and currents and hence, TMS320F28335 DSP does not require additional interfacing circuits. The measurement sensors are designed to have voltages and currents within the read range of the DSP. TMS320F28335 DSP support real-time monitoring and control by sending the data to addressed memory in the RAM and display it by Code Composer Studio V.3.3 software. One of the most important features of the TMS320F28335 DSP, that it can be programmed either by C, C++ coding or MATLAB/SIMULINK. The TMS320F28335 DSP has the following main features**:**

- High-Performance Static CMOS Technology
- High-Performance 32-Bit CPU
    - IEEE-754 Single-Precision Floating-Point Unit (FPU)
    - 150 MHz (6.67-ns Cycle Time)
    - Code-Efficient (in C/C++ and Assembly)
    - Fast Interrupt Response and Processing

- Memory
  - 256K data flash
  - 16K instruction cache
- 128-Bit Security Key/Lock
  - Protects Flash/OTP/RAM Blocks
  - Prevents Firmware Reverse Engineering
- Enhanced Control Peripherals
  - Up to 18 PWM Outputs
- Serial Port Peripherals
  - Up to 2 CAN Modules
  - One Inter-Integrated-Circuit (I2C) Bus
- Analogue to Digital Converters (ADC)
  - 12-Bit ADC, 16 Channels
  - 80-ns Conversion Rate
  - 2 x 8 Channel Input Multiplexer
  - Two Sample-and-Hold
  - Single/Simultaneous Conversions
  - Internal or External Reference
- Digital Inputs and Outputs
  - Up to 88 Individually Programmable, Multiplexed GPIO Pins With Input Filtering
- Emulation Features
  - Analysis and Breakpoint Functions
  - Real-Time Debug via Hardware
- Development Support Includes
  - ANSI C/C++ Compiler/Assembler/Linker
  - Code Composer Studio IDE
  - Digital Motor Control and Digital Power Software Libraries
- Temperature Options:
  - –40°C to 125°C

C.2 Voltage Sensors

Some of the proposed PGs required a sensor based voltage balancing algorithm. Therefore, a voltage sensor board is used, which measures one SM capacitor voltage, thus for N SMs N sensors are required, each of which feeds a measurement signal to the DSP's ADC module. Circuitry on the board scales the input voltage and adds a DC-bias to make the output voltage compatible with the ADC signal level. The sensor, LEM25-P, uses the Hall-effect to measure AC and DC signals. The LEM25-P sensor can measure up to 500V with high frequency bandwidth [90]. The circuit board is shown in Fig.C.1 and schematically in Fig.C.2.

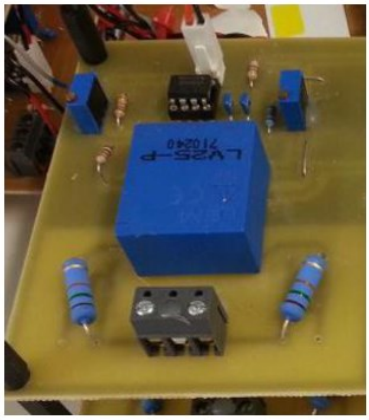

Fig.C.1. Voltage sensor board.

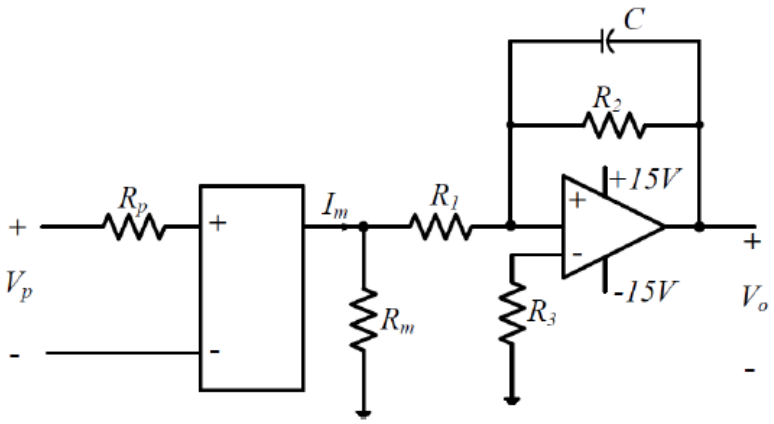

Fig.C.2. Voltage sensor signal conditioning circuit schematic

C.3 IGBTs Gate Drive Circuit

A dedicated gate drive circuit board, shown in Fig.C.3, is used to buffer the switching PWM of the IGBTs from the DSP. This is necessary as the DSP can only inject a few milli-amperes current which is not sufficient to turn on the IGBT switch. The gate drive circuit amplifies the output current of the DSP to reach the IGBT gate current. The gate drive circuit has suitable isolation which is necessary for galvanic isolation between the DSP ground and the common points of the IGBTs. This isolation allows short duration pulses to be transmitted to the switch. The parameters of the gate drive circuit are shown in Table C.1.

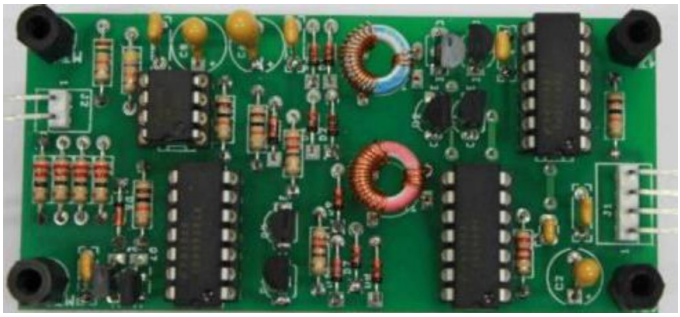

Fig.C.3. IGBT gate drive circuit board.

Table C.1: Specification for Gate Drive Circuit

Parameter	Value
Output voltage	0V, 15 V
Output current	±3 A
Supply voltage (max)	5 V
Measured signal frequency (max)	75 kHz
$t_{d\,on}$	60 ns
$t_{d\,off}$	60 ns

C.4 Estimating Transformer Leakage Inductance

The test was carried out using a nano-crystalline core based transformer. 10 primary turns are wound over a 10 turns secondary. Reference [91] details the used core information of the transformer. The secondary winding is short-circuited, while the primary is connected as shown in Fig.C.4. An IGBT is switched on for 6µs every 400µs, otherwise it is switched off. The primary current i_p and the primary voltage v_p are monitored in order to calculate the leakage inductance L_l. From the obtained results, shown in Fig.C.5, the estimated value of the leakage inductance is calculated as follows:

$$L_l = \frac{\Delta v_p \Delta t_p}{\Delta i_p} \tag{C.1}$$

Substituting for each value yields

$$L_l = \frac{19 \times 6 \times 10^{-6}}{32} = 3.56\ \mu\text{H} \tag{C.2}$$

In order to assess the obtained value, an estimate of the leakage inductance is calculated when the pulse voltage is 10kV, the pulse current is 10kA while the pulse duration is 2µs. This gives $L_l = 2\mu\text{H}$, so the transformer leakage inductance must be less than this.

Although, all the parasitics and the connection leads inductance are not considered in this test, the obtained value shows that transformer coupling is not viable for these short pulse durations.

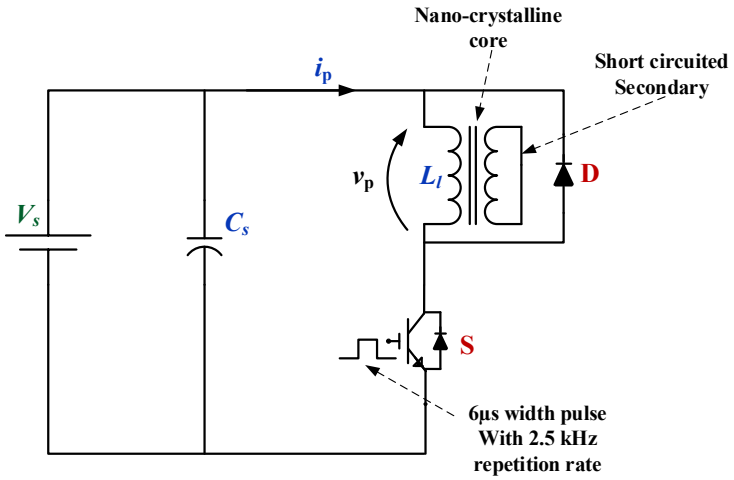

Fig.C.4. The circuit used to carry out the test.

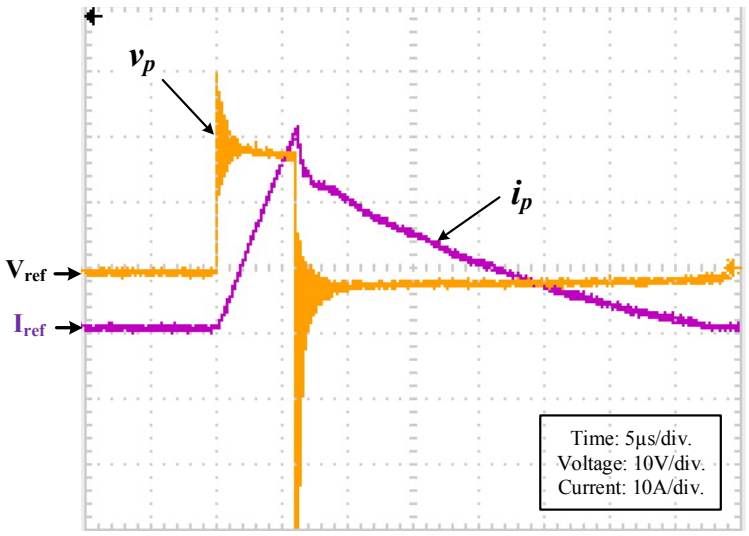

Fig.C.5. The monitored voltage and current.

C.5 Sample Software Codes for Simulation and Experimental Results

Each of the proposed nine PG topologies has a specific software algorithm to control the ON/OFF switching of the IGBTs in simulation and experimentation. For illustration, the software for the GPG, when generating a bipolar multilevel pulse waveform, is taken as an example.

C.5.1 Simulation Code for 10 SMs

```
%==============================
function [S1, S2, S3, S4] = fcn(clk, vc1, vc2,vc3, vc4)
% initiation;
%Ts= the repetation time(the full cycle).
%tp= the pulse width time as a percent of Ts , (the pulse duration).
%t= is the real time time.
%tx = is the fraction inside the pulse fraction.
N = 10;
S1 = ones(1,N);
S2 = ones(1,N);
S3 = ones(1,N);
S4 = ones(1,N);

[Vc1, J1] = sort(vc1);
[Vc2, J2] = sort(vc2);
[Vc3, J3] = sort(vc3);
[Vc4, J4] = sort(vc4);
%==========++++++++++============
if( (clk>=0) && (clk<1))
  S1 = ones(1,N);
  S2 = ones(1,N);
  S3(J3(10)) = 0;
  S4(J4(10)) = 0;
end
if( (clk>=1) && (clk<2))
```

```
  S1 = ones(1,N);
  S2 = ones(1,N);
  S3(J3(9:10)) = 0;
  S4(J4(9:10)) = 0;
end
if( (clk>=2) && (clk<3))
  S1 = ones(1,N);
  S2 = ones(1,N);
  S3(J3(8:10)) = 0;
  S4(J4(8:10)) = 0;
end
if( (clk>=3) && (clk<4))
  S1 = ones(1,N);
  S2 = ones(1,N);
  S3(J3(7:10)) = 0;
  S4(J4(7:10)) = 0;
end
if( (clk>=4) && (clk<5))
  S1 = ones(1,N);
  S2 = ones(1,N);
  S3(J3(6:10)) = 0;
  S4(J4(6:10)) = 0;
end
if( (clk>=5) && (clk<6))
  S1 = ones(1,N);
  S2 = ones(1,N);
  S3(J3(5:10)) = 0;
  S4(J4(5:10)) = 0;
end
if( (clk>=6) && (clk<7))
  S1 = ones(1,N);
  S2 = ones(1,N);
  S3(J3(4:10)) = 0;
  S4(J4(4:10)) = 0;
end
if( (clk>=7) && (clk<8))
  S1 = ones(1,N);
  S2 = ones(1,N);
  S3(J3(3:10)) = 0;
  S4(J4(3:10)) = 0;
end
if( (clk>=8) && (clk<9))
  S1 = ones(1,N);
  S2 = ones(1,N);
  S3(J3(2:10)) = 0;
  S4(J4(2:10)) = 0;
end

if( (clk>=9) && (clk<15))
  S1 = ones(1,N);
  S2 = ones(1,N);
  S3 = zeros(1,N);
  S4 = zeros(1,N);
end
if( (clk>=15) && (clk<16))
  S1 = ones(1,N);
  S2 = ones(1,N);
  S3(J3(2:10)) = 0;
  S4(J4(2:10)) = 0;
end
if( (clk>=16) && (clk<17))
  S1 = ones(1,N);
  S2 = ones(1,N);
  S3(J3(3:10)) = 0;
  S4(J4(3:10)) = 0;
```

```
end
if( (clk>=17) && (clk<18))
  S1 = ones(1,N);
  S2 = ones(1,N);
  S3(J3(4:10)) = 0;
  S4(J4(4:10)) = 0;
end
if( (clk>=18) && (clk<19))
  S1 = ones(1,N);
  S2 = ones(1,N);
  S3(J3(5:10)) = 0;
  S4(J4(5:10)) = 0;
end
if( (clk>=19) && (clk<20))
  S1 = ones(1,N);
  S2 = ones(1,N);
  S3(J3(6:10)) = 0;
  S4(J4(6:10)) = 0;
end
if( (clk>=20) && (clk<21))
  S1 = ones(1,N);
  S2 = ones(1,N);
  S3(J3(7:10)) = 0;
  S4(J4(7:10)) = 0;
end
if( (clk>=21) && (clk<22))
  S1 = ones(1,N);
  S2 = ones(1,N);
  S3(J3(8:10)) = 0;
  S4(J4(8:10)) = 0;
end
if( (clk>=22) && (clk<23))
  S1 = ones(1,N);
  S2 = ones(1,N);
  S3(J3(9:10)) = 0;
  S4(J4(9:10)) = 0;
end
if( (clk>=23) && (clk<24))
  S1 = ones(1,N);
  S2 = ones(1,N);
  S3(J3(10)) = 0;
  S4(J4(10)) = 0;
end
if( (clk>=(24)) && (clk<50))
  S1 = ones(1,N);
  S2 = zeros(1,N);
  S3 = ones(1,N);
  S4 = zeros(1,N);
end
%=============================
if( (clk>=50) && (clk<51))
  S1(J1(10)) = 0;
  S2(J2(10)) = 0;
  S3 = ones(1,N);
  S4 = ones(1,N);
end

if( (clk>=51) && (clk<52))
  S1(J1(9:10)) = 0;
  S2(J2(9:10)) = 0;
  S3 = ones(1,N);
  S4 = ones(1,N);
end
if( (clk>=52) && (clk<53))
  S1(J1(8:10)) = 0;
```

```
  S2(J2(8:10)) = 0;
  S3 = ones(1,N);
  S4 = ones(1,N);
end
if( (clk>=53) && (clk<54))
  S1(J1(7:10)) = 0;
  S2(J2(7:10)) = 0;
  S3 = ones(1,N);
  S4 = ones(1,N);
end
if( (clk>=54) && (clk<55))
  S1(J1(6:10)) = 0;
  S2(J2(6:10)) = 0;
  S3 = ones(1,N);
  S4 = ones(1,N);
end
if( (clk>=55) && (clk<56))
  S1(J1(5:10)) = 0;
  S2(J2(5:10)) = 0;
  S3 = ones(1,N);
  S4 = ones(1,N);
end
if( (clk>=56) && (clk<57))
  S1(J1(4:10)) = 0;
  S2(J2(4:10)) = 0;
  S3 = ones(1,N);
  S4 = ones(1,N);
end
if( (clk>=57) && (clk<58))
  S1(J1(3:10)) = 0;
  S2(J2(3:10)) = 0;
  S3 = ones(1,N);
  S4 = ones(1,N);
end
if( (clk>=58) && (clk<59))
  S1(J1(2:10)) = 0;
  S2(J2(2:10)) = 0;
  S3 = ones(1,N);
  S4 = ones(1,N);
end
if( (clk>=59) && (clk<65))
  S1 = zeros(1,N);
  S2 = zeros(1,N);
  S3 = ones(1,N);
  S4 = ones(1,N);
end
if( (clk>=65) && (clk<66))
  S1(J1(2:10)) = 0;
  S2(J2(2:10)) = 0;
  S3 = ones(1,N);
  S4 = ones(1,N);
end
if( (clk>=66) && (clk<67))
  S1(J1(3:10)) = 0;
  S2(J2(3:10)) = 0;
  S3 = ones(1,N);
  S4 = ones(1,N);
end
if( (clk>=67) && (clk<68))
  S1(J1(4:10)) = 0;
  S2(J2(4:10)) = 0;
  S3 = ones(1,N);
  S4 = ones(1,N);
end
if( (clk>=68) && (clk<69))
```

```
  S1(J1(5:10)) = 0;
  S2(J2(5:10)) = 0;
  S3 = ones(1,N);
  S4 = ones(1,N);
end
if( (clk>=69) && (clk<70))
  S1(J1(6:10)) = 0;
  S2(J2(6:10)) = 0;
  S3 = ones(1,N);
  S4 = ones(1,N);
end
if( (clk>=70) && (clk<71))
  S1(J1(7:10)) = 0;
  S2(J2(7:10)) = 0;
  S3 = ones(1,N);
  S4 = ones(1,N);
end
if( (clk>=71) && (clk<72))
  S1(J1(8:10)) = 0;
  S2(J2(8:10)) = 0;
  S3 = ones(1,N);
  S4 = ones(1,N);
end
if( (clk>=72) && (clk<73))
  S1(J1(9:10)) = 0;
  S2(J2(9:10)) = 0;
  S3 = ones(1,N);
  S4 = ones(1,N);
end
if( (clk>=73) && (clk<74))
  S1(J1(10)) = 0;
  S2(J2(10)) = 0;
  S3 = ones(1,N);
  S4 = ones(1,N);
end
if( (clk>=74) && (clk<100))
  S1 = zeros(1,N);
  S2 = ones(1,N);
  S3 = zeros(1,N);
  S4 = ones(1,N);
end
%==============================
```

C.5.2 Experimental Code for 3 SMs

```
%==============================
function [S1a, S1b, S1c, S2a, S2b, S2c, S3a, S3b, S3c, S4a, S4b, S4c] =
fcn(t, v1, v2, v3, v4, v5, v6, v7, v8, v9, v10, v11, v12)

% initiation;
%Ts= the repetation time(the full cycle).
%tp= the pulse width time as a percent of Ts , (the pulse duration).
%t= is the real time time.
%tx = is the fraction inside the pulse fraction, to allow semi-quasi square
%operation

%====Intializations=======
S1a = 0;
S1b = 0;
S1c = 0;
S2a = 0;
S2b = 0;
```

```
S2c = 0;
S3a = 0;
S3b = 0;
S3c = 0;
S4a = 0;
S4b = 0;
S4c = 0;

%====Positive Pulse=======
if (t>=1 && t<3)
   S1a = 1;
   S1b = 1;
   S1c = 1;
   S2a = 1;
   S2b = 1;
   S2c = 1;

if ((v7>=v8)&&(v7>=v9))
         S3a = 0; S3b = 1; S3c = 1;
elseif((v8>=v9)&&(v8>v7))
         S3a = 1; S3b = 0; S3c = 1;
elseif((v9>v8)&&(v9>v7))
         S3a = 1; S3b = 1; S3c = 0;
end

if ((v4>=v5)&&(v4>=v6))
         S4a = 0; S4b = 1; S4c = 1;
elseif((v5>=v6)&&(v5>v4))
         S4a = 1; S4b = 0; S4c = 1;
elseif((v6>v5)&&(v6>v4))
         S4a = 1; S4b = 1; S4c = 0;
end
end

if (t>=3 && t<5)
   S1a = 1;
   S1b = 1;
   S1c = 1;
   S2a = 1;
   S2b = 1;
   S2c = 1;

if (S3a==0)&&(v8>=v9)
          S3a = 0; S3b = 0; S3c = 1;
elseif(S3a==0)&&(v9>v8)
          S3a = 0; S3b = 1; S3c = 0;
end
if (S3b==0)&&(v7>=v9)
          S3a = 0; S3b = 0; S3c = 1;
elseif(S3b==0)&&(v9>v7)
          S3a = 1; S3b = 0; S3c = 0;
end
if (S3c==0)&&(v7>=v8)
          S3a = 0; S3b = 1; S3c = 0;
elseif(S3c==0)&&(v8>v7)
          S3a = 1; S3b = 0; S3c = 0;
end

if (S4a==0)&&(v5>=v6)
          S4a = 0; S4b = 0; S4c = 1;
elseif(S4a==0)&&(v6>v5)
          S4a = 0; S4b = 1; S4c = 0;
end
if (S4b==0)&&(v4>=v6)
          S4a = 0; S4b = 0; S4c = 1;
```

```
elseif(S4b==0)&&(v6>v4)
          S4a = 1; S4b = 0; S4c = 0;
end
if (S4c==0)&&(v4>=v5)
          S4a = 0; S4b = 1; S4c = 0;
elseif(S4c==0)&&(v5>v4)
          S4a = 1; S4b = 0; S4c = 0;
end
end

if (t>=5 && t<7)
   S1a = 1;
   S1b = 1;
   S1c = 1;
   S2a = 1;
   S2b = 1;
   S2c = 1;
   S3a = 0;
   S3b = 0;
   S3c = 0;
   S4a = 0;
   S4b = 0;
   S4c = 0;
end

if (t>=7 && t<9)
   S1a = 1;
   S1b = 1;
   S1c = 1;
   S2a = 1;
   S2b = 1;
   S2c = 1;

if (S3a==0)&&(v8>=v9)
          S3a = 0; S3b = 0; S3c = 1;
elseif(S3a==0)&&(v9>v8)
          S3a = 0; S3b = 1; S3c = 0;
end
if (S3b==0)&&(v7>=v9)
          S3a = 0; S3b = 0; S3c = 1;
elseif(S3b==0)&&(v9>v7)
          S3a = 1; S3b = 0; S3c = 0;
end
if (S3c==0)&&(v7>=v8)
          S3a = 0; S3b = 1; S3c = 0;
elseif(S3c==0)&&(v8>v7)
          S3a = 1; S3b = 0; S3c = 0;
end

if (S4a==0)&&(v5>=v6)
          S4a = 0; S4b = 0; S4c = 1;
elseif(S4a==0)&&(v6>v5)
          S4a = 0; S4b = 1; S4c = 0;
end
if (S4b==0)&&(v4>=v6)
          S4a = 0; S4b = 0; S4c = 1;
elseif(S4b==0)&&(v6>v4)
          S4a = 1; S4b = 0; S4c = 0;
end
if (S4c==0)&&(v4>=v5)
          S4a = 0; S4b = 1; S4c = 0;
elseif(S4c==0)&&(v5>v4)
          S4a = 1; S4b = 0; S4c = 0;
end
end
```

```
if (t>=9 && t<11)
   S1a = 1;
   S1b = 1;
   S1c = 1;
   S2a = 1;
   S2b = 1;
   S2c = 1;

if ((v7>=v8)&&(v7>=v9))
         S3a = 0; S3b = 1; S3c = 1;
elseif((v8>=v9)&&(v8>v7))
         S3a = 1; S3b = 0; S3c = 1;
elseif((v9>v8)&&(v9>v7))
         S3a = 1; S3b = 1; S3c = 0;
end

if ((v4>=v5)&&(v4>=v6))
         S4a = 0; S4b = 1; S4c = 1;
elseif((v5>=v6)&&(v5>v4))
         S4a = 1; S4b = 0; S4c = 1;
elseif((v6>v5)&&(v6>v4))
         S4a = 1; S4b = 1; S4c = 0;
end
end


%====Negative Pulse=======

if (t>=11 && t<13)
   S3a = 1;
   S3b = 1;
   S3c = 1;
   S4a = 1;
   S4b = 1;
   S4c = 1;

if ((v1>=v2)&&(v1>=v3))
         S1a = 0; S1b = 1; S1c = 1;
elseif((v2>=v3)&&(v2>v1))
         S1a = 1; S1b = 0; S1c = 1;
elseif((v3>v2)&&(v3>v1))
         S1a = 1; S1b = 1; S1c = 0;
end

if ((v10>=v11)&&(v10>=v12))
         S2a = 0; S2b = 1; S2c = 1;
elseif((v11>=v12)&&(v11>v10))
         S2a = 1; S2b = 0; S2c = 1;
elseif((v12>v11)&&(v12>v10))
         S2a = 1; S2b = 1; S2c = 0;
end
end

if (t>=13 && t<15)
   S3a = 1;
   S3b = 1;
   S3c = 1;
   S4a = 1;
   S4b = 1;
   S4c = 1;

if (S1a==0)&&(v2>=v3)
          S1a = 0; S1b = 0; S1c = 1;
elseif(S1a==0)&&(v3>v2)
```

```
          S1a = 0; S1b = 1; S1c = 0;
end
if (S1b==0)&&(v1>=v3)
          S1a = 0; S1b = 0; S1c = 1;
elseif(S1b==0)&&(v3>v1)
          S1a = 1; S1b = 0; S1c = 0;
end
if (S1c==0)&&(v1>=v2)
          S1a = 0; S1b = 1; S1c = 0;
elseif(S1c==0)&&(v2>v1)
          S1a = 1; S1b = 0; S1c = 0;
end

if (S2a==0)&&(v11>=v12)
          S2a = 0; S2b = 0; S2c = 1;
elseif(S2a==0)&&(v12>v11)
          S2a = 0; S2b = 1; S2c = 0;
end
if (S2b==0)&&(v10>=v12)
          S2a = 0; S2b = 0; S2c = 1;
elseif(S2b==0)&&(v12>v10)
          S2a = 1; S2b = 0; S2c = 0;
end
if (S2c==0)&&(v10>=v11)
          S2a = 0; S2b = 1; S2c = 0;
elseif(S2c==0)&&(v11>v10)
          S2a = 1; S2b = 0; S2c = 0;
end
end

if (t>=15 && t<17)
   S1a = 0;
   S1b = 0;
   S1c = 0;
   S2a = 0;
   S2b = 0;
   S2c = 0;
   S3a = 1;
   S3b = 1;
   S3c = 1;
   S4a = 1;
   S4b = 1;
   S4c = 1;
end

if (t>=17 && t<19)
   S3a = 1;
   S3b = 1;
   S3c = 1;
   S4a = 1;
   S4b = 1;
   S4c = 1;

if (S1a==0)&&(v2>=v3)
          S1a = 0; S1b = 0; S1c = 1;
elseif(S1a==0)&&(v3>v2)
          S1a = 0; S1b = 1; S1c = 0;
end
if (S1b==0)&&(v1>=v3)
          S1a = 0; S1b = 0; S1c = 1;
elseif(S1b==0)&&(v3>v1)
          S1a = 1; S1b = 0; S1c = 0;
end
if (S1c==0)&&(v1>=v2)
          S1a = 0; S1b = 1; S1c = 0;
```

```
elseif(S1c==0)&&(v2>v1)
          S1a = 1; S1b = 0; S1c = 0;
end

if (S2a==0)&&(v11>=v12)
          S2a = 0; S2b = 0; S2c = 1;
elseif(S2a==0)&&(v12>v11)
          S2a = 0; S2b = 1; S2c = 0;
end
if (S2b==0)&&(v10>=v12)
          S2a = 0; S2b = 0; S2c = 1;
elseif(S2b==0)&&(v12>v10)
          S2a = 1; S2b = 0; S2c = 0;
end
if (S2c==0)&&(v10>=v11)
          S2a = 0; S2b = 1; S2c = 0;
elseif(S2c==0)&&(v11>v10)
          S2a = 1; S2b = 0; S2c = 0;
end
end

if (t>=19 && t<21)
   S3a = 1;
   S3b = 1;
   S3c = 1;
   S4a = 1;
   S4b = 1;
   S4c = 1;
if ((v1>=v2)&&(v1>=v3))
         S1a = 0; S1b = 1; S1c = 1;
elseif((v2>=v3)&&(v2>v1))
         S1a = 1; S1b = 0; S1c = 1;
elseif((v3>v2)&&(v3>v1))
         S1a = 1; S1b = 1; S1c = 0;
end

if ((v10>=v11)&&(v10>=v12))
         S2a = 0; S2b = 1; S2c = 1;
elseif((v11>=v12)&&(v11>v10))
         S2a = 1; S2b = 0; S2c = 1;
elseif((v12>v11)&&(v12>v10))
         S2a = 1; S2b = 1; S2c = 0;
end
end
%====charging lower legs=======
if (t>=21 && t<35)
   S1a = 1;
   S1b = 1;
   S1c = 1;
   S2a = 0;
   S2b = 0;
   S2c = 0;
   S3a = 1;
   S3b = 1;
   S3c = 1;
   S4a = 0;
   S4b = 0;
   S4c = 0;
end
%====charging upper legs=======
if (t>=35 && t<50)
   S1a = 0;
   S1b = 0;
   S1c = 0;
   S2a = 1;
```

```
    S2b = 1;
    S2c = 1;
    S3a = 0;
    S3b = 0;
    S3c = 0;
    S4a = 1;
    S4b = 1;
    S4c = 1;
end
%====Code Ends here=======
```

Appendix D

List of Figures and Tables

This appendix summarises the list of figures and tables presented within the thesis.

D.1 List of Figures

D.2 List of Tables

Appendix E

Author's PG Publications

This appendix summarises the author's accepted and under-review PG publications. For the full list of the author's other publications, please refer to the following google scholar profile: https://scholar.google.co.uk/citations?user=12Kd474AAAAJ&hl=en

E.1 IEEE Transaction Papers in print

[1] M. A. Elgenedy, A. Darwish, S. Ahmed and B. W. Williams, "A Modular Multilevel-Based High-Voltage Pulse Generator for Water Disinfection Applications," in *IEEE Transactions on Plasma Science*, vol. 44, no. 11, pp. 2893-2900, Nov. 2016. doi: 10.1109/TPS.2016.2610462.

Abstract—The role of irreversible electroporation using pulsed electric field (PEF) is to generate high voltage (HV) pulses with a predefined magnitude and duration. These HV pulses are applied to the treatment chamber until decontamination of the sample is completed. In this paper, a new topology for HV rectangular pulse generation for water disinfection applications is introduced. The proposed topology has four arms comprised of series connected half H-bridge modular multilevel converter cells. The rectangular pulse characteristics can be controlled via a software controller without any physical changes in power topology. The converter is capable of generating both bipolar and monopolar HV pulses with micro-second pulse durations at a high frequency rate with different characteristics. Hence, the proposed topology provides flexibility by software control, along with hardware modularity, scalability, and redundancy. Moreover, a cell's capacitance is relatively small which drastically reduces the converter footprint. The adopted charging and discharging process of the cell capacitors in this topology eliminate the need of any voltage measurements or complex control for cell-capacitors voltage balance. Consequently, continuity of converter operation is assured under cell malfunction. In this paper, analysis and cell-capacitor sizing of the proposed topology are detailed. Converter operation is verified using MATLAB/Simulink simulation and scaled experimentation.

[2] M. A. Elgenedy, A. Darwish, S. Ahmed, B. W. Williams, "A Transition Arm Modular Multilevel Universal Pulse-Waveform Generator for Electroporation Applications," in *IEEE Transactions on Power Electronics*, vol.32, no.12, pp. 8979-8991, 2017. doi: 10.1109/TPEL.2017.2653243.

Abstract – High voltage (HV) pulses are used in electroporation to subject pulsed electric field (PEF) onto a sample under treatment. Pulse-waveform shape, voltage magnitude, pulse duration, and pulse repetition rate are the basic controllable variables required for particular PEF application. In practice, a custom-made pulse generator is dedicated for each PEF application with limited flexibility in changing these variables. In this paper, a universal pulse-waveform generator (UPG) is proposed, where the controller software-algorithm can manipulate a basic generated multilevel pulse-waveform to emulate many different PEF pulse-waveforms. The commonly used PEF HV pulse-waveforms can be generated as bipolar or monopolar with a controllable pulse duration, repetition time, and voltage magnitude. The UPG has the ability to generate multilevel pulses that have controllable dv/dt which allow reduction of the electromagnetic interference (EMI) generated by the converter. The UPG topology is based on half-bridge modular multilevel converter (HB-MMC) cells forming two transition arms in conjunction with two bi-state arms, together creating an H-bridge. The HB-MMC cell-capacitors provide a controllable energy source which charges from the dc input supply and discharge across the load, while the two bi-state arms allow charging the HB-MMC cell-capacitors. Hence, the UPG topology offers modularity, redundancy, and scalability. The HB-MMC cell-capacitance is low and the cell-voltages are balanced by employing the sorting and rotating algorithm used in conventional HB-MMC topologies for HVDC transmission applications. The viability of the proposed UPG converter is validated by MATLAB/Simulink simulation and scaled-down experimentation.

[3] M. A. Elgenedy, A. Darwish, S. Ahmed, B. W. Williams, "A Modular Multilevel Generic Pulse-Waveform Generator for Pulsed Electric Field Applications," in *IEEE Transactions on Plasma Science* , vol. 45, no. 9, pp. 2527-2535, 2017. doi: 10.1109/TPS.2017.2727068.

Abstract— High voltage (HV) pulses are used in pulsed electric field (PEF) applications to provide an effective electroporation process, a process in which harmful microorganisms are disinfected when subjected to a PEF. Depending on the PEF application, different HV pulse specifications are required such as: the pulse-waveform shape, the voltage magnitude, the pulse duration, and the pulse repetition rate. In this paper, a generic pulse-waveform generator (GPG) is proposed, the GPG topology is based on half-bridge modular multilevel converter (HB-MMC) cells. The GPG topology is formed of four identical arms of series connected HB-MMC cells forming an H-bridge. Unlike the conventional HB-MMC based converters in HVDC transmission, the GPG load power flow is not continuous which leads to smaller size cell capacitors utilization, hence smaller

footprint of the GPG is achieved. The GPG topology flexibility allows the controller software to generate a basic multilevel waveform which can be manipulated to generate the commonly used PEF pulse-wave forms. Therefore, the proposed topology offers modularity, redundancy and scalability. The viability of the proposed GPG converter is validated by MATLAB/Simulink simulation and experimentation.

[4] I. Abdelsalam, M. A. Elgenedy, S. Ahmed, B. W. Williams, "Full-Bridge Modular Multilevel Sub-Module Based High-Voltage Bipolar Pulse Generator With Low Voltage DC Input for Pulsed Electric Field Applications" in *IEEE Transactions on Plasma Science* , vol. 45, no. 10, pp. 2857-2864, 2017. doi: 10.1109/TPS.2017.2743822.

Abstract-High voltage (HV) pulse generators (PGs) are the core of pulsed electric field applications. Applying HV pulses produces electrical pores in a biological cell membrane, in which if the size of the pores increases beyond a critical size, the cell will not survive. This paper proposes a new HV-PG, based on the modular multilevel converter with full-bridge sub-modules (FB-SMs). In order to alleviate the need of complicated sensorless or sensor based voltage balancing techniques for the FB-SM capacitors, a dedicated self-regulating charging circuit is connected across each FB-SM capacitor. The individual capacitor charging voltage-level is obtained from three successive stages namely: convert the low-voltage DC input voltage to a high-frequency square AC voltage; increase the AC voltage-level via a nano-crystalline step-up transformer; and rectify the secondary transformer AC voltage via a diode full-bridge rectifier. The HV bipolar pulses are formed across the load in a fourth stage through series connected FB-SMs. The flexibility of inserting and bypassing the FB-SM capacitors, allows the proposed topology to generate different pulse-waveform shapes, including rectangular waveforms with specifically reduced dv/dt and ramp pulses. The practical results, from a scaled down experimental rig with five FB-SMs and a 1kV peak to peak pulse output, validate the proposed topology.

[5] M. A. Elgenedy, A. M. Massoud, S. Ahmed, and B. W. Williams, "A high-gain, high-voltage pulse generator using sequentially-charged modular multilevel converter sub-modules, for water disinfection applications,"*IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. PP, no. 99, pp. 1-1, 2017.

Abstract– Modularity, redundancy and scalability are the key features recently sought in High-Voltage (HV) pulse generators for electroporation applications. Such features are gained by utilizing Modular Multilevel Converter (MMC) Sub-Modules (SMs). In this paper, two arms of MMC Half-Bridge SMs (HB-SMs) are utilised for generating bipolar/unipolar HV pulses for disinfection process in water treatment applications. The HB-SM capacitors are charged sequentially from a low voltage

dc input source via a resistive-inductive branch and a reverse blocking switch (which is turned ON/OFF at zero voltage/current conditions). The energy losses of the proposed capacitor charging technique are established mathematically as well as the charging time per SM-capacitor. Therefore, the proposed Sequential Pulse Generator (SPG) is able to generate high repetitive pulse rates with high efficiency regardless the HV level of the pulse. Different characterizations of bipolar rectangular pulses can be generated. The proposed topology is assessed by Matlab/Simulink platform and scaled down experimentation. The results establish the viability of the SPG topology for HV pulse generation for water disinfection applications.

[6] A. Darwish, M. A. Elgenedy, S. J. Finney, B. W. Williams, and J. R. McDonald, "A Step-Up Modular High-Voltage Pulse Generator Based on Isolated Input-Parallel/Output-Series Voltage-Boosting Modules and Modular Multilevel Sub-modules," in *IEEE Transactions on Industrial Electronics*, vol. PP, no. 99, pp. 1-1, 2017.

Abstract— Irreversible electroporation for disinfection applications involve exposing the specimen cell-membrane to a pulsed electric field in order to kill harmful microorganisms. High voltage (HV) pulses, of relatively short durations in range of few micro-seconds, are generated across the sample chamber. The HV pulse specifications such as: voltage magnitude, waveform, repetition rate, and duration differ according to the conditions of the sample being processed. This paper proposes a new step-up power electronic converter topology for generating the required HV pulses from a relatively low input voltage. The converter consists of two main stages; the first stage is responsible for boosting the input voltage to the desired level using input-parallel/output-series connected dc/dc modules while the second stage forms the required HV pulses with the proper magnitude, duration and repetition rate using modular multilevel converter sub-modules. The proposed topology is able to produce the HV pulses with controlled voltage and current stresses across the employed semiconductor switches and diodes, hence, it can be implemented with the market-available semiconductor technology. Mathematical analysis of the proposed topology is developed and MATLAB/Simulink simulation results explore operational conditions. Experimental results from a scaled-down prototype validate the functionality of the proposed system.

E.2 IEEE Transaction Papers Under-review

[7] M. A. Elgenedy, A. Darwish, S. Ahmed, and B. W. Williams, "A New High Voltage Pulse Generator Based on Sequentially Charged Modular Multilevel Converter Sub modules Operating in a Voltage Boost Mode," *Submitted for review in IEEE Transactions on Plasma Science.*

Abstract—This paper presents a high-voltage (HV) pulse generator (PG). The proposed topology is based on modular multilevel converter (MMC) sub modules (SMs) charged sequentially in a voltage boost mode, such that each SM acts as a boost converter during the SM-capacitor charging process. In contrast, during the discharging process the SM capacitors are connected in series forming a HV pulse across the load. The proposed charging method allows a reduction in the converter footprint in comparison with recently proposed MMC sequentially charged PG topologies. Flexible pulse generation is obtained which promotes the proposed PG for use in a wide range of pulse power applications. The viability of the proposed converter is validated by MATLAB/Simulink simulation and a proof of concept experimentation.

[8] M. A. Elgenedy, A. M. Massoud, D. Holliday, S. Ahmed and B. Williams, "A Voltage-Boosting Modular Multilevel High-Voltage Pulse Generator," ***Submitted for review in IEEE Transactions on Power Electronics.***

Abstract— This paper presents a new High-Voltage (HV) Pulse Generator (PG) for electroporation application, which requires HV pulses to create a high electric field across the subject. A controllable low-voltage input boost converter supplies via directing/blocking diodes, two arms of a series Half-Bridge Sub-Module (HB-SM) Modular Multilevel Converter (MMC). At start the boost converter charges two SM capacitors, one SM capacitor per arm, simultaneously, to the desired voltage level, and progressively via directing diodes, all the arms SM capacitors are charged sequentially. Then, for continuous operation, the SM-capacitors are re-charged sequentially in parallel, after each pulse delivery, to the desired voltage level. The boost converter duty ratio is controlled by measuring the SM capacitor voltage at the boost converter reference level. Due to the proposed SMs structure and the utilization of directing/blocking diodes, each SM capacitor is controlled individually without requiring a voltage sensor across each SM capacitor. Generation of the commonly used pulse waveforms in electroporation applications is possible, whilst assuring balanced capacitor voltages. The proposed PG can utilise a boost converter at its source input, or a buck-boost converter, when ramping the input charging voltage. The proposed PG topology is assessed by simulation, and experimentation explores its viability for electroporation applications.

E.3 Accepted International/National Conference Papers

[9] M. A. Elgenedy, A. M. Massoud, D. Holliday, S. Ahmed and B. Williams, "Low-voltage DC input, high-voltage pulse generator using nano-crystalline transformer and sequentially charged mmc sub-modules, for water treatment applications" in Proc. IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, Ohio, 2017, pp. 2144-2149.

Abstract— This paper proposes a new high-voltage Pulse Generator (PG), fed from low voltage dc supplyV_s. This input supply voltage is utilised to charge two arms of N series-connected modular multilevel converter sub-module capacitors sequentially through a resistive-inductive branch, such that each arm is charged to NV_s. With a step-up nano-crystalline transformer of n turns ratio, the proposed PG is able to generate bipolar rectangular pulses of peak $\pm nNV_s$, at high repetition rates. However, equal voltage-second area of consecutive pulse pair polarities should be assured to avoid transformer saturation. Not only symmetrical pulses can be generated, but also asymmetrical pulses with equal voltage-second areas are possible. The proposed topology is tested via simulations and a scaled-down experimentation, which establish the viability of the topology for water treatment applications.

[10] M. A. Elgenedy, A. M. Massoud, D. Holliday, S. Ahmed and B. Williams, "High-Voltage Pulse Generator Using Sequentially Charged Full-Bridge Modular Multilevel Converter Sub-Modules for Water Treatment Applications" accepted for publication in PEMD Liverpool, UK, 2018.

Abstract–This paper proposes a new high-voltage Pulse Generator (PG), fed from a low voltage dc supply V_s, which charges one arm of N series-connected Full-Bridge (FB) Modular Multilevel Converter (MMC) Sub-Module (SM) capacitors sequentially, through a resistive-inductive branch. By utilizing FB-SMs, the proposed PG is able to generate bipolar rectangular pulses of peak NV_s and unipolar rectangular pulses of either polarity, at high repetition rates. Asymmetrical pulses are also possible. The proposed topology is assessed via simulation and scaled-down experimentation, which establish the viability of the topology for water treatment applications.