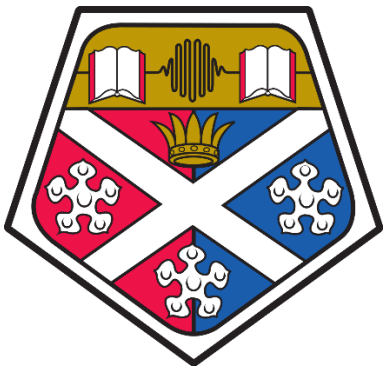

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Power converter controlled as a synchronous machine with fault ride through capability

by

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B.Sc. (*honors*), M.Sc.

A thesis presented in fulfilment of the requirements for the degree of Doctor of Philosophy

2022

To my family

Declaration

This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of any degree.

Signed: *A. Abdelrahim* Date: 24/09/2022

Acknowledgment

A special thanks to my first supervisor Dr. Agustí Egea-Àlvarez for his tremendous help all along my PhD journey, and for his unique contributions, and for his honest guidance in my academic career. Also, special thanks to my second supervisor Dr. Khaled H. Ahmed for helping me getting this PhD opportunity, and for his guidance, support, and great contributions. I am also thankful to my industrial supervisor Dr. Michael Smailes for his contributions, and for providing all the required help to elevate the quality of the thesis.

I am greatly thankful to my dear colleagues Dr. Mohamed Elgenedy, Dr. Ali Abdelaziz, and Dr. Mohamed Saeed for their emotional support during the full time of my study.

I also like to express my deepest gratitude to my wife who gave me all the emotional support that I needed, and for helping me with all the means she had, and for having our cute new-born baby girl.

I am also very thankful to my father for his continuous emotional and financial support, and I wish to be the same caring and loving man he is. I am also very grateful to my late mother may she rest in peace.

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Abstract

Climate change has forced the world to move towards greater use of green energy. This shift is likely to result in a significant increase in renewable energy penetration, which will be reflected in the future of the electrical grids. However, this increased penetration causes operational challenges, such as decrease in system inertia and emergence of weak grids. Grid-forming converters are a promising solution for enhancing the stability of electrical networks; further, these converters address the operational challenges due to renewable energy penetration. This thesis is focused on virtual synchronous machines (VSMs), which are a particular type of grid-forming converters that are implemented without an inner current control (CC) loop. This VSM implementation can provide better inertial response than other grid-forming structures with an inner CC. However, it cannot limit the current through the converter during a fault. Therefore, different grid-forming implementations are reviewed in this thesis. Subsequently, a review of the FRT techniques for different strategies discussed in the literature is provided, followed by a discussion on the basic VSM structure and multiple FRT strategies with regard to their limitations and requirements. Thus, a standard solution that uses VSM as the primary controller with a conventional inner CC acting as a backup controller during fault conditions is established, which is referred to as a dual VSM control structure. The switching action between the primary and backup controllers is dependent on an accurate fault detection algorithm (FDA). Meanwhile, the conventional FDA reported in the literature has limitations in some scenarios. Thus, the limitations of the conventional FDA in weak grids and unbalanced conditions are discussed, and a new FDA with improved performance is proposed. Two types of sensitivity analysis are conducted to study the dynamics of the proposed control approach. The first analysis investigates the sensitivity of the proposed control structure to different fault locations in strong and weak grids, whereas the second analysis investigates the sensitivity of the controller response to changing controller parameters. The second analysis is introduced as a reference for tuning and improving the proposed control structure. Further, the synchronization loop within the backup controller is studied, and common synchronization techniques are compared, including

a new synchronization technique. Finally, the comparison shows the recommendations for the synchronization techniques, which can support the stable behaviour of the backup control with maximum reactive current injection during faults.

List of Symbols

ω	Grid Frequency
$\alpha\beta$	The components representing the three phase vectors after applying Clark's transformation
dq	The components representing the three phase vectors after applying Park's transformation
$V_{c_{abc}}$	The three phase converter voltage
$I_{c_{abc}}$	The converter current output
R_c	The converter filter resistance
L_c	The converter filter Inductance
U_{abc}	The voltage measured at the PCC
θ	The angle used to synchronise the dq components with the abc components
v_{c_q}	The voltage component shifted from the Phase a voltage by θ
v_{c_d}	The voltage component shifted from the V_q component by -90
i_{c_q}	The current component used to control the active power

i_{c_d}	The current component used to control the reactive power
u_q	The q component of the PCC voltage
u_d	The d component of the PCC voltage
T	The matrix used to transform from the abc frame to the dq frame
$G_{CC}(s)$	The PI controller of the current controller
i_d^*	Reference current for the d current component to control active power
i_q^*	Reference current for the q current component to control reactive power
k_{p-CC}	The proportional gain of the $G_{cc}(s)$ controller
k_{i-CC}	The integral gain of the $G_{cc}(s)$ controller
τ_{CC}	The time constant of the $G_{cc}(s)$ controller
S	The complex power of the converter output
P	The active power of the converter output
Q	The reactive power of the converter output
$\tilde{v}_c$	The complex form of the converter voltage
$\bar{\imath}_c$	The complex form conjugate of the converter current output

E_{grid}	The voltage representing the grid Thevenin equivalent voltage
X_c	The converter filter reactance
X_n	The reactance representing the impedance of the grid Thevenin equivalent
L_n	The inductance of the Thevenin equivalent grid impedance divided by the grid frequency
$\|V\|_c$	The magnitude converter voltage
$\|E\|_{grid}$	The magnitude of the grid voltage
δ	The difference between the angle of the voltage V_c and the angle of the voltage U
ω_{PLL}	The angular frequency measured by the PLL in rad./s
δ_{PLL}	The output angle of the PLL
$G_{PLL}(s)$	The PI controller of the PLL controller
τ_{PLL}	The time constant of the PLL PI controller
k_{p-PLL}	The proportional gain of the $G_{PLL}(s)$ controller
u_{fb}	The PLL feedback voltage
θ_g	The angle of the grid voltage
δ_{PLL_0}	The linearization point of the PLL angle

$\Delta\delta_{PLL}$	The difference between the PLL angle and the linearized PLL angle
ω_n	Natural frequency of the closed loop characteristic equation
ζ	Damping factor of the closed loop characteristic equation
θ_c	The angle of the converter voltage
$SCR_{1\rightarrow6}$	Different SCR from low to high
P^*	Reference active power
Q^*	Reference reactive power
i_{dq}^*	dq current components references
$\lvert i_{dq}^* \rvert$	Magnitude of dq current components references
ω_{droop}	The output angular frequency of the grid forming droop controller
θ_{droop}	The output angle of the grid forming droop controller
ω^*	Reference angular frequency
v^*	Reference Voltage
Dp	Droop coefficient of the active power control
Dq	Droop coefficient of the voltage control
$\lvert I \rvert_{c-max}$	The maximum threshold converter current based on the converter ratings

J	Virtual moment of inertia
D	Virtual friction and Damping constant
i_{ds}	The d component of the stator current
i_{qs}	The q component of the stator current
τ_r	The ratio between the rotor inductance and resistance to obtain the slip dynamics
T_e	Virtual electrical torque equation
T_L	Virtual load torque equation
ω_s	Synchronous frequency
ω_r	Rotor frequency
ω_{slip}	Slip frequency
θ_s	Synchronous angle
z	Zeros of the impedance function
p	Poles of the impedance function
k_1	Gain for the filter emulating the current component slip
k_2	Gain representing the relation between the torque and the current squared

V_{DC}	DC bus voltage
i_c^*	Converter current reference
R_s	Synchronous machine stator resistance
L_s	Synchronous machine stator inductance
T_d	Damping torque
T_m	Mechanical torque reference
P_e	Electrical power
e	Three phase voltage based on the angle output from VISMA mechanical part
ω_n	Natural frequency
$M_f i_f$	Excitation field
K	Reactive power gain to calculate the excitation field
$\omega^* t$	Constant angle for regulating the synchronverter angle
E_f	The voltage output of the AVR model
P_m	Mechanical power
Z_c	Converter filter impedance
H	Inertia constant

R_v	Virtual Resistance
L_v	Virtual Inductance
$G_Q(s)$	Reactive power controller
J_q	Moment of inertia of the reactive power loop
D_q	Damping of the reactive power loop
P_f^*	Active power reference in fault condition
Q_f^*	Reactive power reference in fault condition
V_f	Voltage in fault condition
ω_f	Frequency in a fault condition
V_r	Regulating voltage
$\|U\|$	Magnitude of the PCC voltage
ω_P	Frequency output of the active power loop
δ_P	Angle output of the active power loop
$G_P(s)$	Active power loop PI controller
$G_V(s)$	Voltage loop PI controller
$V_{c\,dq}$	Output dq voltage components

k_{p-P}	Active power controller proportional gain
k_{i-P}	Active power controller integral gain
S_{rated}	Converter rated complex power
ω_{n_1}	The natural frequency of the closed loop transfer function of the swing equation
ζ_1	The damping coefficient of the closed loop transfer function of the swing equation
ω_{n_2}	The natural frequency of the closed loop transfer function of the PI controller
ζ_2	The damping coefficient of the closed loop transfer function of the PI controller
k_{i-V}	The integral gain of the voltage controller
k_{p-V}	The proportional gain of the voltage controller
k_{p-Q}	The proportional gain of the reactive power controller
k_{i-Q}	The integral gain of the reactive power controller
$\|S\|$	Magnitude of the complex power
$\|I\|_{cal}$	Calculated current magnitude
$\|S\|_{new}$	New magnitude of complex power based on the maximum current

P_{new}	Active Power new calculated value
Q_{new}	Reactive Power new calculated value
Z_f	Equivalent fault impedance
R_f	Fault resistance
θ_z	Impedance angle
Y_v	Virtual admittance
$G_I(s)$	PI controller for controlling current through a single component (q only)
k_{p-I}	The proportional gain of the $G_I(s)$ controller
k_{i-I}	The integral gain of the $G_I(s)$ controller
$\|I\|_c$	Magnitude of the converter current
$G_f(s)$	Transfer function of a first order filter
$G_{nf}(s)$	Transfer function of a notch filter
u_{dq}^{+}	Positive sequence of PCC voltage dq components
u_q^{+}	Positive sequence of PCC voltage q component
u_d^{+}	Positive sequence of PCC voltage d component
u_{dq}^{-}	Negative sequence of PCC voltage dq components

u_q^-	Negative sequence of PCC voltage q component
u_d^-	Negative sequence of PCC voltage d component
$i_{c_{dq}}^+$	Positive sequence of converter current dq components
$i_{c_q}^+$	Positive sequence of converter current q component
$i_{c_d}^+$	Positive sequence of converter current d component
$i_{c_{dq}}^-$	Negative sequence of converter current dq components
$i_{c_q}^-$	Negative sequence of converter current q component
$i_{c_d}^-$	Negative sequence of converter current d component
$v_{c_q}^+$	Positive sequence of the converter voltage q component
$v_{c_d}^+$	Positive sequence of the converter voltage d component
$v_{c_q}^-$	Negative sequence of the converter voltage q component
$v_{c_d}^-$	Negative sequence of the converter voltage d component
i_q^{+*}	The reference of the q component positive sequence current
i_d^{+*}	The reference of the d component positive sequence current
i_q^{-*}	The reference of the q component negative sequence current
i_d^{-*}	The reference of the d component negative sequence current

Tr signal	Transition signal used to switch between controllers
ω_{nf}	Centre frequency of the notch filter
Q_{nf}	Quality factor of the notch
k_{i-PLL}	The PLL integral gain
$\|U\|_{min}$	The minimum acceptable PCC voltage
τ_f	First order filter time constant
$\|U\|^+$	The positive sequence of the magnitude of the PCC voltage
$\|I\|_c^+$	The positive sequence of the magnitude of the converter output current
ω_c	The bump-less transfer output frequency
$G_{fv}(s)$	First order filter of the voltage signal
$\|U\|^{-/+}$	The PCC voltage magnitude from the negative sequence frame to the positive sequence frame
τ_{fv}	The time constant of the first order filter applied to the voltage signal
$\|U\|_{rated}$	The magnitude of the rated PCC voltage
$G_{OP}(s)$	Active power outer control loop
k_{p-OP}	Proportional gain of the active power outer control loop
k_{i-OP}	Integral gain of the active power outer control loop

$G_{OQ}(s)$	Reactive power outer control loop
k_{p-OQ}	Proportional gain of the reactive power outer control loop
k_{i-OQ}	Integral gain of the reactive power outer control loop
Q_{recalc}	The signal used to recalculate the reactive power reference
k_q	The gain used in the reactive power reference recalculation
k_p	The gain used in the bump-less transfer
Z_n	Grid Thevenin impedance
$FL_{1\rightarrow4}$	Fault locations
k_v	The enhanced outer loop constant used to calculate the new reactive power reference
$\|U\|^-$	Negative sequence PCC voltage magnitude
V_{Pmin}	Minimum positive sequence voltage
V_{Nmax}	Maximum negative sequence voltage
ω_i	The frequency output of the current synchronization loop
$G_{CS}(s)$	Controller of the current synchronization loop
$g_{PLL}(t)$	PLL controller in the time domain
$\dot{\delta}_{PLL}$	First derivative of the PLL angle

$\ddot{\delta}_{PLL}$	Second derivative of the PLL angle
$g_P(t)$	Active power loop controller in the time domain
$\dot{\delta}_P$	First derivative of the APL angle
$\ddot{\delta}_P$	Second derivative of the APL angle
$g_{PSL}(t)$	Power synchronization loop in time domain
ω_{PSL}	Frequency of Power synchronization loop
δ_{PSL}	Angle of Power synchronization loop
$\dot{\delta}_{PSL}$	First derivative of power synchronization loop angle
$g_{CS}(t)$	Current synchronization controller in the time domain
k_{p-CS}	Proportional gain of the current synchronization controller
ω_{CS}	Frequency of the current synchronization controller
δ_{CS}	Angle of the current synchronization controller
$\dot{\delta}_{CS}$	First derivative of the angle of the current synchronization controller

List of Abbreviations

VSM	Virtual Synchronous Machine
CC	Current controller
FDA	Fault Detection Algorithm
COP26	26th Conference of Parties
SM	Synchronous machines
PV	Photovoltaics
FACTS	Flexible alternating current transmission system
PCC	Point of common coupling
PLL	Phase-Locked Loop
RoCoF	Rate of Change of Frequency
FRT	Fault Ride-through
FFR	Fast Frequency Response
IFDA	Improved Fault detection algorithm
VSC	Voltage Source Converter

TSO	Transmission system operator
SCL	Short Circuit Level
HVDC	High Voltage Direct Current
PWM	Pulse width modulation
PI	Proportional and Integral Controller
SCR	Short circuit ratio
PSC	Power synchronization controller
KHI	Kawasaki Heavy Industries
IEPE	Institute of electrical power engineering
AVR	Automatic voltage regulator
SPC	Synchronous power controller
pn	Positive and negative
APL	Active power loop
PSL	Power synchronization loop
CS	Current synchronization

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Chapter 1

Introduction

1.1 Background

The world is facing the consequences of climate change, largely caused by carbon emissions. In November 2021, the 26th Conference of Parties (COP26), which is the decision-making body of the United Nations Framework Convention on Climate Change, was held in Glasgow, UK to discuss climate change and propose coordinated actions to reduce its risks. According to the advice of the Climate Change Committee, countries should formulate a plan to reduce their carbon emissions. In response to this, the UK has planned to reduce its carbon emissions to 68% by 2030 of that in 1990 [1]. In the field of electricity generation, cooperation is being established between the academia and industry towards replacing conventional carbon-emitting energy sources with greener alternatives. For conventional energy generation sources (e.g. coal and steam), synchronous machines (SMs) represent a large portion of the electric energy sources for grids interface. These machines are mechanical systems that are capable of inherently providing inertia and damping to the electrical system. Among the renewable energy sources such as hydro, wind, and solar, wind and photovoltaic (PV) systems are the most common technologies owing to their low cost and high reliability. Meanwhile, PV and wind use power converters instead of a SM to interface with the grid. With the continuous development of high voltage direct current (HVDC), the future of electrical grids will be dominated by power converter-interfaced generation. In the UK, offshore wind generation is expected to increase from 9 to 83.1 GW by 2050 [2]. In Australia, the combined wind and solar market share in the national electricity market has reached 20% [3]. In the ERCOT (Texas) grid, wind energy is 20% of the total energy generation, and it covers 15% of the average total energy

consumption and up to 54% of the instantaneous power consumption [4]. In Ireland, according to EirGrid, the total wind generation was up to 4300 MW in 2020, which was 37.9% of the total electricity generation, and the total renewable energy generation is targeted to be 70% of the total energy generation by 2030 [5]. Meanwhile, some global challenges can lead to an increase in the renewable energy generation share, such as global changes in energy consumption owing to national lockdowns caused by COVID-19. In the UK in the summer of 2020, demand on the electrical grid dropped by 18%, leading to a significant increase in the share of renewable energy sources such as wind and solar energy [1]. These examples show that the challenges posed by the increased penetration of renewable energy need to be addressed to avoid unexpected catastrophic consequences.

Two main challenges posed by the increased penetration of converter-interfaced generation are voltage and frequency instabilities [6]. Voltage instability occurs because of the intermittent nature of the renewable energy generated by wind turbines or PV systems, which are built in remote areas, including offshore wind farms. These areas are connected to the grid through a long transmission line resulting in weak grids. The long transmission line creates high impedance between the renewable energy generation source and the grid, which makes the voltage at the point of common coupling (PCC) very sensitive to any disturbance and easily changed by reactive power injection [7]. This phenomenon is different from that of strong grids in which voltage variations do not affect the PCC voltage as it is secured by the strong grid voltage. The weak grid phenomenon causes another serious problem with the most commonly used synchronization technique called phase-locked loop (PLL). PLL requires a stiff grid to maintain synchronization [6], specific tuning, and operation references in weak grids. Furthermore, frequency instability mostly occurs in low-inertia systems because renewable energy generation methods mostly do not rely on SMs, so that the absence of mechanical rotors reduces the stored kinetic energy that can be released in the form of inertia. During power imbalance, frequency disturbance occurs, which can be characterised by the frequency nadir, rate of change of frequency (RoCoF), and restoration time. Figure 1.1 shows a simplified sketch of the three characteristics, where frequency nadir is the lowest acceptable frequency reached after a disturbance,

RoCoF represents how fast the frequency changes after the disturbance, and restoration time is the time required to stabilize the frequency to the nominal acceptable range.

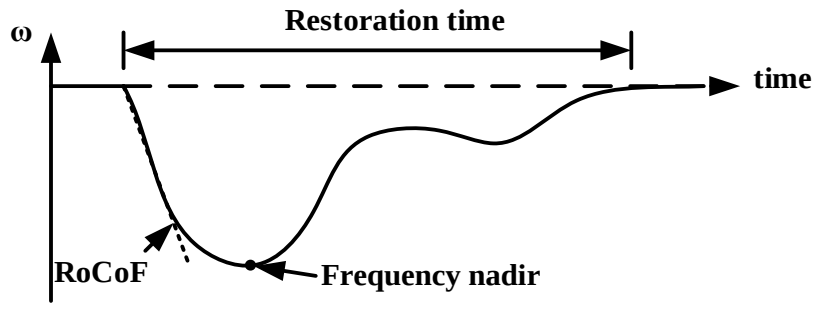


Figure 1.1. Simplified behaviour of the frequency response after a disturbance in the active power or a fault [8]

These characteristics are usually determined by the grid operator to achieve a desired stable operation. The RoCoF of the system is affected by the inertia of the system; thus, a decrease in the inertia causes an increase in the RoCoF after grid disturbance [9]. In the UK, the loss of main protection uses RoCoF relays, which detect and disconnect energy generations with high RoCoF values [10, 11]. This type of protection can lead to tripping in weak grids during frequency disturbance. Hence, the limit of the RoCoF relays was changed from 0.5 to 1 Hz/s in 2016 [12]. However, the resetting of the relays is not sufficient because the decrease in system inertia still requires further solutions to contain the accompanying problem. Another issue caused by the low-inertia system is the inability to dampen a frequency disturbance inherently. Because traditional converter-interfaced generations cannot provide inertia, therefore frequency changes can lead to instability and lack of frequency recovery without a proper frequency control. Figure 1.2 shows different timescales of frequency dynamics and control in which an inertial response is created through the kinetic energy stored in the rotor of the SM. The inertial response of the SM lasts up to 5s and is an instantaneous response to a frequency change. Then, primary and secondary controls are activated by changing the active and reactive power references, and they take some seconds and minutes, respectively. The time required for the tertiary control and generator rescheduling range from a couple of minutes to several hours. Although the standard converter-interfaced generation control has a faster response than the primary

control, its timescale is slower than that of the inertial response. Therefore, the standard converter-interfaced generation control needs to be improved to achieve a similar performance to the inertial response.

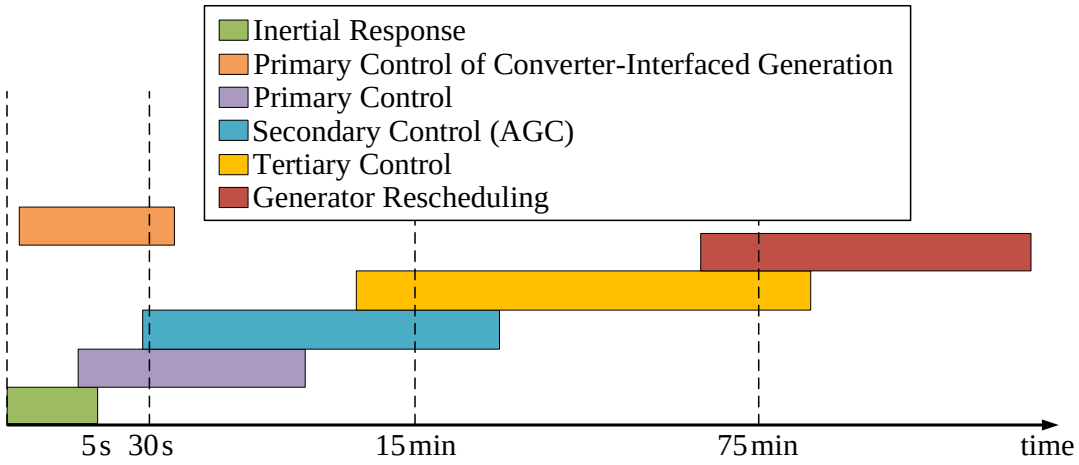


Figure 1.2. Timescales of frequency-related dynamics in conventional power systems and frequency control through converter-interfaced generation [6]

One significant frequency event that caused a major electricity disruption was recorded in Great Britain on 9th August 2019 [13, 14]. The incident affected over 1 million customers, including hospitals and rail services, and it occurred when an overhead transmission line was struck by lightning. Hornsea wind farm, with a maximum capacity of 1200 MW, was affected by voltage fluctuations after the lightning strike. The event triggered an unexpected response from the outdated control system, causing the protection system to deload the capacity of the wind farm from 799 to 62 MW [13]. Further generation disconnections led to further decrease in frequency such that over 1 million customers were disconnected owing to the low frequency demand disconnection action to restore the generation and demand balance. This event is not considered as a low-inertia system but a clear example of the consequences of frequency disturbances [15]. Therefore, a new method is required to support the frequency stability of non-synchronous renewable energy sources.

Modern grid codes specify requirements for renewable energy generators such as fault ride-through (FRT). Additionally, renewable energy generation systems must provide reactive power support and primary frequency support, as well as dampen power oscillations according to their capabilities, similar to conventional synchronous generation systems [16]. The grid code requirements regarding low voltage ride-through in European countries are presented in [17, 18]. A review of FRT specifications in different grid codes for renewable energy generation systems is presented in [19]. A study on different reactive power management methods for renewable energy generation is introduced in [20] as a FRT requirement. Additionally, the technical requirements for grid-connected wind power plants in USA, China, and Turkey are presented in [21, 22].

Several solutions for low inertia have been proposed, such as increasing the number of synchronous condensers [23], using flexible alternating current transmission system (FACTS) devices to enhance voltage support and fault current [23], adopting new fast frequency response (FFR) techniques [24], and upgrading the converter controllers to form grids [24, 25].

Meanwhile, FACTS devices or FFR requires a time to respond, and they increase the grid expansion costs.

A grid-forming converter, which is a promising solution, can produce voltage at the converter terminals without an external grid [26, 27]. One of the most well-known types of grid-forming converters is VSM, which emulates the behaviour of a SM in different degrees of detail. VSMs can provide an inertial response similar to that of SMs [28], achieve stable response in very weak grids [29], and have black start capability [27]. However, the VSM structure requires further study, including the assessment of converter–converter interactions and addition of new energy storage to support inertial power provision [30].

1.2 Scope of work

Although VSM controllers emulate the behaviour of SMs, the inherent current limitation of power electronic converters makes them unable to deal with fault current in the same way as SMs. SMs are more tolerant to current increase than power converters owing to their thermal inertia. Therefore, current limitation techniques need to be considered in VSM-based power converter controllers under normal and fault conditions. During normal conditions in which the voltage is in the nominal range, VSM structures can limit the current through an active power control loop for structures without a current controller or directly through the current controller for other structures. The control loop can keep the current below the maximum current rating. However, under fault conditions, the active power loop (APL) cannot limit the current for structures without a current controller; hence, an alternative control structure is required to protect the power converter during faults. The alternative loop must support the grid under fault conditions by injecting reactive power based on the recommendations of electrical grid codes. This is required for voltage support and the protection devices in the power system to operate and identify the fault conditions.

The scope of this thesis is to investigate the FRT capability of VSM structures without a current controller. This thesis begins with the review of existing grid-forming control structures and the FRT strategies introduced by several authors. Subsequently, the current-limiting capability of a VSM structure is investigated, and the control structure limitations and requirements are identified. Further, an improved control structure is proposed, followed by analyses and assessments under different types of faults under different grid conditions. Finally, a comparative analysis is provided to improve the response of the proposed structure.

1.3 Contributions

This thesis makes some important contributions that can help researchers to improve the performance of VSM structures. These contributions are:

- A steady-state current limitation technique suitable for VSM structures without a current control loop is proposed. The technique can mitigate the overcurrent caused by changes in the grid voltage by recalculating the active and reactive power references.
- A new FDA is developed using sensitivity analysis along with an improved solution to enhance the operation of the VSM control structure for different fault types in strong and weak grid conditions. Another FDA is also proposed to provide detection flexibility under several grid conditions. These algorithms and control structure improvements are based on a study of conventional VSM structures without a current control loop, and they address the limitations of the solutions proposed in past studies.
- A new synchronization technique is introduced, which is a possible alternative for future control structures. Subsequently, possible synchronization techniques that can replace the PLL in the backup current controller are investigated. This study also involves stability analysis using the phase portrait of different synchronization loops. Parametric sweep analysis is then conducted to determine the appropriate tuning parameters of each controller.
- Finally, all the synchronization techniques are compared to highlight the advantages and disadvantages of each technique.

1.4 Thesis structure

This thesis is structured into six chapters. Chapter 1 provides the background and rationale for this study.

In Chapter 2, the conventional converter control, also referred to as grid-following converter control, is explained. The traditional converter control comprises an inner current control loop built according to a converter model. The references of the current controller are fed through active and reactive power controllers, which are independently controlled because the PLL action guarantees this independence. Subsequently, grid-forming control structures are reviewed, with special focus on two categories of VSM structures. These categories are based on the order of the SM model used to build the converter control structure. Further, a comparison table is presented

to summarize the different structures according to the control loops. Finally, different FRT techniques adopted in VSM structures are reviewed.

In Chapter 3, the VSM controller architecture is explained, and a technique is proposed for limiting the active and reactive power references through current calculations. The uncontrollable fault current behaviour of the VSM is then explained, and recommendations for alternative control loops are proposed by investigating different FRT strategies.

In Chapter 4, the conventional VSM structure for controlling fault currents in all fault types is discussed. The conventional structure is first discussed and then subjected to unbalanced faults under strong and weak grid conditions. This study shows that the structure requires improvements because of its limitations. Subsequently, the structure is improved so that it has a wider stability margin that covers unbalanced faults in weak grid conditions. The structure is then subjected to fault location sensitivity analysis to verify its reliability. Furthermore, parametric sweep analysis is conducted and used as a reference for tuning the control structure. An improved fault detection algorithm (IFDA) is then introduced, which further improves the conditions for identifying unbalanced faults in weaker grid conditions. In addition, the proposed structure with IFDA and the conventional grid-following converter are compared, showing the reliability of the proposed control structure compared to the commonly used structures.

In Chapter 5, different synchronisation techniques that can replace the PLL in the backup controller of the VSM structure are explained. Parametric sweep analysis is then conducted for each technique, and the tuning of each technique is discussed. These techniques are then compared, and their individual advantages and disadvantages are highlighted. Finally, the conclusions of this thesis are provided in Chapter 6.

1.5 List of publications

1) A. Abdelrahim, M. Smailes, P. McKeever, K. H. Ahmed, and A. Egea-Alvarez, “Modified grid forming converter controller with fault ride through capability

without PLL or current loop," presented at the 18th Wind Integration Workshop, Dublin, Ireland, 2019.

2) A. Abdelrahim, M. Smailes, K. H. Ahmed, P. McKeever, and A. Egea-Àlvarez, "Indirect current control grid forming converter challenges and limitations during faults," Abstract for EERA DeepWind'2021, Trondheim, Norway, 2021.
3) A. Abdelrahim, M. Smailes, K. H. Ahmed, P. McKeever, and A. Egea-Àlvarez, "New fault detection algorithm for an improved dual VSM control structure with FRT capability," IEEE Access, vol. 9, pp. 125134-125150, 2021, doi: 10.1109/ACCESS.2021.3109165.
4) An article is under preparation with the work reported in Chapter 5.

Chapter 2

Literature Review

2.1 Introduction

In this chapter, the voltage source converters (VSCs) of the most common topologies are discussed. Then, the controls used for the VSCs are described and categorised into grid-following and grid-forming structures. In the next section, the VSMs of grid-forming converters, which are considered the most promising control structures from the author's perspective, are discussed. Subsequently, the key points of different VSM topologies are summarised. Finally, the FRT of the VSM and different methods of enhancing the FRT capability of the VSM are discussed.

2.2 Electrical grid decarbonisation challenges

The UK has ambitious plans of achieving a net zero emission goal by 2050, and several measures have been proposed to reach this goal [31]. These measures include decreasing the use of natural gas in heating, reducing the use of fuel-based vehicles, and decarbonising electricity generation. The last objective requires increasing the penetration of renewable energy generation; however, it is faced with several challenges regarding grid stability and reliability. National Grid ESO envisions an electricity generation of approximately 83.1 GW from offshore windfarms by 2050 [32], as shown in Figure 2.1.

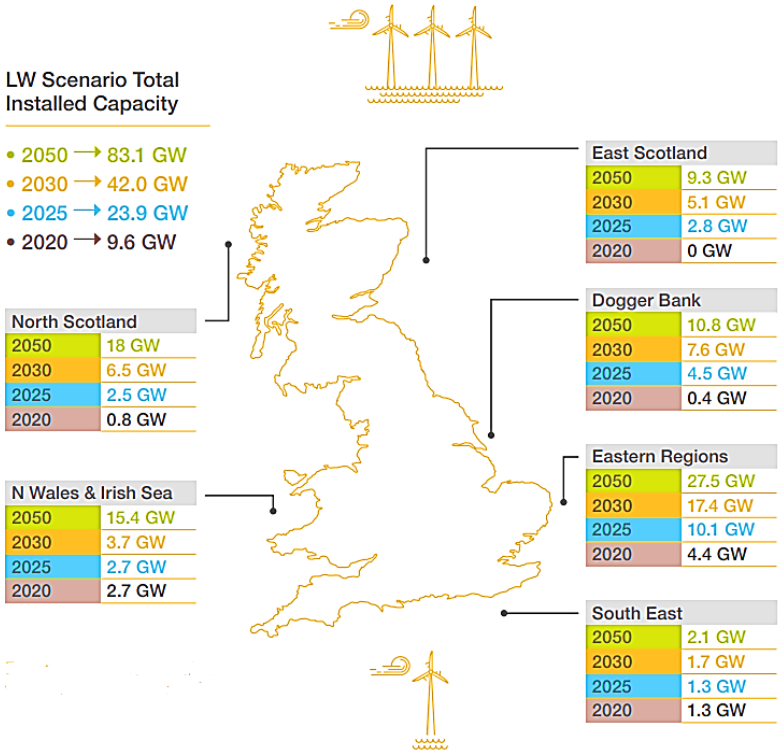


Figure 2.1. Installed offshore wind capacity by 2050 [32]

This penetration causes unexpected challenges that require immediate attention. One of the challenges is changing the electrical system properties such as system strength. System strength is defined by the Australian Energy Market Commission as “the characteristic of an electrical power system that relates to the size of the change in voltage following a fault or disturbance in the power system” [33]. One of the main contributors to voltage stability is SM, and by decreasing the SMs with respect to converter-based generation, the system strength decreases. Additionally, the short-circuit level, which is proportional to the system strength, is expected to significantly decrease over the next years owing to an increase in renewable energy generation, as shown in Figure 2.2.

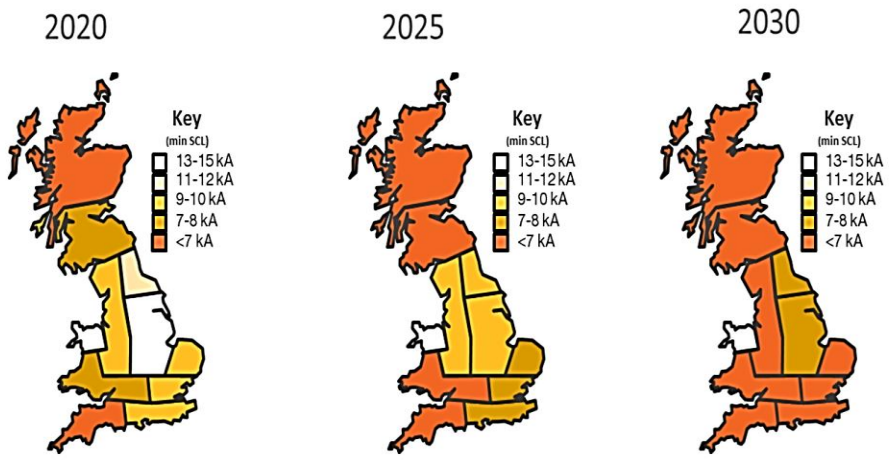


Figure 2.2. Expected short-circuit level in Great Britain from 2020 to 2030 [34]

Both of these phenomena led to the concept of weak grids, which is a serious problem affecting the reliability and protection of electrical systems. In a power-converter-dominated network, weak grids require a different tuning for the protection system. Moreover, it was reported that the standard vector current controller with a PLL had limitations in weak grids as the PLL might exhibit unstable behaviour. Figure 2.3 shows the risks presented by the power converters in weak grids using a PLL, which shows more than 50% increase in a large area of Great Britain.

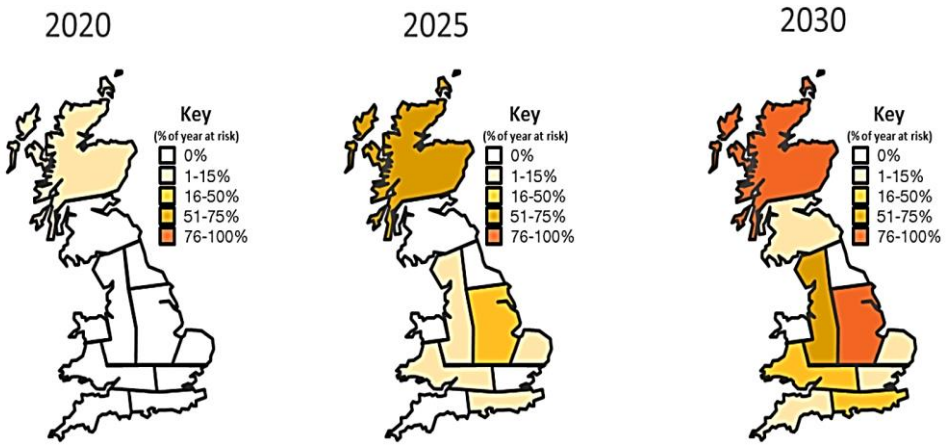


Figure 2.3. Risks presented by PLL in Great Britain from 2020 to 2030 [34]

In addition to weak grids, the decrease in mechanical inertia provided by the grid as a result of reduced SM penetration has introduced further challenges. Figure 2.4 shows the expected trend of the national inertia in Great Britain by 2030, which clearly

indicates that the declining inertia is becoming significant and the impacts of such a change requires a detailed study.

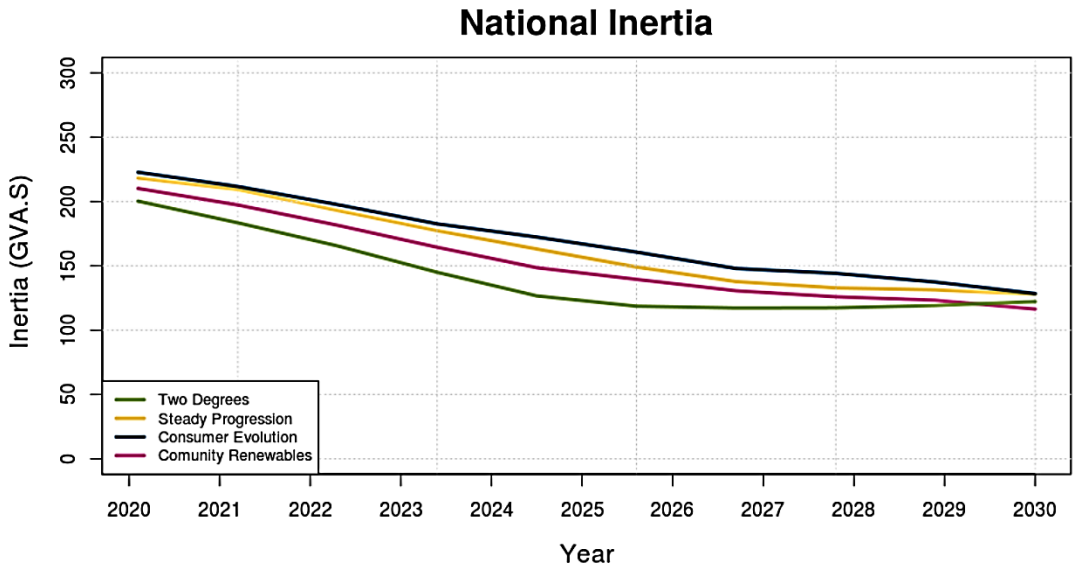


Figure 2.4. Inertia trend up to 2030 [35]

The low-inertia problem has attracted the attention of several governments, and some solutions have been suggested, as presented in Table 2.1. The table presents the initiatives taken by some countries to solve the low-inertia problem, revealing that all the countries are moving towards the same concept of emulating inertia through renewable energy sources.

Table 2.1. Low-inertia solutions by different countries [36]

Country (TSO, Year)	**Nominal frequency [Hz] (Frequency nadir [Hz], maximum duration [s])**	**Applied solutions**
Great Britain [37] (National Grid, 2015)	50 (49.5, 10)	• Adopting self-regulated load enhancements • Adding synchronous condensers • Utilising renewable energy sources with emulated inertia

		• Establishing new storage systems based on synchronous energy (e.g. compressed air energy storage)
Ireland [38] (EirGrid, 2013)	50 (47, 20)	• Setting the maximum renewable energy penetration to 70% • Renewable energy sources are expected to emulate inertia • Adding synchronous condensers and mechanical stabilisers • Increasing the RoCoF relay setting from 0.5 to 1 Hz/s
Australia [39, 40] (Australia Energy Market Operator, 2018)	50 (47.5, 9)	• Setting a minimum synchronous generator penetration • Emulating inertia through renewable energy sources
United States [41] (Electric Reliability Council of Texas, 2018)	60 (59.3, 0.5)	• Adding ancillary services (e.g. synchronous inertial response) • Using flywheel for fast frequency regulation

In this section, the two main problems for the future of electrical grids have been identified as low-inertia systems and weak grids. The study of these network types requires the investigation of the standard control approach for power converters and its limitations. In the next sections, inertia emulation through the control structures mentioned in the literature is discussed, and the limitations of these structures are explained, focusing on FRT as the main topic of this thesis.

2.3 VSC structure

The common VSC structures are two-level, three-level, and modular multilevel converters. The two-level converter comprises two switches per phase, and each switch connects to either a positive or negative DC voltage, as shown in Figure 2.5. The DC source represents the DC side of the converter, which can either be a renewable energy source or a HVDC. The three-phase AC terminals are represented by phase A, phase B, and phase C, and they are connected to a three-phase AC grid. The switches are controlled through the pulse width modulation (PWM) inputs, which are created using the controller structure output.

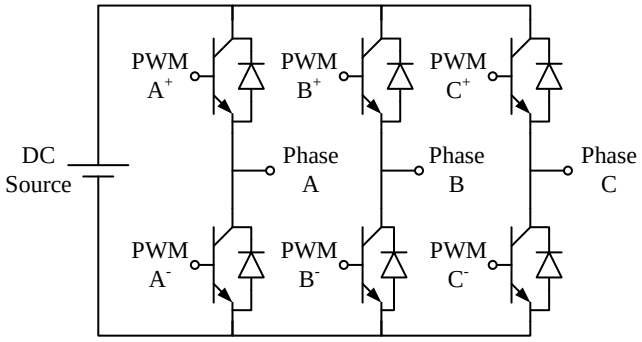


Figure 2.5. Two-level voltage source converter structure

2.4 VSC control structures

Grid-following structures control the active and reactive powers based on the angle measured at the connection point using a PLL. Fig. 2.6 shows a schematic diagram of a representation of a simple grid-following model. Meanwhile, grid-forming model representation is used to produce voltage and frequency, and a simple schematic is shown in Figure 2.7.

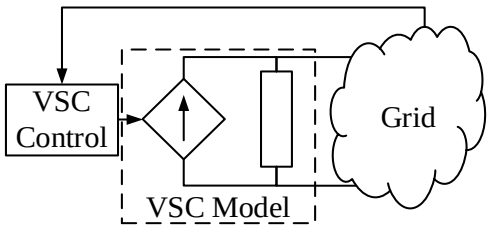


Figure 2.6. Grid-following model

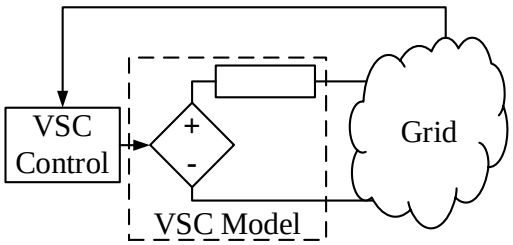


Figure 2.7. Grid-forming model

2.5 Grid-following controllers

There are several implementations of the current controller, including the αβ-frame and dq-frame implementations [42]; however, the traditional dq-oriented vector current controller is commonly used. This vector controller transforms sinusoidal voltages and currents into DC values that can be controlled using simple proportional and integral (PI) controllers. To track the grid angle, a PLL is used to synchronize with the grid voltage. In the following section, the constructions of vector current controllers are described.

2.5.1 Inner loop control

The vector current controller relies on the relationship between the current passing through the filter impedance between the converter terminals and the PCC. Figure 2.8 shows a single line diagram of the converter terminals and PCC.

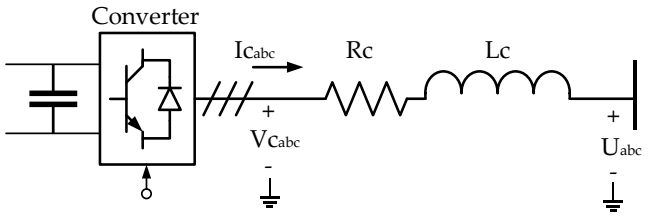


Figure 2.8. Single line diagram of a converter connection to a PCC

The equations for the single line diagram in the abc frame are expressed as:

$$\begin{bmatrix} v_{c_a} \\ v_{c_b} \\ v_{c_c} \end{bmatrix} - \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \begin{bmatrix} R_c & 0 & 0 \\ 0 & R_c & 0 \\ 0 & 0 & R_c \end{bmatrix} \begin{bmatrix} i_{c_a} \\ i_{c_b} \\ i_{c_c} \end{bmatrix} + \begin{bmatrix} L_c & 0 & 0 \\ 0 & L_c & 0 \\ 0 & 0 & L_c \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{c_a} \\ i_{c_b} \\ i_{c_c} \end{bmatrix} \tag{2.1}$$

Substituting $v = Ve^{j\omega t}$, $u = Ue^{j\omega t}$and $i = Ie^{j\omega t}$, then

$$\begin{bmatrix} V_{c_a} \\ V_{c_b} \\ V_{c_c} \end{bmatrix} - \begin{bmatrix} U_a \\ U_b \\ U_c \end{bmatrix} = \begin{bmatrix} R_c & 0 & 0 \\ 0 & R_c & 0 \\ 0 & 0 & R_c \end{bmatrix} \begin{bmatrix} I_{c_a} \\ I_{c_b} \\ I_{c_c} \end{bmatrix} + \begin{bmatrix} L_c & 0 & 0 \\ 0 & L_c & 0 \\ 0 & 0 & L_c \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{c_a} \\ i_{c_b} \\ i_{c_c} \end{bmatrix} + j \begin{bmatrix} \omega L_c & 0 & 0 \\ 0 & \omega L_c & 0 \\ 0 & 0 & \omega L_c \end{bmatrix} \begin{bmatrix} I_{c_a} \\ I_{c_b} \\ I_{c_c} \end{bmatrix} \tag{2.2}$$

where V_c is the converter terminal voltage, U is the PCC voltage, R_c is the filter resistance, L_c is the filter inductance, and ω is the grid frequency.

The dq vectors compared to the abc vectors are shown in Figure 2.9, at which the alignment of the dq components used in the thesis are easily explained.

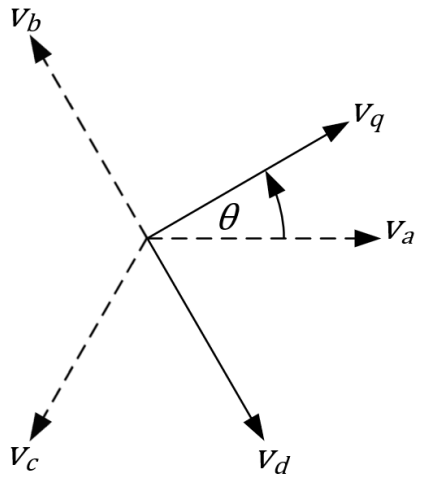


Figure 2.9. dq plane alignment shifted from abc plane

The abc frame is transformed into the synchronous reference frame using Eq. (2.3):

$$x_{dq} = T\, x_{abc} \tag{2.3}$$

$$T = \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix}$$

where θ is the angle of the d component.

The equations are then rewritten as follows:

$$\begin{bmatrix} v_q \\ v_d \end{bmatrix} - \begin{bmatrix} u_q \\ u_d \end{bmatrix} = \begin{bmatrix} R_c & -\omega L_c \\ \omega L_c & R_c \end{bmatrix} \begin{bmatrix} i_q \\ i_d \end{bmatrix} + \begin{bmatrix} L_c & 0 \\ 0 & L_c \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_q \\ i_d \end{bmatrix} \tag{2.4}$$

By applying Laplace transform to the equations, we obtain:

$$\begin{bmatrix} v_q \\ v_d \end{bmatrix} = \begin{bmatrix} R_c + sL_c & -\omega L_c \\ \omega L_c & R_c + sL_c \end{bmatrix} \begin{bmatrix} i_q \\ i_d \end{bmatrix} + \begin{bmatrix} u_q \\ u_d \end{bmatrix} \tag{2.5}$$

These equations can be used to build the current control according to internal model control method [43], as shown in Figure 2.10.

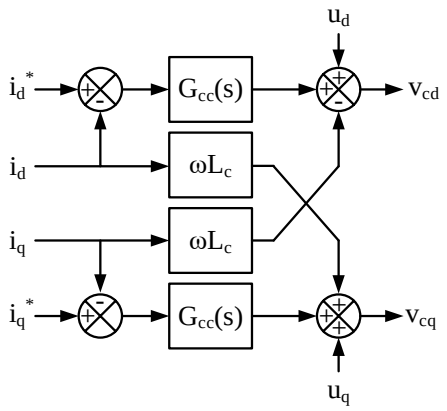


Figure 2.10. Current control structure

$$G_{CC}(s) = \frac{k_{p-CC}s + k_{i-CC}}{s} \tag{2.6}$$

where

$$k_{p-CC} = \frac{L_c}{\tau_{CC}}, k_{i-CC} = \frac{R_c}{\tau_{CC}} \tag{2.7}$$

where τ_{CC} is the time constant of the controller loop.

2.5.2 Outer loop control

There are different types of outer loop structures. In the outer loop structure considered in this section, active and reactive powers are used as references for the current loop. The outer loop control is calculated as follows:

$$S = P + jQ = 3\tilde{v}_{c_{dq}}\bar{\imath}_{c_{dq}} \tag{2.8}$$

$$\tilde{v}_{c_{dq}} = \frac{v_{c_q} - jv_{c_d}}{\sqrt{2}} \tag{2.9}$$

$$\bar{\imath}_{c_{dq}} = \frac{i_{c_q} - ji_{c_d}}{\sqrt{2}} \tag{2.10}$$

$$S = \frac{3}{2}\,(v_{c_q} - jv_{c_d})(i_{c_q} + ji_{c_d}) \tag{2.11}$$

$$P = \frac{3}{2}\left(v_{c_q}i_{c_q} + v_{c_d}i_{c_d}\right) \tag{2.12}$$

$$Q = \frac{3}{2}\left(v_{c_q}i_{c_d} - v_{c_d}i_{c_q}\right) \tag{2.13}$$

The independent controls for both the active and reactive powers are guaranteed by the PLL operation. The principle of operation of the PLL synchronization is that the reactive voltage component $V_d = 0$. Therefore, Eqs. (2.12) and (2.13) can be simplified to

$$P = \frac{3}{2}v_{c_q}i_{c_q} \tag{2.14}$$

$$Q = \frac{3}{2} v_{cq} i_{cd} \tag{2.15}$$

This operation guarantees that the active power control can control the direct current component i_d, whereas the reactive power control can control the quadrature component i_q.

2.5.3 Limitations and challenges

The current controller has control bandwidth limitation in weak grids [44]. This problem is caused by the fact that in weak grids, the value of the short-circuit ratio (SCR) is below three, and grids with SCR values below two are regarded as very weak grids. The lower the SCR, the higher the grid impedance.

$$SCR \approx \frac{1}{X_n} \tag{2.16}$$

where X_n is the reactance of the equivalent Thevenin grid impedance representing the equivalent of network impedances. For a reactive network the impedance is mostly reactive impedance, which leads to the neglection of the resistance. Accordingly, the circuit shown in Figure 2.11 can be used to get the active power equation (power angle equation).

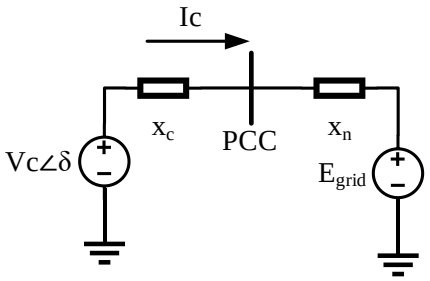


Figure 2.11. Simple representation of a grid connected VSC

The power angle equation is given by:

$$P = \frac{|V|_c |E|_{grid}}{X_c + X_n} \sin \delta \tag{2.17}$$

where δ is the angle difference between voltages V_c and E_{grid}.

As shown in Figure 2.12, the maximum active power decreases as SCR decreases as network impedance X_n increases. This indicates that for a low SCR, the linear area for the power converter stable operation is limited.

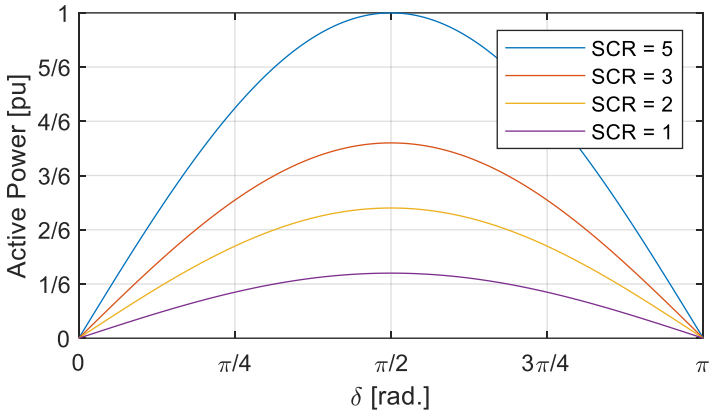


Figure 2.12. Active power versus δ for different SCRs

The VSC active power reference must consider such a limitation especially if the network equivalent impedance was changed as a result of fault, because this leads to the instability of the converter controller in the case of low SCR values. As reported in the literature, current controllers in weak grids have an instability challenge, and several solutions have been suggested [45, 46], such as enhancing the outer loop based on the gain scheduling controller and adopting a multivariable droop synchronous current control strategy.

2.5.3.1 PLL instability

PLL is a source of instability for the converter controller [47]. The PLL tends to instability in low grid strength. In this section, this instability is studied based on the PLL linear model whose schematic shown in Figure 2.13.

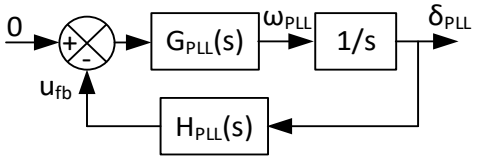


Figure 2.13. PLL linear block diagram

The controller $G_{PLL}(s)$ is expressed by:

$$G_{PLL}(s) = k_{p-PLL}\frac{\frac{1}{\tau_{PLL}} + s}{s} \tag{2.18}$$

The feedback is expressed by:

$$\begin{gathered} u_{fb} = u\sin(\theta_g - \delta_{PLL}) \\ u_{fb} = u(\sin\theta_g \cos\delta_{PLL} - \cos\theta_g \sin\delta_{PLL}) \end{gathered} \tag{2.19}$$

Where θ_g is the angle of the grid Thevenin equivalent voltage.

By linearising Eq. (2.19), the following equations are obtained:

$$\begin{gathered} V_{fb} = u\,(-\sin\delta_{PLL_o}\sin\theta_g\ \Delta\delta_{PLL} - \cos\theta_g\cos\delta_{PLLo}\,\Delta\delta_{PLL}) \\ u_{fb} = \Delta\delta_{PLL}\,u\left(-\cos(\theta_g - \delta_{PLL_o})\right) = \Delta\delta_{PLL}\,u\,(\sin(\theta_g - \delta_{PLL_o} - 90^o)) \end{gathered} \tag{2.20}$$

$$H(S) = u\,(\sin(\theta_g - \delta_{PLL_o} - 90^o)) \tag{2.21}$$

The −90° angle proves that the PLL inherently imposes a quarter-cycle delay for angle detection.

Assume $u_q = u\,(\sin(\theta_g - \delta_{PLL_o} - 90^o))$,

$$H(s) = u_q. \tag{2.22}$$

The characteristic equation is then given by:

$$s^2 + k_{p-PLL}u_q\, s + \frac{k_{p-PLL}u_q}{\tau_{PLL}} = 0 \tag{2.23}$$

$$\therefore \omega_n = \sqrt{\frac{k_{p-PLL}u_q}{\tau_{PLL}}}\ and\ \zeta = \frac{\sqrt{K_{p-PLL}u_q\tau_{PLL}}}{2} \tag{2.24}$$

As mentioned in the modelling of the current controller, the equation for the q-component is given by:

$$v_{c_q} = i_{c_q}R_c + L_c\frac{di_{c_q}}{dt} - \omega L_c i_{c_d} + u_q \tag{2.25}$$

By increasing the inductance, the q-component of the PCC voltage is increased. Thus, for the PLL to maintain the synchronization process, a reference angle (θ_c) is applied, which forces the converter to apply a voltage with a q-component to cancel out the q-component of the voltage at the PCC. Basically, the PLL output angle (δ_{PLL}) increases by increasing the PCC voltage owing to an increase in the Thevenin network impedance caused by the low SCR. Therefore, an increase in the network impedance leads to an increase in the PLL angle, which extends beyond the stability region of the power angle equation and makes the PLL angle value to increase over ($\frac{\pi}{2}$), which is the limit of the converter angle.

A simulation was performed to show that the PLL output loses stability when the SCR is very low. Figure 2.14 and Figure 2.15 show the PLL output frequency for different SCRs in which SCR_6 is the highest and SCR_1 is the lowest. The SCR_3 values in Figure 2.14 and Figure 2.15 are equal. Figure 2.14 shows the frequency measured by the PLL for different low SCRs, revealing that the PLL lost stability at SCR_3 when the active power reference was rated at the maximum active power capacity.

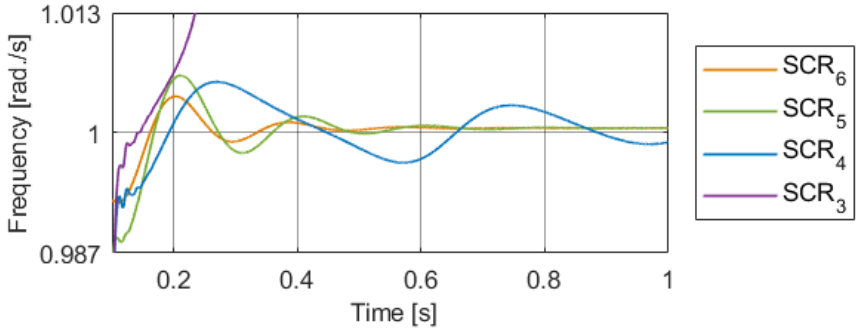


Figure 2.14. Grid frequency measured by PLL for different SCRs at a maximum active power reference P_{ref} = 1 pu. SCR_6 > SCR_5 > SCR_4 > SCR_3

Figure 2.15 shows another simulation to verify that the PLL can maintain its stability for lower SCRs at an active power reference below the rated power capacity.

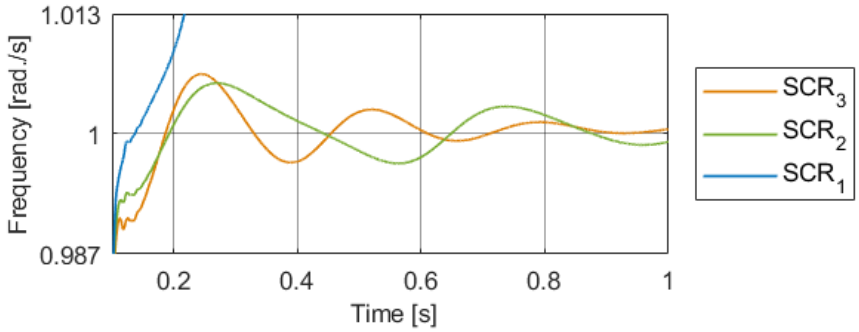


Figure 2.15. Grid frequency measured by PLL for different SCRs at an active power reference below maximum P_{ref} = 0.9 pu. SCR_3 > SCR_2 > SCR_1

The PLL lost stability at SCR = 1.7 because the angle of the converter voltage increased as the power reference increased. The converter angle was calculated using both the values of the PLL and angle created by the PQ controller, which represents the active power reference required by the active power controller. Therefore, the higher the active power reference, the higher the angle of the converter voltage, resulting in an angle that is in the nonlinear region of the power–angle relationship.

2.5.3.2 Inertial provision

Another challenge with traditional vector current controllers is the lack of inertial support. Inertial support has become crucial for the future of electrical grids dominated by renewable energy sources [48]. To tackle this problem, the current-controller-based VSC needs to be improved by adding extra loops to improve the inertial support

capability [49-53]. The references [49, 50, 53] suggest adding an extra loop that uses the PLL output to recalculate the active power reference, as shown in Figure 2.16, thereby enabling the grid-following converter to respond to frequency disturbances.

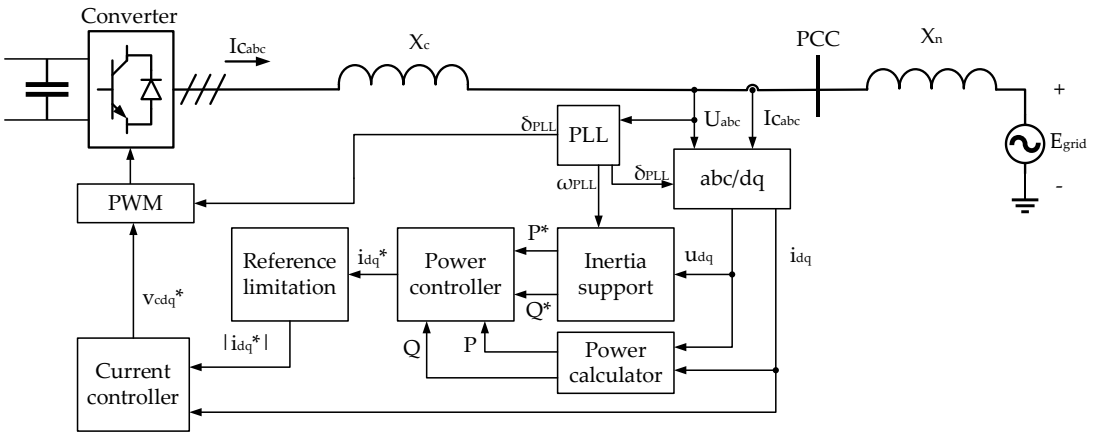


Figure 2.16. Grid-following control with an inertial support block

However, the grid-forming controller is better than the grid-following controller regarding its ability to respond to changes in frequency [50].

Therefore, the traditional vector current controller needs to have a minimum of two extra loops to tackle each problem, and other control structures may be preferred to solve these challenges.

2.6 Grid-forming controllers

In the literature, several grid-forming controllers based on converter voltage and angle have been presented, as shown in Figure 2.7. Some of these topologies replace the traditional PLL synchronization with a reliable alternative, whereas others emulate the mechanical inertia and damping behaviour of SMs. Figure 2.17 shows the classification of grid-forming controllers, which are discussed in the following sections.

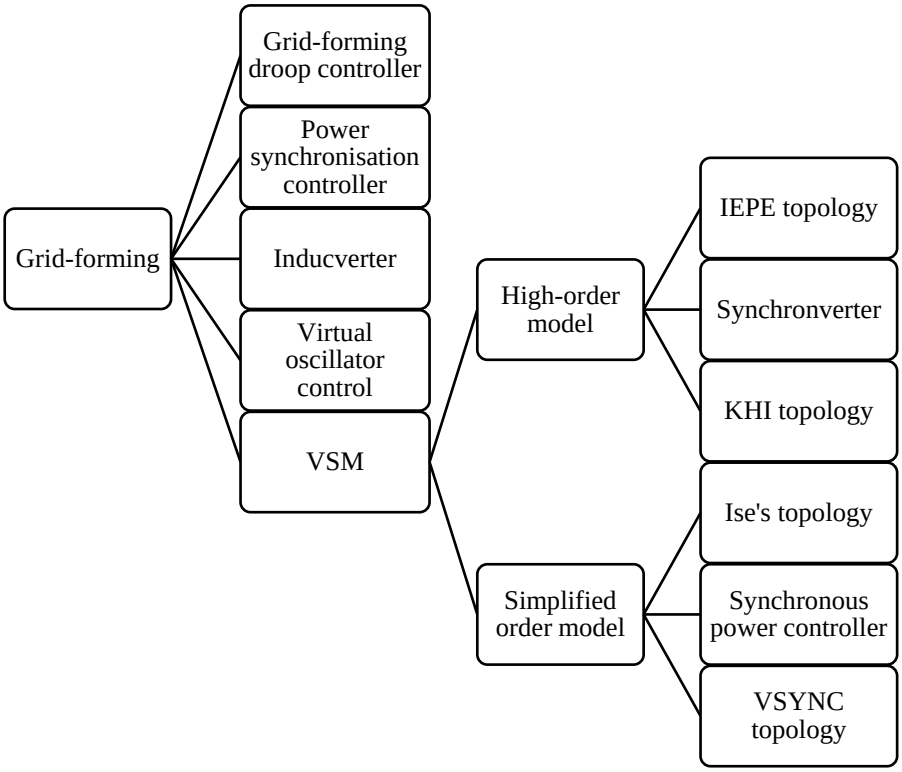


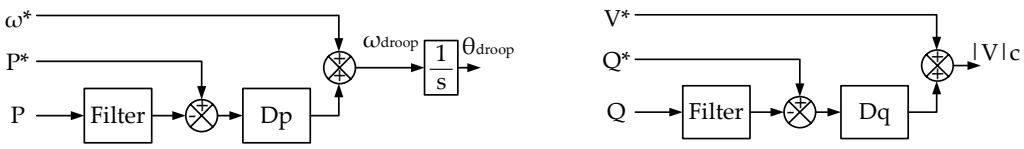
Figure 2.17. Classification of grid-forming controllers

2.6.1 Grid-forming droop controller

The simplest form of a grid-forming controller is the droop controller, which is based on first order equation as the following mathematical expression:

$$\omega_{droop} = \omega^* + Dp(P^* - P) \tag{2.26}$$

where Dp is the droop coefficient of the active power and ω^* is the reference frequency equivalent to the nominal frequency. Figure 2.18 shows the synchronization schematic of the droop controller.



(a) (b)

Figure 2.18. Grid-forming droop controller: (a) synchronization loop, (b) reactive/voltage control loop [54]

The droop controller voltage is controlled through a reactive power controller using the expression:

$$|V|_c = v^* + Dq(Q^* - Q) \tag{2.27}$$

where Dq is the voltage droop coefficient and v^* is the nominal voltage. To emulate both the inertia and damping behaviour of SMs using the droop controller, a first-order filter is required to emulate the inertial response of such a control structure [55].

2.6.2 Power synchronization controller

ABB [56, 57] proposed a popular structure called power synchronisation controller (PSC), which is shown in Figure 2.19. The synchronization loop controller comprises an integrator, which calculates the converter angle through the active power error. The original control structure has no inner current control loop. Therefore, during faults, a current control loop with PLL is activated to mitigate the fault current. The transition between the two control structures is based on comparing the measured current to the maximum converter current $|I|_{c-max}$, so that when the measured current is above $|I|_{c-max}$ the CC with a PLL is activated to limit the converter output current.

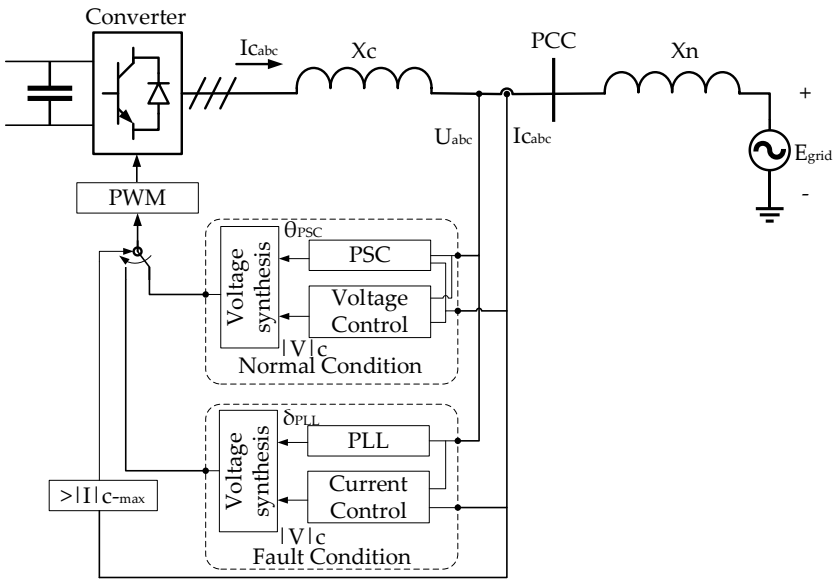


Figure 2.19. Overview of the VSC controller based on power synchronization control [58]

2.6.3 Inducverter

Another type of grid-forming controller discussed in the literature is inducverter, which is shown in Figure 2.20. The inducverter emulates the characteristics of the induction machine, and builds the VSC control structure accordingly [59]. The control structure is complex as the synchronization unit produces the rotor, stator, and slip frequencies, which have four equations represented by four interconnected loops, to produce the synchronization frequency.

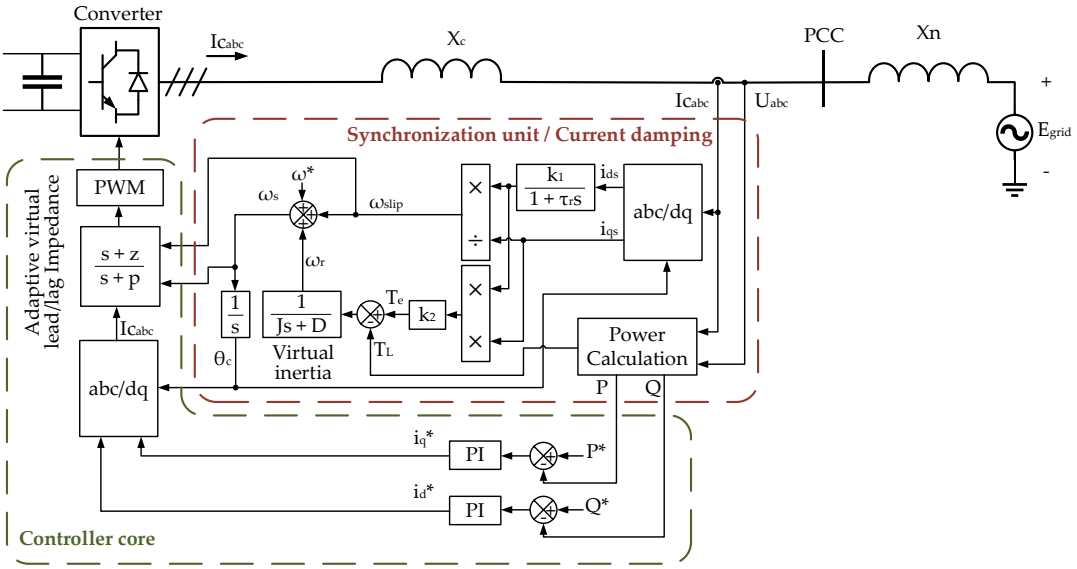


Figure 2.20. Schematic diagram of an inducverter [59]

2.6.4 Virtual oscillator control

Virtual oscillator control is one of the recent control structures with grid-forming capability. This type of control structures applies the behaviour of a weakly nonlinear one-limit oscillators, such as Van der Pol oscillator [60] and dead-zone oscillator [61], on the converter controller dynamics. The control structure benefits from the synchronization capability between converters starting from a random initial point. Figure 2.21 shows a three-phase schematic of the virtual oscillator control (Van der Pol oscillator), and the equations are given in [62]. A comparison of the transient response between the virtual oscillator control and droop control is provided in [63], in which an isolated microgrid system was used in varying voltage and frequency

ranges. Based on the study, the virtual oscillator control had a better performance than the droop controller.

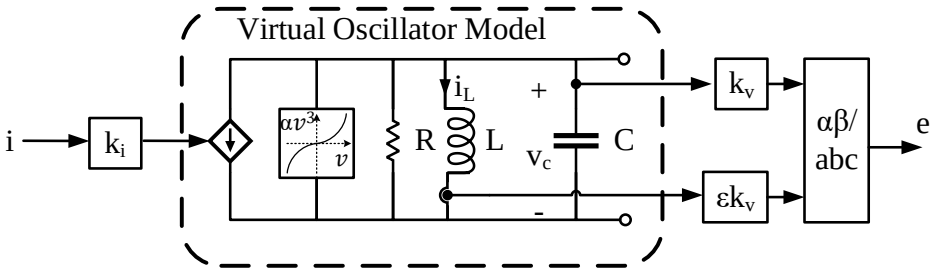


Figure 2.21. Three-phase virtual oscillator model [54]

The most commonly used grid-forming structure is VSM, which is categorised into several implementations, as discussed in the following section.

2.6.5 VSM structure

VSM was originally created by emulating the SM behaviour on the power converter control. This implementation was faced with challenges because the dynamic behaviour and current capacity of a power converter are very different from those of a SM. Therefore, multiple VSM implementations that mimic SMs with different degrees of detail have been proposed in the literature. Table 2.2 presents the classification of these implementations based on the degree of emulation of the SM. The first group comprises converter control structures that mimic the SM behaviour using above second order SM modelling equations. The second group consists of converter control structures that adopt the mechanical properties of SMs and apply swing equation dynamics on the converter controller.

The structures included in the table are accompanied with references to the implementation of each structure. In the following section, the VSM control structures are discussed and compared.

Table 2.2 Classification of different VSM converter controllers

Based on high-order SM model equations	VISMA Approach Method 1 [64-71] and others.
	VISMA Approach Method 2 [68, 72] and others.
	Synchronverters [73-83] and others.
	Kawasaki Heavy Industries (KHI) lab's topology [73, 84, 85] and others.
Based on simplified-order SM model equations	Ise lab's topology [73, 85] and others.
	Synchronous power controller [73, 86-90] and others.
	VSYNC topology [85, 91-95] and others.

VSM converter controller can be represented as a voltage source in series with an impedance, as shown in Figure 2.7. A grid-forming converter can support a low-inertia grid [96], and a VSM (considered as a type of grid-forming converter) exhibits good performance in weak grid conditions [97]. Additionally, VSM can provide inertia [97], which decreases as a result of increasing power converter-based sources [34]. Moreover, it can be tuned to provide a specific inertia and frequency damping based on power availability [85]. The implementation of VSMs can be divided into two categories: high-order and simplified-order models.

2.6.5.1 High-order model

In high-order VSM model, full SM behaviour is applied to the power converter control. The popular implementations are discussed in this section.

2.6.5.1.1 IEPE topology

The Institute of Electrical Power Engineering (IEPE) at the Clausthal University of Technology in Germany proposed the VISMA structure [72]. The VISMA structure was built in two approaches: VISMA method 1 and VISMA method 2. The general schematic of the VISMA method is shown in Figure 2.22, which is based on the high-order SM model.

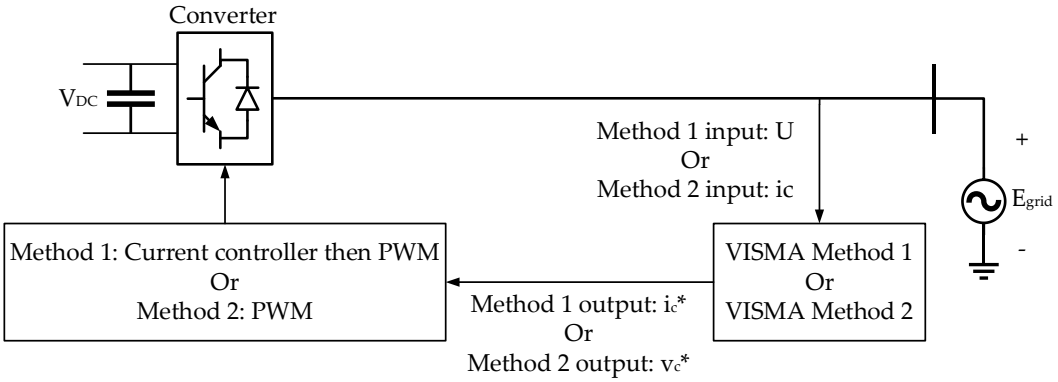


Figure 2.22. General schematic of the VISMA methods [72]

Figure 2.23 shows the schematics of VISMA methods 1 and 2 [64-67, 73, 85, 93, 98]. The VISMA methods comprise two parts: electrical and mechanical parts. The electrical part imitates the stator windings of a synchronous generator, which consists of the stator resistance R_s and inductance L_s. The nominal voltage peak E_P is used to generate three-phase voltage using the converter's calculated angle (from the mechanical part). The electrical part in VISMA method 1 takes the grid voltage as an input to calculate the current reference, whereas the electrical part in VISMA method 2 takes the grid current as an input to calculate the voltage reference. The mechanical part of each method contains two important mechanical characteristics: moment of inertia J and mechanical damping factor D (used to calculate the damping torque T_d). The mechanical part is responsible for calculating the converter angle so that electrical power is calculated in the electrical part and then translated to electrical torque T_e. The mechanical torque reference T_m can be chosen to represent the torque of a certain SM.

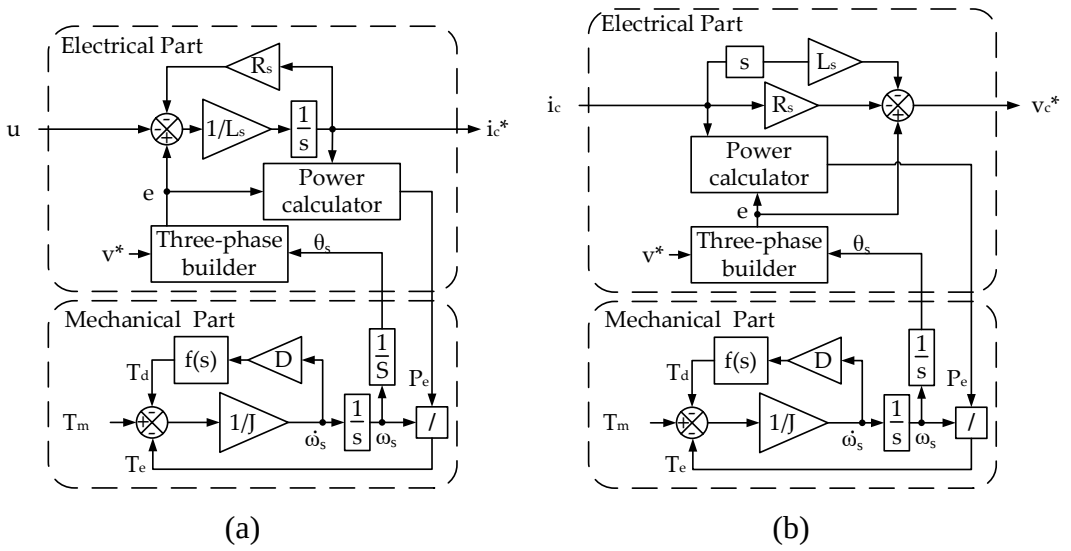


Figure 2.23. VISMA methods: (a) voltage–current model of VISMA method 1 [85], (b) current–voltage model of VISMA method 2 [68]

VISMA method 2 was created to overcome the stability problems of VISMA method 1 [72]. Moreover, the output of VISMA method 2 is a voltage that improves its black start capability compared to that of method 1. A comparison of both methods is given in the literature [68].

2.6.5.1.2 Synchronverter

Synchronverter is another high-order VSM model, which was invented by Prof Zhong as an improvement to VISMA method 1. Thus, both synchronverter and VISMA method 2 were created during the same period. According to the authors in [74], the implementation of synchronverters requires energy storage at the DC side. Figure 2.24 shows the schematic of a synchronverter, where current i_c and voltage u are measured at the PCC to create the converter voltage v_c. The converter frequency and angle are calculated using a synchronization loop similar to the mechanical part of the VISMA methods. The synchronization loop uses the active power reference P^* to calculate the mechanical torque T_m using the natural frequency ω. The damping torque is calculated by multiplying the calculated frequency with the damping factor D. The electrical torque is also calculated using the current i_c and excitation field M_{fif}. The mechanical inertia J is then used with the equivalent torque to calculate the converter frequency. The converter voltage is calculated using the voltage and reactive power control loops.

The voltage control loop takes the voltage error and creates a relevant reactive power based on droop gain D_q. Meanwhile, the reactive power loop calculates the field excitation $M_f i_f$ using the gain K from the voltage loop output, reactive power reference Q^*, and reactive power calculated using the converter frequency and field excitation output. The PLL in this structure is used only when the system starts, as discussed in [74].

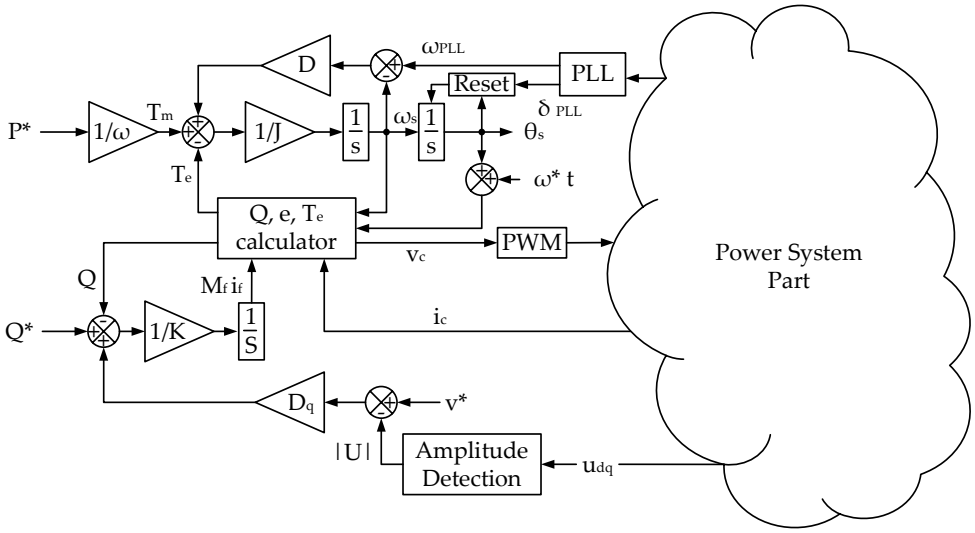


Figure 2.24. Schematic of synchronverter control [99]

2.6.5.1.3 KHI topology

KHI topology is a high-order VSM model similar to VISMA method 1, where the automatic voltage regulator (AVR) model and governor of the KHI topology are similar to the electrical and mechanical parts of VISMA method 1, respectively. Accompanied by a phasor-based current generator, the structure calculates the current reference to be used by a current controller. Unlike VISMA method 1, the KHI topology uses PLL to support the frequency output of the governor loop. Figure 2.25 shows the schematic of the KHI topology.

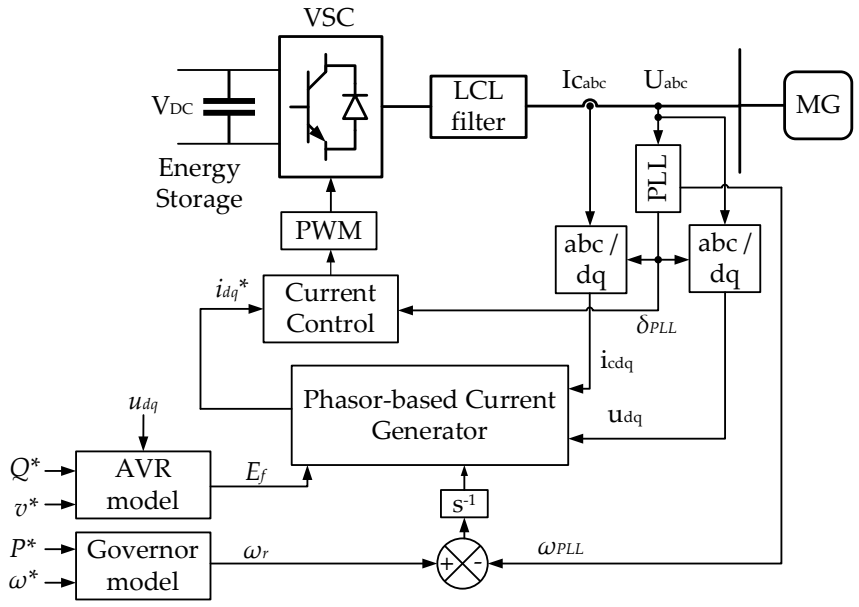


Figure 2.25. Current control-based high-order SM model [85]

2.6.5.2 Simplified-order model

Simplified-order VSM model is an implementation type that mimics the basic mechanical property (swing equation) of SMs on the power converter controller.

2.6.5.2.1 Ise's topology

Prof Ise from Osaka University, Japan, created Ise's topology, which is a simplified structure based on the swing equation of SM given by Eq. ((2.28) [73, 85]:

$$P_m - P_e = J\Delta\omega_s \frac{d\Delta\omega_s}{dt} - D\Delta\omega_s \tag{2.28}$$

where P_m is the power input of the prime mover, P_e is the output power of the synchronous generator, and $\Delta\omega_s$ is the speed of the machine. This equation represents the mechanical property of the SM discussed in the high-order VSM model implementations.

The simplified-order VSM model is implemented without the full SM electrical equations, thereby reducing the complexity arising from several control loops. Figure 2.26 shows the schematic of the control structure, where the VSM controller is used to

calculate the converter angle and the reactive power controller is used to control the converter voltage.

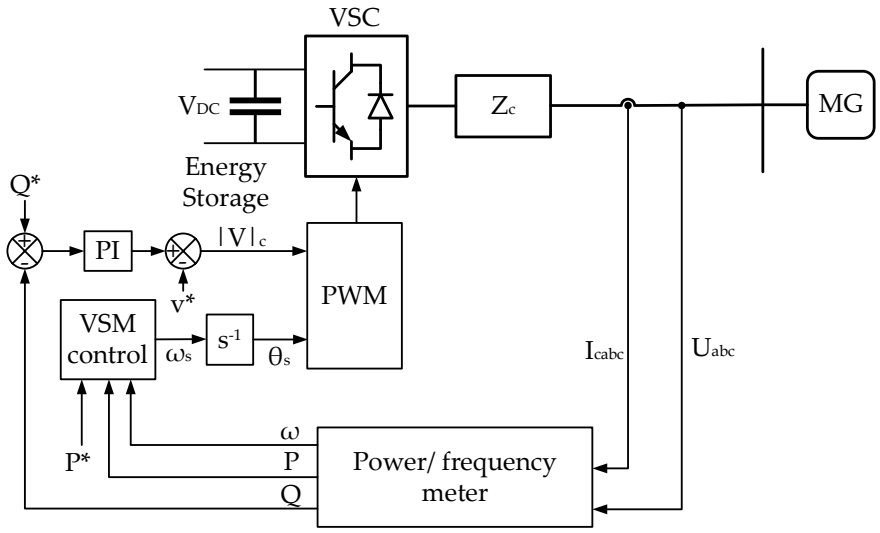


Figure 2.26. Simplified-order VSM structure [85]

The simplified-order model is used in different applications [86, 100-108]. PLL was included in the original Ise's structure but is removed in modern control structures. However, PLL is usually required at the starting of the power converter.

2.6.5.2.2 Synchronous power controller

Synchronous power controller (SPC) is another type of simplified-order VSM model implemented using an inner current loop. Figure 2.27 shows the schematic of a SPC structure [89, 90]. The SPC structure has an active and reactive outer loop controllers, with the addition of virtual impedance and current controller blocks. Virtual admittance is used as a filter stage for the current measurement, and it can replace the filters used to decrease the ripples and transient disturbances.

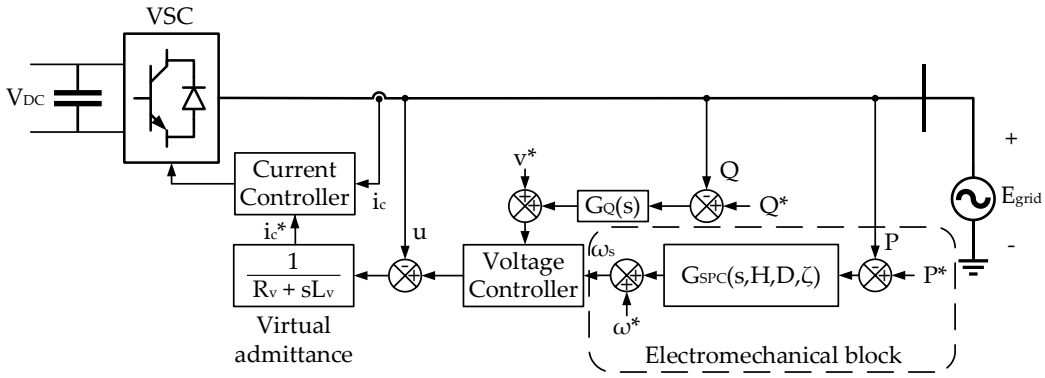


Figure 2.27. Synchronous power controller scheme [90]

2.6.5.2.3 VSYNC topology

VSYNC topology originated from the VSYNC European Project [92]. Figure 2.28 shows the control schematic of the topology, which uses control parameters J and D as the inertia and damping factors, respectively, and J_q and D_q as the inertia and damping of the reactive power loop.

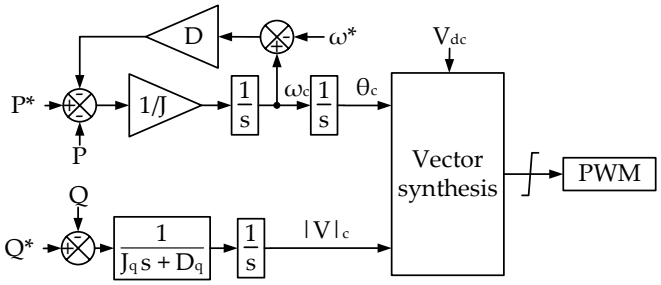


Figure *2.28*. VSYNC block diagram [109]

Summary of the VSM implementations

Table 2.3 summarises the control blocks besides the VSM primary blocks. The table considers the various VSM types described earlier, which are divided into two categories: high-order and simplified-order VSM models. In the high-order VSM model, the absence of the active/reactive outer loop requires extra control loops to define the active and reactive operating powers required for the VSC connected to renewable energy sources. Moreover, the use of mechanical torque as a reference requires an accurate conversion between the electrical system and emulated

mechanical system, which requires a lot of tuning to reach perfect emulation with accurate references. Unlike the synchronverter, the KHI structure has an inner current controller that indirectly controls current through the torque control loop. This makes the KHI structure more similar to the standard vector controller with different outer loops; however, the disadvantages of the standard current controller can also extend to the KHI structure. Although the synchronverter has no current control loop, its implementation is complex because it requires several control loops with high-order equations (above the fourth order). The simplified-order VSM model is preferred as it can be easily applied and tuned; thus, it can be built using a second-order or third-order equation. In this category of VSM models, the main control loops discussed are the outer active/reactive power loops, inner current control loop, and PLL. Most of the implementations use PLL at the beginning of operation; however, this is not required throughout the operation.

Table 2.3 VSM implementation summary

VSM implementation		Active and reactive outer loop	Inner current loop	Using a PLL	General comments
High-order VSM model	VISMA method 1	No	Can be used after the control structure	No	Poor black start capability
	VISMA method 2	No	Inherent	No	Improved black start capability
	KHI	Yes	Yes	Yes	-

	Synchronverter	Yes	No. The current can be indirectly controlled through the torque control loop	Can be used at the beginning of operation or during the entire operation	–
Simplified-order VSM model	ISE	Yes	No	At the beginning of operation	–
	SPC	Yes	Yes	At the beginning of operation	–
	PSL	Some use active power, whereas others use both active and reactive powers	In some implementations	At the beginning of operation	–
	VSYNC	Yes	No	At the beginning of operation	–

Table 2.4 presents the classification of the VSM control methods, which was originally introduced in [110]. In the table, the implementations are classified as high-order and simplified-order models. The columns show structures with a direct PWM (the control structure output is voltage), structures with cascaded voltage and current, and structures with a current vector reference.

Table 2.4 Classification of the references in the literature for VSM controls [110]

Model output / VSM implementation		Direct PWM	Cascaded voltage and current controllers	Current vector reference	General comments
High-order model	Seventh-order or fifth-order reduced-order SM model (second or third order) combined with mechanical dynamics	Voltage output formulation of the VISMA concept [68] and synchronverter concept as in [74],[82] and others by the same authors. Also in [83], [111],[75]. Similar concept in [56] and others [76], [77], [78],	Possible	VISMA concept as in [64], [93], [65], [66], [67], [68], [69], [70], [71], [112].	Voltage amplitude is provided by a reactive power control loop.

		[79], [80], [81].			
Simplified-order model	Second order model-swing equation and voltage amplitude provided by the reactive power controller	Ise's topology [100], [101], [102], [103], [113], [105], [107]. VSYNC project [92], [114], [91], [115], [116], [117]. Also in [118], [119], [120], [121].	Analysed in [122]. Ongoing study of control system tuning in [123].	A similar concept as in [124], [95].	Simple implementation that can be combined with any control scheme.

2.7 Review of the fault ride-through capability of VSM

The FRT of a grid-forming converter is essential for grid-connected applications. After the huge penetration of the renewable energy generation interfaced with the AC grid using a converter, electrical grid codes require that these generation types must contribute in large disturbance events (e.g. electrical faults). In Great Britain, new specifications for grid-forming converters have been suggested [125], in which the converter should respond within 5 ms of the voltage disturbance in case of faults [126]. Moreover, the converter should be able to absorb 2% of the unbalanced current without any alterations in the voltage source waveforms. However, maintaining the grid-forming capability during faults is not strictly mentioned within the specifications. This leads to infinite possibilities for creating a FRT-capable grid-forming converter, including losing the grid-forming capability during faults.

During faults, the main objective of FRT is to maintain the current within acceptable limits [127], which is vital because the thermal capacity of the semiconductor switches of the power converter is limited [128]. Meanwhile, synchronization stability during faults is a challenging problem [54]. The research community is addressing this problem by either considering an external or internal solution. The external solution may require extra hardware to be added to the power system, which operates during faults. The authors in [129] proposed a bridge-type fault current limiter that acts only on the fault current. Another approach was used by the authors in [130], and they proposed an external stabilizer to externally support the FRT of the VSC. Other authors in [131] suggested using smart transformers to improve the FRT. Hence, the external solution can improve the FRT of any type of power converter control. However, adding extra hardware to the system is not cost-effective, especially if this service can be provided by the existing VSC. Therefore, converter software modification based on the implementation of the control structure is the most common approach for grid-forming converters. In Section 2.6, different implementations for grid-forming controllers were explained, and each type had a different behaviour during faults. Thus, a new classification can be made for the FRT of grid-forming converters according to the controller implementation and capabilities. The main categories of this classification are grid-forming converters with an inner current control loop [110, 127, 128, 132-140], as shown in Figure 2.29(a), and control structures without an inner current control loop [141-147], as shown in Figure 2.29(b).

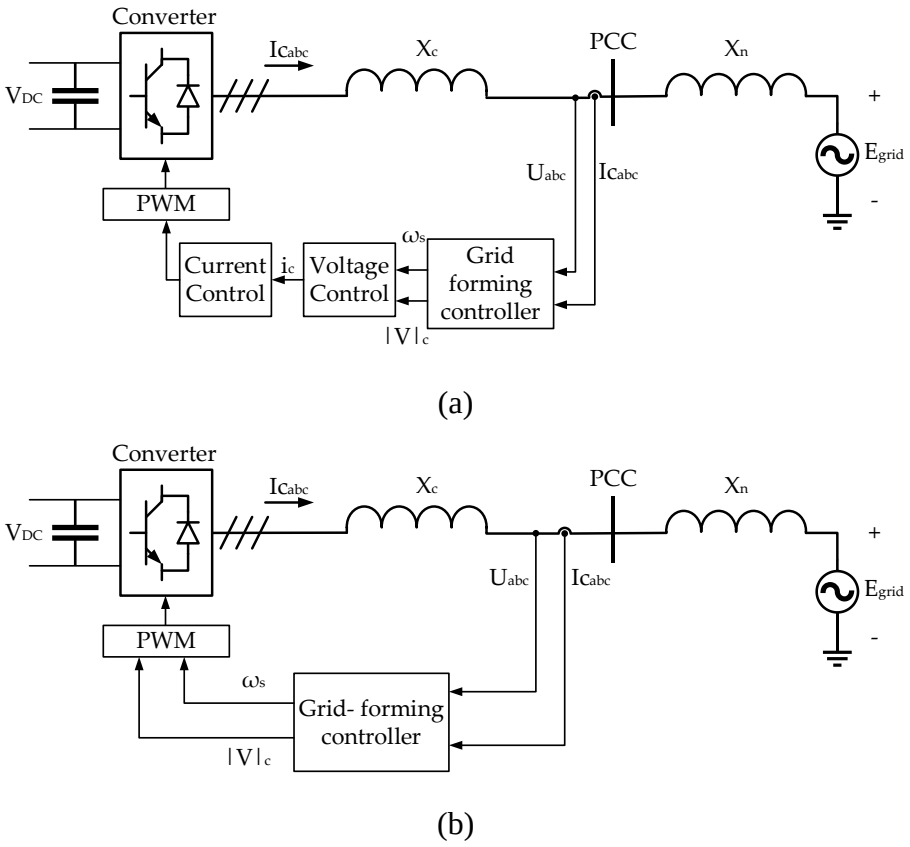


Figure 2.29. Grid-forming converters with FRT classification: (a) grid-forming converter with an inner current loop, (b) grid-forming converter without a current control loop

In the grid-forming converter with inner current control loop, the current is accurately calculated because the current controller facilitates this process. However, current limit needs to be set to avoid overcurrent during large disturbances. Some authors saturated the current loop references [128, 132, 134-140, 146-153] either by traditional saturation (limiting the maximum and minimum values) or by adaptive saturation based on damping gains to decrease the references in case of faults. Adaptive saturation is one form of virtual impedance that modifies the references of the current or voltage controller based on constant or variable gains [127, 128, 132-134, 136, 139, 140, 146-148, 150, 151, 153-155]. Some authors [127, 128, 132, 134, 136, 139, 140, 147, 150, 151, 153] suggested using both techniques to ensure current limitation during faults. Furthermore, some authors suggested maintaining the grid-forming control while changing the references during faults [127, 134, 136, 148], whereas other authors suggested disabling the grid-forming loops and switch control mode to achieve faster

dynamics [132, 136, 137]. Figure 2.30 shows a general control structure of the common techniques used to limit current. The traditional saturation block is used to limit the current references of the current controller, and two types of virtual impedances are shown, according to the literature, representing the two uses of the virtual impedance according to the desired behaviour. The nominal references of the grid-forming block are P* and Q*; meanwhile, some authors suggested that these references can be changed to P_f* and Q_f* during faults. Moreover, the grid-forming block can be substituted during faults so that the fault control block is activated to change the output voltage V and frequency ω to fault voltage V_f and fault frequency ω_f, respectively.

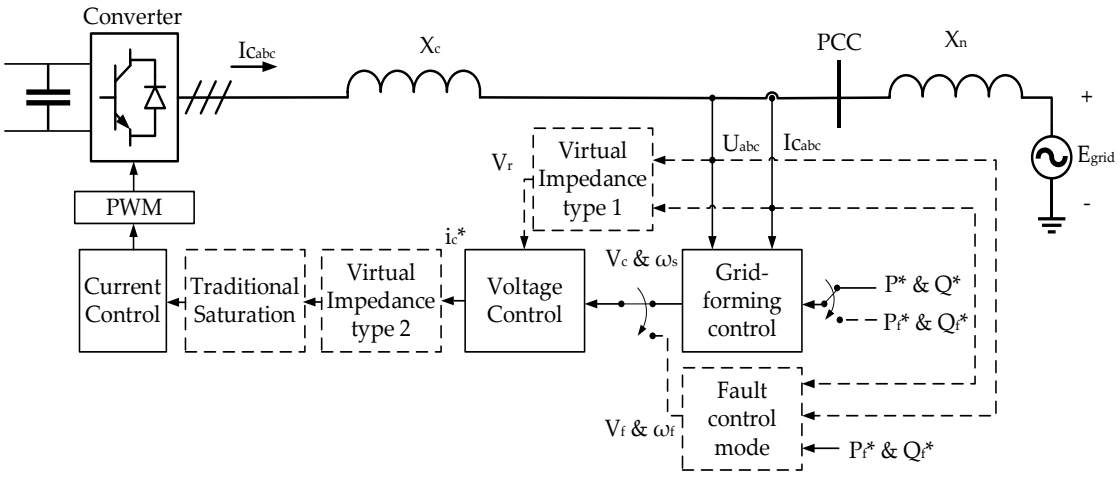


Figure 2.30. General structure of a grid-forming controller with an inner current control loop with the most common current limitation strategies

Several researchers have adopted grid-forming controllers with an inner current control loop; however, some of these controllers have certain limitations. The authors in [156, 157] reported an unstable behaviour related to the virtual impedance, and other authors in [135, 158] reported instability issues related to the current reference saturation. In addition, the authors in [159] reported that a grid-forming controller with an inner current control loop requires careful tuning, which can increase the implementation complexity of the control structure, especially for low switching frequencies.

In this thesis, the grid-forming controller without an inner control loop was adopted. This controller can emulate inertia, avoid PLL problems, operate in weak grid conditions, and avoid the limitations of the current control loop. However, the absence of current control loop imposes a significant restriction on the current limitation capability during faults. The authors in [146, 147] used voltage oscillator topology to emulate the VSM behaviour. Although no current control loop was added, the voltage oscillator gains changed to emulate the grid-following behaviour and limit the current during faults. Moreover, the authors in [144, 145] developed an optimal voltage regulator with an impedance shaping whose behaviour changes under fault conditions to limit the fault current. Other authors [142, 143] introduced a grid-forming converter without a current controller, which switches to grid-following mode with a current controller during faults to mitigate the fault current. Figure 2.31 shows a simple representation of the behaviour of a grid-forming control structure during faults.

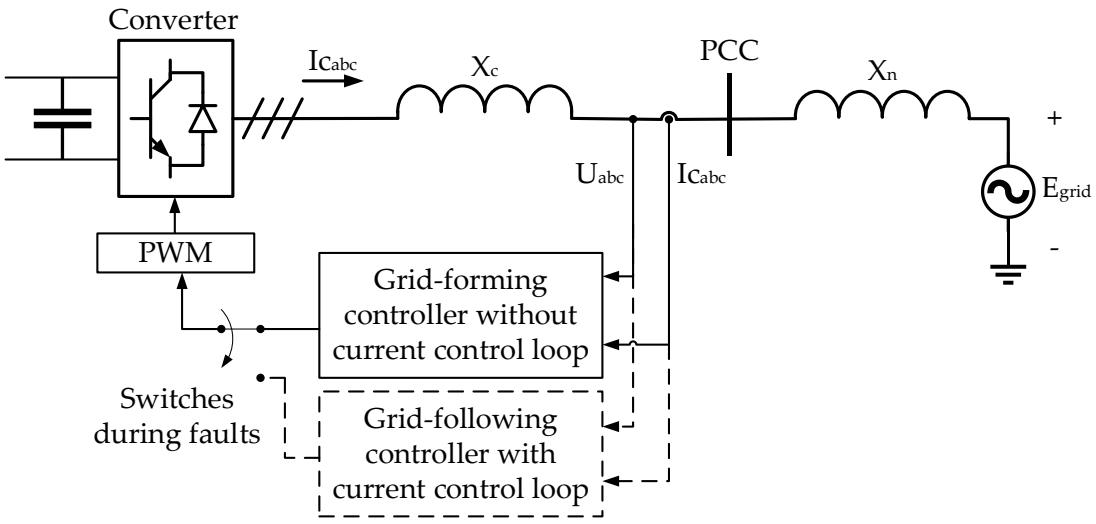


Figure 2.31. Schematic of a grid-forming controller without an inner control loop with FRT strategy

Table 2.5 summarizes the FRT strategies for grid-forming converters based on the previous discussion. The solutions proposed in the literature and references are also included in the table. The table can be used as a reference for grid-forming FRT strategies.

Table 2.5 Summary of the grid-forming FRT classifications

Grid-forming FRT strategies	
Structure with an inner current control loop in normal conditions [110, 127, 128, 132-140]	Structure without an inner current control loop in normal conditions [141-147]
• Virtual impedance [127, 128, 132-134, 136, 139, 140, 146-148, 150, 151, 153-155] • Current reference saturation [128, 132, 134-140, 146-153] • Both virtual impedance and current saturation [127, 128, 132, 134, 136, 139, 140, 147, 150, 151, 153] • Change in references during faults [127, 134, 136, 148] • Grid-forming mode is disabled [132, 136, 137]	• Control mode switch [142, 143, 146, 147, 160]

2.8 Discussion

Although there are several grid-forming controller implementations, the most commonly used are VSM structures because they inherently provide inertia and damping similar to the traditional SM behaviour. Simplified-order VSM structures seem to be more applicable in reduced control loops, indicating easier tuning. Simplified-order VSM models without an inner current control loop, such as ISE, VSYNC, and PSC can be more stable in a wide range of grid strengths as the fast dynamics of the inner current controller is not included. Therefore, these models can be easily represented as a voltage source, which is ideal for a grid-forming converter. However, the absence of an inner controller leads to poor and unstable response during faults.

Furthermore, based on the FRT strategies for grid-forming converters with a current controller, some authors implemented the current controller in positive sequence only [127, 128, 133, 135-140, 148, 150, 151, 153, 155], whereas other authors also included negative sequence controllers [132, 134, 149, 152]. Most of the authors preferred the positive sequence controller only because it is easier to implement and tune. However, because the grid code requires injecting a small percentage of unbalanced voltages, negative sequence has more compliance with the grid code. As stated earlier, the focus of this thesis is on VSM implementations without a current controller, which have better performance during normal conditions. According to the literature, in the absence of a current controller, an alternative control mode is required to achieve current limitation [142, 143, 146, 147, 160]. In the next chapter, possible alternative control modes that can be used to determine the best controller in severe fault conditions will be discussed.

The analysis will be more focused on simulations as almost all the authors used simulations to verify the proposed strategy. Nevertheless, a power–angle curve will be used to justify the instability of VSMs without a current controller during faults as discussed in [133, 135, 139, 153, 155]. Moreover, a phase plane will be used to show the synchronization stability of different synchronization techniques [141, 146, 161]. Some of the authors in the literature ignore asymmetrical fault assessments [128, 131, 133, 135, 136, 138-141, 143, 146-148, 150, 155], which are required to validate the FRT strategy. Therefore, both symmetrical and asymmetrical faults will be used to assess the proposed FRT strategy [127, 132, 134, 142, 144, 145, 149, 151-153, 160]. In addition, few authors discussed fault conditions in weak grids [127, 131-140, 142, 144, 145, 149, 151-153, 155], whereas other authors discussed only the behaviours of symmetrical faults in weak grids [128, 141, 143, 146-148, 150]. In this thesis, the results of symmetrical and asymmetrical faults in weak grids will be validated. Moreover, this thesis will focus on steady-state and transient fault currents [127, 128, 132, 133, 135, 136, 138-141, 143, 146-148, 150, 153, 155, 160]. Furthermore, the effect of the algorithm used to switch between controller modes was not considered in past studies. In this thesis, the effect of FDA will also be discussed.

2.9 Chapter summary

In this chapter, the challenges of high renewable energy penetration were discussed, as well as VSC control structures with multiple control approaches. These approaches included the traditional vector current controller with active and reactive outer loops as the ideal form of grid-following converter. Further, grid-forming converter structures were introduced, such as droop controller, power synchronization controller, inducverter, virtual oscillator control, and VSM. VSM can inherently provide several ancillary services, including inertia and stable operation in weak grids. The VSM implementations were classified into two categories. The first category is the high-order VSM model, which emulates the mechanical and electrical characteristics of SMs. The structures in this category largely share the same features; however, some differences exist in the inputs and control loops of each structure. The second category is the simplified-order VSM model, which mainly considers the mechanical equation (swing equation) of SMs. Different approaches with slightly different synchronisation loops were presented to implement the simplified-order model. Some of these structures use PLL during full operation to correct the converter angle, whereas others use PLL during the start of operation only.

Furthermore, FRT was introduced by categorizing the VSM control structure into grid-forming controllers with an inner current control loop and grid-forming controllers that switch to different control modes. The control structures with an inner current loop can limit the fault current by saturating the current references using adaptive virtual impedance or by switching the outer loops, but multiple inner current control loops can limit the VSM bandwidth. In contrast, VSM control structures without a current controller usually switch to an alternative control structure during faults. Therefore, the structure that considers the current control only when it is required (that is, during faults) is a more appealing research route.

Chapter 3

Current-Limiting VSM Structure

3.1 Introduction

There are various VSM structures, as discussed in Chapter 2. While these structures can control current using different approaches, current controller is the most dominant controller. However, some authors consider current controller with PLL as a source of instability in weak grid conditions [162]. Therefore, a VSM structure without a current controller or PLL is considered the ideal solution for preventing instability in weak grids, which is discussed in this chapter.

In this chapter, the VSM control structure is analysed to reveal the relationship between the controller and SM parameters. The current-limiting capability of the control structure is investigated, and a limiting strategy for the steady-state operation is introduced. Furthermore, several FRT implementations are introduced to explain the possibility of limiting fault current without a current controller. The implementations are:

- Limiting the balanced fault current by using backup control loops.
- Developing a VSM structure capable of injecting reactive current during faults.

This chapter is divided into the following sections: In Section 3.2, the controller architecture is described. In Section 3.3, the normal operation of the current-limiting technique is discussed. In section 3.4, the VSM response to faults is studied. In Section 3.5, the FRT technique is presented; and this chapter is summarised in Section 3.6.

3.2 Description of the control structure

The controller used in this chapter emulates the SM using a variation of the swing equation to create an APL and AVR for the voltage controller. Figure 3.1 shows the simplified-order VSM model, which is similar to the simplified-order VSM structure discussed in Chapter 2. The proposed controller is created using two control loops with PI controllers, and it is reliable, simple to analyse, and tune. Moreover, the control structure does not use current control loop nor PLL to obtain the angle [85], thereby avoiding the problems associated with PLL (e.g. PLL instability in weak grids) [163, 164]. The control structure has two different loops: one loop controls the voltage magnitude at the PCC while the other loop controls the power acting on the converter voltage angle. The description of the controller is provided in the following sub-sections.

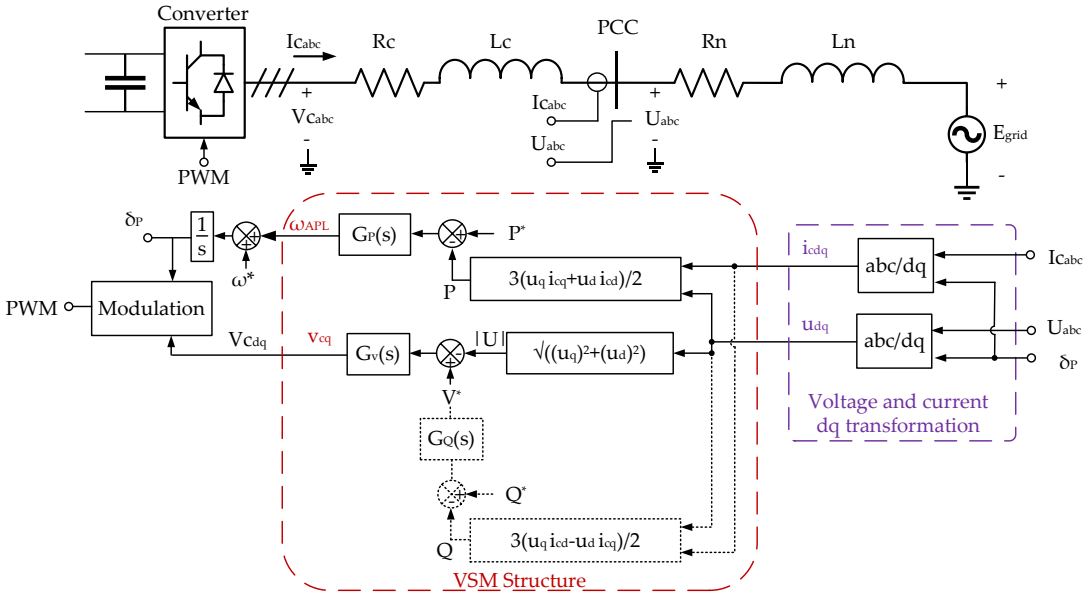


Figure 3.1. Simplified-order VSM control structure

3.2.1 APL control

The VSM structure shown in Figure 3.1 is a simplified version of SM emulation and is based on the PSC in [165]. The APL controller consists of a PI controller that can be easily tuned, which calculates the converter angle to exchange a particular amount of active power. A PI controller is used in this control instead of a P controller to

emulate both the inertia and damping behaviours of the swing equation. The control structure comprises an APL PI controller $G_P(s)$ given by Eq. (3.1):

$$G_P(s) = k_{p-P} + \frac{k_{i-P}}{s} \tag{3.1}$$

where $k_{p\text{-}p}$ and $k_{i\text{-}p}$ are the proportional and integral gains of the PI controller, respectively.

The gains tuning of an APL control can be calculated from the SG swing equation. The first step to finding the equivalency is to manipulate the SG swing equation given by:

$$\frac{\Delta\theta_c}{P_m - P_e} = \frac{1}{\frac{2H\,S_{rated}}{\omega_s}\,s^2 + Ds} \tag{3.2}$$

where H is the inertia constant, S_{rated} is the rated complex power, ω_s is the rotor rated speed or synchronous rated frequency, D is the damping factor, θ_c is the rotor or converter angle, P_m is the mechanical power, and P_e is the electrical power.

The swing equation can be used as a forward path in the closed-loop transfer function, and the gain k_m is the synchronizing torque coefficient. The natural frequency ω_{n_1} and damping factor ζ_1 of the SM are given by:

$$\omega_{n_1} = \sqrt{\frac{\omega_s}{2H}\frac{k_m}{S_{rated}}}, \zeta_1 = \frac{D}{2}\sqrt{\frac{\omega_s}{2H\,S_{rated}k_m}} \tag{3.3}$$

A similar relationship exists for the VSM APL, which represents the relationship between the APL and converter angle. The closed-loop natural frequency ω_{n_2} and damping coefficient ζ_2 of the VSM APL are expressed by:

$$\omega_{n_2} = \sqrt{k_{i-p} k_m}, \zeta_2 = \frac{k_{p-p}}{2} \sqrt{\frac{k_m}{K_{i-p}}} \tag{3.4}$$

Finally, the closed-loop transfer function parameters in Eqs. (3.3) and (3.4) are equated so that $\omega_{n1} = \omega_{n2}$ and $\zeta_1 = \zeta_2$.

Therefore, the integral coefficient k_{i-p} can be tuned by:

$$k_{i-p} = \frac{\omega_s}{2H\ S_{rated}} \tag{3.5}$$

Additionally, the proportional coefficient k_{p-P} can be tuned by:

$$k_{p-p} = \frac{D\ \omega_s}{2H\ S_{rated} k_m} = D \frac{k_{i-p}}{k_m} \tag{3.6}$$

Figure 3.2 and Figure 3.3 show the effects of changing the PI parameters of the APL, and the simulation parameters are presented in Table 3.1. The active power reference was changed from 3 to 5 MW at *t* = 10 s. Figure 3.2 shows the active power response to three different *D* values. It can be seen that the increase in damping decreases the oscillations. Therefore, the change in the proportional gain changes the damping as presented in Eq. (3.6). Moreover, the waveforms in Figure 3.3 shows the effect of changing the inertia *H* while keeping the damping constant, so that the increase in inertia decreases the RoCoF. Therefore, the inertia is changed by changing the integral gain as discussed in Eq. (3.5).

Table 3.1. Simulation parameters

Parameter	**Value**
Lc	0.0398 H
Rc	1.25 Ω
$k_{p\text{-}P}$	10^{-6}
$k_{i\text{-}P}$	10^{-6}
$k_{i\text{-}V}$	0.6
$k_{p\text{-}V}$	8
Nominal value of U_{abc}	20.4 kV (peak)
Nominal value of Ic_{abc}	160 A (peak)

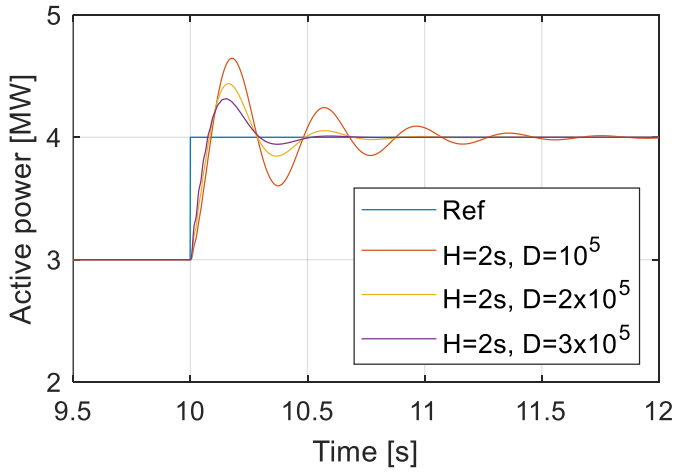


Figure 3.2. Active power response to varying proportional gain of the APL PI controller

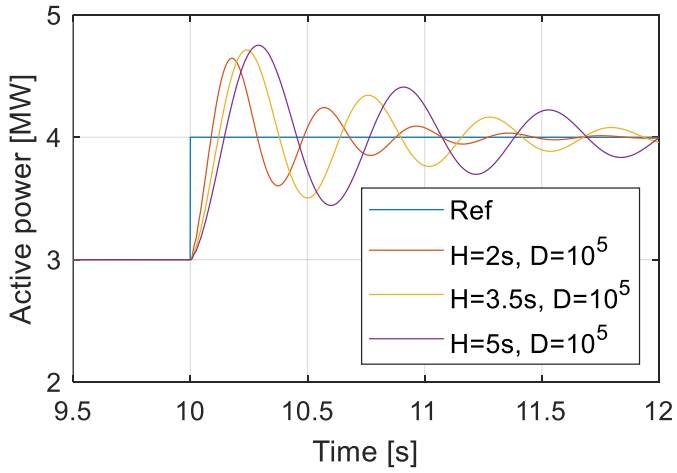


Figure 3.3. Active power response to varying integral gain of the APL PI controller

3.2.2 Voltage loop and reactive power control

The voltage magnitude of the converter is controlled using a PI controller $G_V(s)$, which can be tuned as described in [165].

The voltage controller equation is given by:

$$G_V(s)(V^* - |U|) = v_{c_q} \tag{3.7}$$

where V^* is the voltage reference, $|U|$ is the measured voltage at the PCC, and Vc_q is the converter voltage magnitude.

$G_V(S)$ is a PI controller, which is described as:

$$G_V(s) = \frac{k_{p-V}s + k_{i-V}}{s} \tag{3.8}$$

where $k_{p\text{-}V}$ and $k_{i\text{-}V}$ are the proportional and integral gains of the voltage loop PI controller, respectively. Figure 3.4 shows the block diagram of the voltage controller. The PI controller is used to control the voltage while keeping the error to a minimum. The output of the PI controller is saturated to keep the voltage within the standard voltage limits.

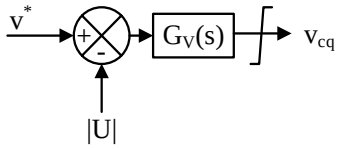


Figure 3.4. Voltage loop controller emulating an automatic voltage regulator

Meanwhile, a reactive power controller can replace the voltage loop. Figure 3.5 shows the block diagram of a reactive power controller with voltage loop.

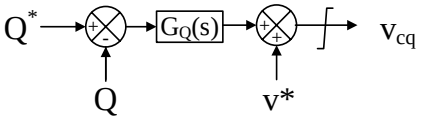


Figure 3.5. Reactive power controller with voltage loop

The reactive power controller $G_Q(s)$ is a PI controller, and it is given by:

$$G_Q(s) = \frac{k_{p-Q}s + k_{i-Q}}{s} \tag{3.9}$$

where $k_{p\text{-}Q}$ and $k_{i\text{-}Q}$ are the proportional and integral gains, respectively. This controller is used to control the reactive power signal, and the output is added to the nominal voltage v^*. The output is a voltage signal that can be controlled using the voltage controller discussed earlier.

Figure 3.6 and Figure 3.7 show the reactive power responses for varying control parameters of the reactive power controller. The reactive power reference was changed from 0 to 2 Mvar at 10 s. The figures show that a decrease in the proportional gain caused a decrease in the steady-state time, whereas an increase in the integral gain led to an increase in the initial oscillations. Therefore, the recommended tuning values are those of the low proportional and integral gains.

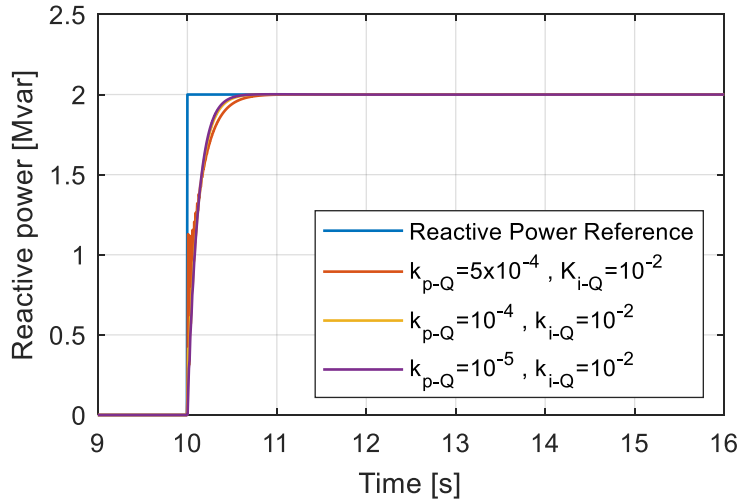


Figure 3.6. Reactive power response to varying proportional gain of the reactive power loop PI controller

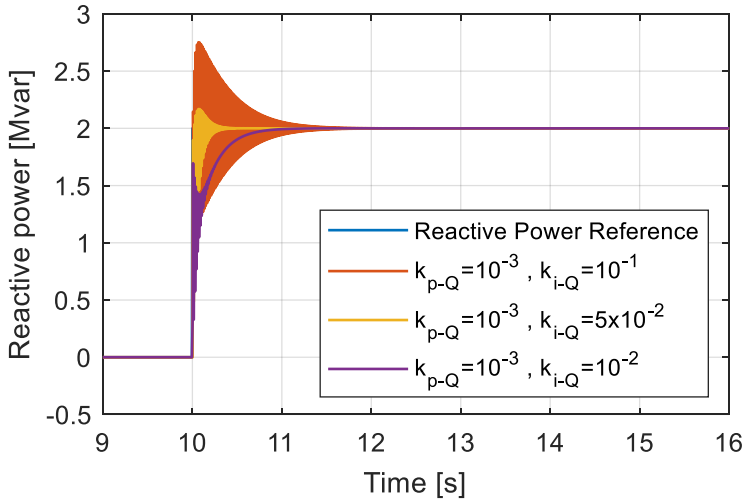


Figure 3.7. Reactive power response to varying integral gain of the reactive power loop PI controller

3.2.3 Measurements and controller parameters

The voltage and current in the *abc* frame are transformed into the *dq* frame using Park transformation as follows:

$$u_q = \frac{2U_a}{3}\cos\theta + \frac{2U_b}{3}\cos(\theta - \frac{2\pi}{3}) + \frac{2U_c}{3}\cos(\theta + \frac{2\pi}{3}) \quad (3.10)$$

$$u_d = \frac{2U_a}{3}\sin\theta + \frac{2U_b}{3}\sin(\theta - \frac{2\pi}{3}) + \frac{2U_c}{3}\sin(\theta + \frac{2\pi}{3}) \quad (3.11)$$

where u_d and u_q represents the dq components of the voltage at the PCC, and U_a, U_b, and U_c are sinusoidal voltages to the PCC voltage. The same equations are also used to transform the currents from abc to dq frame. The voltage magnitude $|U|$ is calculated using:

$$|U| = \sqrt{\left(U_q\right)^2 + (U_d)^2} \quad (3.12)$$

The active and reactive powers are calculated using the following equations:

$$P = \frac{3}{2}\left(u_q i_{c_q} + u_d i_{c_d}\right) \quad (3.13)$$

$$Q = \frac{3}{2}\left(u_q i_{c_d} - u_d i_{c_q}\right) \quad (3.14)$$

The controller parameters should be chosen according to the converter capability and system limitations. Meanwhile, the maximum values of the voltage loop PI parameters are limited by the converter voltage limit, whereas the minimum values are limited by the grid voltage recommendations and standards. Additionally, the APL PI parameters must be tuned with a low bandwidth similar to a SM. The energy storage for inertia emulation should also be considered when choosing the power controller gains.

3.3 Steady-state current limitation algorithm

The proposed VSM structure can control current through an APL. However, a steady-state current-limiting technique is required to maintain the converter safety during steady-state conditions. In case of voltage variations, the control structure references can cause an unexpected increase in current. Therefore, a reference limitation

algorithm based on active/reactive power prioritisation is introduced. The algorithm uses voltage measurement, active power, and reactive power to predict current, subsequently determining whether to maintain or limit the required references according to the predefined priority. The proposed algorithm does not require a current controller, which enables the VSM structure to operate under weak grid conditions.

The active or reactive current priority is selected according to the grid code. The references for the converter controller are active and reactive power, and the apparent power is defined as:

$$|S| = \sqrt{P^2 + Q^2} \tag{3.15}$$

where $|S|$ is the magnitude of the complex power, P is the active power reference, and Q is the reactive power reference. References P and Q are the inputs of the algorithm. The current magnitude is calculated by:

$$|S| = 3|U||I|_{cal} \tag{3.16}$$

where $|U|$ is the magnitude of the phase voltage measured at the PCC and $|I|_{cal}$ is the phase current needed for the limitation process.

The current is compared to a maximum value to satisfy the condition:

$$|I|_{cal} > |I|_{c\text{-}max} \tag{3.17}$$

Then, based on the prioritising sequence, the power references are recalculated using $|I|_{c\text{-}max}$ in Eqs. (3.16) and (3.17) to yield:

$$|S|_{new} = |U||I|_{c-max} \tag{3.18}$$

If the reactive power priority is activated, the new active power is recalculated using:

$$P_{new} = \sqrt{|S|_{new}^2 - Q^2} \tag{3.19}$$

while keeping the reactive reference constant. In contrast, if the active power priority is activated, the reactive power is calculated using:

$$Q_{new} = \sqrt{|S|^2_{new} - P^2} \tag{3.20}$$

while keeping the active power constant.

However, if the reference is set to zero and the current value still does not satisfy the condition in Eq. (3.17), the other power reference is decreased while maintaining the initially controlled power at zero.

Figure 3.8 shows the full controller architecture. The controller uses measured voltage, as well as the active and reactive powers, to estimate current as previously discussed.

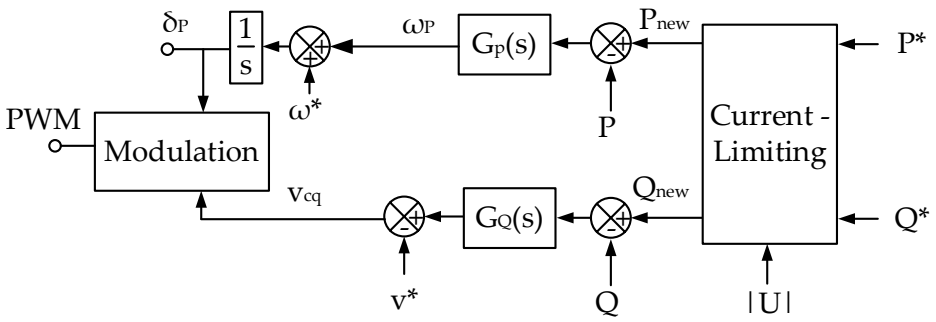


Figure 3.8. First proposed current-limiting controller

3.3.1 Simulation results

The simulation was performed using MATLAB/Simulink. The converter rating was 6 MVA and was connected to a 25-kV MV network. The power system architecture is the same as that shown in Figure 3.1, except for the control structure, which is specified in each simulation case. The magnitude of the grid voltage was changed to emulate voltage sags and three-phase-to-ground faults. Table 3.1 presents the simulation parameters.

3.3.2 Normal operation reference limitation

Voltage variations or undesired reference changes in the system can increase the current magnitude above the converter limit. Therefore, a test case was established to

ensure that current is controlled during normal operation through the power references. The controller shown in Figure 3.8 was applied to the wind turbine converter shown in Figure 3.1. The active power reference was set to 5 MW and kept constant during the simulation. Meanwhile, the reactive power reference was changed from 1 to 3 Mvar to represent voltage variations in the power system. The active power, reactive power, and current magnitude were measured at the PCC and are shown in Figure 3.9 and Figure 3.10.

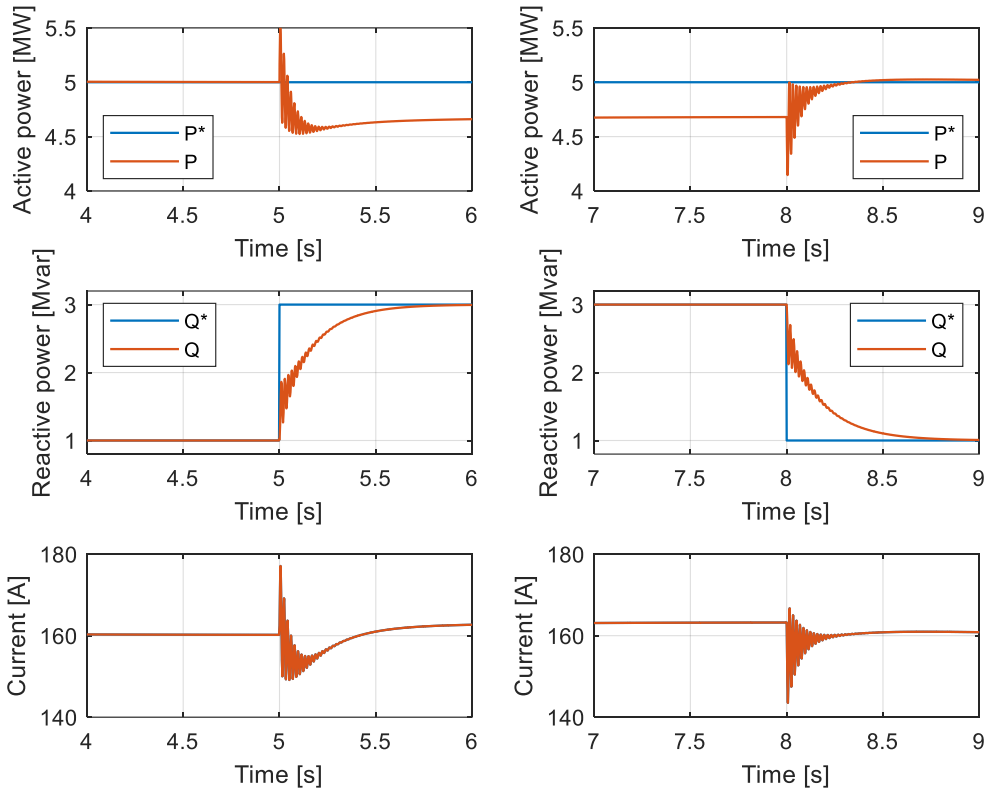


Figure 3.9. Active power, reactive power, and converter current magnitude (reactive power priority)

As shown in Figure 3.9, the algorithm reduced the active power to keep the current magnitude to the set limit (≈164 A_{peak}) while delivering the desired reactive power.

The active power priority was validated through a second case shown in Figure 3.10. The active and reactive power waveforms show the capability of the controller in reducing the reactive power and consequently limiting the current magnitude to

approximately 164 A_{peak}. The current waveforms show transients at 5s and 8s, because the change in both active and reactive power as shown in the figure.

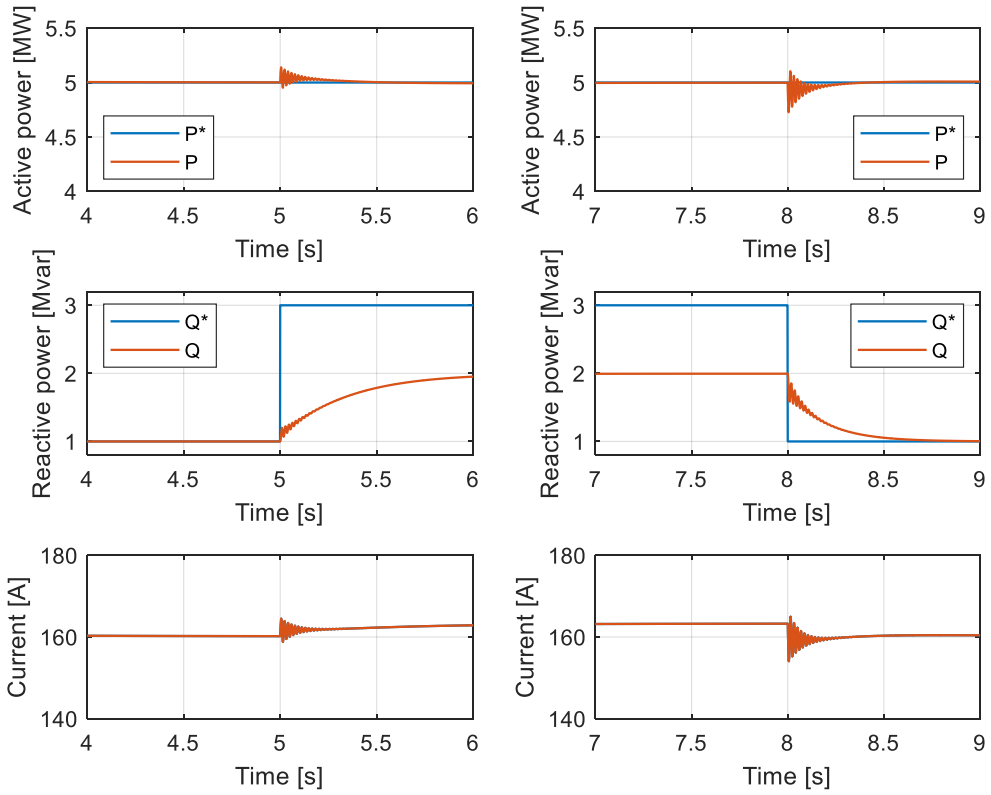


Figure 3.10. Active power, reactive power, and converter current magnitude (active power priority)

Meanwhile, the response speed of the reference in limiting the current was slow because the current was very high during the three-phase-to-ground fault from 5 to 6 s, as shown in Figure 3.11. Therefore an alternative approach is required to limit the fault current.

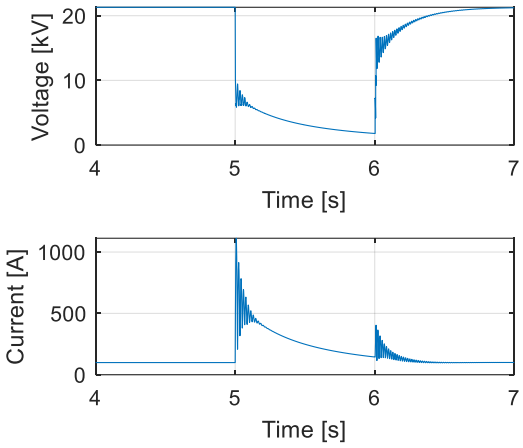


Figure 3.11. Reference limitation fault response

3.4 Simple VSM fault response

Figure 2.11 shows a grid-connected VSC controlled as VSM, and the expression for the power exchange is given by Eq. (2.17). During a severe fault, the VSC can reach a point where it acts in an isolated mode, as shown in Figure 3.12.

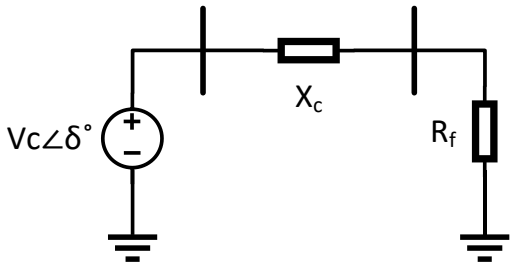


Figure 3.12. Schematic of an isolated VSC

For an isolated VSC, the current can be expressed by:

$$I_c\angle(\delta - \theta_z) = \frac{V_c\angle\delta}{Z_f\angle\theta_z} \tag{3.21}$$

The active power is expressed by:

$$P = V_c I_c \cos\theta_z \tag{3.22}$$

In this case, there is no relationship between δ and P. Therefore, the current can be directly controlled by the voltage magnitude.

A time-domain simulation was used to investigate the response of a VSM structure without a current controller. Here, a controlled voltage source was used to represent an ideal VSC without a DC side, and the grid was represented by a Thevenin equivalent using a voltage source and impedance. Figure 3.13 shows the time-domain simulation results for the voltage, current, P, Q, and change in omega. A three-phase-to-ground fault was applied from 5 to 6 s with no switching in the control structure. A significant increase in the reactive power was observed as the same voltage was applied in the voltage control as in the normal condition. However, the simulation does not consider the converter limitations, which are the DC bus voltage and the maximum converter current. Therefore, the behaviour during the fault can be different, and a power angle curve will be used to explain the difference between a saturated current control structure with and non-saturated current control structure.

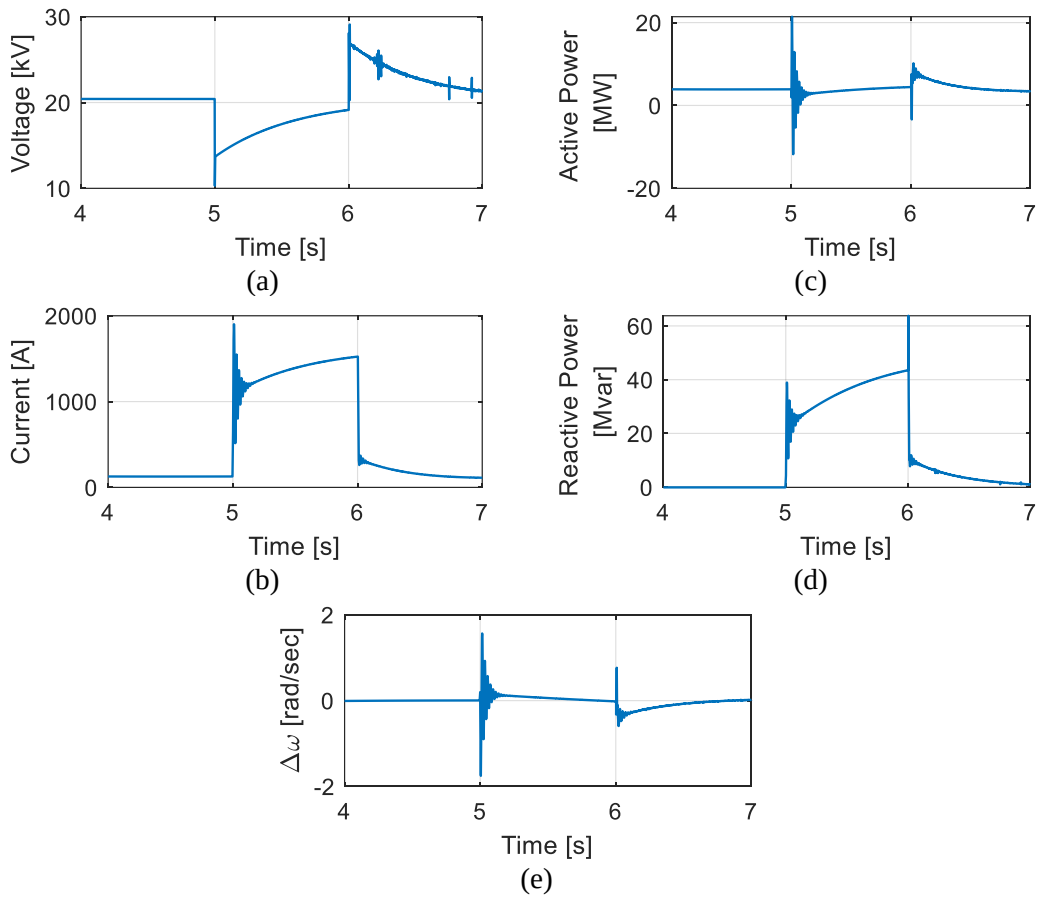


Figure 3.13. MATLAB simulation results for the response of a VSM to a three-phase-to-ground fault through the PCC (a) voltage, (b) current, (c) active power, (d) reactive power, and (e) synchronization loop output

Figure 3.14 shows the power angle curves for a VSC with no current saturation represented in blue, and a VSC with current saturation represented in red. The red curve is shifted 90 degrees from the blue curve and limited to Pc_{sat} as a result of the current saturation, so that the converter is assumed to be unity power factor as presented in [166]. The solid curves representing the operation during normal condition, and the dashed curves representing the operation during voltage sag condition. The VSC with no current saturation operates at point A, then in a voltage sag condition the operating point changes from point A to point B. Under this condition the active power is less than the active power reference, therefore the converter virtual speed accelerates and δ increases. At point C the control structure determines the next operating point either to be point D or point F. In case of a control structure with no current saturation, the converter operation moves from point C to point D. Afterwards, if the fault is cleared at point D, then the operation is moved to point E. At point E the active power is higher than P^* leading to the deceleration of the converter virtual speed, and finally the operation returns to point A. Since The problem of this scenario is the converter current at points D and E can be higher than the maximum converter current, because the control structure has no limitations on the output converter current. The second scenario is for a control structure with a current saturation, which moves the operating point from point C to point F instead of point D. This leads to decreased active power hence lower current. Afterwards, if the fault is cleared at point F, then the operation is moved to point G. The active power at point G is higher than the active power reference, that makes the converter virtual speed decelerates. The operating point is moved to point H, at which the current saturation is not applied. The converter keeps the deceleration, and the converter operation moves to point A. The second scenario keeps the current below the maximum current and maintains the current safety, therefore a FRT strategy is required to limit the current during the fault the same as the action of the current saturation.

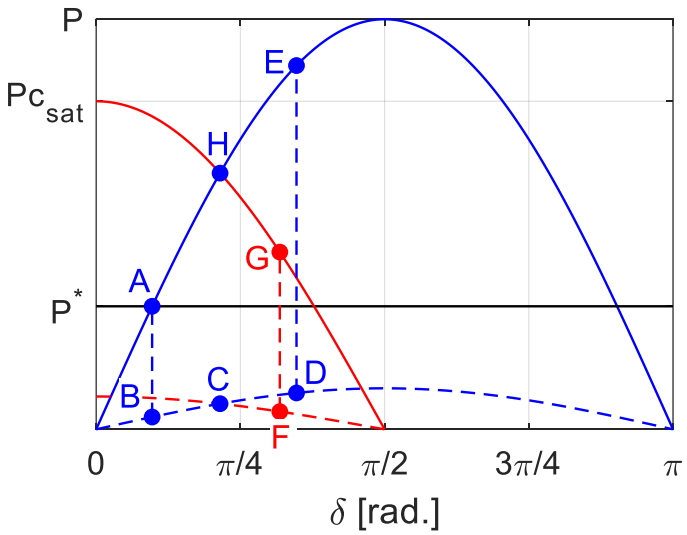


Figure 3.14. Active power curve under the normal and fault conditions

Considering another scenario in which a current controller exist, the orange line is limited below the converter limit. This case allows the converter to inject current within its capability, and with a proper selection of the current reference, the stability can be maintained during fault.

3.5 Fault ride-through strategy

One of the main requirements of a VSC is to limit current during faults and ride through the fault to support the grid. However, the simple VSM structure in Figure 3.1 cannot limit the fault current, as explained in Section 3.4. Thus, it needs to be reinforced with a FRT strategy to protect the VSC and comply with the grid code. In the next subsections, five FRT strategies are introduced to improve the simple VSM structure. In the first strategy, the APL reference is changed. In the second strategy, the voltage loop reference is changed while disabling the synchronization loop. The third strategy is commonly used in the literature, and it involves the addition of a current control loop with virtual admittance and current reference saturation. The fourth strategy involves limiting the current by feeding the PCC voltage through the converter terminals. The fifth strategy involves switching to a vector current controller. Further FRT strategies can be found in Appendix A, at which the same conclusion is obtained as the conclusion from the strategies shown in this chapter.

3.5.1 First FRT strategy

Based on the discussion in Section 3.4 and the P–δ curves in Figure 3.14, the synchronization loop is the first control loop to be modified. Because active power is reduced during faults, the first FRT modification is to change the active power reference to zero during fault. This method confirms the relationship between P and δ during faults and can be used to identify the synchronization problems of a simple VSM during faults. Figure 3.15 shows the schematic of a control structure for the first strategy in which the active power reference is changed to zero using an ideal signal. The change is highlighted with a red box, which will also be used in the other strategies. The integrators used in both active power and voltage controllers are reset using the same ideal source used to switch the active power reference.

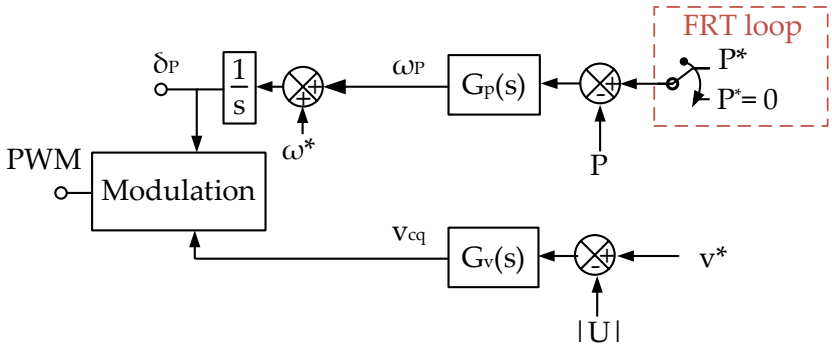
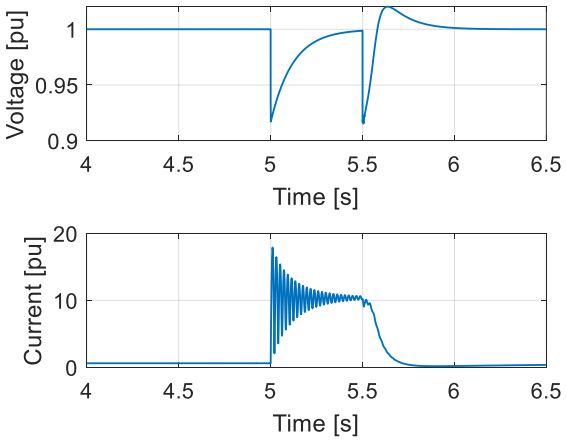


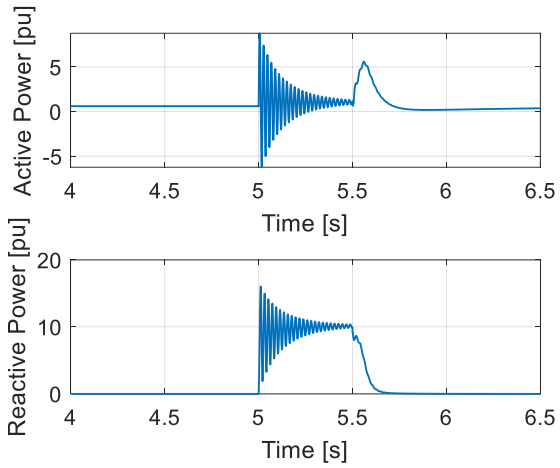
Figure 3.15. Schematic of the first FRT strategy

The active power control parameters in this simulation are the same as those presented in Table 3.1; however, the proportional and integral gains of the voltage controller are changed to 10 and 100, respectively. The control parameters were varied using trial and error to improve the output results. The control structure was tested for a 500-ms balanced fault from 5 to 5.5 s, and the results are shown in Figure 3.16. The results show that uncontrollable fault current reached 10 pu. Moreover, the voltage waveform shows that the voltage controller injected a very high current to maintain the requested voltage reference. The first observation from the results is that the voltage reference needs be changed during faults to avoid excessive current injection. The second observation is that the APL instability led to an uncontrollable current during fault as

the active power waveform in Figure 3.16(b) showed the same active power injection even after changing the active power reference to zero.



(a)



(b)

Figure 3.16. First FRT strategy results: (a) PCC voltage and current waveforms, (b) active and reactive waveforms

The APL failure can also be as a result of changing the operating mode of the VSC from grid-connected mode to isolated mode, which was a result of the solid three-phase fault between the VSC and grid. Therefore, the power angle equation can no longer be applied, as explained in Section 3.4. In conclusion, the APL should not be used during faults, whereas the voltage loop reference needs to be changed during faults. Therefore, the APL will be disabled in the following FRT strategies.

3.5.2 Second FRT strategy

This strategy is an improvement to the first FRT strategy. Here, the APL is disabled during fault, and only the nominal frequency is used to derive the converter angle. Moreover, the voltage controller reference is changed to zero to limit fault current, which is only effective for solid faults. Figure 3.17 shows a schematic of the control structure for the second strategy, where the change of the control loop is highlighted with a red box. The APL was tuned using the values in Table 3.1; however, the voltage controller was tuned to provide the best results so that the proportional and integral gains were 50 and 4000, respectively. In this case, an ideal signal was used to switch the control loops to focus on the control structure behaviour. The signal was set at the beginning of the fault and reset 20 ms after the fault clearance, in which the fault current transient is minimised. This signal was also used to reset the controller integrators at the beginning and end of the fault. The controller gains were kept constant similar to those of the first FRT strategy.

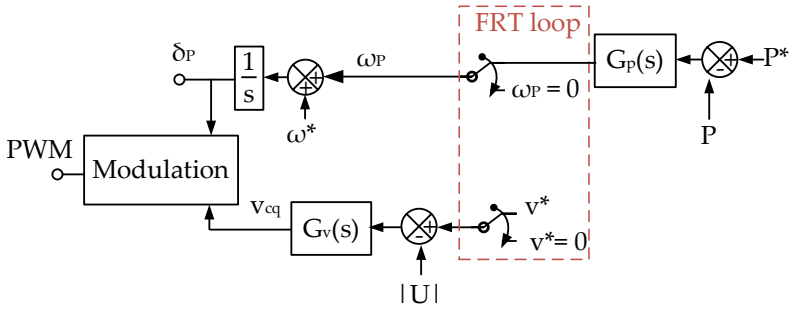
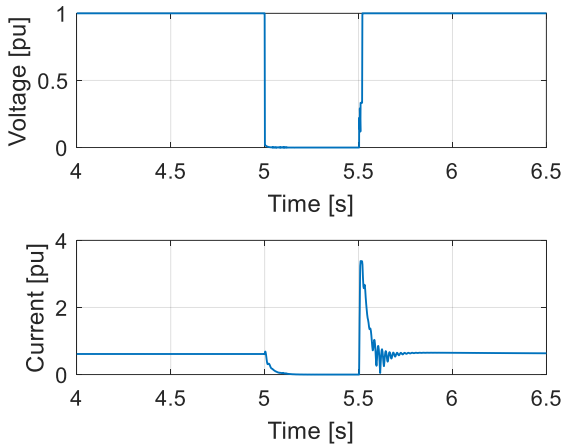
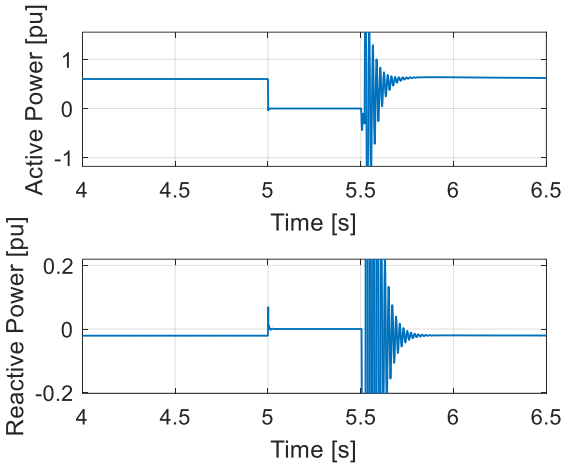


Figure 3.17. Schematic of the second FRT strategy

Figure 3.18 shows the results of the second FRT strategy for balanced faults. Although the current in this case was decreased to zero, a high transient was observed at end of the fault, which is due to the absence of a current controller. After the fault clearance with zero converter voltage, the grid current was high, requiring fast current control action. Based on the results, the VSM structure has slow behaviour, which leads to a slow decrease in the fault current, and the high transient is an indication of the necessity of incorporating a fast current controller. Moreover, the current waveforms for a single-phase fault shown in Figure 3.19 are uncontrollable, further indicating the requirement for a current control loop.



(a)



(b)

Figure 3.18. Second FRT strategy results for balanced faults: (a) PCC voltage and current waveforms, (b) active and reactive waveforms

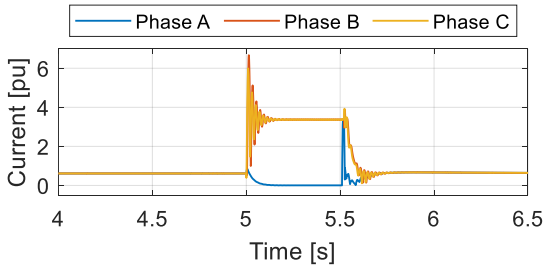


Figure 3.19. Second FRT strategy for a single-phase fault

3.5.3 Third FRT strategy

The third strategy has been adopted by several authors in the literature, and it involves the addition of an inner current control loop to boost performance during faults. The inner current loop has a fast behaviour, which limits the fault current faster than when only voltage control is used. The virtual admittance block is used to calculate the current reference through the voltage controller output using:

$$I^* = Y\ (V^* - |U|)G_V(s), Y_v = \frac{1}{R_v + sL_v} \tag{3.23}$$

where R is the virtual resistance and L is the virtual inductance. Virtual admittance can be used to shape the impedance of the VSC, and some authors have suggested various admittance parameters for current limitation. In this case, the virtual admittance parameters are constants, and a saturation block is added to avoid surpassing the maximum current limit. Figure 3.20 shows the schematic of the third FRT strategy in which the synchronization loop is switched by a simple voltage condition. The voltage condition is high when the measured voltage is below 90% of the nominal voltage, otherwise the output is low. Meanwhile, the voltage condition output is used to reset the controller integrators. The current controller $G_I(s)$ is a PI controller, and the tuning parameters for this control structure are presented in Table 3.2. The parameters were selected to provide the best performance. The change in the control structure is highlighted with red border in Figure 3.20.

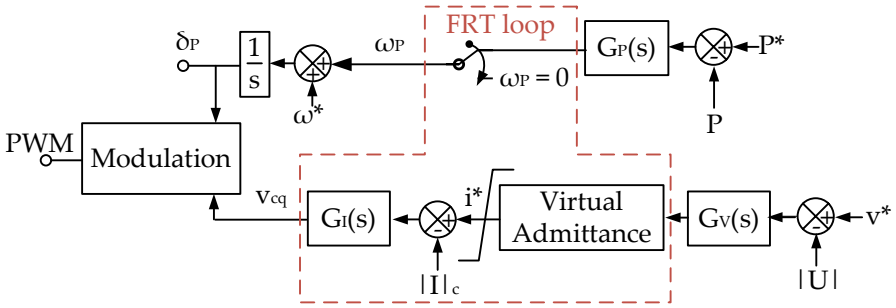
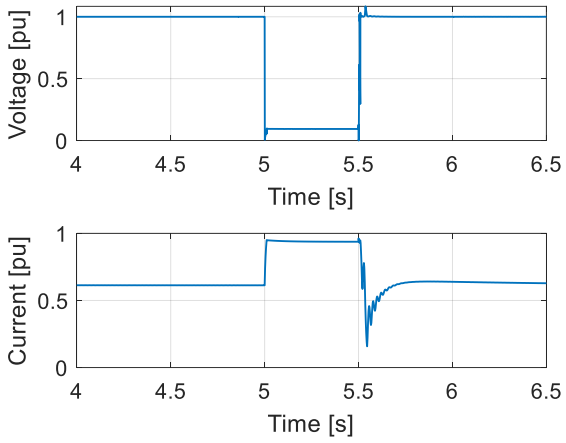


Figure 3.20. Schematic of the third FRT strategy

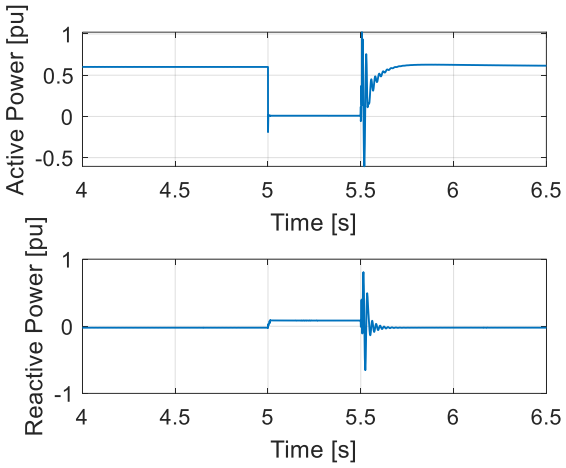
Table 3.2. Parameters of the third FRT strategy

Parameter	Value
k_{p-P}	10^{-6}
k_{i-P}	10^{-6}
k_{p-V}	10^{2}
k_{i-V}	10^{3}
k_{p-I}	8×10^{3}
k_{i-I}	8×10^{4}
R_v	120
L_v	1

Figure 3.21 shows the results for the third FRT strategy in which the current is limited to the maximum of the saturation block and the transients do not exceed 1 pu. Although the results are promising for balanced faults, the structure has low performance regarding unbalanced faults, as shown in Figure 3.22. Therefore, an alternative solution is still required to limit the current in different types of faults. In addition, the inner current control loop with fast dynamics can limit the slow VSM dynamics. Hence, adopting an alternative control loops during faults is beneficial to expanding the capabilities of the VSM structure.



(a)



(b)

Figure 3.21. Third FRT strategy results: (a) PCC voltage and current waveforms, (b) active and reactive waveforms

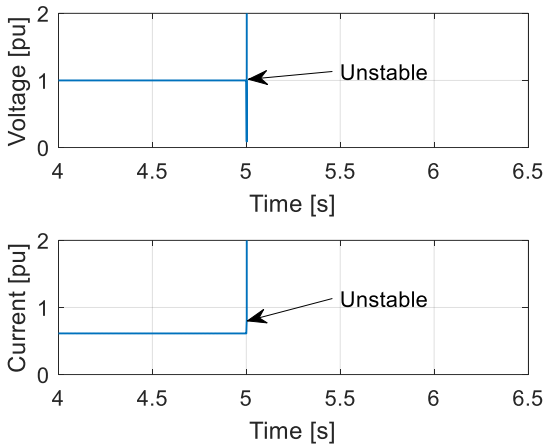


Figure 3.22. Third FRT strategy response to a single-phase fault

3.5.4 Fourth FRT strategy

The fourth strategy aims to limit balanced and unbalanced fault currents, and the schematic of the control structure is shown in Figure 3.23. The control structure uses the measured dq voltage component so that according to Eq. (2.5), Vc_{dq} must be equal to U_{dq} to limit ic_{dq} to zero. Meanwhile, switching between the control loops is ideal; hence, the converter switches instantaneously at the beginning of fault and recovers 20 ms after the fault clearance to decrease the transients. The APL is also disabled during fault because the active power controller fails to synchronise as discussed earlier. The difference between this strategy and the previous strategies is that this strategy is designed to limit the fault current.

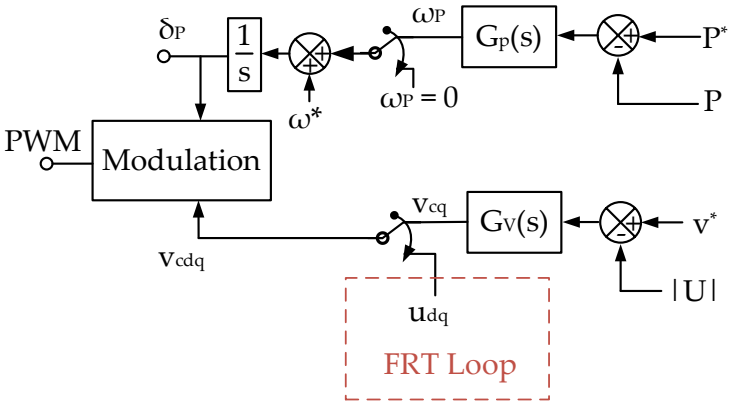
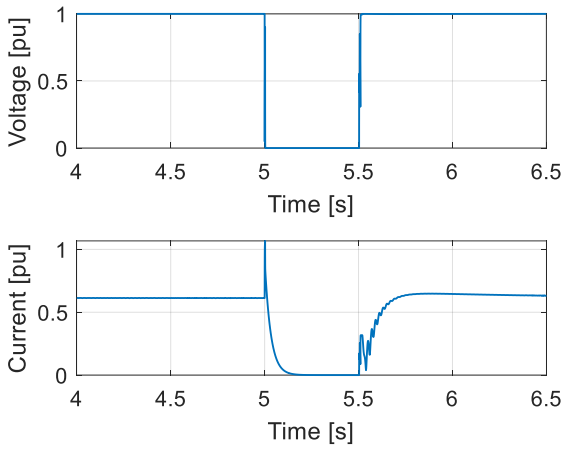
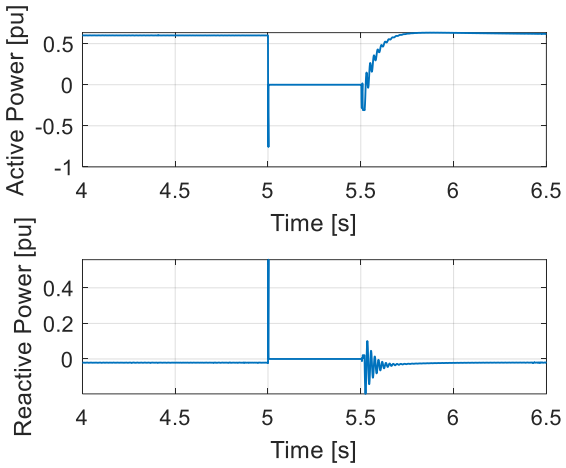


Figure 3.23. Schematic of the fourth FRT strategy

The results for balanced faults are shown in Figure 3.24 in which the current was limited to zero during steady state and some transients were observed at the beginning and end of the fault. The current decrease was slower than that of the previous strategy, which shows the advantage of the inclusion of a current control loop. Moreover, the response to an unbalanced fault is shown in Figure 3.25, revealing the magnitudes of three currents. The current magnitudes show that the currents are not limited below the maximum, which indicates the necessity of adding a current control loop.



(a)



(b)

Figure 3.24. Fourth FRT strategy results for balanced faults: (a) PCC voltage and current waveforms, (b) active and reactive waveforms

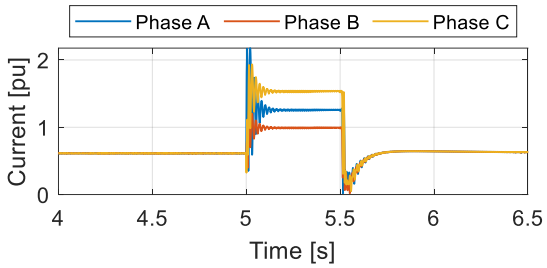


Figure 3.25. Fourth FRT strategy for unbalanced fault currents

3.5.5 Fifth FRT strategy

The fifth strategy is to switch from VSM mode under normal conditions to current control loop under fault conditions. Here, the synchronization loop is disabled similar to those of the previous strategies. The current control is in the dq frame, and the output of the synchronization loop is used for the transformation. The schematic of the control structure is shown in Figure 3.26. The switching between control loops is ideal, and a signal generator is used so that the set signal starts instantaneously as the fault occurs and the reset signal starts 19 ms after the fault clearance (set according to the lowest transient). The simulation parameters are provided in Table 3.3.

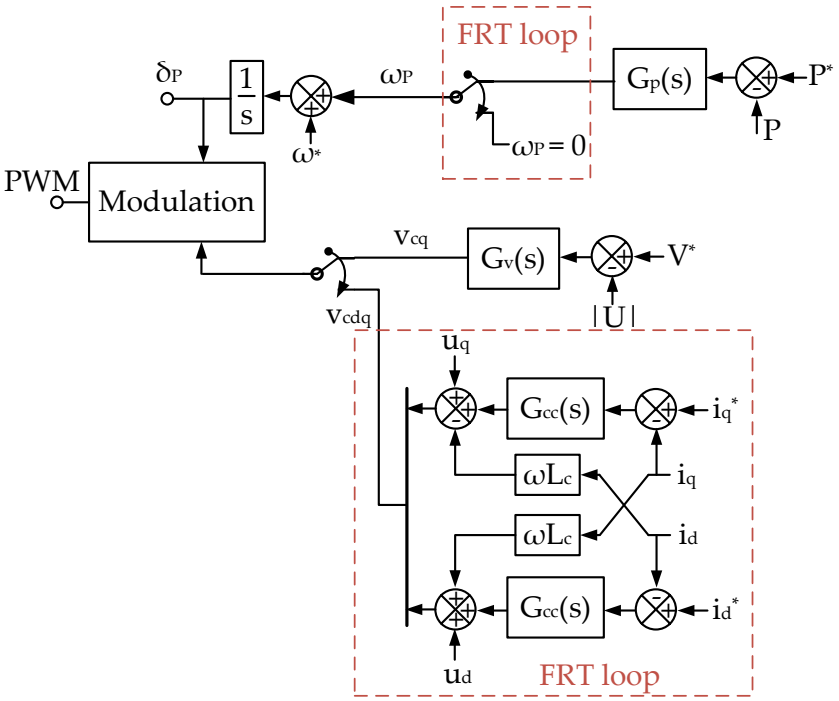
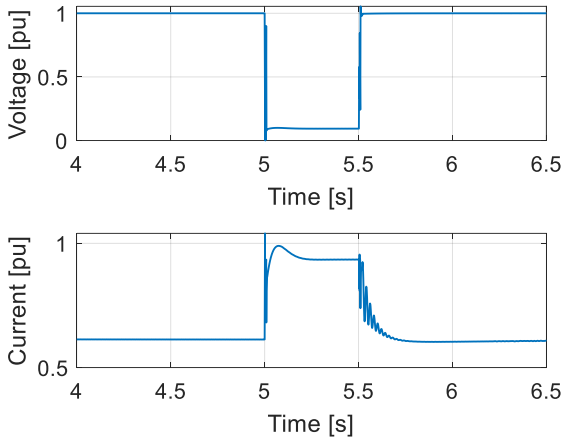


Figure 3.26. Schematic of the fifth FRT strategy

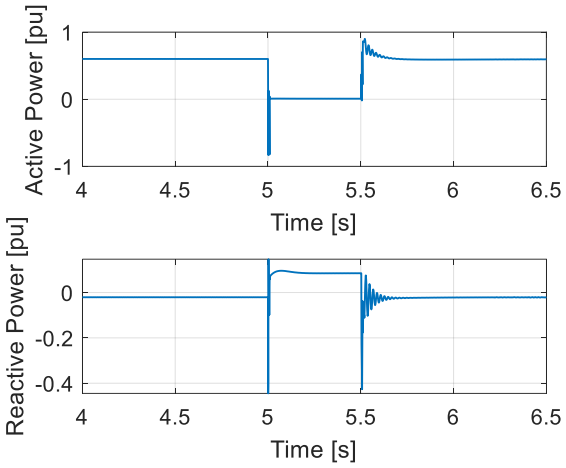
Table 3.3. Parameters of the fifth FRT strategy

Parameter	Value
k_{p-P}	10^{-6}
k_{i-P}	10^{-6}
k_{p-V}	1
k_{i-V}	12
k_{p-CC}	1.25×10^{-3}
k_{i-CC}	3.98×10^{-5}

The results for balanced three-phase faults are shown in Figure 3.27 in which the current magnitude waveform shows that the current is below the maximum limit during fault. However, the currents are uncontrollable for a single-phase fault, as shown in Figure 3.28. In addition, in the case of unbalanced faults, the algorithm used to switch the control loops failed, and an ideal signal was used; hence, the algorithm used for switching loops requires further study. Moreover, a negative sequence is necessary to limit the unbalanced fault current and keep the VSC safe during various faults.



(a)



(b)

Figure 3.27. Fifth FRT strategy results for balanced faults: (a) PCC voltage and current waveforms, (b) active and reactive waveforms

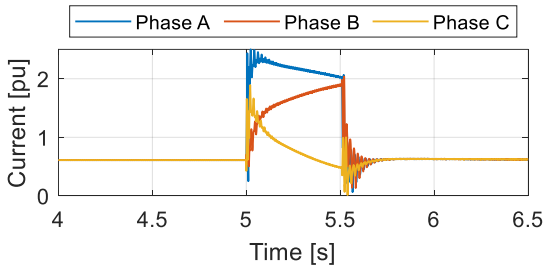


Figure 3.28. Fifth FRT strategy response to a single-phase fault

3.6 Chapter summary

In this chapter, the simplified-order model of the VSM structure was discussed, which was implemented without a current controller or PLL. The tuning relationship between the VSM structure and SM was discussed. Then, the control parameter sensitivity analysis verifies the relation between the PI controller parameters and the inertia and damping factors. Further, the FRT capability of the VSM structure was discussed, and the uncontrollable fault current was highlighted. A technique for limiting the current during normal conditions based on limiting the controller references was also described. The technique can be adapted to prioritise the active or reactive power according to the grid code. However, it limits the fault current only during normal conditions but fails after subjecting the control structure to a fault. Therefore, some FRT strategies were investigated to obtain the key elements required for developing a FRT strategy that maintains the power converter safety and complies with the grid code. The FRT strategies included changing the control structure references, disabling the synchronization loop or integrator of the synchronization loop, adding an inner current control loop with a virtual impedance and saturation block, and disabling the VSM control loop and switching to current control loop. The last strategy was the best choice because it maintains the full VSM capabilities in normal conditions and provides full current limitation capability in fault events. However, a positive and negative current controller is required to control the fault current regardless of the fault type. Moreover, an extensive study is required for the algorithm used in switching between controller loops to ensure that the proposed control structure is reliable and resilient. In the next chapter, a proposed control structure with all the outcomes covered in this chapter is discussed, as well as the algorithm used for switching loops.

Chapter 4

New Fault Detection Algorithm for Dual VSM Structure

4.1 Introduction

The motivation of this chapter is to assess the algorithm responsible for switching between controllers as it has been largely neglected in the literature. Thus, the limitations of the dual VSM structure are discussed in detail in this chapter. First, the behaviour of a conventional FDA inspired by [58, 148, 167], which is used in the dual VSM structure to switch between controllers [58, 152, 167, 168], is discussed. Second, a new FDA is proposed to mitigate the limitations of the conventional FDA in low SCRs and different fault types. The limitation of directly controlling the current control (CC) reference is presented. In addition, an outer loop is presented with a current reference saturation method inspired by [169] to limit the current in both weak and strong grid conditions. The full proposed control structure is referred to here as the improved dual VSM.

Two types of analysis are conducted to evaluate the performance of the proposed controller: fault location sensitivity and control parameter sensitivity analyses. The fault location sensitivity analysis shows the response of the proposed structure to balanced and unbalanced faults in low and high SCRs, and it is used to verify the reliability and performance of the proposed structure. The control parameter sensitivity analysis demonstrates the difference in controller behaviour when each control parameter changes, and it is discussed for low and high SCR grid conditions, which can be used as a tuning reference for such a control structure.

The dual VSM structure configuration is discussed in Section 4.2. In Section 4.3, the FRT capability of a dual VSM structure for high and low SCRs is discussed. In Section 4.4, the improved dual VSM structure and new FDA are discussed. In Section 4.5, the improved dual VSM structure is validated through fault location sensitivity analysis in low and high SCRs. In Section 4.6, the response sensitivity to control parameters is assessed. In Section 4.7, another FRT algorithm is proposed. Finally, the chapter is summarised in Section 4.8.

4.2 Conventional dual VSM configuration

The dual VSM structure [148, 152, 165, 168] consists of a primary VSM controller without CC and backup positive and negative (pn) CC for fault conditions. When a fault is detected, the FDA switches from VSM to CC mode. The main parts of the controller are voltage and current sequence calculation, VSM controller, backup current control, and FDA. Figure 4.1 shows the full converter control.

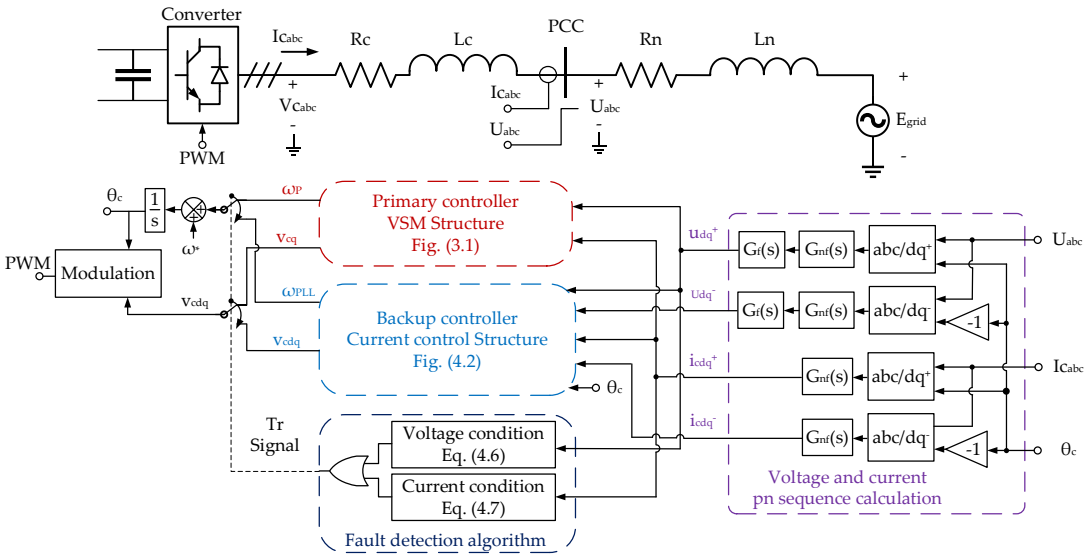


Figure 4.1. Dual VSM structure. pn voltage and current calculation (purple), VSM structure (red), current control structure (blue), and fault detection algorithm (navy)

In this study, the grid is represented by a Thevenin equivalent and is considered a standard model for assessing the performance of the FRT of VSCs [148, 170-173]. The grid equivalent voltage, grid Thevenin resistance, and Thevenin inductance are denoted by E_{grid}, R_n, and L_n, respectively. The converter voltage is Vc_{abc}, and the line

reactor resistance and inductance are R_c and L_c, respectively. The PCC measurements are the voltage U_{abc} and current Ic_{abc}.

4.2.1 Measurement and sequence calculation

The dual VSM structure uses PCC measurements for all the control loops. Park transformation is applied to the PCC measurements to calculate the dq components. The q component is aligned to the active power and the d components lag by 90°.

A notch filter $G_{nf}(s)$ is used to decouple the pn sequence of the voltage and current as follows:

$$G_{nf}(s) = \frac{s^2 + \omega_{nf}^2}{s^2 + \frac{\omega_{nf}}{Q_{nf}} s + \omega_{nf}^2} \tag{4.1}$$

where ω_{nf} is the centre frequency of the filter and Q_{nf} is the filter quality factor.

An extra first-order filter is used to filter the voltage components of the pn sequence to enhance the converter's stability [174], which has a time constant τ_f. The pn sequence components are u_{qd}^{+}, $i_{c_{qd}}^{+}$, u_{qd}^{-}, and $i_{c_{qd}}^{-}$ for the voltage and current.

The primary controller (VSM controller) used in this study has the same schematic as that shown in Fig. 3.1, and the voltage is controlled using a voltage controller.

4.2.2 Conventional pn sequence current controller

A conventional pn sequence CC is used as a backup controller during grid fault conditions. The pn sequence CC is based on [152, 165, 168] and can control the current during balanced and unbalanced faults. The control structure shown in Figure 4.2 takes U_{qd}^{+}, Ic_{qd}^{+}, U_{qd}^{-}, and Ic_{qd}^{-} from the pn voltage and current components calculation. The references Ic_{qd}^{+*}, Ic_{qd}^{-*} of the pn sequence CC are used to set the current limit during faults. The converter voltages of the pn sequences are Vc_{qd}^{+} and Vc_{qd}^{-}. The negative sequence converter voltage component is added to the positive sequence converter component using the conversion block (dq^{-}/dq^{+}) based on Eq. (4.2).

$$\begin{bmatrix} u_q^+ \\ u_d^+ \end{bmatrix} = \begin{bmatrix} \cos(2\theta_c) & -\sin(2\theta_c) \\ \sin(2\theta_c) & \cos(2\theta_c) \end{bmatrix} \begin{bmatrix} u_q^- \\ u_d^- \end{bmatrix} \tag{4.2}$$

The control structure consists of a current control loop PI controller $G_{CC}(s)$ [175], which is explained in section 2.5.1

A PLL is used for synchronization with a PI controller $G_{PLL}(s)$, which is given by:

$$G_{PLL}(s) = k_{p-PLL} + \frac{k_{i-PLL}}{s} \tag{4.3}$$

where $k_{p\text{-}PLL}$ and $k_{i\text{-}PLL}$ are the proportional and integral gains of the PI controller, respectively. The ratio between the control parameters $k_{i\text{-}PLL}/k_{p\text{-}PLL}$ dictates the bandwidth of the controller [176]. Low PLL bandwidths were suggested in [176] to stabilise the standard controller during faults in low and high SCRs.

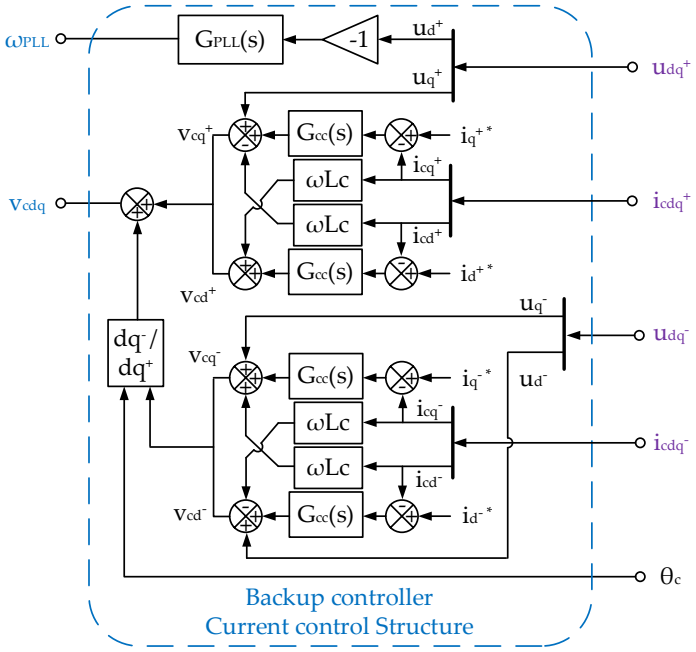


Figure 4.2. Schematic of the pn sequence current controller (backup controller)

4.2.3 Conventional FDA

The conventional FDA uses positive components to calculate the Tr signal, which is the FDA output that determines whether the operating mode is a normal (VSM

structure) or fault condition (alternative structure). The conventional FDA conditions are developed based on [148, 165, 167] and expressed by Eqs. (4.4) and (4.5):

$$\sqrt{\left(u_q^+\right)^2 + \left(u_d^+\right)^2} < |U|_{min} \tag{4.4}$$

$$\sqrt{\left(i_{c_q}^+\right)^2 + \left(i_{c_d}^+\right)^2} > |I|_{C-max} \tag{4.5}$$

where $|U|_{min}$ is the minimum voltage magnitude measured at the PCC (as specified by the local grid code) and $|I|_{c\text{-}max}$ is the maximum current magnitude chosen below or equal to the maximum current capacity of the converter switches.

The primary operating mode is the VSM (when both Eqs. (4.4) and (4.5) are false and Tr signal = 0), whose outputs are ω_P, change in frequency in relation to the power, and voltage loop output Vc_{dq}. The backup operating mode is the CC (when either Eq. (4.4) and (4.5) is true and Tr signal = 1), whose outputs are ω_{PLL}, change in frequency in relation to the change in the d voltage component, Vc_{dq}, and CC voltage output. The converter angle θ_c is derived after adding the change in frequency to the rated frequency as reference ω^*.

4.3 Study of FRT capability in strong and weak grid conditions

To show the limitation of the conventional dual VSM structure, a model was created in MATLAB/Simulink and simulated under an unbalanced fault condition using high (5) and low SCRs (1.4). The parameters used for all the test case scenarios are presented in Table 4.1. The notch filter in Eq. (4.1) was tuned for the simulations to ensure a centre frequency ω_f equal to 200π rad/s for all the filters, and the quality factor Q_f was set to 1 for all the filters, except the positive sequence current, which was set to 10.

Table 4.1. Power network simulation parameters

Parameter name	Parameter value
S_{rated}	5 MVA
Nominal value of U	25 kV
X_n/R_n	10
R_c	0.01 pu
x_c	0.1 pu

The time constant of the first-order filter τ_f was set to 1 ms for the positive sequence voltage component and 10 ms for the negative sequence component. The fault is applied at the mid-point of the network Thevenin equivalent impedance, and the fault is applied at 5s for 500ms.

A test scenario was considered for the two SCR conditions, where a converter operating at 60% loading in steady-state conditions was subjected to a single-phase-to-ground fault. During the fault, the converter injected 92% of its peak current. Based on the simulation parameters in Table 4.1, this peak current is 163.3 A. The converter rating and references were designed to account for this peak and a 20% safety threshold [177], arriving at a peak current of 196 A (approximately 200 A). The safety threshold accounts for overcurrent transients that are caused when switching between the controllers and are especially severe in weak networks. Inspired by the study in [178] and considering the converter rating, the reactive positive current component i_d^{+*} was set to 150 A, and all the other current references were set to zero based on the local grid code.

Figure 4.3(c) shows the conventional FDA output during unbalanced faults in both low and high SCRs. The fault began at $t = 5\ s$ and lasted for 500 ms. Figure 4.3(a) and Figure 4.3(b) show the positive sequence voltage and current, respectively, and Figure 4.3(c) shows the FDA output.

The standard FDA correctly detected the fault for high SCR but disengaged after some time for low SCR. The suboptimal early FDA reset in the low SCR is driven by the higher grid Thevenin impedance, which requires the CC to apply a higher voltage to

achieve the same current. The higher converter voltage increases the PCC voltage. For a single-phase-to-ground fault, the two remaining healthy phase voltages were increased by the higher converter voltage, and the total voltage magnitude calculated by the FDA was within the specified nominal range shown in Figure 4.3(a); thus, the voltage appeared to be healthy. Meanwhile, the fault detection current condition was not reliable because the current decreased over time as a result of the current controller action. The combination of the voltage and current conditions makes the conventional FDA less effective in low SCRs. Furthermore, the injection of maximum current by the high healthy phase voltage drives the power transfer above the maximum complex power limit of the converter.

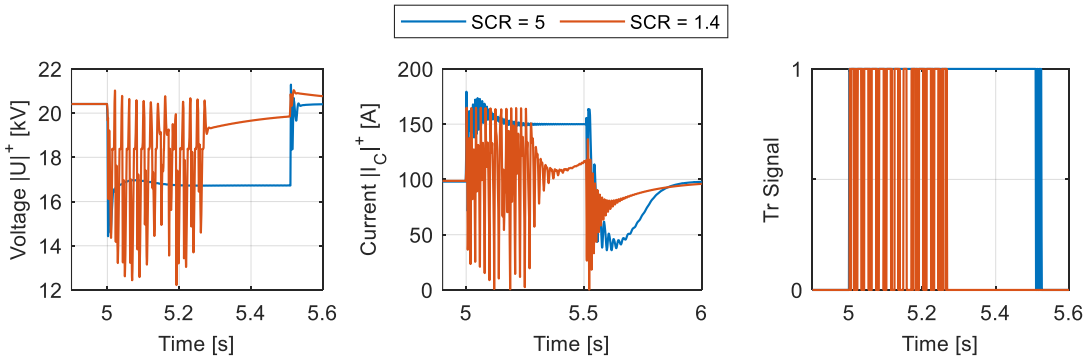


Figure 4.3. Comparison between low SCR (1.4) and high SCR (5): (a) positive sequence voltage magnitude $|U|^+$ at the PCC, (b) positive sequence current magnitude $|I|_c^+$, and (c) FDA output signal (Tr signal)

4.4 New FDA with improved dual VSM structure

In this section, a new FDA and the enhancements added to support faults in weak grids are discussed. Comparisons between the conventional and improved dual VSMs are also presented.

4.4.1 New FDA and controller enhancements

Figure 4.4 shows the full schematic of the proposed structure. An outer loop was added to the CC loop to deal with the weak network scenario, and a bump-less transfer was also added.

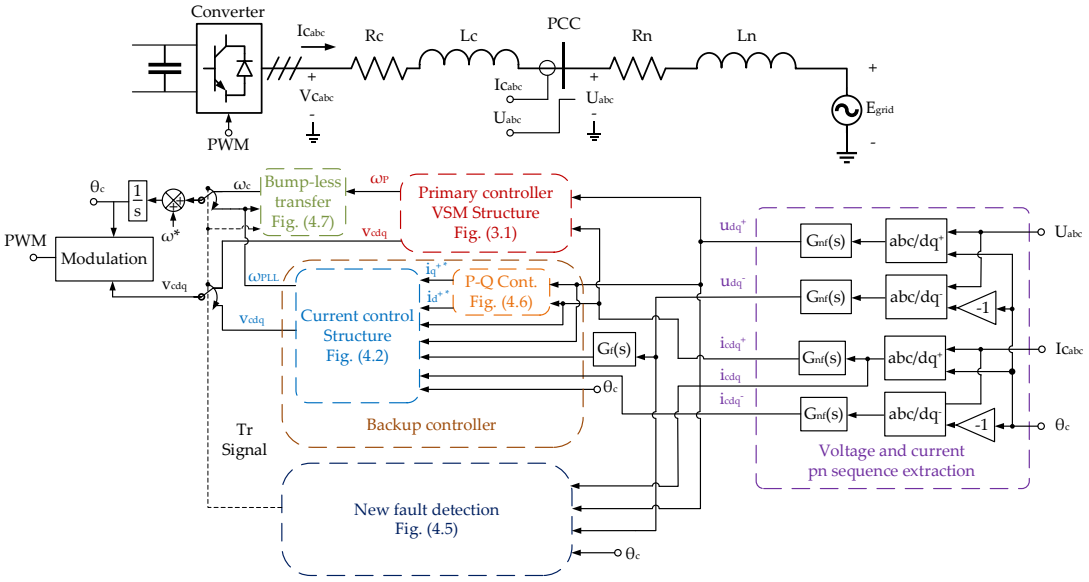


Figure 4.4. Full schematic of the improved dual VSM structure: outer loop (orange), bump-less transfer (green), and new FDA (dark blue)

The new FDA was designed to operate effectively under different fault types and SCRs. It achieves better operation during unbalanced faults by considering the pn sequence voltage and current components unlike the conventional FDA. The negative sequence is a key component for the new FDA, especially in weak networks. The voltage condition is given by:

$$G_{fv}(s)\left(|U|^{+}-|U|^{-/+}\right)<|U|_{min} \tag{4.6}$$

where $0<|U|^{+}<|U|_{rated}$, $|U|^{-/+}$ is the negative sequence voltage aligned to the positive sequence frame, and $G_{fv}(s)$ is a first-order filter applied to the voltage signal before the condition, which is given by:

$$G_{fv}(s)=\frac{1}{\tau_{fv}s+1} \tag{4.7}$$

where τ_{fv} is the time constant of the first-order filter $G_{fv}(s)$.

The new voltage condition guarantees the detection of unbalanced faults in weak grid conditions, because the measured negative sequence voltage is subtracted from

the measured positive sequence voltage, so that the voltage created by the healthy phases is decreased by the negative sequence voltage created due to the unbalanced fault. The current condition is the same as that given by Eq. (4.5) but the condition input is the current measurement after Park transformation. Thus, the negative sequence is also considered.

During fault recovery, the new FDA clears the Tr signal when both conditions are false. However, the voltage condition may experience a false voltage drop, which is caused by the transients created during transition to the primary controller. As a result, the voltage condition is disabled for a short period using a Set/Reset flip-flop, an edge trigger, and an off-delay time. This method prevents false re-engaging for a short time during fault recovery while protecting the converter as current is continuously monitored according to Eq. (4.5). Figure 4.5 shows the schematic of the new FDA.

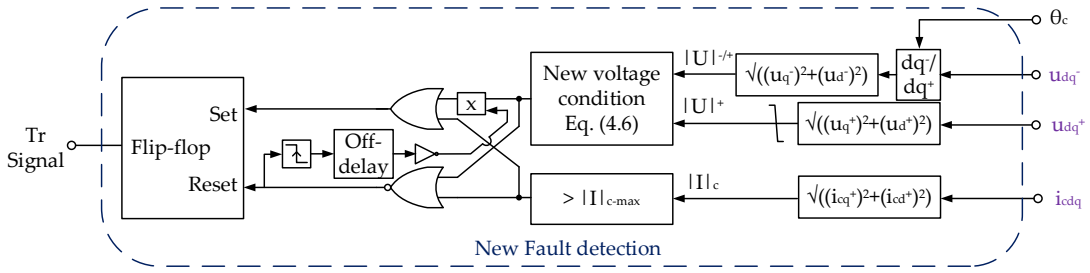


Figure 4.5. Schematic of the new FDA

An outer loop is added to limit high voltages in the healthy phases during unbalanced faults in weak grids, as observed in the simulations described in Section 4.3. The active power loop outer controller $G_{OP}(s)$ is expressed by:

$$G_{OP}(s) = k_{p-OP} + \frac{k_{i-OP}}{s} \tag{4.8}$$

where $k_{p\text{-}OP}$ and $k_{i\text{-}OP}$ are the proportional and integral gains of the PI controller, respectively.

The reactive power loop outer controller $G_{OQ}(s)$ is expressed by:

$$G_{OQ}(s) = k_{p-OQ} + \frac{k_{i-OQ}}{s} \tag{4.9}$$

where $k_{p\text{-}OQ}$ and $k_{i\text{-}OQ}$ are the proportional and integral gains of the PI controller, respectively.

The outer P-Q cont. loop has a good performance in low SCR conditions; however, a current reference limitation is required in high SCR conditions. The current reference limitation is implemented using a reference recalculation method. This method is applied for the reactive power loop, and it is given by:

$$Q_{recalc} = k_q \times (i_d^{+*} - |\mathrm{I}|_{c-max}), \text{ where } 0 < Q_{recalc} < \infty \tag{4.10}$$

where $|\mathrm{I}|_{c\text{-}max}$ is the specified maximum converter current, k_q is a factor used to convert the current reference to power, and Q_{recalc} is subtracted from the reactive power reference.

The P-Q cont. loop current outputs are saturated to avoid negative current reference. The active power outer loop is set to zero to prioritise reactive power injection. The active power controller can be used to provide flexible active power control for future developments. Figure 4.6 shows the schematic of the outer P-Q cont. loop.

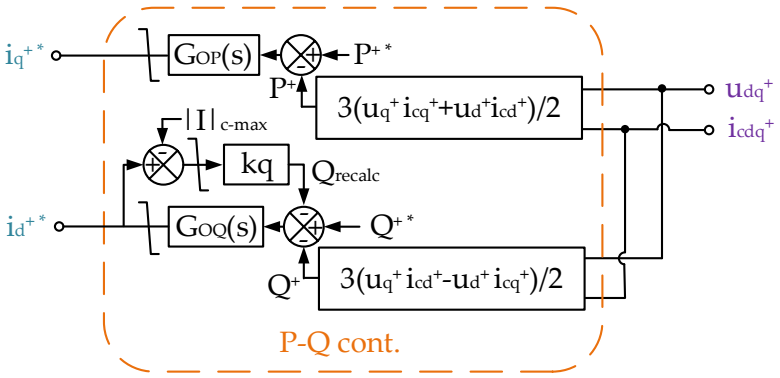


Figure 4.6. Schematic of the P-Q cont. loop

The bump-less transfer shown in Figure 4.7 is added to smoothen the transition between the controllers during recovery. The method uses the PLL output for one cycle

to support the APL resynchronization. The method multiplies the PLL output by a gain k_p, which is subtracted from the APL output.

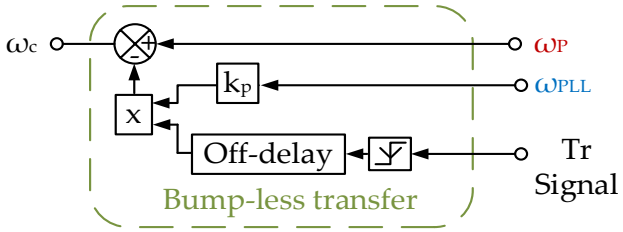


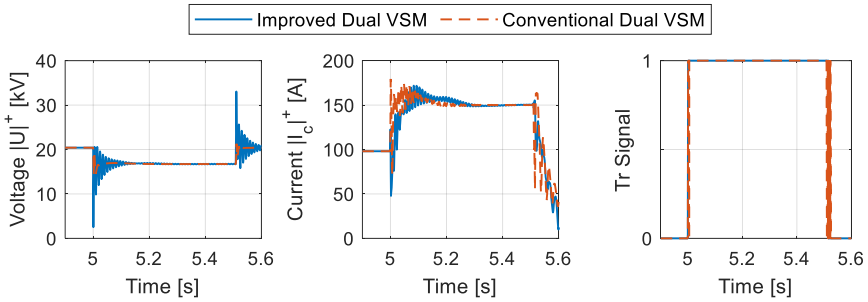
Figure 4.7. Bump-less transfer activated during fault recovery

This method is activated for one cycle after a reset signal is received from the new FDA, which is implemented using an edge detector and off-delay timer. The APL reference is gradually increased to the rated value after fault clearance, which introduces further damping in the transitional transients.

4.4.2 Comparison between the improved and conventional dual VSM structures

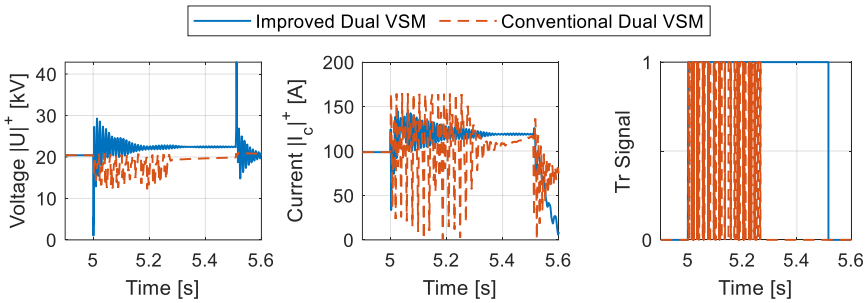
In this section, the conventional and improved dual VSM structures are compared. The same test conditions applied in Section 4.3 are reapplied on the improved dual VSM structure to produce a fair comparison for both control structures.

Figure 4.8(a)–(c) show the comparison between the two control structures with a high SCR based on positive sequence voltage, positive sequence current, and Tr signal, respectively. The improved dual VSM structure had lower current transients compared to the conventional structure. Moreover, Figure 4.9(a)–(c) show a stable operation for the improved dual VSM structure, whereas the conventional dual VSM structure could not detect fault in low SCR, as discussed in Section 4.3.



(a) (b) (c)

Figure 4.8. Comparison between the improved and conventional dual VSMs in the high SCR case



(a) (b) (c)

Figure 4.9. Comparison between the improved and conventional dual VSMs in the low SCR case

4.5 Verification of the improved dual VSM structure under different test conditions

The improved dual VSM structure was tested for balanced and unbalanced faults in low and high SCR grid conditions using the same parameters presented in Table 4.1. The test cases involved four different fault locations, as shown in Figure 4.10, where Z_C is the equivalent impedance of the filter and transformer and Zn is the grid Thevenin impedance. The fault locations were moved further away from the PCC and ranged from FL1 to FL4. The faults were applied at 5 s and cleared at 5.5 s, as in Section 3.

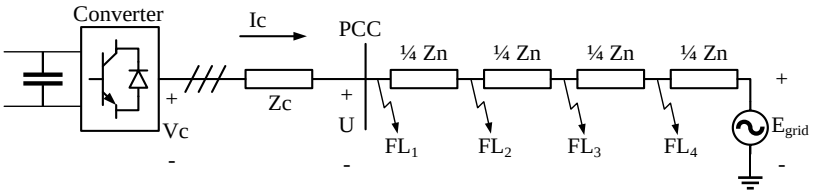


Figure 4.10. Fault locations used in the first analysis

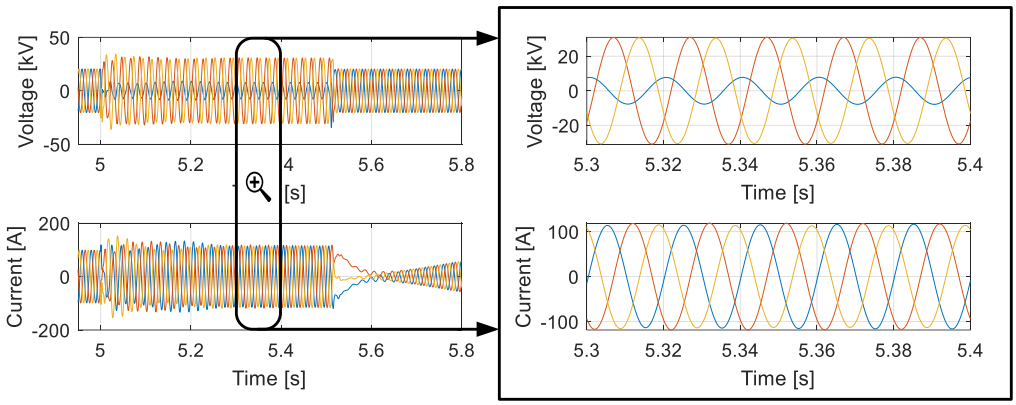
4.5.1 Fault distance sensitivity analysis in low SCR

The improved dual VSM structure with new FDA was tested in low SCR (1.4) to investigate its response to faults at specific locations.

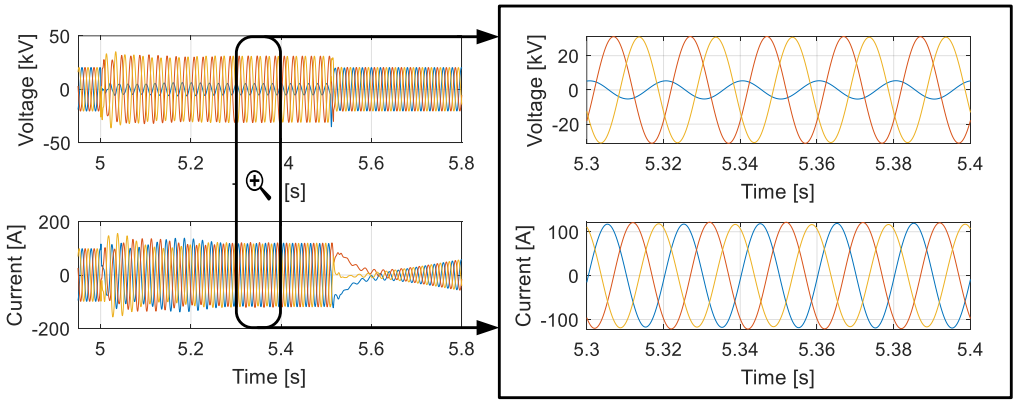
Figure 4.11 shows the controller voltage and current waveform responses to a single-phase-to-ground fault. The new FDA showed good accuracy in detecting single-phase-to-ground fault and its clearance at all locations. Figure 4.11(a)–(b) show the controller responses to single-phase-to-ground faults at FL_4 and FL_3, revealing that the controller responded to the fault applied at approximately 5 s, and the new FDA detected the fault clearance at 5.5 s and switched back to primary controller at 5.52 s. Figure 4.11(c)–(d) show the controller response to single-phase-to-ground faults at FL_2 and FL_1, where the fault was detected at almost 5 s and the controller began to inject maximum reactive current (was tuned to be 150 A peak). The controller was switched back to VSM before 5.52 s. The zoomed area on the right of each figure shows that the proposed structure can inject balanced currents under all the test cases.

Figure 4.12 shows the controller responses to three-phase-to-ground faults at the same fault locations discussed before. The new FDA also showed good accuracy in detecting all the three-phase-to-ground faults and clearances. Figure 4.12(a)–(d) show the voltage and current waveforms for faults applied at FL_4–FL_1. The new FDA detected the fault at almost 5 s and the clearance before 5.52 s. The current during the fault was kept at 150 A peak, and a short-time high current transient was observed during the first instance of the fault, which remained within the converter capability limit of 200 A. The tuning of the PQ outer loop and the reactive power recalculation helped in damping the rise of the fault current at the beginning of the fault, which led to smooth current transients in these test cases shown. Also, a slow recovery can be

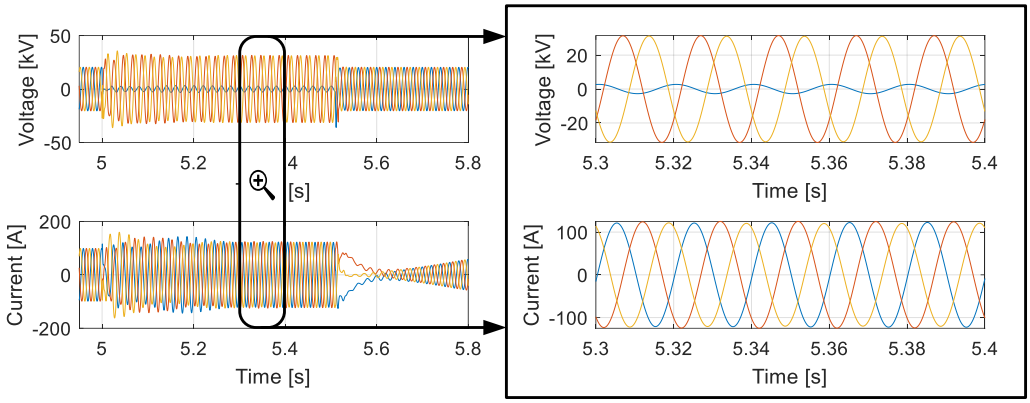
observed in all the figures because of the gradual increase of the active power reference rather than the instant injection of the full active power reference. Moreover, the slow dynamics of the VSM participated in slowing the injection of the full current after the recovery, and in the recovery the current decreases to almost zero at some cases and rise back again which is due to injecting full reactive current during fault, and in the recovery the reactive power is highly reduced, and the active power is mostly injected. Most of the test cases show the slow recovery behaviour, however the slow recovery was a solution to the high current transients in the recovery.



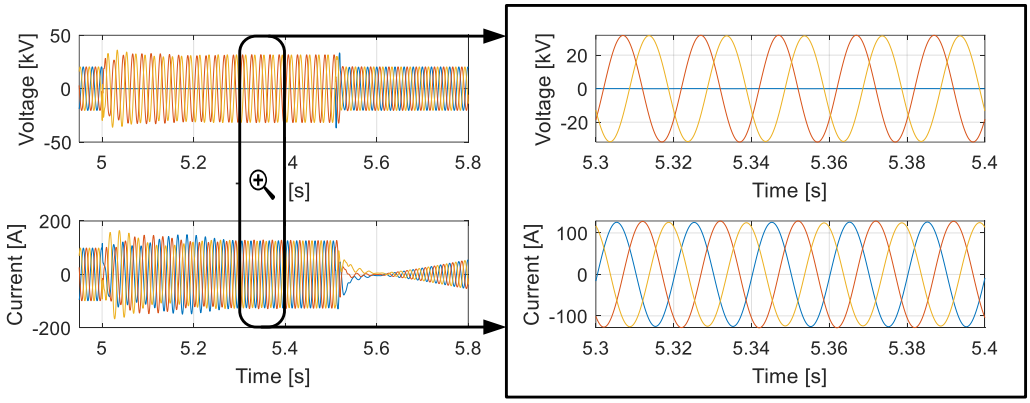
(a)



(b)

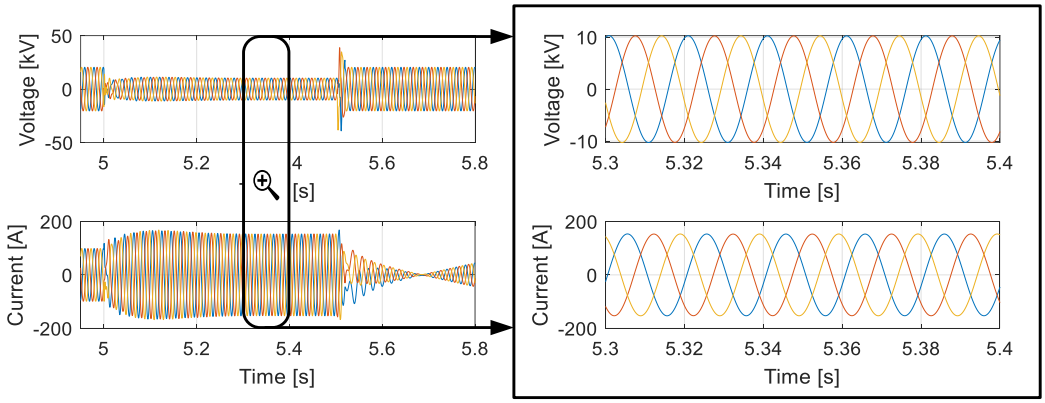


(c)

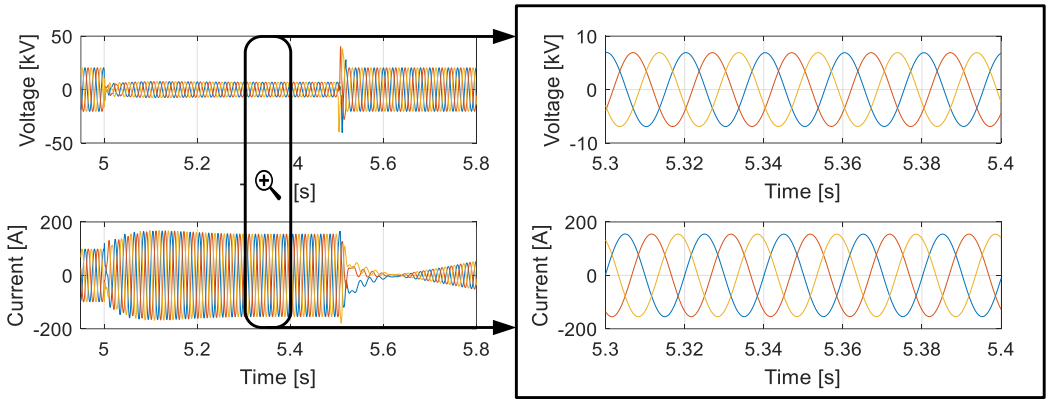


(d)

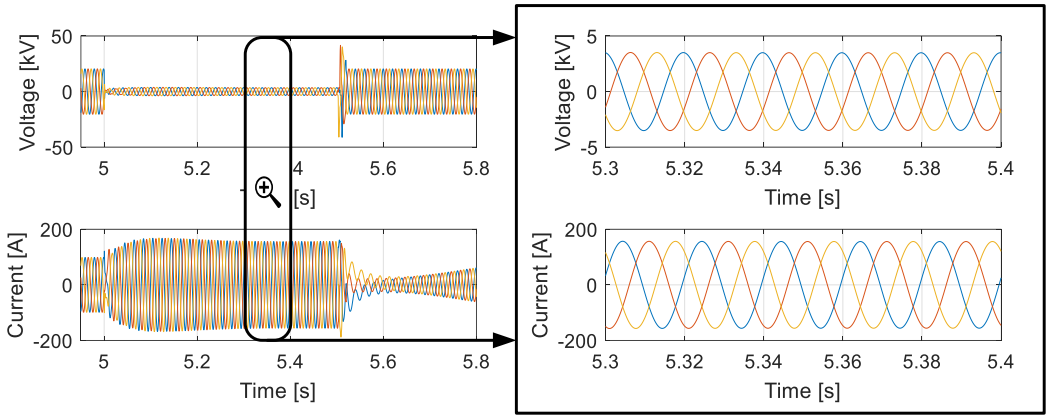
Figure 4.11. Single-phase-to-ground faults at different locations in low SCR: (a) FL_4, (b) FL_3, (c) FL_2, and (d) FL_1



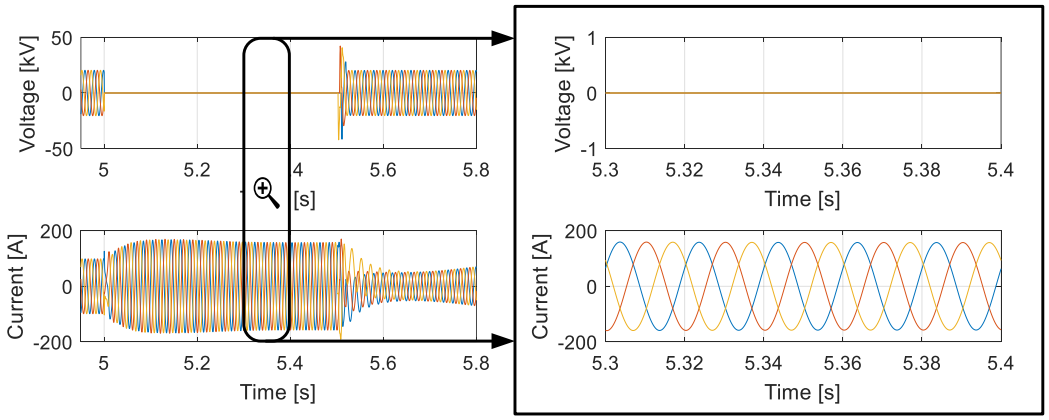
(a)



(b)



(c)



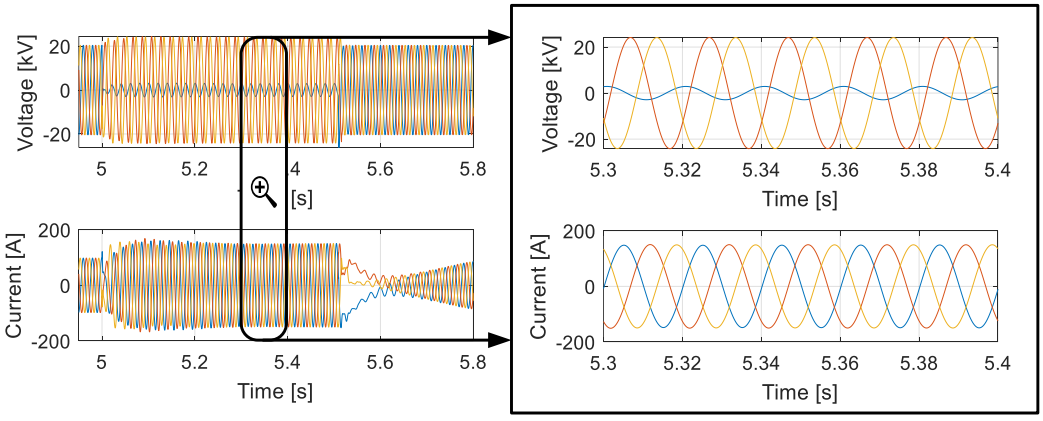
(d)

Figure 4.12. Three-phase-to-ground fault at different locations in low SCR: (a) FL_4, (b) FL_3, (c) FL_2, and (d) FL_1

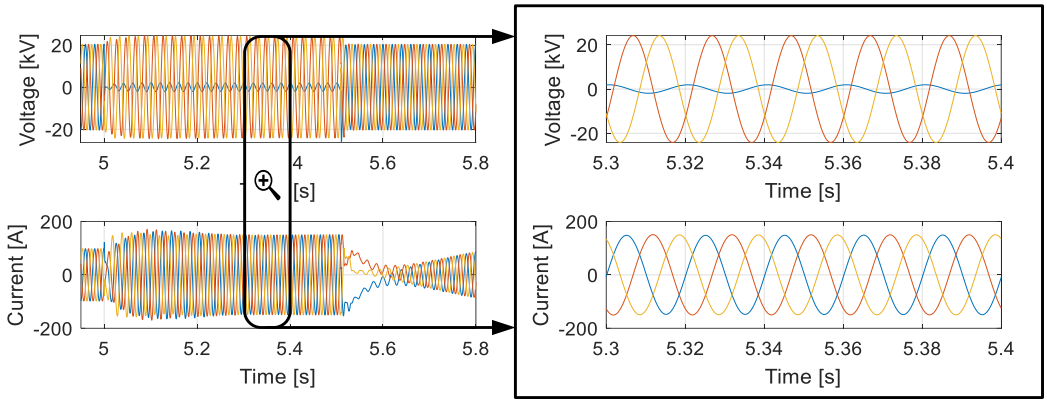
4.5.2 Fault distance sensitivity analysis in high SCR

The same test case scenarios were adopted for high SCR to investigate the controller behaviour. Figure 4.13 shows the controller responses to single-phase-to-ground faults, where Figure 4.13(a) depicts the voltage and current waveforms for an unbalanced fault applied at FL_4. The waveforms showed stable operation and the current was quickly limited. Figure 4.13(b)–(d) show the voltage and current waveform responses to unbalanced faults applied at FL_3, FL_2, and FL_1. Considering the four locations, the new FDA successfully identified the fault at almost the same time as it was applied and reset the fault signal to switch back to the VSM structure at approximately 5.52 s.

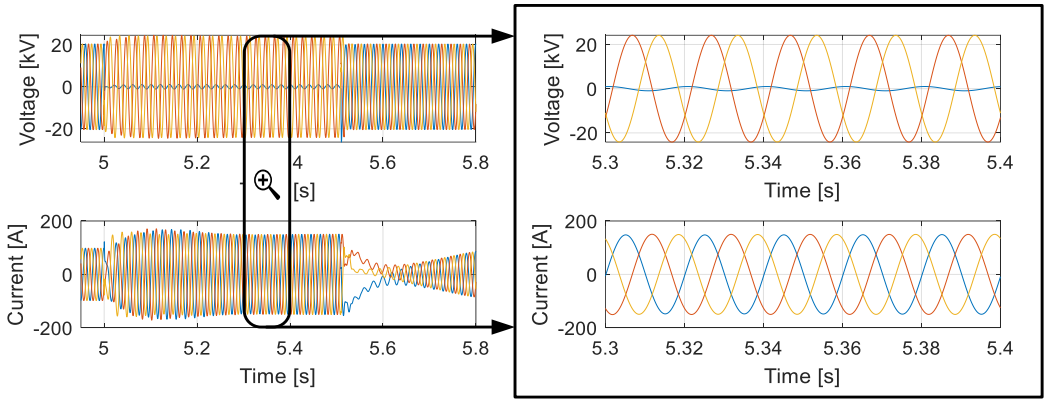
Figure 4.14 shows the controller responses to three-phase-to-ground faults at the same fault locations specified before. Figure 4.14(a)–(d) show the voltage and current waveforms when balanced faults were applied at FL_4, FL_3, FL_2, and FL_1. The four responses show that the controller detected the fault at almost 5 s with high peak current transient observed in the waveforms at the beginning of each fault, and the current was maintained at 150 A peak in the steady-state of the fault. Finally, the new FDA successfully reset the fault signal at approximately 5.52 s, and the structure switched from CC to VSM. The zoomed areas show the balanced current injection in all the test cases.



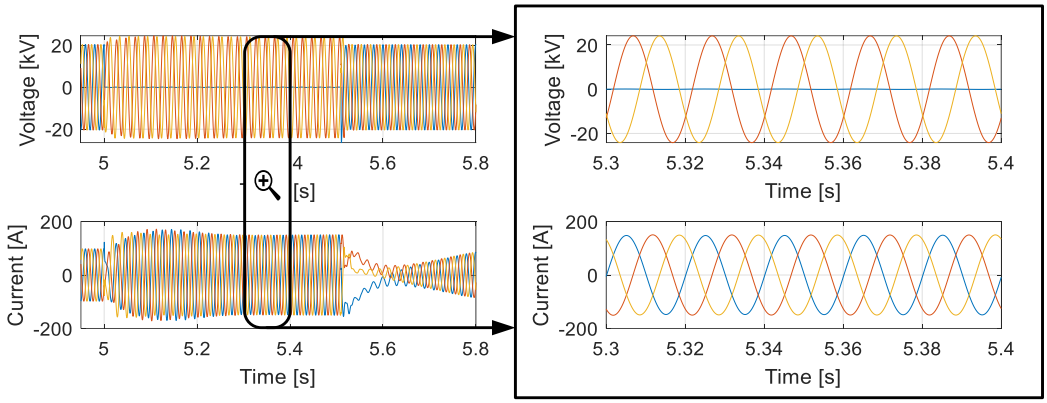
(a)



(b)

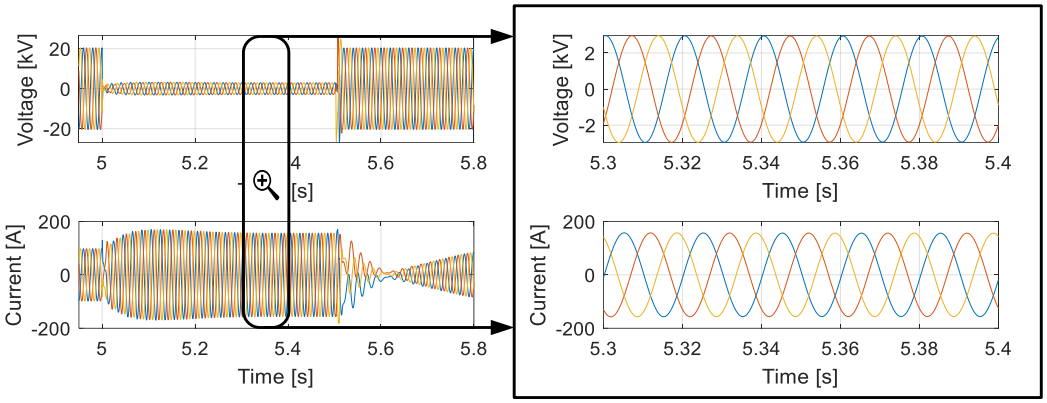


(c)

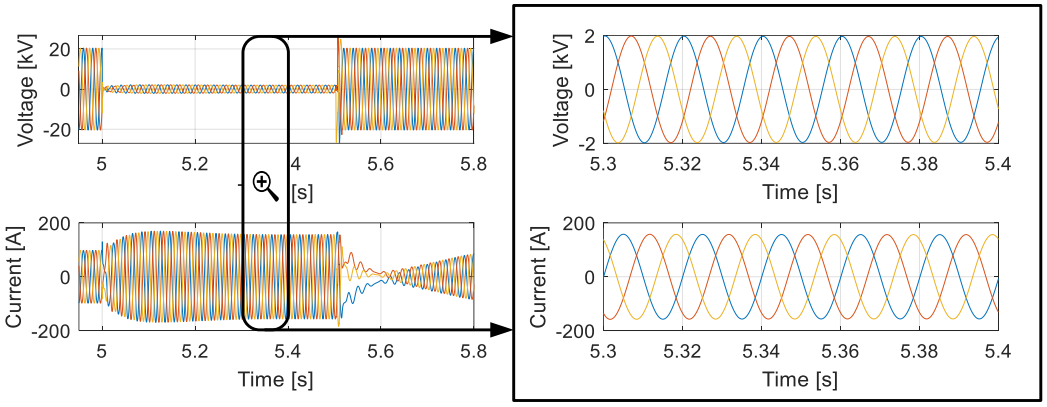


(d)

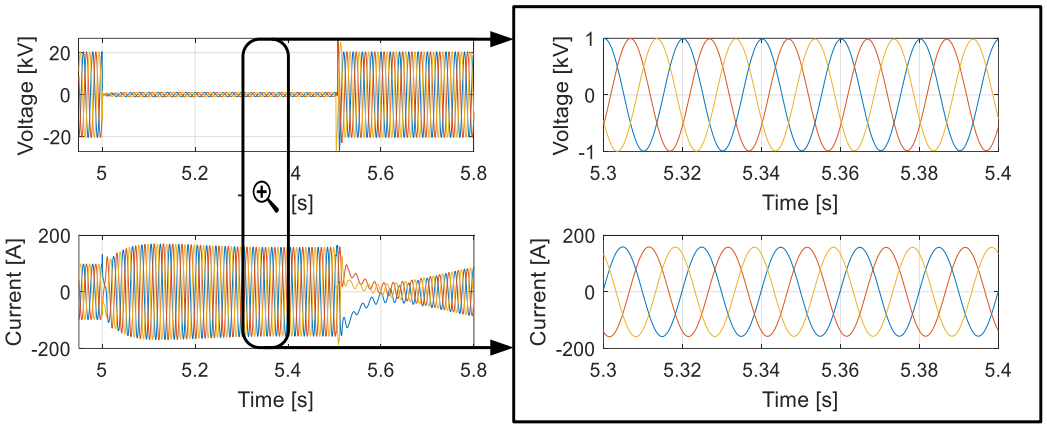
Figure 4.13. Single-phase-to-ground faults at different locations with high SCR: (a) FL_4, (b) FL_3, (c) FL_2, and (d) FL_1


Voltage [kV]
Current [A]
Time [s]
Voltage [kV]
Current [A]
Time [s]

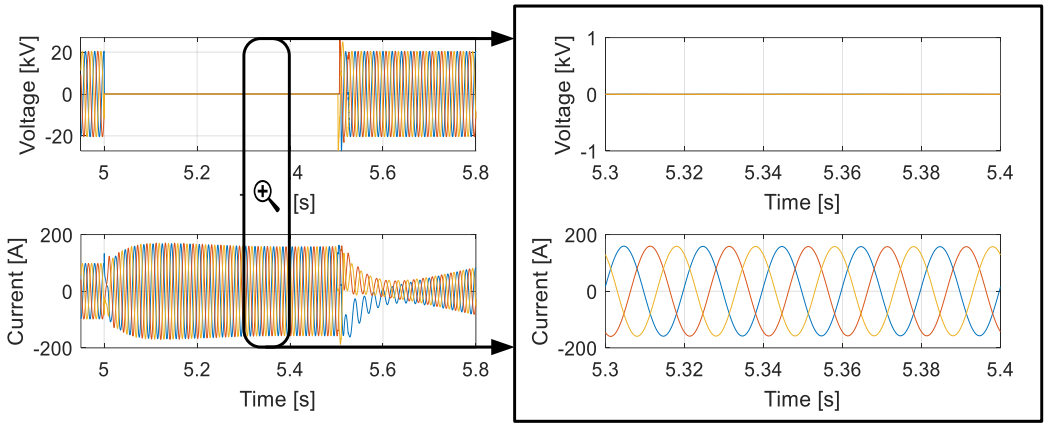
(a)


Voltage [kV]
Current [A]
Time [s]
Voltage [kV]
Current [A]
Time [s]

(b)


Voltage [kV]
Current [A]
Time [s]
Voltage [kV]
Current [A]
Time [s]

(c)



(d)

Figure 4.14. Three-phase-to-ground faults at different locations in high SCR: (a) FL_4, (b) FL_3, (c) FL_2, and (d) FL_1

4.5.3 Consecutive faults analysis

In this analysis, the response of the improved dual VSM structure in two consecutive fault scenarios was investigated. The simulation aims to show that although the voltage condition is disabled during recovery, the improved FDA can operate safely if two consecutive faults occur.

The analysis involves subjecting the VSC to a single-phase-to-ground fault from 5 to 5.5 s and then to a three-phase-to-ground fault from 5.55 to 6.05 s. These two faults were applied in strong and weak grid conditions, and the PCC voltage and current were observed.

Figure 4.15 shows the voltage and current waveforms after applying the two consecutive faults in high SCR. The current waveform showed that the control structure was switched from the primary to the backup controller, which limited the current within the safe operational range. The controller switched back to the primary controller at 6.07 s.

Figure 4.16 shows the voltage and current waveforms in low SCR. The current waveform shows that the current was successfully limited, and the controller switched back to the VSM 20 ms after both faults were cleared.

The current peak during the unbalanced fault was lower than that during the balanced fault. This is caused by the outer loop action because the voltage created by the healthy phases during unbalanced fault is increased by decreasing the SCR.

This analysis shows that the improved dual VSM structure can survive two or more consecutive faults, and the blocked voltage condition during recovery does not impact the reliability of the new FDA. Additionally, the current peak during the single-phase-to-ground fault was mitigated, which is used to dampen the healthy phase voltage.

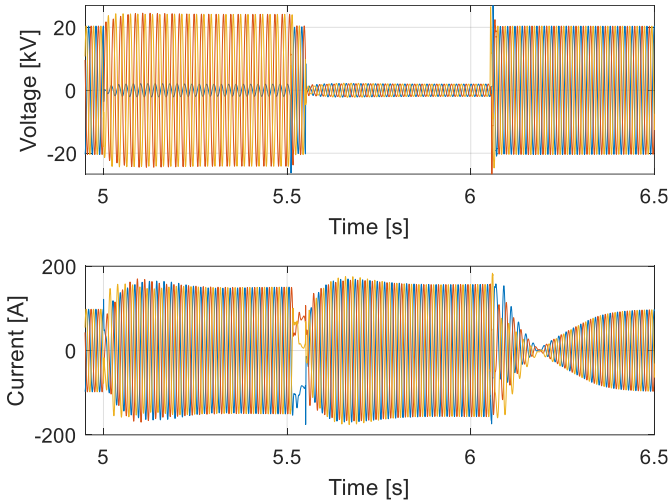


Figure 4.15. Unbalanced fault followed by balanced fault in high SCR

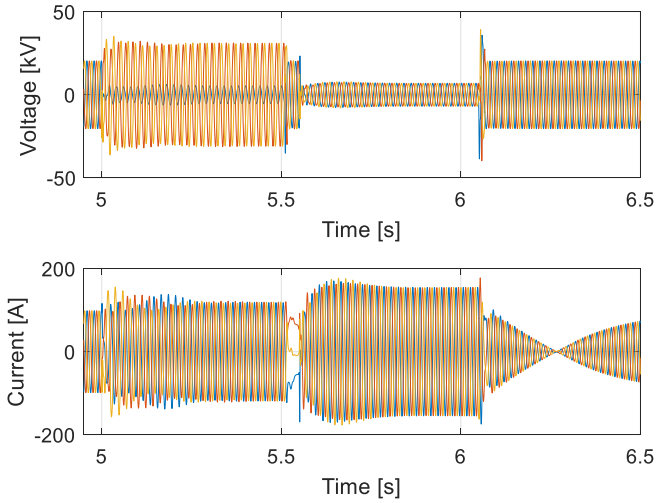


Figure 4.16. Unbalanced fault followed by balanced fault in low SCR

4.6 Control parameter sensitivity analysis for the improved dual VSM structure

In this section, parameter sensitivity analysis is used to determine the best tuning parameters of the improved dual VSM structure. The parameters considered are the voltage first-order filter time constant τ_{fv} of the new FDA, current first-order filter time constant τ_{fi} of the new FDA, CC loop time constant τ_{cc}, bandwidth of the PLL $k_{i\text{-}PLL}/k_{p\text{-}PLL}$, and tuning of the active power loop $k_{i\text{-}P}/k_{p\text{-}P}$. Each parameter configuration was subjected to a single-phase-to-ground fault, and its effect on the control response was observed at the beginning of the fault, during the fault, and during recovery. The controller response was assessed using the current magnitude and the new FDA output for high and low SCRs.

4.6.1 High SCR case

Parameter sensitivity analysis was used to investigate changes in the control response for high SCR. The first assessed parameter is the time constant of the voltage first-order filter in the new FDA.

Figure 4.17(a) shows that an increase in the filter time constant causes an increase in the transient peak in the first instance after the fault. The transient peak is driven by the delay introduced by the first-order filter time constant to the new FDA action. However, the filters are necessary for smoothing the new FDA inputs. The steady-state fault current (Figure 4.17(b)) and recovery period after fault clearance (Figure 4.17(c)) are not significantly affected by the time constant of the voltage filter. Figure 4.17(d) shows that the change in the filter time constant has no effect on the new FDA output.

The second parameter is τ_{cc}. Figure 4.17(e)–(g) show that as the controller time constant increases, the oscillations in the fault current escalate and degrade the controller performance. Figure 4.17(h) shows that an increase in τ_{cc} has no effect on the new FDA output.

The third parameter is $k_{i\text{-}PLL}/k_{p\text{-}PLL}$, which is the ratio of the PLL proportional and integral control parameters. Figure 4.17(i) shows that an increase in the proportional

gain leads to increase in oscillations at the beginning of the fault. Additionally, a decrease in the proportional gain introduces delays to the transient current during fault recovery, as shown in Figure 4.17(k). Figure 4.17(l) shows that the new FDA output clearance is delayed by the highest tuning parameter ratio.

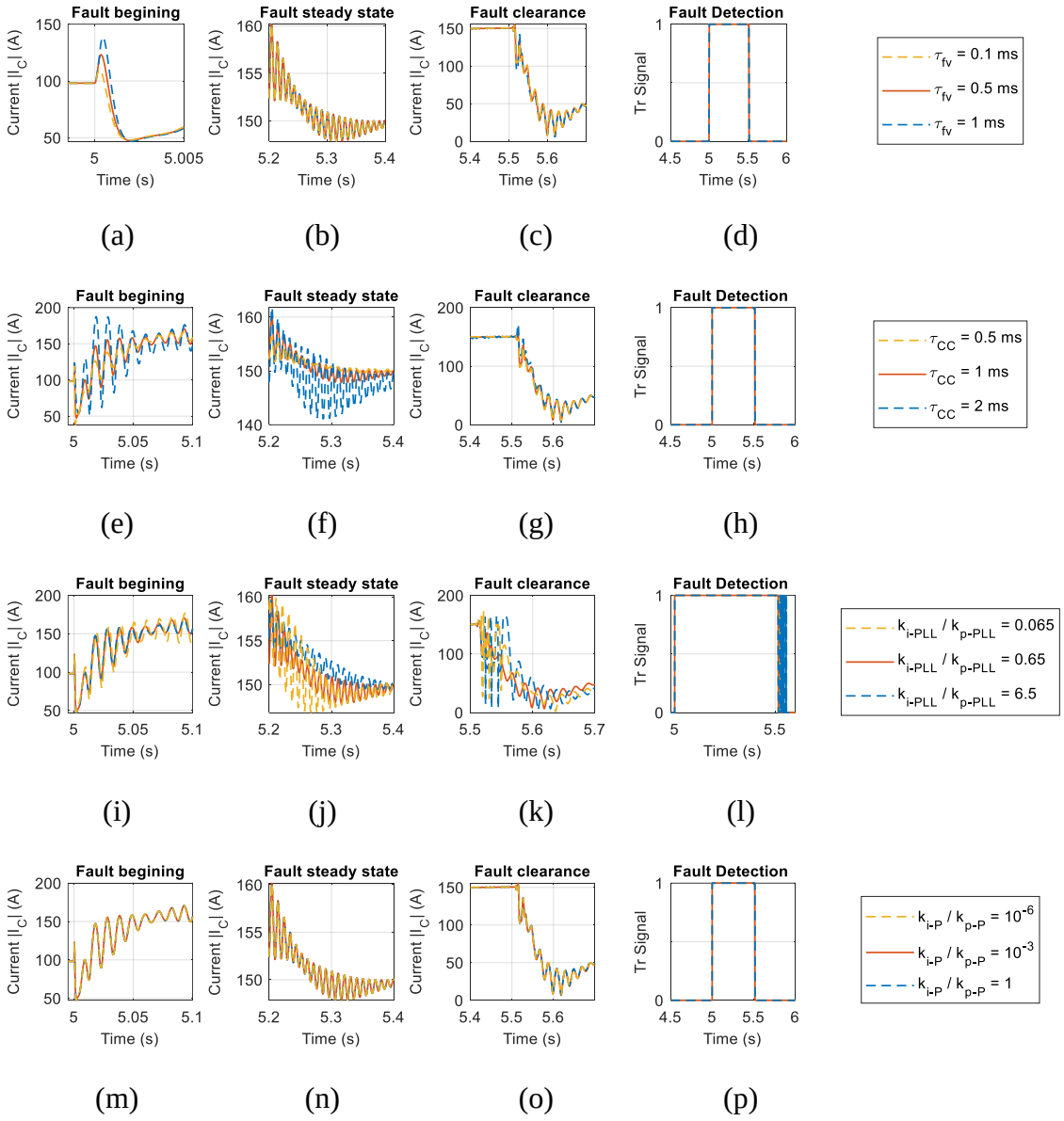


Figure 4.17. Parameter sensitivity analysis in the high SCR case: column (a,e,i,m) shows the currents at the beginning of the fault, column (b,f,j,n) shows the currents during the fault steady-state, column (c,g,k,o) shows the currents during fault recovery, and column (d,h,l,p) shows the new FDA outputs. Row (a,b,c,d) shows the response for varying time constant $\boldsymbol{\tau}_{fv}$ of the new FDA voltage filter, row (e,f,g,h) shows the response for varying time constant $\boldsymbol{\tau}_{cc}$ of the current controller, row (m,n,o,p) shows the response for varying PLL bandwidth $k_{i\text{-}PLL}/k_{p\text{-}PLL}$, and row (q,r,s,t) shows the response for varying APL bandwidth $k_{i\text{-}P}/k_{p\text{-}P}$

The fourth parameter is $k_{i\text{-}P}/k_{p\text{-}P}$, which is the ratio of the proportional and integral gains of the APL. Figure 4.17(m)–(p) show that the tuning of the APL does not affect the response of the new FDA responses even for the large change in the controller gains ratio.

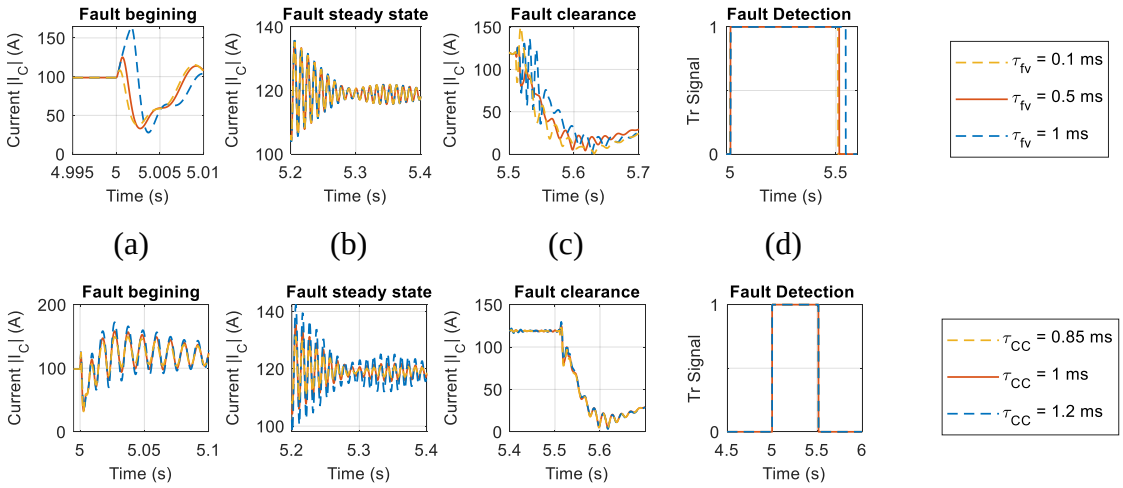
4.6.2 Low SCR case

The same parameters were considered for the low SCR case, which is more challenging owing to voltage instability in weak grid conditions. The first parameter is τ_{fv} in the new FDA. Figure 4.18(a) shows that a low filter time constant has the lowest transient peak. Figure 4.18(c) shows that the lowest time constant has the highest peak during recovery. Figure 4.18(d) shows the new FDA output in which the lowest time constant has the fastest recovery.

The second parameter is τ_{cc}. An increase in τ_{cc} caused the oscillations in the fault current to increase at the fault beginning, steady-state, and clearance (Figure 4.18(e)–(g)). Figure 4.18(h) shows that no change occurred on the new FDA output.

The third parameter is $k_{i\text{-}PLL}/k_{p\text{-}PLL}$. The medium proportional gain value of the PLL had the best response at the beginning and recovery periods of the fault, as shown in Figure 4.18(i)–(l).

The fourth parameter is $k_{i\text{-}P}/k_{p\text{-}P}$. The sensitivity of the control response to the tuning of the APL was the same as in the high SCR case, and no change was observed with changes in the tuning of the APL, as shown in Figure 4.18(m)–(p).



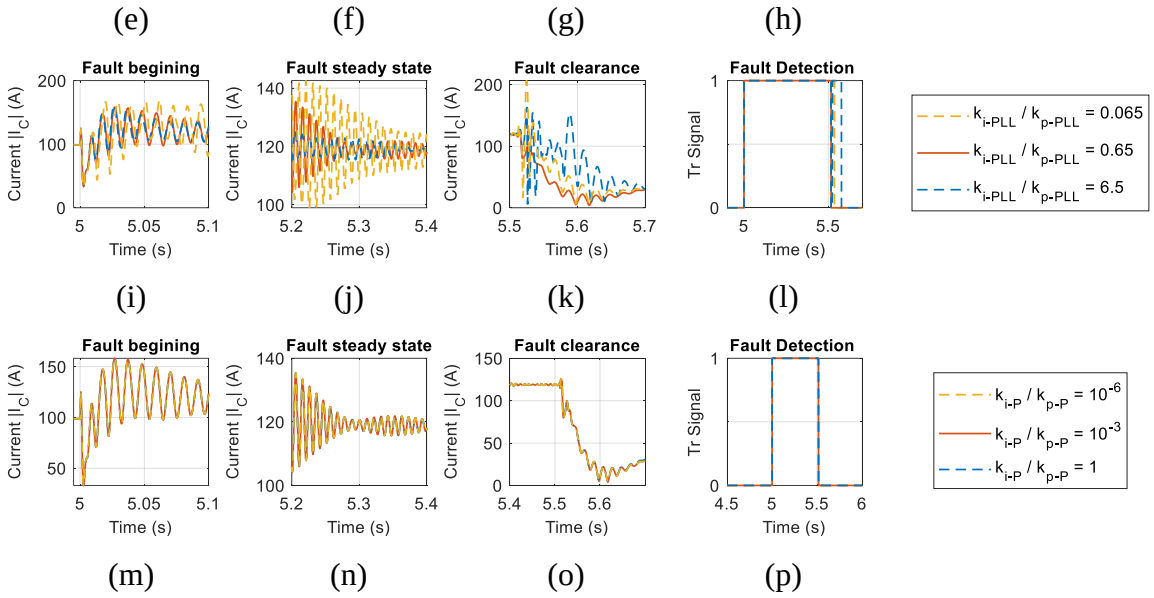


Figure 4.18. Parameter sensitivity analysis in the low SCR case: column (a,e,i,m) shows the currents at the beginning of the fault, column (b,f,j,n) shows the currents during the fault steady-state, column (c,g,k,o) shows the currents during fault recovery, and column (d,h,l,p) shows the new FDA outputs. Row (a,b,c,d) shows the response for varying time constant $\boldsymbol{\tau}_{fv}$ of the new FDA voltage filter, row (e,f,g,h) shows the response for varying time constant $\boldsymbol{\tau}_{cc}$ of the current controller, row (m,n,o,p) shows the response for varying PLL bandwidth $k_{i\text{-}PLL}/k_{p\text{-}PLL}$, and row (q,r,s,t) shows the response for varying APL bandwidth $k_{i\text{-}P}/k_{p\text{-}P}$

4.6.3 Comparison between the low and high SCR cases

Parameter sensitivity analysis can be used as a reference for tuning the improved dual VSM structure. Table 4.2 summarizes the best values for each case.

The lowest τ_{fv} was the best for two fault periods (beginning and recovery) in both SCR cases. The same effect was observed for τ_{cc}, where the lowest value showed the best current response in both SCR cases, indicating that a faster current controller is recommended. Meanwhile, $k_{i\text{-}PLL}/k_{p\text{-}PLL}$ had a better performance for the medium value in both SCR cases because the PLL behaviour is highly affected by faults, and inappropriate tuning may cause unsuccessful controller switching during fault recovery. Furthermore, $k_{i\text{-}P}/k_{p\text{-}P}$ had no effect on the control response.

Table 4.2. Summary of the optimal control parameters with respect to the fault beginning, steady-state, and recovery

Factors	SCR	Fault response performance		
		Fault beginning	Fault steady-state	Fault recovery
τ_{fv} for the filter voltage signal	1.4	Low	No change	No change
	5	Low	No change	No change
PLL parameters ratio $k_{i\text{-}PLL}/k_{p\text{-}PLL}$	1.4	Medium	Medium	Medium
	5	Medium	Medium	Medium
CC time constant τ_{cc}	1.4	Low	Low	Low
	5	Low	Low	Low
APL parameters ratio $k_{i\text{-}P}/k_{p\text{-}P}$	1.4	No change	No change	No change
	5	No change	No change	No change

4.7 Introduction of an improved FDA for future implementations

In this section, an Improved FDA (IFDA), which is applicable for wider range of SCR, is introduced. The IFDA can operate at very low SCRs (SCR ≥ 1). The voltage injected by the converter in very low SCRs is very high; therefore, a voltage reduction method is required (referred to here as reference calculator for voltage regulation). The method uses the voltage magnitude of pn sequences to dampen the reactive power reference, as shown in Figure 4.19. The nominal voltage is multiplied by 1.2 and then subtracted from the addition of both voltage magnitudes, which is a voltage surplus. Subsequently, the difference is multiplied by k_v and then subtracted from the reactive power reference.

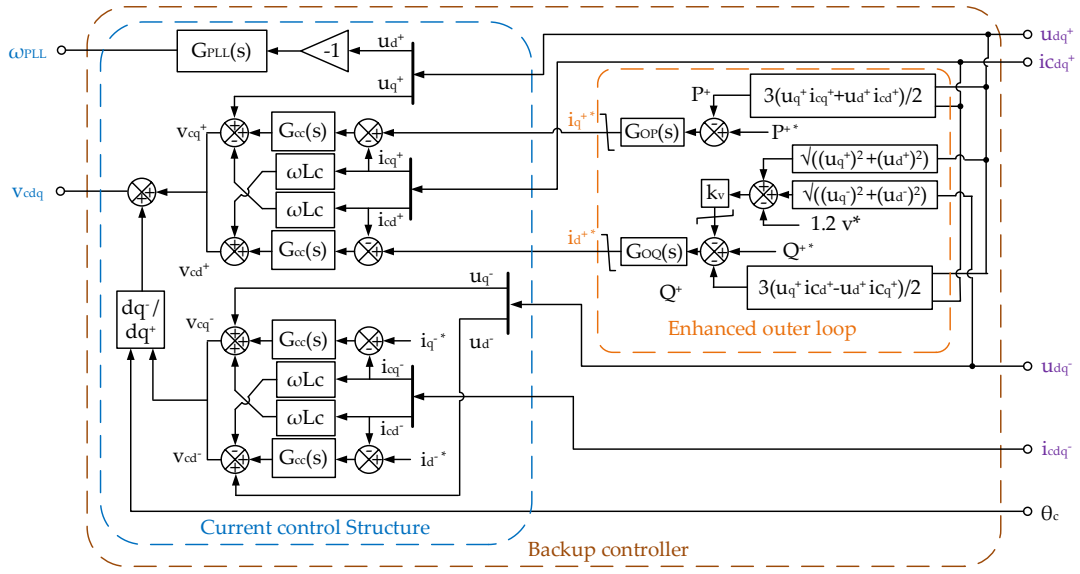


Figure 4.19. Enhanced backup controller with an outer loop with reference calculator for voltage regulation

Figure 4.20 shows the IFDA, where a separate condition for the negative sequence voltage is created to identify unbalanced faults in very low SCRs.

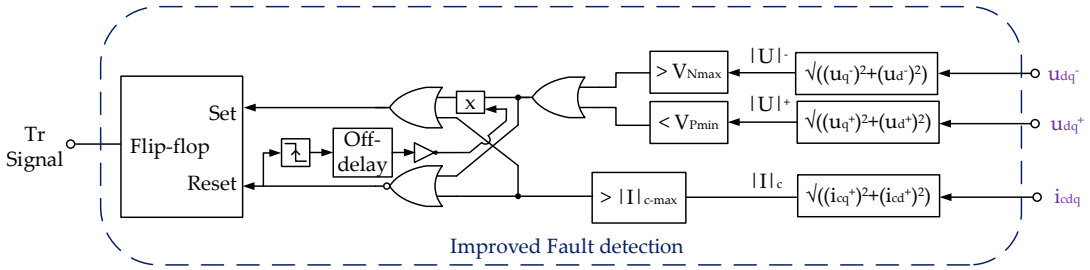


Figure 4.20. Schematic of the IFDA

Figure 4.21 and 4.22 show the voltage and current for the improved controller subjected to single-phase and three-phase-to-ground faults, respectively, in which a high SCR is used to verify the controller response behaviour. Moreover, the same study is applied in very low SCR, as shown in Figure 4.23 for a single-phase-to-ground fault and in Figure 4.24 for a three-phase-to-ground fault. The figures show a decrease in the beginning of the fault current, which is a result of the new reactive power recalculation based on the PCC voltage rather than calculating the new reference from the current reference.

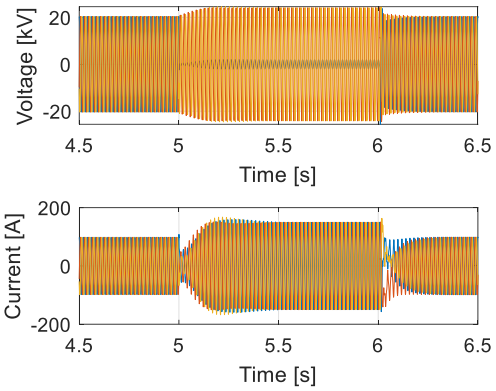


Figure 4.21. Three-phase waveforms at the PCC for the voltage and current after applying a single-phase-to-ground fault in high SCR

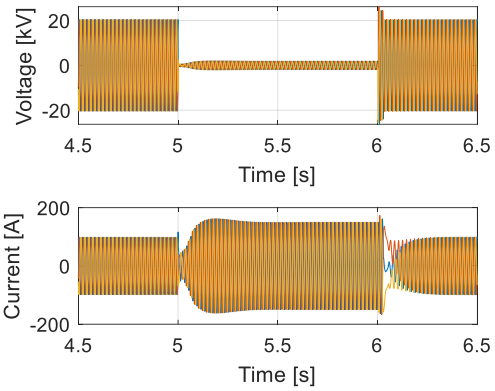


Figure 4.22. Three-phase waveforms at the PCC for the voltage and current after applying a three-phase-to-ground fault in high SCR

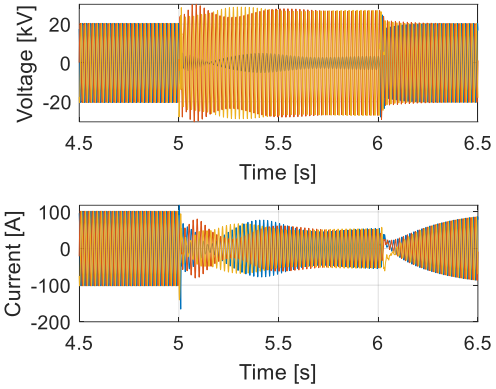


Figure 4.23. Three-phase waveforms at the PCC for the voltage and current after applying a single-phase-to-ground fault in low SCR

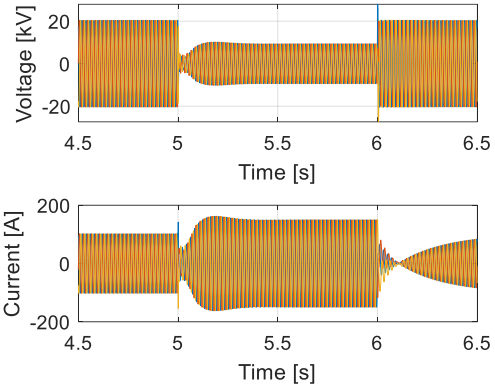


Figure 4.24. Three-phase waveforms at the PCC for the voltage and current after applying a three-phase-to-ground fault in low SCR

4.7.1 Comparison between the proposed structure and grid-following mode

In this section, the responses of the improved dual VSM structure shown in Figure 4.4 is compared to that of grid following converter with a pn CC structure shown in Figure 4.27 whose references are changed during faults.

The converter is assumed to work on 60% of the full load during the normal condition. The control structure was subjected to two types of faults to reveal its strength. Both faults were applied at the midpoint of the grid Thevenin impedance (Rn and Ln), where the first fault is a single-phase-to-ground fault and the second fault is a three-phase-to-ground fault. The faults were applied at 5 s and cleared at 6 s to show the steady-state performance of the current during faults. Figure 4.25 shows the voltage and current waveforms for a single-phase-to-ground fault, which shows a good current control capability and smooth transition between controllers. Figure 4.26 shows the three-phase-to-ground voltage and current waveforms, which also shows good control capability and smooth transition.

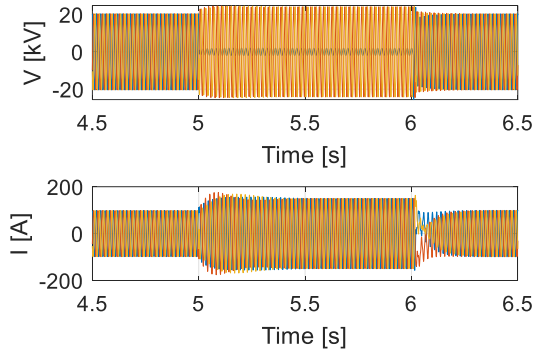


Figure 4.25 PCC voltage and current for VSM–CC for a single-phase-to-ground fault

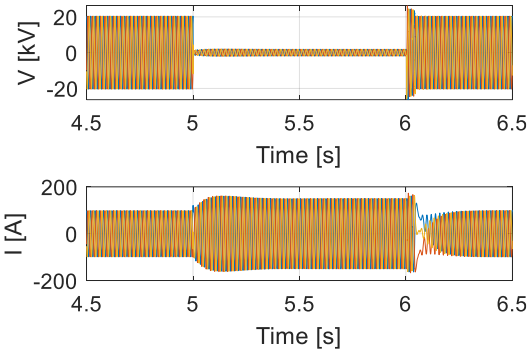


Figure 4.26 PCC voltage and current for VSM–CC for a three-phase-to-ground fault

The second test is for pn CC in which the CC has no outer loop. The absence of the outer loop decreases any control loop interaction and enhances the current control capability. Under a fault condition, the fault detection output was used to switch from active current injection to full reactive current injection. The fault detection method, filters, and CC tunings were the same as in the previous test case. The same fault

scenarios were applied for comparison with the prementioned control scheme. The schematic of the CC is shown in Figure 4.27.

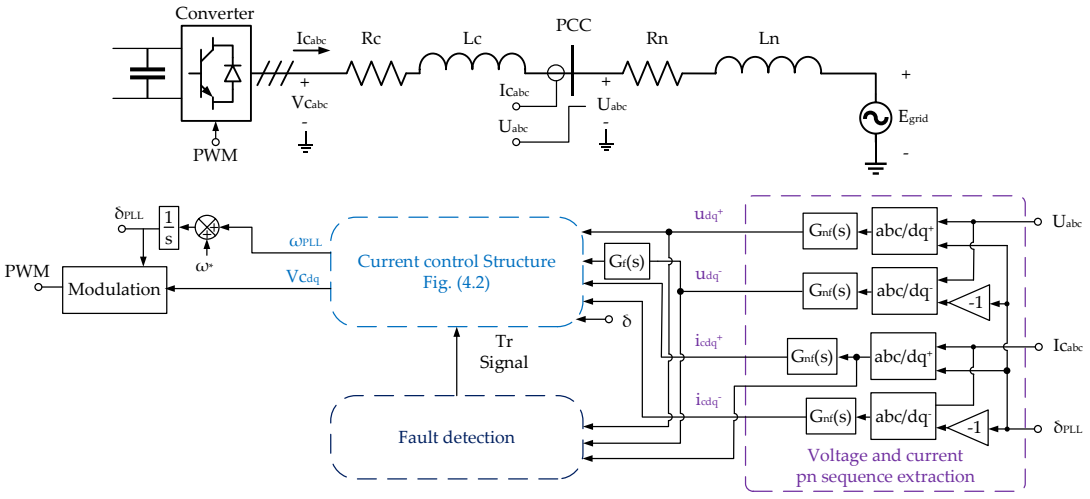


Figure 4.27 Schematic of a CC

Figure 4.28 shows the PCC voltage and current waveforms for a single-phase-to-ground fault in which almost no difference was observed between Figure 4.28 and Figure 4.25. Moreover, the recovery of the CC had a small current overshoot, as shown in Figure 4.28. The same case was applied for Figure 4.29, and almost no difference was observed except for the current recovery.

This comparison shows that a VSM with a backup CC is a viable alternative to the CC.

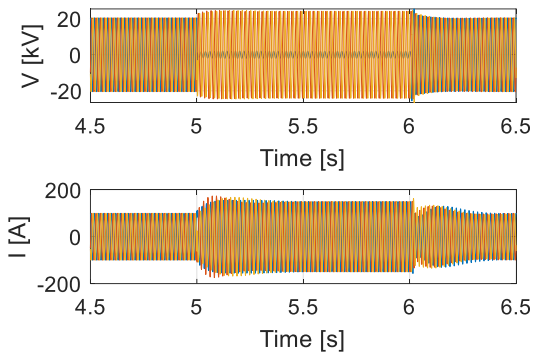


Figure 4.28 PCC voltage and current for a CC during a single-phase-to-ground fault

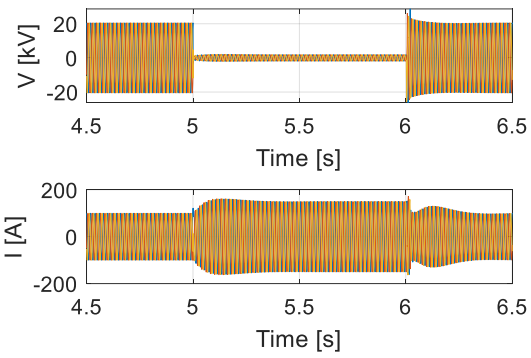


Figure 4.29 PCC voltage and current for a CC during a three-phase-to-ground fault

4.8 Chapter summary

In this chapter, the limitations of the conventional dual VSM structure were discussed. The structure was tested in Section 4.3 to reveal the challenges introduced by weak grid conditions. Under weak grid conditions, an increase in the voltage applied by the converter as a result of an increase in the grid impedance caused the voltage signal of the conventional FDA to fail. Therefore, a new FDA was proposed in Section 4.4, which had a better performance in strong and weak grids. Moreover, an outer loop was added to the current controller, which used a current reference saturation method to limit the current in strong grids.

Furthermore, the sensitivity analysis of the improved dual VSM structure at different fault locations was conducted under strong and weak grid conditions. The analysis showed that the new FDA overcomes the high voltage issue prevalent in weak grids. The balanced and unbalanced faults were handled by the improved dual VSM structure at each fault location.

In addition, the outer loop provided adequate maximum reactive current injection for the fault locations in low and high SCRs. The current reference saturation method limited the current in all the test cases in the strong grid condition it was designed for.

The consecutive faults test showed that the controller can limit the current even under tough conditions such as two consecutive faults. A control parameter sensitivity analysis was introduced to reveal the effect of changing the controller parameters on the control response. The control response was stable for all the test cases using medium tuning values. Subsequently, each control parameter was changed to two different values to observe the change in the control response. The result showed the effect of changing each control parameter on the controller response during unbalanced faults in low and high SCRs.

Several observations were obtained from the control parameter sensitivity analysis, including:

- The lower the voltage time constant of the new FDA, the better the fault detection response.

- Significantly reducing the PLL bandwidth as suggested in the literature is less effective in stabilising the response during low SCR during faults.

- The faster the CC time constant is recommended as it reduces the current transients.

- The tuning of the APL has no effect on the controller response.

The control parameter sensitivity analysis can be used as a reference for the tuning of a control structure resembling the improved dual VSM.

An improved FDA was also introduced as part of a future work, and it operates until SCR = 1. This FDA uses negative sequence as a separate condition, which can directly identify the negative sequence and generate a switching action for the converter so that the converter can inject a balanced reactive current. This approach was compared to a traditional grid-following control approach, revealing no noticeable difference between both controllers in handling faults. This comparison proves the reliability of the proposed control structure.

Chapter 5

Comparison of Synchronization Techniques During FRT

5.1 Introduction

Based on the research conducted in Chapter 4 on switching to a current control-based loop during AC faults, it was proved that the improved dual VSM structure can limit the AC fault current. However, there is no extensive research on the impact of different synchronization techniques on the backup controller. In this chapter, the performance of the most common synchronisation techniques that can be used during faults is assessed. The synchronization techniques considered are PLL, PSL, and PLL output freezing (disabling of the synchronization loop). Furthermore, a new synchronization technique based on the current magnitude is introduced.

The methodology used in this chapter begins with large signal stability analysis using phase portrait, which exhibits the VSC controller angle stability during grid voltage sags. However, the equations used to model the VSC for large signal analysis are usually approximate and some of the converter behaviours are ignored, which requires further evaluation methods to explain the controller behaviour during the fault steady-state and transient periods. As an alternative, small signal analysis can provide detailed information of the steady-state operation but it is not suitable for large disturbances. Therefore, extensive time-domain simulations for multiple scenarios are used to conduct comparative parametric sweep analysis, which is then used to study the behaviour of each synchronization technique. The comparative analysis of the synchronization techniques is performed, and different variables are evaluated, including the current magnitude, active power, and reactive power. The current

magnitude is used to show that the converter output current is maintained within limit during the fault steady-state and transient periods, and the active and reactive power waveforms are used to explain the grid support capability for each synchronization technique. The analysis starts with a parametric sweep analysis for the controller gains of each synchronisation technique, which identifies the best tuning for each synchronization. Based on this analysis, the controller gains are tuned and used to compare different synchronization techniques in strong and weak grid conditions. The comparison evaluates the current transients resulting from controller loop switching and the active and reactive power injection capability. The comparison output reveals the synchronization technique that can satisfy most of the grid code requirements.

5.2 Current synchronization

Contemporary grid codes require converter-based generation to inject reactive power to help boost the AC voltage in case of faults. However, during faults, synchronization is required to provide maximum reactive current to support the grid voltage.

Based on the principle that the power converter must inject maximum current during faults, a new synchronisation method is suggested in this section. As during fault, current injection is unlimited, but the voltage is limited by the fault. Current synchronization is a new synchronization technique that seeks to keep the power converter connected with a control structure that uses current for synchronization with the grid during faults. In the following sections, the principle of the current synchronisation technique will be described.

5.2.1 Relationship between the current magnitude and power angle

Figure 5.1 shows the relationship between the current magnitude and voltage angle, which shows two voltage sources, representing the converter voltage and Thevenin grid voltage, connected through an impedance that represents the equivalent of the converter filter impedance and Thevenin grid impedance.

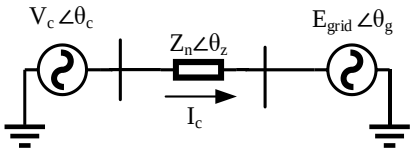


Figure 5.1. Two sources connected through an impedance

The converter is assumed to be in the inverter mode such that current flows from the converter to the grid. Hence, the current equation is given by:

$$\tilde{I}_c = \frac{V_c \angle\theta_c - E_{grid} \angle\theta_g}{Z_n \angle\theta_c} \tag{5.1}$$

The voltage magnitude of the converter is assumed to be equal the grid voltage, since both voltages magnitudes can be approximately equal. Thus, the assumption $E_{grid} = V_c$ is applicable. After applying the assumption, the current equation in Eq. (5.1) in rectangular form is given by:

$$\tilde{I}_c = \frac{E_{grid}}{Z_n}(\cos(\theta_g - \theta_z) - \cos(\theta_g - \theta_z)) + j\,\frac{E_{grid}}{Z_n}(\sin(\theta_c - \theta_z) - \sin(\theta_g - \theta_z)) \tag{5.2}$$

By simplifying Eq. (5.2) using some trigonometric functions, the current is given by:

$$\tilde{I}_c = \frac{2E_{grid}}{Z_n}\left(\cos\frac{\theta_c + \theta_g - 2\theta_z}{2}\sin\frac{\theta_c - \theta_g}{2}\right) - j\,\frac{2E_{grid}}{Z_n}(\sin\frac{\theta_c + \theta_g - 2\theta_z}{2}\sin\frac{\theta_c - \theta_g}{2}) \tag{5.3}$$

Therefore, the magnitude of the current can be expressed by:

$$|I|_c = \frac{2|E|_{grid}}{Z_n}\sin\frac{\theta_c - \theta_{grid}}{2} \tag{5.4}$$

A phasor diagram for circuit shown in Figure 5.1 is shown in Figure 5.2, at which the equal voltage magnitudes assumption is applied as the previous derivation and the same result is obtained.

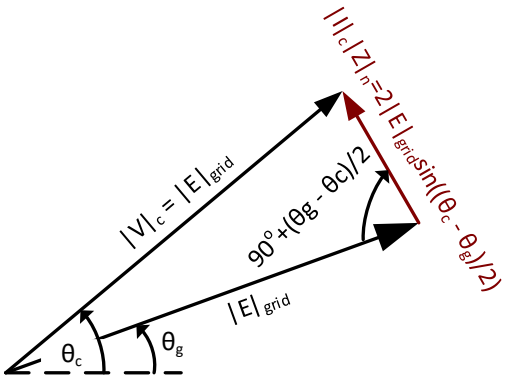


Figure 5.2. Phasor diagram for calculating the current magnitude

From the power angle equation, the difference between the two voltage angles is δ, which leads to a relationship between the magnitude and power angle as $I \propto \frac{\delta}{2}$. This relationship is similar to the power angle relationship, which can help in creating a relevant synchronization control structure. The PSC, as mentioned in Chapter 2, is a proportional controller based on power angle relationship that calculates the angle according to the error between the active power reference and feedback. Similarly, current synchronization can be created using a proportional controller based on the relationship in Eq. (5.4) that calculates the angle according to the error between the current reference and feedback.

5.2.2 Time-domain simulation

In this section, the performance of the suggested current synchronisation loop is analysed by replacing the APL of the VSM structure in the normal condition. Figure 5.3 shows the schematic of the control structure, where a voltage controller is added to control the converter voltage magnitude, and current magnitude is used for synchronization. The angle output of the current synchronization is used to modulate the voltage but it is not used to calculate the converter feedback signals. The current synchronization controller $G_{cs}(s)$ is a proportional controller tuned using two different

values to show the effect on the current settling time and oscillations. The voltage controller $G_v(s)$ is tuned with the same tuning of the VSM structure discussed before.

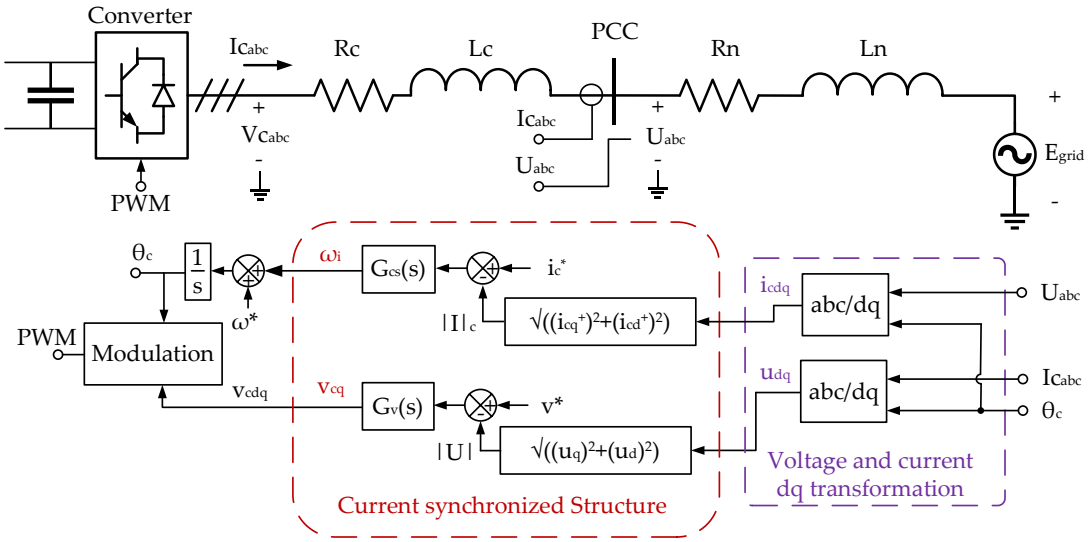
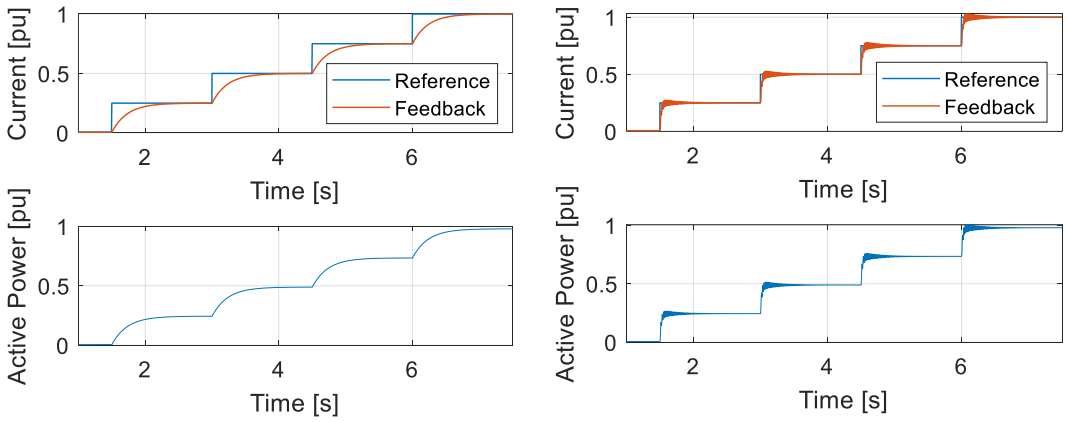


Figure 5.3. Schematic of a current-synchronised controller

The current-synchronized controller was tested by changing the current reference and observing the changes in voltage, current, active, and reactive power. Figure 5.4(a) shows the response at $G_{cs}(s) = 0.008\ \Delta\omega/\Delta I$, where the settling time of the current is almost 1 s. The figure shows that the current reference change is directly linked with the active power as relative active power changes were observed within the active and reactive power waveforms.



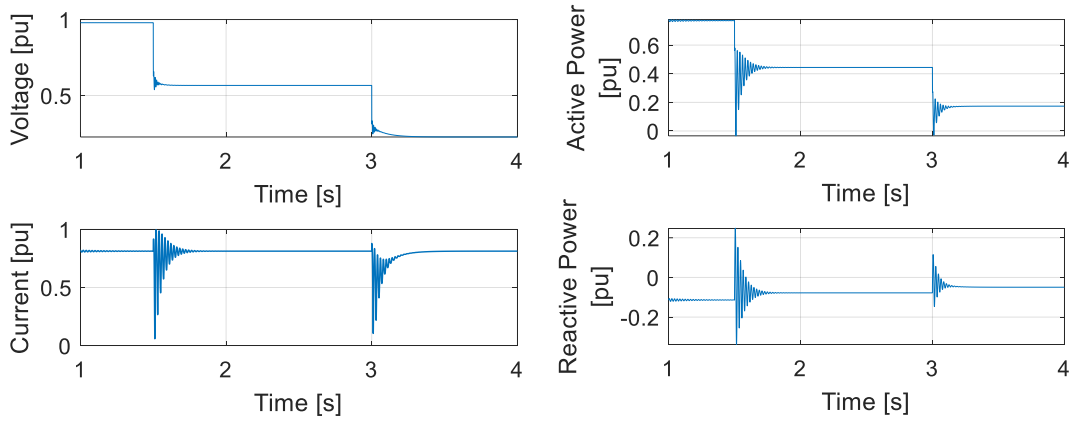
(a) (b)

Figure 5.4. Current-synchronized controller response through current magnitude and active power waveforms: (a) $G_{cs}(s)=0.008\ \Delta\omega/\Delta I$, and (b) $G_{cs}(s)=0.1\ \Delta\omega/\Delta I$

The second tuning for the current synchronization is $G_{cs}(s) = 0.1\ \Delta\omega/\Delta I$, as shown in Figure 5.4(b). The figure shows an improvement in the settling time from 1 to 0.03 s. However, some transient oscillations were observed at the beginning of the current and active power waveforms, which were damped after 0.4 s from the reference change.

Another test case was introduced to show the capability of the current synchronization in different voltage sags. During fault, the voltage controller is disabled and the converters yield a voltage output equal to the PCC voltage. Therefore, the voltage controller is disabled, and the measured voltage is used without any controller.

Multiple voltage sags were applied in this test case, in which 100% voltage sag was maintained until 1.5 s, followed by a 40% voltage sag from 1.5 to 3 s and then a 70% voltage sag from 3 to 4.5 s. The voltage and current waveforms are shown in Figure 5.5(a), which revealed that the current tracked the reference at all values. The active and reactive waveforms were also affected, as shown in Figure 5.5(b), revealing that the active power decreased, whereas the reactive power was slightly increased by increasing the voltage sag. The study shows that current synchronization can control the current as the grid voltage changes. Nevertheless, some considerations are required for a stable operation.



(a) (b)

Figure 5.5. Current synchronization response to 40% voltage sag from 1.5 to 3 s and 70% voltage sag from 3 to 4.5 s: (a) voltage and current waveforms, (b) active and reactive power waveforms

This study reveals the response of a controller synchronized with current, and some observations made are as follows:

- An increase in the synchronization loop gain G_{cs} improves the settling time but introduces oscillations after the step change.
- An increase in the current reference is directly linked to an increase in the active power.
- Current synchronization can control the current for different voltage variations, except for very low voltage magnitudes.

Meanwhile, some disadvantages were observed during operation in the rectifying mode, which requires further study of the current and angle coupling for operation in different modes. Additionally, a step change in the frequency made the current synchronization unstable, which lost control over the current.

However, these disadvantages can be disregarded because during fault, especially for a fault close to the PCC, VSC is not required to operate in the rectifying mode, and changes in frequency cannot affect the VSC response as the VSC can be considered in isolated mode.

5.3 Methodology of the comparison of synchronization techniques

A study to show the benefits of different VSC synchronization techniques is required to improve the implementation of a VSC control structure that complies with the grid code. The study involves analysing the synchronization techniques within different voltage sags and fault types. Large signal analysis was used to show the angle stability for each synchronization technique, and a mathematical model or graphical representation was used to identify the stable operating condition [179]. This analysis was used to study the large disturbances (that is, faults) affecting a nonlinear converter control system [179], unlike small signal analysis, which can be applied on linearised operating points [180]. However, the large signal model is unsuitable for studying the dynamics of a power converter during faults [181], especially the transients caused by switching to alternative control structure. Therefore, a set of extensive time-domain simulations are studied to investigate the dynamic behaviour of power converters

during faults, which cannot be discussed through approximate models used in large signal analysis. The schematics of techniques for the synchronization loop of the alternative control structure replacing the VSM loops during faults, which are included in this analysis:

- PLL shown in Figure 5.6(a)
- APL shown in Figure 5.6(b)
- PSL shown in Figure 5.6(c)
- Current synchronization (CS) shown in Figure 5.6(d)

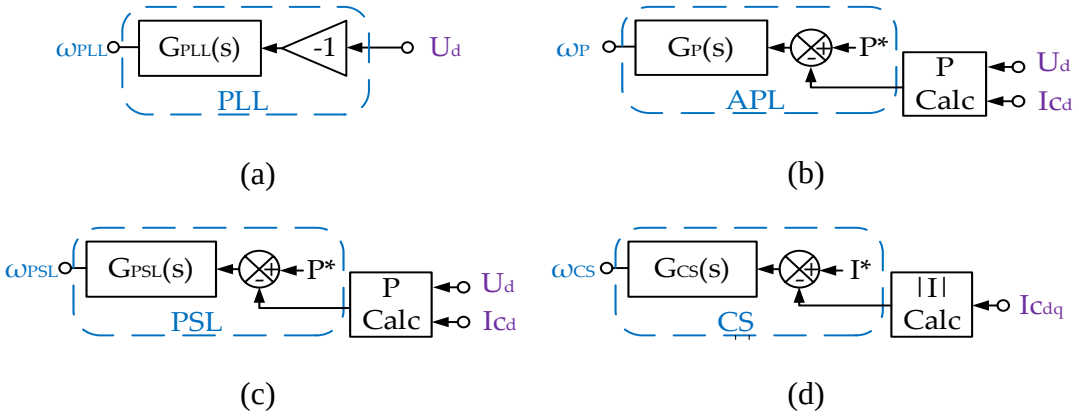


Figure 5.6. Schematic of the controller Synchronization techniques: (a) PLL, (b) APL, (c) PSL, (d) CS

Phase portrait is a large signal analysis method [182], and it is a sketch of the converter control structure [161]. The sketch uses the relationship between the converter angle and the derivative of the converter angle in terms of voltage or reactive power. Phase portrait identifies stable synchronization techniques within different voltage sags, which are then used in the time-domain simulation analysis. Subsequently, time-domain simulations begin with parametric sweep analysis, which is used to find the tuning parameters of the synchronization controller and evaluate its effect on the controller behaviour. In the next step, the accepted tuning parameters from the previous study are used to compare all the synchronization techniques. The comparison shows the advantage and disadvantage of each synchronization technique, which helps in identifying the FRT implementation that complies with the grid code.

5.4 Large signal analysis

In this section, the stability of the synchronization loops for different grid voltage sags is discussed. Phase portrait was used to analyse the synchronization loops while assuming that the converter voltage controller is the same as the grid voltage. The phase portrait is a sketch of the relationship between the angle and angle derivative.

The phase portrait sketch describes the stability of the synchronization loop according to a trajectory at the operating conditions [161]. The synchronization loop with an integrator in the controller (that is, PLL or APL) shows stable operating conditions when the trajectory tends to the zero axis ($\dot{\delta} = 0$) as the integrator action is successful. The synchronization loop without an integrator (i.e. PSL or CS loop) is stable when the trajectory is converging towards zero axis ($\dot{\delta} = 0$), and moving from positive side ($\dot{\delta} > 0$). A simplified VSC model was used to derive the equations used in the analysis. The model uses the synchronization loop equation and assumes that the converter voltage is the same as the grid voltage. This model was used to analyse only the stability of the synchronization loop, and other control loops were ignored.

5.4.1 PLL analysis

Figure 5.7 shows the block diagram of a PLL, which is a standard implementation without automatic gain control. The PLL controller is a PI controller, whose expression is given by:

$$g_{PLL}(t) = k_{p-PLL} + \int k_{i-PLL} dt \tag{5.5}$$

where $k_{p\text{-}PLL}$ and $k_{i\text{-}PLL}$ are the proportional and integral gains, respectively.

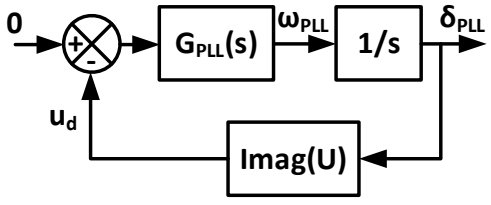


Figure 5.7. PLL block diagram

The PLL angle is the integration of the frequency (controller output), which is given by:

$$\dot{\delta}_{PLL} = \omega_{PLL} \tag{5.6}$$

Because the controller's objective is to force the direct voltage component to zero, the reference is always zero and the equation is:

$$\omega_{PLL} = -u_d \times g_{PLL}(t) \tag{5.7}$$

where $u_d$is the imaginary component of U.

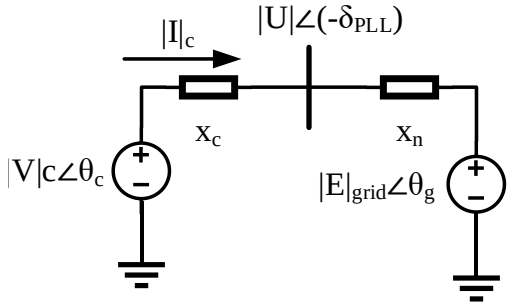


Figure 5.8. Simple VSC connected to the grid

According to a simple representation of a grid-connected converter shown in Figure 5.8, using the voltage divider rule the relation between the converter voltage and the PCC voltage is:

$$|U|e^{-j\delta_{PLL}} = |V|_c e^{j\theta_c} \frac{x_n}{x_c + x_n} \tag{5.8}$$

From the imaginary part of Eq. (5.8) u_d is

$$u_d = v_c \frac{\sin(\theta_c)}{\sin(-\delta_{PLL})} \frac{x_n}{x_c + x_n} \tag{5.9}$$

By substituting Eq. (5.5), Eq. (5.6), and Eq. (5.9)into Eq. (5.7), the result becomes:

$$\dot{\delta}_{PLL} = -k_{p-PLL}|V|_c \frac{\sin(\theta_c)}{\sin(-\delta_{PLL})} \frac{x_n}{x_c + x_n} - \int k_{i-PLL}|V|_c \frac{\sin(\theta_c)}{\sin(-\delta_{PLL})} \frac{x_n}{x_c + x_n} dt \tag{5.10}$$

By differentiating both sides

$$\ddot{\delta}_{PLL} = \frac{x_n v_c}{x_c + x_n} k_{p_{PLL}} \frac{d}{dt}\left(-\frac{\sin(\theta_c)}{\sin(-\delta_{PLL})}\right) + \frac{x_n v_c}{x_c + x_n} k_{i_{PLL}} \left(-\frac{\sin(\theta_c)}{\sin(-\delta_{PLL})}\right) \tag{5.11}$$

From The power transfer of the circuit shown in Figure 5.8 between the converter voltage v_C and the PCC voltage u the converter angle θ_c can be expressed by:

$$\theta_c = \sin^{-1}\left(\frac{2Px_c}{3|U||V|_c}\right) - \delta_{PLL} \tag{5.12}$$

By substituting Eq. (5.12) into Eq. (5.11), the equation is:

$$\ddot{\delta}_{PLL} = \frac{x_n|V|_c}{x_c + x_n} k_{p_{PLL}} \frac{d}{dt}\left(-\frac{\sin\left(\sin^{-1}\left(\frac{2Px_c}{3|U||V|_c}\right) - \delta_{PLL}\right)}{\sin(-\delta_{PLL})}\right) + \frac{x_n|V|_c}{x_c + x_n} k_{i_{PLL}} \left(-\frac{\sin\left(\sin^{-1}\left(\frac{2Px_c}{3|U||V|_c}\right) - \delta_{PLL}\right)}{\sin(-\delta_{PLL})}\right) \tag{5.13}$$

By applying the differentiation, the final equation is:

$$\ddot{\delta}_{PLL} = \frac{x_n|V|_c}{x_c + x_n} k_{p_{PLL}}(-\dot{\delta}_{PLL}) \left(\frac{\sin\left(\sin^{-1}\left(\frac{2Px_c}{3|U||V|_c}\right) - \delta_{PLL}\right)\cos(-\delta_{PLL})}{\sin^2(-\delta_{PLL})} - \frac{\sin(-\delta_{PLL})\cos\left(\sin^{-1}\left(\frac{2Px_c}{3|U||V|_c}\right) - \delta_{PLL}\right)}{\sin^2(-\delta_{PLL})} \right) + \frac{x_n|V|_c}{x_c + x_n} k_{i_{PLL}} \left(- \frac{\sin\left(\sin^{-1}\left(\frac{2Px_c}{3|U||V|_c}\right) - \delta_{PLL}\right)}{\sin(-\delta_{PLL})} \right) \quad (5.14)$$

The phase portrait of the PLL for different grid voltages (E_{grid}) is shown in Figure 5.9 at 1 pu active power, where the different curves are for different voltage magnitudes that represent different voltage sags. The 1 pu and 0.7 pu grid voltages are stable as both tends to zero as shown in the zoomed part, however the 0.2 pu grid voltage is unstable as the curve is above zero axis ($\dot{\delta} = 0$).

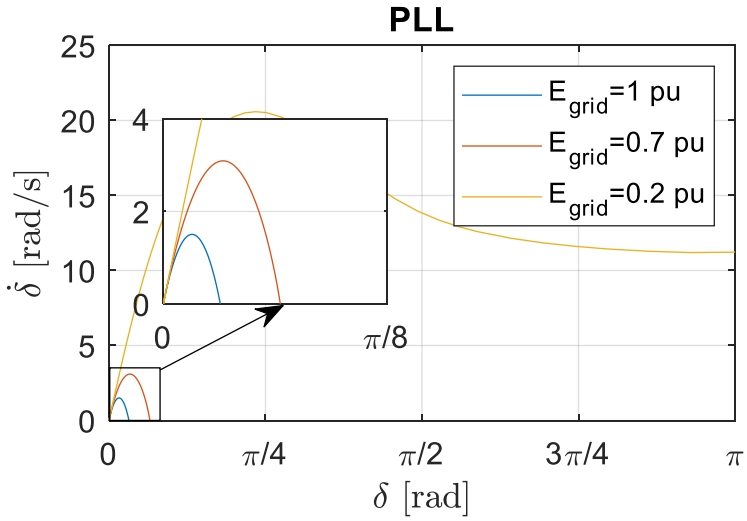


Figure 5.9. Phase portrait for the PLL at P = 1 pu

The results of the phase portrait sketch was validated using a time-domain simulation, which shows the response of a grid-connected VSC for different voltage sags. The

VSC controller used is a current controller with an active and reactive power outer loop and a PLL for synchronization.

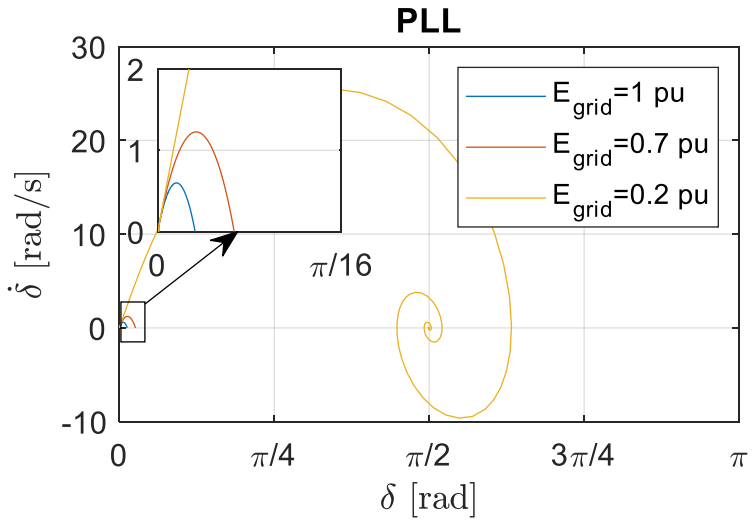


Figure 5.10. Phase portrait for the PLL at P = 0.4 pu

Figure 5.10 shows a VSC synchronized with PLL with 0.4 pu active power. In this case the curve of the 0.2 pu grid voltage tends to zero, which shows that the PLL can maintain the stability for lower active power reference.

5.4.2 APL analysis

Figure 5.11 shows the active power loop, where the controller is a PI controller expressed by:

$$g_{APL}(t) = k_{p-APL} + \int k_{i-APL}\, dt \tag{5.15}$$

where $k_{p\text{-}APL}$ and $k_{i\text{-}APL}$ are the proportional and integral gains, respectively.

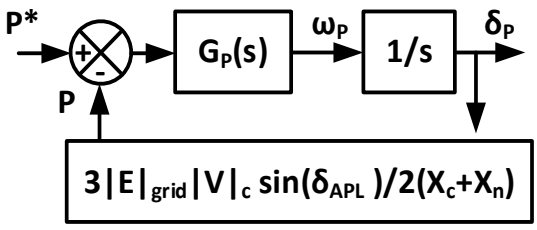


Figure 5.11. Schematic of an active power loop

The forward path is expressed as:

$$\dot{\delta}_P = \omega_P = g_P(t)(P^* - P) \tag{5.16}$$

By substituting Eq. (5.15) into Eq. (5.16), we obtain:

$$\ddot{\delta}_P = (k_{i-P})P^* - \left(k_{p-P}\dot{P} + k_{i-P}P\right) \tag{5.17}$$

The feedback power can be calculated using the power angle equation, which is expressed by:

$$P = \frac{3}{2}\frac{|E|_{grid}|V|_c}{X_n + X_c}\sin\delta_P \tag{5.18}$$

By substituting Eq. (5.18) into Eq. (5.17), the final equation becomes:

$$\begin{aligned}\ddot{\delta}_P = (k_{i-P})P^* \\ -\Bigg(k_{p-P}\frac{3}{2}\frac{|E|_{grid}\cos\delta_P}{X_n + X_c}|V|_c\dot{\delta}_P \\ + k_{i-P}\frac{3|E|_{grid}\sin\delta_P}{2\,(X_n + X_c)}\,|V|_c\Bigg)\end{aligned} \tag{5.19}$$

Figure 5.12 shows the phase portrait of the APL for different grid voltages (E_{grid}), where the synchronization loop is stable for both 1 and 0.7 pu voltages as both trajectories tend to the zero axis. However, the trajectory of the 0.2 pu voltage tends to infinity, which represents an unstable operation in very low voltage condition.

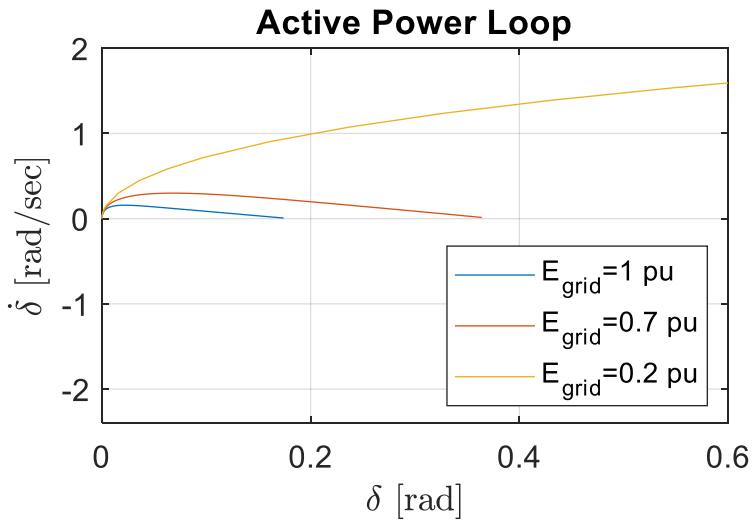


Figure 5.12. Phase portrait for the active power loop

Therefore, the active power loop is a source of instability during faults. Figure 5.13 shows the results from a simulation where a VSM is synchronized using an APL. The results show the relationship between the frequency and magnitude of the converter angle, which resembles the phase portrait sketch. The blue curve represents the VSM response during normal condition, which was stable as the curve tended to the zero axis. The red curve shows the response during a three-phase-to-ground fault, which tended to infinity and represents an unstable condition.

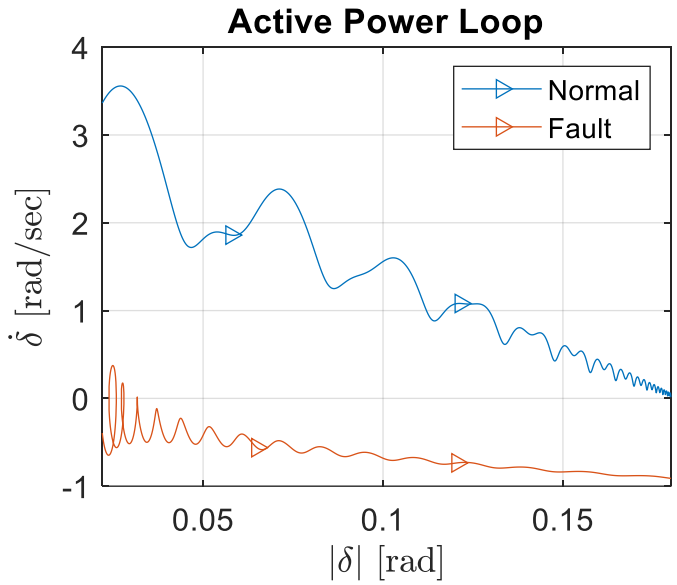


Figure 5.13. Phase portrait sketch from simulation

5.4.3 PSL analysis

PSL controller is a proportional controller only, unlike APL that has a PI controller. Figure 5.14 shows the block diagram of the PSL.

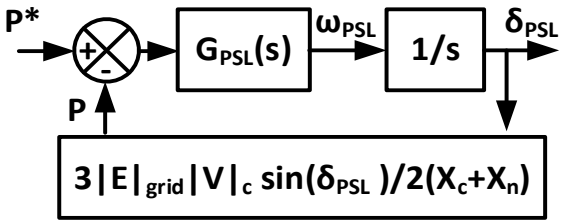


Figure 5.14. PSL block diagram

The controller consists of a proportional gain given by:

$$g_{PSL}(t) = k_{p-PSL} \tag{5.20}$$

$$\dot{\delta}_{PSL} = g_{PSL}(t)\ (P^* - P) \tag{5.21}$$

The forward path can be expressed by:

The feedback is expressed by:

$$P = \frac{3}{2}\frac{|E|_{gid}|V|_c}{(X_n + X_c)}\sin\delta_{PSL} \tag{5.22}$$

By substituting Eq. (5.22) into Eq. (5.21), the result becomes:

$$\dot{\delta}_{PSL} = k_{p-PSL}P^* - k_{p-PSL}\frac{3}{2}\frac{|E|_{grid}\sin\delta_{PSL}}{(X_n + X_c)}|V|_c \tag{5.23}$$

PSL has no integral controller; therefore, the curve in the phase portrait sketch passes through the zero axis ($\dot{\delta} = 0$) for a stable operation. Figure 5.15 shows the PSL phase portrait sketch, where the blue and the red curves passing through the zero axis show a stable operation for the 1 and 0.7 pu voltages. However, the yellow curve representing the 0.2 pu voltage is unstable because it did not intersect with the zero axis. The instability at a very low voltage was a result of high power reference. The

stability was regained after decreasing the power reference, as shown in Figure 5.16, where all the curves shifted downwards such that the yellow curve passed through the zero axis.

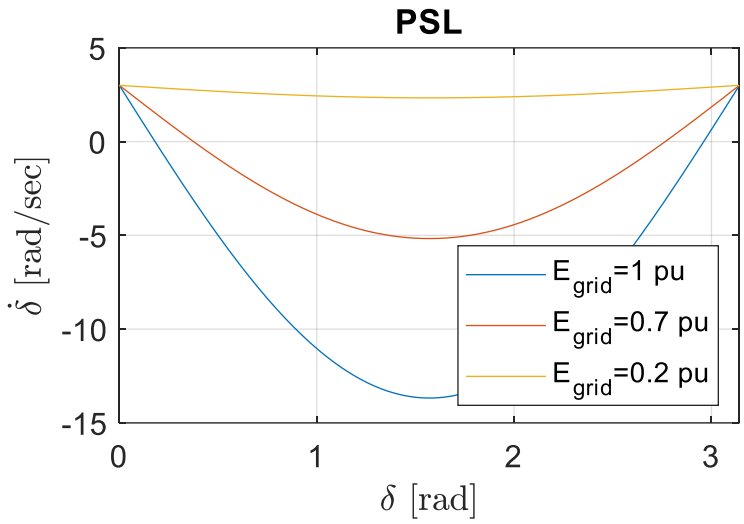


Figure 5.15. Phase portrait for the power synchronization loop at 0.6 P_{ref}

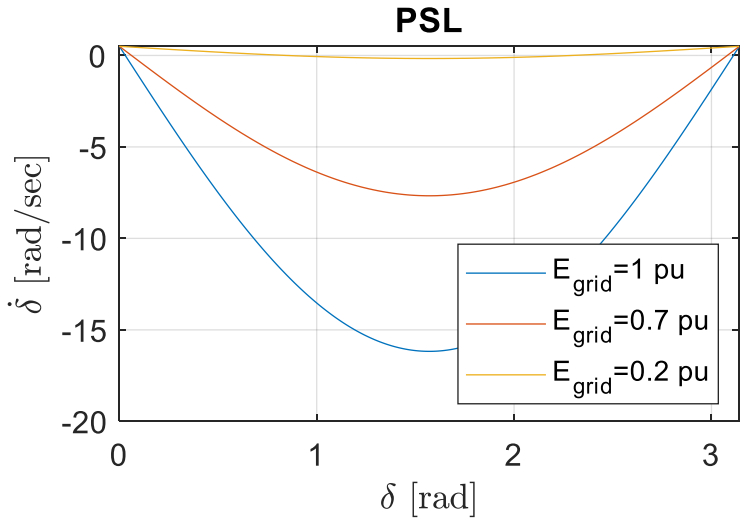


Figure 5.16. Phase portrait for the power synchronization loop at 0.1 P_{ref}

5.4.4 CS analysis

In this section, the stability of the current synchronization magnitude is discussed using phase portrait. Figure 5.17 shows the block diagram of a full CS structure.

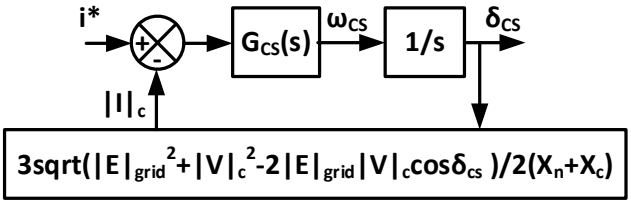


Figure 5.17. Block diagram of current synchronization

The CS controller consists of a proportional gain expressed by:

$$g_{CS}(t) = k_{p-CS} \tag{5.24}$$

The forward path is expressed by:

$$\dot{\delta}_{CS} = G_{CS}(i^* - |I|_c) \tag{5.25}$$

The current feedback is expressed by:

$$|I|_c = \frac{|S|}{|V|_c} = \frac{\sqrt{P^2 + Q^2}}{|V|_c} \tag{5.26}$$

where

$$P = \frac{3}{2}\frac{|E|_{grid}|V|_c}{X_n + X_c}\sin\delta_{CS} \tag{5.27}$$

$$Q = \frac{3}{2}\frac{|V|_n{}^2 - |E|_{grid}|V|_c\cos\delta_{CS}}{X_n + X_c} \tag{5.28}$$

By substituting Eqs. (5.27) and (5.28) into Eq. (5.26), we have:

$$|I|_c = \frac{3}{2}\frac{1}{X_c + X_n}\sqrt{|E|_{grid}{}^2 + |V|_c{}^2 - 2|E|_{grid}|V|_c\cos\delta_{CS}} \tag{5.29}$$

Finally, by substituting Eq. (5.29) into Eq. (5.25), the result becomes:

$$\dot{\delta} = k_{p-CS}\left(i_0 - \frac{3}{2}\frac{\sqrt{V^2 + E^2 - 2EV\cos\delta_{CS}}}{x}\right) \tag{5.30}$$

Based on Eq. (5.30), the phase portrait for CS is shown in Figure 5.18. Compared to PSL, CS was stable for all voltage levels as all the curves intersected with the zero axis ($\dot{\delta} = 0$). Therefore, CS has an advantage over PSL as it can maintain stability at low voltages.

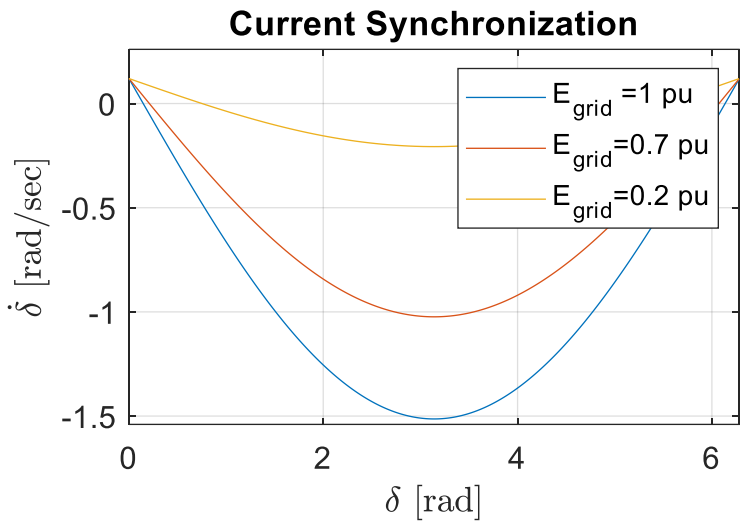


Figure 5.18. Phase portrait for CS at 0.7 pu current reference

5.4.5 Comments

Phase portrait sketches were used in this study to show the large signal stability of synchronization loops while ignoring the behaviour of inner control loops. Table 5.1 presents the summary of the findings of large signal analysis, including the description of the instability of the synchronization techniques in low voltage condition, the instability reason, and the action required to restore stability.

Table 5.1. Summary of the large signal analysis study

	Stability	**Instability reason**	**Action to restore stability during faults**
PLL	Stable in low voltage condition	N/A	N/A
APL	Unstable in low voltage condition for high and low power references	The controller integrator gain is unsuitable for the low voltage condition, and the change in controller tuning cannot maintain stability in high and low voltage conditions	Alternative synchronization is required in the low voltage condition
PSL	Unstable in low voltage condition for high power reference but stable in low voltage condition for low power reference	The high active power reference drives the converter angle to an unstable region under low voltage condition	The active power reference must be reduced while detecting a low voltage condition
CS	Stable in low voltage condition	N/A	N/A

The outcome of the analysis is that power-based methods have challenges with current limitation, especially PI-based structures. However, large signal stability (phase portrait) is an approximate study that ignores inner controllers such as current controller. Therefore, to support the findings, a set of simulations were used to gain a better insight into the response of each synchronization loop.

5.5 Analysis of the time-domain simulations

Large signal analysis is an approximate analysis that uses assumptions and simplifications to investigate the large signal stability of a system. Meanwhile, the transient analysis of the control structure proposed in Chapter 4 cannot be studied using small signal analysis. Therefore, a set of simulations were performed to analyse the behaviour of the control structure (specially the transients) using different synchronization techniques. The simulations begin with the analysis of the best tuning for each technique using parametric sweep analysis. The techniques are then compared using the best tuning parameters from the parametric sweep analysis to show the advantages of each technique.

5.5.1 Parametric sweep analysis

Parametric sweep analysis reveals the most suitable tuning parameters for each synchronization technique considering the stability during fault and transients peaks during transition between the controller loops. The control structure is the same as that in Fig. 4.1, and the rating of the power converter and power system parameters are the same those listed in Table 4.1. The synchronization loop of the backup controller varies in each case. The analysis was divided into two sections: strong and weak grid conditions. Each condition involved subjecting the power converter to single-phase-to-ground and three-phase-to-ground faults. These faults were applied at 5 s and lasted for 1 s to ensure that the steady state of the fault is properly observed for a long fault period. The FDA was idealised using a signal generator, which switched to current control at the same instance of the fault beginning and reset the signal 2 cycles after the fault clearance. The 2-cycle delay was added to show the difference in the transients during recovery after fault.

5.5.1.1 Strong grid condition

The strong grid condition applied here is the same as that considered in Chapter 4. The synchronization control parameters were changed to identify the best tuning parameters in terms of stability and transients. The waveforms used to assess the tuning parameters are current magnitude for the balanced and unbalanced faults and active and reactive power magnitudes for the unbalanced fault.

5.5.1.1.1 Phase-locked loop

In this section, the effect of changing both PLL controller gains are independently analysed. The gains were tuned to have the best performance according to the simulation results, and each gain was changed while keeping the other at the chosen best tuned value. Based on the results in each case, the effect of each controller gain can be explained. The proportional gain ($k_{p\text{-}PLL}$) was changed during a single-phase-to-ground fault, and the current waveform is shown in Figure 5.19(a)–(b), where the current transients increased as a result of a reduction in the proportional gain. The current during three-phase-to-ground fault is shown in Figure 5.19(c)–(d), where the higher proportional gain had the lowest current transients. Figure 5.19(e)–(f) show the active and reactive powers during a single-phase-to-ground fault, where the highest proportional gain had zero active power because the active current component reference was zero. The integral gain ($k_{i\text{-}PLL}$) was then changed to show the effect on the current response. Figure 5.20(a)–(b),(e)–(f) show the current and power responses during a single-phase-to-ground fault in which no change was observed. However, a slight difference was observed in the current response during three-phase-to-ground fault, as shown in Figure 5.20(c)–(d); nevertheless, the lowest $k_{i\text{-}PLL}$ had the lowest transient. This study shows that higher $k_{p\text{-}PLL}$ and lower $k_{i\text{-}PLL}$ are preferred for obtaining a better response during faults.

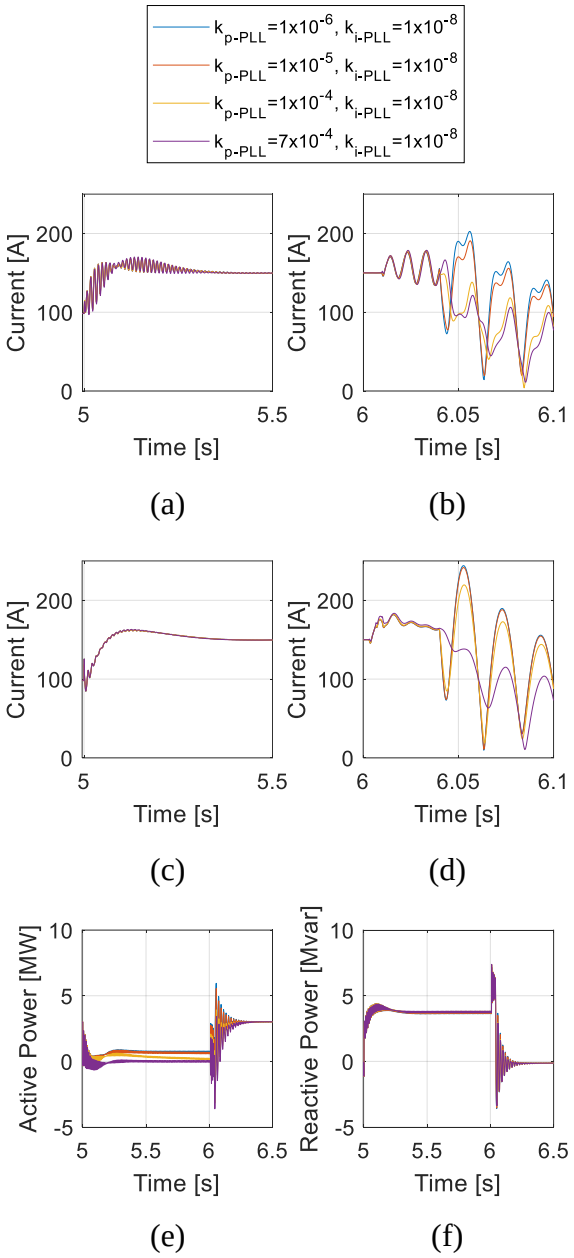


Figure 5.19. Waveforms showing the response for varying proportional gain $k_{p\text{-}PLL}$ of the PLL in strong grid condition. The waveforms are (a) current beginning during an unbalanced fault, (b) current transients during recovery after an unbalanced fault, (c) current beginning during a balanced fault, (d) current transients during recovery after a balanced fault, (e) active power during an unbalanced fault, and (f) reactive power during an unbalanced fault

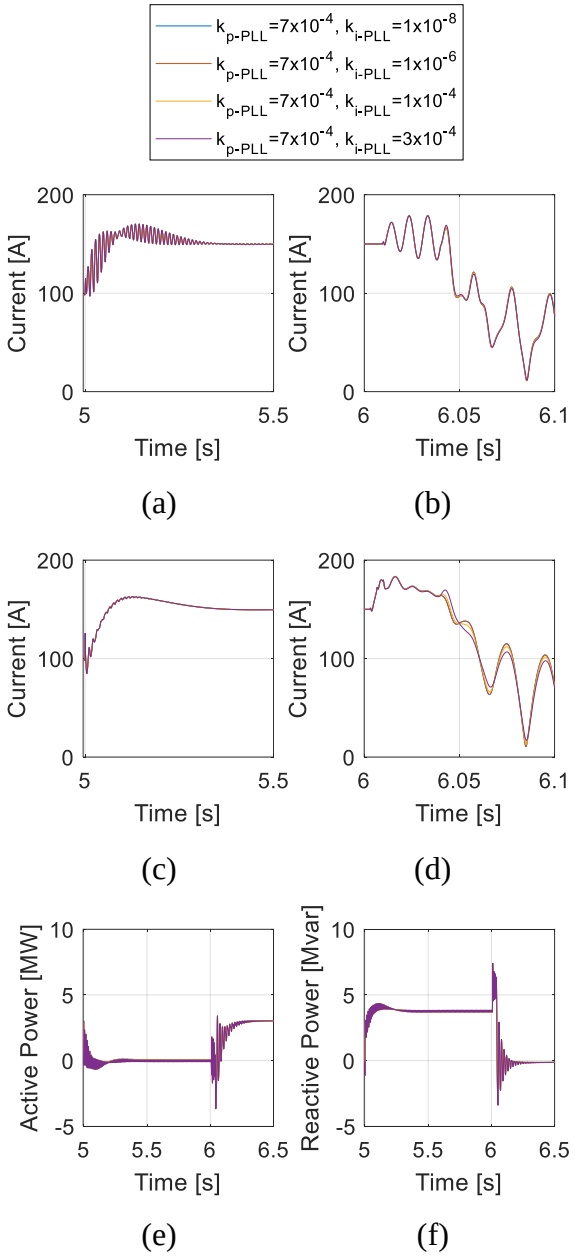


Figure 5.20. Waveforms showing the response for varying integral gain $k_{i\text{-}PLL}$ of the PLL in strong grid condition. The waveforms are (a) current beginning during an unbalanced fault, (b) current transients during recovery after an unbalanced fault, (c) current beginning during a balanced fault, (d) current transients during recovery after an balanced fault, (e) active power during an unbalanced fault, and (f) reactive power during an unbalanced fault

5.5.1.1.2Power synchronization loop

PSL is a loop that synchronizes with power. Figure 5.21(a)–(b) show the current magnitude for varying proportional gain ($k_{p\text{-}PSL}$) of the PSL during a single-phase-to-

ground fault in which the highest proportional gain had the lowest transients during fault recovery.

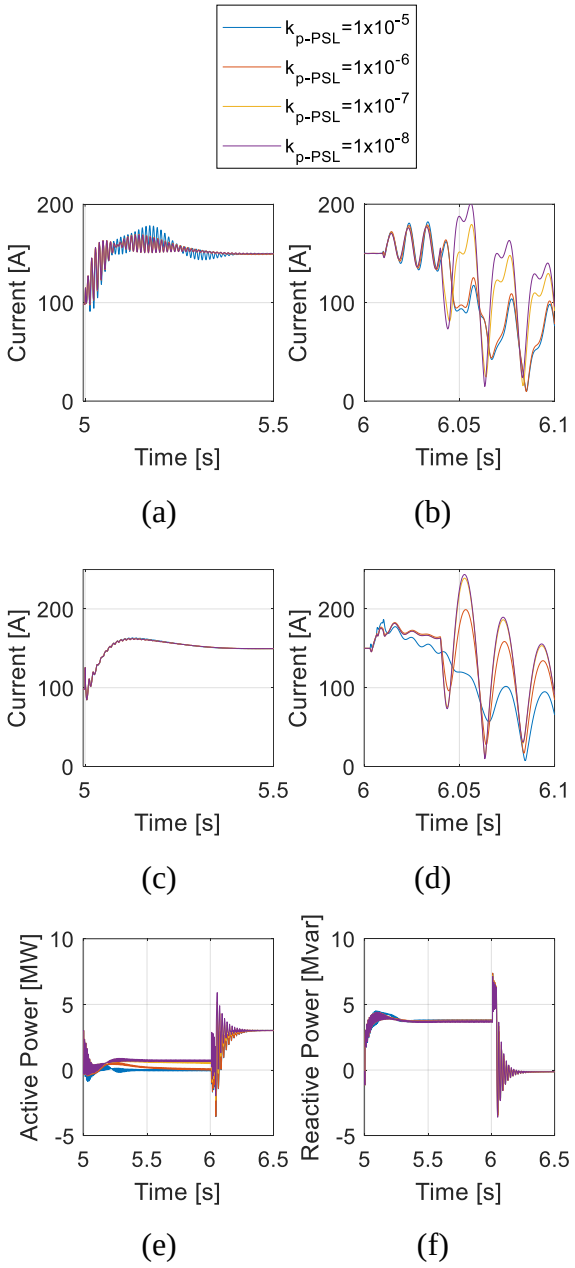
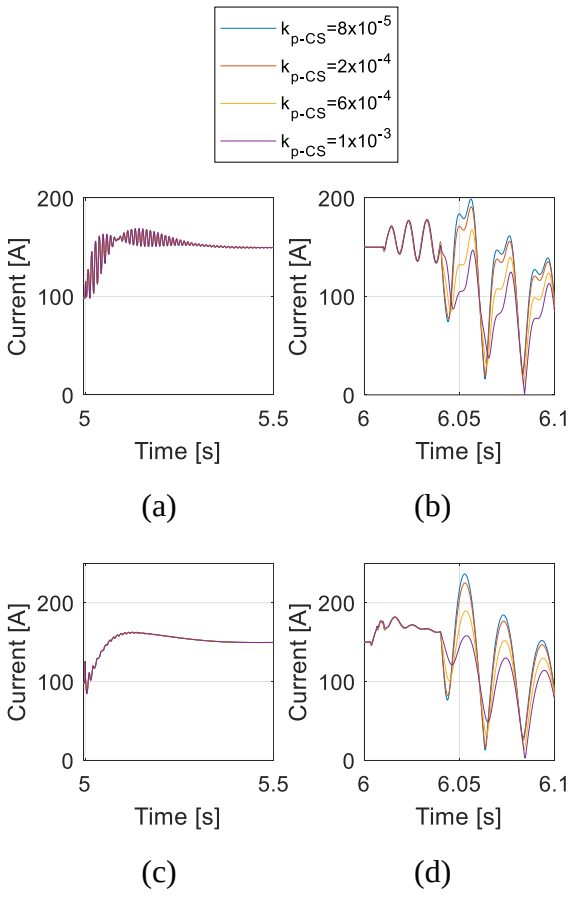


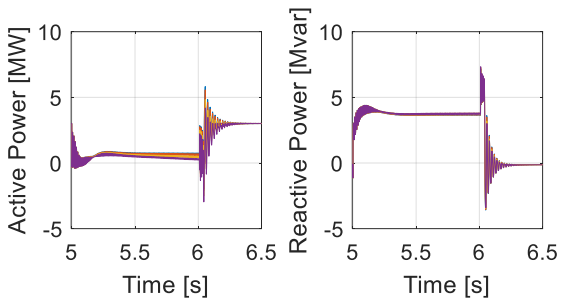
Figure 5.21. Waveforms showing the response for varying proportional gain $k_{p\text{-}PSL}$ of the PSL in strong grid condition. The waveforms are (a) current beginning during an unbalanced fault, (b) current transients during recovery after an unbalanced fault, (c) current beginning during a balanced fault, (d) current transients during recovery after a balanced fault, (e) active power during an unbalanced fault, and (f) reactive power during an unbalanced fault

Figure 5.21(c)–(d) show the current during a three-phase-to-ground fault, where the higher proportional gain had the lowest recovery transients. Figure 5.21(e)–(f) show the active and reactive power waveforms in which the highest proportional gain forced the active power to zero to align with the zero active power reference.

5.5.1.1.3 Current synchronization

CS was proposed earlier as an alternative synchronization technique, which is still under study. Parametric sweep analysis was performed to tune the CS technique. The current magnitude waveforms during a single-phase-to-ground fault for varying proportional gain ($k_{p\text{-}CS}$) is shown in Figure 5.22(a)–(b) in which the current transients increased as the proportional gain reduced. Figure 5.22(c)–(d) show the current response during a three-phase-to-ground fault, and the same observation was made as the unbalanced fault. However, the active and reactive power waveforms shown in Figure 5.22(e)–(f) revealed the highest proportional gain as all the other values had non-constant active power values.





(e) (f)

Figure 5.22. Waveforms showing the response for varying proportional gain $k_{p\text{-}CS}$ of the CS in strong grid condition. The waveforms are (a) current beginning during an unbalanced fault, (b) current transients during recovery after an unbalanced fault, (c) current beginning during a balanced fault, (d) current transients during recovery after a balanced fault, (e) active power during an unbalanced fault, and (f) reactive power during an unbalanced fault

5.5.1.2Weak grid condition

In this section, the change of the tuning in very weak grid condition (SCR =1) is analysed. The changes in the tuning performed in the strong grid condition for all the synchronisation techniques was adopted in this case study to observe the differences in the controller response in low SCR.

5.5.1.2.1 Phase-locked loop

The proportional gain $k_{p\text{-}PLL}$ of PLL was changed similar to that for high SCR case. Figure 5.23(a)–(b) show the current magnitude response during a single-phase-to-ground fault, where the highest $k_{p\text{-}PLL}$ (recommended from the high SCR case study) had oscillations in the fault current beginning and current transient after the fault clearance. The high transients in the beginning of the fault can be mitigated by retuning the notch filters of the pn sequence calculations. The fault current of a three-phase-to-ground fault is shown in Figure 5.23(c)–(d), where the highest proportional gain is also preferred. Moreover, zero active power was achieved using the highest proportional gain, as shown in Figure 5.23(e)–(f), such that the zero reference of the active current component was aligned with the active power. The waveforms shown in Figure 5.24 show no significant differences between the different parameters.

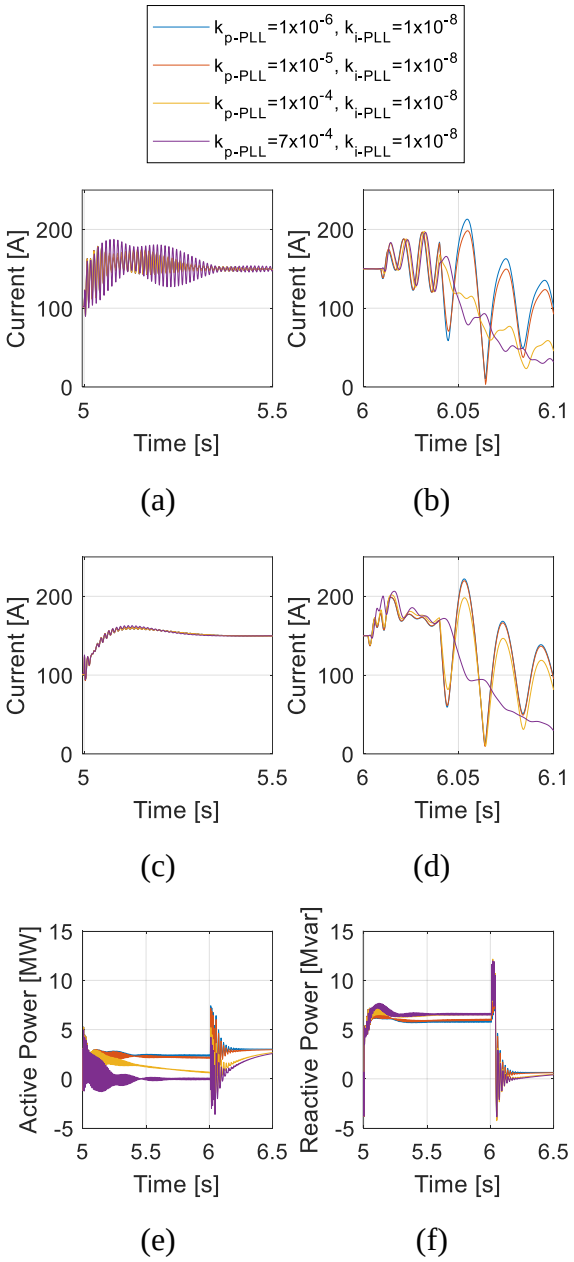


Figure 5.23. Waveforms showing the response for varying proportional gain $k_{p\text{-}PLL}$ of the PLL in weak grid condition. The waveforms are (a) current beginning during an unbalanced fault, (b) current transients during recovery after an unbalanced fault, (c) current beginning during a balanced fault, (d) current transients during recovery after a balanced fault, (e) active power during an unbalanced fault, and (f) reactive power during an unbalanced fault

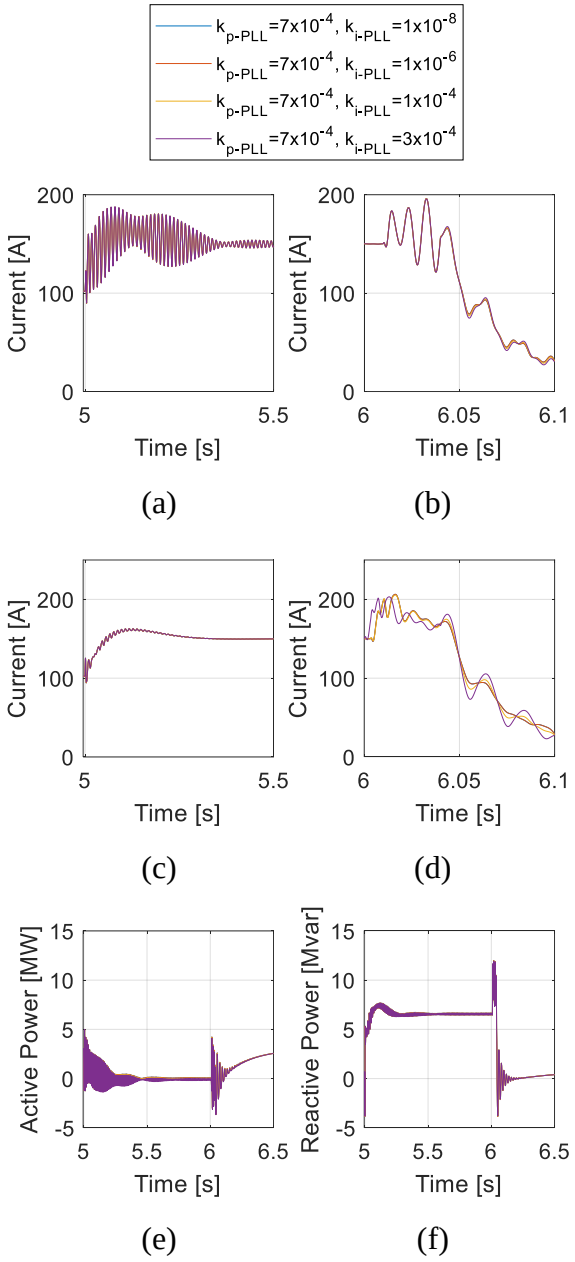


Figure 5.24. Waveforms showing the response for varying integral gain $k_{i\text{-}PLL}$ of the PLL in weak grid condition. The waveforms are (a) current beginning during an unbalanced fault, (b) current transients during recovery after an unbalanced fault, (c) current beginning during a balanced fault, (d) current transients during recovery after a balanced fault, (e) active power during an unbalanced fault, and (f) reactive power during an unbalanced fault

5.5.1.2.2Power synchronization loop

Parametric sweep analysis was applied on the PSL in the low SCR case. The current magnitude waveform during a single-phase-to-ground fault is shown in Figure

5.25(a)–(b) in which there was no best $k_{p\text{-}PSL}$ gain value as the notch filter may require further tuning.

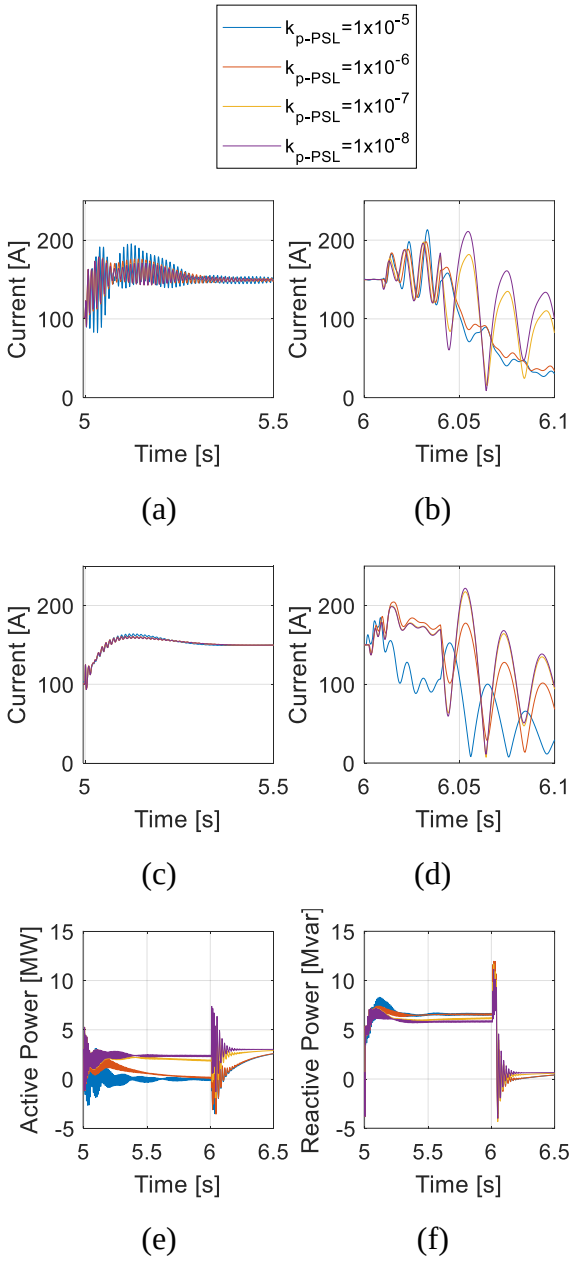
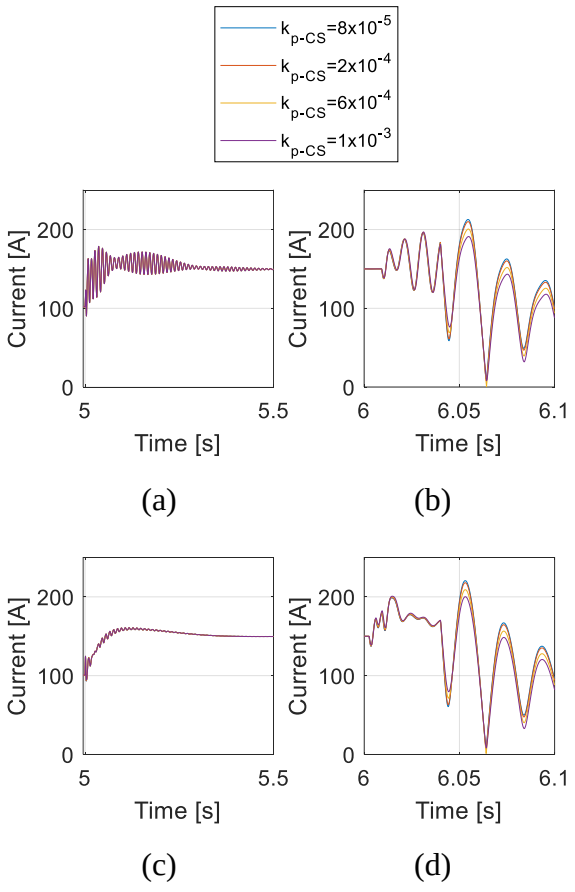


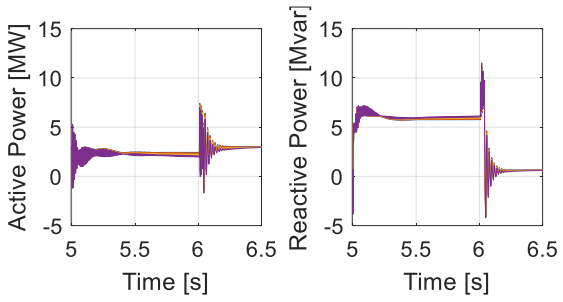
Figure 5.25. Waveforms showing the response for varying proportional gain $k_{p\text{-}PSL}$ of the PSL in weak grid condition. The waveforms are (a) current beginning during an unbalanced fault, (b) current transients during recovery after an unbalanced fault, (c) current beginning during a balanced fault, (d) current transients during recovery after a balanced fault, (e) active power during an unbalanced fault, and (f) reactive power during an unbalanced fault

However, the waveforms in Figure 5.25(c)–(d) for a three-phase-to-ground fault show that the best value is the highest proportional gain. Moreover, the highest proportional gain can achieve the desired zero active power from the active power reference, as shown in Figure 5.25(e)–(f).

5.5.1.2.3 Current synchronization

The new current magnitude synchronization technique is studied in low SCR case. Figure 5.26(a)–(b) show the current magnitude for a single-phase-to-ground fault in which the transients increased with decreasing $k_{p\text{-}CS}$ gain. The same observation was made for the three-phase-to-ground fault, as shown in Figure 5.26(c)–(d). However, based on the constant active power shown in Figure 5.26(e)–(f), the lowest control gain is suggested.





(e) (f)

Figure 5.26. Waveforms showing the response for varying proportional gain $k_{p\text{-}CS}$ of the CS in weak grid condition. The waveforms are (a) current beginning during an unbalanced fault, (b) current transients during recovery after an unbalanced fault, (c) current beginning during a balanced fault, (d) current transients during recovery after a balanced fault, (e) active power during an unbalanced fault, and (f) reactive power during an unbalanced fault

5.5.1.3 Summary

Table 5.2 presents the summary of the results of the parametric sweep analysis. The best control parameters for the synchronization techniques are high PLL proportional gain, low PLL integral gain, high PSL proportional gain, and low CS proportional gain.

Table 5.2. Summary of the parametric analysis results

	SCR	Fault steady state	Recovery transients
PLL	High	Zero active power is achieved by high proportional gain ($k_{p\text{-}PLL}$) and low integral gain ($k_{i\text{-}PLL}$)	Low transients and slow recovery are observed for high proportional gain ($k_{p\text{-}PLL}$) and low integral gain ($k_{i\text{-}PLL}$)
	Low	The same results as the high SCR case	The same results as the high SCR case
PSL	High	The highest proportional gain ($k_{p\text{-}PSL}$) has the fastest steady state time in the active power.	The highest proportional gain ($k_{p\text{-}PSL}$) shows the lowest transients and slowest recovery

	Low	The same results as the high SCR case	The same results as the high SCR case
CS	High	For a zero current reference, the lowest proportional gain ($k_{p\text{-}CS}$) shows a stable active power	The lowest proportional gain ($k_{p\text{-}CS}$) has the highest transients at the fault recovery
	Low	The same results as the high SCR case	The same results as the high SCR case

5.5.2 Comparison between synchronization techniques

The best tuning was used to compare the synchronisation techniques based on parametric sweep analysis and the same simulation conditions used in the parametric sweep analysis. The synchronization techniques considered were PLL, PSL, CS, and disabled synchronisation loop (NoSynch). The comparison study involved subjecting the power converter to single-phase-to-ground and three-phase-to-ground faults. The fault time was from 5 to 6 s. The grid condition was also varied to study the responses in strong and weak grid conditions.

5.5.2.1 Strong grid condition

The grid impedance was changed such that a converter was connected to a strong grid (SCR=5). The control structure shown in Fig. 4.1 was used but the synchronization loop of the backup controller was changed according to the desired technique in each test case. Figure 5.27(a)–(b) show the current magnitude for each synchronisation technique during a single-phase-to-ground fault, where both PLL and PSL had lower recovery transients compared to CS and NoSynch. However, the oscillations of the fault current beginning for both the PSL and PLL techniques were relatively higher. Moreover, the current transient during the three-phase-to-ground fault shown in Figure 5.27(c)–(d) were much higher for both CS and NoSynch, and no oscillations were observed. Therefore, the oscillations observed during the unbalanced fault are a factor

of the notch filters used to extract the negative sequence components, and it can be damped by fine tuning these filters.

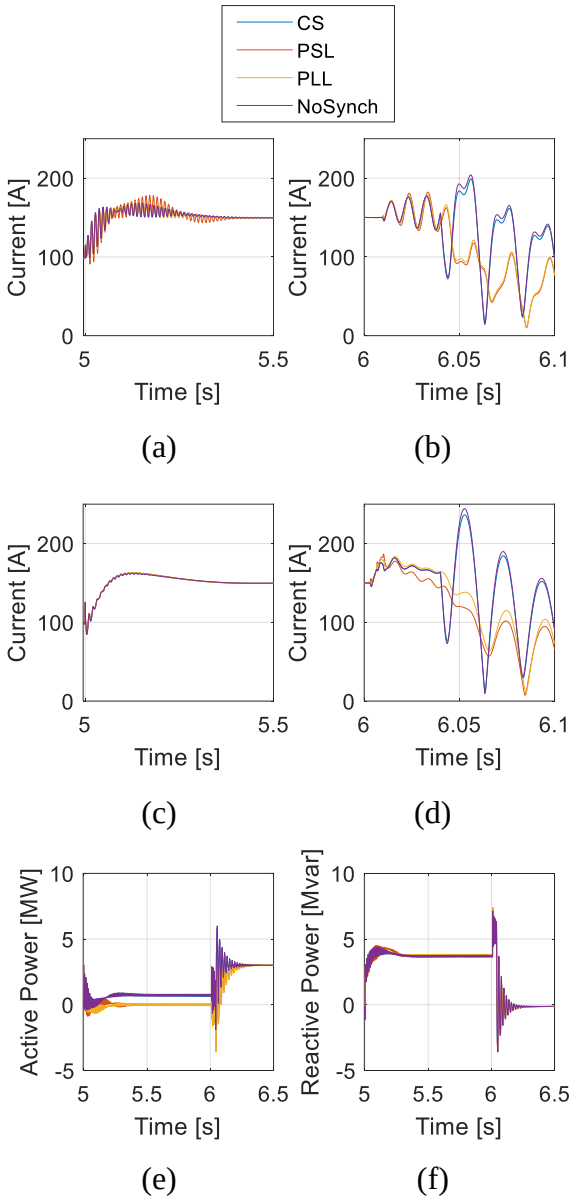


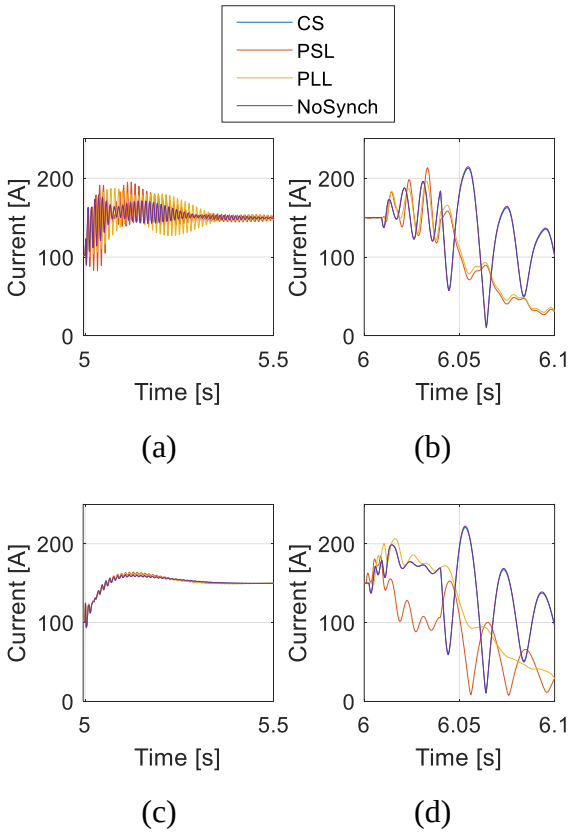
Figure 5.27. Waveforms showing the response for different synchronisation techniques in strong grid condition. The waveforms are (a) current beginning during an unbalanced fault, (b) current transients during recovery after an unbalanced fault, (c) current beginning during a balanced fault, (d) current transients during recovery after a balanced fault, (e) active power during an unbalanced fault, and (f) reactive power during an unbalanced fault

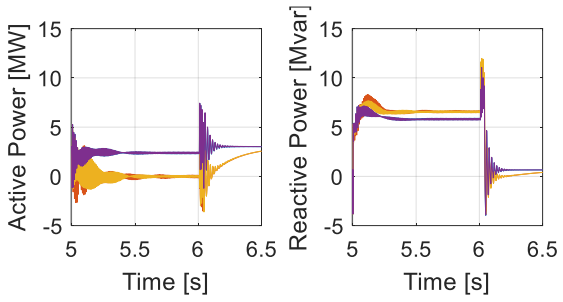
Additionally, the active and reactive power waveforms during an unbalanced fault are shown in Figure 5.27(e)–(f), which show that both PLL and PSL can inject zero active

power. This capability leaves a room for injecting a higher reactive without surpassing the maximum complex power of the converter.

5.5.2.2 Weak grid condition

The same study was conducted for a converter connected to a grid with very high impedance (SCR=1). The current magnitude waveforms during a single-phase-to-ground fault are shown in Figure 5.28(a)–(b), where PLL had the lowest recovery transients followed by PSL. However, high oscillations in current were observed at the fault beginning for both PLL and PSL. Figure 5.28(c)–(d) show the current waveforms for a three-phase-to-ground fault in which the lowest recovery transients in this case was PSL followed by PLL. Moreover, the active and reactive power waveforms shown in Figure 5.28(e)–(f) clearly show that a reduction in the active power to zero increased the reactive power injection capability.





(e) (f)

Figure 5.28. Waveforms showing the response for different synchronisation techniques in weak grid condition. The waveforms are (a) current beginning during an unbalanced fault, (b) current transients during recovery after an unbalanced fault, (c) current beginning during a balanced fault, (d) current transients during recovery after a balanced fault, (e) active power during an unbalanced fault, and (f) reactive power during an unbalanced fault

5.5.2.3Comparison in strong grid condition using a fault detection algorithm

In this section, the same comparison in strong grid condition discussed in Section 5.5.2.1 is presented; however, IFDA was adopted instead of the ideal signal generator because it influences the current transients. Fig. 4.20 shows the schematic of the IFDA. The initialisation of the simulation parameters is the same as discussed in Section 5.5.2.1. Based on the fault current resulting from a single-phase-to-ground fault shown in Figure 5.29(a)–(b), the recovery transients were reduced for all the synchronization techniques compared to the waveforms shown in Figure 5.27(a)–(b). The same transient peak reduction was observed in the balanced fault current shown in Figure 5.29(c)–(d). These results solve the high transients problem introduced before using the ideal control switching. However, zero active power injection was only achieved by using PLL and PSL, as shown in Figure 5.29(e)–(f). Hence, both PLL and PSL are more recommended for the zero active power injection capability.

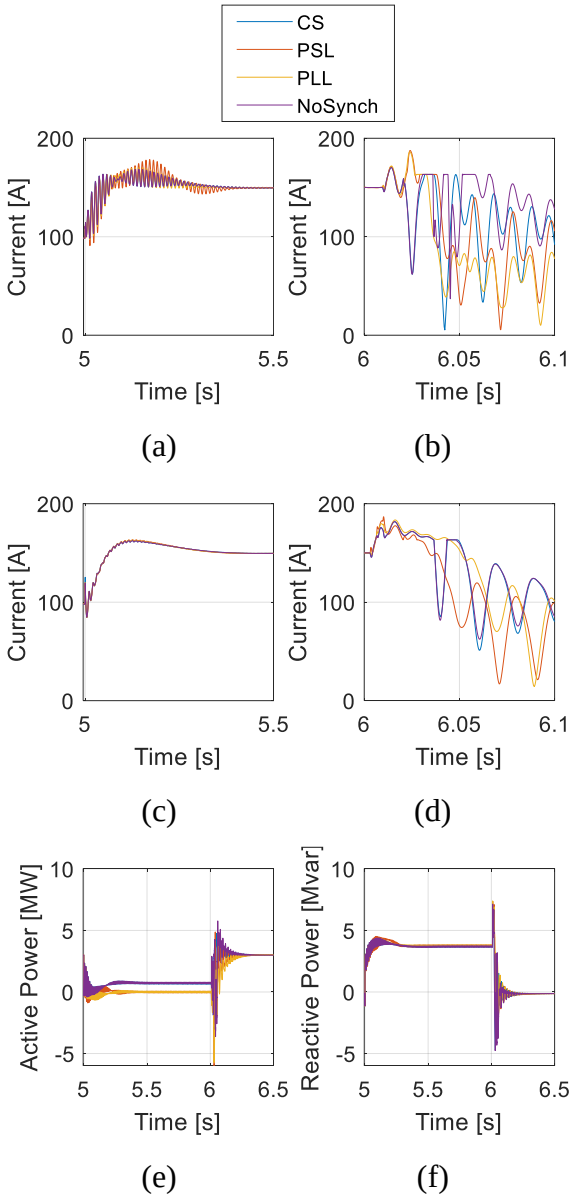


Figure 5.29. Waveforms showing the response for different synchronization techniques in strong grid condition using a fault detection algorithm. The waveforms are (a) current beginning during an unbalanced fault, (b) current transients during recovery after an unbalanced fault, (c) current beginning during a balanced fault, (d) current transients during recovery after a balanced fault, (e) active power during an unbalanced fault, and (f) reactive power during an unbalanced fault

5.5.2.4 Comparison summary

Based on the comparison of the synchronization techniques, both PLL and PSL can maintain the independent control during fault. However, CS and NoSynch cannot control the active and reactive power independently, which requires extra loops.

According to the study, PLL and PSL techniques are recommended because they have slow current recovery after fault, leading to lower current transients after the fault. Meanwhile, CS and NoSynch have fast recovery after fault; however, extra reserve current capacity is required to keep the converter safe during the transients. Table 5.3 presents the summary of the analysis results.

Table 5.3. Summary of the comparison between the synchronization techniques

	Steady state	Transients
PLL	Can inject zero active power and therefore a higher reactive power for the same current	High oscillations at the beginning but slow recovery with low transients
PSL	Can inject zero active power and therefore higher reactive power for the same current	Oscillations are lower than PLL in the beginning but slow recovery with low transients
CS	Cannot control active power to zero	Low oscillations in the beginning compared to the first two techniques but fast recovery leading to high transients. The recovery transients are reduced using the IFDA.
NoSynch	Cannot control active power to zero	Low oscillations in the beginning same as the CS but fast recovery leading to high transients. The recovery transients are reduced using the IFDA.

5.6 Chapter summary

In this chapter, a new synchronization technique called current synchronization technique was introduced. Furthermore, large signal stability was introduced to investigate the stability of several synchronisation techniques such as PLL, APL, PSL, and CS. The stability analysis showed that APL loses stability by decreasing the voltage, which aligns with the analysis for the VSM FRT capability discussed in Chapter 3. The other techniques can maintain stability; therefore, a further study was applied using a set of time-domain simulations.

Subsequently, parametric sweep analysis was performed for these synchronization techniques in strong and weak grid conditions. The analysis showed the best tuning for each technique required for comparison.

Further, the synchronization techniques were compared to obtain the best technique/s for the dual VSM structure. The results showed that PLL and PSL can provide better responses because they had low transients during switching between controllers and injected zero active power during an unbalanced fault.

Finally, FDA was adopted in the comparison rather than the ideal signal, which showed that the current transient can be easily mitigated. Therefore, CS or NoSynch can be used in cases where independent active and reactive power injections are not considered.

Chapter 6

Conclusions

6.1 Conclusions

The focus of this thesis was on the FRT of a VSM structure. Chapter 1 began by introducing changes worldwide in electrical grids. In Chapter 2, power converter structures were reviewed, and the control structures presented in the literature were introduced. The control structures were categorised into grid-following and grid-forming modes. Subsequently, as a recommendation for future electrical grids, several grid-forming controller implementations were reviewed, which were subcategorised into several control structures while focusing on the VSM control structures. The VSM control structures were classified into several implementations according to the degree of SM emulation, and the two main categories were high-order and simplified-order models.

Furthermore, a review on the FRT in the literature regarding the VSM was introduced. The FRT review indicates that for a VSM structure with an inner current loop, the current can be limited by saturating the current references using adaptive virtual admittance or switching the outer loops. However, for a VSM without a current controller, alternative control loops with a current controller are required to maintain the controllability of the current during faults.

In Chapter 3, the basic VSM control structure was analysed, and its response during faults was investigated. A current-limiting technique was then introduced to limit the current in the normal condition. Subsequently, several FRT strategies were proposed to deal with the limitations of VSM and improve the control structure during balanced faults.

In Chapter 4, a conventional solution for injecting maximum reactive current was studied to show the possible limitations. These limitations appeared after subjecting the converter to an unbalanced fault in weak grid condition. The failure of the control structure was caused by a failure in the FDA conditions used to switch between the controllers. The main problem was that the grid impedance increased under the weak grid condition; hence, the converter was required to apply more voltage to inject the required current. During the unbalanced fault, the healthy phases created high voltage magnitude such that the FDA output failed to identify the fault.

Therefore, an improvement to the FDA was required to mitigate the high voltage problem. The new conditions considered the negative sequence voltage, and the overall voltage decreased below the minimum acceptable voltage. These conditions helped the full control structure to operate in weak grid conditions. Moreover, an active and reactive power loop was added to the current controller to limit the reactive power injection below the converter capability.

Moreover, the full structure was subjected to fault distance sensitivity analysis to investigate the voltage and current waveforms during different types of faults and grid conditions. The analysis showed that the structure can maintain the current below the maximum in all the test cases, which proves the reliability of the proposed control structure.

In addition, parametric sensitivity analysis was conducted to investigate the effect of the tuning of multiple controller parameters on the current response of the converter. The analysis was conducted in strong and weak grid conditions, and recommendations for the best tuning were provided as a reference for such a control structure.

Furthermore, another improved implementation that can be used for weaker grid conditions was introduced. This implementation targets the FDA conditions, which uses three conditions instead of two to provide a more flexible algorithm. The proposed structure and normal grid-following converter were then compared, which showed that the current responses of both structures were almost the same and the proposed control structure could replace the grid-following converter.

In Chapter 5, the effect of the synchronization loop in the backup controller was studied, and synchronization alternatives were introduced, including a new synchronisation technique under development. The synchronization techniques were PLL, PSL, CS, and NoSynch. These techniques were studied using phase portrait method and multiple simulations. The simulations involved subjecting the converter to balanced and unbalanced faults in strong and weak grid conditions to reveal the current, active and reactive power, and synchronization loop output waveforms. First, parametric sweep analysis was used to tune each technique to the best performance. Then, the techniques were compared, and the advantages and disadvantages of each synchronisation technique were highlighted.

Finally, the output of the comparison showed that PLL and PSL can provide the lowest transients during transition between both controllers, which was a result of the slow recovery after fault clearance. Moreover, zero active power was achieved using these synchronization techniques, which leads to the increase in the reactive power injection without outer loops. This will help building an independent active and reactive power control. However, CS and NoSynch had faster recovery, which leads to higher transients. Moreover, these techniques cannot provide zero active power injection; thus, they require extra loops for active and reactive power control.

The thesis conclusion is that a grid forming converter without a current controller must have an alternative control structure during fault, which is based on a CC structure that is capable of controlling and limiting a fault current. Moreover, a pn CC is more complying to the grid code, so that the controller is able control the negative sequence in case of unbalanced faults. Also, the FDA is very crucial for reliable and stable controller, therefore it was thoroughly discussed and improved to satisfy different operating conditions. The synchronization in the alternative control structure can be a PLL or a PSL based on the study, so that both synchronizations have better performance over the other techniques studied.

6.2 Future work

The following points are recommended as future work:

- Studying and analysing the synchronization techniques based on the current signal
- Further analysing the new IFDA to determine the reliability of this structure.
- Developing a new transient analysis to support the simulation results.
- Investigating multi-infeed converter scenarios to study the converter-converter interactions operating with dual VSM structures limitation of the interactions.
- Using real-time simulator to support the simulations' findings and reveal new challenges that need to be addressed.

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Appendix A

Alternative VSM FRT strategies

A.1 First FRT Strategy

This strategy aims to limit the current through grid voltage sag, which is based on applying the same voltage that appears at the converter PCC. In this way the current flow in the coupling reactor is close to zero.

This is done by changing the voltage loop to feedforward the voltage measured during the fault. The references of both control loops are changed. The power controller reference is set to zero to limit the active power. The voltage loop reference is changed to the voltage feedback signal, preventing the voltage controller integrator from increasing during the fault. The control structure is shown in Figure A.1.

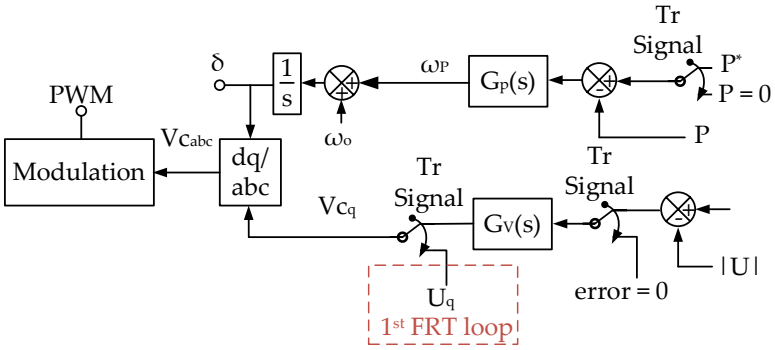

Figure A.1. Schematic of the first FRT strategy controller

Several simulations are adopted to verify the FRT action of the proposed controller, during three-phase faults. The test case includes different voltage sags, and different short circuit ratios (SCR). The following list shows the sequence of voltage sags for each SCR:

1. 100% voltage sag (Three phase to ground fault) starting at t=5 sec. to t=10 sec.

2. 80% voltage sag starting at t=15 sec. to t=20 sec.

The voltage dips duration is not a standard grid code requirement, but it was chosen to test the control action for a couple of seconds. Each case is studied for different SCR keeping constant the control parameters. This is done to validate the control structure for several grid conditions. The cases are discussed as follows:

A.1.1.1First scenario: 100% voltage sag

The purpose of the first scenario is to show the control performance in weak grids. The control structure is shown in Figure A.1. The waveforms shown in Figure A.2 are display the active and reactive powers and the current during a 100% voltage sag. Each row represents different SCRs, and the first column is for active (blue line) and reactive (orange line) power waveforms, then the second column is for the initial current transients, and the third one for the final transients of the currents. The currents for all SCRs are almost zero, but the final transients increase by increasing the SCR. The transients in the active and reactive powers are very high.

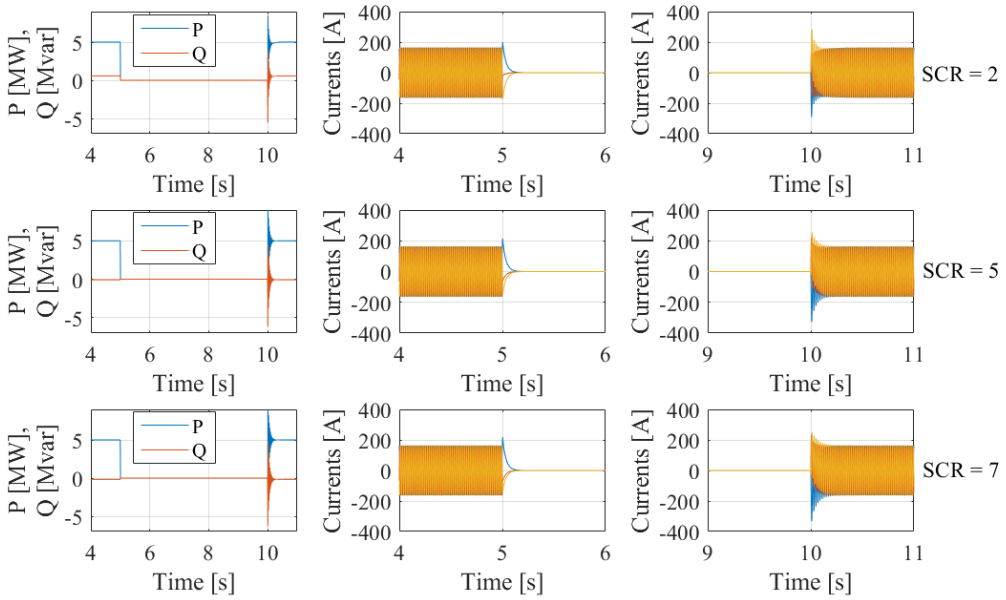

Figure A.2. The voltages and currents for 100% voltage sag for SCR = (2,5,7) for the first switching action controller

A.1.1.2Second scenario: 80% voltage sag

The second scenario is to verify the previous controller on 80% voltage sag. The active, reactive powers and currents waveforms are shown in Figure A.3. The figure is divided as in the same way as the first scenario. The currents are limited to a low value, which makes the controller safe during this type of fault. However, it can be seen that by increasing the SCR, the initial current transients decrease. The active and reactive powers transients are decreased compared to the 100% voltage sag.

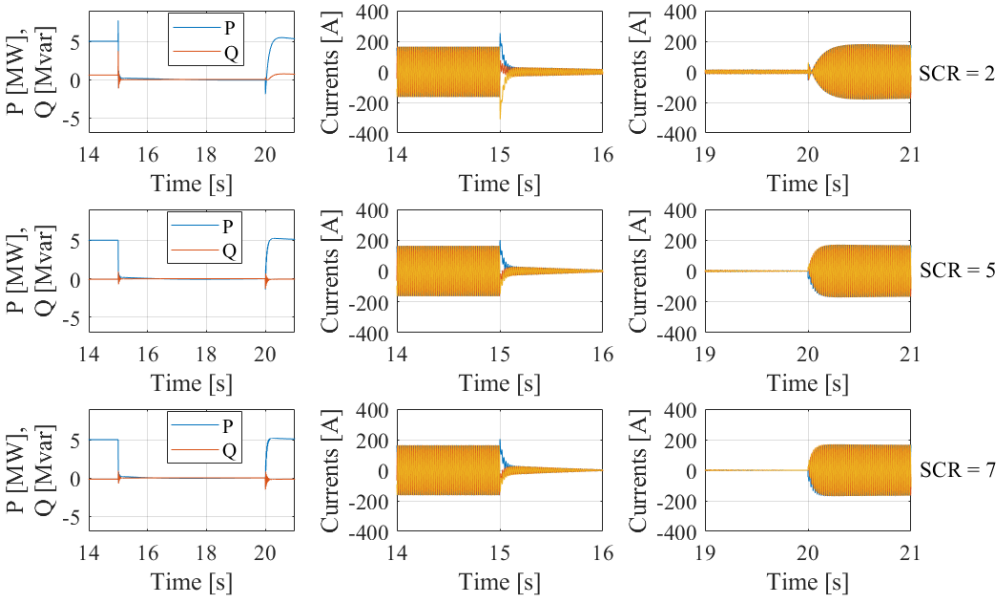

Figure A.3. The voltages and currents for 80% voltage sag for SCR = (2,5,7) for the first switching action controller

A.2 Second FRT Strategy

The second strategy aims to limit and inject a controlled current through grid voltage sag as shown in Figure A.4, which allows the converter to provide reactive power during the fault. This is done by adding a voltage component, V_{FRT} to the voltage feedback. V_{FRT} can be calculated a:

$$V_{FRT} = I_{inj}Z \qquad \text{(A.1)}$$

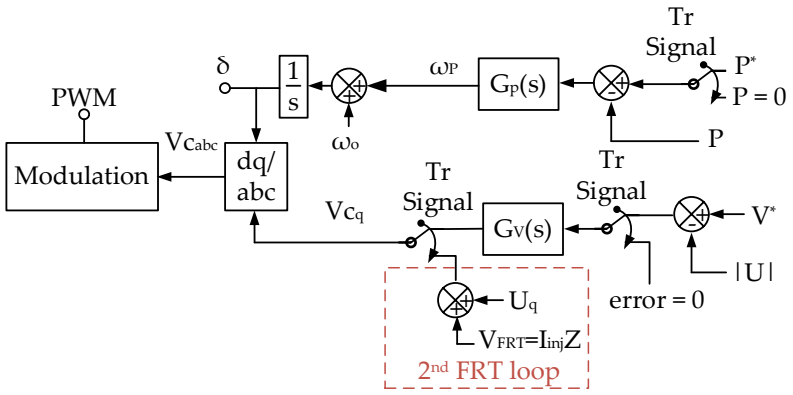

Figure A.4. Schematic of the second FRT strategy controller

Where I_{inj} is the value of the desired current magnitude needed to be injected during the fault, and Z is the impedance between the converter and the PCC.

The simulation scenarios are repeated to validate the modified controller.

A.2.1.1First scenario: 100% Voltage Sag

The active, reactive powers and currents for 100% voltage sag are shown in Figure A.5. The controller provides a current during the fault. The final current transients are slightly increased by increasing the SCR. The transients in the active and reactive powers are much decreased compared to the first FRT strategy.

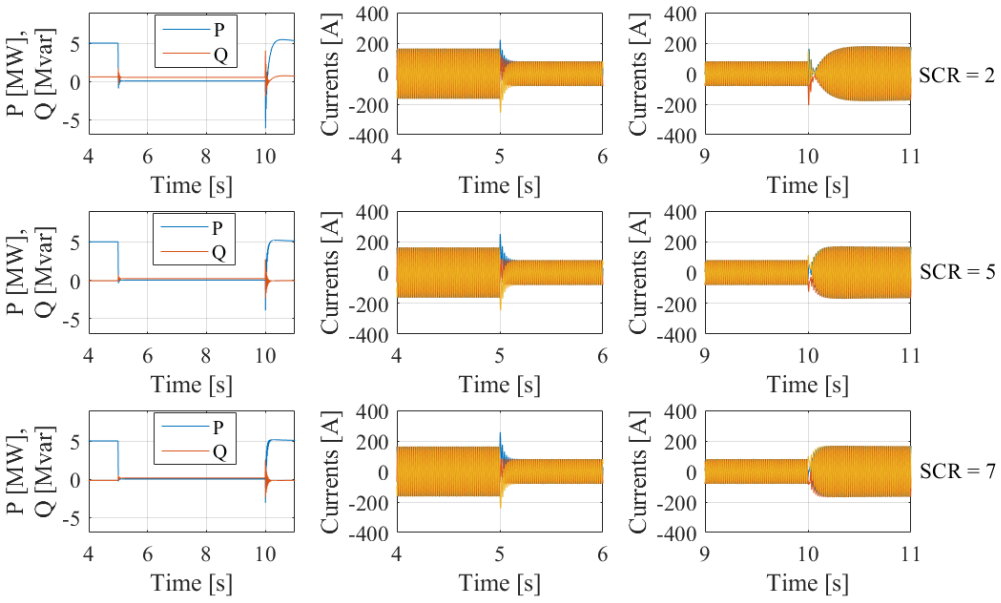

Figure A.5. The voltages and currents for 100% voltage sag for SCR = (2,5,7) for the second switching action controller

A.2.1.2Second scenario: 80% voltage Sag

The second scenario is to test the same structure at 80% voltage sag. The active, reactive powers and current waveforms are shown in Figure A.6. The controller is still able to provide some current during the fault. The behaviour of the controller to both voltage sags is almost the same.

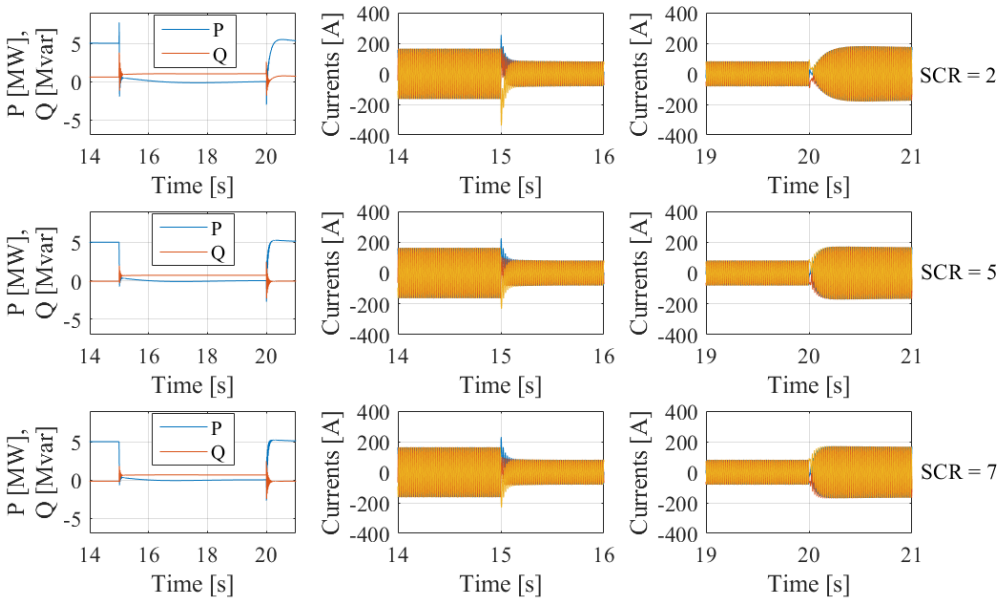

Figure A.6. The voltages and currents for 80% voltage sag for SCR = (2,5,7) for the second switching action controller

A.3 Third FRT strategy

The third strategy aims to inject current during the fault, unlike the third Strategy that aims to limit the current only. The current injection is based on the same concept introduced in the second FRT strategy, which add the voltage V_{FRT} to the voltage. Since, the control structure

uses both voltage components, therefore this schematic shows the sensitivity of injecting current through U_q component. The schematic of the control structure is shown in Figure A.7.

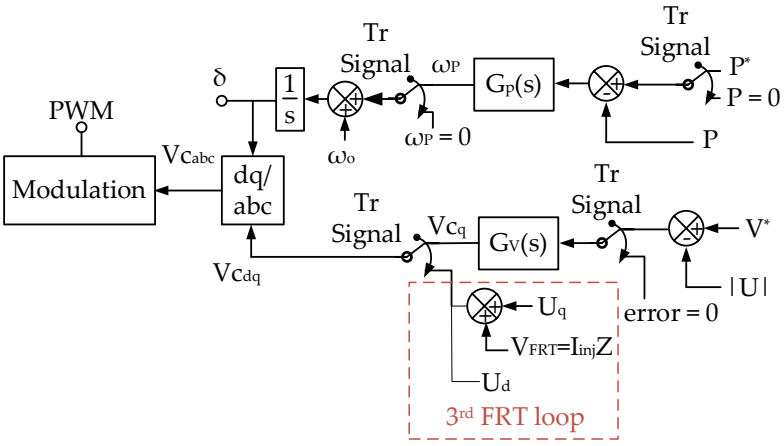

Figure A.7. Schematic of the third FRT strategy controller

The same simulations were applied on the third FRT strategy, and the voltage, the current, the active, and reactive power were recorded. For a single phase to ground fault the voltage and current injected are unbalanced, which leads to an unexpected current peak and high transients as shown in Figure A.8. For the same case, the active power is almost zero while the reactive power is almost 1.5 Mvar as shown in Figure A.9.

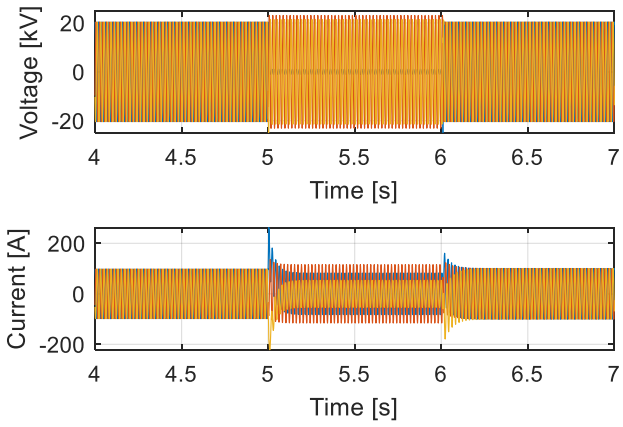

Figure A.8. Voltage and current waveforms of the third FRT strategy in a single phase to ground fault

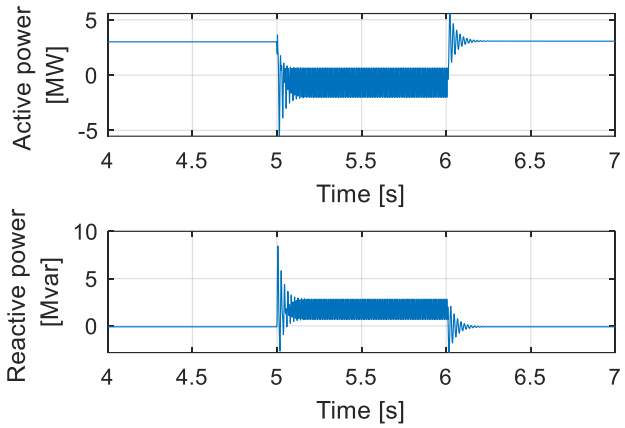

Figure A.9. Active and reactive power waveforms of the third FRT strategy in a single phase to ground fault

The voltage and current waveforms in a three phase to ground fault are shown in Figure A.10, at which the current injected during the fault is almost the same as in normal condition. However, high current transients are observed in the first and last fault periods. The active power value during fault is zero and the reactive power value is low as shown in Figure A.11.

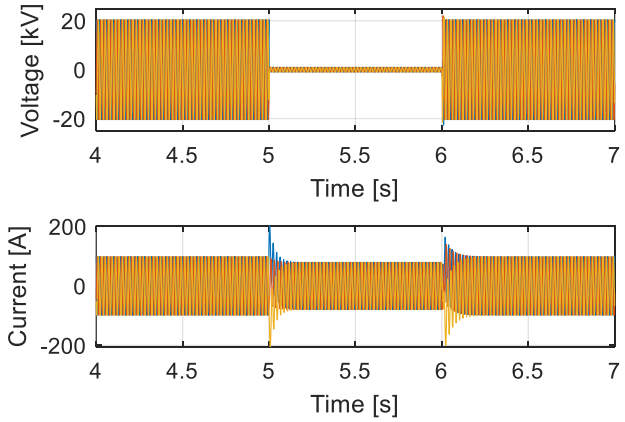

Figure A.10. Voltage and current waveforms of the third FRT strategy in a three phase to ground fault

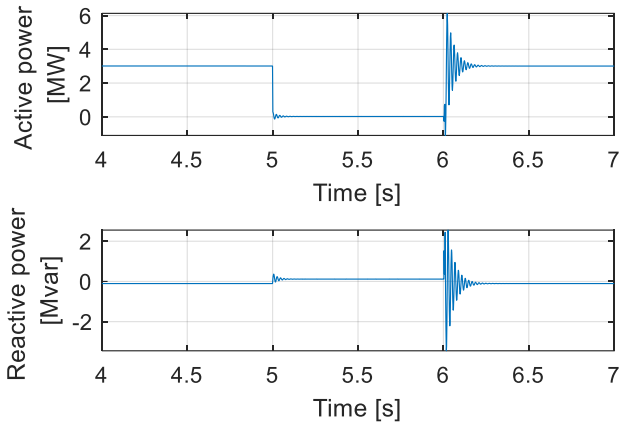

Figure A.11. Active and reactive power waveforms of the third FRT strategy in a three phase to ground fault

A.4 Fourth FRT strategy

The fourth strategy aims to discuss the sensitivity of injecting current through the U_d component as shown in Figure A.12.

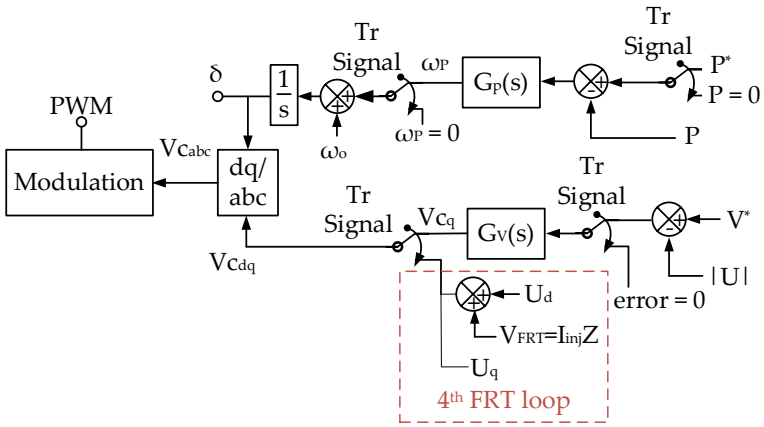

Figure A.12. Schematic of the fourth FRT strategy controller

The same simulation scenarios were applied on the fourth case, so that the difference between injecting the voltage through the d and the q component is detected. In the single phase to ground fault, the current injected during is higher than the three FRT strategy as shown in Figure A.13. Moreover, a negative active power is detected as shown in Figure A.14.

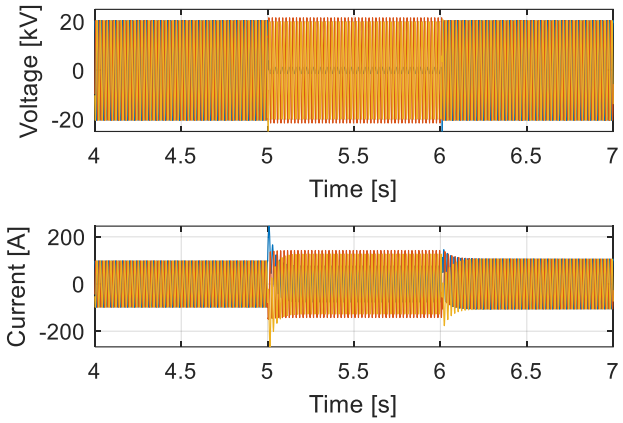

Figure A.13. Voltage and current waveforms of the fourth FRT strategy in a single phase to ground fault

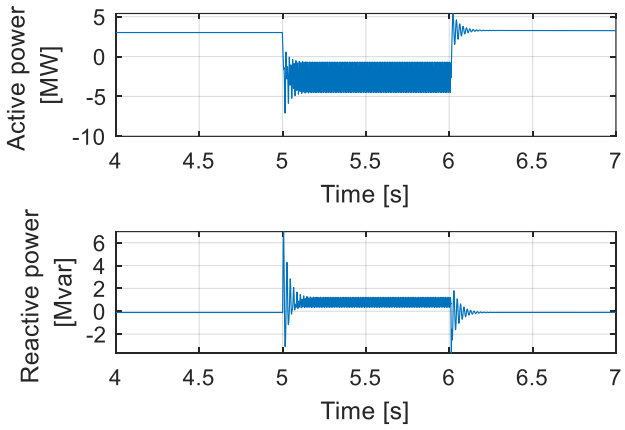

Figure A.14. Active and reactive power waveforms of the fourth FRT strategy in a single phase to ground fault

A simulation for a three phase to ground fault is shown in Figure A.15 and Figure A.16, at which the transients in the current are higher than the fourth FRT strategy. These simulations show that the reactive power is affected by changing the voltage q component, while changing the d component affects the active power. Therefore a proper synchronization is required during the fault, and a positive and current controller is required for accurate current control.

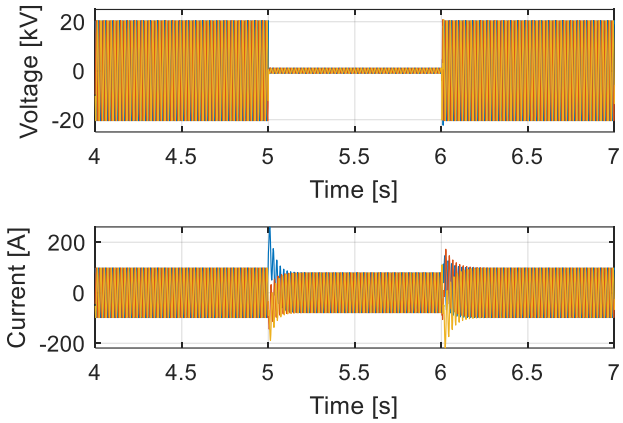

Figure A.15. Voltage and current waveforms of the fourth FRT strategy in a three phase to ground fault

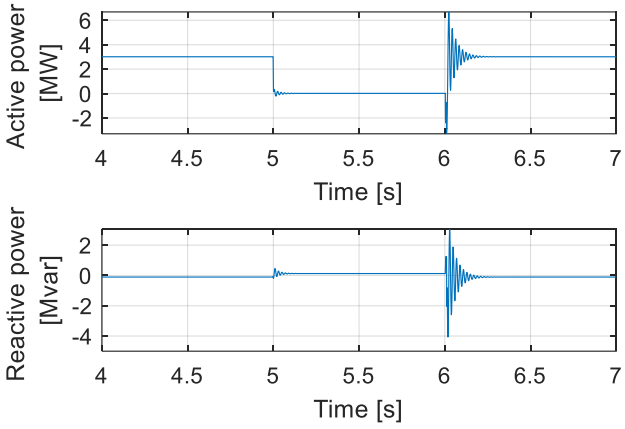

Figure A.16. Active and reactive waveforms of the fourth FRT strategy in a three phase to ground fault